

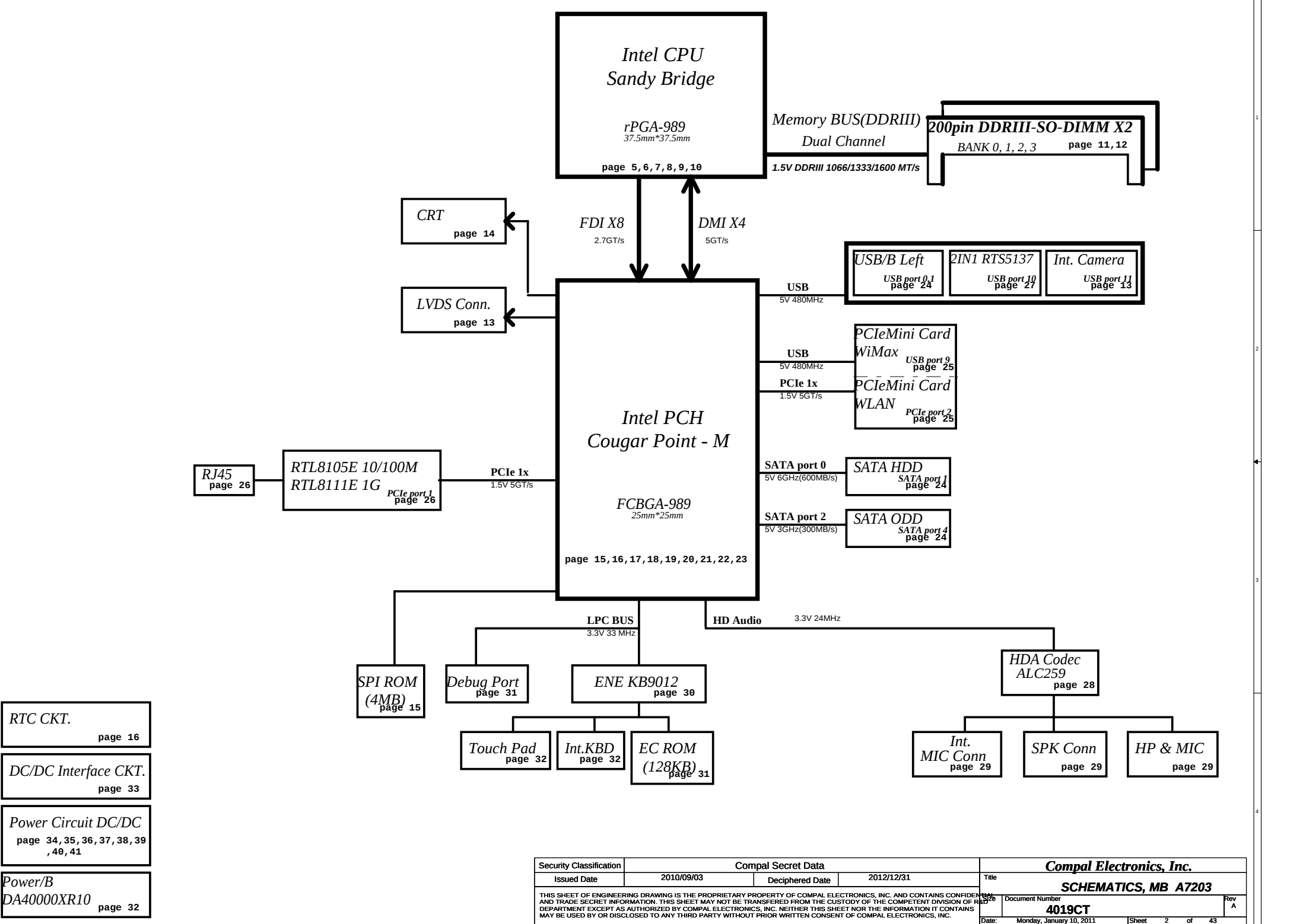
PWWHA

TaiDi1 Plus

LA-7203P REV 0.1 Schematic

Intel Processor(Sandy Bridge) / PCH(Cougar Point)
2010-12-27 Rev 0.1

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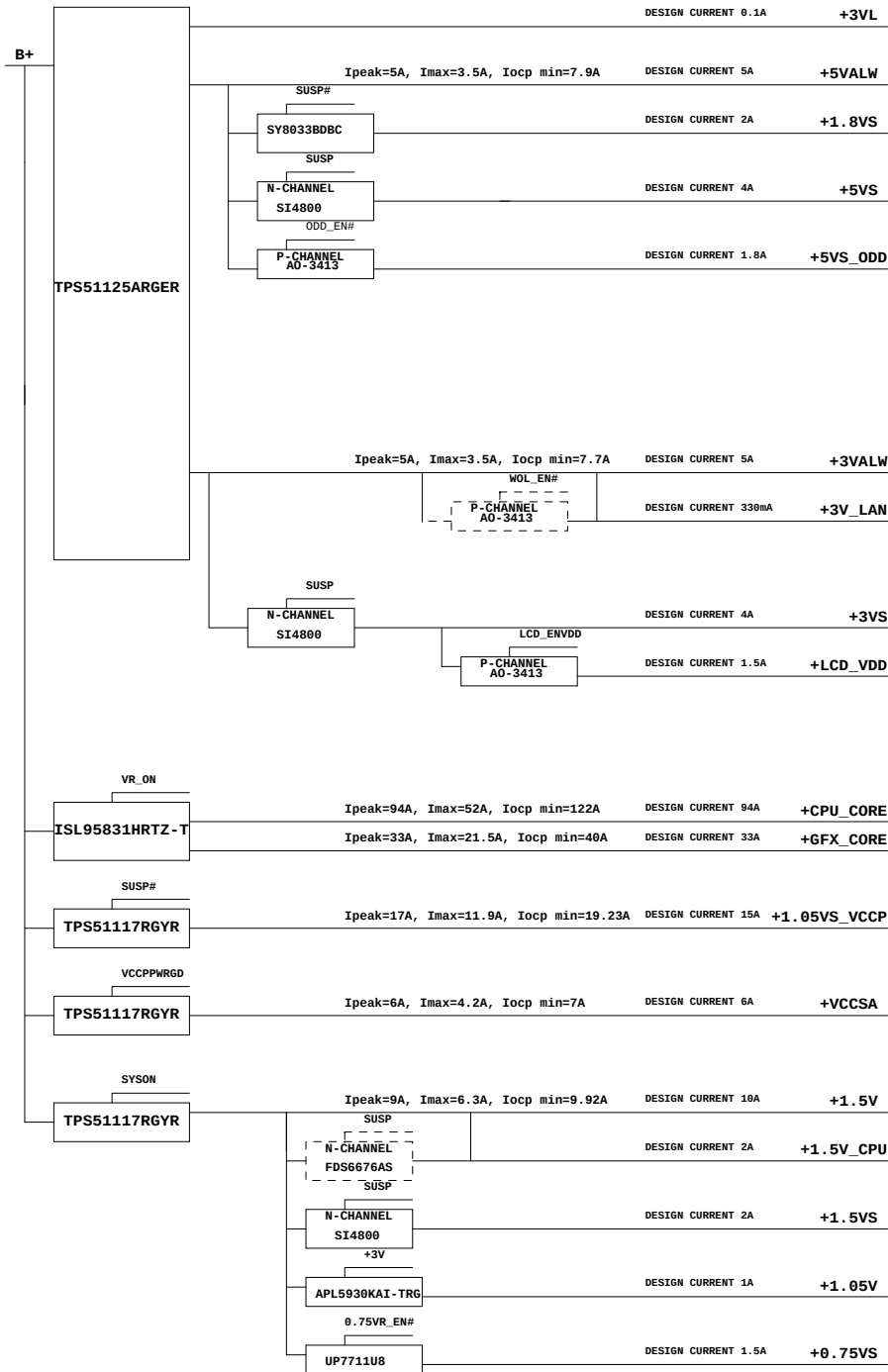
RTC CKT.
page 16

DC/DC Interface CKT.
page 33

Power Circuit DC/DC
page 34, 35, 36, 37, 38, 39, 40, 41

Power/B
DA40000XR10
page 32

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Voltage Rails (0 MEANS ON X MEANS OFF)

power plane State	+RTCVCC	B+	+3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.05VS +0.75VS +CPU_CORE +GFX_CORE
S0	0	0	0	0	0	0
S1	0	0	0	0	0	0
S3	0	0	0	0	0	X
S5 S4/AC	0	0	0	0	X	X
S5 S4/ Battery only	0	0	0	X	X	X
S5 S4/AC & Battery don't exist	0	X	X	X	X	X

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	Clock Generator	D2 H	1101 0010 b
+3VS	WLAN/WIMAX		

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b

EC SM Bus2 Address

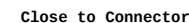
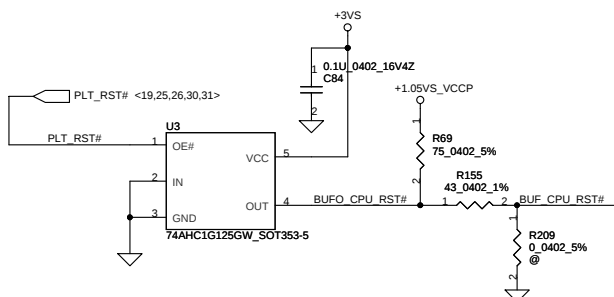
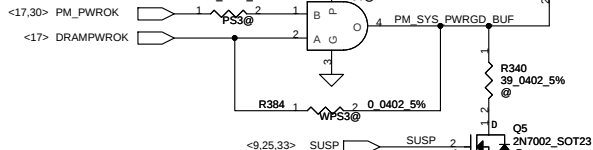
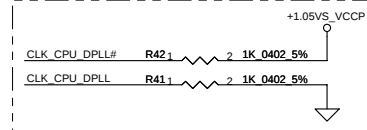
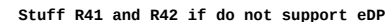
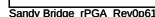
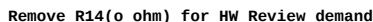
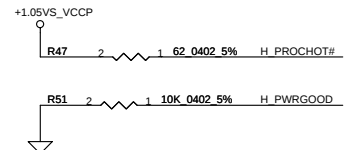
Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b

BTO Option Table

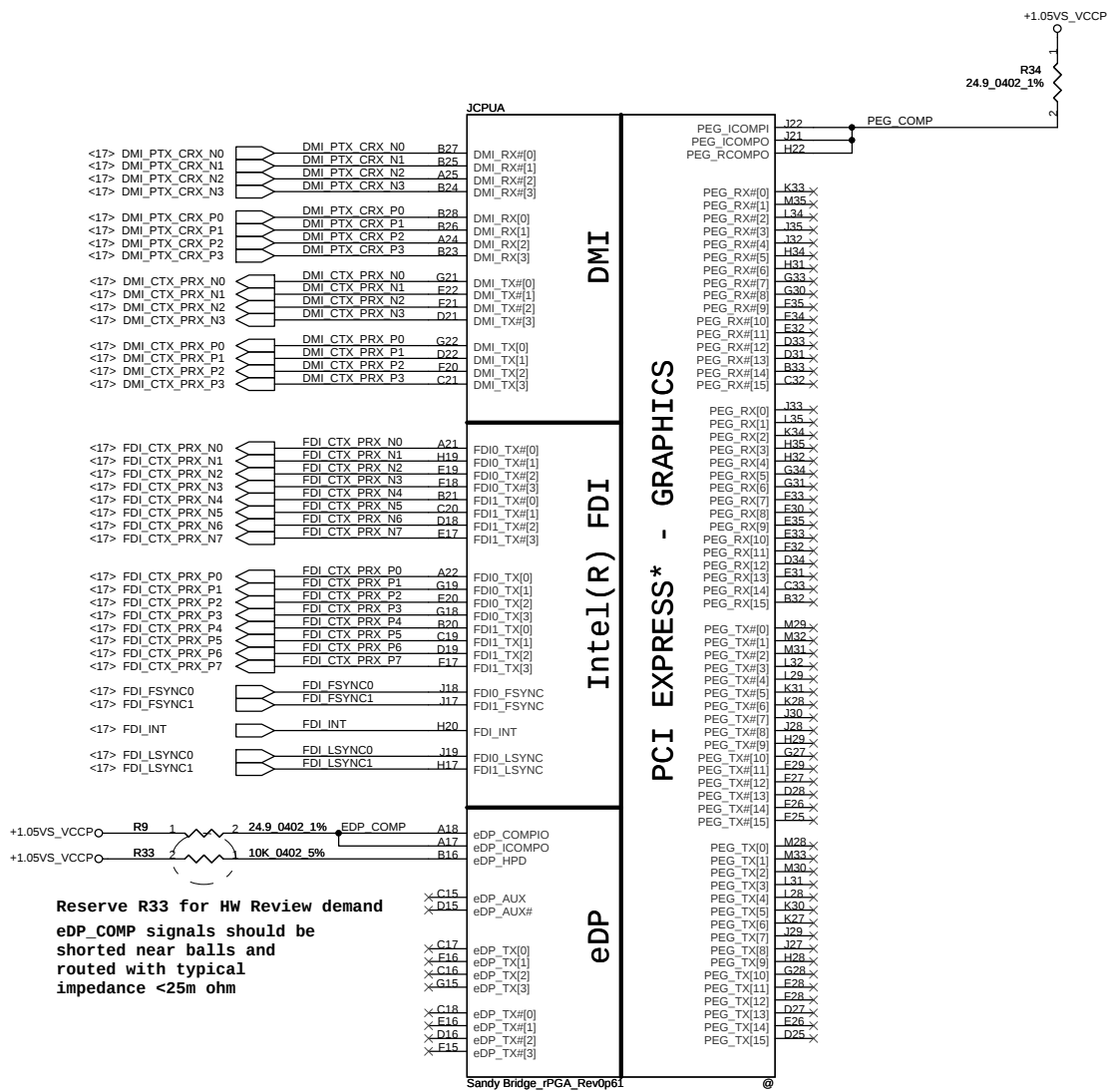
Function	MINI PCI-E SLOT	LAN		Camera & Mic		
description	SLOT1	LAN		Camera & Mic		
explain	WIMAX	10/100M	Giga	Camera & Mic		
BTO	WIMAX@	8105E@	8111E@	CAM@		

SIGNAL STATE	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1(Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

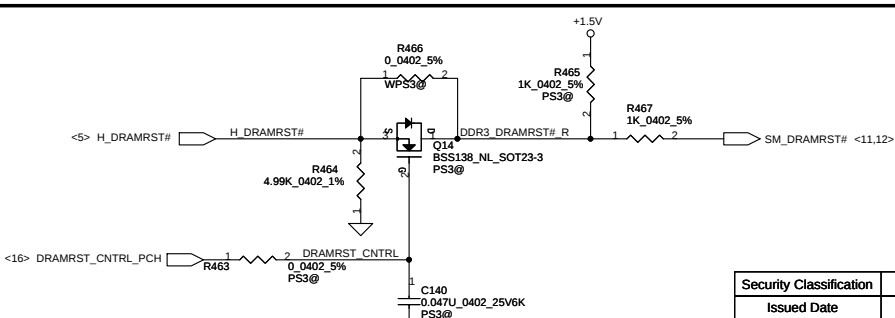
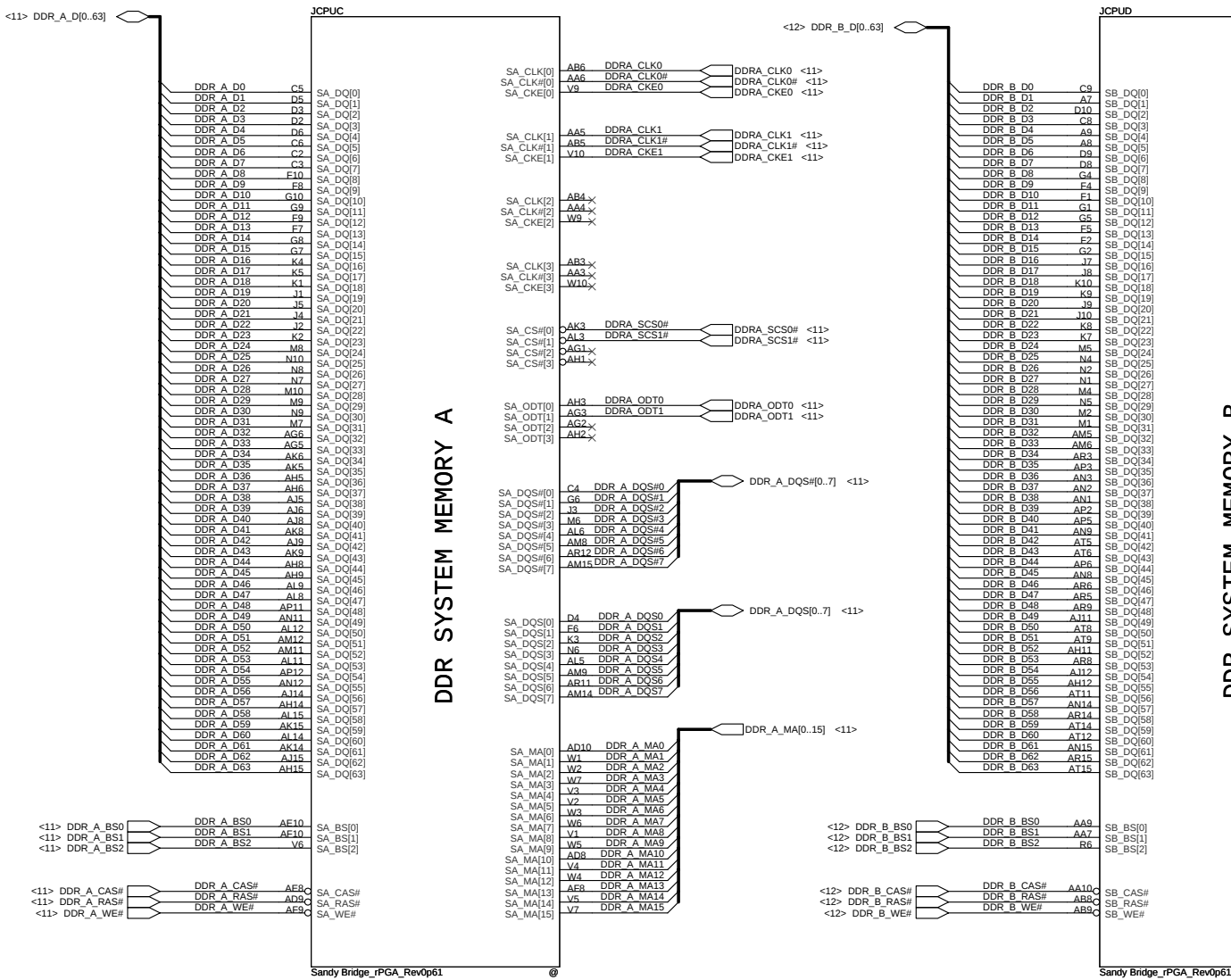
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+CPU_CORE

POWER

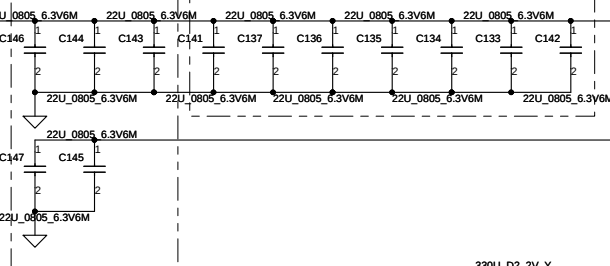
JCPUF

94A (Quad Core 45W)
53A (SV 35W)

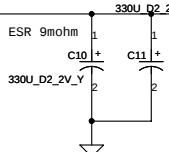
8.5A

+1.05VS_VCCP Decoupling:
2X 330U (6m ohm), 12X 22U

TOP Socket Cavity x 7

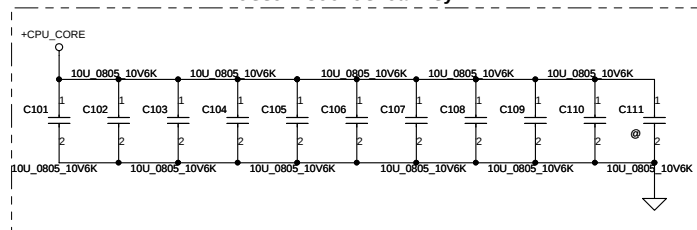


Bottom Socket Cavity x 5

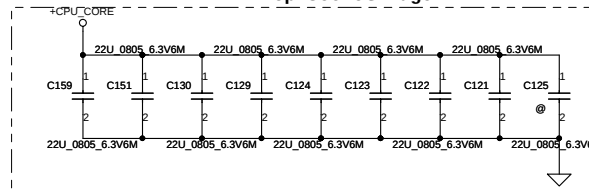


+CPU_CORE Decoupling:
4X 470U (4m ohm), 16X 22U, 10X 10U

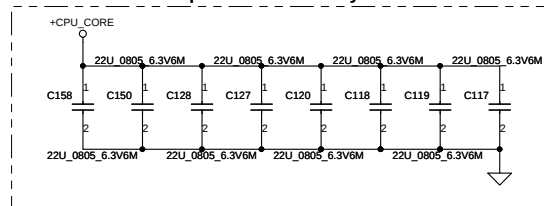
Bottom Socket Cavity



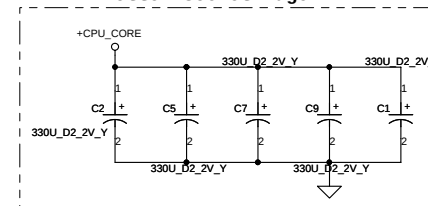
Top Socket Edge



Top Socket Cavity



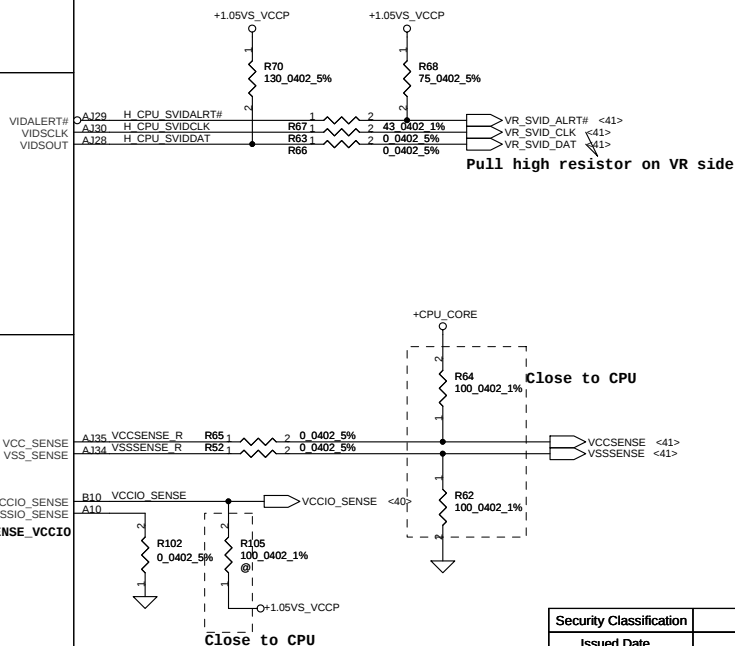
Bottom Socket Edge



PEG AND DDR

SVID

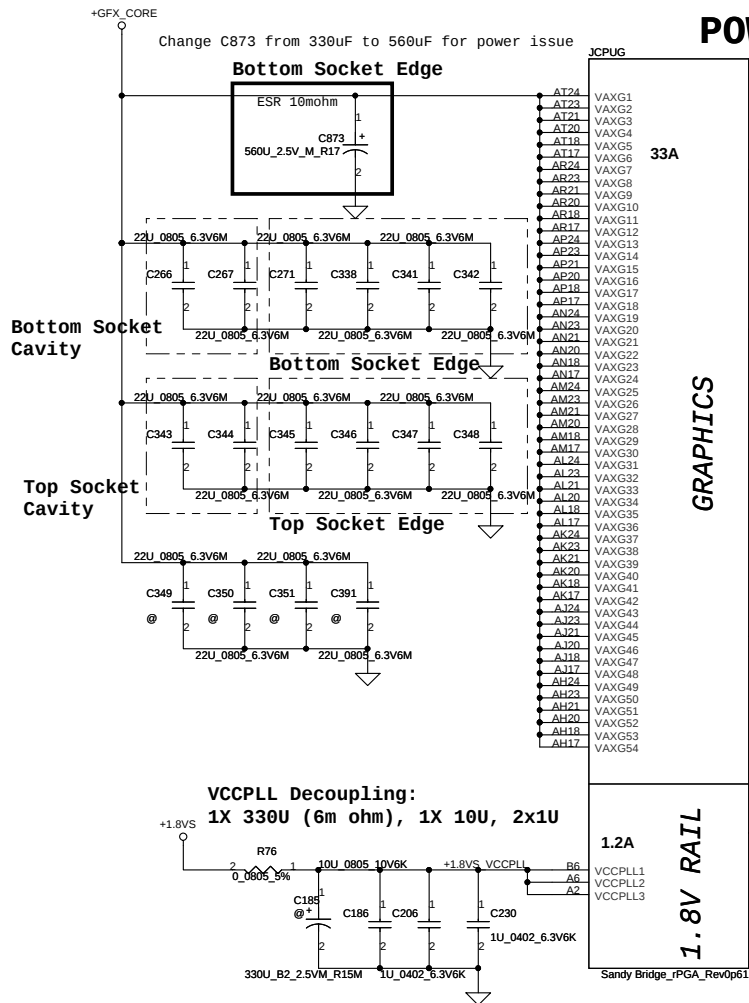
SENSE LINES



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Sandy Bridge_rPGA_Rev0p61

+GFX_CORE Decoupling:
1X 560U (10m ohm), 12X 22U



POWER

SENSE LINES

VREF

DDR3 -1.5V RAILS

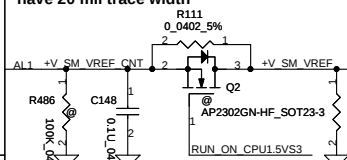
SA RAIL

MISC

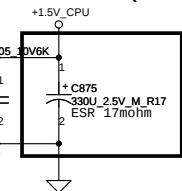
GRAPHICS

AK35 VCC_AXG_SENSE
AK34 VSS_AXG_SENSE

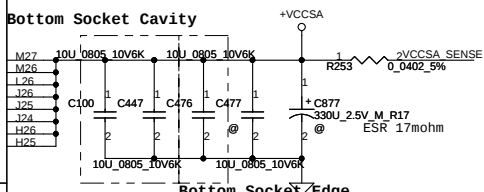
+V_SM_VREF should have 20 mil trace width



+1.5V_CPU Decoupling:
1X 330U (17m ohm), 6X 10U

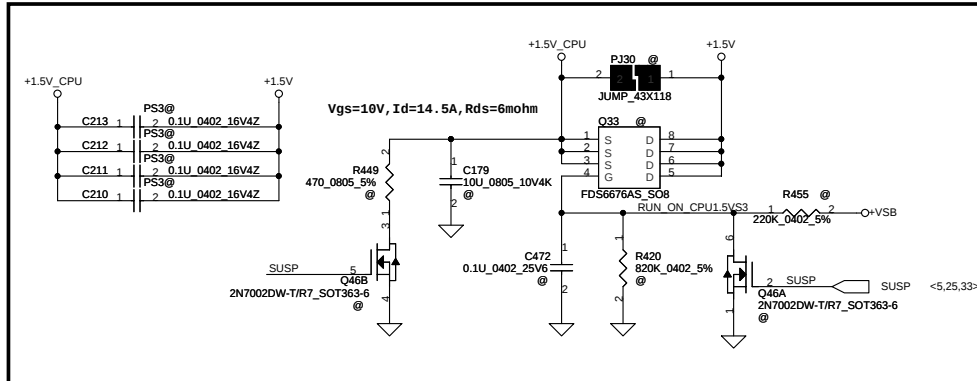


+VCCSA Decoupling:
1X 330U (17m ohm), 4X 10U

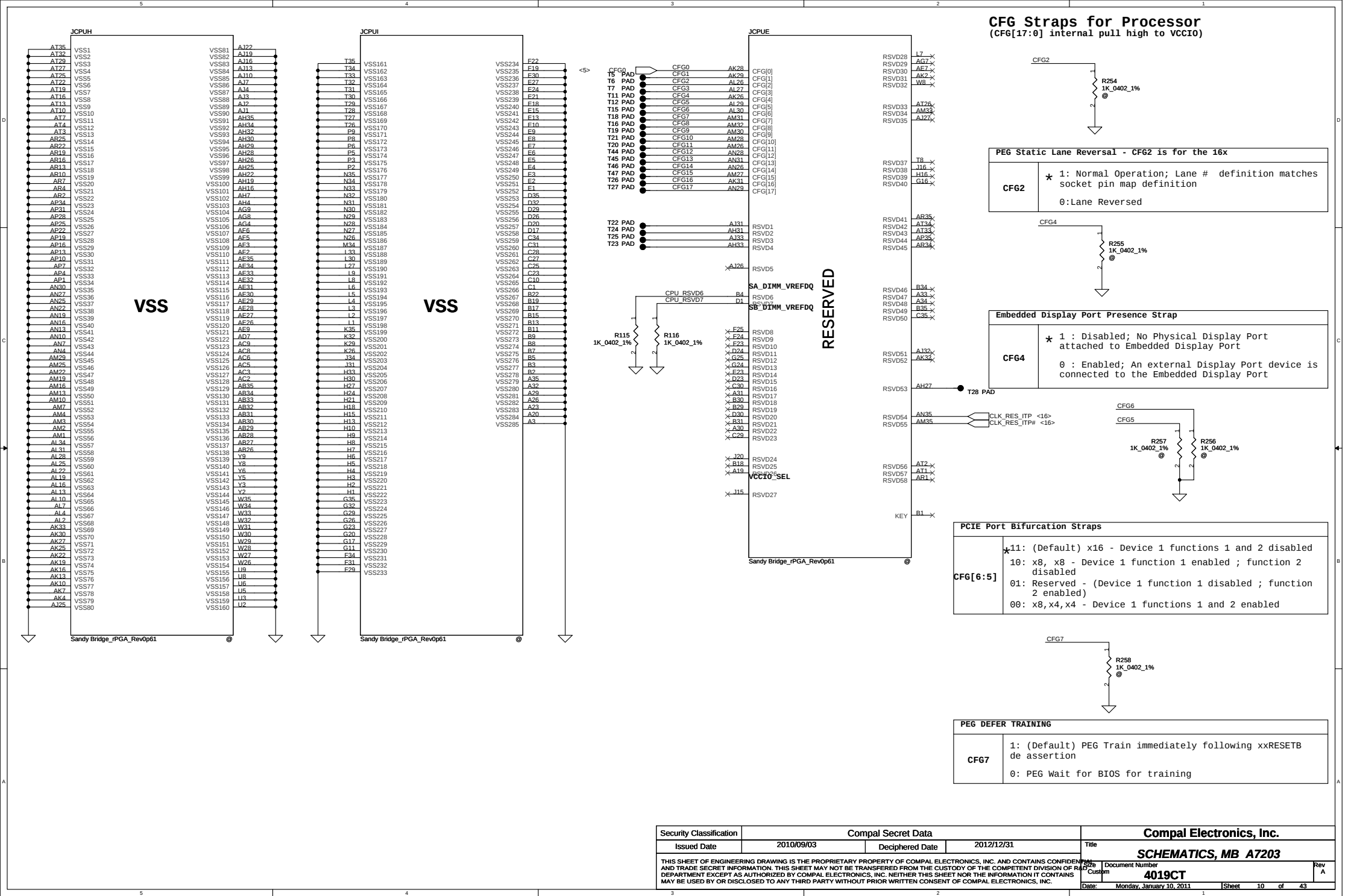


VCCSA_VID0	VCCSA_VID1	+VCCSA
0	0	0.90 V
0	1	0.80 V
1	0	0.75 V
1	1	0.65 V

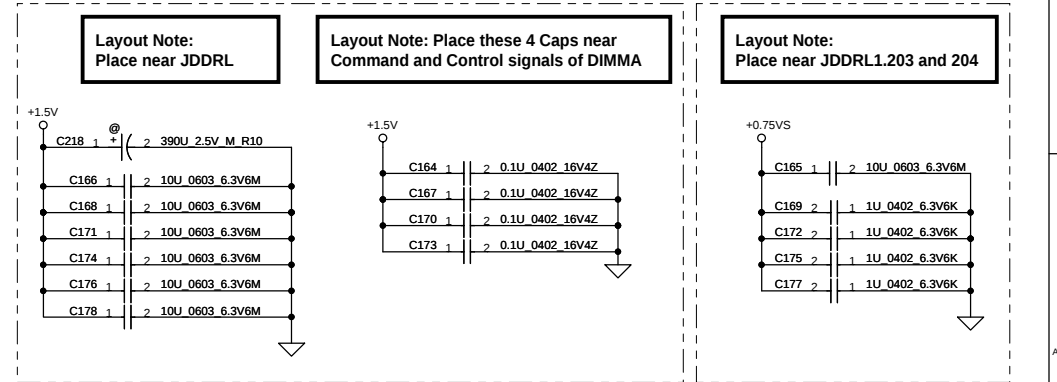
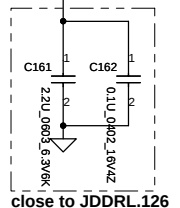
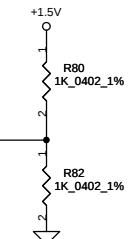
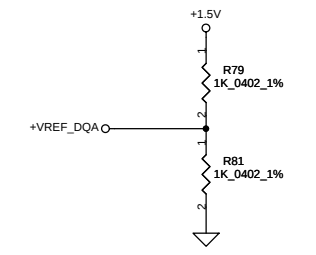
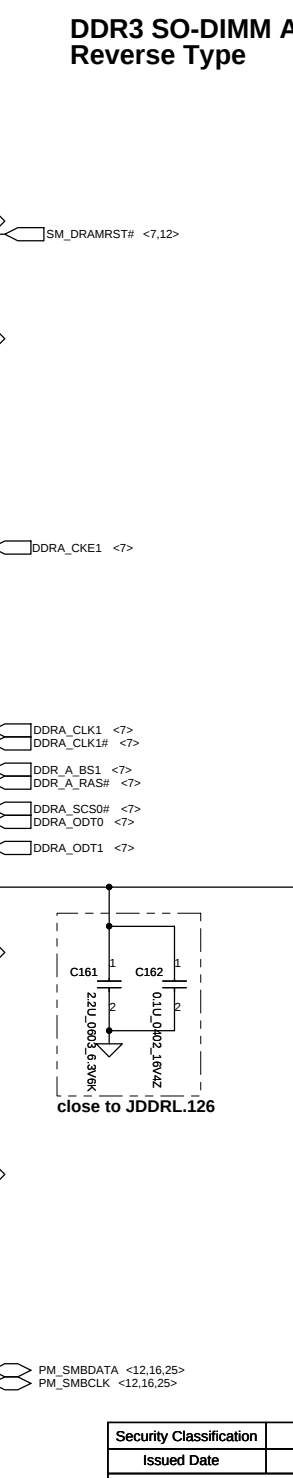
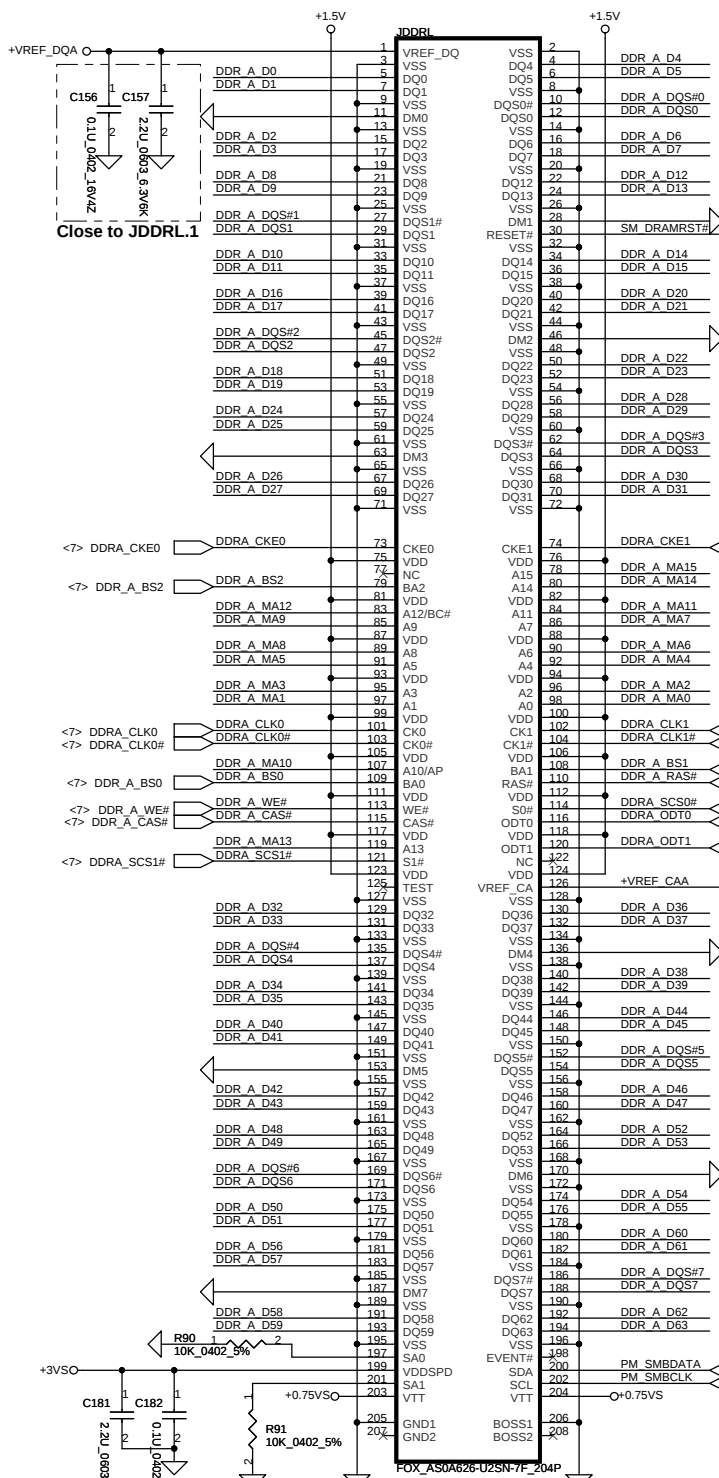
For Sandy Bridge



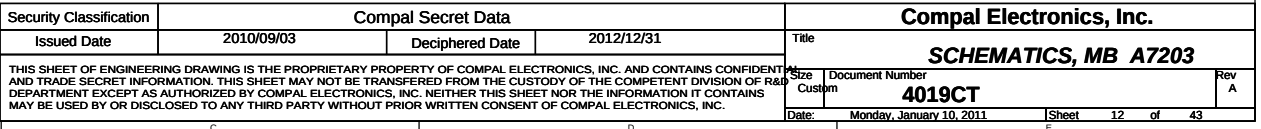
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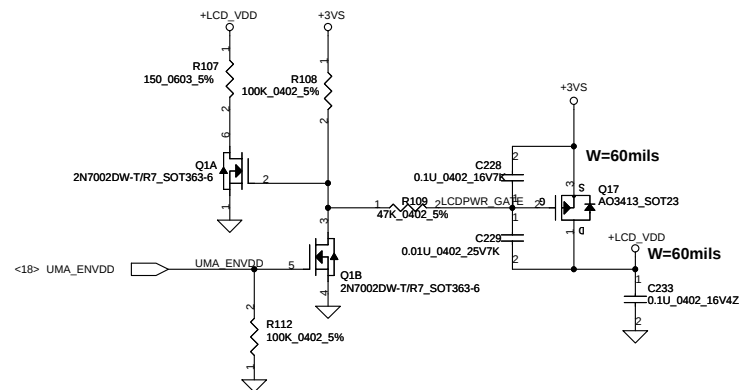
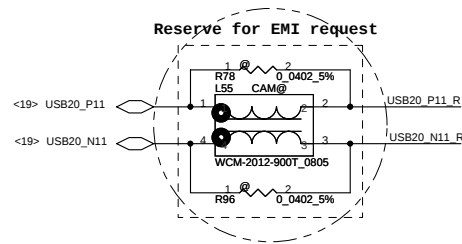
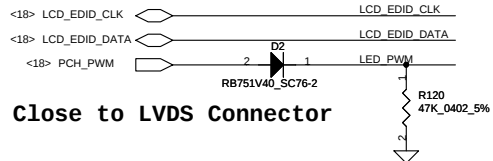


DDR3 SO-DIMM A Reverse Type

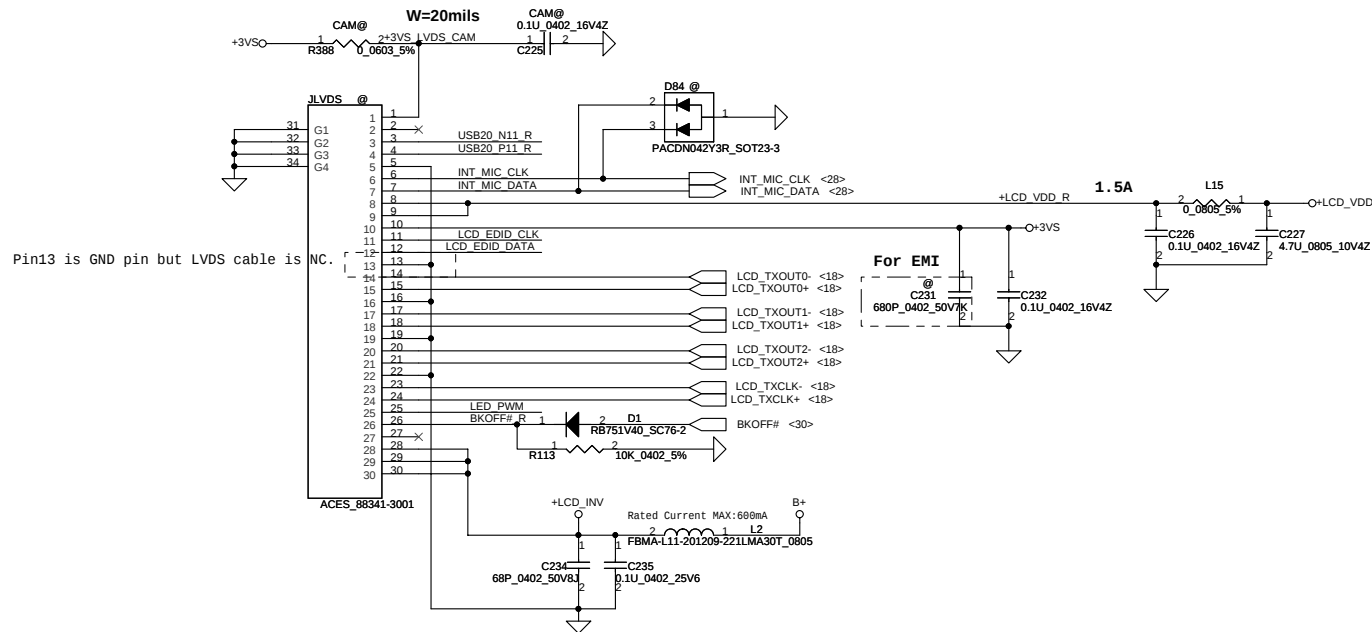


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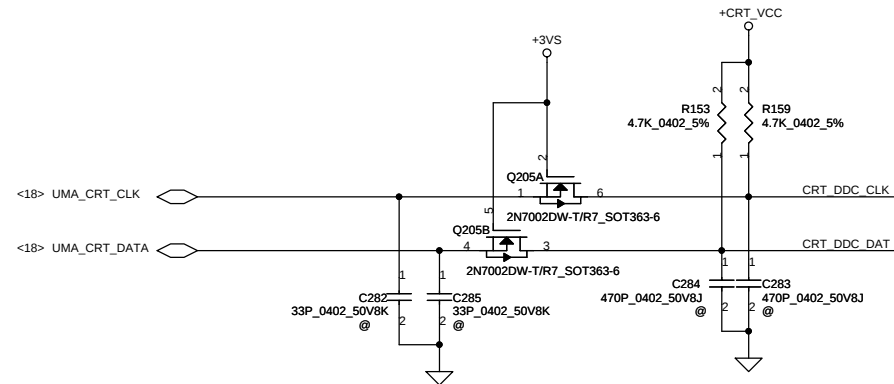
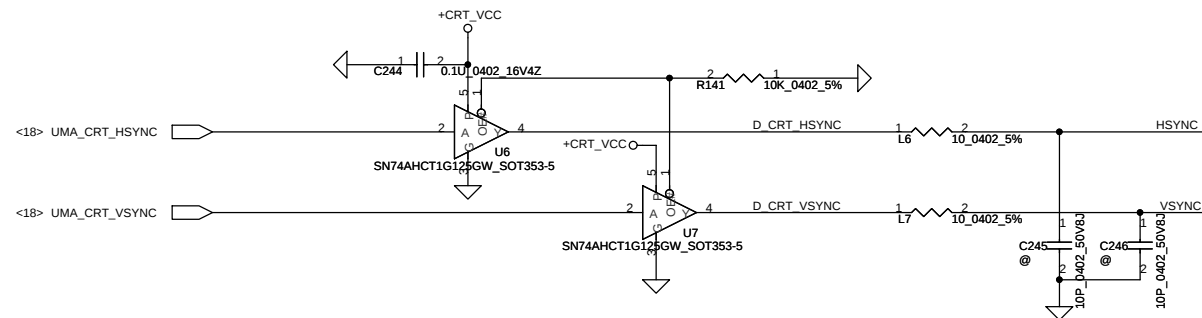
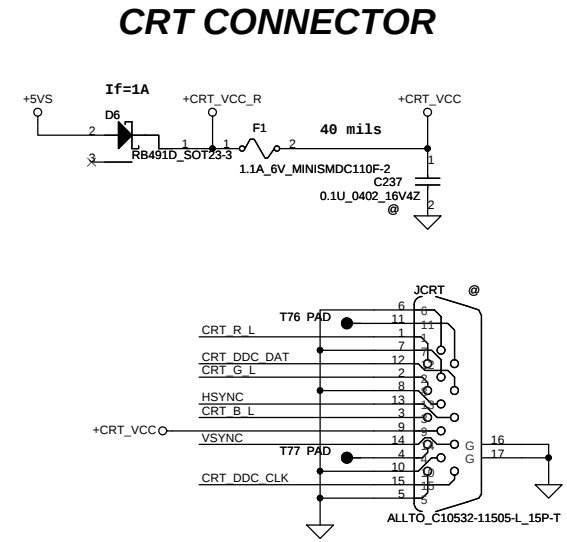
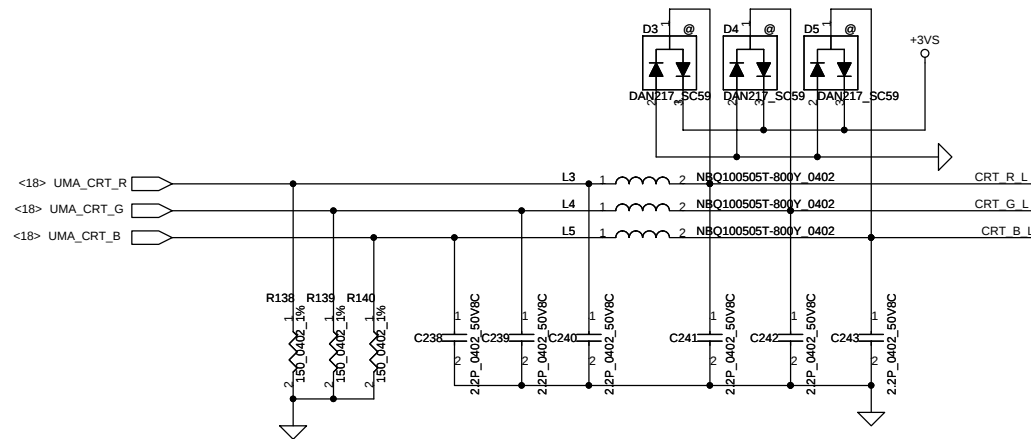




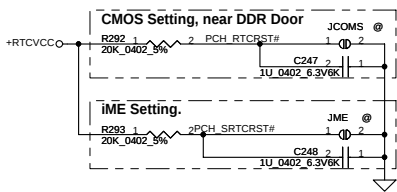
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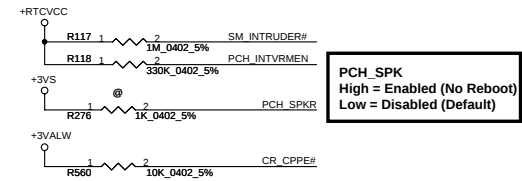


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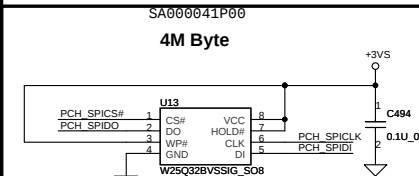
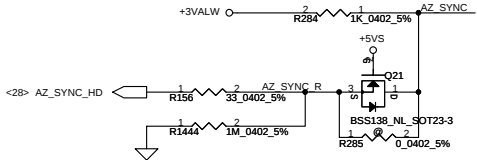
Integrated SUS 1.05V VRM Enable

PCH_INTVRMEN High - Enable Internal VRs (must be always pulled high)

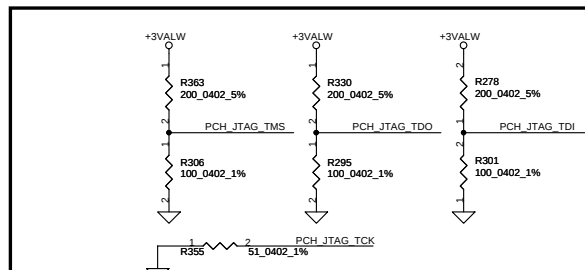
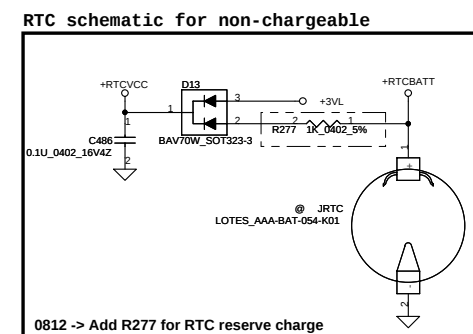
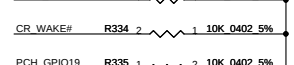
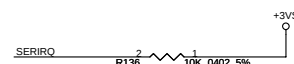
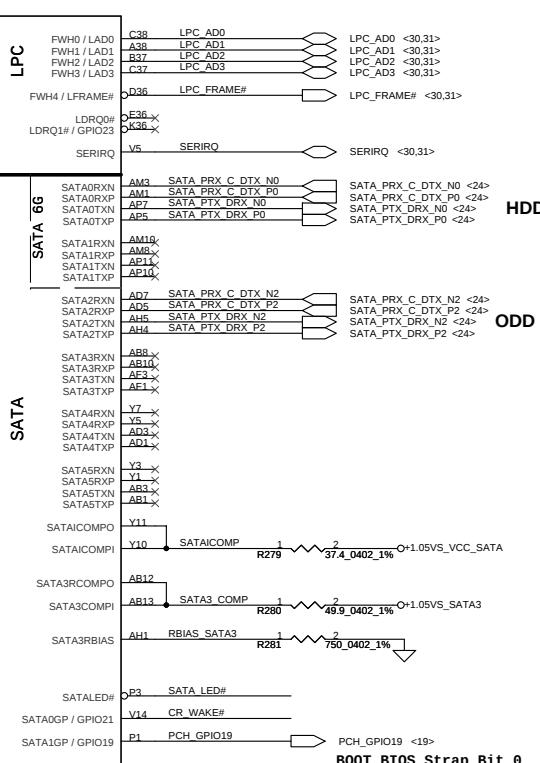
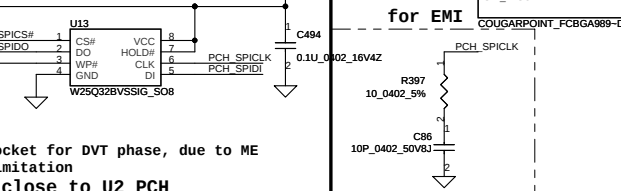
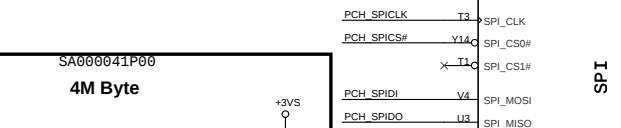
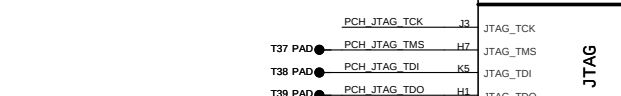
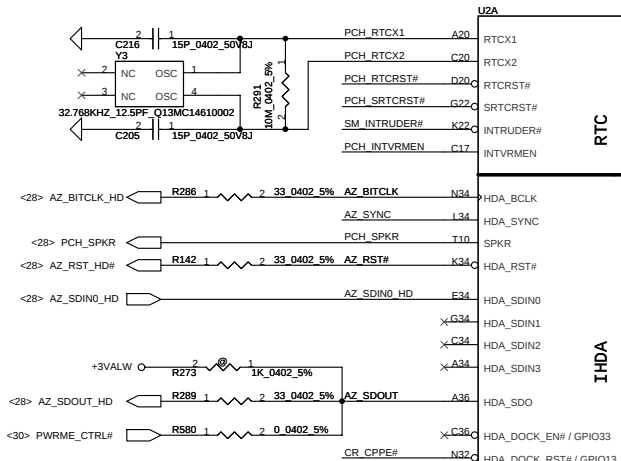


HDA_SDO
ME debug mode,
this signal has a weak internal pull down
*Low = Disable (default)
High = Enable (flash descriptor security override)

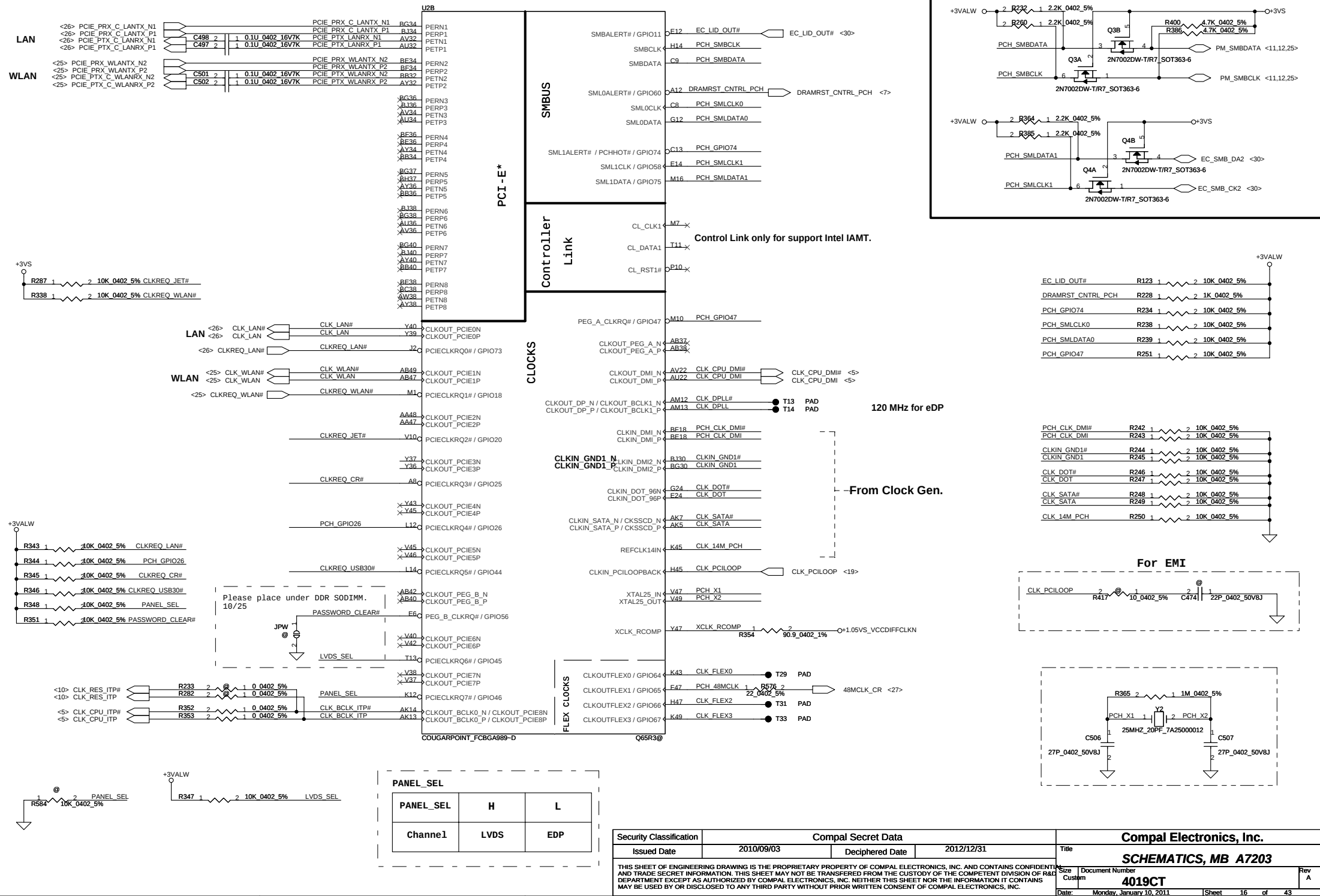
HDA_SYNC
*This signal has a weak internal pull down
H=>On Die PLL is supplied by 1.5V
L=>On Die PLL is supplied by 1.8V
Need to pull high for Huron River platform



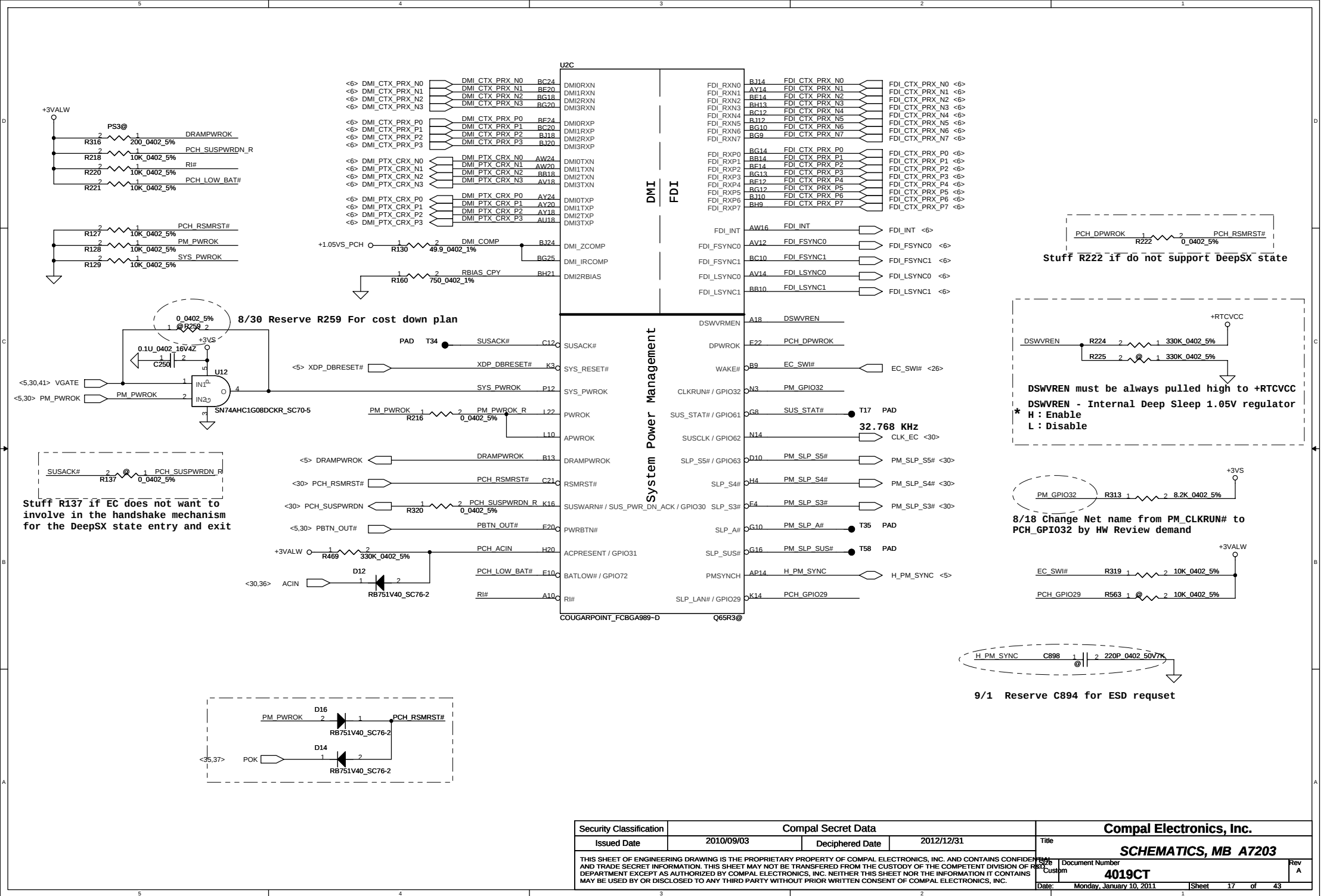
remove socket for DVT phase, due to ME height limitation
Please close to U2 PCH

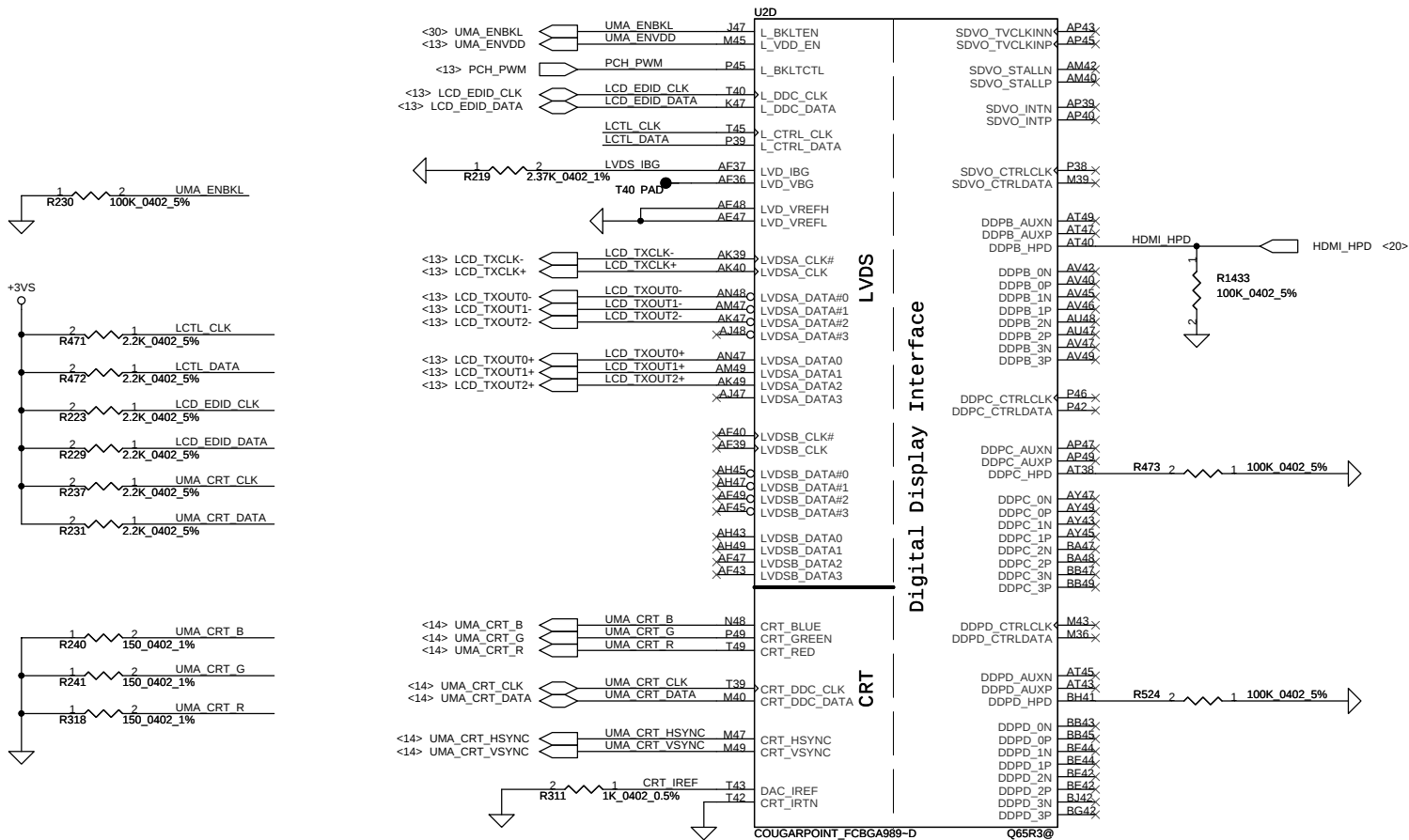


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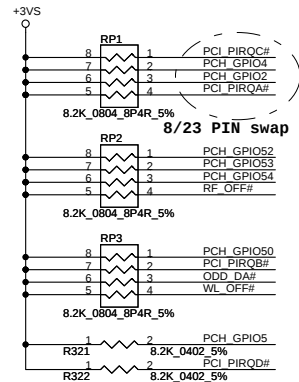


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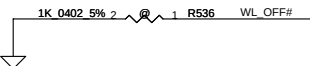
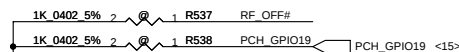
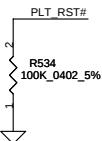
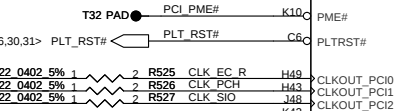
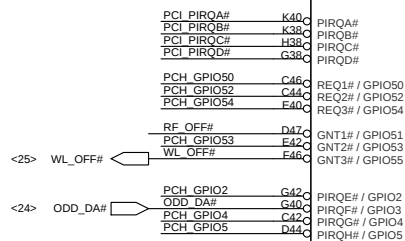




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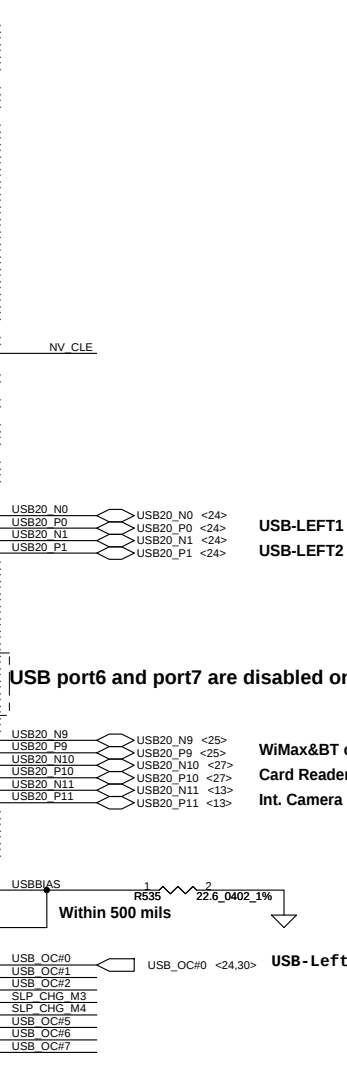
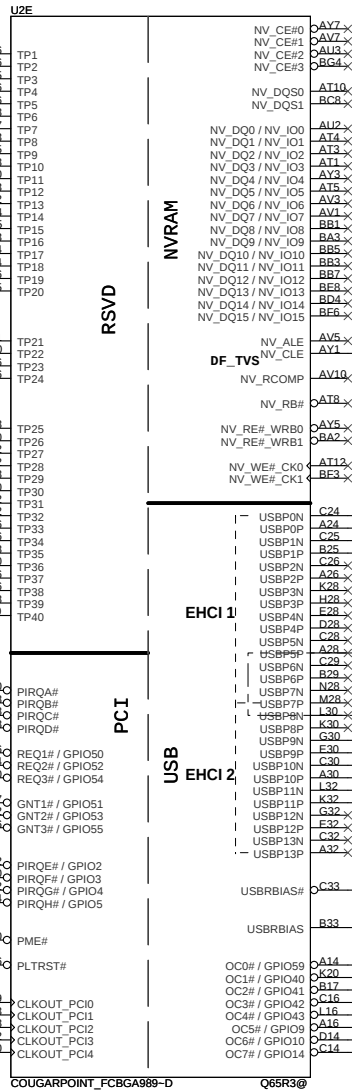


8/23 PIN swap for layout request

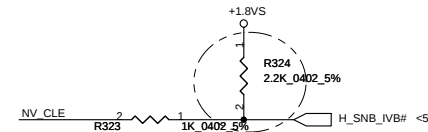


Boot BIOS Strap		
RF_OFF#	PCH_GPIO19	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI *

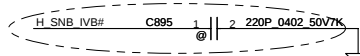
A16 Swap Override Strap	
WL_OFF#	
*	Low= A16 swap override Enable High= A16 swap override Disable



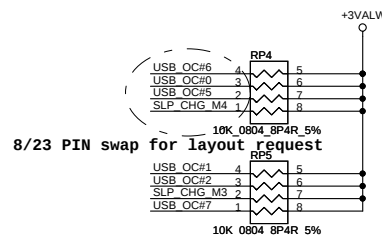
DMI & FDI Termination Voltage	
NV_CLE	Set to VCC when HIGH Set to VSS when LOW



8/18 Change R324 From 1K to 2.2K by Intel check list demand

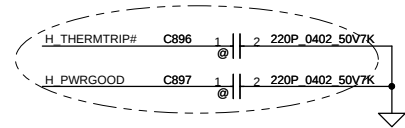
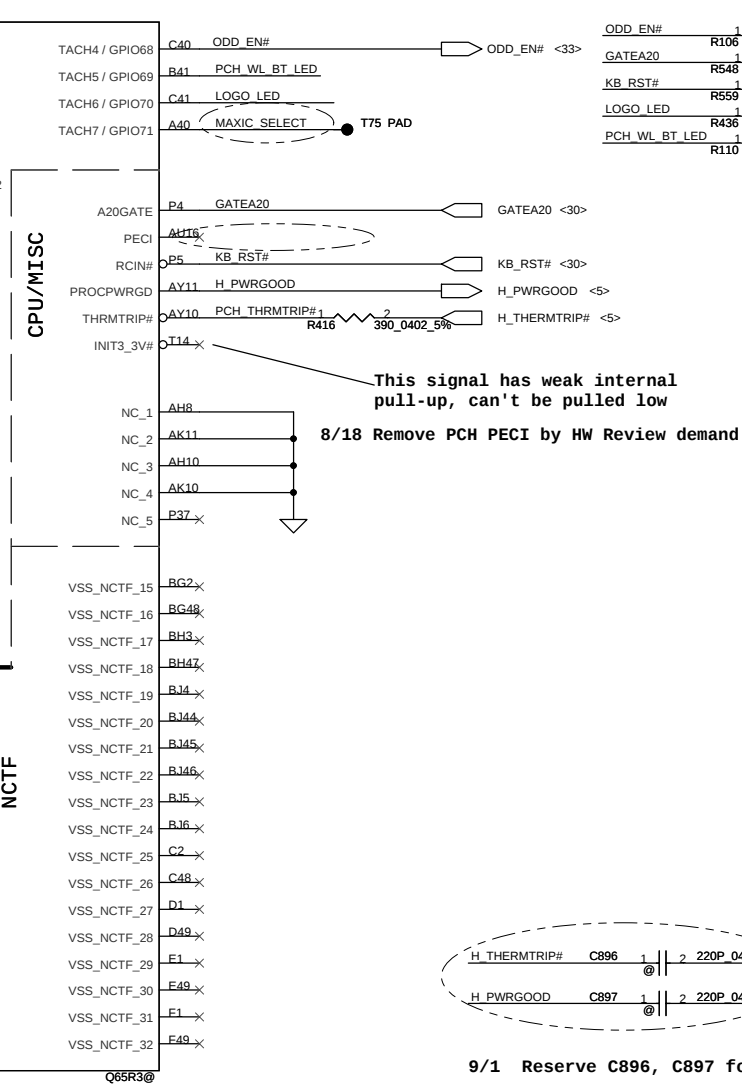
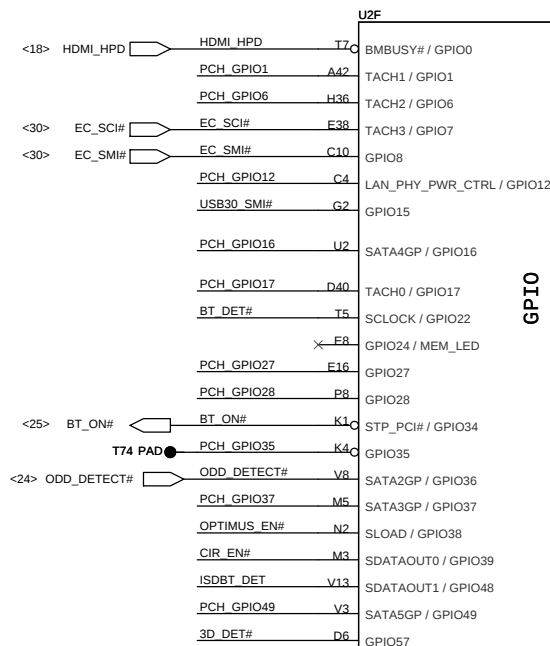
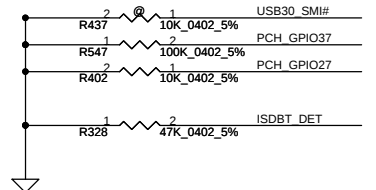
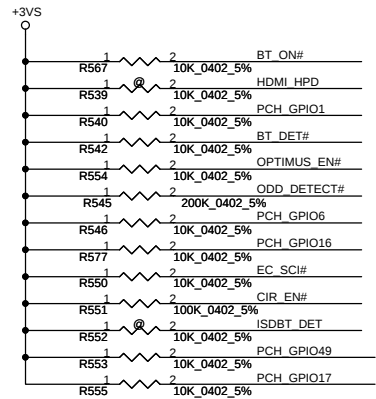
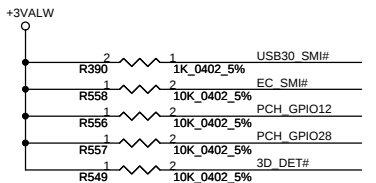


9/1 Reserve C895 for ESD request



8/23 PIN swap for layout request

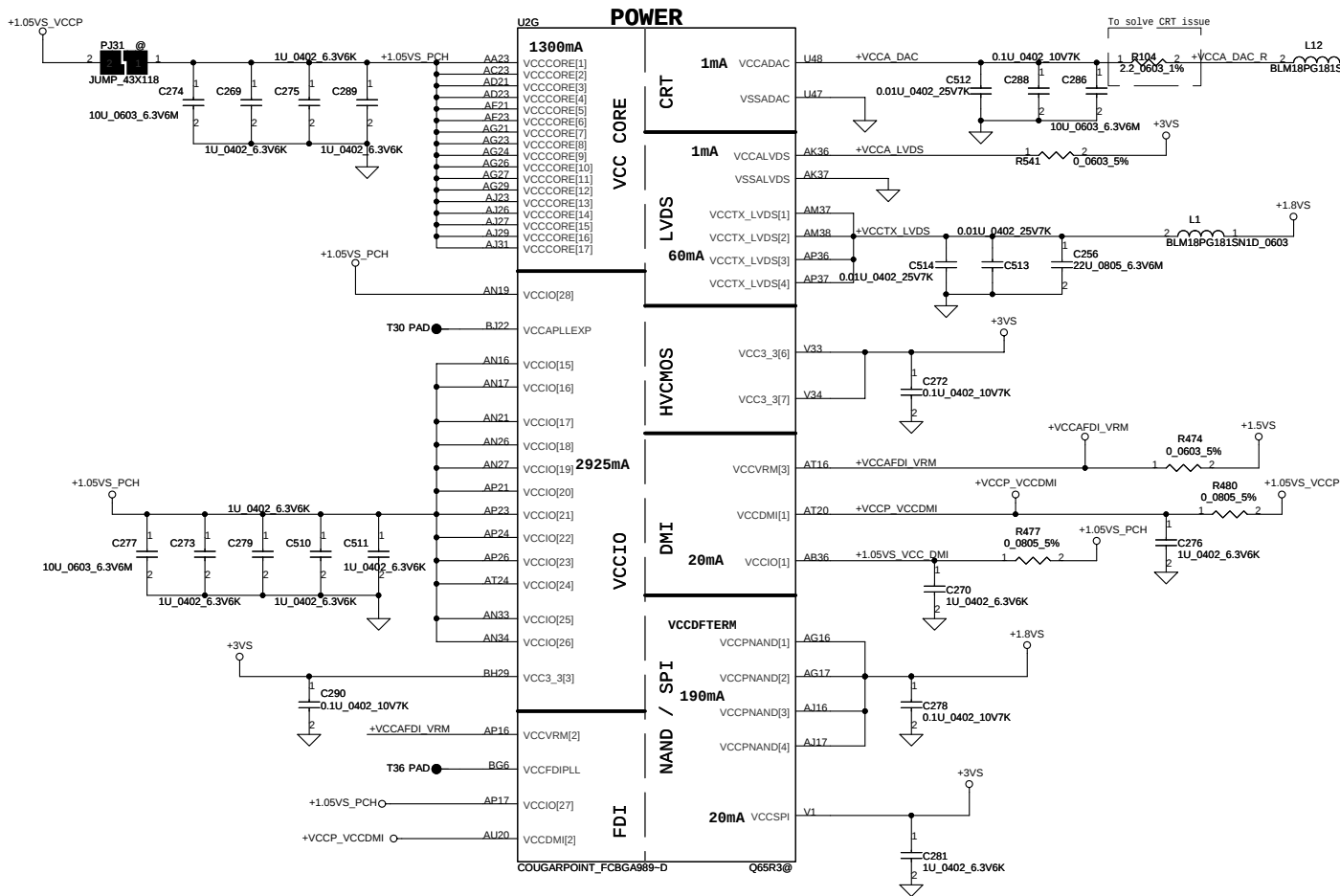
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								SCHEMATICS, MB A7203					
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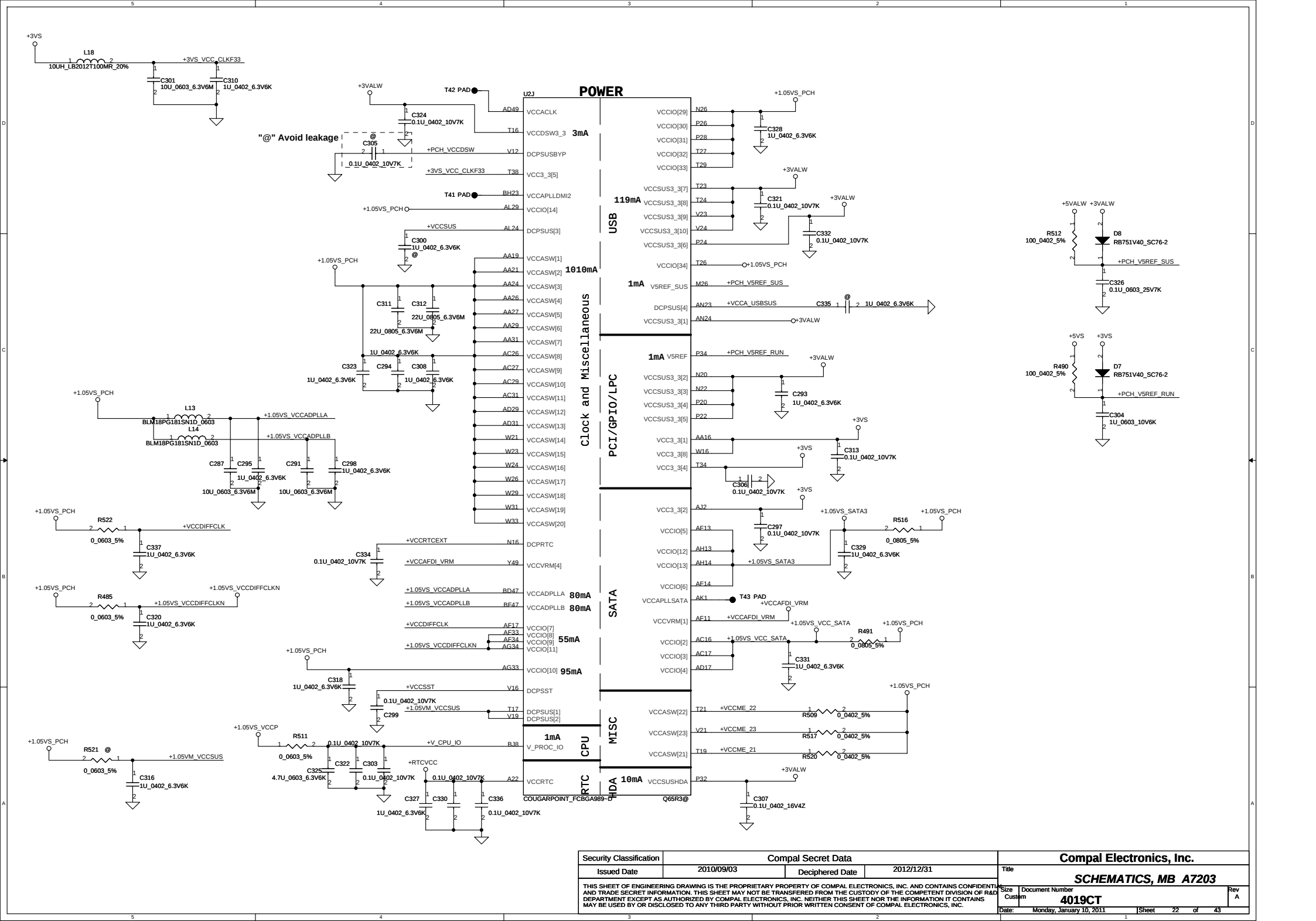
GPIO28
On-Die PLL Voltage Regulator
H: Enable
L: Disable

GPIO8
Integrated Clock Chip Enable (Removed)
H: Disable
* L: Enable

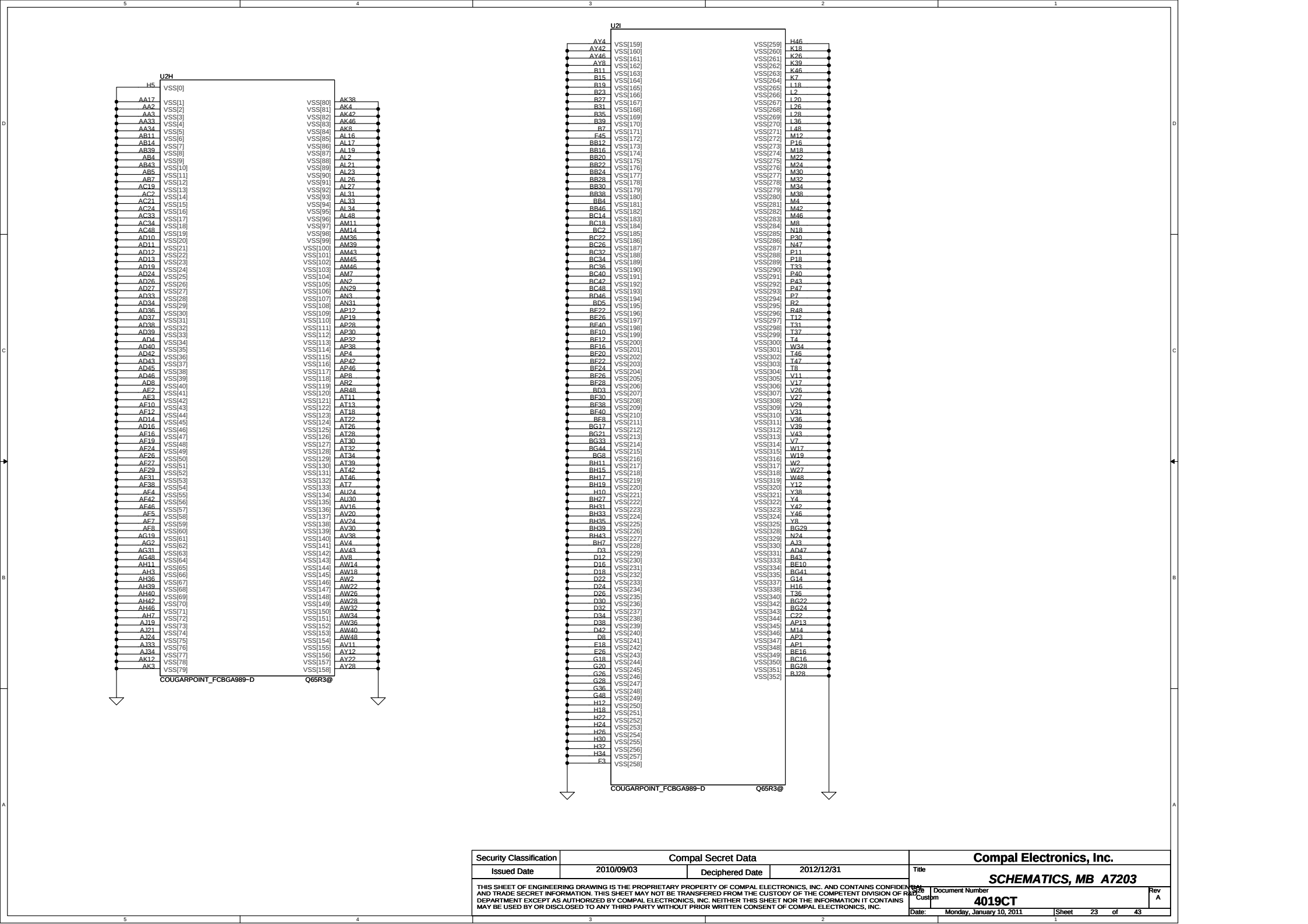
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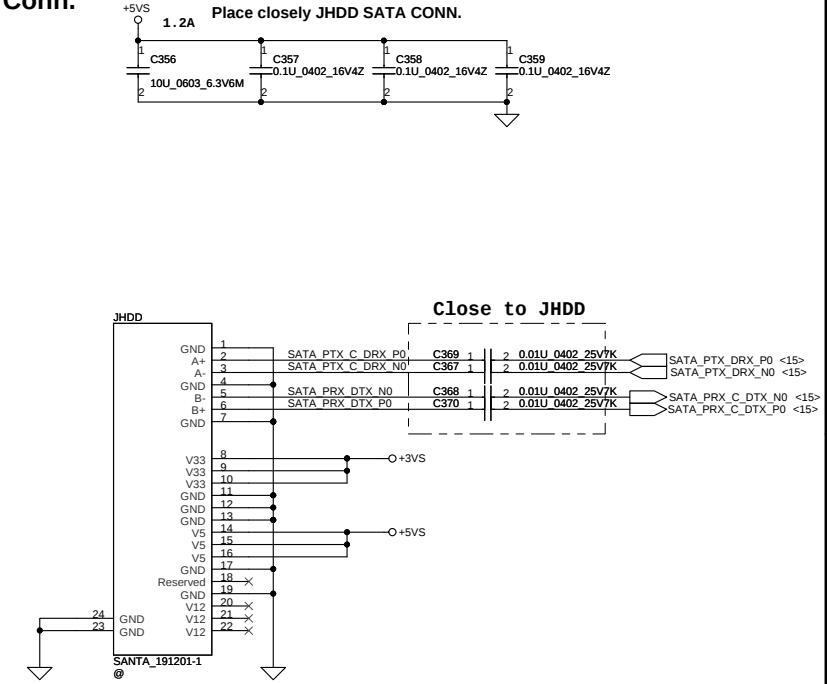
PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_SUS	5	0.001
VCC3_3	3.3	0.266
VCCADAC	3.3	0.001
VCCADPLLA	1.05	0.08
VCCADPLL	1.05	0.08
VCCCORE	1.05	1.3
VCCDMI	1.05	0.042
VCCIO	1.05	2.925
VCCASW	1.05	1.01
VCCSPI	3.3	0.02
VCCDSW	3.3	0.002
VCCDFTERM	1.8	0.19
VCCRTC	3.3	6 uA
VCCSUS3_3	3.3	0.97
VCCSUSHDA	3.3 / 1.5	0.01
VCCVRM	1.5	0.16
VCCCLKDMI	1.05	0.02
VCCSSC	1.05	0.095
VCCDIFFCLKN	1.05	0.055
VCCALVDS	3.3	0.001
VCCTX_LVDS	1.8	0.06



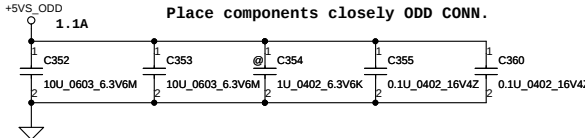
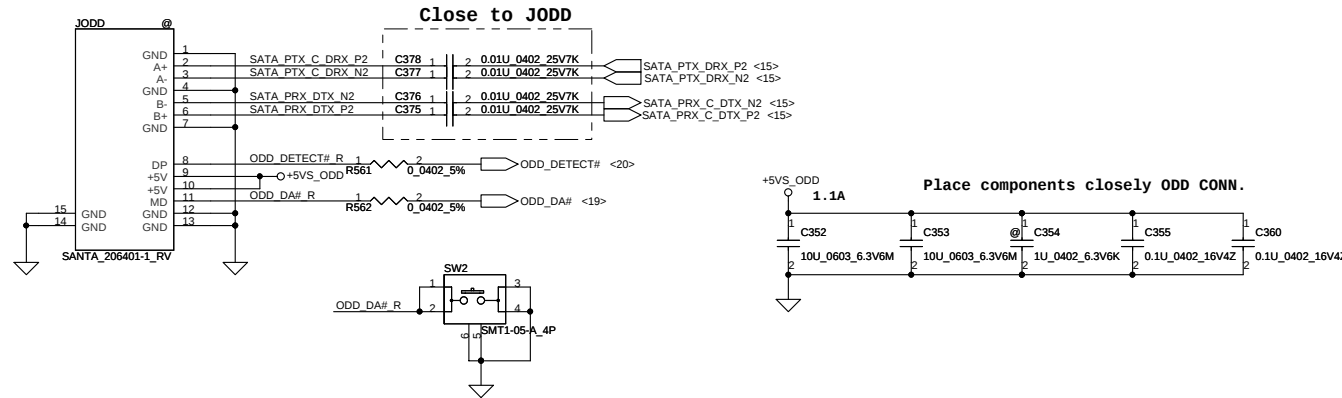
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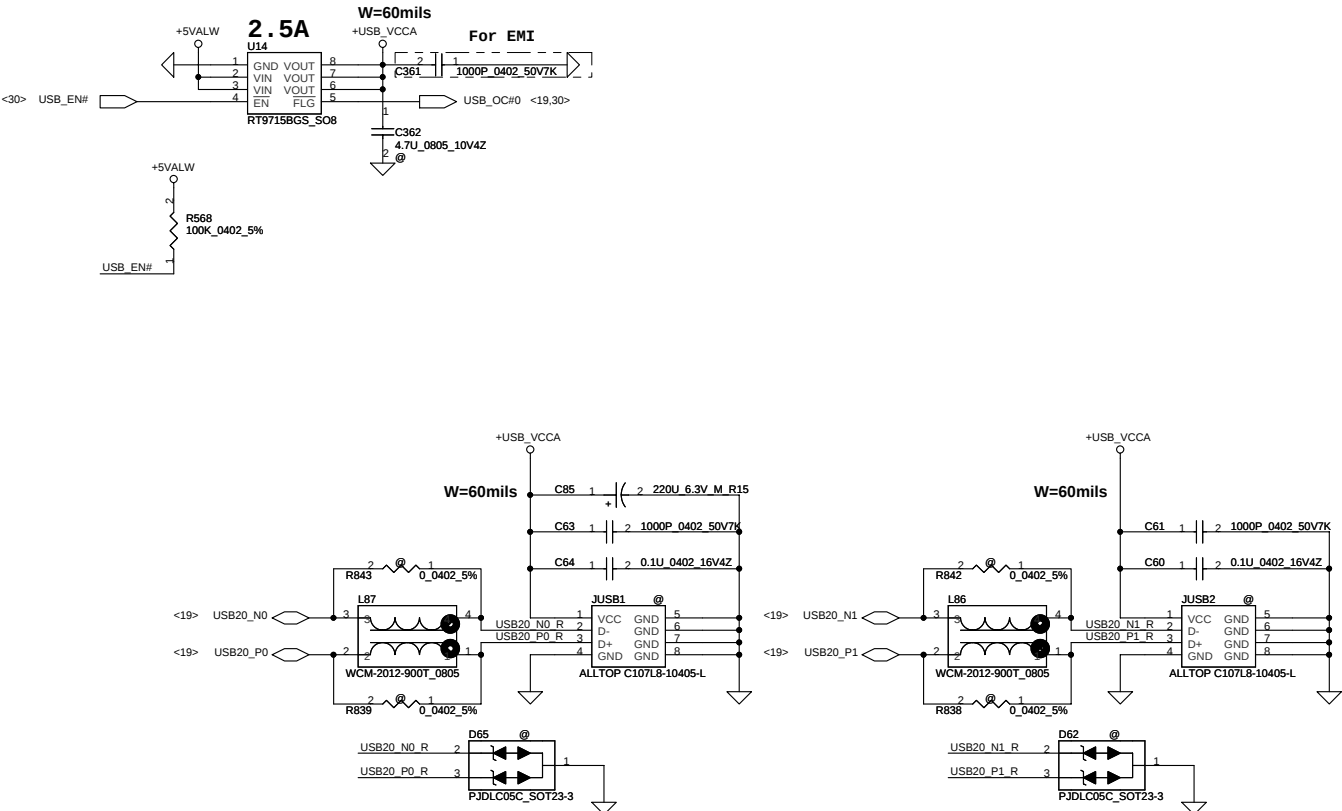
SATA HDD Conn.



SATA ODD Conn

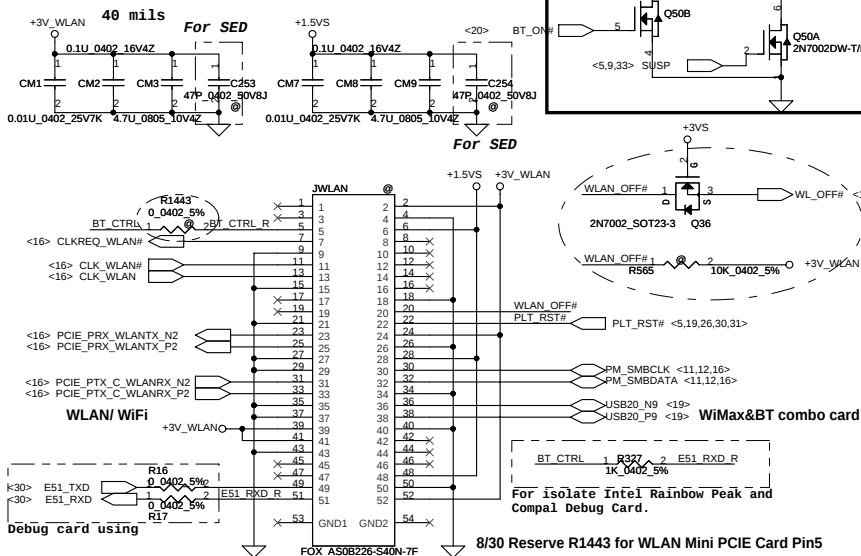
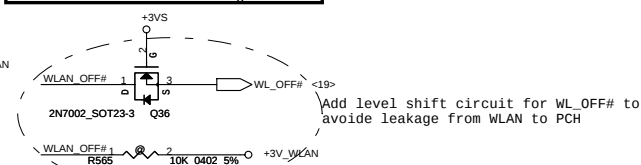
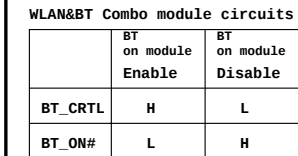


USB Conn. Left Side



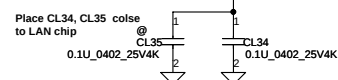
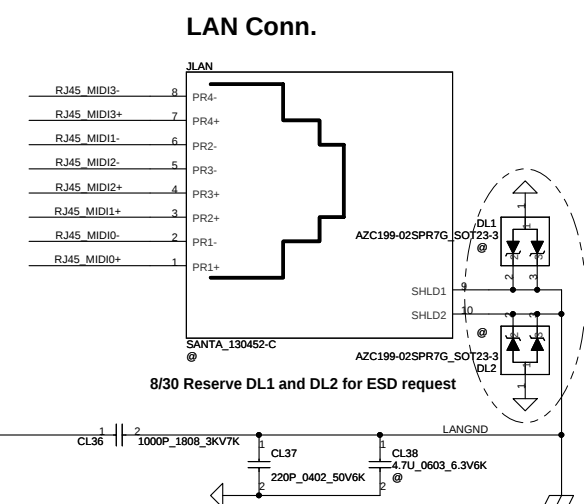
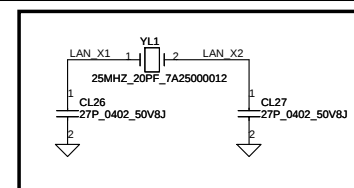
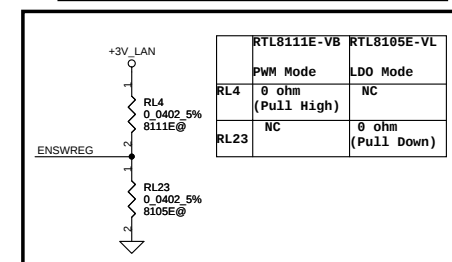
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Diagram showing the jumper configuration for WLAN/Wimax. It features two jumpers, PJ27 and PJ26, both labeled "JUMP_43X79". PJ27 is connected to +3VALW (pin 2) and +3V_WLAN (pin 1). PJ26 is connected to +3V50 (pin 2) and +3V_WLAN (pin 1). Below the diagram, a box contains the text: "Short PJ27 for Wimax" and "Short PJ26 for WLAN".



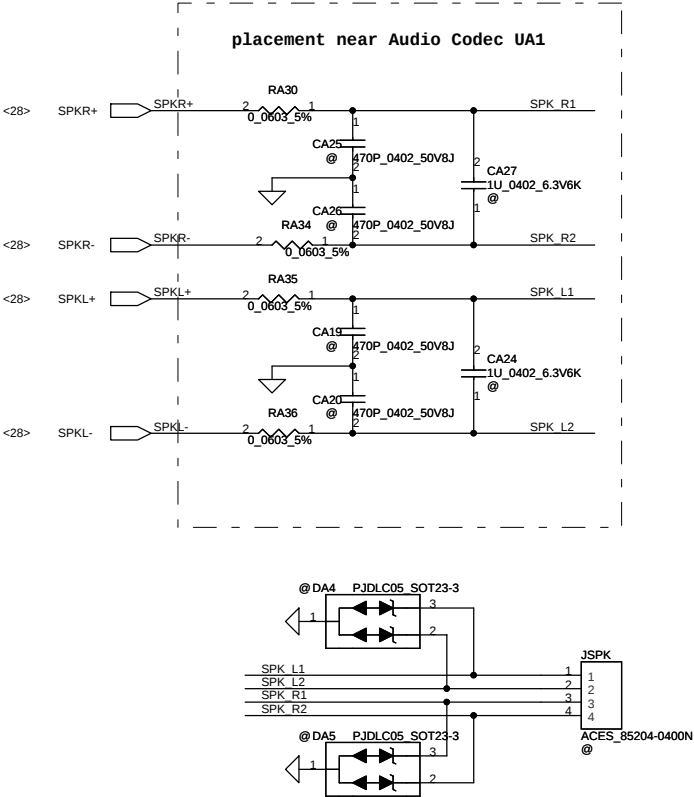
8/30 Reserve R1443 for WLAN Mini PCIE Card Pin5

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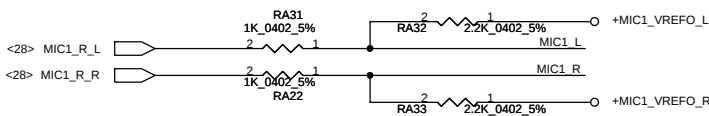


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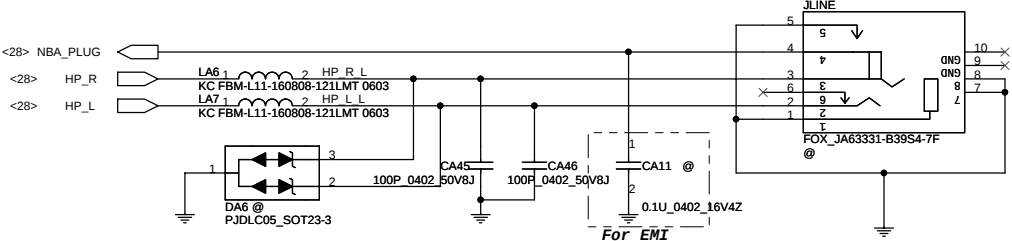
Speaker Connector



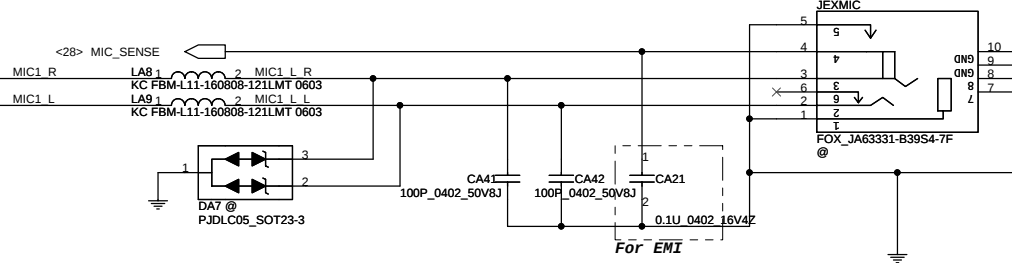
Ext. Mic



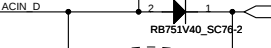
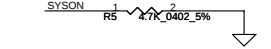
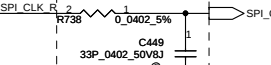
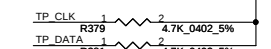
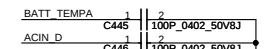
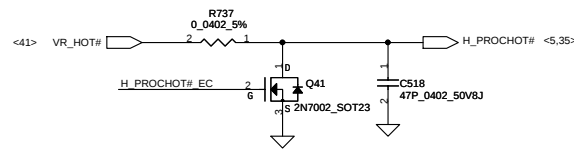
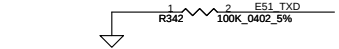
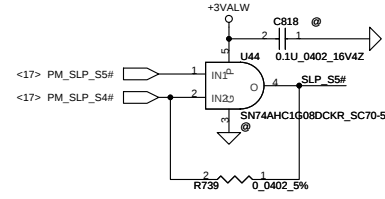
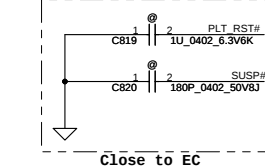
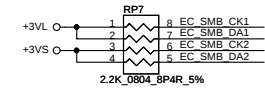
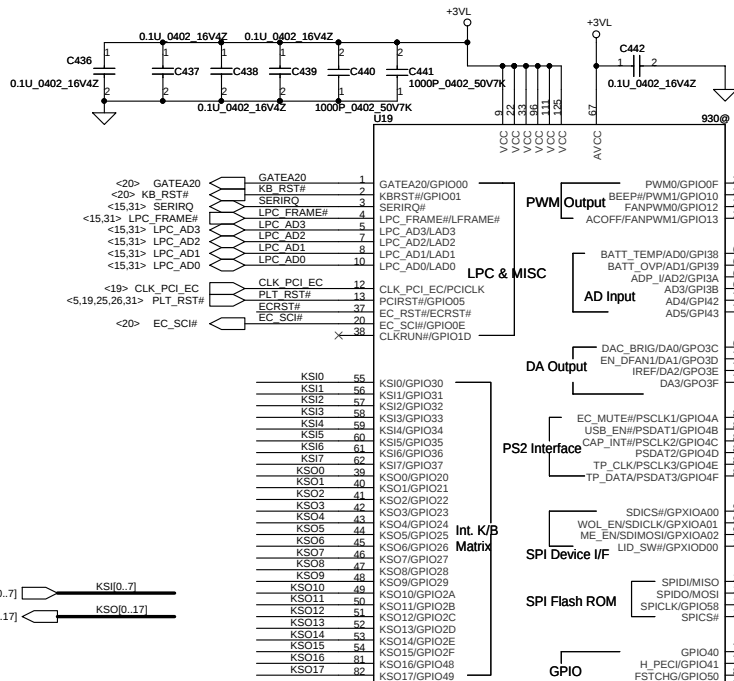
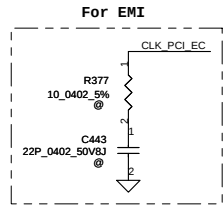
HeadPhone/LINE Out JACK



Ext.MIC/LINE IN JACK

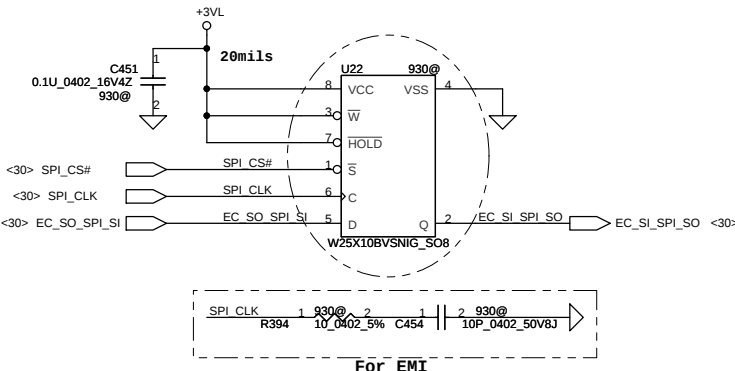


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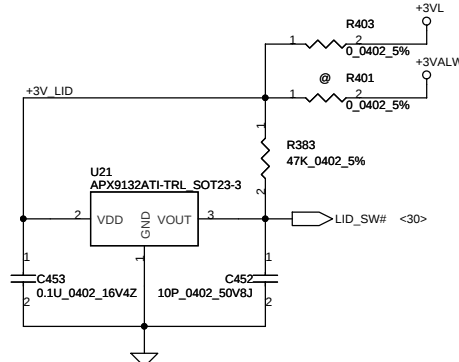


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SPI Flash (256KB)

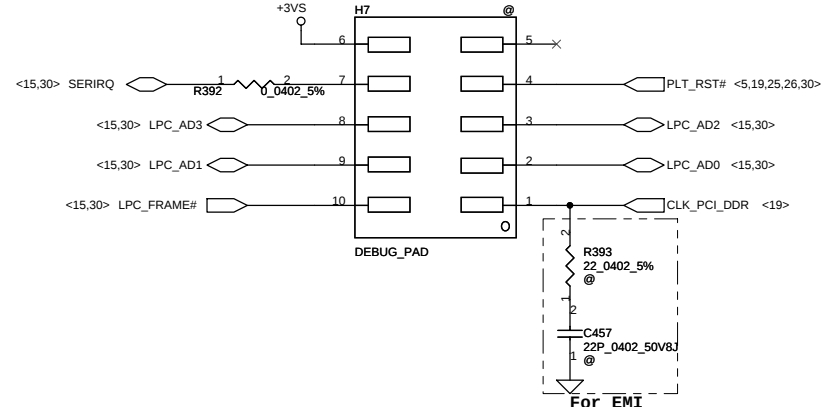


Lid SW

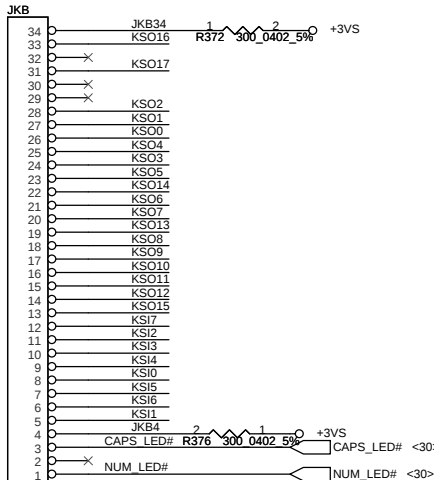
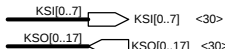


LPC Debug Port

Place the PAD under DDR DIMM

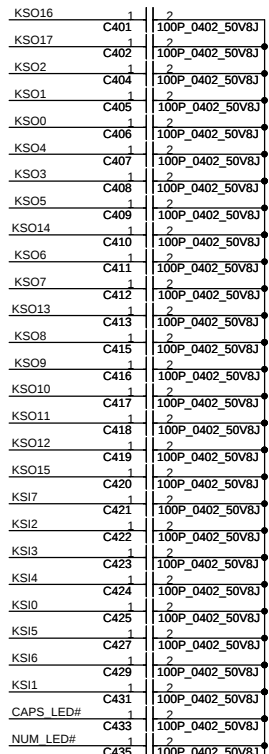


KEYBOARD CONN.



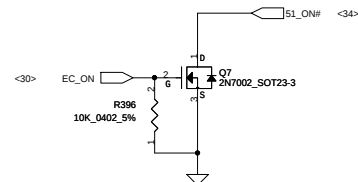
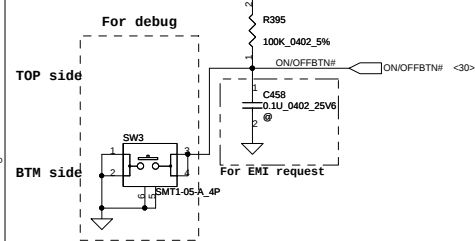
For EMI

Close to JKE

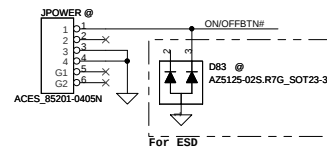


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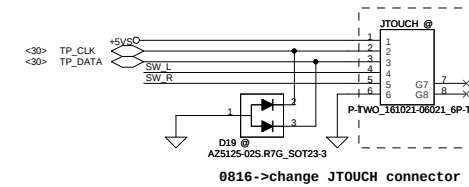
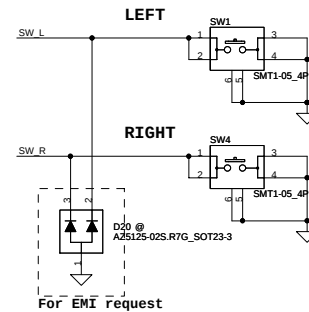
Power Button



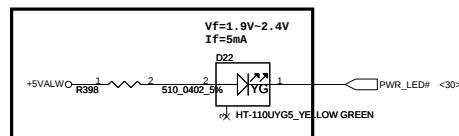
PWR/B to MB Conn.



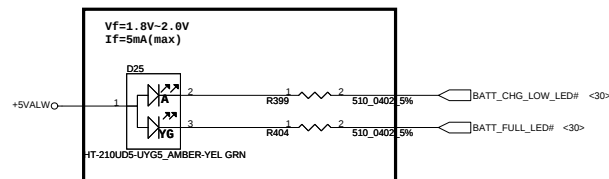
TP Button/Conn.



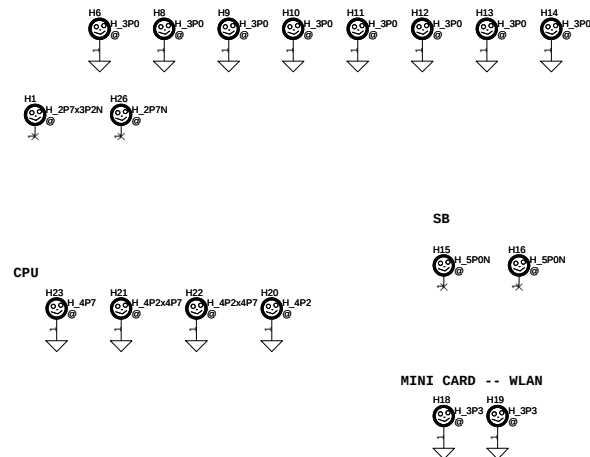
POWER/SUSPEND LED



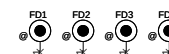
BATT CHARGE/FULL LED



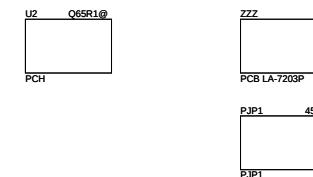
Screw Hole



PCB Fedical Mark PAD

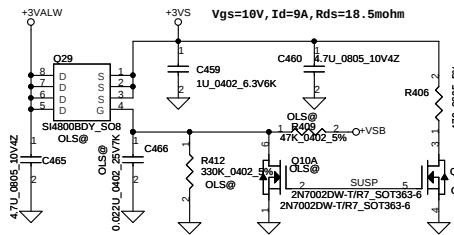


ISPD

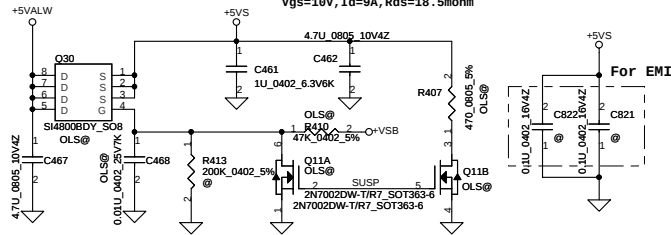


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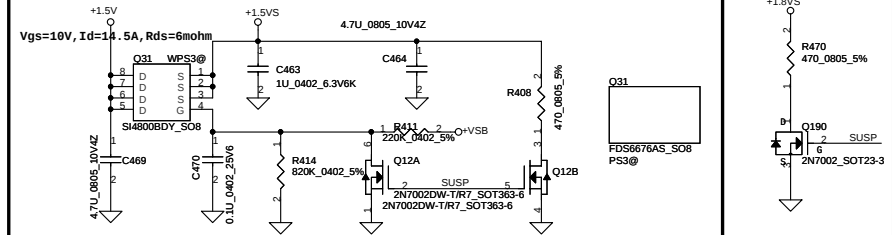
+3VALW TO +3VS



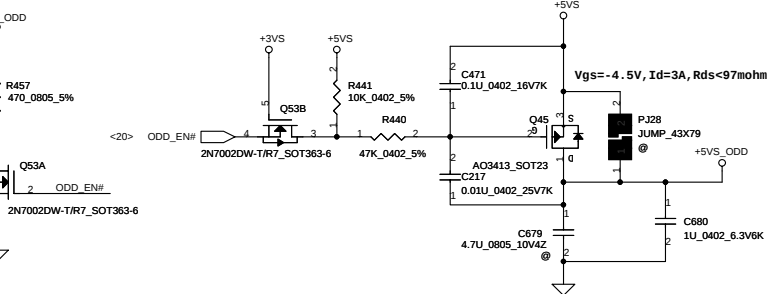
+5VALW TO +5VS



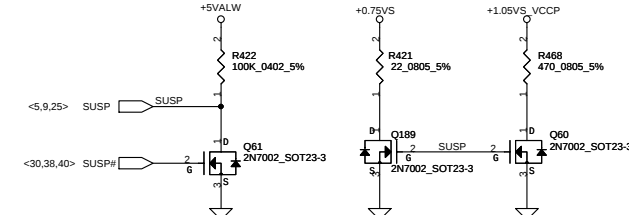
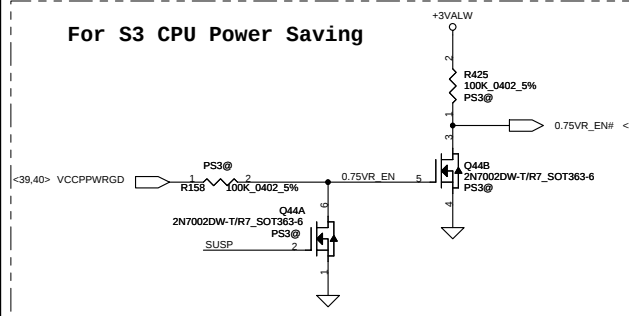
+1.5V to +1.5VS



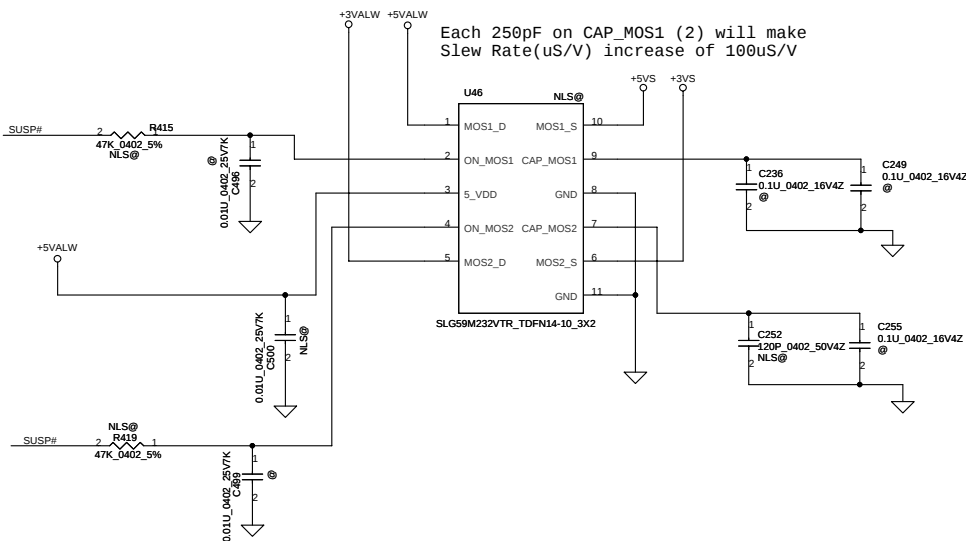
+5VS TO +5VS_ODD



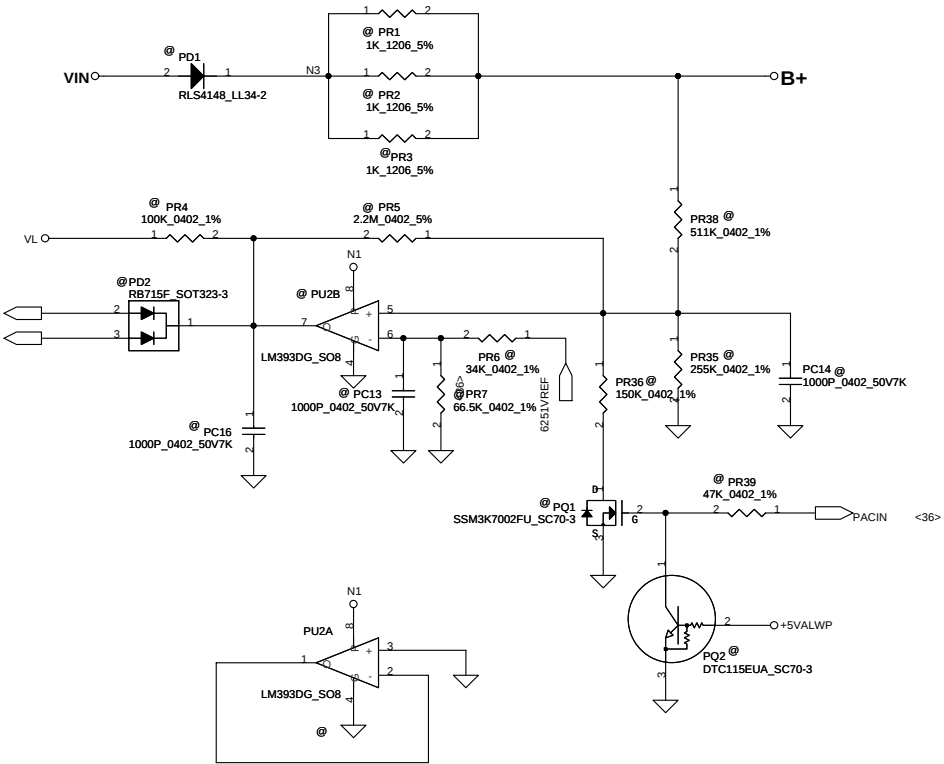
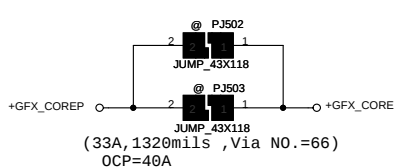
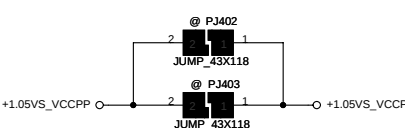
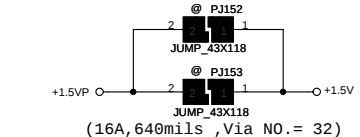
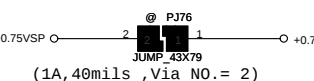
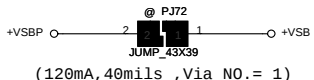
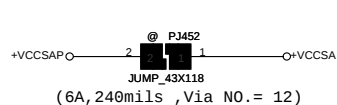
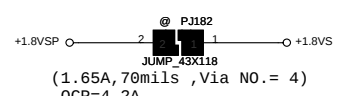
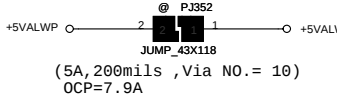
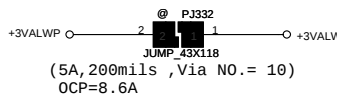
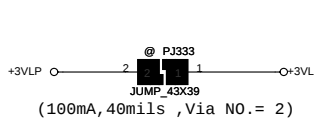
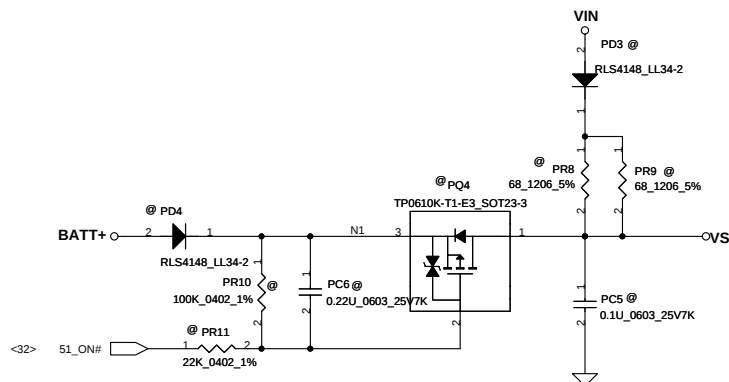
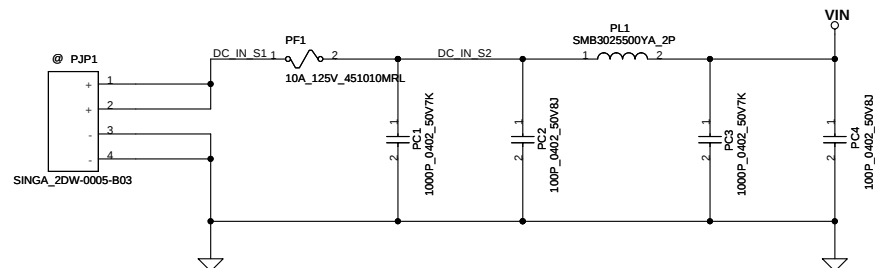
For S3 CPU Power Saving



Each 250pF on CAP_MOS1 (2) will make Slew Rate(uS/V) increase of 100uS/V

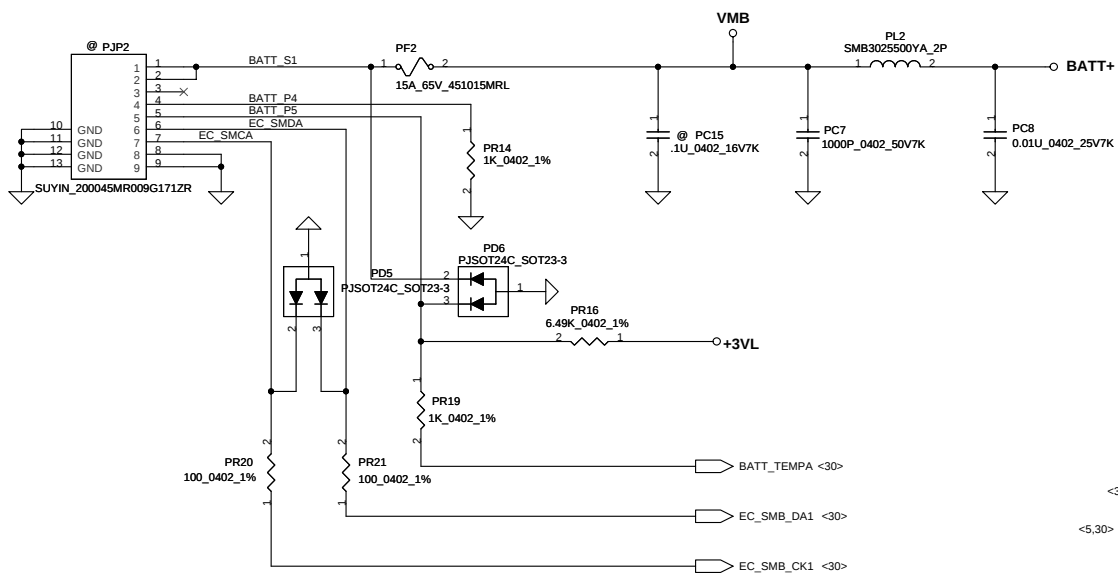


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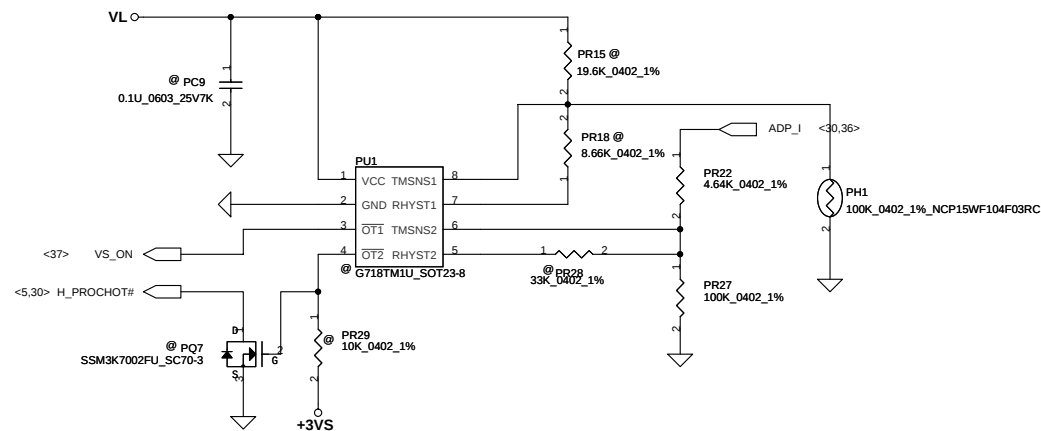


ACIN			
Precharge detector			
	Min.	typ.	Max
H->L	14.42V	14.74V	15.23V
L->H	15.39V	15.88V	16.39V

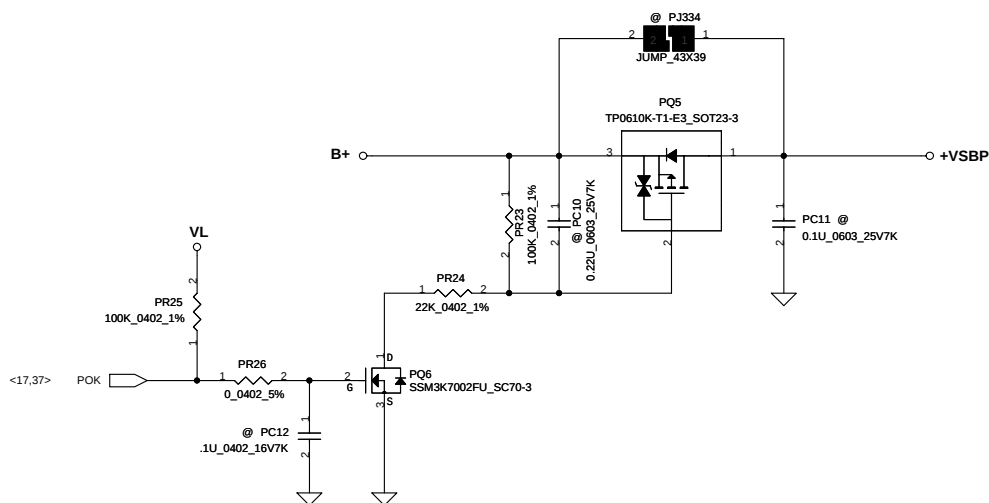
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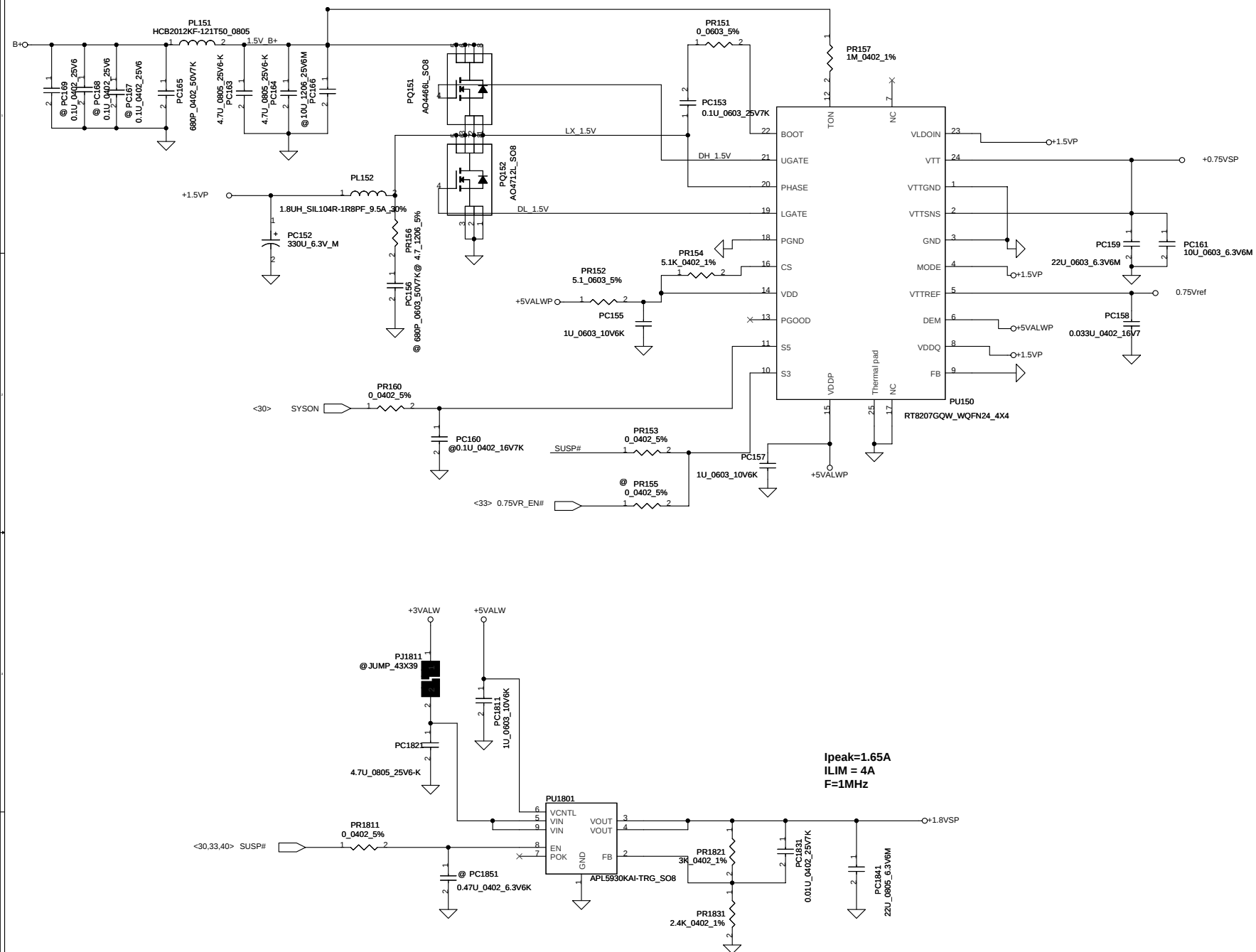


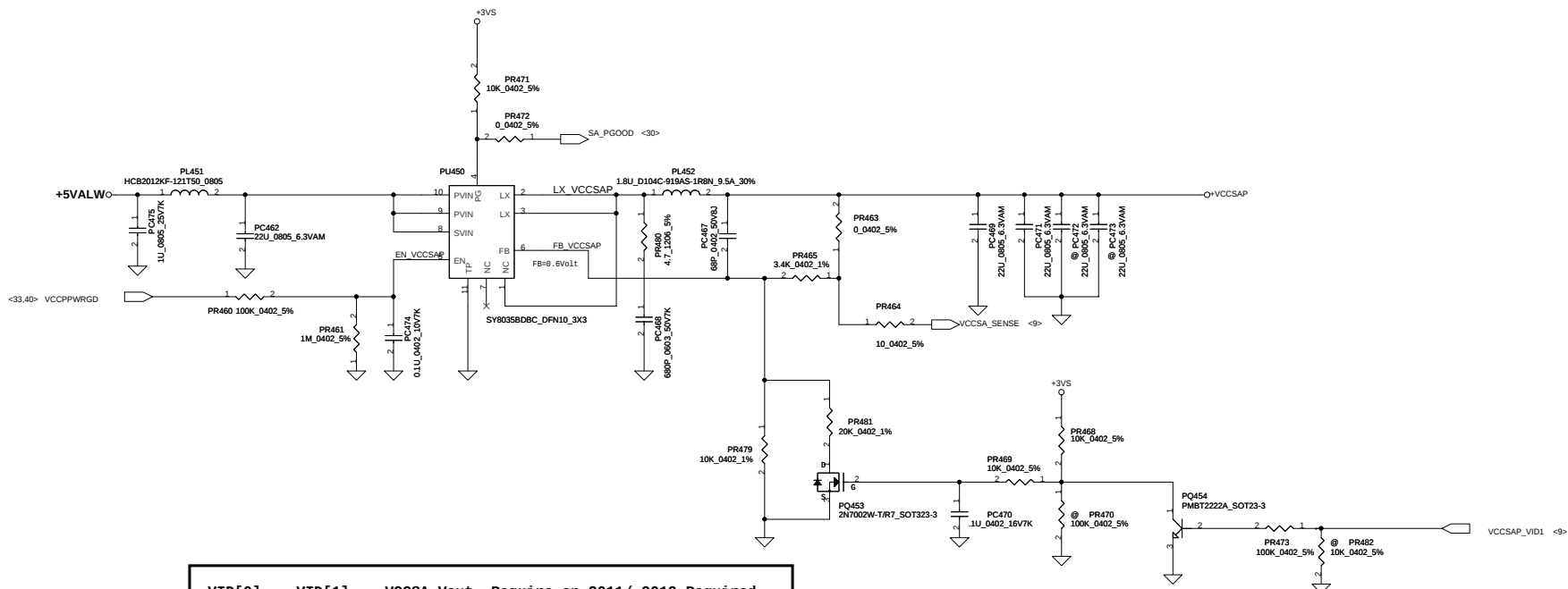
PH1 under CPU botten side :
CPU thermal protection at 95 degree C
Recovery at 56 degree C



Adapter	Throttle Watt	Recovery Watt	Throttle Point	Recovery Point
65W_UMA	71.25W	62.4W	1.48V	1.308V
75W_DIS	85.5W	72W	1.78V	1.5V
75W_QCore	85.5W	72W	1.78V	1.5V



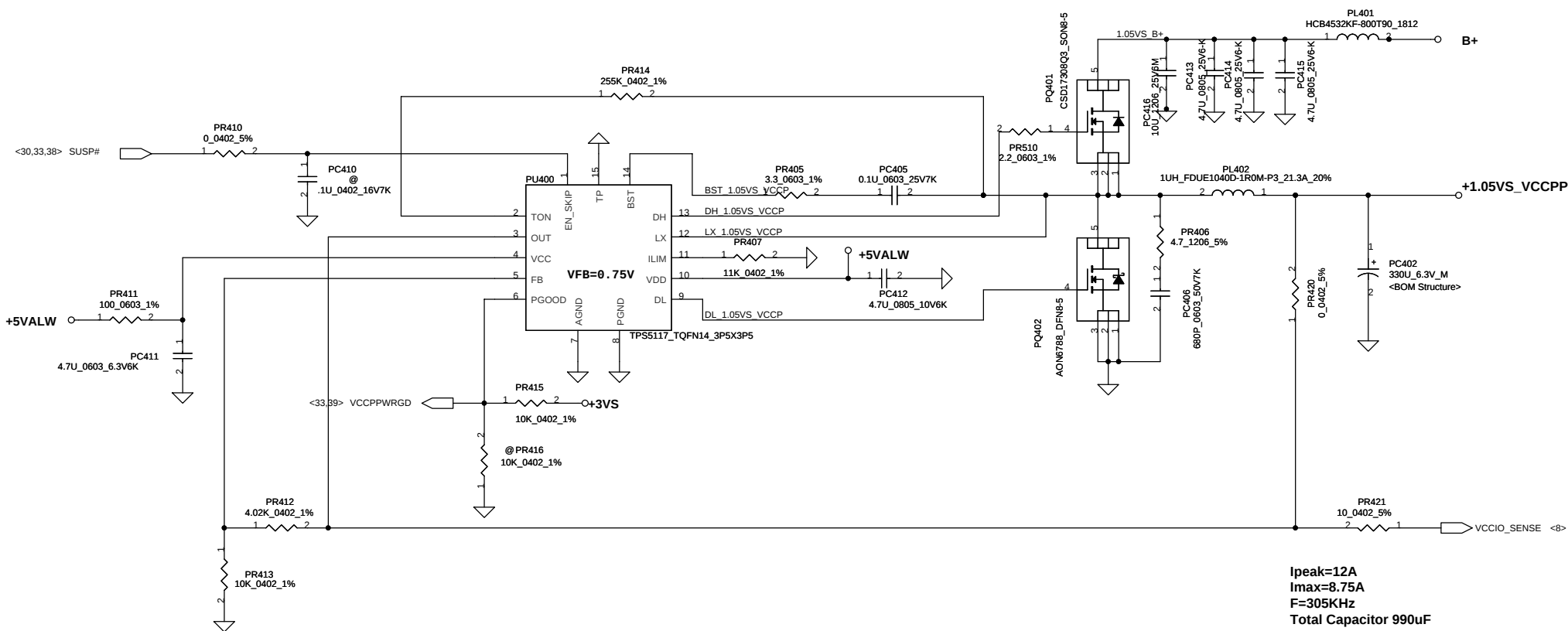




VID[0]	VID[1]	VCCSA Vout	Require on 2011/ 2012	Required
0	0	0.9 V	Yes/Yes	
0	1	0.8 V	Yes/Yes	
1	1	0.75V	No/Yes	
1	1	0.65V	No/Yes	

Note: Use VCCSA_SEL to switch High & Low Level for VID[1]
(ie. VCCSA_SEL) due to the VID[0] is don't care for this setting.

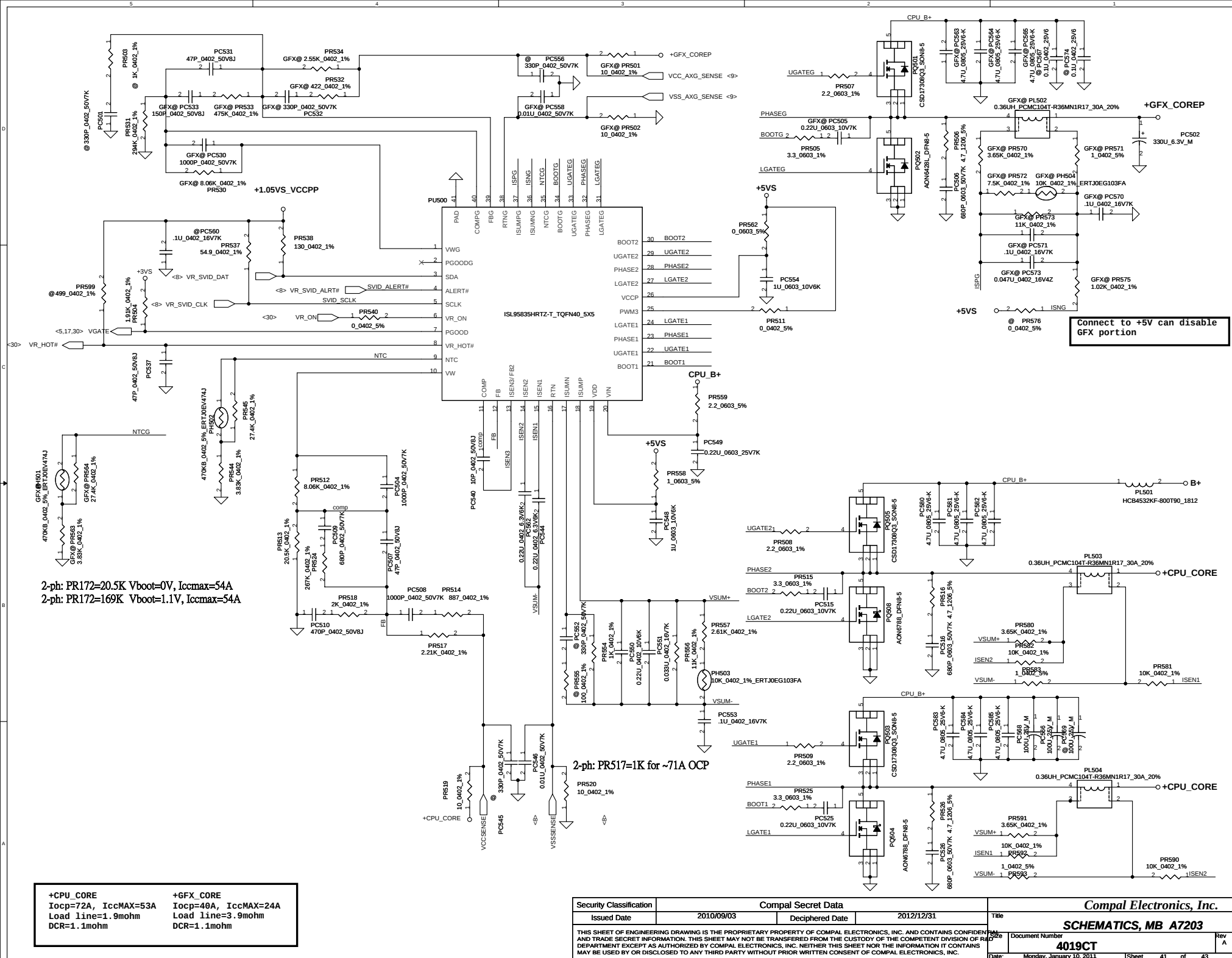
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Ipeak=12A
 Imax=8.75A
 F=305KHz
 Total Capacitor 990uF

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2-ph: PR172=20.5K Vboot=0V, Iccmax=54A
2-ph: PR172=169K Vboot=1.1V, Iccmax=54A

2-ph: PR517=1K for ~71A OCP

Connect to +5V can disable
GFX portion

+CPU_CORE	+GFX_CORE
Iocp=72A, IccMAX=53A	Iocp=40A, IccMAX=24A
Load line=1.9mohm	Load line=3.9mohm
DCR=1.1mohm	DCR=1.1mohm

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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	2010/04/20	P36-P45	Release	

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HW PIR (Product Improve Record)

PWWHA LA-7203P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1
GERBER-OUT DATE: 2011/01/04
NO DATE PAGE MODIFICATION LIST

PURPOSE

1) 12/29 33 Co-lay KB9012 with KB930, only change pin 118 For new EC design

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