

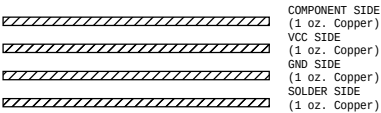
Model Name: 8I915G PRO REV2.1

SHEET TITLE

01	COVER SHEET
02	BLOCK DIAGRAM
03	BOM & PCB MODIFY HISTORY
04	P4_LGA775_A
05	P4_LGA775_C
06	P4_LGA775_B
07	P4_LGA775_D, E, F, G
08	VCORE POWER
09	GMCH-GRANTSDALE_HOST
10	GMCH-GARNTSDALE_DDR
11	GMCH-GRANTSDALE_PCI E, DMI
12	GMCH-GRANTSDALE_INT VGA
13	GMCH-GRANTSDALE_GND
14	GMCH-GRANTSDALE_PWR
15	DDR CHANNEL A
16	DDR CHANNEL B
17	DDR TERMINATION
18	PCI EXPRESS*16 SLOT
19	ICH6 PCI, USB, DMI, LAN
20	ICH6 IDE, GPIO, SATA, CTRL
21	ICH6 VCC, GND
22	CLK GEN

SHEET TITLE

23	PCI SLOT 1
24	PCI EXPRESS*1 SLOT 1, 2
25	ITE8712HX
26	HWM0/SMART_FAN/PROCESSOR_HOT
27	KB_MS/GAME
28	COM/LPT/FDD
29	(FRONT+REAR)USB/RING/IDE
30	AZALIA CODEC ALC880/CMI9880
31	REAR AUDIO JACK
32	FRONT AUDIO CONNECTOR
33	MARVELL 88E8001 LAN
34	ATX POWER CONN./DUAL BIOS
35	DISCRETE POWER
36	TI TSB43AB23 1394A
37	FRONT PANEL/CURRENT_OUT
38	RAID IT8212 (1)
39	RAID IT8212 (2)
40	GPIO CONFIGURATION
41	GPIO & RESET CONFIGURATION



GIGABYTE

Title

Cover Sheet

Size Custom

Document Number

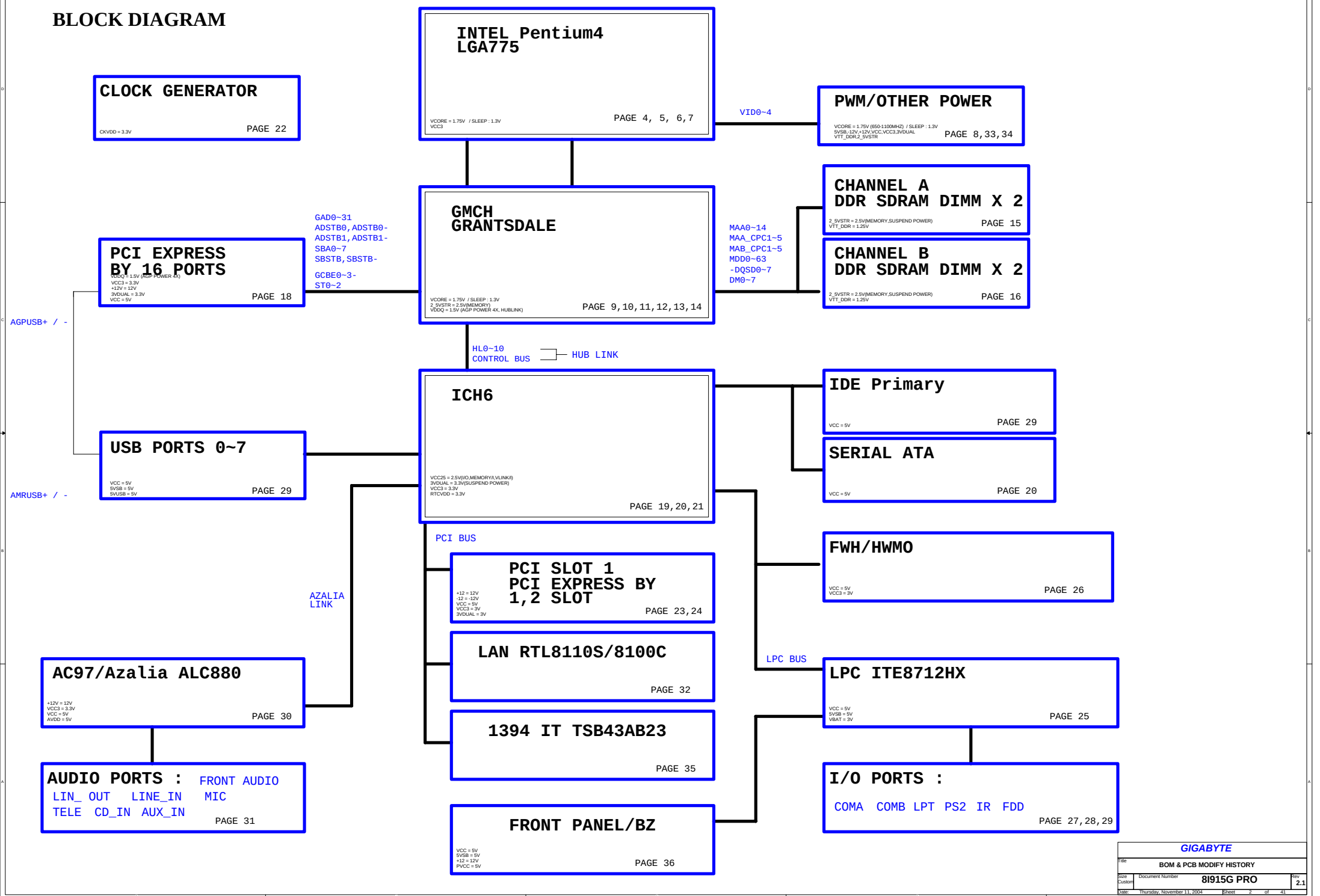
8I915G PRO

Rev 2.1

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BLOCK DIAGRAM



Model Name: 8I915G PRO

Component value change history

2003/12/12

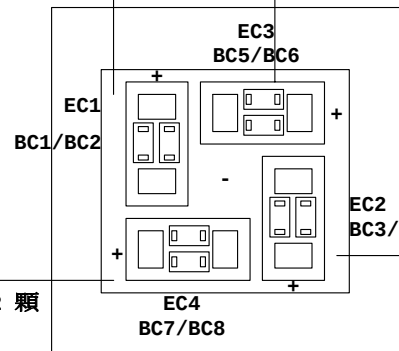
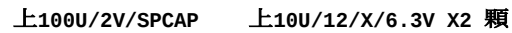
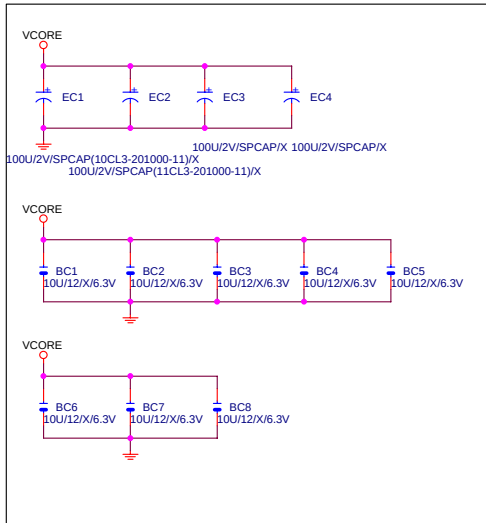
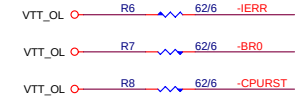
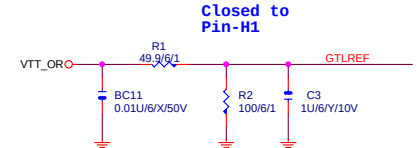
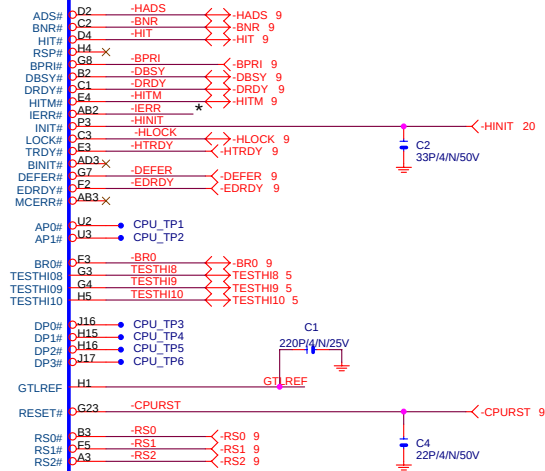
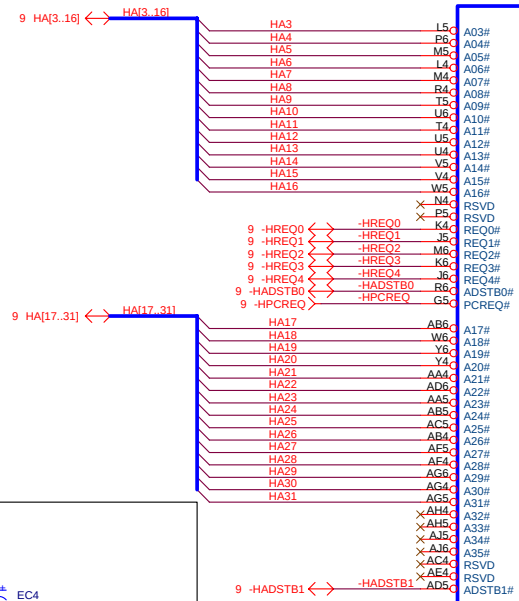
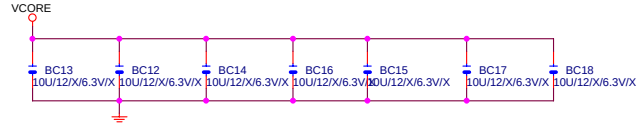
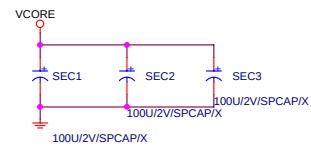
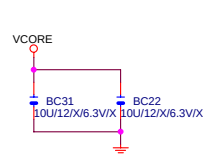
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Circuit or PCB layout change for next version

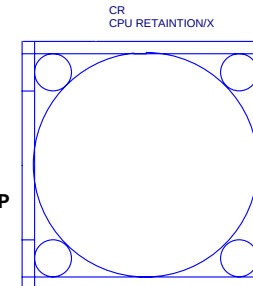
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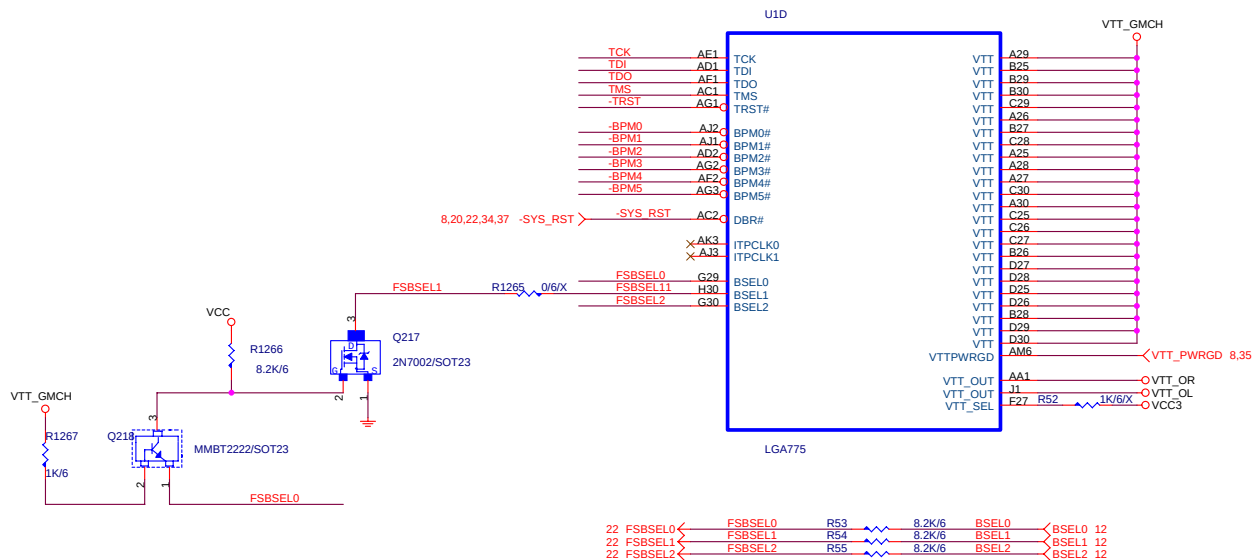
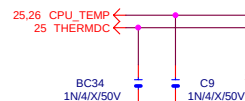
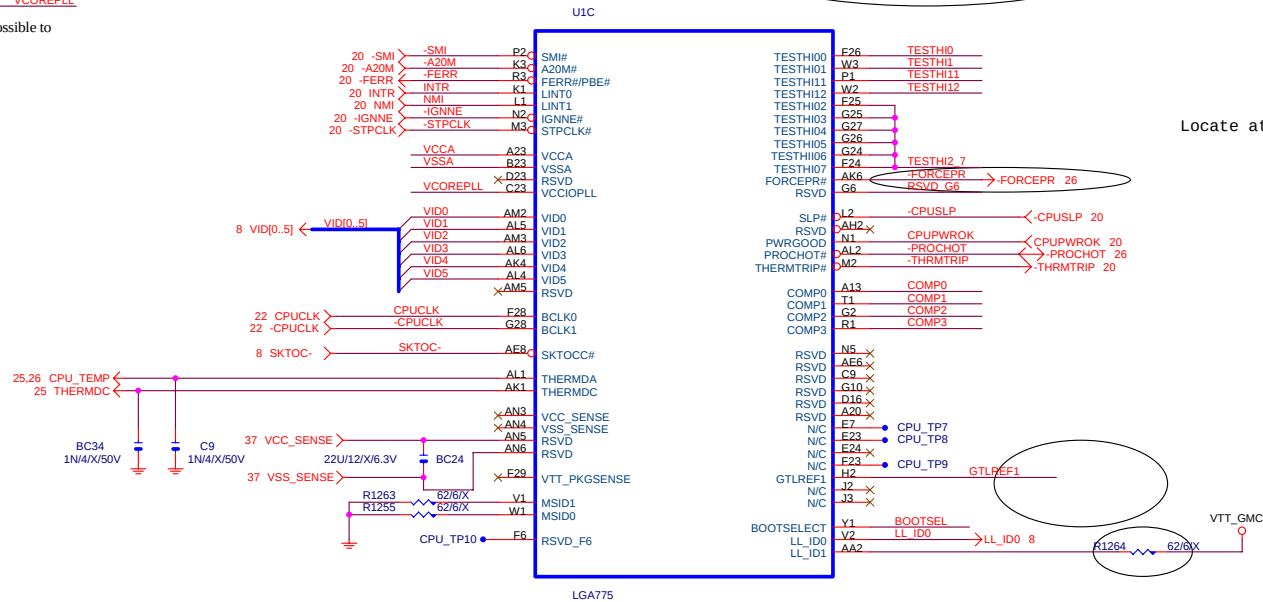
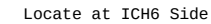
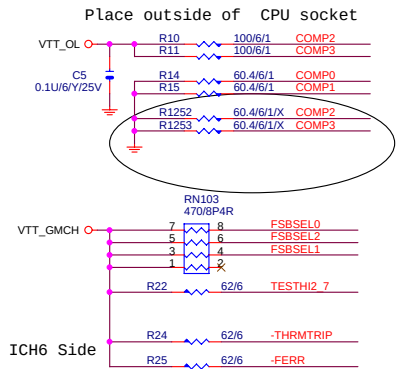
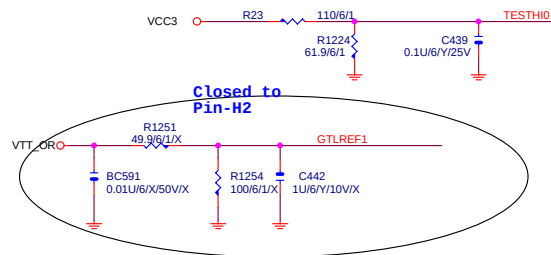
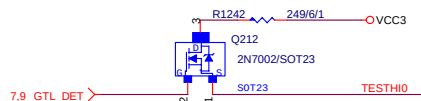
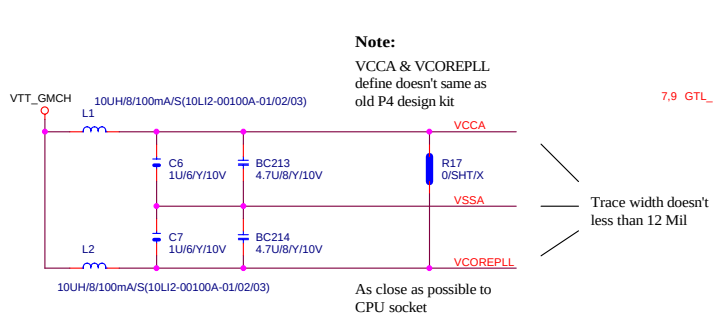
GIGABYTE			
Title BOM & PCB MODIFY HISTORY			
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SP-CAP X 4PCS

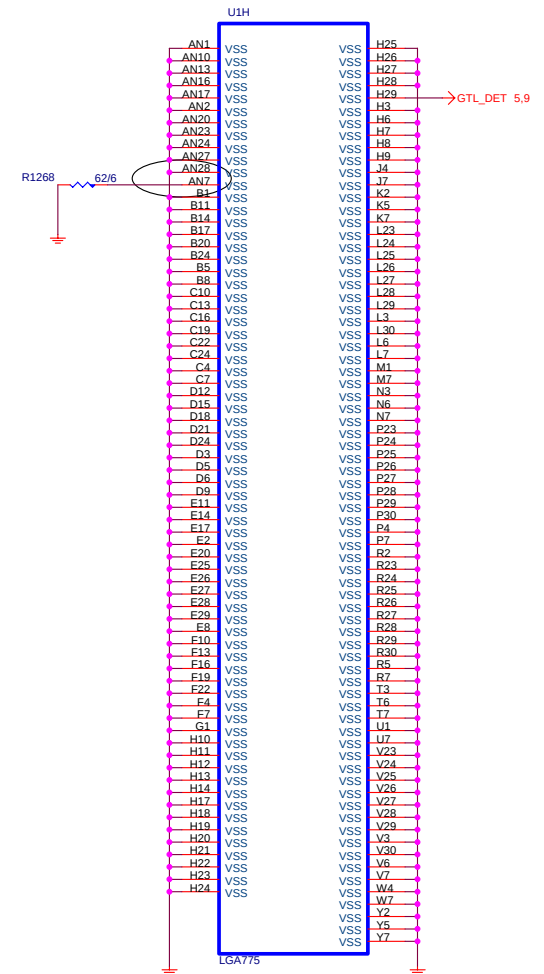
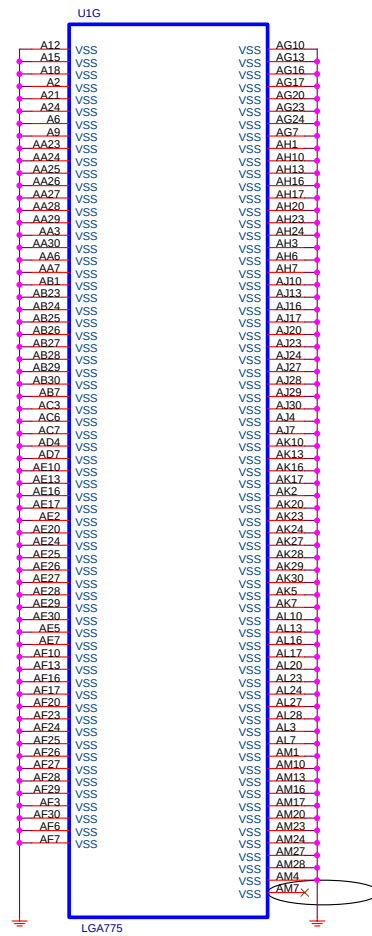
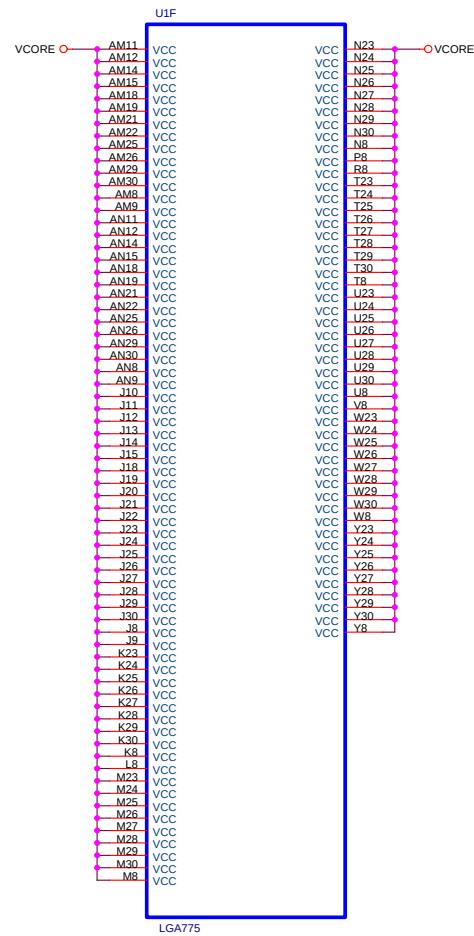
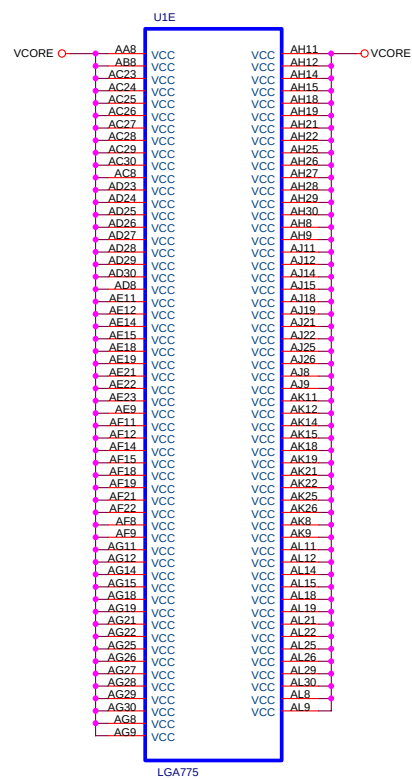


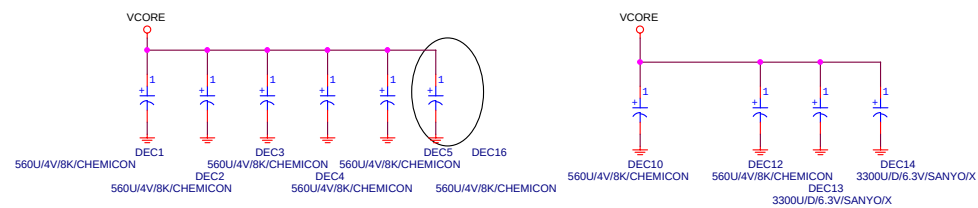
– 上100U/2V/SPCAP











DD1 :在HIGH SIDE 發生S-D SHORT 時(OVP), LOW SIDE MOSFET TURN ON ,讓Vcore 降壓,同時V12 也會下降6~7V以下時,造成PWM 無法提供POWER TO LOW SIDE TURN ON,所以加DD1 延長PWM POWER 提供給LOW SIDE MOSFET TURN ON 保護CPU VOLTAGE 過高.

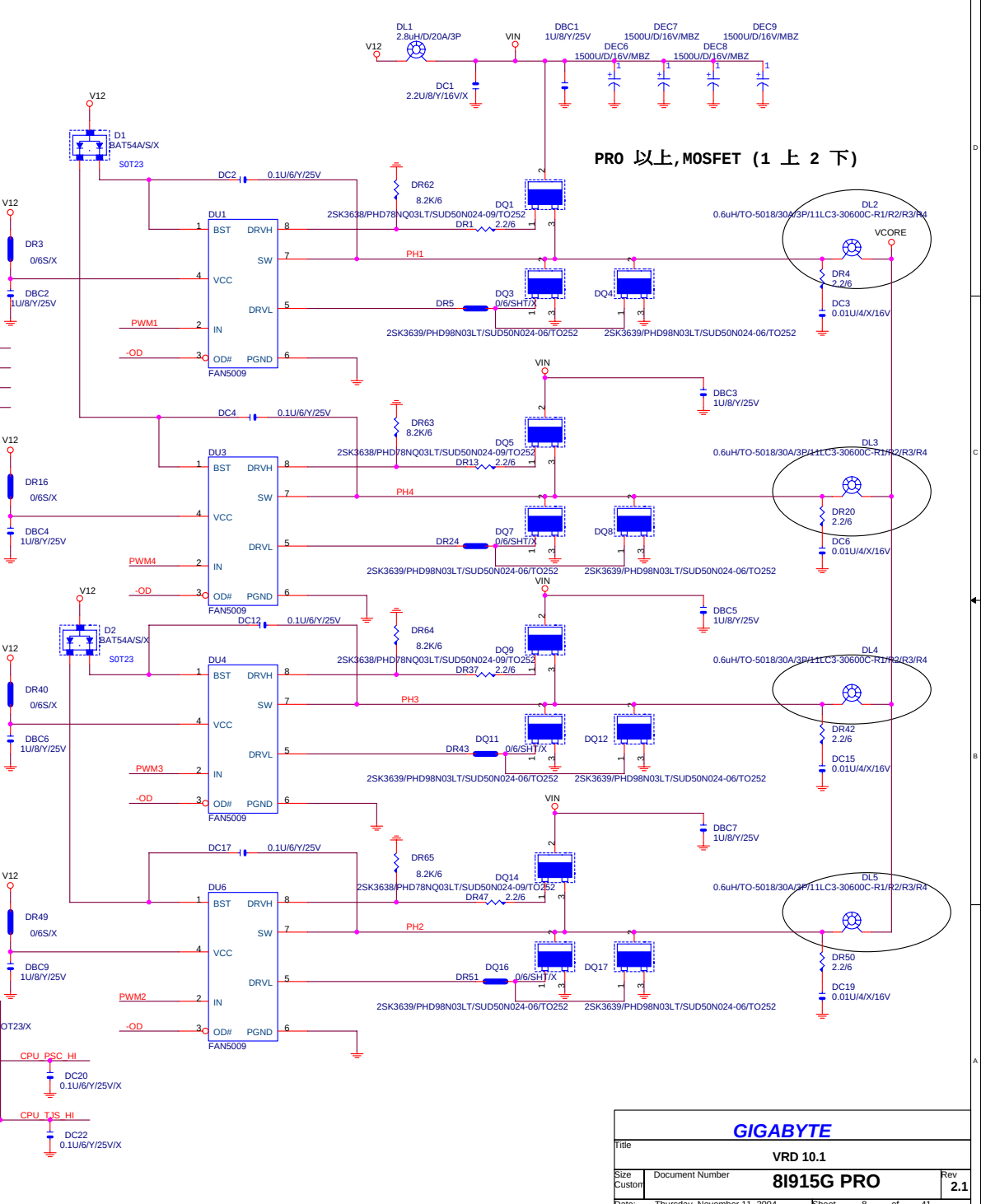
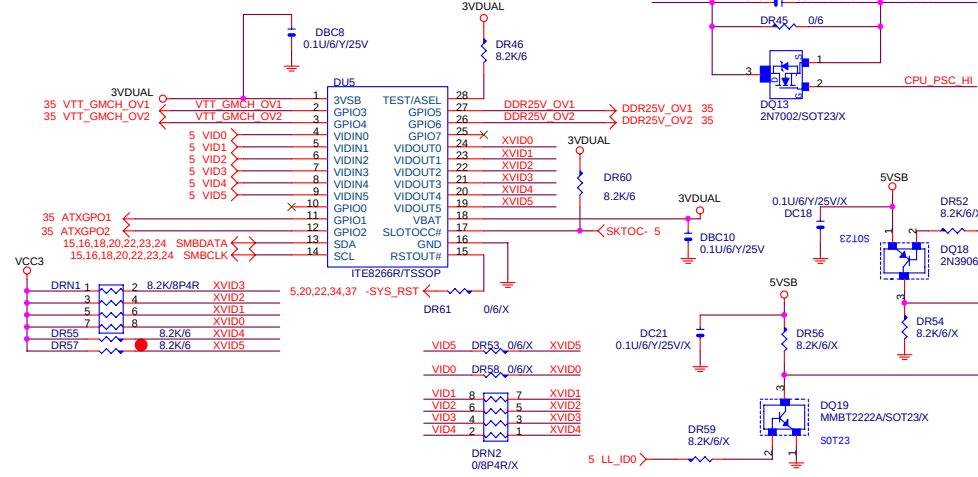
DR9,DC5 FOR V12 OVER 19V 以上, SPEC (18V)

DR12 為一個 CYCLE的DUTY(50%)
DELAY :讓限流時間DELAY (DR35,DC13) 才啟動.
DR39:240K
工作頻率=720KHZ / 4PHASE=180K(1 PHASE)

靠近CPU(Vcore/GND)

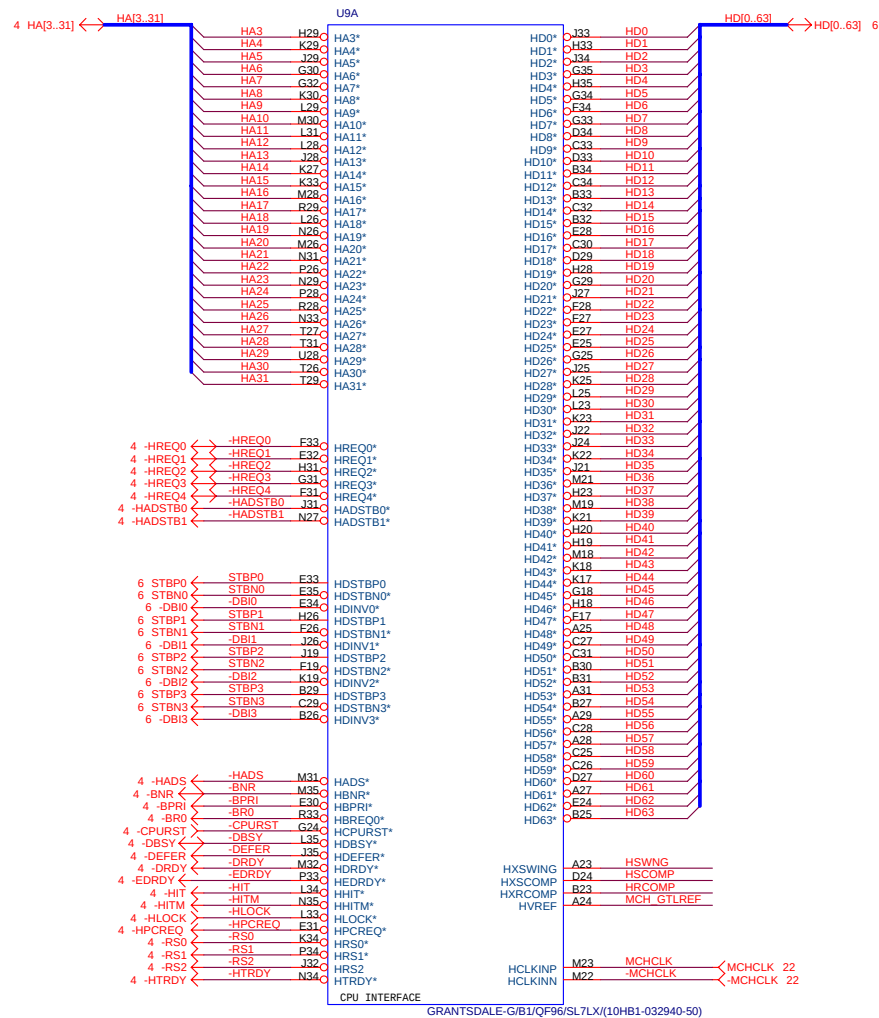
DR41:約200A
DR36 :TRACER 拉到 CHOKE,算出CHOKE 兩端壓降

DR27 放到CHOKE 為溫度補償

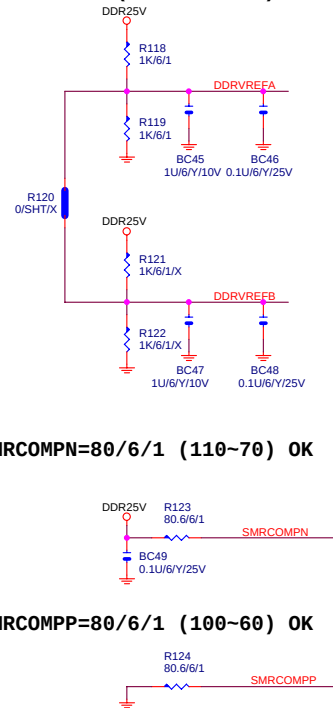


PRO 以上, MOSFET (1 上 2 下)

GIGABYTE			
VRD 10.1			
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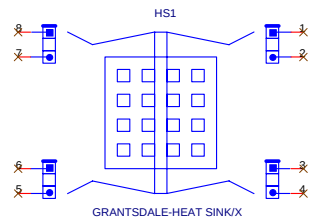
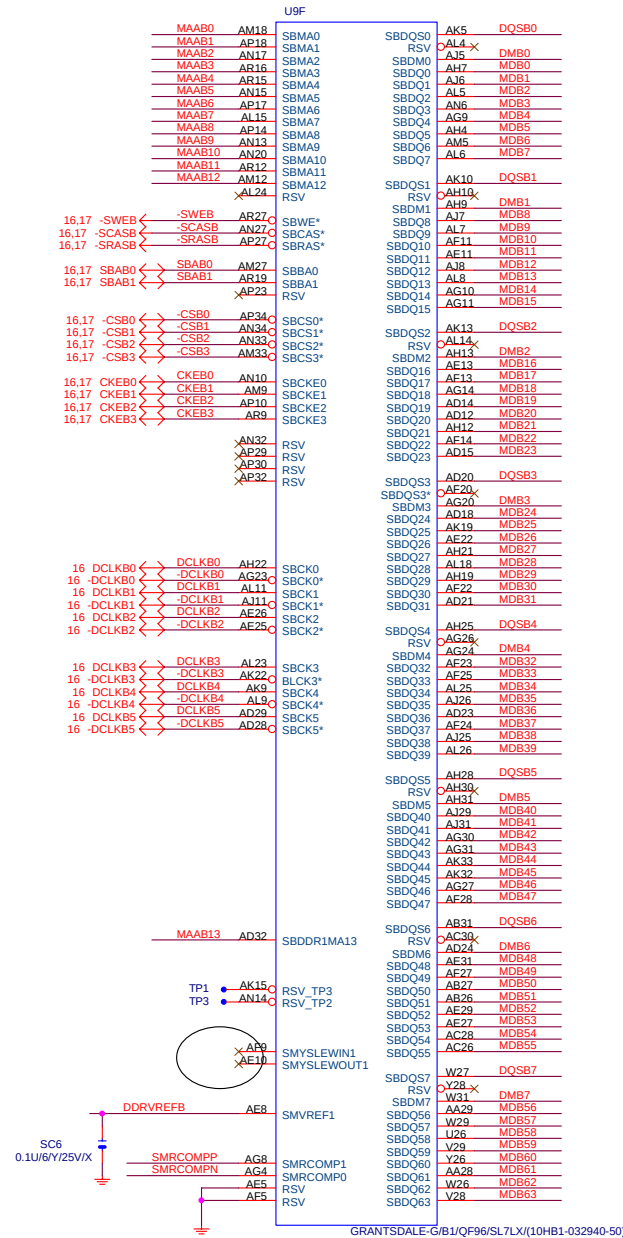
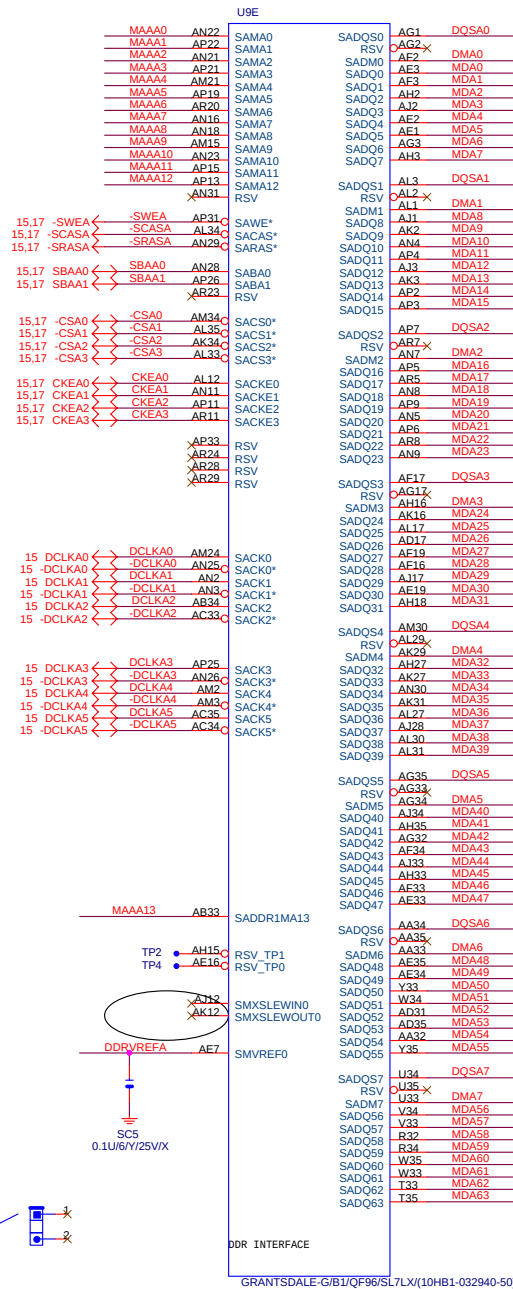
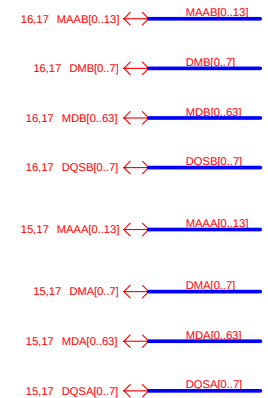


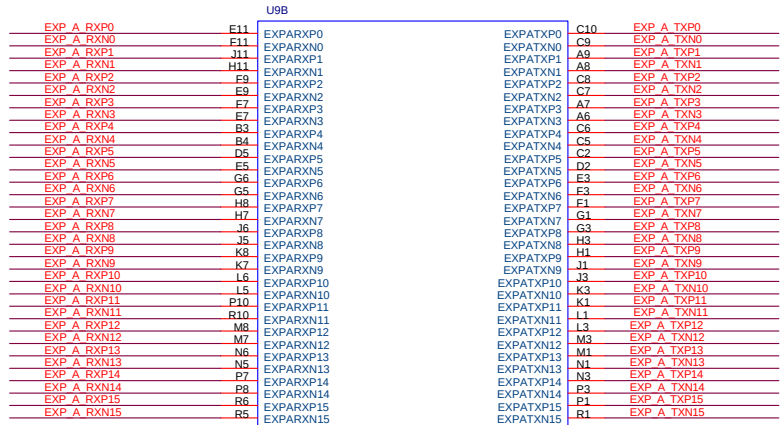
DDRVREFA=1.32V (1.55V~1.15V)OK



SMRCOMPN=80/6/1 (110~70) OK

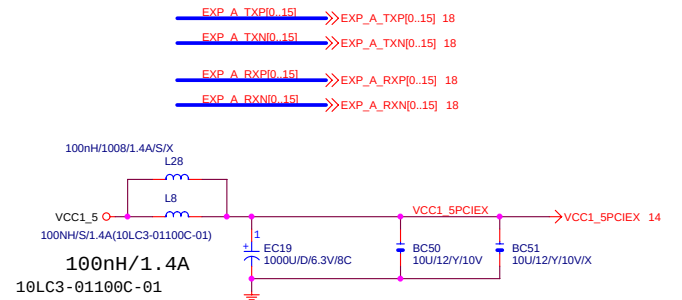
SMRCOMPV=80/6/1 (100~60) OK

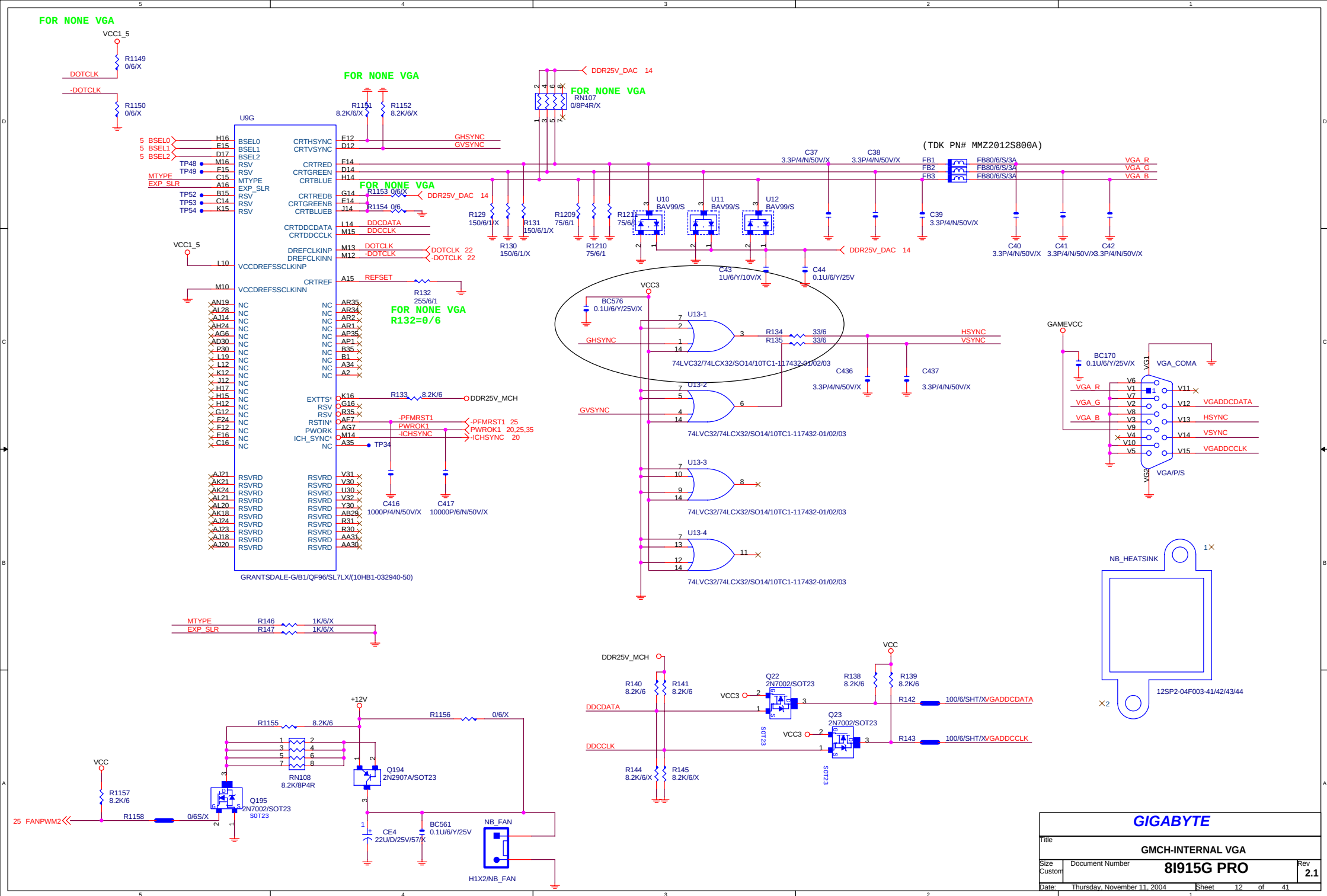


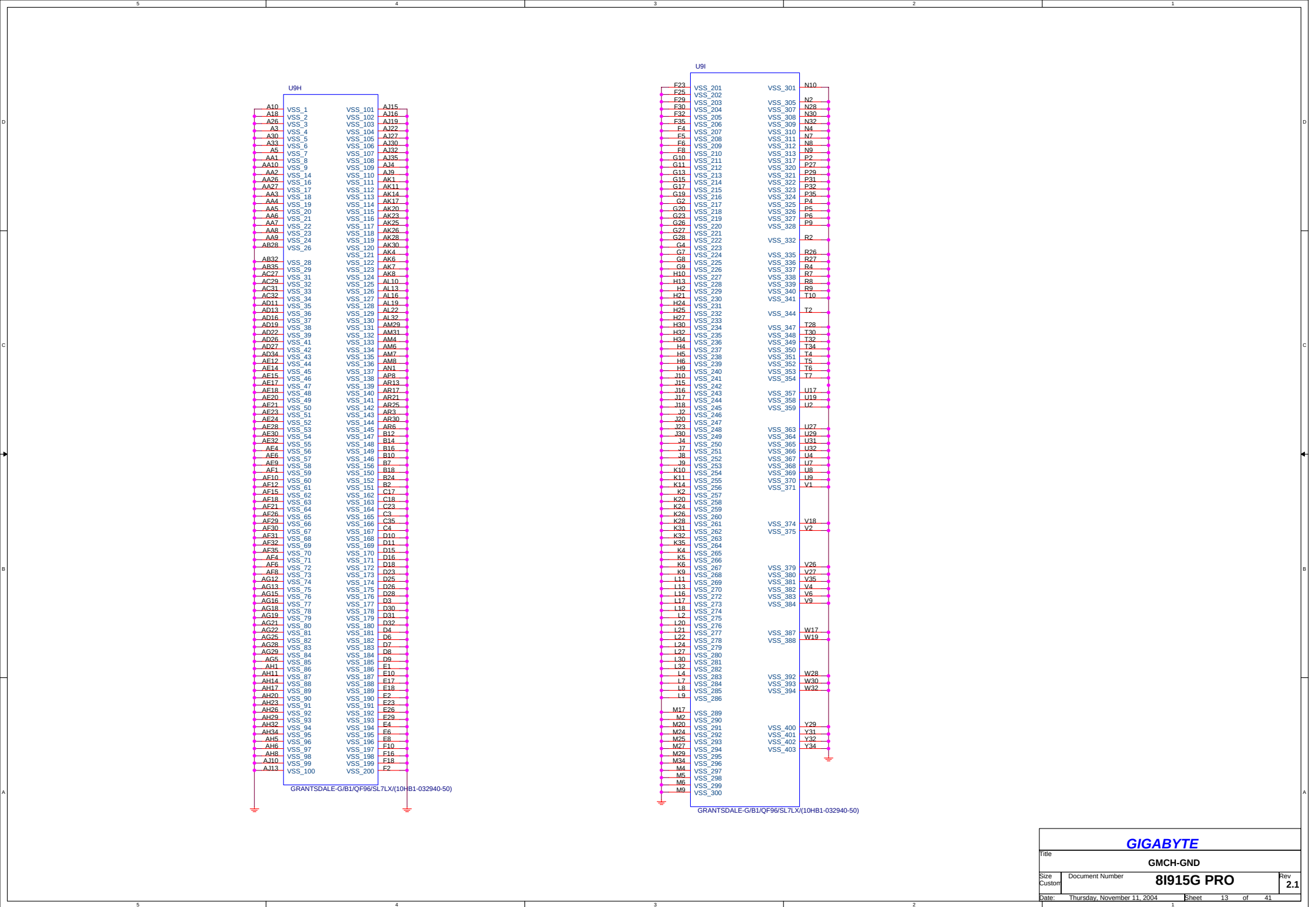


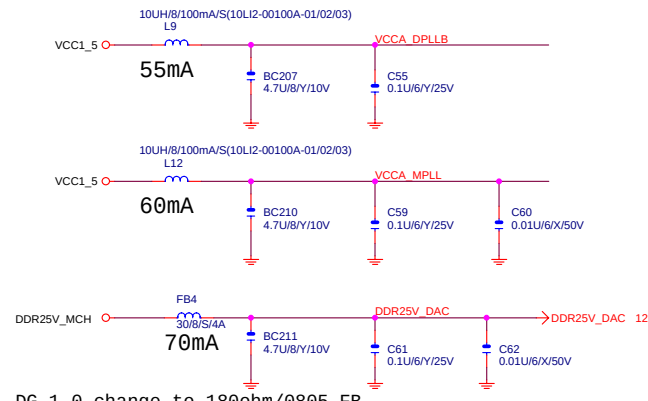
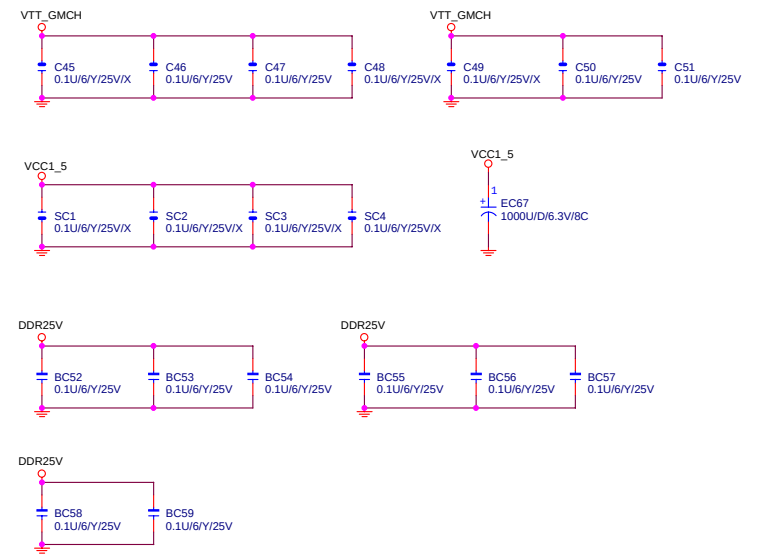
For DVO Function

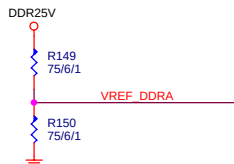
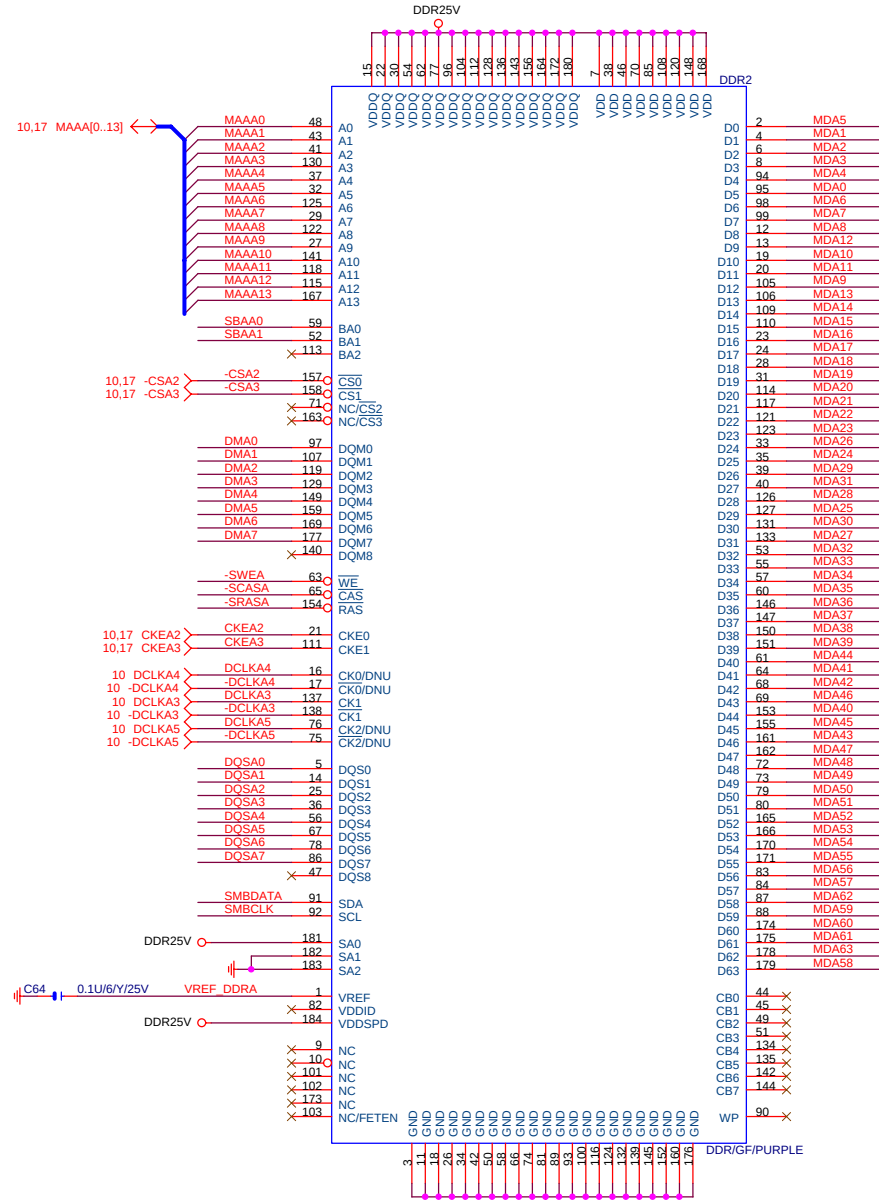
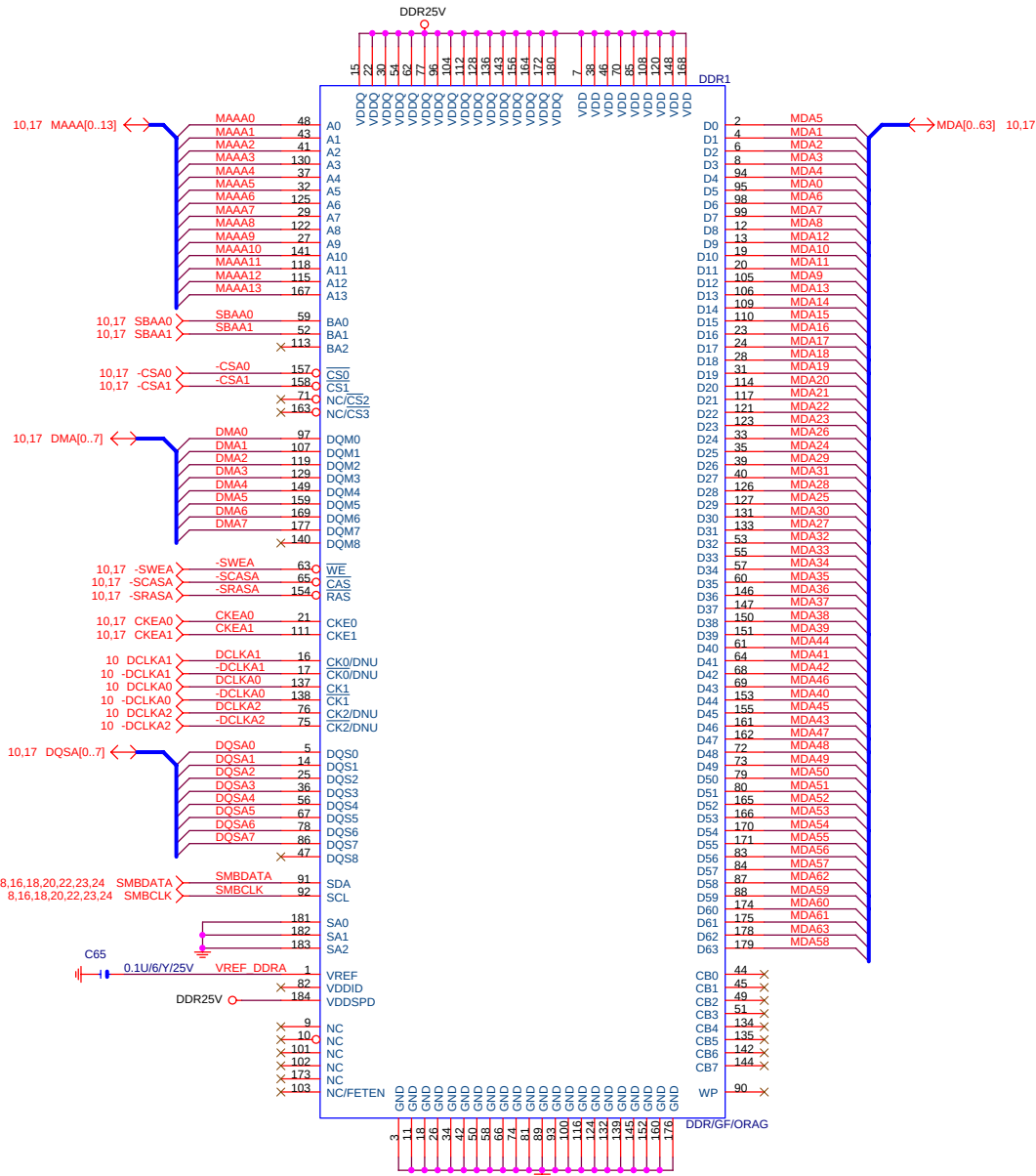
GRANTSDALE-G/B1/QF96/SL7LX(10HB1-032940-50)



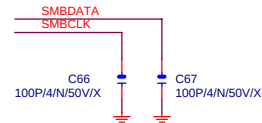


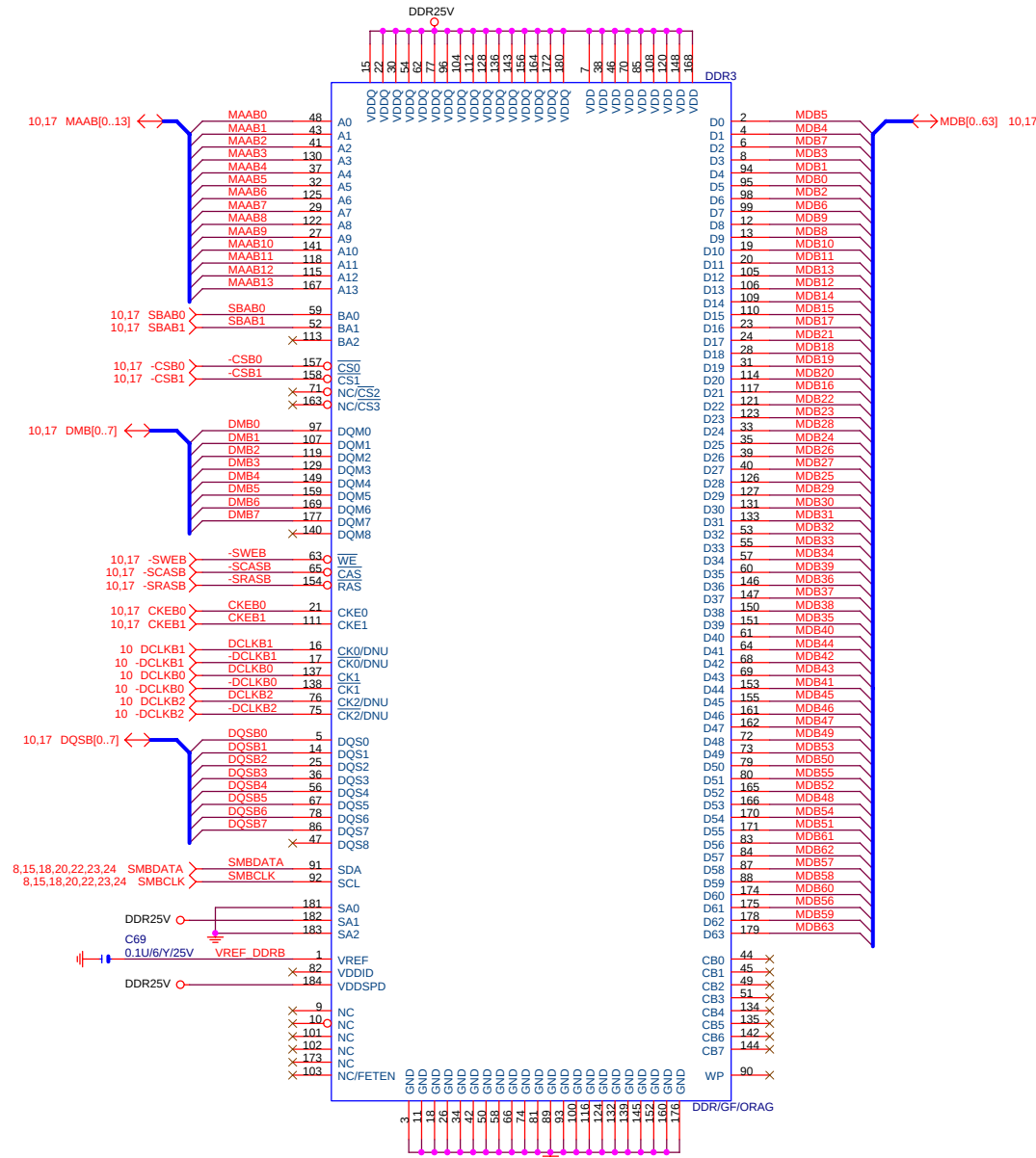






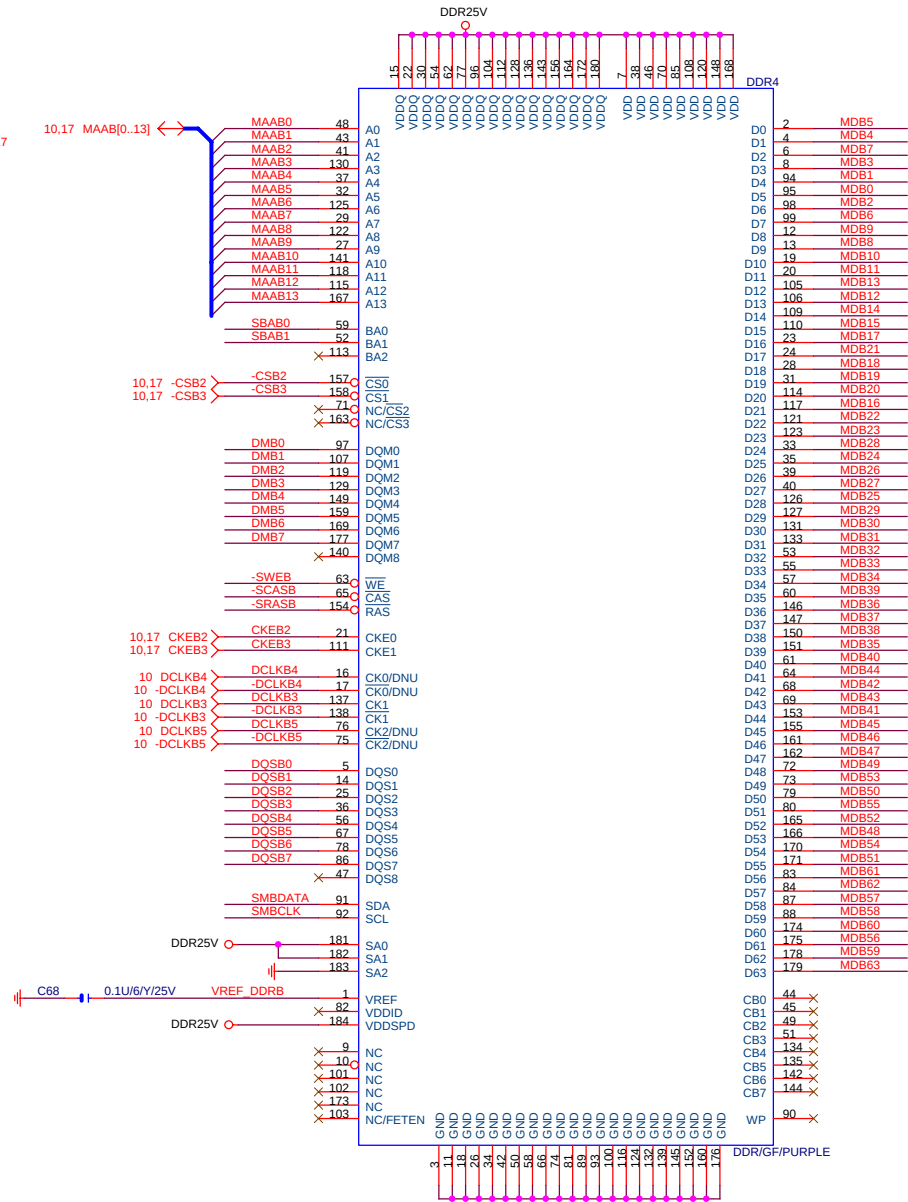
WINBOND 512MX4
B0=1.45V~1.2V OK





WINBOND 512MX4
VREF_DDRB MARGIN
B0=1.40V~1.2V OK
B1=1.45V~1.2V OK

WINBOND 256MX2
VREF_DDRB MARGIN
B1=1.60V~1.0V OK

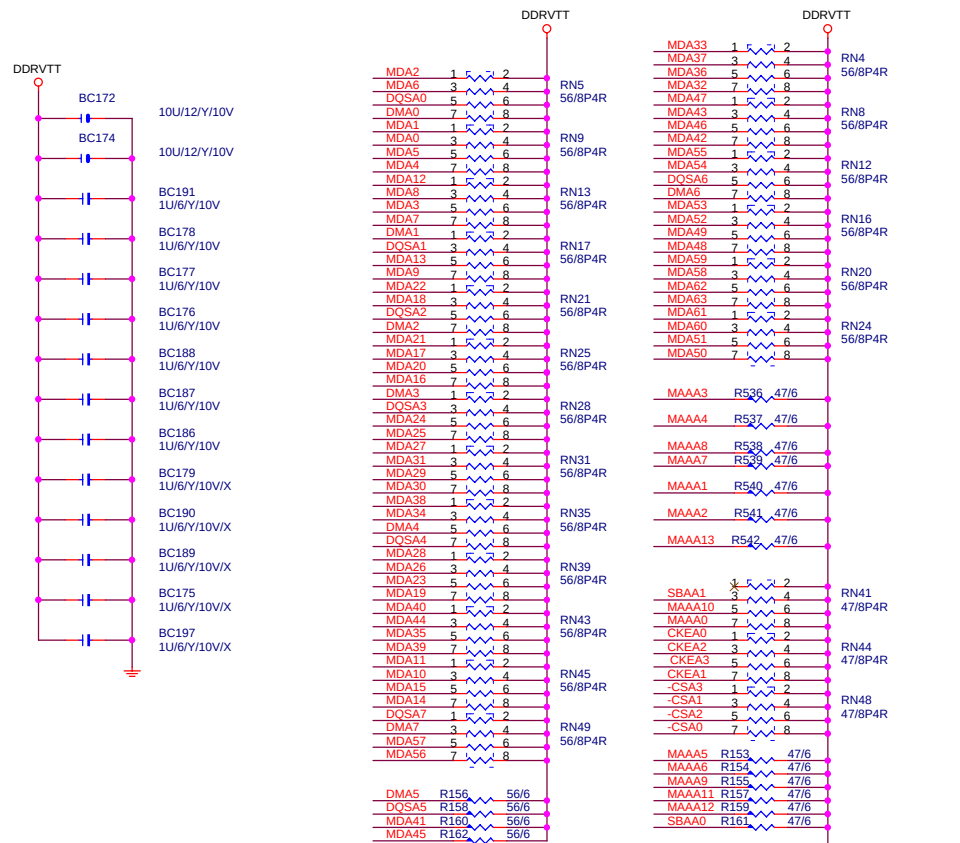


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DDR CHANNEL B

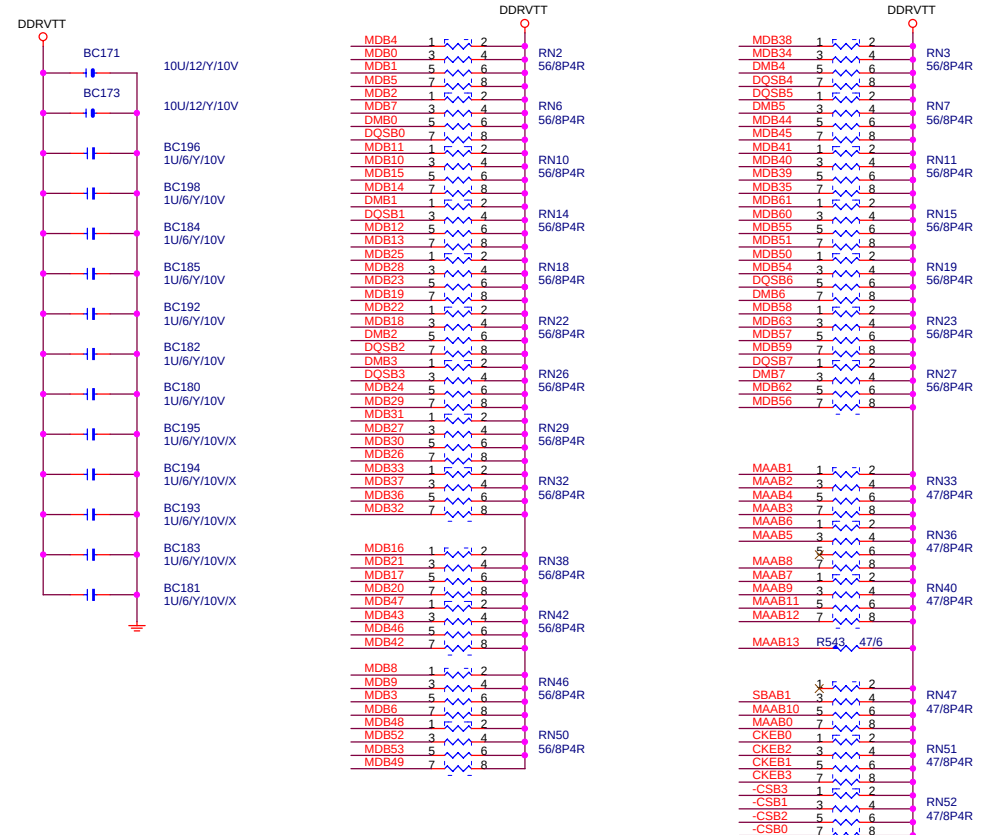
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DDRVTT Decouple



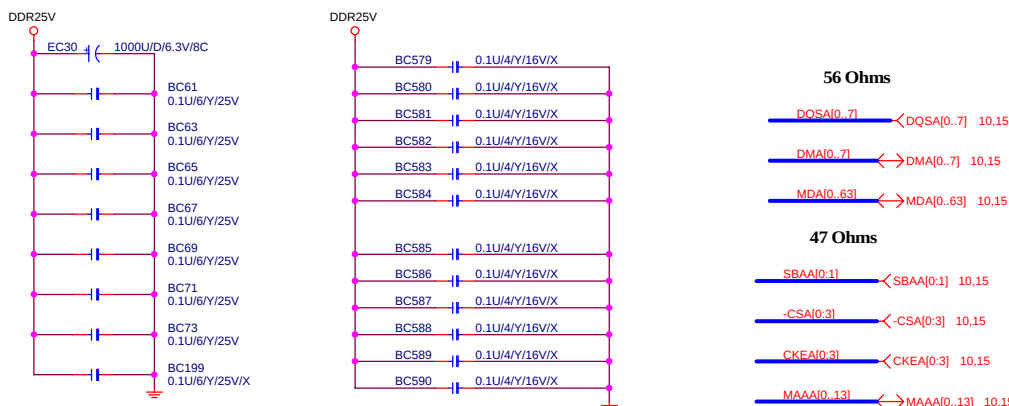
DDR TERMINATION CHANNEL A

DDRVTT Decouple

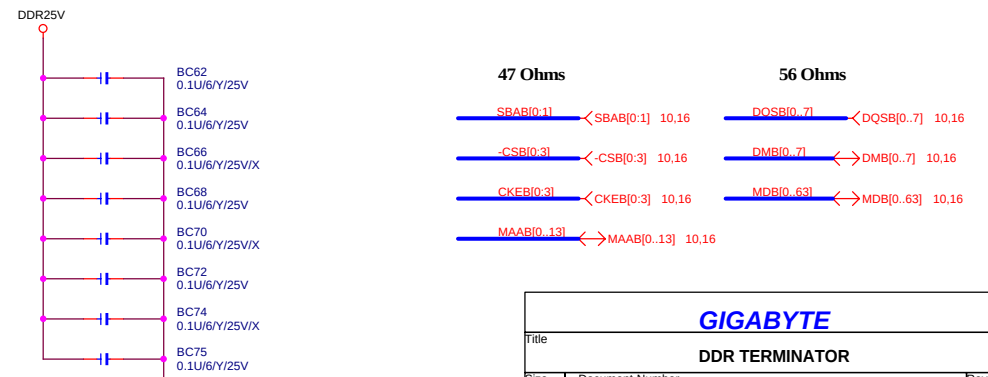


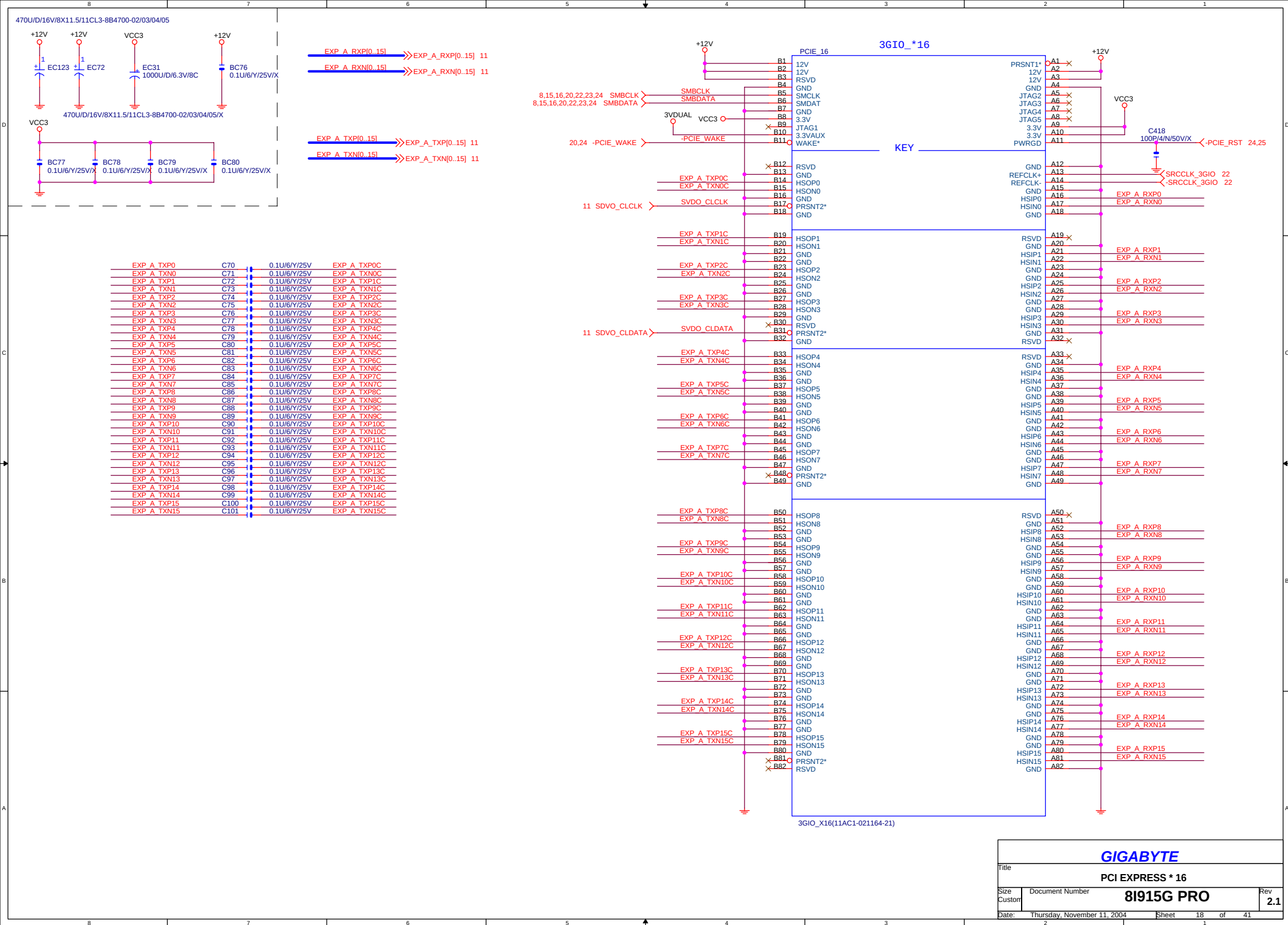
CHANNEL B

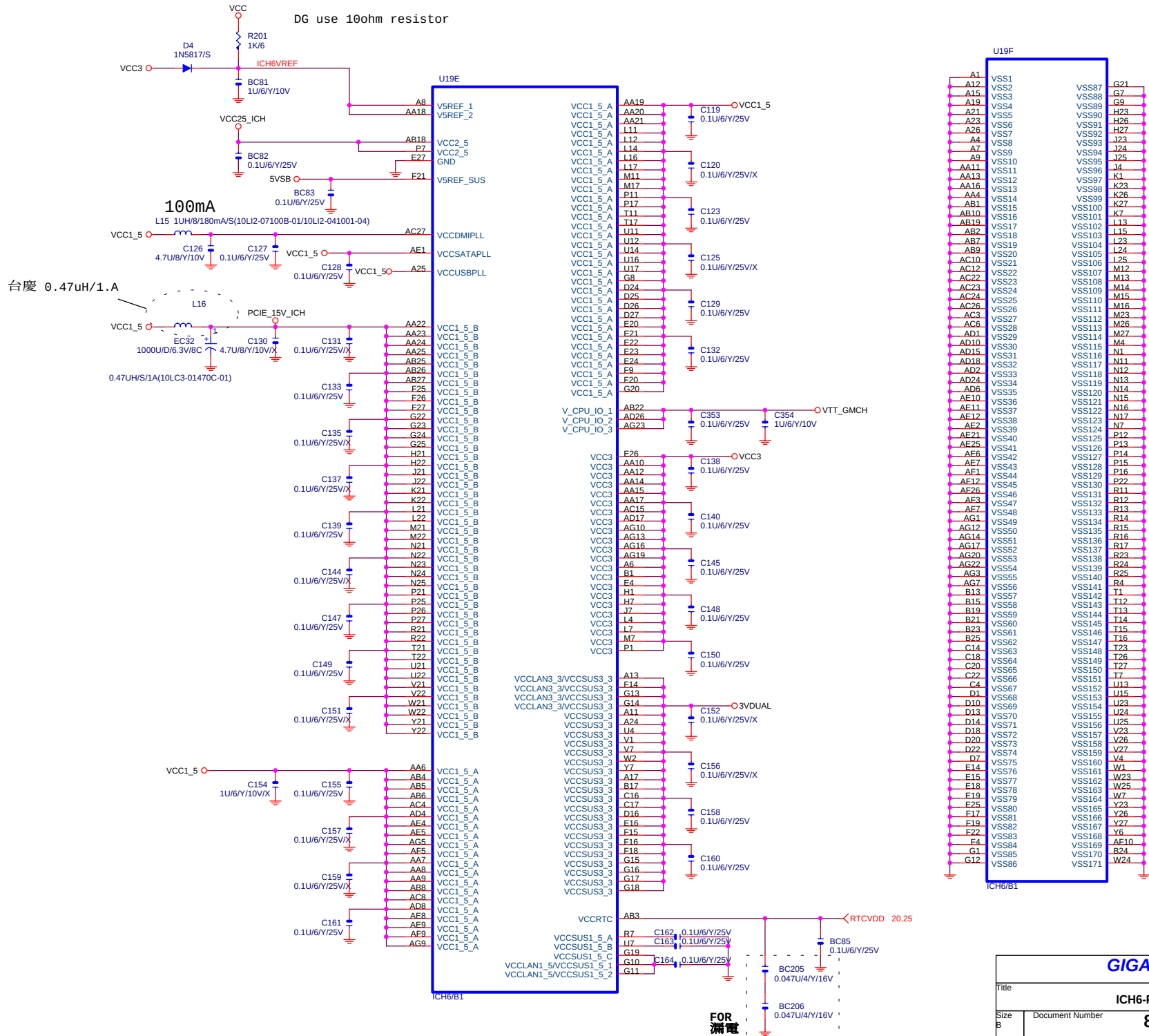
DDR25V Decouple

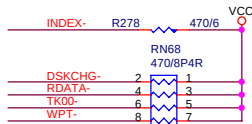


DDR25V Decouple



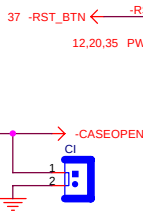




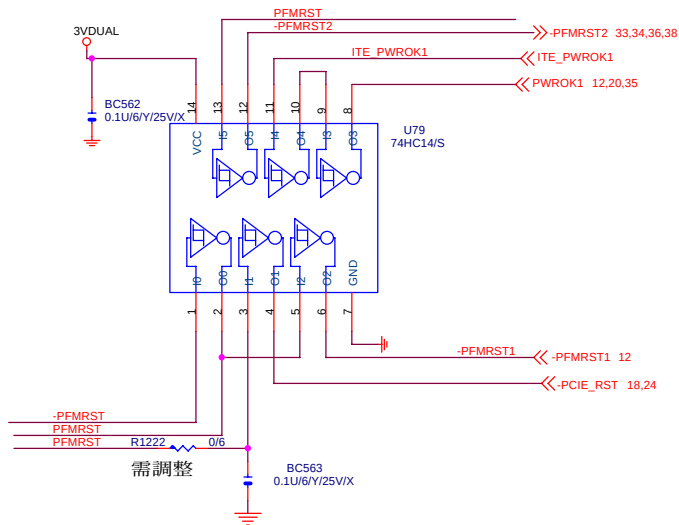


RTS2- ==LOW CPU FAN 50%
==HIGH 100%

DTR2- ==LOW PUSH-PULL
==HIGH EOD



Case Open Circuits
CASE OPEN (N/A)



Have P.U at ICH6 side

INPUT

-PFMRST>> ICH6 TO IT8712/-IDERST
PWROK1>> GD/ICH6/ITE8712

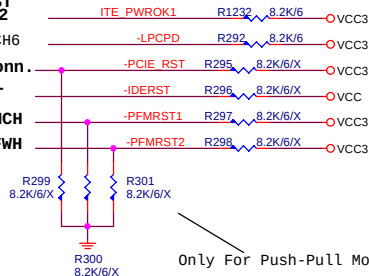
To GMCH & ICH6

To ALL PCI Express Conn.

To IDE Connector

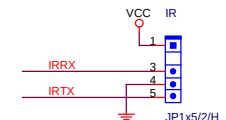
To PCI_EXP(LAN ONBOARD)/SATA/GMCH

To PCI LAN/1394/FWH



Only For Push-Pull Mode

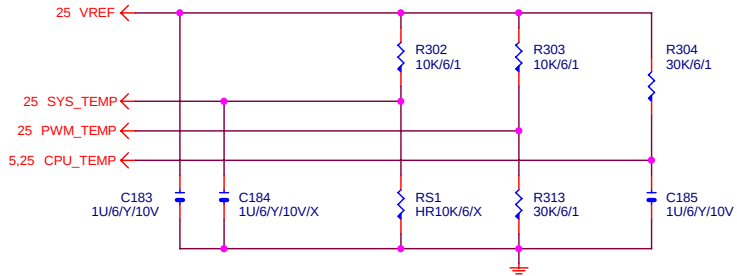
IR CONNECTOR



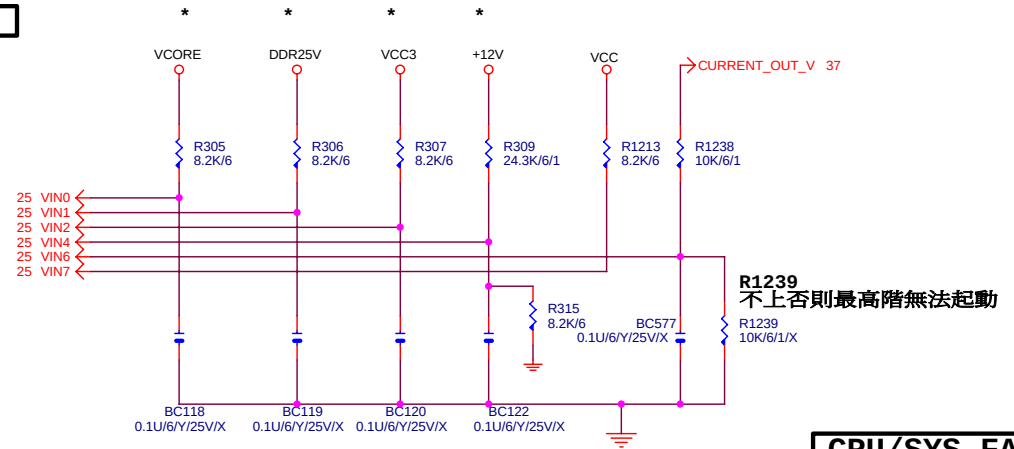
GIGABYTE

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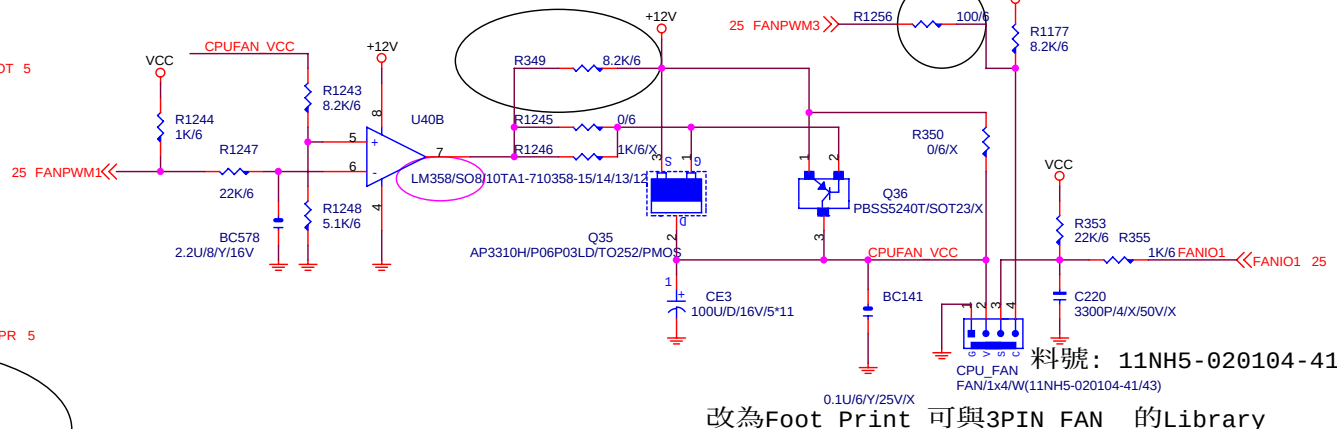
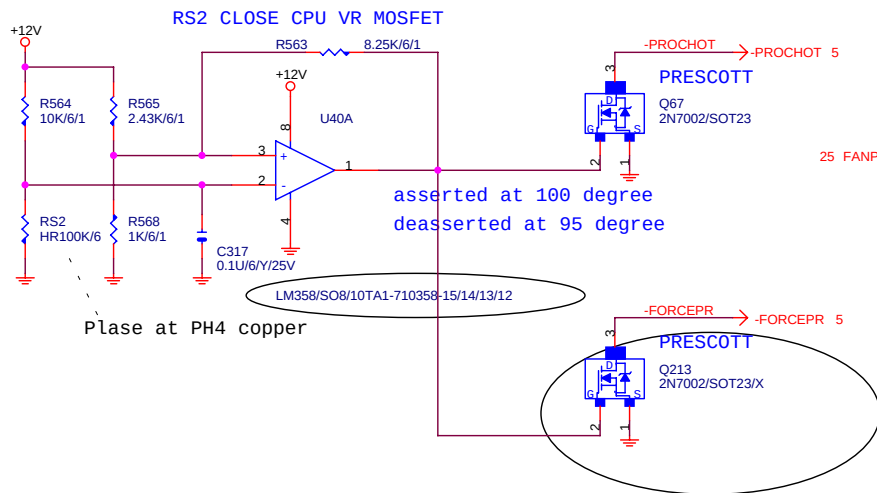
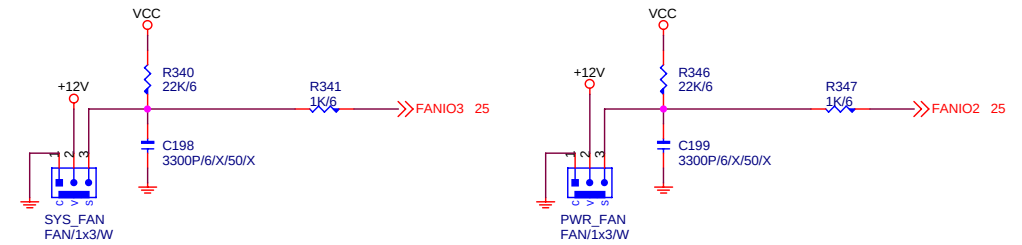
TEMP. SENSE



VOLTAGE SENSE

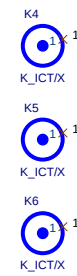
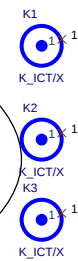
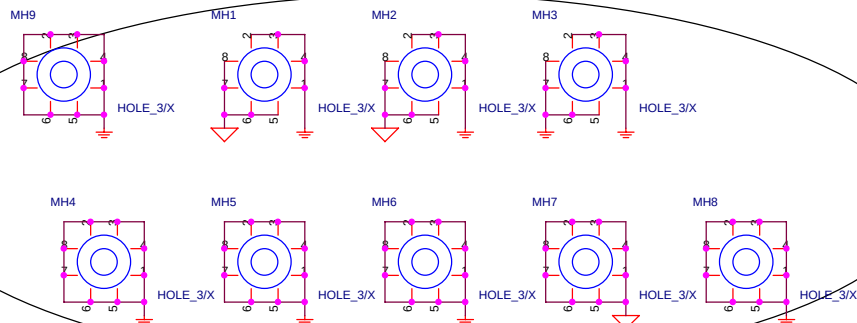
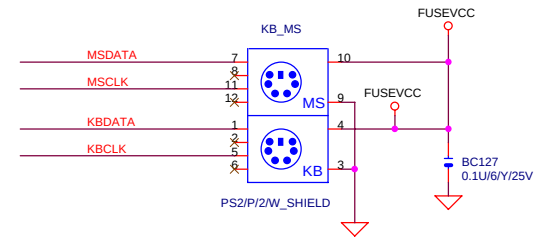
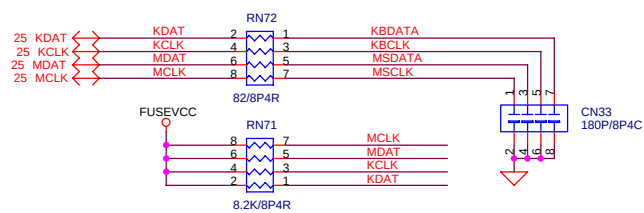


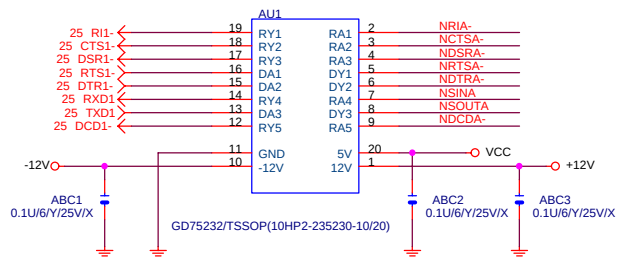
CPU/SYS FAN



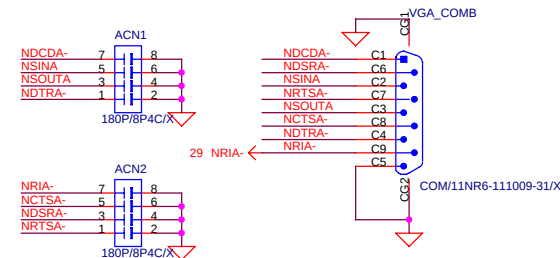
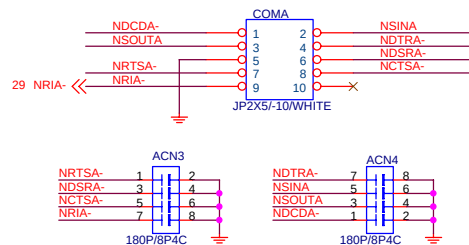
GIGABYTE

Title		
HWM/FAN/CI/BIOS		
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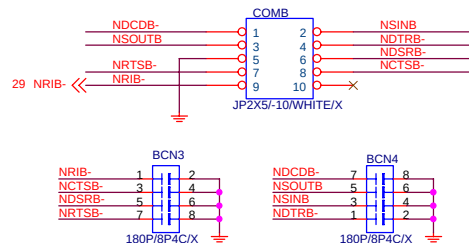
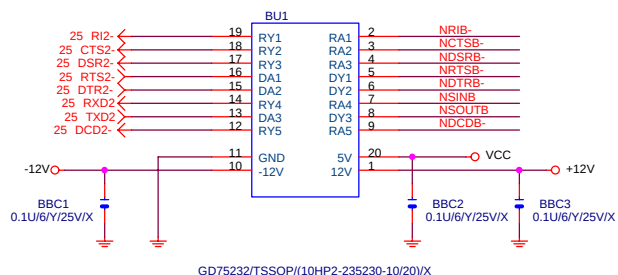
COMA/COMB

INTERNAL COMA

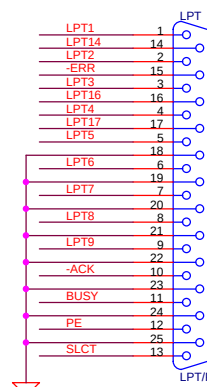
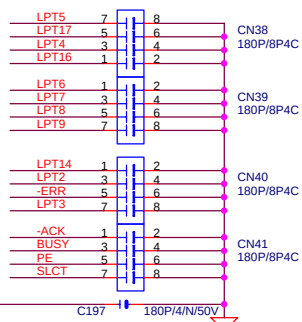
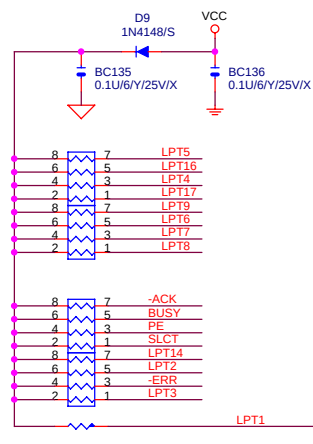
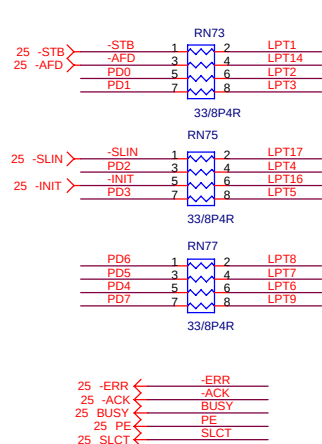


PLACE NEAR VGA_COM CONNECTOR

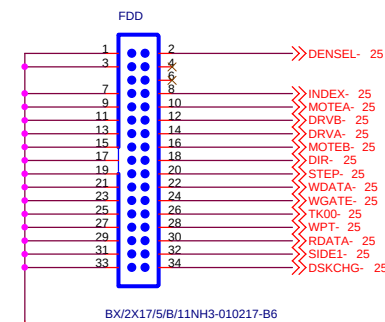
INTERNAL COMB



LPT



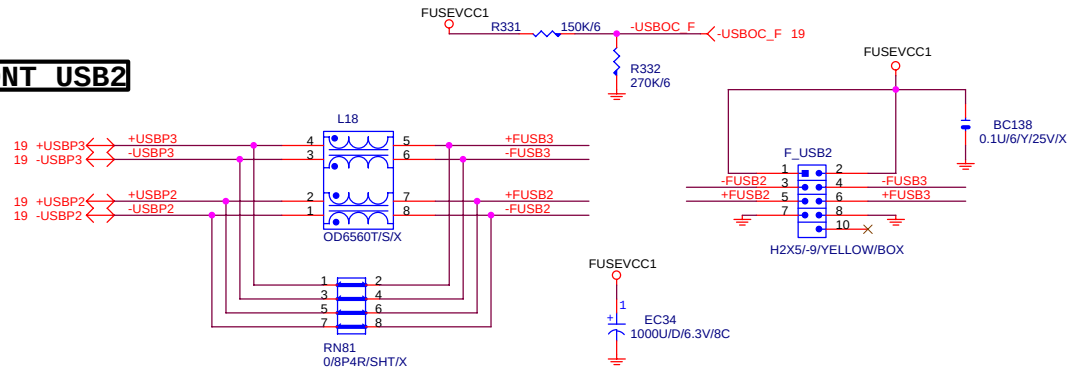
FLOPPY



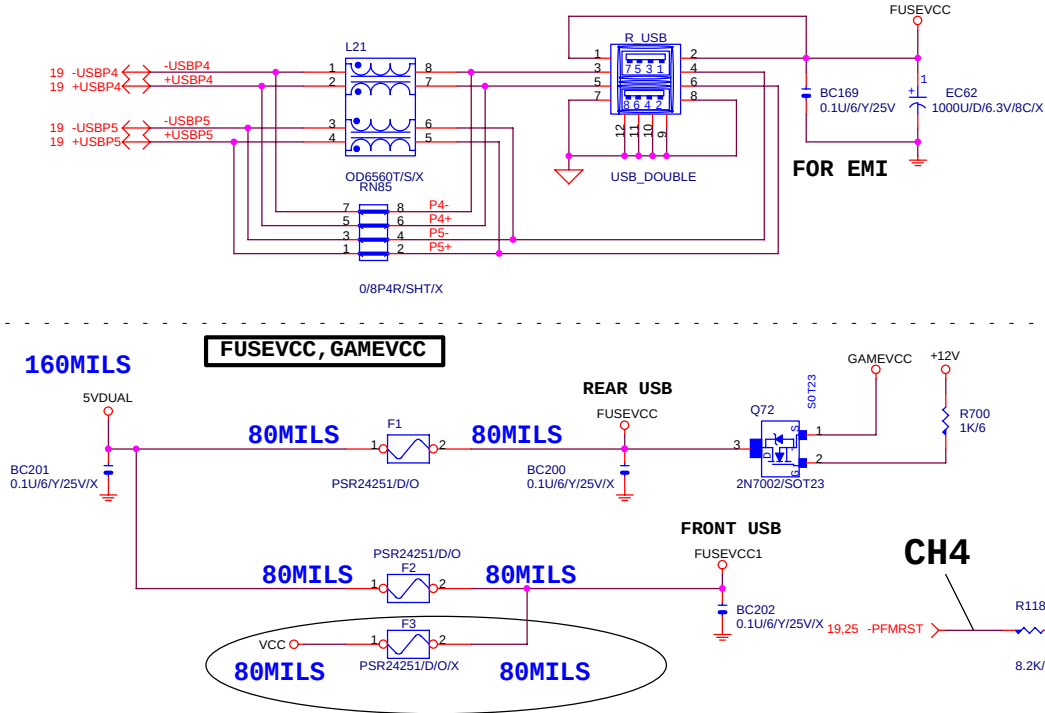
GIGABYTE

Title			
COM, LPT, FDD			
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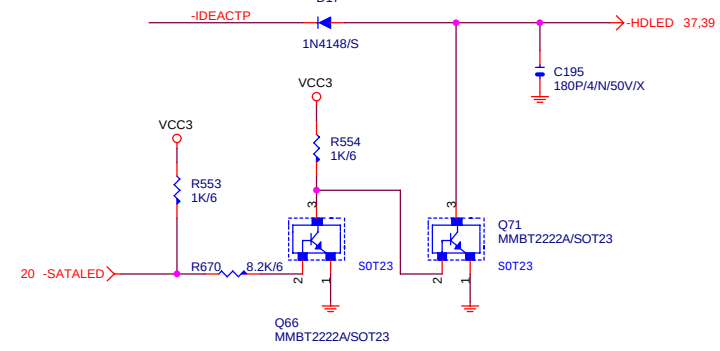
FRONT USB2



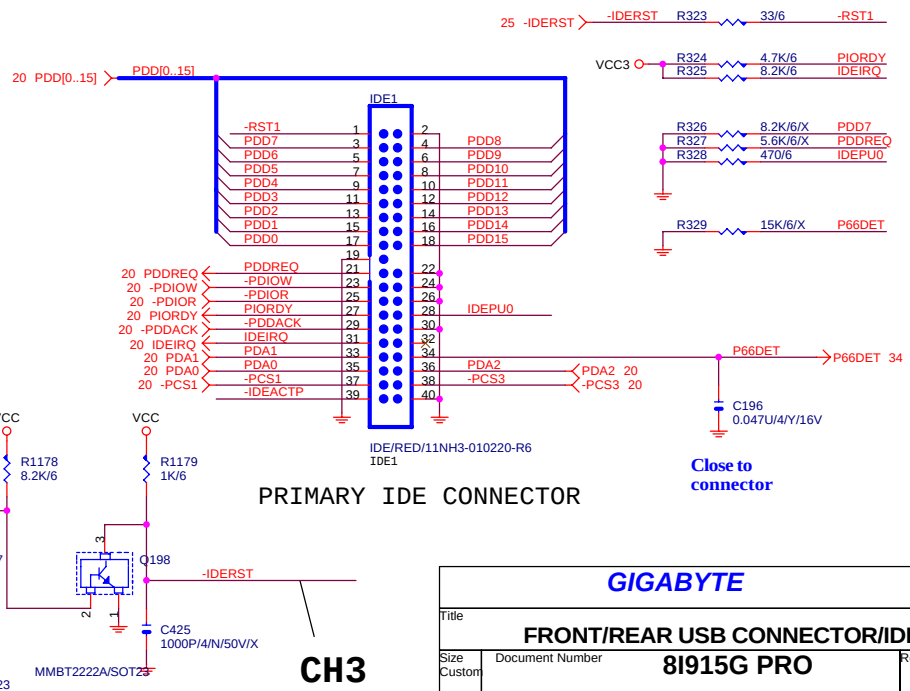
160MTLS FUSEVCC, GAMEVCC



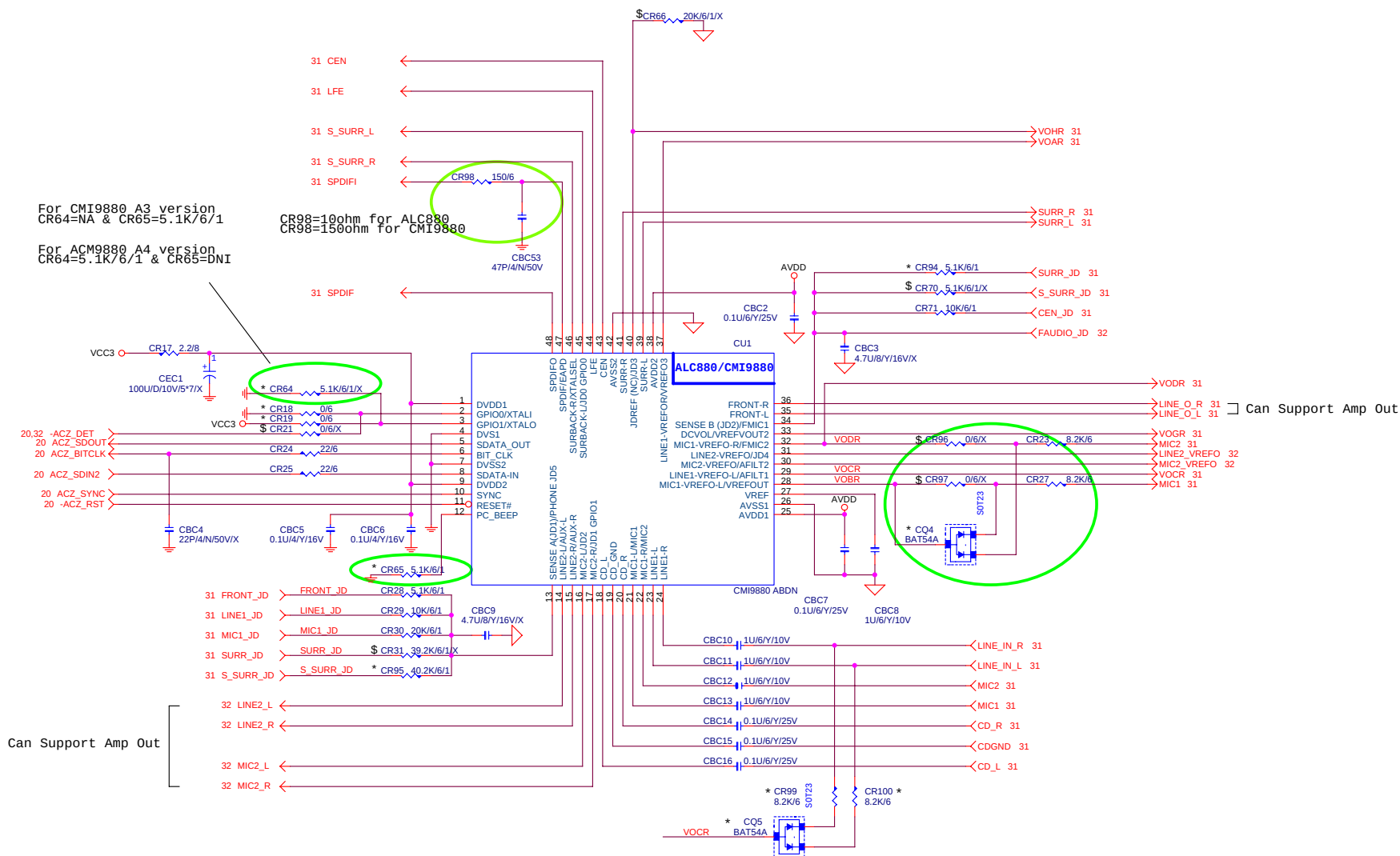
IDE/SATA LED

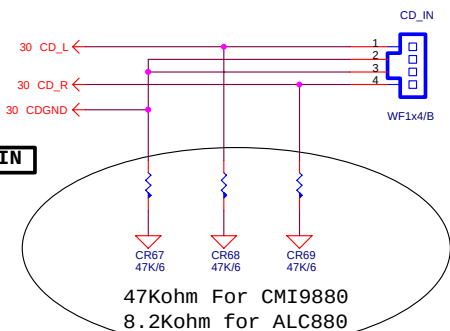
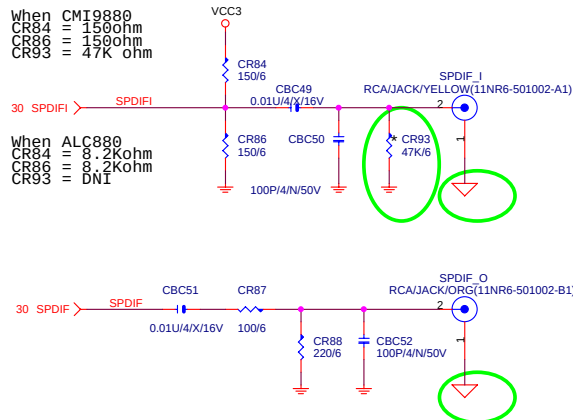
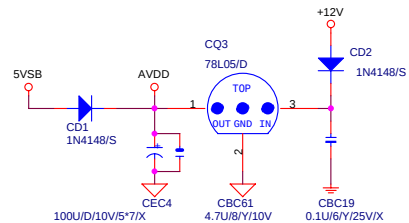
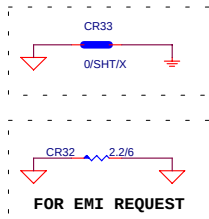


PRIMARY IDE CONNECTOR



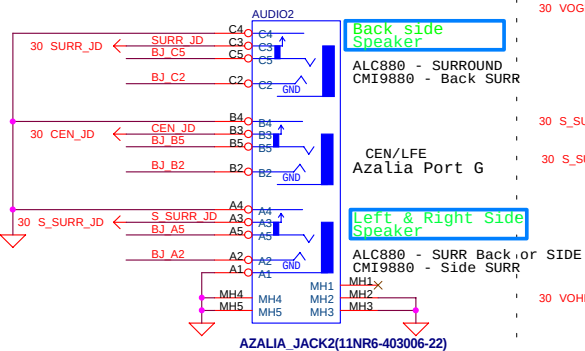
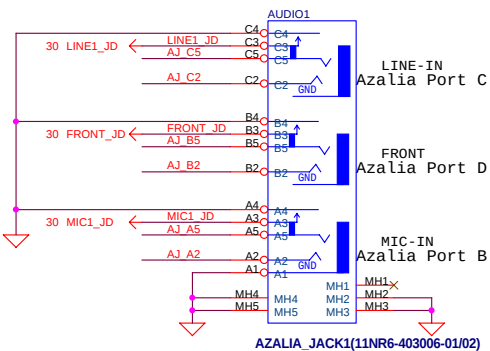
"\$" means for ALC880 only
"*" means for CMI9880 only



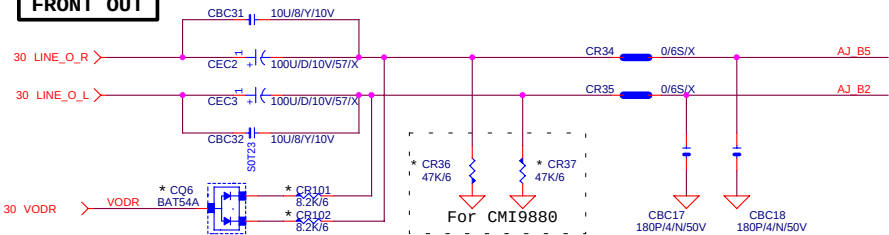


Azalia Jack
Normal --> pin4/pin3 open
Plug jack --> pin4/pin3 close

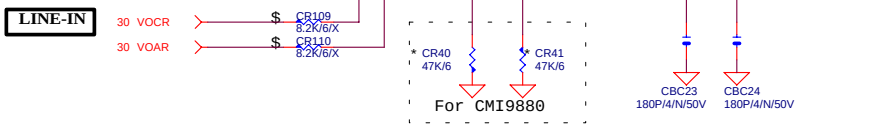
CMI9880 Port A is Side SURROUND, Port H is Back SURROUND
ALC880 Port A is SURROUND, Port H is SIDE



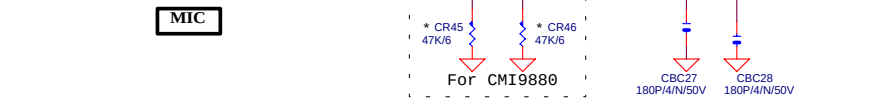
LINE OUT FRONT OUT



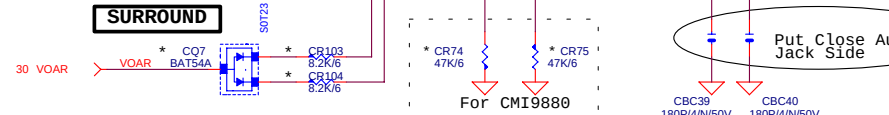
LINE-IN



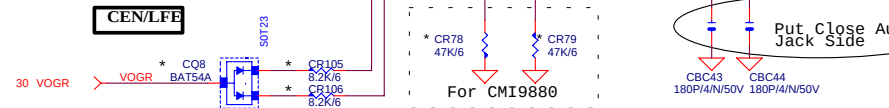
MIC



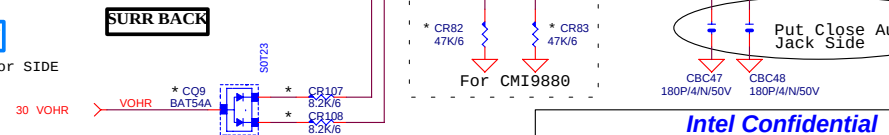
SURROUND



CEN/LFE



SURR BACK

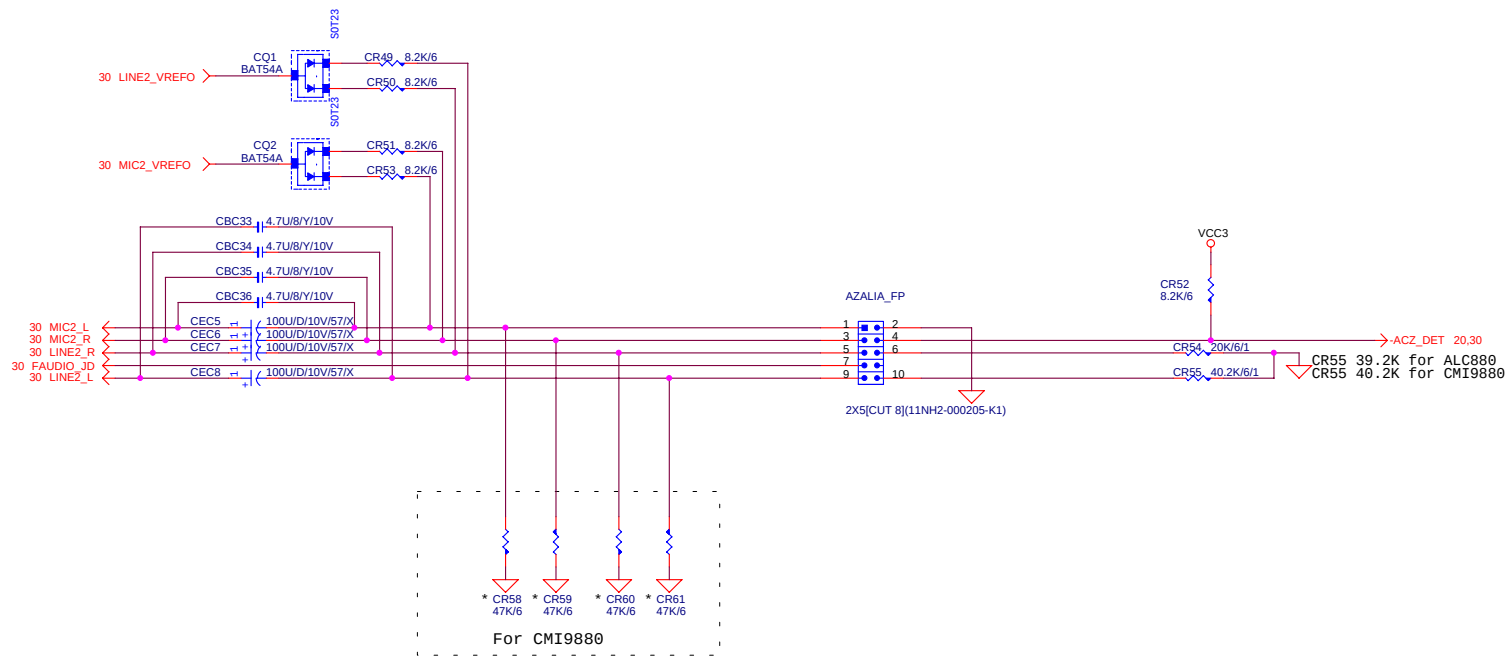


Intel Confidential

Title			AUDIO JACK	
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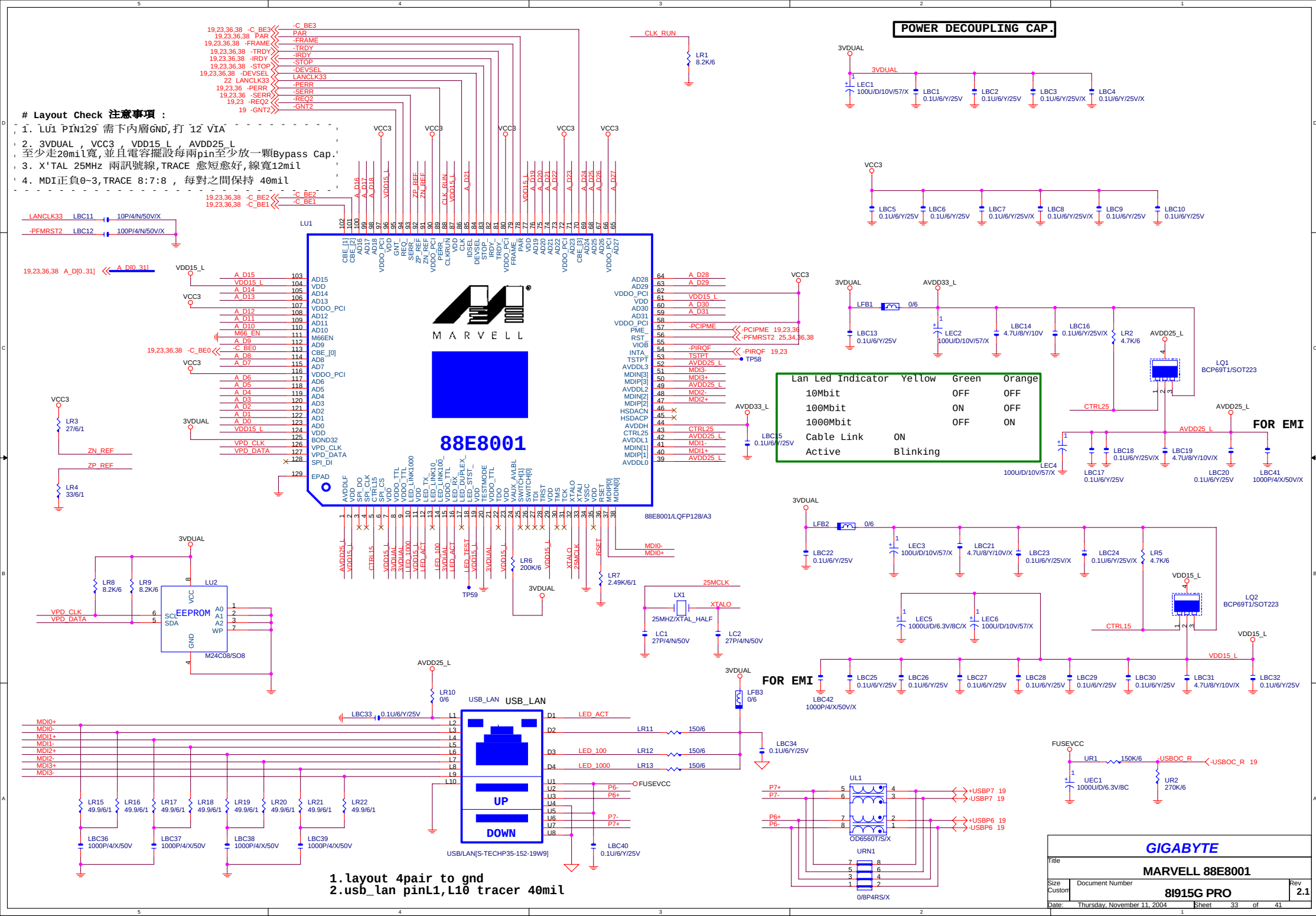
Azalia Port F

Azalia Port E

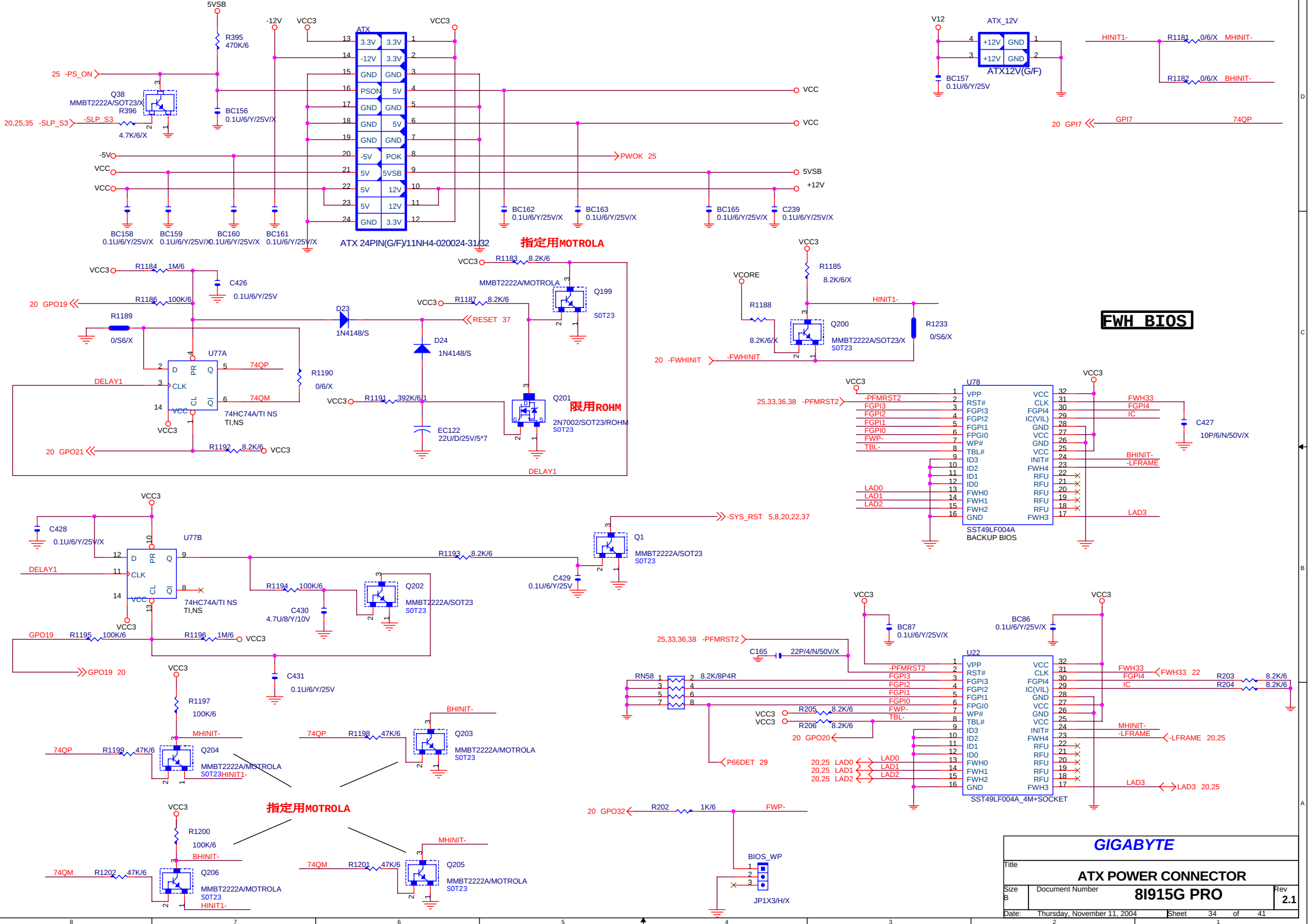


Intel Confidential

Title			
FRONT AUDIO CONNECTOR			
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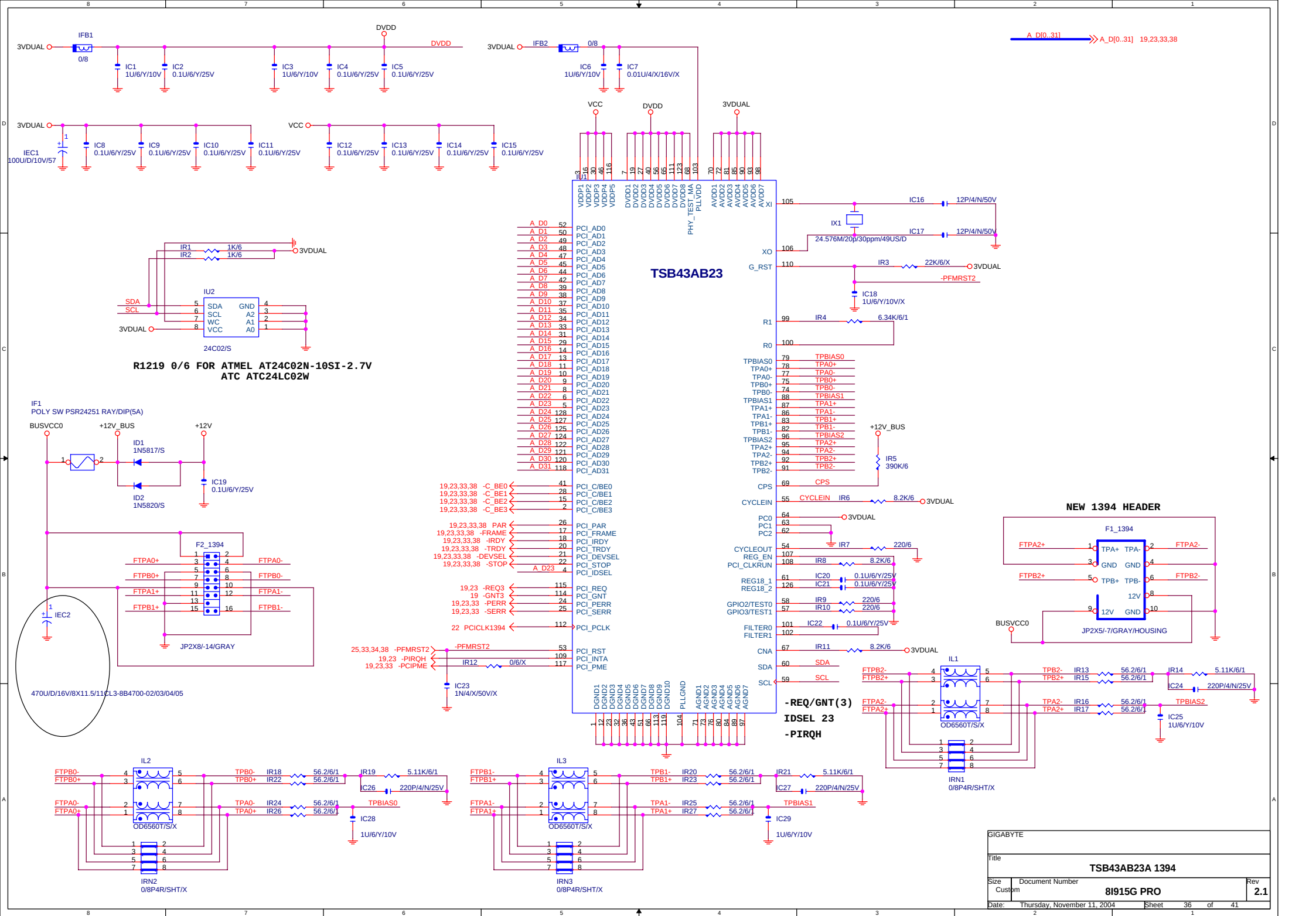


ATX POWER CONNECTOR

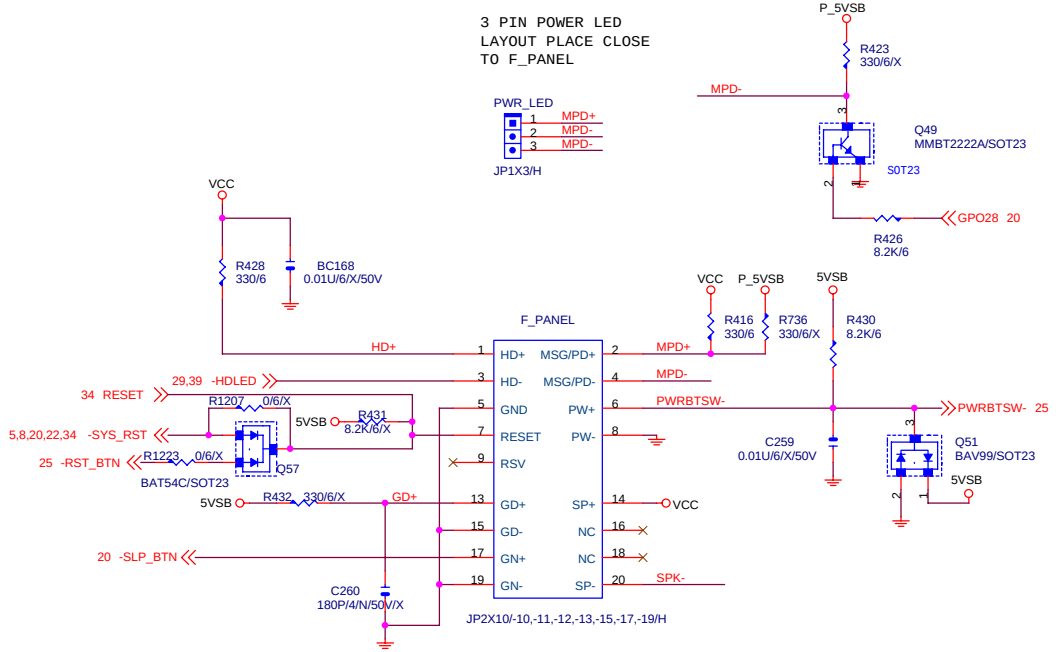


The schematic diagram illustrates the power management circuitry for the ZN7002 SoC. It features two operational amplifiers, U45A and U45B (LM393/SO8), configured as comparators or buffers. The input stage includes a network of resistors (R1240, R1257, R1115, R1118, R1258) and capacitors (C404, C443). A MOSFET driver stage uses U46 (SI3443DV/P MOS/T SOP-6) to drive the gate of Q214 (SOT23). The output stage involves a diode-connected MOSFET Q184 (AP40T03H4IP/D2ON03/L/AOD408/ZSK3641-ZK/TO25) connected to a +12V supply through resistor R1113 (8.2K/6). Various other components like FUSEVCC, R1259, EC129, and EC121 are shown, along with multiple 5VSB and 5VDUAL supply pins.

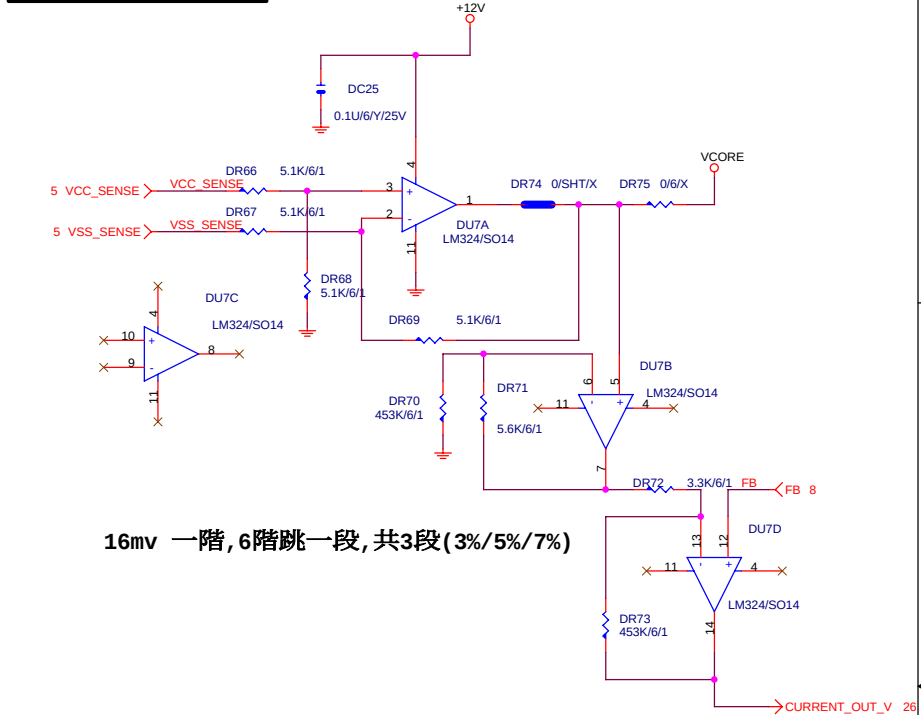
[illegible]



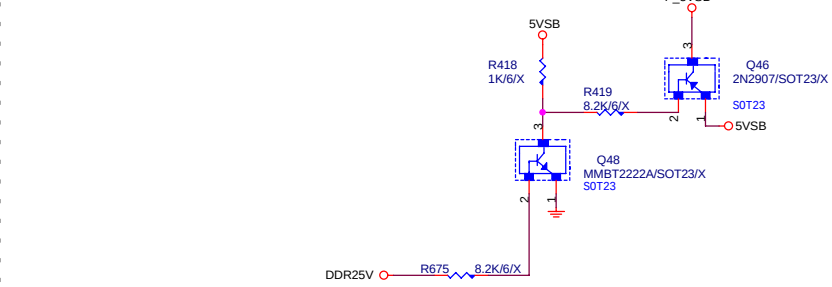
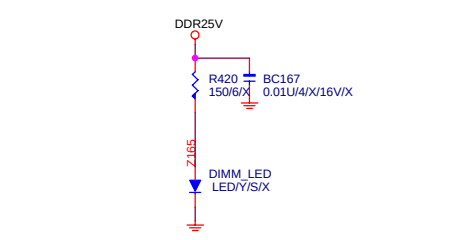
INTEL FRONT PANEL



CURRENT OUT (N/A)



16mv 一階,6階跳一段,共3段(3%/5%/7%)



States for green LED N01 GP022 only S1 PROGRAMMING LOW

LED States	ACPI States	GP028
ON	S1,S3	0
OFF	S0,S5	1

(GP022 DEFAULT HIGH, main power)

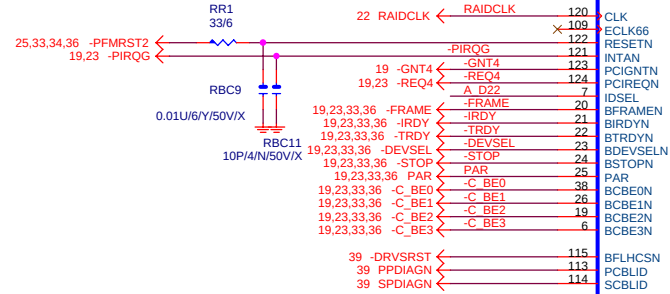
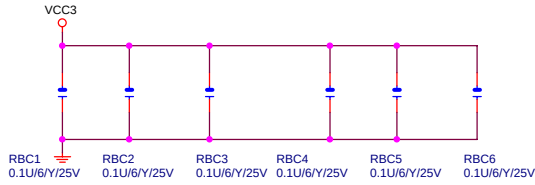
States for a single-color power LED

LED States	ACPI States	GP025	GP027	GP024
OFF	S1,S3,S5	1	1	N01
Steady Green	S0	1	1	1
Blinking Green	S0(message waiting)	1	0	1

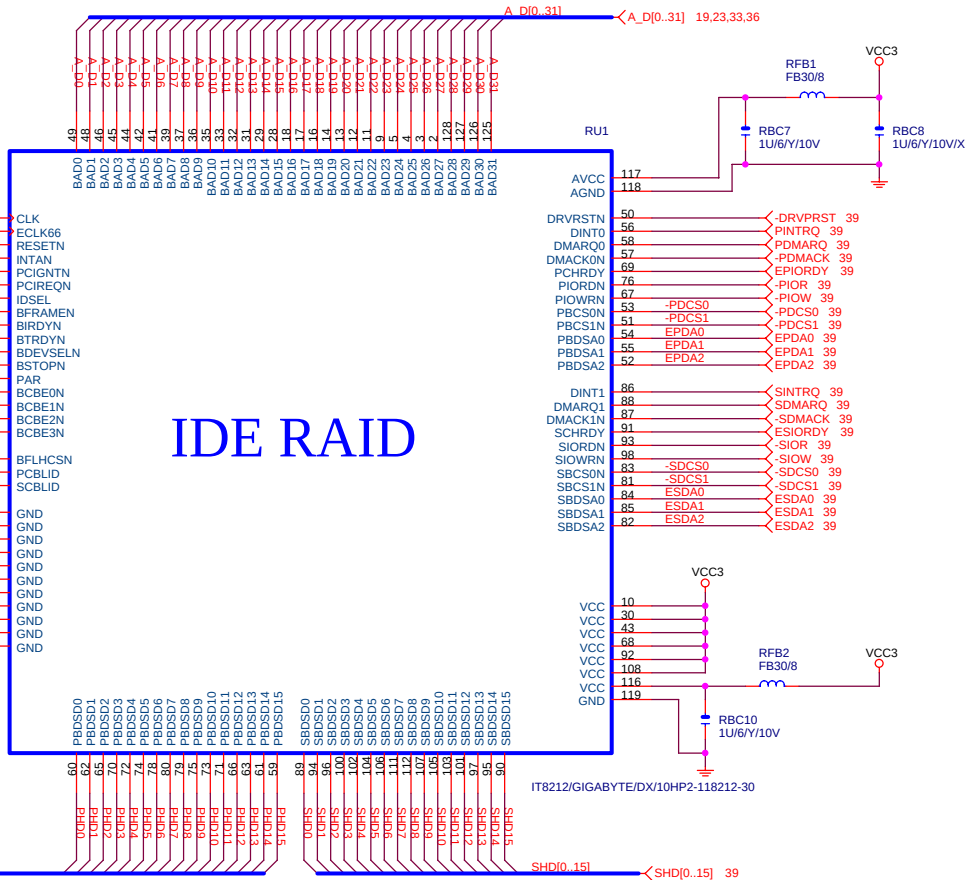
LED States	ACPI States	GP025	GP027	GP022
OFF	S5	1	1	X
Steady Green	S0	1	1	1
Blinking Green	S0(message waiting)	1	0	1
Steady Yellow	S1,S3	1	0	N01
Blinking Yellow	S1,S3(message waiting)	1	0	N01

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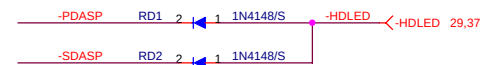
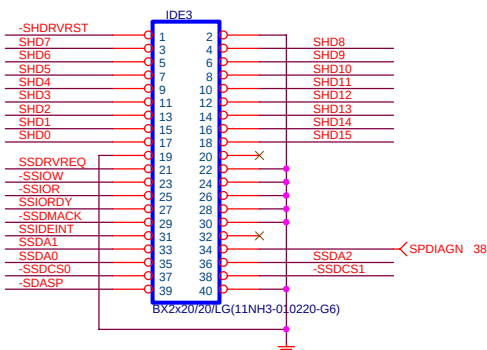
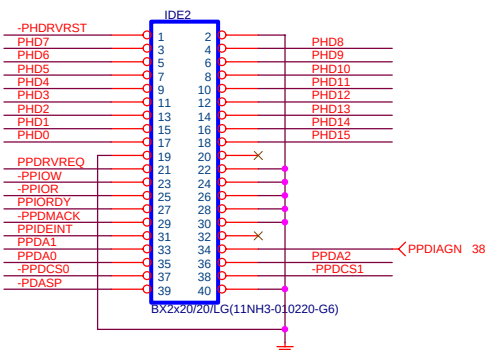
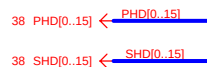
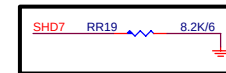
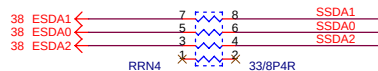
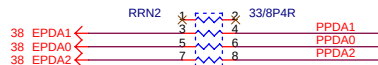
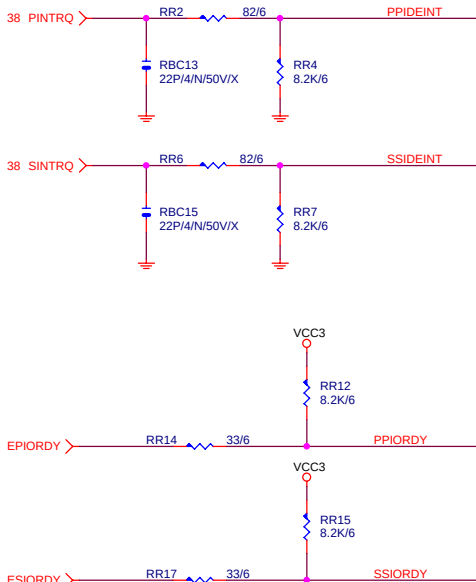
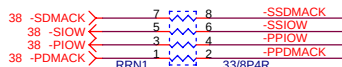
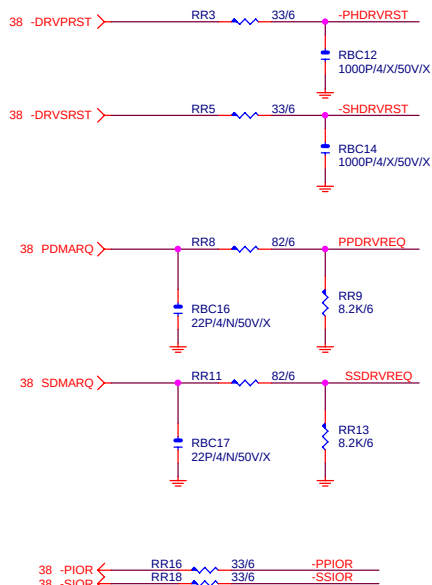
ALL INPUT PIN MUST HAVE 0.1 CAPACITOR



IDE RAID



GIGABYTE



INTEL ICH6 GPIO Implementation

GPI PIN

Pin Name	Pin Type	Power Well			GPIO Application
GPI[0]	Input	V5REF	-REQ[6]	(P.U VCC)	MB_ID0 Reserved
GPI[5:2]	Input	V5REF	-PIRQ[H:E]	(P.U VCC)	PCI/LAN/NA/1394
GPI[6]	Input	VCC3	GPI[6]	(P.U VCC3)	-SLP_BTN
GPI[7]	Input	VCC3	GPI[7]	(NA)	DUALBIOS_INPUT
GPI[8]	Input	3VDUAL	GPI[8]	(P.U 3VDUAL)	-LANWAKE
GPI[10:9]	Input	3VDUAL	0C 4/5	(P.U 5VDUAL 分屬)	-USBOC_R
GPI[11]	Input	3VDUAL	-SMBALERT	(P.U 3VDUAL)	-SMBALRT
GPI[12]	Input	VCC3	GPI[12]	(P.U VCC3)	MB_ID2
GPI[13]	Input	3VDUAL	GPI[13]	(P.U 3VDUAL)	-LPCPME
GPI[15:14]	Input	3VDUAL	0C 6/7	(P.U 5VDUAL 分屬)	-USBOC_R
GPO[16]	OUTPUT	VCC3	-GNT[6]	(integrated VCC3)	Reserved
GPO[17]	OUTPUT	VCC3	-GNT[5]	(integrated VCC3)	Reserved
GPO[18]	OUTPUT	VCC3	GPO[18]	(NA blinking)	Reserved
GPO[19]	OUTPUT	VCC3	GPO[19]	(P.U VCC3)	DUAL_BIOS_OUTPUT
GPO[20]	OUTPUT	VCC3	GPO[20]	(P.U VCC3)	TBL-
GPO[21]	OUTPUT	VCC3	GPO[21]	(P.U VCC3)	DUAL_BIOS_OUTPUT
GPO[22]	Not Implemented		Not Implemented		Not Implemented
GPO[23]	OUTPUT	VCC3	GPO[23]	(NA)	Reserved
GPO[24]	IN/OUT	3VDUAL	GPO[24]	(NA)	GREEN_LED
GPO[25]	IN/OUT	3VDUAL	vcc_25vregulator	(NA)	Reserved
GPI[26]	Input	VCC3	SATA[0]GP	(P.U VCC3)	SATA[0]GP
GPIO[27]	IN/OUT	3VDUAL	GPIO[27]	(NA)	Reserved
GPIO[28]	IN/OUT	3VDUAL	GPO[28]	(NA)	PWD_LED
GPI[29]	Input	VCC3	SATA_1GP	(P.U VCC3)	SATA_1GP
GPI[30]	Input	VCC3	SATA_2GP	(P.U VCC3)	SATA_2GP
GPI[31]	Input	VCC3	SATA_3GP	(P.U VCC3)	SATA_3GP
GPIO[32]	IN/OUT	VCC3	GPO[32]	(NA)	FWP-
GPIO[33]	IN/OUT	VCC3	GPI[33]	(P.U VCC3)	-ACZ_DET
GPIO[34]	IN/OUT	VCC3	GPIO[34]	(NA)	Reserved
GPI[40]	Input	V5REF	-REQ[4]	(P.U VCC)	-REQ[4]
GPI[41]	Input	VCC3	GPI[41]	(P.U VCC3)	MB_ID1
GPO[48]	OUTPUT	VCC3	-GNT[4]	(integrated VCC3)	Reserved
GPO[49]	OD O	V CPU IO	CPUPWROK	(P.U VTT OR)	CPUPWROK
GPIO[35-39,42-47]		NOT IMPLEMENTED		NOT IMPLEMENTED	

GPO PIN

[illegible]

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GPIO TABLE

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ICH6 GPIO Table:

NAME	PWR LANE	USAGE	NAME	PWR LANE	USAGE
GPI0	V5REF	M/B ID (-REQ6)	GPI41	VCC3	M/B ID
GPI1	V5REF	-REQ5	GP048	VCC3	-GNT4
GPI2	V5REF	-PIRQE	GP049	V-CPUIO	CPUPWOK
GPI3	V5REF	-PIRQF			
GPI4	V5REF	-PIRQG			
GPI5	V5REF	-PIRQH			
GPI6	VCC3	-SLP BTN			
GPI7	VCC3	DUAL BIOS			
GPI8	3VDAUL	-LANWAKE			
GPI9	3VDAUL	-USBOC4			
GPI10	3VDAUL	-USBOC5			
GPI11	3VDAUL	-SMBALT			
GPI12	VCC3	ATX_DET			
GPI13	3VDAUL	-LPCPME			
GPI14	3VDAUL	-USBOC6			
GPI15	3VDAUL	-USBOC7			
GP016	VCC3	CPU OV1 (-GNT6)			
GP017	VCC3	-GNT5			
GP018	VCC3	CPU OV2			
GP019	VCC3	DUAL BIOS			
GP020	VCC3	BIOS T-BLOCK			
GP021	VCC3	DUAL BIOS			
GP023	VCC3	DDR OV0			
GPI024	3VDAUL	GREEN LED			
GPI025	3VDAUL	DDR OV1			
GPI26	VCC3	SATA GP0			
GPI027	3VDAUL	+PWRLED			
GPI028	3VDAUL	-PWRLED			
GPI29	VCC3	SATA GP1			
GPI30	VCC3	SATA GP2			
GPI31	VCC3	SATA GP3			
GPI032	VCC3	BIOS WP			
GPI033	VCC3	AZALIA DET			
GPI034	VCC3	PWRLED			
GPI40	V5REF	-REQ4			

PWROK/RESET Table:

ITE8712BHX PIN	NET NAME	TARGET
PIN62/-PCIRST1	-PCIE_RST	1. PCI-E * 1 Slot1 2. PCI-E * 1 Slot2 3. PCI-E * 1 Slot3 4. PCI-E * 16 Slot
PIN64/-PCIRST2	-PFMRST2	1. Onboard PCI Lan 2. Onboard 1394 Chip 3. OnBoard FWH
PIN65/-PCIRST3	-PFMRST1	1. Onboard PCI-E Lan 2. Onboard SATA Chip 3. GMCH
PIN115/-PCIRST4	-PFMRST- -IDERST	Reserved For IDE
PIN63/PWROK1	PWROK1	1. GMCH 2. ICH6 3. 5VDUAL SWITCH 4. DPS CONTROL
PIN109/PWROK2	-THERM	1. ICH6

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