

Model Name: 8I915PL-G REV2.0

SHEET	TITLE
01	COVER SHEET
02	BLOCK DIAGRAM
03	BOM & PCB MODIFY HISTORY
04	P4_LGA775_A
05	P4_LGA775_B
06	P4_LGA775_C
07	P4_LGA775_D
08	VCORE POWER
09	GMCH-GRANTSDALE_HOST
10	GMCH-GARNTSDALE_DDR
11	GMCH-GRANTSDALE_PCI E, DMI
12	GMCH-GRANTSDALE_INT VGA
13	GMCH-GRANTSDALE_GND
14	GMCH-GRANTSDALE_PWR
15	DDR CHANNEL A
16	DDR CHANNEL B
17	DDR TERMINATION
18	PCI EXPRESS*16 SLOT
19	ICH6 PCI, USB, DMI, LAN
20	ICH6 IDE, GPIO, SATA, CTRL
21	ICH6 VCC, GND
22	CLK GEN

SHEET	TITLE
23	PCI SLOT
24	PCI EXPRESS*1 SLOT
25	ITE8712HX
26	HWM0/FAN/FWH BIOS
27	KB_MS/GAME
28	COM/LPT/FDD
29	(FRONT+REAR)USB/RING/IDE
30	AZALIA CODEC ALC880/CMI9880
31	AUDIO JACK
32	LAN BCM5705E/5751
33	LAN BCM5751
34	ATX POWER CONN.
35	ALL POWER
36	1394 TSB43AB23
37	FRONT PANEL/BZ
38	RAID VIA6410
39	RAID IDE CONNECTOR
40	GPIO TABLE
41	RESET TABLE

COMPONENT SIDE
(1 oz. Copper)
VCC SIDE
(1 oz. Copper)
GND SIDE
(1 oz. Copper)
SOLDER SIDE
(1 oz. Copper)

GIGABYTE

Title

Cover Sheet

Size Custom

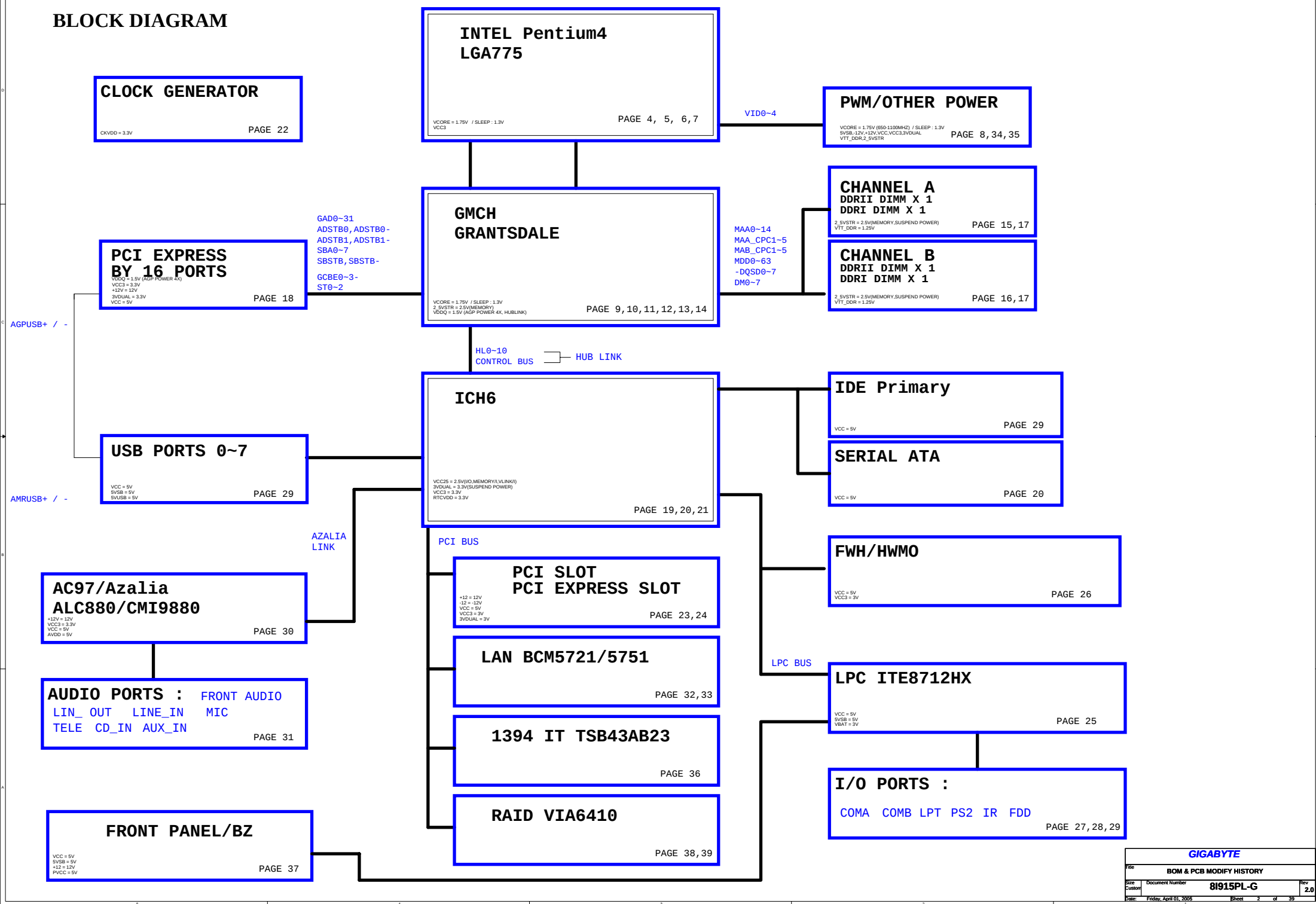
Document Number8I915PL-G

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BLOCK DIAGRAM



Version: 2.0

Component value change history

2004/11/22

[illegible]

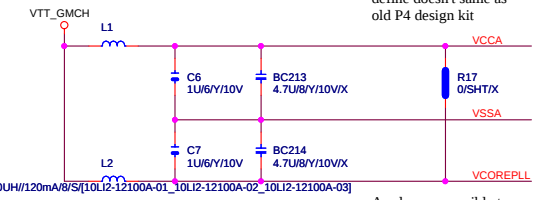
**Circuit or PCB layout change
for next version**

[illegible]

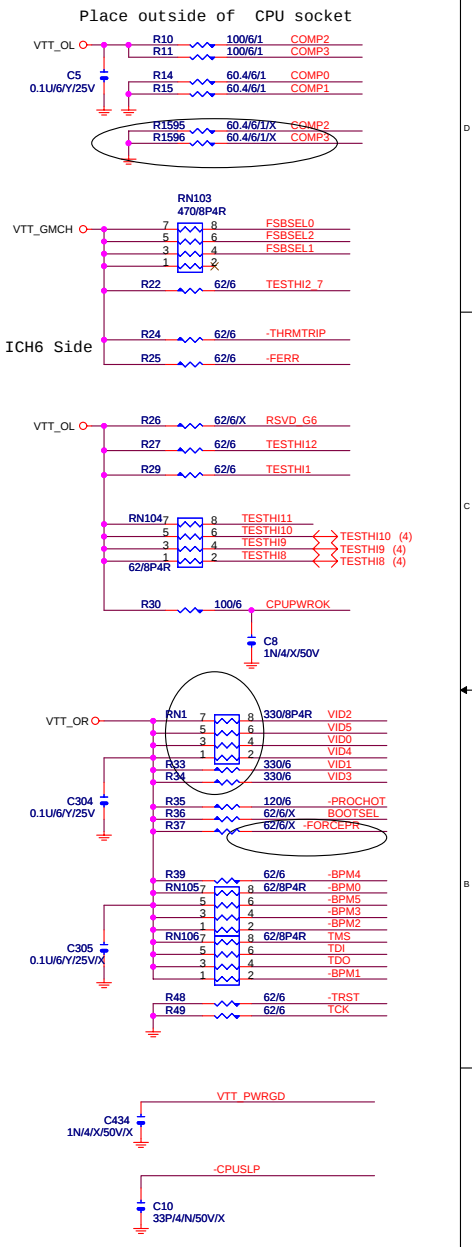
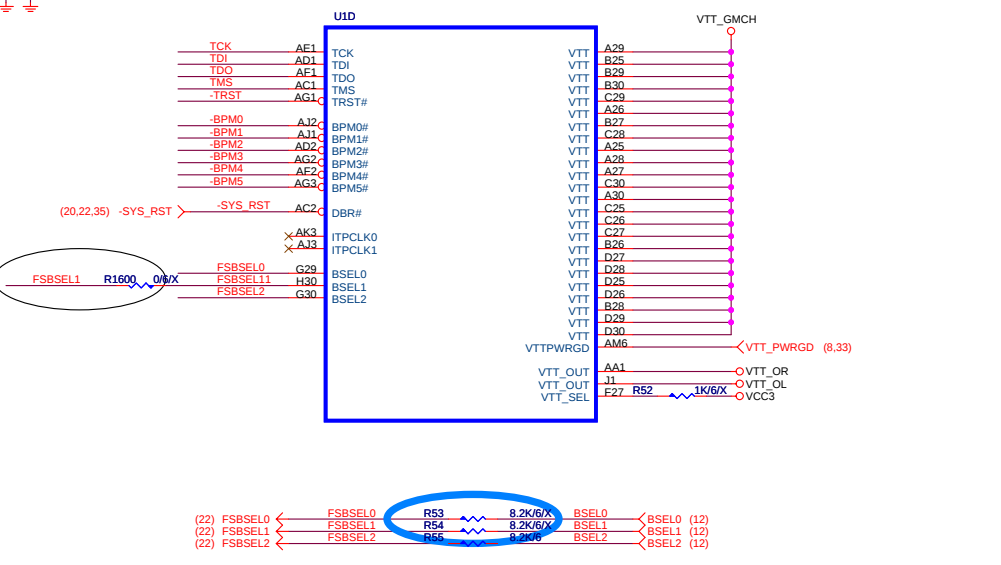
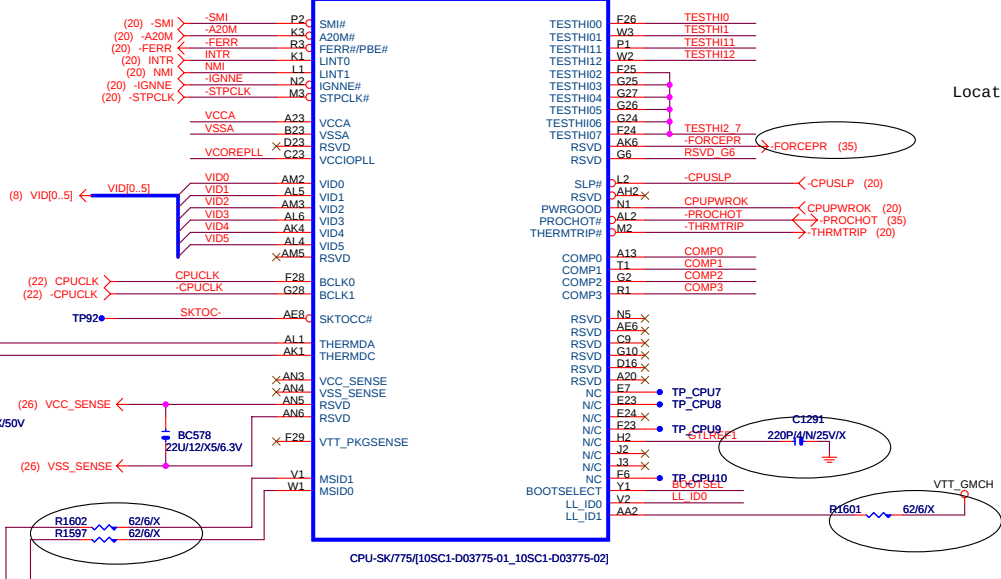
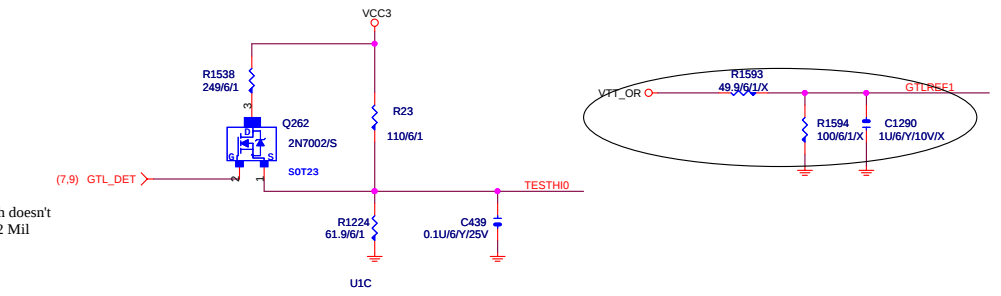
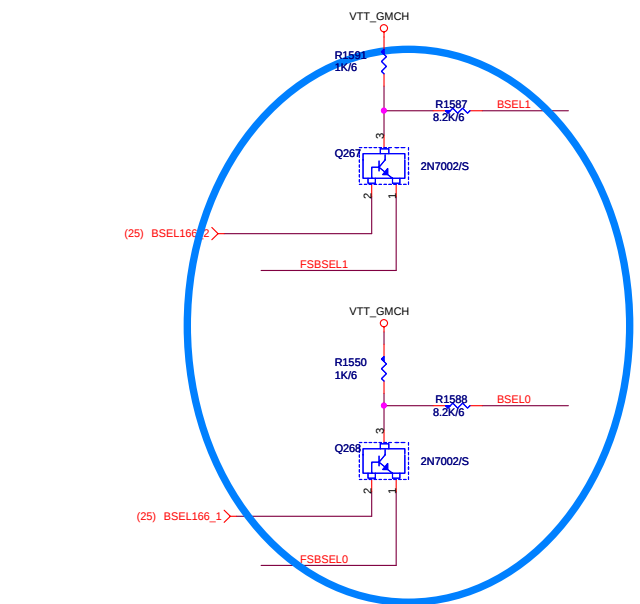
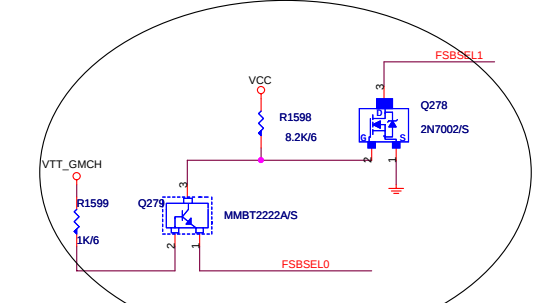
GIGABYTE			
Title BOM & PCB MODIFY HISTORY			
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10UH/120mA/8/S/[10LI2-12100A-01_10LI2-12100A-02_10LI2-12100A-03]

Note:
VCCA & VCOREPLL
define doesn't same as
old P4 design kit

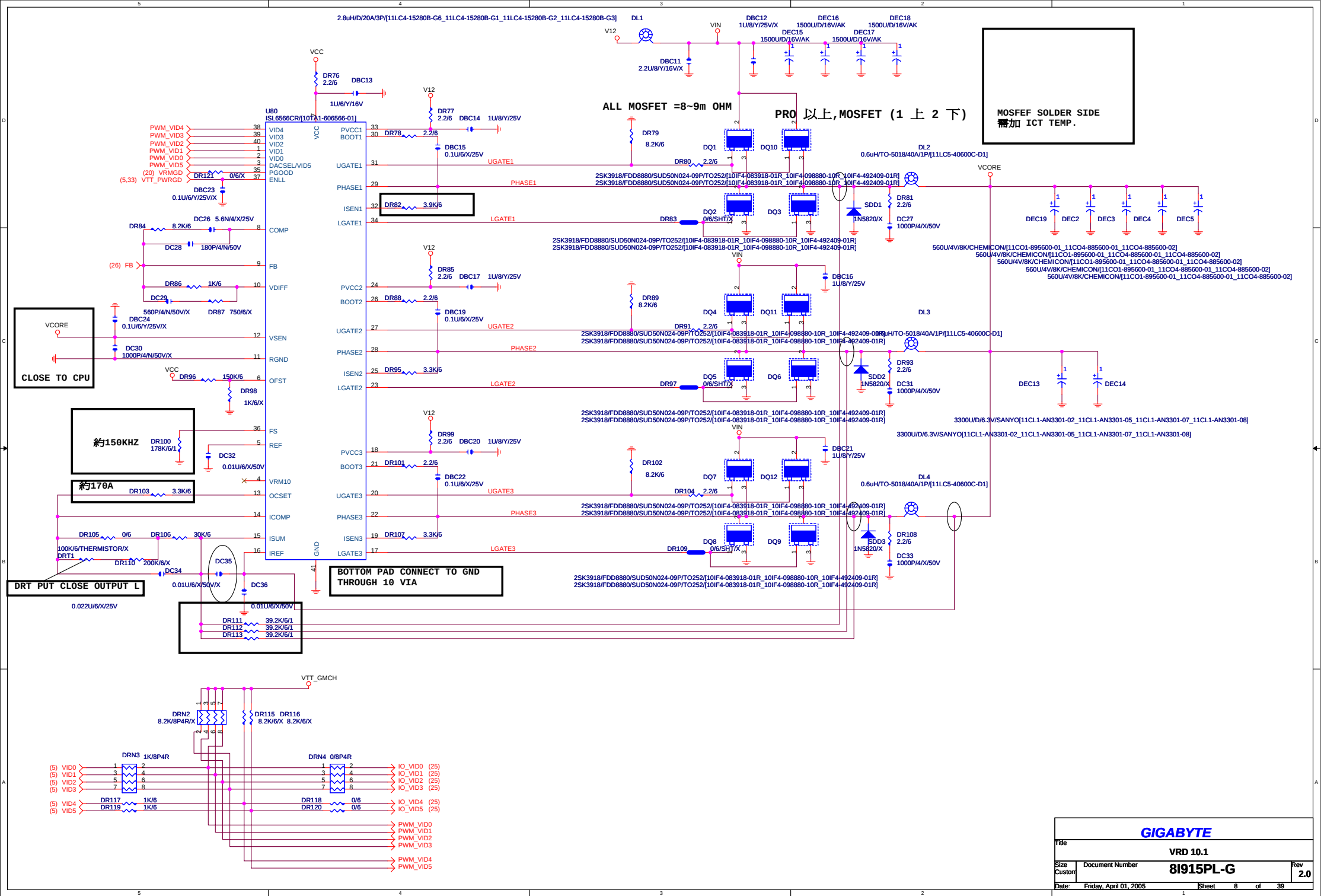


As close as possible to CPU socket

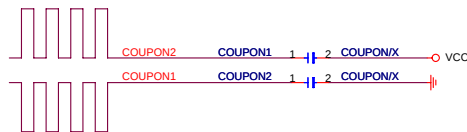


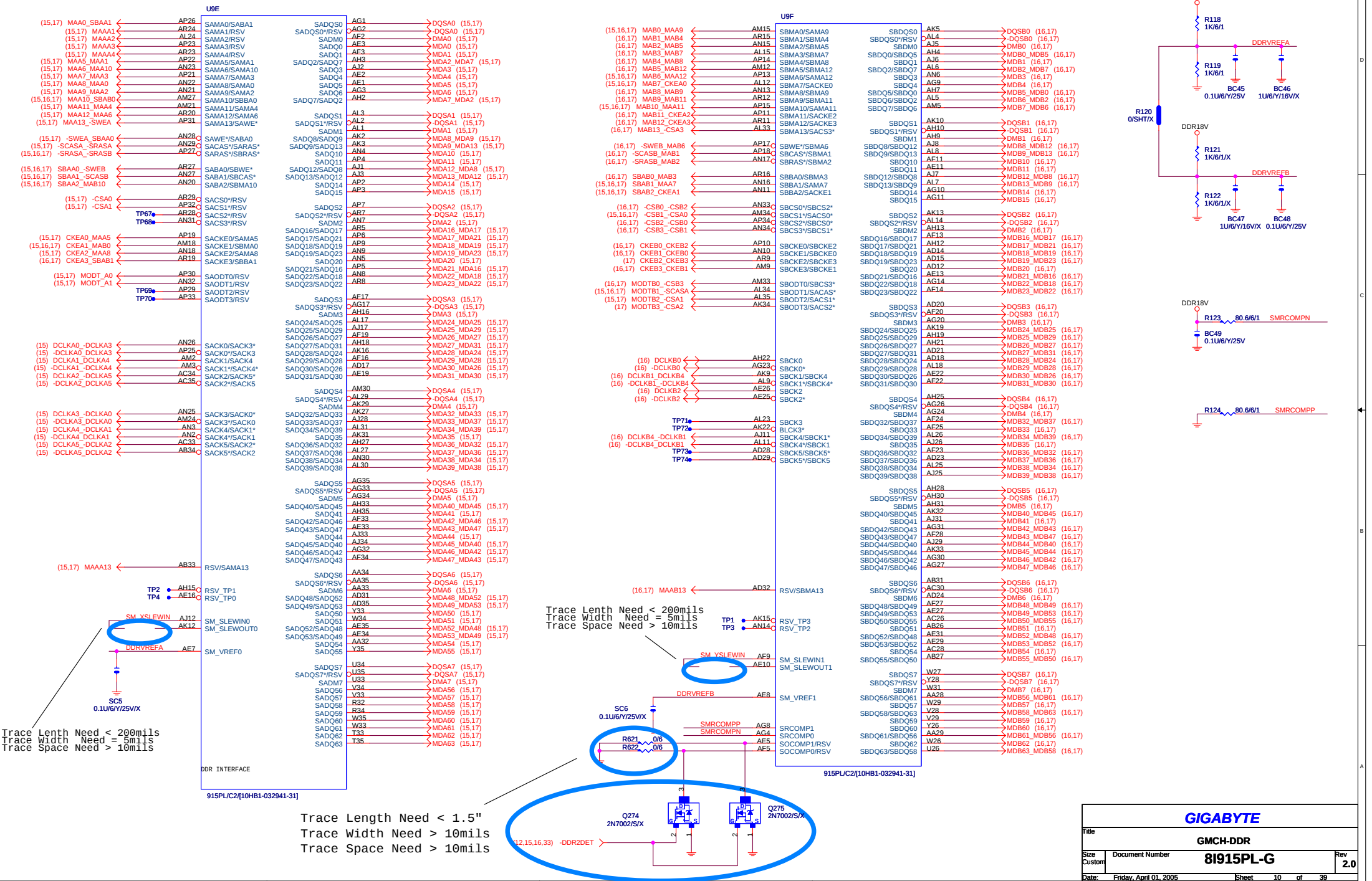
GIGABYTE			
P4_LGA775-B			
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GIGABYTE			
VRD 10.1			
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Trace Length Need < 290mils
Trace Width Need = 5mils
Trace Space Need > 10mils

Trace Length Need < 290mils
Trace Width Need = 5mils
Trace Space Need > 10mils

Trace Length Need < 1.5"
Trace Width Need > 10mils
Trace Space Need > 10mils

GIGABYTE			
Title			
GMCH-DDR			
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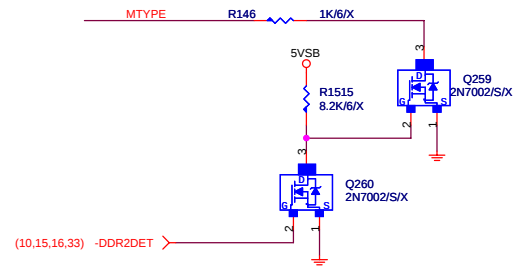
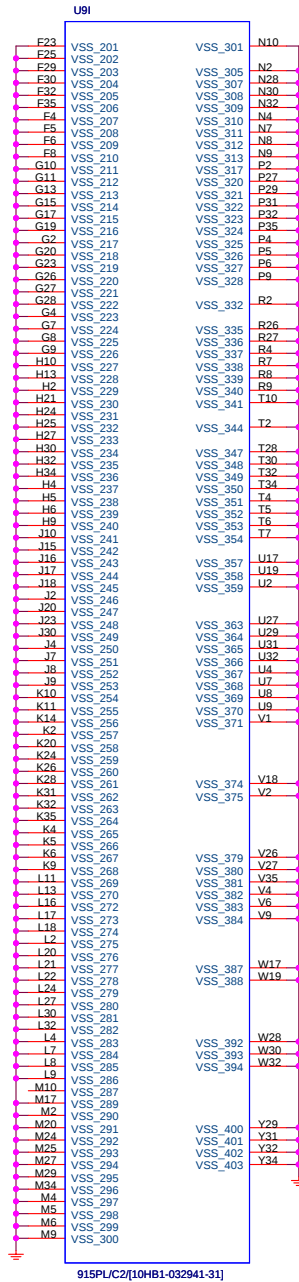
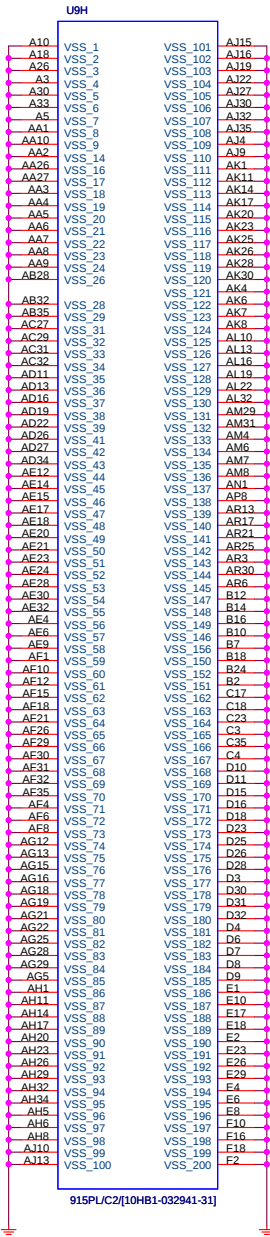
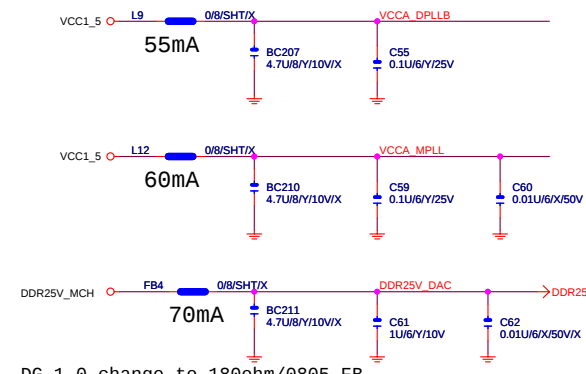
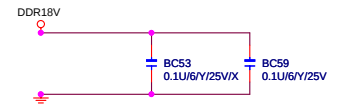
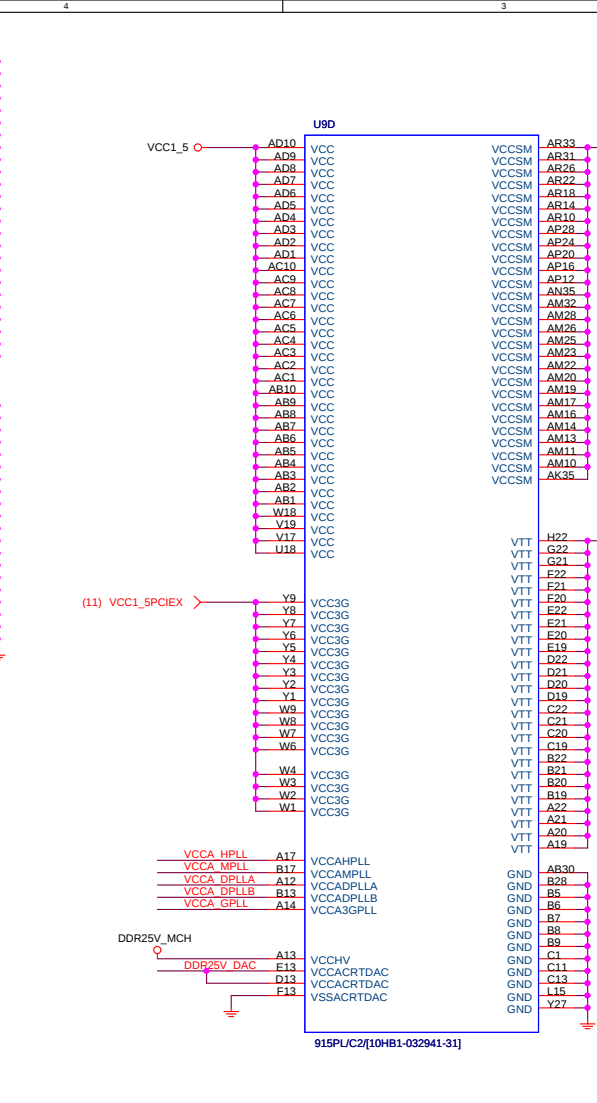


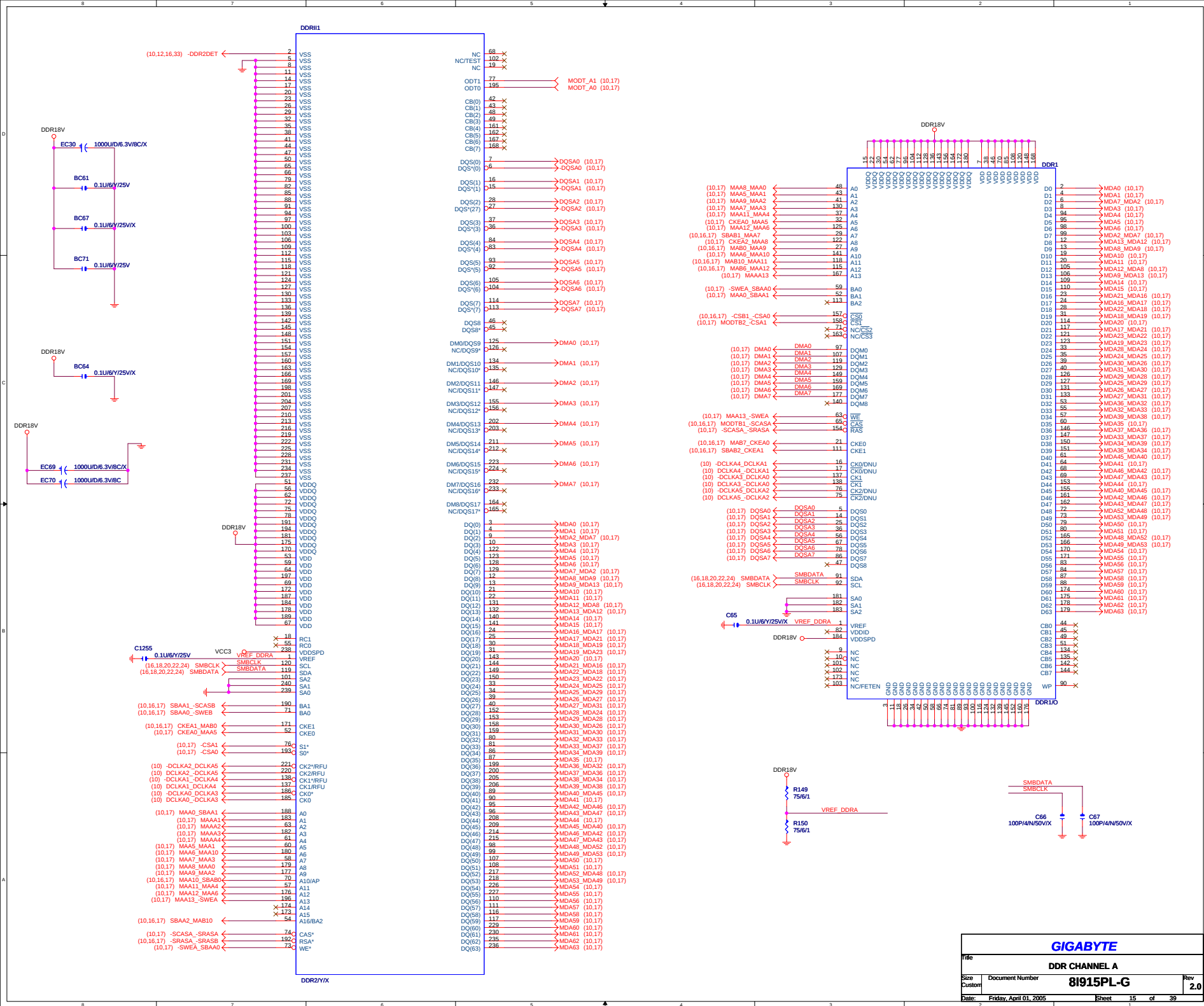
Diagram of a rectangular plate with a top flange and a bottom flange. The top flange has a circular hole with a diameter of 1 inch. The bottom flange has a circular hole with a diameter of 2 inches. The main body of the plate is labeled NB_HS.

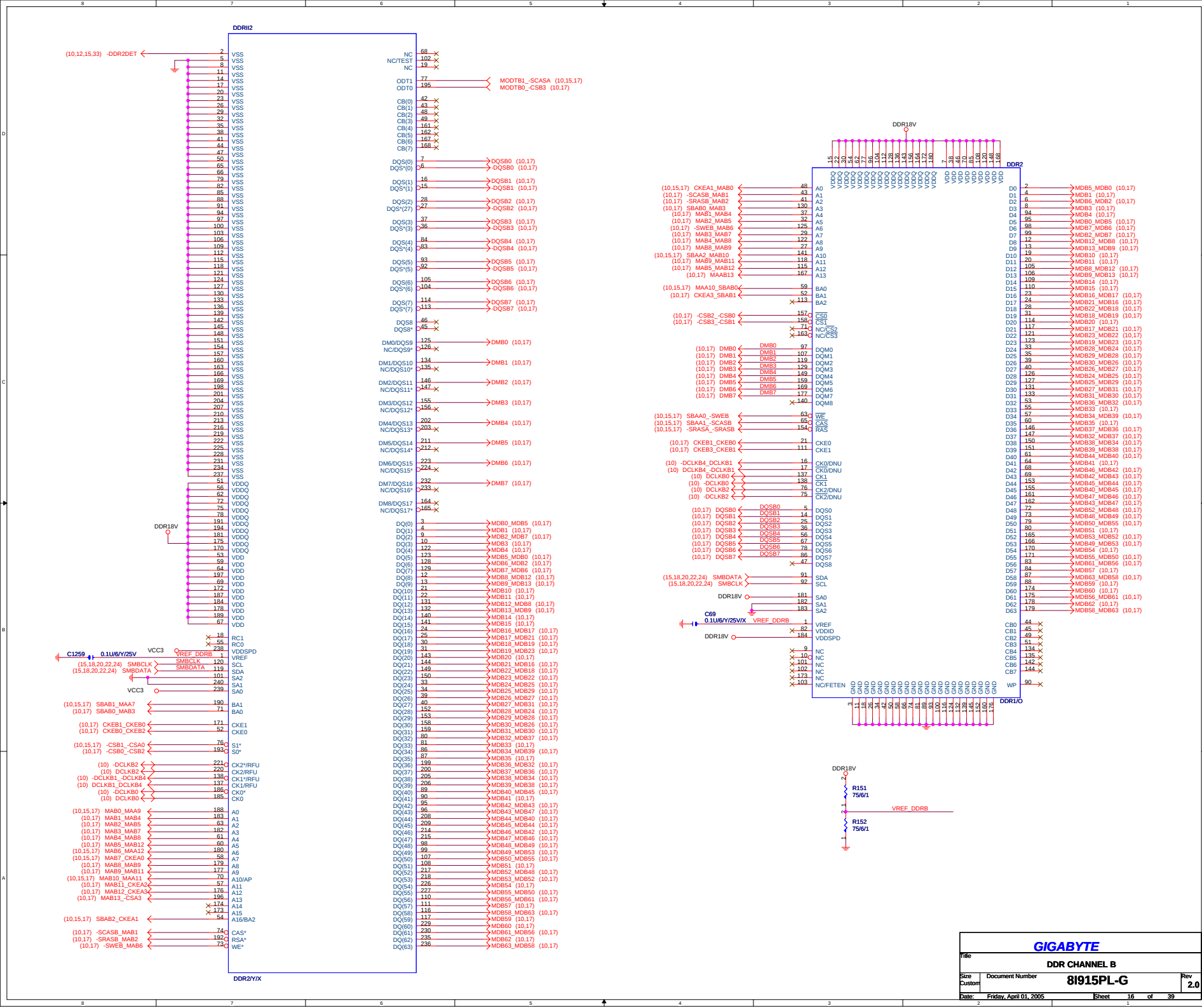
GIGABYTE			
Title			
GMCH-INTERNAL VGA			
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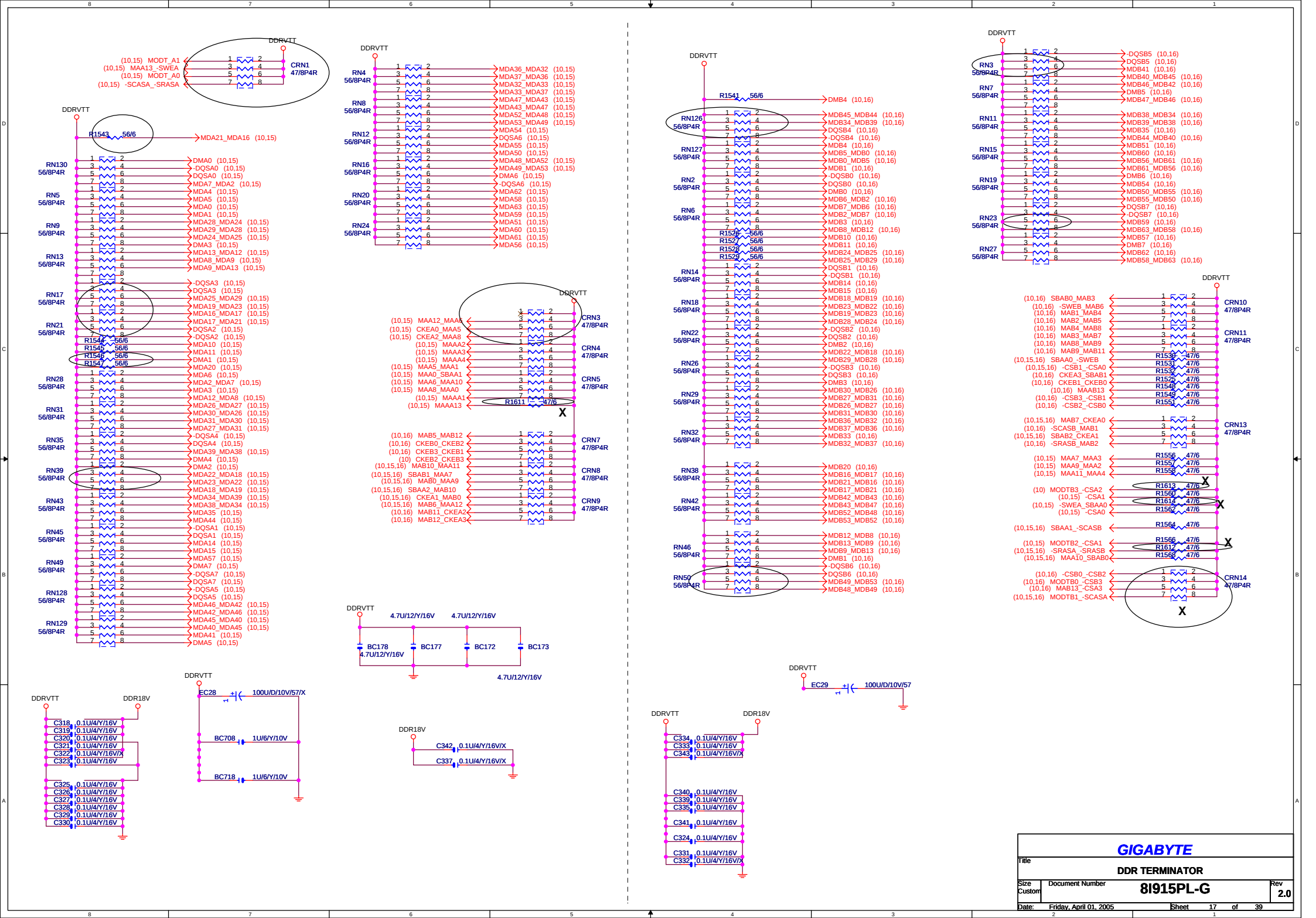


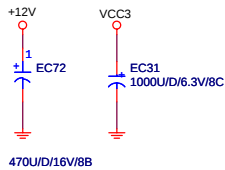


GIGABYTE			
Title			
GMCH-PWR			
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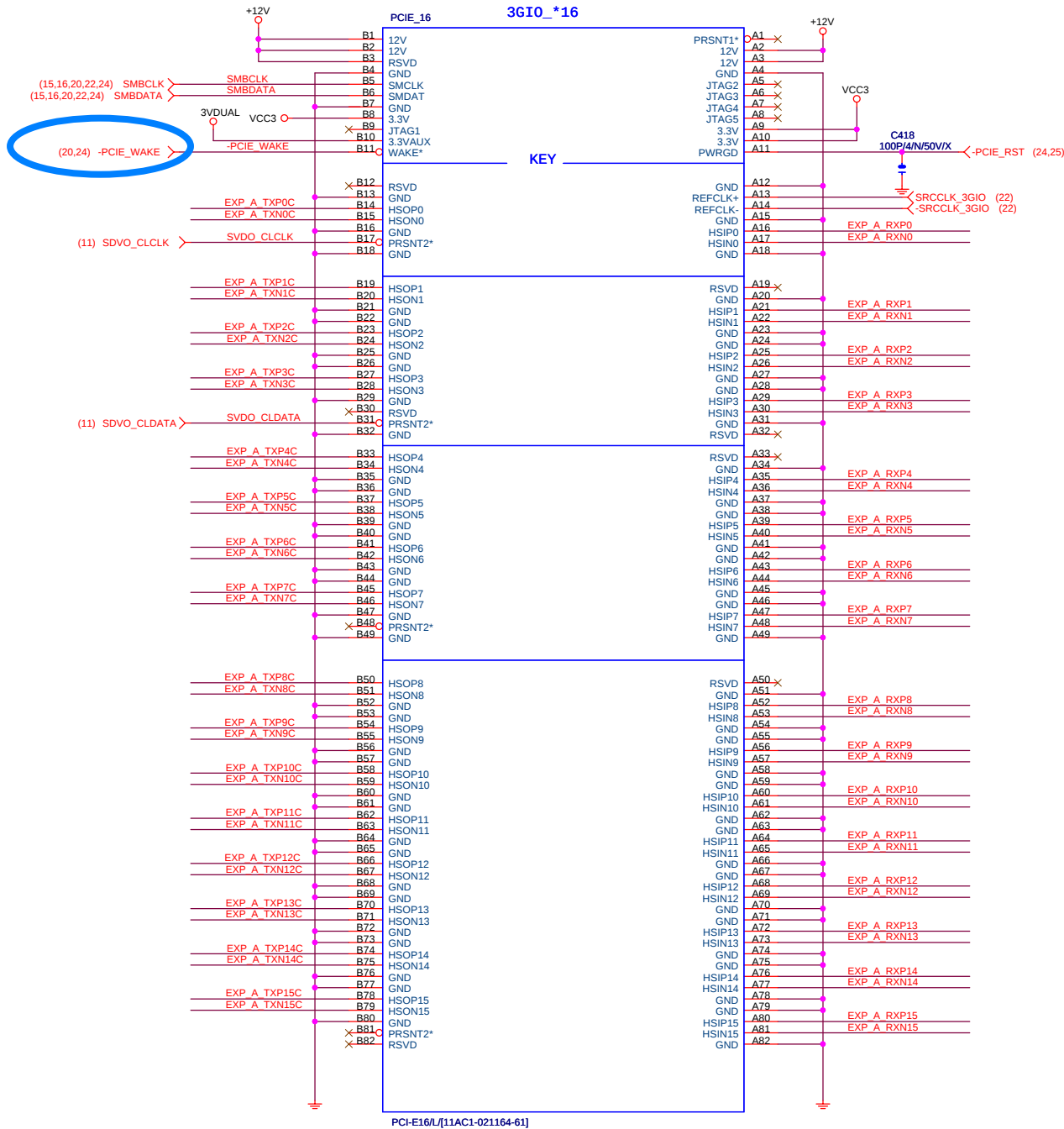


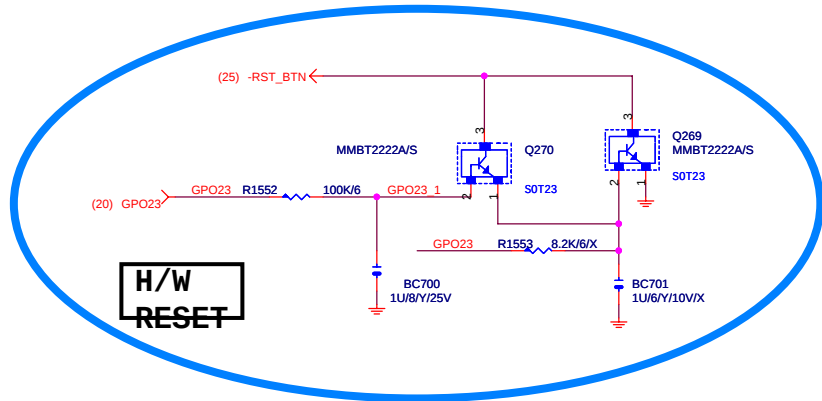


EXP A RXP[0..15] >> EXP_A_RXP[0..15] (11)
EXP A RXN[0..15] >> EXP_A_RXN[0..15] (11)

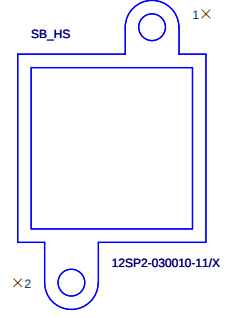
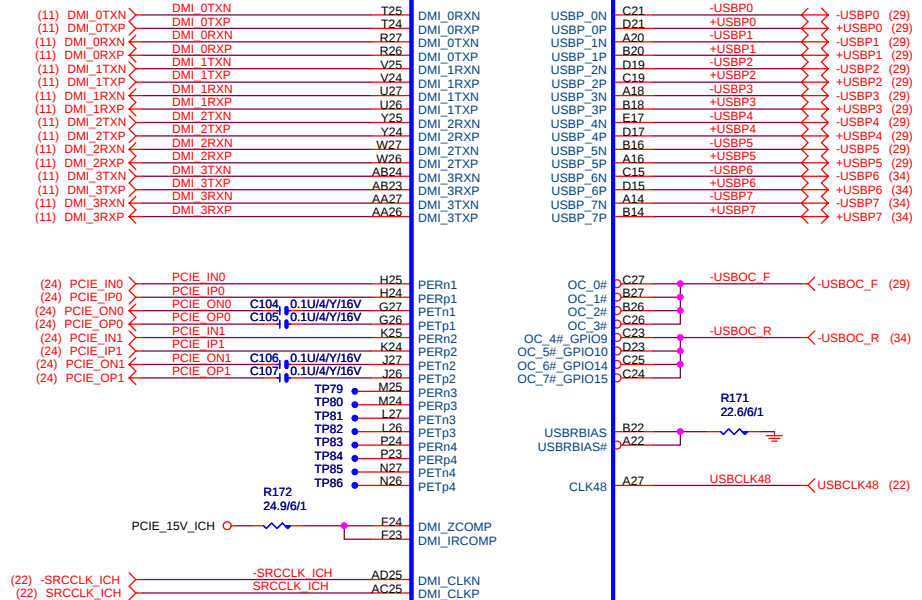
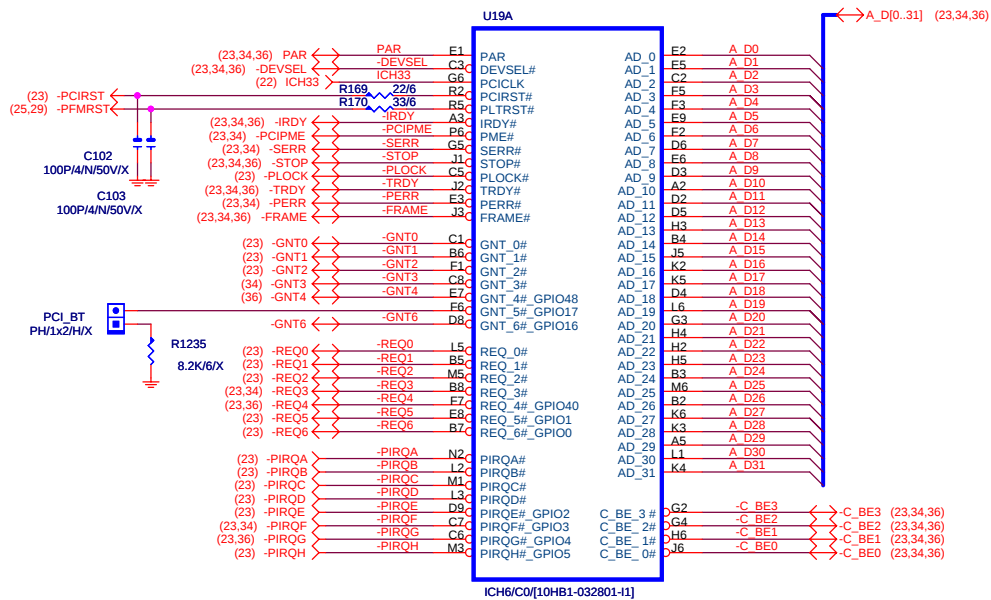
EXP A TXP[0..15] >> EXP_A_TXP[0..15] (11)
EXP A TXN[0..15] >> EXP_A_TXN[0..15] (11)

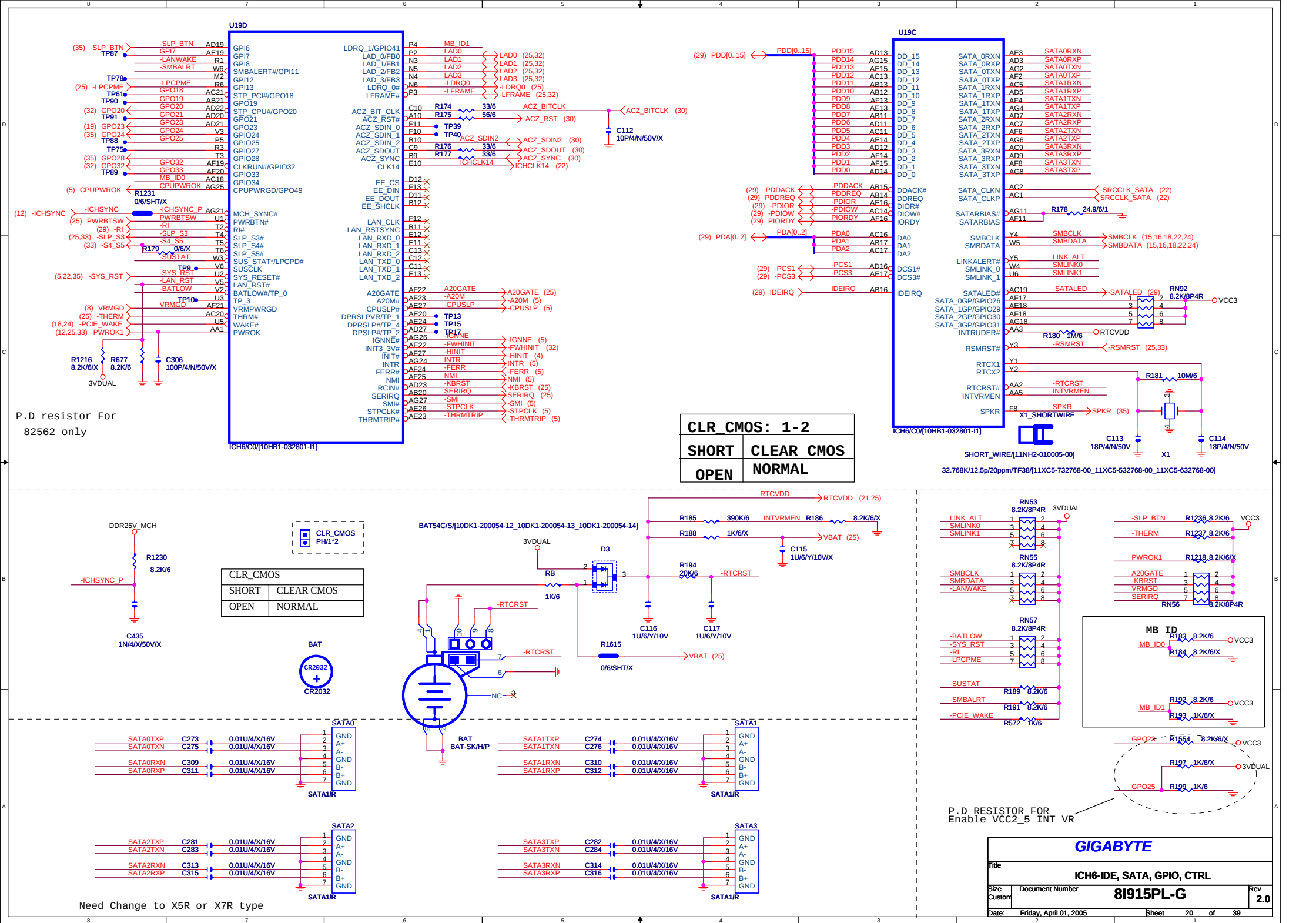
EXP A TXP0	C70	0.1u/6/Y/25V	EXP A TXP0C
EXP A TXN0	C71	0.1u/6/Y/25V	EXP A TXN0C
EXP A TXP1	C72	0.1u/6/Y/25V	EXP A TXP1C
EXP A TXN1	C73	0.1u/6/Y/25V	EXP A TXN1C
EXP A TXP2	C74	0.1u/6/Y/25V	EXP A TXP2C
EXP A TXN2	C75	0.1u/6/Y/25V	EXP A TXN2C
EXP A TXP3	C76	0.1u/6/Y/25V	EXP A TXP3C
EXP A TXN3	C77	0.1u/6/Y/25V	EXP A TXN3C
EXP A TXP4	C78	0.1u/6/Y/25V	EXP A TXP4C
EXP A TXN4	C79	0.1u/6/Y/25V	EXP A TXN4C
EXP A TXP5	C80	0.1u/6/Y/25V	EXP A TXP5C
EXP A TXN5	C81	0.1u/6/Y/25V	EXP A TXN5C
EXP A TXP6	C82	0.1u/6/Y/25V	EXP A TXP6C
EXP A TXN6	C83	0.1u/6/Y/25V	EXP A TXN6C
EXP A TXP7	C84	0.1u/6/Y/25V	EXP A TXP7C
EXP A TXN7	C85	0.1u/6/Y/25V	EXP A TXN7C
EXP A TXP8	C86	0.1u/6/Y/25V	EXP A TXP8C
EXP A TXN8	C87	0.1u/6/Y/25V	EXP A TXN8C
EXP A TXP9	C88	0.1u/6/Y/25V	EXP A TXP9C
EXP A TXN9	C89	0.1u/6/Y/25V	EXP A TXN9C
EXP A TXP10	C90	0.1u/6/Y/25V	EXP A TXP10C
EXP A TXN10	C91	0.1u/6/Y/25V	EXP A TXN10C
EXP A TXP11	C92	0.1u/6/Y/25V	EXP A TXP11C
EXP A TXN11	C93	0.1u/6/Y/25V	EXP A TXN11C
EXP A TXP12	C94	0.1u/6/Y/25V	EXP A TXP12C
EXP A TXN12	C95	0.1u/6/Y/25V	EXP A TXN12C
EXP A TXP13	C96	0.1u/6/Y/25V	EXP A TXP13C
EXP A TXN13	C97	0.1u/6/Y/25V	EXP A TXN13C
EXP A TXP14	C98	0.1u/6/Y/25V	EXP A TXP14C
EXP A TXN14	C99	0.1u/6/Y/25V	EXP A TXN14C
EXP A TXP15	C100	0.1u/6/Y/25V	EXP A TXP15C
EXP A TXN15	C101	0.1u/6/Y/25V	EXP A TXN15C

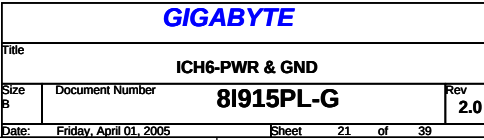


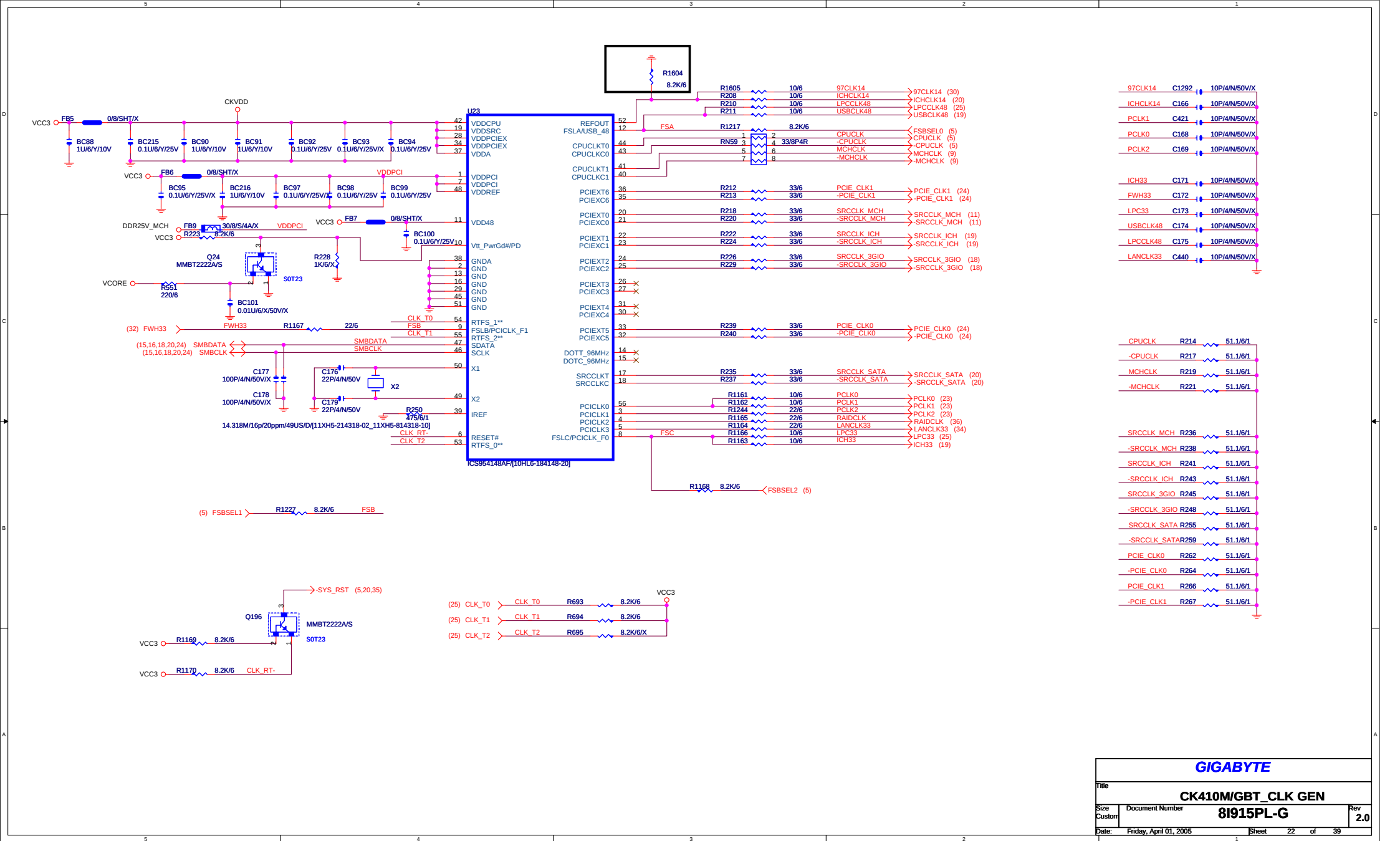


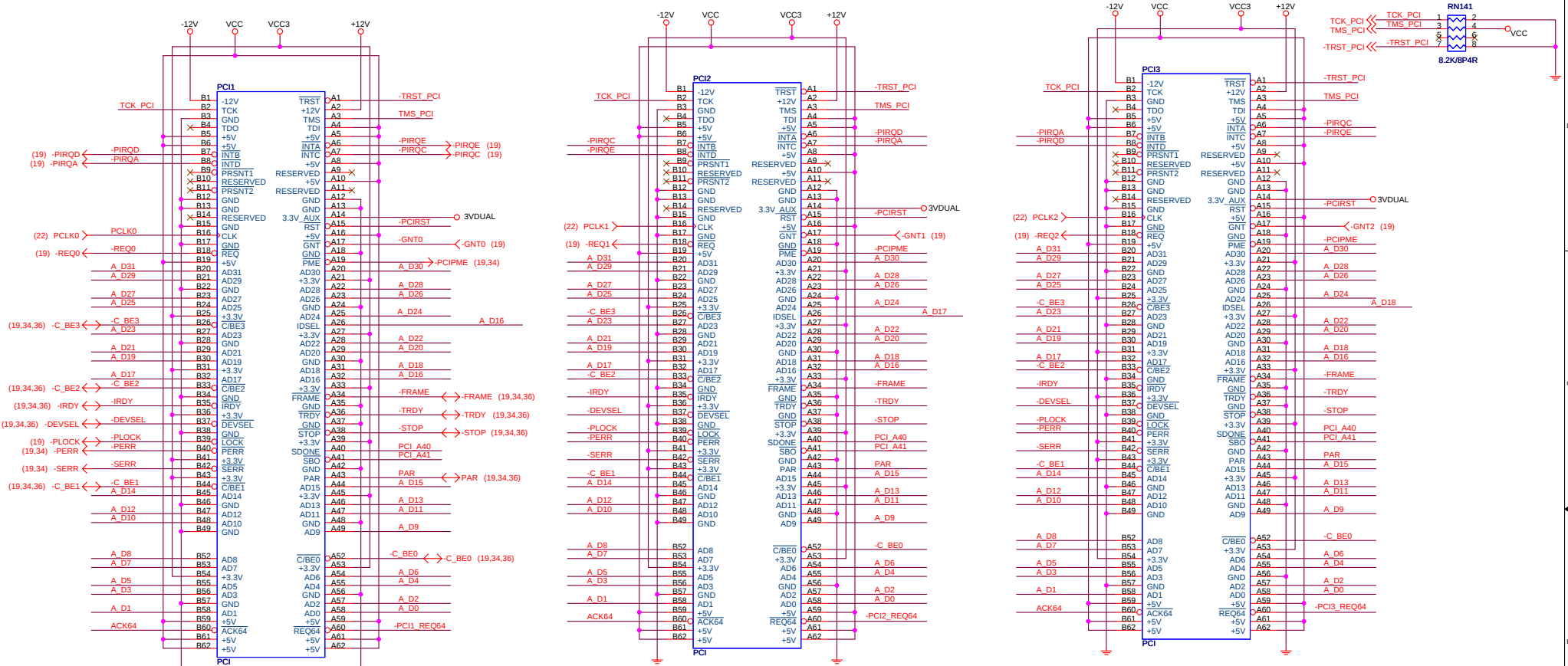
DMI Connection Note
GMCH TX Pin Need Connect to ICH6 RX Pin
ICH6 TX Pin Need Connect to GMCH RX Pin











AD16/-PIRQ(E-D-C-A)/-REQ0/-GNT0

(19,34,36) A_D[0..31] <-> A_D[0..31]

-PCIRST <-> PCIRST (19)

C180
33P/4N/50V/X

Place close to PCI1

(19,36) -REQ4 <-> -REQ4
(19) -REQ2 <-> -REQ2
(19,34) -REQ3 <-> -REQ3
(19) -REQ1 <-> -REQ1

(19,34,36) PAR <-> PAR
(19) -REQ6 <-> -REQ6
(19) -REQ5 <-> -REQ5
(19) -REQ0 <-> -REQ0

VCC <-> VCC
ACK64 <-> ACK64
PC13_REQ64 <-> PC13_REQ64
PC11_REQ64 <-> PC11_REQ64
PC12_REQ64 <-> PC12_REQ64

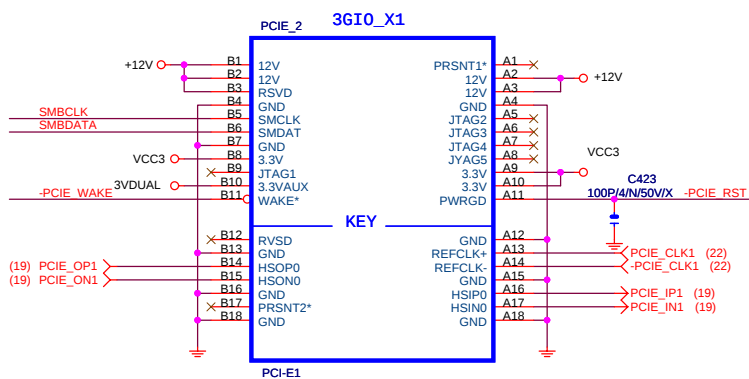
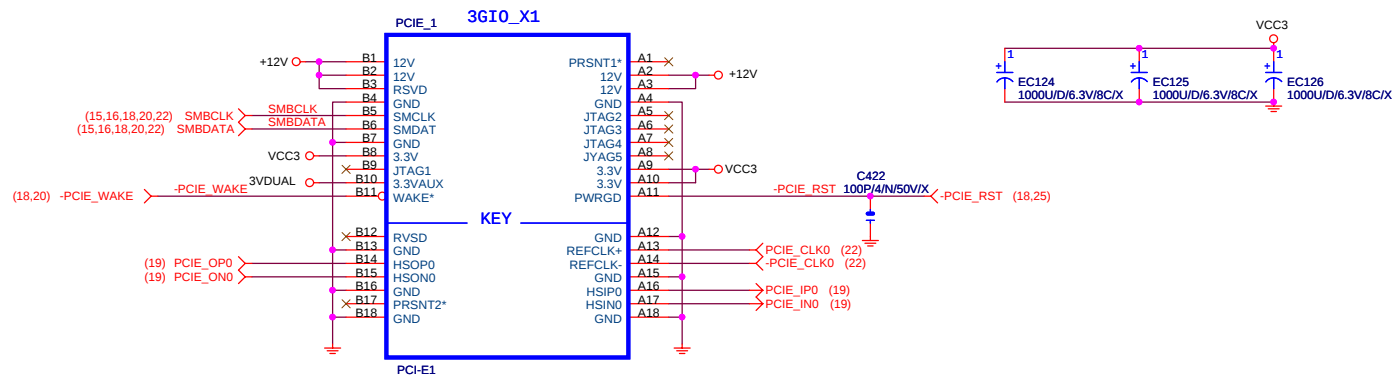
(19,36) -REQ4 <-> -REQ4
(19) -REQ2 <-> -REQ2
(19,34) -REQ3 <-> -REQ3
(19) -REQ1 <-> -REQ1

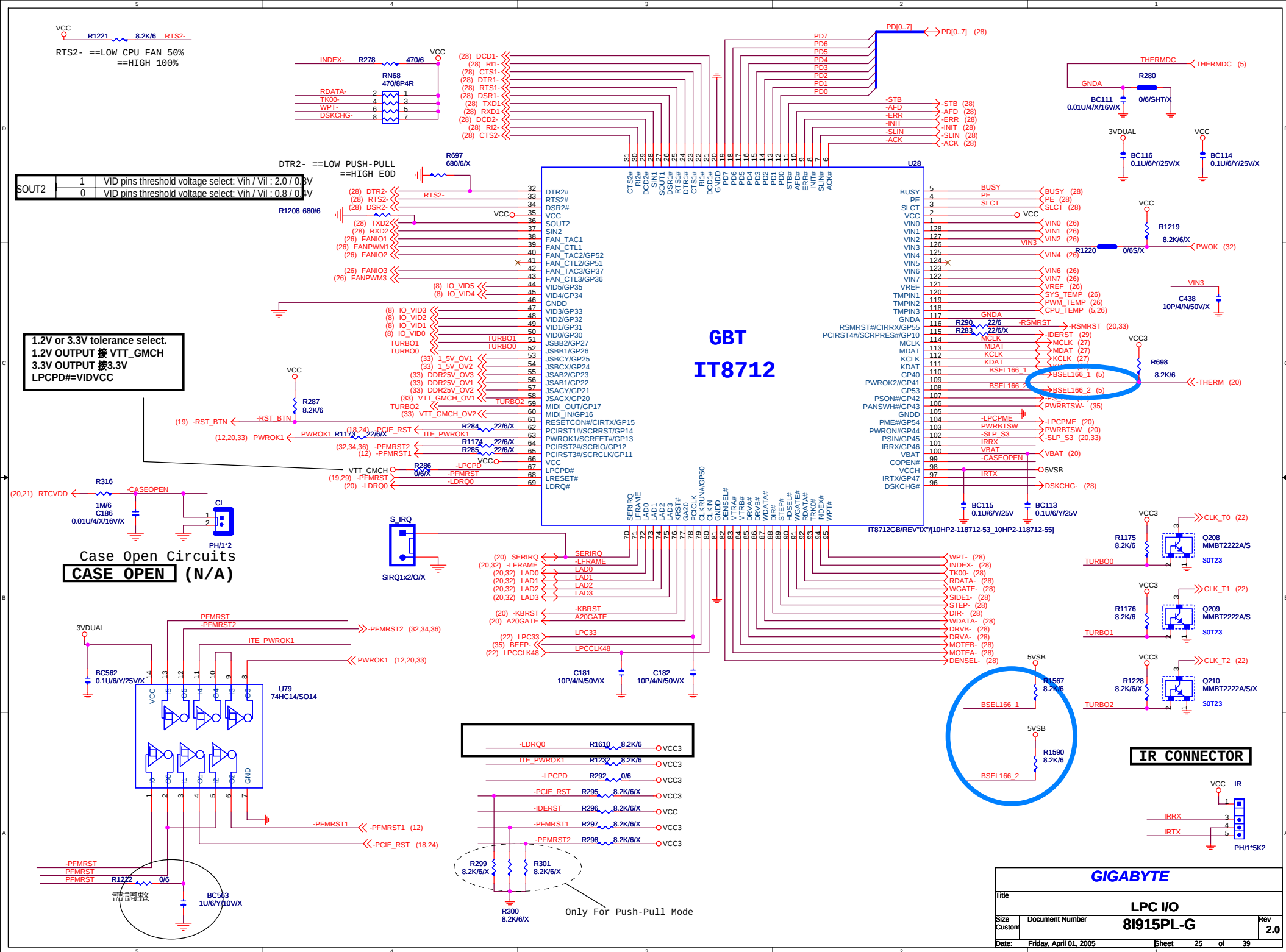
(19,34,36) PAR <-> PAR
(19) -REQ6 <-> -REQ6
(19) -REQ5 <-> -REQ5
(19) -REQ0 <-> -REQ0

VCC <-> VCC
ACK64 <-> ACK64
PC13_REQ64 <-> PC13_REQ64
PC11_REQ64 <-> PC11_REQ64
PC12_REQ64 <-> PC12_REQ64

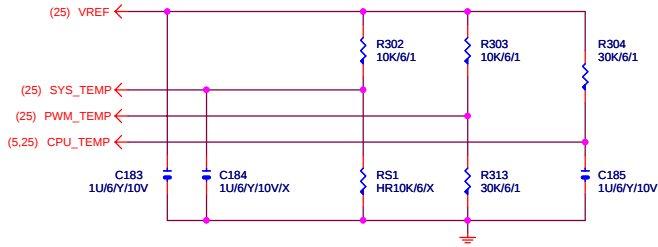
VCC <-> VCC
EC68
1000U/D/6.3V/8C/X

GIGABYTE			
PCI SLOT			
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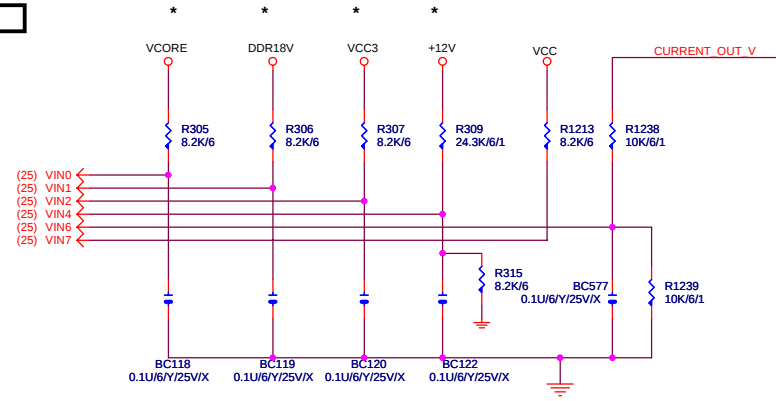




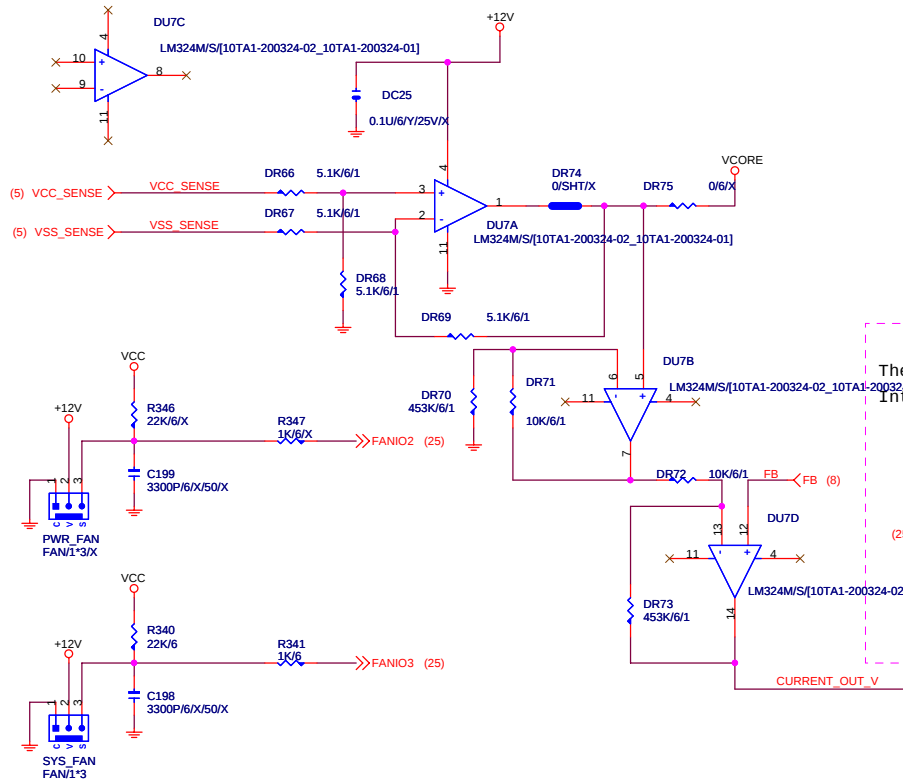
TEMP. SENSE



VOLTAGE SENSE



DUAL POWER



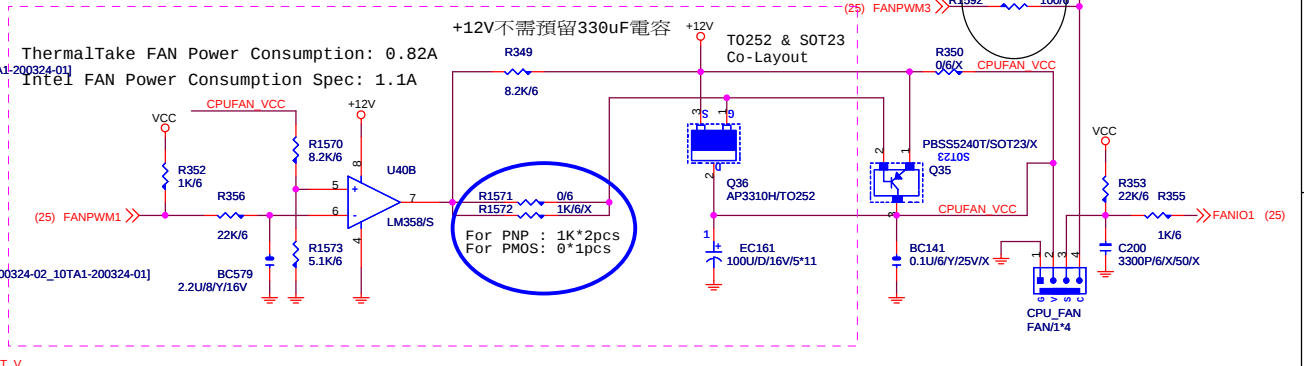
CPU/SYS FAN

If use PBSS5240 1pcs : (non airflow)

CPUFAN_VCC=12V: Temp=40 deg
CPUFAN_VCC=11V: Temp=82 deg
CPUFAN_VCC=10V: Temp=70 deg
CPUFAN_VCC= 9V: Temp=110 deg
CPUFAN_VCC= 8V: Temp>200 deg

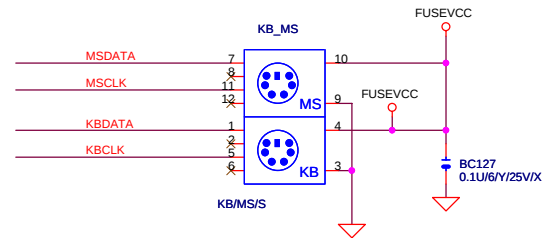
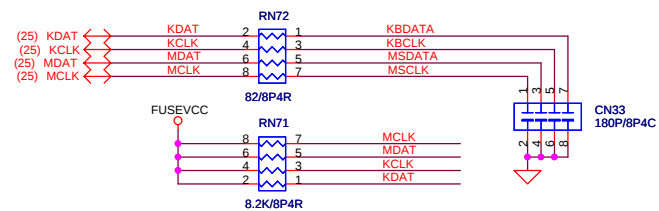
If use PBSS5240 1pcs : (with airflow)

CPUFAN_VCC=12V: Temp=33 deg
CPUFAN_VCC=11V: Temp=62 deg
CPUFAN_VCC=10V: Temp=86 deg
CPUFAN_VCC= 9V: Temp=117 deg
CPUFAN_VCC= 8V: Temp>122 deg

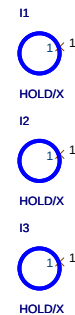
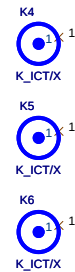
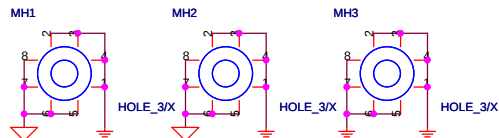
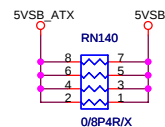
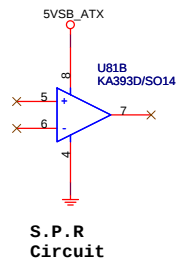
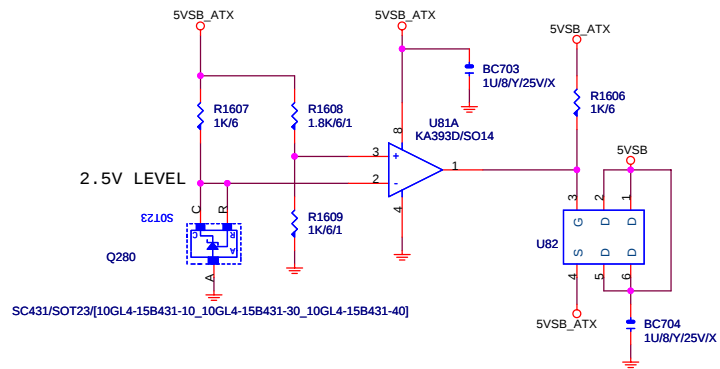


GIGABYTE			
Title			
HWM/FAN/C/BIOS			
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KB/MS



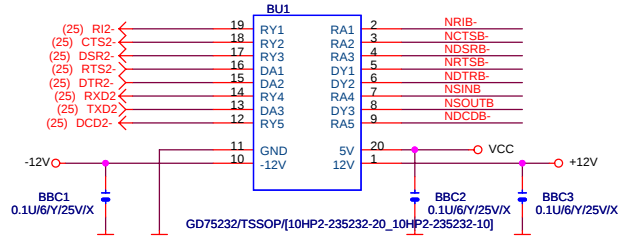
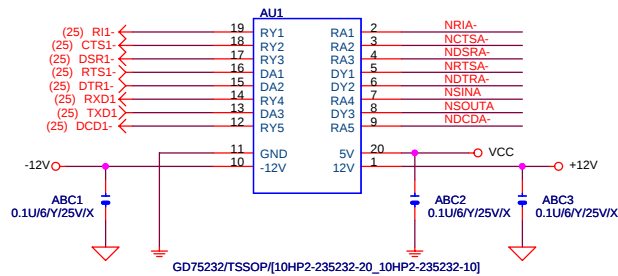
S.P.P.



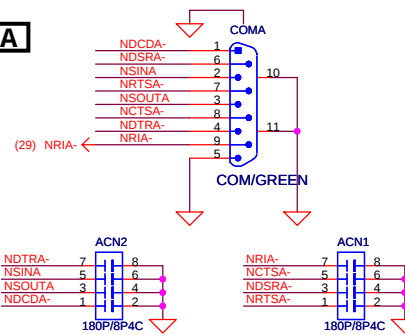
GIGABYTE

Title		
PS/2 KB & MS		
Size B	Document Number	Rev
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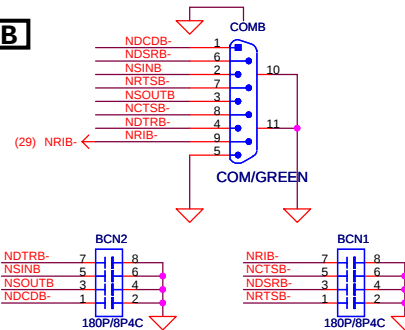
COMA/COMB



COMA

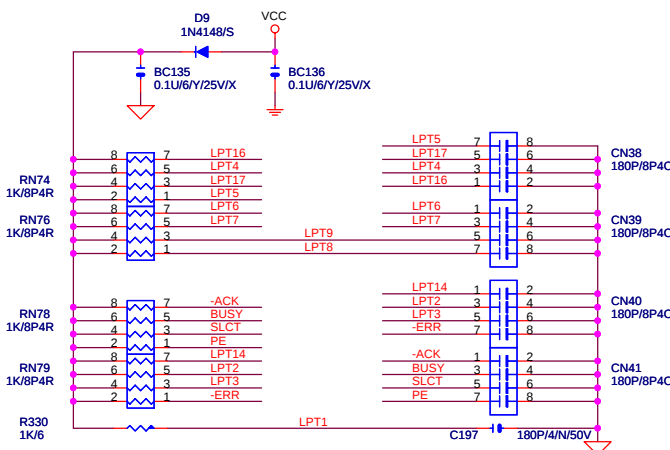
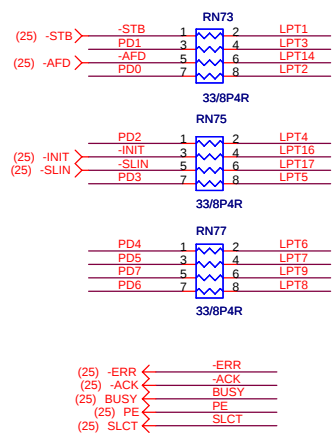


COMB

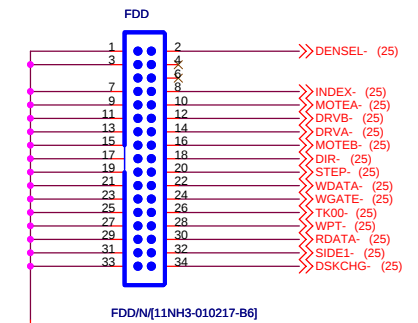


LPT

(25) PD[0..7] PD[0..7]



FLOPPY



GIGABYTE

Title		
COM, LPT, FDD		
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[illegible]

The left diagram illustrates four fuse options for USB lines. Each option (Q229, Q230, Q231, Q232) shows a fuse connected between the USB lines and FUSEVCC. The USB lines are labeled as (19) -USBP5, (19) +USBP5, (19) -USBP4, and (19) +USBP4. The fuse is connected to FUSEVCC and ground.

The right diagram illustrates an EMI filter circuit. It shows a USB/S component connected to the USB lines. A BC702 varistor (0.1uF/25V/X) is connected between the USB lines and FUSEVCC. The circuit is labeled "FOR EMI".

The image displays two PCB layout sections for USB connectors. The top section, labeled 'REAR USB', shows a signal trace from a 5VDUAL pin, passing through a capacitor BC201 (0.1U/6/Y/25V/X) to ground, and then through a via F1 (80MILS) to a FUSEVCC pin, which also has a capacitor BC200 (0.1U/6/Y/25V/X) to ground. The bottom section, labeled 'FRONT USB', shows a similar setup with 5VDUAL and VCC pins, capacitors BC201 and BC202, and vias F4 and F5. A yellow oval highlights the area around vias F4 and F5, which are connected to a common signal line. The traces are labeled with dimensions like '80MILS' and component values like 'PSR24251/D/O[11FP1-30250B-21_11FP1-30250B-04_11FP1-30250B-12]'.

(28) NR1A-
(28) NR1B-
BAT54C/S/[10DK1-200054-12_10DK1-200054-13_10DK1-200054-14]
D21
R335 75K/6
R336 8.2K/6
Q25 MMBT2222A/S
S0T23
-RI
-RI (20)

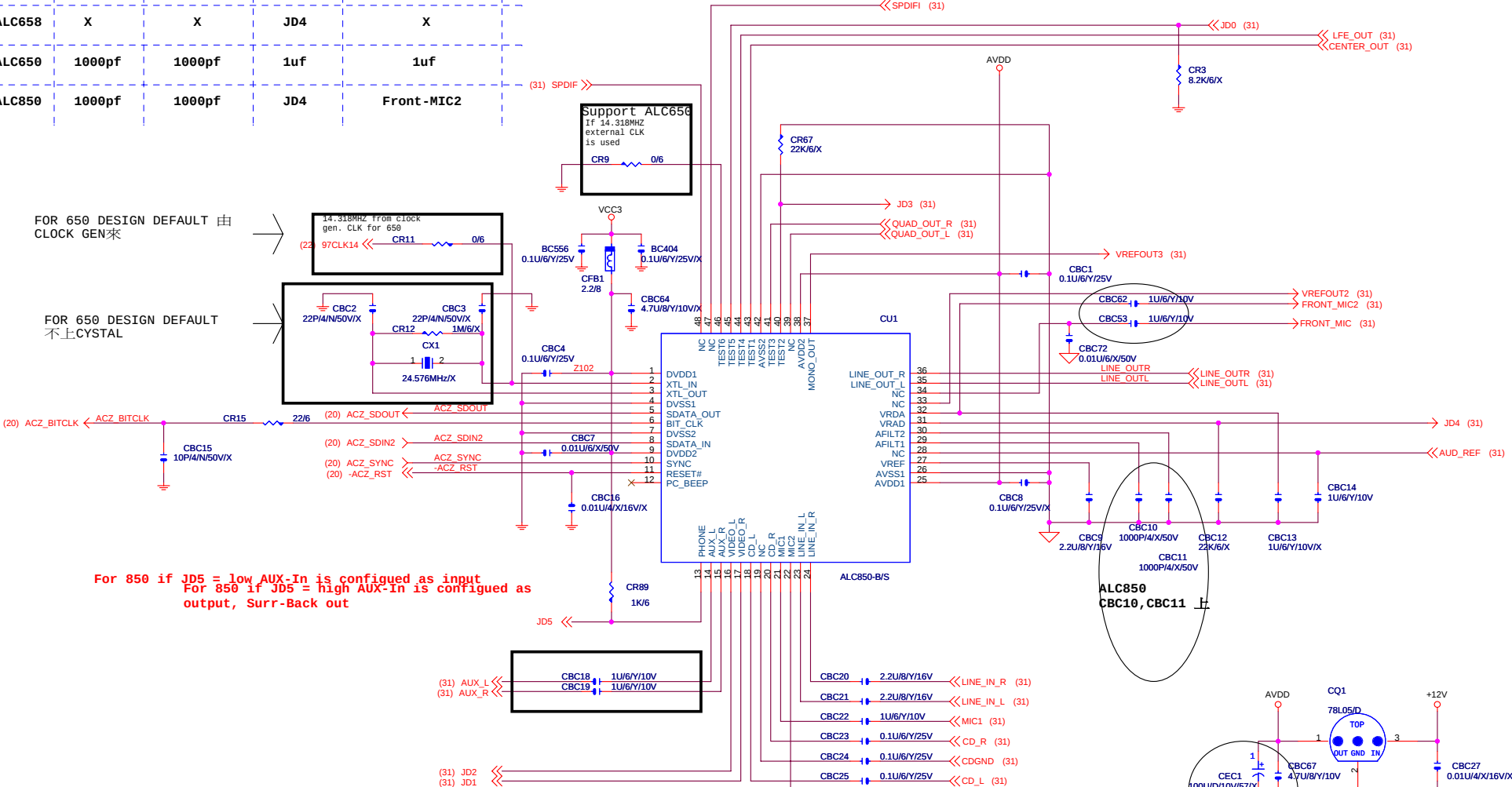
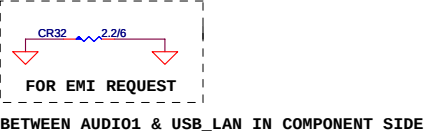
PRIMARY IDE CONNECTOR

CH3

GIGABYTE			
Title			
FRONT/REAR USB CONNECTOR/IDE			
Size	Document Number	8I915PL-G	
Custom			Rev 2.0

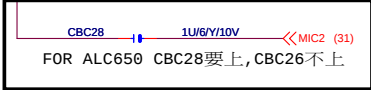
Filter Cap design:

	Pin-29	Pin-30	Pin-31	Pin-32
ALC655 Rev D	1000pf	1000pf	1uf	Front-MIC2
ALC655 Rev C	1000pf	1000pf	1uf	X
ALC658	X	X	JD4	X
ALC650	1000pf	1000pf	1uf	1uf
ALC850	1000pf	1000pf	JD4	Front-MIC2



Arrangement of Jack detection Pin:

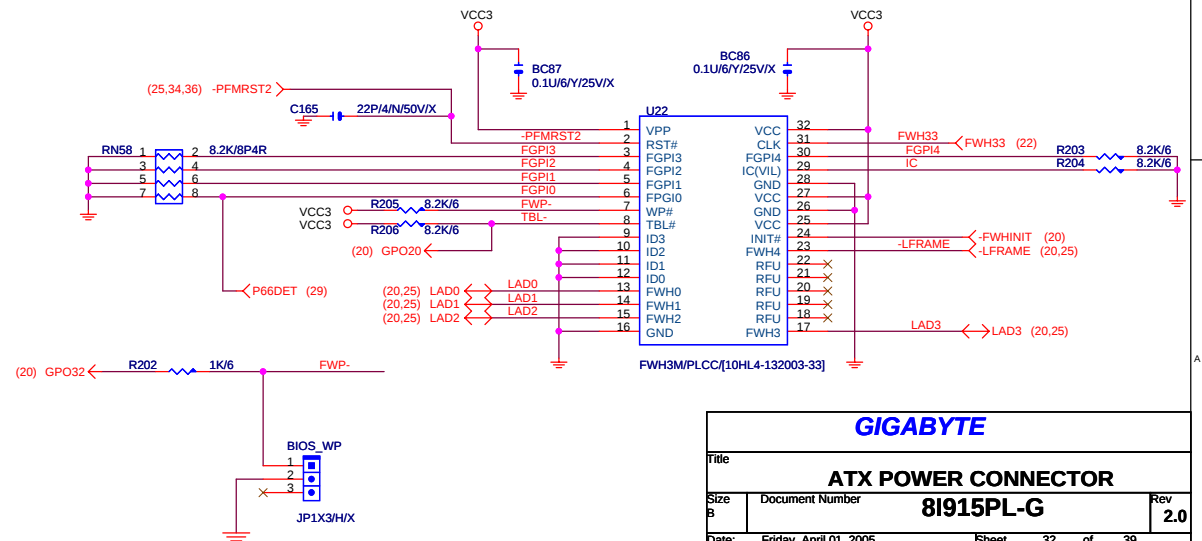
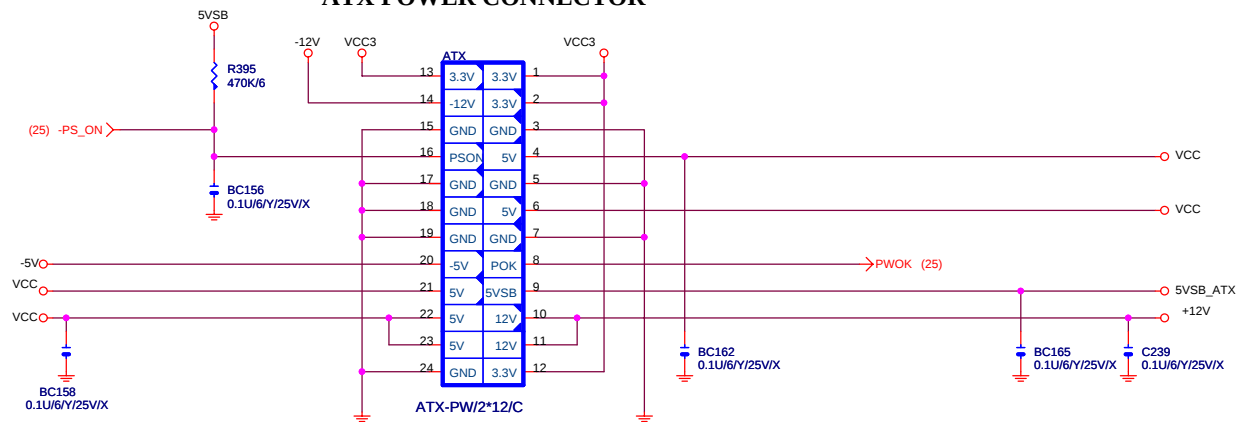
	Pin-45(JD0)	Pin-17(JD1)	Pin-16(JD2)	Pin-40(JD3)	Pin-31(JD4)	Pin-13(JD5)
ALC655	for MIC-IN	for FRONT-OUT	for LINE-IN			
ALC658	for MIC-IN	for UAJ1	for UAJ2	for FRONT-OUT External pull high is needed	for LINE-IN External pull high is needed	
ALC850	for MIC-IN	for Front Pannel OUT	for Front Pannel IN	for FRONT-OUT	for LINE-IN	for SurrBack Out



For 850 if JD5 = low AUX-In is configured as input
For 850 if JD5 = high AUX-In is configured as output, Surr-Back out

U22_BIOS_SOCKET

BIOS_SOCKET/X

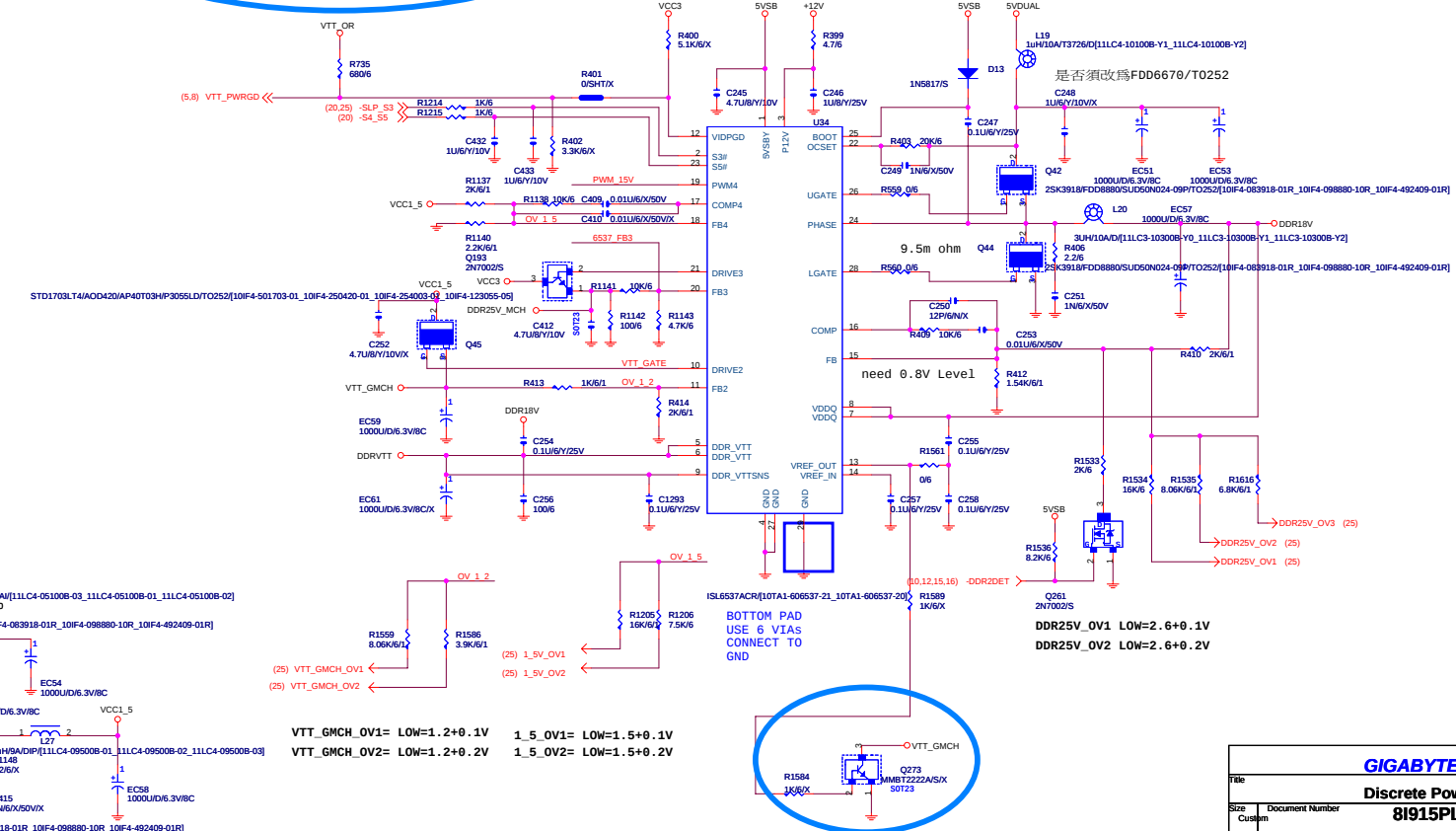
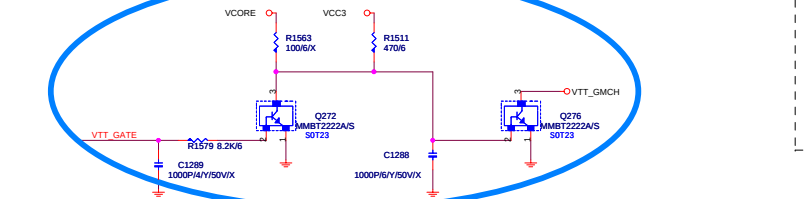


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Title			
ATX POWER CONNECTOR			
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[illegible][illegible]

APL1084/20252[10GL6-501084-02_10GL6-501084-04_10GL6-501084-05_10GL6-501084-07]



VTT_GMCH_OV2= LOW=1.2+0.2V

1_5_0V2= LOW=1.5+0.2V

1_5_0V2= LOW=1.5+0.2V

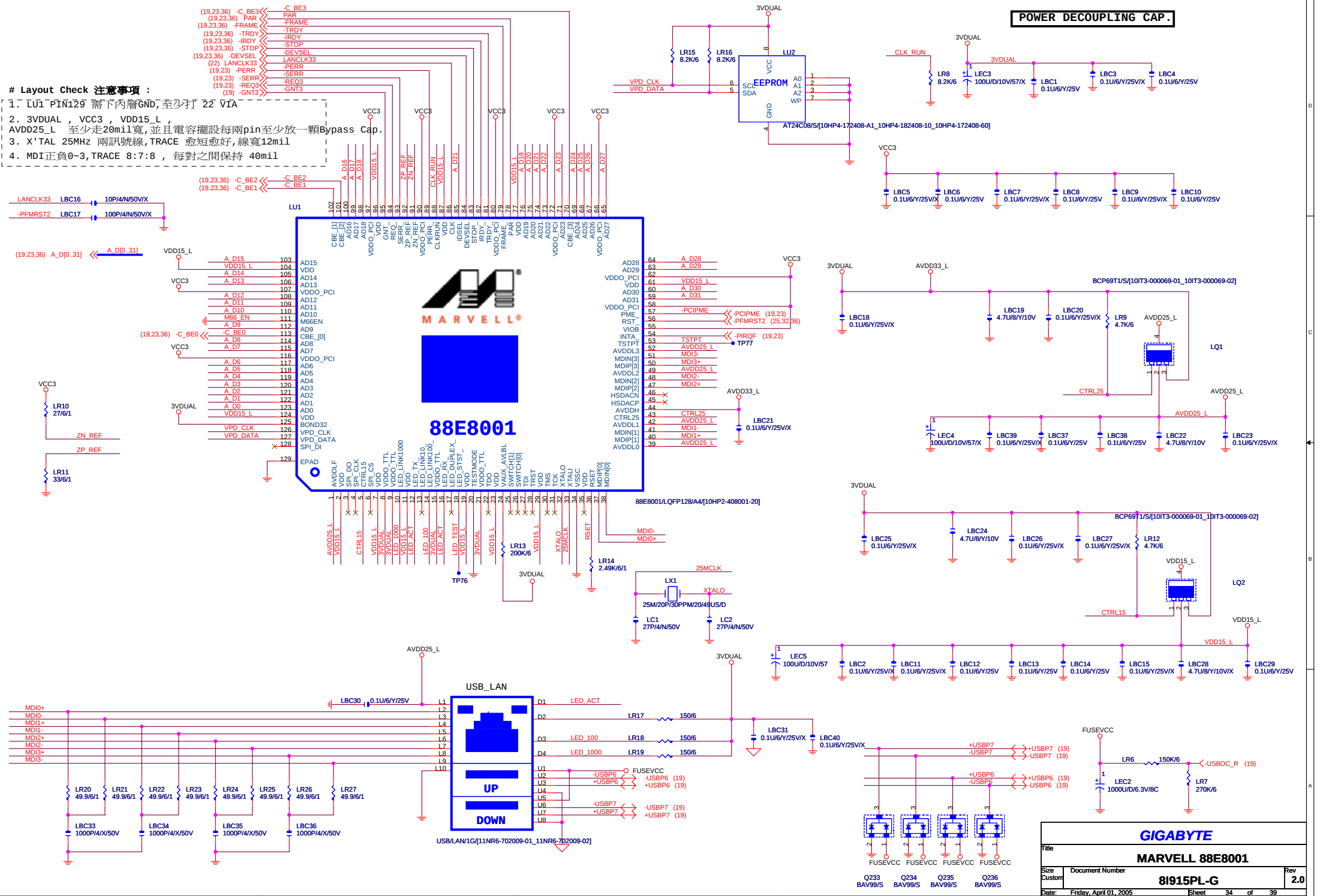
DDR25V_OV2 LOW=2.6+0.2V

Discrete Power

8I915PL-G

2.0

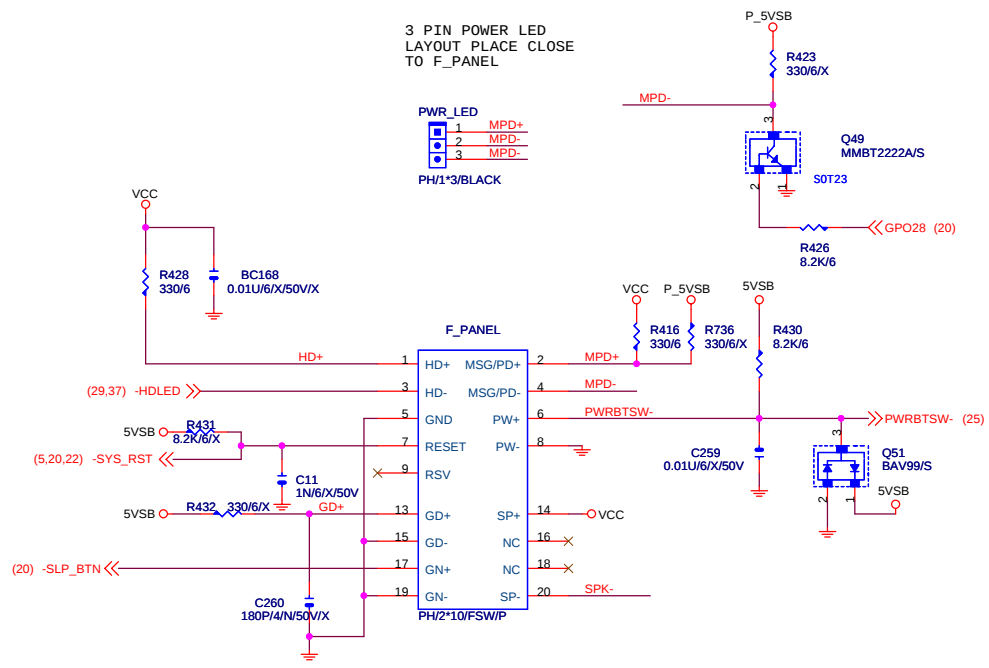
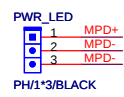
- # Layout Check 注意事項：
1. LU1 PIN129 需下內層GND,至少打 22 VIA
 2. 3VDUAL , VCC3 , VDD15_L , AVDD25_L 至少走20mil寬,並且電容擺設每兩pin至少放一顆Bypass Cap.
 3. X'TAL 25MHz 兩訊號線,TRACE 愈短愈好,線寬12mil
 4. MDI正負0-3,TRACE 8:7:8 , 每對之間保持 40mil



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MARVELL 88E8001			
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INTEL FRONT PANEL

3 PIN POWER LED
LAYOUT PLACE CLOSE
TO F_PANEL

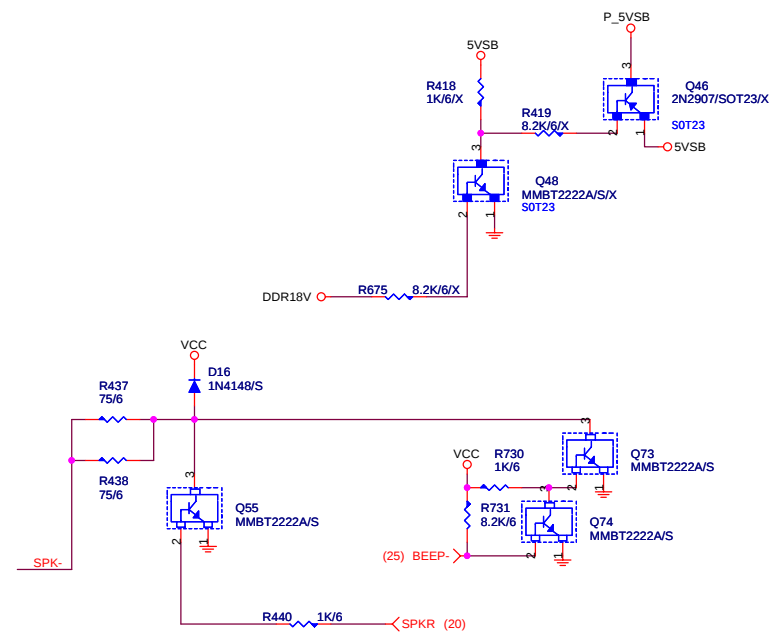
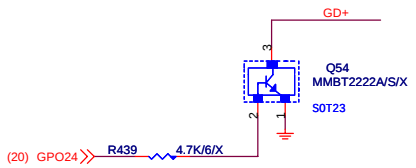
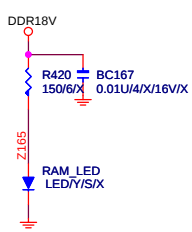
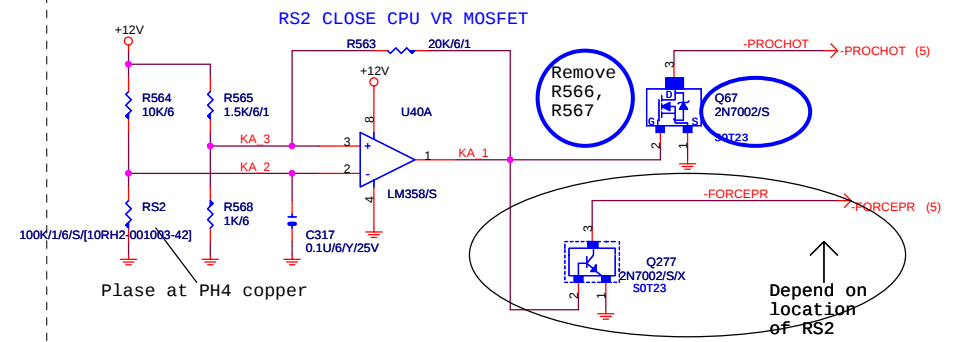


PROCESSOR HOT

(N/A)

如果要用2N7002需注意OP output
H1時的電壓是否遠大於2V。

asserted at 130 degree (RS2=720 ohm)
deasserted at 115 degree (RS2=1270 ohm)
KA393改為LM358，電源pin改接+12V，Prochot#溫度需重新調整之。



States for green LED N01 GP022 only S1 PROGRAMMING LOW

LED States	ACPI States	GP028
ON	S1,S3	0
OFF	S0,S5	1

(GP022 DEFAULT HIGH, main power)

States for a single-color power LED

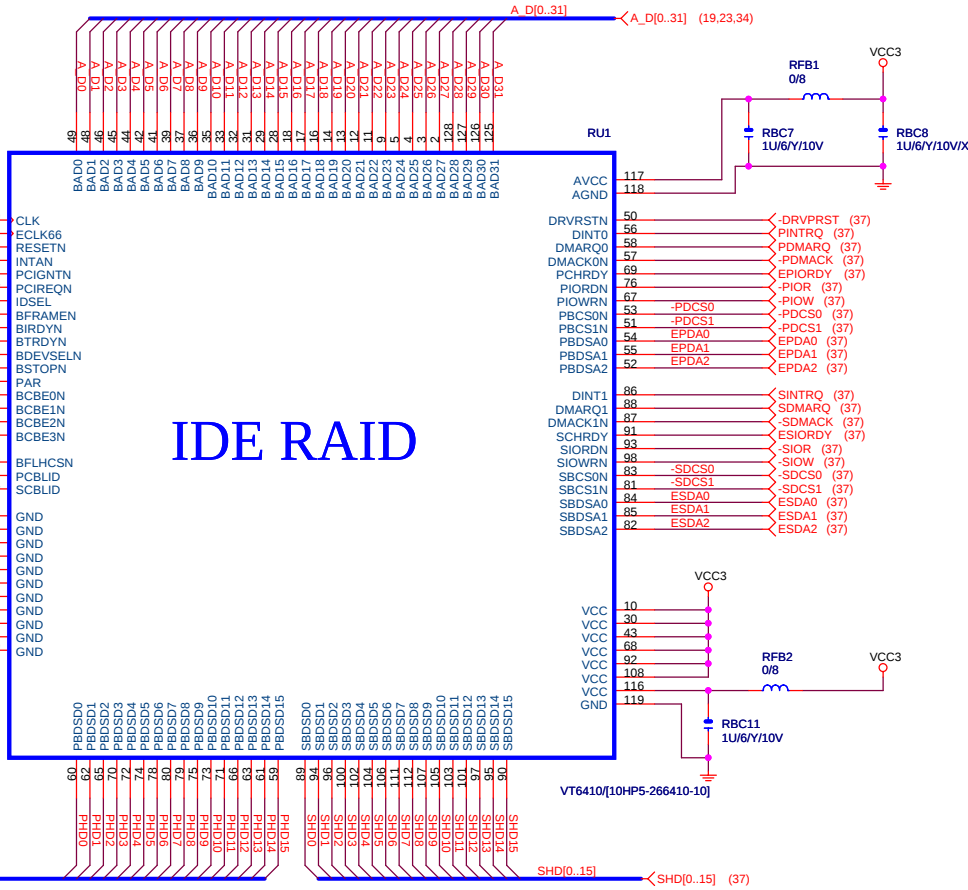
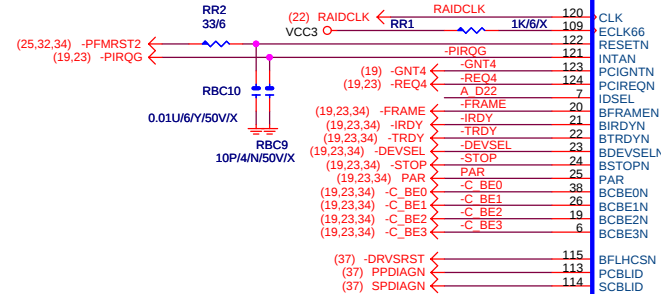
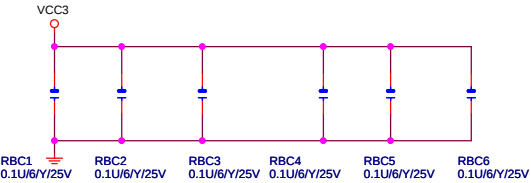
LED States	ACPI States	GP025	GP027	GP024
OFF	S1,S3,S5	1	1	N01
Steady Green	S0	1	1	1
Blinking Green	S0(message waiting)	1	0	1

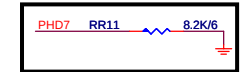
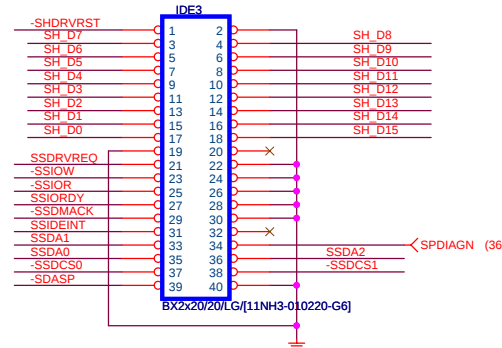
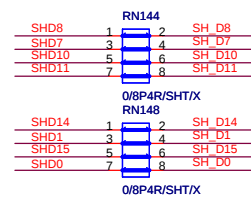
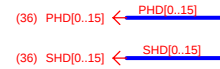
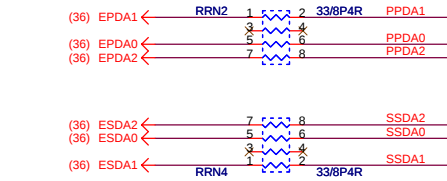
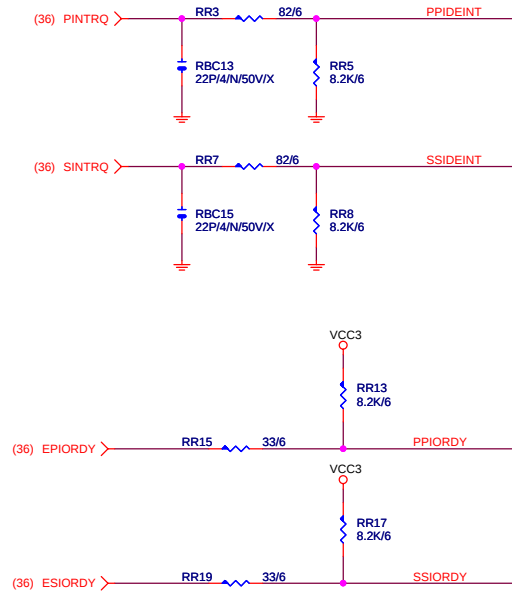
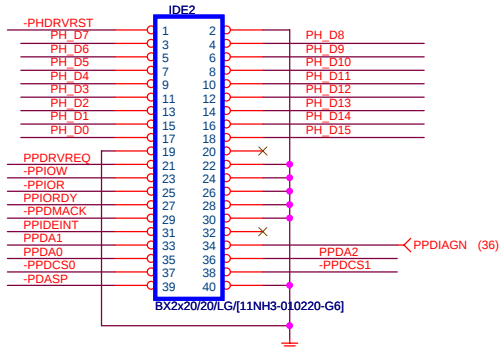
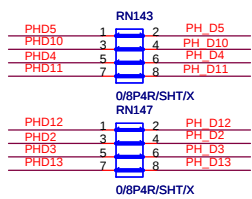
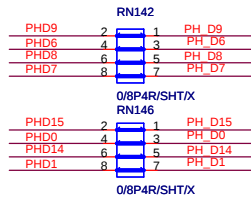
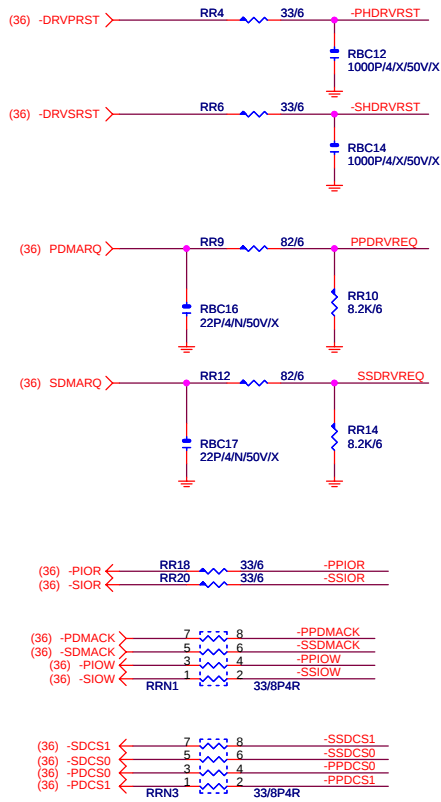
LED States	ACPI States	GP025	GP027	GP022
OFF	S5	1	1	X
Steady Green	S0	1	1	1
Blinking Green	S0(message waiting)	1	0	1
Steady Yellow	S1,S3	1	0	N01
Blinking Yellow	S1,S3(message waiting)	1	0	N01

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ALL INPUT PIN MUST HAVE 0.1 CAPACITOR





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紅字表示CPI/O 同PIN

GPO PIN

Pin Name	Pin Type	Power Well			GPIO Application
GPI[0]	Input	V5REF	-REQ[6]	(P.U VCC)	Reserved
GPI[5:2]	Input	V5REF	-PIRQ[H:E]	(P.U VCC)	PCI/LAN/NA/1394
GPI[6]	Input	VCC3	GPI[6]	(P.U VCC3)	-SLP_BTN
GPI[7]	Input	VCC3	GPI[7]	(NA)	DUALBIOS_INPUT
GPI[8]	Input	3VDUAL	GPI[8]	(P.U 3VDUAL)	-LANWAKE
GPI[10:9]	Input	3VDUAL	0C_4/5	(P.U 5VDUAL分壓)	-USB0C_R
GPI[11]	Input	3VDUAL	-SMBALERT	(P.U 3VDUAL)	-SMBALRT
GPI[12]	Input	VCC3	GPI[12]	(P.U VCC3)	ATX24_DET
GPI[13]	Input	3VDUAL	GPI[13]	(P.U 3VDUAL)	-LPCPME
GPI[15:14]	Input	3VDUAL	0C_6/7	(P.U 5VDUAL分壓)	-USB0C_R
GPO[16]	OUTPUT	VCC3	-GNT[6]	(Integrated VCC3)	Reserved
GPO[17]	OUTPUT	VCC3	-GNT[5]	(Integrated VCC3)	Reserved
GPO[18]	OUTPUT	VCC3	GPO[18]	(P.U VCC3)	LANRST-
GPO[19]	OUTPUT	VCC3	GPO[19]	(P.U VCC3)	DUAL_BIOS_OUTPUT
GPO[20]	OUTPUT	VCC3	GPO[20]	(P.U VCC3)	TBL-
GPO[21]	OUTPUT	VCC3	GPO[21]	(P.U VCC3)	DUAL_BIOS_OUTPUT
GPO[22]	Not Implemented		Not Implemented		Not Implemented
GPO[23]	OUTPUT	VCC3	GPO[23]	(P.U VCC3)	LANRST-
GPO[24]	IN/OUT	3VDUAL	GPO[24]	(NA)	GREEN_LED
GPO[25]	IN/OUT	3VDUAL	vcc_25vregulator	(NA)	Reserved
GPI[26]	Input	VCC3	SATA[0]GP	(P.U VCC3)	SATA[0]GP
GPIO[27]	IN/OUT	3VDUAL	GPIO[27]	(NA)	Reserved
GPIO[28]	IN/OUT	3VDUAL	GPO[28]	(NA)	PWD_LED
GPI[29]	Input	VCC3	SATA_1GP	(P.U VCC3)	SATA_1GP
GPI[30]	Input	VCC3	SATA_2GP	(P.U VCC3)	SATA_2GP
GPI[31]	Input	VCC3	SATA_3GP	(P.U VCC3)	SATA_3GP
GPIO[32]	IN/OUT	VCC3	GPO[32]	(NA)	FWP-
GPIO[33]	IN/OUT	VCC3	GPI[33]	(P.U VCC3)	-ACZ_DET
GPIO[34]	IN/OUT	VCC3	GPIO[34]	(P.U VCC3)	MB_ID0
GPI[40]	Input	V5REF	-REQ[4]	(P.U VCC)	-REQ[4]
GPI[41]	Input	VCC3	GPI[41]	(P.U VCC3)	MB_ID1
GPO[48]	OUTPUT	VCC3	-GNT[4]	(Integrated VCC3)	Reserved
GPO[49]	OD O	V_CPU_IO	CPUPWROK	(P.U VTT_OR)	CPUPWROK
GPIO[35-39,42-47]		NOT IMPLEMENTED		NOT IMPLEMENTED	

[illegible]**GIGABYTE**

GPIO TABLE

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ICH6 GPIO Table:

NAME	PWR LANE	USAGE	NAME	PWR LANE	USAGE
GPI0	V5REF	M/B ID (-REQ6)	GPI41	VCC3	M/B ID
GPI1	V5REF	-REQ5	GP048	VCC3	-GNT4
GPI2	V5REF	-PIRQE	GP049	V-CPUIO	CPUPWOK
GPI3	V5REF	-PIRQF			
GPI4	V5REF	-PIRQG			
GPI5	V5REF	-PIRQH			
GPI6	VCC3	-SLP BTN			
GPI7	VCC3	DUAL BIOS			
GPI8	3VDAUL	-LANWAKE			
GPI9	3VDAUL	-USBOC4			
GPI10	3VDAUL	-USBOC5			
GPI11	3VDAUL	-SMBALT			
GPI12	VCC3	ATX DET			
GPI13	3VDAUL	-LPCPME			
GPI14	3VDAUL	-USBOC6			
GPI15	3VDAUL	-USBOC7			
GP016	VCC3	CPU OV1 (-GNT6)			
GP017	VCC3	-GNT5			
GP018	VCC3	CPU OV2			
GP019	VCC3	DUAL BIOS			
GP020	VCC3	BIOS T-BLOCK			
GP021	VCC3	DUAL BIOS			
GP023	VCC3	DDR OV0			
GPI024	3VDAUL	GREEN LED			
GPI025	3VDAUL	DDR OV1			
GPI26	VCC3	SATA GP0			
GPI027	3VDAUL	+PWRLED			
GPI028	3VDAUL	-PWRLED			
GPI29	VCC3	SATA GP1			
GPI30	VCC3	SATA GP2			
GPI31	VCC3	SATA GP3			
GPI032	VCC3	BIOS WP			
GPI033	VCC3	AZALIA DET			
GPI034	VCC3	M/B ID			
GPI40	V5REF	-REQ4			

PWR0K/RESET Table:

ITE8712BHX PIN	NET NAME	TARGET
PIN62/-PCIRST1	-PCIE_RST	1. PCI-E * 1 Slot1 2. PCI-E * 1 Slot2 3. PCI-E * 1 Slot3 4. PCI-E * 16 Slot
PIN64/-PCIRST2	-PFMRST2	1. Onboard PCI Lan 2. Onboard 1394 Chip 3. OnBoard FWH
PIN65/-PCIRST3	-PFMRST1	1. Onboard PCI-E Lan 2. Onboard SATA Chip 3. GMCH
PIN115/-PCIRST4	-PFMRST_ -IDERST	Reserved For IDE
PIN63/PWROK1	PWROK1	1. GMCH 2. ICH6 3. 5VDUAL SWITCH 4. DPS CONTROL
PIN109/PWROK2	-THERM	1. ICH6

GIGABYTE THCNOLOGIES , INC.

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