

Model Name: 965GM-S2

Revision 1.01

SHEET TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	POWER MAP
05	P4_LGA775_A
06	P4_LGA775_B
07	P4_LGA775_C
08	P4_LGA775_D
09	GMCH-BROADWATER_HOST
10	GMCH-BROADWATER_DDRII
11	GMCH-BROADWATER_PCI E, DMI
12	GMCH-BROADWATER_INT VGA
13	GMCH-BROADWATER_GND
14	GMCH-BROADWATER_PWR
15	DDRII CHANNEL A 1,2
16	DDRII CHANNEL B 1,2
17	DDRII TERMINATION
18	PCI EXPRESS*16 SLOT
19	ICH8 PCI, USB, DMI, LAN
20	ICH8 GPIO, CTRL
21	ICH8 SATA, FAN PWM
22	ICH8 VCC, GND
23	CLOCK GEN CK505
24	PCI EXPRESS*1 ,PCI SLOT 1,2
25	ITE8718GB,RESET DRIVE
26	COM,LPT
27	BIOS,CI,HWM,KB/MS

SHEET TITLE

28	AZALIA ALC883
29	AUDIO JACK
30	VCORE PWM ISL6312
31	DISCRETE POWER
32	ATX POWER
33	JMicron 2S1P ATA
34	1394 TI TSB43AB23
35	LAN MARVELL 88E8056
36	FAN CONTROL
37	FRONT PANEL,FUSB,FDD

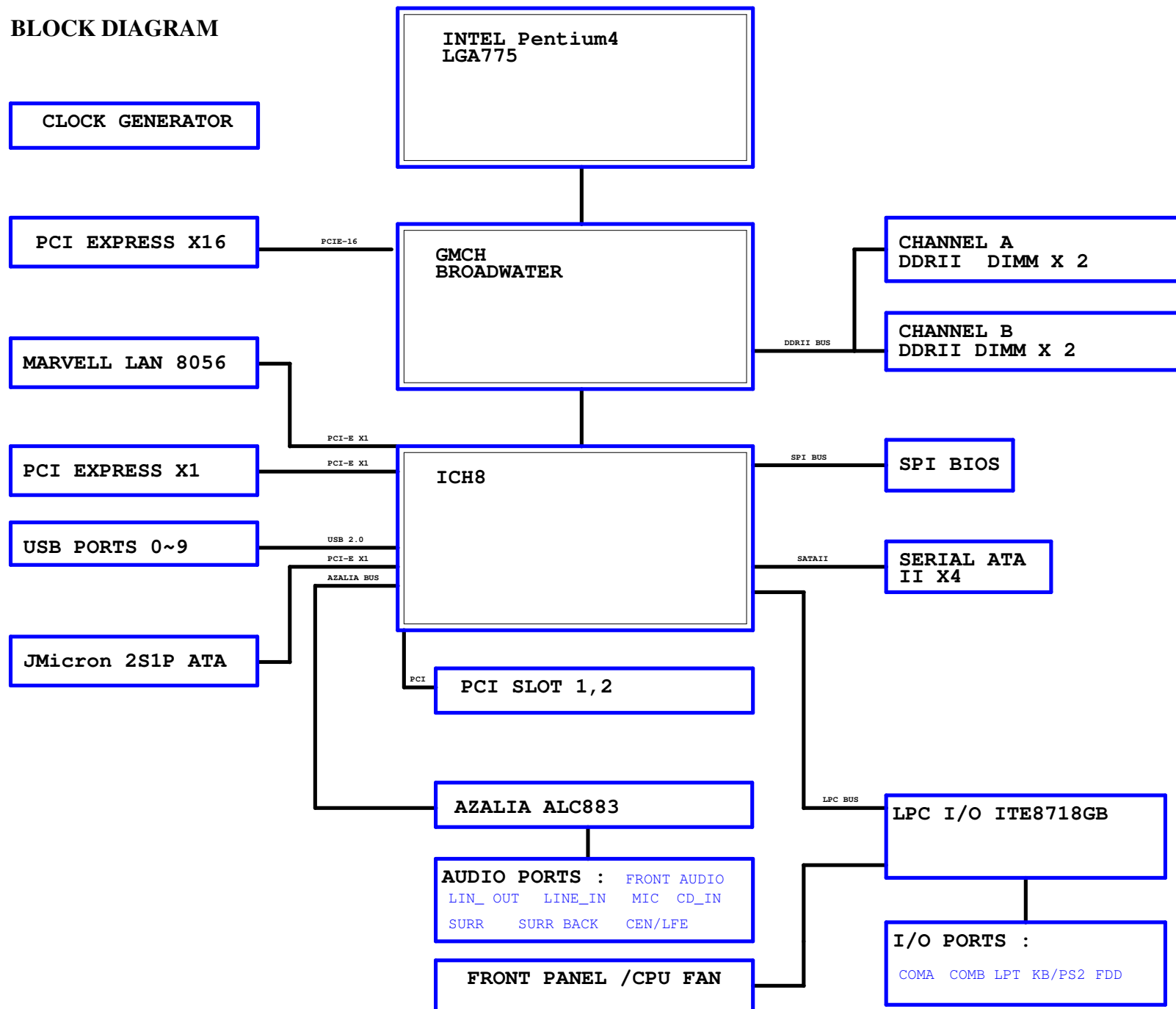
Gigabyte Technology			
Title			
Cover Sheet			
Size	Document Number	Rev	
Custom	965GM-S2	1.01	
Date:	Friday, August 18, 2006	Sheet	1 of 36

Version: 1.01

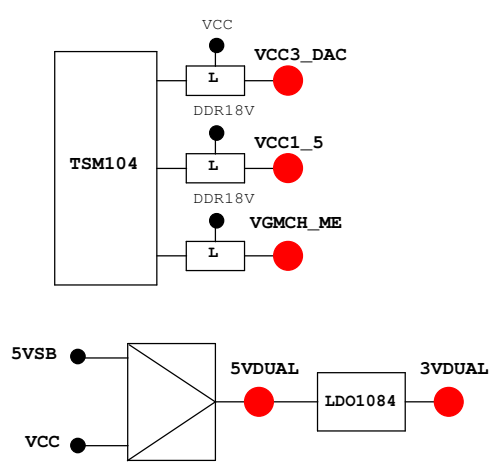
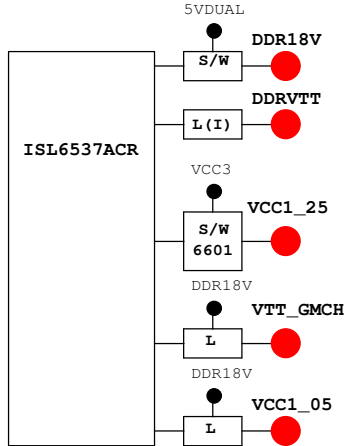
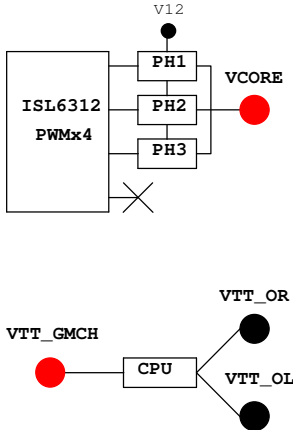
Component value change history

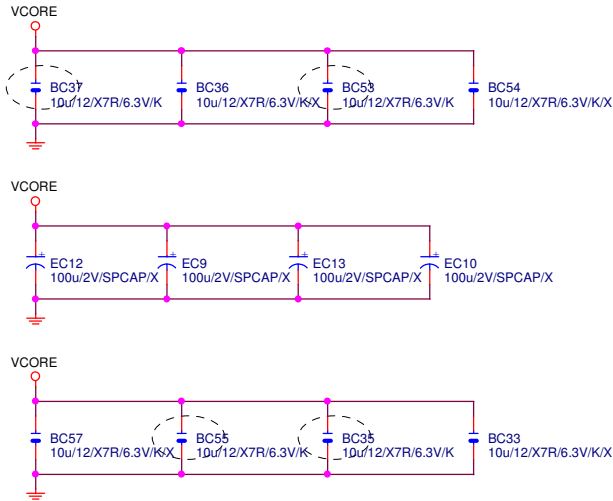
[illegible][illegible]

BLOCK DIAGRAM

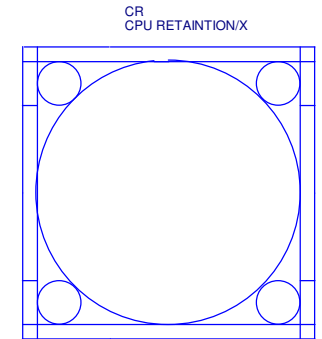
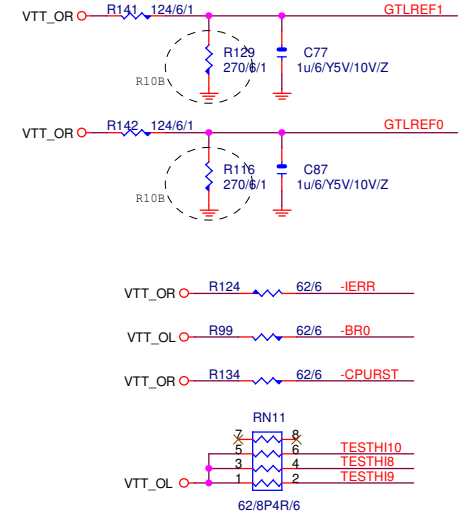
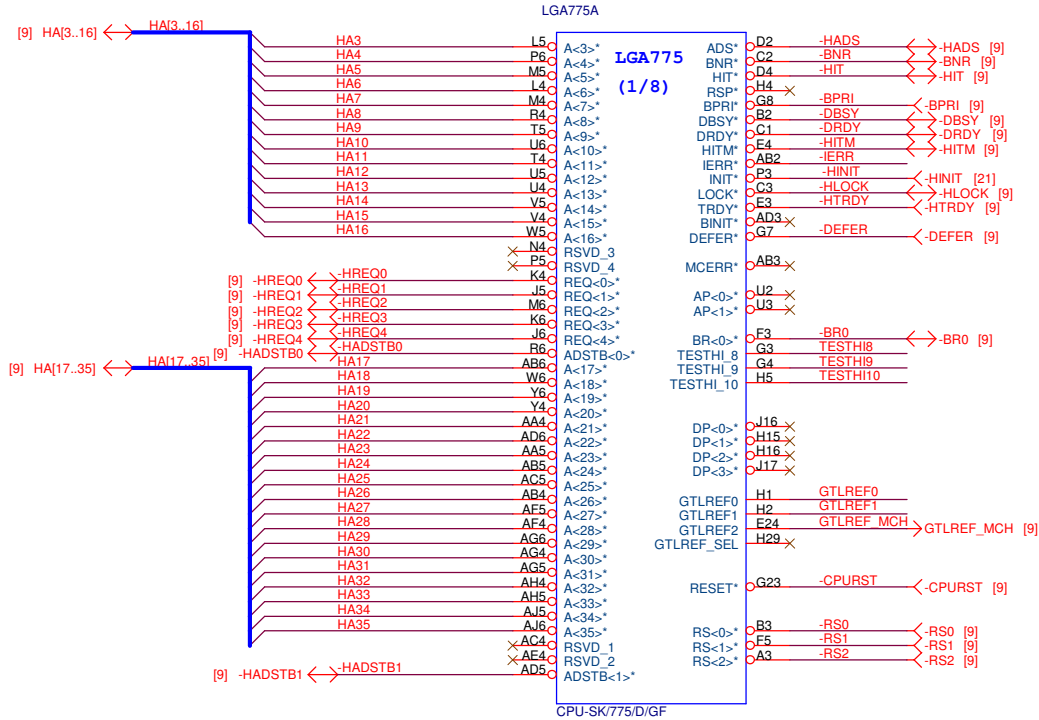


PIN NAME	PWR WELL	AFTER/ PLTRST	USAGE	NOTE
GP0	MAIN	IN	-ACZ_DET	P/U 8.2K VCC3
GP1/TACH1	MAIN	IN	N/A	P/U 8.2K VCC3
GP2/PIRQE#	MAIN	IN	-PIRQE	P/U 8.2K VCC3
GP3/PIRQF#	MAIN	IN	-PIRQF	P/U 8.2K VCC3
GP4/PIRQG#	MAIN	IN	-PIRQG	P/U 8.2K VCC3
GP5/PIRQH#	MAIN	IN	-PIRQH	P/U 8.2K VCC3
GP6/TACH2	MAIN	IN	N/A	P/U 8.2K VCC3
GP7/TACH3	MAIN	IN	N/A	P/U 8.2K VCC3
GP8	STBY	IN	GPIO8	P/U 8.2K 3VDUAL
GP9	STBY	OUT	WOL_ONLY	P/D 100K GND
GP10	STBY	OUT	GPIO10	P/U 8.2K 3VDUAL
GP11/SMBALERT#	STBY	OUT	-SMBALRT	P/U 8.2K 3VDUAL
GP12	STBY	IN	MB_ID3	P/U 8.2K 3VDUAL
GP13	STBY	IN	-LPCPME	P/U 8.2K 3VDUAL
GP14	STBY	IN	GPIO14	P/U 8.2K 3VDUAL
GP15	STBY	OUT	GPIO15 (TP)	N/A
GP16	MAIN	IN	MB_ID1	P/U 8.2K VCC3
GP17/TACH0	MAIN	IN	N/A (OPT-ITE)	P/U 8.2K VCC3
GP18	MAIN	IN	MB_ID2	P/U 8.2K VCC3
GP19	MAIN	IN	GPIO19	P/U 8.2K VCC3
GP20	MAIN	OUT	GPIO20	N/A
GP21	MAIN	IN	GPIO21	P/U 8.2K VCC3
GP22	MAIN	IN	GPIO22	P/U 8.2K VCC3
GP23	MAIN	OUT	-LDRQ1	P/U 8.2K VCC3
GP24	STBY	OUT	GPIO24 (TP)	N/A
GP25	STBY	IN	MB_ID4	P/U 8.2K 3VDUAL
GP26/S4_STATE#	STBY	OUT	GPIO26	P/U 8.2K 3VDUAL
GP27	STBY	LOW	GPIO27	ENERGY-LAKE LED: GREEN
GP28	STBY	LOW	GPIO28	ENERGY-LAKE LED: YEL
GP29/OC5#	STBY	IN	-USBOC_F	P/U FUSEVCC1
GP30/OC6#	STBY	IN	-USBOC_F	P/U FUSEVCC1
GP31/OC7#	STBY	IN	-USBOC_F	P/U FUSEVCC1
GP32	MAIN	IN	MB_ID0	P/U 8.2K VCC3
GP33	MAIN	IN	GPIO33	P/U 8.2K VCC3
GP34	MAIN	IN	GPIO34	P/U 8.2K VCC3
GP35	MAIN	IN	N/A (TP)	N/A
GP36	MAIN	IN	GPIO36	P/U 8.2K VCC3
GP37	MAIN	IN	GPIO37	P/U 8.2K VCC3
GP38	MAIN	IN	GPIO38	P/U 8.2K VCC3
GP39	MAIN	IN	GPIO39	P/D 8.2K GND
GP48	MAIN	IN	GPIO48	P/U 8.2K VCC3
GP49	MAIN	IN	CPUPWROK	P/U 100 VTT_OL

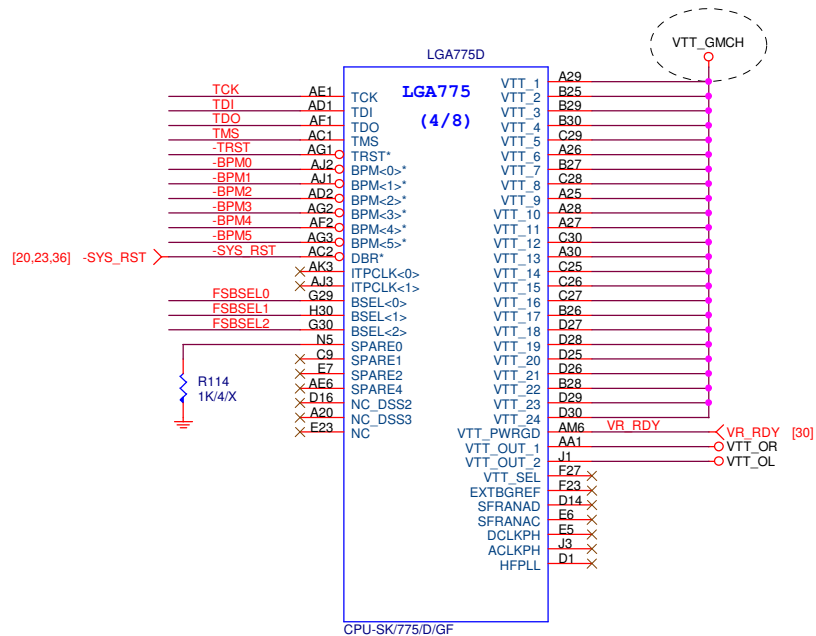
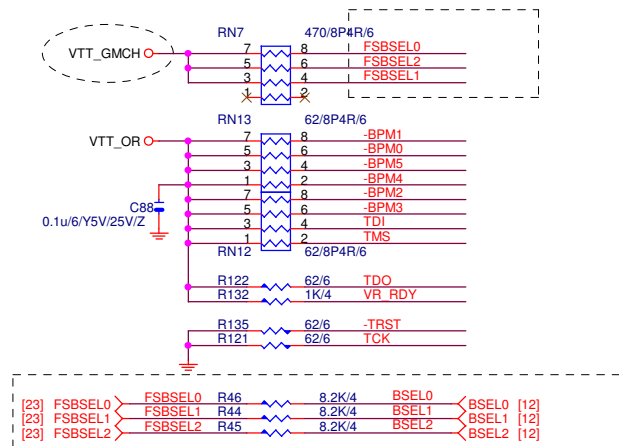
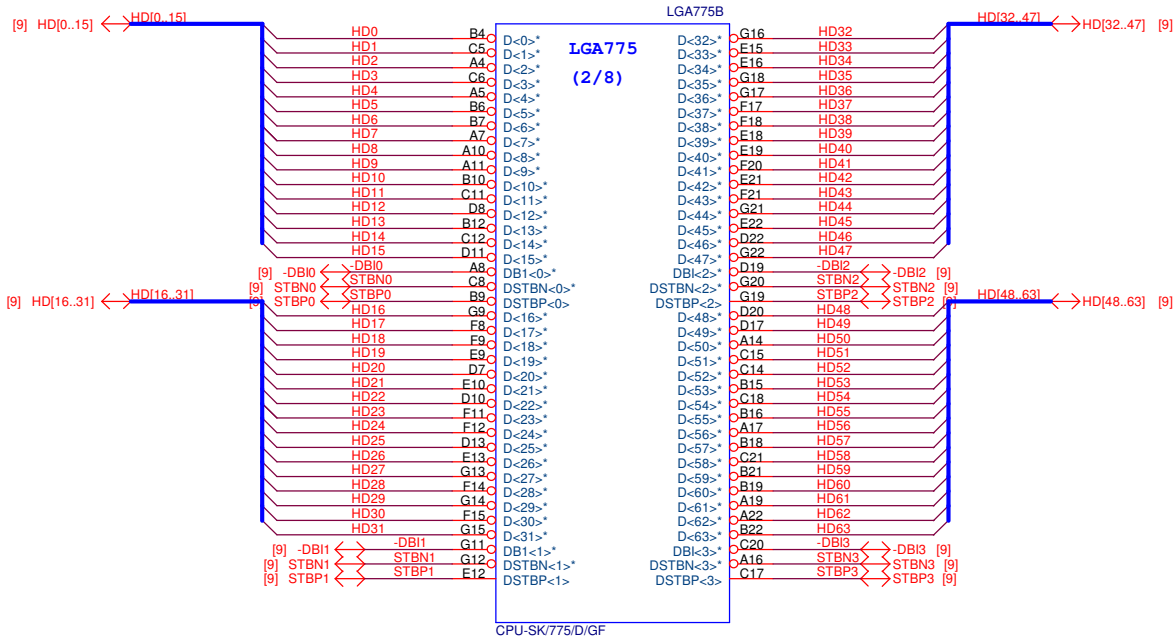




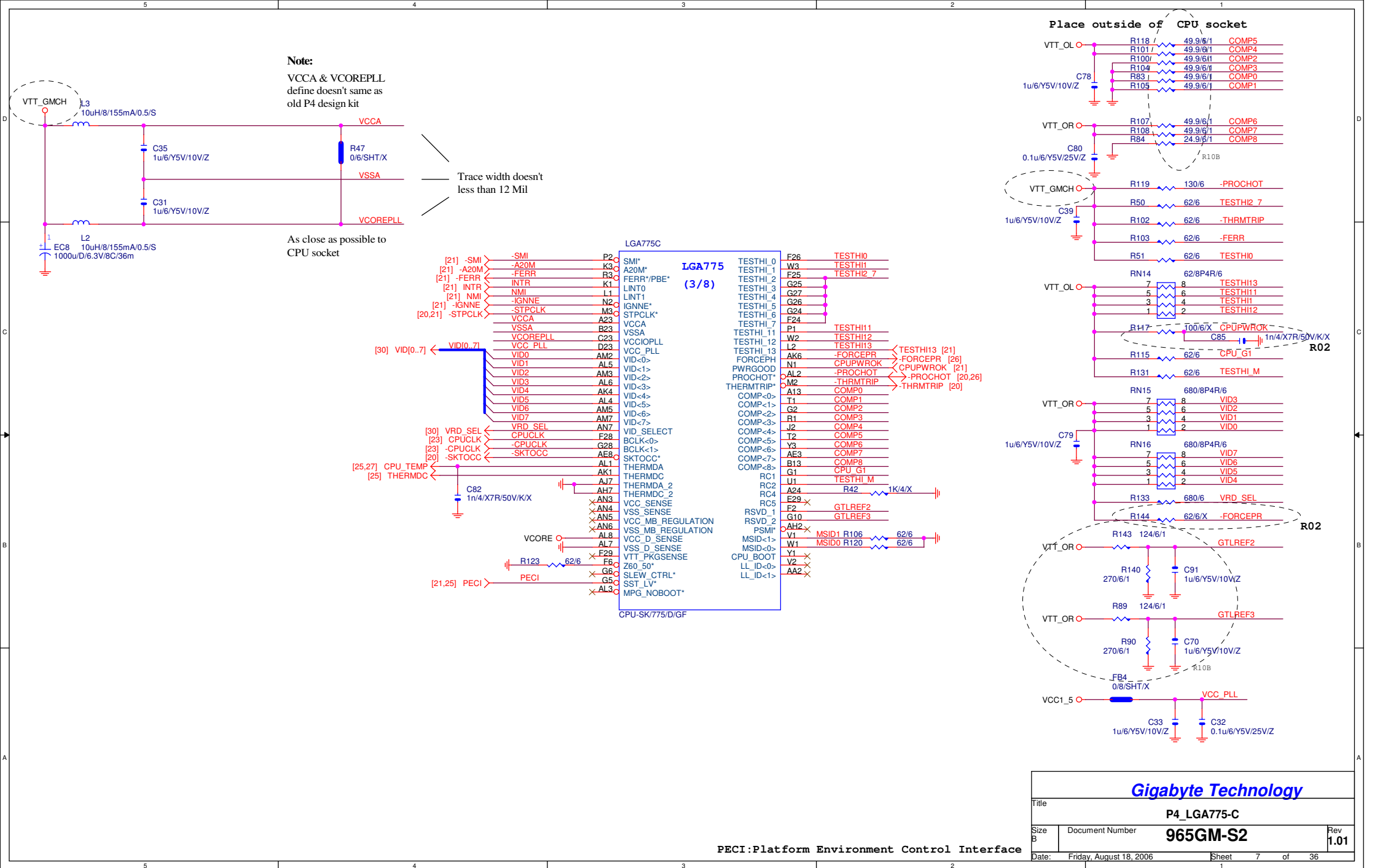
LGA775-D: FOOTPRINT

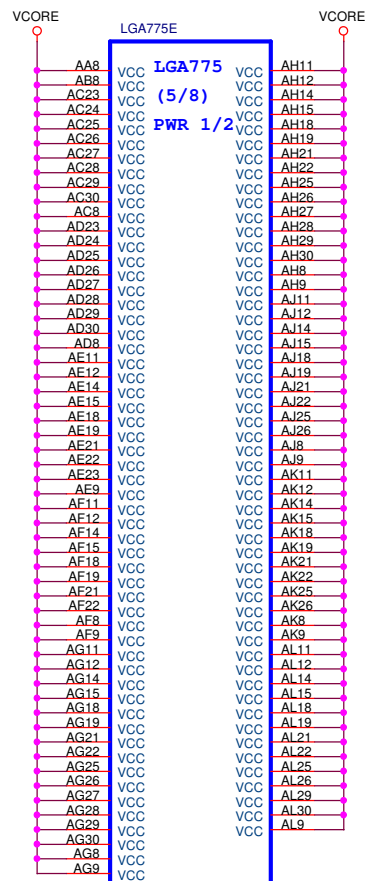


Gigabyte Technology			
Title			
P4_LGA775-A			
Size	Document Number	965GM-S2	
B		Rev	
		1.01	
Date:	Friday, August 18, 2006	Sheet	5 of 36

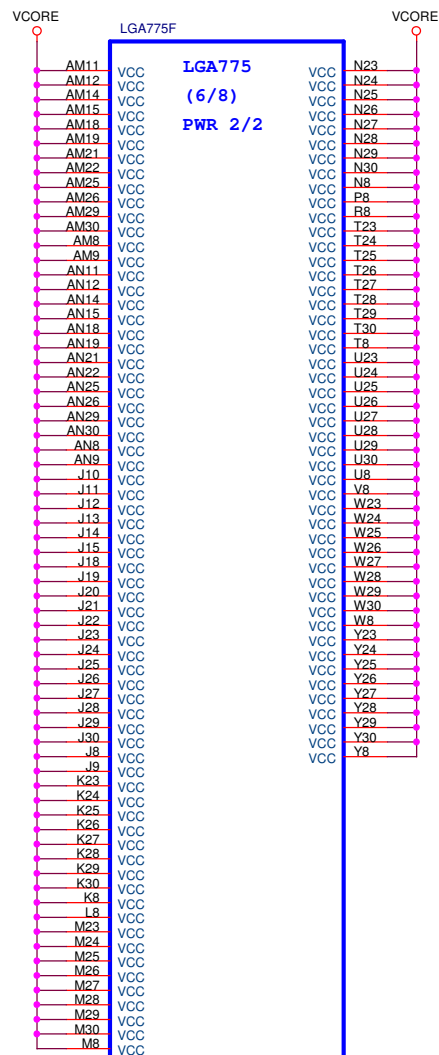


Gigabyte Technology			
Title			
P4_LGA775-B,D			
Size	Document Number	965GM-S2	
B		Rev	
		1.01	
Date:	Friday, August 18, 2006	Sheet	6 of 36

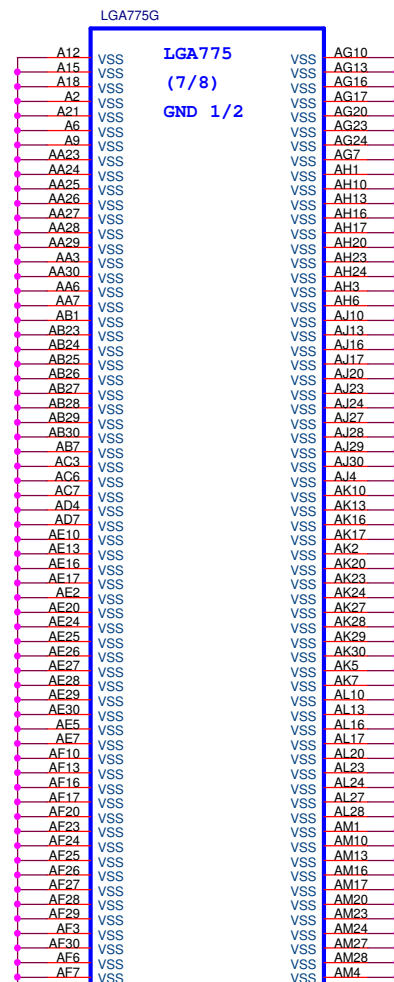




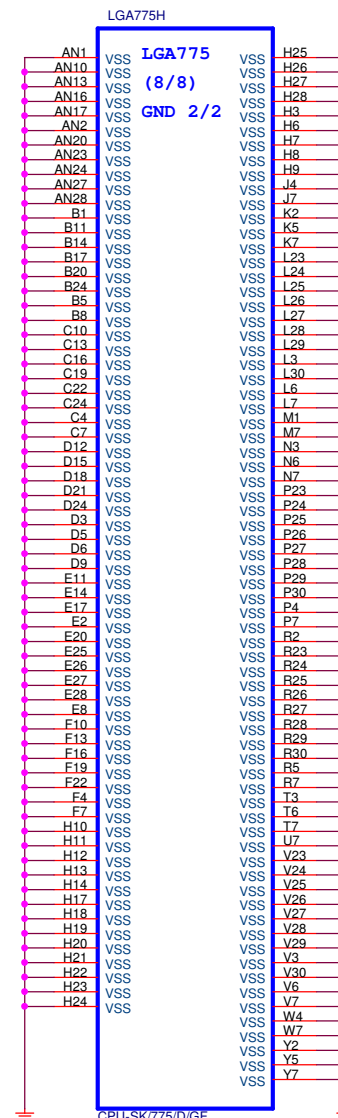
CPU-SK/775/D/GF



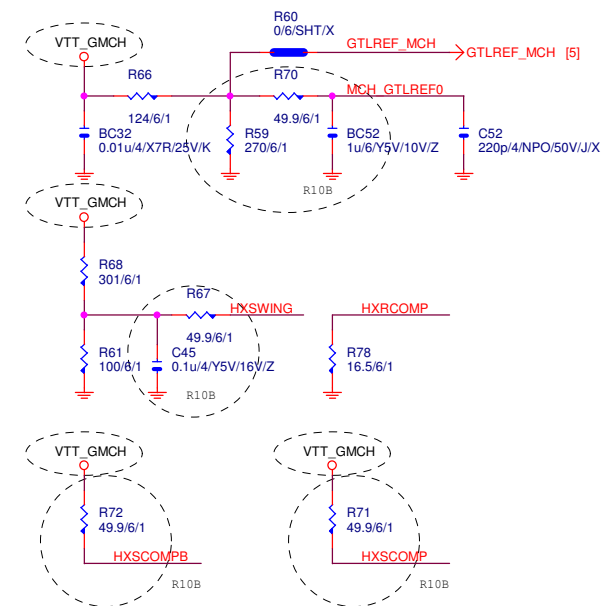
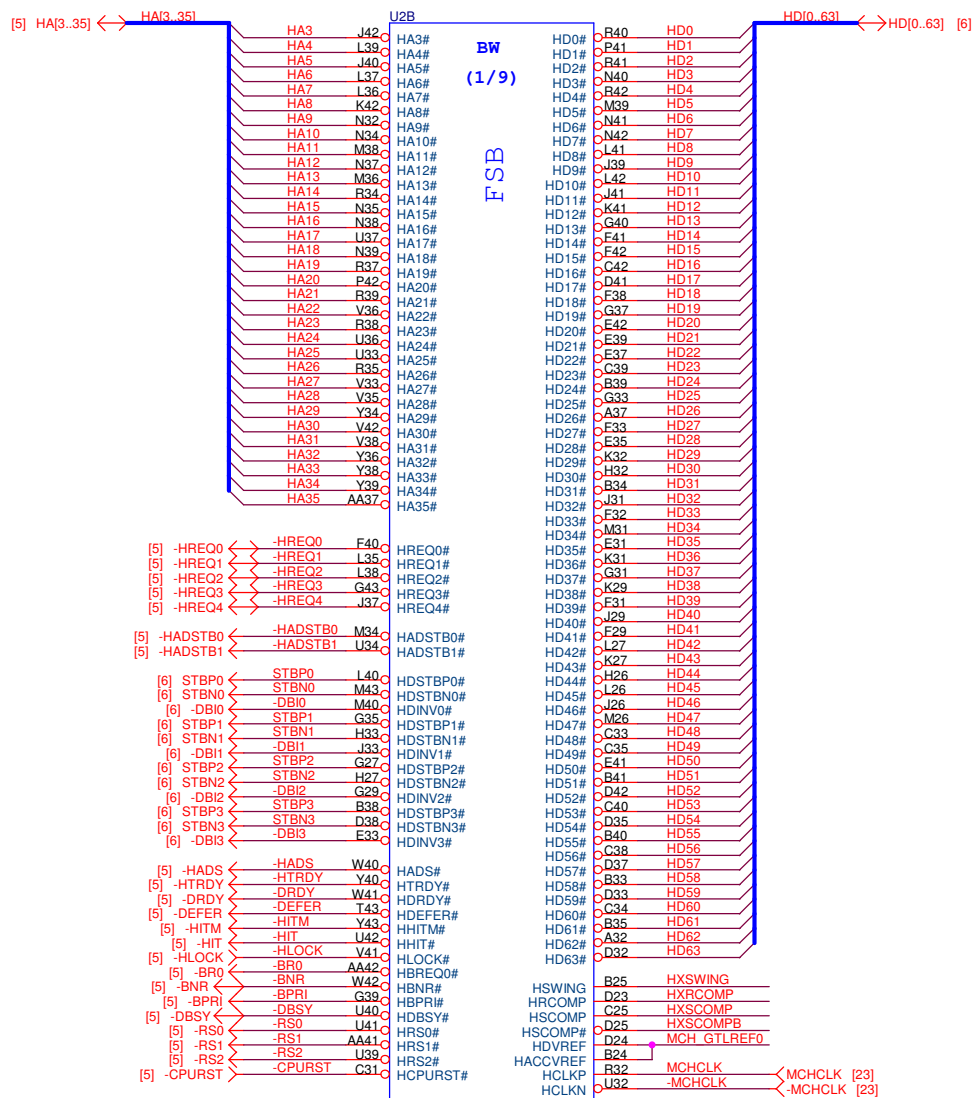
CPU-SK/775/D/GF



CPU-SK/775/D/GF



CPU-SK/775/D/GF



COMP量測有CURRENT SENSE,不可上電容



Gigabyte Technology

Title		
GMCH-HOST		
Size	Document Number	Rev
B	965GM-S2	1.01
Date:	Friday, August 18, 2006	Sheet 9 of 36

U2C

MAAA0 BA31 SMA_A0
MAAA1 BB25 SMA_A1
MAAA2 BA26 SMA_A2
MAAA3 BA25 SMA_A3
MAAA4 AY25 SMA_A4
MAAA5 BA23 SMA_A5
MAAA6 AY24 SMA_A6
MAAA7 AY23 SMA_A7
MAAA8 BB23 SMA_A8
MAAA9 BA22 SMA_A9
MAAA10 AY33 SMA_A10
MAAA11 BB22 SMA_A11
MAAA12 AW21 SMA_A12
MAAA13 AY38 SMA_A13
MAAA14 BA21 SMA_A14

[15,17] -SWEA SWEA BB34
[15,17] -SCASA SCASA AB#
[15,17] -SRASA SRASA AB#

[15,17] SBA00 BA33 SBA00
[15,17] SBA01 AW32 SBA01
[15,17] SBA02 BB21 SBA02

[15,17] CSA0 CSA0 AW35
[15,17] CSA1 CSA1 BA32
[15,17] CSA2 CSA2 BA34
[15,17] CSA3 CSA3 BB38

[15,17] CKEA0 CKEA0 BC20
[15,17] CKEA1 CKEA1 AY20
[15,17] CKEA2 CKEA2 AY21
[15,17] CKEA3 CKEA3 BA19

MODT_A0 AY37
MODT_A1 BA38
MODT_A2 BB35
MODT_A3 BA39

[15] DCLKA0 DCLKA0 AU31
[15] DCLKA0 DCLKA0 AB31
[15] DCLKA1 DCLKA1 AF27
[15] DCLKA1 DCLKA1 AN27
[15] DCLKA2 DCLKA2 AV33
[15] DCLKA2 DCLKA2 AW33
[15] DCLKA3 DCLKA3 AF29
[15] DCLKA3 DCLKA3 AS33
[15] DCLKA4 DCLKA4 AT33
[15] DCLKA4 DCLKA4 AN27
[15] DCLKA5 DCLKA5 AT33
[15] DCLKA5 DCLKA5 AU33

SDQS_A0
SDQS_A1
SDQS_A2
SDQS_A3
SDQS_A4
SDQS_A5

SDQ_A0
SDQ_A1
SDQ_A2
SDQ_A3
SDQ_A4
SDQ_A5

SDQ_A6
SDQ_A7
SDQ_A8
SDQ_A9
SDQ_A10
SDQ_A11
SDQ_A12
SDQ_A13
SDQ_A14
SDQ_A15

SDQ_A16
SDQ_A17
SDQ_A18
SDQ_A19
SDQ_A20
SDQ_A21
SDQ_A22
SDQ_A23
SDQ_A24
SDQ_A25

SDQ_A26
SDQ_A27
SDQ_A28
SDQ_A29
SDQ_A30
SDQ_A31
SDQ_A32
SDQ_A33
SDQ_A34
SDQ_A35

SDQ_A36
SDQ_A37
SDQ_A38
SDQ_A39
SDQ_A40
SDQ_A41
SDQ_A42
SDQ_A43
SDQ_A44
SDQ_A45
SDQ_A46
SDQ_A47
SDQ_A48
SDQ_A49
SDQ_A50
SDQ_A51
SDQ_A52
SDQ_A53
SDQ_A54
SDQ_A55

SDQ_A56
SDQ_A57
SDQ_A58
SDQ_A59
SDQ_A60
SDQ_A61
SDQ_A62
SDQ_A63
SDQ_A64
SDQ_A65

SDQ_A66
SDQ_A67
SDQ_A68
SDQ_A69
SDQ_A70
SDQ_A71
SDQ_A72
SDQ_A73
SDQ_A74
SDQ_A75

SDQ_A76
SDQ_A77
SDQ_A78
SDQ_A79
SDQ_A80
SDQ_A81
SDQ_A82
SDQ_A83
SDQ_A84
SDQ_A85

SDQ_A86
SDQ_A87
SDQ_A88
SDQ_A89
SDQ_A90
SDQ_A91
SDQ_A92
SDQ_A93
SDQ_A94
SDQ_A95

SDQ_A96
SDQ_A97
SDQ_A98
SDQ_A99
SDQ_A100
SDQ_A101
SDQ_A102
SDQ_A103
SDQ_A104
SDQ_A105

SDQ_A106
SDQ_A107
SDQ_A108
SDQ_A109
SDQ_A110
SDQ_A111
SDQ_A112
SDQ_A113
SDQ_A114
SDQ_A115

SDQ_A116
SDQ_A117
SDQ_A118
SDQ_A119
SDQ_A120
SDQ_A121
SDQ_A122
SDQ_A123
SDQ_A124
SDQ_A125

SDQ_A126
SDQ_A127
SDQ_A128
SDQ_A129
SDQ_A130
SDQ_A131
SDQ_A132
SDQ_A133
SDQ_A134
SDQ_A135

SDQ_A136
SDQ_A137
SDQ_A138
SDQ_A139
SDQ_A140
SDQ_A141
SDQ_A142
SDQ_A143
SDQ_A144
SDQ_A145

SDQ_A146
SDQ_A147
SDQ_A148
SDQ_A149
SDQ_A150
SDQ_A151
SDQ_A152
SDQ_A153
SDQ_A154
SDQ_A155

SDQ_A156
SDQ_A157
SDQ_A158
SDQ_A159
SDQ_A160
SDQ_A161
SDQ_A162
SDQ_A163
SDQ_A164
SDQ_A165

SDQ_A166
SDQ_A167
SDQ_A168
SDQ_A169
SDQ_A170
SDQ_A171
SDQ_A172
SDQ_A173
SDQ_A174
SDQ_A175

SDQ_A176
SDQ_A177
SDQ_A178
SDQ_A179
SDQ_A180
SDQ_A181
SDQ_A182
SDQ_A183
SDQ_A184
SDQ_A185

SDQ_A186
SDQ_A187
SDQ_A188
SDQ_A189
SDQ_A190
SDQ_A191
SDQ_A192
SDQ_A193
SDQ_A194
SDQ_A195

DDR_0

LE82G965-C2/BGA1226[10H81-030082-40R]

CHANNEL A

CHANNEL B

U2D

MAAB0 BB17 SMA_B0
MAAB1 AY17 SMA_B1
MAAB2 BA17 SMA_B2
MAAB3 BB18 SMA_B3
MAAB4 AW15 SMA_B4
MAAB5 BA15 SMA_B5
MAAB6 BB15 SMA_B6
MAAB7 BA14 SMA_B7
MAAB8 BB14 SMA_B8
MAAB9 BA13 SMA_B9
MAAB10 AW18 SMA_B10
MAAB11 BB13 SMA_B11
MAAB12 BB13 SMA_B12
MAAB13 AY20 SMA_B13
MAAB14 BA13 SMA_B14

[16,17] -SWEB SWEB BA27
[16,17] -SCASB SCASB AB#
[16,17] -SRASB SRASB AB#

[16,17] SBA00 BA33 SBA00
[16,17] SBA01 AW32 SBA01
[16,17] SBA02 BB21 SBA02

[16,17] CSA0 CSA0 AW35
[16,17] CSA1 CSA1 BA32
[16,17] CSA2 CSA2 BA34
[16,17] CSA3 CSA3 BB38

[16,17] CKEB0 CKEB0 BC20
[16,17] CKEB1 CKEB1 AY20
[16,17] CKEB2 CKEB2 AY21
[16,17] CKEB3 CKEB3 BA19

MODT_B0 AY37
MODT_B1 BA38
MODT_B2 BB35
MODT_B3 BA39

[16] DCLKB0 DCLKB0 AU31
[16] DCLKB0 DCLKB0 AB31
[16] DCLKB1 DCLKB1 AF27
[16] DCLKB1 DCLKB1 AN27
[16] DCLKB2 DCLKB2 AV33
[16] DCLKB2 DCLKB2 AW33
[16] DCLKB3 DCLKB3 AF29
[16] DCLKB3 DCLKB3 AS33
[16] DCLKB4 DCLKB4 AT33
[16] DCLKB4 DCLKB4 AN27
[16] DCLKB5 DCLKB5 AT33
[16] DCLKB5 DCLKB5 AU33

SDQS_B0
SDQS_B1
SDQS_B2
SDQS_B3
SDQS_B4
SDQS_B5

SDQ_B0
SDQ_B1
SDQ_B2
SDQ_B3
SDQ_B4
SDQ_B5

SDQ_B6
SDQ_B7
SDQ_B8
SDQ_B9
SDQ_B10
SDQ_B11
SDQ_B12
SDQ_B13
SDQ_B14
SDQ_B15

SDQ_B16
SDQ_B17
SDQ_B18
SDQ_B19
SDQ_B20
SDQ_B21
SDQ_B22
SDQ_B23
SDQ_B24
SDQ_B25

SDQ_B26
SDQ_B27
SDQ_B28
SDQ_B29
SDQ_B30
SDQ_B31
SDQ_B32
SDQ_B33
SDQ_B34
SDQ_B35

SDQ_B36
SDQ_B37
SDQ_B38
SDQ_B39
SDQ_B40
SDQ_B41
SDQ_B42
SDQ_B43
SDQ_B44
SDQ_B45
SDQ_B46
SDQ_B47
SDQ_B48
SDQ_B49
SDQ_B50
SDQ_B51
SDQ_B52
SDQ_B53
SDQ_B54
SDQ_B55

SDQ_B56
SDQ_B57
SDQ_B58
SDQ_B59
SDQ_B60
SDQ_B61
SDQ_B62
SDQ_B63
SDQ_B64
SDQ_B65

SDQ_B66
SDQ_B67
SDQ_B68
SDQ_B69
SDQ_B70
SDQ_B71
SDQ_B72
SDQ_B73
SDQ_B74
SDQ_B75

SDQ_B76
SDQ_B77
SDQ_B78
SDQ_B79
SDQ_B80
SDQ_B81
SDQ_B82
SDQ_B83
SDQ_B84
SDQ_B85

SDQ_B86
SDQ_B87
SDQ_B88
SDQ_B89
SDQ_B90
SDQ_B91
SDQ_B92
SDQ_B93
SDQ_B94
SDQ_B95

SDQ_B96
SDQ_B97
SDQ_B98
SDQ_B99
SDQ_B100
SDQ_B101
SDQ_B102
SDQ_B103
SDQ_B104
SDQ_B105

SDQ_B106
SDQ_B107
SDQ_B108
SDQ_B109
SDQ_B110
SDQ_B111
SDQ_B112
SDQ_B113
SDQ_B114
SDQ_B115

SDQ_B116
SDQ_B117
SDQ_B118
SDQ_B119
SDQ_B120
SDQ_B121
SDQ_B122
SDQ_B123
SDQ_B124
SDQ_B125

SDQ_B126
SDQ_B127
SDQ_B128
SDQ_B129
SDQ_B130
SDQ_B131
SDQ_B132
SDQ_B133
SDQ_B134
SDQ_B135

SDQ_B136
SDQ_B137
SDQ_B138
SDQ_B139
SDQ_B140
SDQ_B141
SDQ_B142
SDQ_B143
SDQ_B144
SDQ_B145

SDQ_B146
SDQ_B147
SDQ_B148
SDQ_B149
SDQ_B150
SDQ_B151
SDQ_B152
SDQ_B153
SDQ_B154
SDQ_B155

SDQ_B156
SDQ_B157
SDQ_B158
SDQ_B159
SDQ_B160
SDQ_B161
SDQ_B162
SDQ_B163
SDQ_B164
SDQ_B165

SDQ_B166
SDQ_B167
SDQ_B168
SDQ_B169
SDQ_B170
SDQ_B171
SDQ_B172
SDQ_B173
SDQ_B174
SDQ_B175

SDQ_B176
SDQ_B177
SDQ_B178
SDQ_B179
SDQ_B180
SDQ_B181
SDQ_B182
SDQ_B183
SDQ_B184
SDQ_B185

SDQ_B186
SDQ_B187
SDQ_B188
SDQ_B189
SDQ_B190
SDQ_B191
SDQ_B192
SDQ_B193
SDQ_B194
SDQ_B195

DDR_1

LE82G965-C2/BGA1226[10H81-030082-40R]

[15,17] MODT_A[0..3] MODT_A0..3

[16,17] MODT_B[0..3] MODT_B0..3

[16] -DQSB[0..7] DQSB0..7

[16,17] MAAB[0..14] MAAB0..14

[16] DMB[0..7] DMB0..7

[16] MDB[0..63] MDB0..63

[16] DQSB[0..7] DQSB0..7

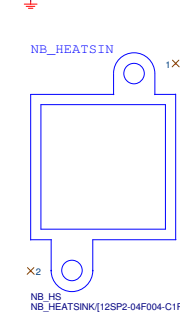
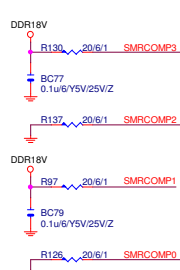
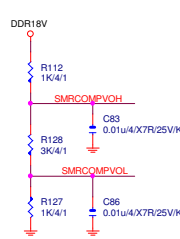
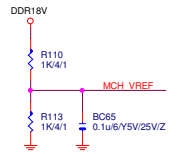
[15,17] MAAB[0..14] MAAB0..14

[15] DMA[0..7] DMA0..7

[15] MDAB[0..63] MDAB0..63

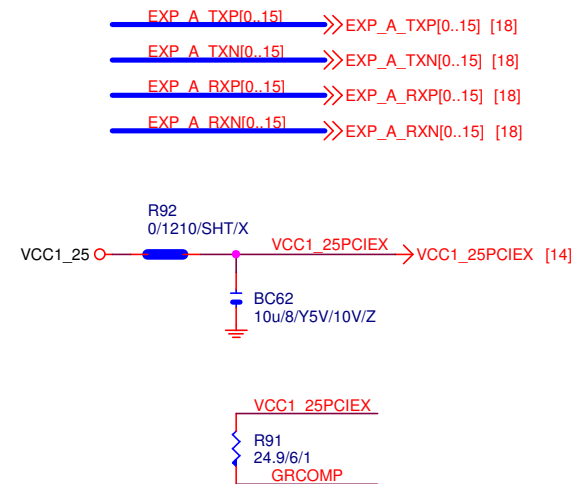
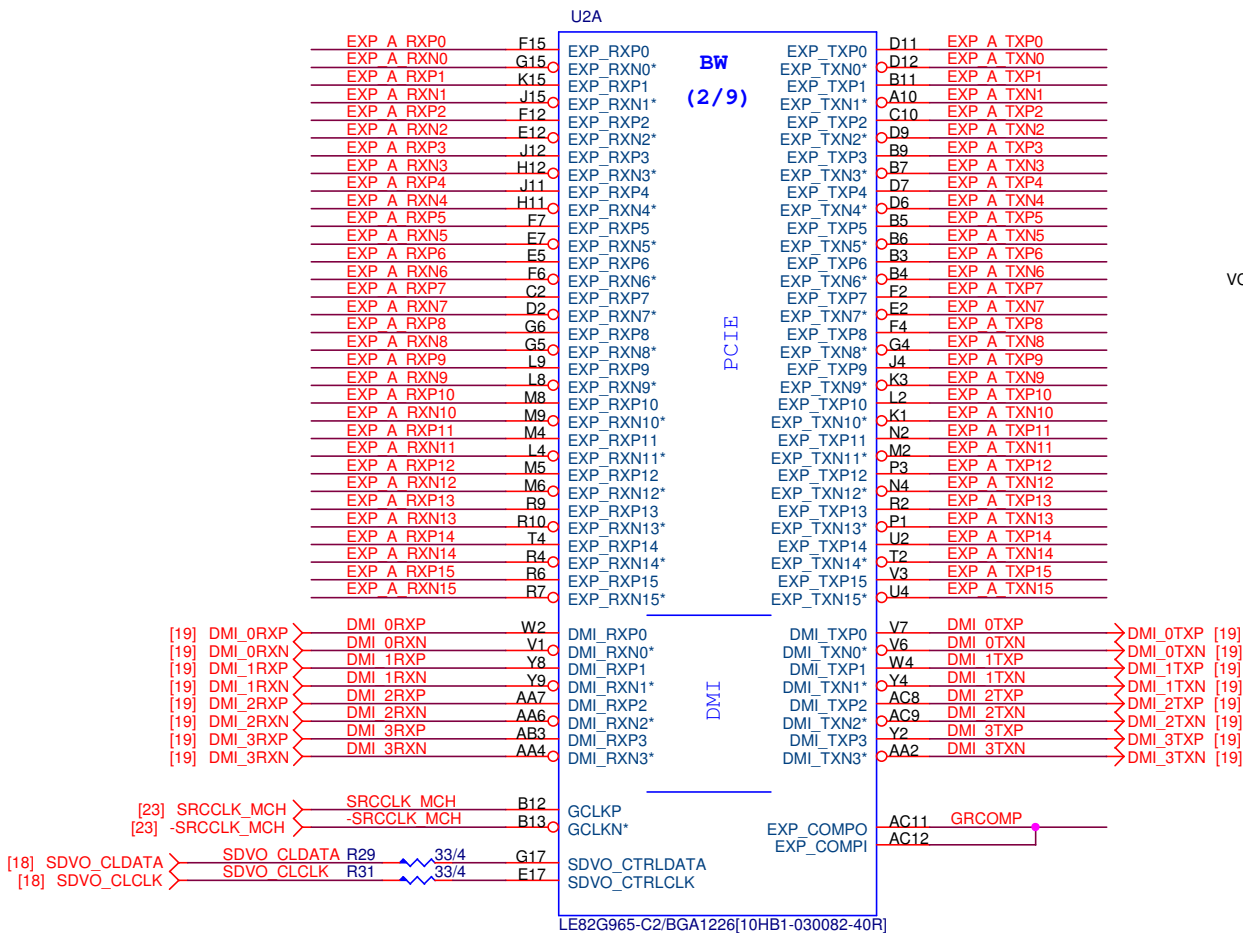
[15] DQSA[0..7] DQSA0..7

[15] -DQSA[0..7] DQSA0..7

NB_HS
NB_HEATSINK[12SP2-04F004-C1R_12SP2-04F004-C3R]

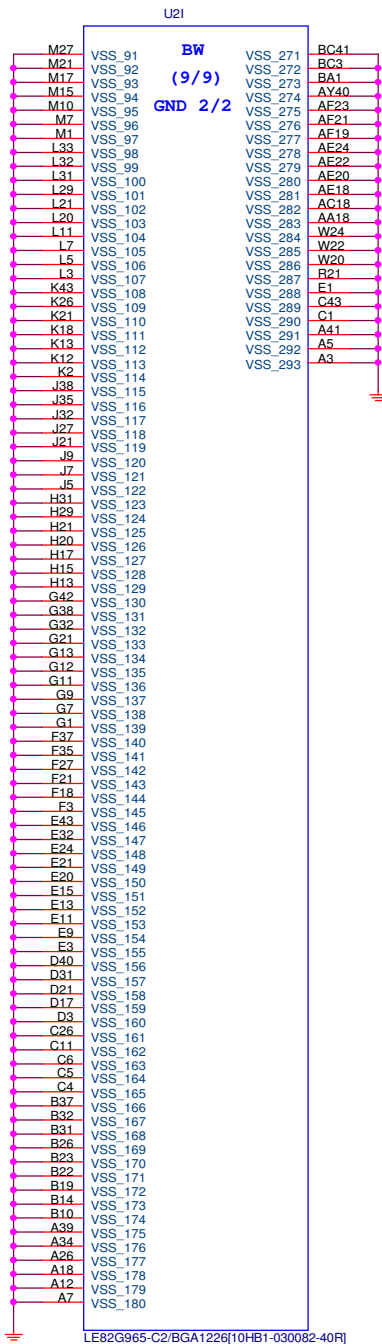
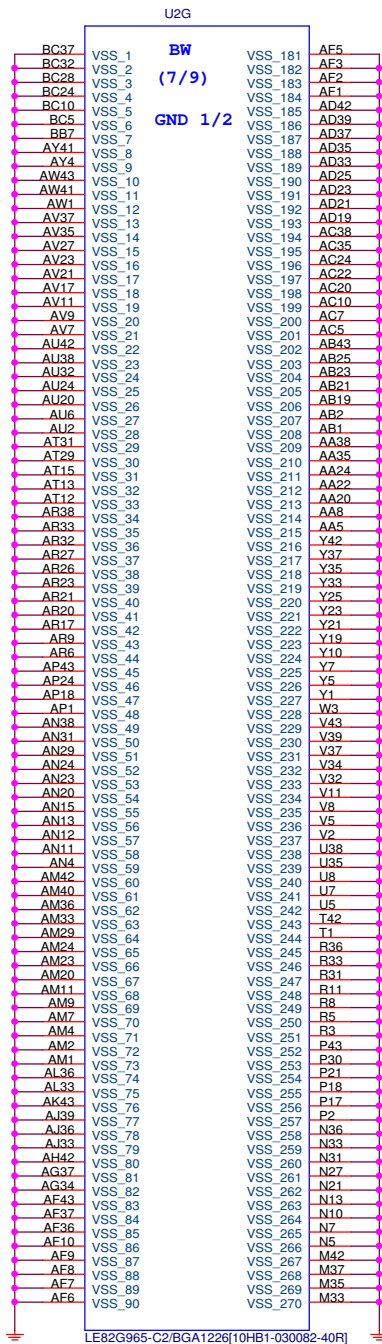
Gigabyte Technology

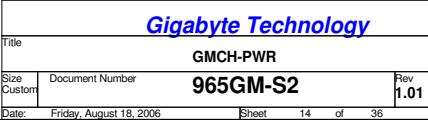
Title			GMCH-DDR11
Size	Document Number	965GM-S2	Rev
Custom			1.01
Date	Friday, August 18, 2006	Sheet	10 of 36

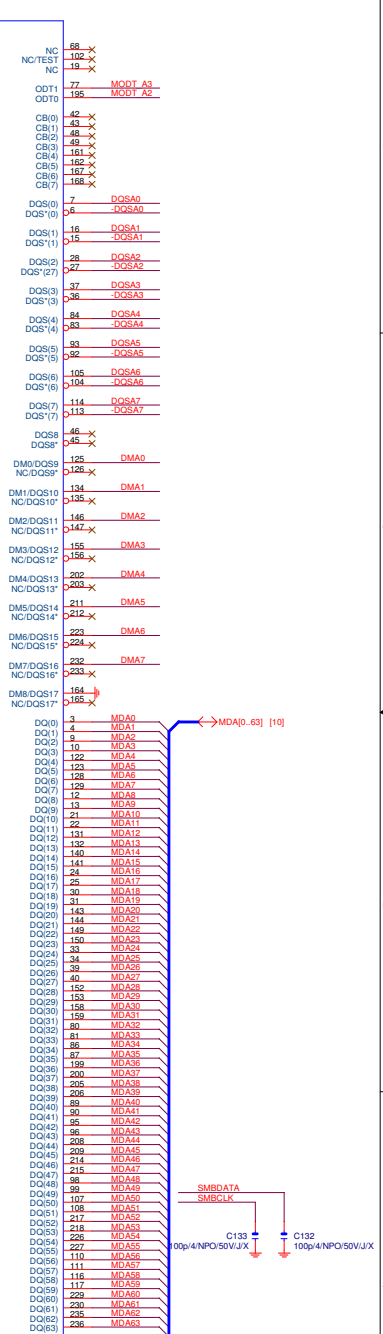
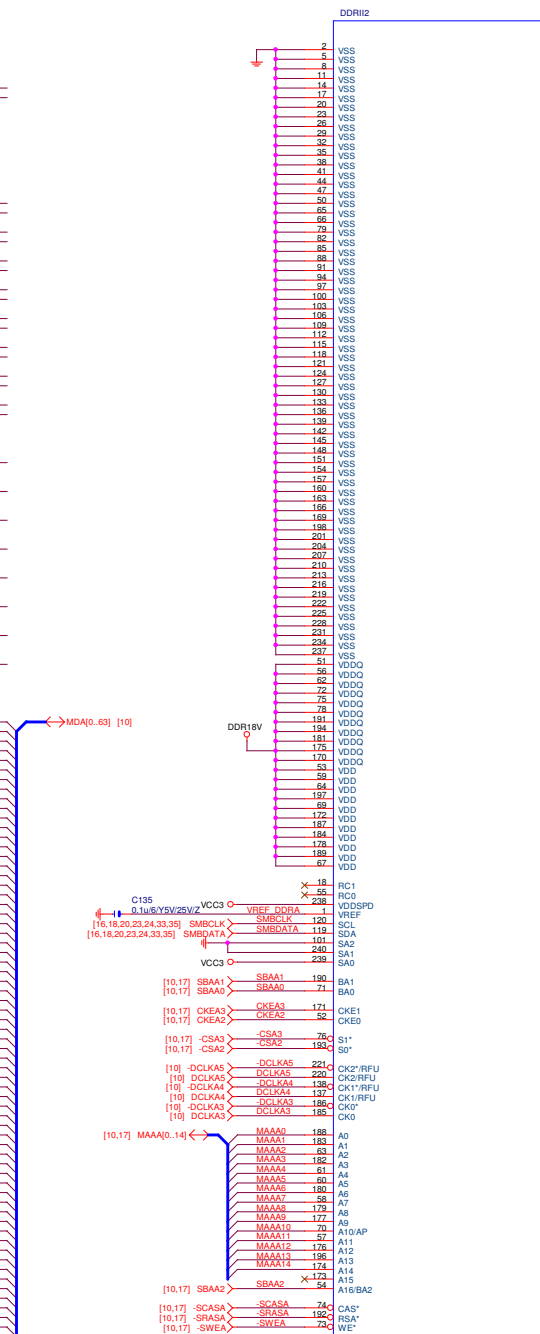
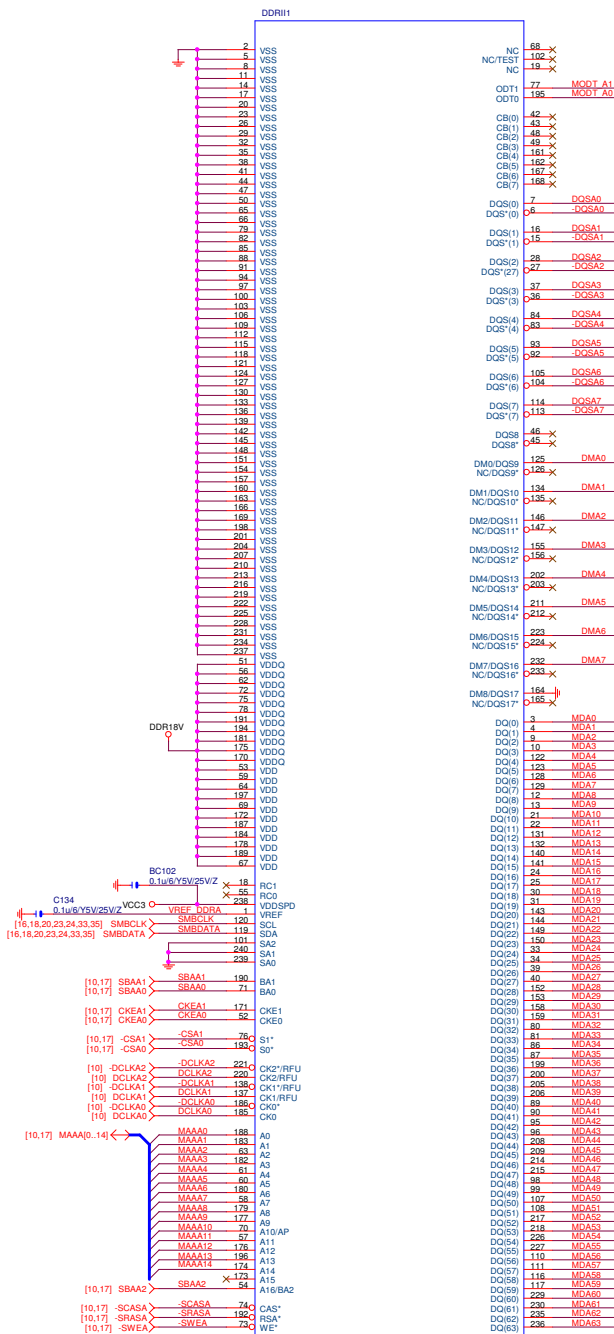


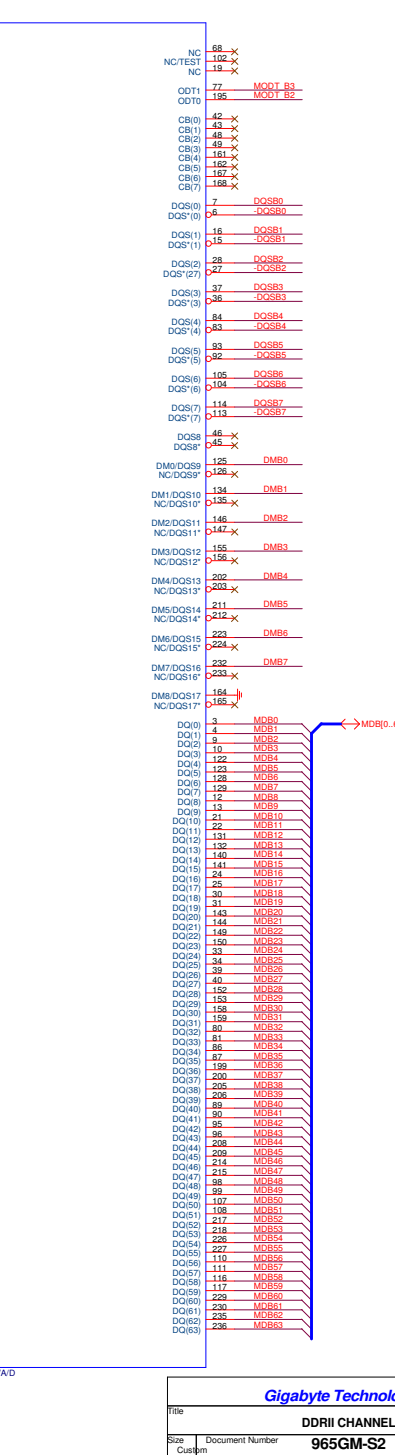
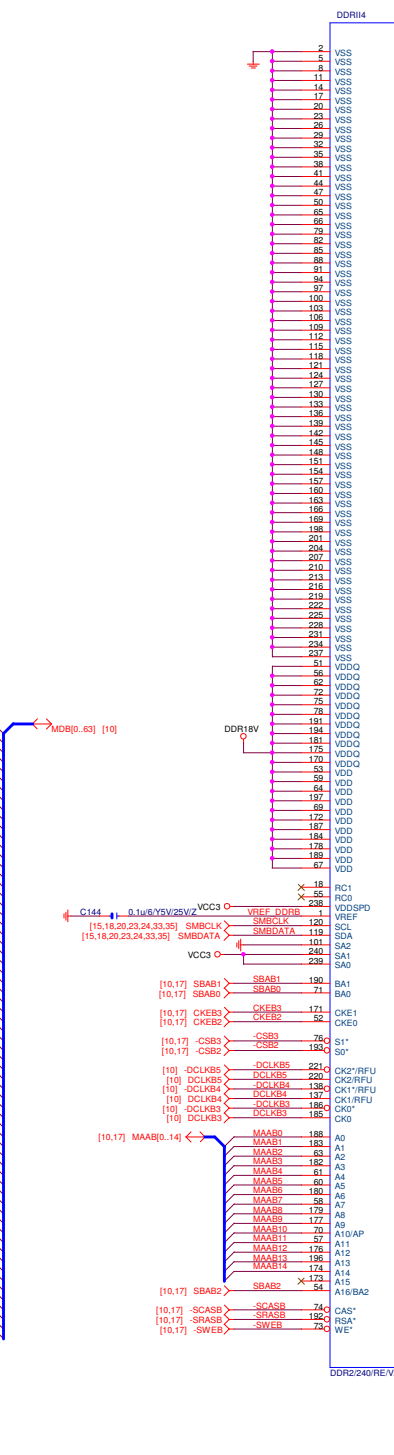
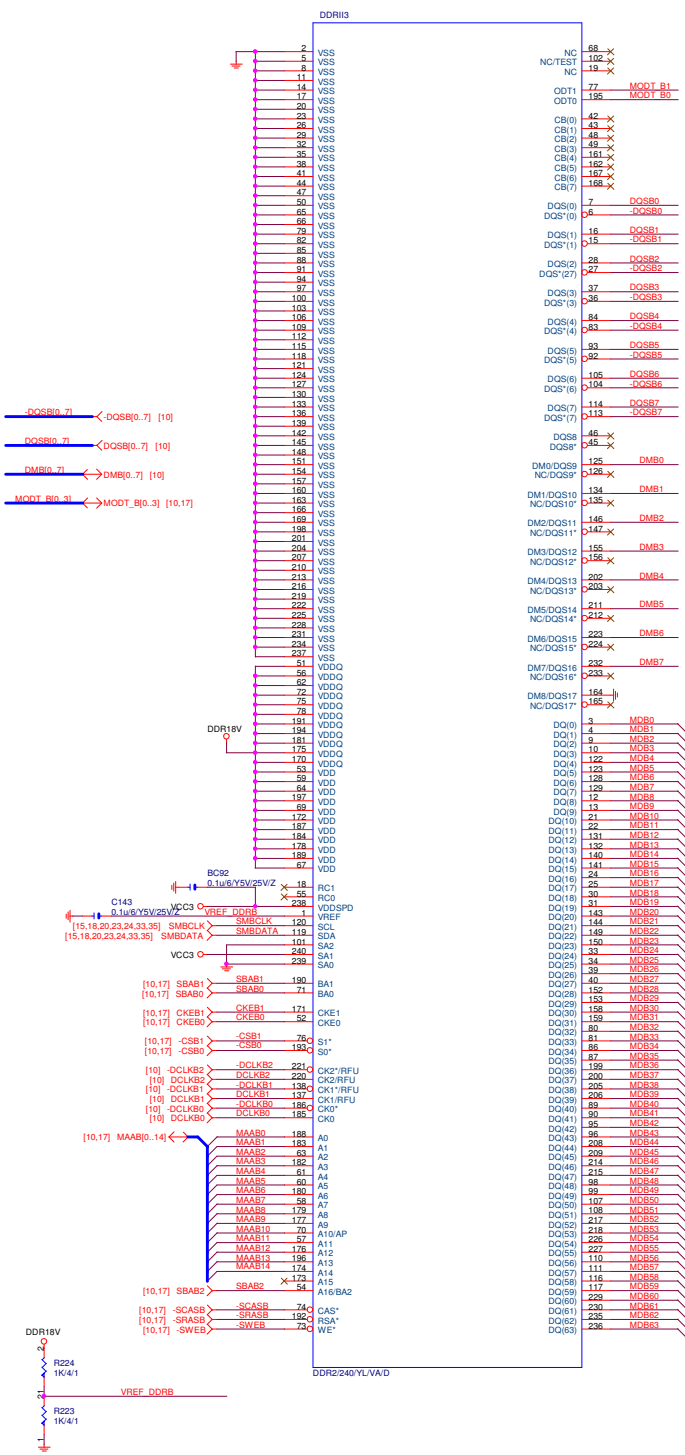
Gigabyte Technology

Title			GMCH-PCI E & DMI	
Size	Document Number	965GM-S2		Rev
Custom				1.01
Date:	Friday, August 18, 2006	Sheet	11	of 36

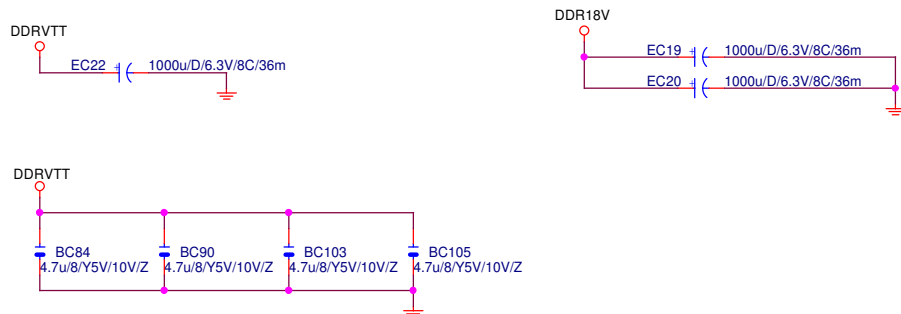




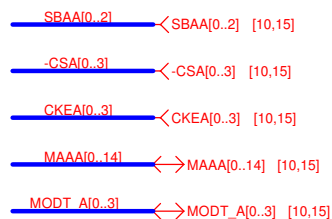
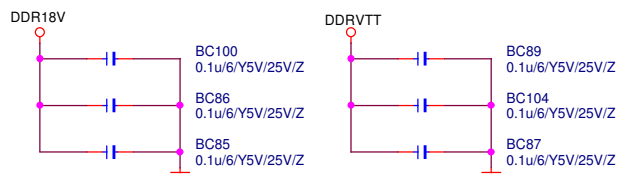




DDRVTT Decouple



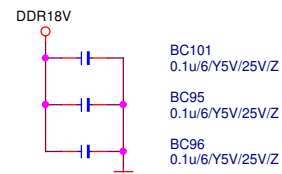
DDRVTT Decouple



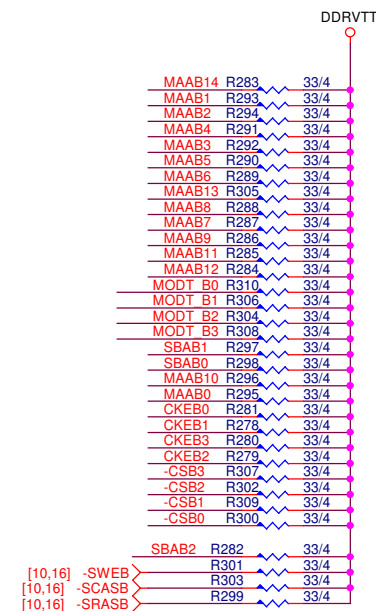
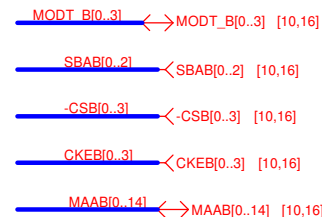
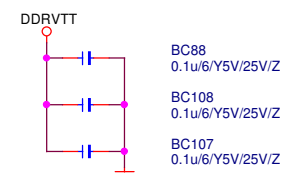
Timing diagram for DDRVT1. The diagram shows the relationship between various signals and the DDRVT1 clock signal. The signals are listed on the left, and their corresponding values are shown on the right. The clock signal is represented by a red line with a red circle at the top right.

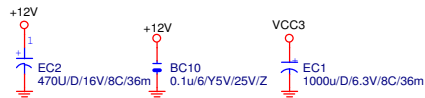
Signal	Value	Value
MODT_A0	R200	33/4
MODT_A1	R211	33/4
MODT_A2	R207	33/4
MODT_A3	R212	33/4
MAAA8	R216	33/4
MAAA7	R215	33/4
MAAA4	R193	33/4
MAAA1	R195	33/4
MAAA13	R209	33/4
MAA2	R196	33/4
MAA3	R194	33/4
SBA2	R189	33/4
SBA1	R198	33/4
MAAA10	R201	33/4
MAAA0	R197	33/4
CKEA0	R186	33/4
CKEA3	R184	33/4
CKEA2	R187	33/4
CKEA1	R185	33/4
CSA3	R210	33/4
CSA1	R208	33/4
CSA2	R204	33/4
CSA0	R199	33/4
MAA5	R191	33/4
MAA6	R192	33/4
MAA9	R214	33/4
MAA11	R213	33/4
MAA12	R190	33/4
SBA0	R202	33/4
MAA14	R188	33/4
CASKA	R206	33/4
SWEA	R205	33/4
RASA	R203	33/4

DDR18V Decouple

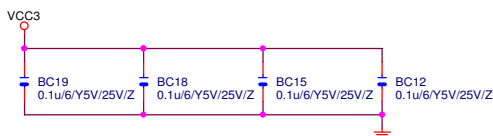


DDRVTT Decouple





PCIESLOT-164DN-2



[15,16,20,23,24,33,35] SMBCLK
[15,16,20,23,24,33,35] SMBDATA

[20,24,35] -PCIE_WAKE

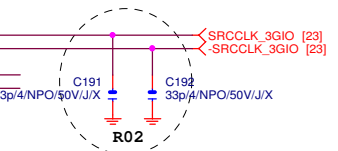
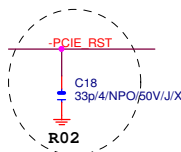
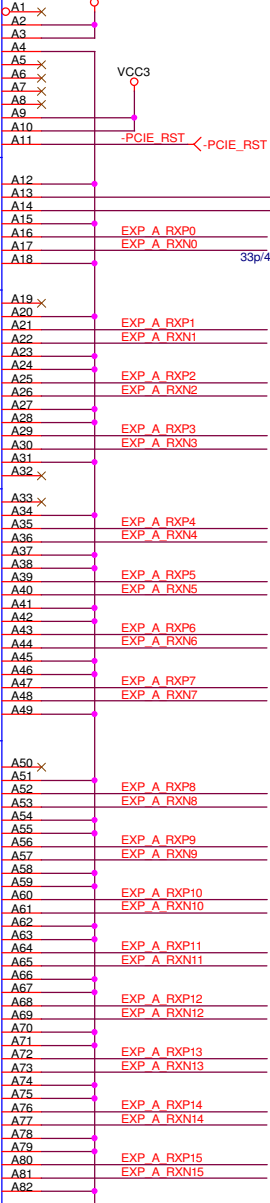
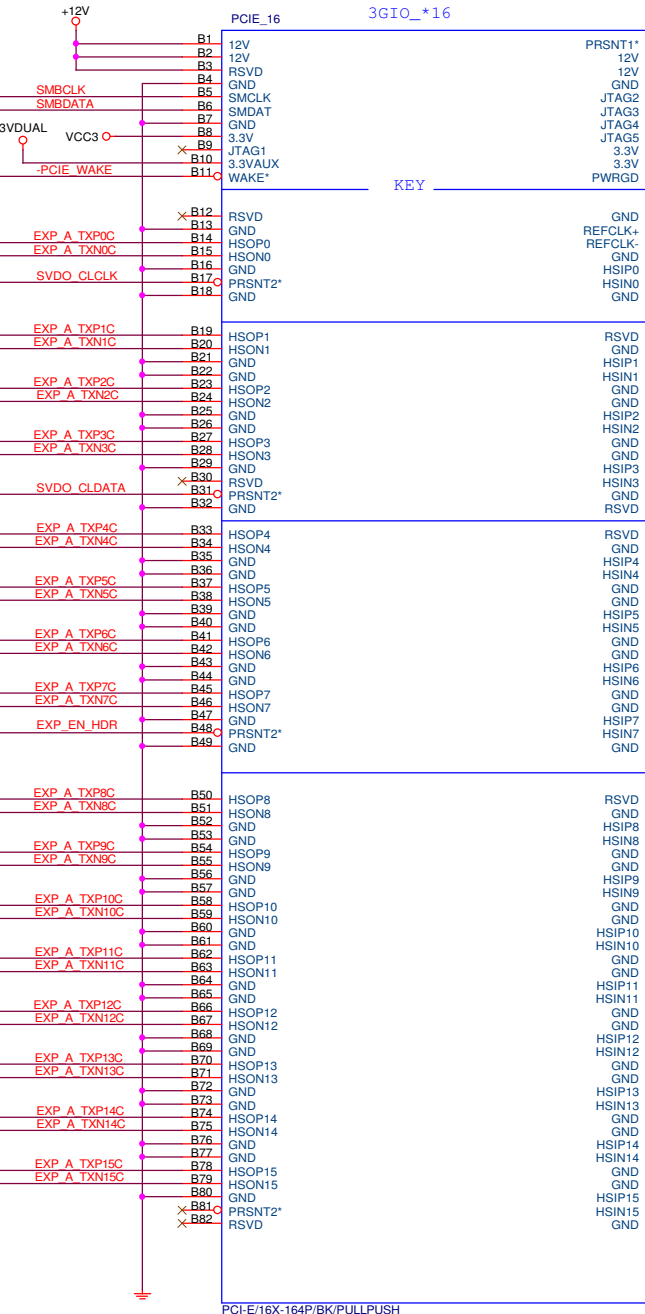
EXP_A_TXP0[0..15] >> EXP_A_TXP[0..15] [11]
EXP_A_TXN0[0..15] >> EXP_A_TXN[0..15] [11]

EXP_A_TXP0	C28	0.1u4/Y5V/16V/Z	EXP_A_TXP0C
EXP_A_TXN0	C27	0.1u4/Y5V/16V/Z	EXP_A_TXN0C
EXP_A_TXP1	C29	0.1u4/Y5V/16V/Z	EXP_A_TXP1C
EXP_A_TXN1	C34	0.1u4/Y5V/16V/Z	EXP_A_TXN1C
EXP_A_TXP2	C37	0.1u4/Y5V/16V/Z	EXP_A_TXP2C
EXP_A_TXN2	C38	0.1u4/Y5V/16V/Z	EXP_A_TXN2C
EXP_A_TXP3	C40	0.1u4/Y5V/16V/Z	EXP_A_TXP3C
EXP_A_TXN3	C41	0.1u4/Y5V/16V/Z	EXP_A_TXN3C
EXP_A_TXP4	C43	0.1u4/Y5V/16V/Z	EXP_A_TXP4C
EXP_A_TXN4	C44	0.1u4/Y5V/16V/Z	EXP_A_TXN4C
EXP_A_TXP5	C47	0.1u4/Y5V/16V/Z	EXP_A_TXP5C
EXP_A_TXN5	C46	0.1u4/Y5V/16V/Z	EXP_A_TXN5C
EXP_A_TXP6	C49	0.1u4/Y5V/16V/Z	EXP_A_TXP6C
EXP_A_TXN6	C48	0.1u4/Y5V/16V/Z	EXP_A_TXN6C
EXP_A_TXP7	C51	0.1u4/Y5V/16V/Z	EXP_A_TXP7C
EXP_A_TXN7	C50	0.1u4/Y5V/16V/Z	EXP_A_TXN7C
EXP_A_TXP8	C55	0.1u4/Y5V/16V/Z	EXP_A_TXP8C
EXP_A_TXN8	C56	0.1u4/Y5V/16V/Z	EXP_A_TXN8C
EXP_A_TXP9	C59	0.1u4/Y5V/16V/Z	EXP_A_TXP9C
EXP_A_TXN9	C60	0.1u4/Y5V/16V/Z	EXP_A_TXN9C
EXP_A_TXP10	C64	0.1u4/Y5V/16V/Z	EXP_A_TXP10C
EXP_A_TXN10	C61	0.1u4/Y5V/16V/Z	EXP_A_TXN10C
EXP_A_TXP11	C66	0.1u4/Y5V/16V/Z	EXP_A_TXP11C
EXP_A_TXN11	C65	0.1u4/Y5V/16V/Z	EXP_A_TXN11C
EXP_A_TXP12	C68	0.1u4/Y5V/16V/Z	EXP_A_TXP12C
EXP_A_TXN12	C67	0.1u4/Y5V/16V/Z	EXP_A_TXN12C
EXP_A_TXP13	C71	0.1u4/Y5V/16V/Z	EXP_A_TXP13C
EXP_A_TXN13	C69	0.1u4/Y5V/16V/Z	EXP_A_TXN13C
EXP_A_TXP14	C73	0.1u4/Y5V/16V/Z	EXP_A_TXP14C
EXP_A_TXN14	C72	0.1u4/Y5V/16V/Z	EXP_A_TXN14C
EXP_A_TXP15	C75	0.1u4/Y5V/16V/Z	EXP_A_TXP15C
EXP_A_TXN15	C74	0.1u4/Y5V/16V/Z	EXP_A_TXN15C

[11] SDVO_CLKCLK >> SVDO_CLKCLK

[11] SDVO_CLDATA >> SVDO_CLDATA

[12] EXP_EN_HDR >> EXP_EN_HDR



EXP_A_RXP[0..15] >> EXP_A_RXP[0..15] [11]
EXP_A_RXN[0..15] >> EXP_A_RXN[0..15] [11]

PCI-E/16X-164P/BK/PULLPUSH

Gigabyte Technology

Title

PCI EXPRESS * 16

Size

Custom

Document Number

965GM-S2

Date:

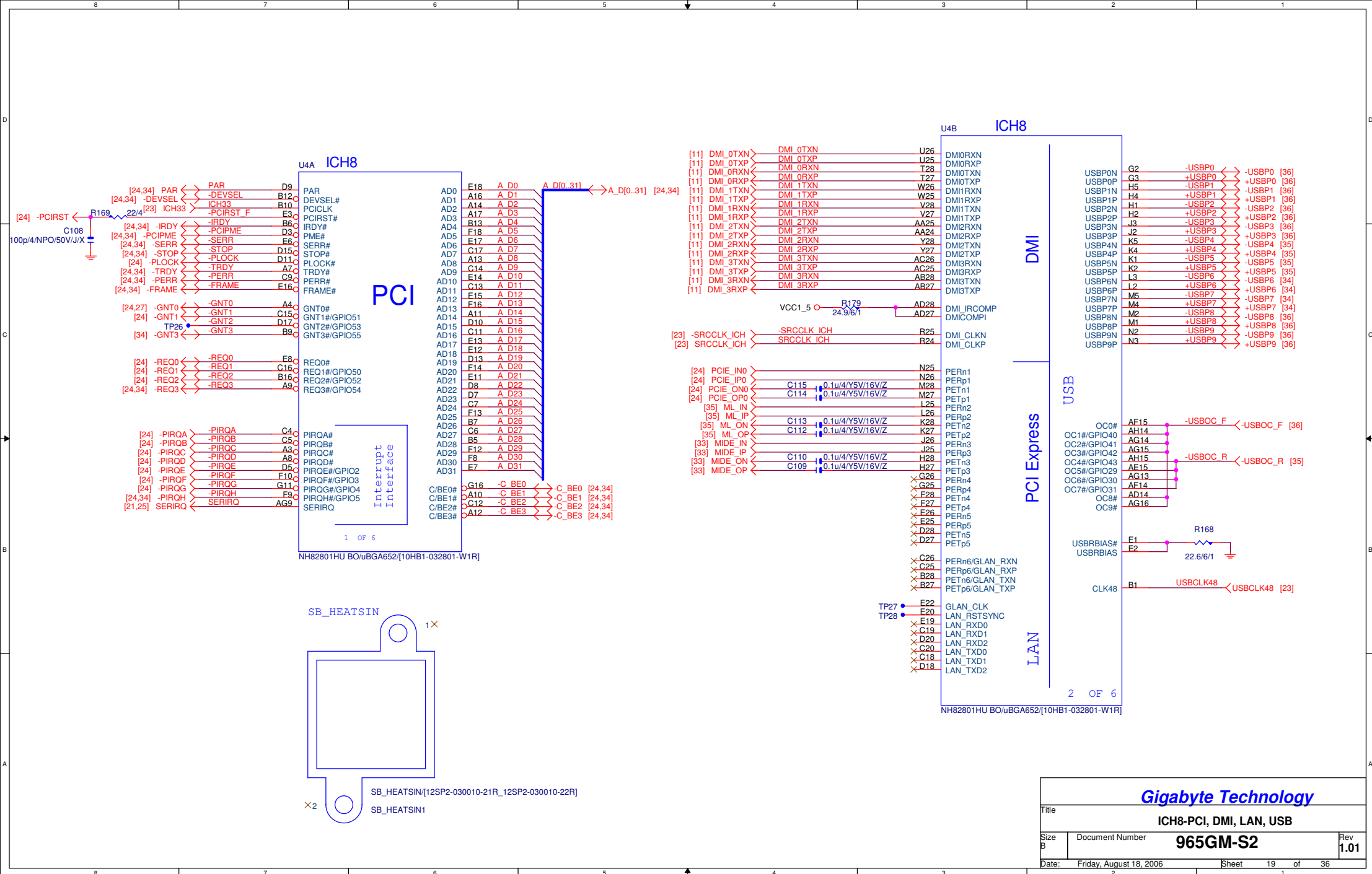
Friday, August 18, 2006

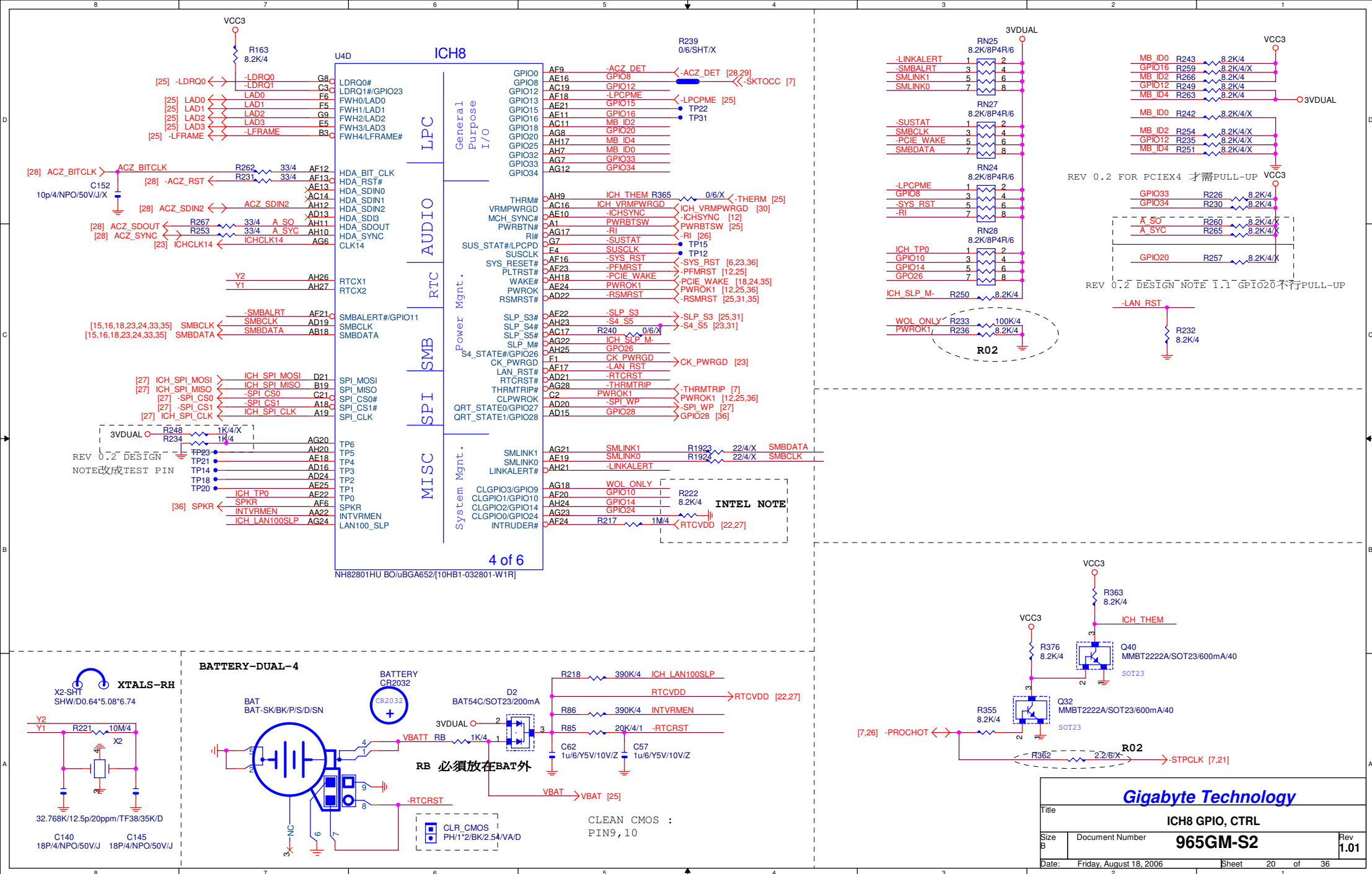
Sheet

18 of 36

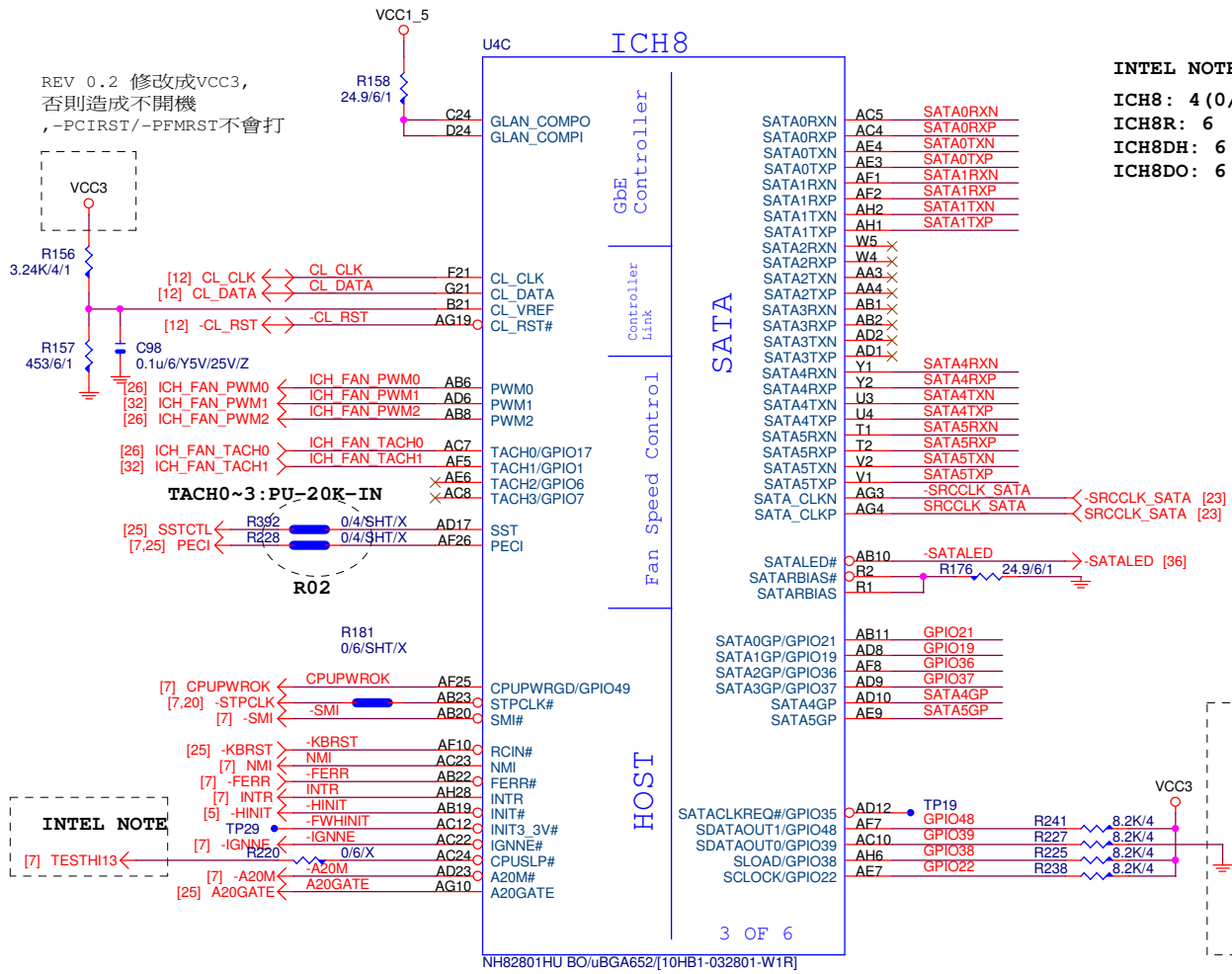
Rev

1.01

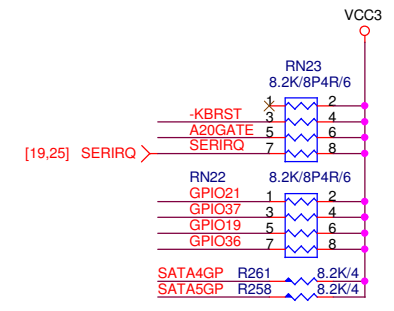




REV 0.2 修改成VCC3,
否則造成不開機
,-PCIRST/-PFMRST不會打

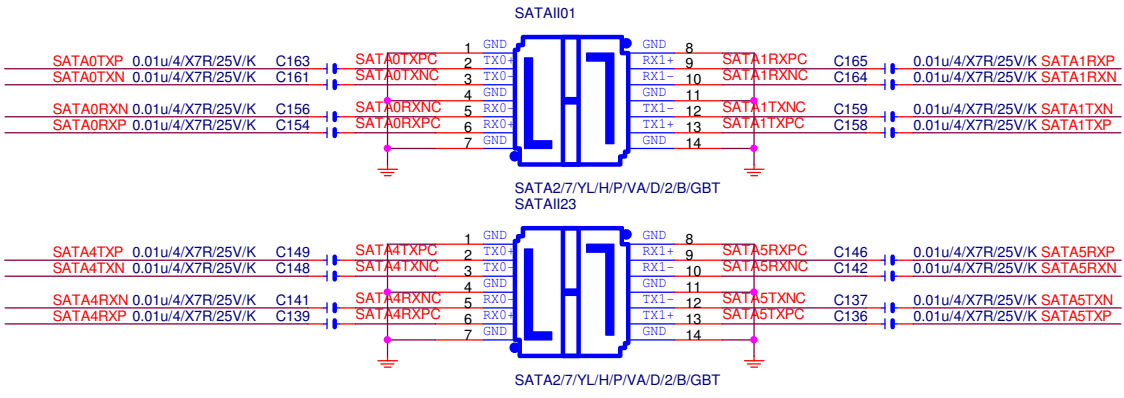


INTEL NOTE:SATAII PORT
ICH8: 4(0/1/4/5 PORT,2/3:N/A)
ICH8R: 6
ICH8DH: 6
ICH8DO: 6



The ICH8 integrated GbE LAN test mode is activated any time the ICH8 GPIO39 signal is not at a low logic level.

Workaround
Under investigation. Possible workaround is to use a weak pulldown resistor on GPIO39 to ensure signal is always low

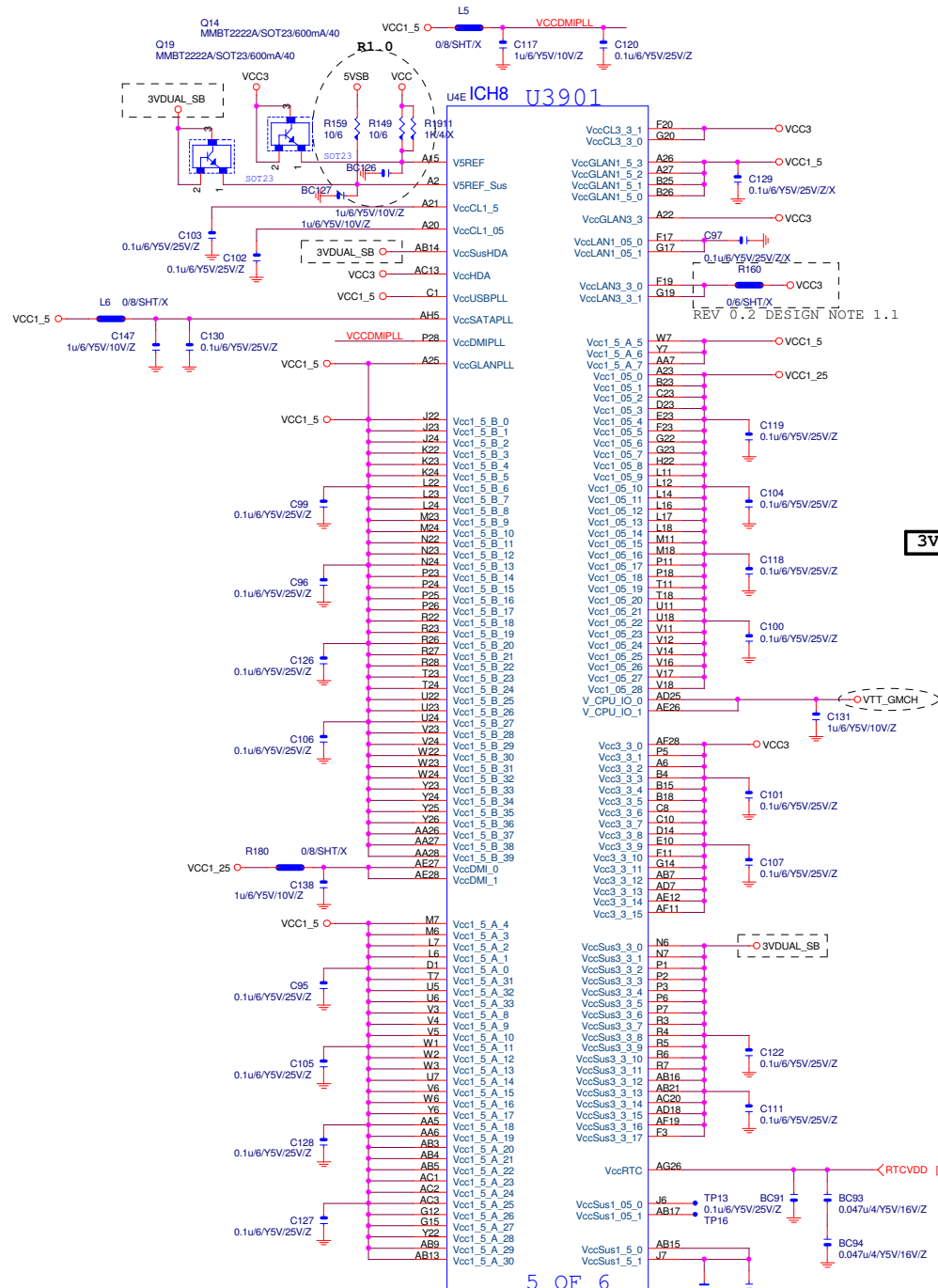


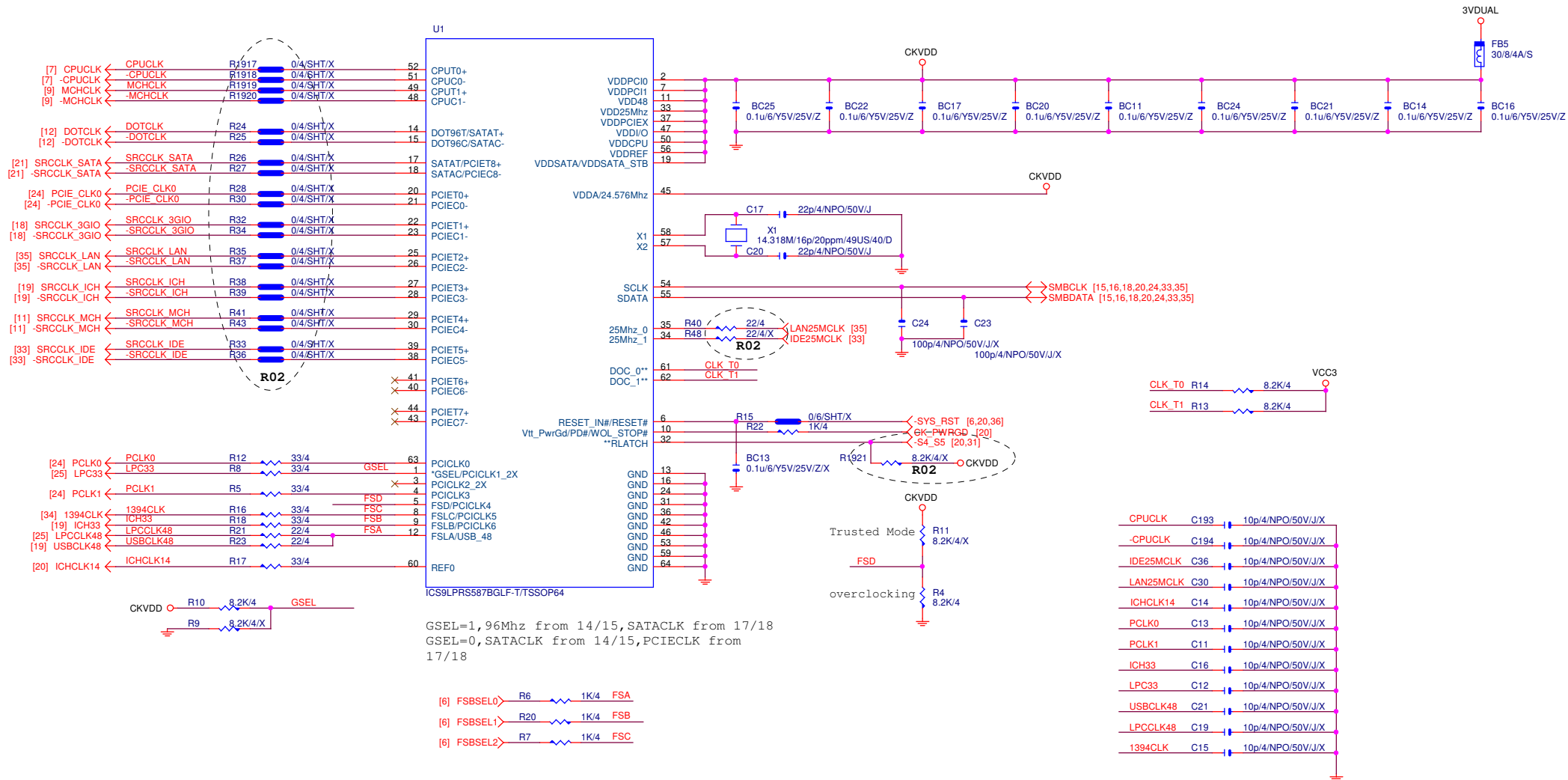
U4F ICH8

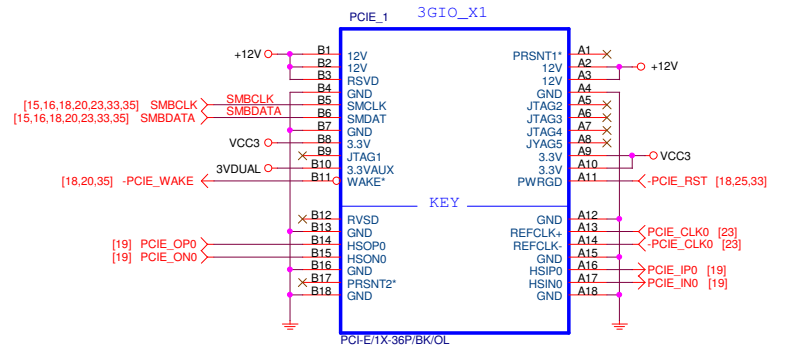
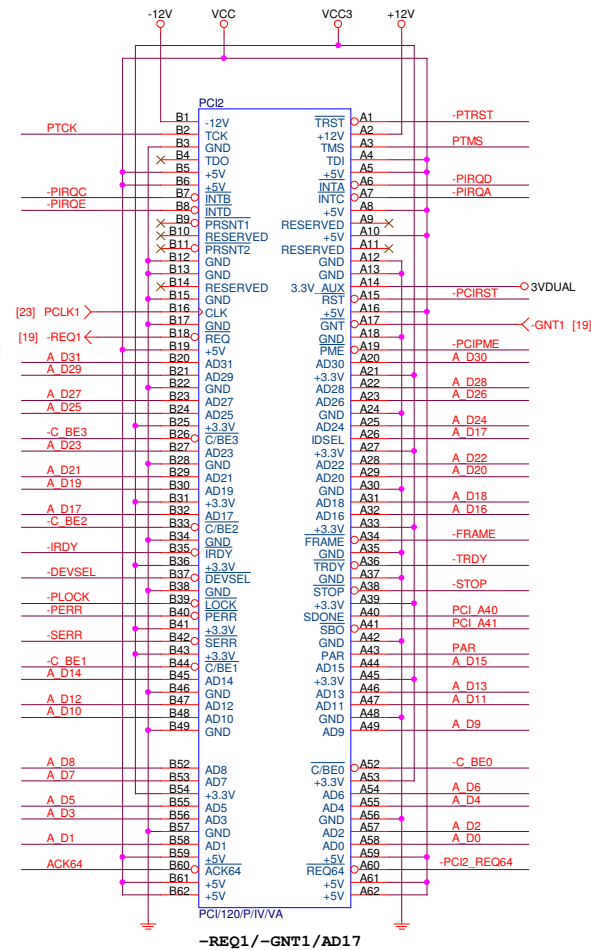
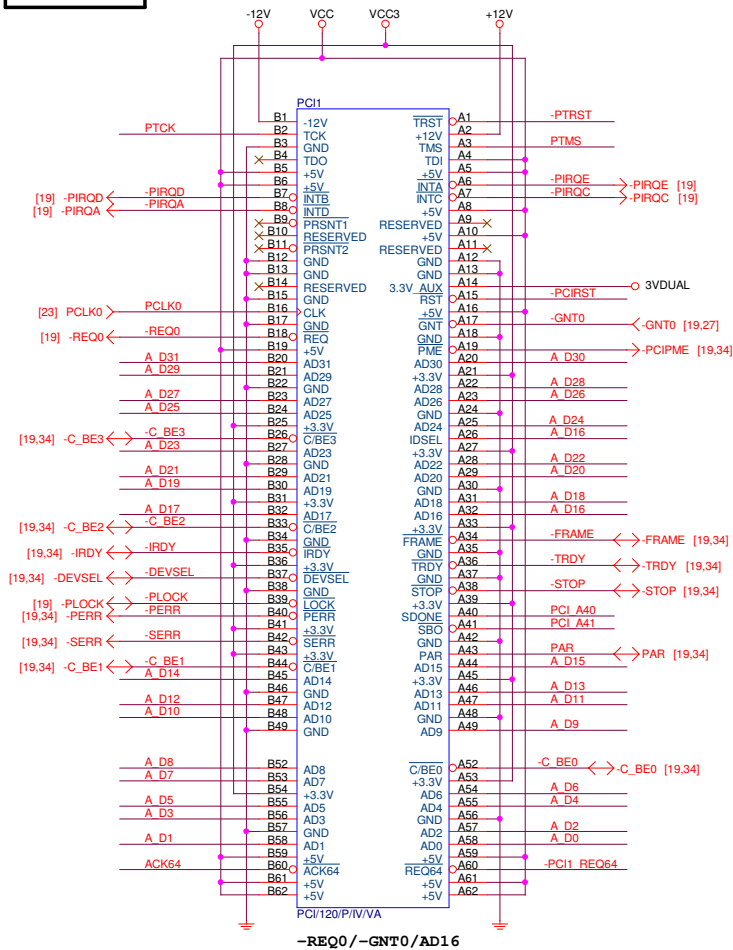
R11	VSS_099	P27
R12	VSS_100	P22
R13	VSS_101	VSS_097
R14	VSS_102	VSS_096
R15	VSS_103	VSS_095
R16	VSS_104	VSS_094
R17	VSS_105	VSS_093
R18	VSS_106	VSS_092
T3	VSS_107	VSS_091
T4	VSS_108	VSS_090
T5	VSS_109	VSS_089
T6	VSS_110	VSS_088
T12	VSS_111	VSS_087
T13	VSS_112	VSS_086
T14	VSS_113	VSS_085
T15	VSS_114	VSS_084
T16	VSS_115	VSS_083
T17	VSS_116	VSS_082
T25	VSS_117	VSS_081
T26	VSS_118	VSS_080
U1	VSS_119	VSS_079
U2	VSS_120	VSS_078
U12	VSS_121	VSS_077
U13	VSS_122	VSS_076
U14	VSS_123	VSS_075
U15	VSS_124	VSS_074
U16	VSS_125	VSS_073
U17	VSS_126	VSS_072
U27	VSS_127	VSS_071
U28	VSS_128	VSS_070
V7	VSS_129	VSS_069
V13	VSS_130	VSS_068
V15	VSS_131	VSS_067
V22	VSS_132	VSS_066
V25	VSS_133	VSS_065
V26	VSS_134	VSS_064
V27	VSS_135	VSS_063
W28	VSS_136	VSS_062
Y3	VSS_137	VSS_061
Y4	VSS_138	VSS_060
Y5	VSS_139	VSS_059
AA1	VSS_140	VSS_058
AA2	VSS_141	VSS_057
AA3	VSS_142	VSS_056
AB2	VSS_143	VSS_055
AB4	VSS_144	VSS_054
AB5	VSS_145	VSS_053
AB6	VSS_146	VSS_052
AC6	VSS_147	VSS_051
AC9	VSS_148	VSS_050
AC15	VSS_149	VSS_049
AC18	VSS_150	VSS_048
AC21	VSS_151	VSS_047
AC27	VSS_152	VSS_046
AC28	VSS_153	VSS_045
AD3	VSS_154	VSS_044
AD4	VSS_155	VSS_043
AD5	VSS_156	VSS_042
AD11	VSS_157	VSS_041
AD26	VSS_158	VSS_040
AE1	VSS_159	VSS_039
AE2	VSS_160	VSS_038
AE5	VSS_161	VSS_037
AE8	VSS_162	VSS_036
AE17	VSS_163	VSS_035
AE14	VSS_164	VSS_034
AE20	VSS_165	VSS_033
AE23	VSS_166	VSS_032
AF3	VSS_167	VSS_031
AG1	VSS_168	VSS_030
AG2	VSS_169	VSS_029
AG5	VSS_170	VSS_028
AG11	VSS_171	VSS_027
AG25	VSS_172	VSS_026
AG27	VSS_173	VSS_025
AH3	VSS_174	VSS_024
AH4	VSS_175	VSS_023
AH13	VSS_176	VSS_022
AH16	VSS_177	VSS_021
AH19	VSS_178	VSS_020
AH22	VSS_179	VSS_019
	VSS_180	VSS_018
	VSS_181	VSS_017
	VSS_182	VSS_016
AH8	VSS_183	VSS_015
AF27	VSS_184	VSS_014
F4	VSS_185	VSS_013
B22	VSS_186	VSS_012
	VSS_187	VSS_011
	VSS_188	VSS_010
	VSS_189	VSS_009
	VSS_190	VSS_008
	VSS_191	VSS_007
	VSS_192	VSS_006
	VSS_193	VSS_005
	VSS_194	VSS_004
	VSS_195	VSS_003
	VSS_196	VSS_002
	VSS_197	VSS_001

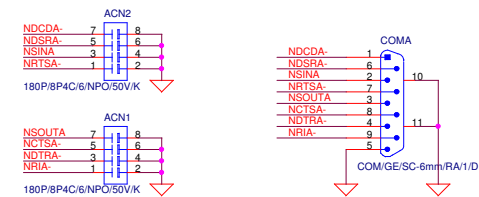
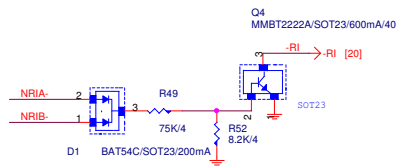
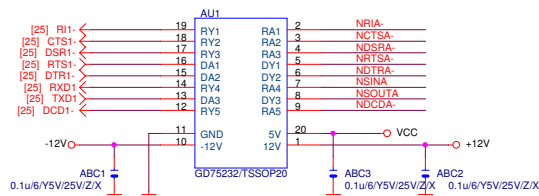
6 OF 6

NH82801HU BO/UBGA652(10HB1-032801-W1R)

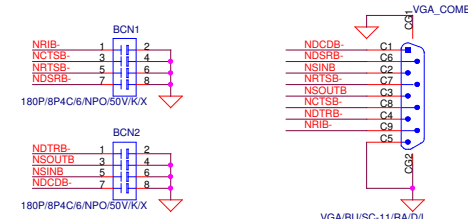
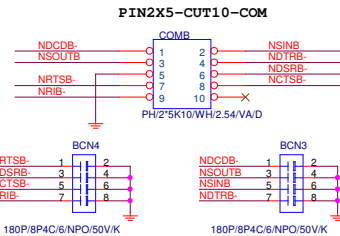
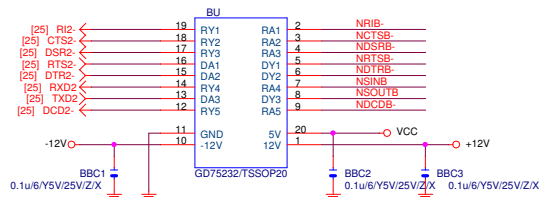




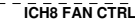
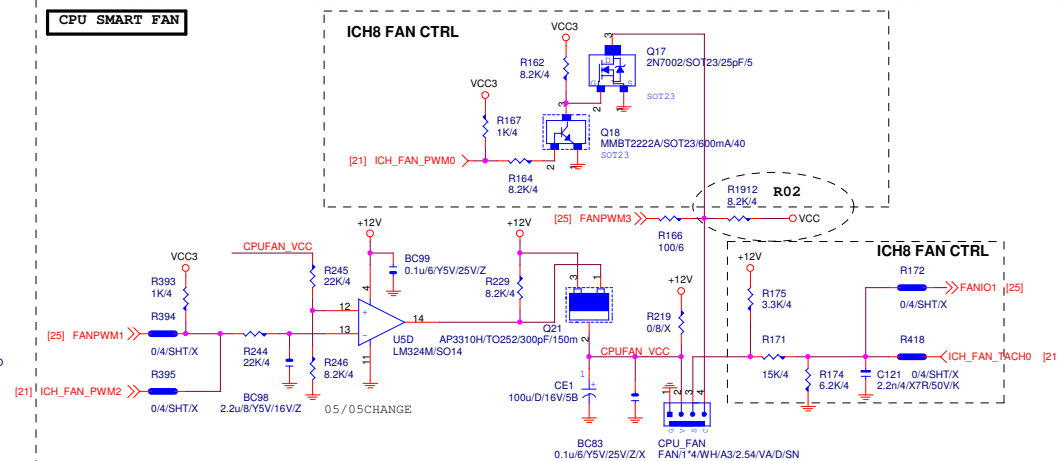
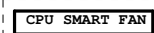
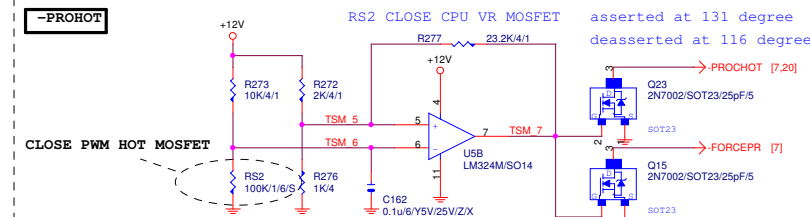
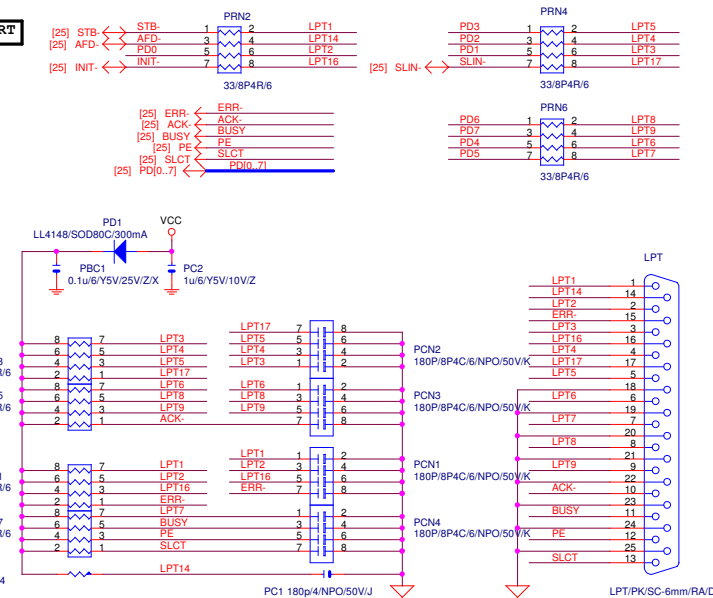
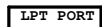




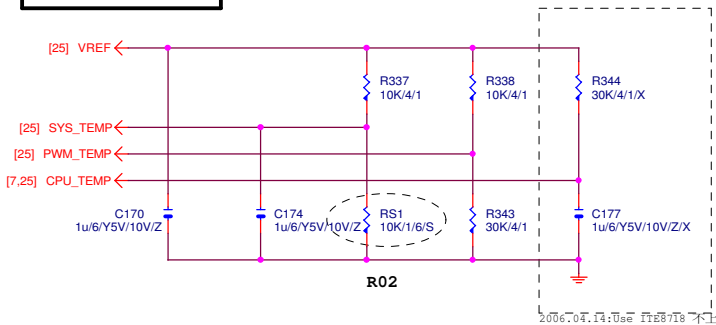
PLACE NEAR COM CONNECTOR



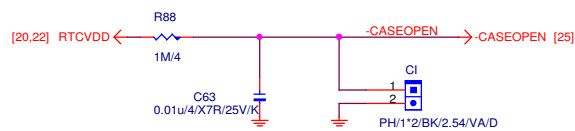
PLACE NEAR VGA_COM CONNECTOR



TEMP H/W MONITOR

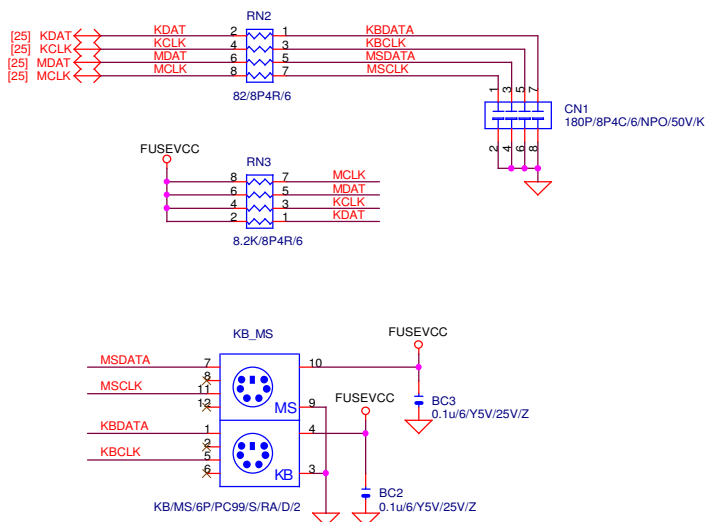


CASE OPEN

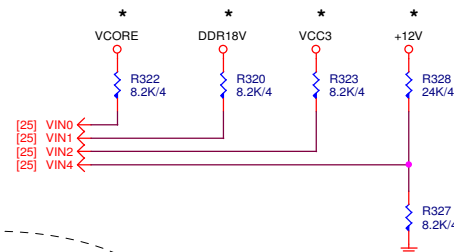


Case Open Circuits

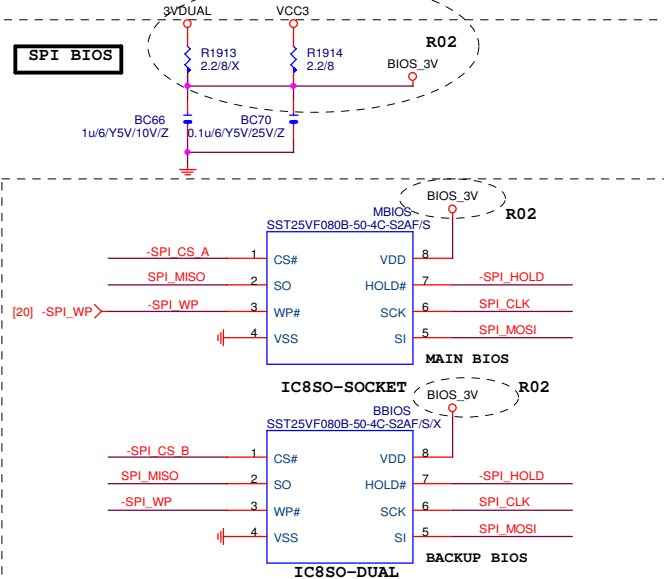
KB/MS



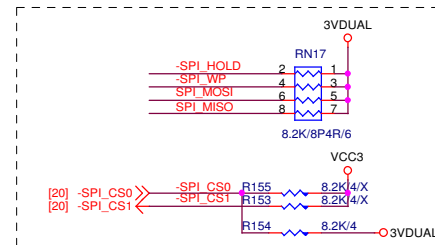
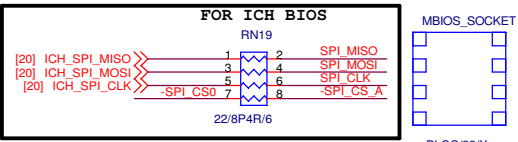
VOLTAGE-- H/W MONITOR



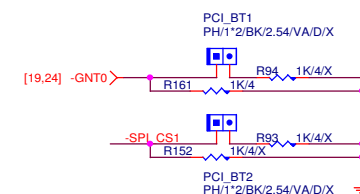
SPI BIOS



FOR ICH BIOS



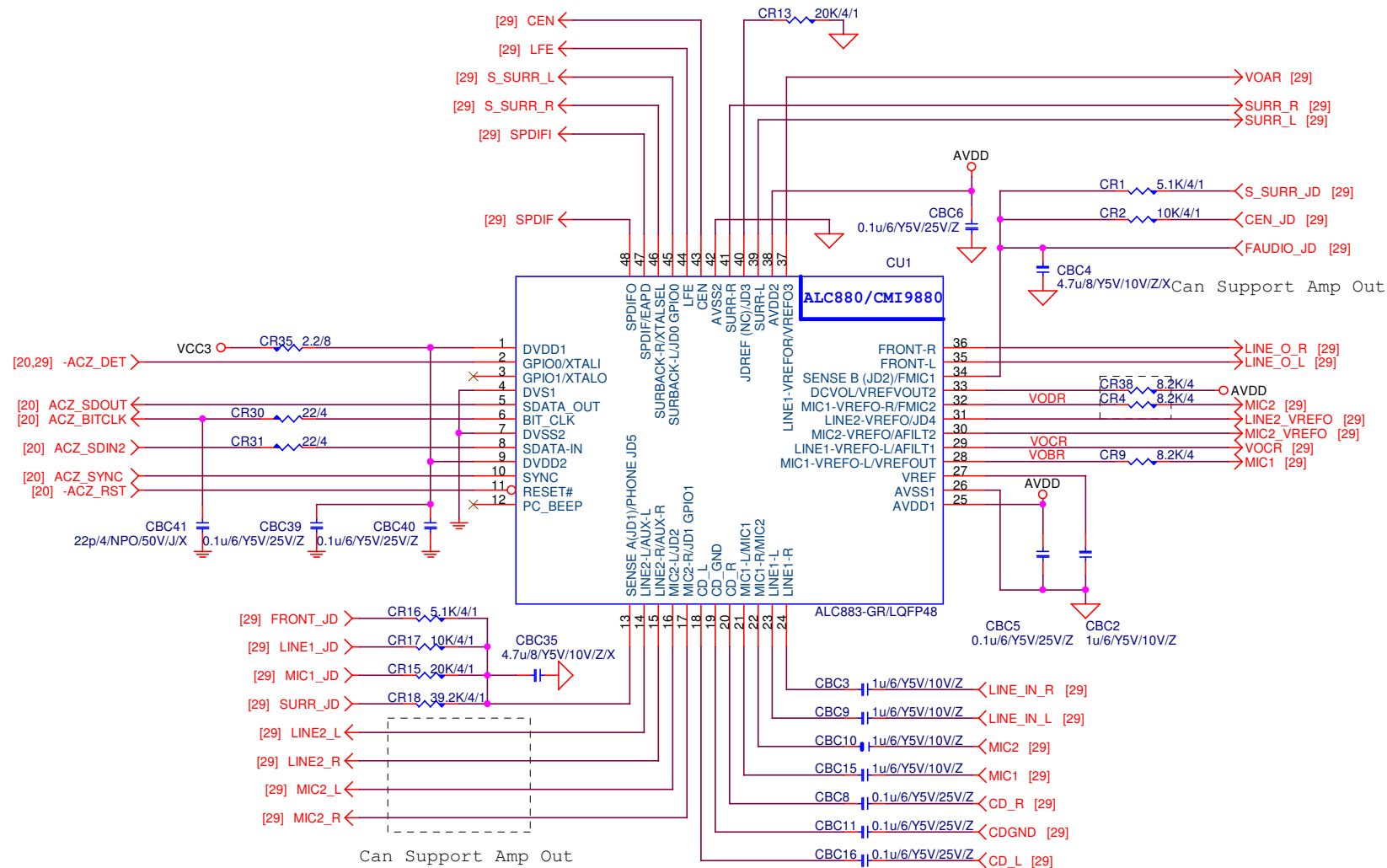
FOR ITE8718 DUAL BIOS



BOOT DEVICE	GNT0	CS1
SPI	0	X
PCI	1	0
FWH	1	1

Gigabyte Technology

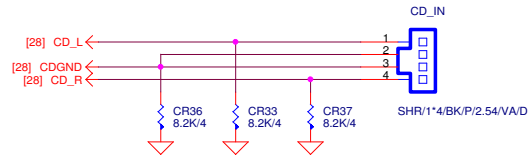
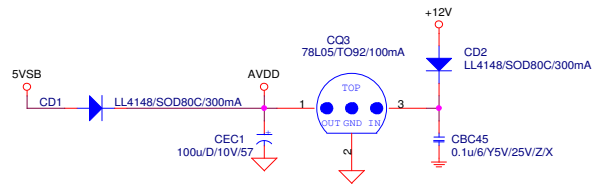
Title		
BIOS/HW-MONITOR/CI/KB/MS		
Size B	Document Number	Rev
	965GM-S2	1.01
Date:	Friday, August 18, 2006	Sheet 27 of 36



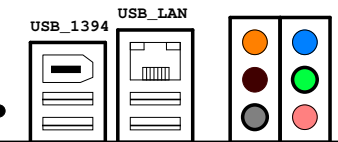
Gigabyte Technology

Title		
AZALIA ALC883		
Size	Document Number	Rev
Custom	965GM-S2	1.01
Date: Friday, August 18, 2006		
Sheet 28 of 36		

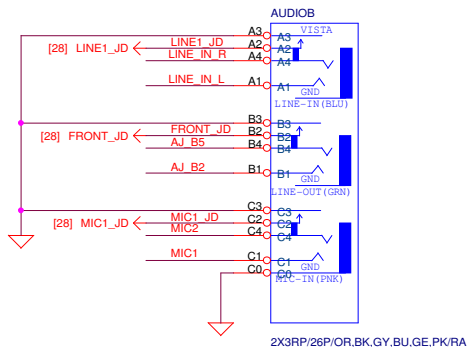
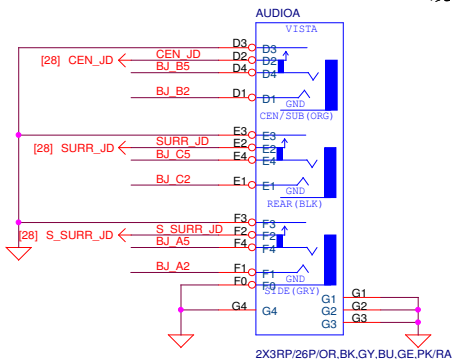
CD IN



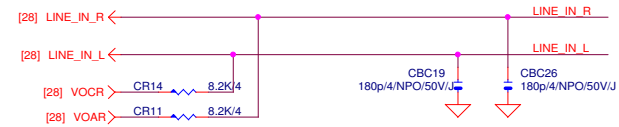
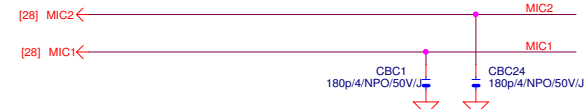
AZALIA JACK



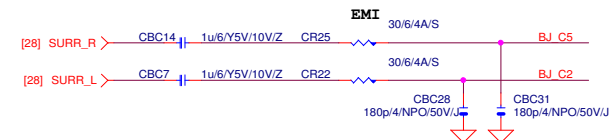
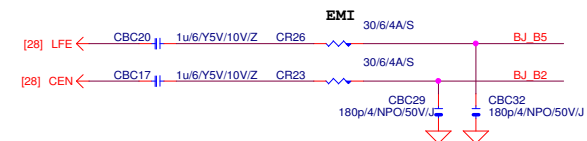
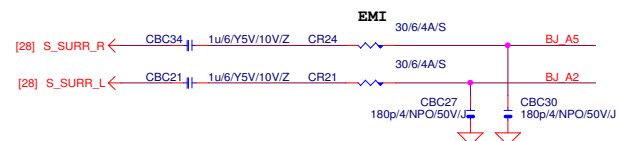
3RP/26P/OR,BK,GY,BU,GE,PK/RA/D/1/B
VISTA規範: REAR-->BLK,CEN/SUB-->ORG



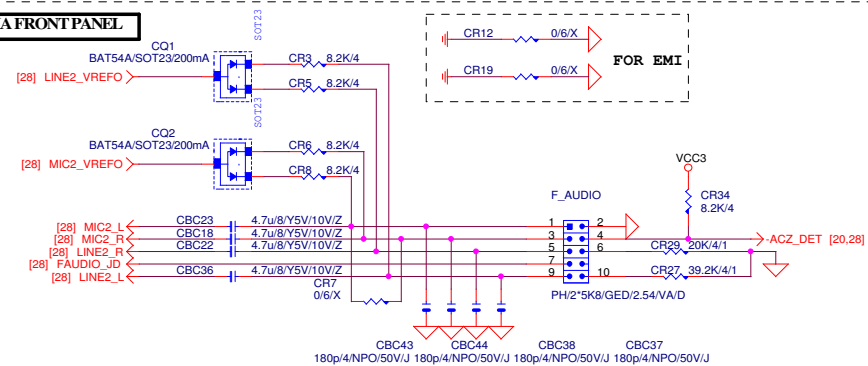
LINE-IN

**MIC-IN**

SURROUND

**CEN/LFE****SURR BACK**

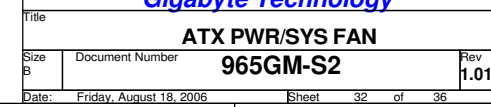
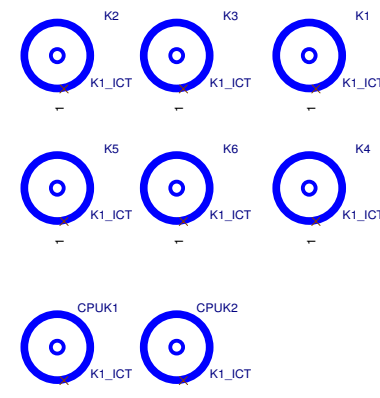
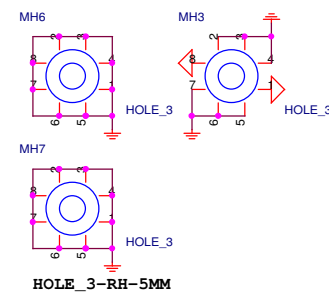
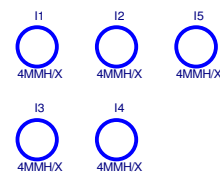
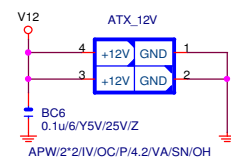
AZALIA FRONT PANEL

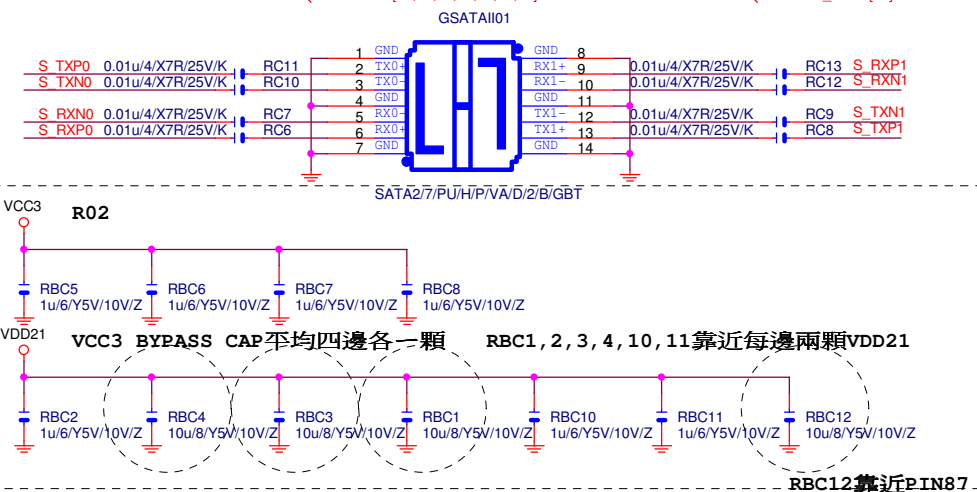
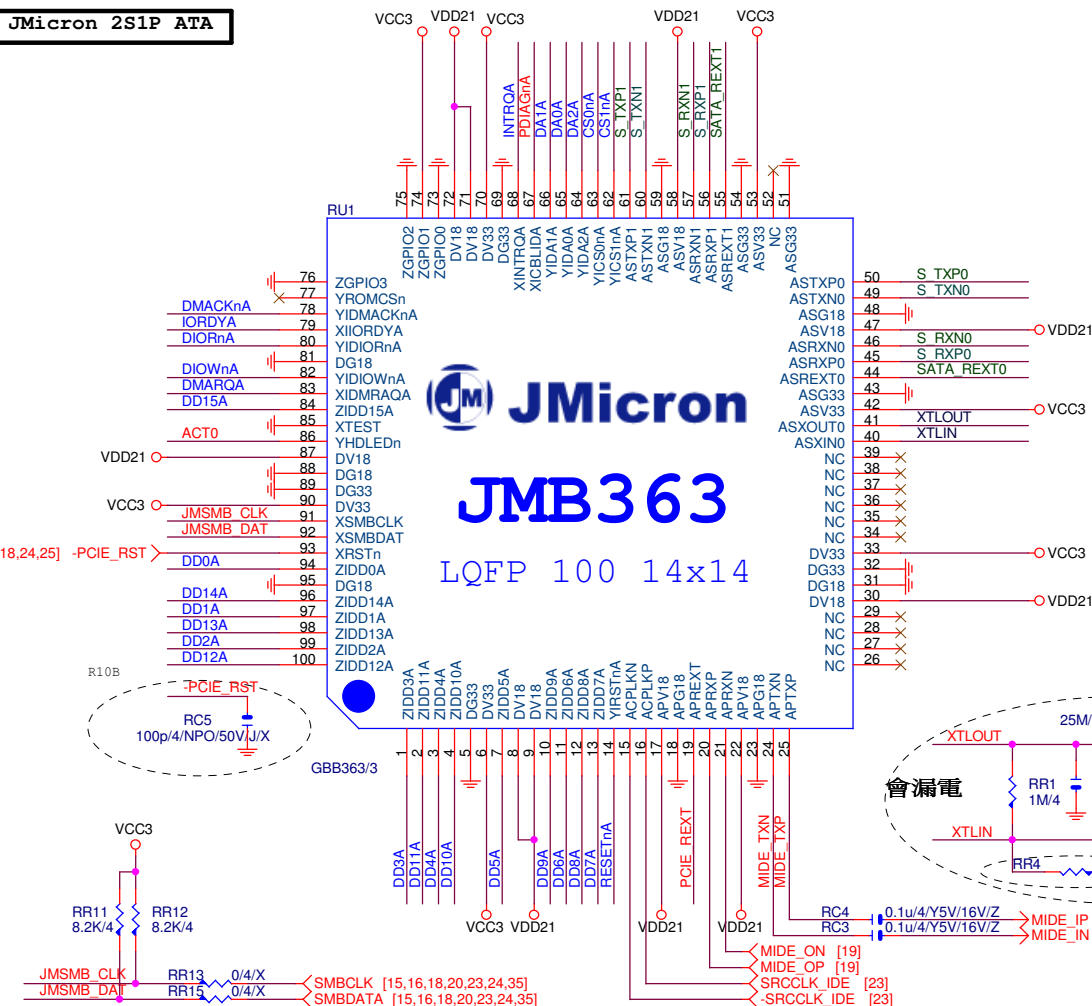


Gigabyte Technology

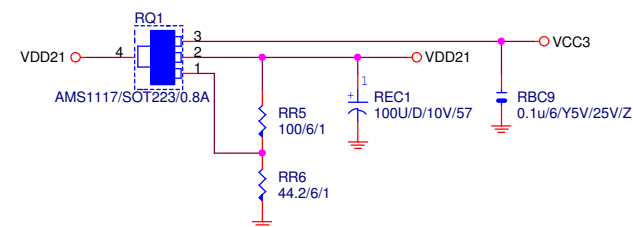
Title			
AUDIO JACK			
Size Custom	Document Number	965GM-S2	Rev 1.01
Date:	Friday, August 18, 2006	Sheet 29 of 36	

ATXPWR_24-2

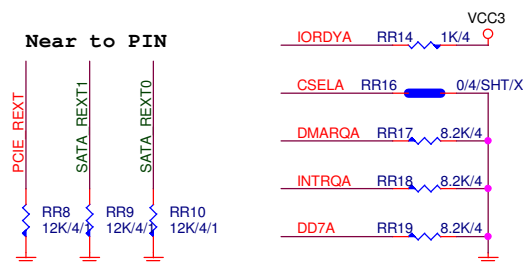
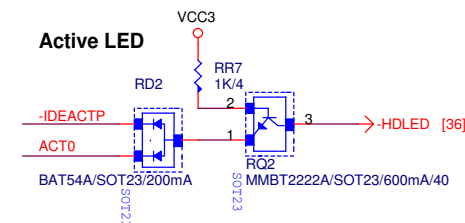




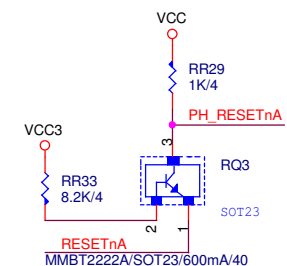
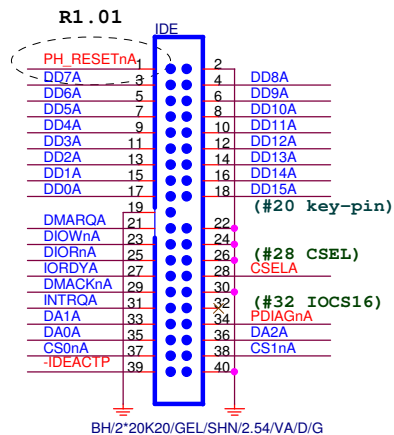
3.3V to 1.8V Voltage Regulator

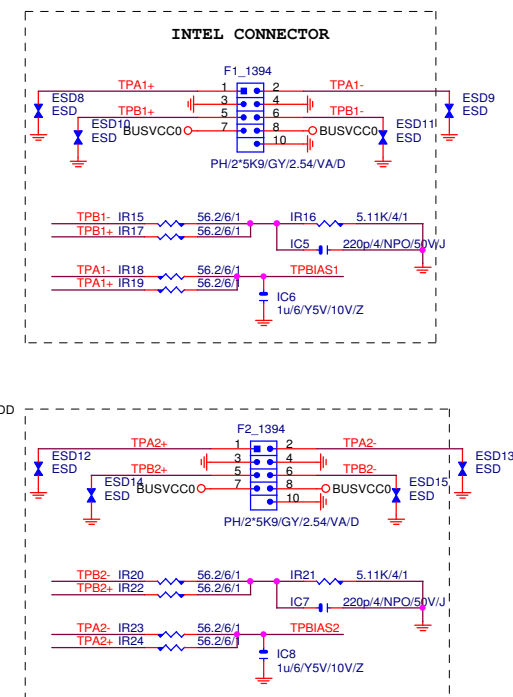
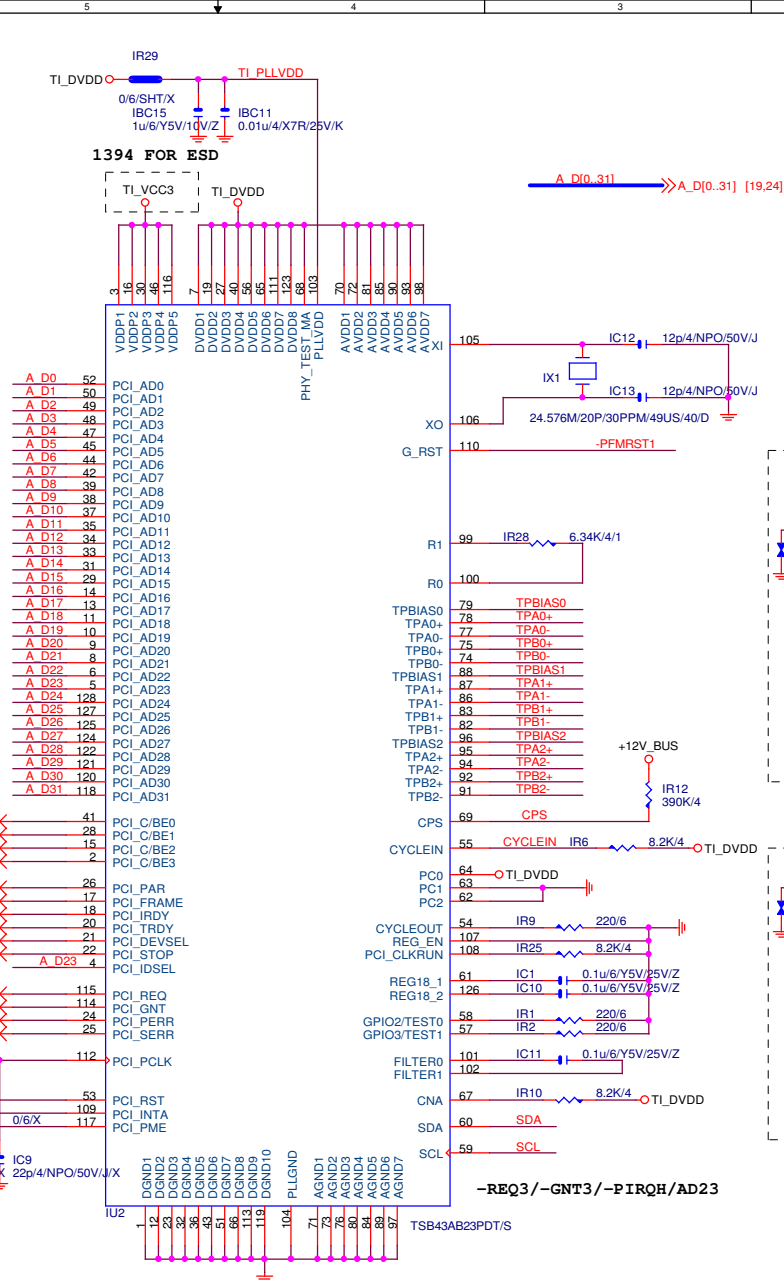
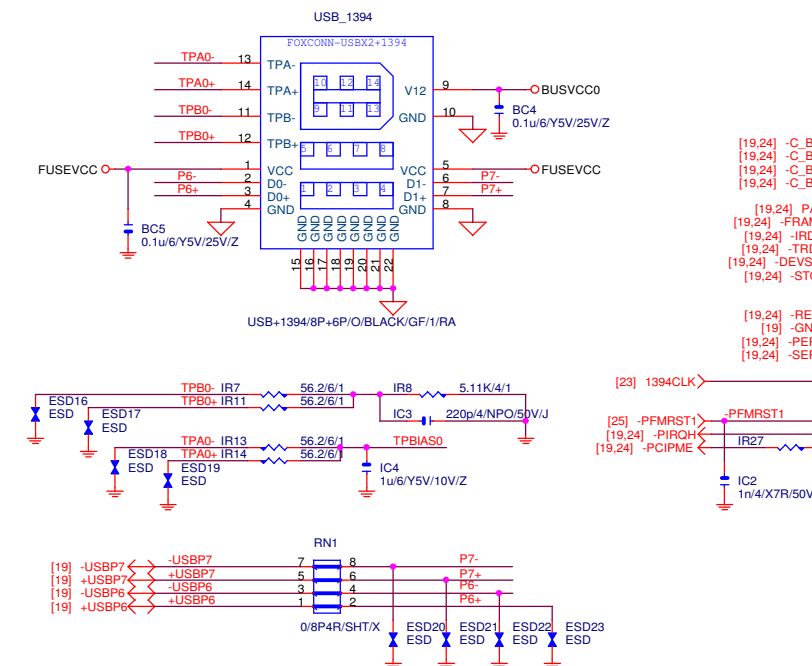


JMicron suggest to change 1.8V to 2.1V



IDE Connector



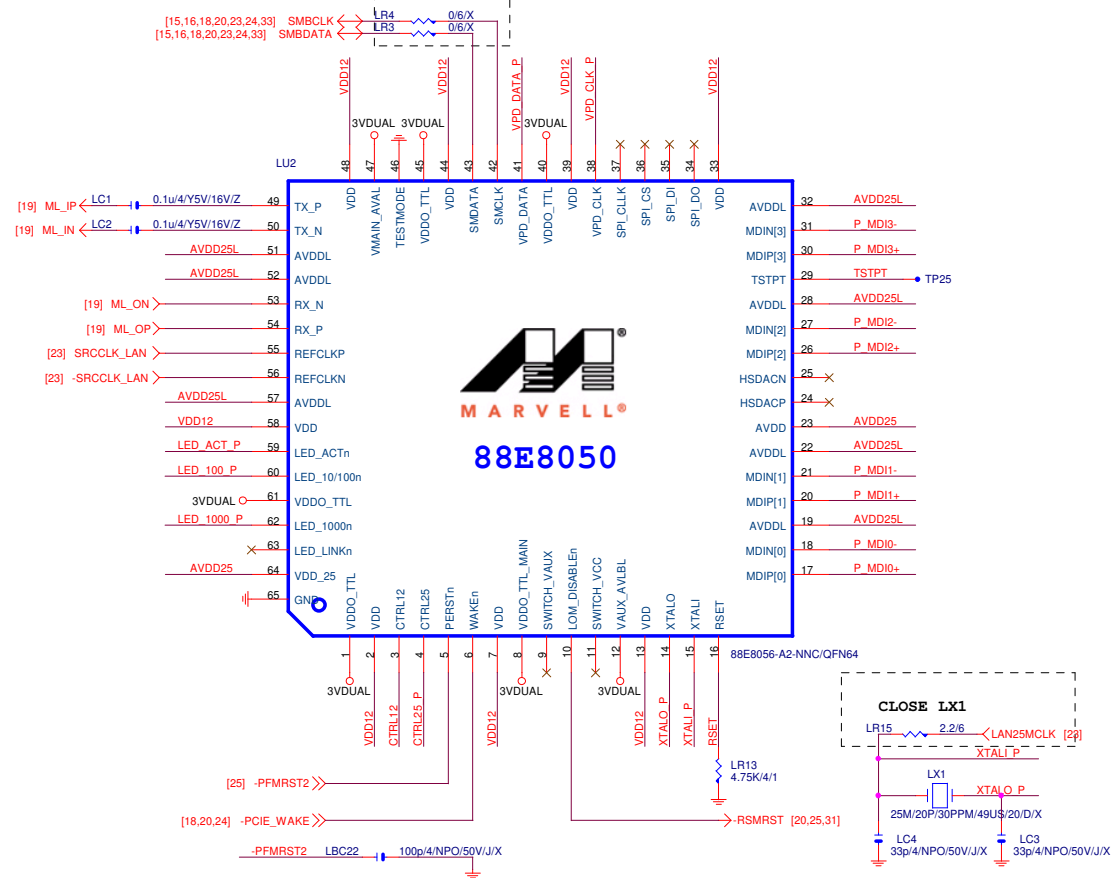


PCIE-1G LAN

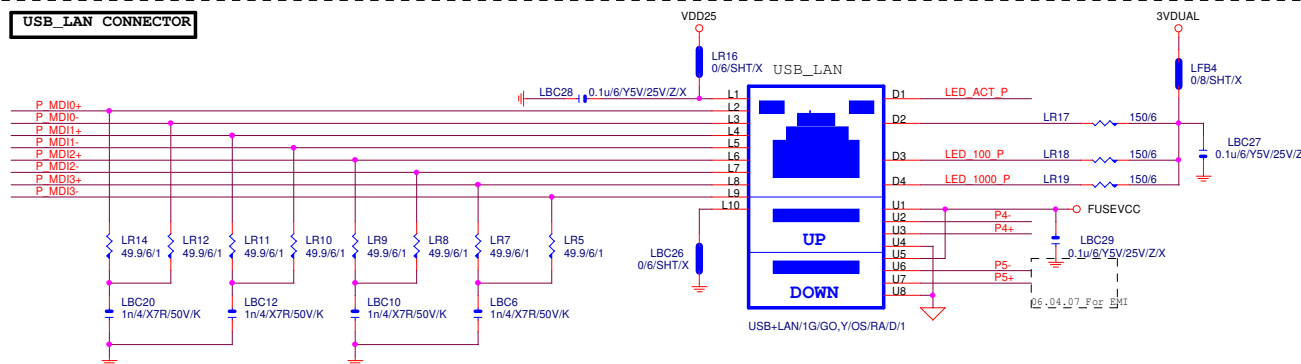
Layout Check 注意事項

1. LUL PIN6 需下內層GND, 打 I2 VIA
2. 3VDDAL, VCC3, VDD15_L, AVDD25_L
至少下20mil寬, 並且電容擺設每兩pin至少放一顆Bypass Cap.
3. X'TAL 25MHz 兩訊號線, TRACE 愈短愈好, 線寬12mil
4. MDI正負0~3, TRACE 8:7:8, 每對之間保持 40mil

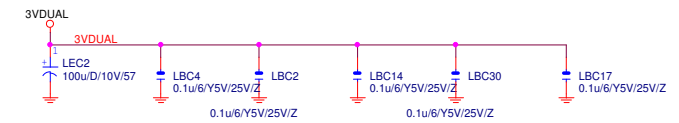
88E8056 NO POP, I2C FAIL



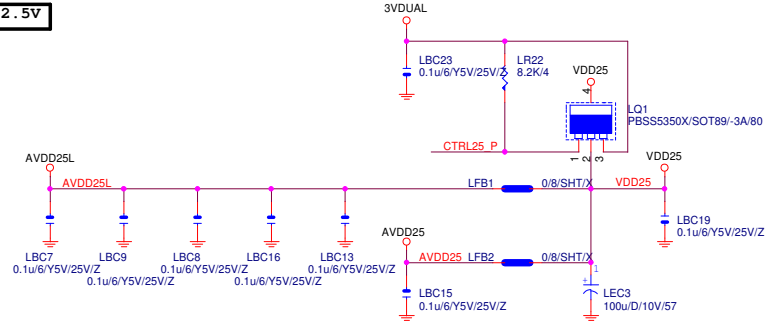
USB_LAN CONNECTOR



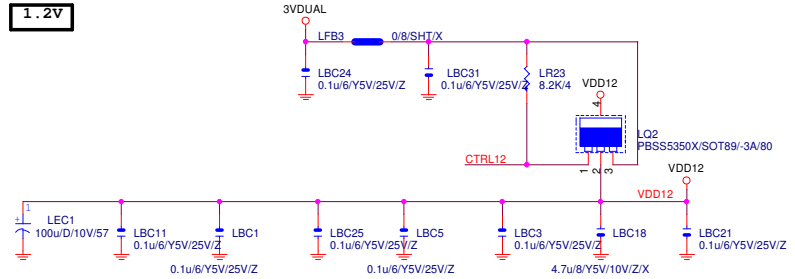
3VDUAL



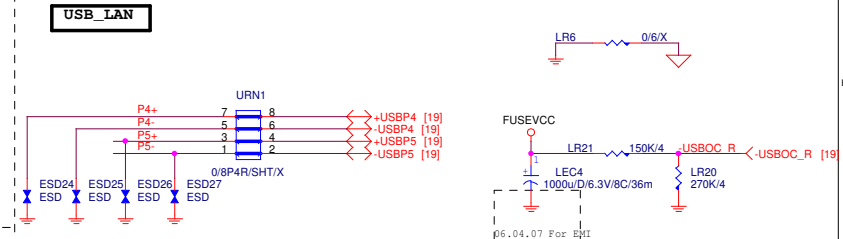
2.5V



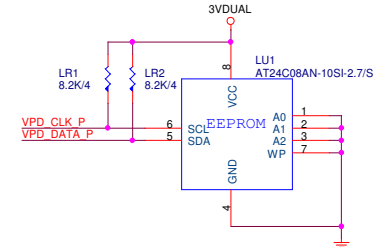
1.2V



USB_LAN



EEPROM



<i>Gigabyte Technology</i>			
MARVELL 88E8056			
Size Custom	Document Number	965GM-S2	Rev 1.01
Date:	Friday, August 18, 2006	Sheet 35 of 36	

FRONT USB1



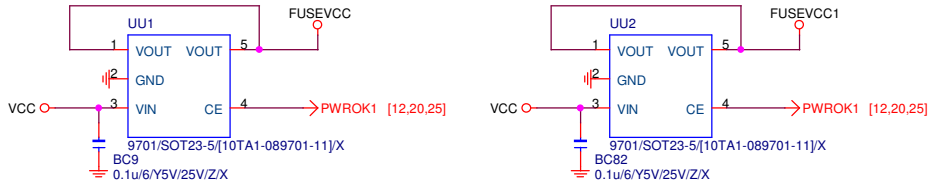
FRONT USB2



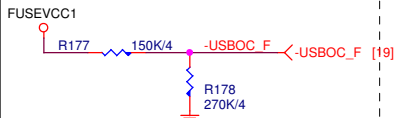
FRONT USB3



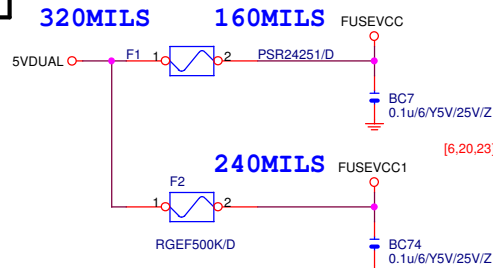
USB DROP



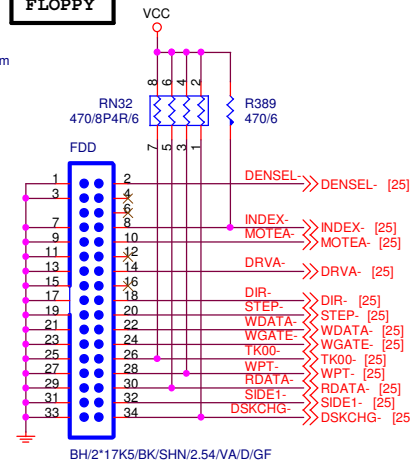
FRONT USB OC1



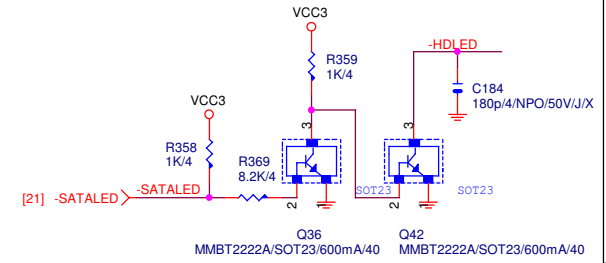
USB POWER



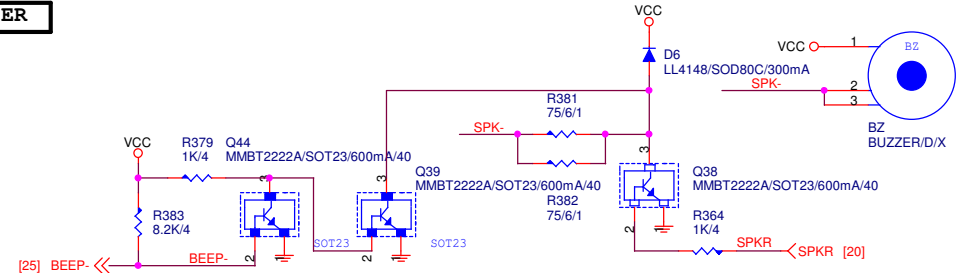
FLOPPY



SATA LED



BUZZER



INTEL FRONT PANEL

