

Model Name: 965P-DQ6

Revision 1.01F

SHEET

TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	POWER MAP
05	P4_LGA775_A
06	P4_LGA775_B
07	P4_LGA775_C
08	P4_LGA775_D
09	GMCH-BROADWATER_HOST
10	GMCH-BROADWATER_DDRII
11	GMCH-BROADWATER_PCI E, DMI
12	GMCH-BROADWATER_INT VGA
13	GMCH-BROADWATER_GND
14	GMCH-BROADWATER_PWR
15	DDRII CHANNEL A 1,2
16	DDRII CHANNEL B 1,2
17	DDRII TERMINATION
18	PCI EXPRESS*16 SLOT
19	ICH8 PCI, USB, DMI, LAN
20	ICH8 GPIO, CTRL
21	ICH8 SATA, FAN PWM
22	ICH8 VCC, GND
23	CLOCK GEN ICS9LPRS587
24	PCI EXPRESS X4 PORT1 SLOT
25	PCI SLOT 1, 2, 3
26	PCIE_1, SW
27	ITE 8718 CX

SHEET

TITLE

28	COM_LPT, -PROHOT, DYNAMIC OC
29	DUAL BIOS
30	ALC888DD
31	REAR AUDIO JACK
32	VCORE PWM_ISL6307-1
33	VCORE PWM_ISL6307-2
34	VCORE PWM_ISL6307-3
35	DISCRETE POWER
36	ATX, OTHERS POWER
37	MARVELL 88E8053
38	TI TSB43AB23 1394
39	FP, FUSB, FDD
40	JMB363
41	CI, HWM, KB/MS, FAN CTRL
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43	
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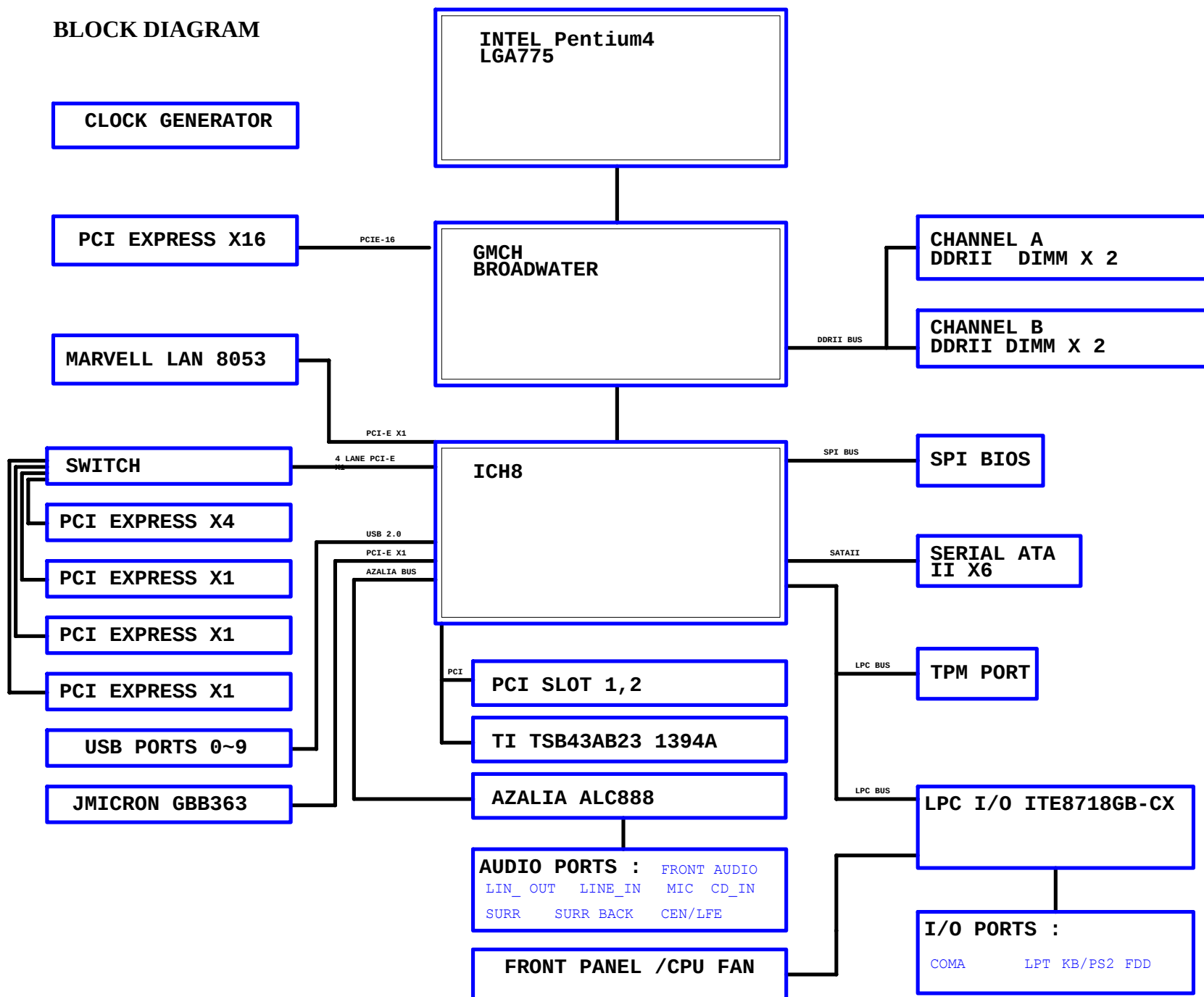
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Title		
Cover Sheet		
Size	Document Number	Rev
Custom	965P-DQ6	1.01F
Date:	Wednesday, August 09, 2006	Sheet 1 of 41

Circuit or PCB layout change for next version

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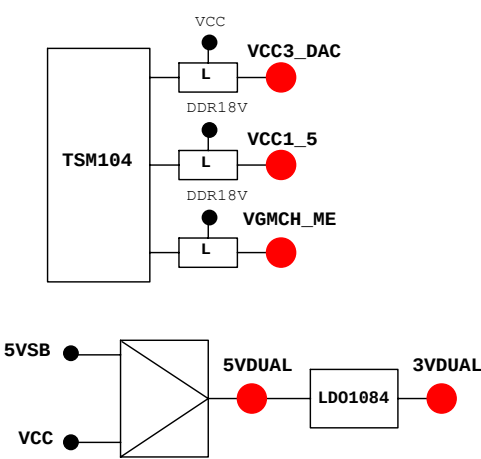
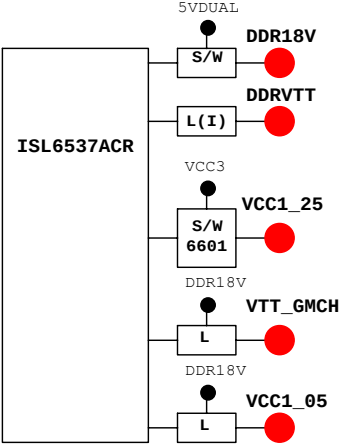
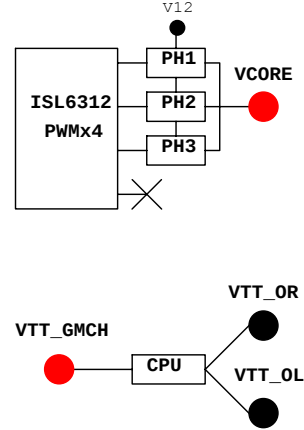
BLOCK DIAGRAM



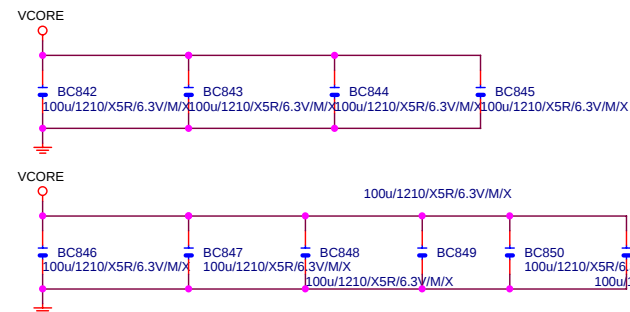
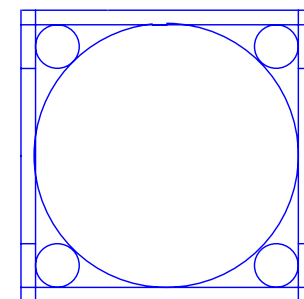
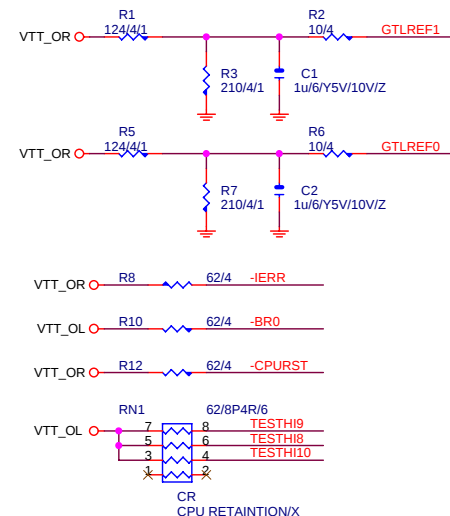
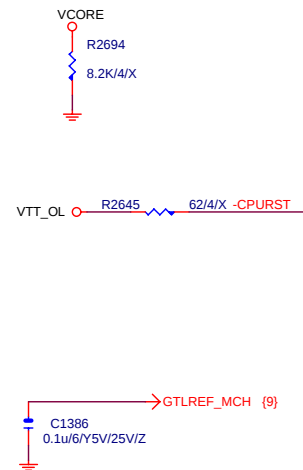
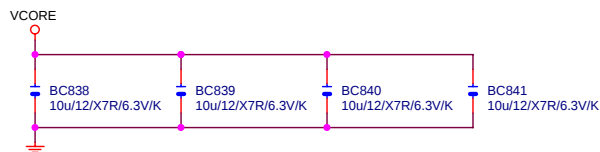
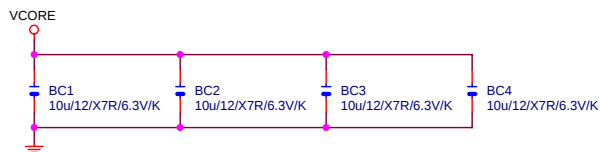
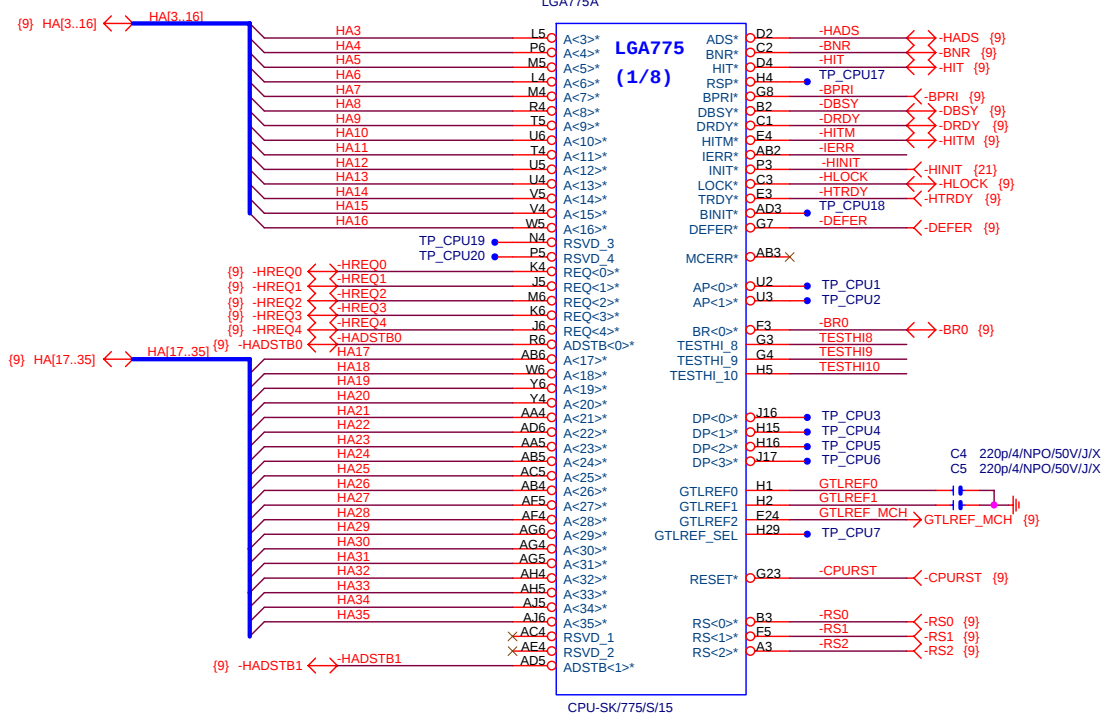
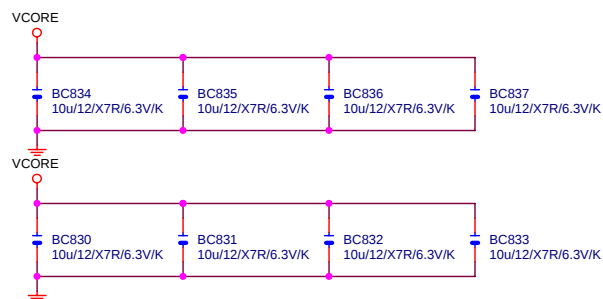
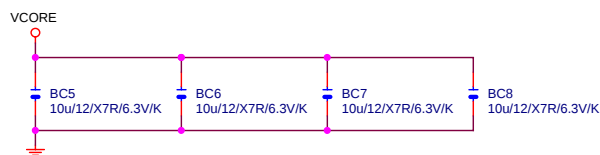
ICH8 GPIO LIST TABLE

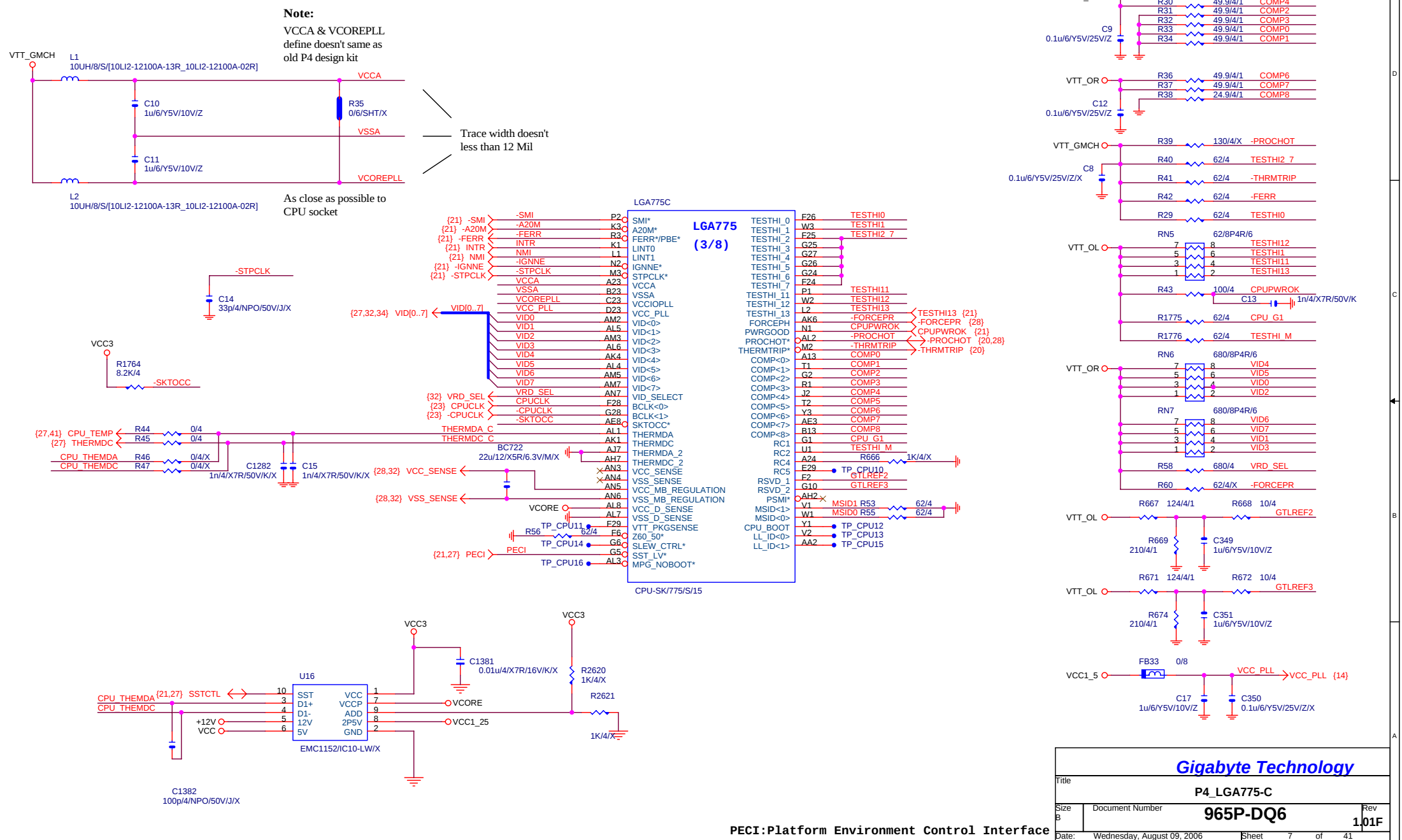
PIN	NAME	PWR WELL	AFTER/ ELTRST	USAGE	NOTE
GP0		MAIN	IN	-ACZ_DET	P/U 8.2K VCC3
GP1/TACH1		MAIN	IN	ICH_FAN_TACH1	P/U 8.2K VCC3
GP2/PIRQE#		MAIN	IN	-PIRQE	P/U 8.2K VCC3
GP3/PIRQF#		MAIN	IN	-PIRQF	P/U 8.2K VCC3
GP4/PIRQ6#		MAIN	IN	-PIRQ6	P/U 8.2K VCC3
GP5/PIRQH#		MAIN	IN	-PIRQH	P/U 8.2K VCC3
GP6/TACH2		MAIN	IN	ICH_FAN_TACH2	P/U 8.2K VCC3
GP7/TACH3		MAIN	IN	VTT_GMCH_OV3	P/U 8.2K VCC3
GP8		STBY	IN	GPI08(DUALBIOS_INPUT)	P/U 8.2K 3VDUAL
GP9		STBY	OUT	WOL_ONLY	P/D 100K GND
GP10		STBY	IN	CLGPIO1	P/U 8.2K 3VDUAL
GP11/SMBALERT#		STBY	OUT	-SMBALRT	P/U 8.2K 3VDUAL
GP12		STBY	IN	DDR18V_OV5	P/U 8.2K 3VDUAL
GP13		STBY	IN	-LPCPME	P/U 8.2K 3VDUAL
GP14		STBY	IN	CLGPIO2	P/U 8.2K 3VDUAL
GP15		STBY	OUT	RM	N/A
GP16		MAIN	OUT/LOW	RESET	N/A
GP17/TACH0		MAIN	IN	ICH_FAN_TACH0	P/U 8.2K VCC3
GP18		MAIN	OUT	MB_ID1	P/U 8.2K VCC3
GP19		MAIN	IN	VCC15_OV1	P/U 8.2K VCC3
GP20		MAIN	OUT	-SPI_WP0	P/U 1K 3VCL
GP21		MAIN	IN	VCC15_OV3	P/U 8.2K VCC3
GP22		MAIN	IN	VCORE_OV3	P/U 8.2K VCC3
GP23		MAIN	OUT	-LDRQ1	P/U 8.2K VCC3
GP24		STBY	OUT	TLS	P/U 8.2K 3VDUAL
GP25		STBY	IN	MB_ID2(STP_CPU-)	P/U 8.2K 3VDUAL
GP26/S4_STATE#		STBY	OUT	S4_STATE#	P/U 8.2K 3VDUAL
GP27		STBY	OUT/LOW	GPI027(EL_STATE0)	P/U 8.2K 3VDUAL
GP28		STBY	OUT/LOW	-SPI_WP0	N/A
GP29/OC5#		STBY	IN	-USB0C_R	P/U FUSEVCC
GP30/OC6#		STBY	IN	-USB0C_R	P/U FUSEVCC
GP31/OC7#		STBY	IN	-USB0C_R	P/U FUSEVCC
GP32		MAIN	OUT	DUAL_BIOS	P/U 100K+1M VCC3
GP33		MAIN	OUT	DUAL_BIOS	P/U 8.2K VCC3
GP34		MAIN	OUT/LOW	GPI034/SMB_RST	N/A
GP35		MAIN	OUT	VCC15_OV2	N/A
GP36		MAIN	IN	VCORE_OV4	P/U 8.2K VCC3
GP37		MAIN	IN	VCORE_OV5	P/U 8.2K VCC3
GP38		MAIN	IN	VCORE_OV2	P/U 8.2K VCC3
GP39		MAIN	IN	GPI039	P/D 8.2K GND
GP48		MAIN	IN	VCORE_OV1	P/U 8.2K VCC3
GP49		MAIN	IN	CPUPWROK	P/U 100 VTT_OL

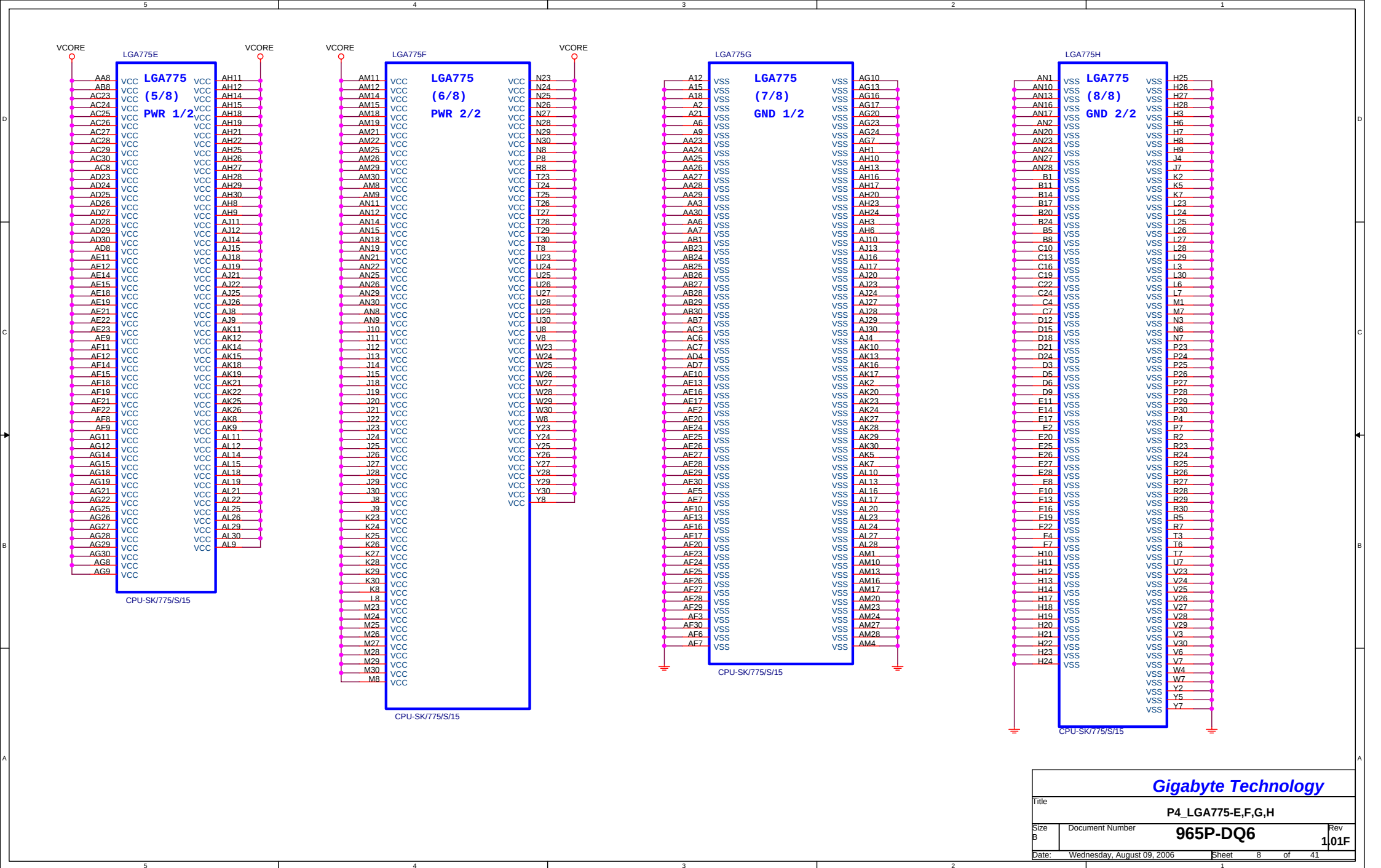
VCORE:3 PHASE PWM--ISL6312

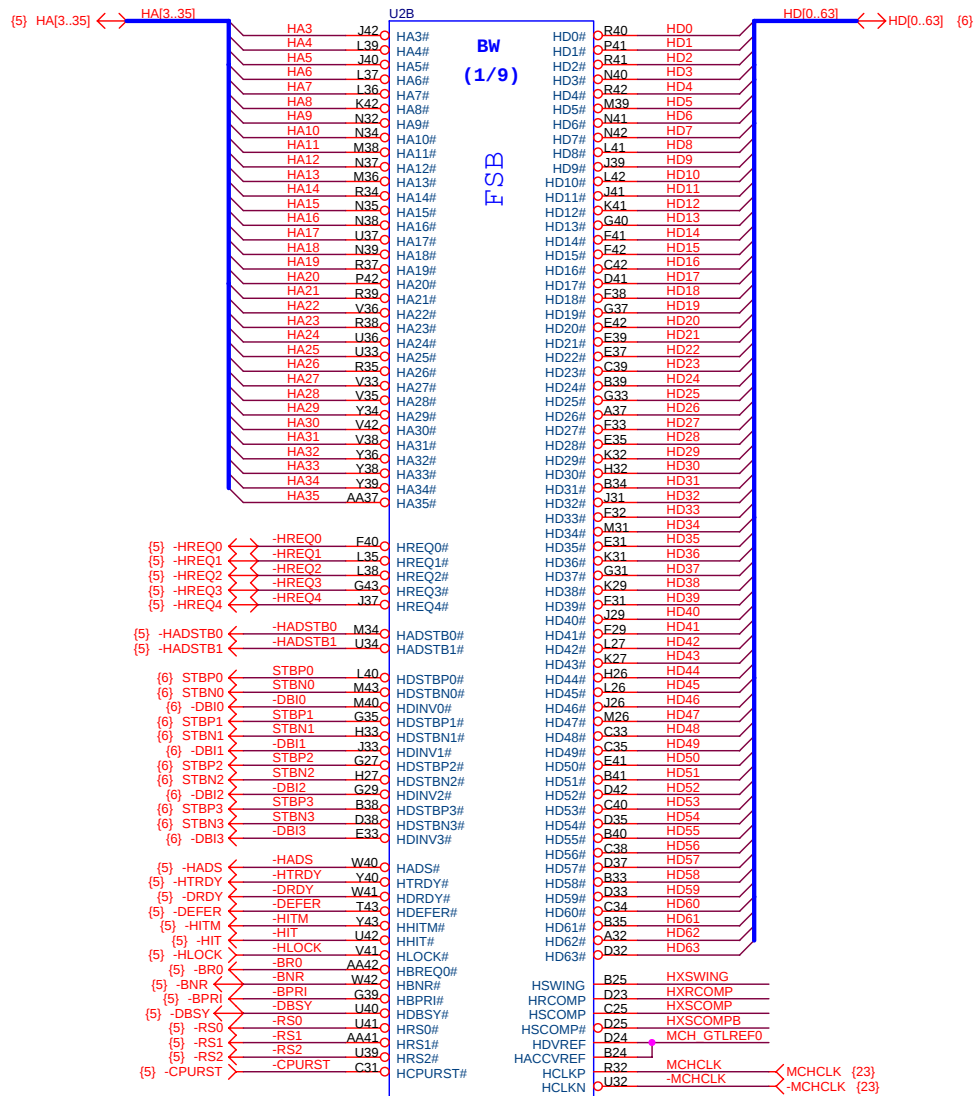


	3 pin FAN control	4 pin FAN control	FAN speed	Controller
CPU FAN	FANPWM1	FANPWM3	FANIO1	IT8718
	ICH_FAN_PWM2	ICH_FAN_PWM0	ICH_FAN_TACH0	ICH8
SYS FAN	FANPWM2	N/A	FANIO2	IT8718
	ICH_FAN_PWM1	N/A	ICH_FAN_TACH1	ICH8
PWR FAN	N/A	N/A	FANIO3	IT8718
			ICH_FAN_TACH2	ICH8

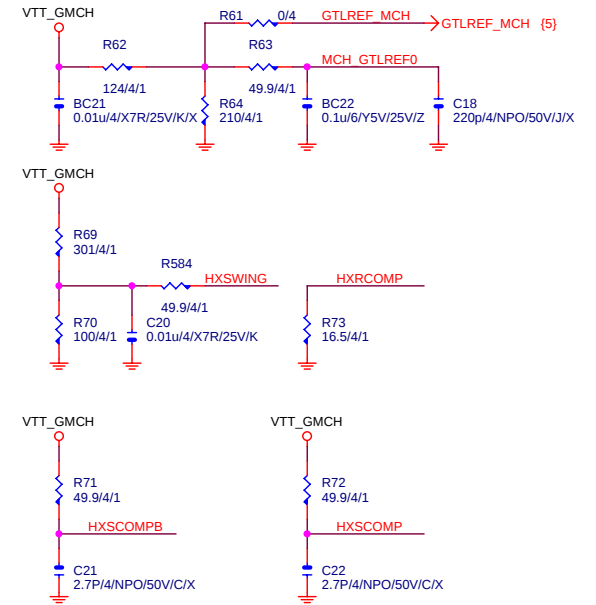








P965-C1/QM62[10HB1-030082-30R]
CPU INTERFACE



Gigabyte Technology

Title		GMCH-HOST	
Size	Document Number	965P-DQ6	Rev
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U2C

MAAA0 BA31 SMA_A0
 MAAA1 BB25 SMA_A1
 MAAA2 BA26 SMA_A2
 MAAA3 BA25 SMA_A3
 MAAA4 AY25 SMA_A4
 MAAA5 BA23 SMA_A5
 MAAA6 AY24 SMA_A6
 MAAA7 AY23 SMA_A7
 MAAA8 BB23 SMA_A8
 MAAA9 BA22 SMA_A9
 MAAA10 AY33 SMA_A10
 MAAA11 BB22 SMA_A11
 MAAA12 AW21 SMA_A12
 MAAA13 AY38 SMA_A13
 MAAA14 BA21 SMA_A14

BW
(3/9)

SDQS_A0 AU4 DQSA0
 SDQS_A0# AU3 -DQSA0
 SDM_A0 AR2 DMA0
 SDQ_A1 AR5 MDA0
 SDQ_A1 AR4 MDA1
 SDQ_A1 AR2 MDA2
 SDQ_A1 AR3 MDA3
 SDQ_A1 AR2 MDA4
 SDQ_A1 AU1 MDA6
 SDQ_A1 AV4 MDA7

SDQS_A1 BB3 DQSA1
 SDQS_A1# BA4 DMA1
 SDM_A1

(15.17) -SWEA ← -SWEA BB34 SWE_A#
 (15.17) -SCASA ← -SCASA AY25 SCAS_A#
 (15.17) -SRASA ← -SRASA BB33 SRAS_A#
 (15.17) SBA0 ← SBA0 BA33 SBS_A0
 (15.17) SBA1 ← SBA1 AW32 SBS_A1
 (15.17) SBA2 ← SBA2 BB21 SBS_A2
 (15.17) CSA0 ← CSA0 AW35 SCS_A0#
 (15.17) CSA1 ← CSA1 BA35 SCS_A1#
 (15.17) CSA2 ← CSA2 BA34 SCS_A2#
 (15.17) CSA3 ← CSA3 BB38 SCS_A3#
 (15.17) CKEA0 ← CKEA0 BC20 SCKE_A0
 (15.17) CKEA1 ← CKEA1 AY20 SCKE_A1
 (15.17) CKEA2 ← CKEA2 AY21 SCKE_A2
 (15.17) CKEA3 ← CKEA3 BA19 SCKE_A3

MODT_A0 AY37
 MODT_A1 BA38
 MODT_A2 BB35
 MODT_A3 BA39

(15) DCLKA0 ← DCLKA0 AU31 SCLK_A0
 (15) DCLKA0 ← DCLKA0 AR31 SCLK_A0#
 (15) DCLKA1 ← DCLKA1 AF27 SCLK_A1#
 (15) DCLKA1 ← DCLKA1 AN27 SCLK_A1#
 (15) DCLKA2 ← DCLKA2 AV33 SCLK_A2
 (15) DCLKA2 ← DCLKA2 AR33 SCLK_A2#
 (15) DCLKA3 ← DCLKA3 AF29 SCLK_A3
 (15) DCLKA4 ← DCLKA4 AF31 SCLK_A4
 (15) DCLKA4 ← DCLKA4 AN27 SCLK_A4#
 (15) DCLKA5 ← DCLKA5 AT33 SCLK_A5
 (15) DCLKA5 ← DCLKA5 AU33 SCLK_A5#

DDR_0

TP43 → AN21

P965-C1/QM62[10HB1-030082-30R]

DDR INTERFACE

U2D

MAAB0 BB17 SMA_B0
 MAAB1 AY17 SMA_B1
 MAAB2 BA17 SMA_B2
 MAAB3 BC16 SMA_B3
 MAAB4 AW15 SMA_B4
 MAAB5 BA15 SMA_B5
 MAAB6 BB15 SMA_B6
 MAAB7 BA14 SMA_B7
 MAAB8 AY15 SMA_B8
 MAAB9 BB14 SMA_B9
 MAAB10 AW18 SMA_B10
 MAAB11 BB13 SMA_B11
 MAAB12 AY28 SMA_B12
 MAAB13 AY28 SMA_B13
 MAAB14 AY13 SMA_B14

BW
(4/9)

SDQS_B0 AV6 DQSB0
 SDQS_B0# AU5 -DQSB0
 SDM_B0 AR7 DMB0
 SDQ_B1 AN7 MDB0
 SDQ_B1 AN6 MDB1
 SDQ_B1 AV5 MDB2
 SDQ_B1 AW7 MDB3
 SDQ_B1 AN6 MDB5
 SDQ_B1 AN9 MDB6
 SDQ_B1 AU7 MDB7

SDQS_B1 AR12 DQSB1
 SDQS_B1# AR12 DQSB1
 SDM_B1 AW2 DMB1

(16.17) -SWEB ← -SWEB BA27C SWE_B#
 (16.17) -SCASB ← -SCASB AW28C SCAS_B#
 (16.17) -SRASB ← -SRASB AW28C SRAS_B#
 (16.17) SBA0 ← SBA0 AY19 SBS_B0
 (16.17) SBA1 ← SBA1 BA18 SBS_B1
 (16.17) SBA2 ← SBA2 BC12 SBS_B2
 (16.17) CSB0 ← CSB0 BB27C SCS_B0#
 (16.17) CSB1 ← CSB1 BB30C SCS_B1#
 (16.17) CSB2 ← CSB2 AY27C SCS_B2#
 (16.17) CSB3 ← CSB3 AY31C SCS_B3#
 (16.17) CKEB0 ← CKEB0 AY12 SCKE_B0
 (16.17) CKEB1 ← CKEB1 AW12 SCKE_B1
 (16.17) CKEB2 ← CKEB2 BB11 SCKE_B2
 (16.17) CKEB3 ← CKEB3 BA11 SCKE_B3
 (16.17) MODT_B0 BA28 SODT_B0
 (16.17) MODT_B1 BA30 SODT_B1
 (16.17) MODT_B2 BB29 SODT_B2
 (16.17) MODT_B3 BB31 SODT_B3

(16) DCLKB0 ← DCLKB0 AY31 SCLK_B0
 (16) DCLKB0 ← DCLKB0 AW31C SCLK_B0#
 (16) DCLKB1 ← DCLKB1 AU27 SCLK_B1
 (16) DCLKB1 ← DCLKB1 AT27C SCLK_B1#
 (16) DCLKB2 ← DCLKB2 AY32 SCLK_B2
 (16) DCLKB2 ← DCLKB2 AT32C SCLK_B2#
 (16) DCLKB3 ← DCLKB3 AR29C SCLK_B3#
 (16) DCLKB4 ← DCLKB4 AY29 SCLK_B4
 (16) DCLKB5 ← DCLKB5 AN33 SCLK_B5
 (16) DCLKB5 ← DCLKB5 AP32C SCLK_B5#

(16) DCLKB0 ← DCLKB0 AY31 SCLK_B0
 (16) DCLKB0 ← DCLKB0 AW31C SCLK_B0#
 (16) DCLKB1 ← DCLKB1 AU27 SCLK_B1
 (16) DCLKB1 ← DCLKB1 AT27C SCLK_B1#
 (16) DCLKB2 ← DCLKB2 AY32 SCLK_B2
 (16) DCLKB2 ← DCLKB2 AT32C SCLK_B2#
 (16) DCLKB3 ← DCLKB3 AR29C SCLK_B3#
 (16) DCLKB4 ← DCLKB4 AY29 SCLK_B4
 (16) DCLKB5 ← DCLKB5 AN33 SCLK_B5
 (16) DCLKB5 ← DCLKB5 AP32C SCLK_B5#

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TP16 → AP21
 TP17 → AA39

DDR_1

TP2 → AM21

MCH_VREF → AM6

SVREF

RESERVED_7

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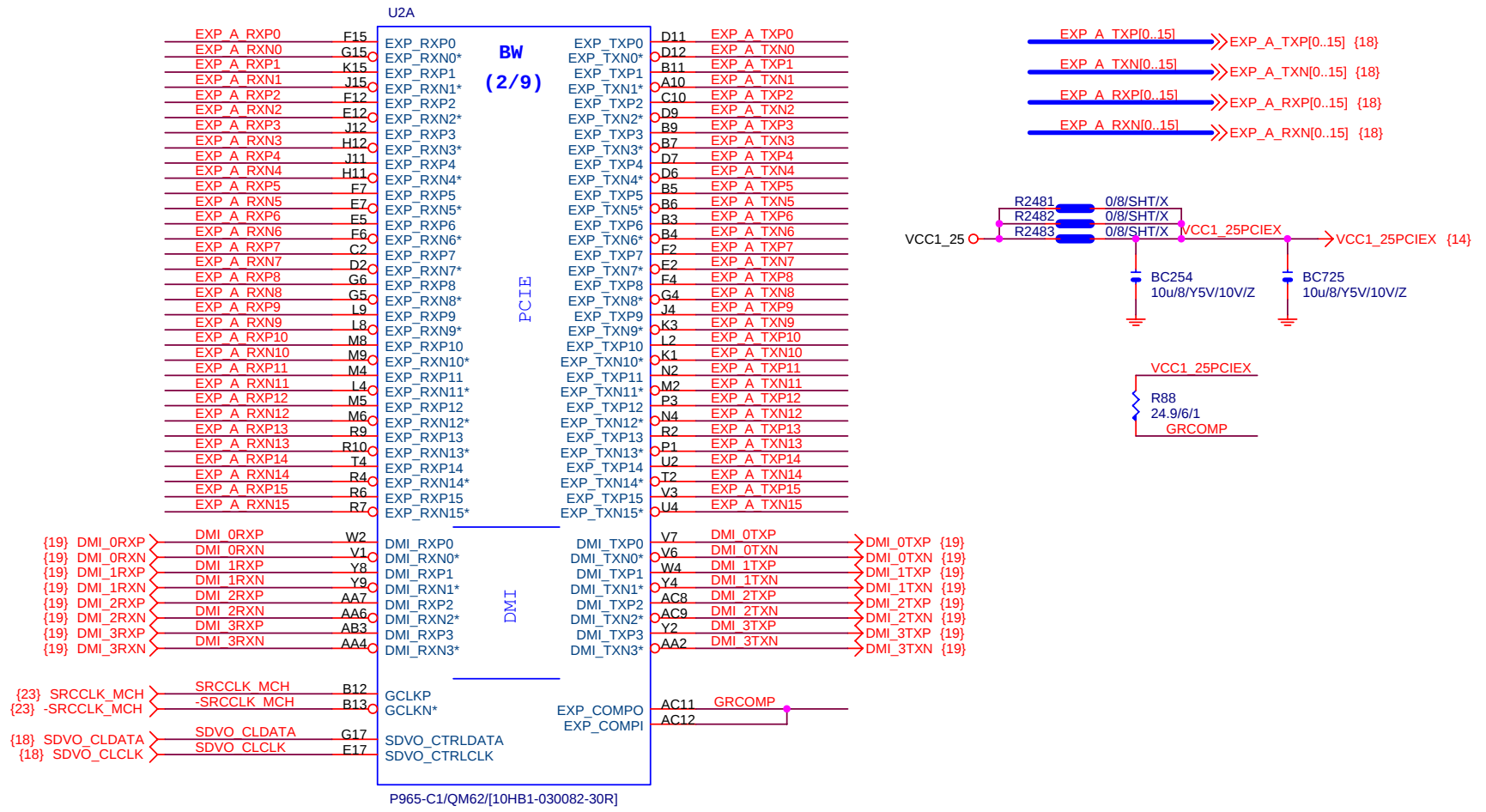
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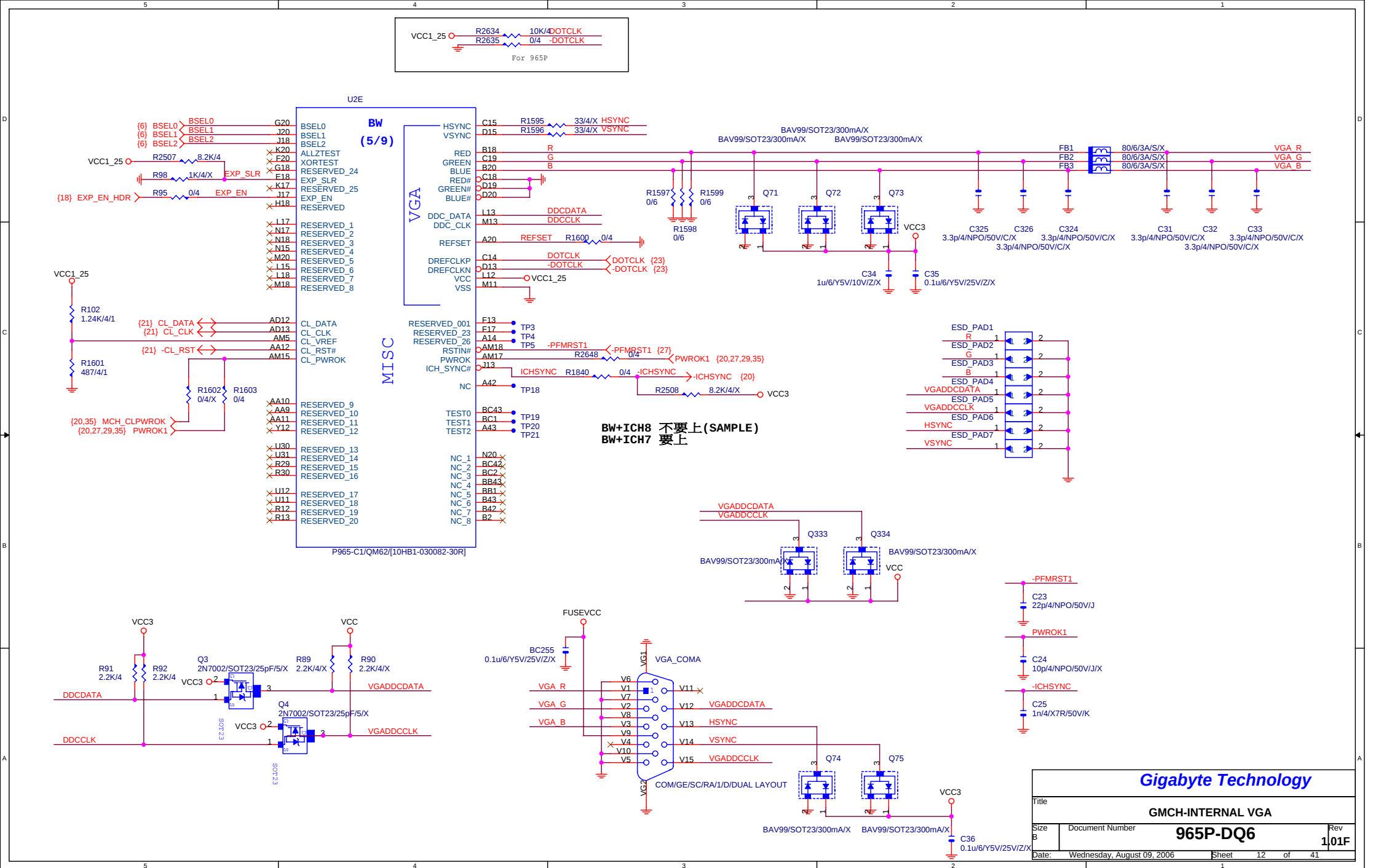
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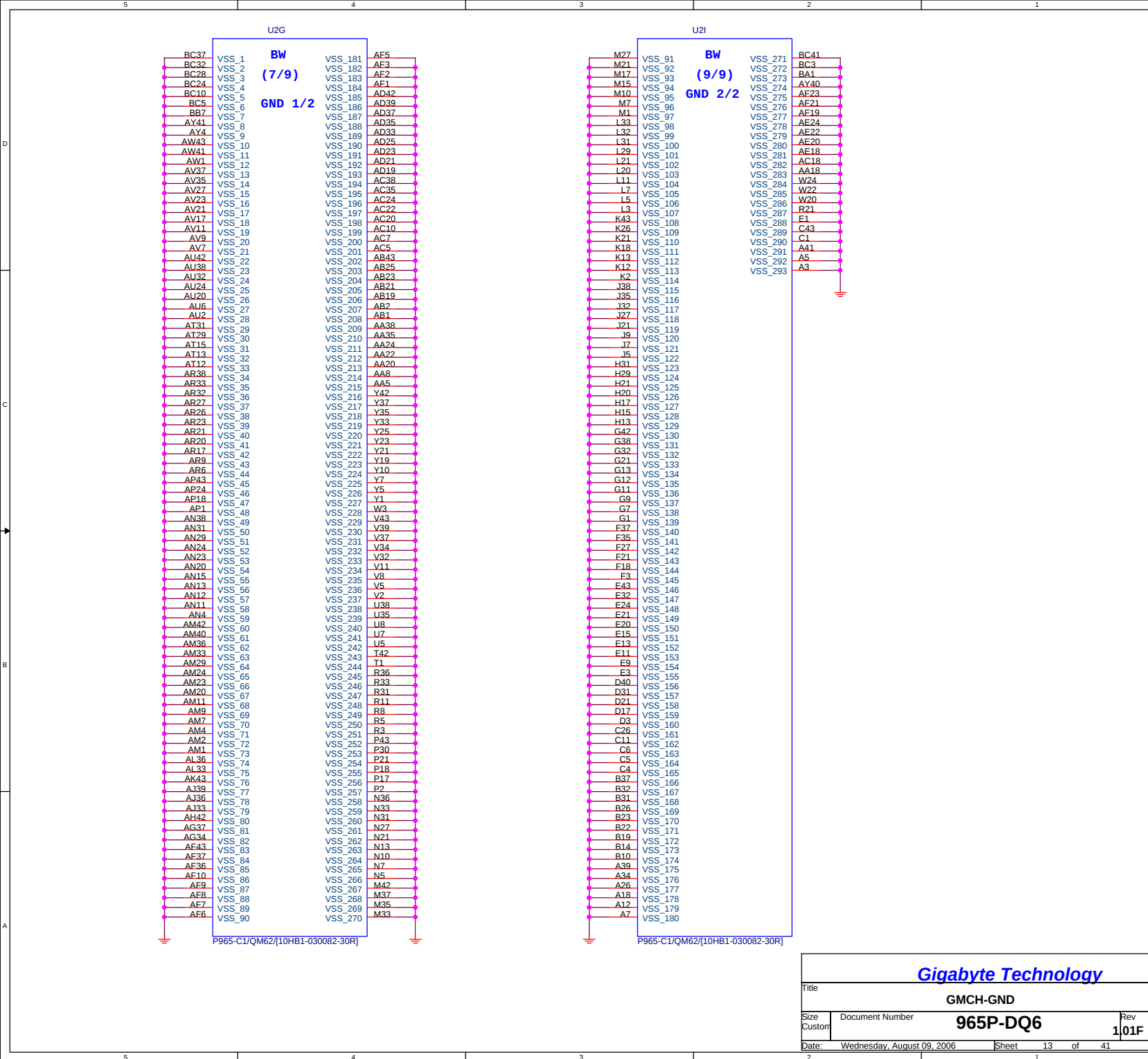
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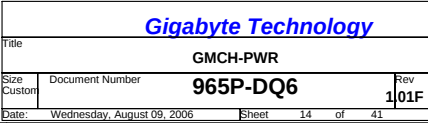
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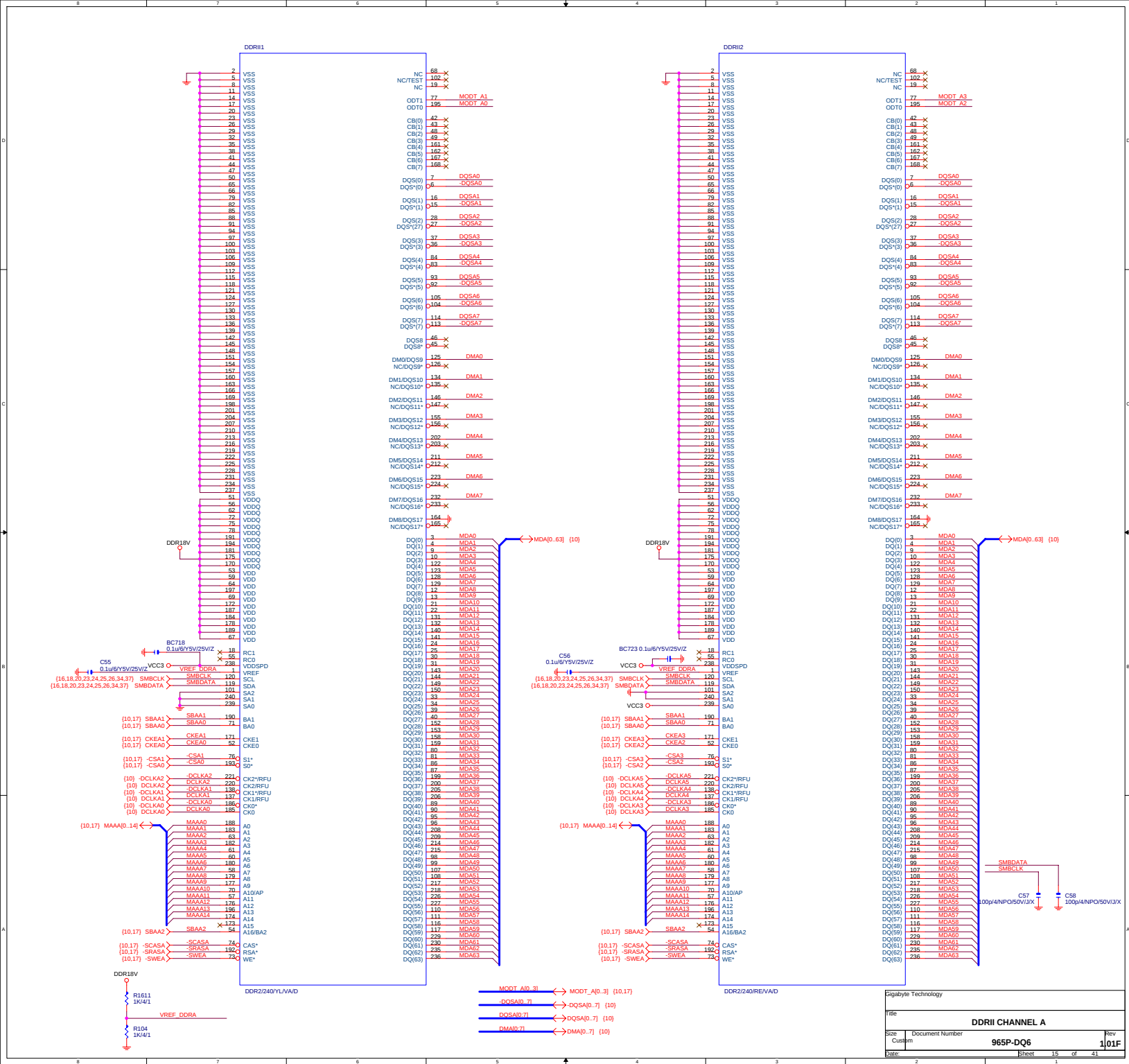
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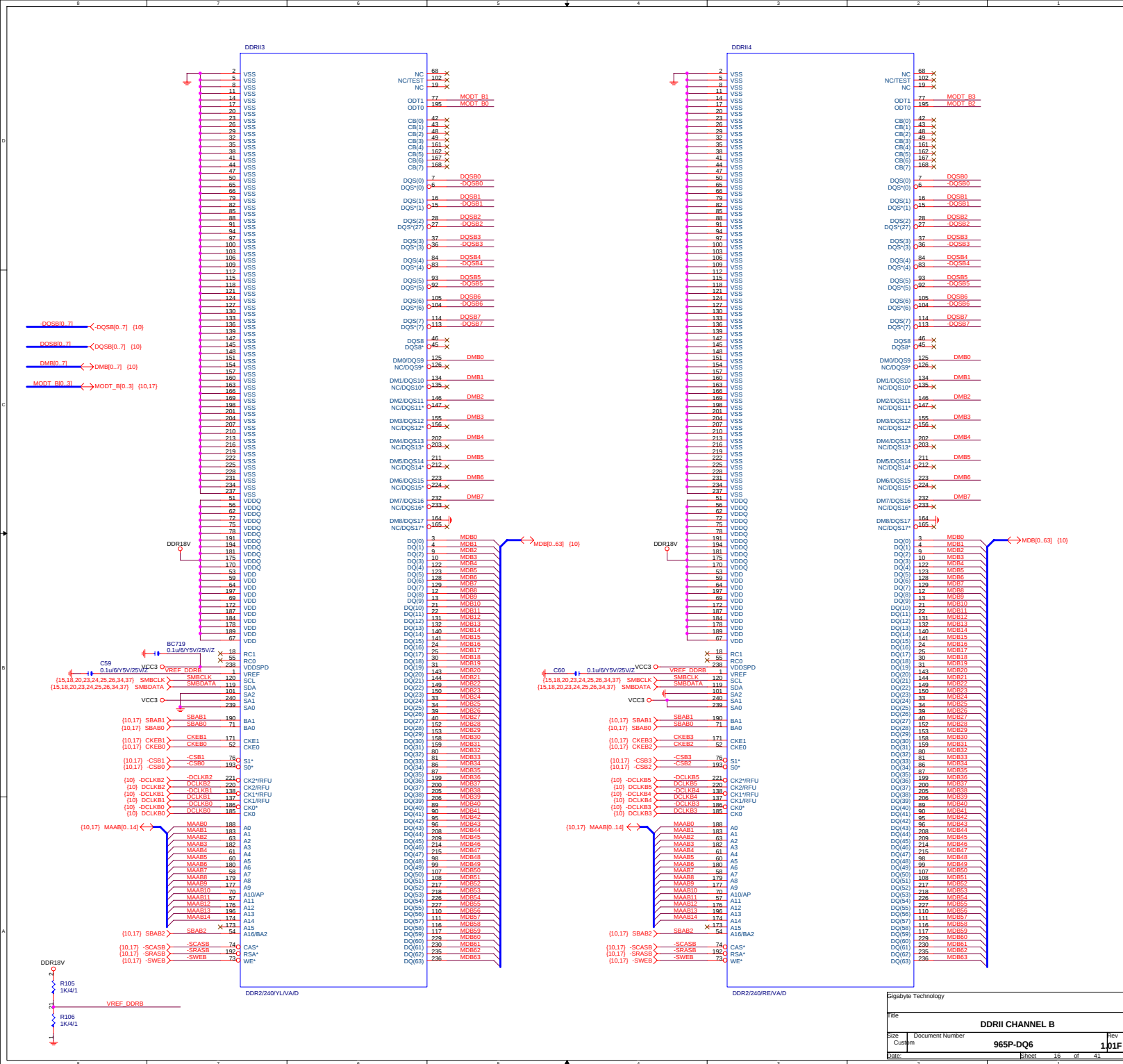
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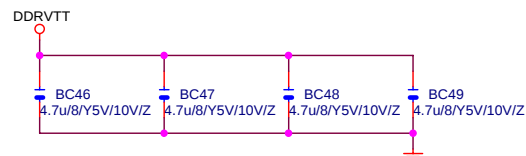
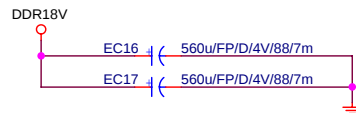
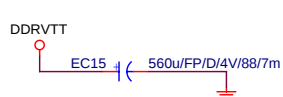






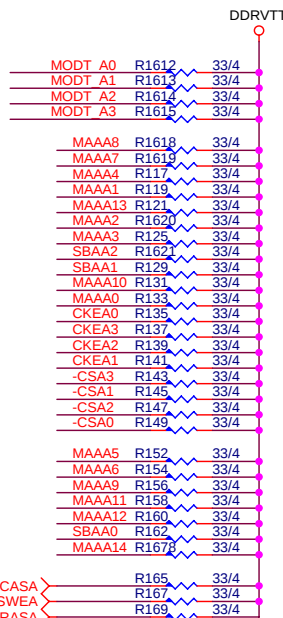
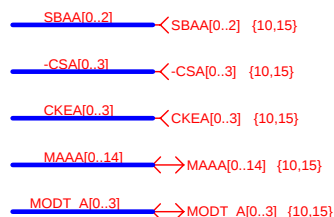
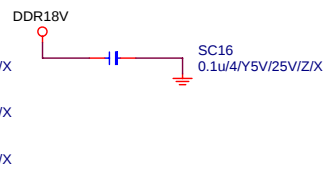
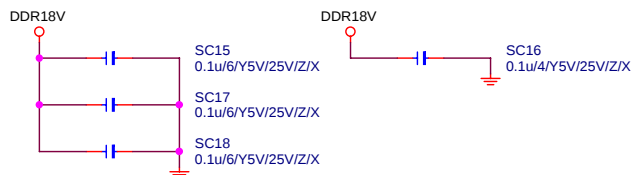
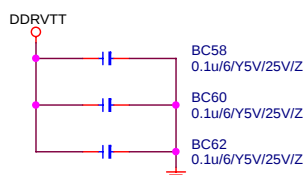
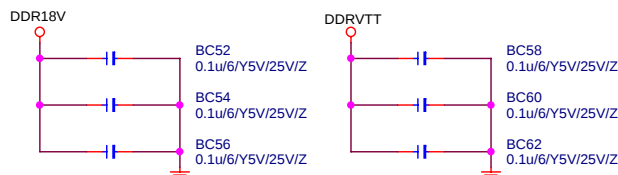
DDR TERMINATION CHANNEL A

DDRVTT Decouple



DDR18V Decouple

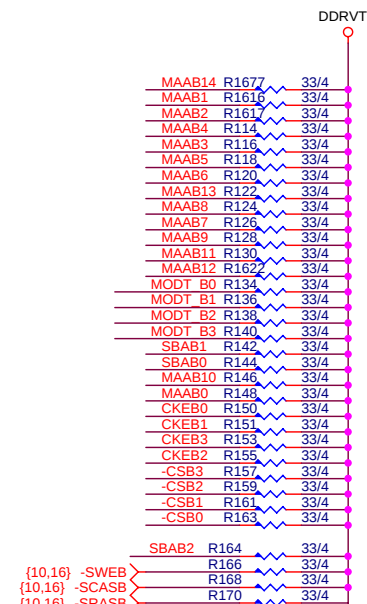
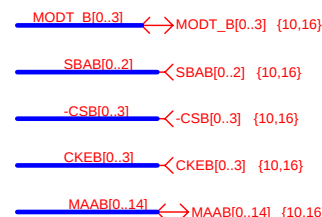
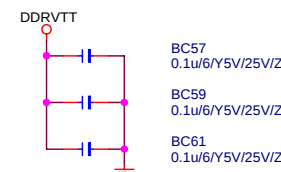
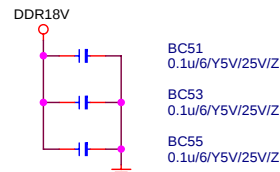
DDRVTT Decouple



DDR TERMINATION CHANNEL B

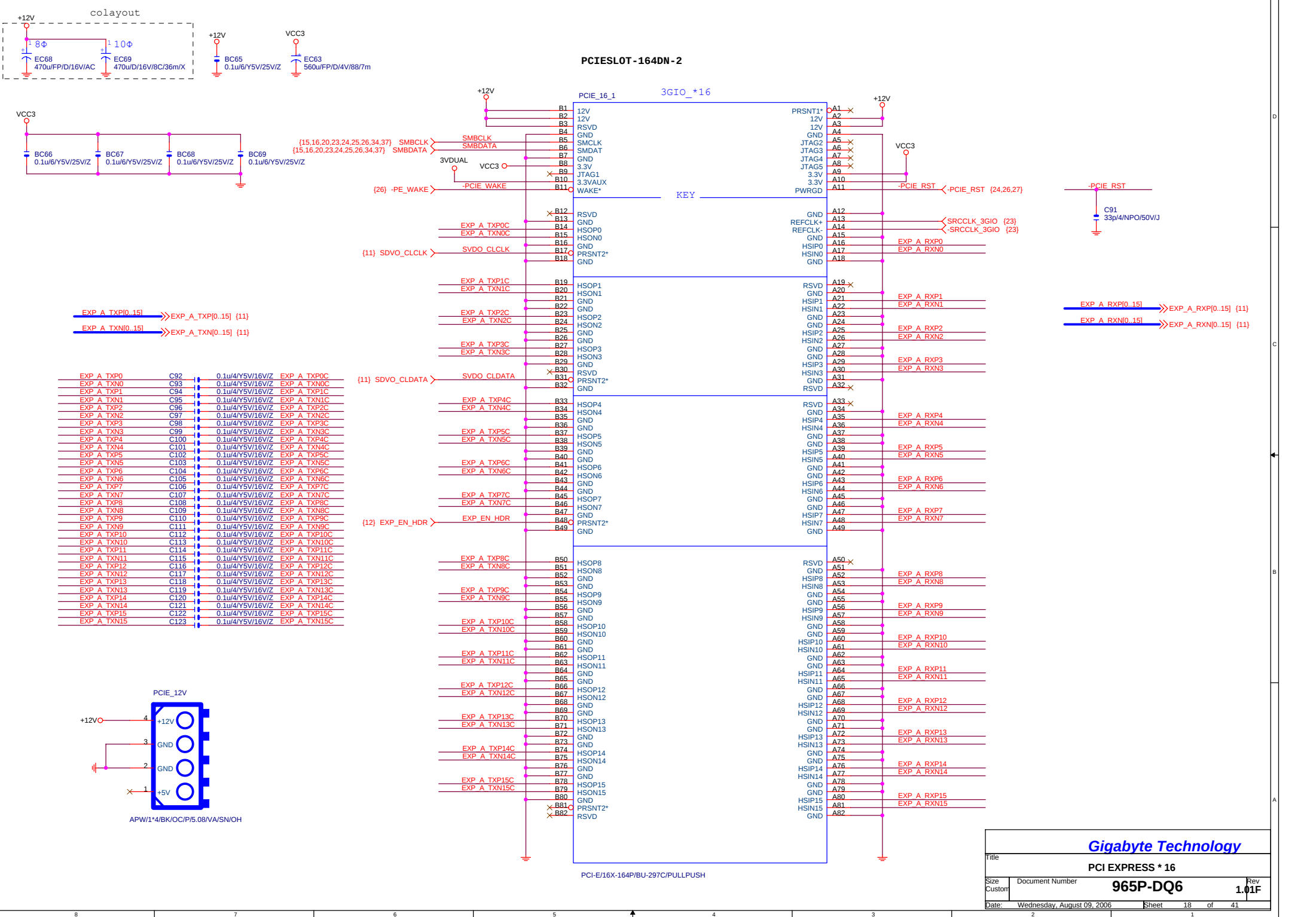
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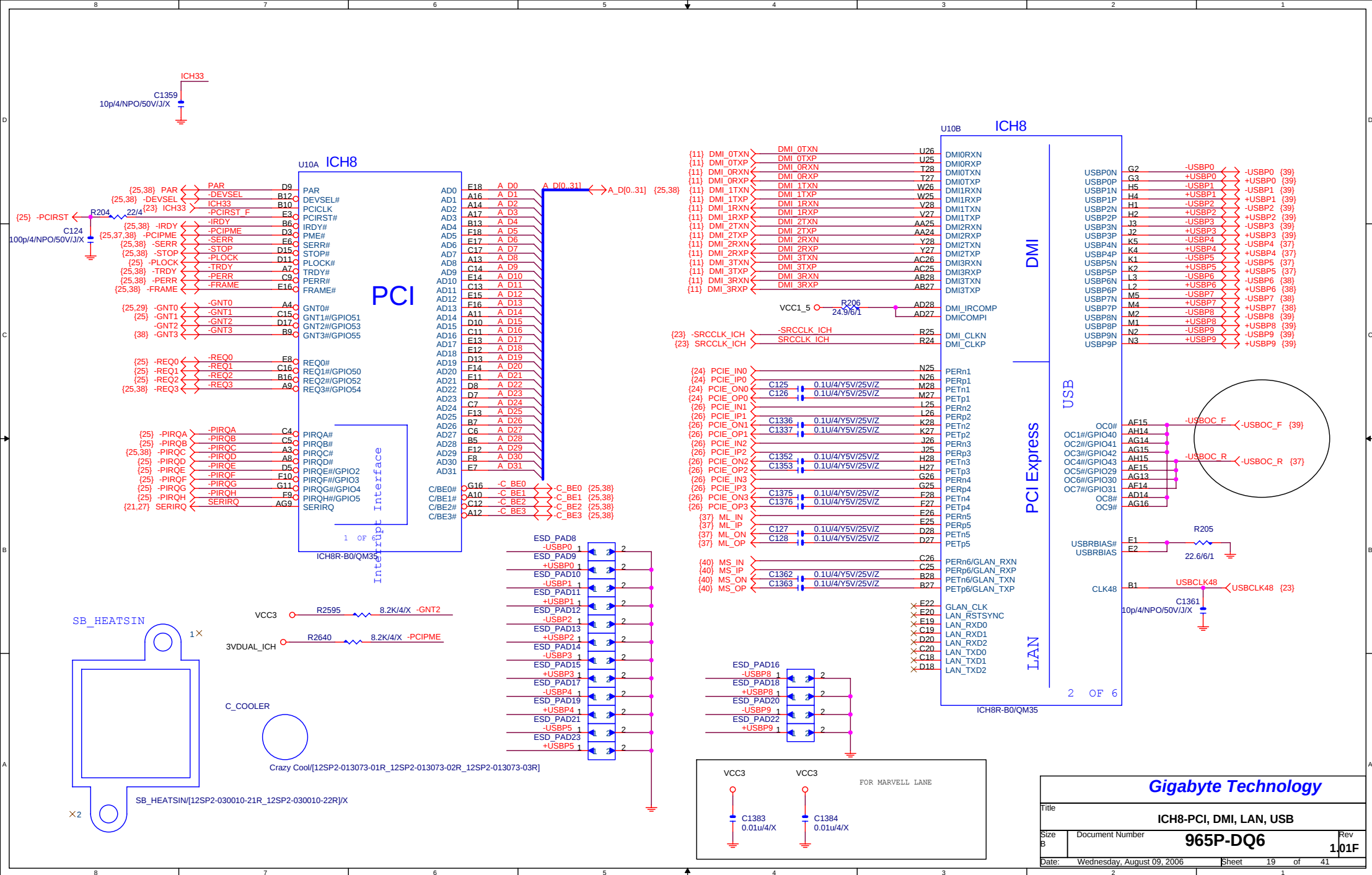
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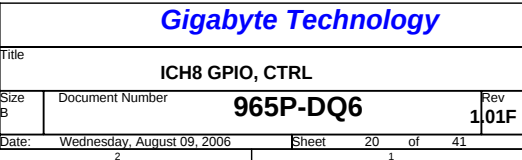


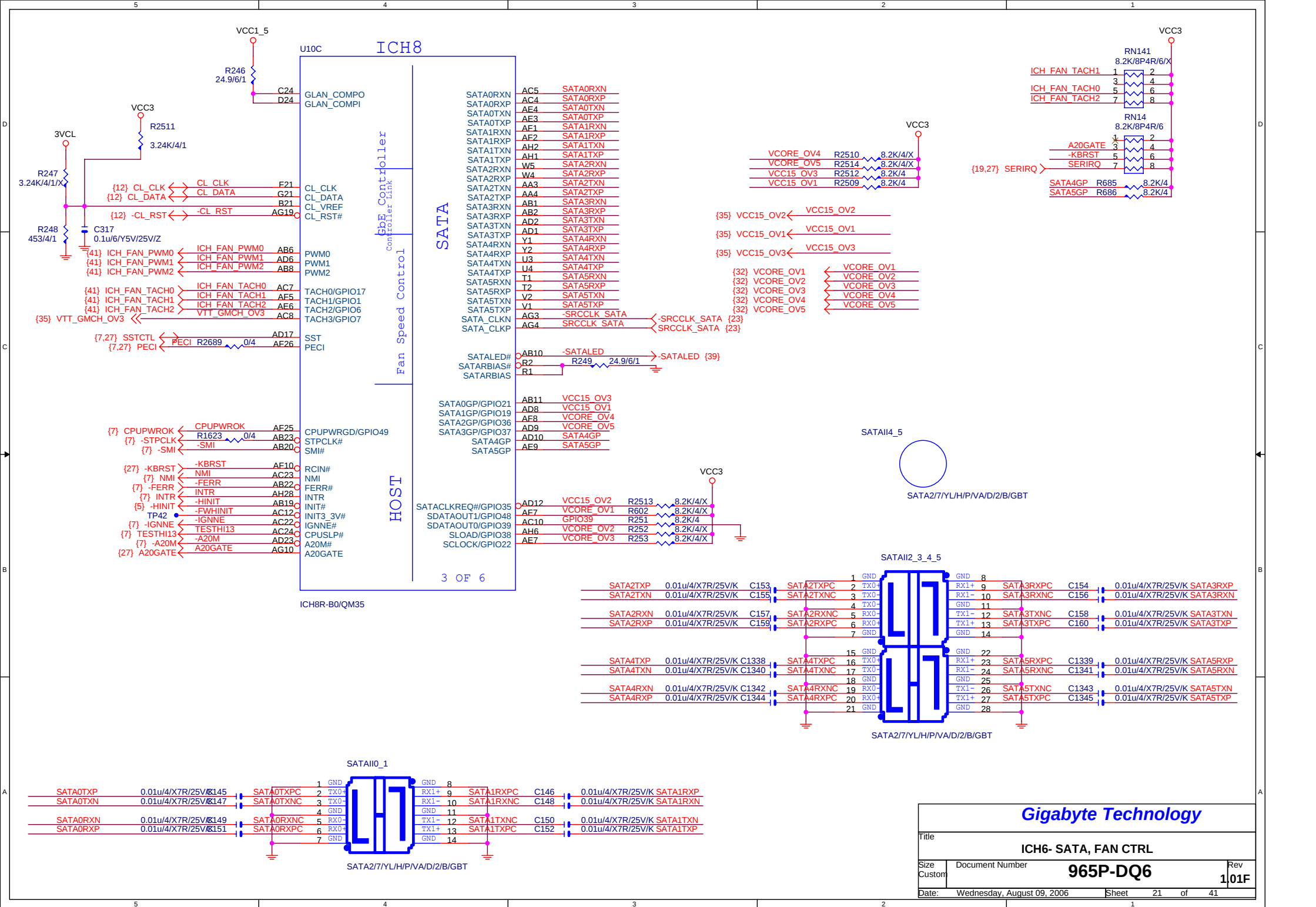
Gigabyte Technology

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Custom					101F
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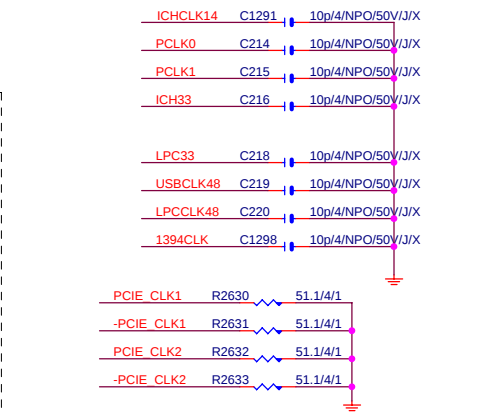
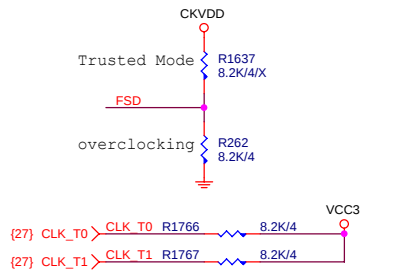
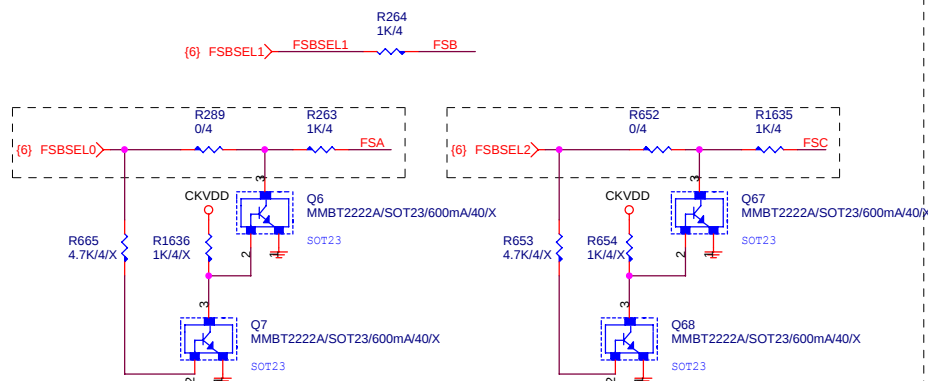
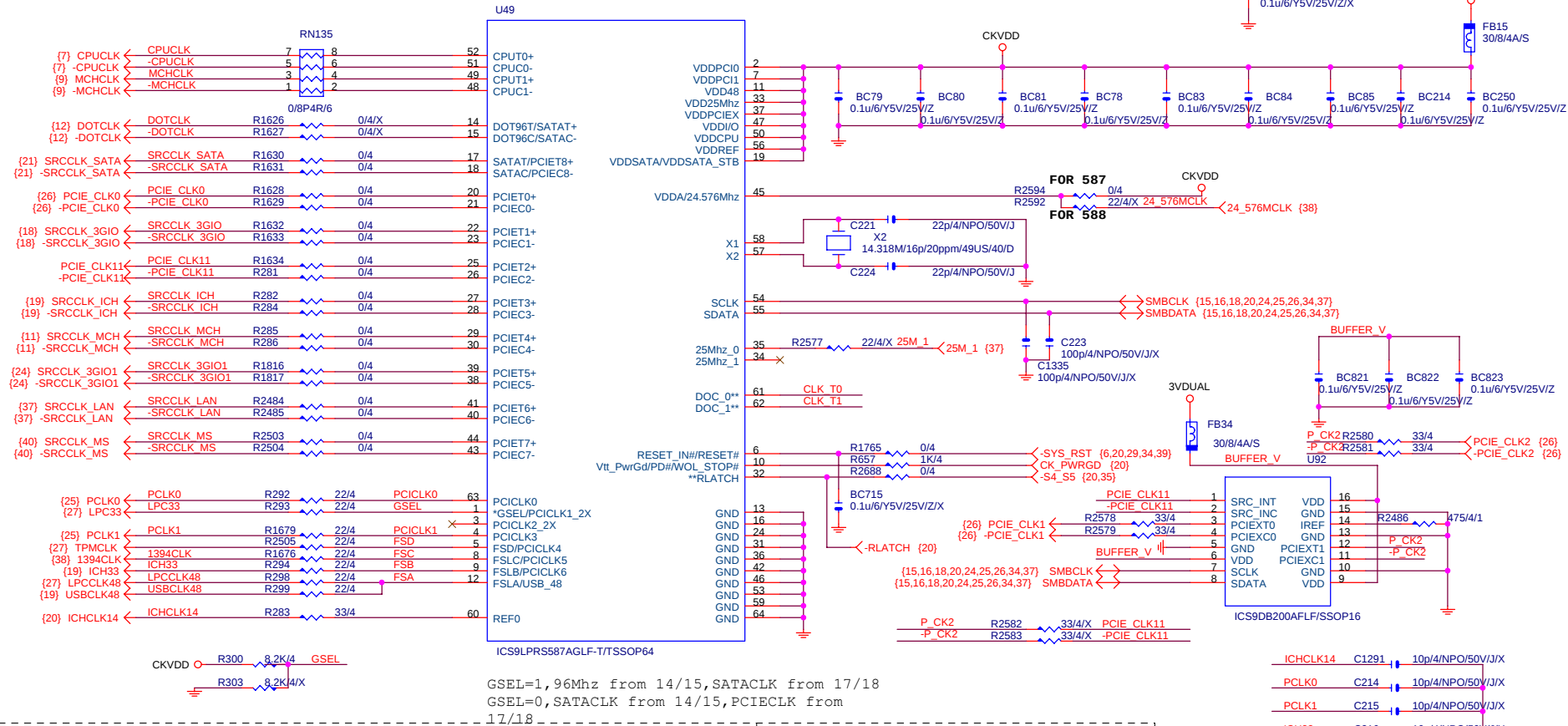


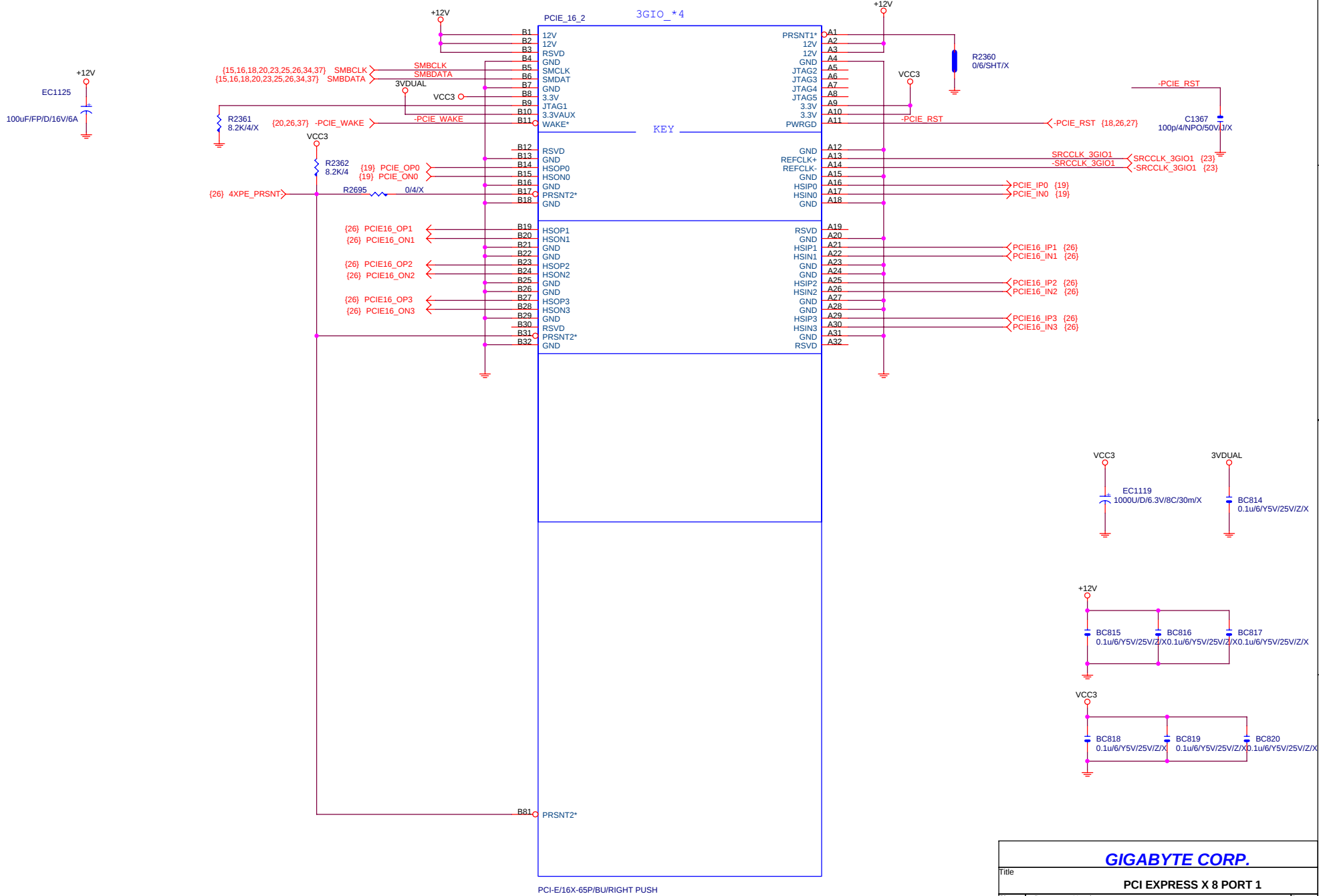




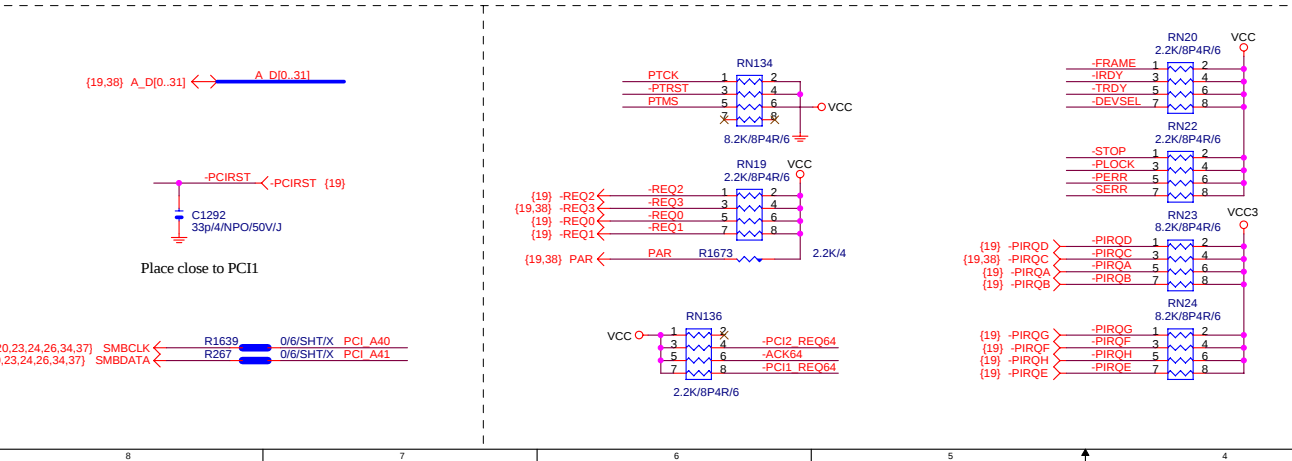
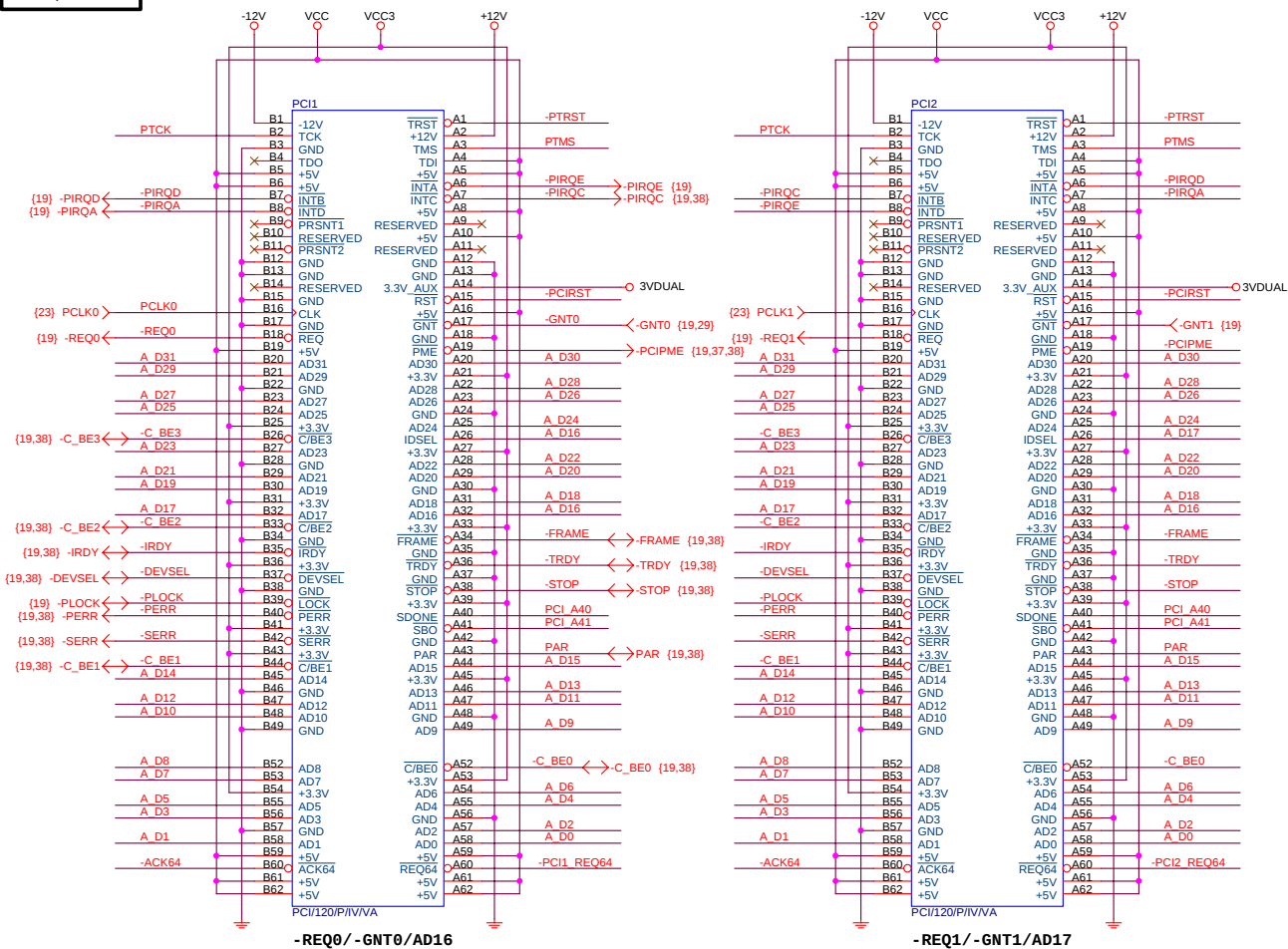


CLK GEN CK505

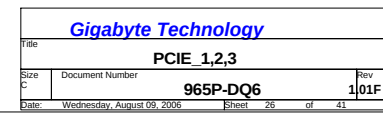


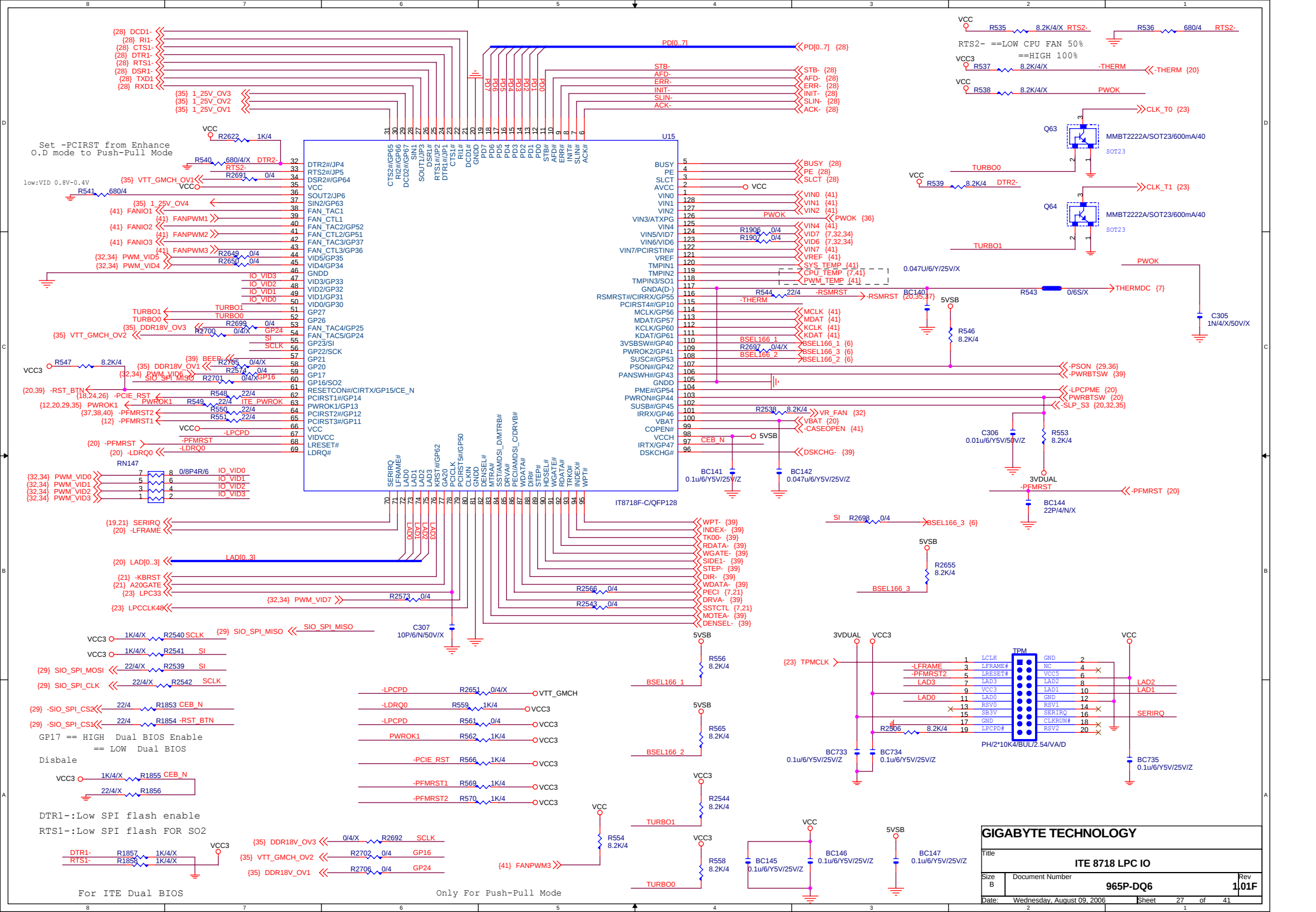


PCI1, 2 SLOT

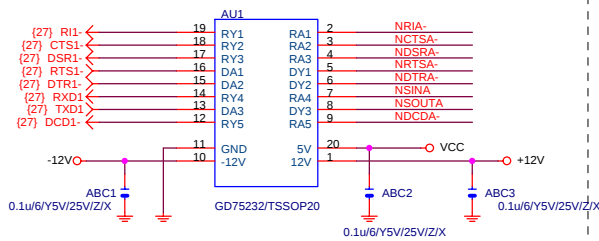


For Vih level consideration

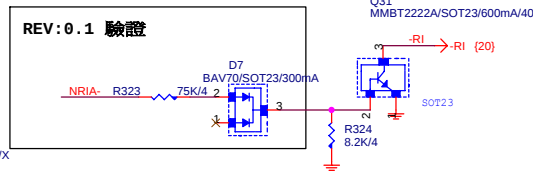




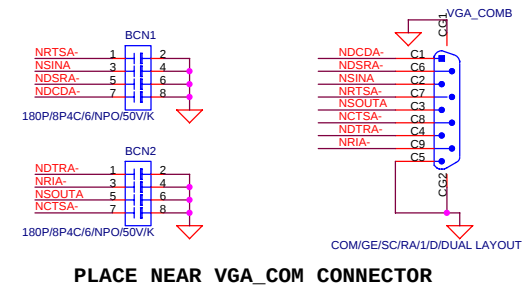
COMA



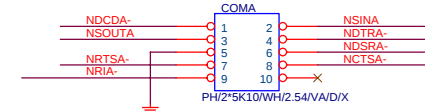
COM RI



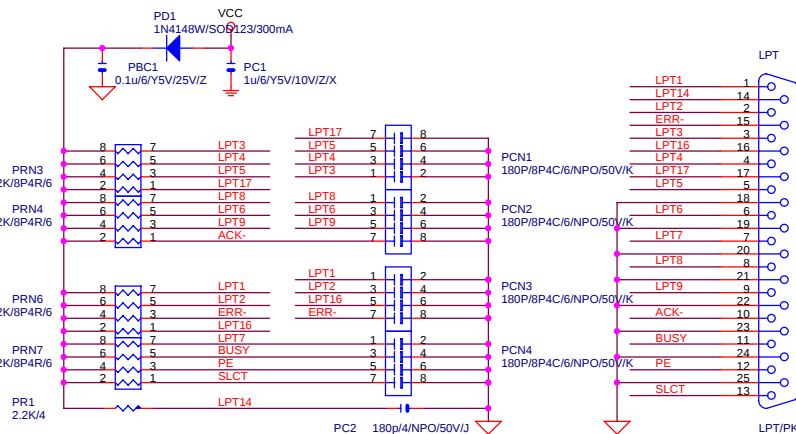
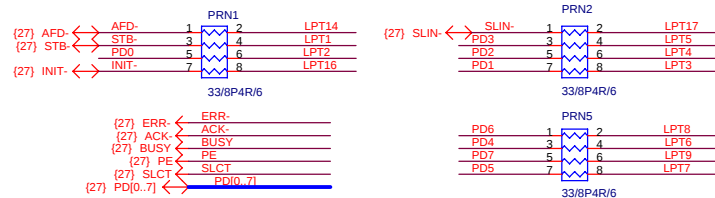
EXTERNAL COMB



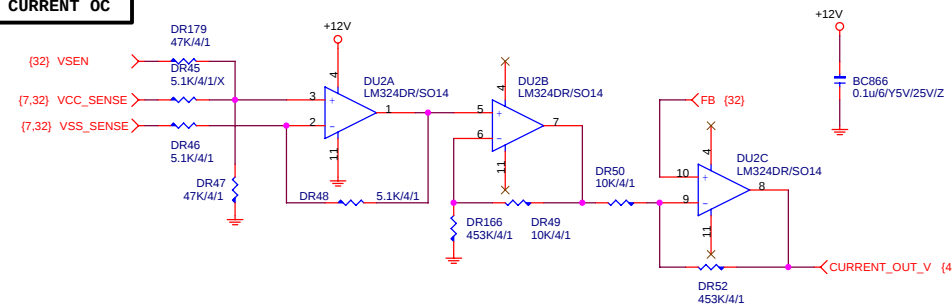
PLACE NEAR VGA_COM CONNECTOR



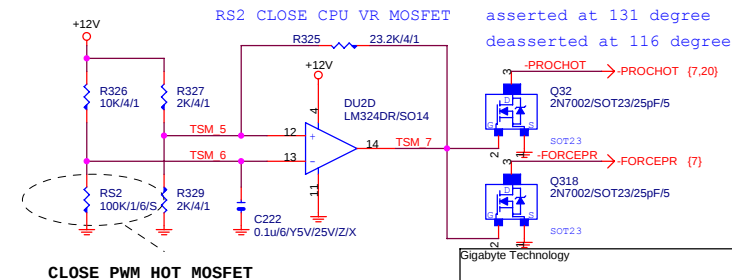
LPT PORT



DYNAMIC CURRENT OC

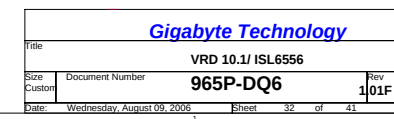


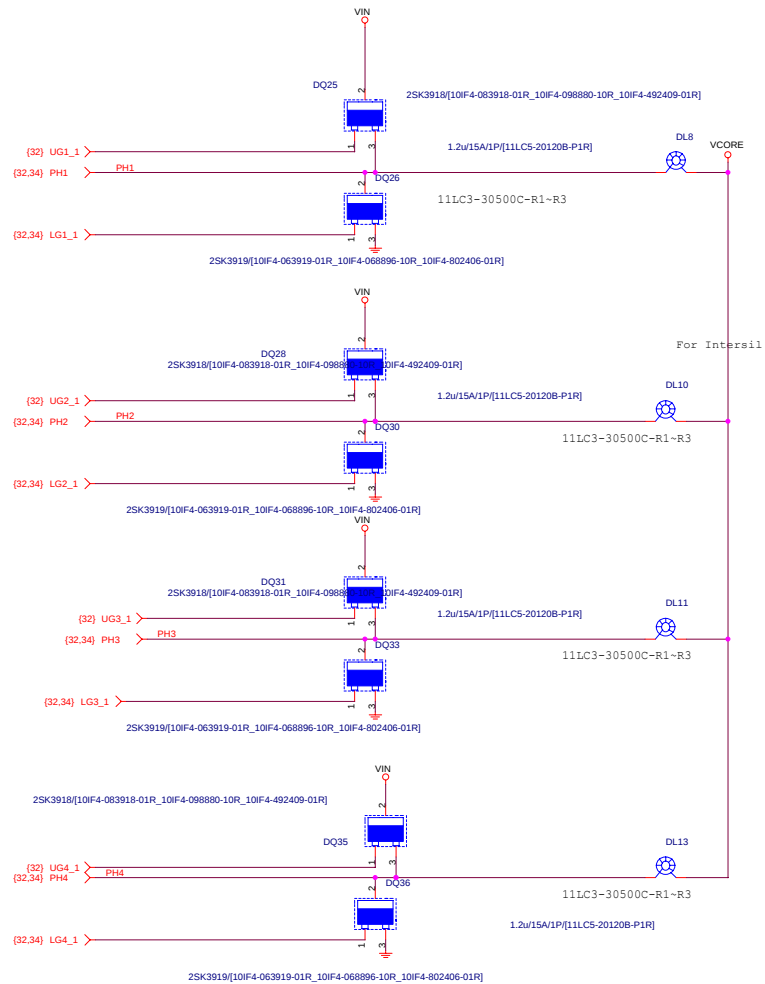
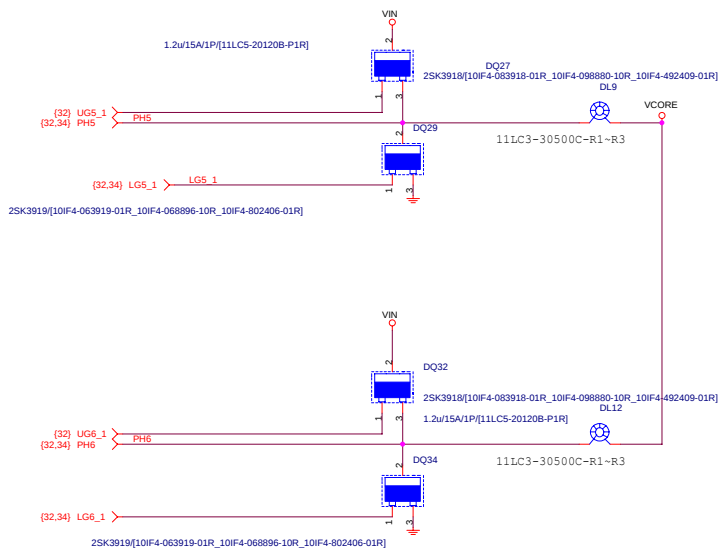
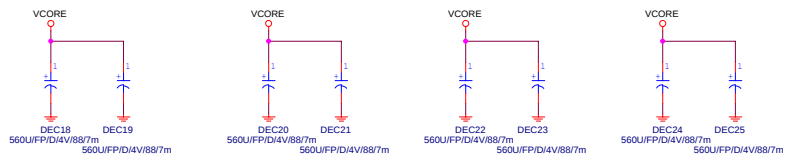
-PROHOT

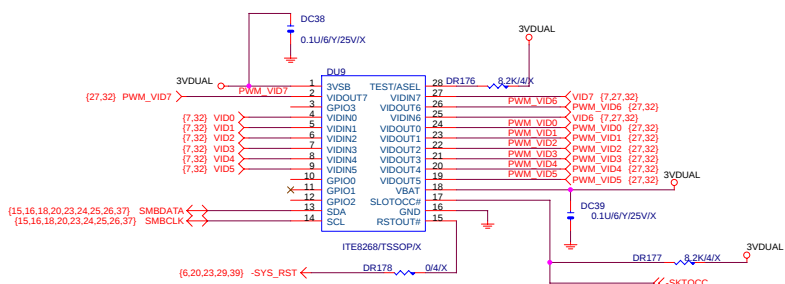
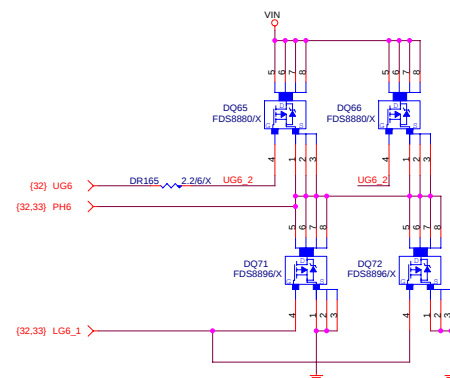
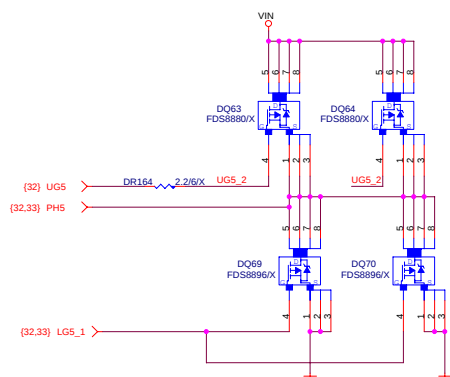
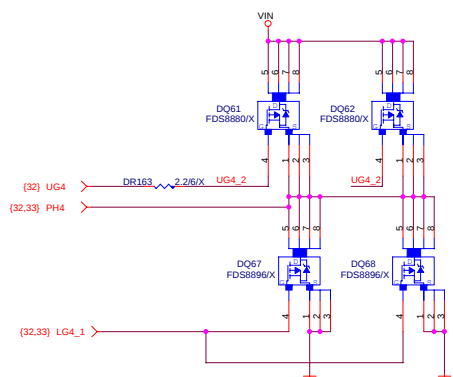
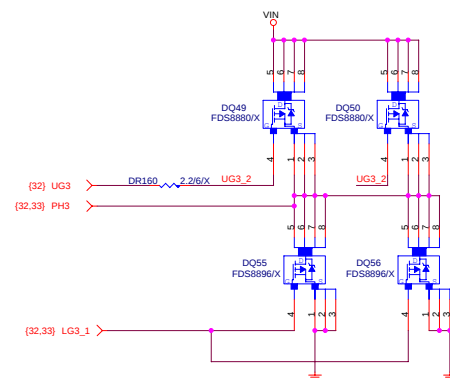
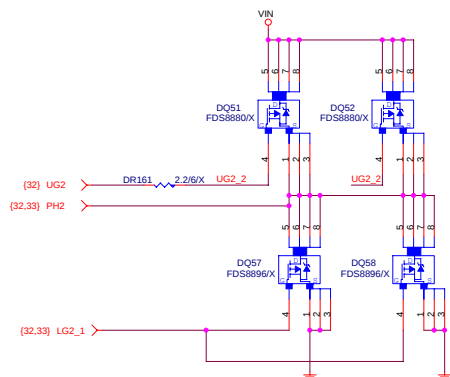
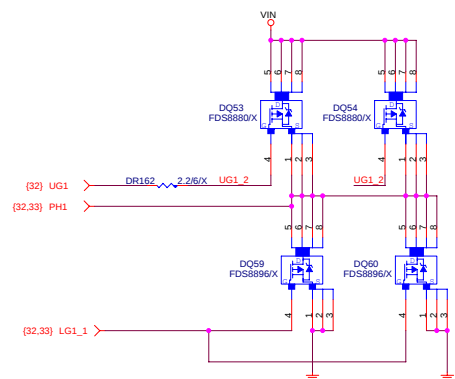


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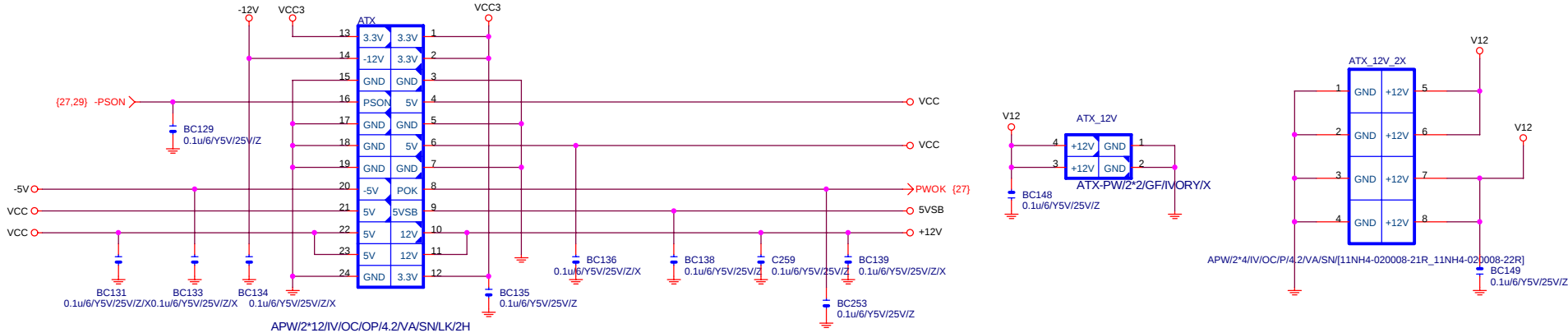
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Size	Document Number	Rev	
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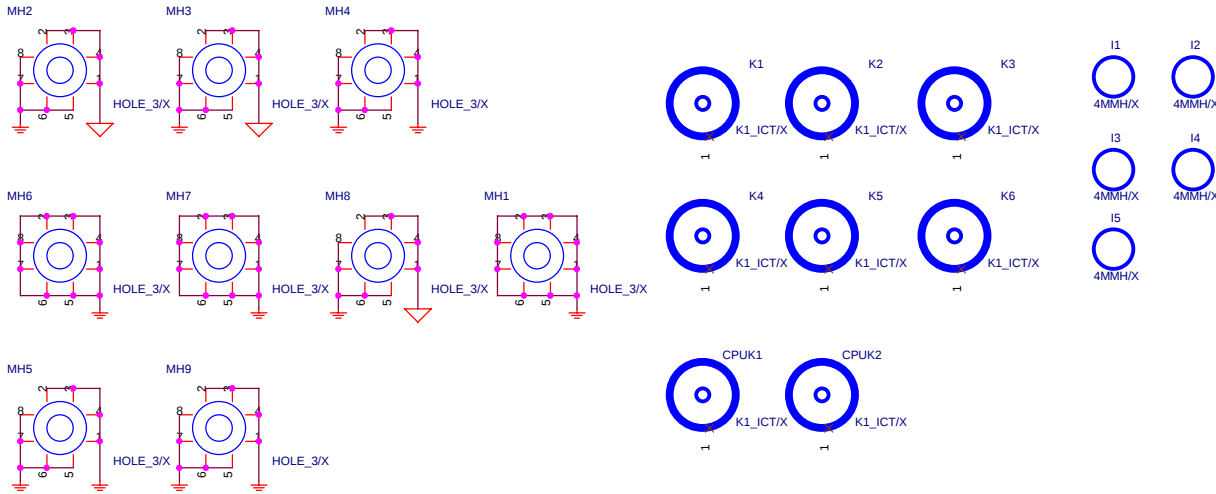




ATX POWER CONNECTOR



HOLE_3-2--->有鉛



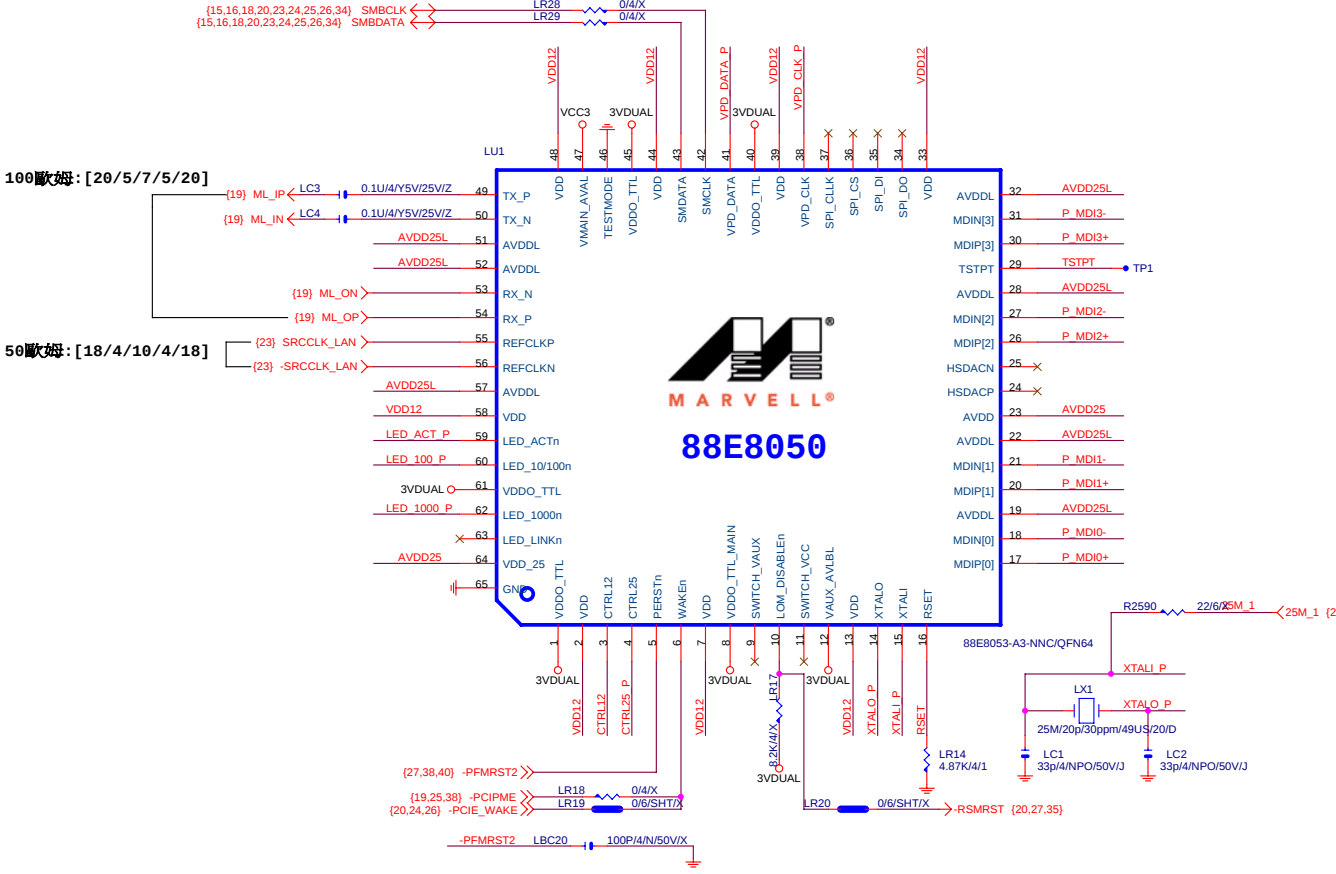
PCIE-16 LAN

Layout Check 注意事項

1. LU1 PIN65 需下內層GND,打12 VIA
2. 3VDUAL, VCC3, VDD15 L, AVDD25 L 至少走20mil寬,並且電容擺設每兩pin至少放一顆Bypass Cap.
3. X'TAL 25MHz 兩訊號線,TRACE 愈短愈好,線寬12mil
4. MDI正負0~3,TRACE 8:7:8, 每對之間保持 40mil

100歐母: [20/5/7/5/20]

50歐母: [18/4/10/4/18]



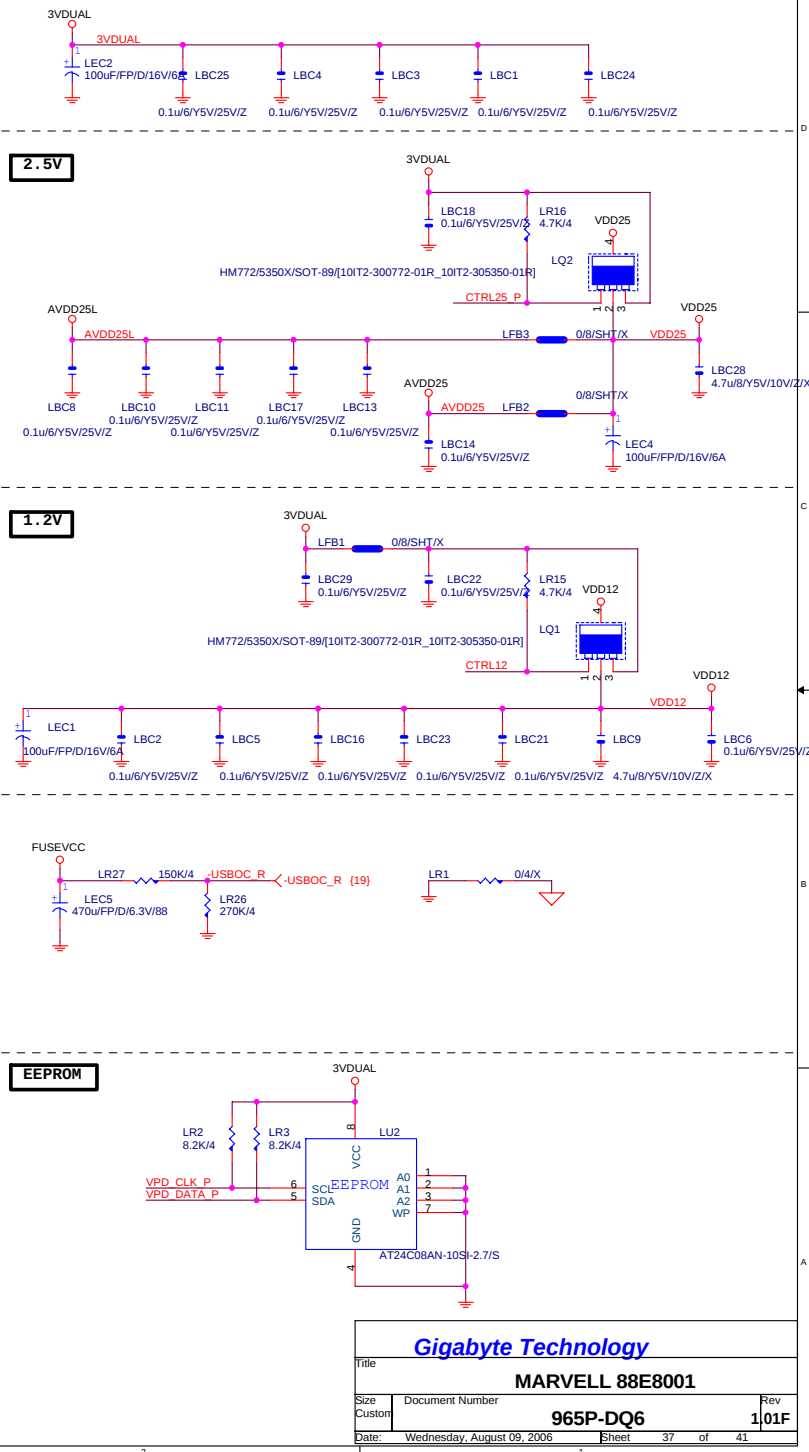
3VDUAL

2.5V

1.2V

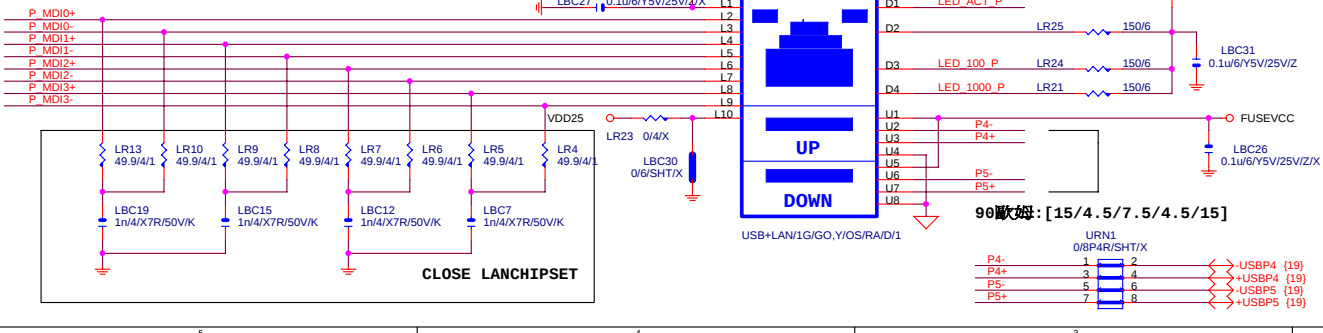
FUSEVCC

EEPROM

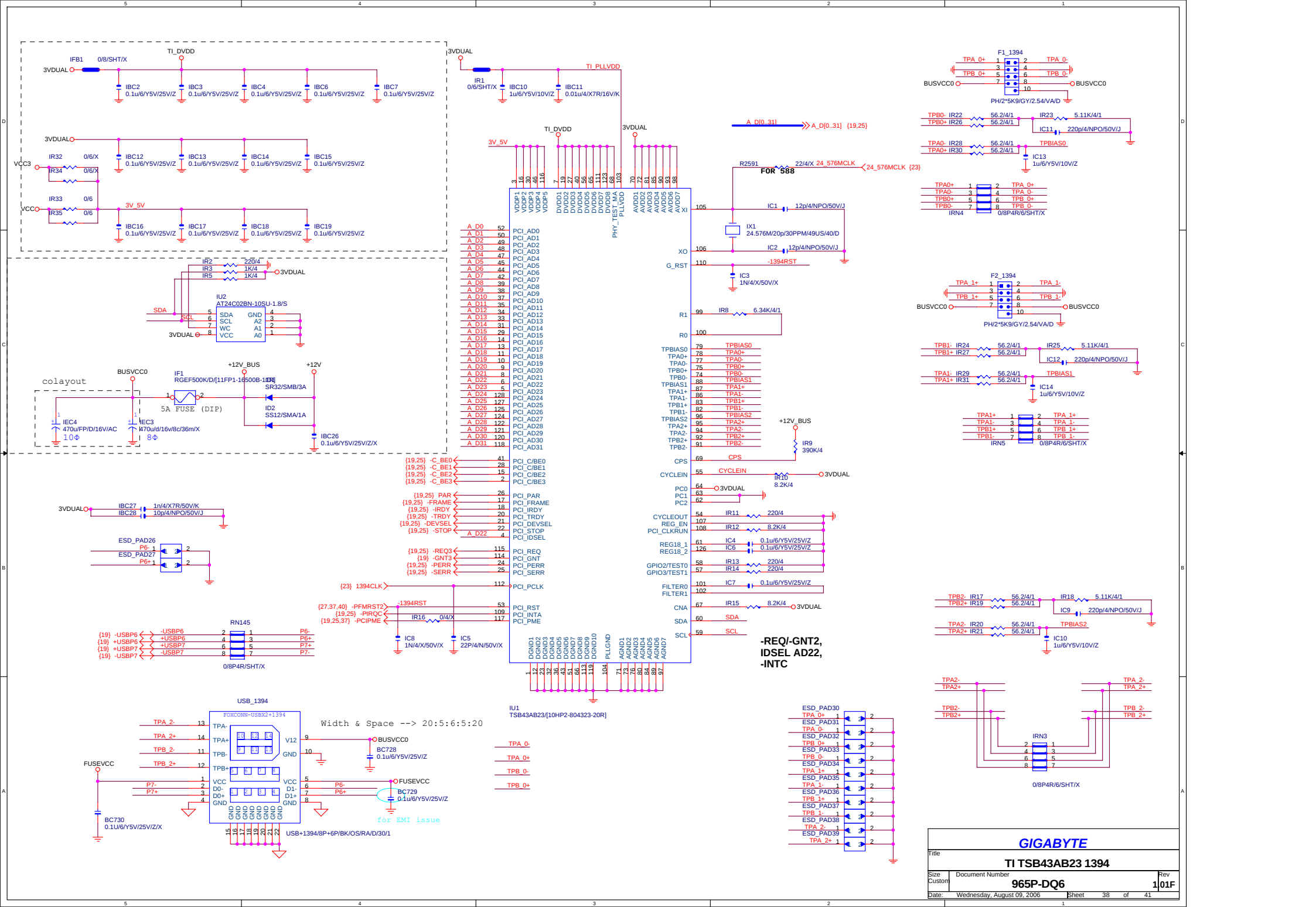


USB LAN CONNECTOR

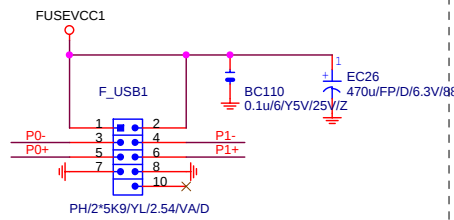
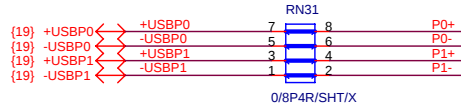
100歐母: [20/5/7/5/20]



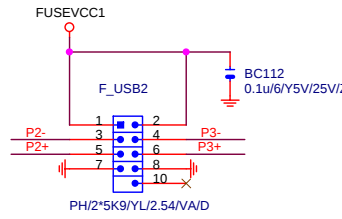
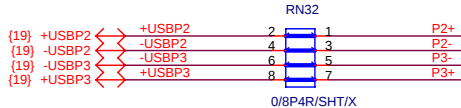
Gigabyte Technology			
MARVELL 88E8001			
Size	Document Number	Rev	
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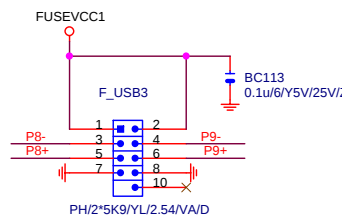
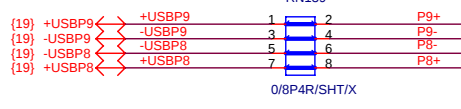
FRONT USB1



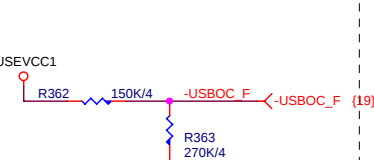
FRONT USB2



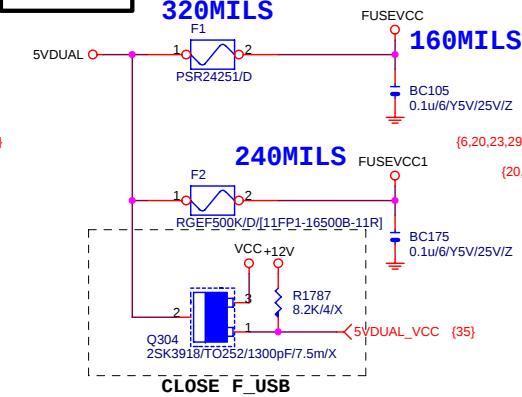
FRONT USB3



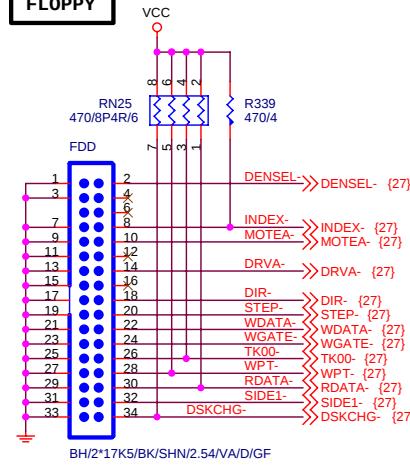
FRONT USB OC1



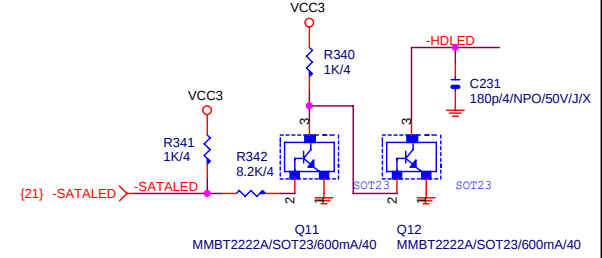
USB POWER



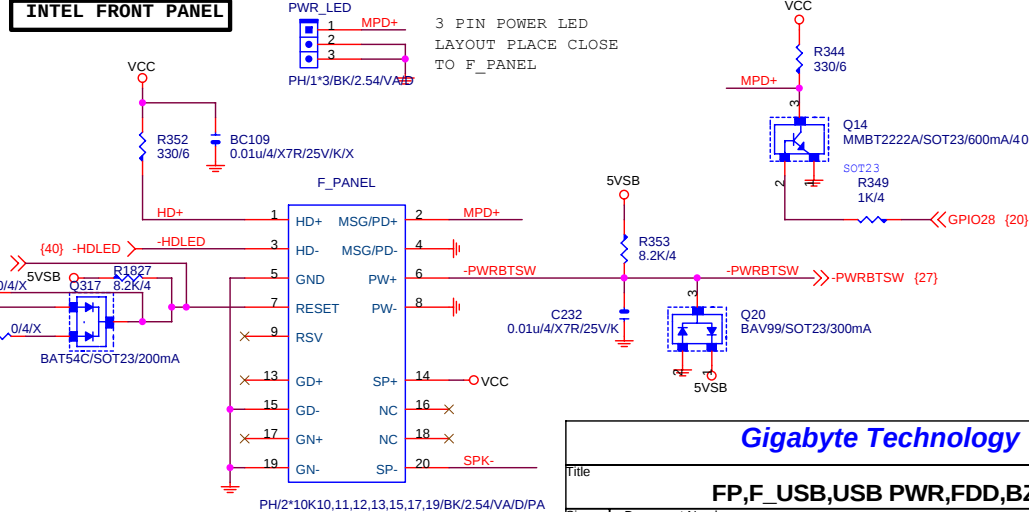
FLOPPY



SATA LED



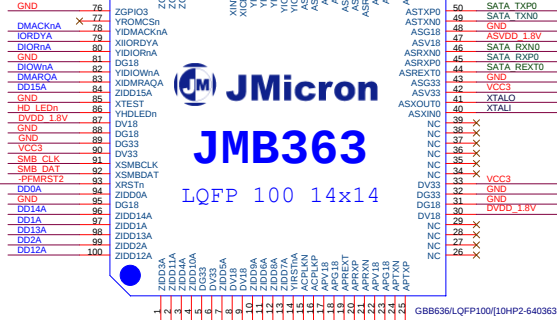
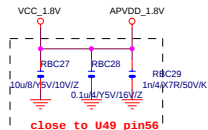
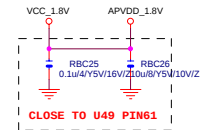
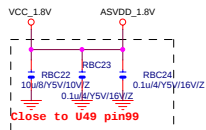
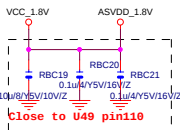
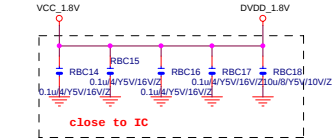
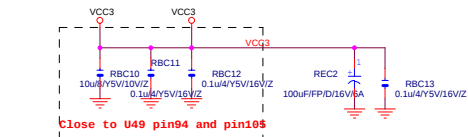
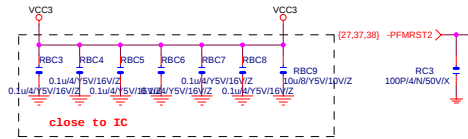
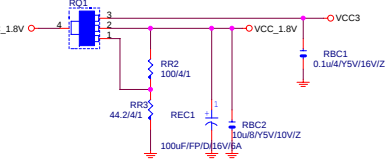
INTEL FRONT PANEL



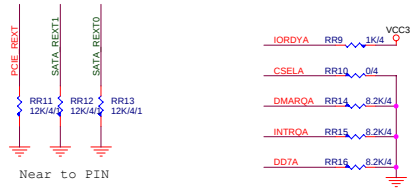
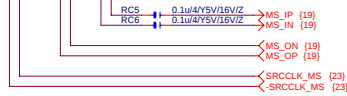
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3.3V to 1.8V Voltage Regulator

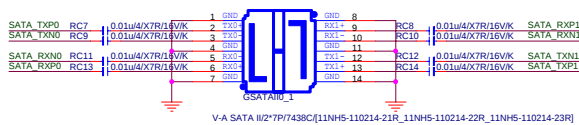
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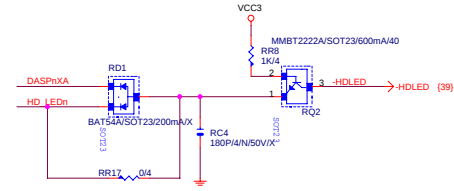
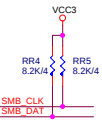
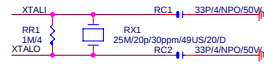
GBB836/LQFP100[10HP2-640363-20R]



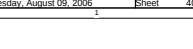
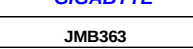
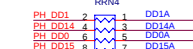
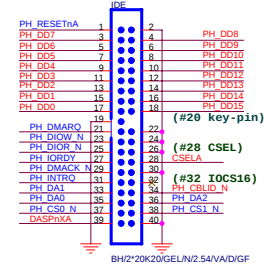
SATA Connector



V-A SATA N2*7P/7438C[11NH5-110214-21R_11NH5-110214-22R_11NH5-110214-23R]



IDE Connector



GIGABYTE

JMB363

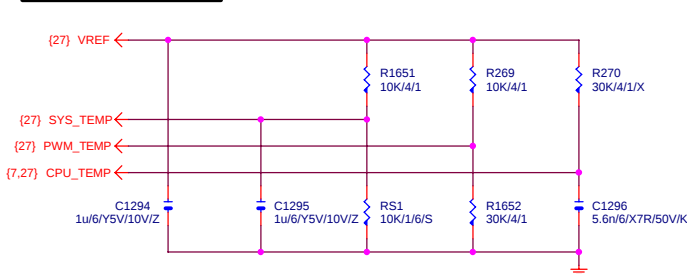
965P-DQ6

101F

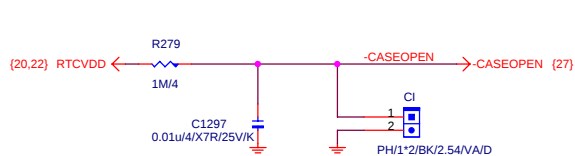
Rev

1

TEMP H/W MONITOR

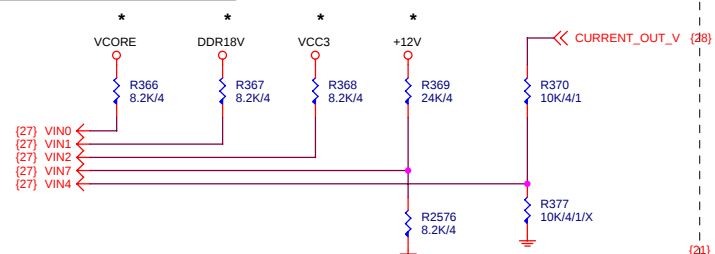


CASE OPEN

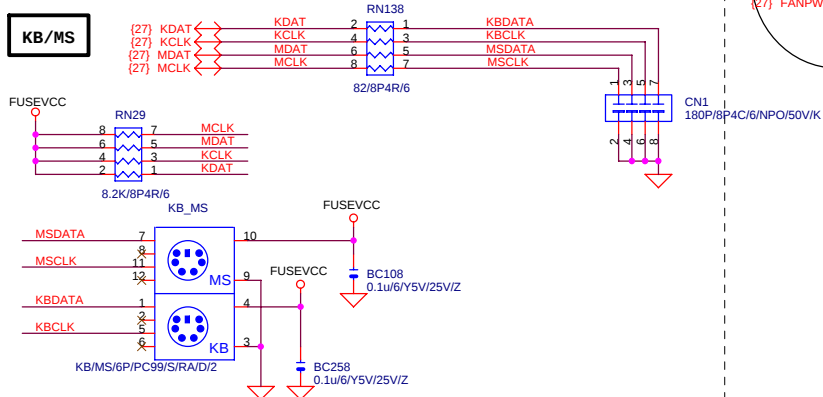


Case Open Circuits

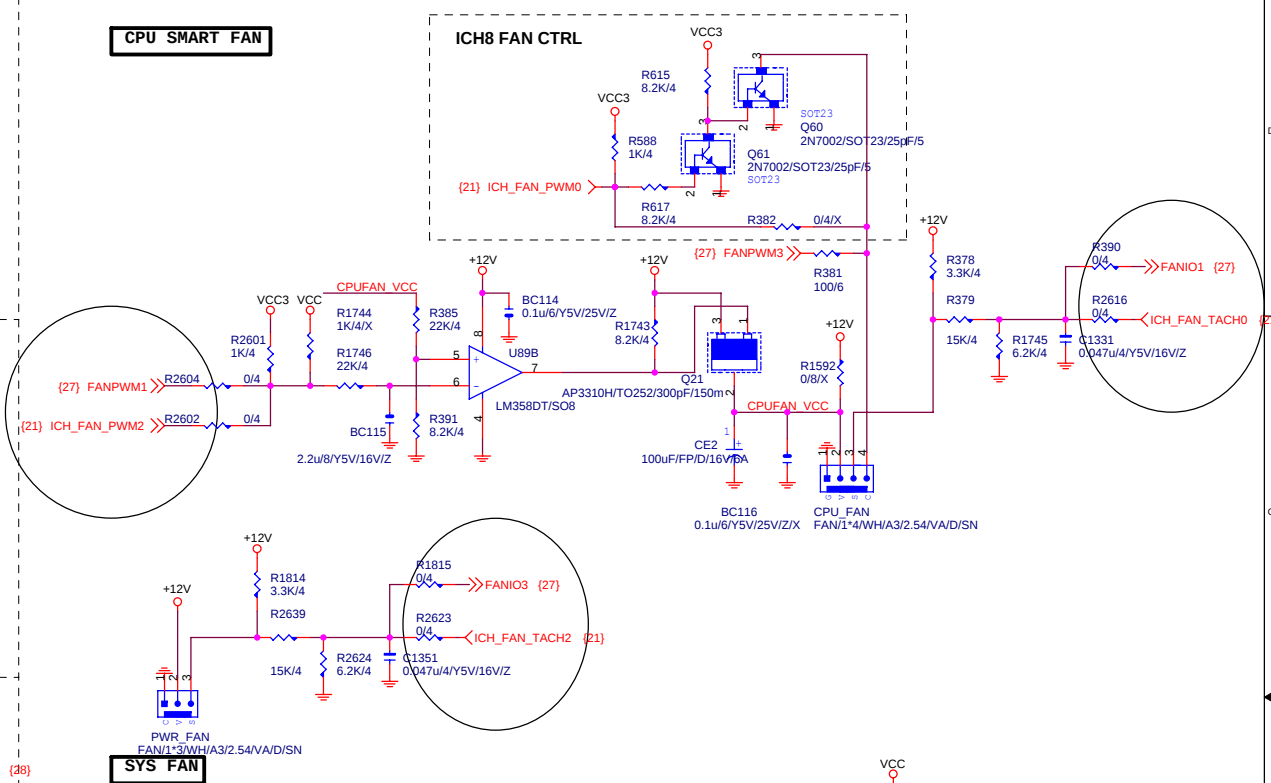
VOLTAGE - - H/W MONITOR



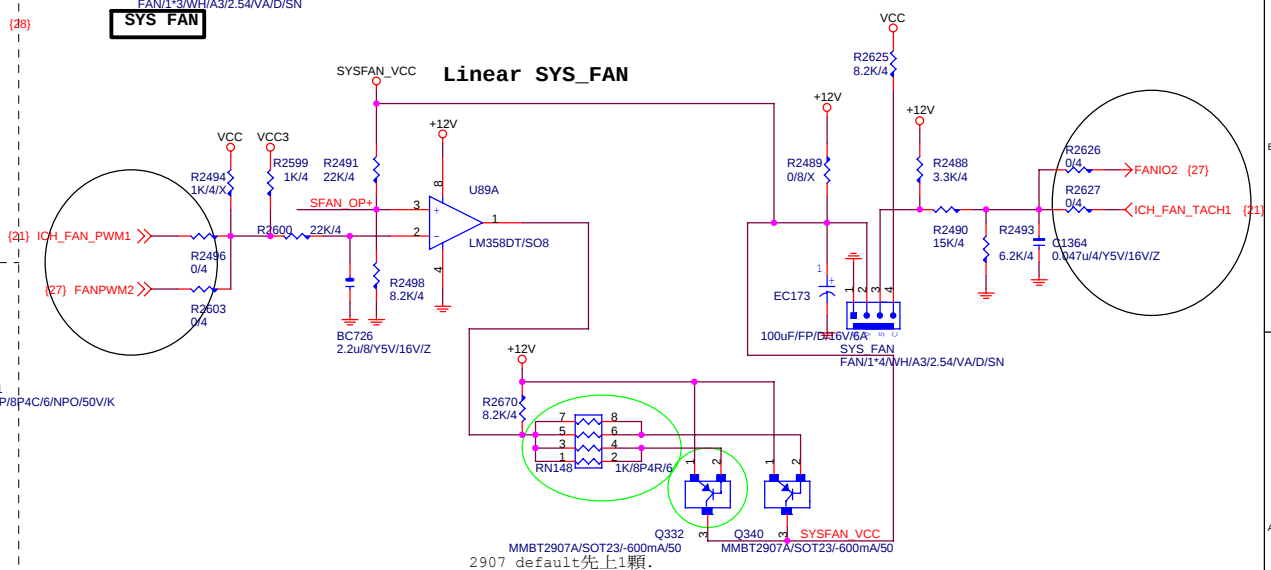
KB/MS



CPU SMART FAN



Linear SYS_FAN



Gigabyte Technology

Title

COM & LPT PORT

Size	Custom
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Date: Wednesday, August 09, 2006

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