

SHEET

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07	P4_LGA775_C
08	P4_LGA775_D
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10	GMCH-BROADWATER_DDRII
11	GMCH-BROADWATER_PCI E, DMI
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13	GMCH-BROADWATER_GND
14	GMCH-BROADWATER_PWR
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SHEET

TITLE

28	AZALIA ALC883
29	AUDIO JACK
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31	DISCRETE POWER
32	ATX POWER
33	IDE RAID IT8212
34	1394 TI TSB43AB23
35	LAN MARVELL 88E8053
36	FAN CONTROL
37	FRONT PANEL, FUSB, FDD

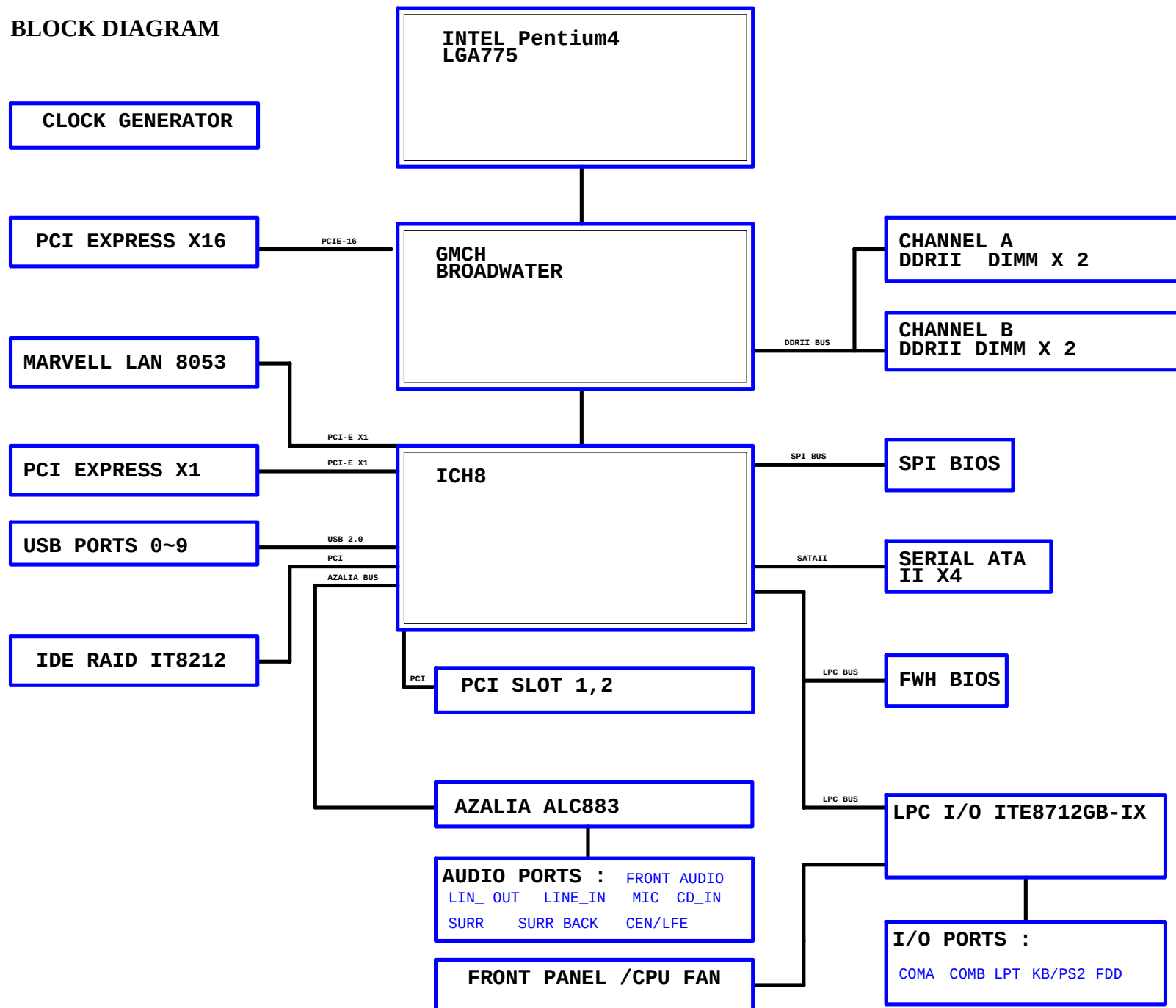
Component value change history

Data	Change Item	Reason
1.1A	EVT release	
1.1B	1. ADD F_AUDIO HEADPHONE FOR VISTA CR103-CR106	
2.0A	1. DVT RELEASE	
2.0B	1. SB, N/B HEATSINK CHANGE	
	2. 包材修改	
	3. PWM 阻值修改	
	4. 電阻,電容種類統一化	
	5. EC174 560uF -- >100uF	
	6. U11 加替料 WINBOND 8M FLASH:10HP4-152580-11R	
	7. USB_LAN1 加替料 UDE:11NR6-702009-09R	
	8. U49替料移除:CLK GEN ICS9LPRS587BGLF-T	
2.0C	1. 1.2uH修改料號:1.2uH/20A/PMU109/W/D	
	2. N/B , S/B HEATSINK順序修改 (965P-DS3/965G-DS3 Silent-pipe , 965P-S3 New Heatsink)	
	3 .Q330,Q331 Q_SOT23 Remove to Q330 Q_T0252	
	4 .R1955~R1958 R0402-2-SHORT10 to R0402-2	
	5. R1970 1K/4 --> 100/4/1	
	6. ADD PECI CTRL CIRCUIT	
	7. F1,F2,F3 SMD FUSE 1.1A --> 1.6A	
	8. PCB REV2.01 --> REV2.02	
2.0C-PVT	1. 包材修改	
2.0D-DVT	1. PCB REV2.02 --> REV2.03	
2.0E	1. DL2~DL7 0.3uH --> 0.4uH	
	2. DR11 3.16K/4/1 --> 3.24K/4/1	
	3. PWM FS CHANGE 200KHz DR103 82K/4 --> 120K/4	
	4. DDRVTT CHANGE R1882 1.78K/6/1 REMOVE , ADD 1876 1K/6/1	
	5. DDR18V_OV3 4.02K/6/1 --> 3.01K/6/1	
2.0E-ECN	3. PWM FS CHANGE 200KHz DR103 120K/4 --> 82K/4	
2.0F	1. PCB REV2.02 --> REV2.03	
2.0G	1. 0.4uH修改料號	
	2. DR105 加替料10RC4-002433-23R	
	3. 主料10CM2-024704-51R,加替料10CM2-024704-53R	

Circuit or PCB layout change for next version

DATE	Change Item	Reason
1.02	EVT release	
2.0	1. PWM 3 PHASE --> 6 PHASE	
	2. SUPPORT VISTA FUNCTION	
	3. APPROVE POWER-ON SHUN DOWN ISSUE	
2.01	1. REMOVE CQ10,CR101,CR102	
	2. PWR_FAN R1814 VCC --> +12V	
	3. PWM 6 PHASE COPY FROM 946GZ-S3 Rev2.0	
	4. U11 FOOTPRINT IC8S0-SOCKET-1 --> IC8S0-SOCKET-2	
	5. EC174 EC10D8MM --> EC6D8MM,BC730 C0603 --> C0805	
2.02	1 .Q330,Q331 Q_SOT23 Remove a Q330 Q_T0252 FOR SYS_FAN POWER	
	2 .R1955~R1958 R0402-2-SHORT10 a R0402-2	
	3. ADD CPU PIN.E7=CPU_TP21	
	4. L15,L16 Footprint change to "CHOKE2U-20A-SQ-1"	
	5. CHANGE PECI CTRL CIRCUIT	
2.03	1. RU2 PIN40,41 NET CHANGE TO GND	
2.04	1. L13,L14 1.2uH Change Footprint "CHOKE08U-15A 1P-1"	
	2. L15,L15 2uH Change Footprint "CHOKE2U-20A-SQ-2"	
3.3	1. FOR FSB1333 CPU SUPPORT	
下板修改	1. 增加 CPU FSBSEL2 Pull uP 電阻	
BOM		
2.0H	1. PCB REV2.03 --> REV 2.04	
	2. 470uF/6.3V & 560uF/4V --> 560uF/6.3V(僅試產,量產版本要改回來)	
	3. D3,D9,CD1,CD2,PD1 10DS1-124148-04R/05R--> 10DS7-734148-01R/02R (僅試產,量產版本要改回來)	
	4. U54 M8056/A2 --> M8056/B0	
3.3A	1. FOR FSB1333 CPU SUPPORT	
	BOM要再建立9M965PS3-00-33A	
3.3B	1. VTT_GMCH Q329 AP40T03H/T0252/655pF/25m-->2SK3918/T0252	
	2. U51,U53 REMOVE LD7120	
3.3C	1. U54 8056 REV.A2 --> B0	
	2. CD DRIVER REV1.02 --> REV1.03	

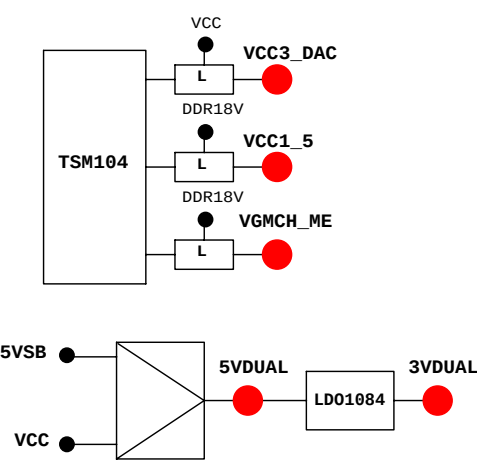
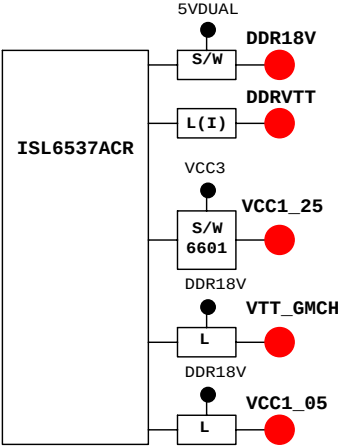
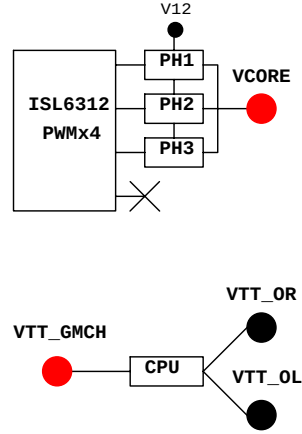
BLOCK DIAGRAM



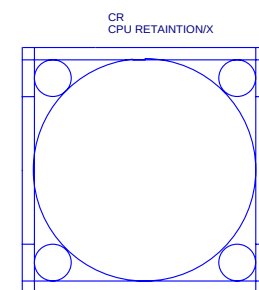
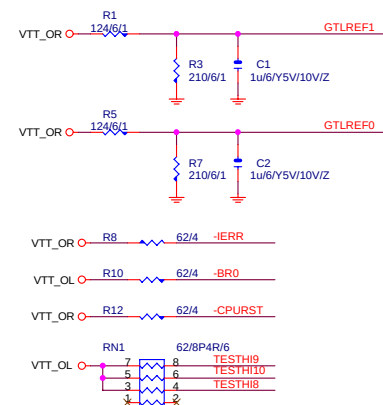
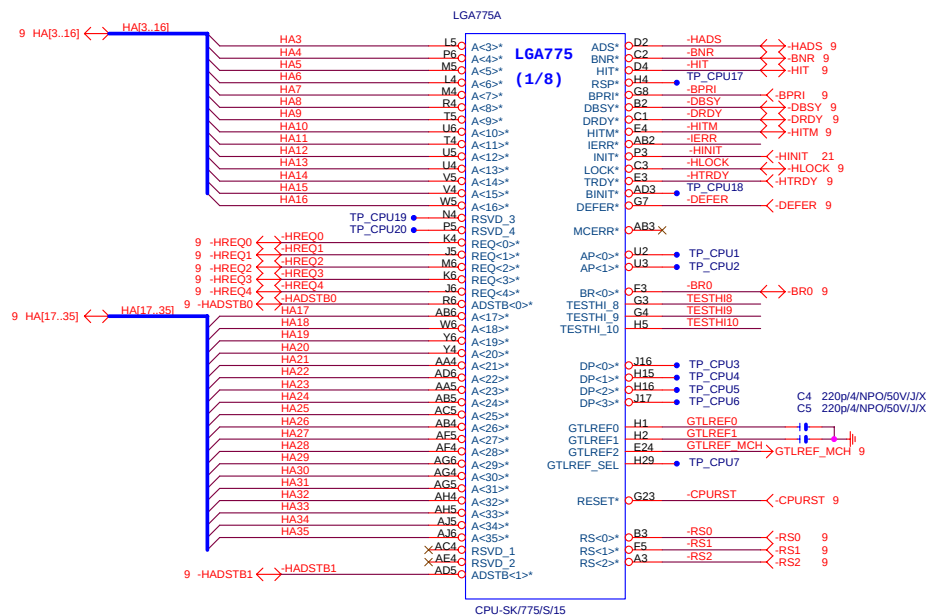
ICH8 GPIO LIST TABLE

PIN	NAME	PWR WELL	AFTER/ PLTRST	USAGE	NOTE
GP0		MAIN	IN	-ACZ_DET	P/U 8.2K VCC3
GP1/TACH1		MAIN	IN	ICH_FAN_TACH1	P/U 8.2K VCC3
GP2/PIRQE#		MAIN	IN	-PIRQE	P/U 8.2K VCC3
GP3/PIRQF#		MAIN	IN	-PIRQF	P/U 8.2K VCC3
GP4/PIRQG#		MAIN	IN	-PIRQG	P/U 8.2K VCC3
GP5/PIRQH#		MAIN	IN	-PIRQH	P/U 8.2K VCC3
GP6/TACH2		MAIN	IN	ICH_FAN_TACH2	P/U 8.2K VCC3
GP7/TACH3		MAIN	IN	ICH_FAN_TACH3	P/U 8.2K VCC3
GP8		STBY	IN	GPIO8(DUALBIOS_INPUT)	P/U 8.2K 3VDUAL
GP9		STBY	OUT	WOL_ONLY	P/D 100K GND
GP10		STBY	IN	CLGPIO1	P/U 8.2K 3VDUAL
GP11/SMBALERT#		STBY	OUT	-SMBALRT	P/U 8.2K 3VDUAL
GP12		STBY	IN	MB_ID0	P/U 8.2K 3VDUAL
GP13		STBY	IN	-LPCPME	P/U 8.2K 3VDUAL
GP14		STBY	IN	CLGPIO2	P/U 8.2K 3VDUAL
GP15		STBY	OUT	LAN_DISABLE(STP_PCI-)	N/A
GP16		MAIN	OUT/LOW	RESET	N/A
GP17/TACH0		MAIN	IN	ICH_FAN_TACH0	P/U 8.2K VCC3
GP18		MAIN	OUT	MB_ID1	P/U 8.2K VCC3
GP19		MAIN	IN	SATA1GP	P/U 8.2K VCC3
GP20		MAIN	OUT	-SPI_WP0	P/U 1K 3VCL
GP21		MAIN	IN	SATA0GP	P/U 8.2K VCC3
GP22		MAIN	IN	SCLOCK	P/U 8.2K VCC3
GP23		MAIN	OUT	-LDRQ1	P/U 8.2K VCC3
GP24		STBY	OUT	CLGPIO0	P/U 8.2K 3VDUAL
GP25		STBY	IN	MB_ID2(STP_CPU-)	P/U 8.2K 3VDUAL
GP26/S4_STATE#		STBY	OUT	S4_STATE#	P/U 8.2K 3VDUAL
GP27		STBY	OUT/LOW	GPIO27(EL_STATE0)	P/U 8.2K 3VDUAL
GP28		STBY	OUT/LOW	PWR_LED(EL_STATE1)	N/A
GP29/OC5#		STBY	IN	-USB0C_R	P/U FUSEVCC
GP30/OC6#		STBY	IN	-USB0C_R	P/U FUSEVCC
GP31/OC7#		STBY	IN	-USB0C_R	P/U FUSEVCC
GP32		MAIN	OUT	DUAL_BIOS	P/U 100K+1M VCC3
GP33		MAIN	OUT	DUAL_BIOS	P/U 8.2K VCC3
GP34		MAIN	OUT/LOW	GPIO34/SMB_RST	N/A
GP35		MAIN	OUT	SATACLKREQ#	N/A
GP36		MAIN	IN	SATA2GP	P/U 8.2K VCC3
GP37		MAIN	IN	SATA3GP	P/U 8.2K VCC3
GP38		MAIN	IN	SLOAD	P/U 8.2K VCC3
GP39		MAIN	IN	GPIO39	P/D 8.2K GND
GP48		MAIN	IN	GPIO48	P/U 8.2K VCC3
GP49		MAIN	IN	CPUPWROK	P/U 100 VTT_OL

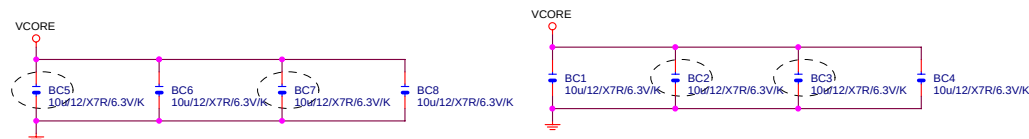
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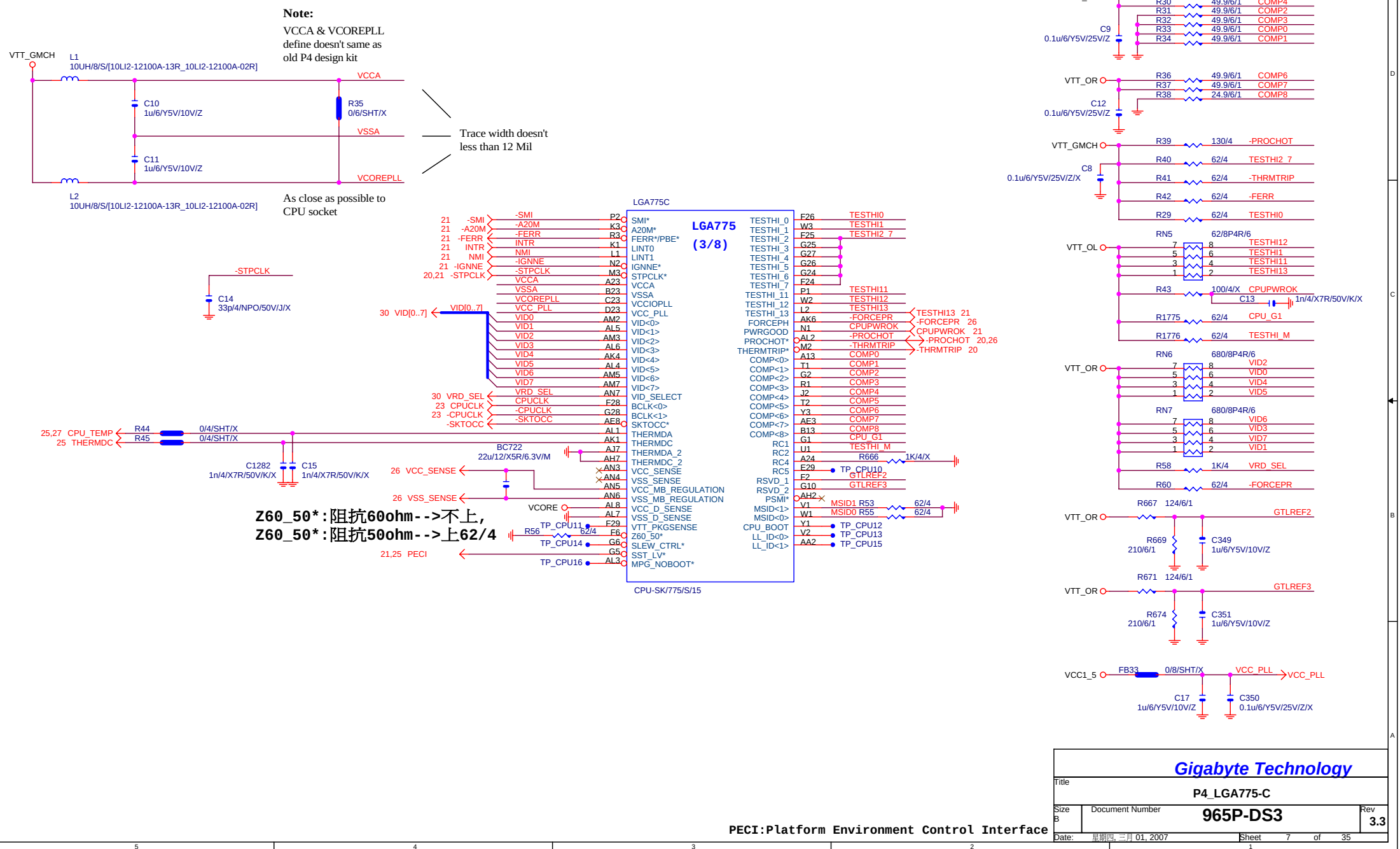


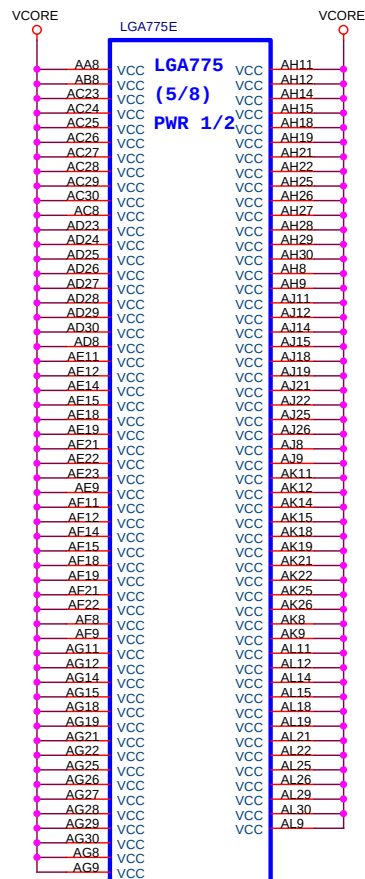
HA/REQ: 4/14
ADSTB: 4/17



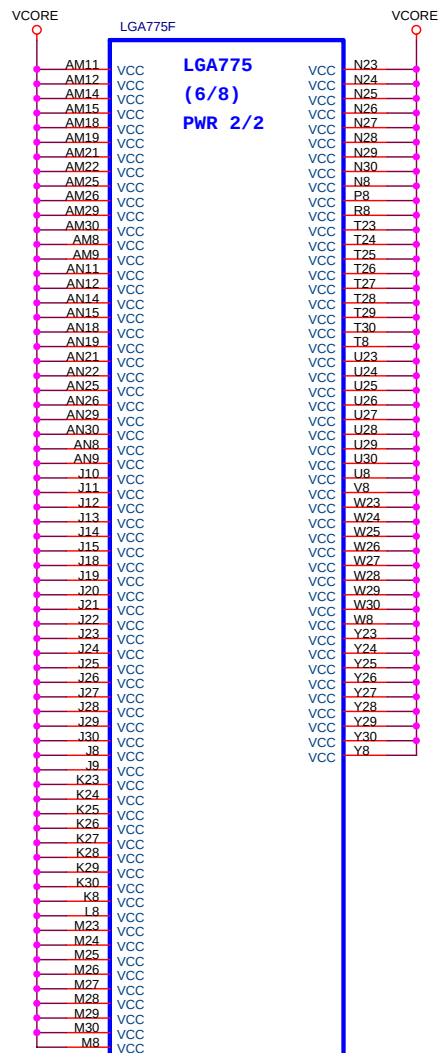
Impedance=50 +- 15% for 4 -layer



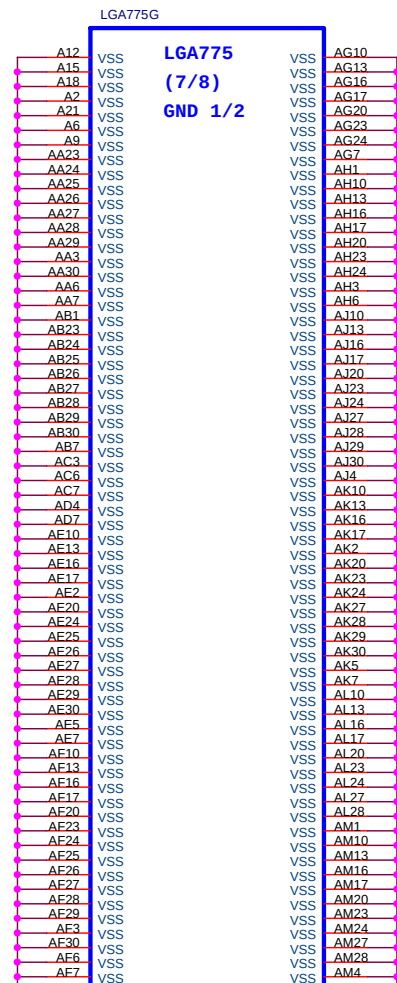




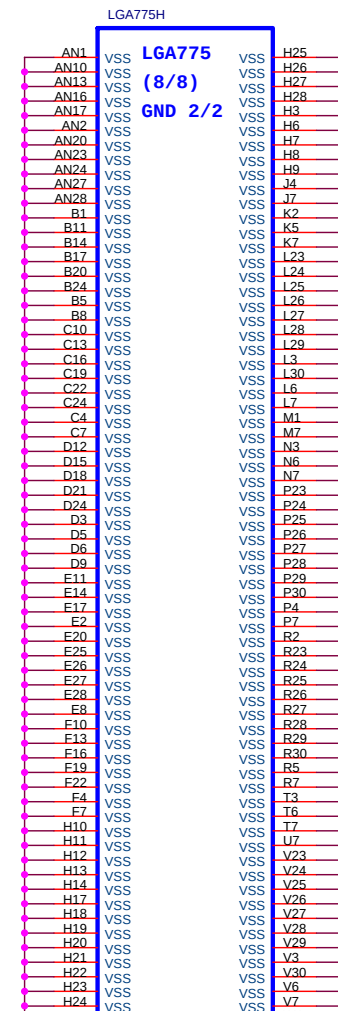
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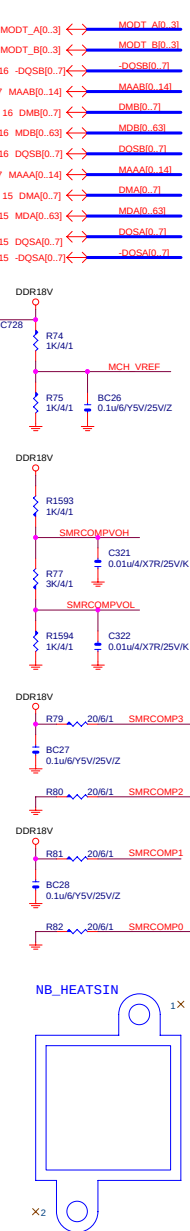
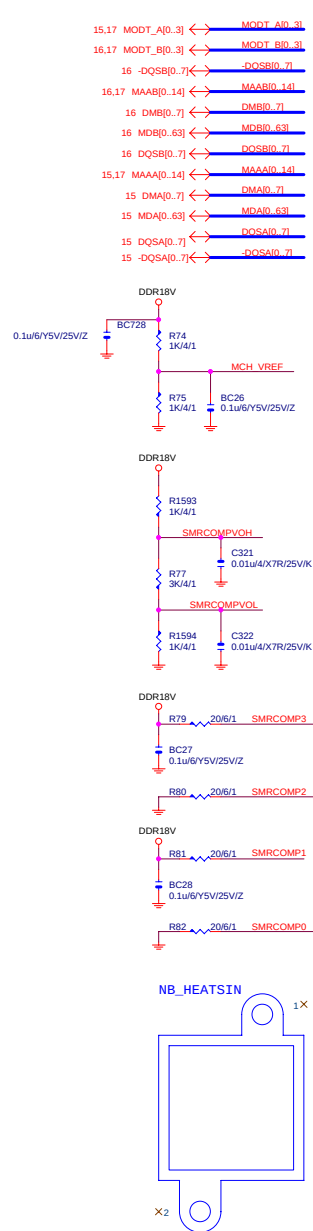
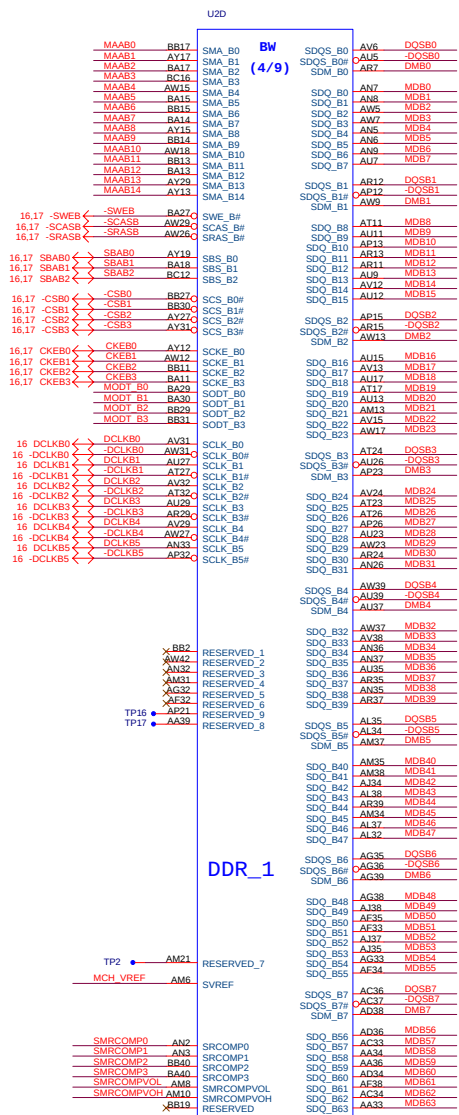
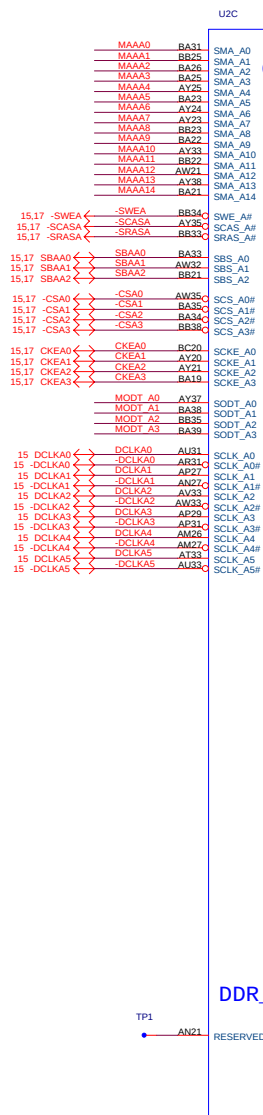
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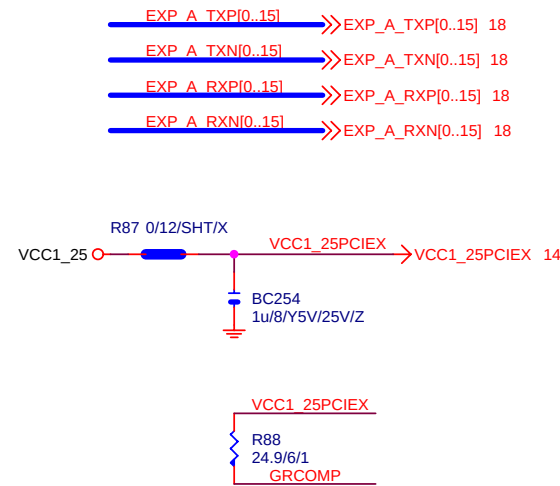
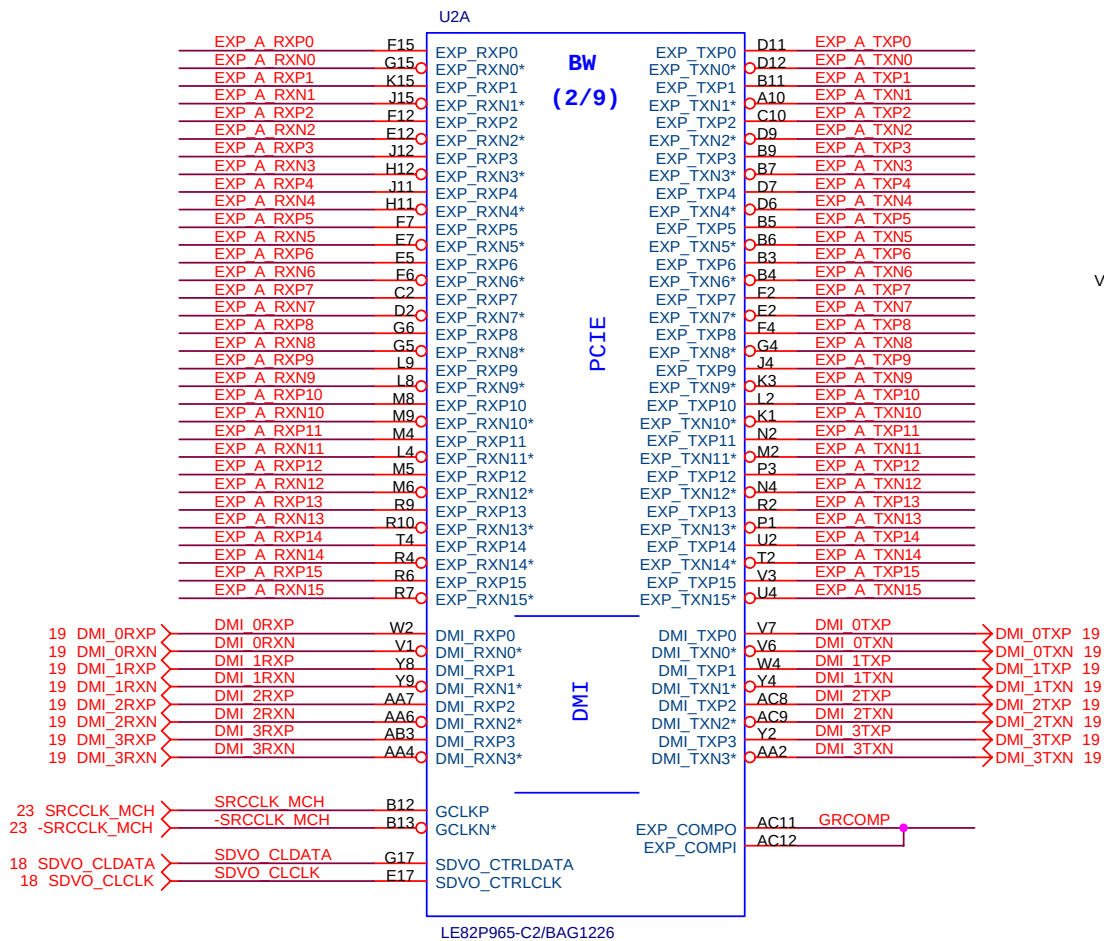


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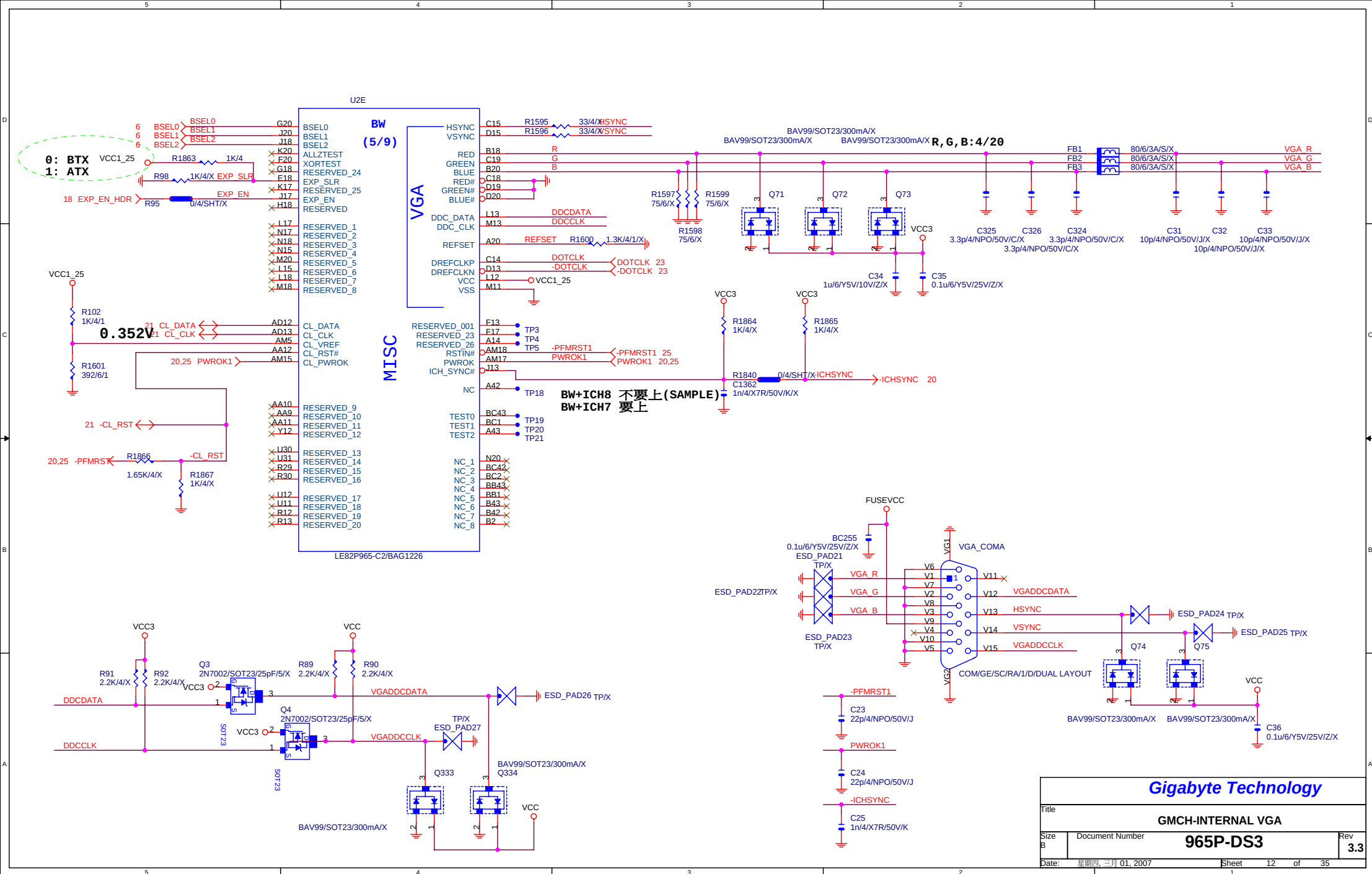


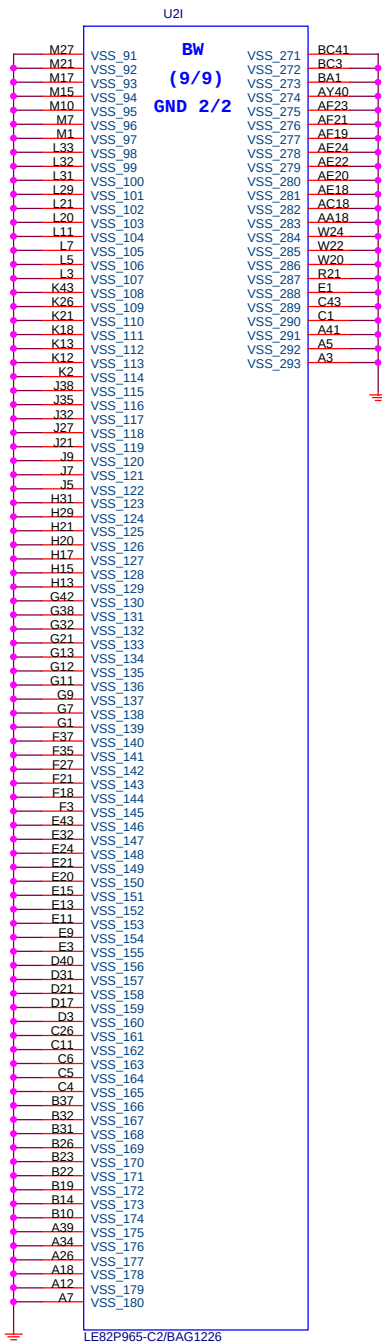
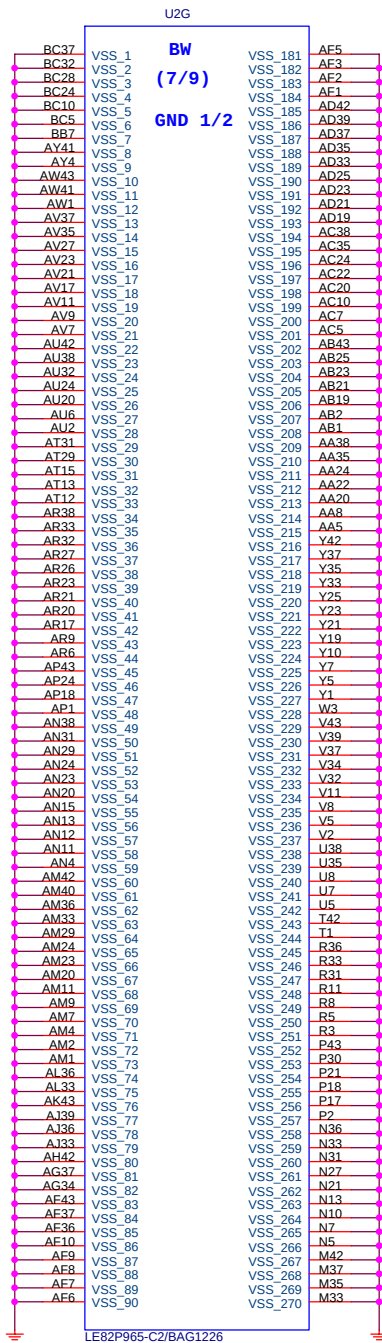
CPU-SK/775/S/15





Gigabyte Technology			
Title			
GMCH-PCI E & DMI			
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Title
GMCH-GND

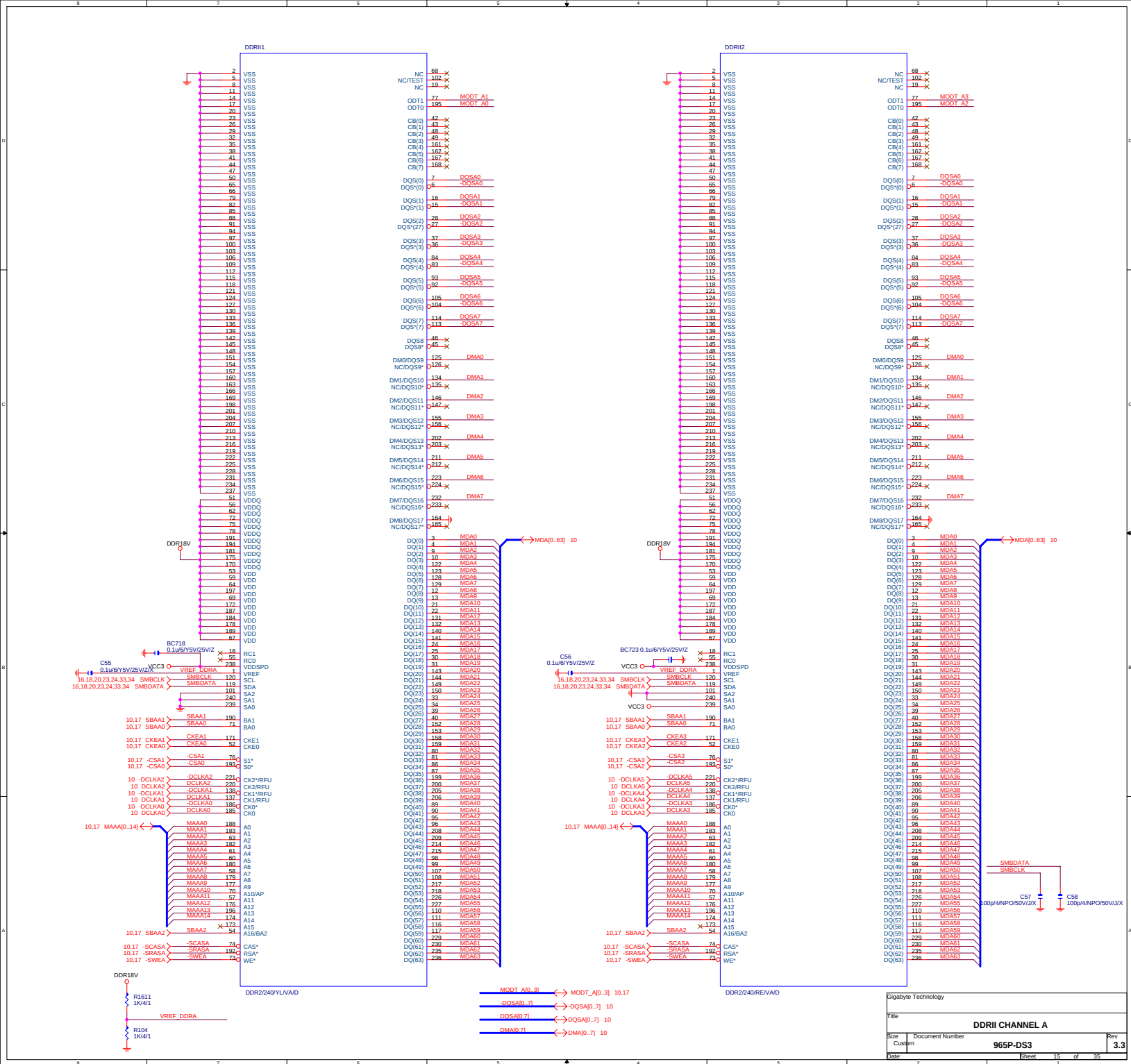
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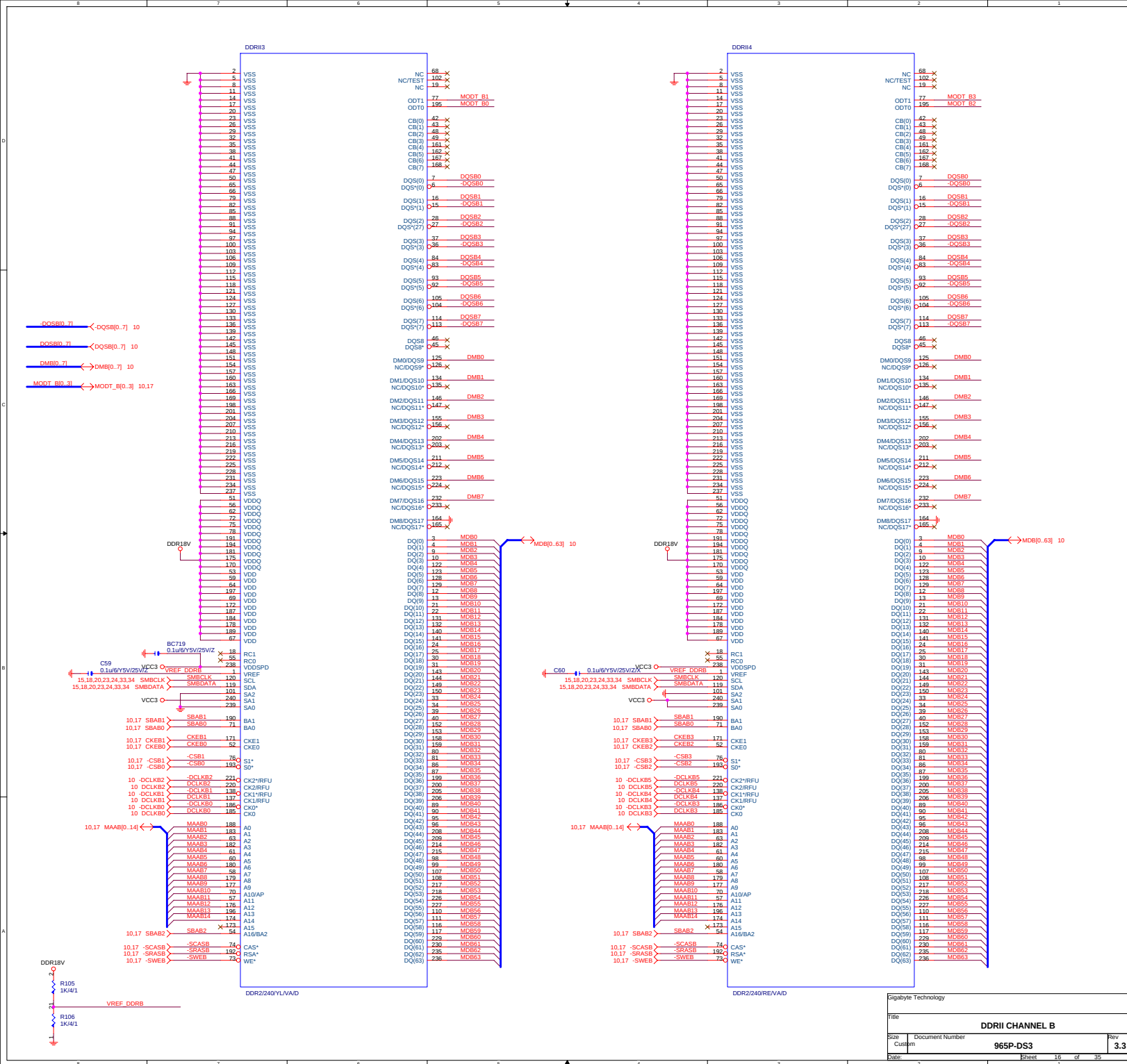
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965P-DS3

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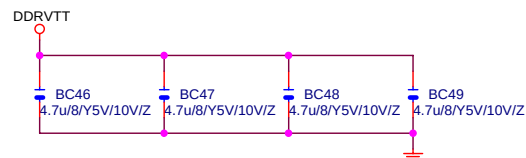
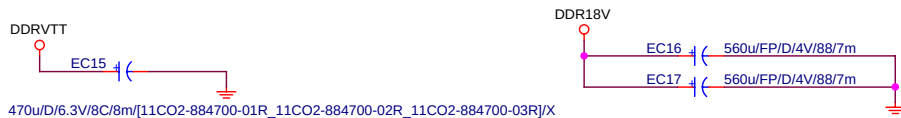
Rev
3.3





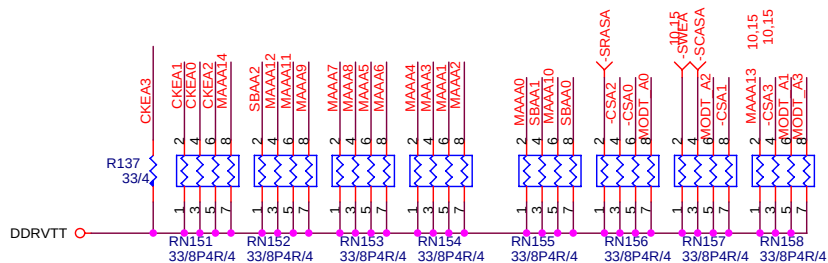
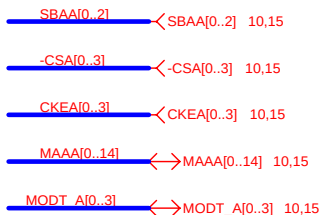
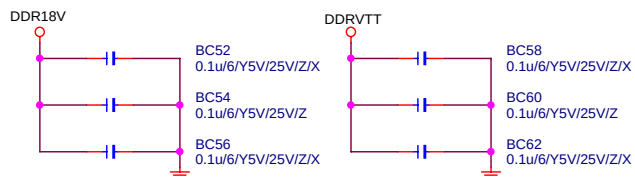
DDR TERMINATION CHANNEL A

DDRVTT Decouple



DDR18V Decouple

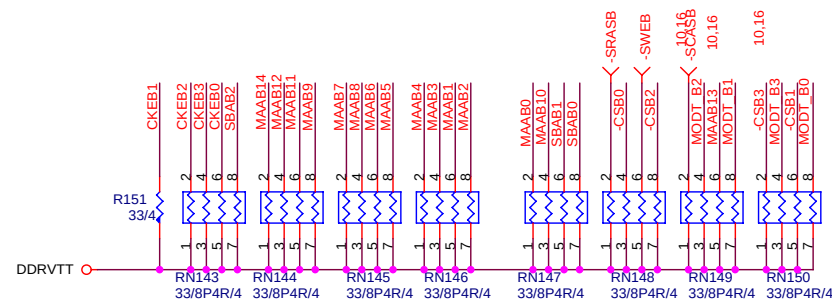
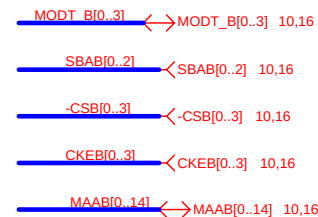
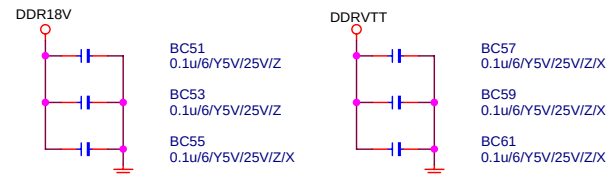
DDRVTT Decouple



DDR TERMINATION CHANNEL B

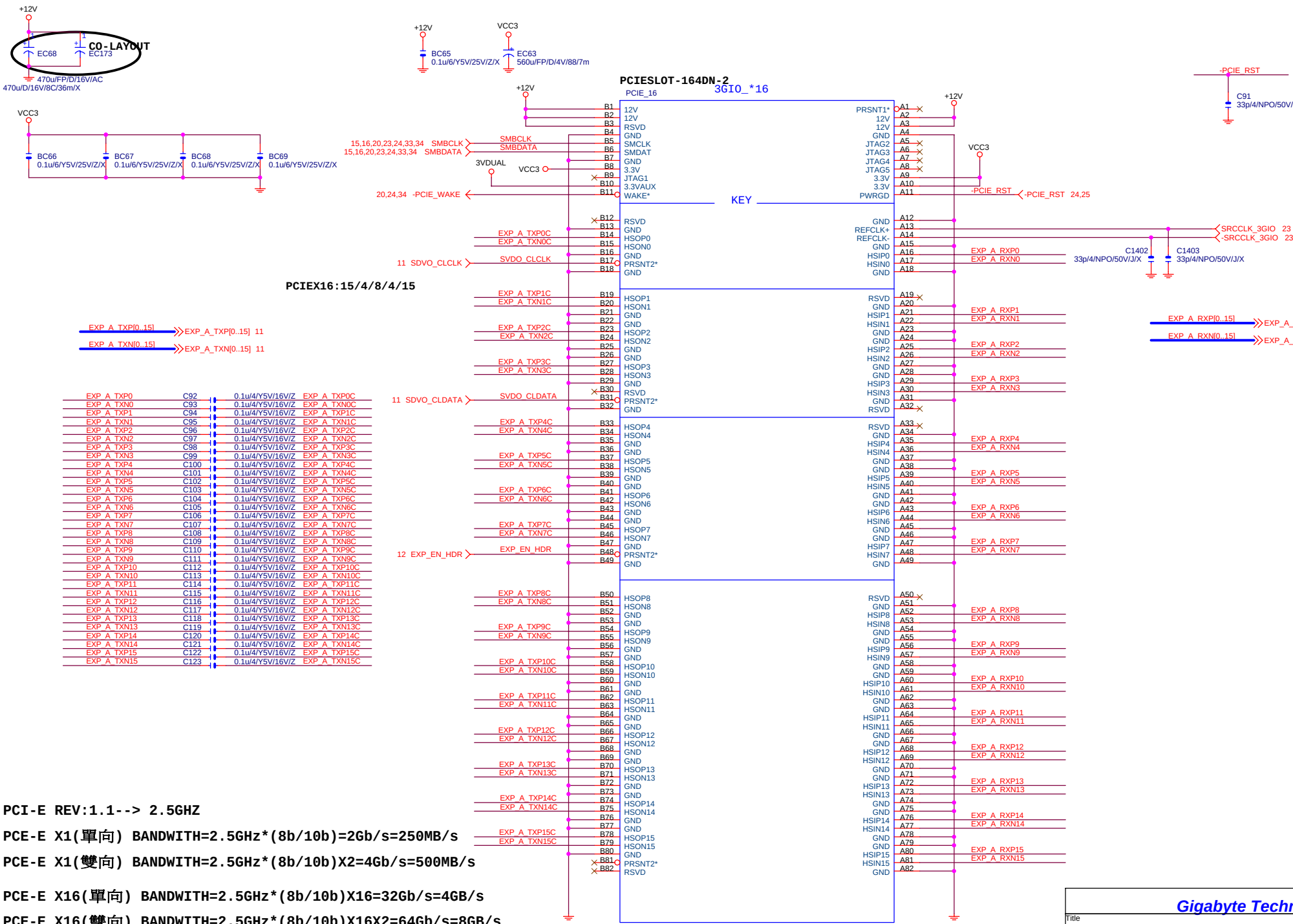
DDR18V Decouple

DDRVTT Decouple



Gigabyte Technology

Title		
DDRII TERMINATOR		
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PCI-E REV:1.1--> 2.5GHZ

PCE-E X1(單向) BANDWITH=2.5GHZ*(8b/10b)=2Gb/s=250MB/s

PCE-E X1(雙向) BANDWITH=2.5GHZ*(8b/10b)X2=4Gb/s=500MB/s

PCE-E X16(單向) BANDWITH=2.5GHZ*(8b/10b)X16=32Gb/s=4GB/s

PCE-E X16(雙向) BANDWITH=2.5GHZ*(8b/10b)X16X2=64Gb/s=8GB/s

PCI-E REV:2.0--> 5GHZ

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Title

PCI EXPRESS * 16

Document Number

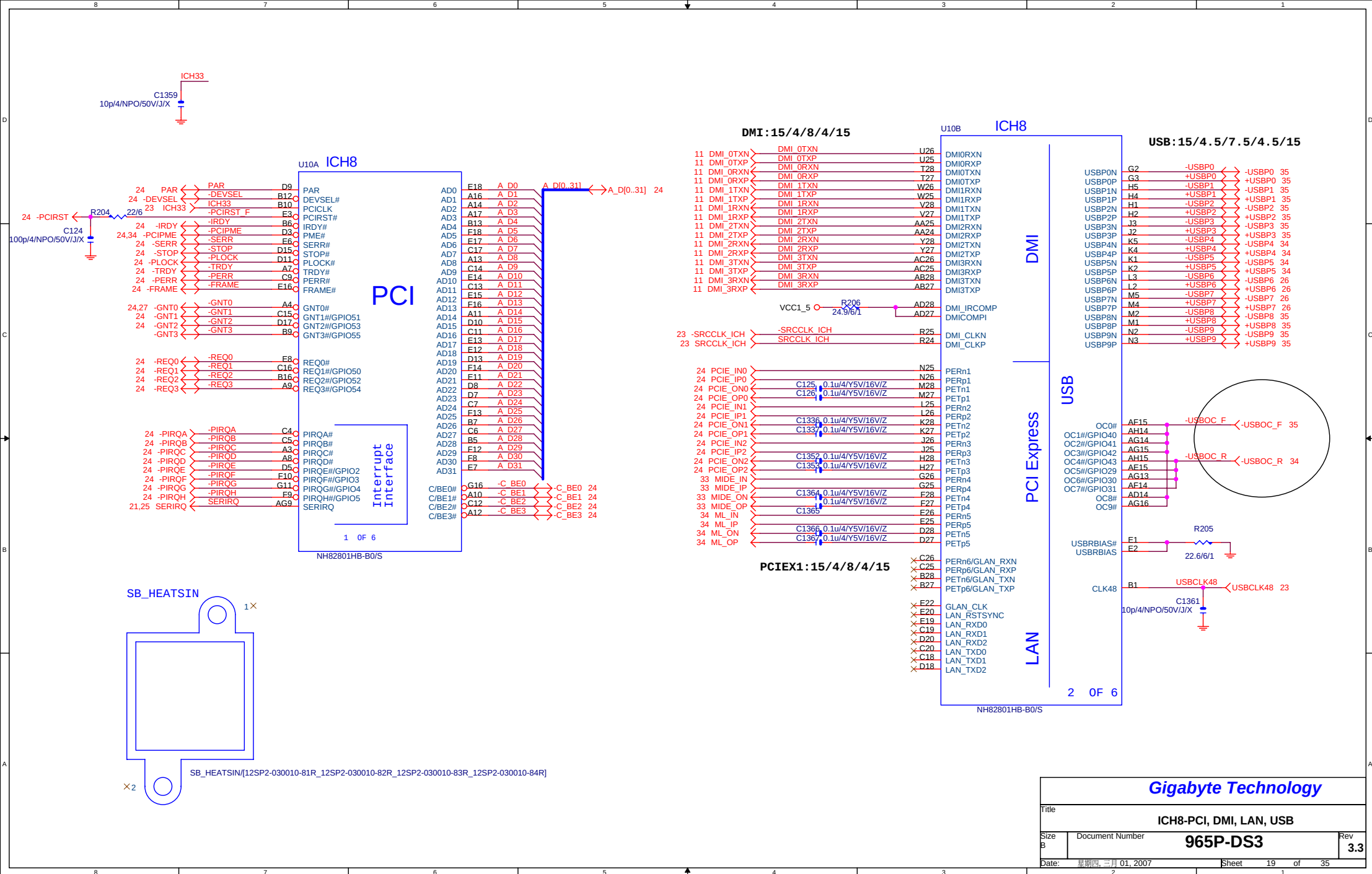
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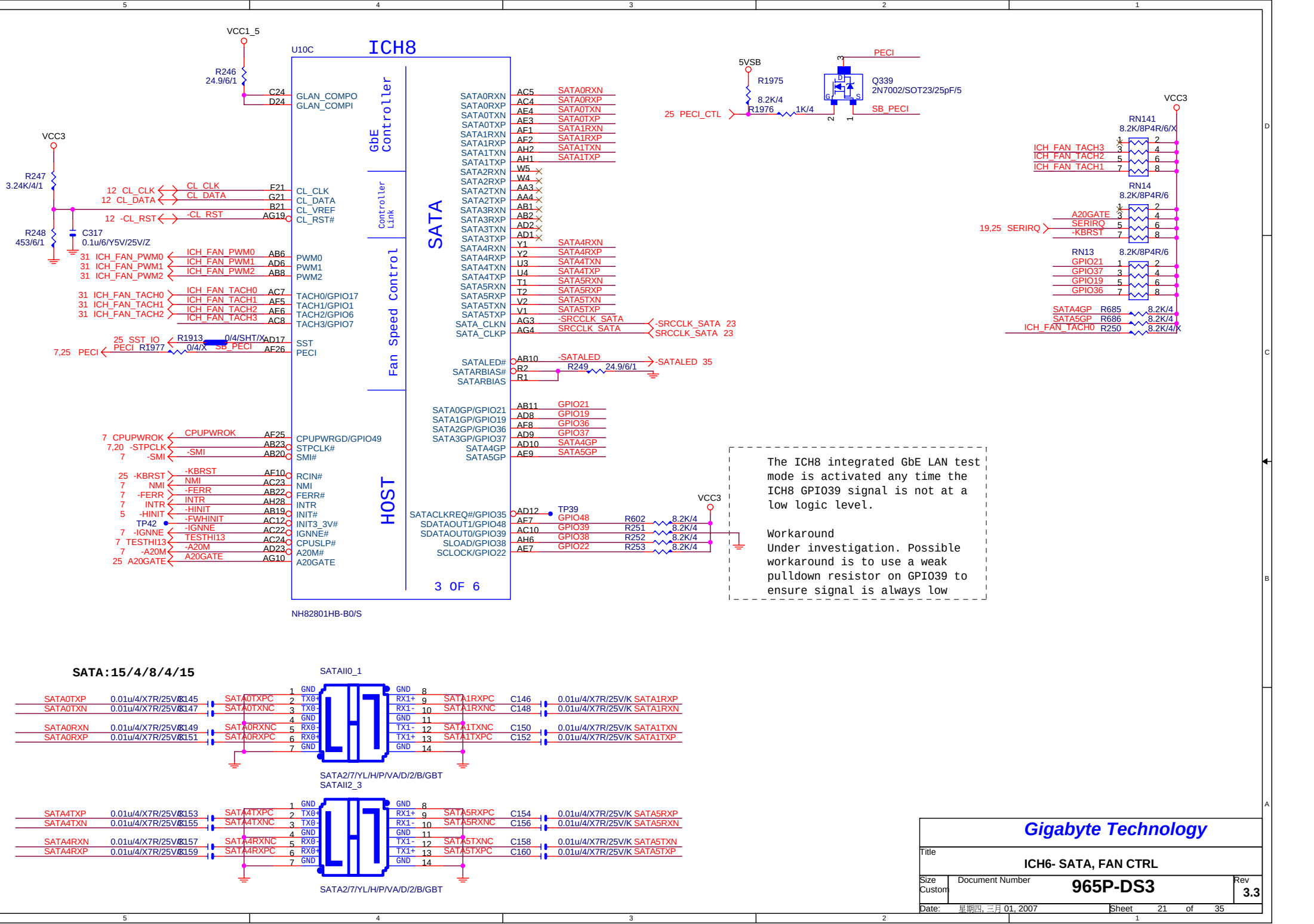
Rev

3.3

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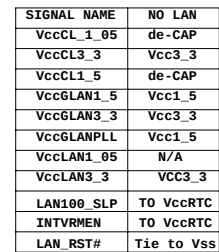
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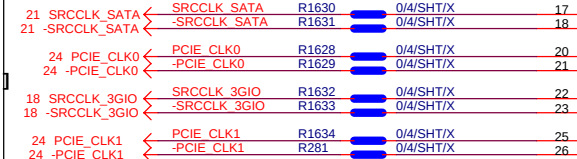
<i>Gigabyte Technology</i>			
Title			
ICH6-PWR & GND			
Size	Document Number	965P-DS3	Rev
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CLK GEN CK505

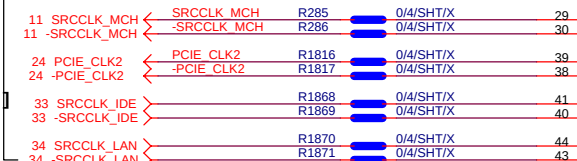
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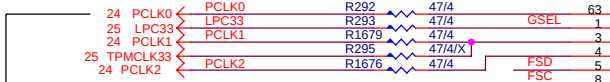
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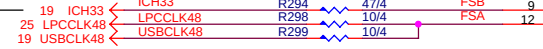
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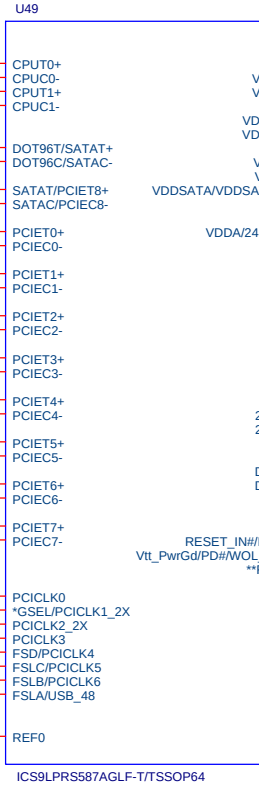
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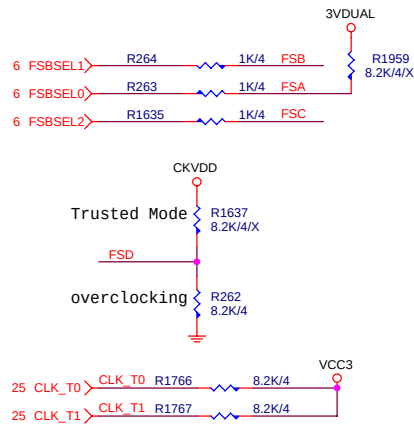
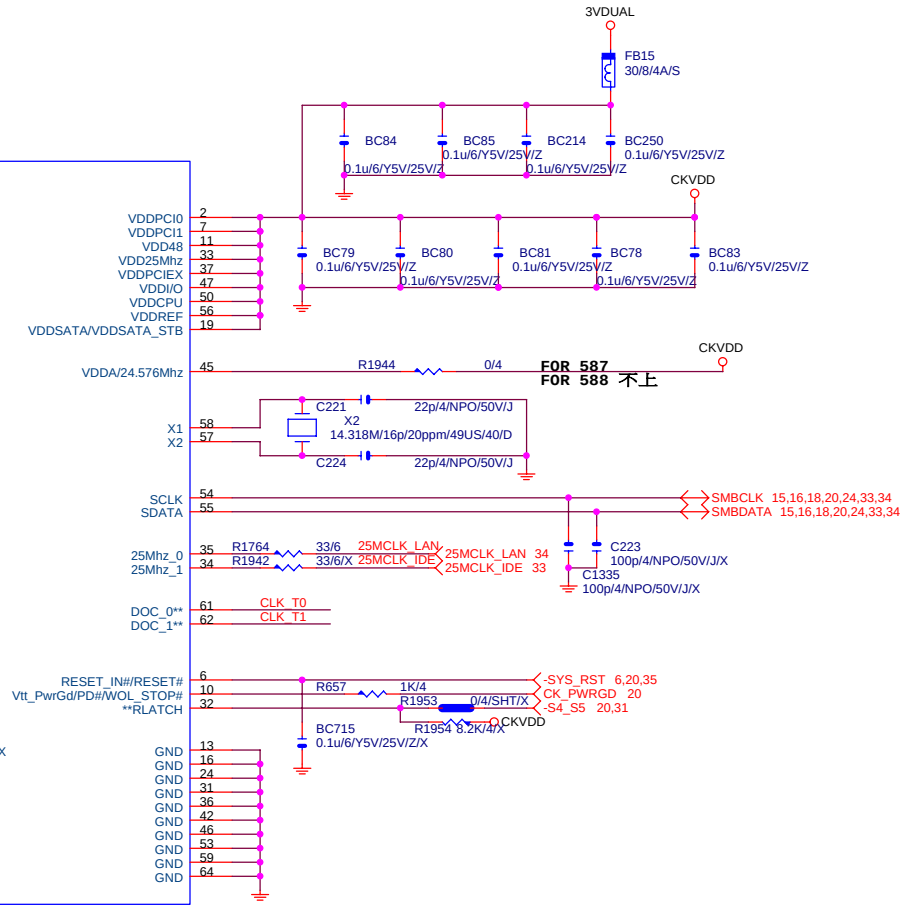
50欧姆: [4/10]



50欧姆: [4/10]



GSEL=1,96Mhz from 14/15,SATACLK from 17/18
GSEL=0,SATACLK from 14/15,PCIECLK from 17/18

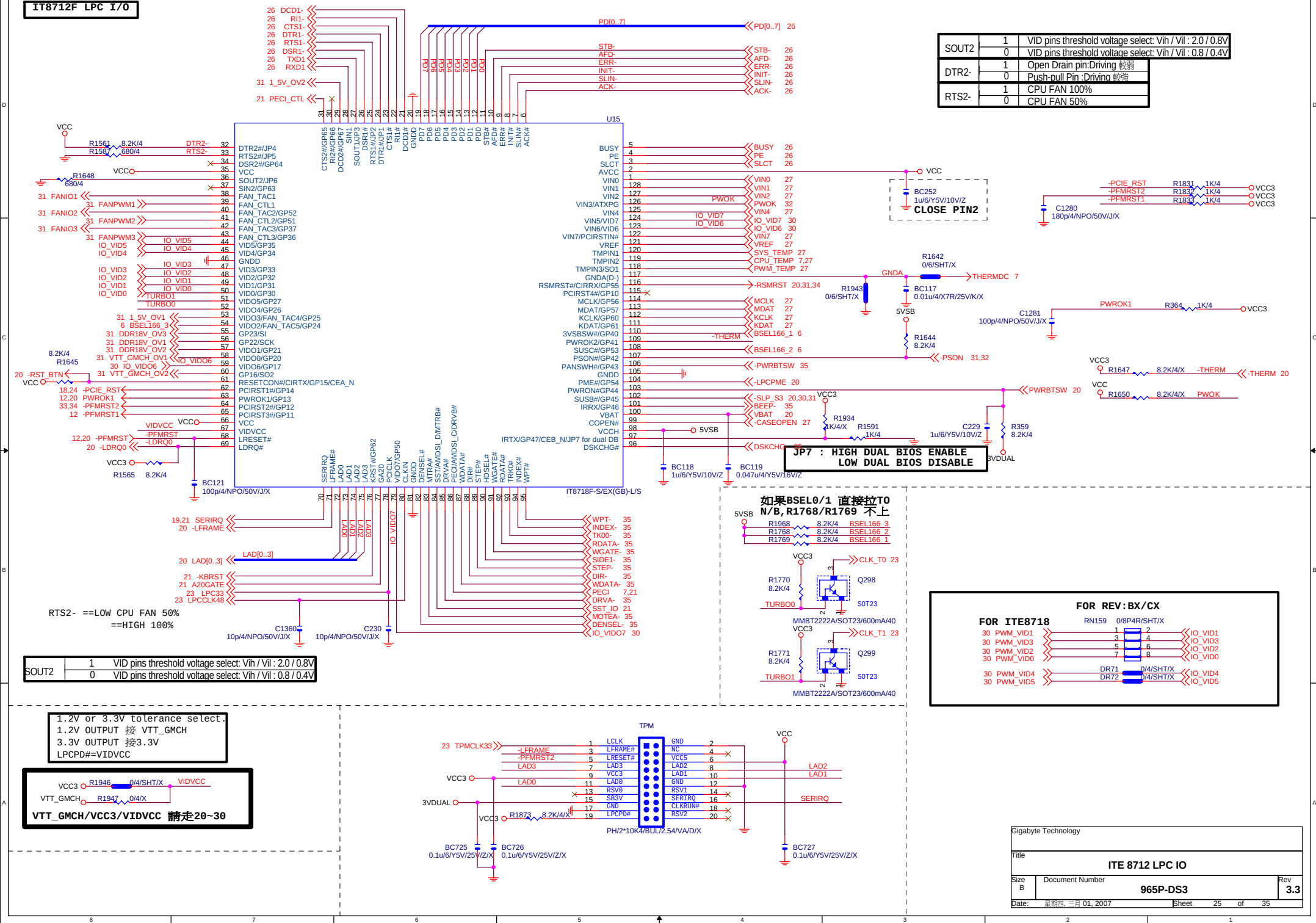


Gigabyte Technology

CK505 CLK GEN
965P-DS3

Title	CK505 CLK GEN		
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IT8712F LPC I/O



SOUT2	1	VID pins threshold voltage select: Vih / Vil : 2.0 / 0.8V
	0	VID pins threshold voltage select: Vih / Vil : 0.8 / 0.4V
DTR2-	1	Open Drain pin: Driving 軟體
	0	Push-pull Pin : Driving 軟體
RTS2-	1	CPU FAN 100%
	0	CPU FAN 50%

SOUT2	1	VID pins threshold voltage select: Vih / Vil : 2.0 / 0.8V
	0	VID pins threshold voltage select: Vih / Vil : 0.8 / 0.4V

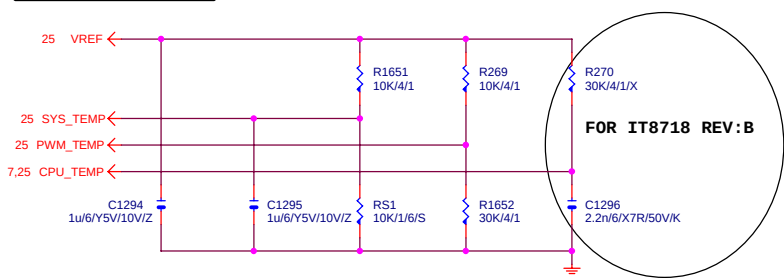
```
1.2V or 3.3V tolerance select.  
1.2V OUTPUT 接 VTT_GMCH  
3.3V OUTPUT 接3.3V  
LPCPD#=VIDVCC
```

VCC3 R1946 0/4/SHT/X VIDVCC
VTT_GMCH R1947 0/4/X

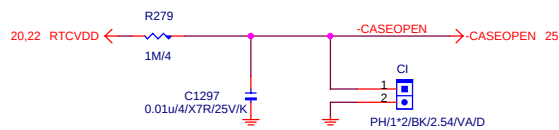
VTT_GMCH/VCC3/VIDVCC 請走20~30

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ITE 8712 LPC IO			
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TEMP H/W MONITOR

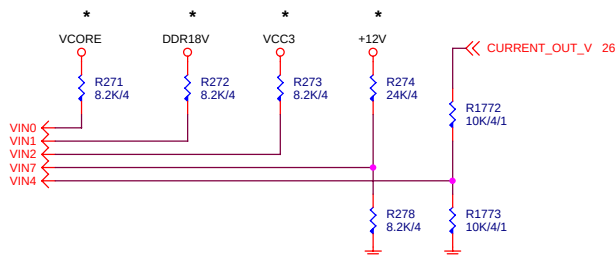


CASE OPEN

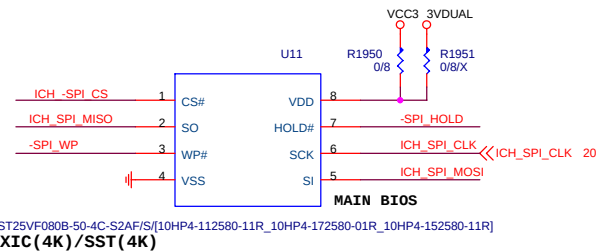
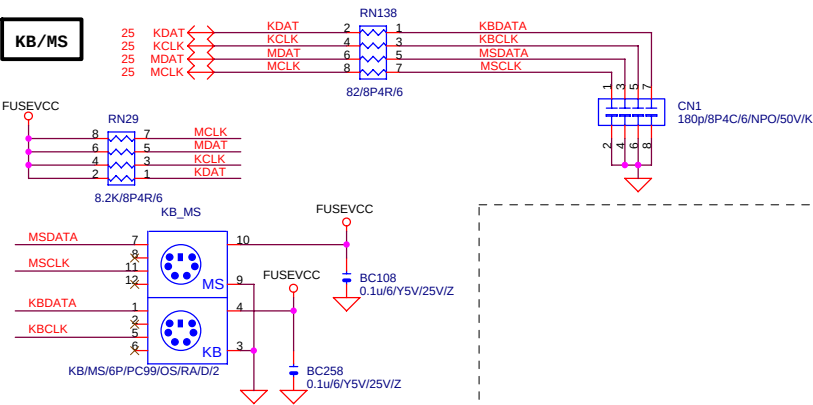


Case Open Circuits

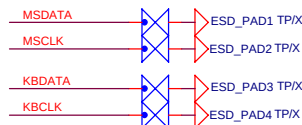
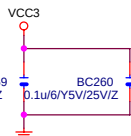
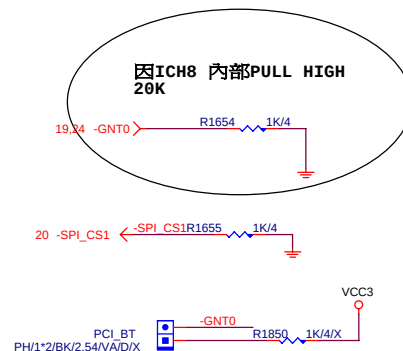
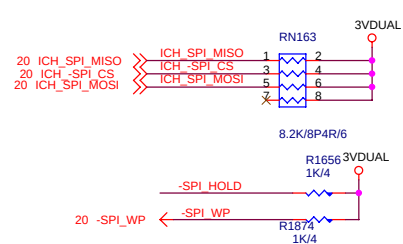
VOLTAGE-- H/W MONITOR



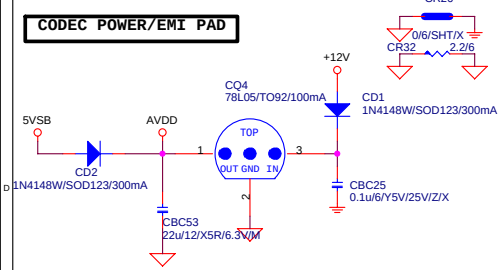
KB/MS



BOOT DEVICE	GNT0	CS1
SPI	0	X
PCI	1	0
FWH	1	1

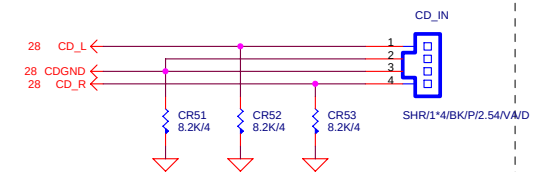


CODEC POWER/EMI PAD

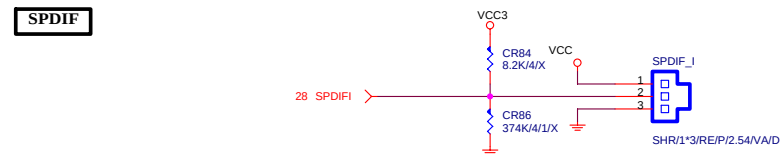


CO-LAYOUT

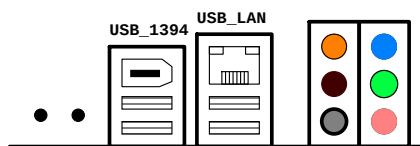
CD IN



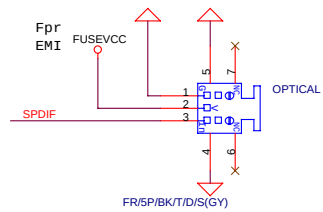
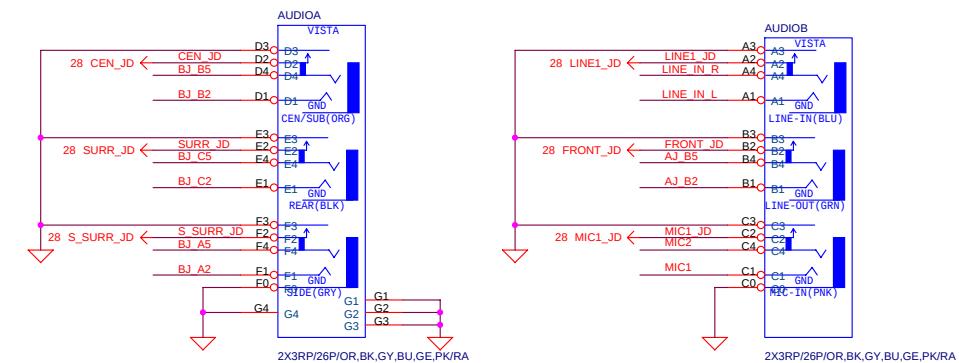
SPDIF



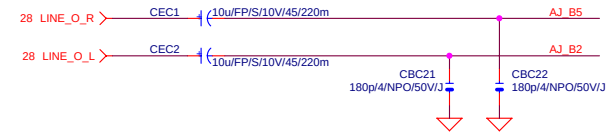
AZALIA JACK



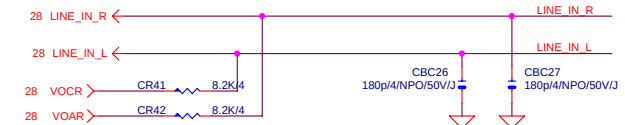
3RP/26P/OR, BK, GY, BU, GE, PK/RA/D/1/B
VISTA規範: REAR-->BLK, CEN/SUB-->ORG



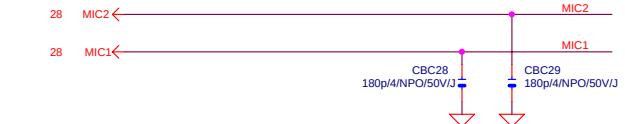
LINE-OUT



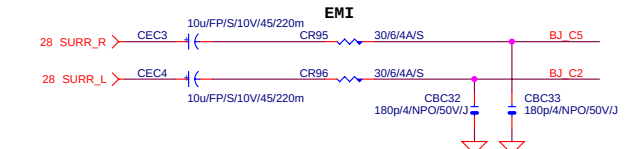
LINE-IN



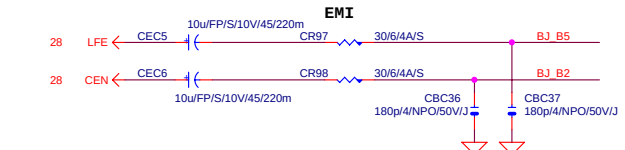
MIC-IN



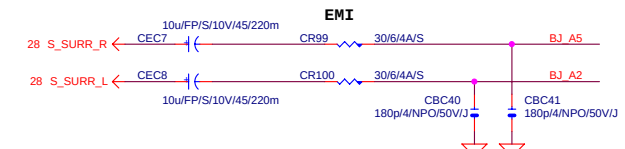
SURROUND



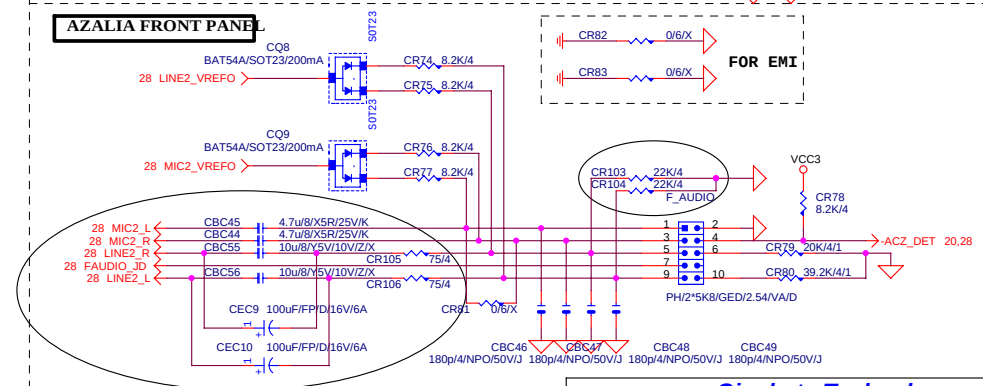
CEN/LFE



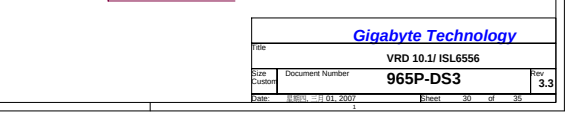
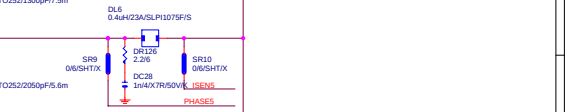
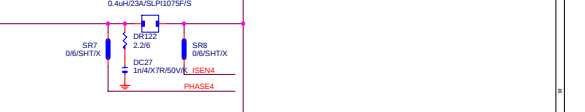
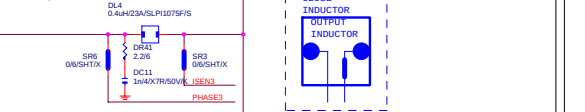
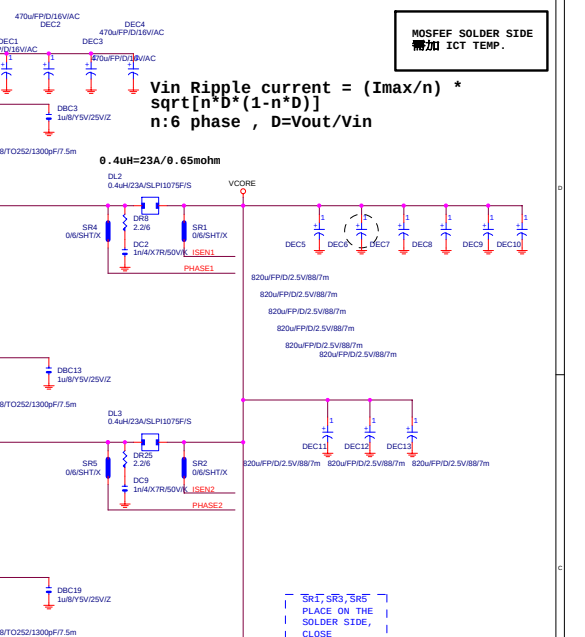
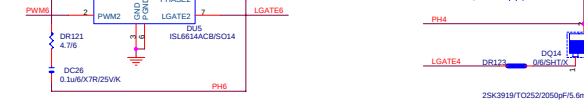
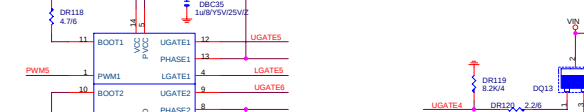
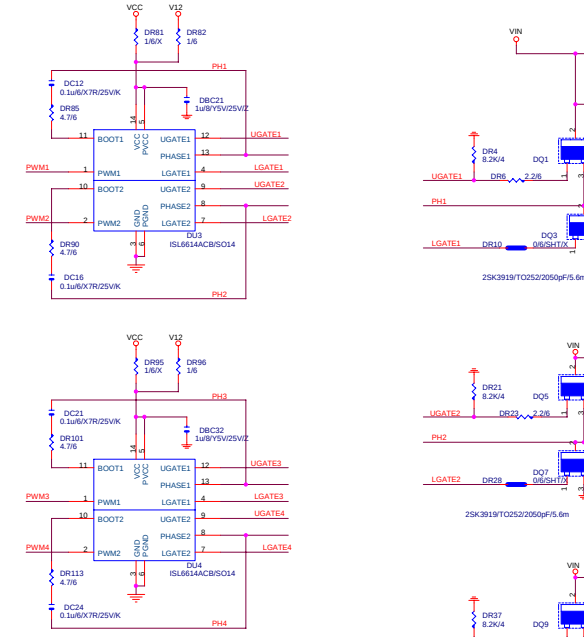
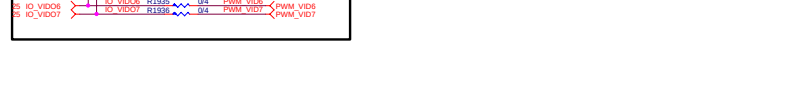
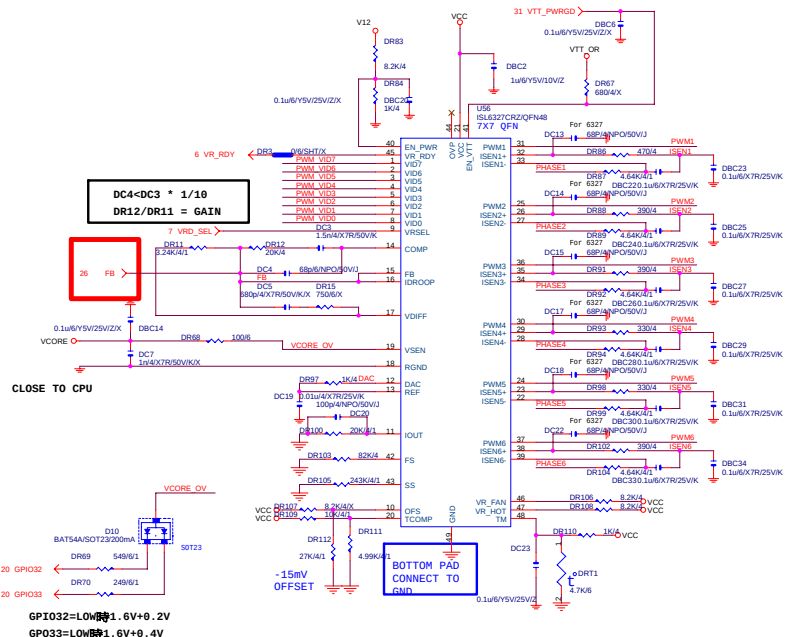
SURR BACK



AZALIA FRONT PANEL



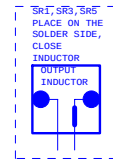
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AUDIO JACK		
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Custom		
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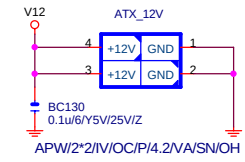
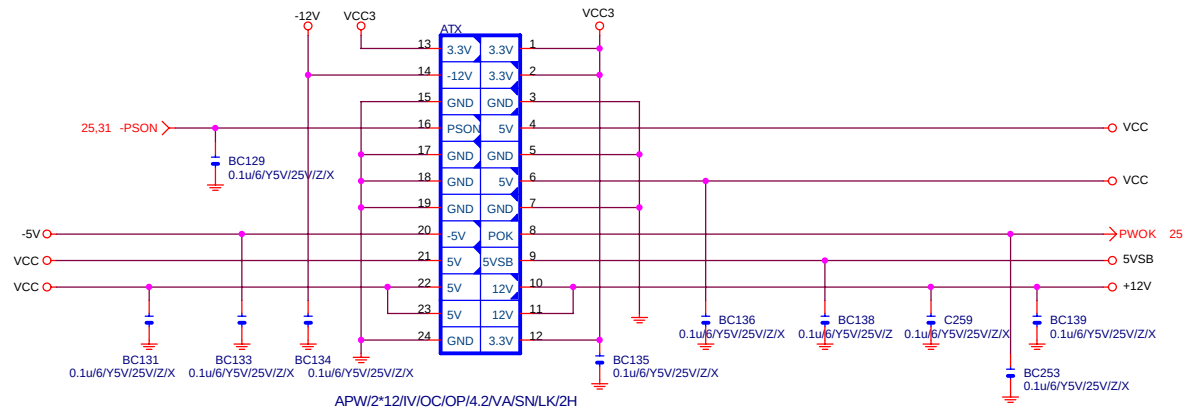
$$V_{in} \text{ Ripple current} = (I_{max}/n) \cdot \sqrt{n \cdot D \cdot (1 - n \cdot D)}$$

$$n: 6 \text{ phase}, D = V_{out}/V_{in}$$

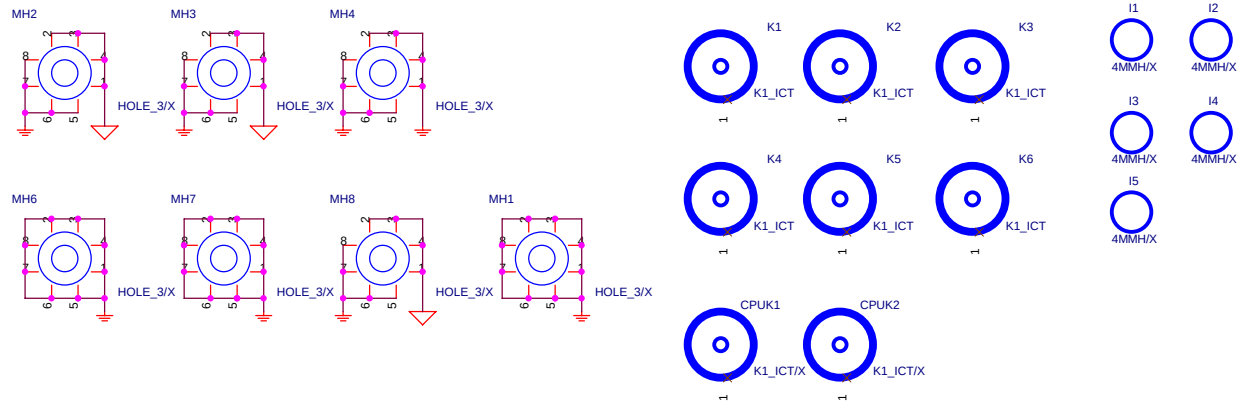
MOSFET SOLDER SIDE
需加 ICT TEMP.



ATX POWER CONNECTOR



HOLE_3-2--->有鉛

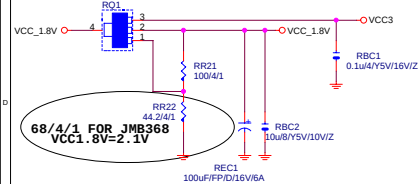


Gigabyte Technology

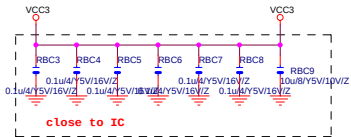
Title			
ATX POWER CONNECTOR			
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3.3V to 1.8V Voltage Regulator

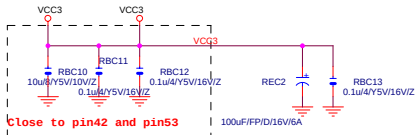
AMC11175SOT23/0.8A



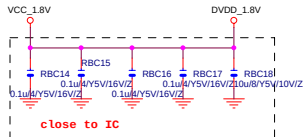
68/4/1 FOR JMB368
VCC1.8V=2.1V



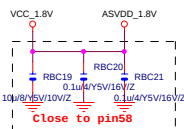
close to IC



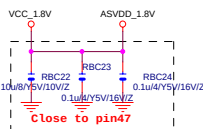
close to pin42 and pin53



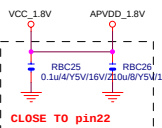
close to IC



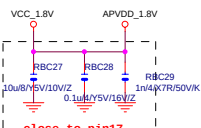
close to pin58



close to pin47

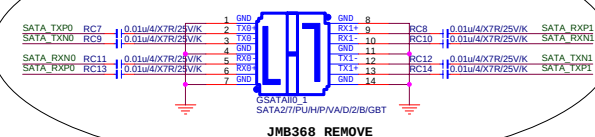


CLOSE TO pin22

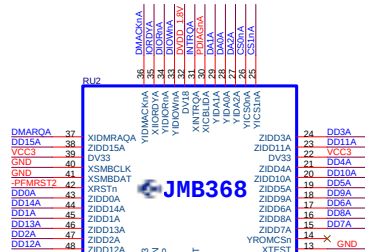


close to pin17

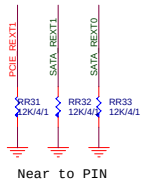
SATA Connector



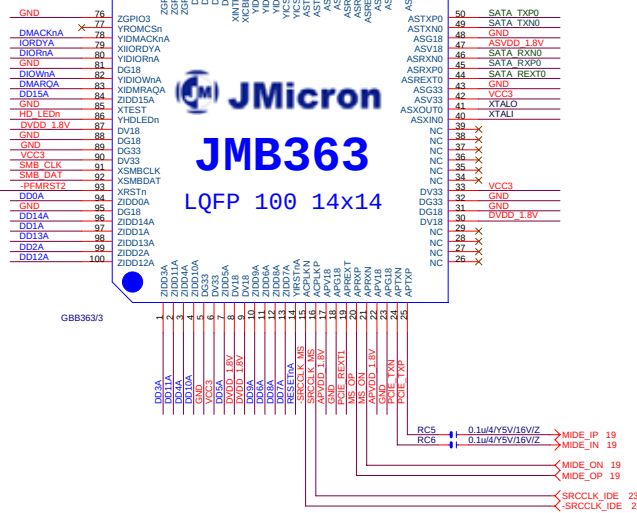
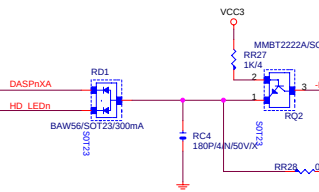
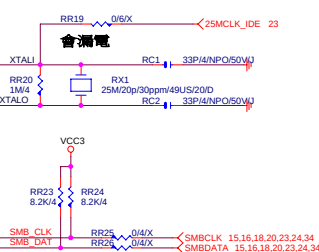
JMB368 REMOVE



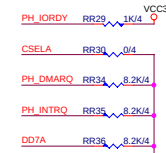
JMB368LQFP40X



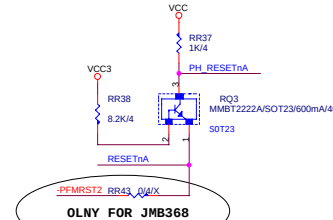
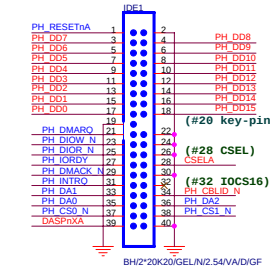
Near to PIN



JMicron
JMB363
LQFP 100 14x14



IDE Connector



OLN FOR JMB368

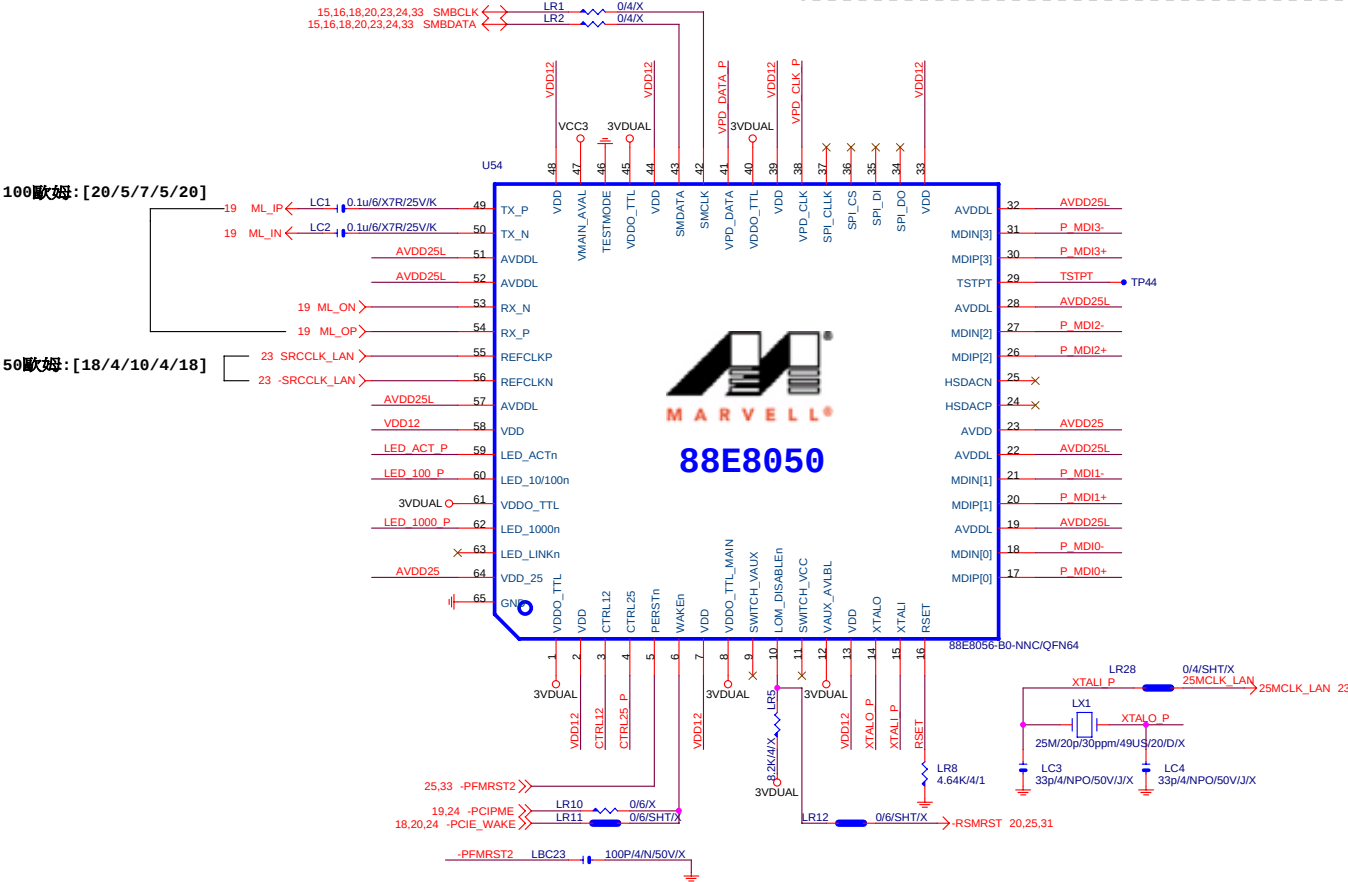
Gigabyte Technology

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PCIE-1G LAN

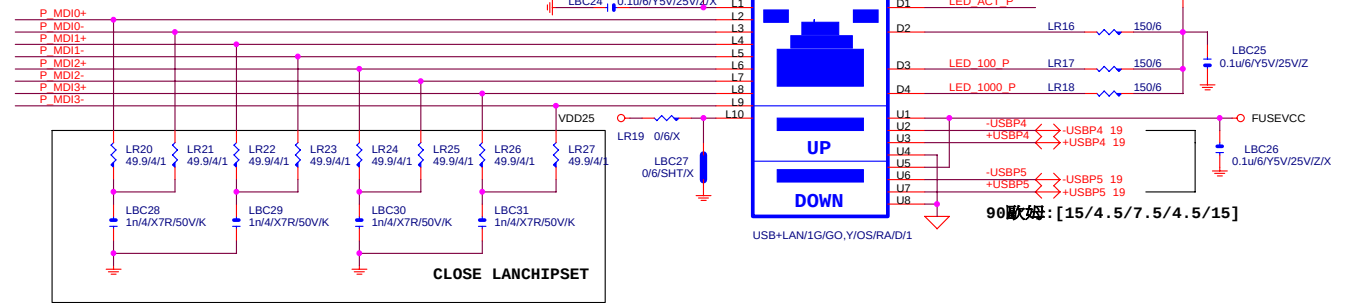
Layout check 注意事項

1. LUI1 PIN65 需下內層GND, 打 12 V1A
2. 3VDDUAL, VCC3, VDD15_L, AVDD25_L
至少走20mil寬, 並且電容擺設每兩pin至少放一顆Bypass Cap.
3. X1'TAL 25MHz 兩訊號線, TRACE 愈短愈好, 線寬12mil
4. MDI正負0-3, TRACE 8:7:8, 每對之間保持 40mil

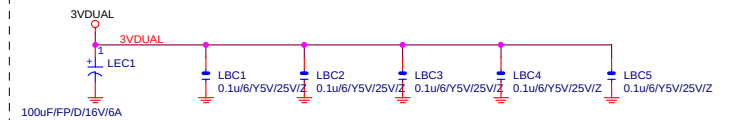


USB_LAN CONNECTOR

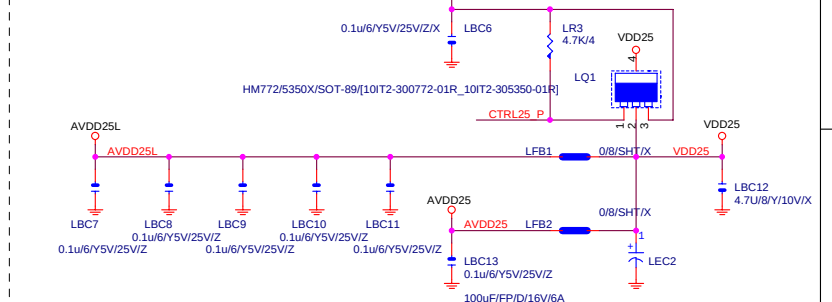
LAN 100 欧姆:[30/4/8/4/30] FOR B 製程



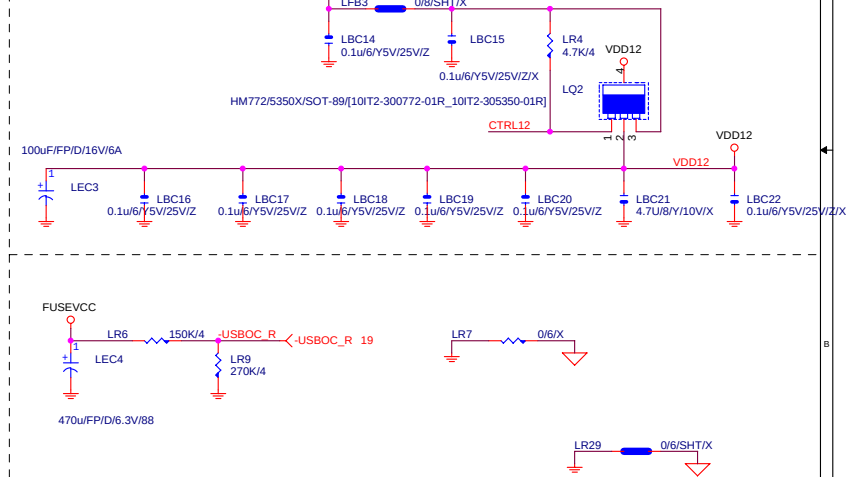
3VDUAL



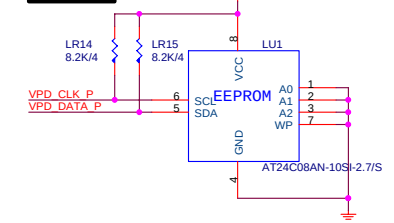
2.5V



1.2V



EEPROM

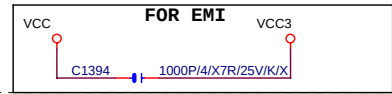
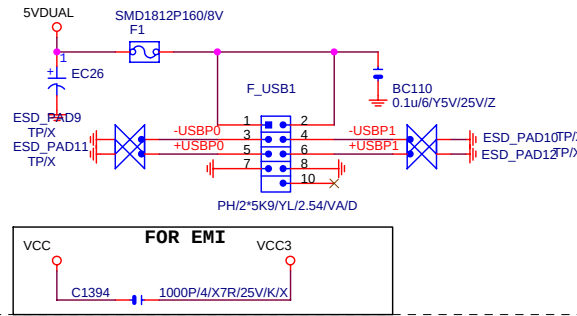


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FRONT USB1

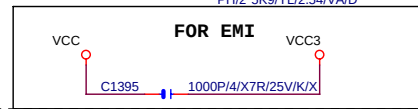
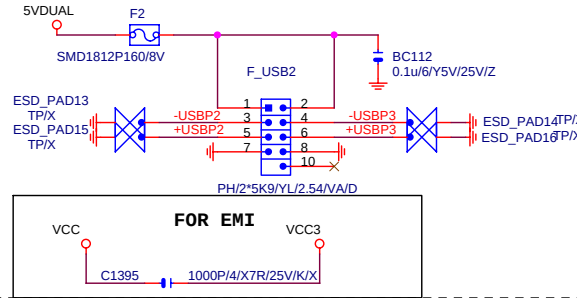
19 +USBP0 <-> +USBP0
19 -USBP0 <-> -USBP0
19 +USBP1 <-> +USBP1
19 -USBP1 <-> -USBP1

470uF/FP/D/6.3V/88



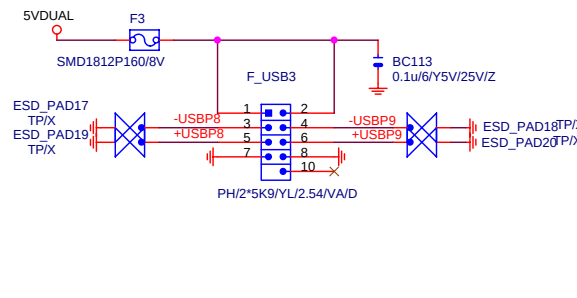
FRONT USB2

19 +USBP2 <-> +USBP2
19 -USBP2 <-> -USBP2
19 +USBP3 <-> +USBP3
19 -USBP3 <-> -USBP3

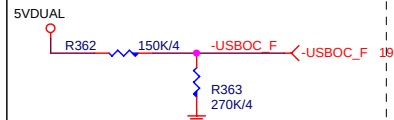


FRONT USB3

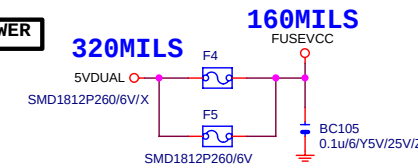
19 -USBP9 <-> -USBP9
19 +USBP9 <-> +USBP9
19 -USBP8 <-> -USBP8
19 +USBP8 <-> +USBP8



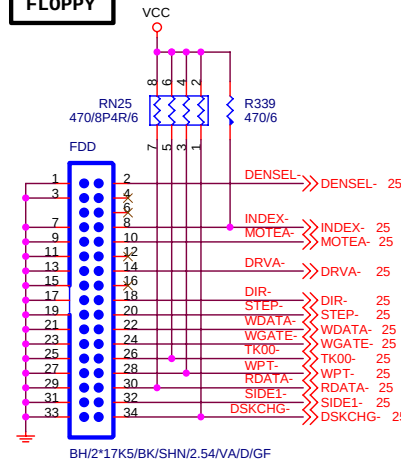
FRONT USB OC1



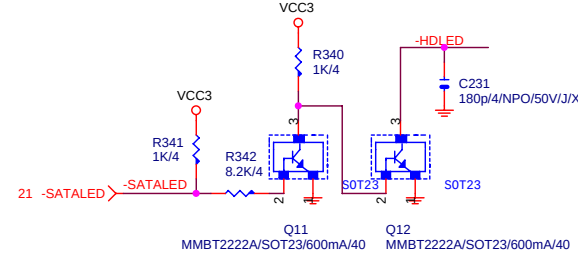
USB POWER



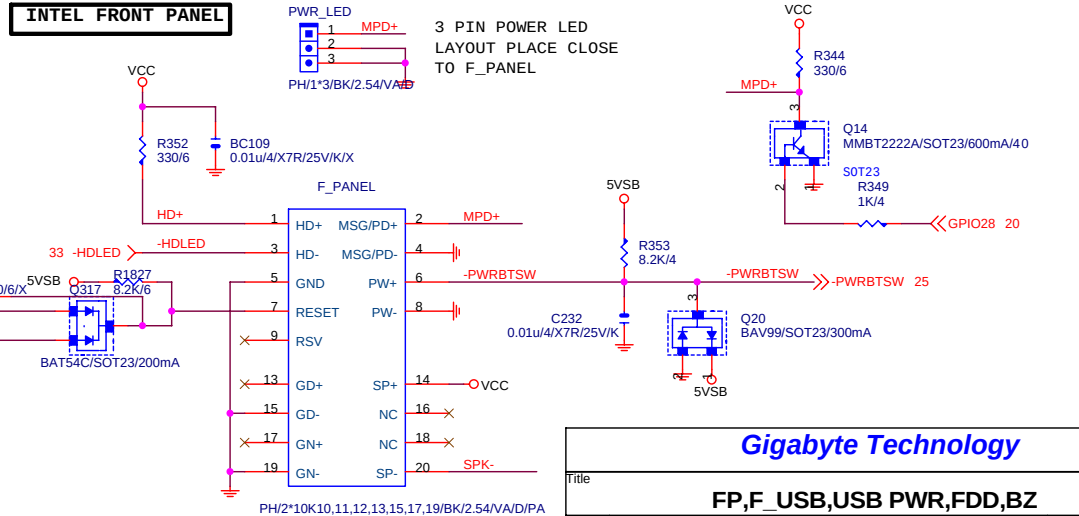
FLOPPY



SATA LED



INTEL FRONT PANEL



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Title			
FP,F_USB,USB PWR,FDD,BZ			
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Custom			
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