Model Name: 965P-S3

Revision 3.3

SHEET	TITLE
01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	POWER MAP
05	P4_LGA775_A
06	P4_LGA775_B
07	P4_LGA775_C
08	P4_LGA775_D
09	GMCH-BROADWATER_HOST
10	GMCH-BROADWATER_DDRII
11	GMCH-BROADWATER_PCI E, DMI
12	GMCH-BROADWATER_INT VGA
13	GMCH-BROADWATER_GND
14	GMCH-BROADWATER_PWR
15	DDRII CHANNEL A 1,2
16	DDRII CHANNEL B 1,2
17	DDRII TERMINATION
18	PCI EXPRESS*16 SLOT
19	ICH8 PCI, USB, DMI, LAN
20	ICH8 GPIO, CTRL
21	ICH8 SATA, FAN PWM
22	ICH8 VCC, GND
23	CLOCK GEN CK505
24	PCI EXPRESS*1 ,PCI SLOT 1,2
25	ITE8712GB,RESET DRIVE
26	COM,LPT
27	BIOS,CI,HWM,KB/MS

SHEET	TITLE
28	AZALIA ALC883
29	AUDIO JACK
30	VCORE PWM ISL6312
31	DISCRETE POWER
32	ATX POWER
33	IDE RAID IT8212
34	1394 TI TSB43AB23
35	LAN MARVELL 88E8053
36	FAN CONTROL
37	FRONT PANEL,FUSB,FDD

Gigabyte Technology

Title: Cover Sheet		
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Component value change history

Data	Change Item	Reason
1.1A	EVT release	
1.1B	1. ADD F_AUDIO HEADPHONE FOR VISTA CR103~CR106	
2.0A	1. DVT RELEASE	
2.0B	1. SB, N/B HEATSINK CHANGE	
	2. 包材修改	
	3. PWM 阻值修改	
	4. 電阻,電容種類統一化	
	5. EC174 560uF -- >100uF	
	6. U11 加替料 WINBOND 8M FLASH:10HP4-152580-11R	
	7. USB_LAN1 加替料 UDE:11NR6-702009-09R	
	8. U49替料移除:CLK GEN ICS9LPRS587BGLF-T	
2.0C	1. 1.2uH修改料號:1.2uH/20A/PMU109/W/D	
	2. N/B , S/B HEATSINK順序修改 (965P-DS3/965G-DS3 Silent-pipe , 965P-S3 New Heatsink)	
	3 .Q330,Q331 Q_SOT23 Remove to Q330 Q_TO252	
	4 .R1955~R1958 R0402-2-SHORT10 to R0402-2	
	5. R1970 1K/4 --> 100/4/1	
	6. ADD PECI CTRL CIRCUIT	
	7. F1,F2,F3 SMD FUSE 1.1A --> 1.6A	
	8. PCB REV2.01 --> REV2.02	
2.0C-PVT	1. 包材修改	
2.0D-DVT	1. PCB REV2.02 --> REV2.03	
2.0E	1. DL2~DL7 0.3uH --> 0.4uH	
	2. DR11 3.16K/4/1 --> 3.24K/4/1	
	3. PWM FS CHANGE 200KHz DR103 82K/4 --> 120K/4	
	4. DDRVTT CHANGE R1882 1.78K/6/1 REMOVE , ADD 1876 1K/6/1	
	5. DDR18V_OV3 4.02K/6/1 --> 3.01K/6/1	
2.0E-ECN	3. PWM FS CHANGE 200KHz DR103 120K/4 --> 82K/4	
2.0F	1. PCB REV2.02 --> REV2.03	
2.0G	1. 0.4uH修改料號	
	2. DR105 加替料10RC4-002433-23R	
	3. 主料10CM2-024704-51R,加替料10CM2-024704-53R	

Circuit or PCB layout change for next version

DATE	Change Item	Reason
1.02	EVT release	
2.0	1. PWM 3 PHASE --> 6 PHASE	
	2. SUPPORT VISTA FUNCTION	
	3. APPROVE POWER-ON SHUN DOWN ISSUE	
2.01	1. REMOVE CQ10,CR101,CR102	
	2. PWR_FAN R1814 VCC --> +12V	
	3. PWM 6 PHASE COPY FROM 946GZ-S3 Rev2.0	
	4. U11 FOOTPRINT IC8SO-SOCKET-1 --> IC8SO-SOCKET-2	
	5. EC174 EC10D8MM --> EC6D8MM,BC730 C0603 --> C0805	
2.02	1 .Q330,Q331 Q_SOT23 Remove a Q330 Q_TO252	
	2 .R1955~R1958 R0402-2-SHORT10 a R0402-2	
	3. ADD CPU PIN.E7=CPU_TP21	
	4. L15,L16 Footprint change to "CHOKE2U-20A-SQ-1"	
	5. CHANGE PECI CTRL CIRCUIT	
2.03	1. RU2 PIN40,41 NET CHANGE TO GND	
2.04	1. L13,L14 1.2uH Change Footprint "CHOKE08U-15A_1P-1"	
	2. L15,L15 2uH Change Footprint "CHOKE2U-20A-SQ-2"	
BOM		
2.0H	1. PCB REV2.03 --> REV 2.04	
	2. 470uF/6.3V & 560uF/4V --> 560uF/6.3V(僅試產,量產版本要改回來)	
	3. D3,D9,CD1,CD2,PD1 10DS1-124148-04R/05R--> 10DS7-734148-01R/02R (僅試產,量產版本要改回來)	
	4. U54 M8056/A2 --> M8056/B0	
3.3A	1. FOR FSB1333 CPU SUPPORT	
	BOM要再建立9M965PS3-00-33A	

Gigabyte Technology

Title: BOM & PCB MODIFY HISTORY

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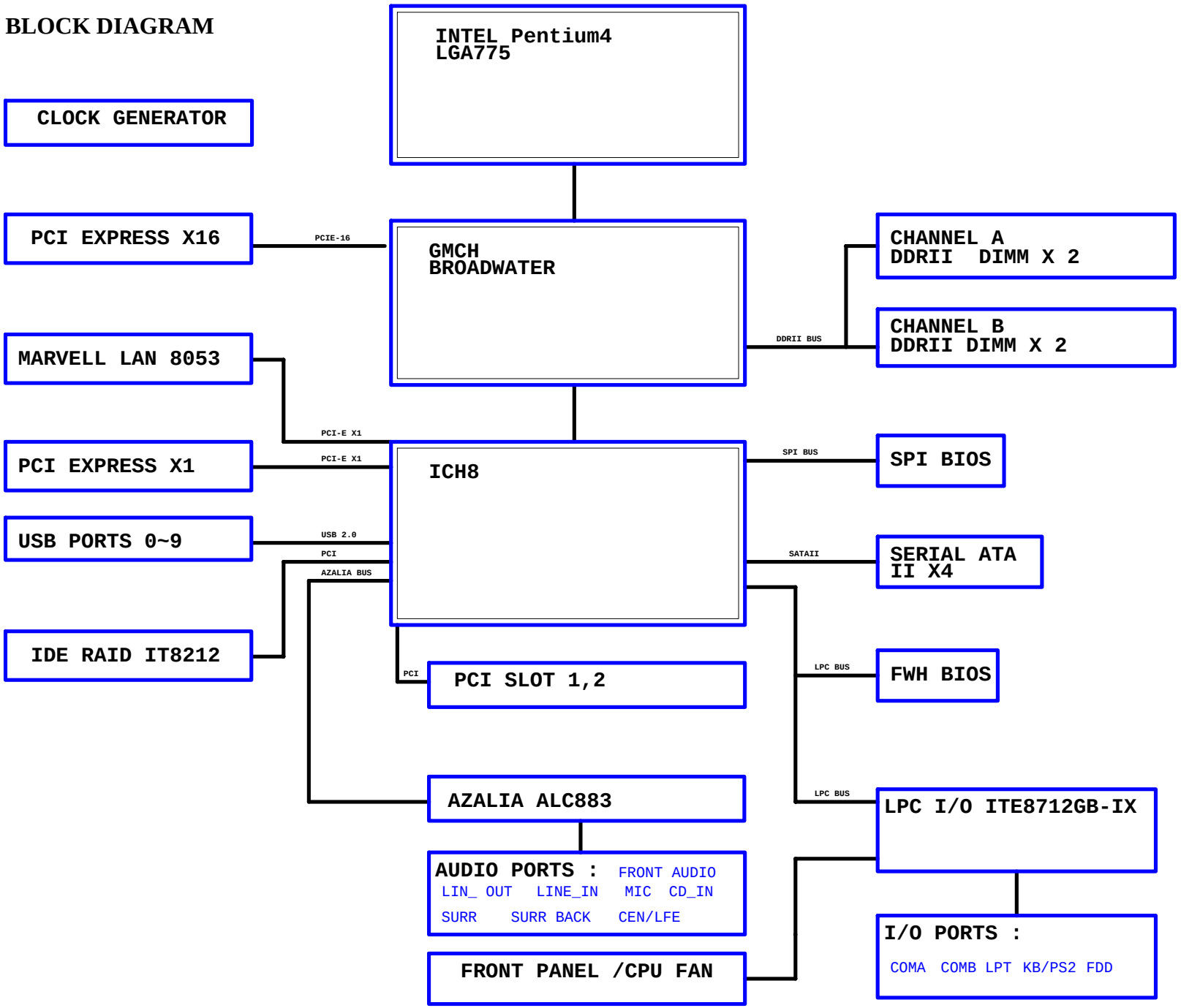
BLOCK DIAGRAM



Gigabyte Technology

Title	BLOCK DIAGRAM	
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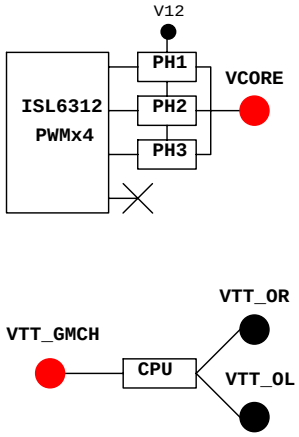
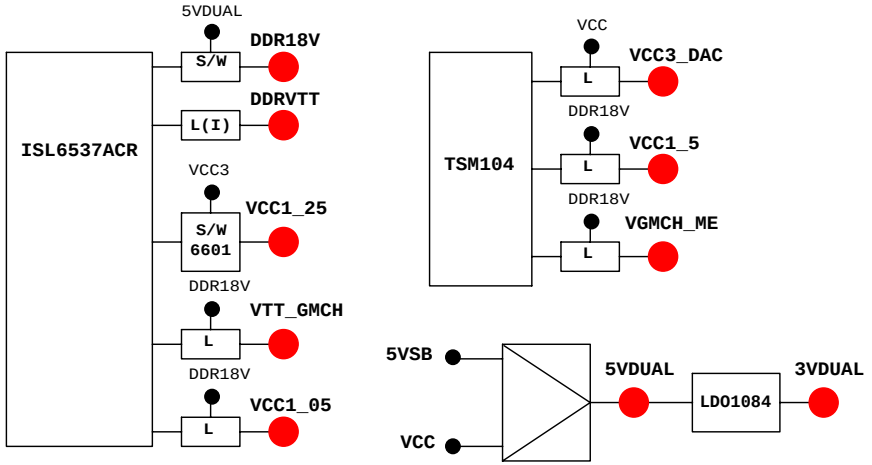
ICH8 GPIO LIST TABLE

PIN NAME	PWR WELL	AFTER/ PLTRST	USAGE	NOTE
GP0	MAIN	IN	-ACZ_DET	P/U 8.2K VCC3
GP1/TACH1	MAIN	IN	ICH_FAN_TACH1	P/U 8.2K VCC3
GP2/PIRQE#	MAIN	IN	-PIRQE	P/U 8.2K VCC3
GP3/PIRQF#	MAIN	IN	-PIRQF	P/U 8.2K VCC3
GP4/PIRQG#	MAIN	IN	-PIRQG	P/U 8.2K VCC3
GP5/PIRQH#	MAIN	IN	-PIRQH	P/U 8.2K VCC3
GP6/TACH2	MAIN	IN	ICH_FAN_TACH2	P/U 8.2K VCC3
GP7/TACH3	MAIN	IN	ICH_FAN_TACH3	P/U 8.2K VCC3
GP8	STBY	IN	GPIO8(DUALBIOS_INPUT)	P/U 8.2K 3VDUAL
GP9	STBY	OUT	WOL_ONLY	P/D 100K GND
GP10	STBY	IN	CLGPIO1	P/U 8.2K 3VDUAL
GP11/SMBALERT#	STBY	OUT	-SMBALRT	P/U 8.2K 3VDUAL
GP12	STBY	IN	MB_ID0	P/U 8.2K 3VDUAL
GP13	STBY	IN	-LPCPME	P/U 8.2K 3VDUAL
GP14	STBY	IN	CLGPIO2	P/U 8.2K 3VDUAL
GP15	STBY	OUT	LAN_DISABLE(STP_PCI-)	N/A
GP16	MAIN	OUT/LOW	RESET	N/A
GP17/TACH0	MAIN	IN	ICH_FAN_TACH0	P/U 8.2K VCC3
GP18	MAIN	OUT	MB_ID1	P/U 8.2K VCC3
GP19	MAIN	IN	SATA1GP	P/U 8.2K VCC3
GP20	MAIN	OUT	-SPI_WP0	P/U 1K 3VCL
GP21	MAIN	IN	SATA0GP	P/U 8.2K VCC3
GP22	MAIN	IN	SCLOCK	P/U 8.2K VCC3
GP23	MAIN	OUT	-LDRQ1	P/U 8.2K VCC3
GP24	STBY	OUT	CLGPIO0	P/U 8.2K 3VDUAL
GP25	STBY	IN	MB_ID2(STP_CPU-)	P/U 8.2K 3VDUAL
GP26/S4_STATE#	STBY	OUT	S4_STATE#	P/U 8.2K 3VDUAL
GP27	STBY	OUT/LOW	GPIO27(EL_STATE0)	P/U 8.2K 3VDUAL
GP28	STBY	OUT/LOW	PWR_LED(EL_STATE1)	N/A
GP29/OC5#	STBY	IN	-USBOC_R	P/U FUSEVCC
GP30/OC6#	STBY	IN	-USBOC_R	P/U FUSEVCC
GP31/OC7#	STBY	IN	-USBOC_R	P/U FUSEVCC
GP32	MAIN	OUT	DUAL_BIOS	P/U 100K+1M VCC3
GP33	MAIN	OUT	DUAL_BIOS	P/U 8.2K VCC3
GP34	MAIN	OUT/LOW	GPIO34/SMB_RST	N/A
GP35	MAIN	OUT	SATACLKREQ#	N/A
GP36	MAIN	IN	SATA2GP	P/U 8.2K VCC3
GP37	MAIN	IN	SATA3GP	P/U 8.2K VCC3
GP38	MAIN	IN	SLOAD	P/U 8.2K VCC3
GP39	MAIN	IN	GPIO39	P/D 8.2K GND
GP48	MAIN	IN	GPIO48	P/U 8.2K VCC3
GP49	MAIN	IN	CPUPWROK	P/U 100 VTT_OL

VCORE:3 PHASE PWM--ISL6312





Gigabyte Technology		
Title: TABLE LIST		
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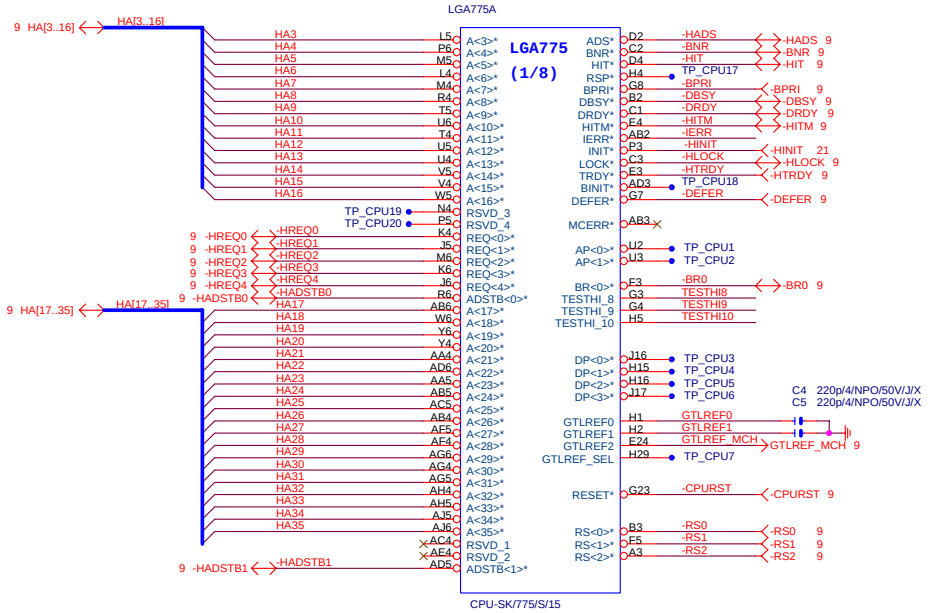
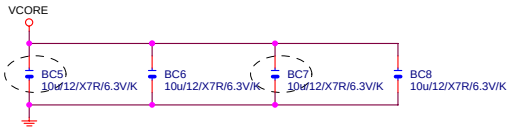
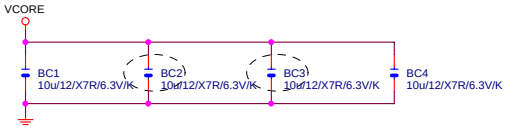
HA/REQ:4/14

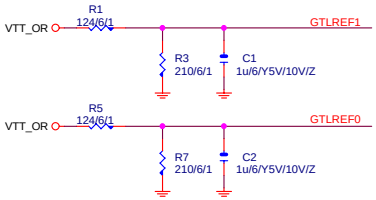
ADSTB:4/17

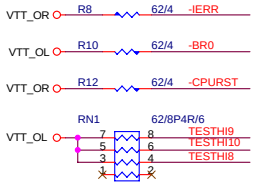


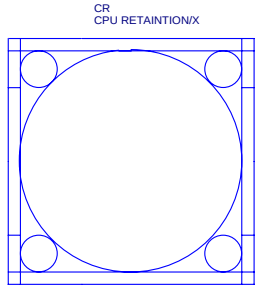
Impedance=50 +- 15% for 4 -layer











Gigabyte Technology		
Title: **P4_LGA775-A**		
Size: Custom	Document Number: **965P-DS3**	Rev: **3.3**
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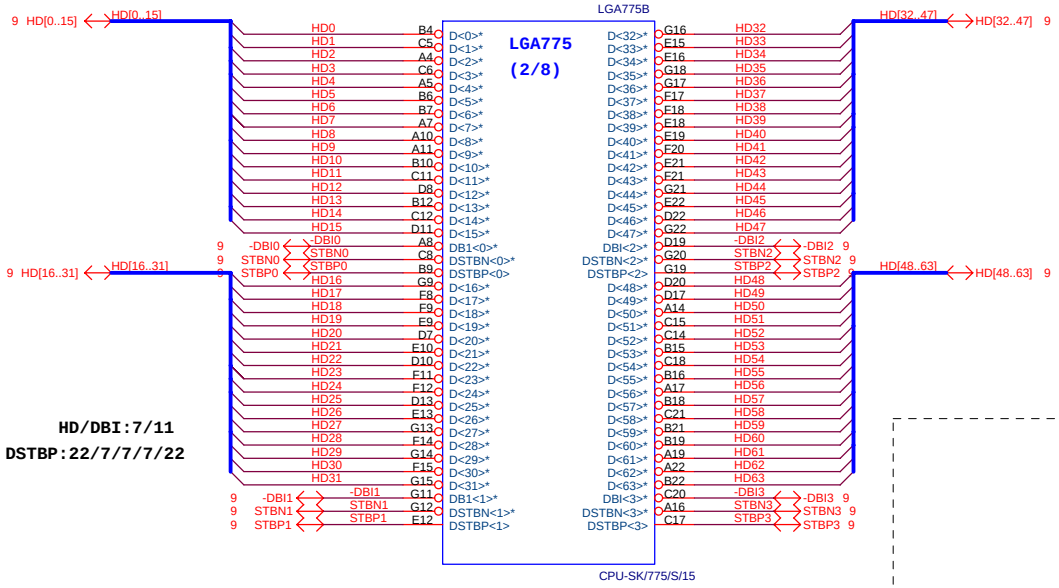

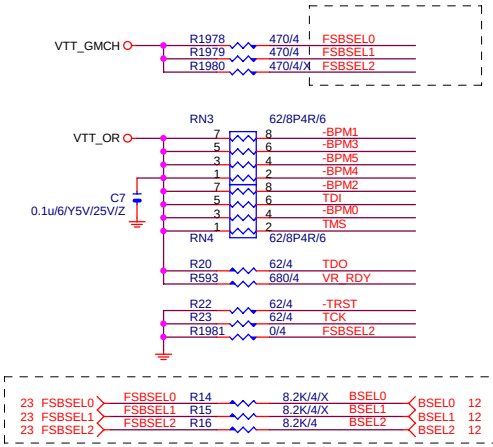

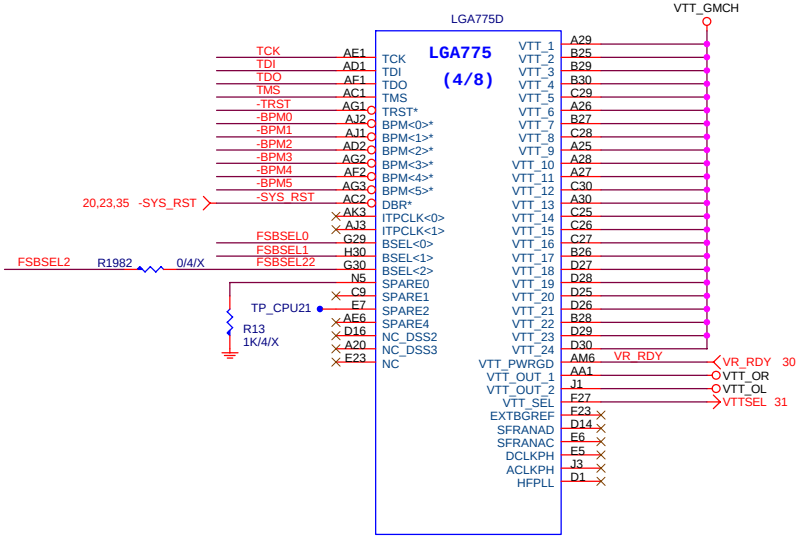

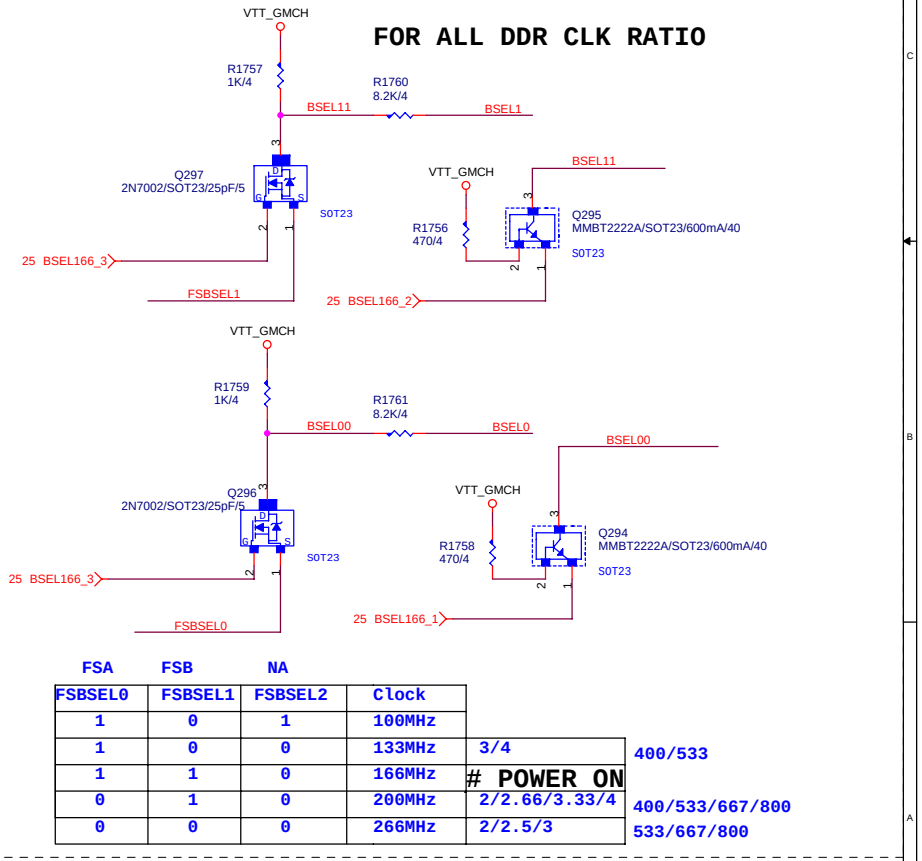

FSA	FSB	NA			
FSBSEL0	FSBSEL1	FSBSEL2	Clock		
1	0	1	100MHz		
1	0	0	133MHz	3/4	400/533
1	1	0	166MHz	# POWER ON	
0	1	0	200MHz	2/2.66/3.33/4	400/533/667/800
0	0	0	266MHz	2/2.5/3	533/667/800

Gigabyte Technology			
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Note:

VCCA & VCOREPLL define doesn't same as old P4 design kit

Trace width doesn't less than 12 Mil

As close as possible to CPU socket

VTT_GMCH L1 10UH/8/S/[10LI2-12100A-13R_10LI2-12100A-02R]

C10 1u/6/Y5V/10V/Z

C11 1u/6/Y5V/10V/Z

L2 10UH/8/S/[10LI2-12100A-13R_10LI2-12100A-02R]

VCCA — R35 0/6/SHT/X — VSSA — VCOREPLL

LGA775C

LGA775 (3/8)

CPU-SK/775/S/15

-STPCLK — C14 33p/4/NPO/50V/J/X

VID[0..7] — 30 VID[0..7]

30 VRD_SEL — VRD_SEL

23 CPUCLK — CPUCLK

23 -CPUCLK — -CPUCLK

-SKTOCC — SKTOCC*

25,27 CPU_TEMP — R44 0/4/SHT/X

25 THERMDC — R45 0/4/SHT/X

C1282 1n/4/X7R/50V/K/X

C15 1n/4/X7R/50V/K/X

BC722 22u/12/X5R/6.3V/M

26 VCC_SENSE

26 VSS_SENSE

VCORE

TP_CPU11 — R56 62/4 — F6

TP_CPU14 — G6

TP_CPU16 — G5

21,25 PECI — AL3

21 -SMI	-SMI	P2	SMI*
21 -A20M	-A20M	K3	A20M*
21 -FERR	-FERR	R3	FERR*/PBE*
21 INTR	INTR	K1	LINT0
21 NMI	NMI	L1	LINT1
21 -IGNNE	-IGNNE	N2	IGNNE*
20,21 -STPCLK	-STPCLK	M3	STPCLK*
	VCCA	A23	VCCA
	VSSA	B23	VSSA
	VCOREPLL	C23	VCCIOPLL
	VCC_PLL	D23	VCC_PLL
	VID0	AM2	VID<0>
	VID1	AL5	VID<1>
	VID2	AM3	VID<2>
	VID3	AL6	VID<3>
	VID4	AK4	VID<4>
	VID5	AL4	VID<5>
	VID6	AM5	VID<6>
	VID7	AM7	VID<7>
	VRD_SEL	AN7	VID_SELECT
	CPUCLK	F28	BCLK<0>
	-CPUCLK	G28	BCLK<1>
	-SKTOCC	AE8	SKTOCC*
		AL1	THERMDA
		AK1	THERMDC
		AJ7	THERMDA_2
		AH7	THERMDC_2
		AN3	VCC_SENSE
		AN4	VSS_SENSE
		AN5	VCC_MB_REGULATION
		AN6	VSS_MB_REGULATION
		AL8	VCC_D_SENSE
		AL7	VSS_D_SENSE
		F29	VTT_PKGSENSE
		F6	Z60_50*
		G6	SLEW_CTRL*
		G5	SST_LV*
		AL3	MPG_NOBOOT*

	TESTHI_0	F26	TESTHI0
	TESTHI_1	W3	TESTHI1
	TESTHI_2	F25	TESTHI2_7
	TESTHI_3	G25	
	TESTHI_4	G27	
	TESTHI_5	G26	
	TESTHI_6	G24	
	TESTHI_7	F24	
	TESTHI_11	P1	TESTHI11
	TESTHI_12	W2	TESTHI12
	TESTHI_13	L2	TESTHI13
	FORCEPH	AK6	-FORCEPR — TESTHI13 21, -FORCEPR 26
	PWRGOOD	N1	CPUPWROK — CPUPWROK 21
	PROCHOT*	AL2	-PROCHOT — -PROCHOT 20,26
	THERMTRIP*	M2	-THRMTRIP — -THRMTRIP 20
	COMP<0>	A13	COMP0
	COMP<1>	T1	COMP1
	COMP<2>	G2	COMP2
	COMP<3>	R1	COMP3
	COMP<4>	J2	COMP4
	COMP<5>	T2	COMP5
	COMP<6>	Y3	COMP6
	COMP<7>	AE3	COMP7
	COMP<8>	B13	COMP8
	RC1	G1	CPU_G1
	RC2	U1	TESTHI_M
	RC4	A24	R666 1K/4/X
	RC5	E29	TP_CPU10
	RSVD_1	F2	GTLREF2
	RSVD_2	G10	GTLREF3
	PSMI*	AH2	
	MSID<1>	V1	MSID1 R53 62/4
	MSID<0>	W1	MSID0 R55 62/4
	CPU_BOOT	Y1	TP_CPU12
	LL_ID<0>	V2	TP_CPU13
	LL_ID<1>	AA2	TP_CPU15

Z60_50*:阻抗60ohm-->不上,
Z60_50*:阻抗50ohm-->上62/4

PECI:Platform Environment Control Interface

Place outside of CPU socket

VTT_OL — R28 49.9/6/1 COMP5; R30 49.9/6/1 COMP4; R31 49.9/6/1 COMP2; R32 49.9/6/1 COMP3; R33 49.9/6/1 COMP0; R34 49.9/6/1 COMP1; C9 0.1u/6/Y5V/25V/Z

VTT_OR — R36 49.9/6/1 COMP6; R37 49.9/6/1 COMP7; R38 24.9/6/1 COMP8; C12 0.1u/6/Y5V/25V/Z

VTT_GMCH — R39 130/4 -PROCHOT; R40 62/4 TESTHI2_7; R41 62/4 -THRMTRIP; R42 62/4 -FERR; R29 62/4 TESTHI0; C8 0.1u/6/Y5V/25V/Z/X

VTT_OL — RN5 62/8P4R/6: TESTHI12, TESTHI1, TESTHI11, TESTHI13; R43 100/4/X CPUPWROK — C13 1n/4/X7R/50V/K/X; R1775 62/4 CPU_G1; R1776 62/4 TESTHI_M

VTT_OR — RN6 680/8P4R/6: VID2, VID0, VID4, VID5; RN7 680/8P4R/6: VID6, VID3, VID7, VID1; R58 1K/4 VRD_SEL; R60 62/4 -FORCEPR

VTT_OR — R667 124/6/1 GTLREF2; R669 210/6/1 — C349 1u/6/Y5V/10V/Z

VTT_OR — R671 124/6/1 GTLREF3; R674 210/6/1 — C351 1u/6/Y5V/10V/Z

VCC1_5 — FB33 0/8/SHT/X — VCC_PLL — VCC_PLL; C17 1u/6/Y5V/10V/Z; C350 0.1u/6/Y5V/25V/Z/X

Gigabyte Technology		
Title: P4_LGA775-C		
Size: B	Document Number: 965P-DS3	Rev: 3.3
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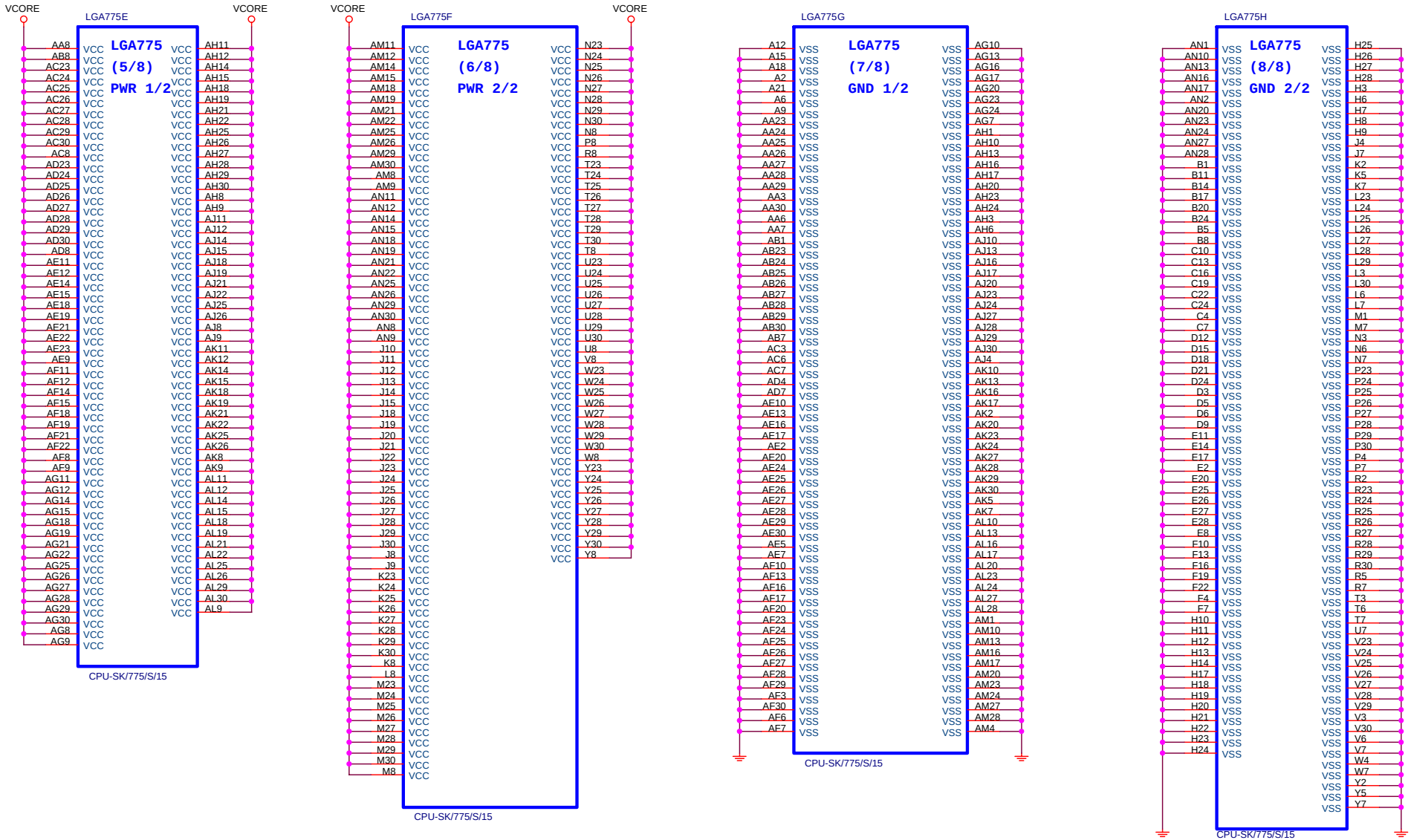

Gigabyte Technology		
Title: P4_LGA775-E,F,G,H		
Size: B	Document Number: 965P-DS3	Rev: 3.3
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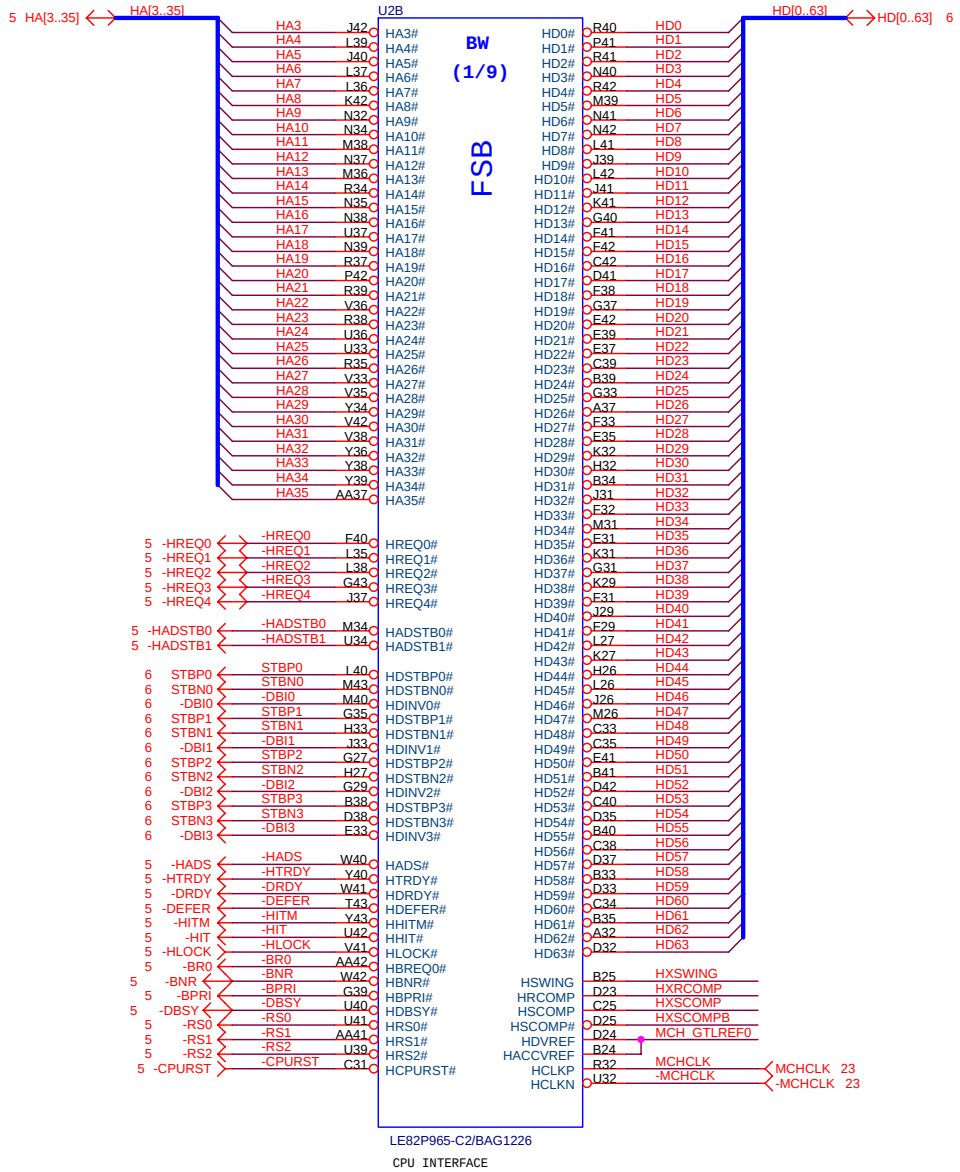

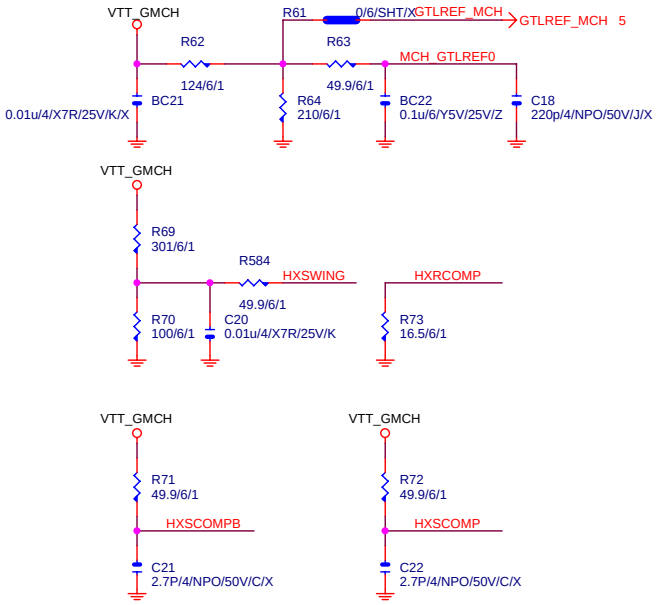

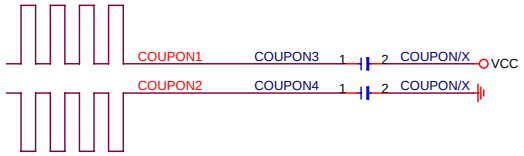

Gigabyte Technology		
Title: GMCH-HOST		
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U2C

BW (3/9)

DDR_0

LE82P965-C2/BAG1226

DDR INTERFACE

U2D

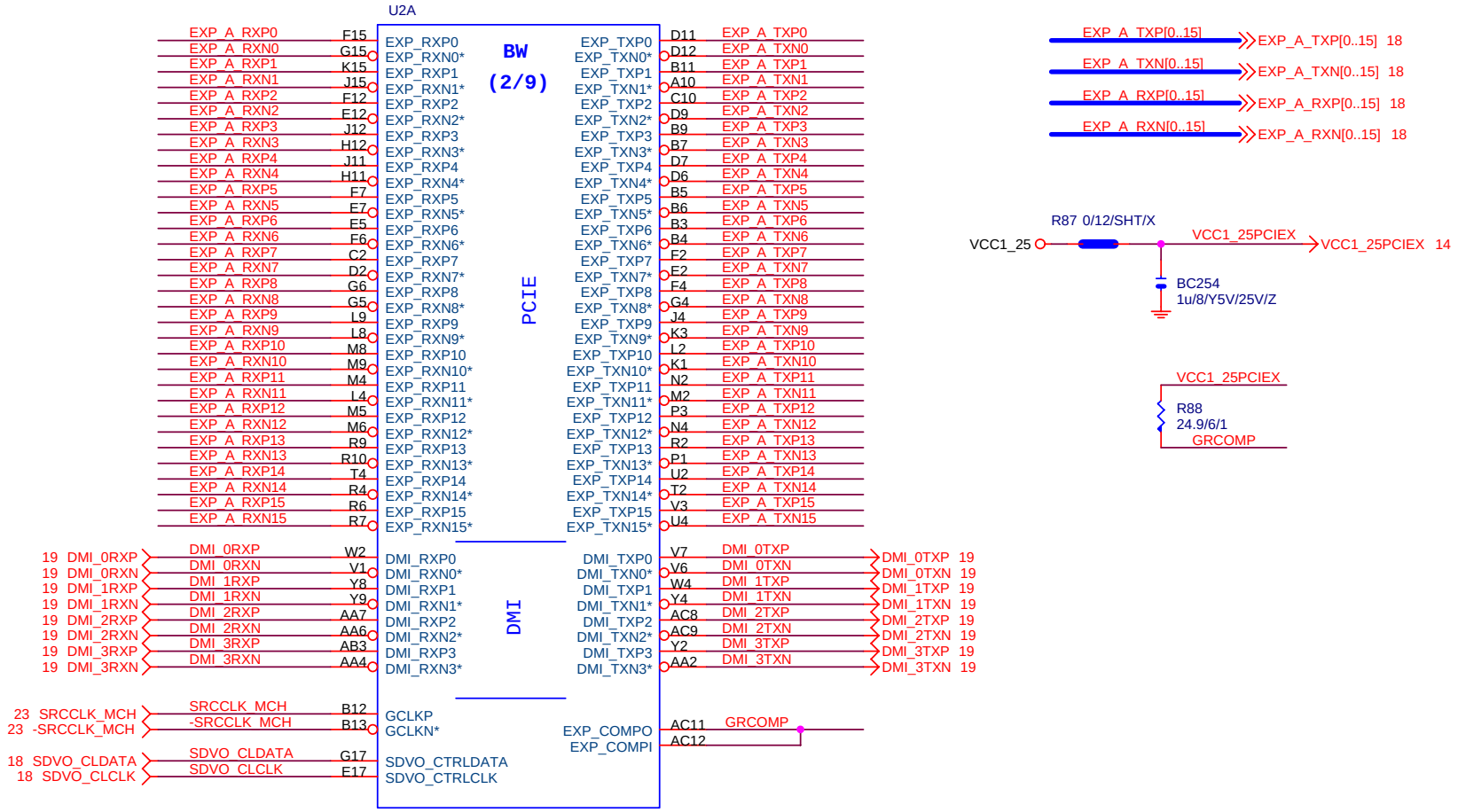
BW (4/9)

DDR_1

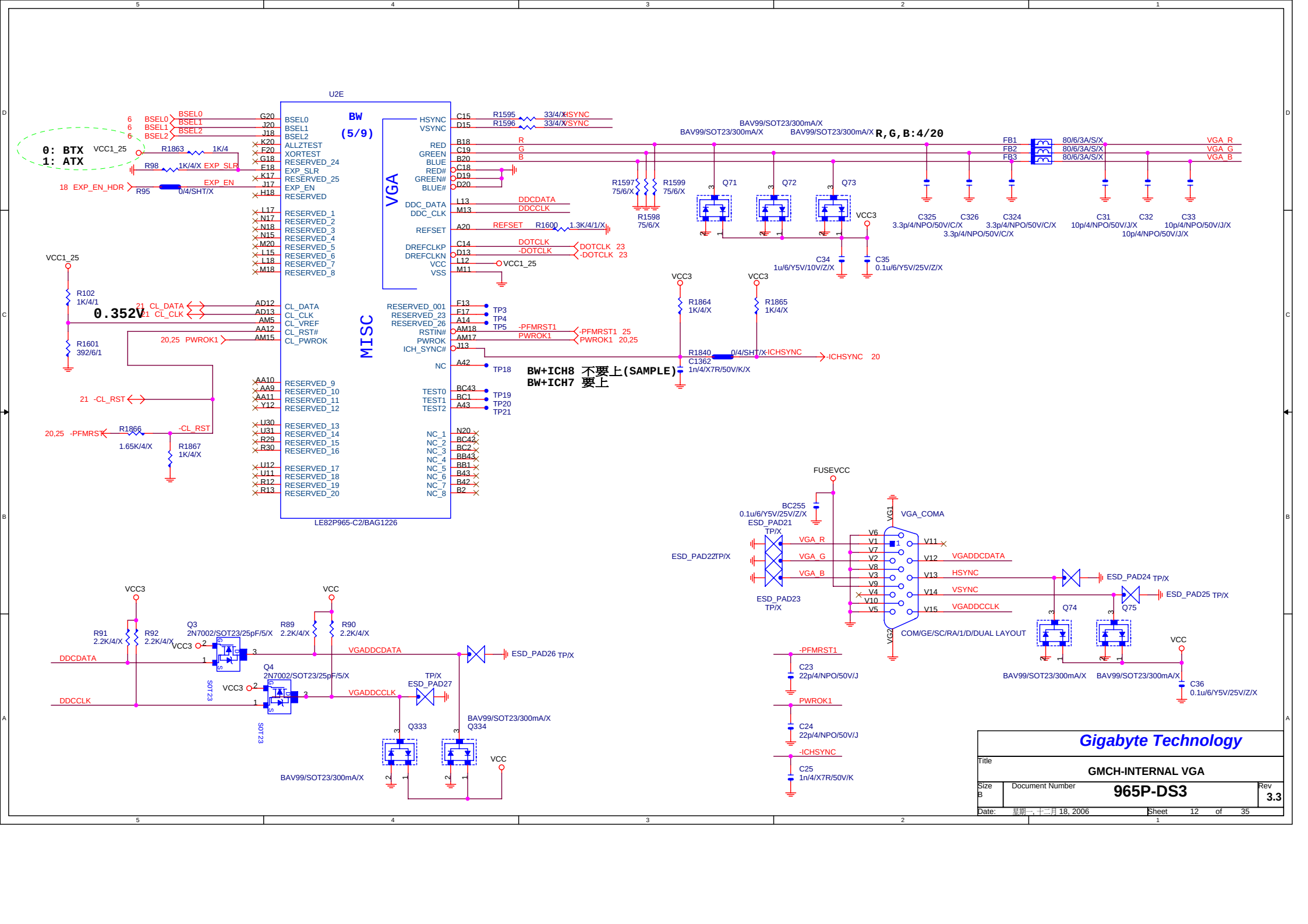
LE82P965-C2/BAG1226

NB_HEATSINK/[12SP2-04F004-71R_12SP2-04F004-72R_12SP2-04F004-73R_12SP2-04F004-74R]

Gigabyte Technology	
Title	GMCH-DDRII
Size: Custom	Document Number: 965P-DS3
Rev	3.3
Date: 星期一, 十二月 18, 2006	Sheet 10 of 35



Gigabyte Technology		
Title: GMCH-PCI E & DMI		
Size: Custom	Document Number: 965P-DS3	Rev: 3.3
Date: 星期一, 十二月 18, 2006	Sheet 11 of 35	


U2E
BW
(5/9)
VGA
MISC
LE82P965-C2/BAG1226
0: BTX
1: ATX
VCC1_25
R1863 1K/4
R98 1K/4/X EXP_SLR
R95 0/4/SHT/X
18 EXP_EN_HDR
EXP_EN
BSEL0
BSEL1
BSEL2
ALLZTEST
XORTEST
RESERVED_24
EXP_SLR
RESERVED_25
EXP_EN
RESERVED
RESERVED_1
RESERVED_2
RESERVED_3
RESERVED_4
RESERVED_5
RESERVED_6
RESERVED_7
RESERVED_8
HSYNC
VSYNC
RED
GREEN
BLUE
RED#
GREEN#
BLUE#
DDC_DATA
DDC_CLK
REFSET
DREFCLKP
DREFCLKN
VCC
VSS
R1595 33/4/X HSYNC
R1596 33/4/X VSYNC
DDCDATA
DDCCLK
R1600 1.3K/4/1/X
DOTCLK 23
-DOTCLK 23
R1597 75/6/X
R1598 75/6/X
R1599 75/6/X
BAV99/SOT23/300mA/X
Q71
Q72
Q73
R,G,B:4/20
FB1
FB2
FB3
80/6/3A/S/X
VGA_R
VGA_G
VGA_B
C325 3.3p/4/NPO/50V/C/X
C326 3.3p/4/NPO/50V/C/X
C324 3.3p/4/NPO/50V/C/X
C31 10p/4/NPO/50V/J/X
C32 10p/4/NPO/50V/J/X
C33 10p/4/NPO/50V/J/X
C34 1u/6/Y5V/10V/Z/X
C35 0.1u/6/Y5V/25V/Z/X
R102 1K/4/1
0.352V
R1601 392/6/1
CL_DATA
CL_CLK
CL_VREF
CL_RST#
CL_PWROK
PWROK1
-CL_RST
R1866 1.65K/4/X
R1867 1K/4/X
-PFMRST
RESERVED_9
RESERVED_10
RESERVED_11
RESERVED_12
RESERVED_13
RESERVED_14
RESERVED_15
RESERVED_16
RESERVED_17
RESERVED_18
RESERVED_19
RESERVED_20
RESERVED_001
RESERVED_23
RESERVED_26
RSTIN#
PWROK
ICH_SYNC#
NC
TEST0
TEST1
TEST2
NC_1
NC_2
NC_3
NC_4
NC_5
NC_6
NC_7
NC_8
TP3
TP4
TP5
TP18
TP19
TP20
TP21
-PFMRST1
PWROK1 20,25
R1864 1K/4/X
R1865 1K/4/X
R1840 0/4/SHT/X
C1362 1n/4/X7R/50V/K/X
-ICHSYNC
-ICHSYNC 20
BW+ICH8 不要上(SAMPLE)
BW+ICH7 要上
FUSEVCC
BC255 0.1u/6/Y5V/25V/Z/X
ESD_PAD21 TP/X
ESD_PAD22TP/X
ESD_PAD23 TP/X
VGA_COMA
COM/GE/SC/RA/1/D/DUAL LAYOUT
VGADDCDATA
HSYNC
VSYNC
VGADDCCLK
ESD_PAD24 TP/X
ESD_PAD25 TP/X
Q74
Q75
BAV99/SOT23/300mA/X
C36 0.1u/6/Y5V/25V/Z/X
C23 22p/4/NPO/50V/J
C24 22p/4/NPO/50V/J
C25 1n/4/X7R/50V/K
R91 2.2K/4/X
R92 2.2K/4/X
Q3 2N7002/SOT23/25pF/5/X
R89 2.2K/4/X
R90 2.2K/4/X
DDCDATA
DDCCLK
VGADDCDATA
VGADDCCLK
ESD_PAD26 TP/X
ESD_PAD27 TP/X
Q4 2N7002/SOT23/25pF/5/X
SOT23
Q333
Q334
BAV99/SOT23/300mA/X
Gigabyte Technology
Title
GMCH-INTERNAL VGA
Size B
Document Number
965P-DS3
Rev 3.3
Date: 星期一, 十二月 18, 2006
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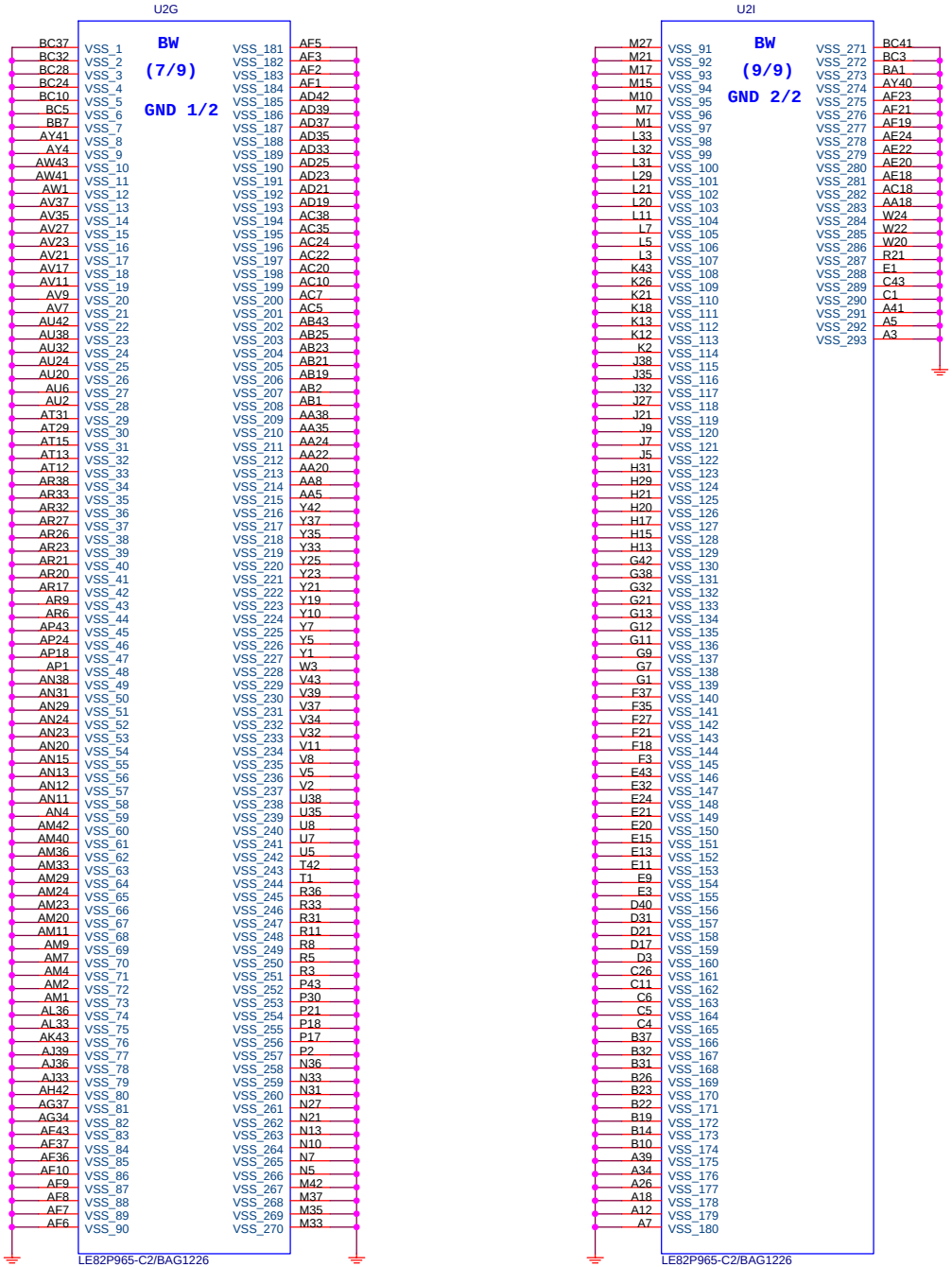

Gigabyte Technology

Title	GMCH-GND	
Size: Custom	Document Number: 965P-DS3	Rev: 3.3
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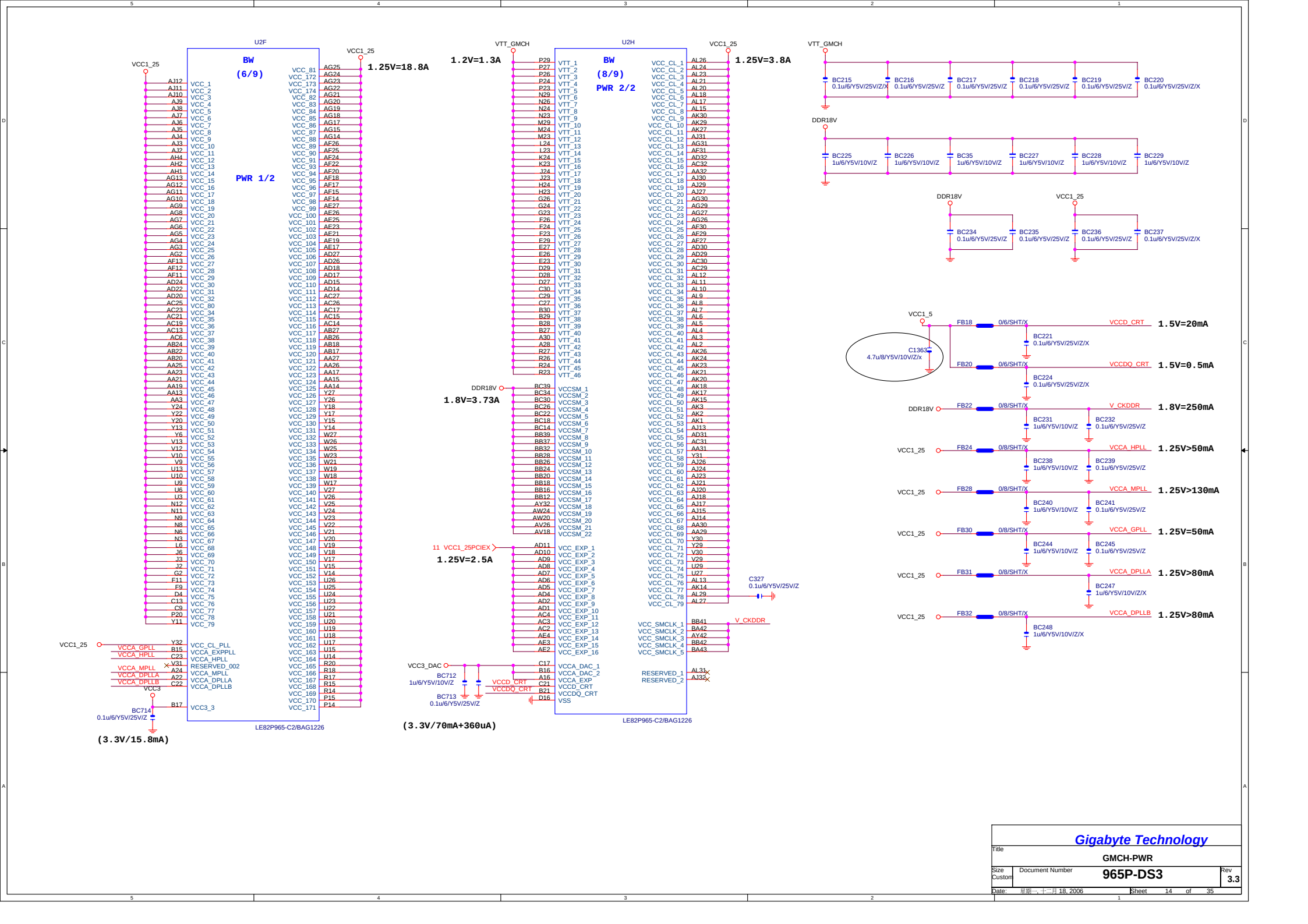
U2F
BW
(6/9)
PWR 1/2
VCC1_25
1.25V=18.8A
LE82P965-C2/BAG1226
(3.3V/15.8mA)
VCC3
BC714
0.1u/6Y5V/25V/Z
VCC3_DAC
BC712
1u/6Y5V/10V/Z
BC713
0.1u/6Y5V/25V/Z
VCCD_CRT
VCCDQ_CRT
U2H
BW
(8/9)
PWR 2/2
VTT_GMCH
1.2V=1.3A
1.25V=3.8A
DDR18V
1.8V=3.73A
11 VCC1_25PCIEX
1.25V=2.5A
C327
0.1u/6Y5V/25V/Z
V_CKDDR
LE82P965-C2/BAG1226
(3.3V/70mA+360uA)
BC215 0.1u/6Y5V/25V/Z/X
BC216 0.1u/6Y5V/25V/Z
BC217 0.1u/6Y5V/25V/Z
BC218 0.1u/6Y5V/25V/Z
BC219 0.1u/6Y5V/25V/Z
BC220 0.1u/6Y5V/25V/Z/X
BC225 1u/6Y5V/10V/Z
BC226 1u/6Y5V/10V/Z
BC35 1u/6Y5V/10V/Z
BC227 1u/6Y5V/10V/Z
BC228 1u/6Y5V/10V/Z
BC229 1u/6Y5V/10V/Z
BC234 0.1u/6Y5V/25V/Z
BC235 0.1u/6Y5V/25V/Z
BC236 0.1u/6Y5V/25V/Z
BC237 0.1u/6Y5V/25V/Z/X
VCC1_5
C1363 4.7u/8Y5V/10V/Z/x
FB18 0/6/SHT/X
VCCD_CRT
1.5V=20mA
BC221 0.1u/6Y5V/25V/Z/X
FB20 0/6/SHT/X
VCCDQ_CRT
1.5V=0.5mA
BC224 0.1u/6Y5V/25V/Z/X
FB22 0/8/SHT/X
V_CKDDR
1.8V=250mA
BC231 1u/6Y5V/10V/Z
BC232 0.1u/6Y5V/25V/Z
FB24 0/8/SHT/X
VCCA_HPLL
1.25V>50mA
BC238 1u/6Y5V/10V/Z
BC239 0.1u/6Y5V/25V/Z
FB28 0/8/SHT/X
VCCA_MPLL
1.25V>130mA
BC240 1u/6Y5V/10V/Z
BC241 0.1u/6Y5V/25V/Z
FB30 0/8/SHT/X
VCCA_GPLL
1.25V=50mA
BC244 1u/6Y5V/10V/Z
BC245 0.1u/6Y5V/25V/Z
FB31 0/8/SHT/X
VCCA_DPLLA
1.25V>80mA
BC247 1u/6Y5V/10V/Z/X
FB32 0/8/SHT/X
VCCA_DPLLB
1.25V>80mA
BC248 1u/6Y5V/10V/Z/X
Gigabyte Technology
Title
GMCH-PWR
Size Custom
Document Number
965P-DS3
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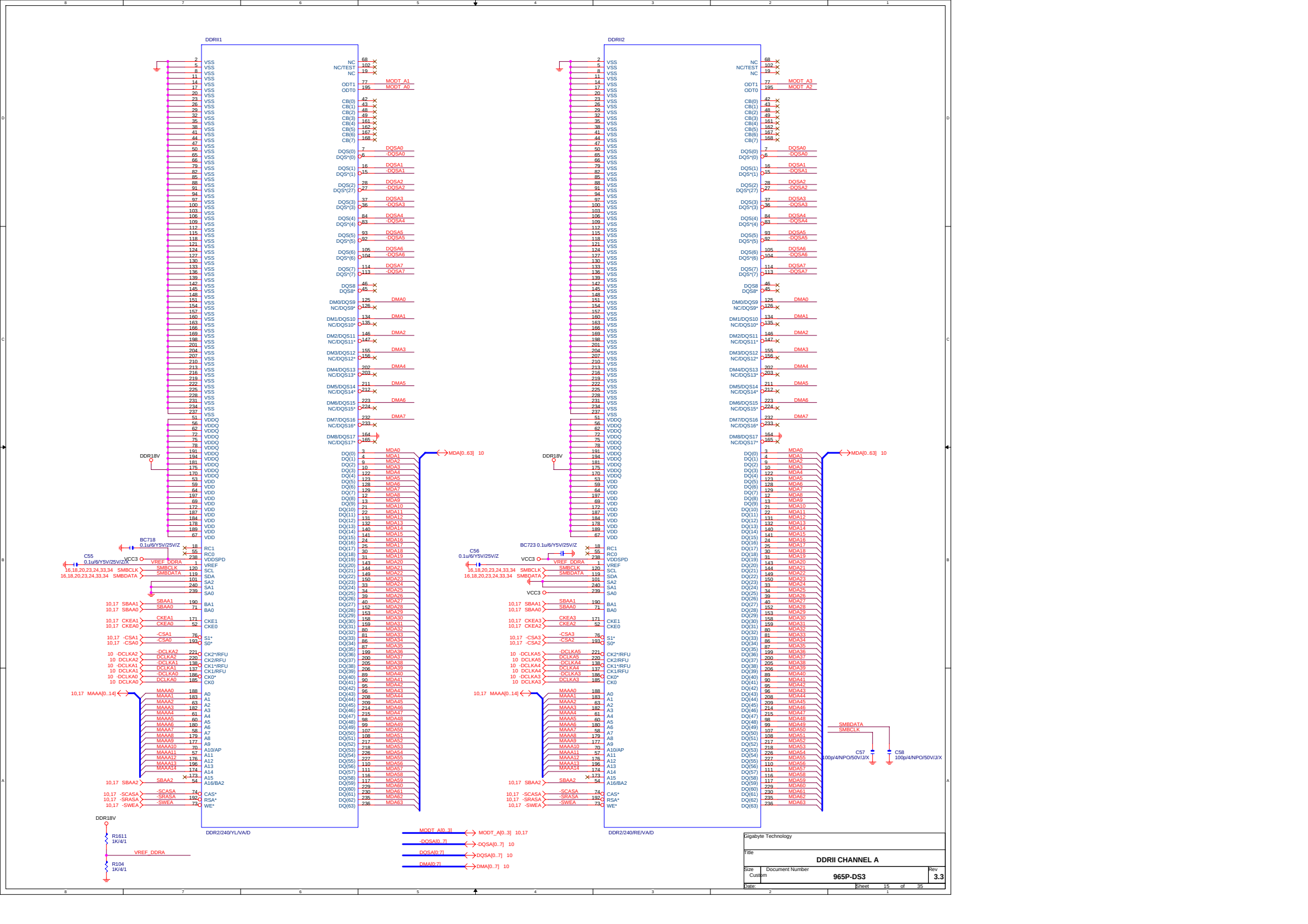
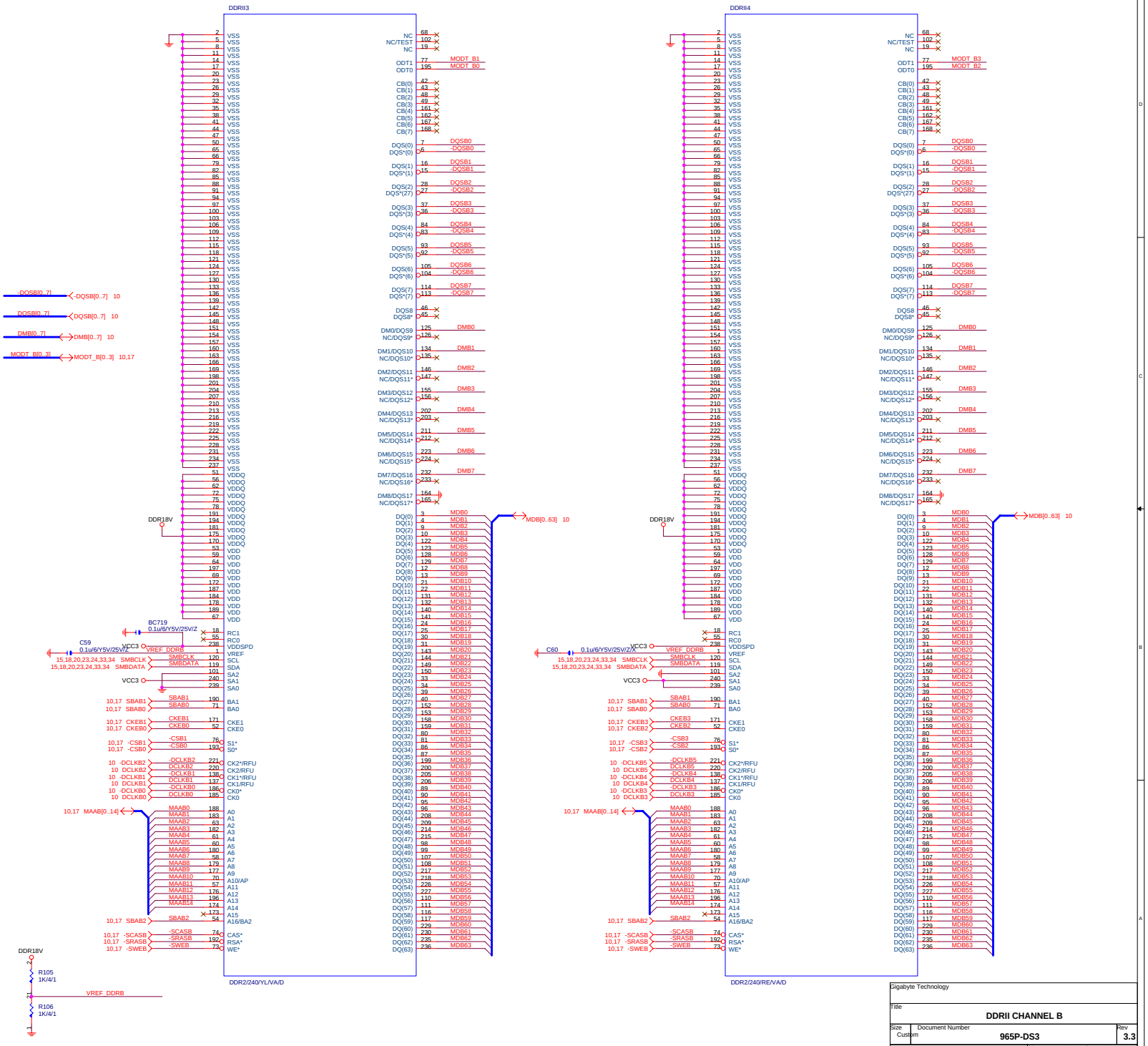


Gigabyte Technology		
Title	DDRII CHANNEL A	
Size: Custom	Document Number: 965P-DS3	Rev: 3.3
Date:	Sheet 15 of 35	



Gigabyte Technology	
Title	DDRII CHANNEL B
Size: Custom	Document Number: 965P-DS3
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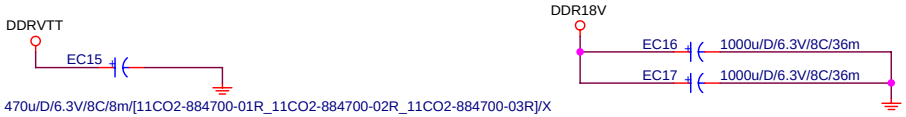
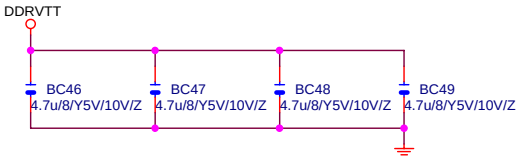
DDR TERMINATION CHANNEL A

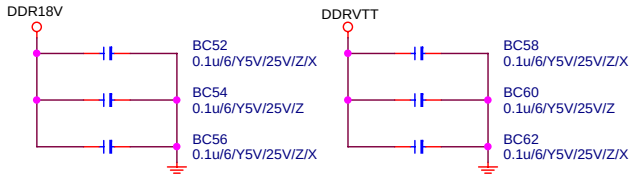
DDRVTT Decouple

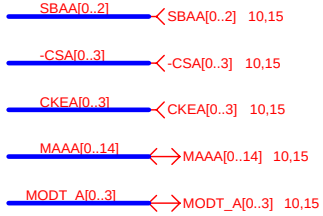


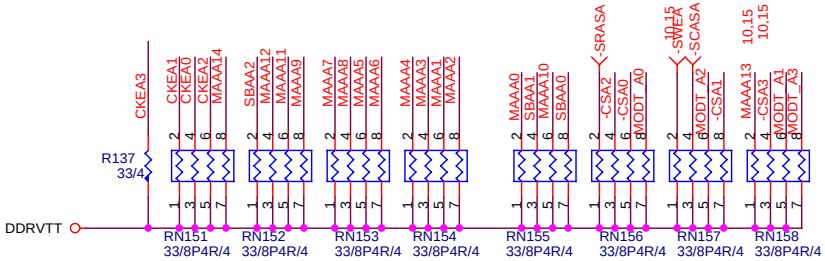


DDR18V Decouple

DDRVTT Decouple



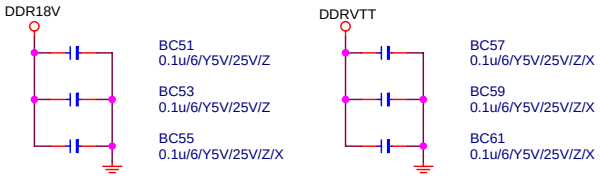


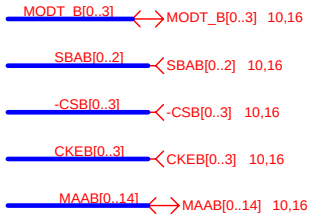


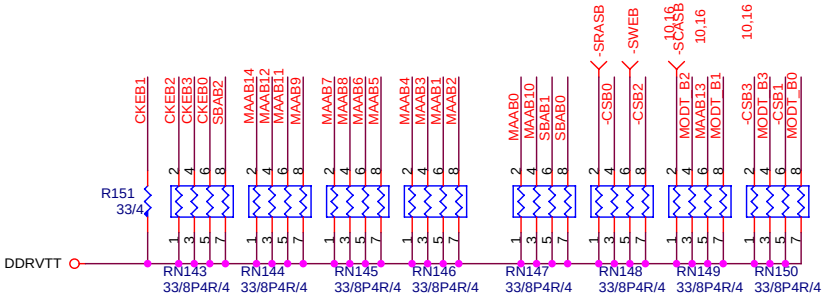
DDR TERMINATION CHANNEL B

DDR18V Decouple

DDRVTT Decouple







Gigabyte Technology		
Title: DDRII TERMINATOR		
Size: Custom	Document Number: 965P-DS3	Rev: 3.3
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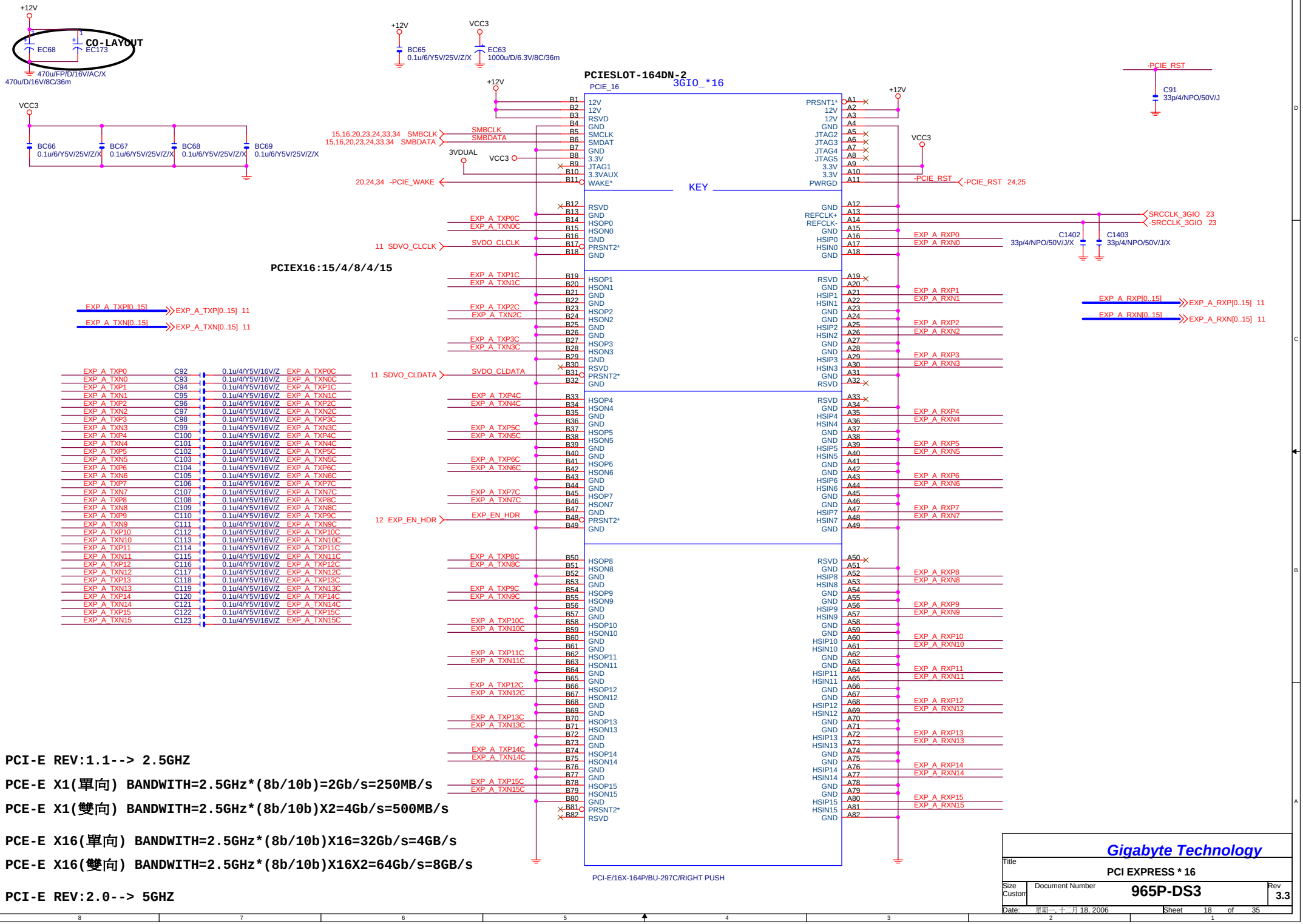
+12V
EC68
EC173
CO-LAYOUT
470u/FP/D/16V/AC/X
470u/D/16V/8C/36m
VCC3
BC66
0.1u/6/Y5V/25V/Z/X
BC67
0.1u/6/Y5V/25V/Z/X
BC68
0.1u/6/Y5V/25V/Z/X
BC69
0.1u/6/Y5V/25V/Z/X
+12V
BC65
0.1u/6/Y5V/25V/Z/X
VCC3
EC63
1000u/D/6.3V/8C/36m
PCIESLOT-164DN-2
PCIE_16
3GIO_*16
KEY
PCIEX16:15/4/8/4/15
-PCIE_RST
C91
33p/4/NPO/50V/J
SRCCLK_3GIO 23
-SRCCLK_3GIO 23
C1402
33p/4/NPO/50V/J/X
C1403
33p/4/NPO/50V/J/X
EXP_A_RXP[0..15] EXP_A_RXP[0..15] 11
EXP_A_RXN[0..15] EXP_A_RXN[0..15] 11
EXP_A_TXP[0..15] EXP_A_TXP[0..15] 11
EXP_A_TXN[0..15] EXP_A_TXN[0..15] 11
15,16,20,23,24,33,34 SMBCLK
15,16,20,23,24,33,34 SMBDATA
3VDUAL
20,24,34 -PCIE_WAKE
-PCIE_RST -PCIE_RST 24,25
11 SDVO_CLCLK
11 SDVO_CLDATA
12 EXP_EN_HDR
PCI-E/16X-164P/BU-297C/RIGHT PUSH
PCI-E REV:1.1--> 2.5GHZ
PCE-E X1(單向) BANDWITH=2.5GHz*(8b/10b)=2Gb/s=250MB/s
PCE-E X1(雙向) BANDWITH=2.5GHz*(8b/10b)X2=4Gb/s=500MB/s
PCE-E X16(單向) BANDWITH=2.5GHz*(8b/10b)X16=32Gb/s=4GB/s
PCE-E X16(雙向) BANDWITH=2.5GHz*(8b/10b)X16X2=64Gb/s=8GB/s
PCI-E REV:2.0--> 5GHZ
Gigabyte Technology
Title
PCI EXPRESS * 16
Size
Custom
Document Number
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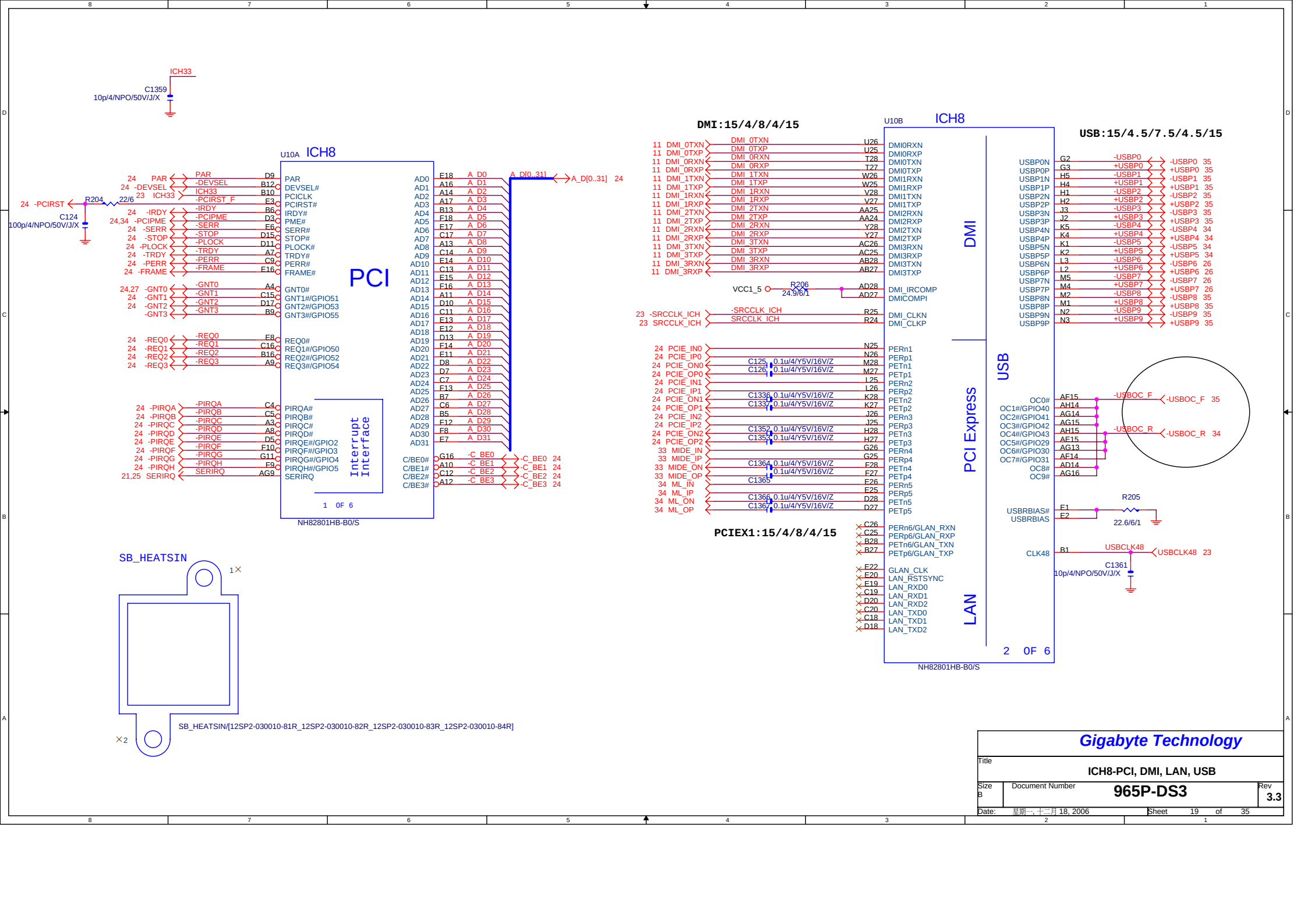

Gigabyte Technology		
Title: ICH8-PCI, DMI, LAN, USB		
Size: B	Document Number: 965P-DS3	Rev: 3.3
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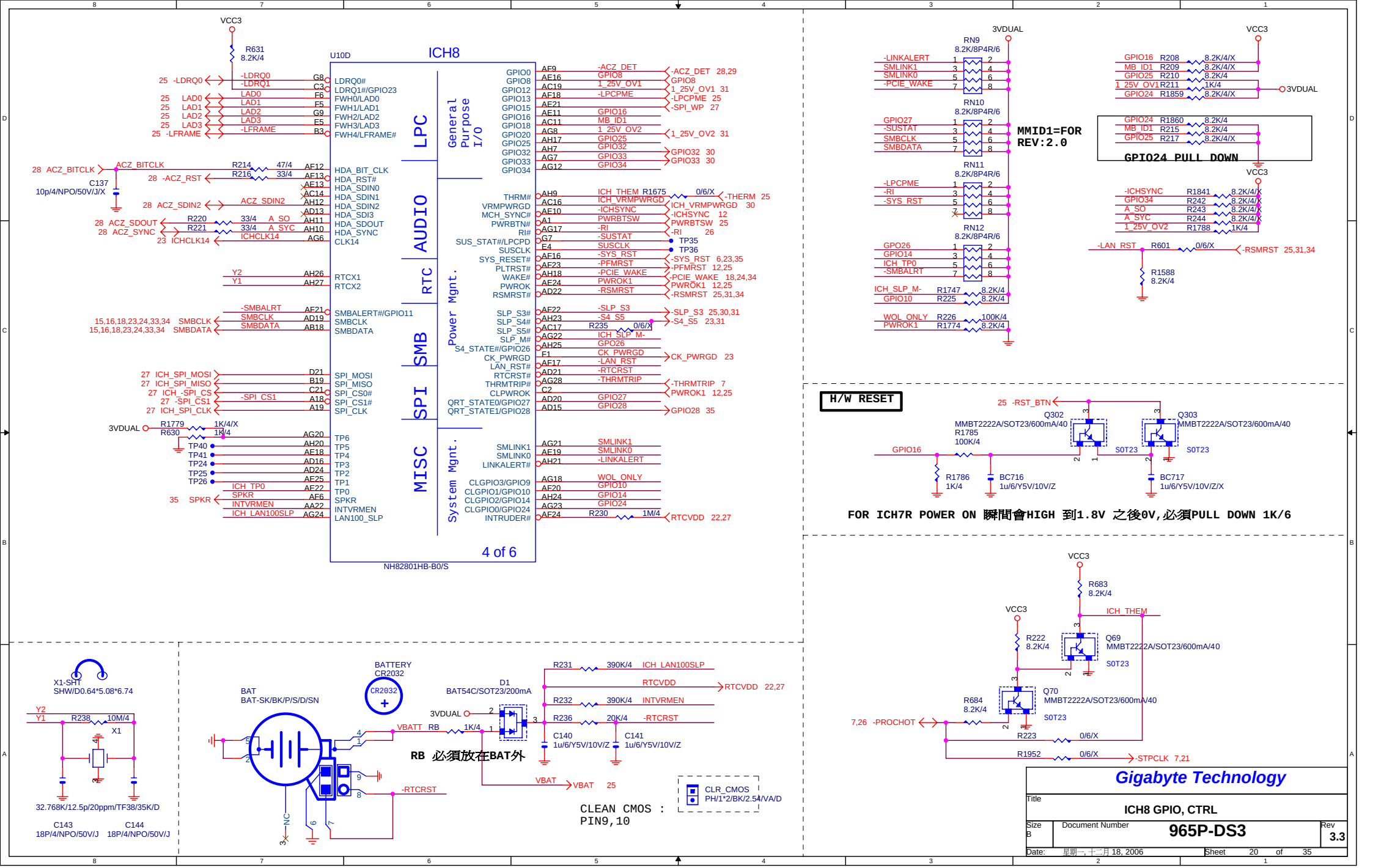
U10D
ICH8
LPC
AUDIO
RTC
SMB
SPI
MISC
General Purpose I/O
Power Mgnt.
System Mgnt.
NH82801HB-B0/S
4 of 6
3VDUAL
MMID1=FOR REV:2.0
GPIO24 PULL DOWN
H/W RESET
FOR ICH7R POWER ON 瞬間會HIGH 到1.8V 之後0V,必須PULL DOWN 1K/6
RB 必須放在BAT外
CLEAN CMOS : PIN9,10
BAT-SK/BK/P/S/D/SN
CR2032
32.768K/12.5p/20ppm/TF38/35K/D
Gigabyte Technology
ICH8 GPIO, CTRL
965P-DS3
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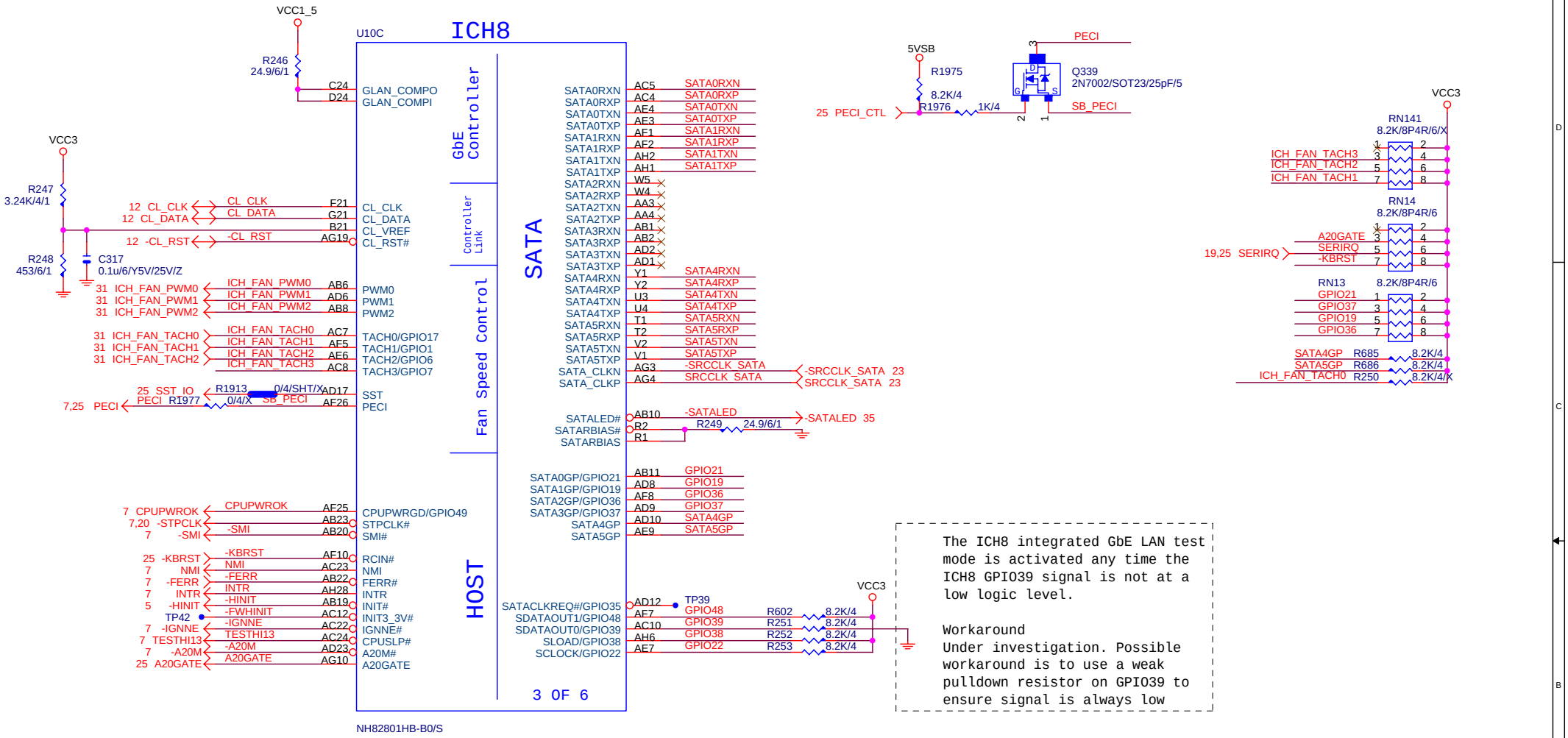

Gigabyte Technology		
Title: ICH6- SATA, FAN CTRL		
Size: Custom	Document Number: 965P-DS3	Rev: 3.3
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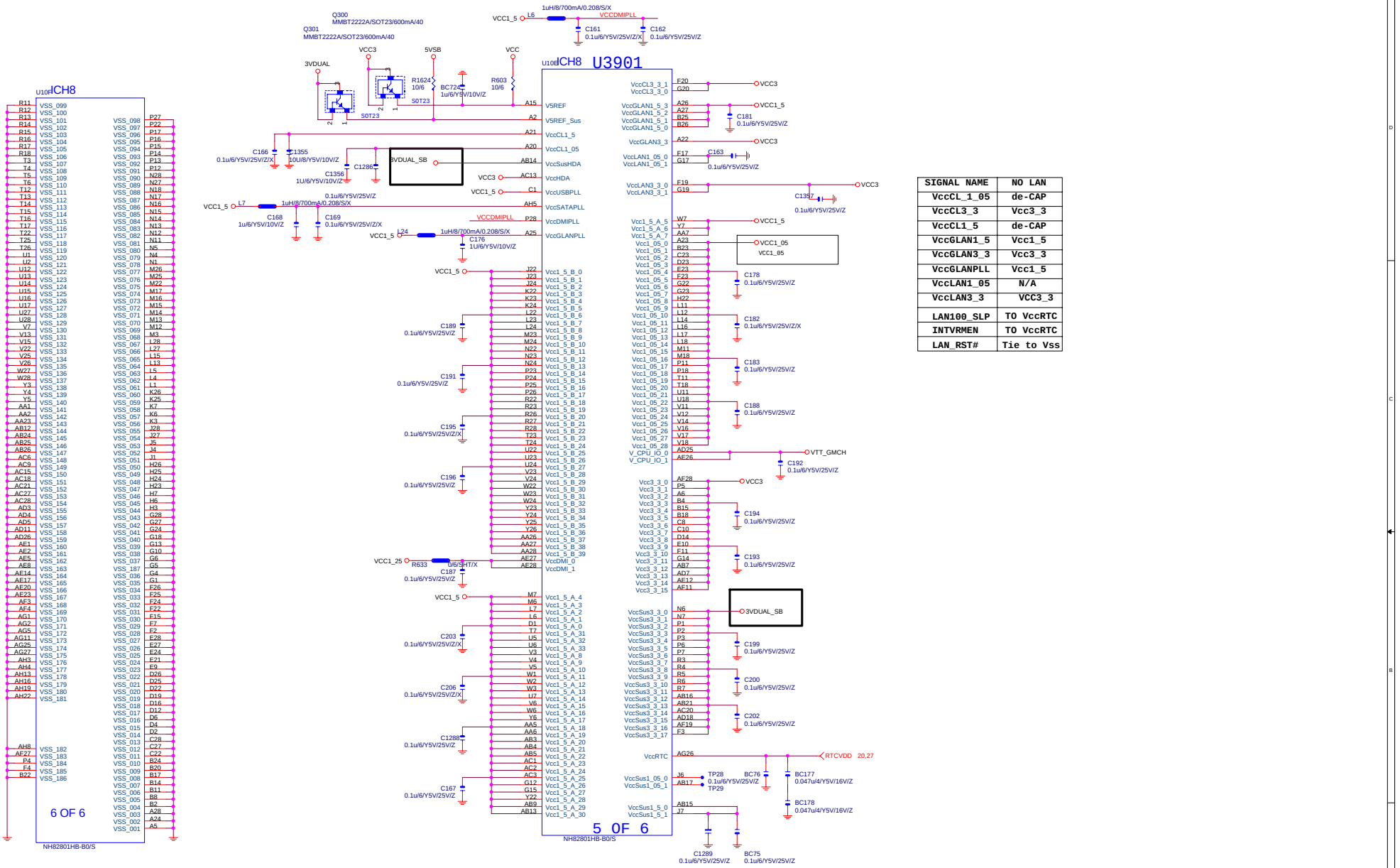

SIGNAL NAME	NO LAN
VccCL_1_05	de-CAP
VccCL3_3	Vcc3_3
VccCL1_5	de-CAP
VccGLAN1_5	Vcc1_5
VccGLAN3_3	Vcc3_3
VccGLANPLL	Vcc1_5
VccLAN1_05	N/A
VccLAN3_3	VCC3_3
LAN100_SLP	TO VccRTC
INTVRMEN	TO VccRTC
LAN_RST#	Tie to Vss

Gigabyte Technology

Title	ICH6-PWR & GND	
Size C	Document Number 965P-DS3	Rev 3.3
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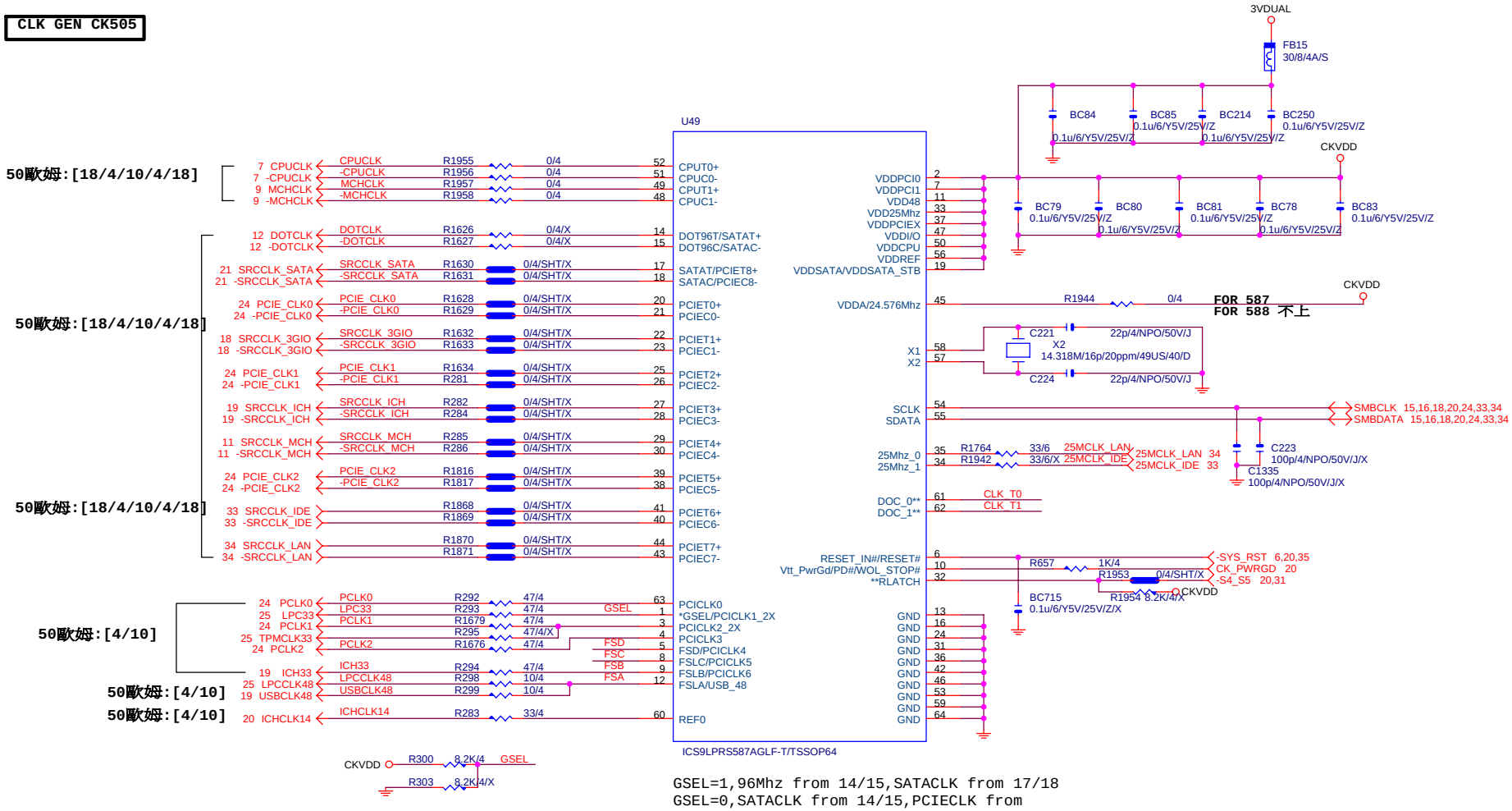
CLK GEN CK505



Title	CK505 CLK GEN
Size: Custom	Document Number: 965P-DS3
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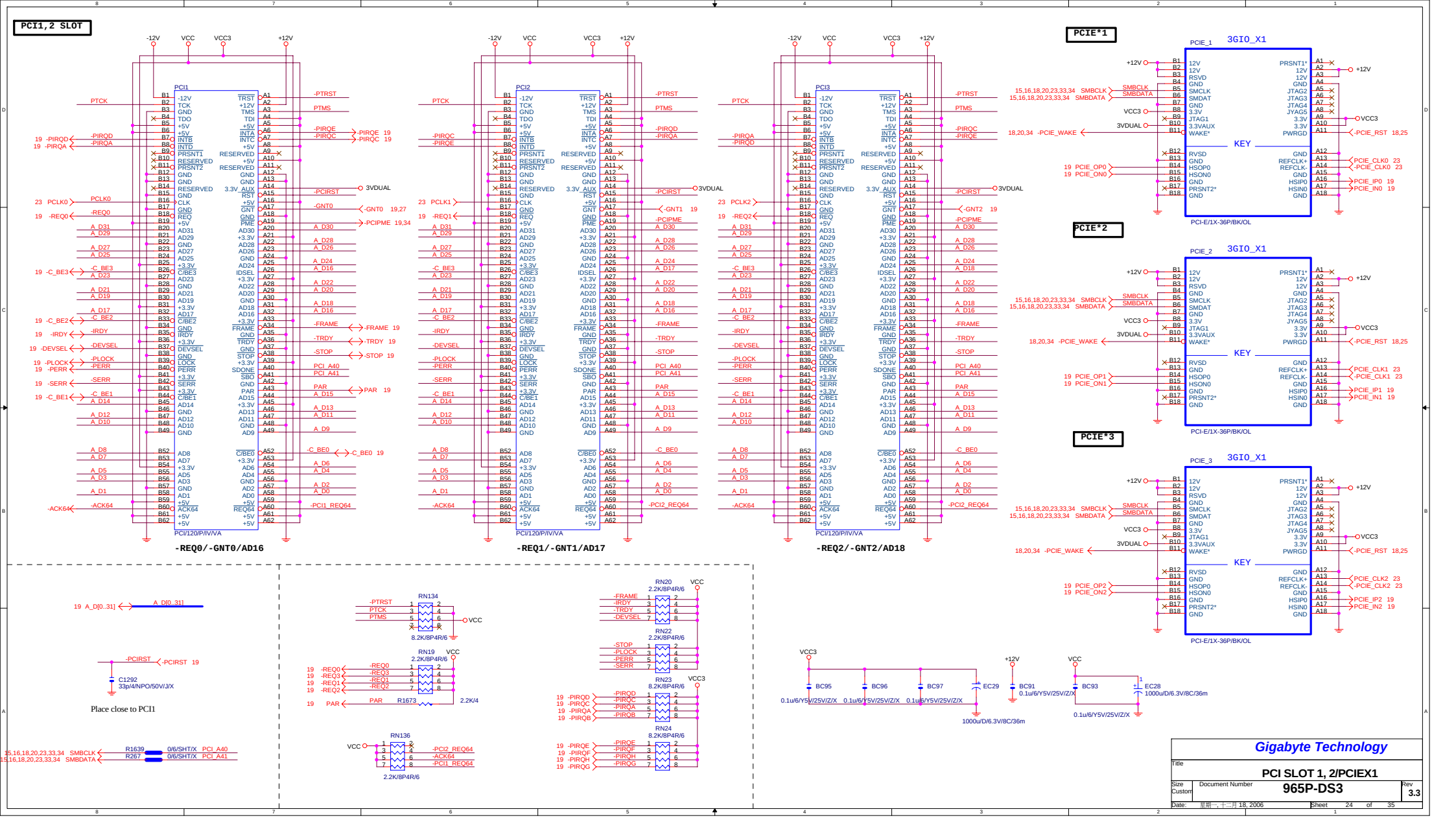
PCI1,2 SLOT
PCI1
PCI2
PCI3
PCI/120/P/IV/VA
-REQ0/-GNT0/AD16
-REQ1/-GNT1/AD17
-REQ2/-GNT2/AD18
PCIE*1
PCIE*2
PCIE*3
PCIE_1
PCIE_2
PCIE_3
3GIO_X1
KEY
PCI-E/1X-36P/BK/OL
Place close to PCI1
C1292
33p/4/NPO/50V/J/X
RN134
RN19
RN20
RN22
RN23
RN24
RN136
2.2K/8P4R/6
8.2K/8P4R/6
R1639
R267
0/6/SHT/X
R1673
2.2K/4
BC95
BC96
BC97
EC29
BC91
BC93
EC28
1000u/D/6.3V/8C/36m
0.1u/6/Y5V/25V/Z/X
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PCI SLOT 1, 2/PCIEX1
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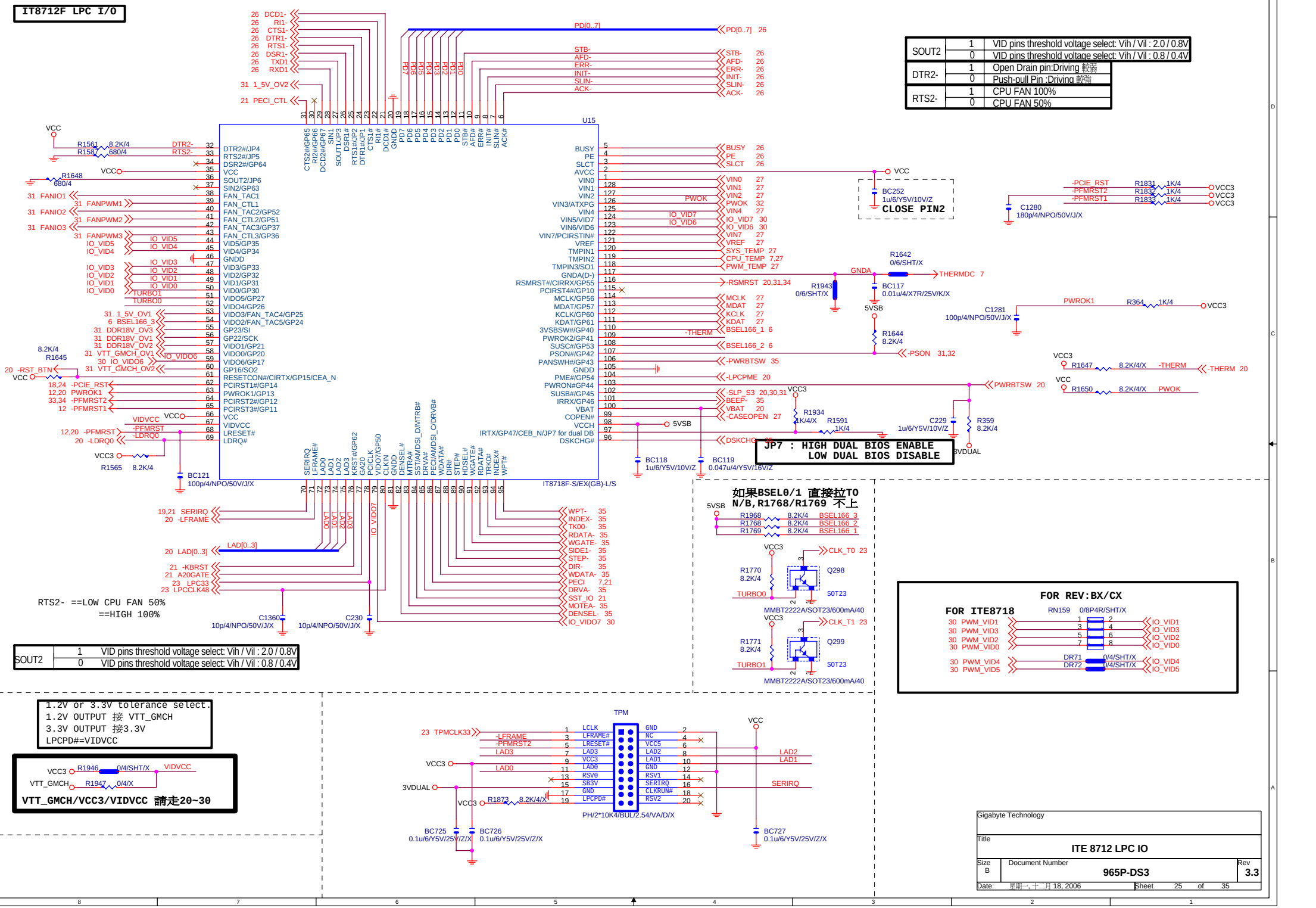
IT8712F LPC I/O



SOUT2		
	1	VID pins threshold voltage select: Vih / Vil : 2.0 / 0.8V
	0	VID pins threshold voltage select: Vih / Vil : 0.8 / 0.4V
DTR2-	1	Open Drain pin:Driving 較弱
	0	Push-pull Pin :Driving 較強
RTS2-	1	CPU FAN 100%
	0	CPU FAN 50%

SOUT2		
	1	VID pins threshold voltage select: Vih / Vil : 2.0 / 0.8V
	0	VID pins threshold voltage select: Vih / Vil : 0.8 / 0.4V

Gigabyte Technology	
Title	ITE 8712 LPC IO
Size: B	Document Number: 965P-DS3
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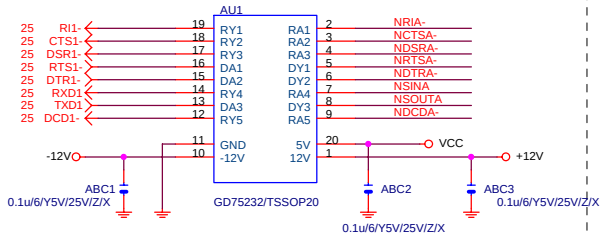
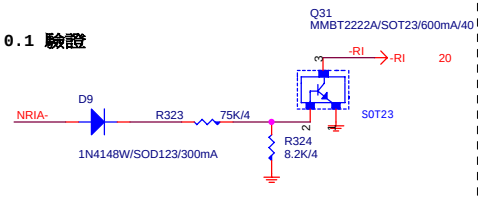
COMA

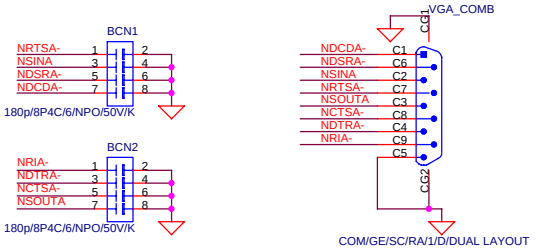


COM RI

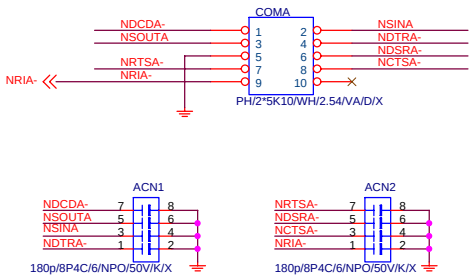
REV:0.1 驗證

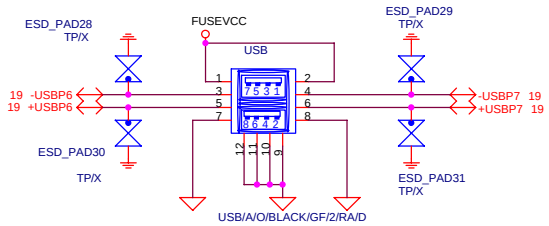


EXTERNAL COMB

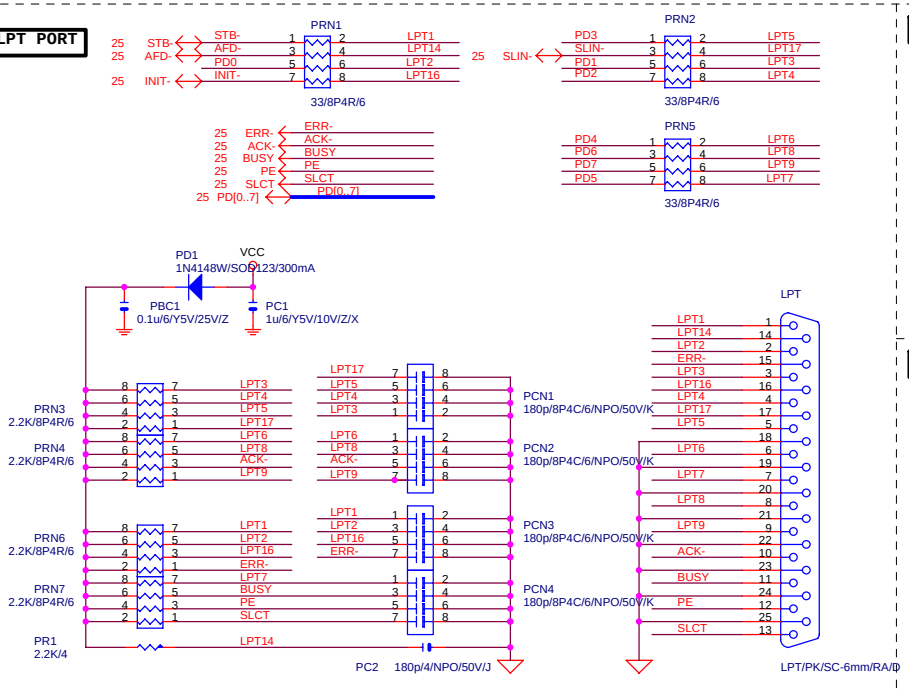


PLACE NEAR VGA_COM CONNECTOR

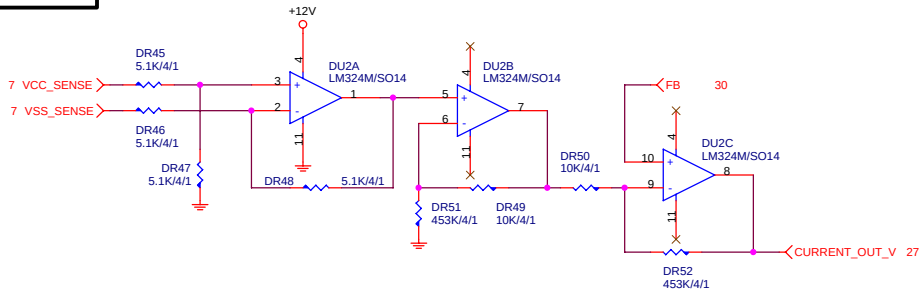




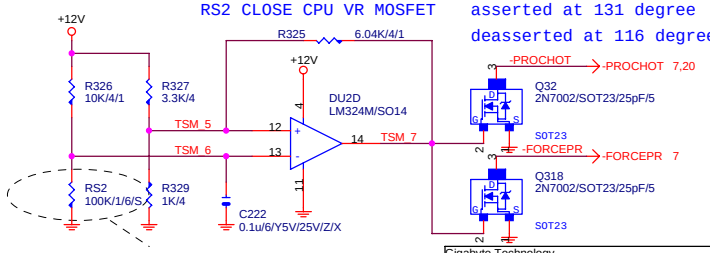
LPT PORT



DYNAMIC CURRENT OC



-PROHOT



CLOSE PWM HOT MOSFET

Gigabyte Technology

Title: **COM & LPT PORT**

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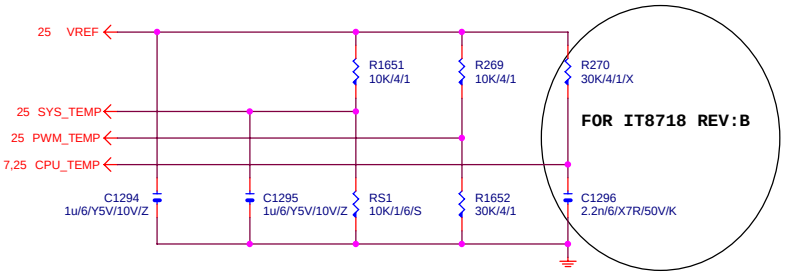
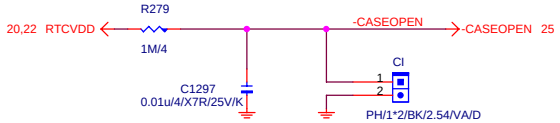
TEMP H/W MONITOR

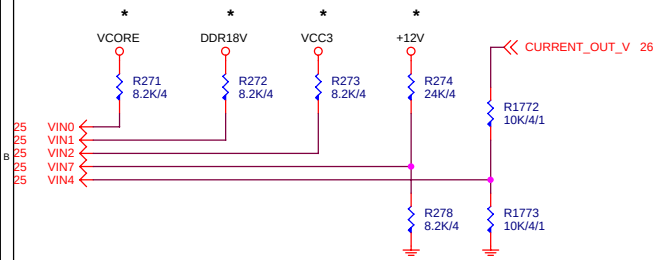


CASE OPEN

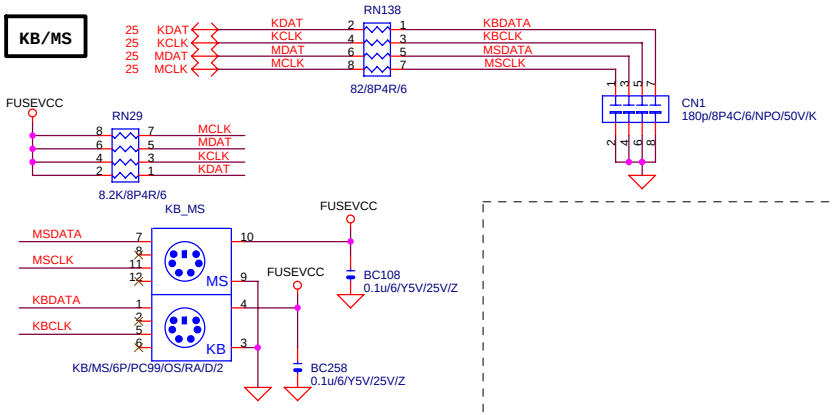


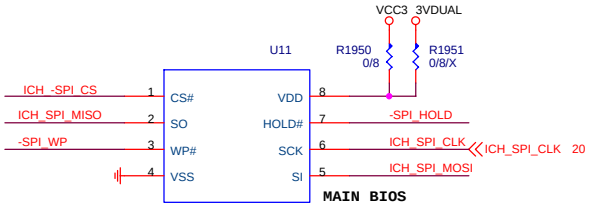
Case Open Circuits

VOLTAGE-- H/W MONITOR



KB/MS

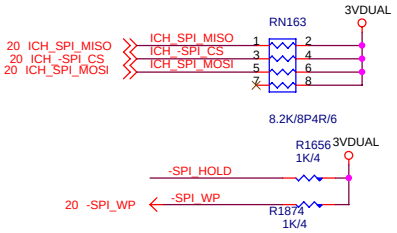


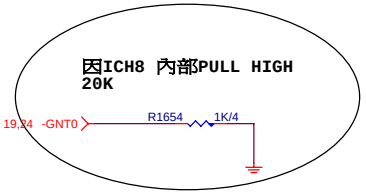


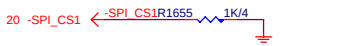
SST25VF080B-50-4C-S2AF/S/[10HP4-112580-11R_10HP4-172580-01R_10HP4-152580-11R]

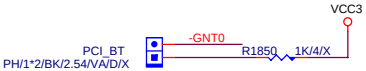
MXIC(4K)/SST(4K)

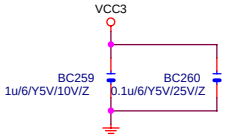
BOOT DEVICE	GNT0	CS1
SPI	0	X
PCI	1	0
FWH	1	1

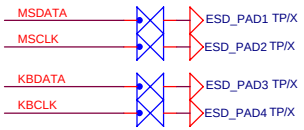












Gigabyte Technology

Title: **BIOS/HW-MONITOR/CI/KB/MS**

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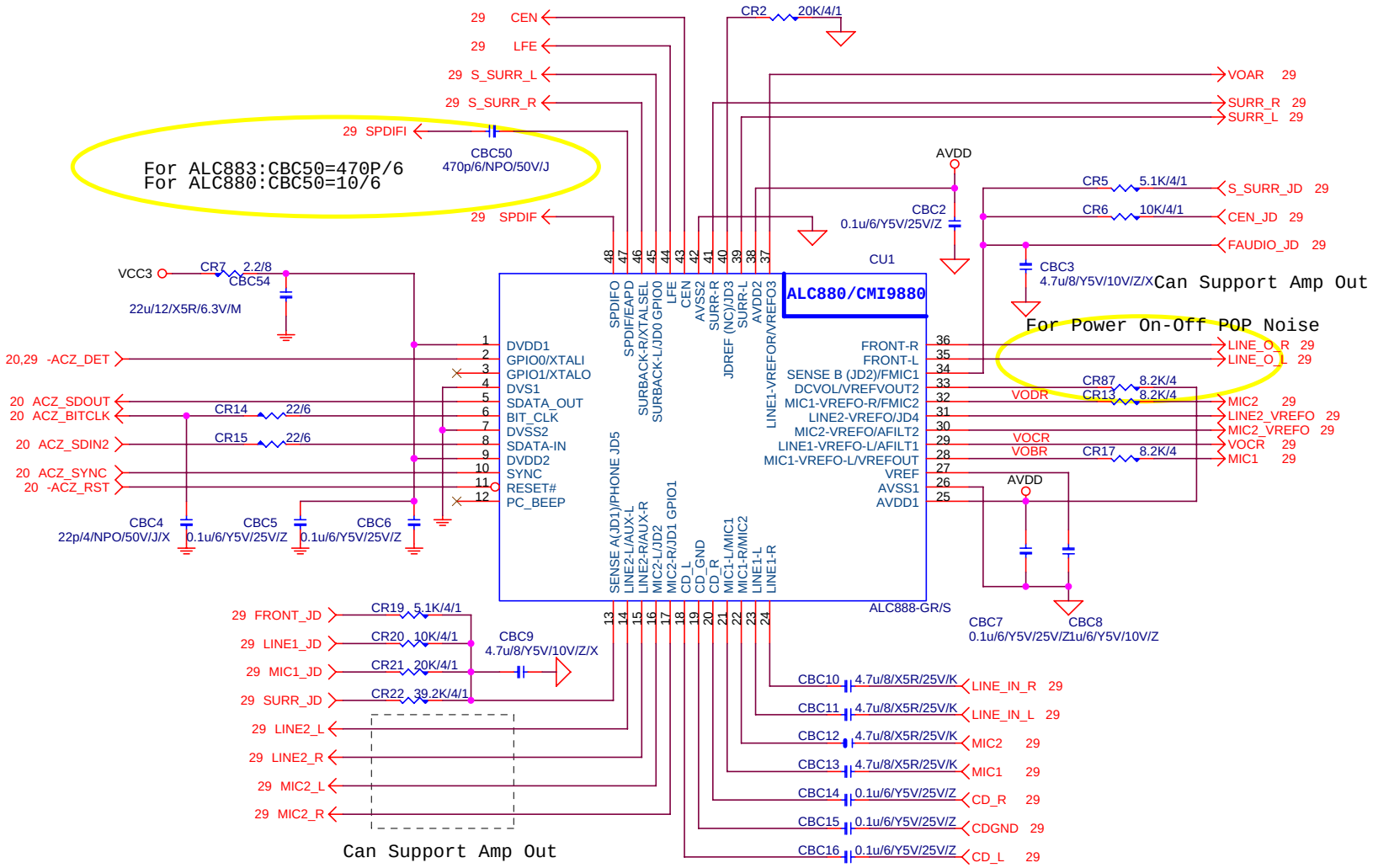
AZALIA CODEC



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Size: Custom	Document Number: 965P-DS3	Rev: 3.3
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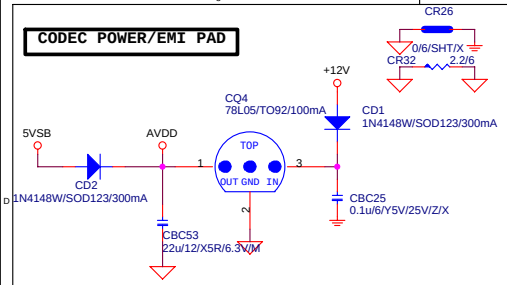
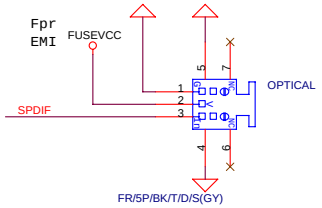
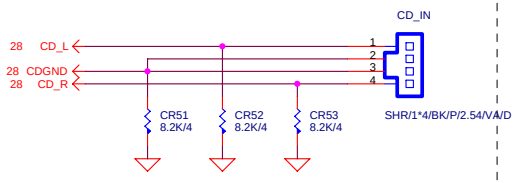
CODEC POWER/EMI PAD

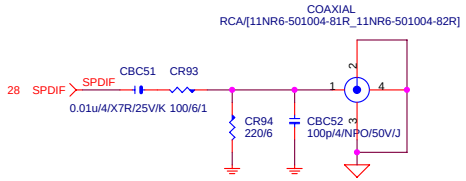


CO-LAYOUT

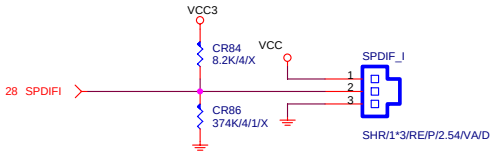


CD IN

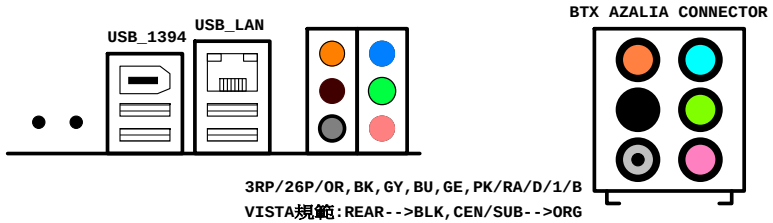


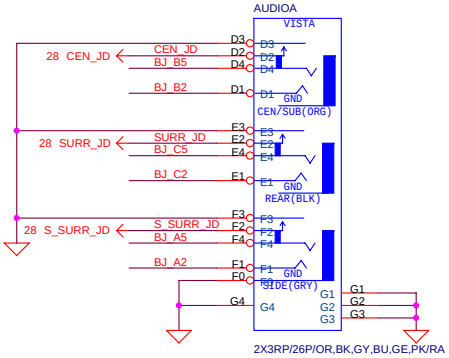


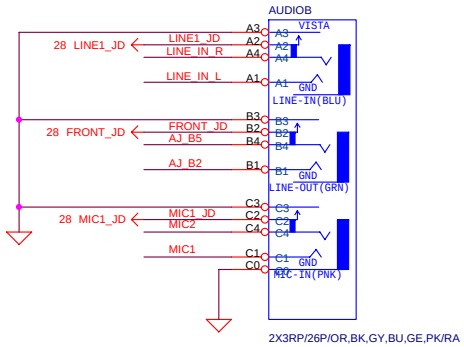
SPDIF



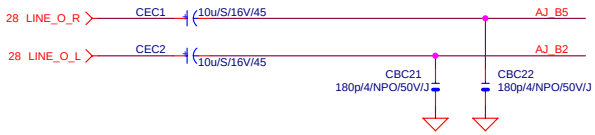
AZALIA JACK



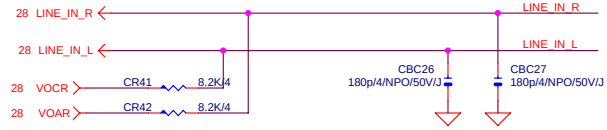




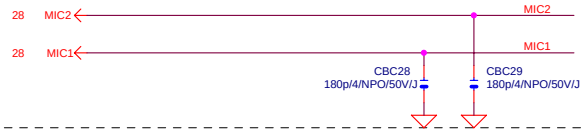
LINE-OUT



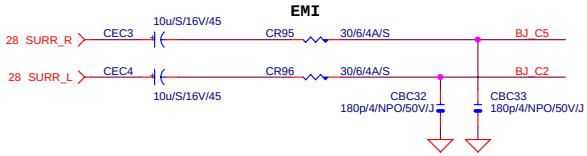
LINE-IN



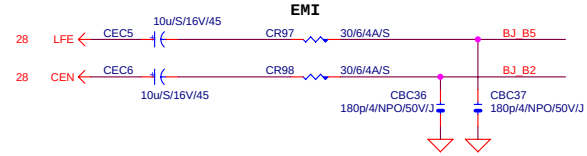
MIC-IN



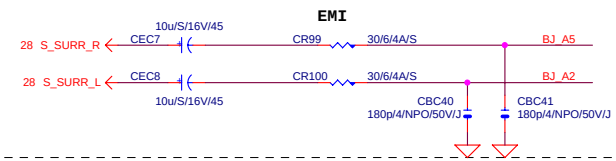
SURROUND



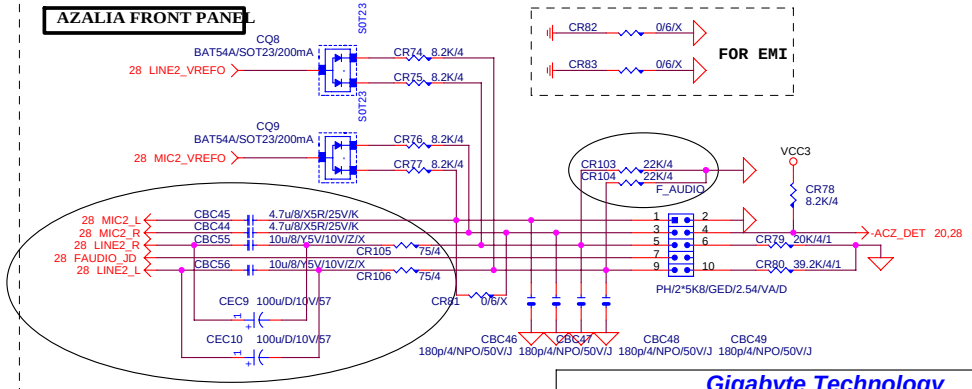
CEN/LFE



SURR BACK



AZALIA FRONT PANEL



Gigabyte Technology

Title: AUDIO JACK

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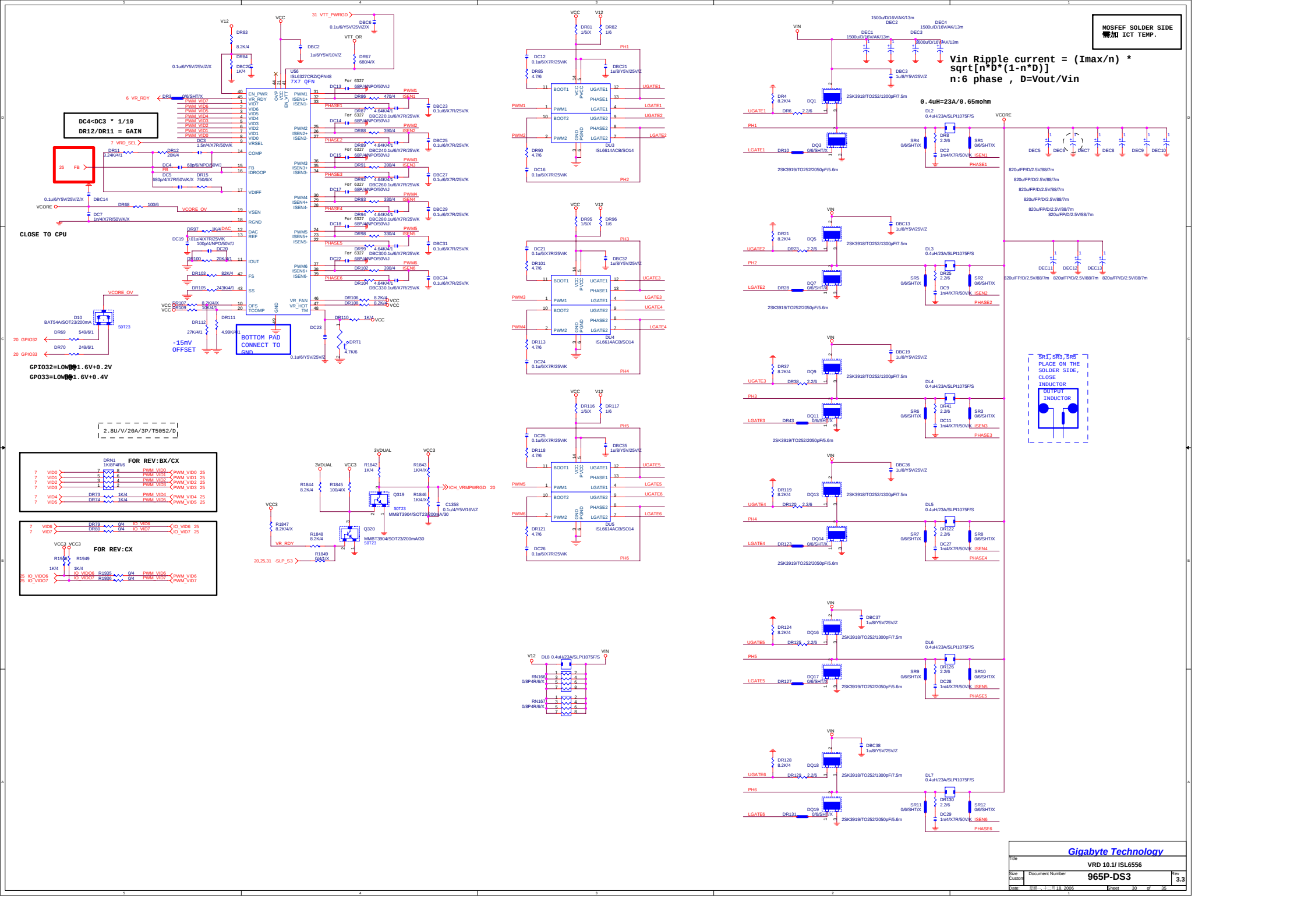
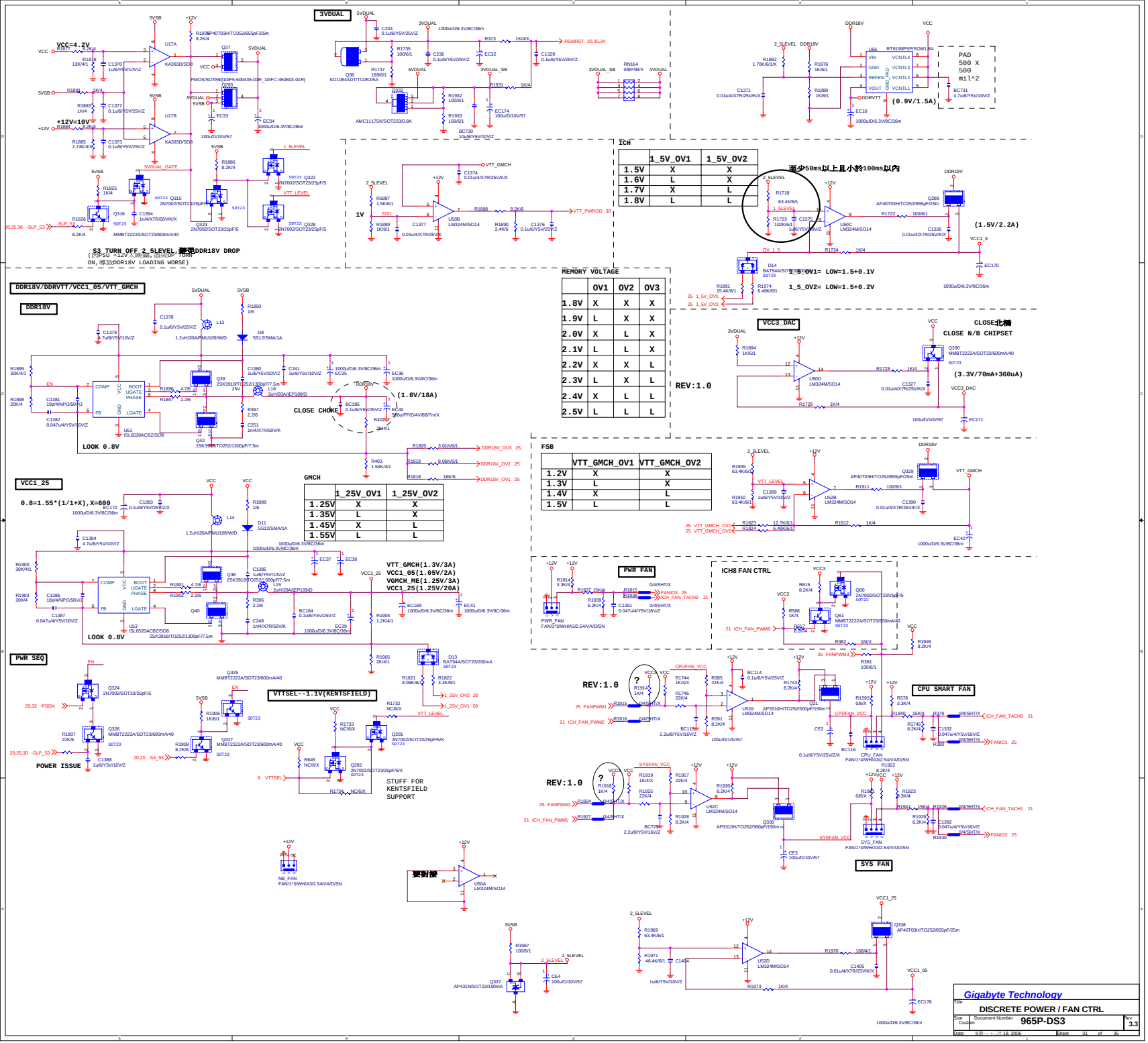
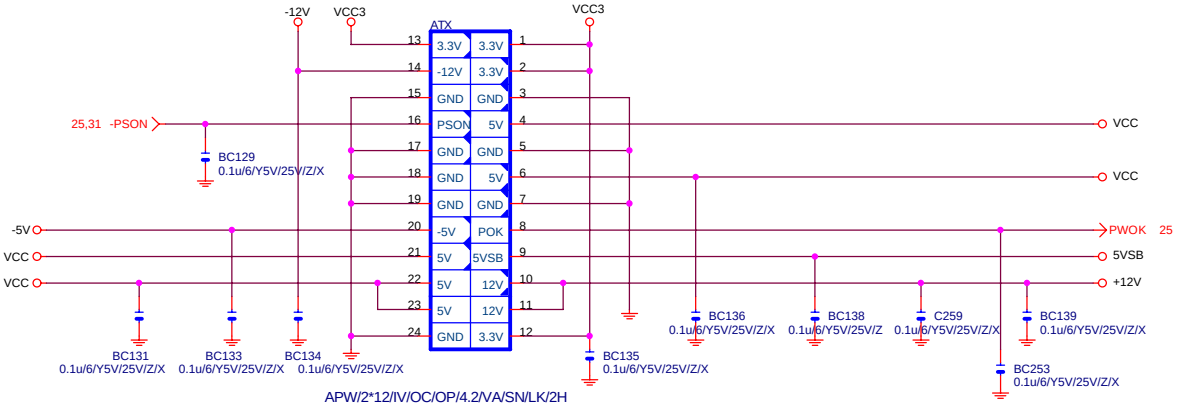
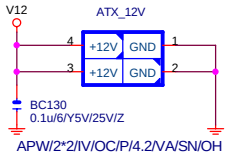

MOSFET SOLDER SIDE
需加 ICT TEMP.
Vin Ripple current = (Imax/n) * sqrt[n*D*(1-n*D)]
n:6 phase , D=Vout/Vin
0.4uH=23A/0.65mohm
DC4<DC3 * 1/10
DR12/DR11 = GAIN
CLOSE TO CPU
GPIO32=LOW時1.6V+0.2V
GPO33=LOW時1.6V+0.4V
~15mV OFFSET
BOTTOM PAD CONNECT TO GND
2.8U/V/20A/3P/T5052/D
FOR REV:BX/CX
FOR REV:CX
SR1,SR3,SR5 PLACE ON THE SOLDER SIDE, CLOSE INDUCTOR
OUTPUT INDUCTOR
Gigabyte Technology
VRD 10.1/ ISL6556
965P-DS3
3.3

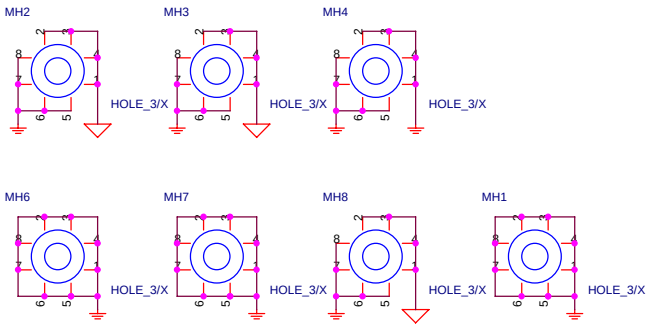

3VDUAL
VCC=4.2V
+12V=10V
S3_TURN_OFF_2_5LEVEL_最終DDR18V DROP
ON, 讓到DDR18V LOADING WORSE)
ICH
1_5V_OV1
1_5V_OV2
1.5V X X
1.6V L X
1.7V X L
1.8V L L
至少50ms以上且小於100ms以內
(1.5V/2.2A)
1_5_OV1= LOW=1.5+0.1V
1_5_OV2= LOW=1.5+0.2V
MEMORY VOLTAGE
0V1 0V2 0V3
1.8V X X X
1.9V L X X
2.0V X L X
2.1V L L X
2.2V X X L
2.3V L X L
2.4V X L L
2.5V L L L
DDR18V/DDRVTT/VCC1_05/VTT_GMCH
DDR18V
(1.8V/18A)
CLOSE CHOKE
LOOK 0.8V
REV:1.0
VCC3_DAC
CLOSE北橋
CLOSE N/B CHIPSET
(3.3V/70mA+360uA)
VCC1_25
0.8=1.55*(1/1+X),X=600
GMCH
1_25V_OV1 1_25V_OV2
1.25V X X
1.35V L X
1.45V X L
1.55V L L
FSB
VTT_GMCH_OV1 VTT_GMCH_OV2
1.2V X X
1.3V L X
1.4V X L
1.5V L L
VTT_GMCH(1.3V/3A)
VCC1_05(1.05V/2A)
VGMCH_ME(1.25V/3A)
VCC1_25(1.25V/20A)
PWR SEQ
POWER ISSUE
VTTSEL--1.1V(KENTSFIELD)
STUFF FOR KENTSFIELD SUPPORT
PWR FAN
ICH8 FAN CTRL
CPU SMART FAN
SYS FAN
REV:1.0
PAD 500 X 500 mil^2
(0.9V/1.5A)
Gigabyte Technology
DISCRETE POWER / FAN CTRL
965P-DS3
3.3

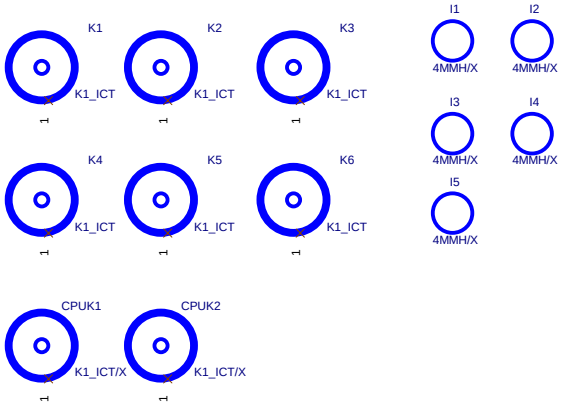
ATX POWER CONNECTOR





HOLE_3-2--->有鉛





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3.3V to 1.8V Voltage Regulator

AMC1117SK/SOT223/0.8A

RQ1

VCC_1.8V

VCC3

RR21 100/4/1

RBC1 0.1u/4/Y5V/16V/Z

RR22 44.2/4/1

RBC2 10u/8/Y5V/10V/Z

REC1 100u/D/10V/57

68/4/1 FOR JMB368
VCC1.8V=2.1V

JMB368

JM368/LQFP40/X

RU2

JMicron JMB363

LQFP 100 14x14

GBB363/3

RU1

25,34 -PFMRST2

RC3 100P/4/N/50V/X

RC5 0.1u/4/Y5V/16V/Z MIDE_IP 19

RC6 0.1u/4/Y5V/16V/Z MIDE_IN 19

MIDE_ON 19

MIDE_OP 19

SRCCLK_IDE 23

-SRCCLK_IDE 23

RBC3 RBC4 RBC5 RBC6 RBC7 RBC8 RBC9

0.1u/4/Y5V/16V/Z 0.1u/4/Y5V/16V/Z 0.1u/4/Y5V/16V/Z 0.1u/4/Y5V/16V/Z 0.1u/4/Y5V/16V/Z 10u/8/Y5V/10V/Z

close to IC

RBC10 10u/8/Y5V/10V/Z RBC11 0.1u/4/Y5V/16V/Z RBC12 0.1u/4/Y5V/16V/Z REC2 RBC13 0.1u/4/Y5V/16V/Z

Close to pin42 and pin53

100u/D/10V/57

PCIE_REXT1 SATA_REXT1 SATA_REXT0

RR31 12K/4/1 RR32 12K/4/1 RR33 12K/4/1

Near to PIN

RBC14 0.1u/4/Y5V/16V/Z RBC15 0.1u/4/Y5V/16V/Z RBC16 0.1u/4/Y5V/16V/Z RBC17 0.1u/4/Y5V/16V/Z RBC18 10u/8/Y5V/10V/Z

close to IC

RR19 0/6/X 25MCLK_IDE 23

會漏電

XTALI RR20 1M/4 XTALO RX1 25M/20p/30ppm/49US/20/D RC1 33P/4/NPO/50V/J RC2 33P/4/NPO/50V/J

RR23 8.2K/4 RR24 8.2K/4

SMB_CLK RR25 0/4/X SMBCLK 15,16,18,20,23,24,34

SMB_DAT RR26 0/4/X SMBDATA 15,16,18,20,23,24,34

PH_IORDY RR29 1K/4

CSELA RR30 0/4

PH_DMARQ RR34 8.2K/4

PH_INTRQ RR35 8.2K/4

DD7A RR36 8.2K/4

IDE Connector

IDE1

PH_RESETnA PH_DD7 PH_DD6 PH_DD5 PH_DD4 PH_DD3 PH_DD2 PH_DD1 PH_DD0

PH_DD8 PH_DD9 PH_DD10 PH_DD11 PH_DD12 PH_DD13 PH_DD14 PH_DD15

(#20 key-pin)

PH_DMARQ PH_DIOW_N PH_DIOR_N PH_IORDY PH_DMACK_N PH_INTRQ PH_DA1 PH_DA0 PH_CS0_N DASPnXA

(#28 CSEL)

CSELA

(#32 IOCS16)

PH_CBLID_N PH_DA2 PH_CS1_N

BH/2*20K20/GEL/N/2.54/VA/D/GF

VCC

RR37 1K/4

PH_RESETnA

RR38 8.2K/4

RQ3 MMBT2222A/SOT23/600mA/40

S0T23

RESETnA

-PFMRST2 RR43 0/4/X

OLNY FOR JMB368

VCC_1.8V ASVDD_1.8V

RBC19 10u/8/Y5V/10V/Z RBC20 0.1u/4/Y5V/16V/Z RBC21 0.1u/4/Y5V/16V/Z

Close to pin58

RBC22 10u/8/Y5V/10V/Z RBC23 0.1u/4/Y5V/16V/Z RBC24 0.1u/4/Y5V/16V/Z

Close to pin47

VCC_1.8V APVDD_1.8V

RBC25 0.1u/4/Y5V/16V/Z RBC26 10u/8/Y5V/10V/Z

CLOSE TO pin22

RBC27 10u/8/Y5V/10V/Z RBC28 0.1u/4/Y5V/16V/Z RBC29 1n/4/X7R/50V/K

close to pin17

DASPnXA HD_LEDn RD1 BAW56/SOT23/300mA S0T23

MMBT2222A/SOT23/600mA/40 RR27 1K/4 RQ2 S0T23

-HDLED -HDLED 35

RC4 180P/4/N/50V/X

RR28 0/4/X

SATA Connector

SATA_TXP0 RC7 0.01u/4/X7R/25V/K SATA_RXP1

SATA_TXN0 RC9 0.01u/4/X7R/25V/K SATA_RXN1

SATA_RXN0 RC11 0.01u/4/X7R/25V/K SATA_TXN1

SATA_RXP0 RC13 0.01u/4/X7R/25V/K SATA_TXP1

RC8 RC10 RC12 RC14 0.01u/4/X7R/25V/K

GSATAII0_1

SATA2/7/PU/H/P/VA/D/2/B/GBT

JMB368 REMOVE

PH_DD7 DD7A
PH_DD8 DD8A
PH_DD6 DD6A
PH_DD9 DD9A

PH_DD5 DD5A
PH_DD4 DD4A
PH_DD10 DD10A
PH_DD11 DD11A

PH_DD3 DD3A
PH_DD12 DD12A
PH_DD2 DD2A
PH_DD13 DD13A

PH_DD1 DD1A
PH_DD0 DD0A
PH_DD14 DD14A
PH_DD15 DD15A

PH_DIOW_N DIOWnA
PH_DIOR_N DIORnA
PH_DMACK_N DMACKnA
PH_DA1 DA1A
PH_DA0 DA0A
PH_CS0_N CS0nA
PH_DA2 DA2A
PH_CS1_N CS1nA

PH_IORDY IORDYA
PH_DMARQ DMARQA
PH_INTRQ INTRQA
PH_CBLID_N PDIAGnA

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PCIE-1G LAN

 # Layout Check 注意事項

1. LU1 PIN65 需下內層GND,打 12 VIA
2. 3VDUAL , VCC3 , VDD15_L , AVDD25_L 至少走20mil寬,並且電容擺設每兩pin至少放一顆Bypass Cap.
3. X'TAL 25MHz 兩訊號線,TRACE 愈短愈好,線寬12mil
4. MDI正負0~3,TRACE 8:7:8 , 每對之間保持 40mil

100歐姆:[20/5/7/5/20]

50歐姆:[18/4/10/4/18]

88E8050

88E8056-A2-NNC/QFN64

3VDUAL

2.5V

1.2V

USB_LAN CONNECTOR

LAN 100歐姆:[30/4/8/4/30] FOR B 製程

USB_LAN

UP

DOWN

USB+LAN/1G/GO,Y/OS/RA/D/1

90歐姆:[15/4.5/7.5/4.5/15]

CLOSE LANCHIPSET

EEPROM

AT24C08AN-10SI-2.7/S

Gigabyte Technology

Title: MARVELL 88E8001

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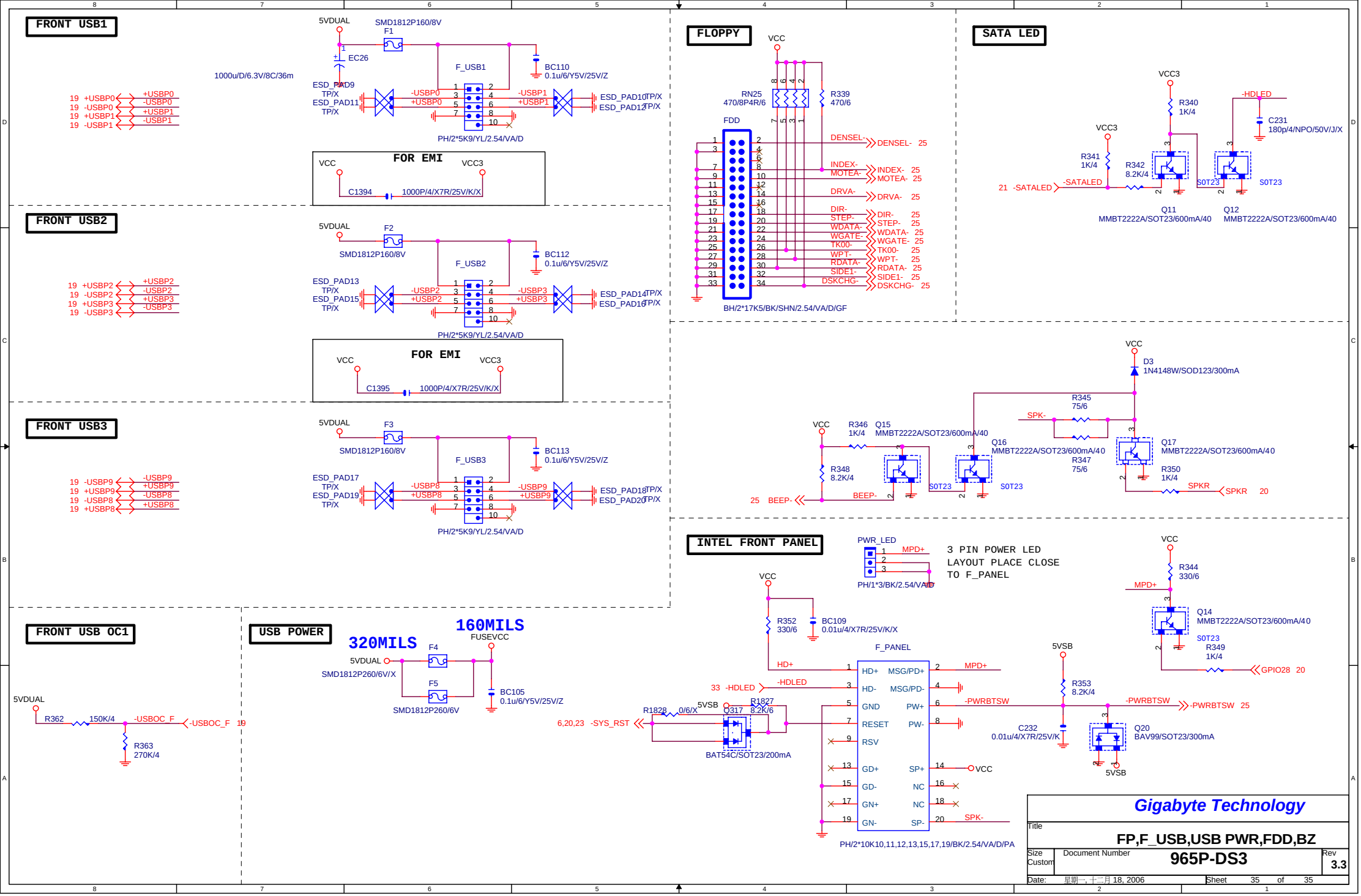
FRONT USB1
5VDUAL
SMD1812P160/8V
F1
EC26
1000u/D/6.3V/8C/36m
F_USB1
BC110
0.1u/6/Y5V/25V/Z
ESD_PAD9
ESD_PAD11
ESD_PAD10
ESD_PAD12
TP/X
PH/2*5K9/YL/2.54/VA/D
19 +USBP0
19 -USBP0
19 +USBP1
19 -USBP1
FOR EMI
VCC
VCC3
C1394
1000P/4/X7R/25V/K/X
FRONT USB2
F2
SMD1812P160/8V
F_USB2
BC112
0.1u/6/Y5V/25V/Z
ESD_PAD13
ESD_PAD15
ESD_PAD14
ESD_PAD16
19 +USBP2
19 -USBP2
19 +USBP3
19 -USBP3
C1395
FRONT USB3
F3
SMD1812P160/8V
F_USB3
BC113
0.1u/6/Y5V/25V/Z
ESD_PAD17
ESD_PAD19
ESD_PAD18
ESD_PAD20
19 -USBP9
19 +USBP9
19 -USBP8
19 +USBP8
FRONT USB OC1
R362
150K/4
-USBOC_F
R363
270K/4
USB POWER
160MILS
320MILS
FUSEVCC
F4
F5
SMD1812P260/6V/X
SMD1812P260/6V
BC105
0.1u/6/Y5V/25V/Z
FLOPPY
RN25
470/8P4R/6
R339
470/6
FDD
DENSEL-
INDEX-
MOTEA-
DRVA-
DIR-
STEP-
WDATA-
WGATE-
TK00-
WPT-
RDATA-
SIDE1-
DSKCHG-
BH/2*17K5/BK/SHN/2.54/VA/D/GF
SATA LED
R340
1K/4
R341
1K/4
R342
8.2K/4
C231
180p/4/NPO/50V/J/X
-HDLED
-SATALED
Q11
MMBT2222A/SOT23/600mA/40
Q12
MMBT2222A/SOT23/600mA/40
S0T23
D3
1N4148W/SOD123/300mA
R345
75/6
R346
1K/4
Q15
MMBT2222A/SOT23/600mA/40
R348
8.2K/4
Q16
MMBT2222A/SOT23/600mA/40
R347
75/6
Q17
MMBT2222A/SOT23/600mA/40
R350
1K/4
SPK-
SPKR
BEEP-
INTEL FRONT PANEL
PWR_LED
MPD+
3 PIN POWER LED
LAYOUT PLACE CLOSE
TO F_PANEL
PH/1*3/BK/2.54/VA/D
R352
330/6
BC109
0.01u/4/X7R/25V/K/X
F_PANEL
HD+
HD-
GND
RESET
RSV
GD+
GD-
GN+
GN-
MSG/PD+
MSG/PD-
PW+
PW-
SP+
SP-
NC
R1828
0/6/X
R1827
8.2K/6
Q317
BAT54C/SOT23/200mA
-SYS_RST
-PWRBTSW
R353
8.2K/4
C232
0.01u/4/X7R/25V/K
Q20
BAV99/SOT23/300mA
R344
330/6
Q14
MMBT2222A/SOT23/600mA/40
R349
1K/4
GPIO28
PH/2*10K10,11,12,13,15,17,19/BK/2.54/VA/D/PA
Gigabyte Technology
Title
FP,F_USB,USB PWR,FDD,BZ
Size
Custom
Document Number
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3.3
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