

GIGABYTE XP-K8U-X Schematics

REV:1.0 DATE: 94/04/04

SHEET	TITLE
1	COVER SHEET
2	BOM & PCB MODIFY HISTORY
3	BLOCK DIAGRAM
4,5,6,7	AMD K8 CLAWHAMMER
8 ~ 13	ULI M1689 SINGLE CHIP
14	CLOCK GENERATOR
15,16,17	DDR SDRAM DIMMS 1,2,3 & DDR Termination
18	AGP SLOT
19,20	PCI SLOT 1,2,3,4,5
21	IDE , FRONT USB , SATA
22	SMSC LPC I/O
23	BIOS & FDD
24	AUDIO AC97
25	AUDIO JACK & GAMEPORT
26	COM,PRT,KB/MS
27	RTL8100C & USB CONNECTOR
28	VCORE (PWM ISL6568CR)
29	FRONT PANEL
30	VCC12,VCC18,VCC25,VDDQ
31	ATX, DC POWER
32	DDR POWER(5VDUAL,3VDUAL,25VSTR,VTTDDR)
33	POWER SEQUENCE
34	R_USB , RESET
35	H/W SETTING

SHEET	TITLE

COMPONENT SIDE
(0.5 oz. Copper)
VCC SIDE
(1 oz. Copper)
GND SIDE
(1 oz. Copper)
SOLDER SIDE
(0.5 oz. Copper)

AXPER

Title

COVER SHEET

Size Custom

Document Number

Date: Thursday, July 21, 2005

Rev 1.0

XP-K8U-X

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XP-K8U-X REV. 1.0

Component value change history

[illegible]

ULi M1689 single chip FOR AMD K8_754

Circuit or PCB layout change for next version

[illegible]

Title <Title>			
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ULi M1689 single chip FOR AMD K8_754

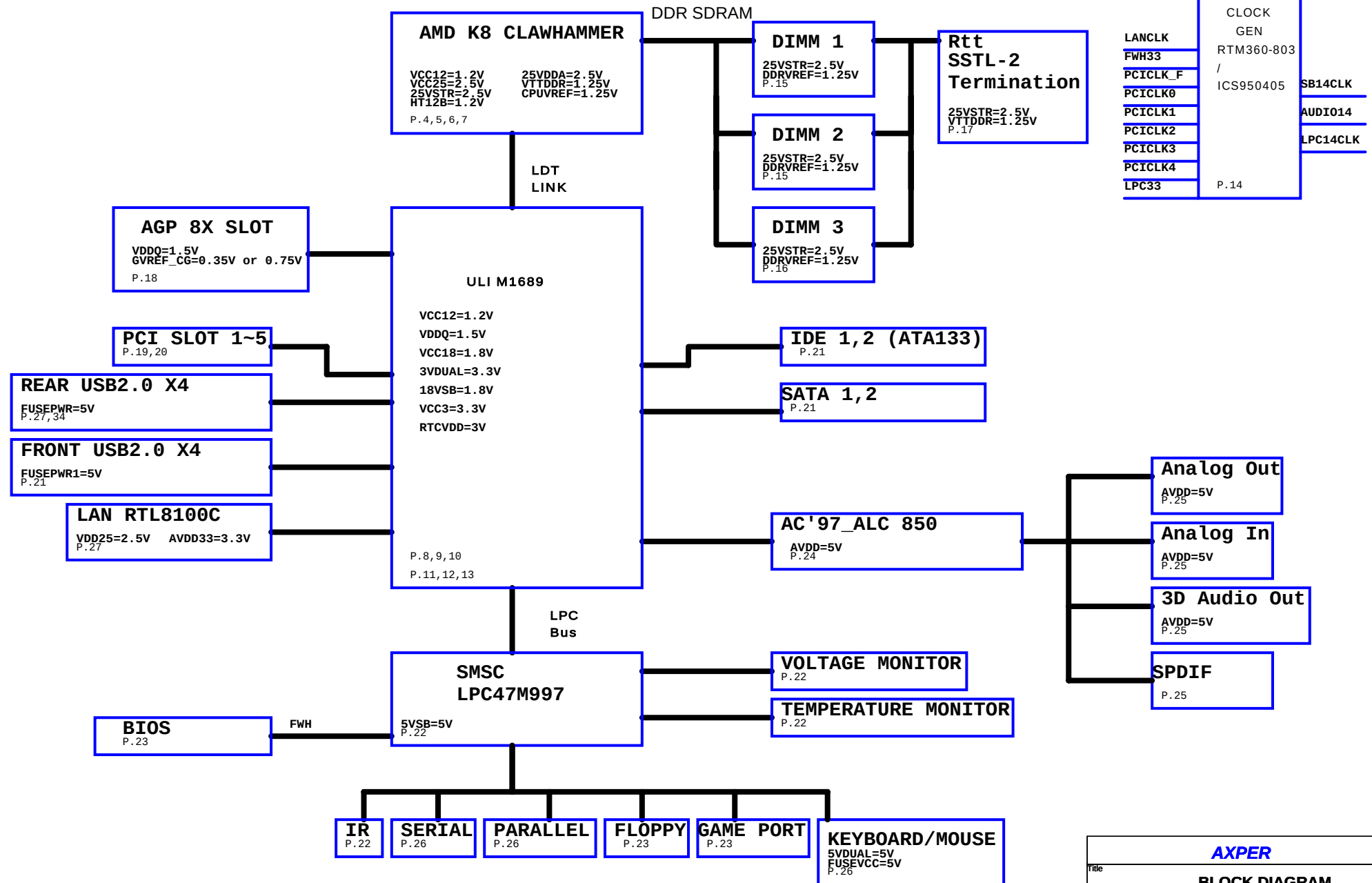
Circuit or PCB layout change for next version

[illegible]

AXPER				
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BOM & PCB MODIFY HISTORY				
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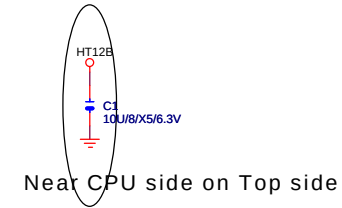
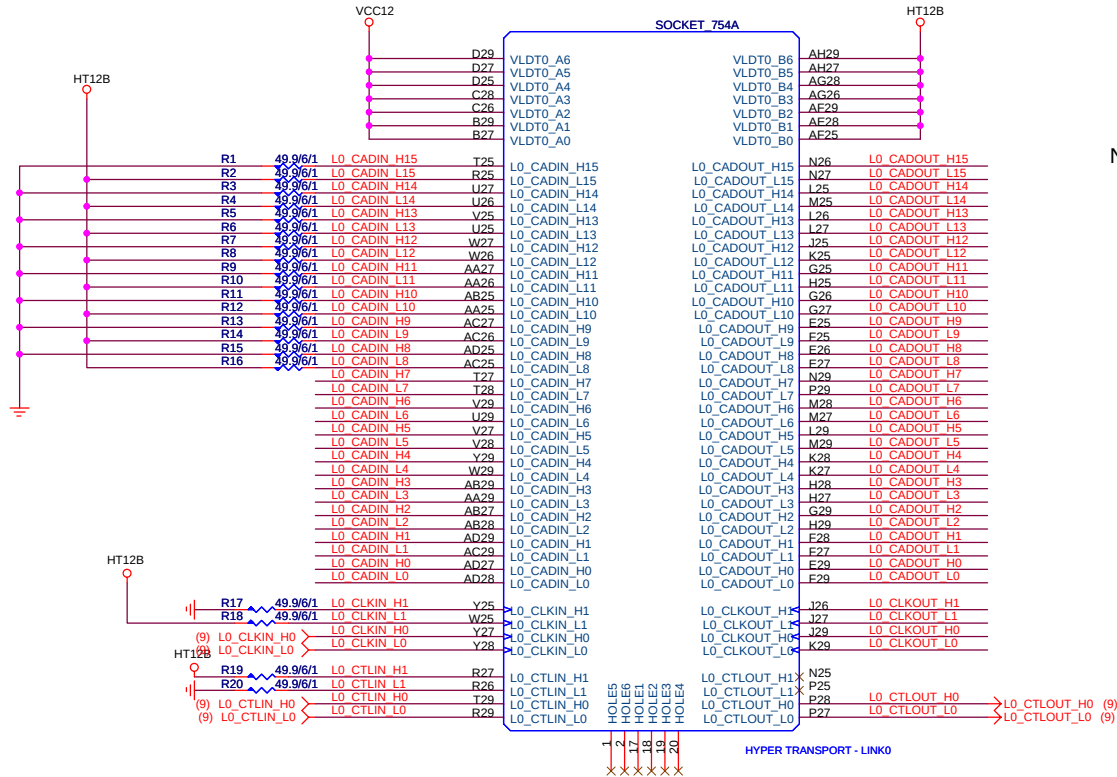
XP-K8U-X BLOCK DIAGRAM

System Block Diagram

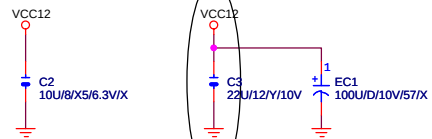


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BLOCK DIAGRAM			
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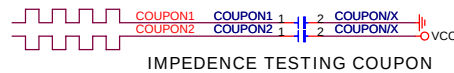
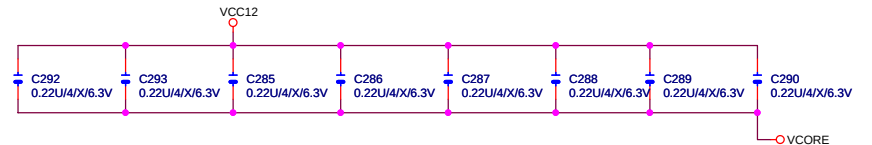
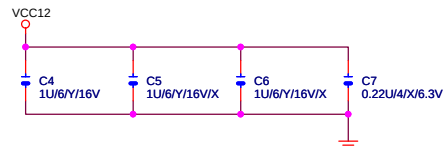
Clawhammer HT Interface



L0_CADIN_L[0..7] < L0_CADIN_L[0..7] (9)
L0_CADIN_H[0..7] < L0_CADIN_H[0..7] (9)
L0_CADOUT_L[0..15] < L0_CADOUT_L[0..15] (9)
L0_CADOUT_H[0..15] < L0_CADOUT_H[0..15] (9)
L0_CLKOUT_L[0..1] < L0_CLKOUT_L[0..1] (9)
L0_CLKOUT_H[0..1] < L0_CLKOUT_H[0..1] (9)

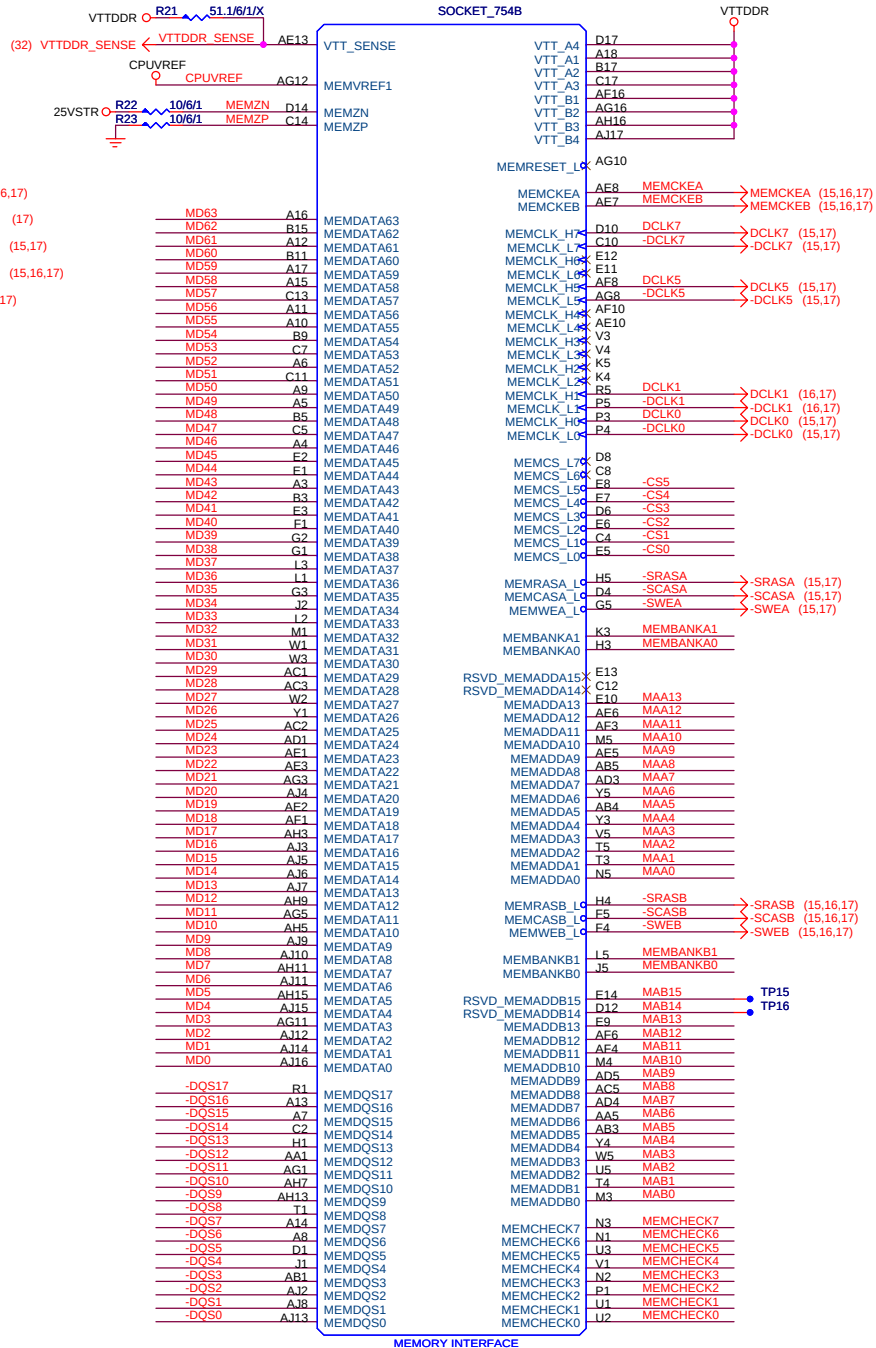


Near CPU side

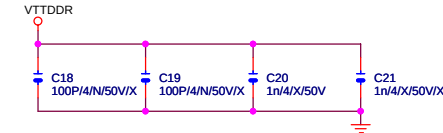
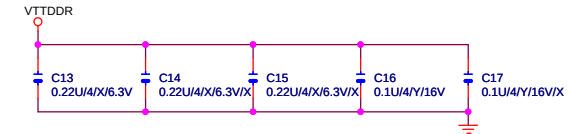
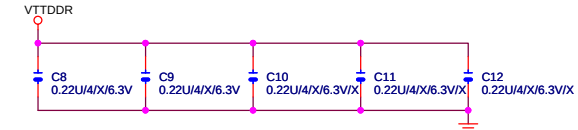


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K8 SOCKET 754-1			
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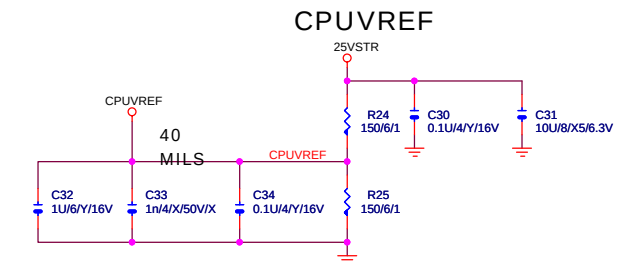
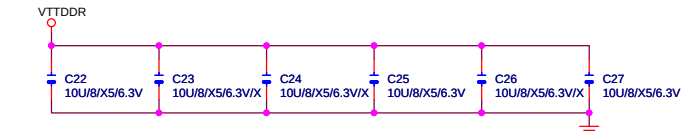
MD[0..63] ↔ MD[0..63] (17)
MAA[0..13] → MAA[0..13] (15,17)
-DQS[0..17] → -DQS[0..17] (17)



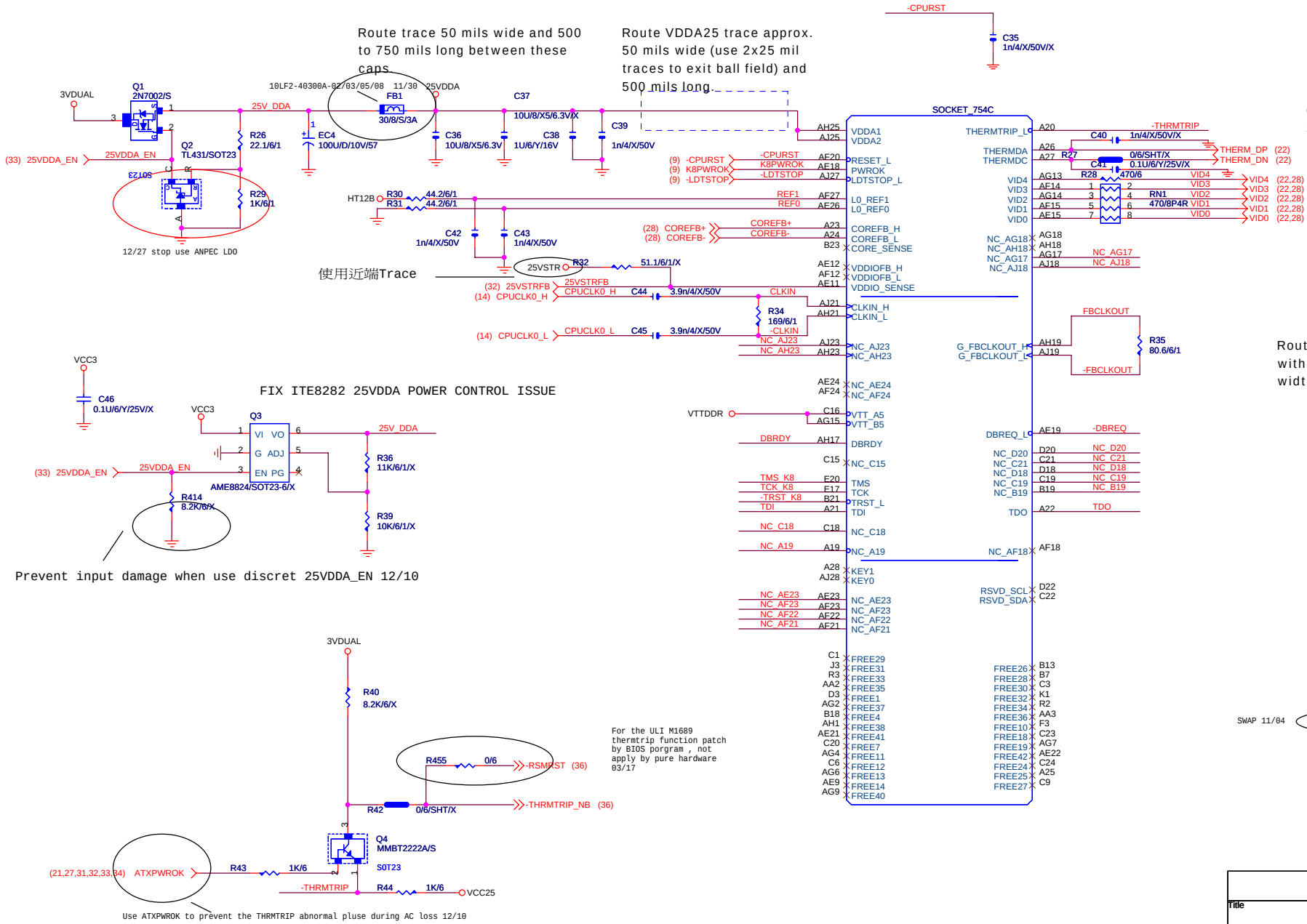
Place a cap every 0.5 in. on VTTDDR traces between CPU and DDR.



Locate close to CPU socket

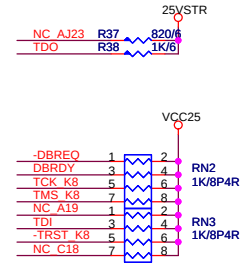


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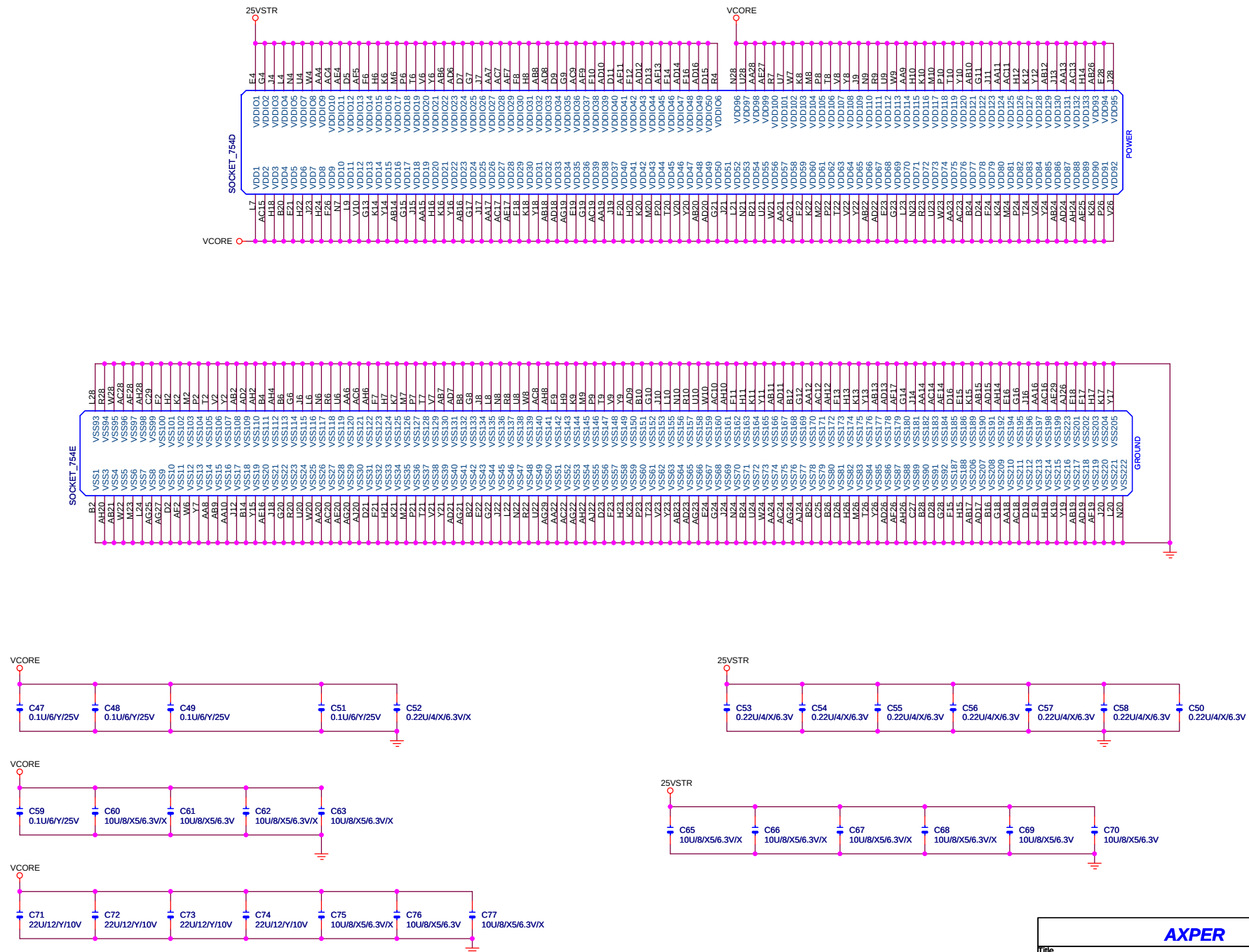
C548,C549 MUST NEAR SOCKET_754

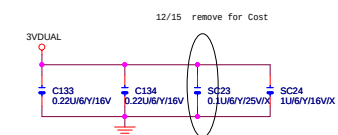
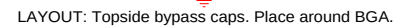
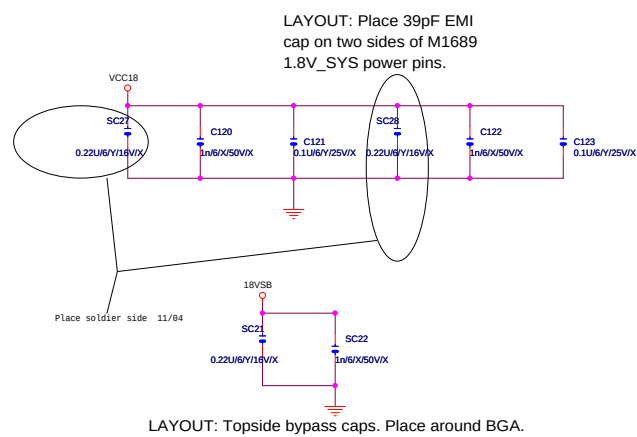
Route FBCLKOUT_H/L differentially with 20/8/5/8/20 spacing and trace width.



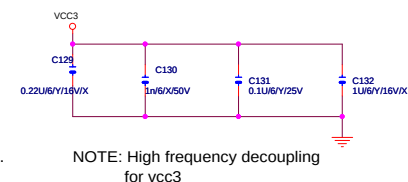
SWAP 11/04

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Title			
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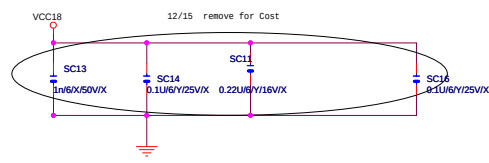
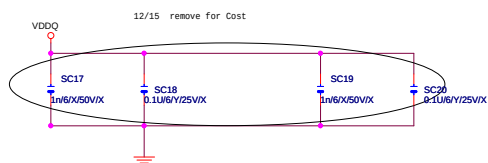
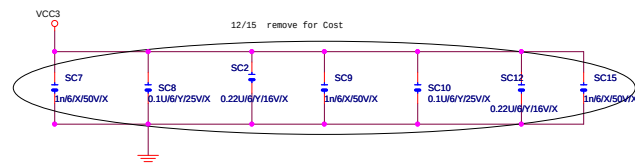
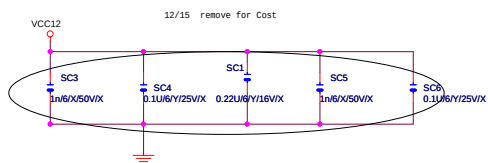


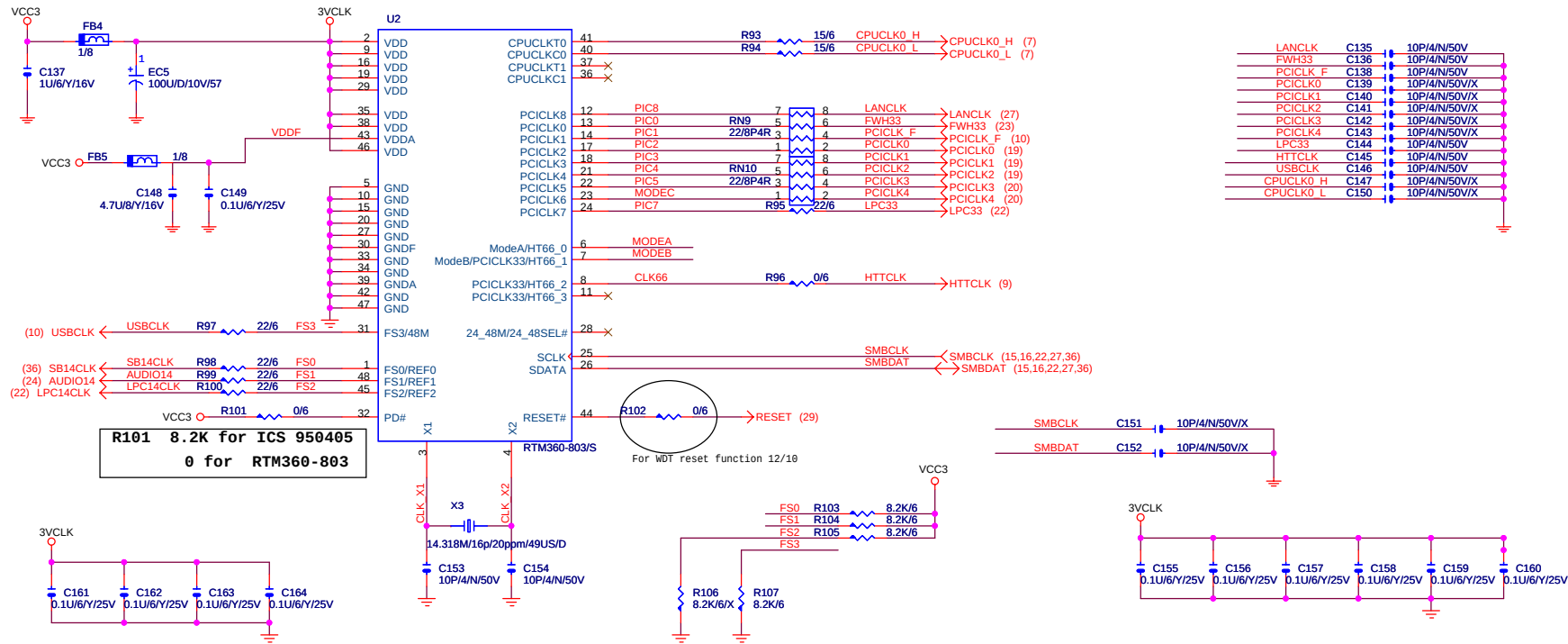


LAYOUT: Place caps on backside of the board.



NOTE: High frequency decoupling
for vcc3





Internal PH *
Internal PL **

**	FS3	FS2	FS1	FS0	CPU MHz	HTT MHz	PCI MHz	
0	0	0	0	0	100.90	67.27	33.63	
0	0	0	1	0	133.90	66.95	33.48	
0	0	1	0	0	168.00	67.20	33.60	
0	0	1	1	0	202.00	67.33	33.67	
0	1	0	0	0	100.20	66.80	33.40	
0	1	0	1	0	133.50	66.75	33.38	
0	1	1	0	0	166.70	66.68	33.34	
0	1	1	1	0	200.40	66.80	33.40	Default
1	0	0	0	0	150.00	60.00	30.00	
1	0	0	1	0	180.00	60.00	30.00	
1	0	1	0	0	210.00	70.00	35.00	
1	0	1	1	0	240.00	60.00	30.00	
1	1	0	0	0	270.00	67.50	33.75	
1	1	0	1	0	233.33	66.67	33.33	
1	1	1	0	0	266.67	66.67	33.33	
1	1	1	1	0	300.00	75.00	37.50	

Internal PH *

24_48_sel	Pin 28	
0	48MHz	
1 *	24MHz	(Default)

Internal PH *

MODE_A	MODE_B	Pin 6	Pin 7	Pin 8	Pin 11	
0	0	HTTCLK0	HTTCLK1	HTTCLK2	PCICLK10	(Default)
0	1	MODE_A (Input Only)	HTTCLK1	HTTCLK2	HTTCLK3	
1	0	PCICLK7	PCICLK8	PCICLK9	PCICLK10	
1 *	1 *	MODE_A (Input Only)	PCICLK8	PCICLK9	PCICLK10	

MODEC only for RTM360-803

MODEC	Pin 23	Pin 24	
0	33MHz	33MHz	(Default)
1	33MHz	PCI_STOP#	

R408 N/A for ICS 950405
PD 8.2K for RTM360-803

AXPER

CLOCK GEN

XP-K8U-X

Rev 1.0

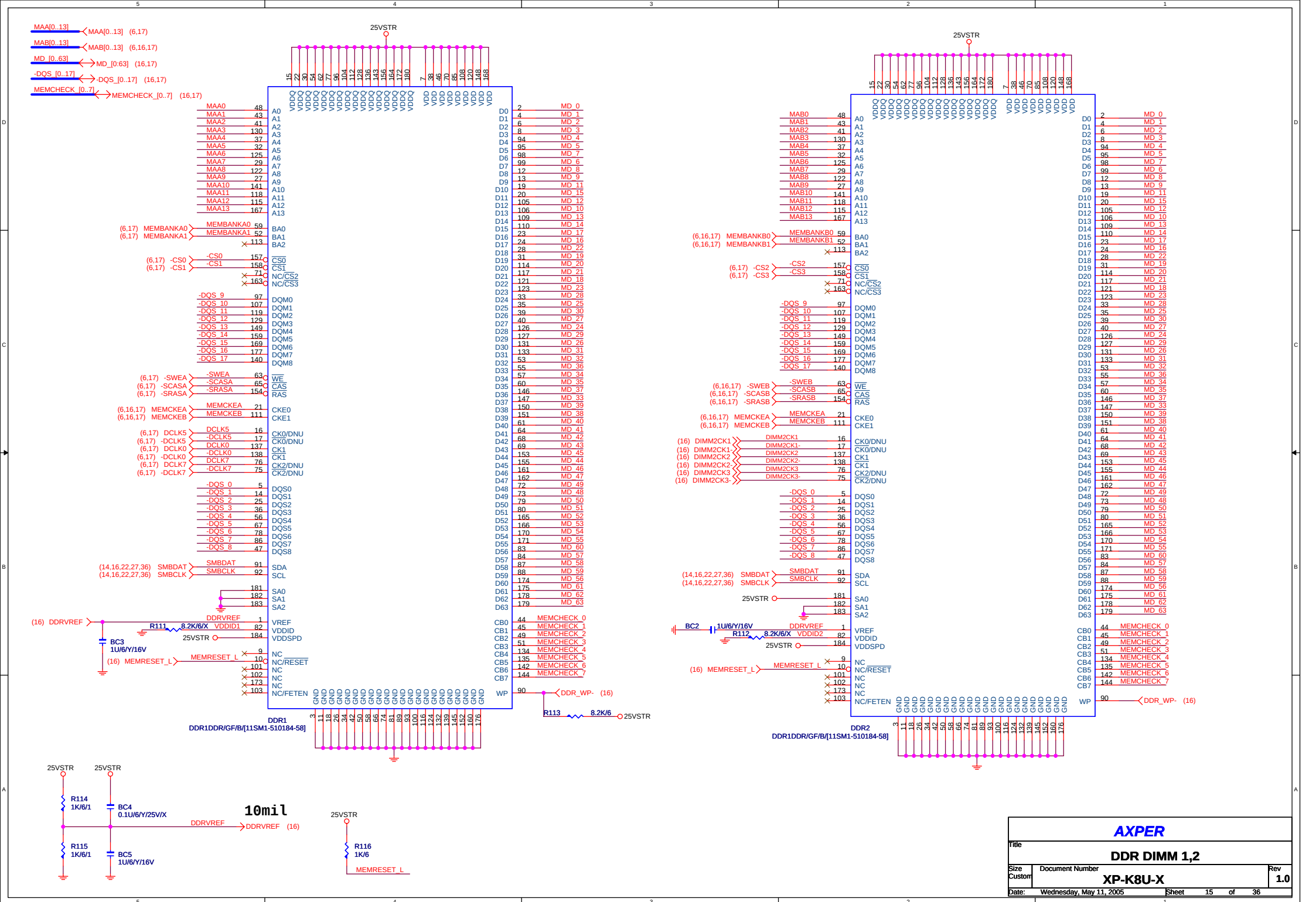
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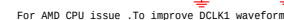
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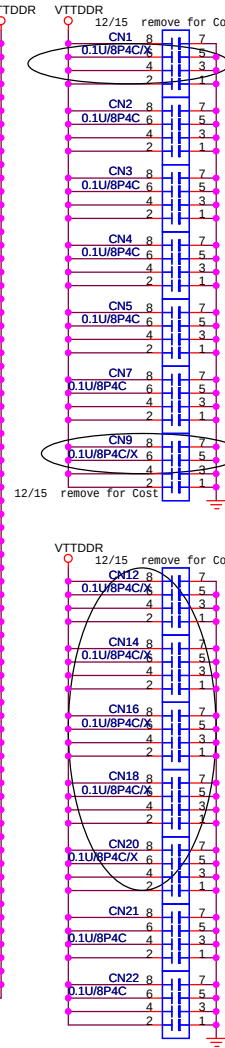
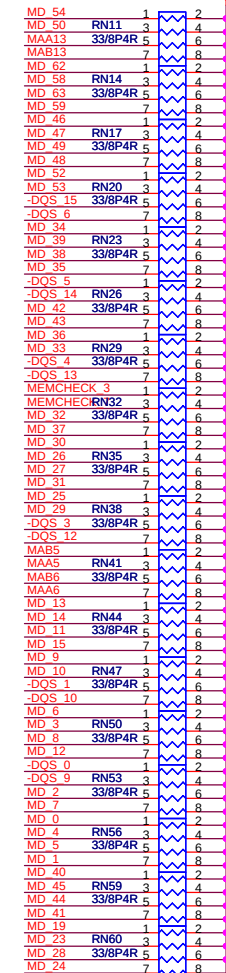
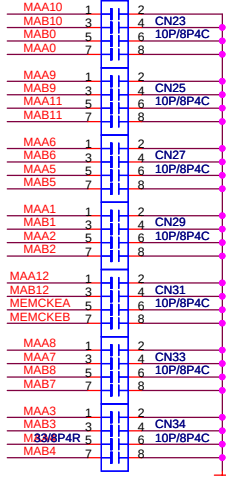
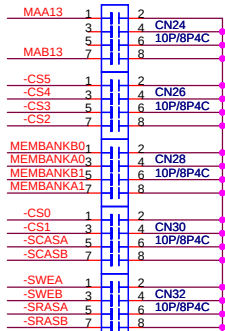
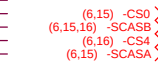
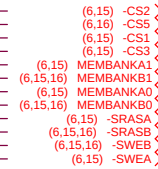
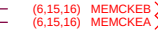
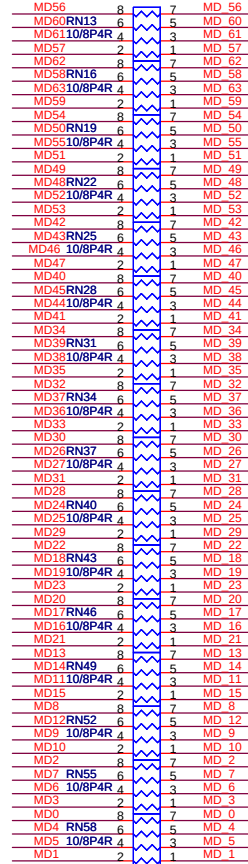
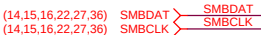
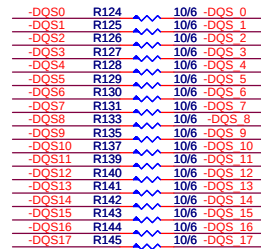
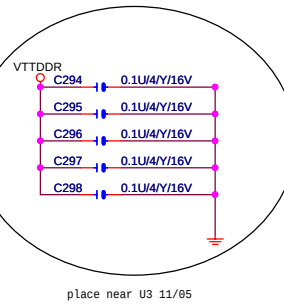
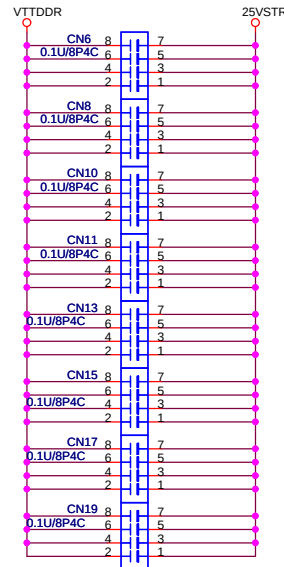
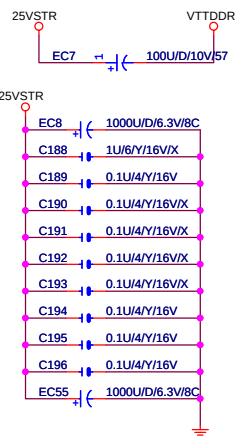
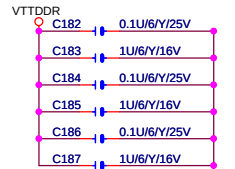
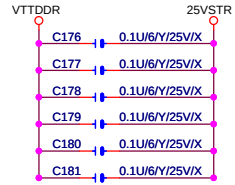
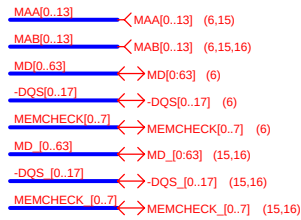
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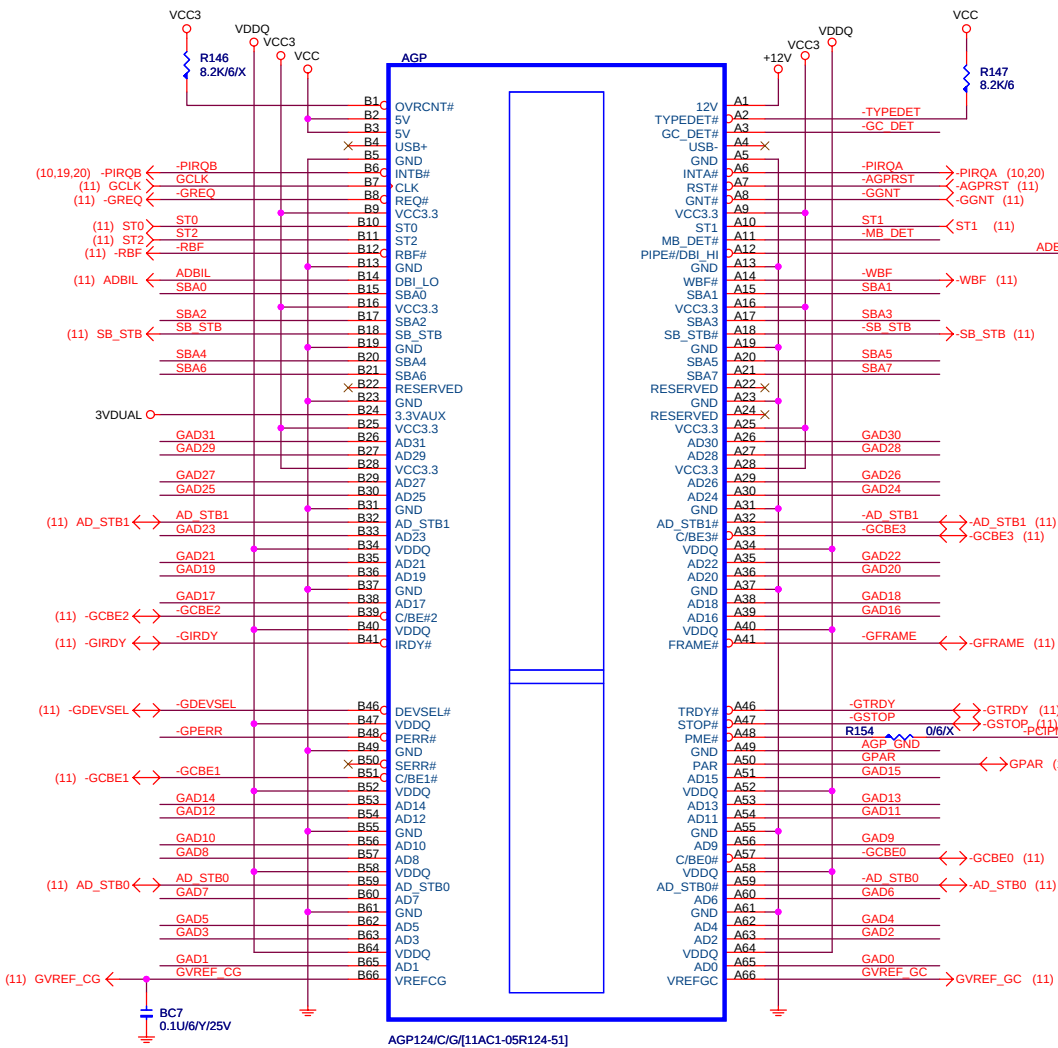
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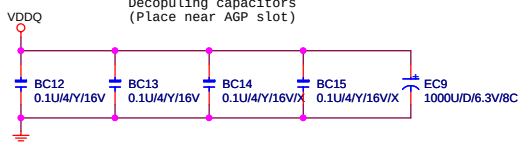






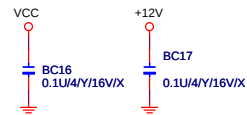
Place 1 at each pair of 3.3V pins

Decoupling capacitors
(Place near AGP slot)

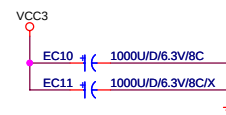


Place 1 at each pair of VDDQ pins

Place an additional for spread from A14 - A33

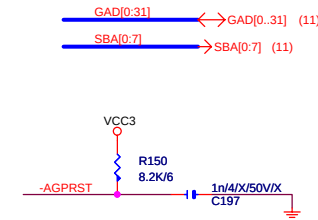


1000U Close
to AGP



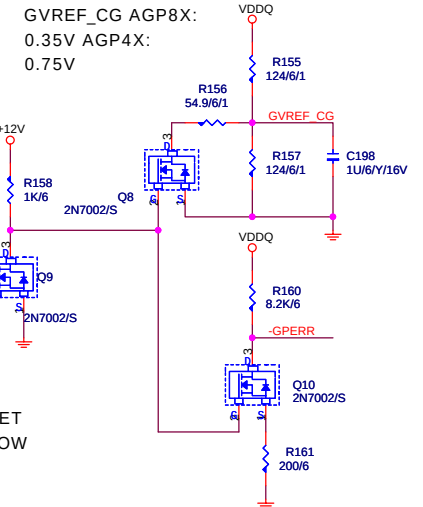
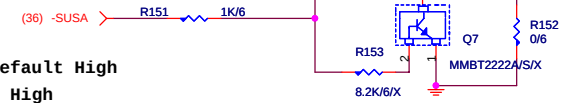
For R300

Add AGP 8X / 4X SELECTION



- 1.GP014 pin must power on default High
- 2.GP014 pin must Reset keep High
- 3.Dip switch default not mount

AGX_4X: OFF-->AUTO (GPI014=Hi)
ON -->Force 4X(GPI014=Lo)

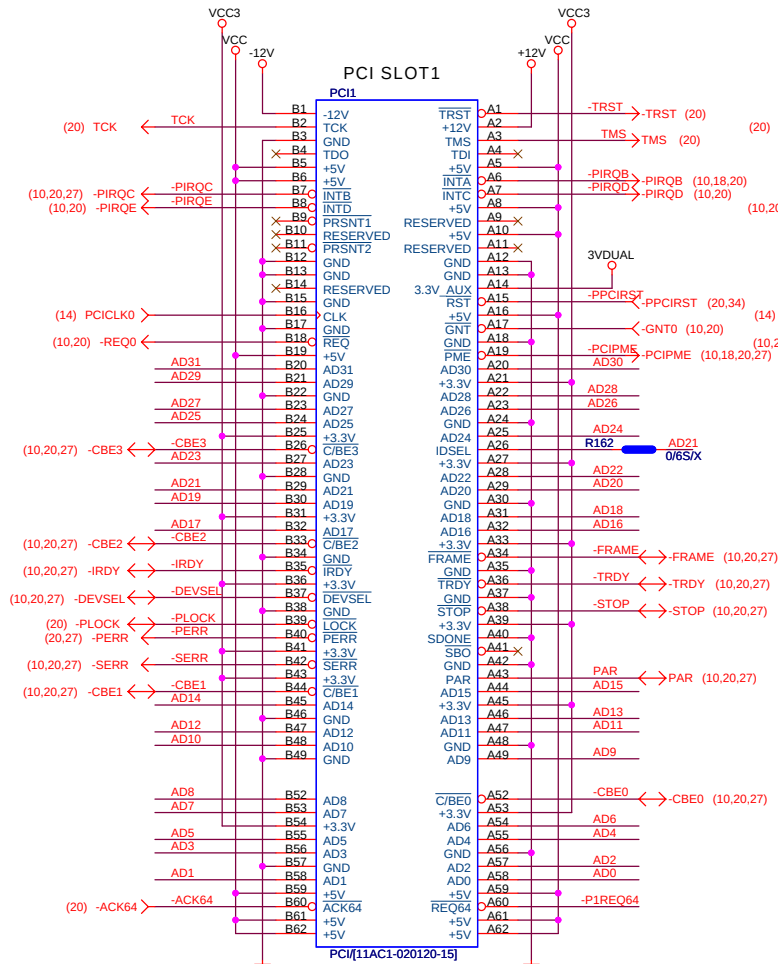


-AGP8XDET
AGP8X:LOW
Other:NC

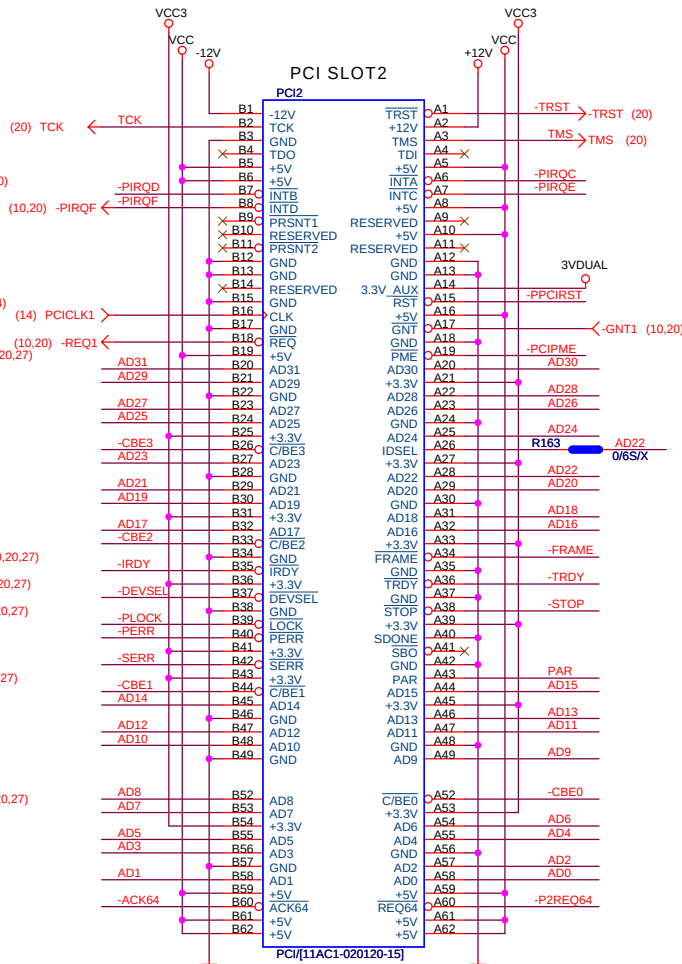
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AGP 8X SLOT			
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PCI SLOT 1,2,3

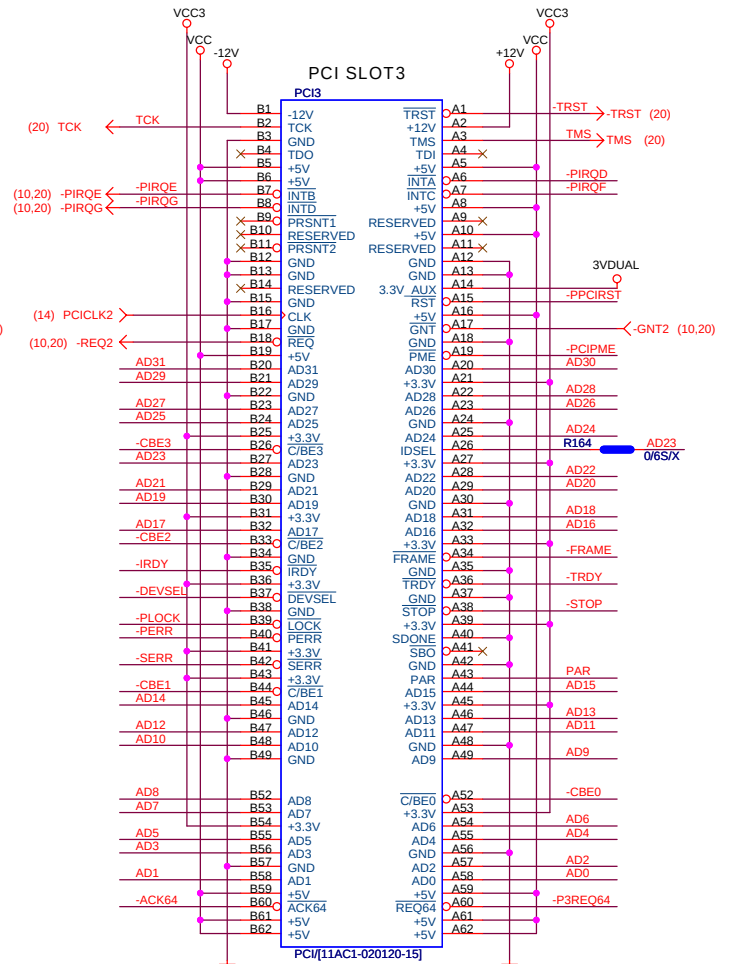
AD[0..31] ↔ AD[0..31] (10,20,27)



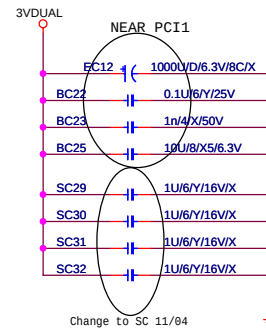
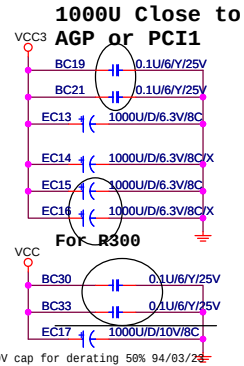
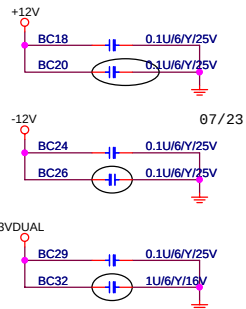
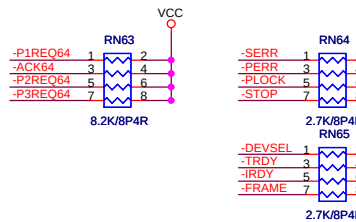
IDSEL(A21)



IDSEL(A22)

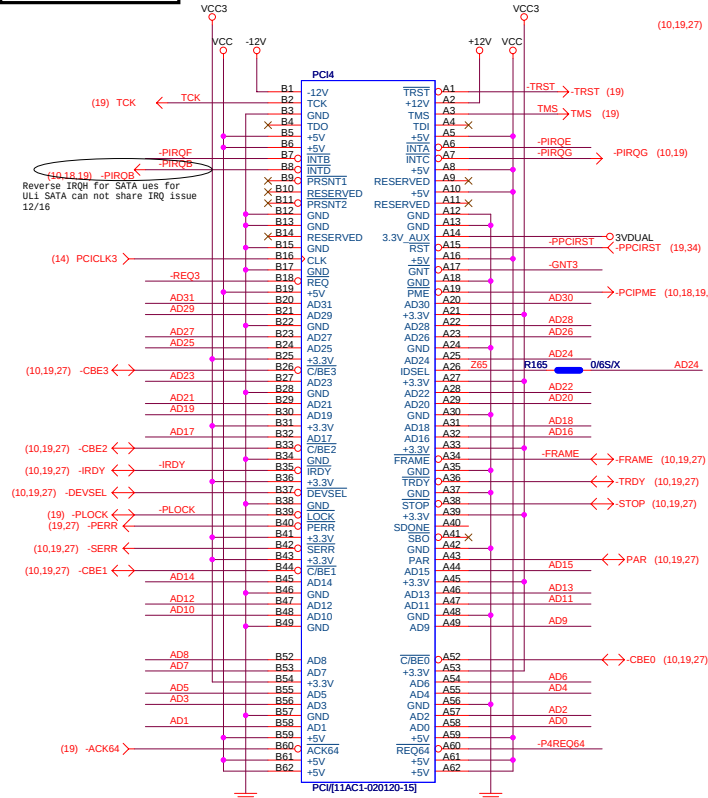
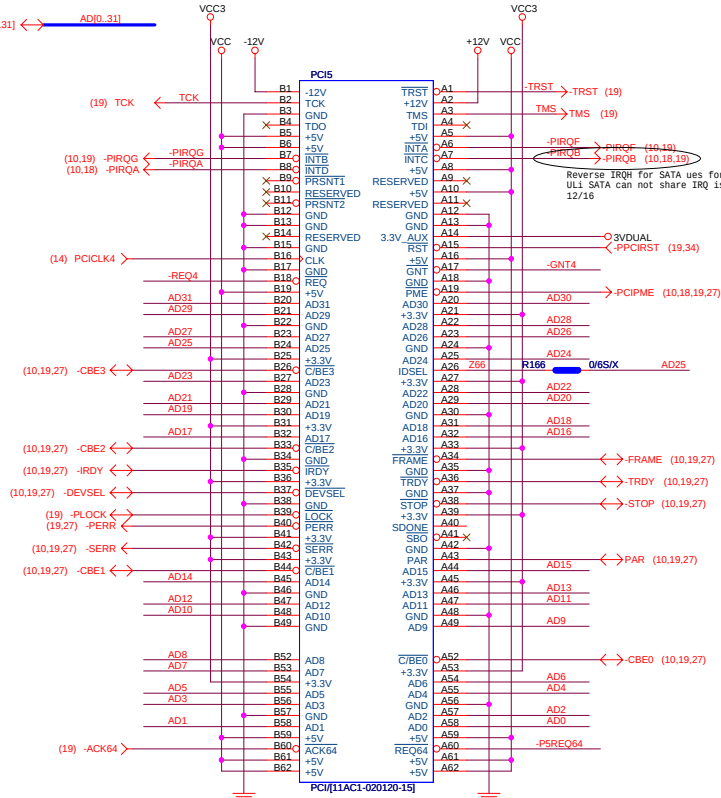
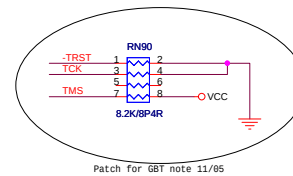
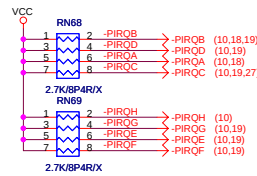
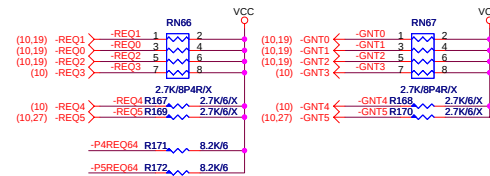


IDSEL(A23)



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PCI SLOT 1,2,3		
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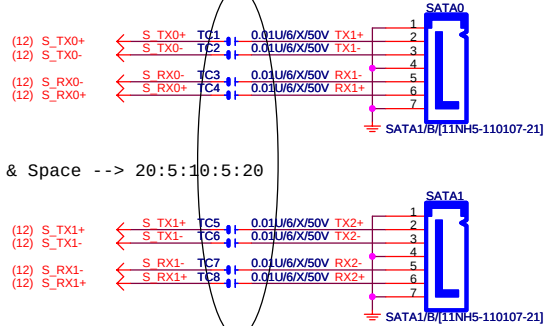
PCI SLOT 4,5

IDSEL(A24)
(A)IDSEL(A25)
(B)

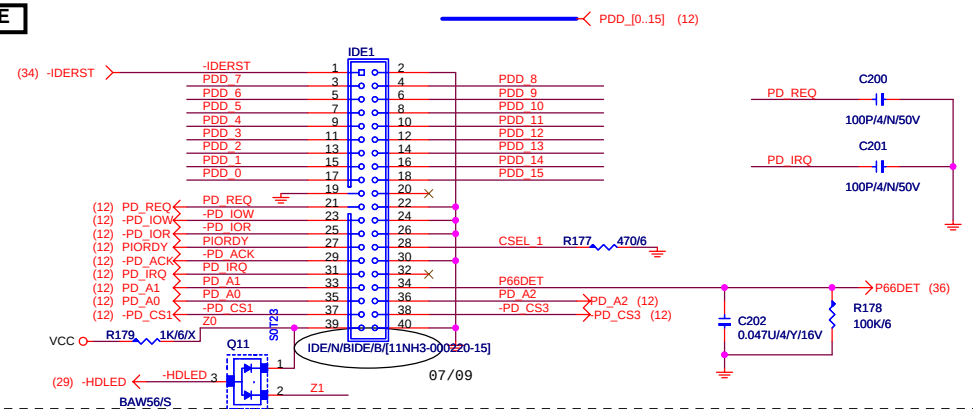
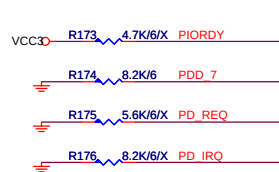
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Title			
PCI SLOT 4, 5			
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SATA

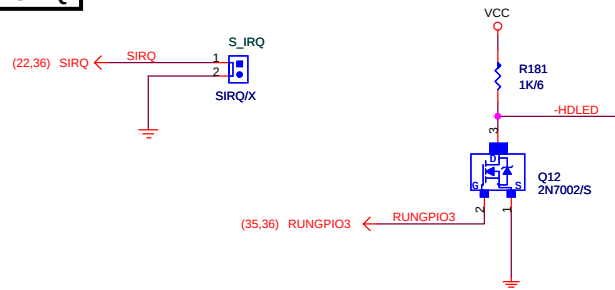
TC1-TC8 value change to 0.01U/6/X/50V from 0.01U/4/X/25V to fit footprint 11/30



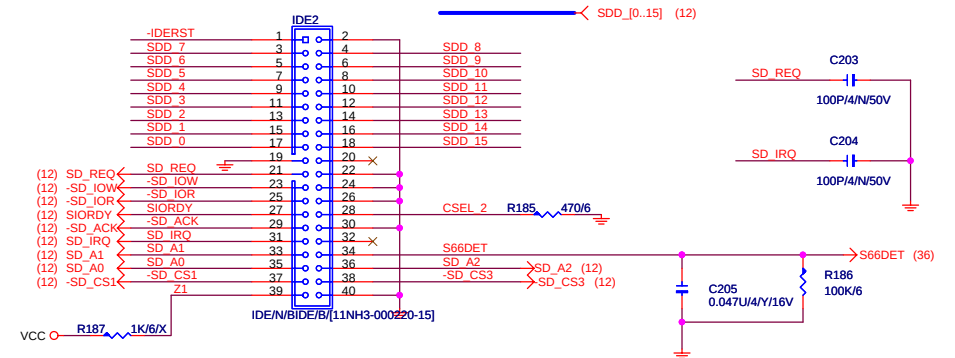
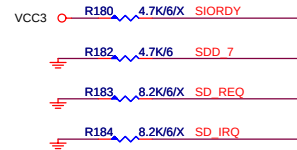
PRIMARY IDE



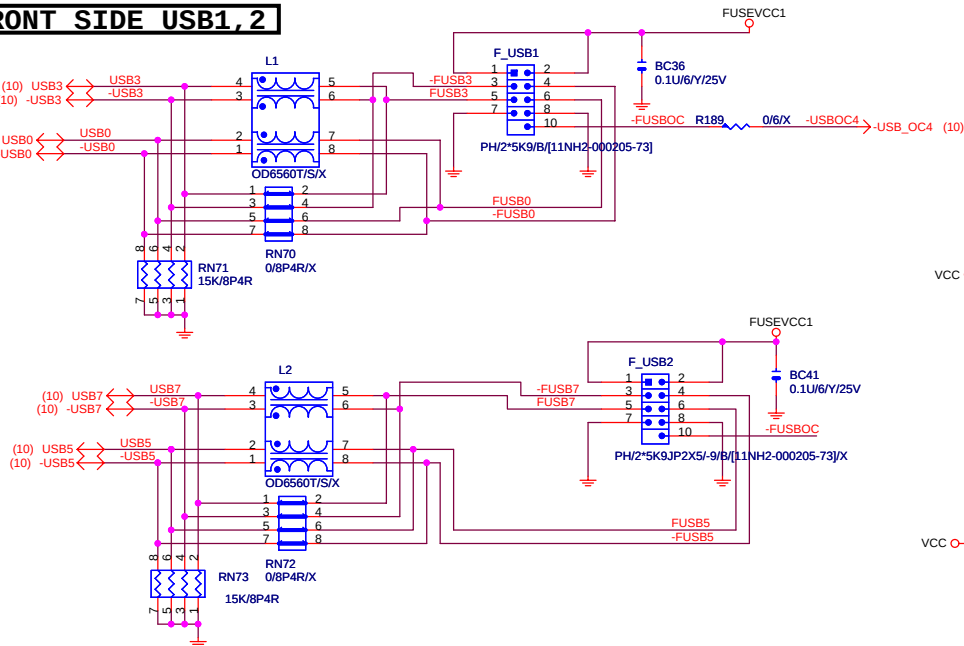
SIRQ



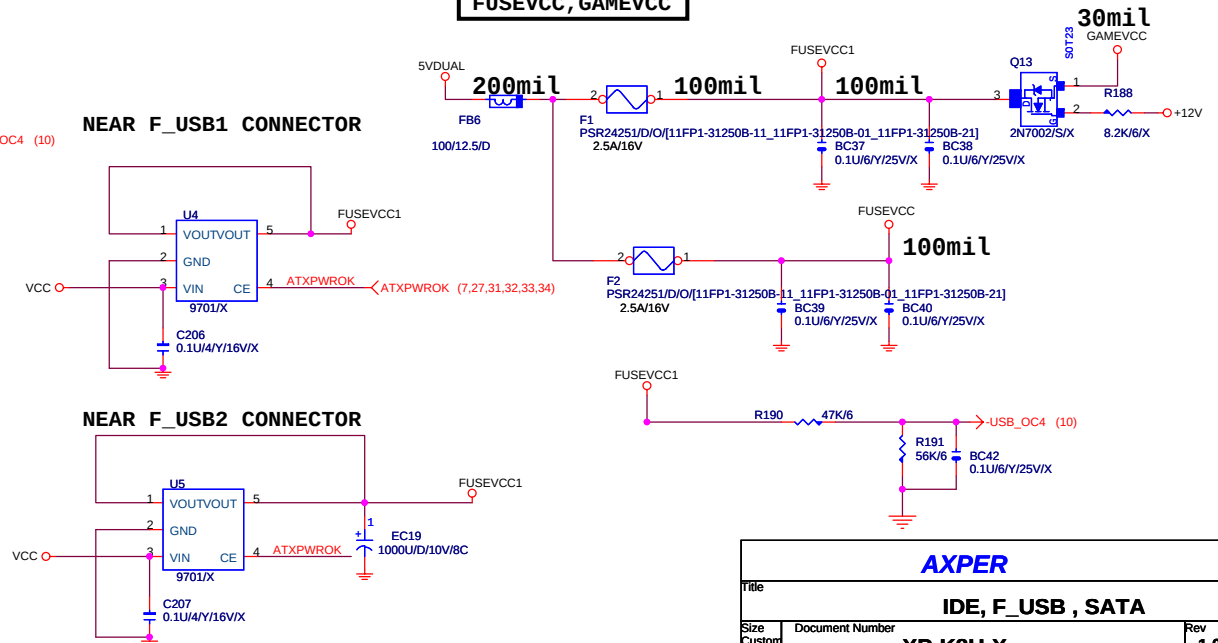
SECONDARY IDE



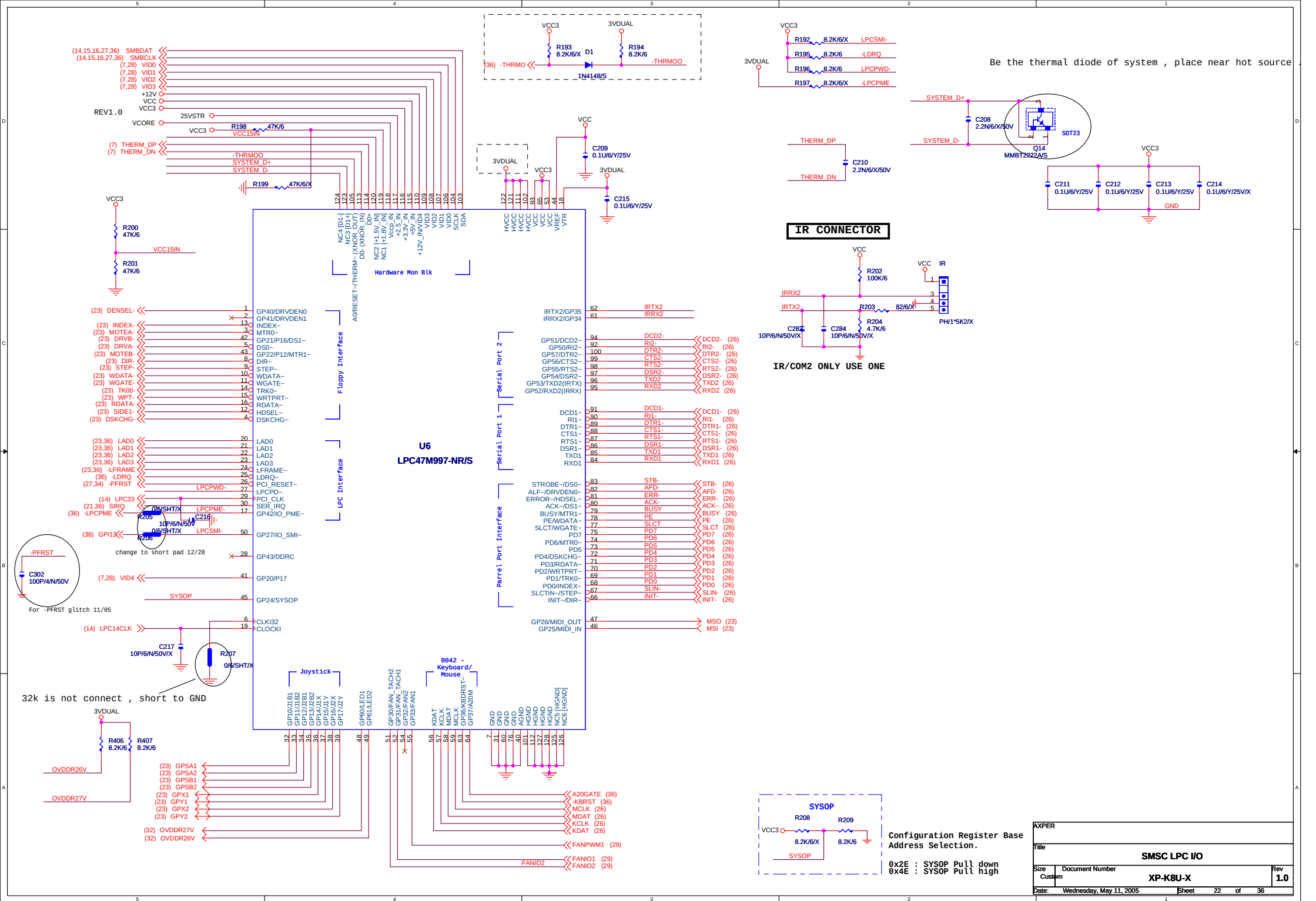
FRONT SIDE USB1, 2

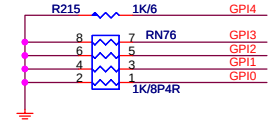
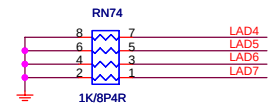


FUSEVCC, GAMEVCC

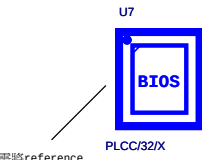


AXPER			
File			
IDE, F_USB, SATA			
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For -PCIRST glitch 11/05



需將reference 改成U7,也就是與BIOS同一參考,但是因為valu不同,在上件時會分成SMD階與DIP階 11/15



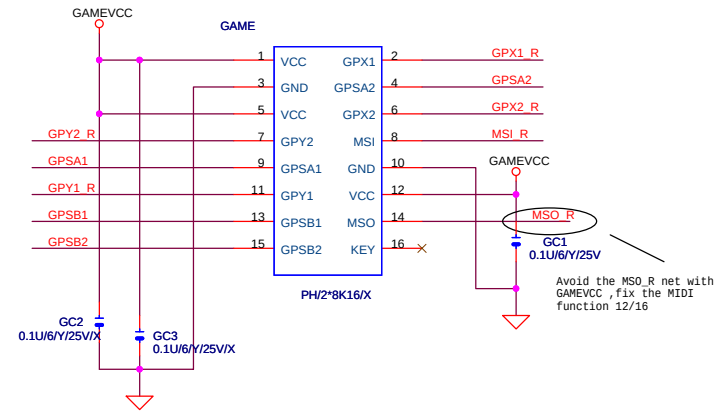
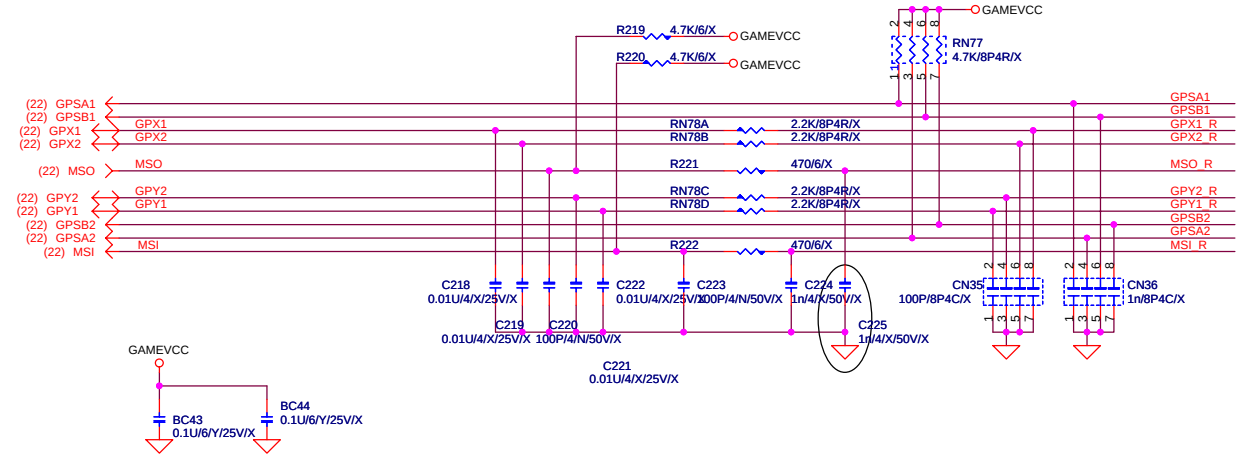
NOTE: INIT and RESET have the same function internally.

REV 1.0

BIOS_WP: BIOS WRITE PROTECT

PIN	BIOS_WP
1-2	WRITE PROTECT
2-3	WRITE ENABLE (default)

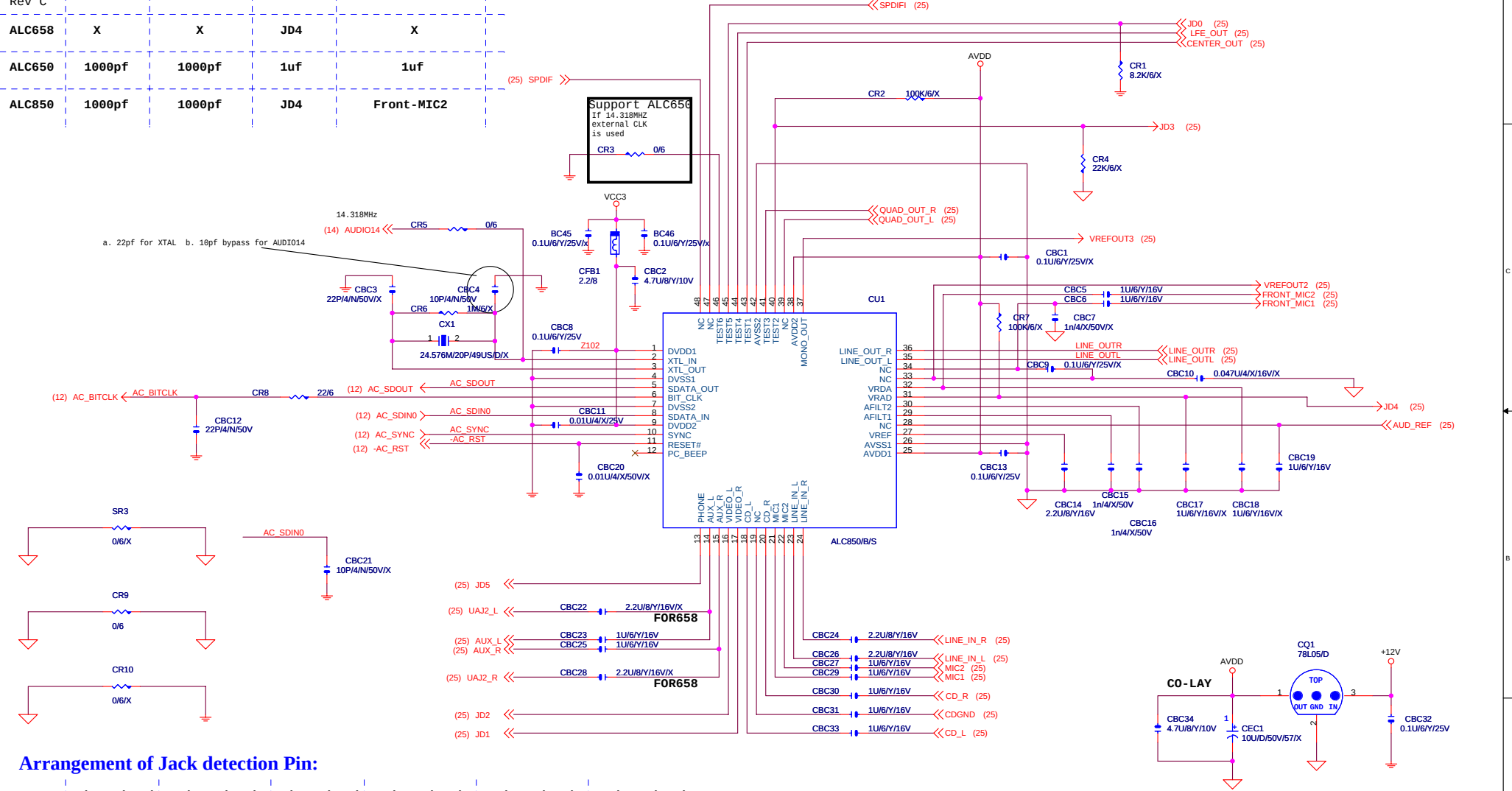
GAME PORT



AXPER			
File			
BIOS , FDD , GAME PORT			
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Filter Cap design:

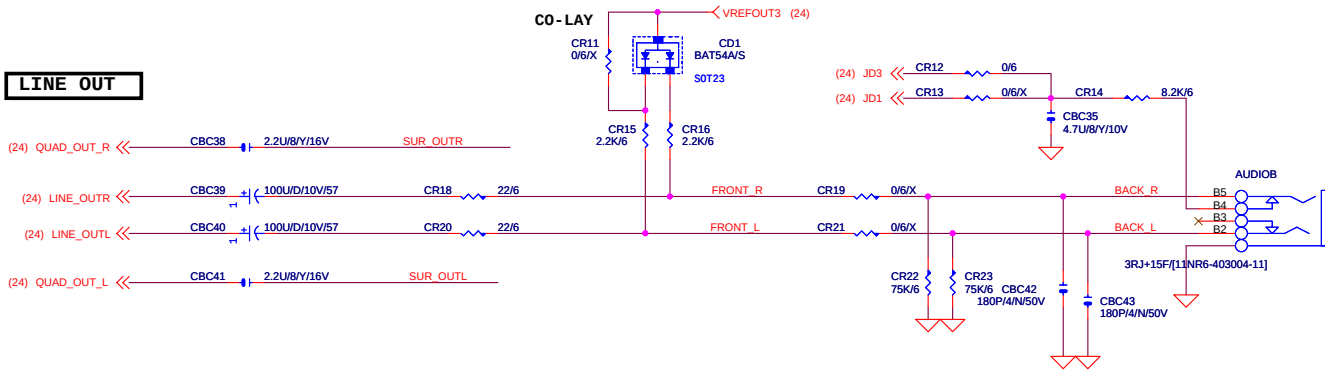
	Pin-29	Pin-30	Pin-31	Pin-32
ALC655 Rev D	1000pf	1000pf	1uf	Front-MIC2
ALC655 Rev C	1000pf	1000pf	1uf	X
ALC658	X	X	JD4	X
ALC650	1000pf	1000pf	1uf	1uf
ALC850	1000pf	1000pf	JD4	Front-MIC2



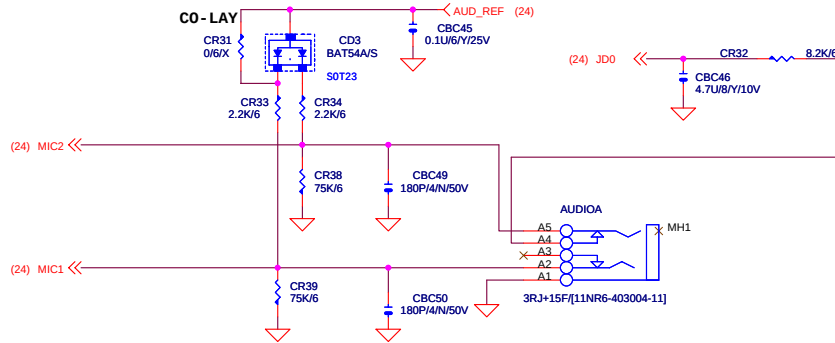
Arrangement of Jack detection Pin:

	Pin-45(JD0)	Pin-17(JD1)	Pin-16(JD2)	Pin-40(JD3)	Pin-31(JD4)	Pin-13(JD5)
ALC655	for MIC-IN	for FRONT-OUT	for LINE-IN			
ALC658	for MIC-IN	for UAJ1	for UAJ2	for FRONT-OUT	for LINE-IN	
ALC850	for MIC-IN	for Front Pannel OUT	for Front Pannel IN	for FRONT-OUT	for LINE-IN	for SurrBack Out

LINE OUT

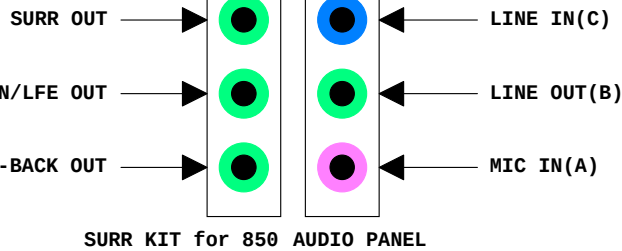


MIC



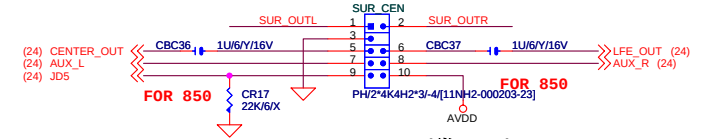
MICROPHONE IN SENSING(當INPUT)(利用vref 偏壓
與CR43, CR32 並聯求出阻抗)
7.1k ohm>R>2.3k ohm==>microphone in
R<2.3k ohm or R>7.1k ohm==>unknown device

MICROPHONE IN SENSING(當OUTPUT)
R>4K OHM=>POWER SPEAKER
4K OHM>R>400 OHM=>MICROPHONE
R<400 OHM=>HEADPHONE

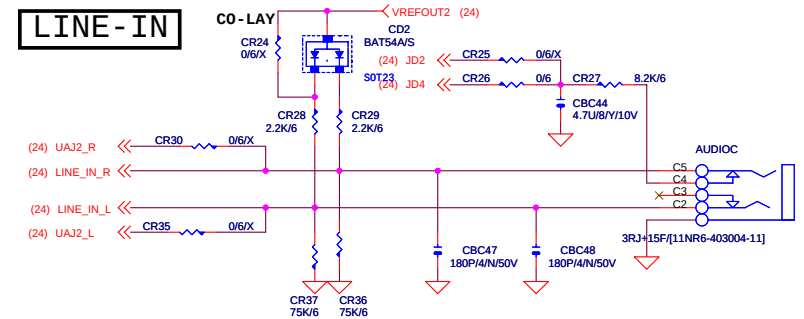


SURR KIT for 850 AUDIO PANEL

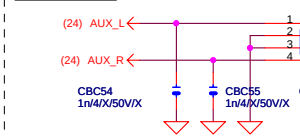
2x5 header for 850
For 850 if JD5 = low AUX-In is configured as input
For 850 if JD5 = high AUX-In is configured as output, Surr-Back out
FOR SUPPORT 6 CHANNEL,
SURROUND OUT
CENTER OUT, LOW FREQUENCY
EFFECT OUT



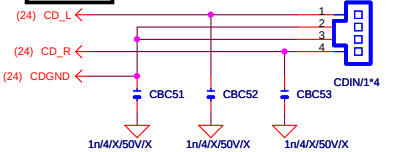
LINE-IN



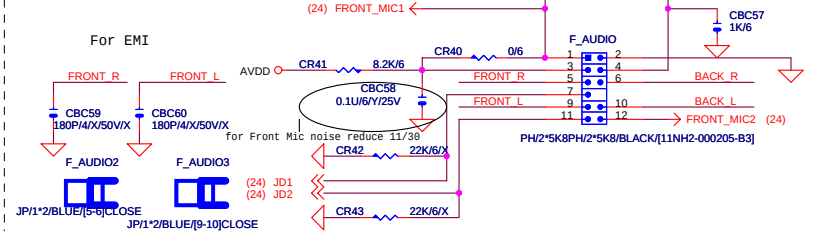
AUX IN DEFAULT NO POP



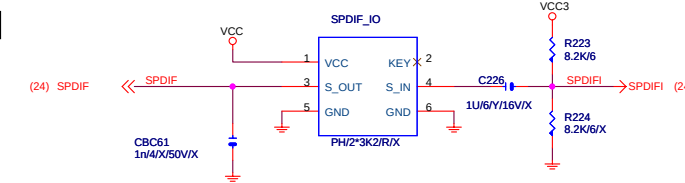
CD IN



INTEL FRONT AUDIO



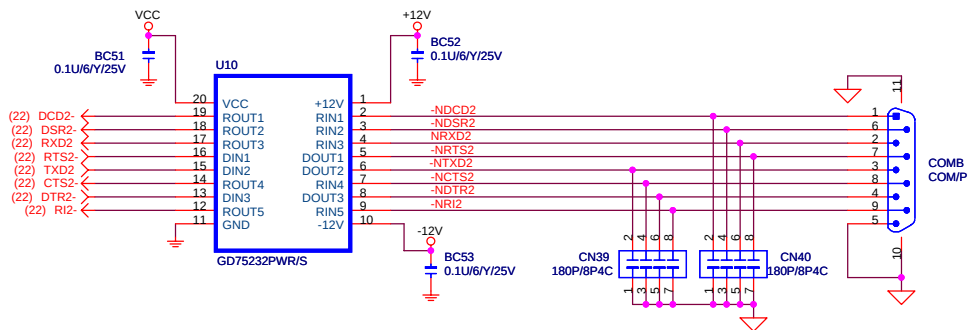
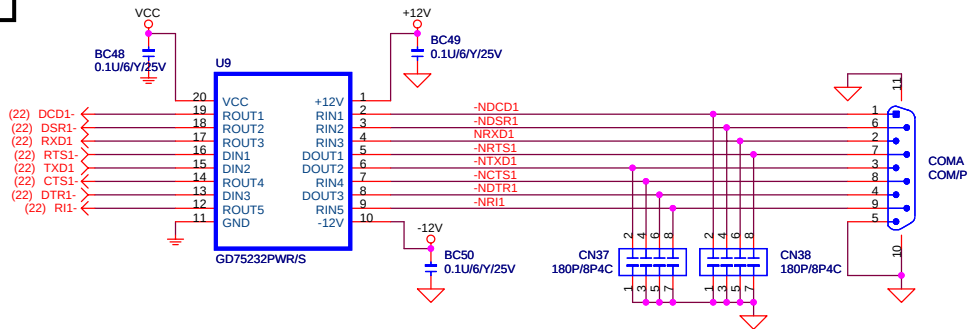
SPDIF



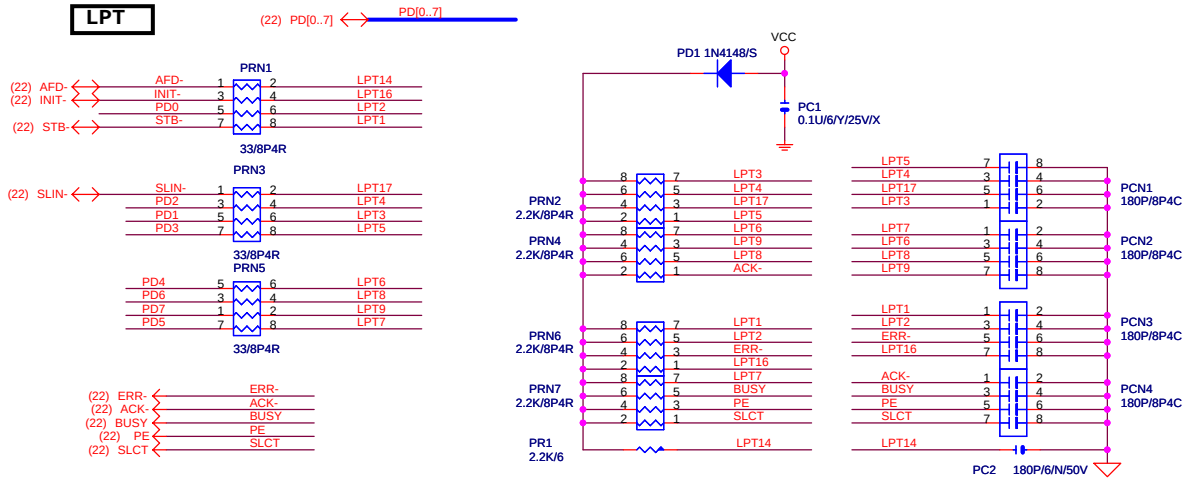
AXPER

Title			AUDIO OUTPUT, GAME PORT	
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COM A, B

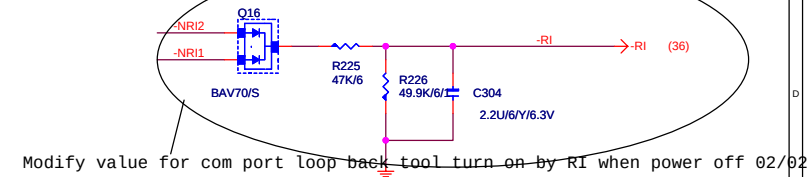


LPT

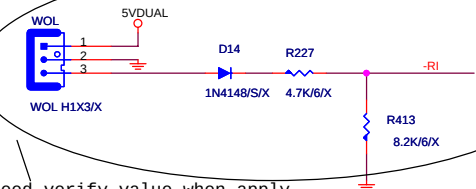


WAKE UP

-RI set to HIGH active, modify circuit .
11/30

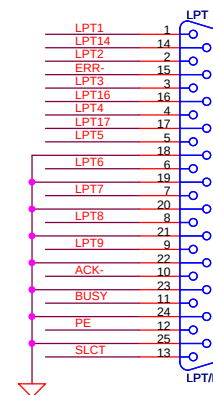
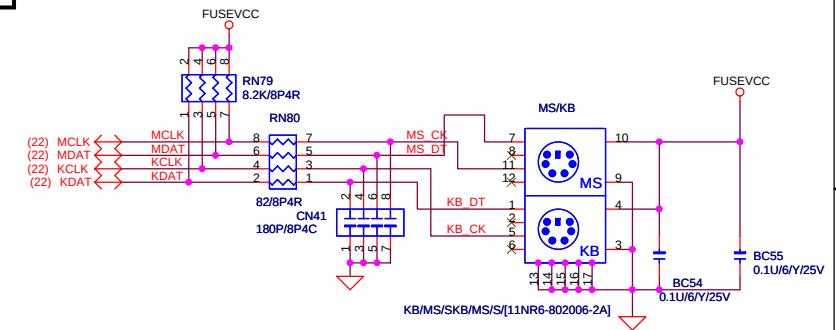


WAKE ON LAN



Need verify value when apply the function 02/02

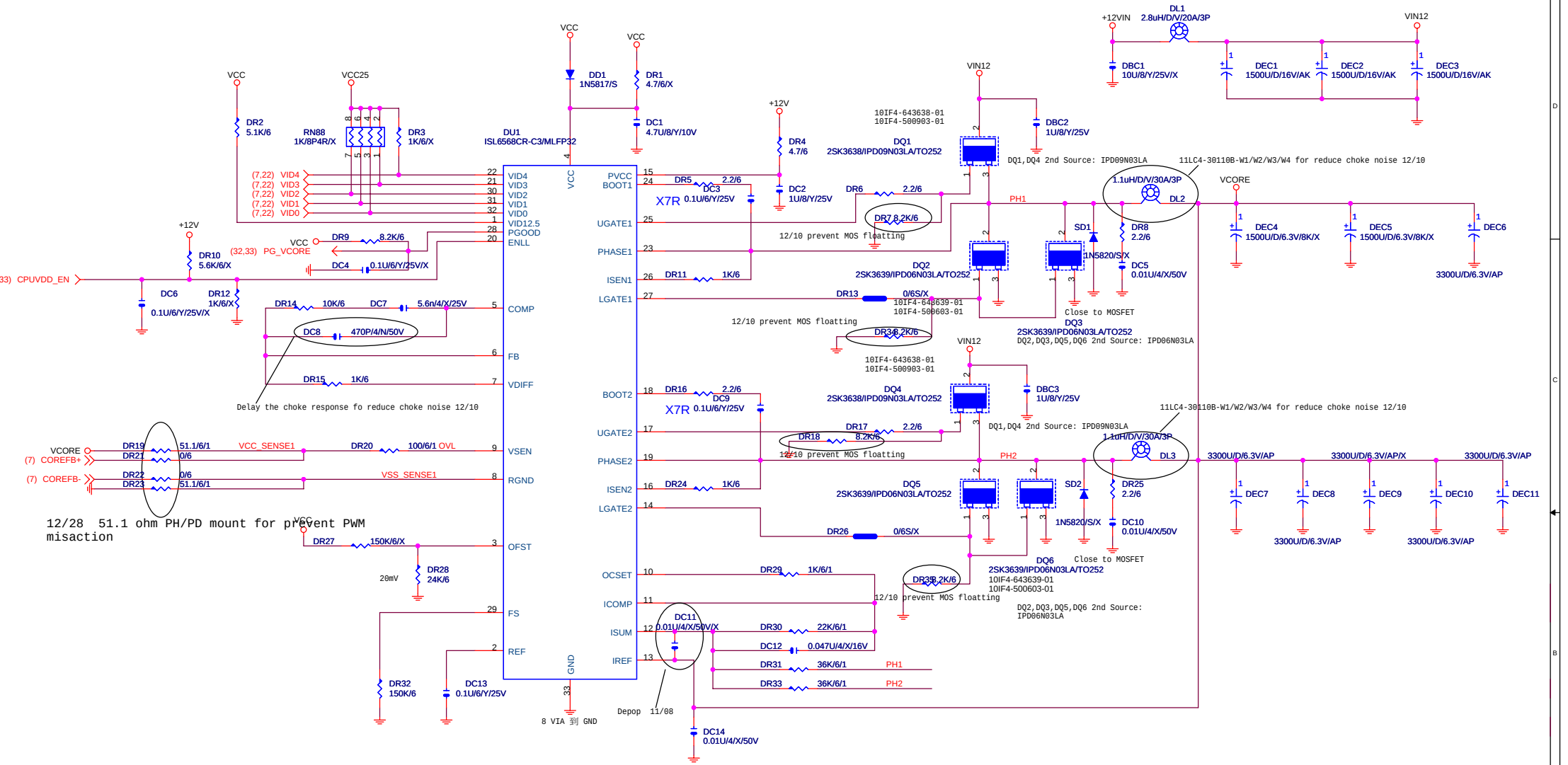
KBC/PS2

**AXPER**

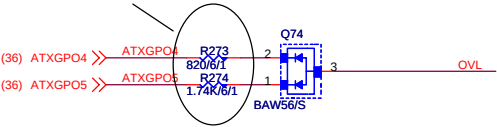
Title	COM,PRT,KB/MS,IR
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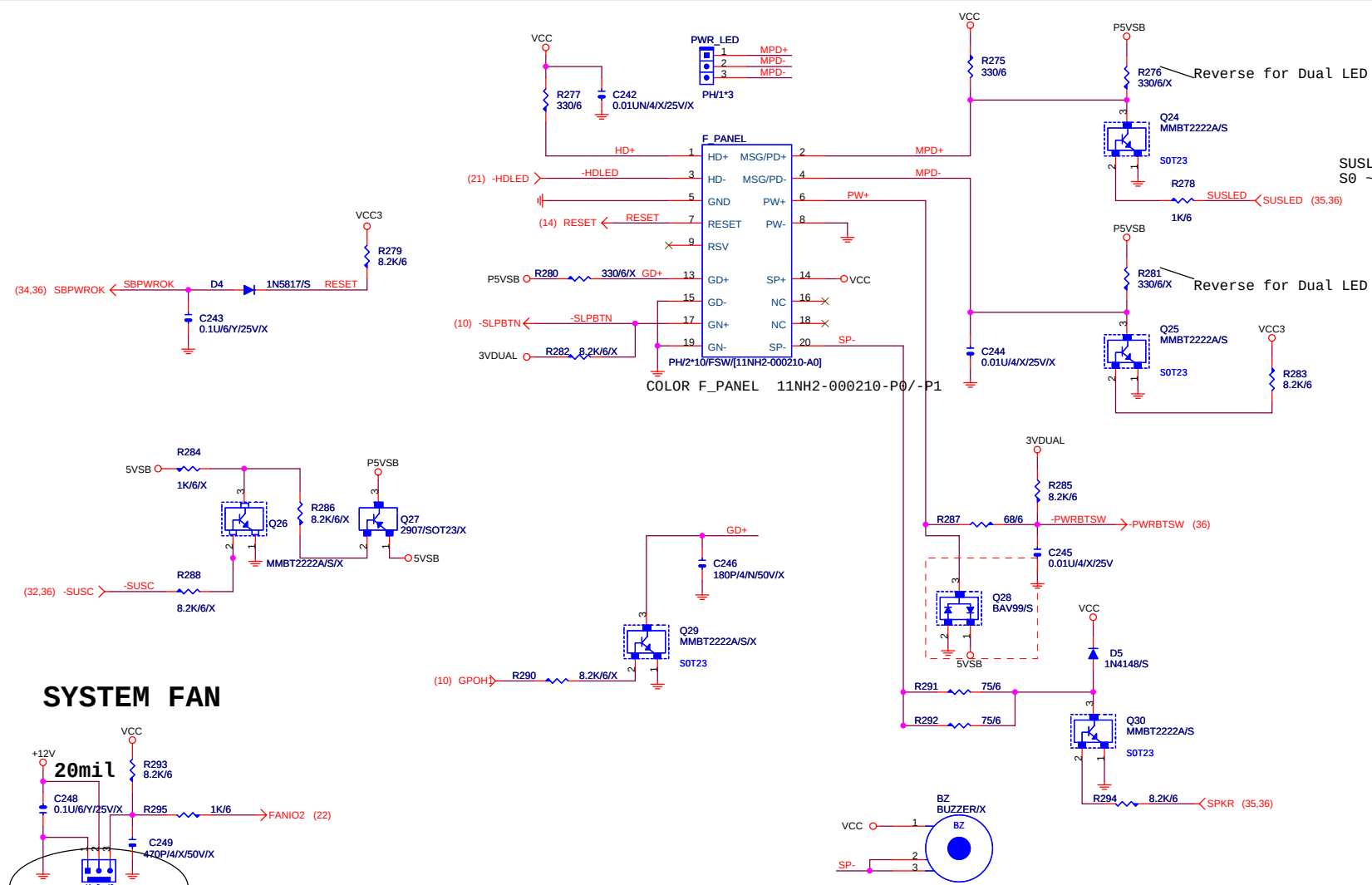
ATXGP05



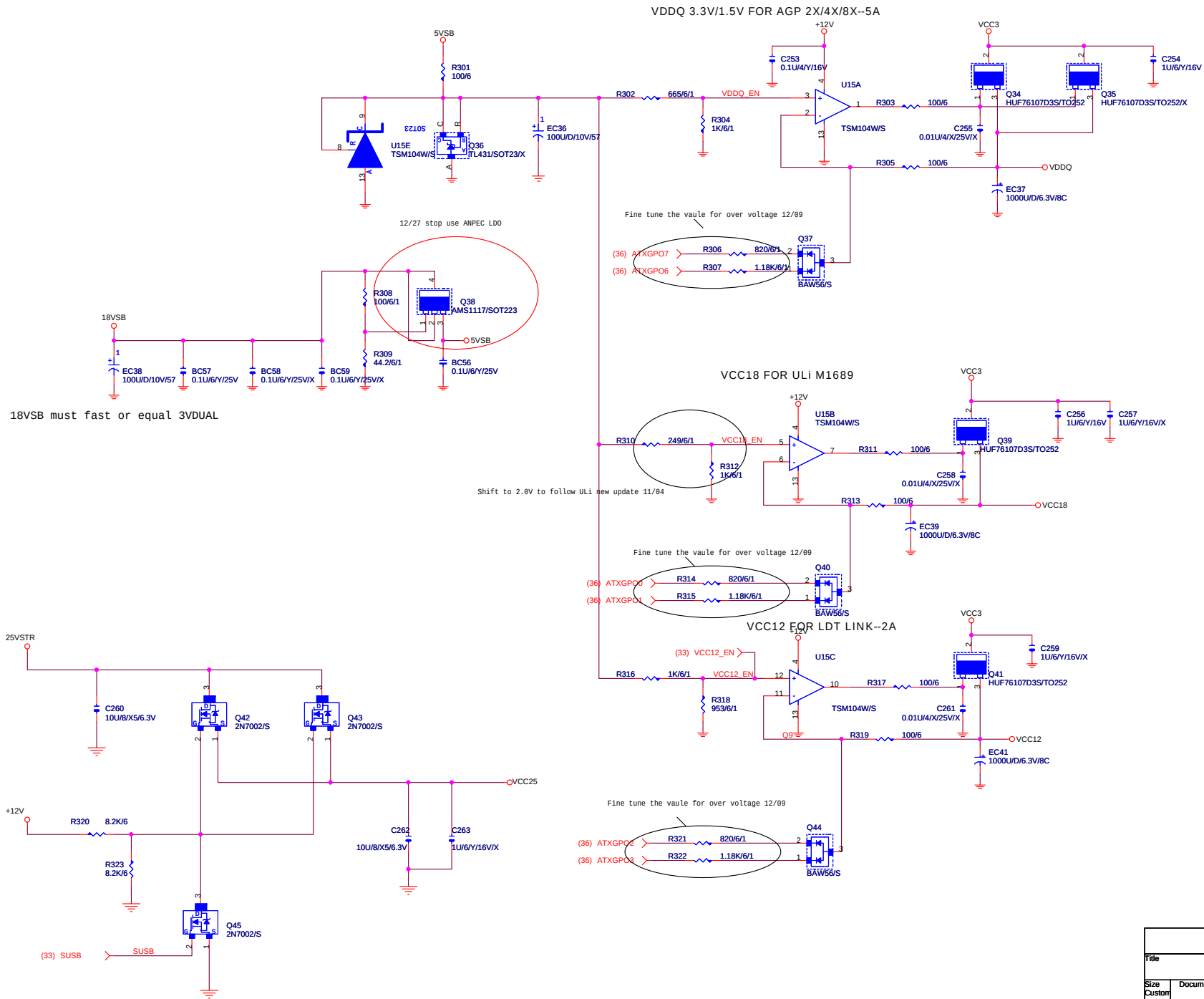
Fine tune the vaule for over voltage 12/09



	ATXGP04	ATXGP05
5%	HI	LO
7.5%	LO	HI
10%	LO	LO
Default	HI	HI



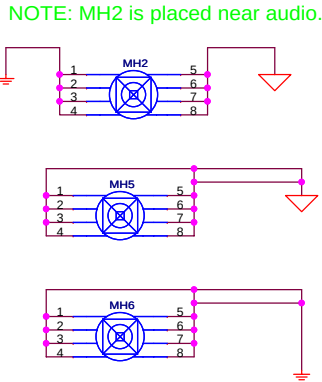
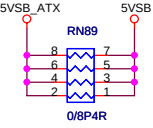
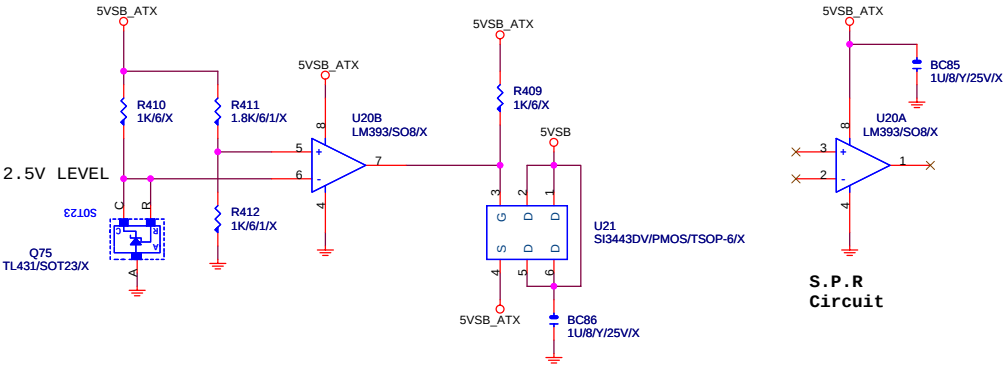
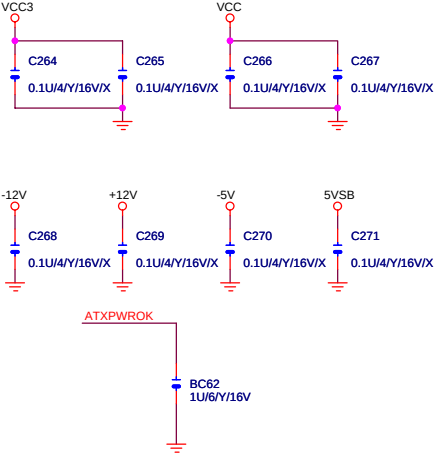
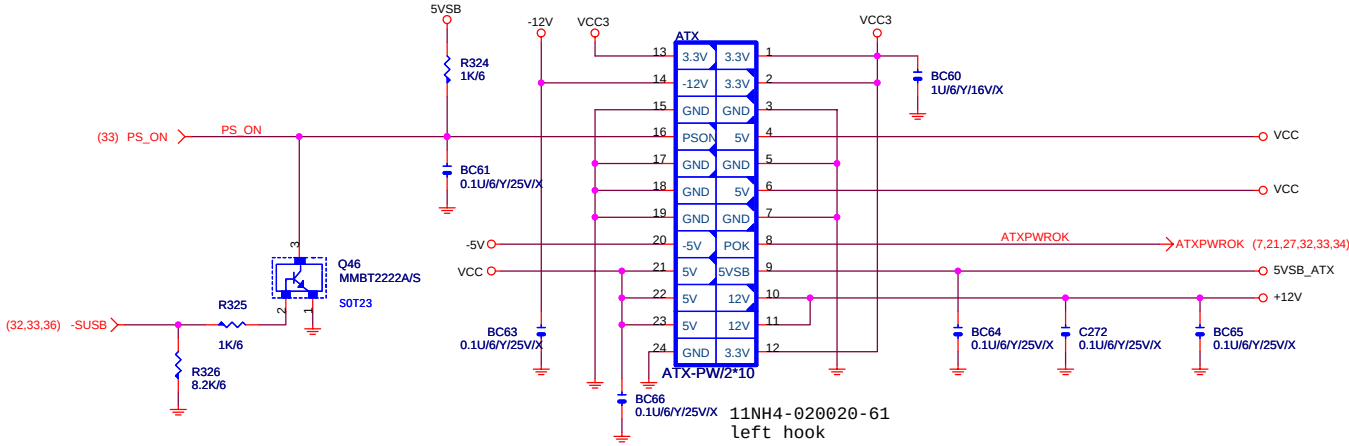
	No CPU	S0	S1	S3	S4/S5
MPD+	H	H	Blink	Blink	L
MPD-	L	L	L	H	H
Led	Green		Orange/reverse		



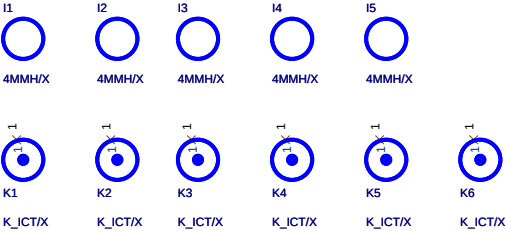
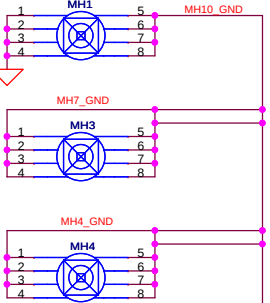
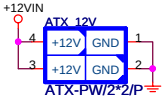
AXPER			
Title			
VCC12,VCC18,VCC25,VDDQ			
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ATX CONN, DC POWER

ATX POWER CONNECTOR



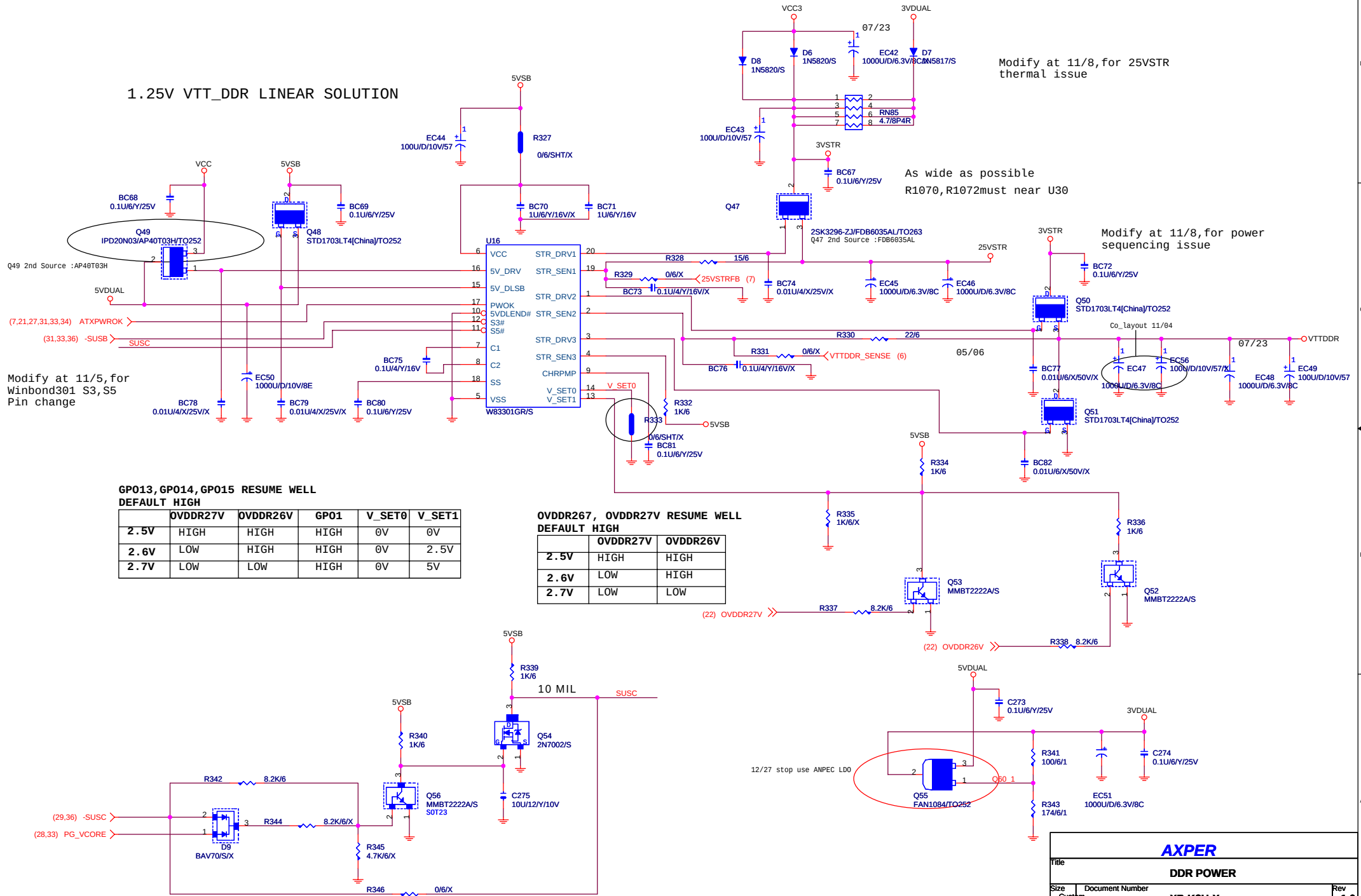
ATX-12V CONNECTOR



LAYOUT: Located near PS/2 ports and connects all I/O port CGND's

AXPER			
File			
ATX, DC POWER			
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1.25V VTT_DDR LINEAR SOLUTION

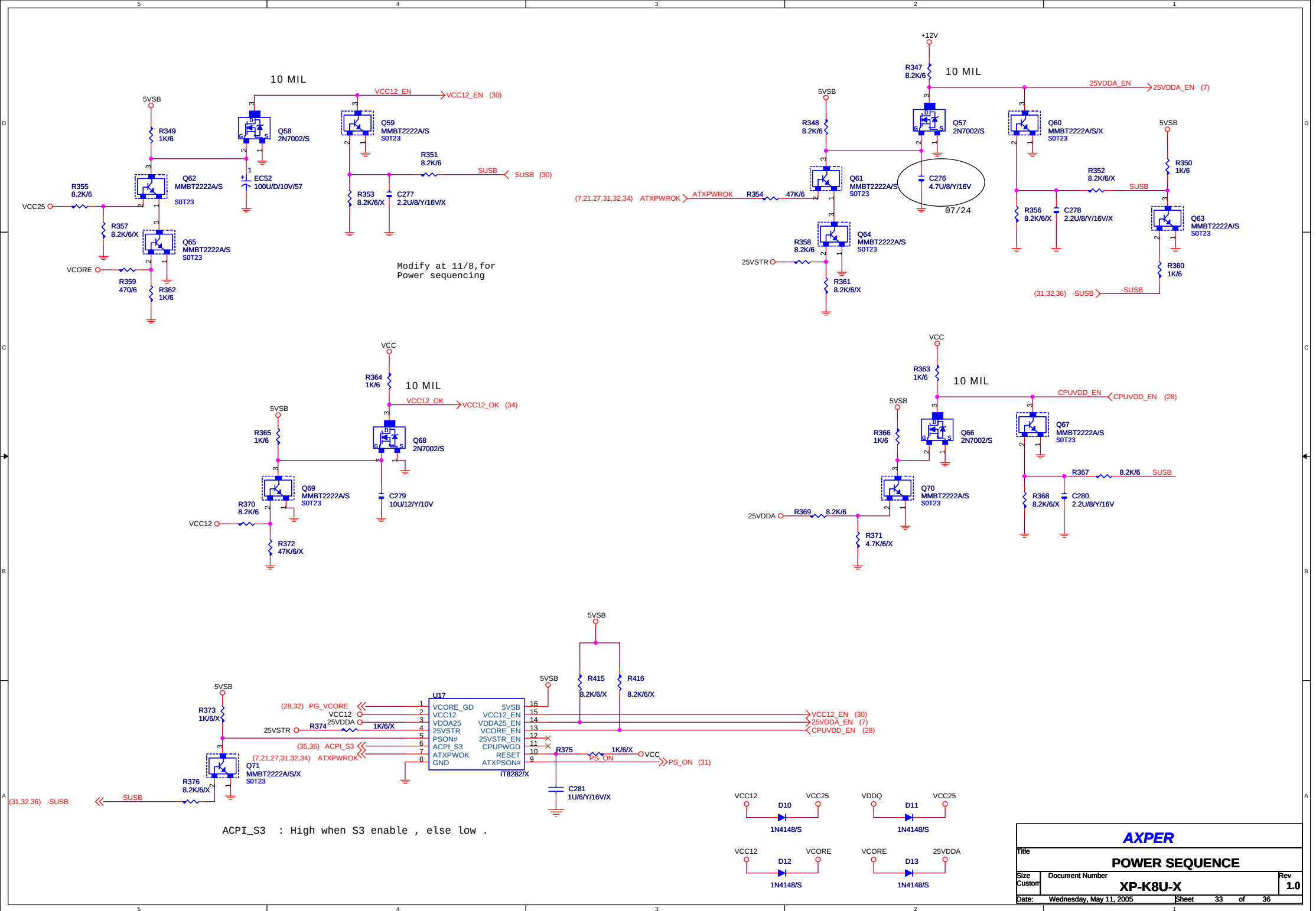


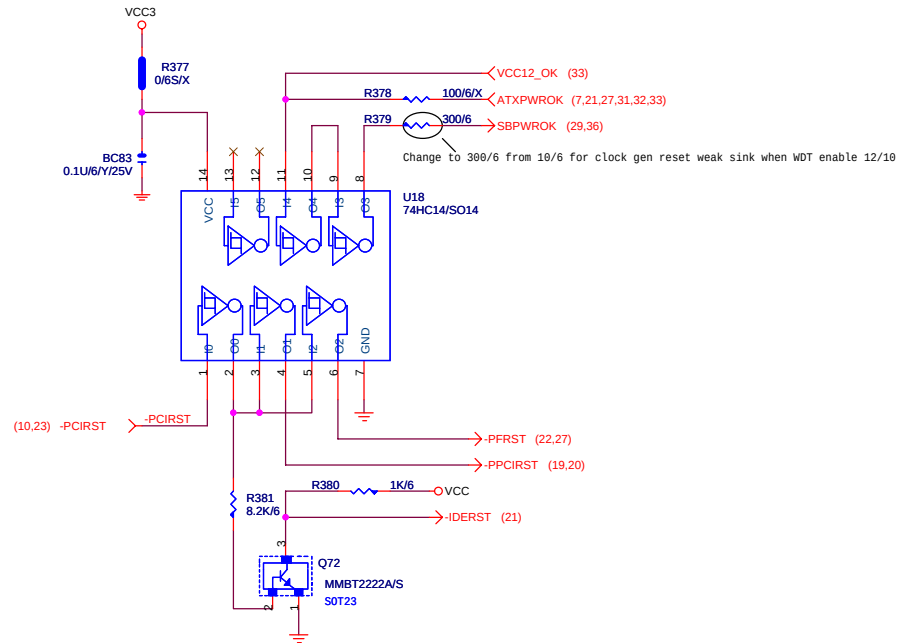
**GP013,GP014,GP015 RESUME WELL
DEFAULT HIGH**

	OVDDR27V	OVDDR26V	GP01	V_SET0	V_SET1
2.5V	HIGH	HIGH	HIGH	0V	0V
2.6V	LOW	HIGH	HIGH	0V	2.5V
2.7V	LOW	LOW	HIGH	0V	5V

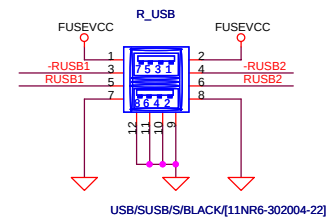
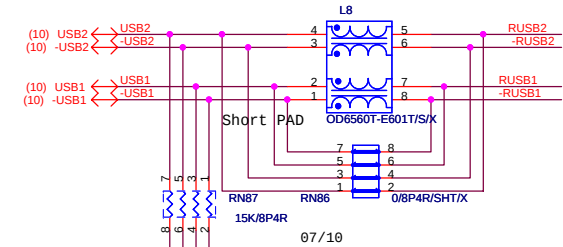
OVDDR267, OVDDR27V RESUME WELL
DEFAULT HIGH

	OVDDR27V	OVDDR26V
2.5V	HIGH	HIGH
2.6V	LOW	HIGH
2.7V	LOW	LOW

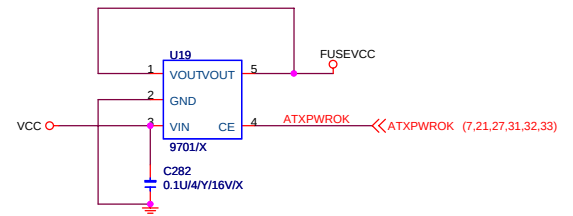
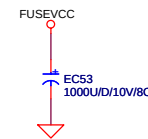




REAR USB2



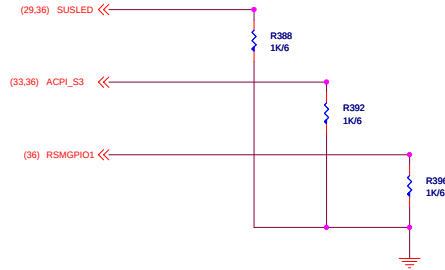
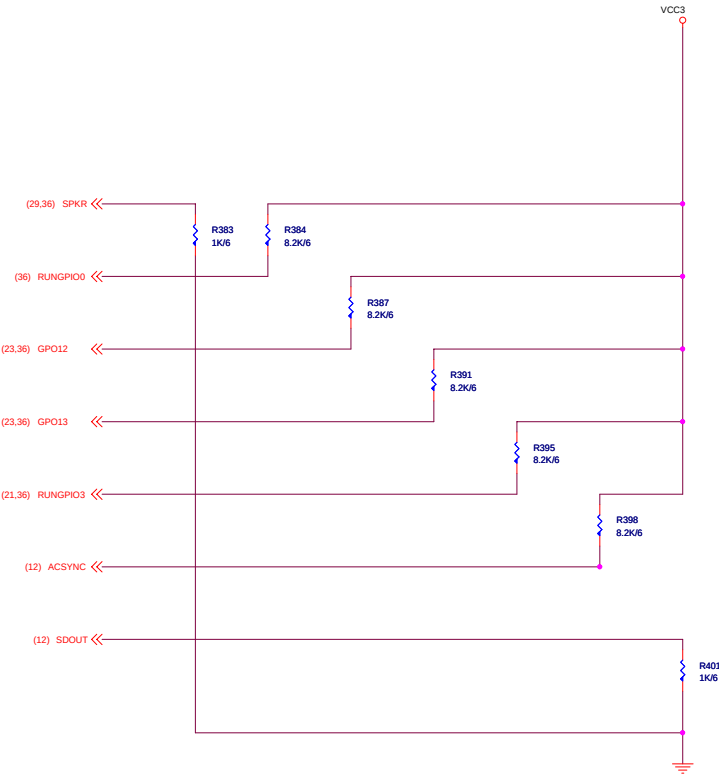
NEAR R_USB CONNECTOR



AXPER			
Title			
REAR USB & RESET			
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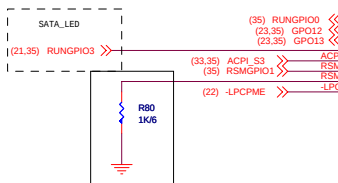
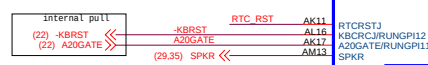
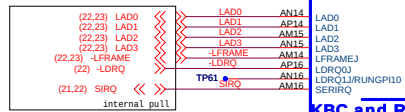
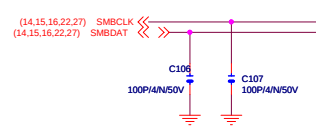
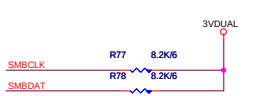
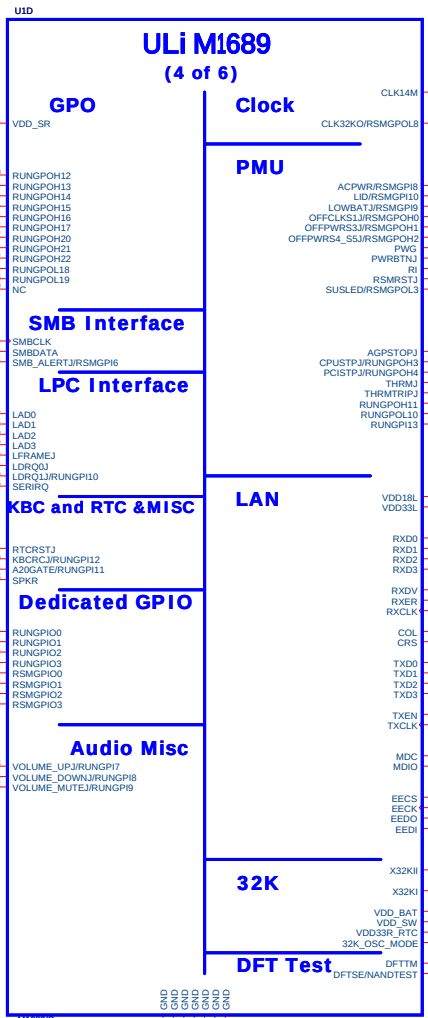
HW SETTING

The HW setting fixed for MP , remove the unuse resistor footprint



H:8.2K		L:1K	
R388 SUSLED	(Default)	L	Normal Operation Mode
		H	Enable 32K Test Mode to select external 32K clock source from 32K Clock Test input pin ACPWR
R383 SPKR	(Default)	L	Normal Operation Mode
		H	Enable Debug Mode to route requests of internal high-speed PCI devices externally and replace requests form PCI slots
R384 RUNGPIO0		L	33MHz reference input for HTT PHY PLL
	(Default)	H	60MHz reference input for HTT PHY PLL
R387 GPO12		L	Enable Simulation Mode to reduce reset active duration for pattern simulation
	(Default)	H	Normal Operation Mode
R391 GPO13		L	Enable Tester Mode to bypass PLL clock and select the external clock source form input pad PCICK
	(Default)	H	Normal Operation Mode
R395 RUNGPIO3		L	External PCI bus type select to BUS0
	(Default)	H	External PCI bus type select to BUSN

H:8.2K		L:1K		
R398 ACSYNC	R401 SDOUT	L	L	On chip core PLL output clock setting 33MHZ
		L	H	60MHZ
		H	L	133MHZ (Default)
		H	H	33MHZ
R396 RSMGPIO1	R392 ACPI_S3	L	L	HTT Unit ID of on-chip host bridge is assigned as 0 (Default)
		L	H	HTT Unit ID of on-chip host bridge is assigned as 2
		H	L	HTT Unit ID of on-chip host bridge is assigned as 3
		H	H	HTT Unit ID of on-chip host bridge is assigned as 4
RSMGPIO2	Look page 11			



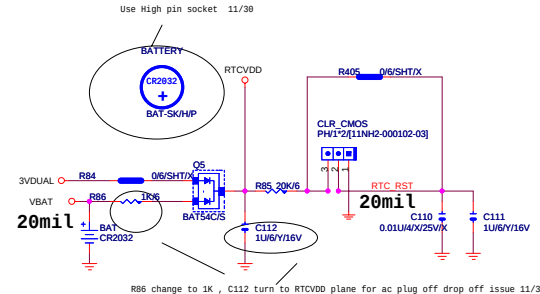
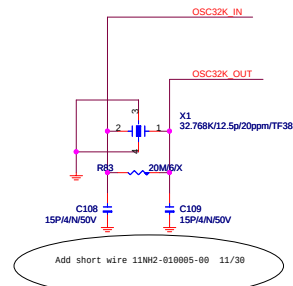
ACPI_S3 status:

S0	S1	S3	S4	S5
L0	L0	HI	L0	L0

Hardware Setting Pins

RSMGPI02

L	Configure M1689 to operate in AMD Atlon64 platform (Default)
H	Configure M1689 to operate in non-AMD Atlon64 like platform



CLR_CMOS	CLEAR COMS JUMPER
1-2	Enable
2-3	Disable (Default)

AXPER		
Title		
ULI GBE & SMB		
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