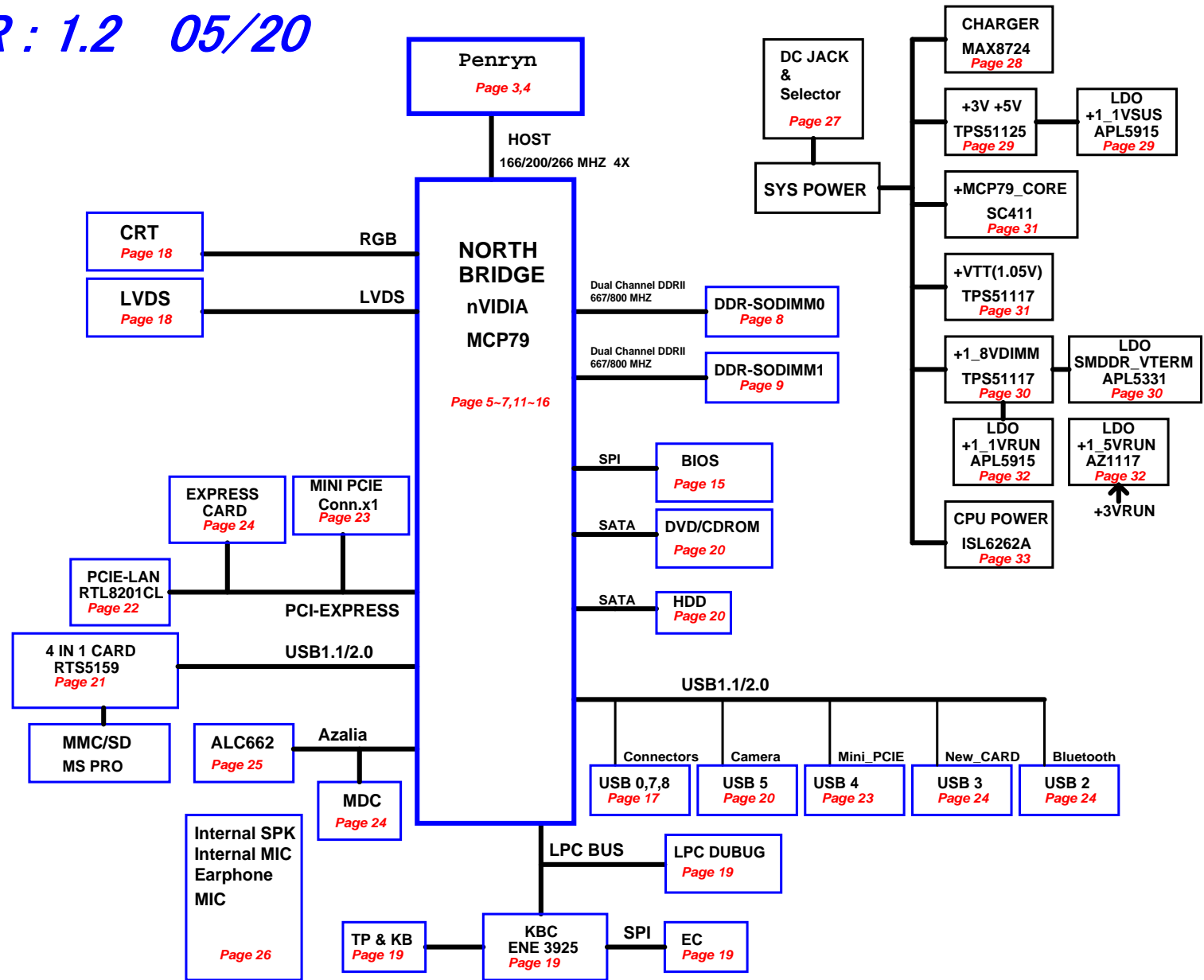
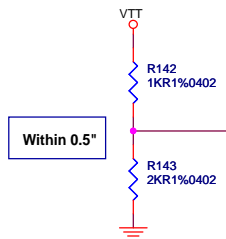
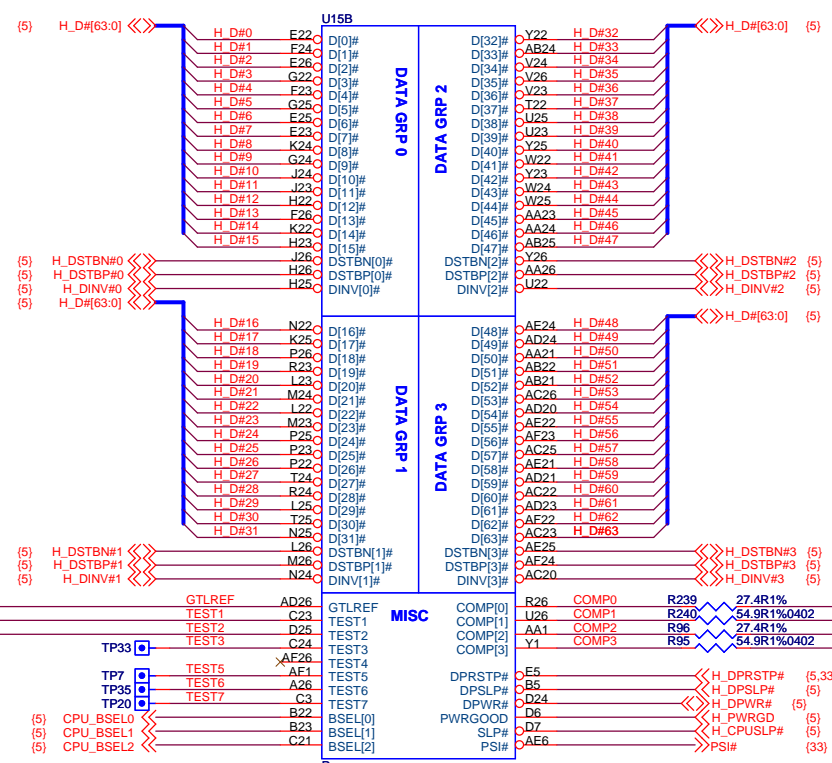
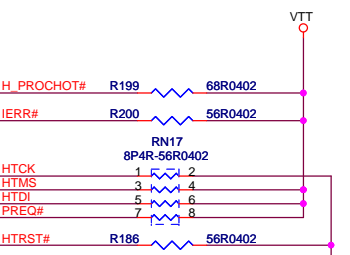
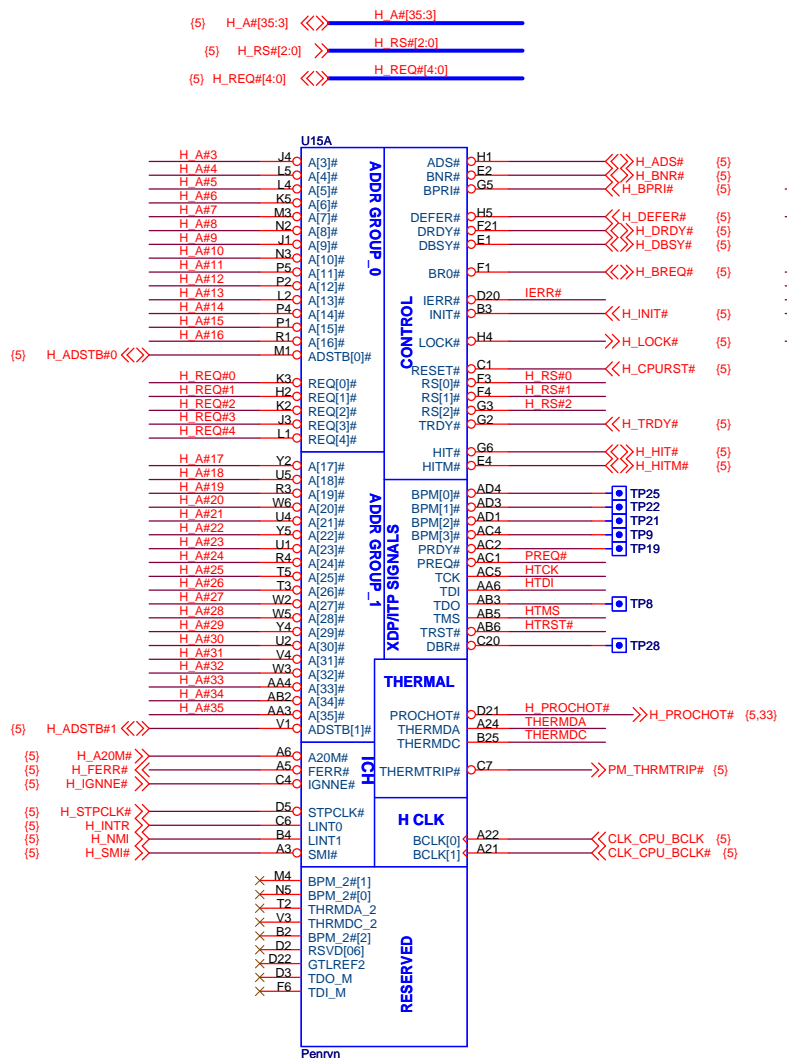
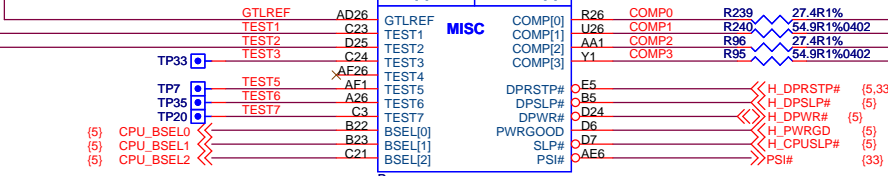
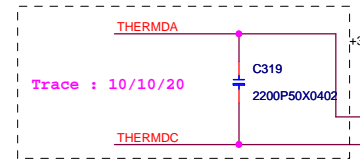


MS-1451 VER : 1.2 05/20

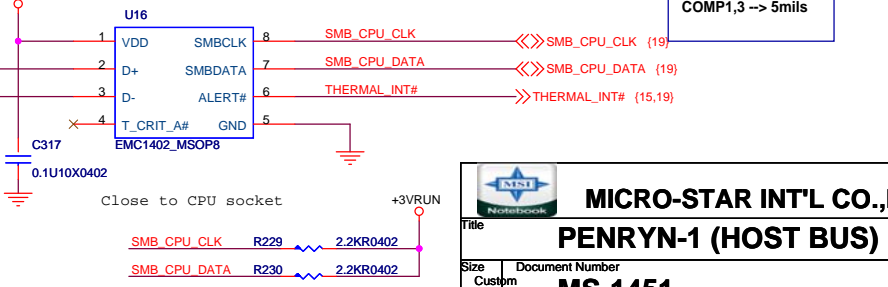




Cap close to thermal sensor



Within 0.5" 25mils Spacing
COMP0,2 -> 18mils
COMP1,3 -> 5mils

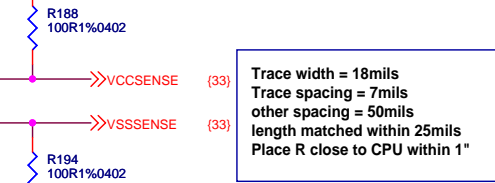
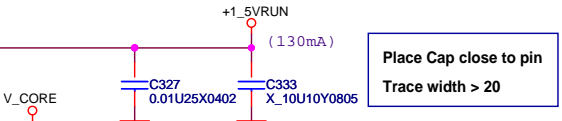
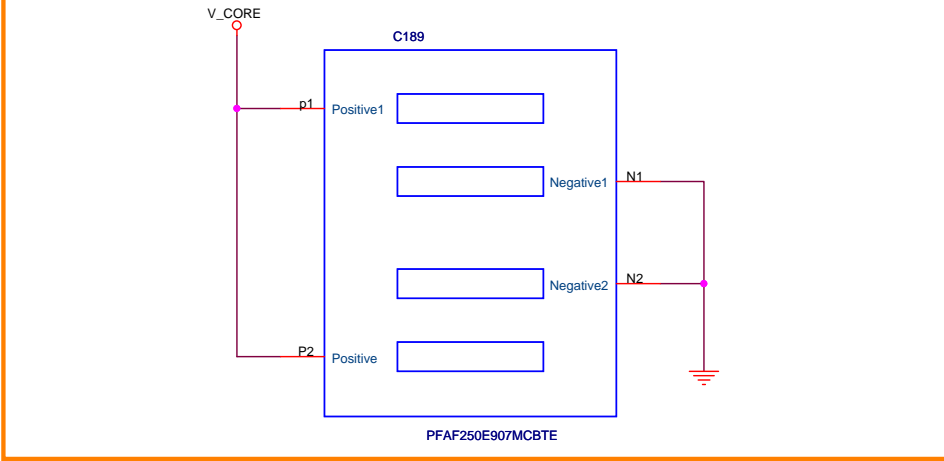
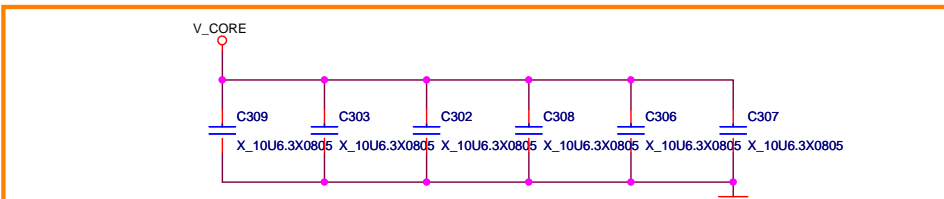
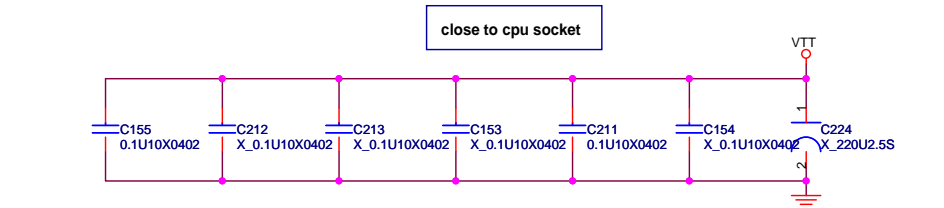
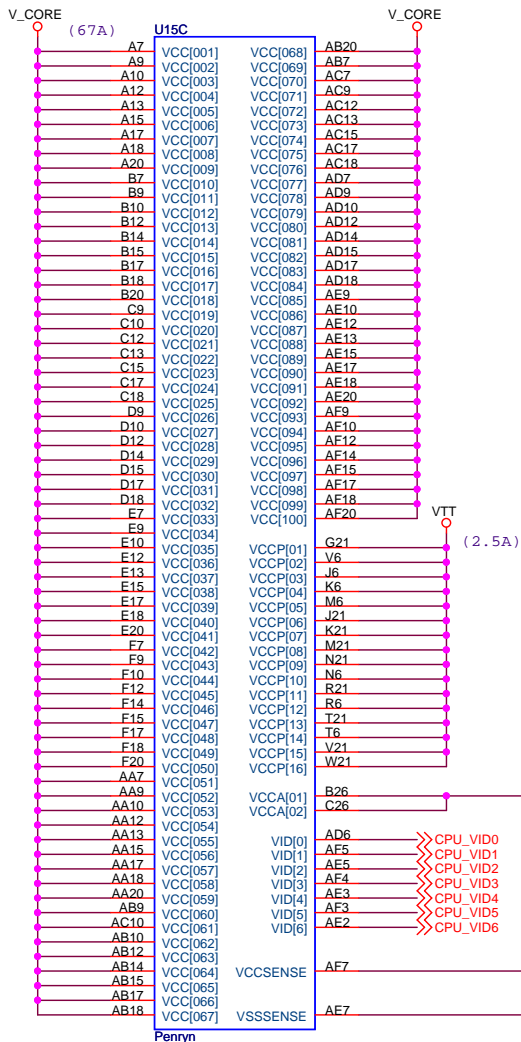
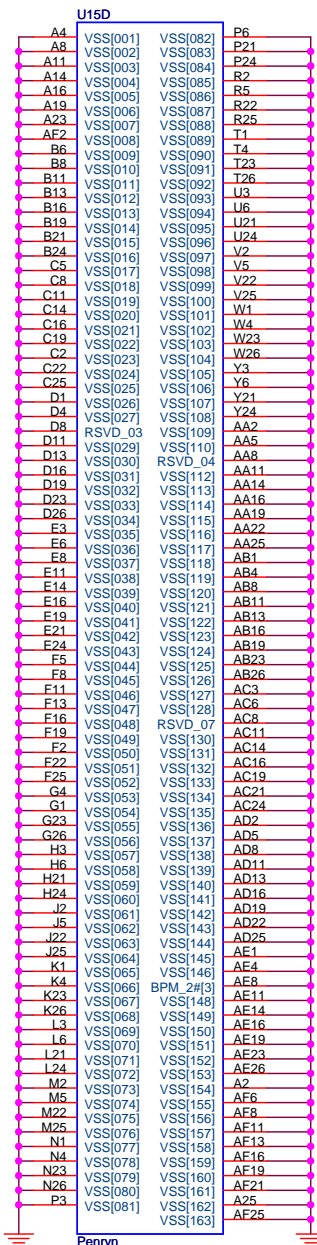


MICRO-STAR INT'L CO.,LTD.

PENRYN-1 (HOST BUS)

Size: Custom | Document Number: MS-1451 | Rev: 1.2

Date: Wednesday, May 20, 2009 | Sheet: 3 of 37

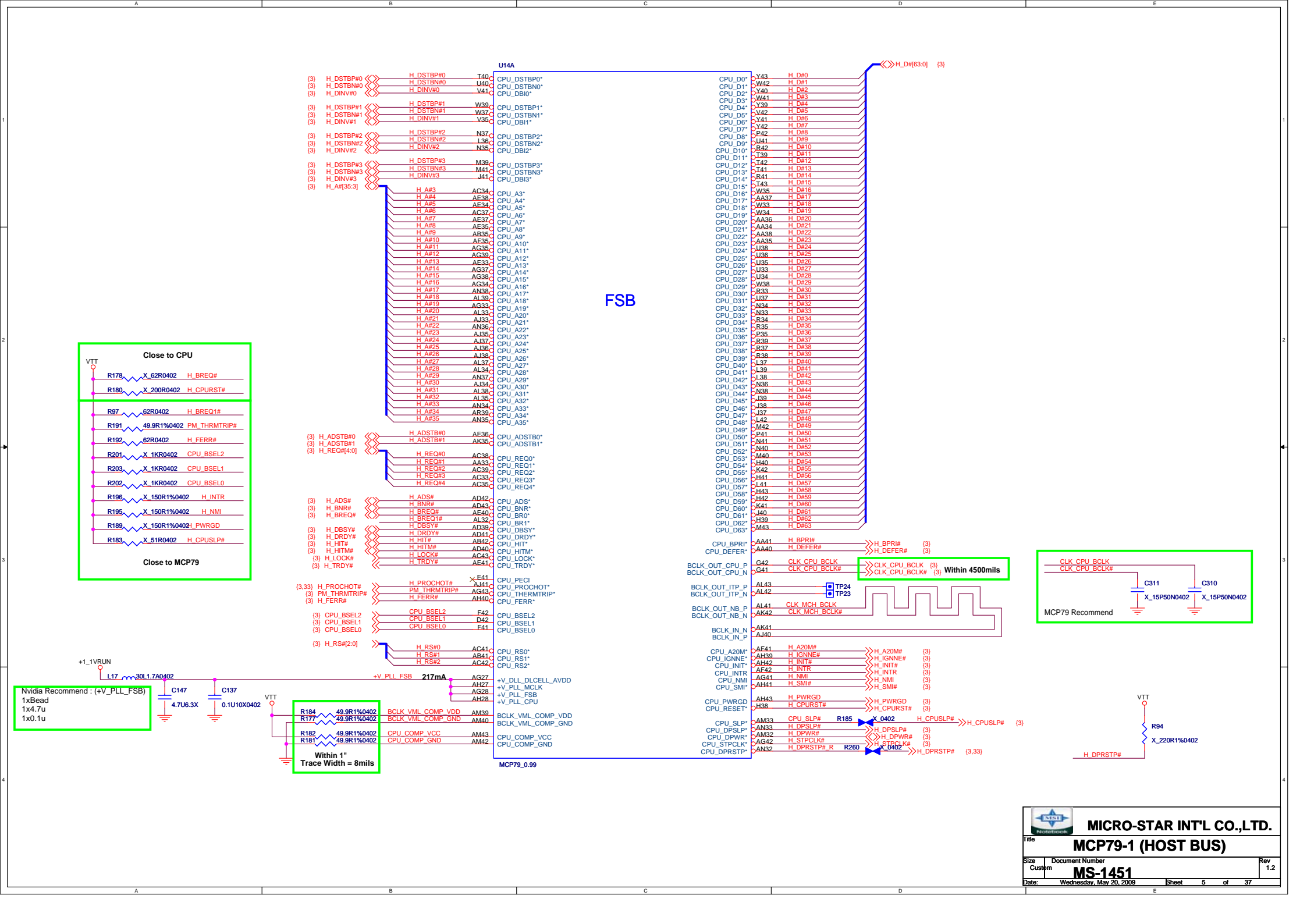


MICRO-STAR INT'L CO.,LTD.

Title: **PENRYN-2 (POWER/GND)**

Size	Document Number	Rev
Custom	MS-1451	1.2

Date: Wednesday, May 20, 2009 Sheet 4 of 37



Close to CPU

VTT

R178 X 62R0402 H_BREQ#

R180 X 200R0402 H_CPUURST#

R97 62R0402 H_BREQI#

R191 49.9R1%0402 PM_THRMTRIP#

R192 62R0402 H_FERR#

R201 X 1KR0402 CPU_BSEL2

R203 X 1KR0402 CPU_BSEL1

R202 X 1KR0402 CPU_BSEL0

R196 X 150R1%0402 H_INTR

R195 X 150R1%0402 H_NMI

R189 X 150R1%0402 PWRGD

R183 X 51R0402 H_CPUSLP#

Close to MCP79

U14A

(3) H_DSTBP#0	H_DSTBP#0	T40	CPU_DSTBP0*	CPU_D0*
(3) H_DSTBN#0	H_DSTBN#0	U44	CPU_DSTBN0*	CPU_D1*
(3) H_DINV#0	H_DINV#0	V44	CPU_DB0*	CPU_D2*
(3) H_DSTBP#1	H_DSTBP#1	W39	CPU_DSTBP1*	CPU_D3*
(3) H_DSTBN#1	H_DSTBN#1	W37	CPU_DSTBN1*	CPU_D4*
(3) H_DINV#1	H_DINV#1	V35	CPU_DB1*	CPU_D5*
(3) H_DSTBP#2	H_DSTBP#2	N37	CPU_DSTBP2*	CPU_D6*
(3) H_DSTBN#2	H_DSTBN#2	L36	CPU_DSTBN2*	CPU_D7*
(3) H_DINV#2	H_DINV#2	N35	CPU_DB2*	CPU_D8*
(3) H_DSTBP#3	H_DSTBP#3	M39	CPU_DSTBP3*	CPU_D9*
(3) H_DSTBN#3	H_DSTBN#3	M41	CPU_DSTBN3*	CPU_D10*
(3) H_DINV#3	H_DINV#3	J41	CPU_DB3*	CPU_D11*
(3) H_A#[35:3]	H_A#3	AC34	CPU_A3*	CPU_D12*
	H_A#4	AE38	CPU_A4*	CPU_D13*
	H_A#5	AE34	CPU_A5*	CPU_D14*
	H_A#6	AC32	CPU_A6*	CPU_D15*
	H_A#7	AE37	CPU_A7*	CPU_D16*
	H_A#8	AE35	CPU_A8*	CPU_D17*
	H_A#9	AE36	CPU_A9*	CPU_D18*
	H_A#10	AE38	CPU_A10*	CPU_D19*
	H_A#11	AE35	CPU_A11*	CPU_D20*
	H_A#12	AG39	CPU_A12*	CPU_D21*
	H_A#13	AE33	CPU_A13*	CPU_D22*
	H_A#14	AG37	CPU_A14*	CPU_D23*
	H_A#15	AG36	CPU_A15*	CPU_D24*
	H_A#16	AG34	CPU_A16*	CPU_D25*
	H_A#17	AN38	CPU_A17*	CPU_D26*
	H_A#18	AL38	CPU_A18*	CPU_D27*
	H_A#19	AG33	CPU_A19*	CPU_D28*
	H_A#20	AL33	CPU_A20*	CPU_D29*
	H_A#21	AJ33	CPU_A21*	CPU_D30*
	H_A#22	AN36	CPU_A22*	CPU_D31*
	H_A#23	AJ35	CPU_A23*	CPU_D32*
	H_A#24	AJ32	CPU_A24*	CPU_D33*
	H_A#25	AJ36	CPU_A25*	CPU_D34*
	H_A#26	AJ38	CPU_A26*	CPU_D35*
	H_A#27	AL37	CPU_A27*	CPU_D36*
	H_A#28	AL36	CPU_A28*	CPU_D37*
	H_A#29	AN34	CPU_A29*	CPU_D38*
	H_A#30	AJ34	CPU_A30*	CPU_D39*
	H_A#31	AL38	CPU_A31*	CPU_D40*
	H_A#32	AL33	CPU_A32*	CPU_D41*
	H_A#33	AN34	CPU_A33*	CPU_D42*
	H_A#34	AR39	CPU_A34*	CPU_D43*
	H_A#35	AN35	CPU_A35*	CPU_D44*
(3) H_ADSTB#0	H_ADSTB#0	AE36	CPU_ADSTB0*	CPU_D45*
(3) H_ADSTB#1	H_ADSTB#1	AK36	CPU_ADSTB1*	CPU_D46*
(3) H_REQ#0	H_REQ#0	AC38	CPU_REQ0*	CPU_D47*
(3) H_REQ#1	H_REQ#1	AC33	CPU_REQ1*	CPU_D48*
(3) H_REQ#2	H_REQ#2	AC38	CPU_REQ2*	CPU_D49*
(3) H_REQ#3	H_REQ#3	AC33	CPU_REQ3*	CPU_D50*
(3) H_REQ#4	H_REQ#4	AC33	CPU_REQ4*	CPU_D51*
(3) H_ADS#	H_ADS#	AD42	CPU_ADS*	CPU_D52*
(3) H_BNR#	H_BNR#	AD43	CPU_BNR*	CPU_D53*
(3) H_BREQ#	H_BREQ#	AE40	CPU_BR0*	CPU_D54*
(3) H_BREQI#	H_BREQI#	AL32	CPU_BR1*	CPU_D55*
(3) H_DBSY#	H_DBSY#	AD39	CPU_DBSY*	CPU_D56*
(3) H_DRDY#	H_DRDY#	AD42	CPU_DRDY*	CPU_D57*
(3) H_HIT#	H_HIT#	AB42	CPU_HIT*	CPU_D58*
(3) H_HITM#	H_HITM#	AD40	CPU_HITM*	CPU_D59*
(3) H_LOCK#	H_LOCK#	AC43	CPU_LOCK*	CPU_D60*
(3) H_TRDY#	H_TRDY#	AE41	CPU_LOCK*	CPU_D61*
(3) H_PROCHOT#	H_PROCHOT#	E41	CPU_PROCHOT*	CPU_D62*
(3) PM_THRMTRIP#	PM_THRMTRIP#	AJ41	CPU_THERMTRIP*	CPU_D63*
(3) H_FERR#	H_FERR#	AG40	CPU_FERR*	CPU_D64*
(3) CPU_BSEL2	CPU_BSEL2	F42	CPU_BSEL2	CPU_D65*
(3) CPU_BSEL1	CPU_BSEL1	D42	CPU_BSEL1	CPU_D66*
(3) CPU_BSEL0	CPU_BSEL0	F41	CPU_BSEL0	CPU_D67*
(3) H_RS#[2:0]	H_RS#0	AC41	CPU_RS0*	CPU_D68*
	H_RS#1	AB41	CPU_RS1*	CPU_D69*
	H_RS#2	AC42	CPU_RS2*	CPU_D70*

FSB

H_D#[63:0] (3)

CPU_D0* Y43 H_D#0

CPU_D1* W42 H_D#1

CPU_D2* W40 H_D#2

CPU_D3* W41 H_D#3

CPU_D4* Y39 H_D#4

CPU_D5* Y42 H_D#5

CPU_D6* Y41 H_D#6

CPU_D7* Y42 H_D#7

CPU_D8* P42 H_D#8

CPU_D9* U41 H_D#9

CPU_D10* R42 H_D#10

CPU_D11* T39 H_D#11

CPU_D12* T42 H_D#12

CPU_D13* T41 H_D#13

CPU_D14* R41 H_D#14

CPU_D15* T43 H_D#15

CPU_D16* W35 H_D#16

CPU_D17* AA37 H_D#17

CPU_D18* W33 H_D#18

CPU_D19* AA36 H_D#19

CPU_D20* AA34 H_D#20

CPU_D21* AA36 H_D#21

CPU_D22* AA38 H_D#22

CPU_D23* U38 H_D#23

CPU_D24* U36 H_D#24

CPU_D25* U36 H_D#25

CPU_D26* U35 H_D#26

CPU_D27* U33 H_D#27

CPU_D28* U34 H_D#28

CPU_D29* W38 H_D#29

CPU_D30* R33 H_D#30

CPU_D31* U37 H_D#31

CPU_D32* N33 H_D#32

CPU_D33* R34 H_D#33

CPU_D34* R35 H_D#34

CPU_D35* R35 H_D#35

CPU_D36* R35 H_D#36

CPU_D37* R37 H_D#37

CPU_D38* R37 H_D#38

CPU_D39* R38 H_D#39

CPU_D40* L37 H_D#40

CPU_D41* L38 H_D#41

CPU_D42* L38 H_D#42

CPU_D43* N36 H_D#43

CPU_D44* N38 H_D#44

CPU_D45* J38 H_D#45

CPU_D46* J37 H_D#46

CPU_D47* L42 H_D#47

CPU_D48* M42 H_D#48

CPU_D49* E41 H_D#49

CPU_D50* N41 H_D#50

CPU_D51* N40 H_D#51

CPU_D52* M40 H_D#52

CPU_D53* H40 H_D#53

CPU_D54* K42 H_D#54

CPU_D55* H41 H_D#55

CPU_D56* L41 H_D#56

CPU_D57* H43 H_D#57

CPU_D58* H42 H_D#58

CPU_D59* K41 H_D#59

CPU_D60* J40 H_D#60

CPU_D61* H39 H_D#61

CPU_D62* M43 H_D#62

CPU_D63* M43 H_D#63

CPU_BPRI# AA41 H_BPRI# (3)

CPU_DEFER# AA40 H_DEFER# (3)

BCLK_OUT_CPU_P G42 CLK_CPU_BCLK (3)

BCLK_OUT_CPU_N G41 CLK_CPU_BCLK# (3)

BCLK_OUT_ITP_P AL43 CLK_CPU_BCLK (3)

BCLK_OUT_ITP_N AL42 CLK_CPU_BCLK# (3)

BCLK_OUT_NB_P AL41 CLK_MCH_BCLK (3)

BCLK_OUT_NB_N AK42 CLK_MCH_BCLK# (3)

BCLK_IN_N AJ40

BCLK_IN_P AJ40

CPU_A20M# AE41 H_A20M# (3)

CPU_IGNNE# AH30 H_IGNNE# (3)

CPU_INTR# AH42 H_INTR# (3)

CPU_INTR# AF42 H_INTR# (3)

CPU_NMI# AG41 H_NMI# (3)

CPU_SMI# AH41 H_SMI# (3)

CPU_PWRGD# AH43 H_PWRGD# (3)

CPU_RESET# H38 H_CPURST# (3)

CPU_SLP# AM33 CPU_SLP# R185 X 0402 H_CPUSLP# (3)

CPU_DPSLP# AN33 H_DPSLP# (3)

CPU_DPWR# AM32 H_DPWR# (3)

CPU_STPCLK# AG42 H_STPCLK# (3)

CPU_DPRSTP# AN32 H_DPRSTP# R260 X 0402 H_DPRSTP# (3.33)

MCP79 Recommend

CLK_CPU_BCLK

CLK_CPU_BCLK#

C311

X_15P50N0402

C310

X_15P50N0402

Nvidia Recommend : (+V_PLL_FSB)

1xBead

1x4.7u

1x0.1u

Within 1"

Trace Width = 8mils

R184 49.9R1%0402 BCLK_VML_COMP_VDD AM39

R177 49.9R1%0402 BCLK_VML_COMP_GND AM40

R182 49.9R1%0402 CPU_COMP_VCC AM43

R181 49.9R1%0402 CPU_COMP_GND AM42

+V_PLL_FSB 217mA

AG27 +V_DLL_DLCCELL_AVDD

AH27 +V_PLL_MCLK

AG28 +V_PLL_FSB

AH28 +V_PLL_CPU

MCP79_0.99

MICRO-STAR INT'L CO.,LTD.

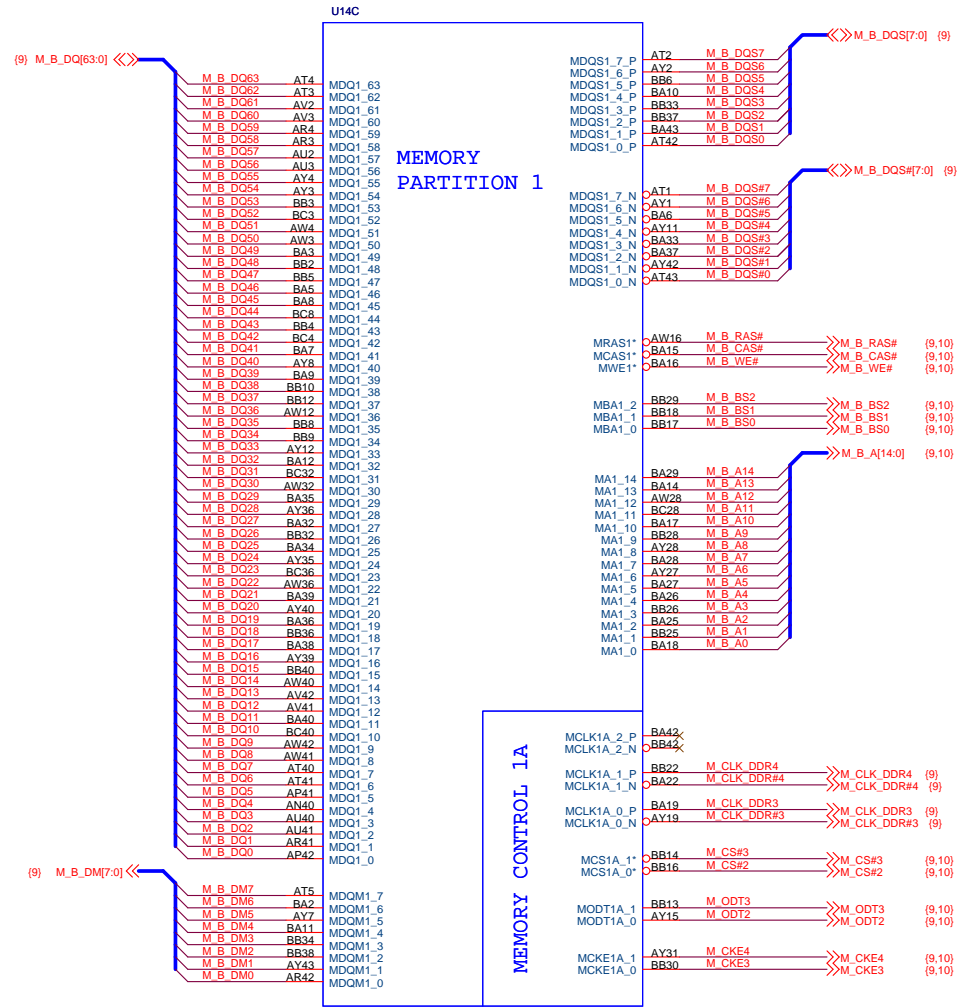
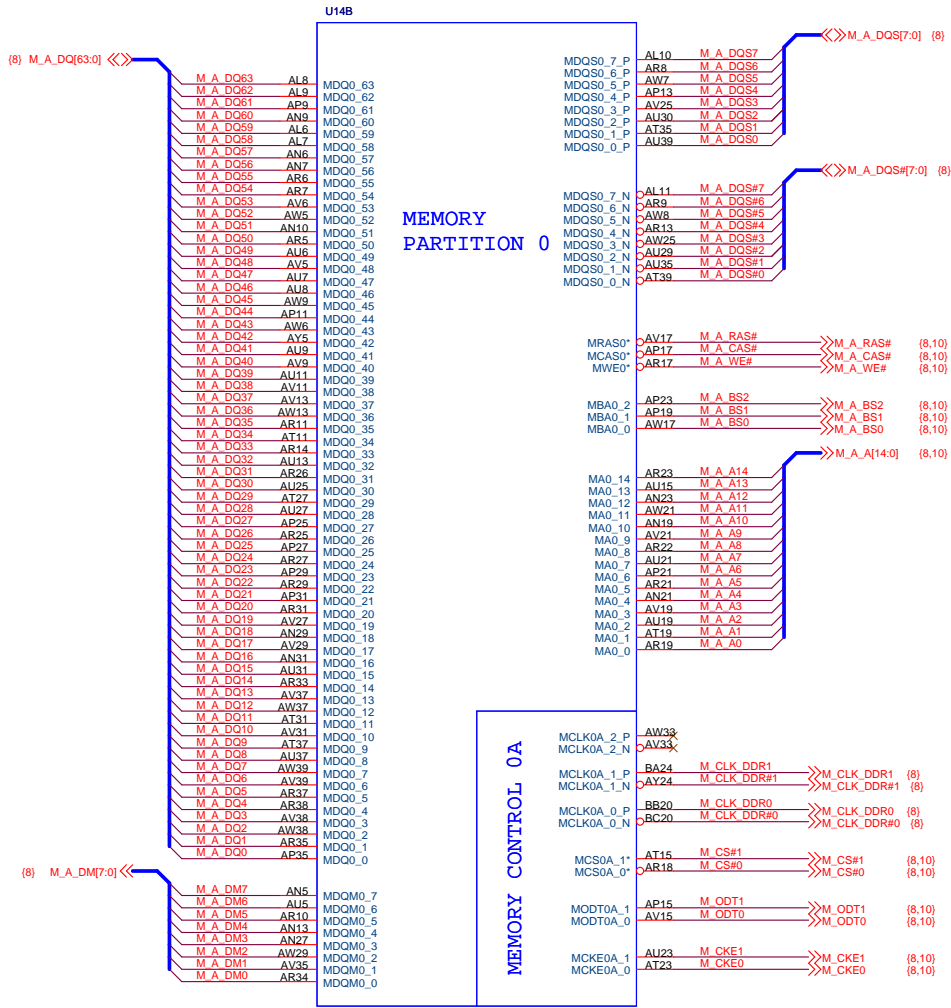
MCP79-1 (HOST BUS)

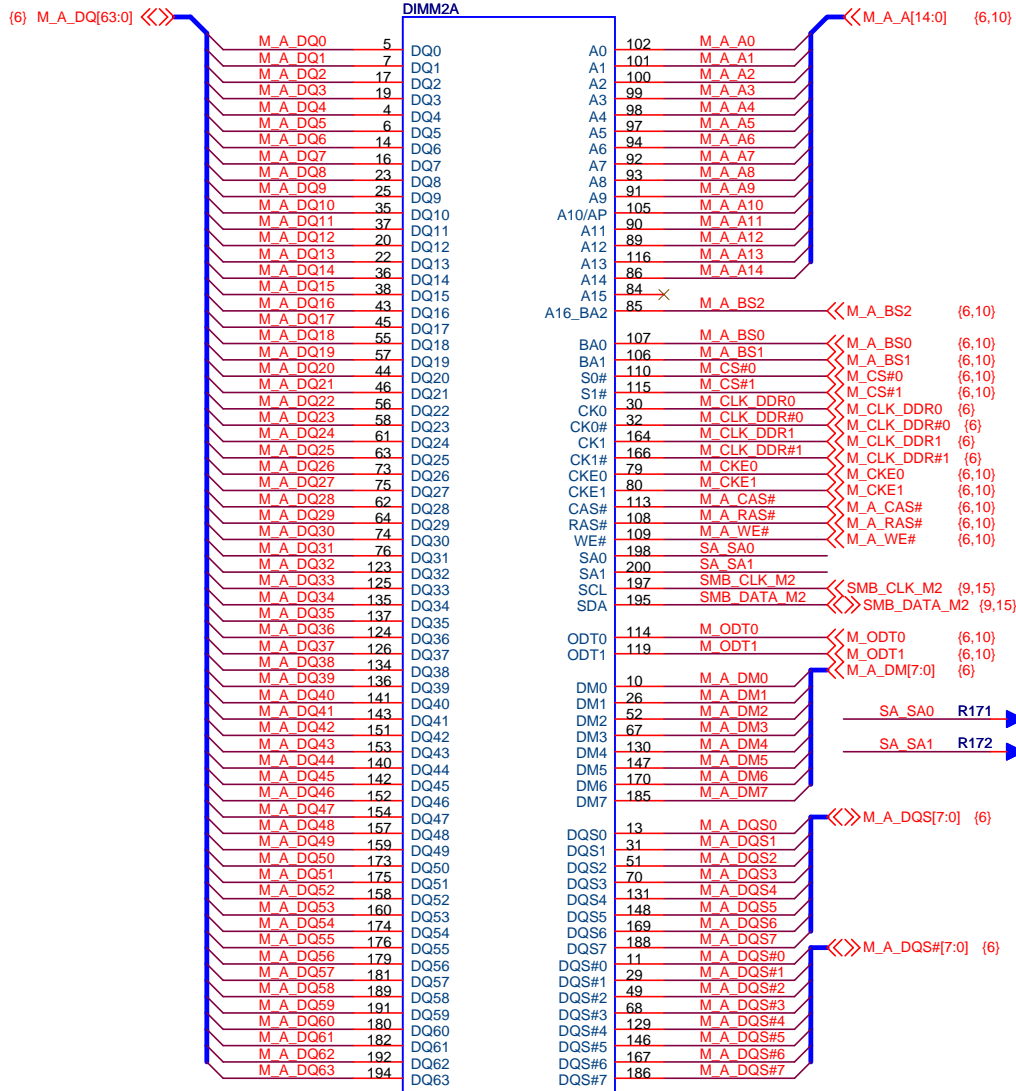
Rev 1.2

MS-1451

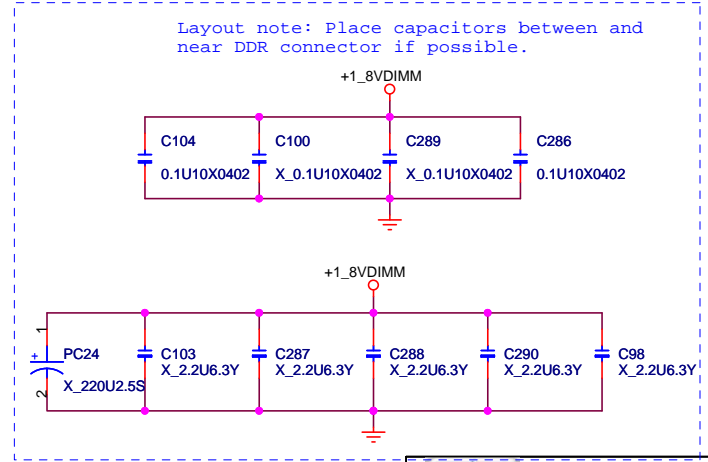
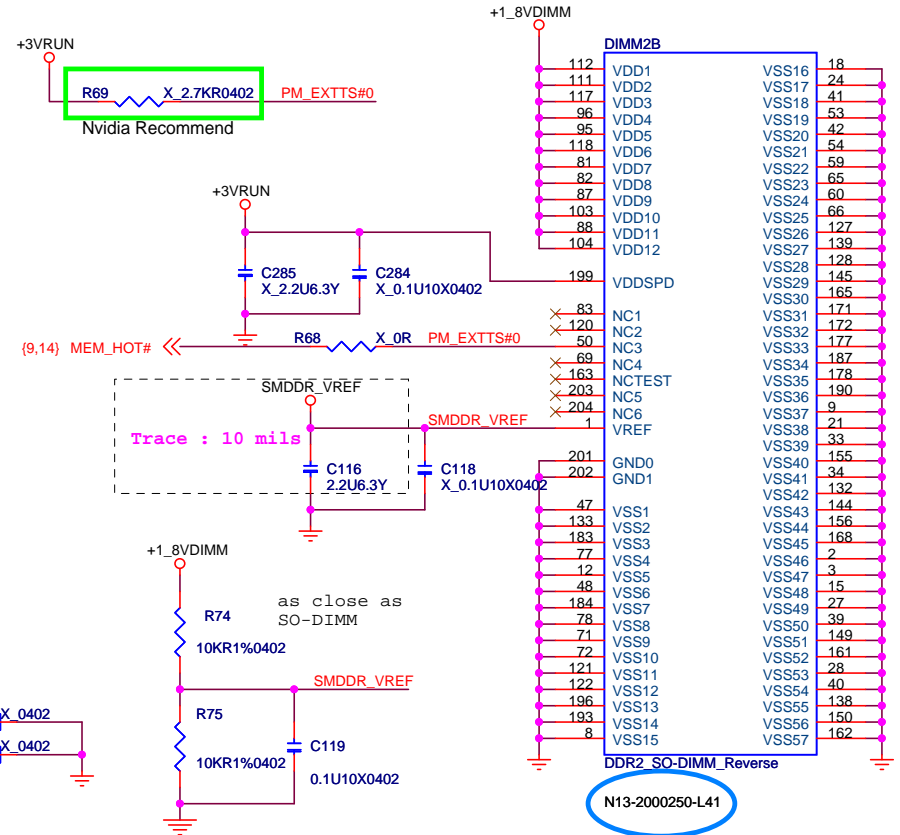
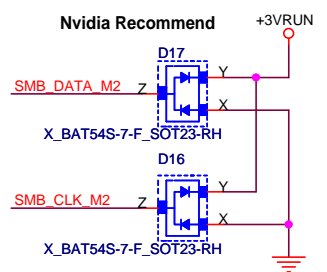
Date: Wednesday, May 20, 2009

Sheet 5 of 37





DDR2_SO-DIMM_Reverse
N13-2000250-L41

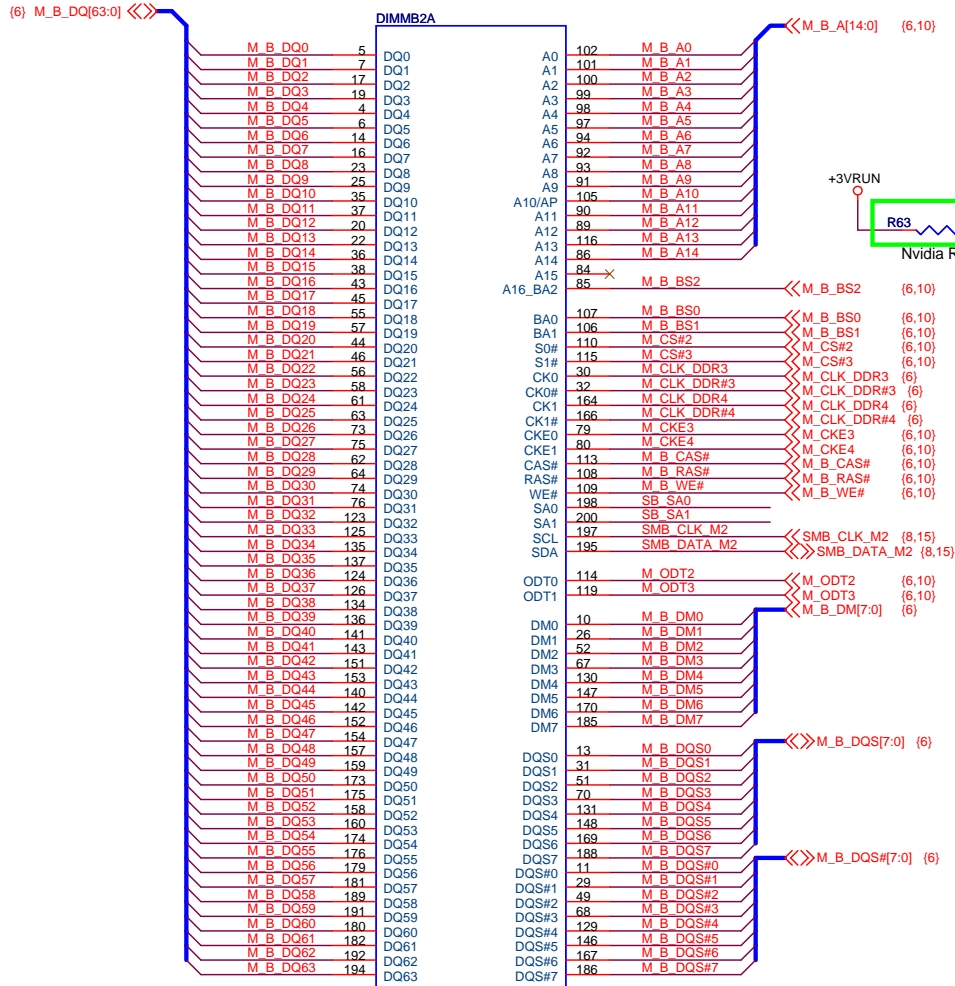


MSI Notebook

MICRO-STAR INT'L CO.,LTD.

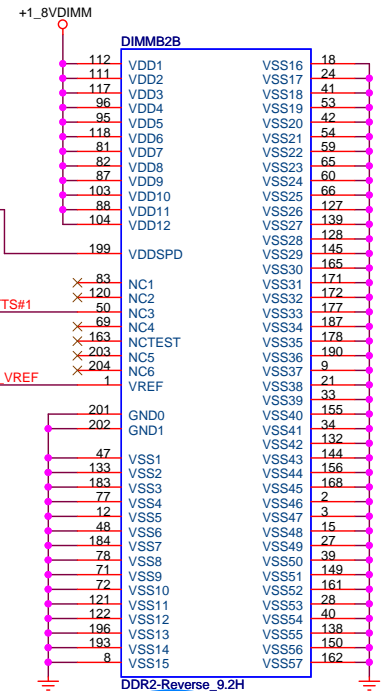
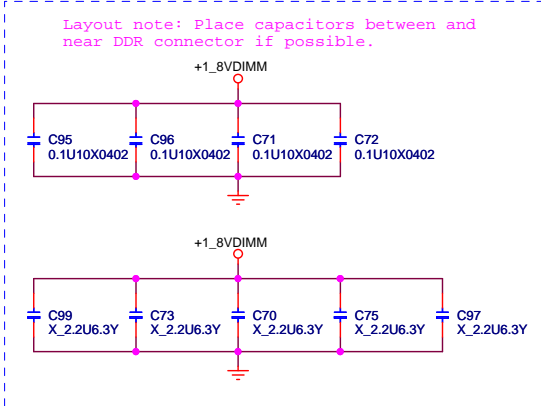
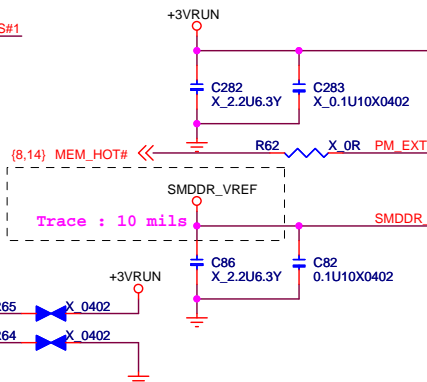
Title: **DDR2 SODIMM 0**

Size: Custom	Document Number: MS-1451	Rev: 1.2
Date: Wednesday, May 20, 2009	Sheet: 8	of 37



DDR2-Reverse_9.2H
N13-2000240-L41

R63 X 2.7KR0402
Nvidia Recommend



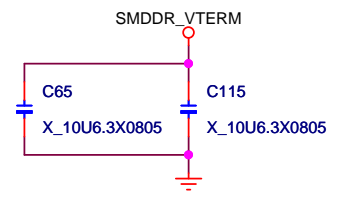
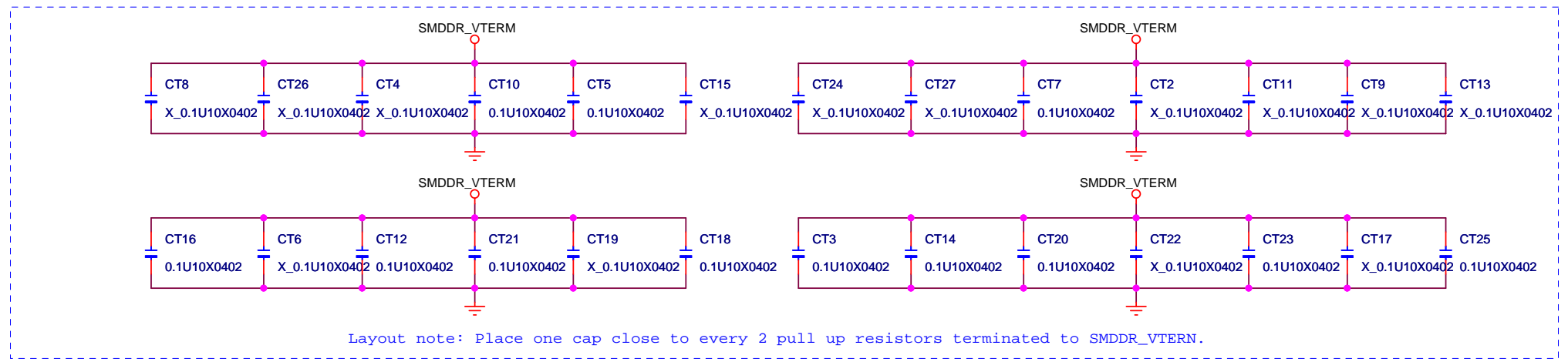
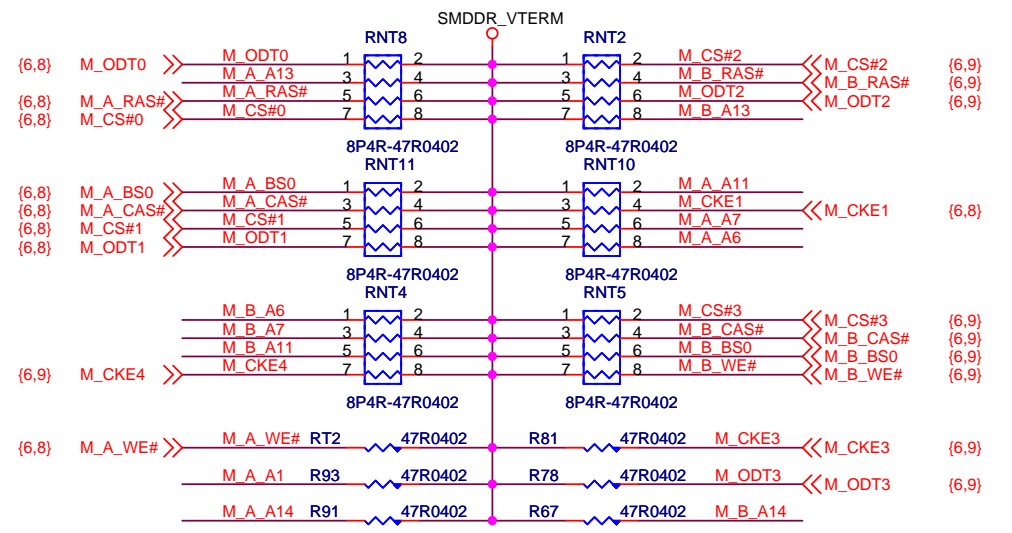
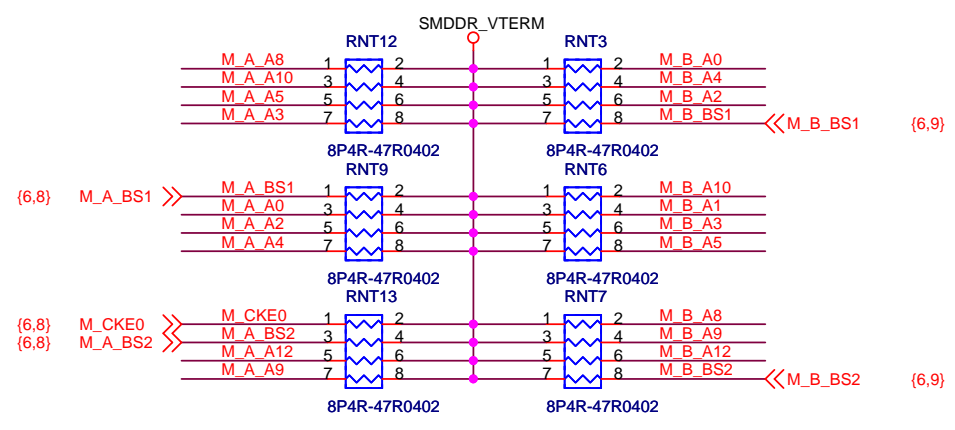
DDR2-Reverse_9.2H
N13-2000240-L41

MICRO-STAR INT'L CO.,LTD.

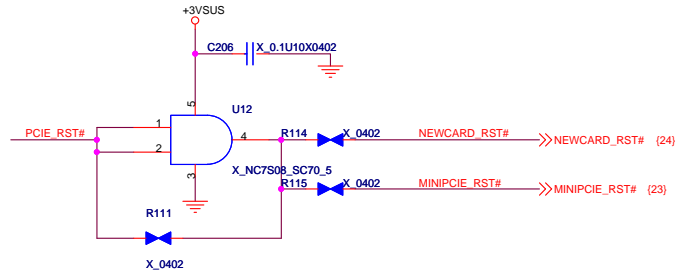
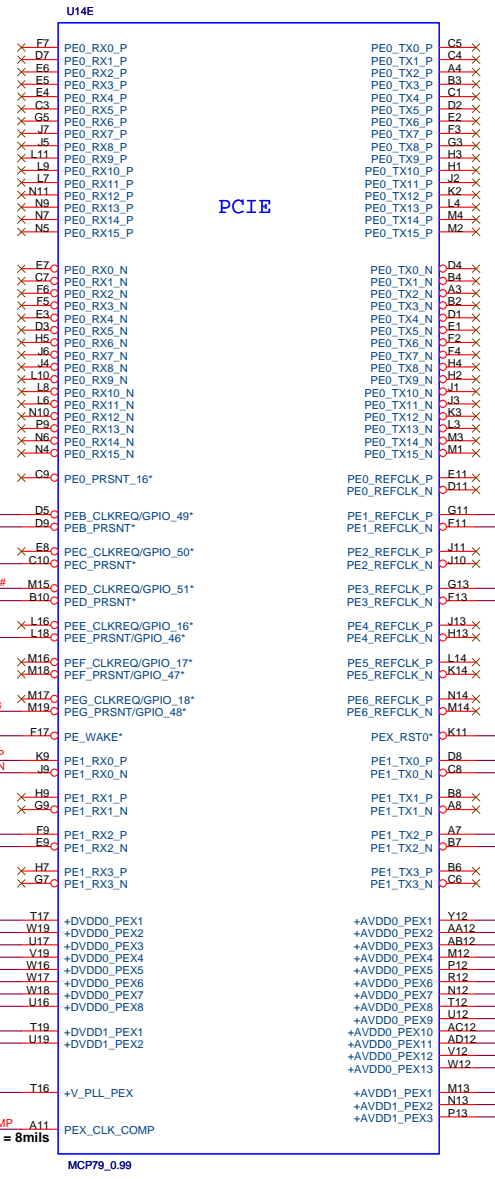
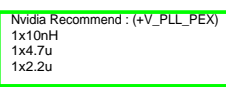
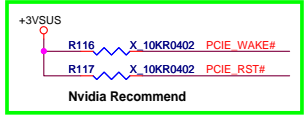
Title: **DDR2 SODIMM 1**

Size: Custom	Document Number: MS-1451	Rev: 1.2
Date: Wednesday, May 20, 2009	Sheet: 9 of 37	

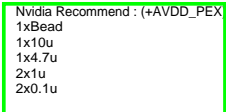
M_A_A[14:0] << M_A_A[14:0] (6,8)
M_B_A[14:0] << M_B_A[14:0] (6,9)

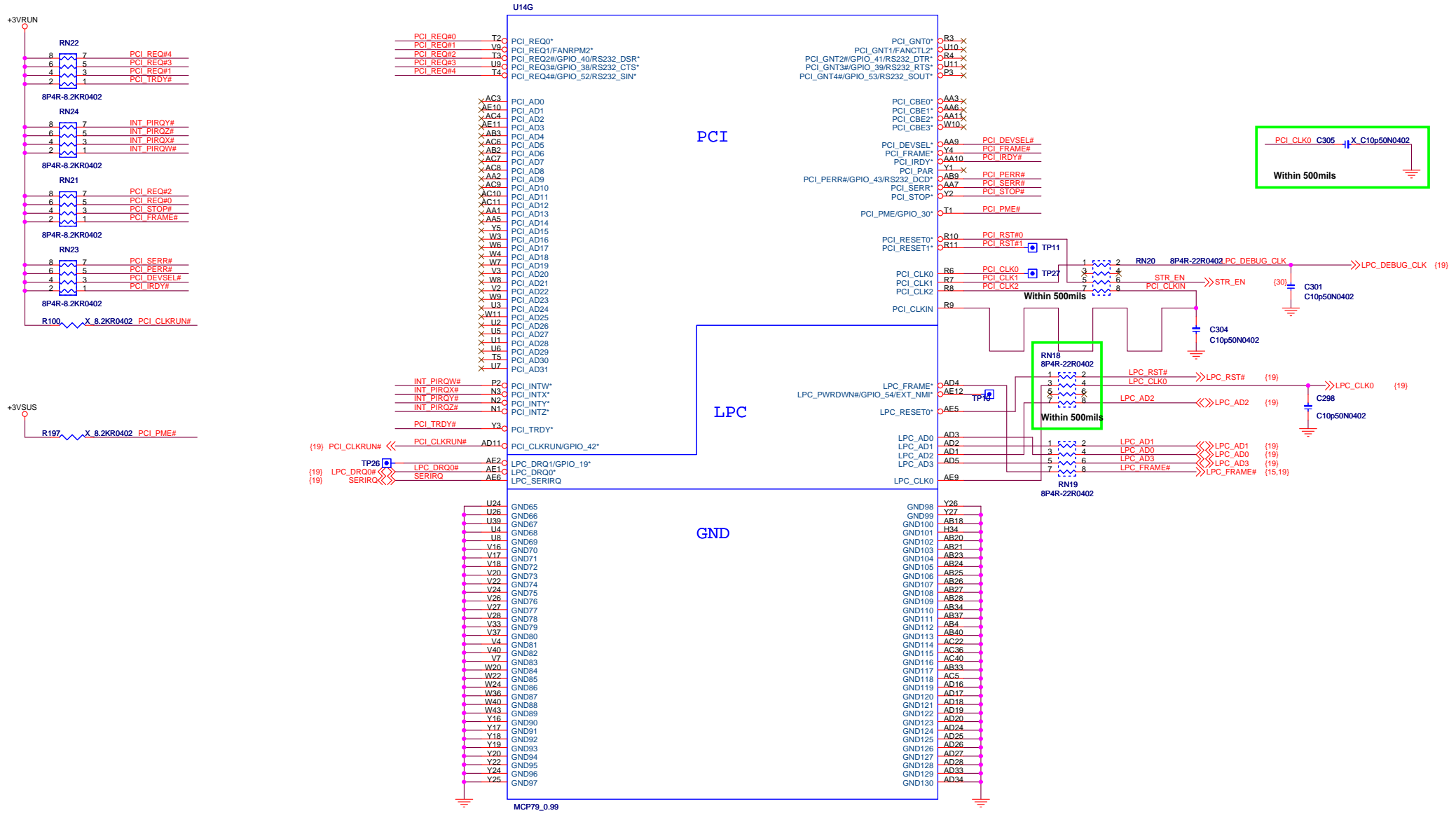


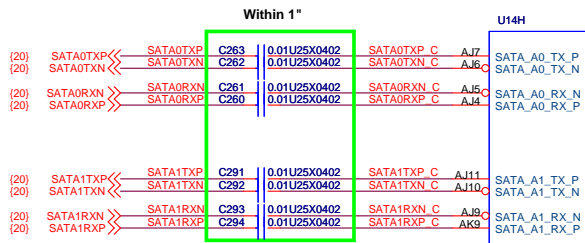
		MICRO-STAR INT'L CO.,LTD.	
Title		DDR2 TREMINATION	
Size	Document Number	MS-1451	
Custom			
Date:	Wednesday, May 20, 2009	Sheet	10 of 37
			Rev 1.2



close to connector

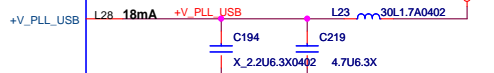
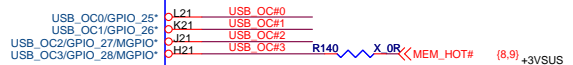
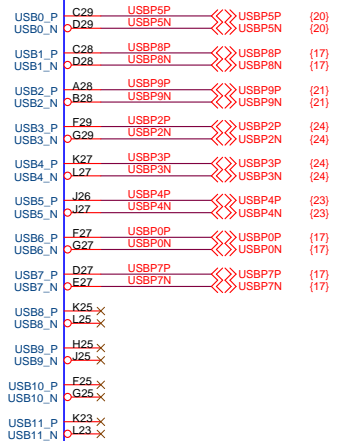
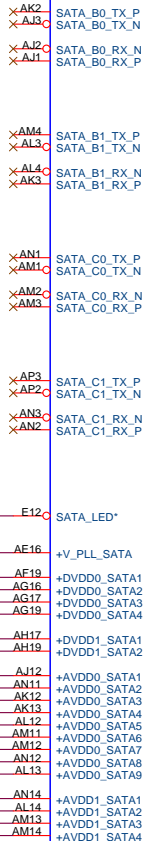




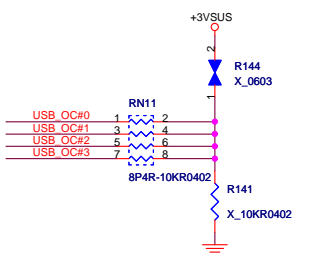


Place Cap Close to Connector

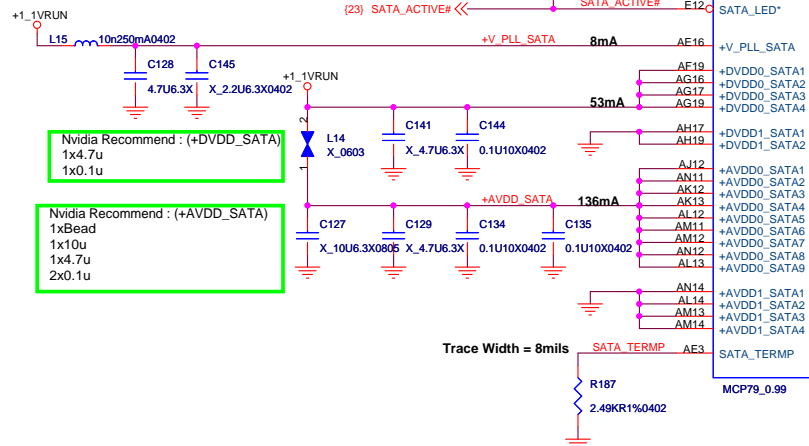
SATA USB



Nvidia Recommend : (+V_PLL_USB)
1xBead
1x4.7u
1x2.2u



Nvidia Recommend : (+V_PLL_SATA)
1x10nH
1x4.7u
1x2.2u

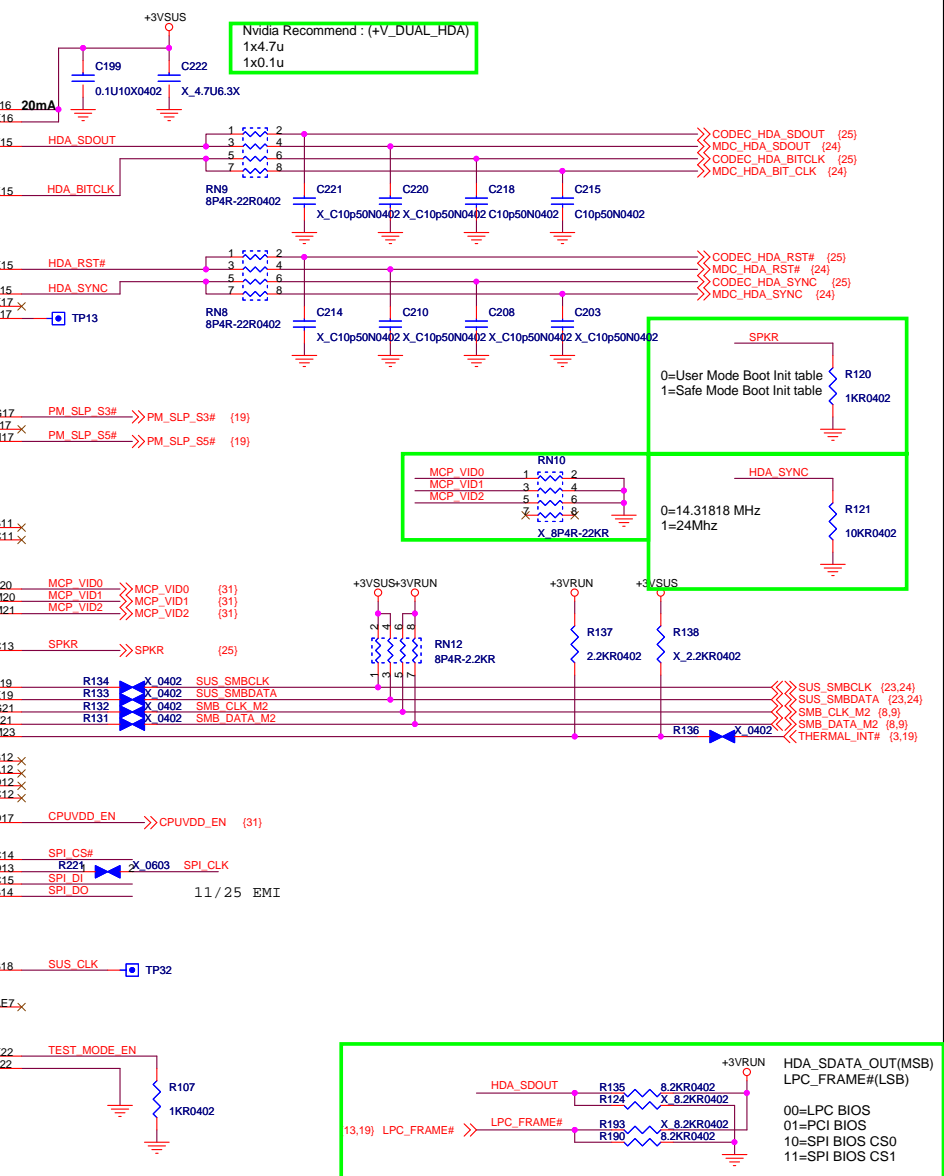
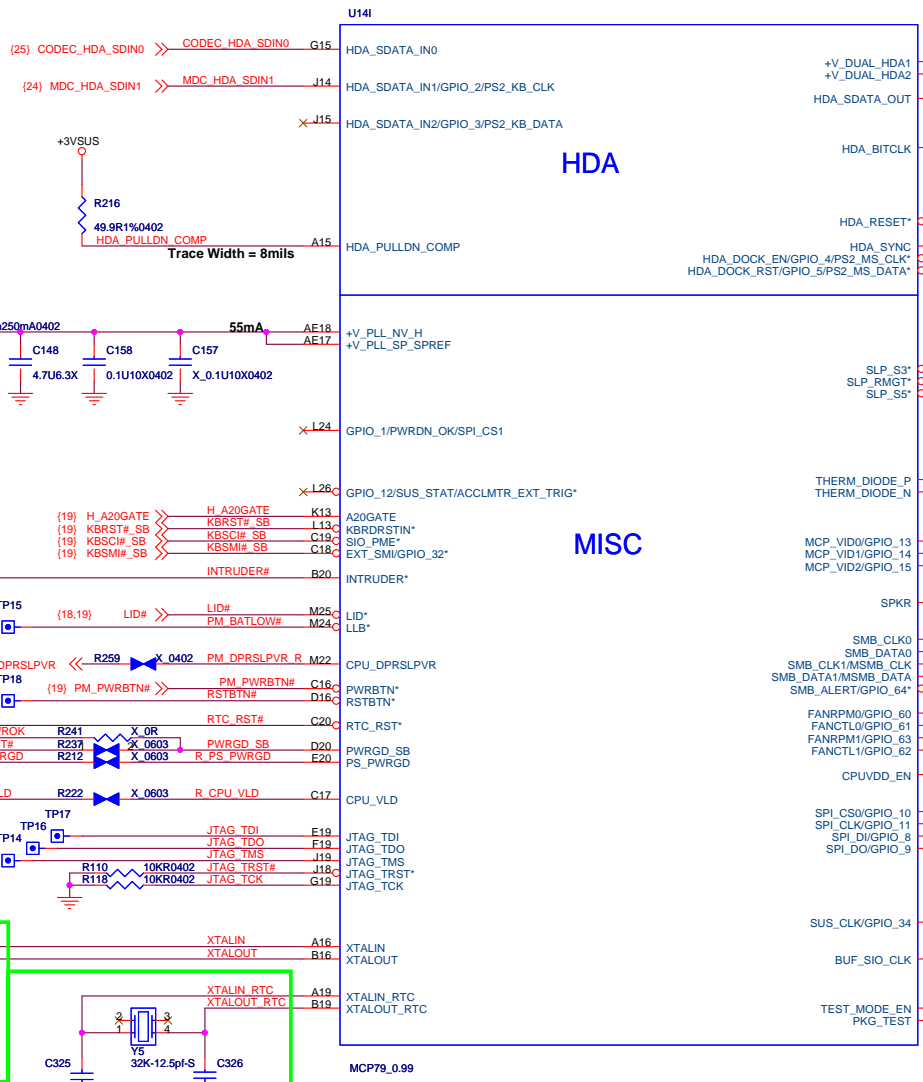


Nvidia Recommend : (+DVDD_SATA)
1x4.7u
1x0.1u

Nvidia Recommend : (+AVDD_SATA)
1xBead
1x10u
1x4.7u
2x0.1u

Trace Width = 8mils

Trace Width = 8mils



Nvidia Recommend : (+V_PLL_NV_H)
1xBead
1x4.7u
2x0.1u

Nvidia Recommend : (+V_DUAL_HDA)
1x4.7u
1x0.1u

Nvidia Recommend
PWRGD SB
R228 X 100KR0402

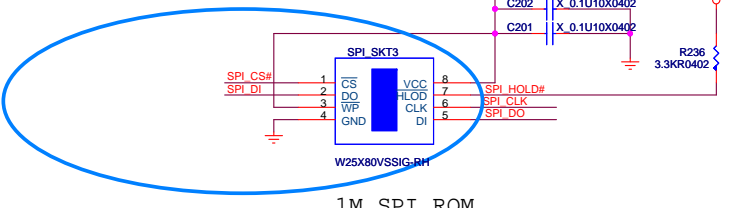
Within 1"
C332 15P50N0402
C331 15P50N0402
Y4 25MHZ18p S-RH

Within 1"
C325 18P50N0402
Y5 32K-12.5p-S
C326 18P50N0402

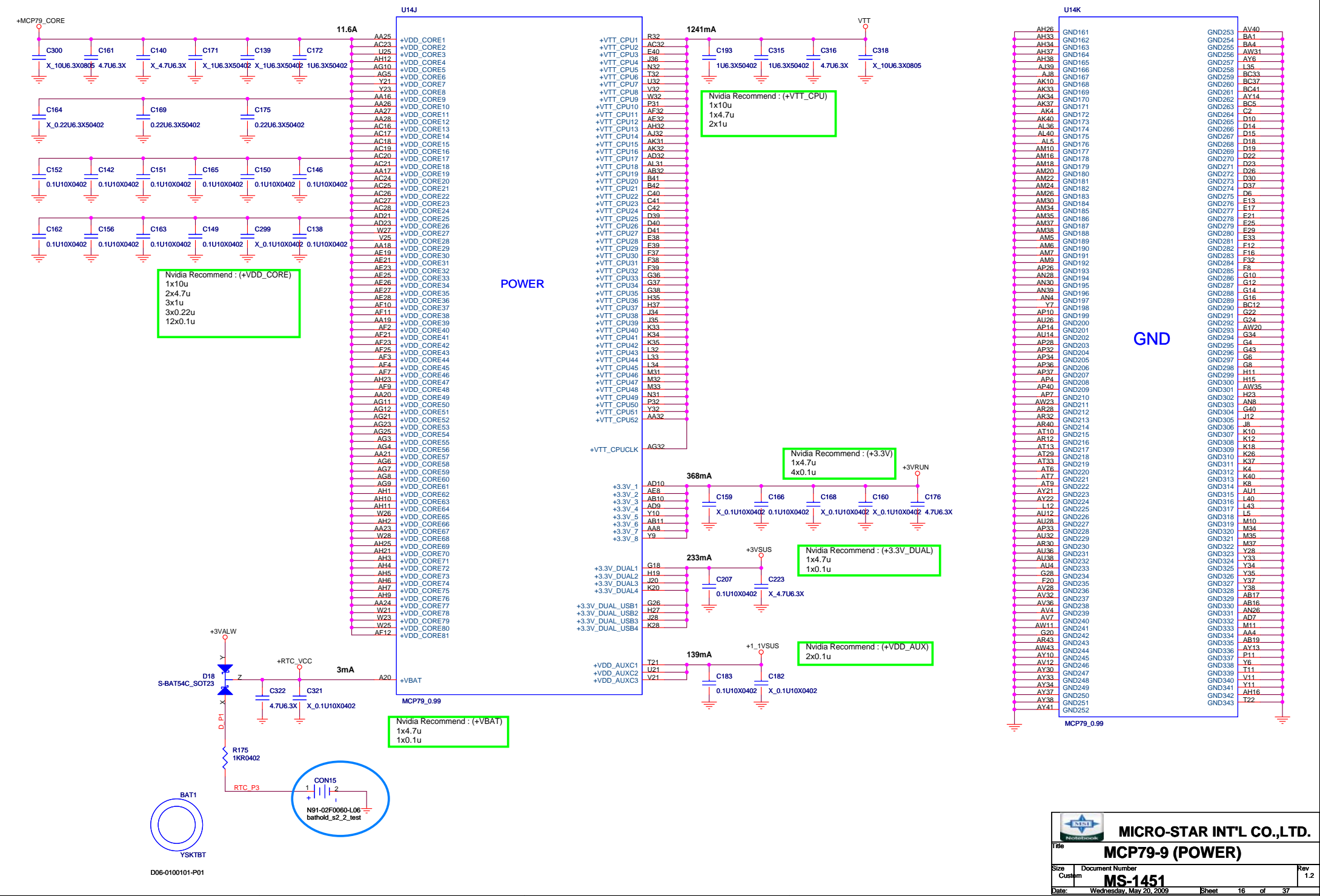
HDA_SDOUT(MSB)
LPC_FRAME#(LSB)
00=LPC BIOS
01=PCI BIOS
10=SPI BIOS CS0
11=SPI BIOS CS1

R_SPI_MOSI(MSB)
R_SPI_CLK(LSB)
00=31MHz
01=42MHz
10=25MHz
11=1MHz

EMI Solution
C102 X_C10p50N0402



1M SPI ROM



Nvidia Recommend : (+VDD_CORE)
 1x10u
 2x4.7u
 3x1u
 3x0.22u
 12x0.1u

Nvidia Recommend : (+VTT_CPU)
 1x10u
 1x4.7u
 2x1u

Nvidia Recommend : (+3.3V)
 1x4.7u
 4x0.1u

Nvidia Recommend : (+3.3V_DUAL)
 1x4.7u
 1x0.1u

Nvidia Recommend : (+VDD_AUX)
 2x0.1u

Nvidia Recommend : (+VBA1)
 1x4.7u
 1x0.1u

POWER

GND

MICRO-STAR INT'L CO.,LTD.

MCP79-9 (POWER)

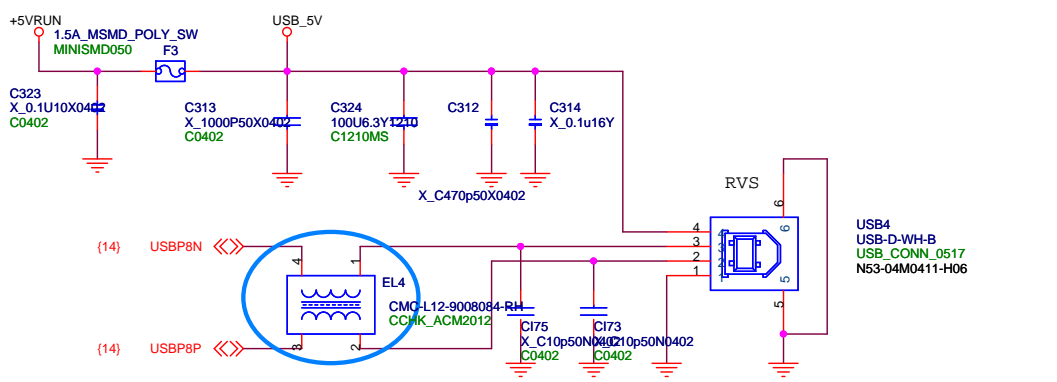
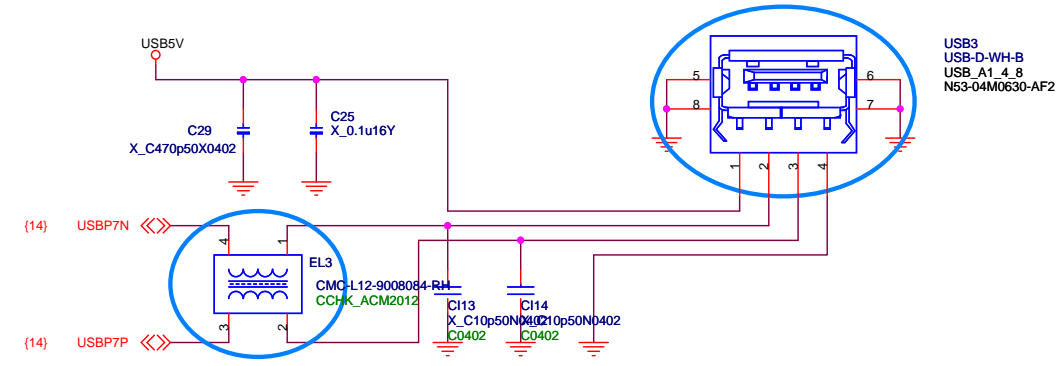
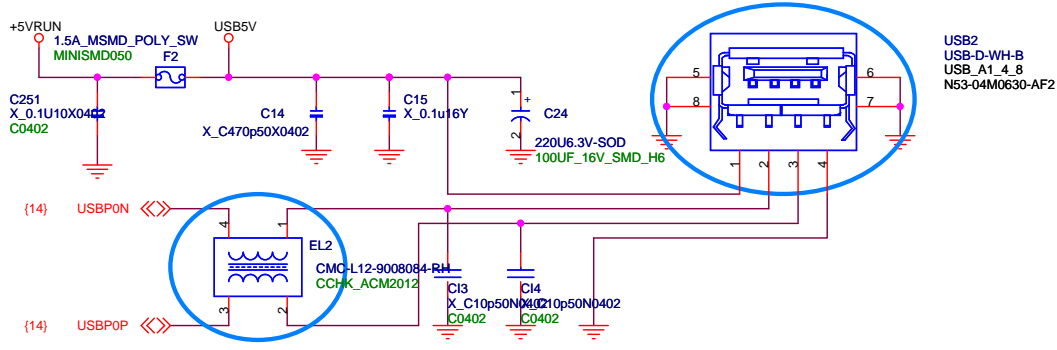
MS-1451

Wednesday, May 20, 2009

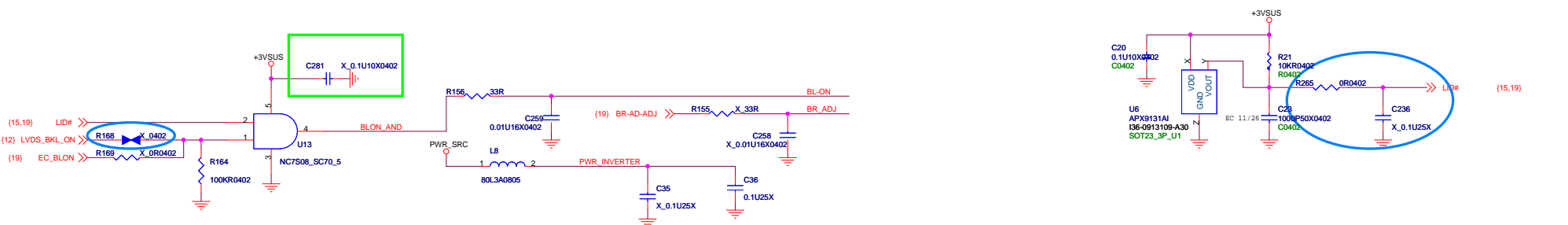
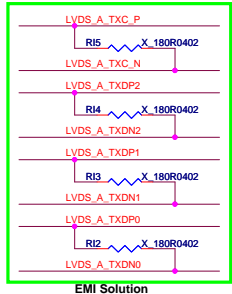
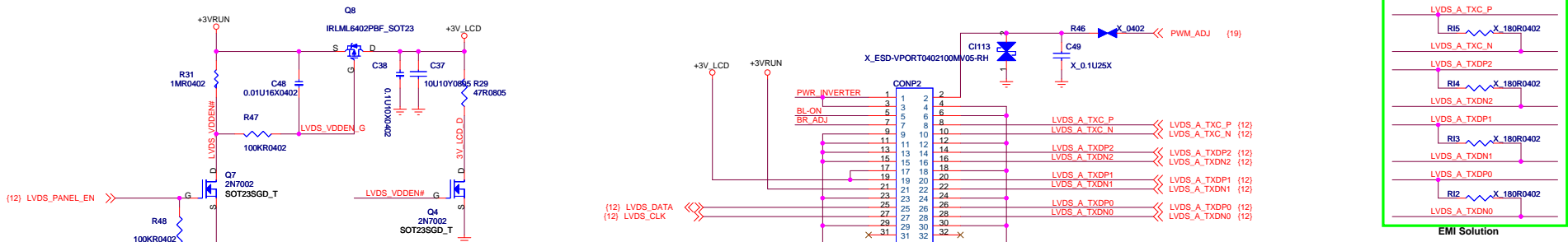
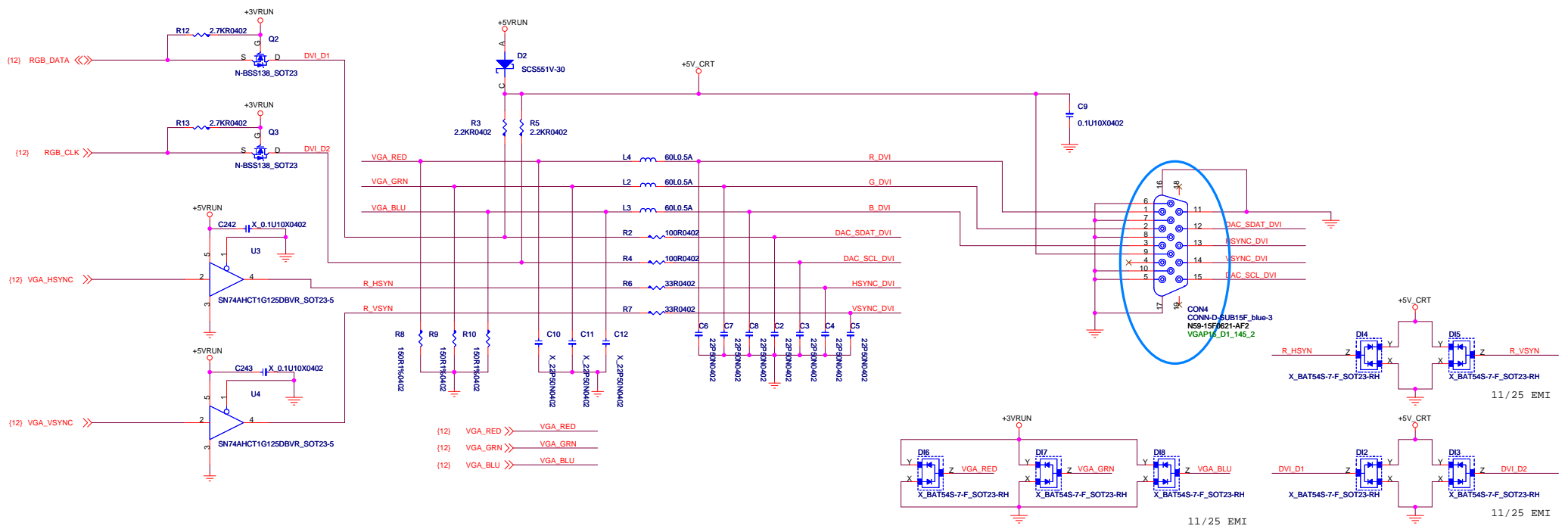
Sheet 16 of 37

D06-0100101-P01

Rev 1.2



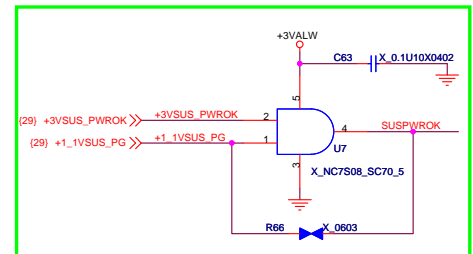
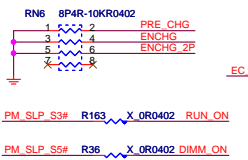
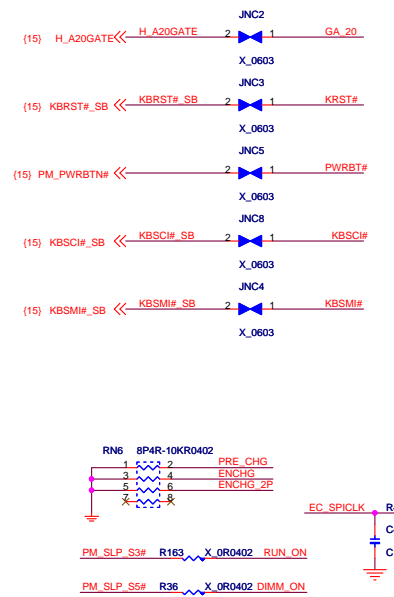
Title		
USB_CONN		
Size	Document Number	Rev
B	MS-1451	1.2
Date:	Wednesday, May 20, 2009	Sheet 17 of 37



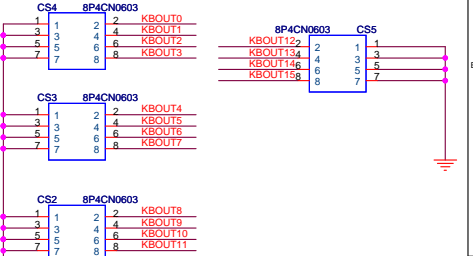
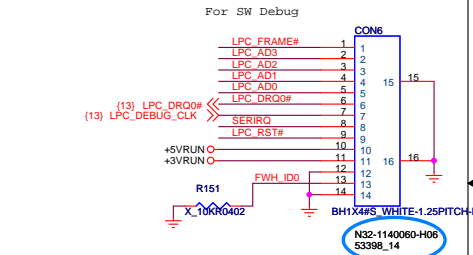
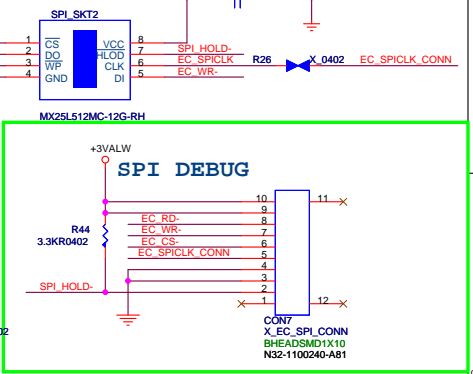
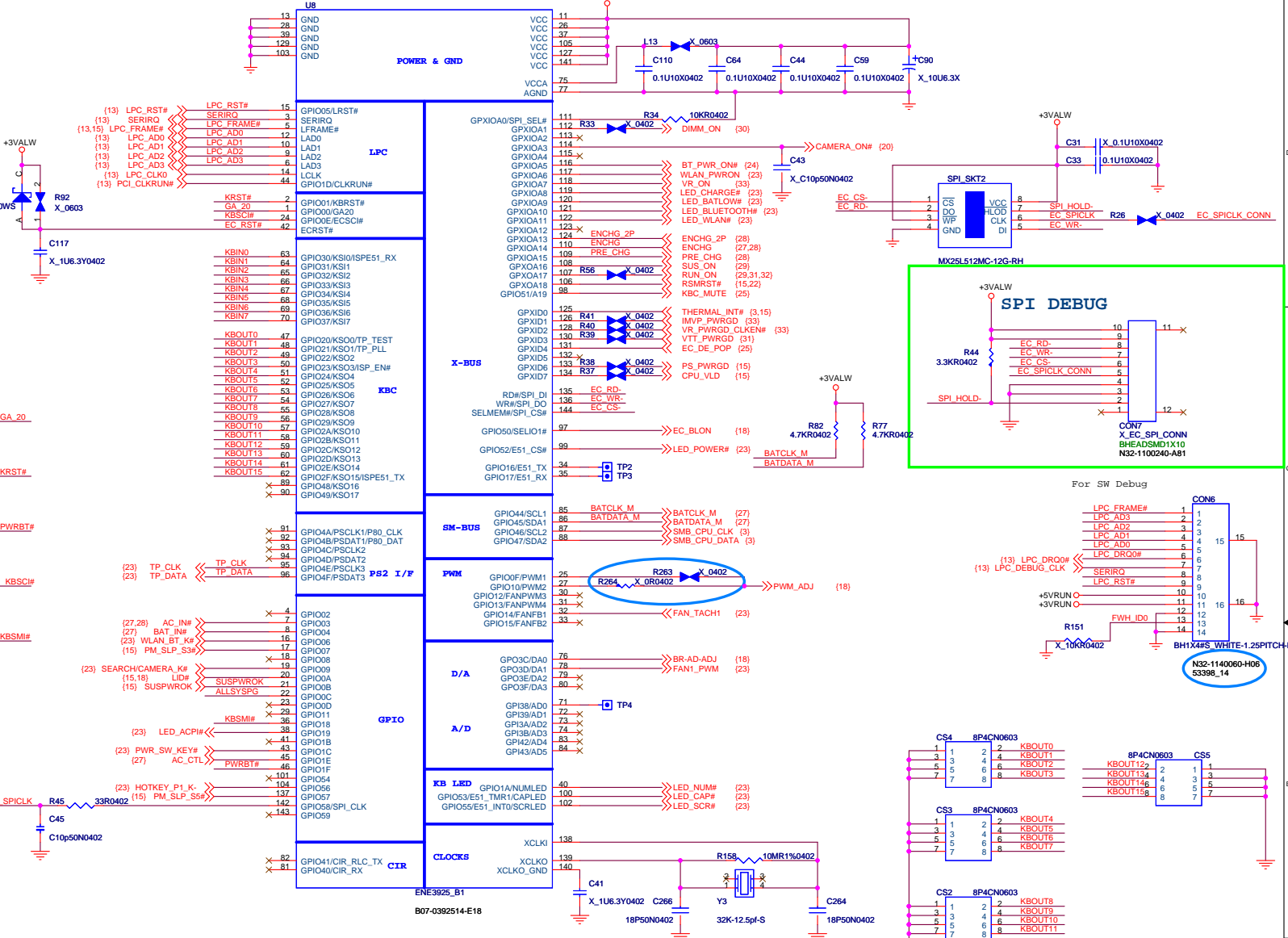
KeyBoard

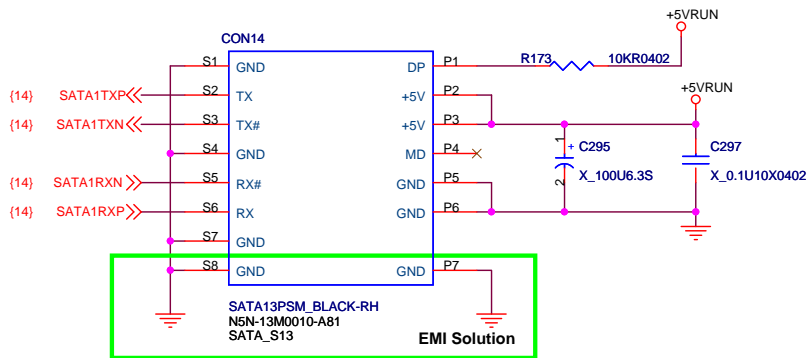
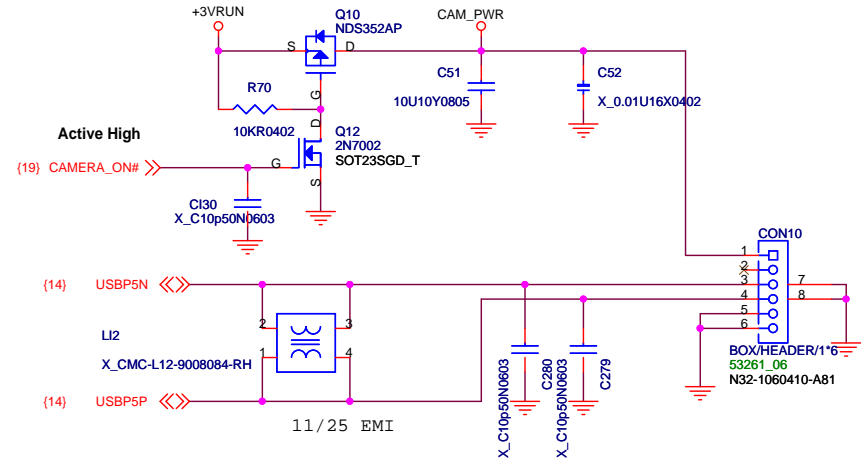
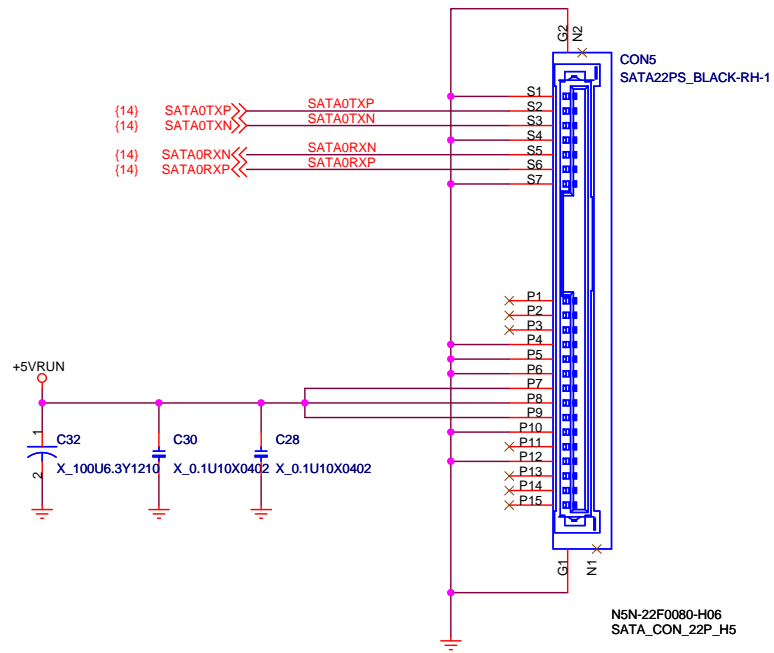
KBOUT0	25	25
KBOUT1	24	24
KBOUT2	23	23
KBIN0	22	22
KBIN1	21	21
KBIN2	20	20
KBIN3	19	19
KBOUT3	18	18
KBOUT4	17	17
KBIN4	16	16
KBIN5	15	15
KBIN6	14	14
KBIN7	13	13
KBOUT5	12	12
KBOUT6	11	11
KBOUT7	10	10
KBOUT8	9	9
KBOUT9	8	8
KBOUT10	7	7
KBOUT11	6	6
KBOUT12	5	5
KBOUT13	4	4
KBOUT14	3	3
KBOUT15	2	2

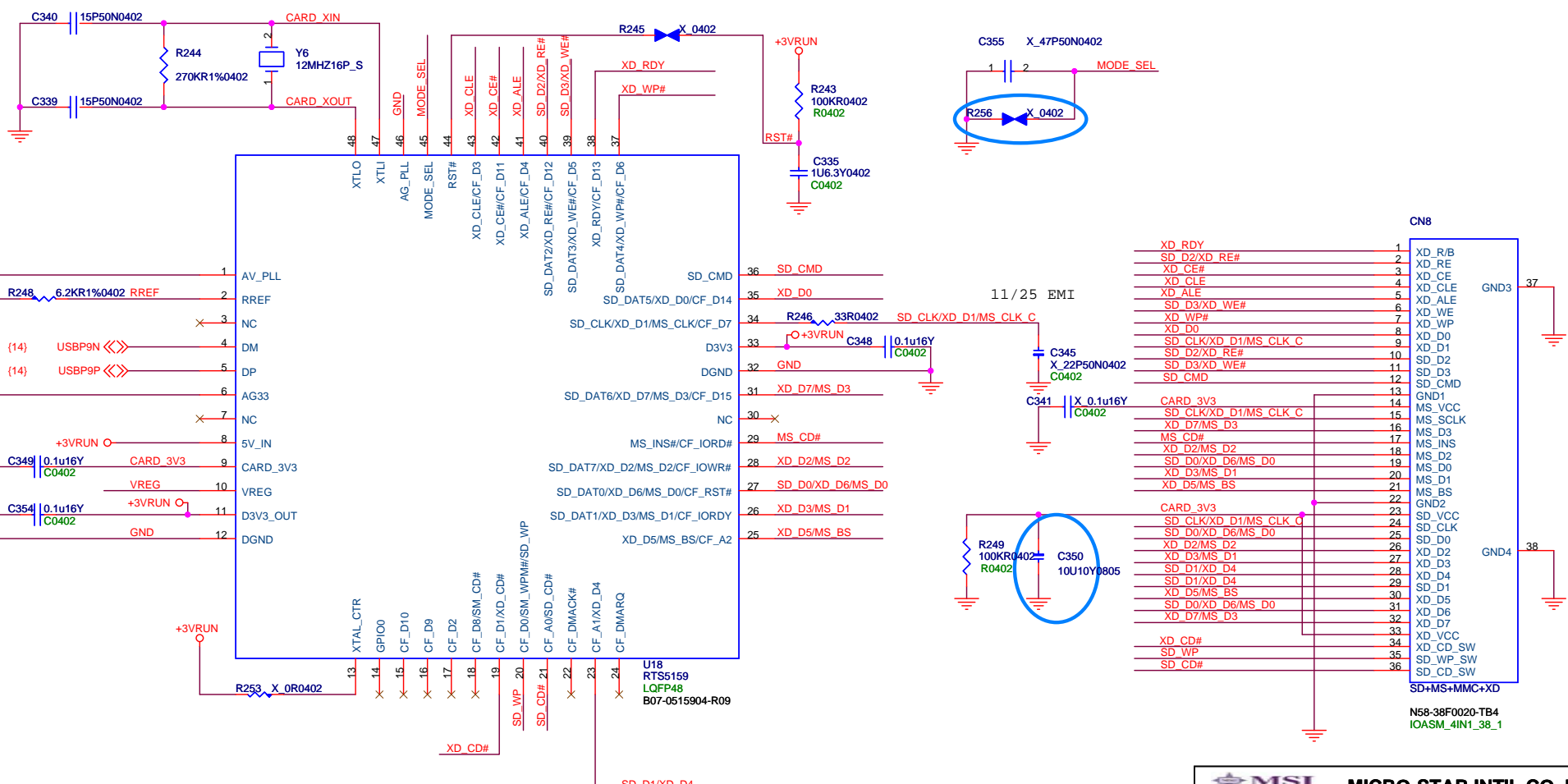
CONN2
CONN-FFC25B_WHITE-RH
FFC_S25_1
NSA-25F0080-A81



ADD R370 for Cost Down





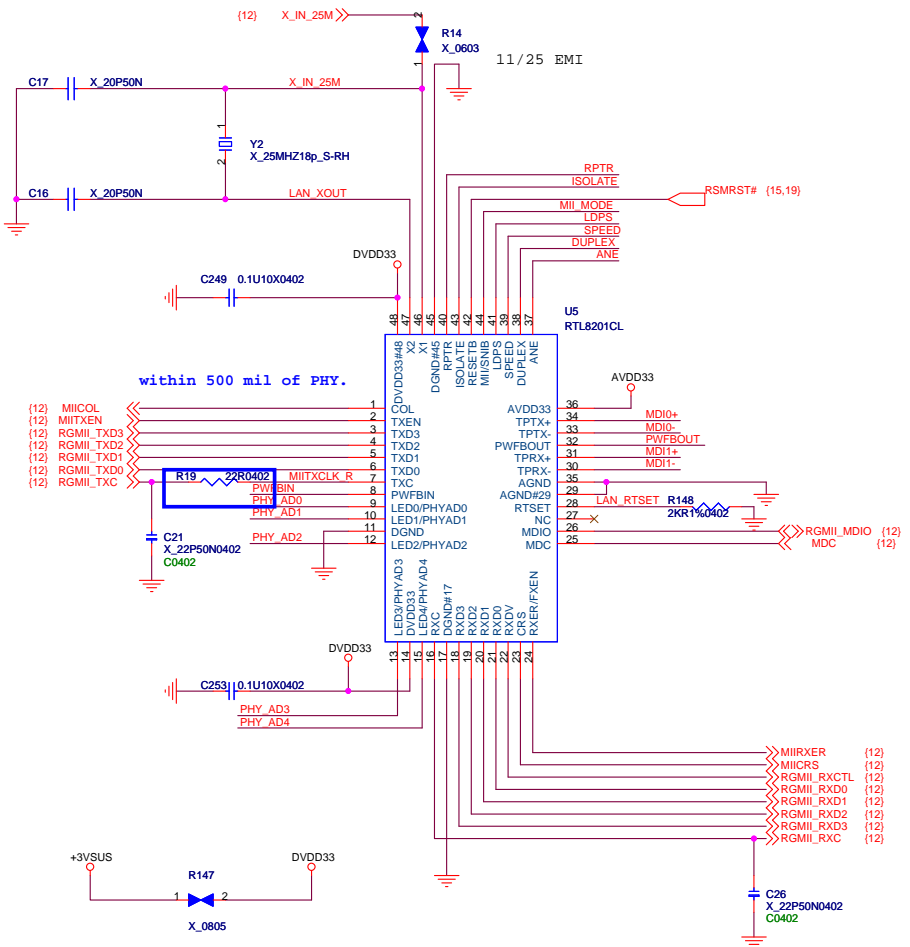


MSI MICRO-STAR INT'L CO.,LTD.

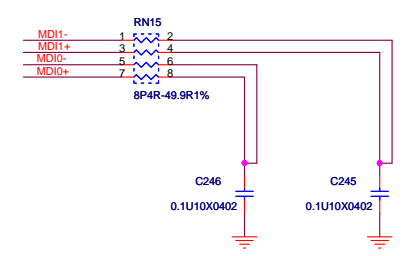
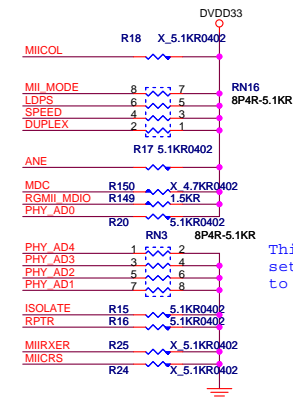
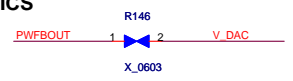
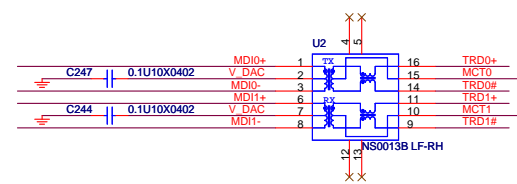
Title: **CARD READER (RTS5159)**

Size: Custom Document Number: **MS-1451** Rev: 1.2

Date: Wednesday, May 20, 2009 Sheet 21 of 37

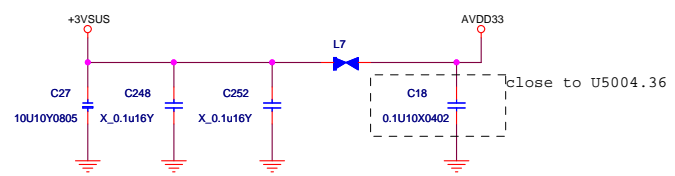
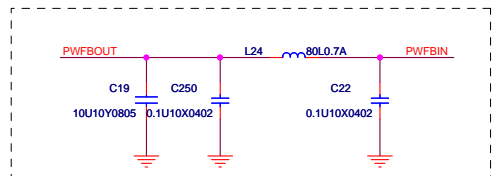
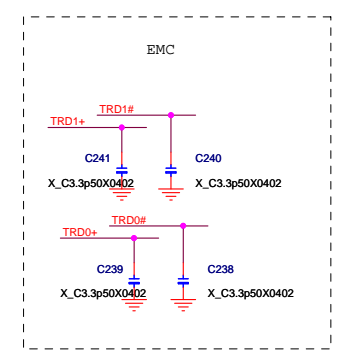
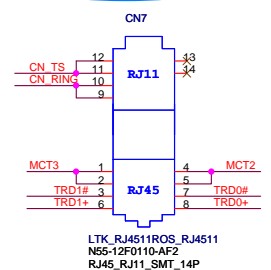
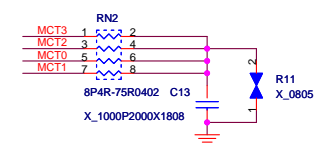
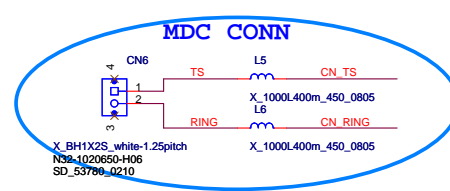


LAN MAGNETICS



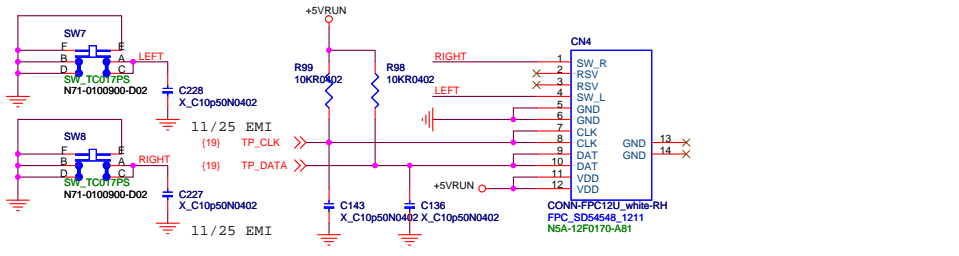
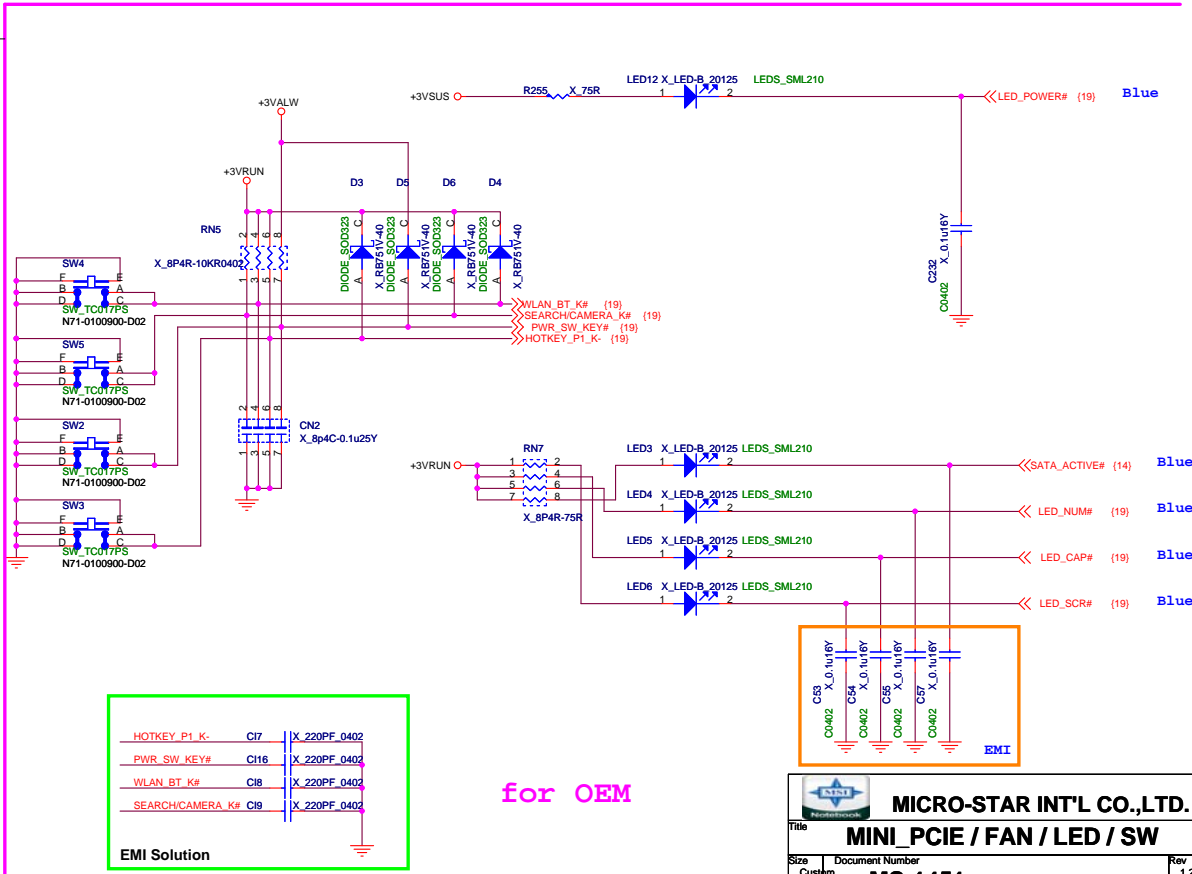
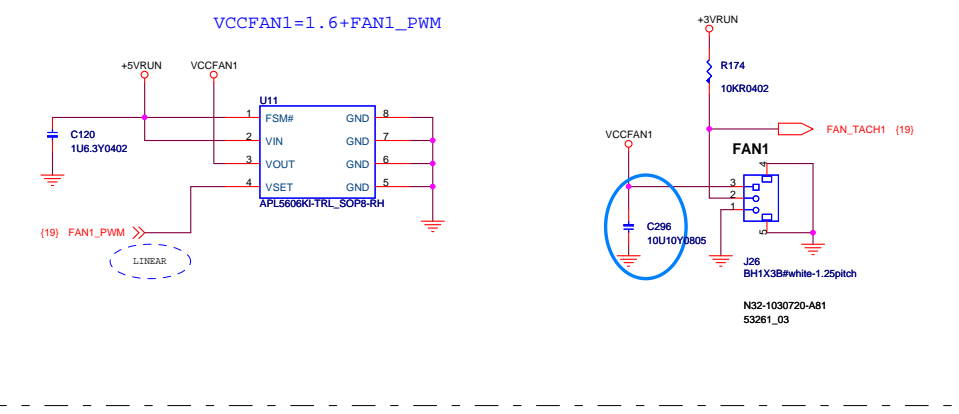
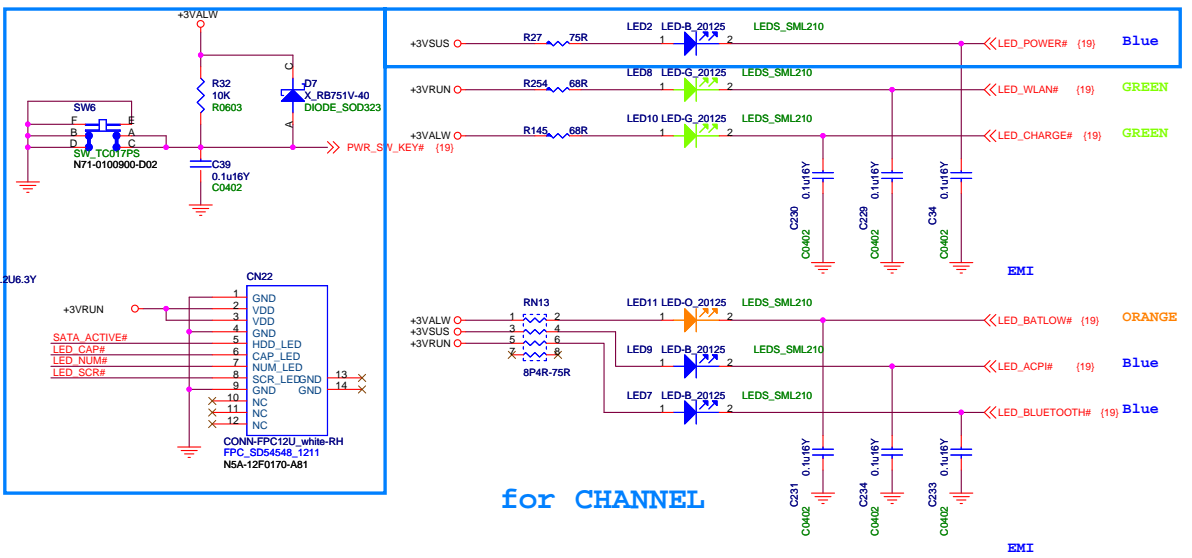
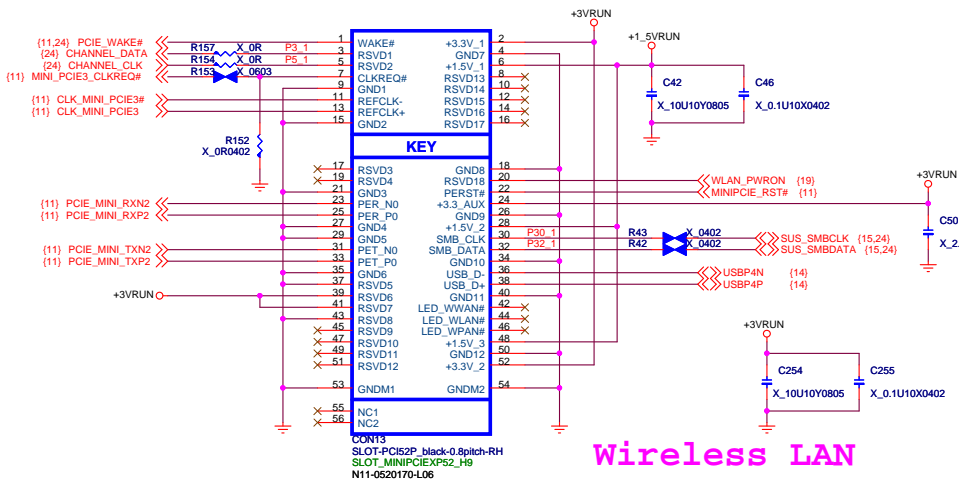
This schematic sets PHY address to 00001b.

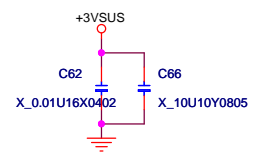
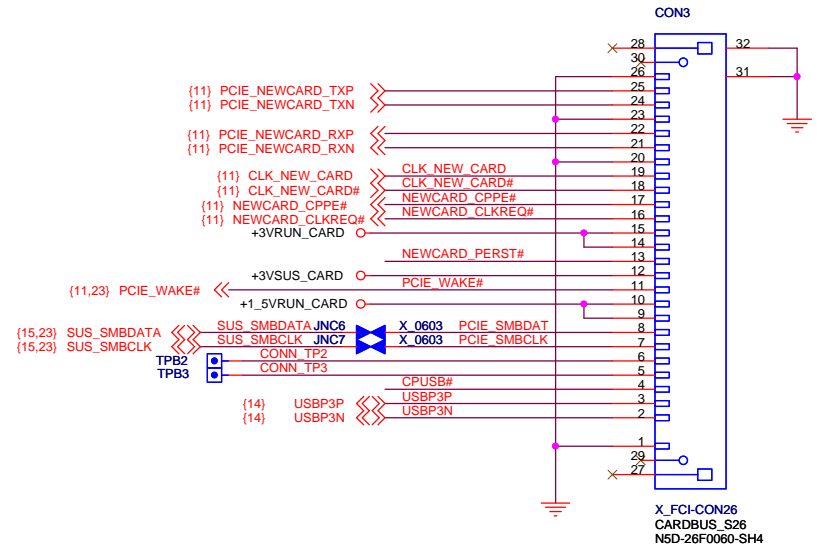
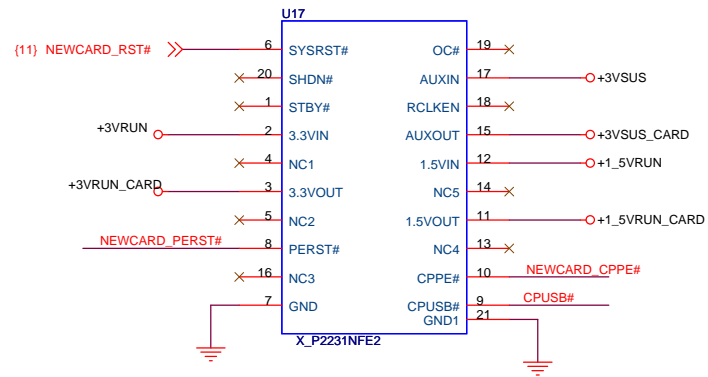
R375 R376 C514 close U5004
R377 R379 C513 close U5003



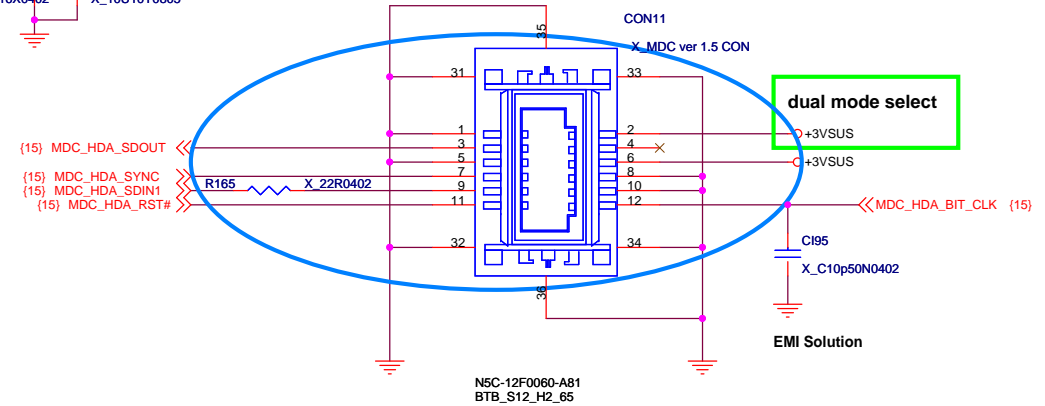
please C416, C417, L32 close to PWFBOOUT(U5004.32) and C418 close to PWFBIN (U5004.8)

MICRO-STAR INT'L CO.,LTD.
LAN (RTL8201CL)
 Title: _____
 Size: _____ Document Number: **MS-1451** Rev: 1.2
 Date: Wednesday, May 20, 2009 Sheet: 22 of 37





MDC Connector Ver 1.5

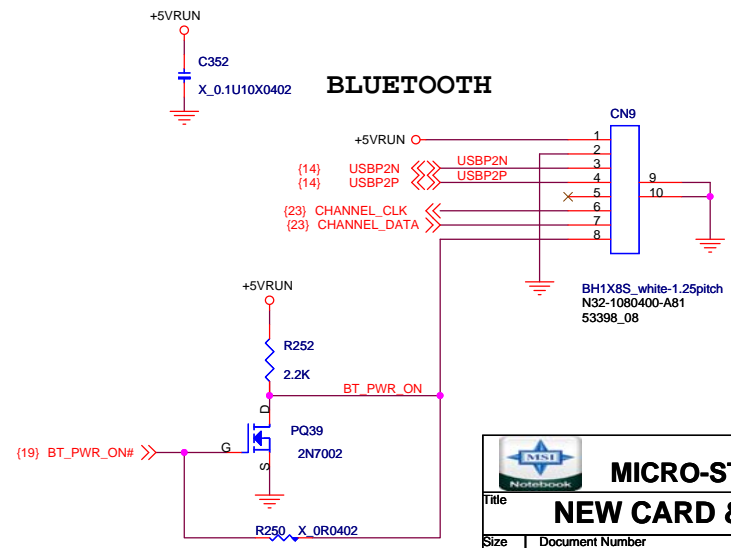


N5C-12F0060-A81
BTB_S12_H2_65

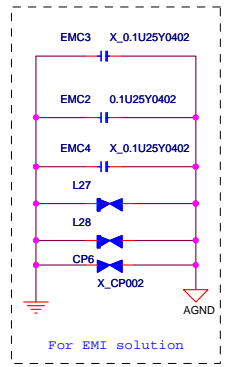
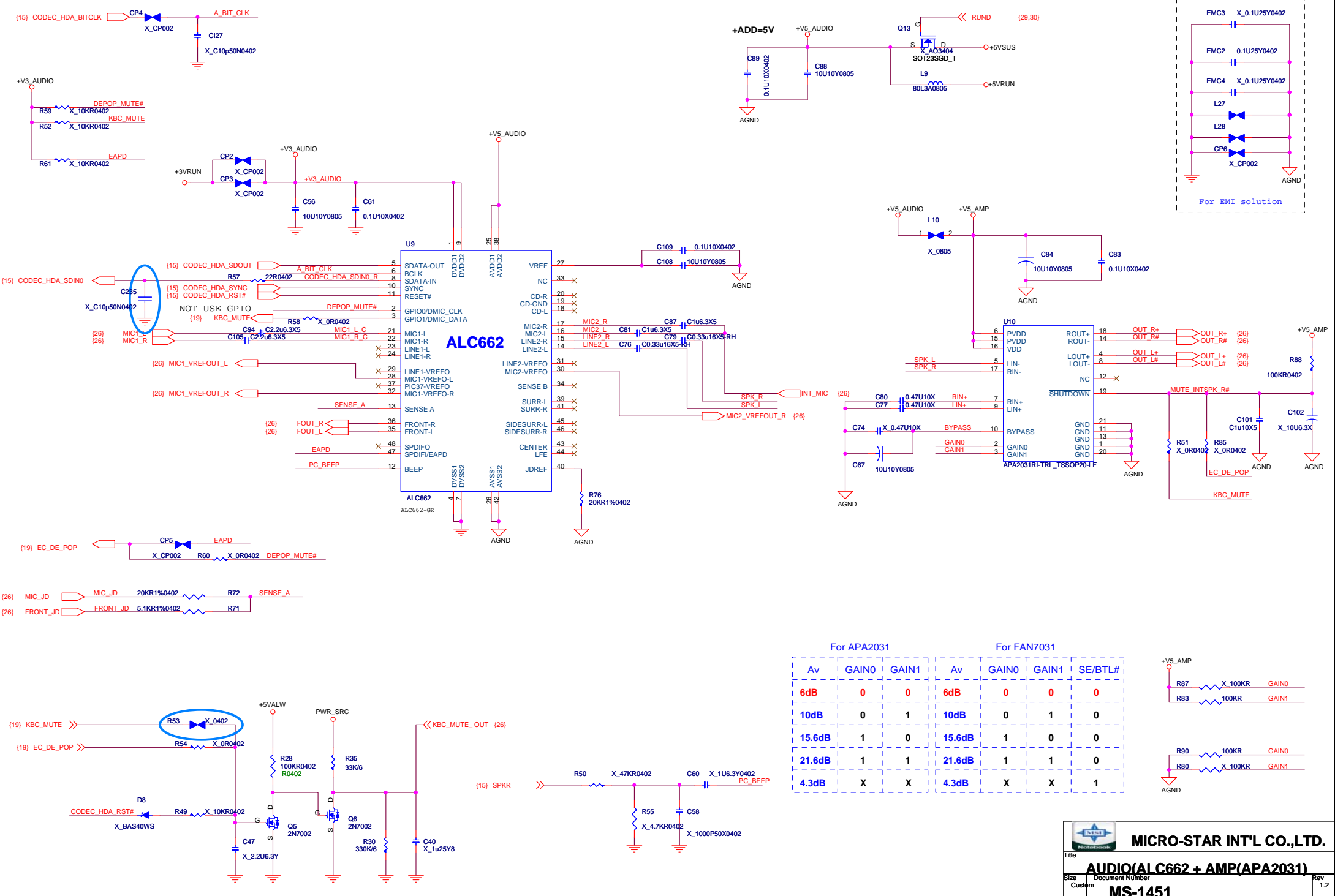
dual mode select

EMI Solution

BLUETOOTH



MICRO-STAR INT'L CO.,LTD.		
NEW CARD & MDC CONN		
Title	Document Number	Rev
	MS-1451	1.2
Date:	Wednesday, May 20, 2009	Sheet 24 of 37

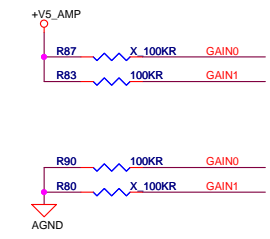


For APA2031

Av	GAIN0	GAIN1
6dB	0	0
10dB	0	1
15.6dB	1	0
21.6dB	1	1
4.3dB	X	X

For FAN7031

Av	GAIN0	GAIN1	SE/BTL#
6dB	0	0	0
10dB	0	1	0
15.6dB	1	0	0
21.6dB	1	1	0
4.3dB	X	X	1



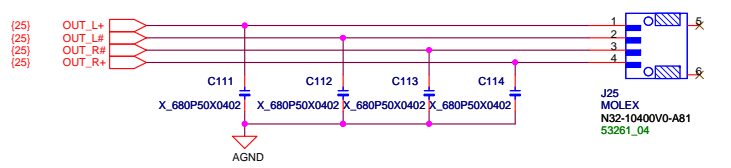
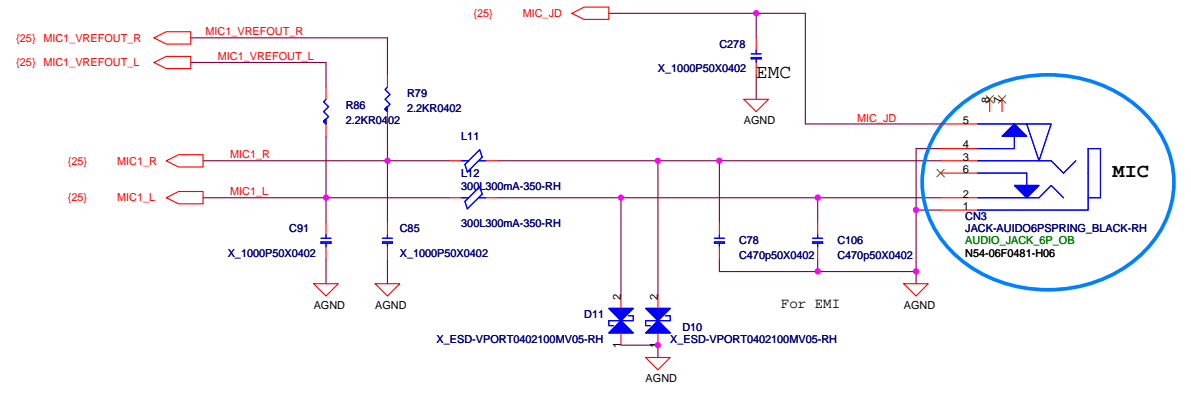
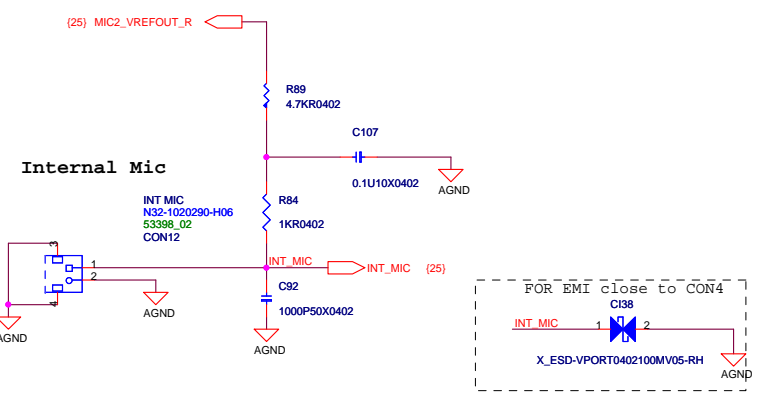
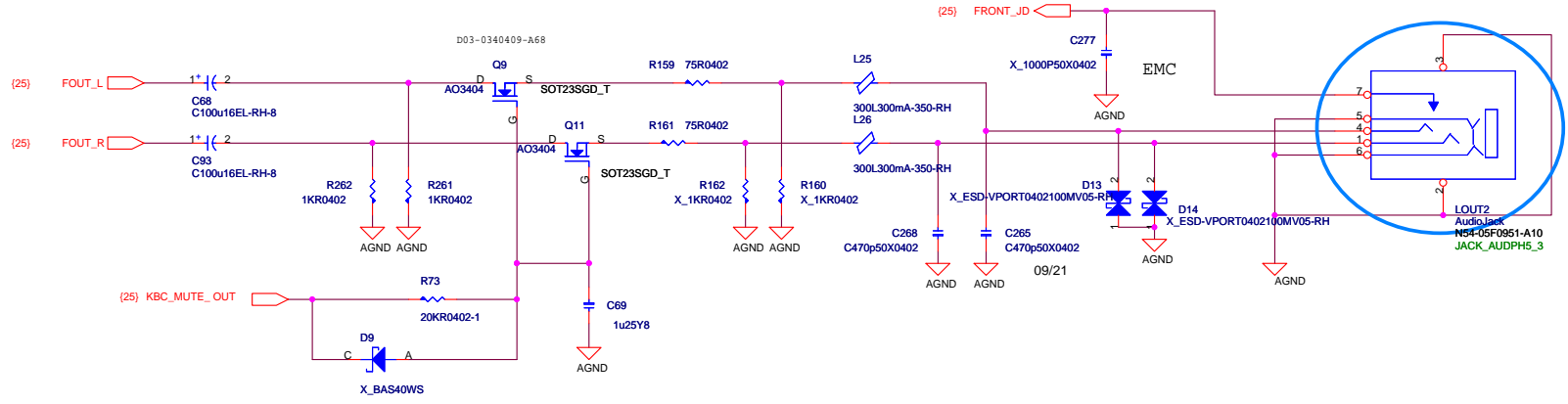
MICRO-STAR INT'L CO.,LTD.


Title: **AUDIO(ALC662 + AMP(APA2031))**

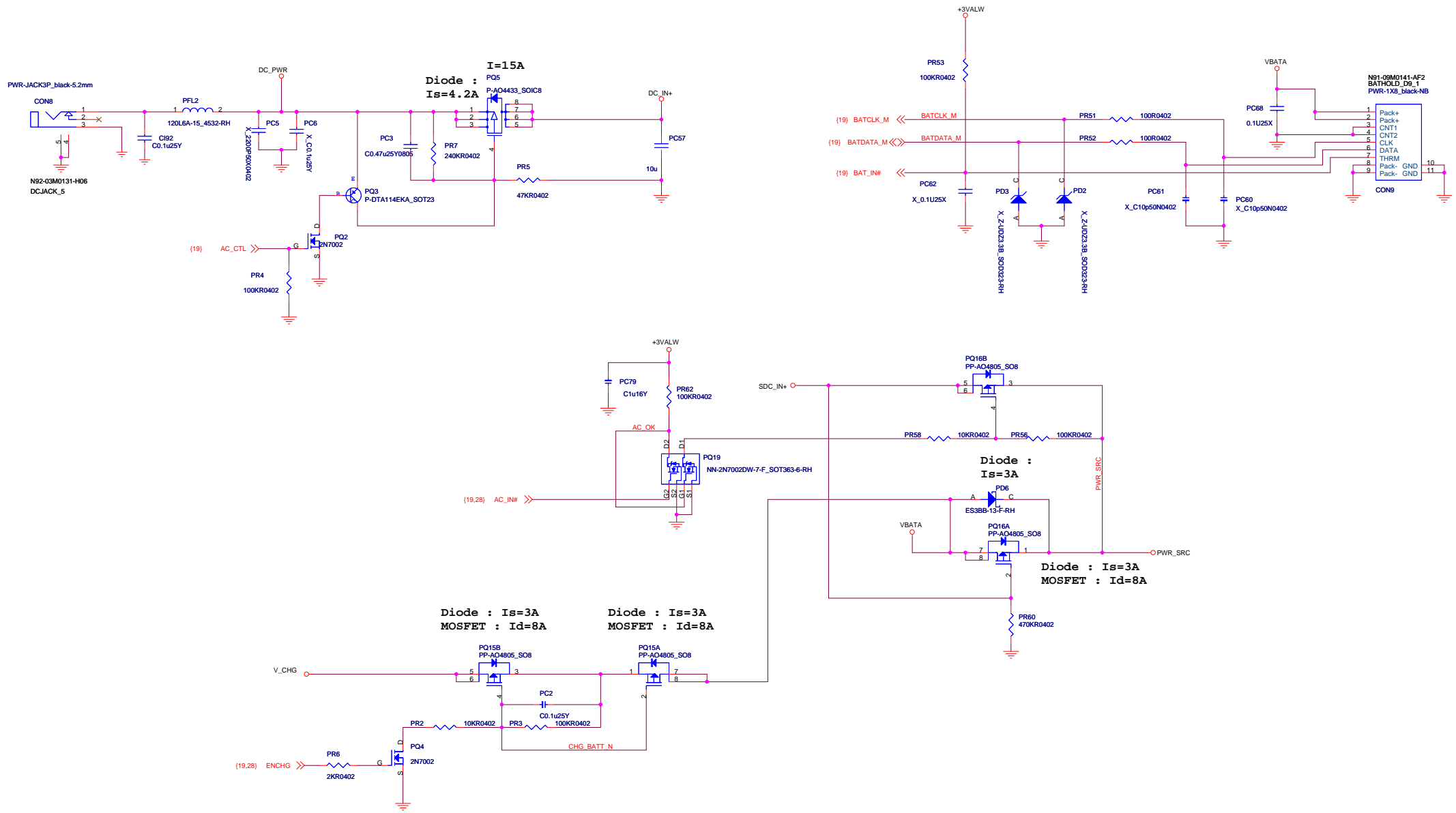
Size: Custom Document Number

Customer: **MS-1451**

Date: Wednesday, May 20, 2009 Sheet 25 of 37



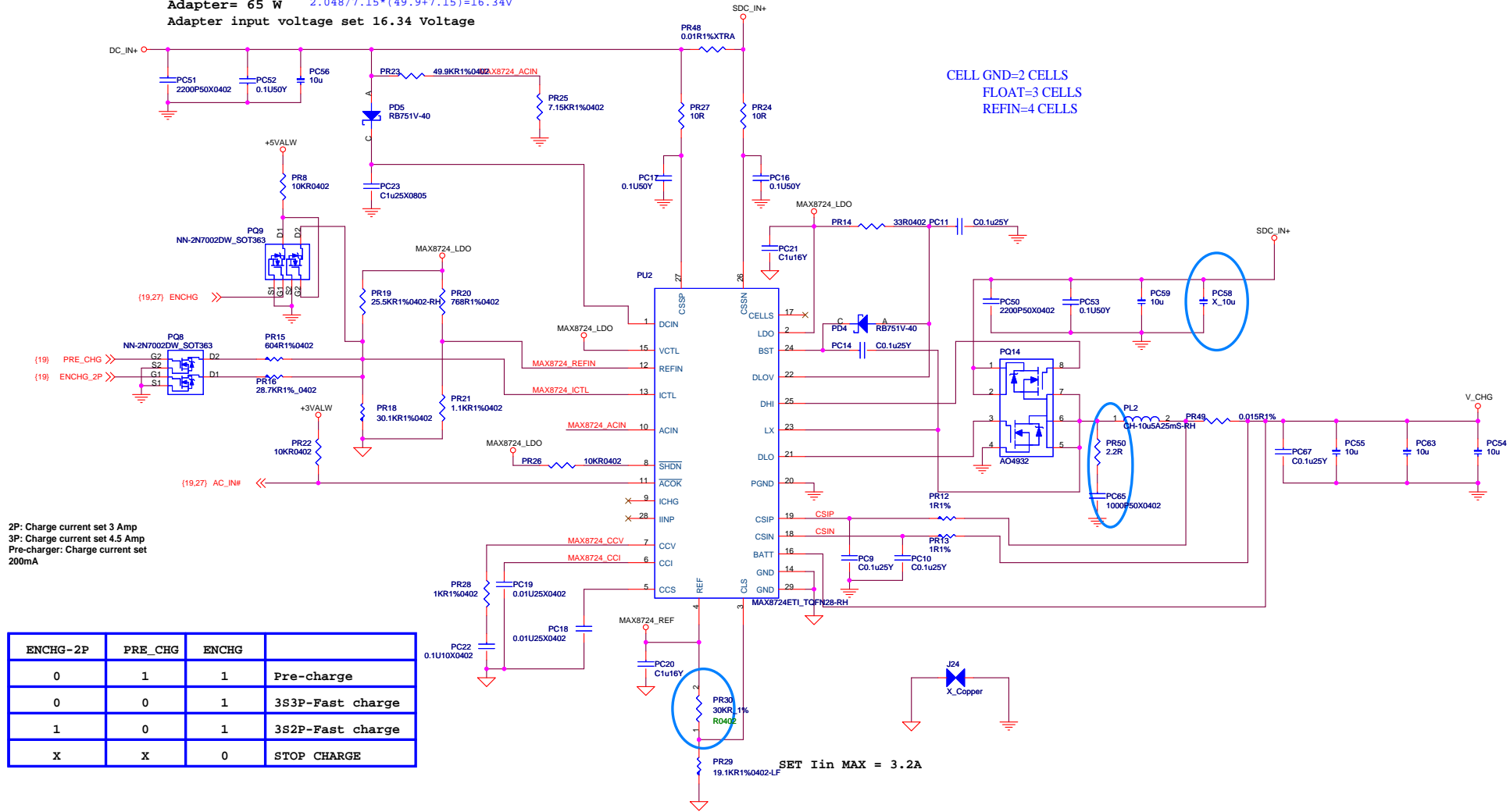
		MICRO-STAR INT'L CO.,LTD.	
Title			
SPK / HP / MIC			
Size Document Number			
Custom MS-1451			
Date: Wednesday, May 20, 2009			
Sheet		26 of 37	
Rev		1.2	



MSI CORPORATION		
Title Battery Select		
Size Custom	Document Number MS-1451	Rev 1.2
Date: Wednesday, May 20, 2009	Sheet 27 of 37	

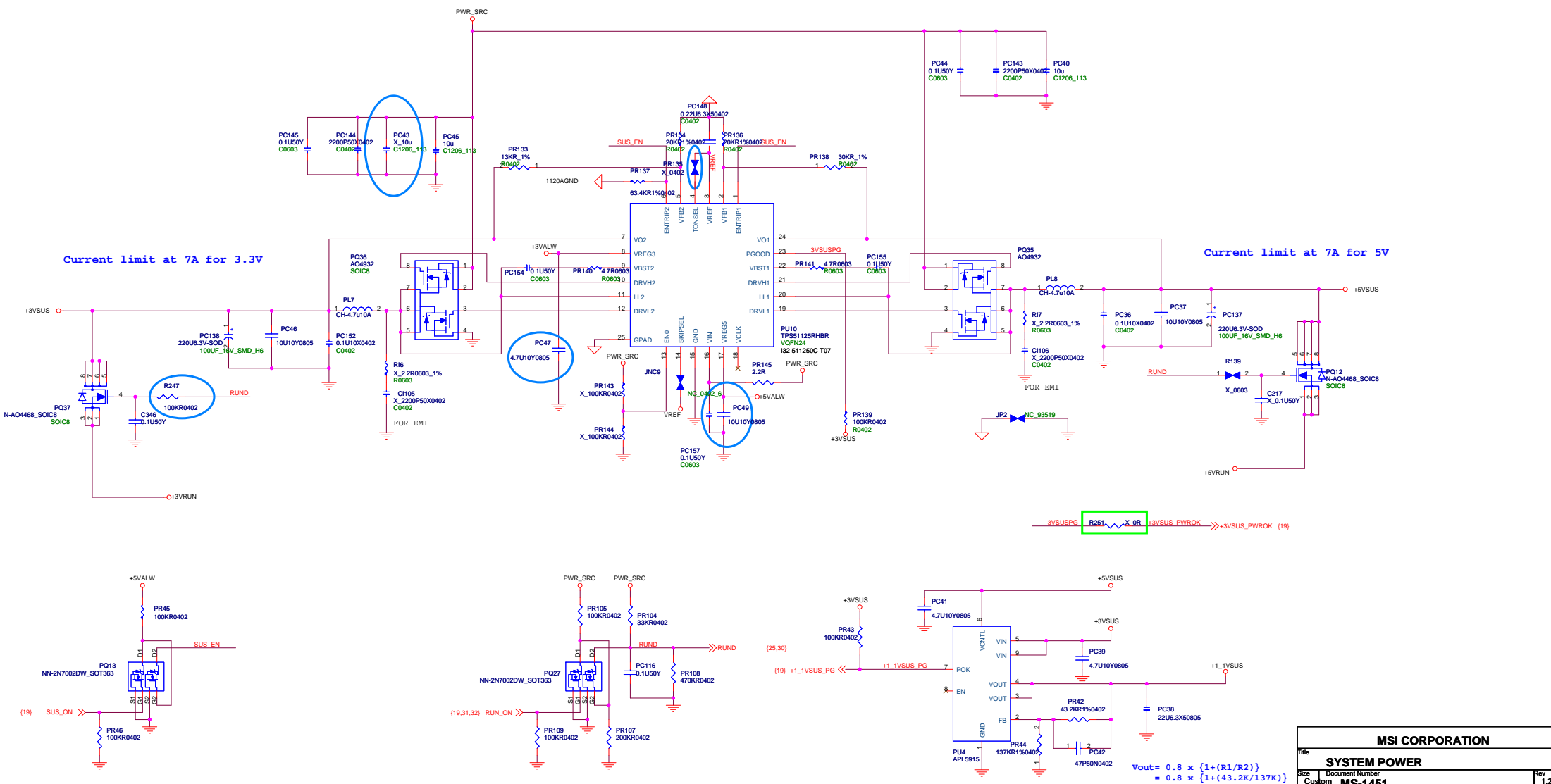
Adapter= 65 W $2.048/7.15*(49.9+7.15)=16.34V$
 Adapter input voltage set 16.34 Voltage

CELL_GND=2 CELLS
 FLOAT=3 CELLS
 REFIN=4 CELLS



2P: Charge current set 3 Amp
 3P: Charge current set 4.5 Amp
 Pre-charger: Charge current set 200mA

ENCHG-2P	PRE_CHG	ENCHG	
0	1	1	Pre-charge
0	0	1	3S3P-Fast charge
1	0	1	3S2P-Fast charge
X	X	0	STOP CHARGE

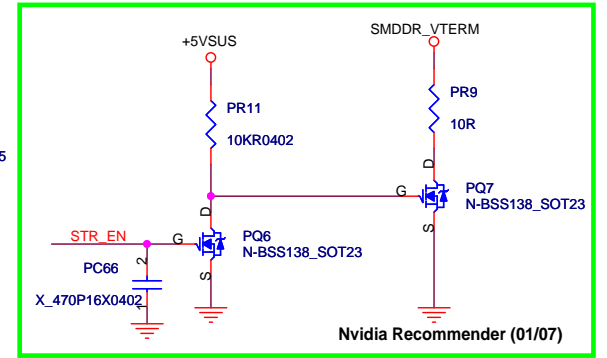
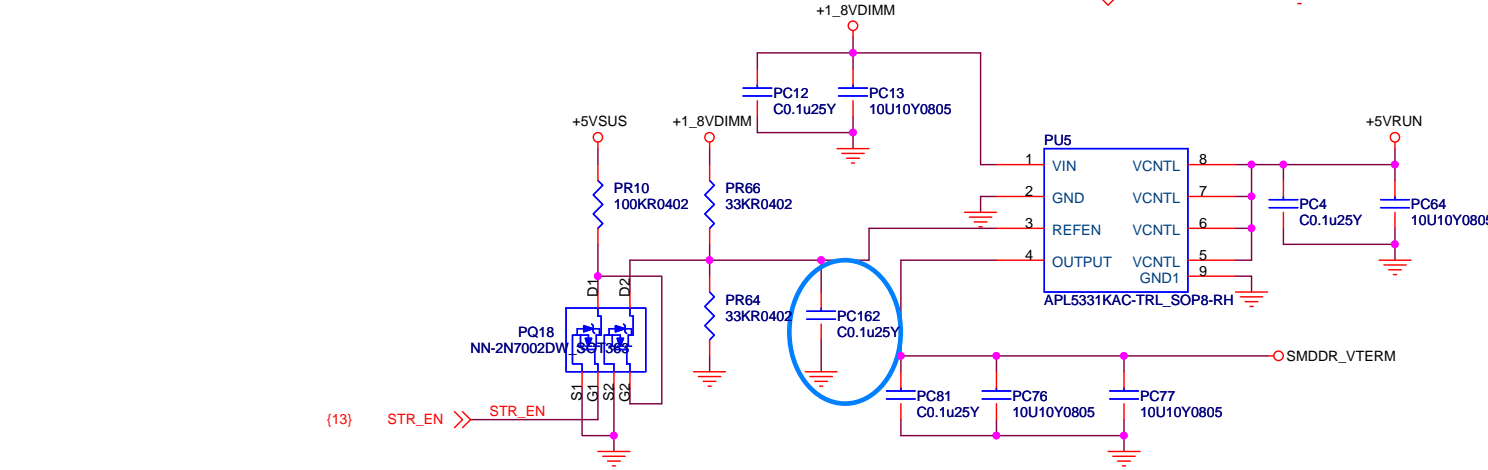
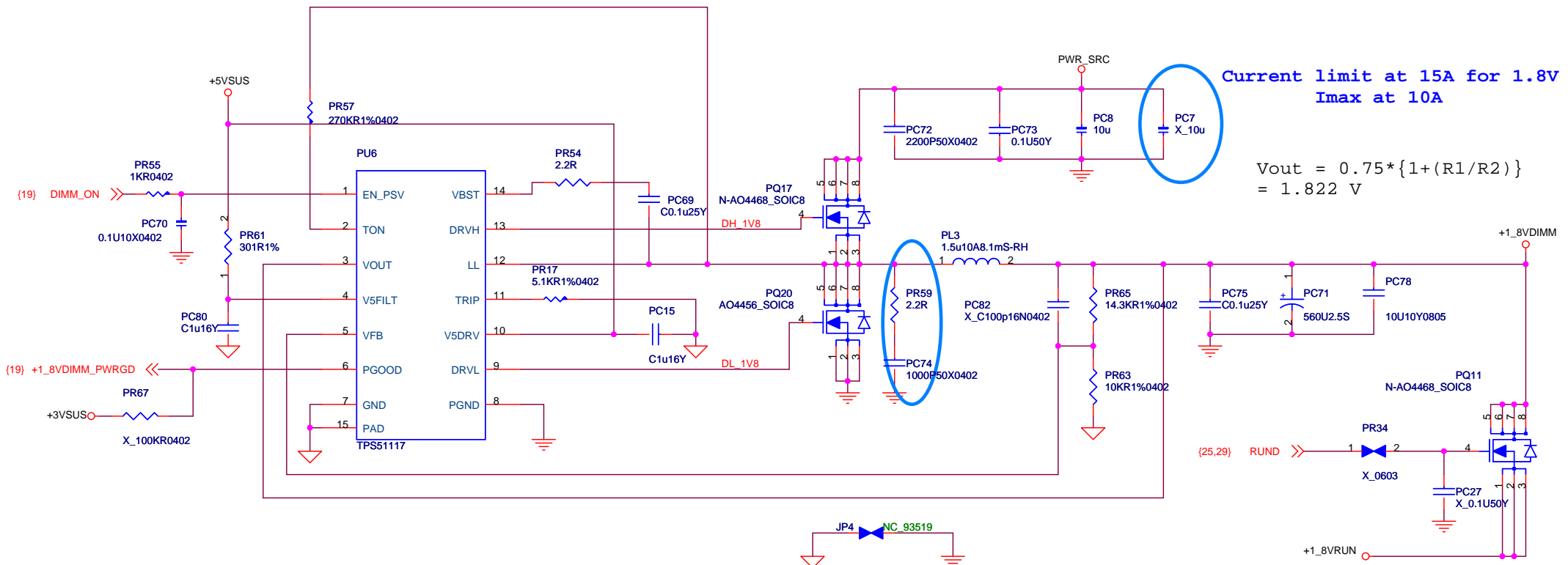


MSI CORPORATION		
Title: SYSTEM POWER		
Size: Document Number	Custom MS-1451	
Date: Wednesday, May 20, 2009	Sheet: 29	of 37
		Rev: 1.2

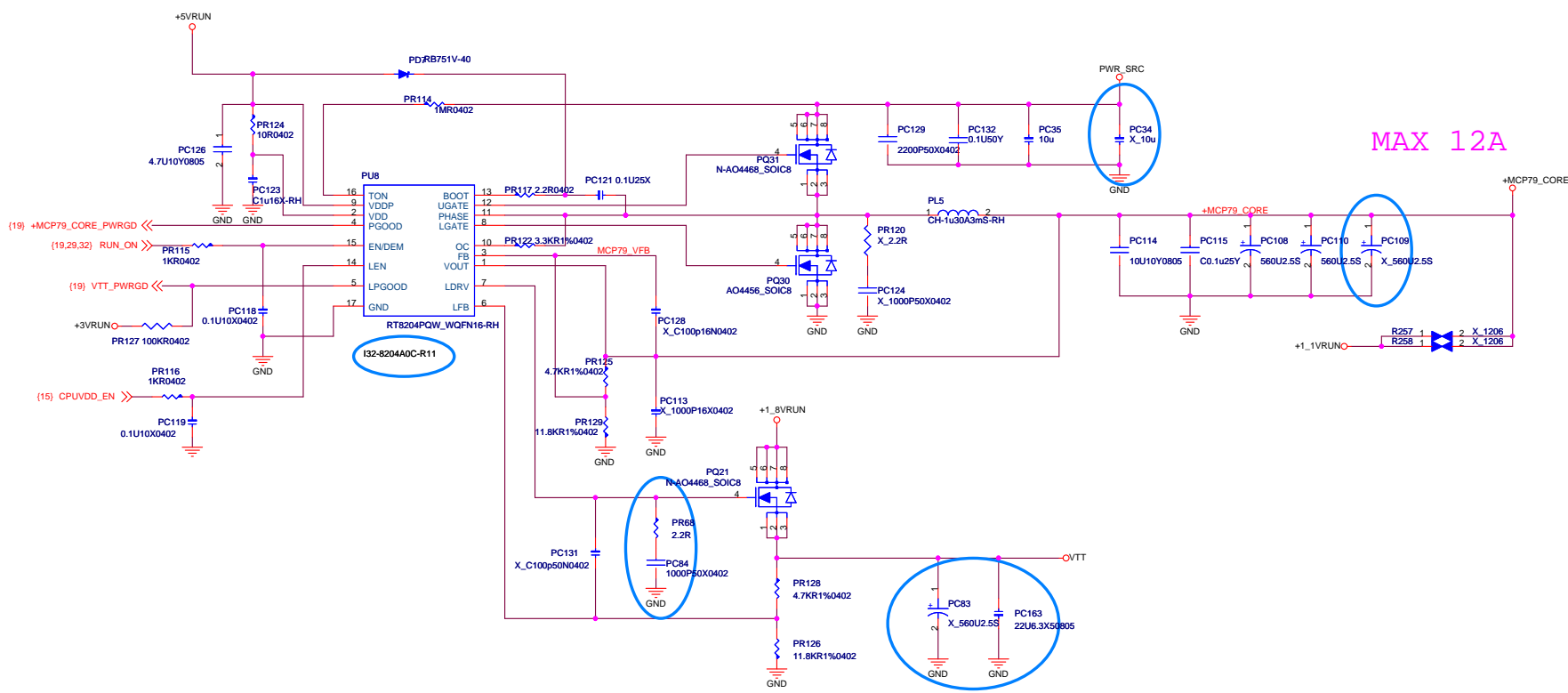
$$V_{out} = 0.8 \times \left(1 + \frac{R1}{R2}\right)$$

$$= 0.8 \times \left(1 + \frac{43.2K}{137K}\right)$$

$$= 1.052 \text{ V}$$



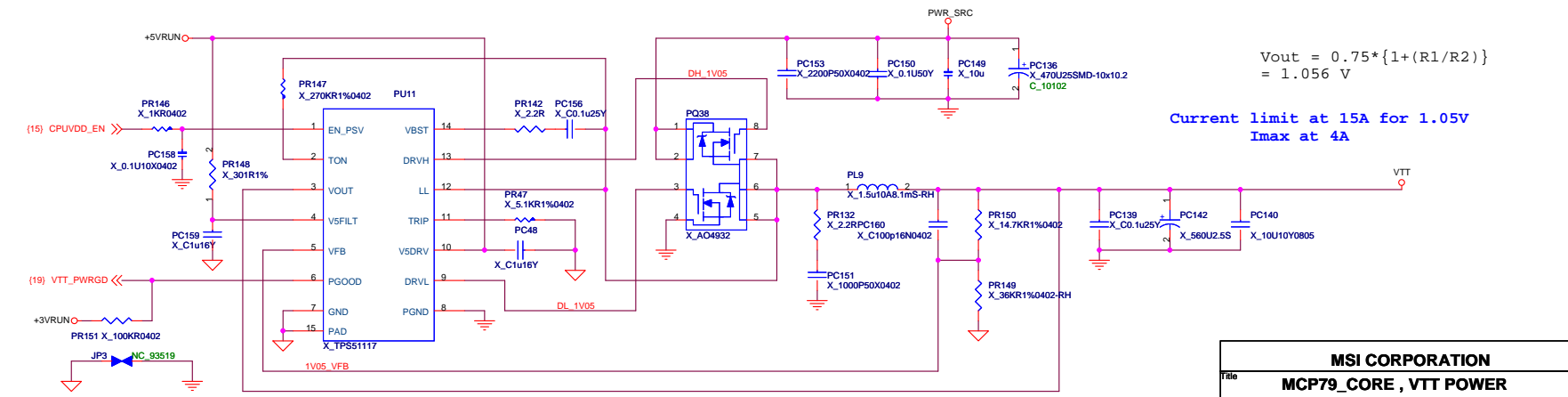
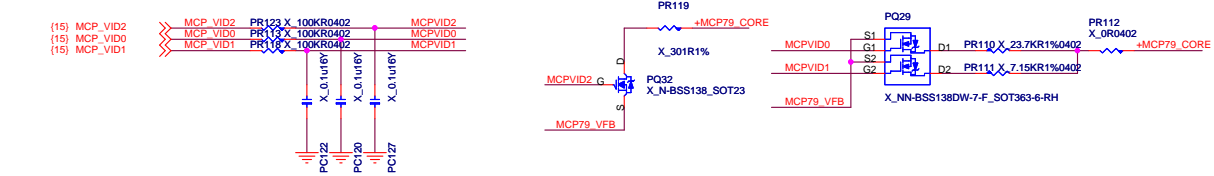
MSI CORPORATION		
Title DDR2 RAM POWER		
Size Custom	Document Number MS-1451	Rev 1.2
Date: Wednesday, May 20, 2009	Sheet 30	of 37



MAX 12A

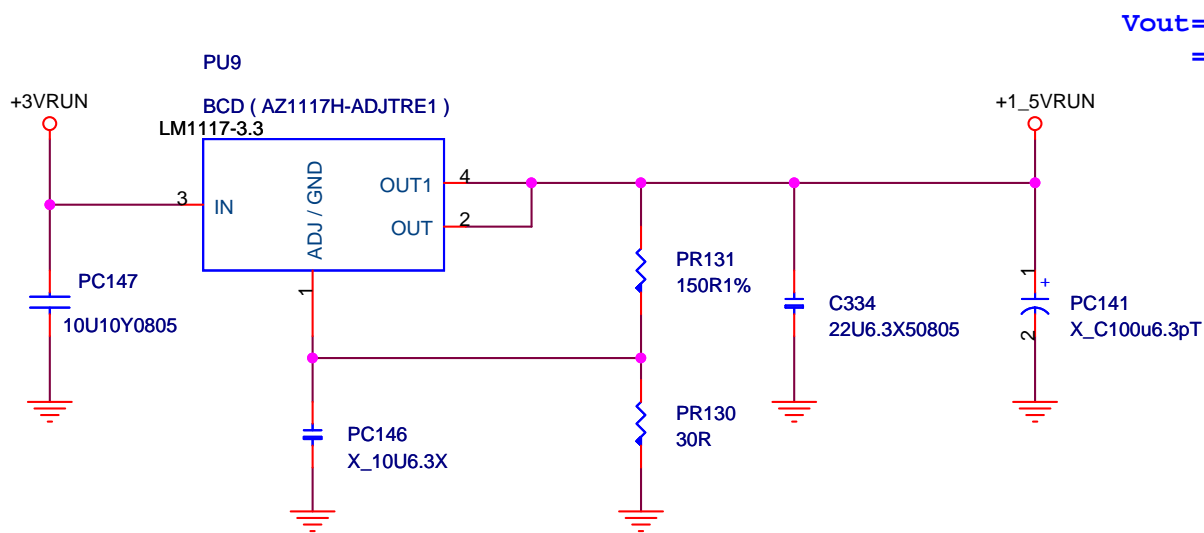
+MCP CORE POWER TABLE

VID2	VID1	VID0	+MCP CORE POWER
0	0	0	1.056 V
0	0	1	1.007 V
0	1	0	0.937 V
0	1	1	0.918 V

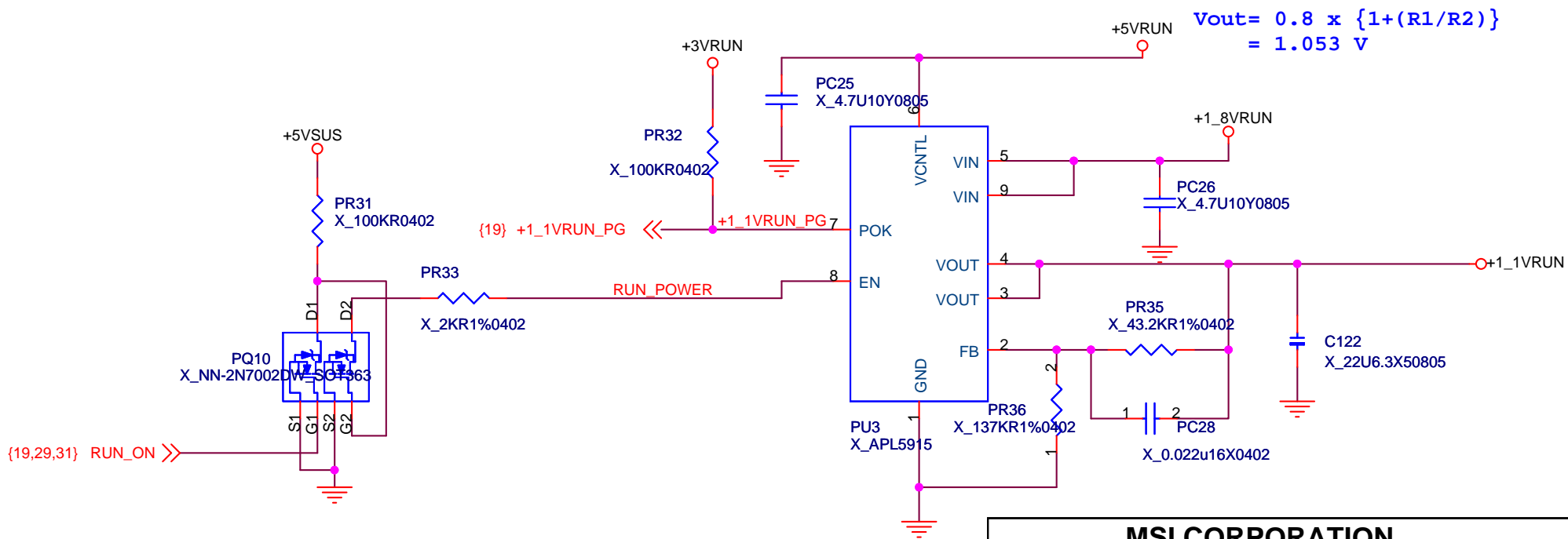


$$V_{out} = 0.75 * \{1 + (R1/R2)\} = 1.056 V$$

Current limit at 15A for 1.05V
Imax at 4A



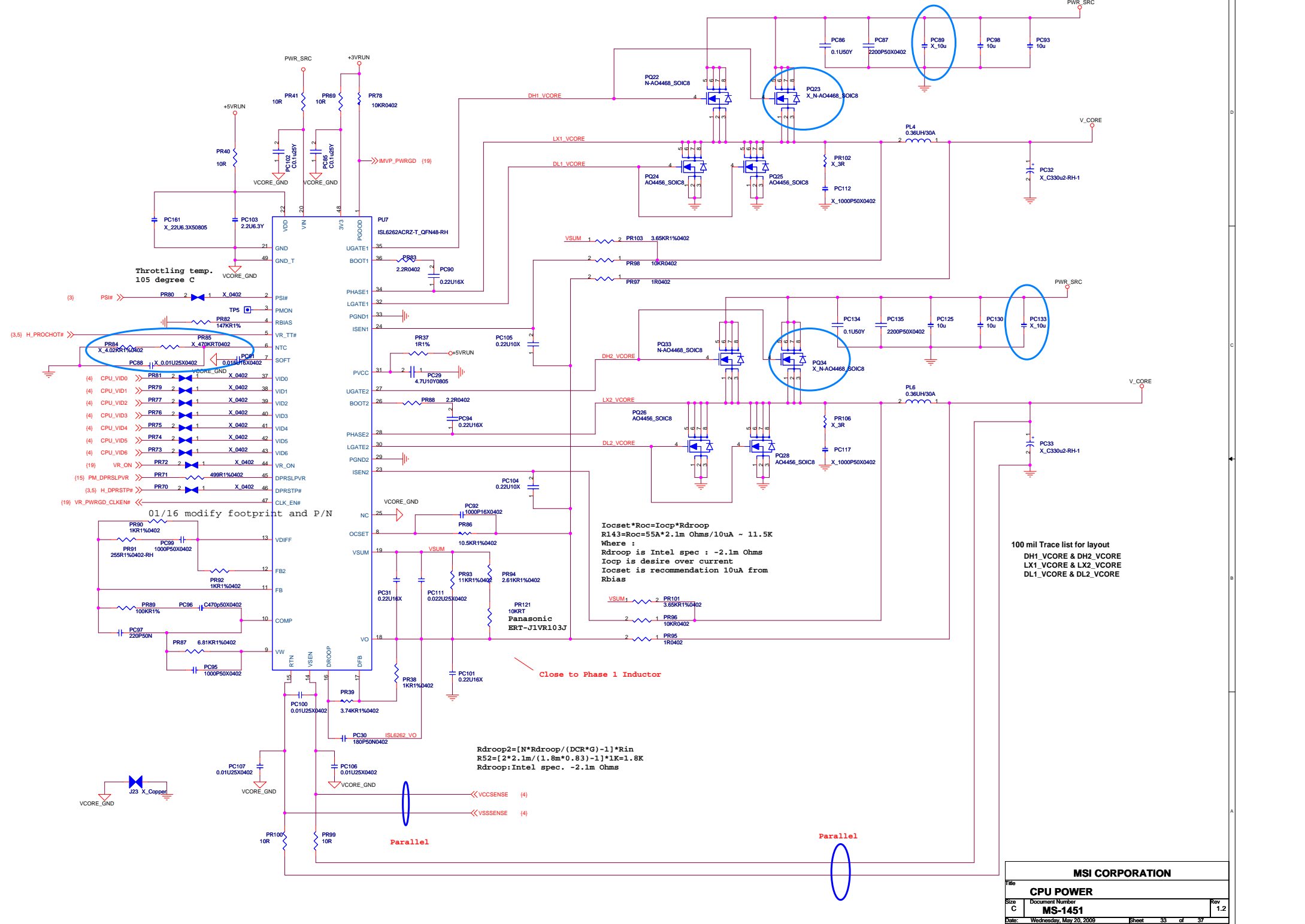
$$V_{out} = 1.25 \times \{1 + (30/150)\} = 1.5 \text{ V}$$



$$V_{out} = 0.8 \times \{1 + (R1/R2)\} = 1.053 \text{ V}$$

MSI CORPORATION

Title		
+1_5VRUN , +1_1VRUN		
Size A	Document Number MS-1451	Rev 1.2
Date:	Wednesday, May 20, 2009	Sheet 32 of 37



Throttling temp.
105 degree C

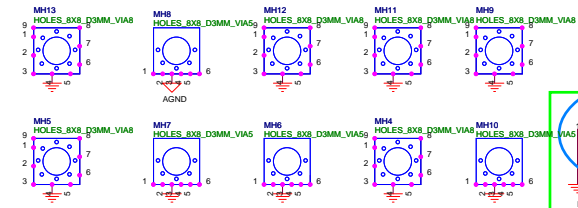
$I_{ocset} * R_{oc} = I_{ocp} * R_{droop}$
 $R_{143} = R_{oc} = 55A * 2.1m \text{ Ohms} / 10uA \sim 11.5K$
 Where :
 R_{droop} is Intel spec : -2.1m Ohms
 I_{ocp} is desire over current
 I_{ocset} is recommendation 10uA from Rbias

$R_{droop2} = [N * R_{droop} / (DCR * G) - 1] * R_{in}$
 $R_{52} = [2 * 2.1m / (1.8m * 0.83) - 1] * 1K = 1.8K$
 R_{droop} : Intel spec. -2.1m Ohms

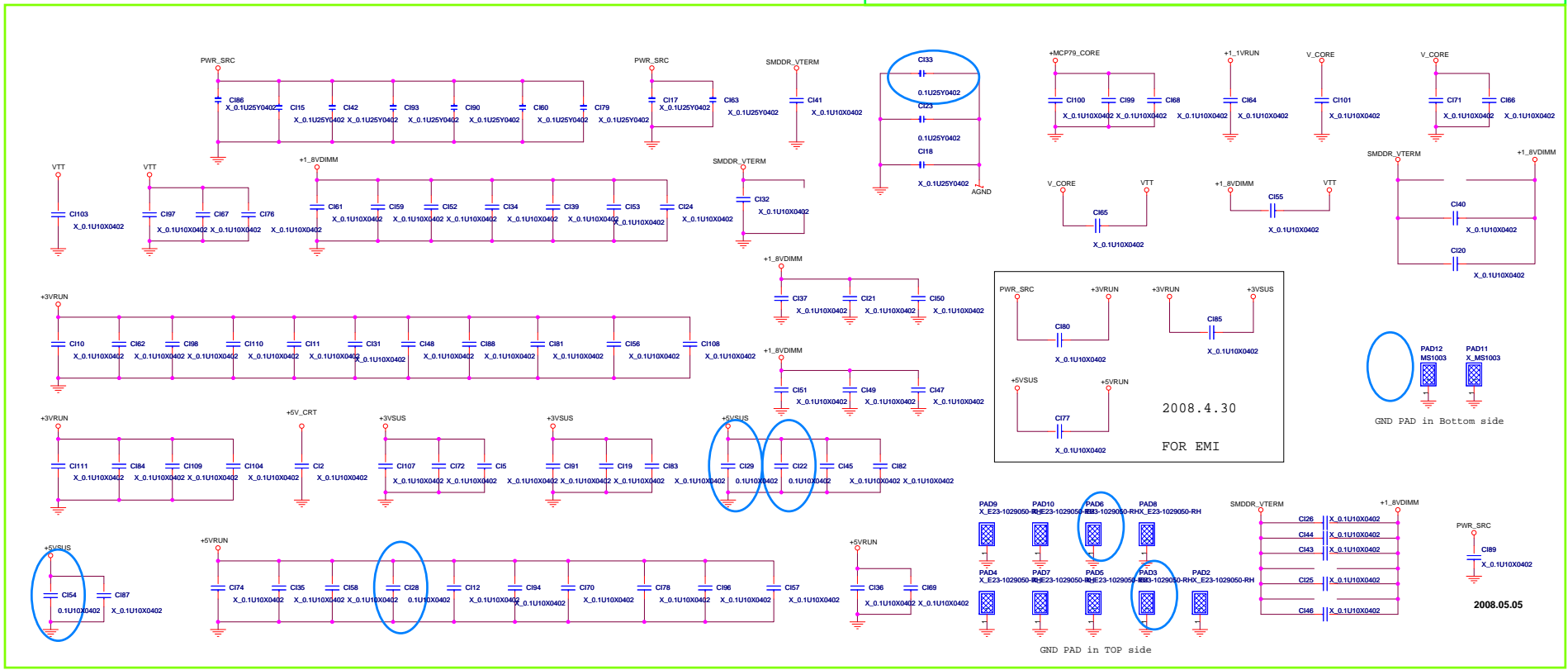
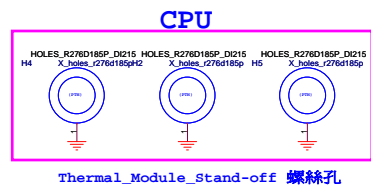
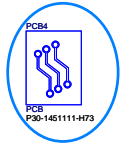
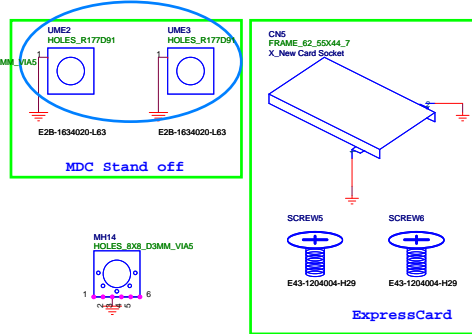
100 mil Trace list for layout
 DH1_VCORE & DH2_VCORE
 LX1_VCORE & LX2_VCORE
 DL1_VCORE & DL2_VCORE

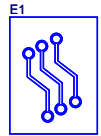
MSI CORPORATION		
CPU POWER		
Size	Document Number	Rev
C	MS-1451	1.2
Date:	Wednesday, May 20, 2009	Sheet 33 of 37

C-case & D-case

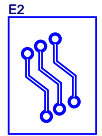


12/1 EMI

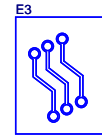




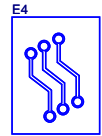
E1
X_NEW CARD MYLAR
E2P-4521411-G40



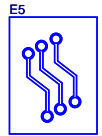
E2
HDD MYLAR
E2P-4521311-G40



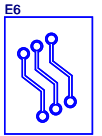
E3
Touchpad Rubber
E2Y-4520311-Y40



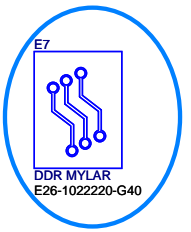
E4
Touchpad Rubber
E2Y-4520311-Y40



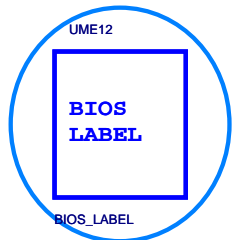
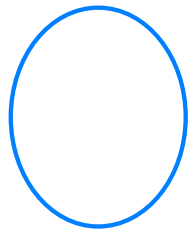
E5
Touchpad Rubber
E2Y-4520311-Y40



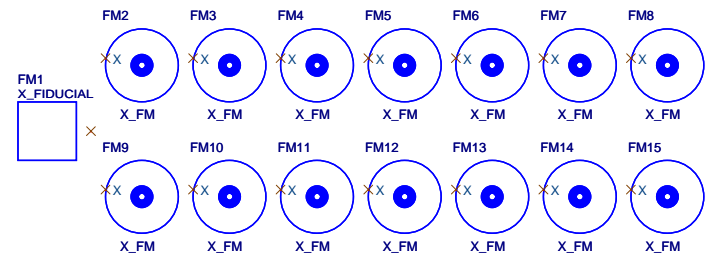
E6
Touchpad Rubber
E2Y-4520311-Y40



E7
DDR MYLAR
E26-1022220-G40

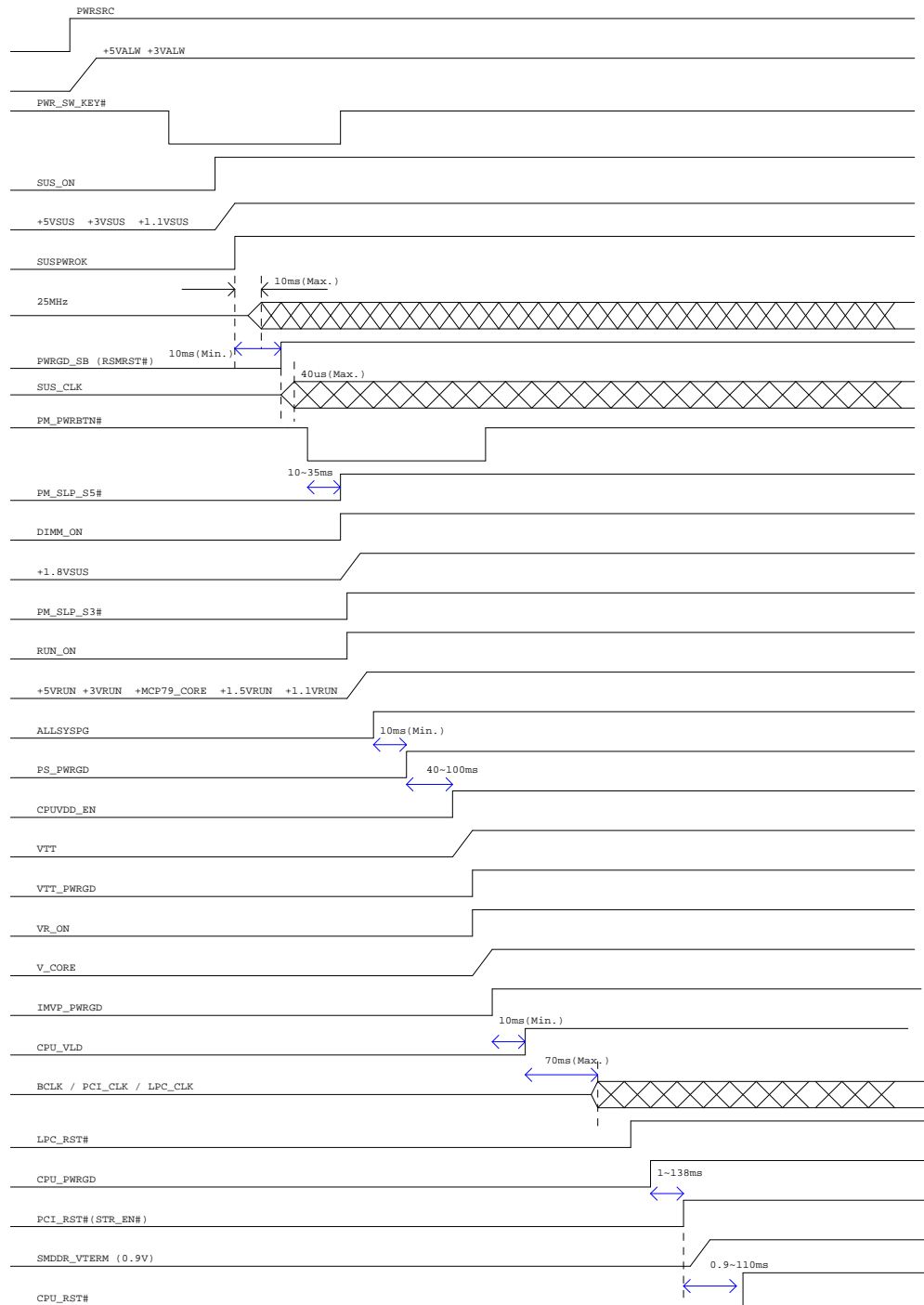


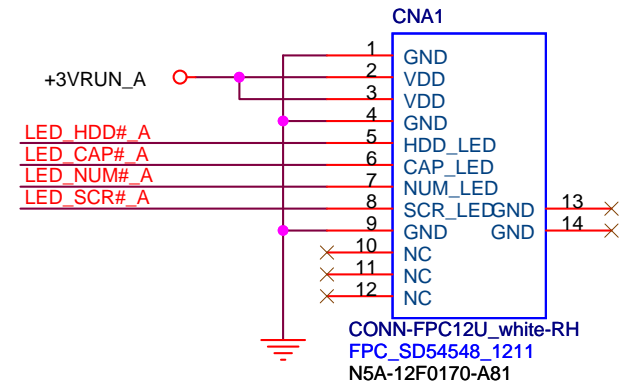
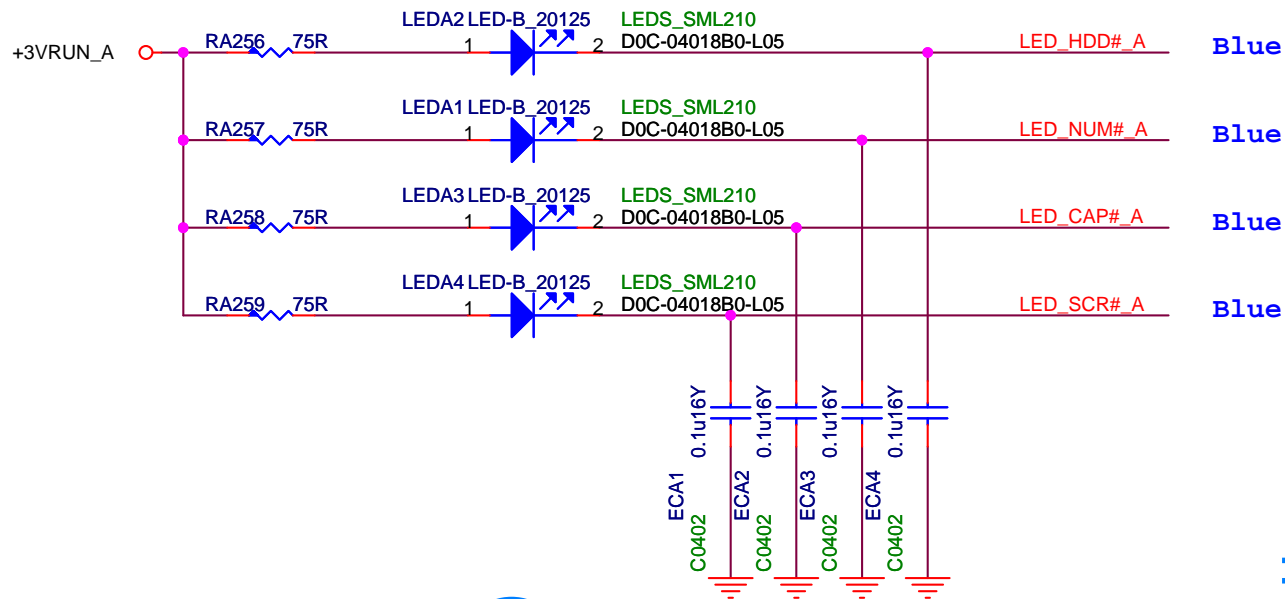
UME12
BIOS
LABEL
BIOS_LABEL



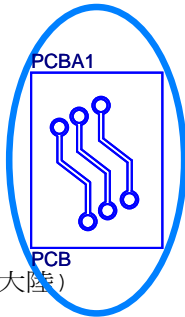
		MICRO-STAR INT'L CO.,LTD.	
Title		Non-Footprint for BOM	
Size	Document Number	Rev	
B	MS-1451	1.2	
Date:	Wednesday, May 20, 2009	Sheet	35 of 37

G0 to S0 Power-Up Timing

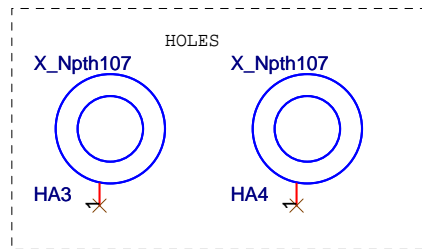
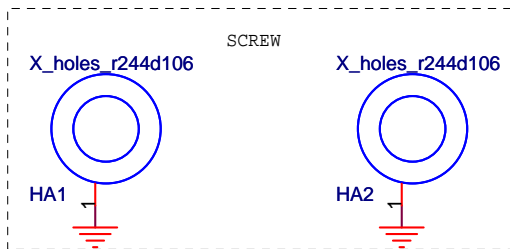
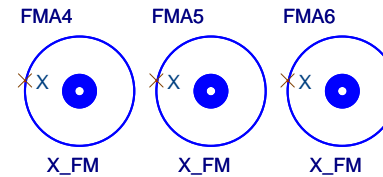
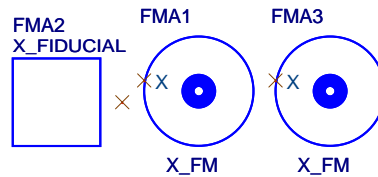





for CHANNEL



P30-1451A11-H73, 瀚宇博德
P30-1451A11-D05, 昆穎 (定穎大陸)



 MICRO-STAR INT'L CO.,LTD.	
Title	
LED BOARD	
Size	Document Number
A	MS-1451A
Date:	Rev
Wednesday, May 20, 2009	1.2
Sheet	37 of 37