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ATI RS690MC & SB600

MS-163B1

Version 0A

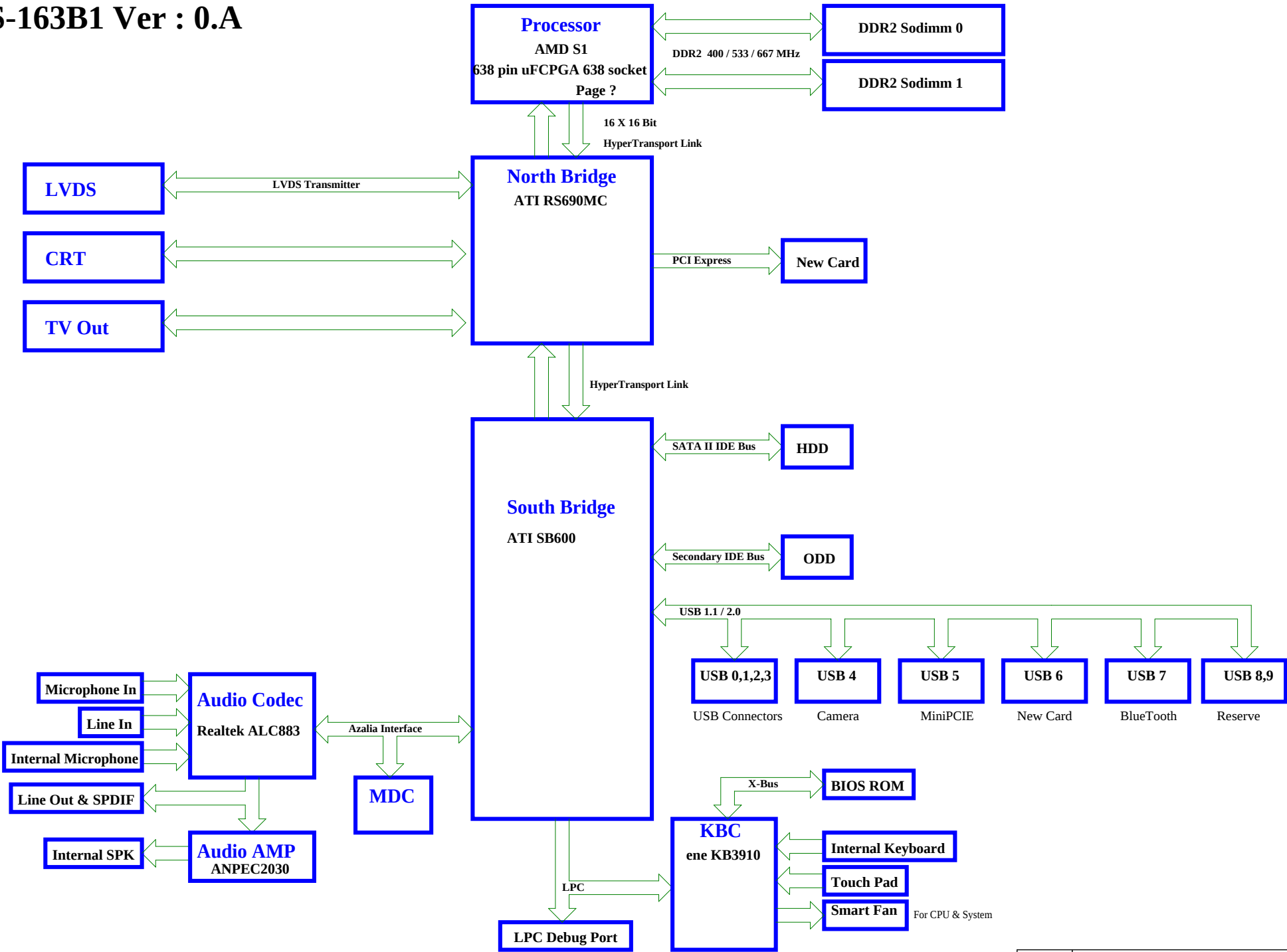
CPU:
AMD S1 638

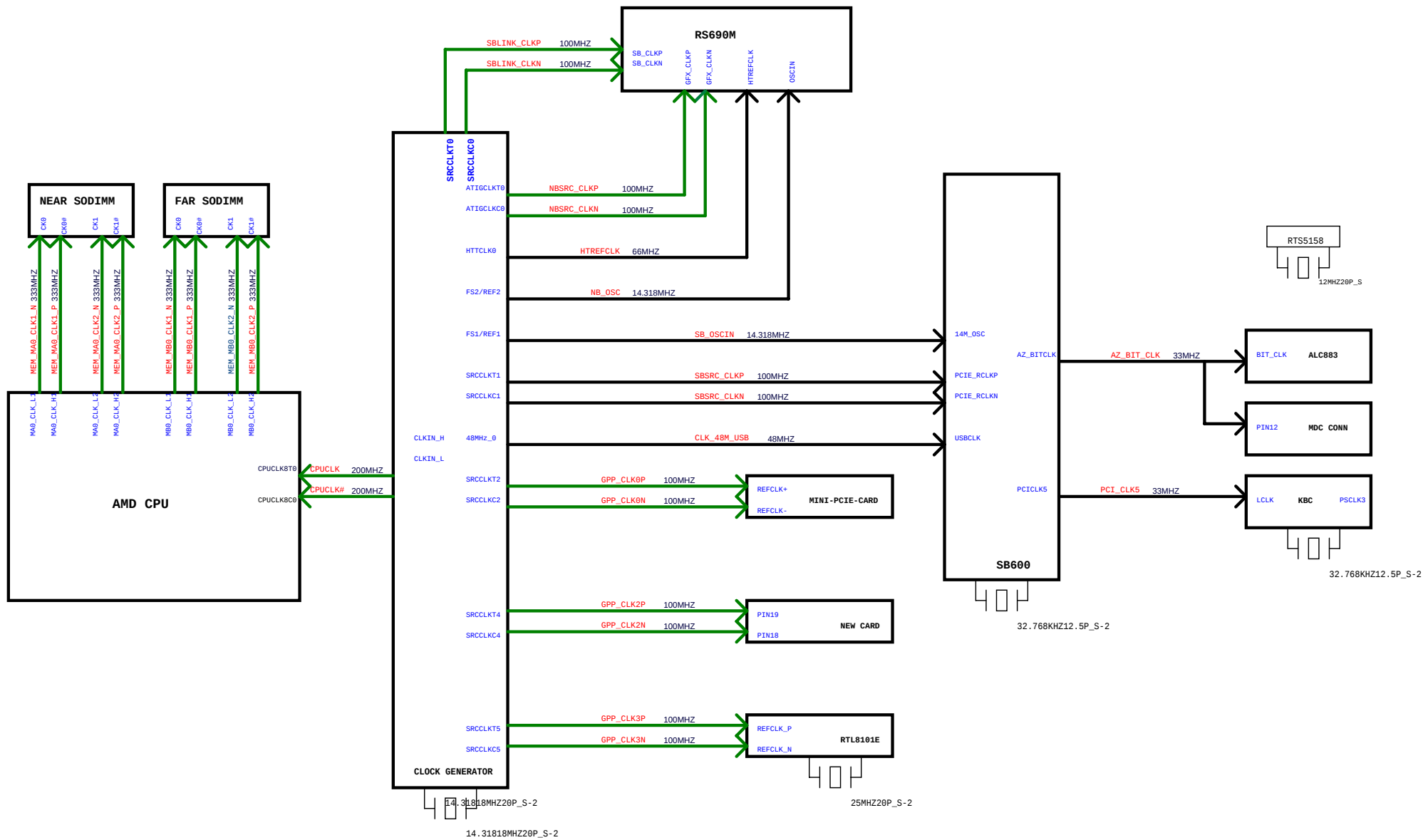
System Chipset:
ATI RS690MC - North Bridge
ATI SB600 - South Bridge

On Board Chipset:
BIOS -- ISA EEPROM SHARE WITH EC/uP CONTROLLER
AUDIO -- REALTAK ALC883 AZALIA Audio CODEC
AMPLIFIER -- ANPEC APA2030 or TI TPA0212
KBC/EC/uP -- ENE3910
LAN -- MII PHY REALTEK RTL8101E
CLOCK -- ICS951462
1394 & Card Reader Controller -- REALTEK

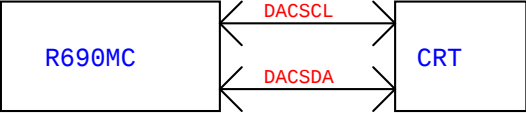
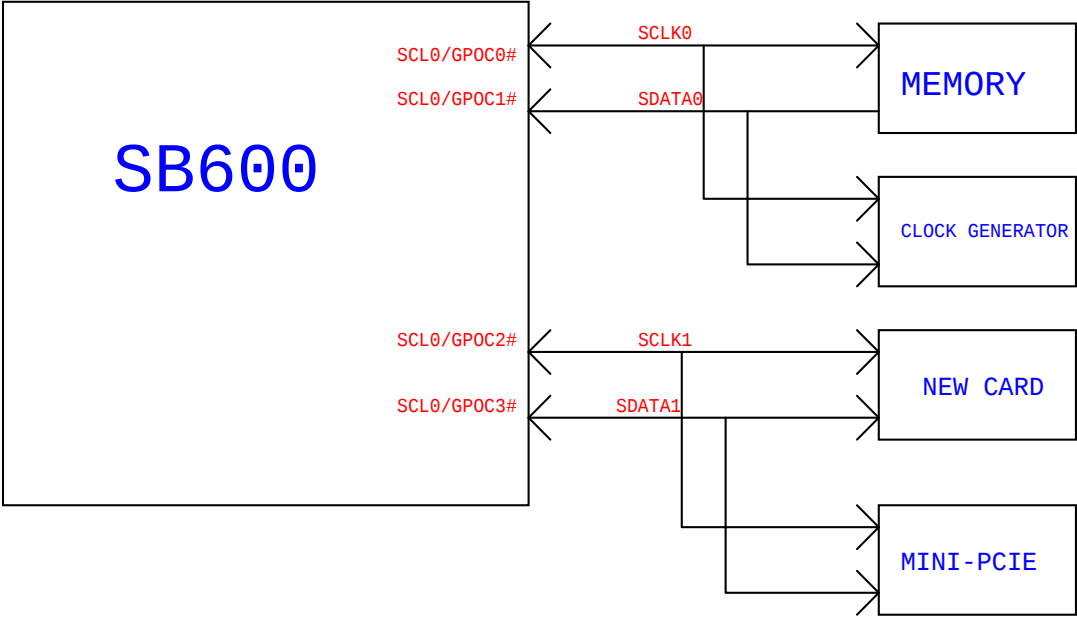
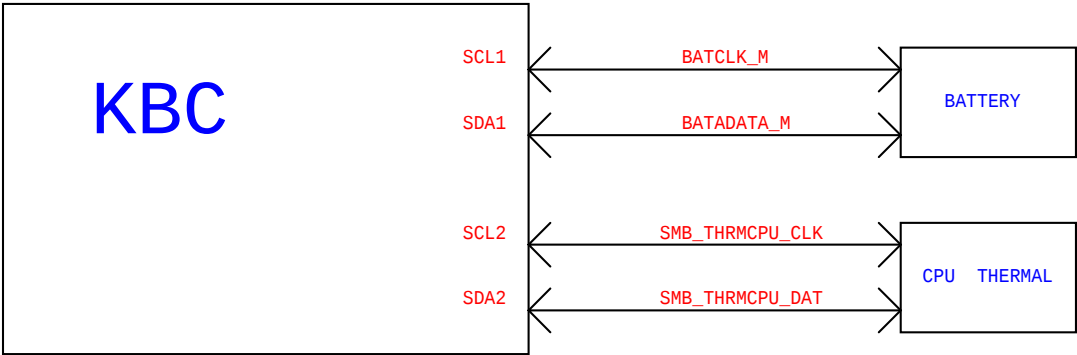
Main Memory:
DDR II * 2 (Max 2GB)

Expansion Slots & Connector :
New Card X1
Mini-PCIE X1



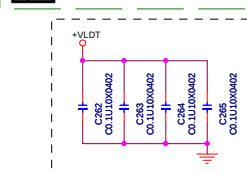


Title		
CLOCK DISTRIBUTION		
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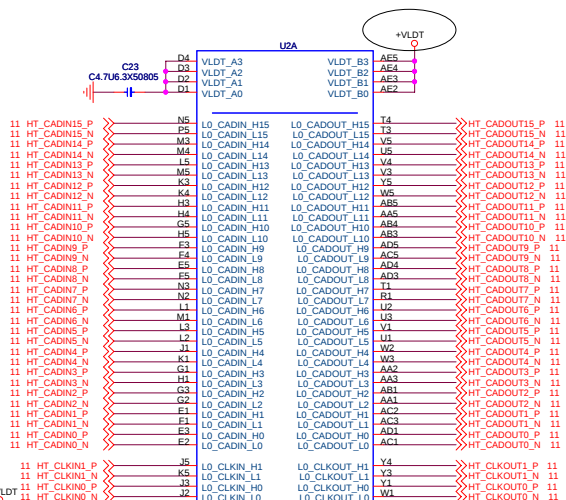


Title			
I2C ILLUSTRATE			
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 NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
PLACE CLOSE TO VLDT0 POWER PINS

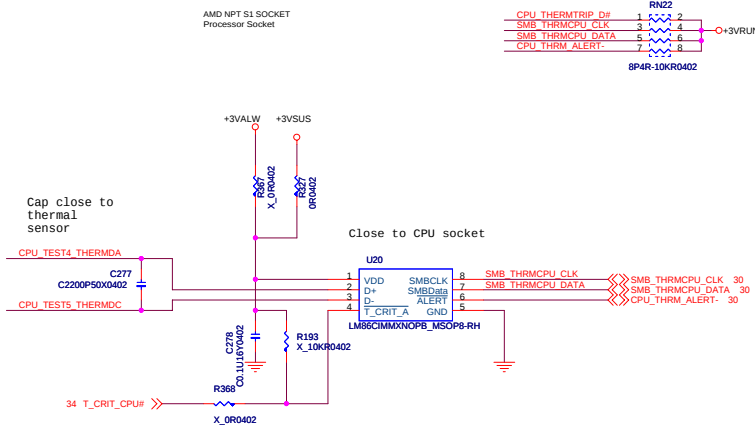
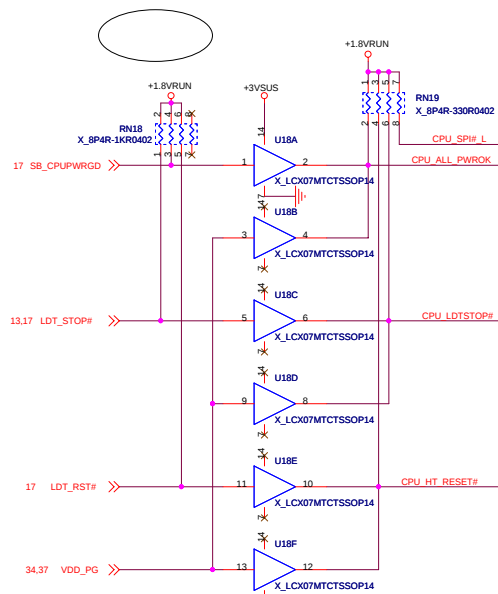
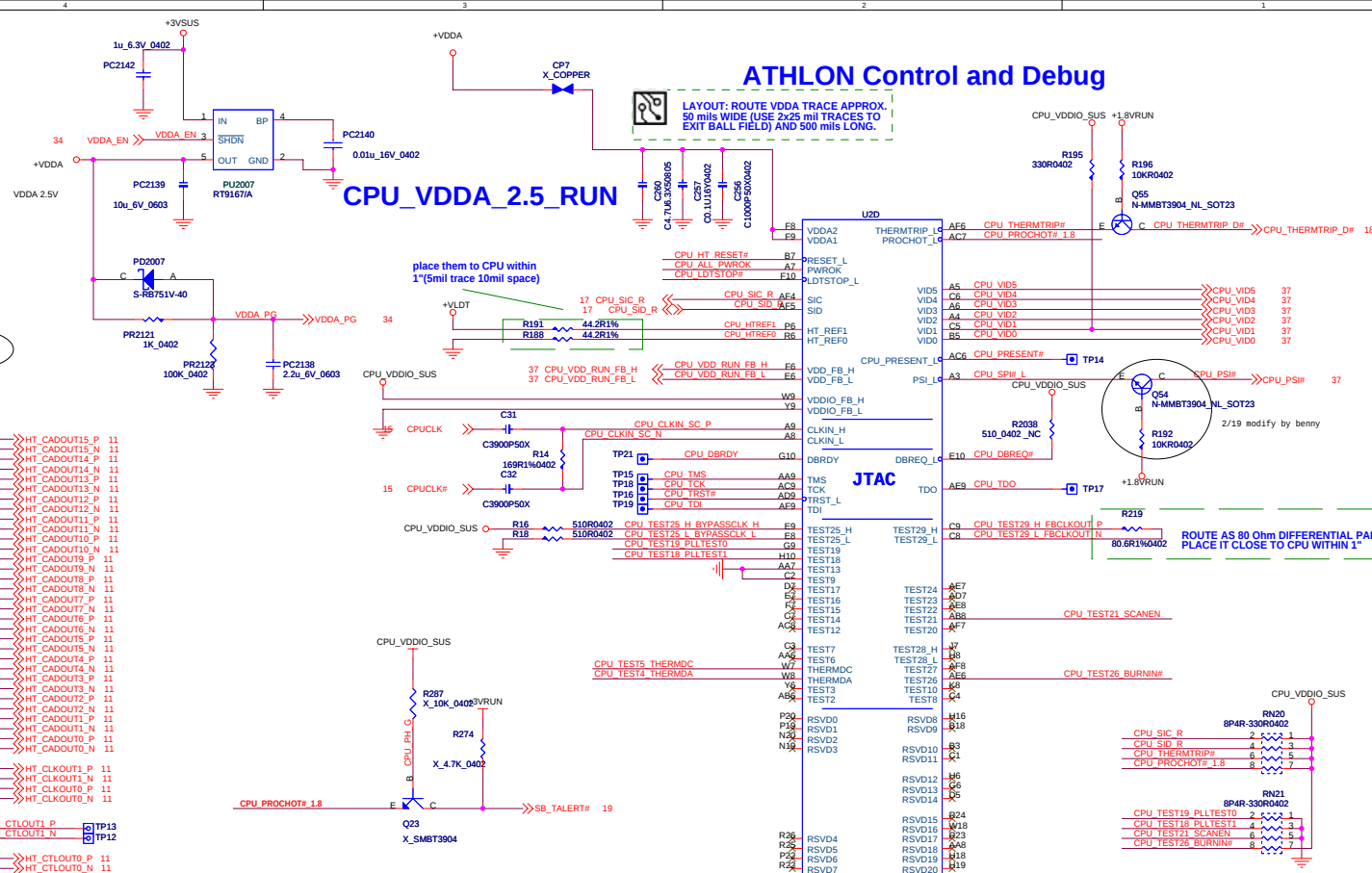
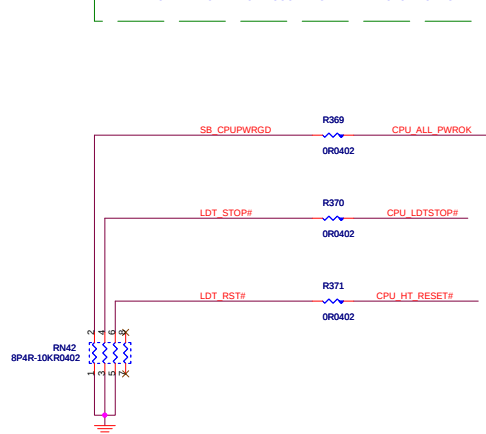


place them to CPU within
1"(5mil trace 10mil space)



Athlon 64 S1 Processor Socket

VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



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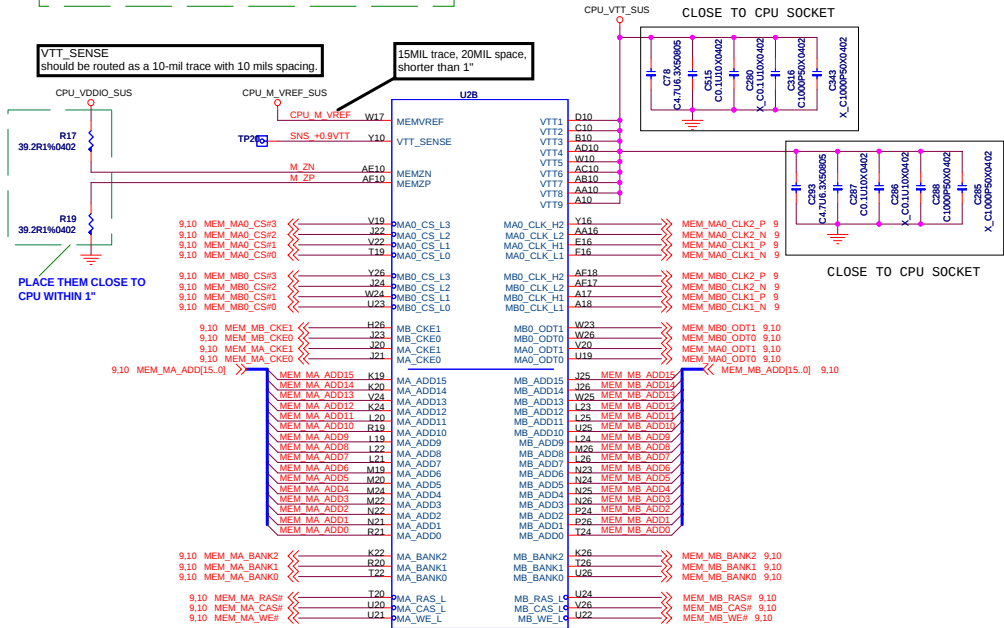
Size C	Document Description AMD S1 HT & CTRL I/F
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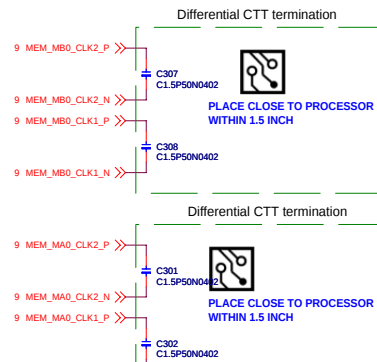
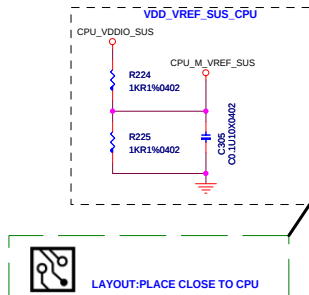
VDD_VTT_SUS_CPU IS CONNECTED TO THE VDD_VTT_SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

VTT_SENSE
should be routed as a 10-mil trace with 10 mils spacing

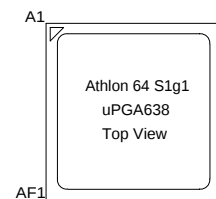
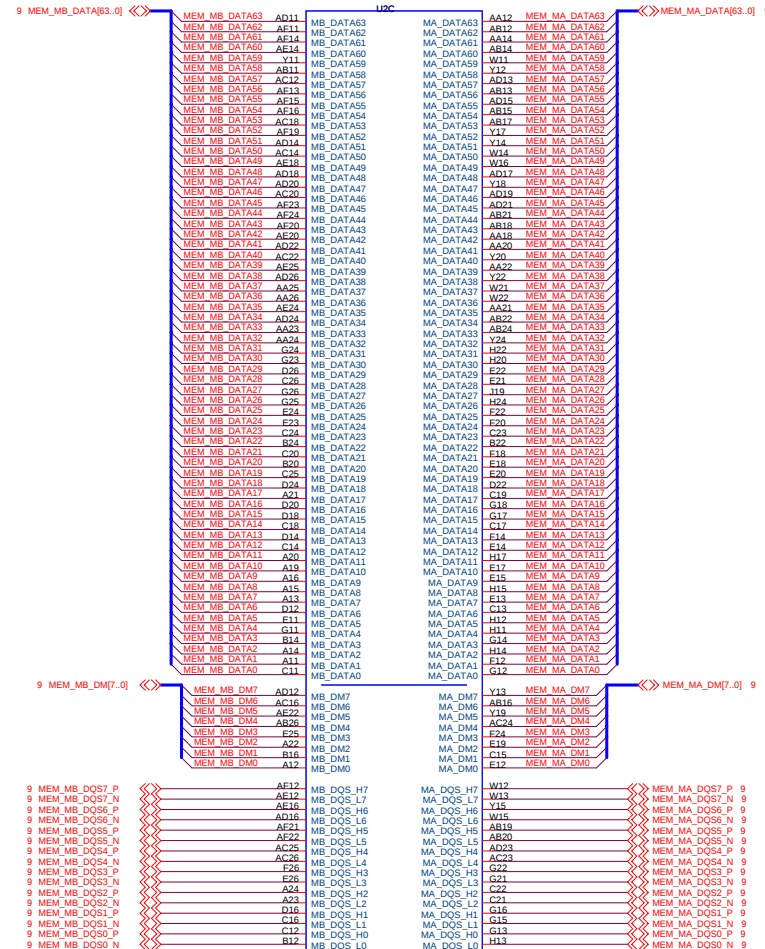
15MIL trace, 20MIL space,
shorter than 1"

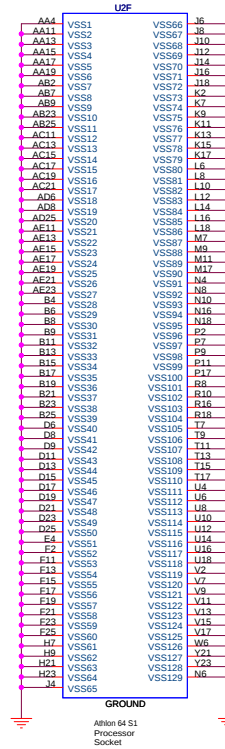
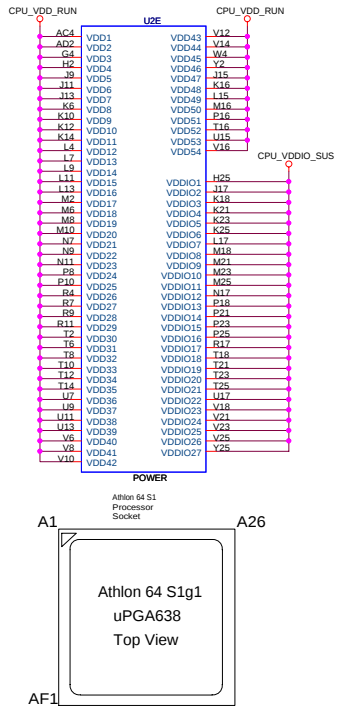


DDR II: CMD/CTRL/CLK
Athlon 64 S1
Processor
Socket

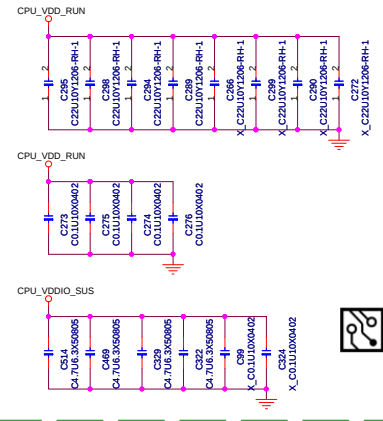


Processor DDR2 Memory Interface

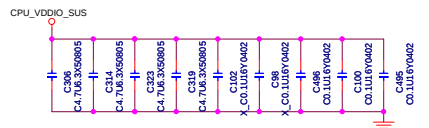




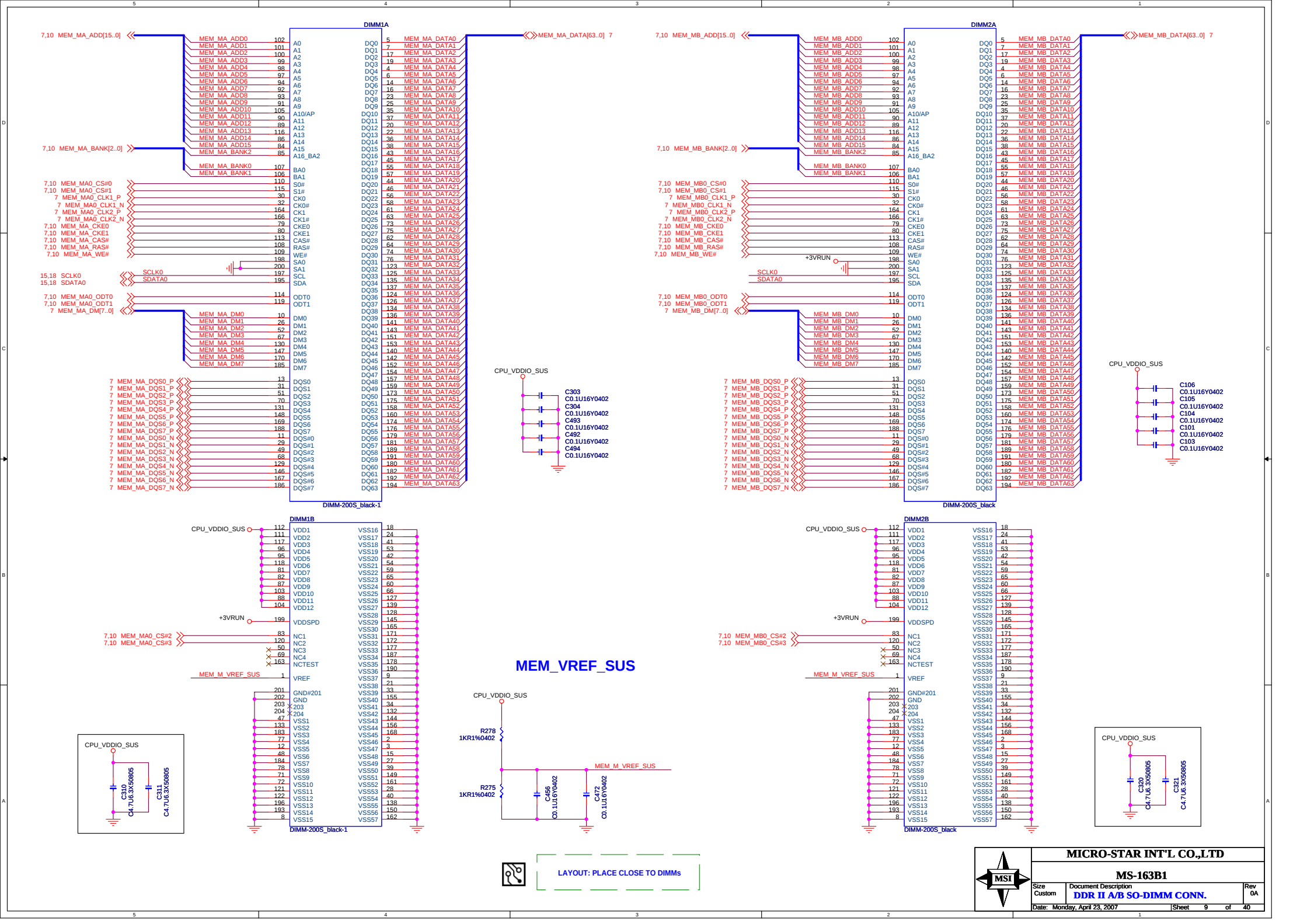
BOTTOMSIDE DECOUPLING

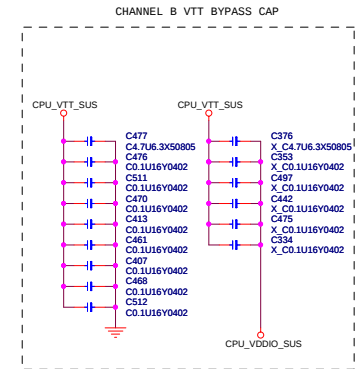
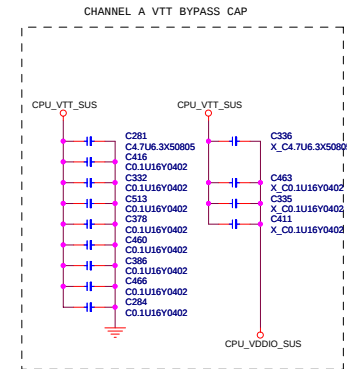
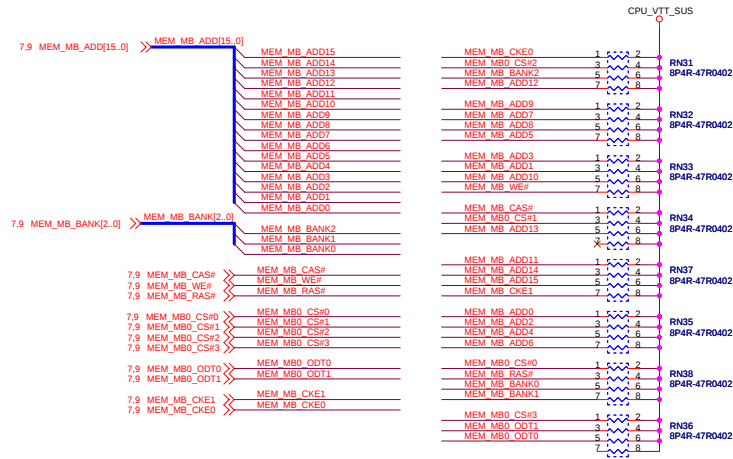
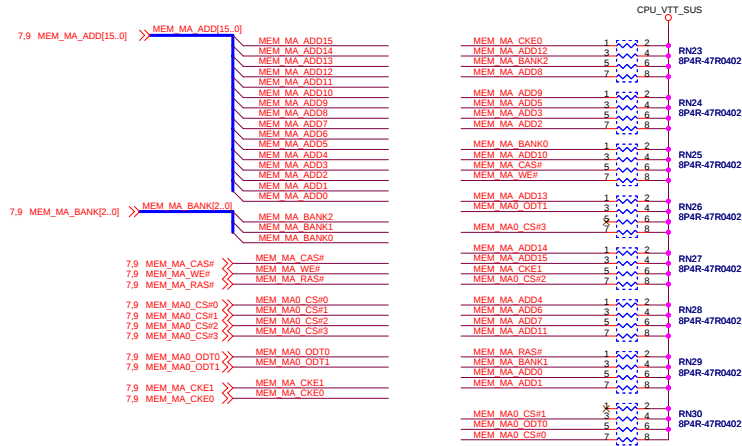


DECOUPLING BETWEEN PROCESSOR AND DIMMS PLACE CLOSE TO PROCESSOR AS POSSIBLE



PROCESSOR POWER AND GROUND





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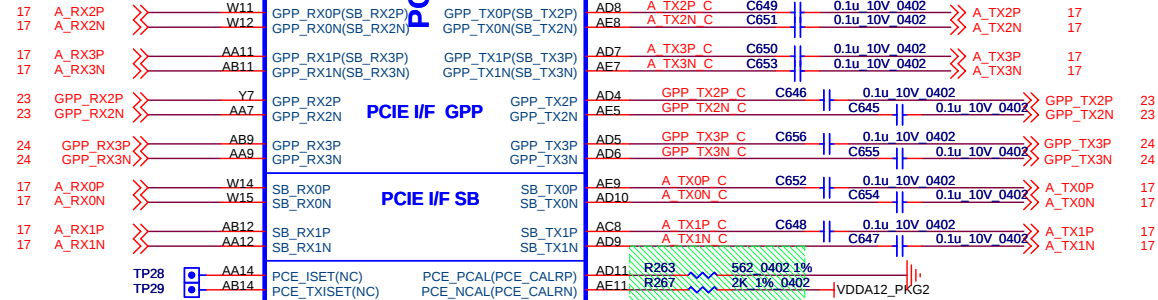
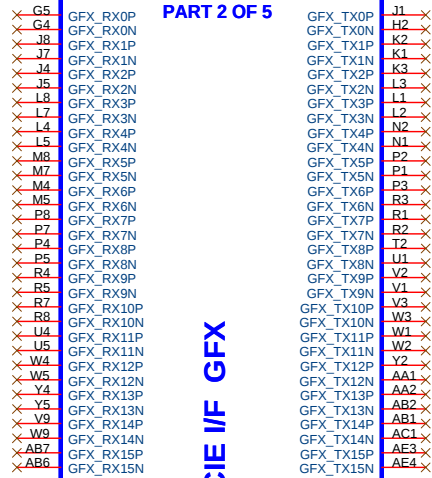
MS-163B1

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version A12

U2016B

PART 2 OF 5



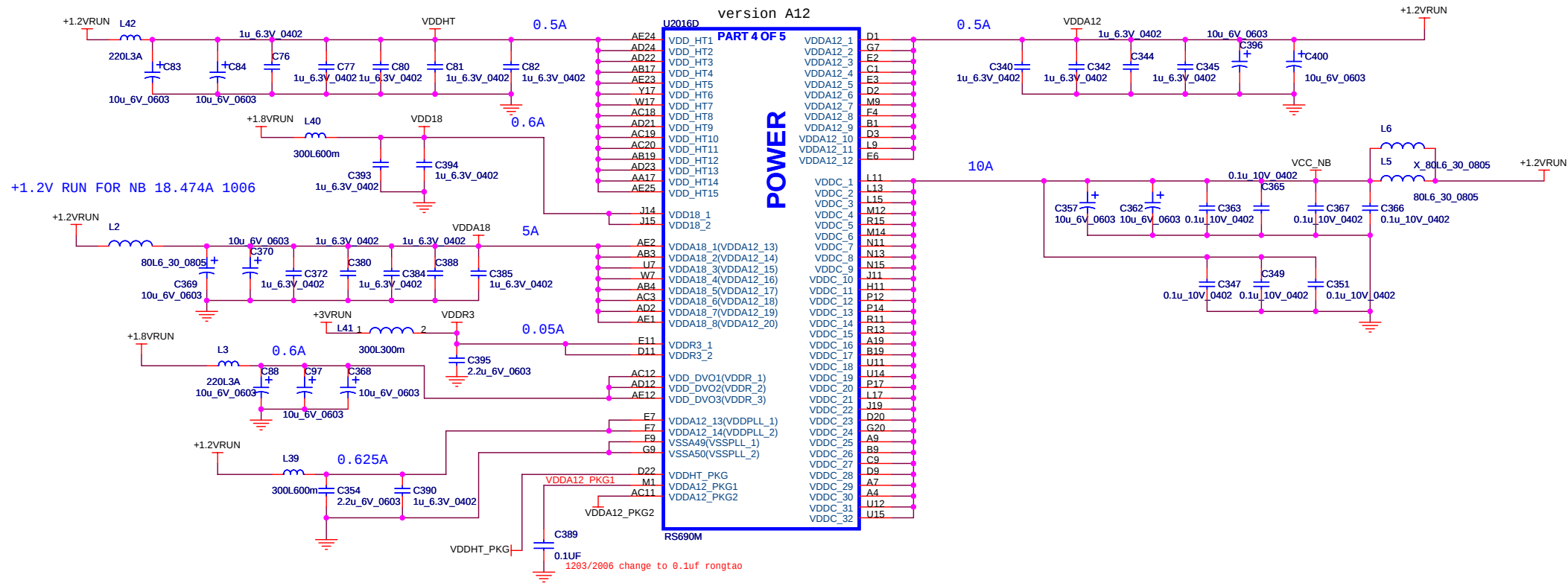
TO NEW CARD

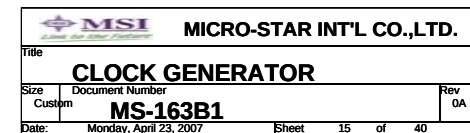
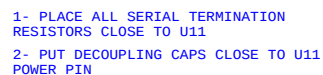
TO LAN

RS690M

R50 5620hm
R52 2K0hm

		MICRO-STAR INT'L CO.,LTD.	
Title			
RS690T PCI-E LINK&HDMI I/F			
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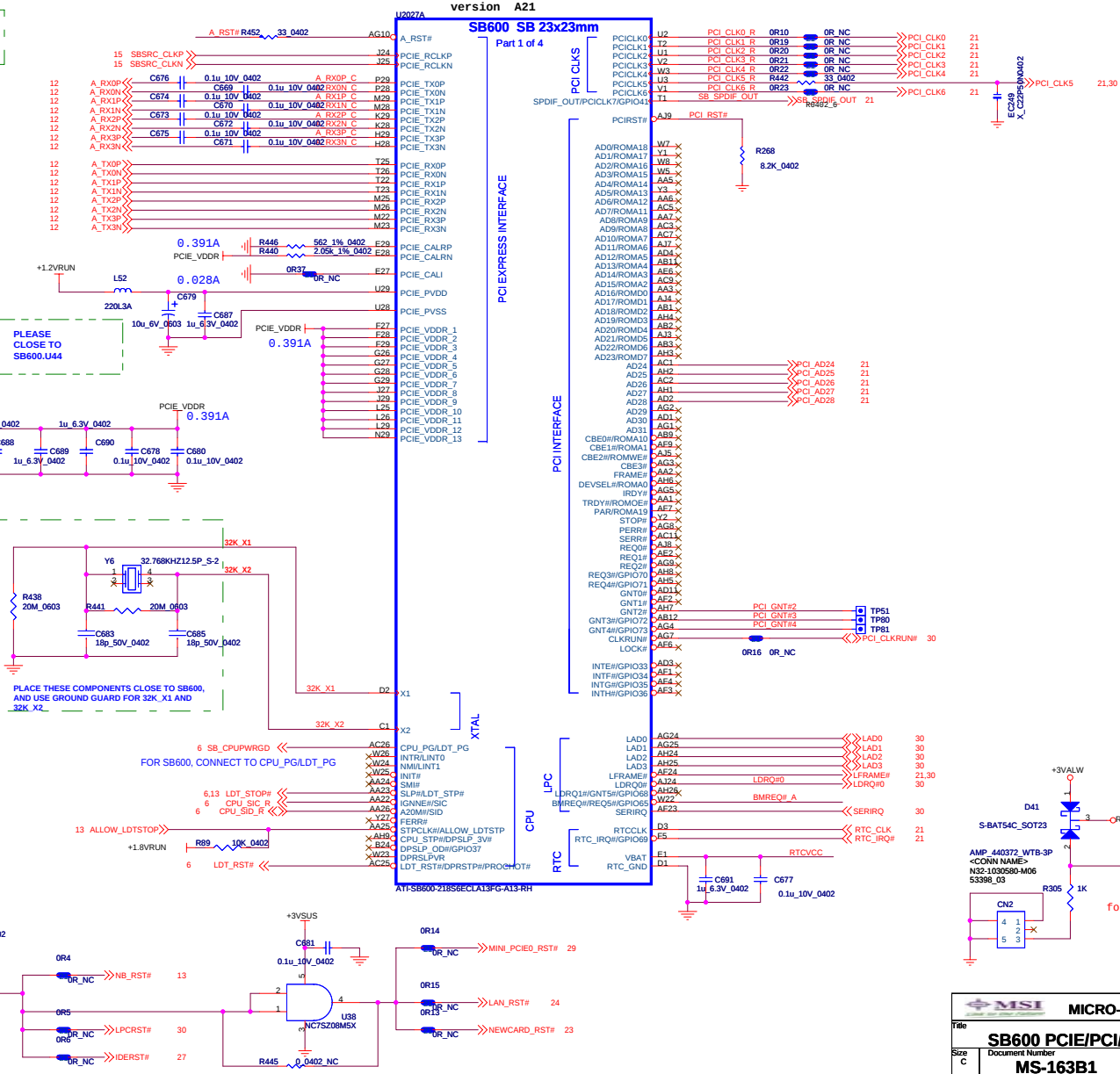


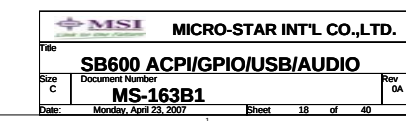
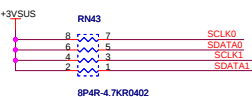
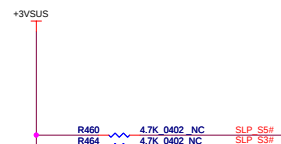


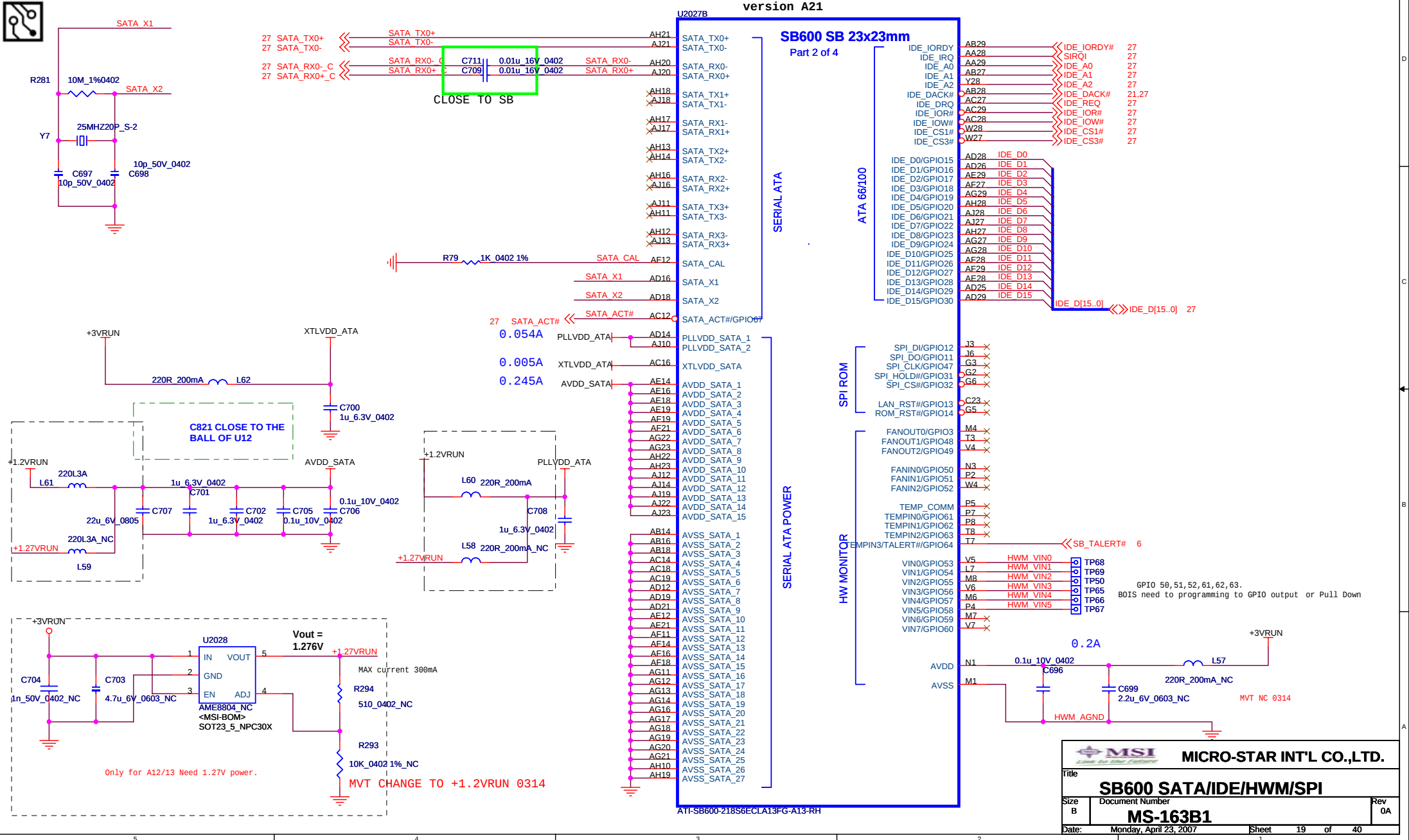


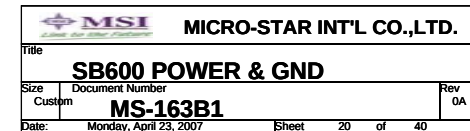
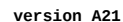
PLACE THESE PCIE AC COUPLING
CAPS CLOSE TO SB600

	SB600
C325 to C332	0.1uF
R165	562 Ohm 1%
R166	2.05K 1%
R167	0 Ohm
R179	10K





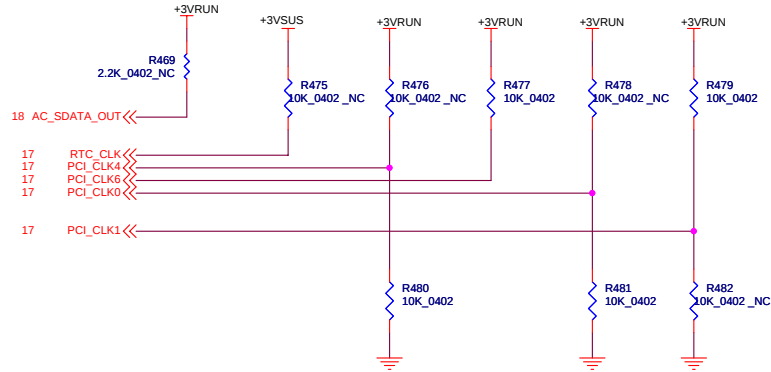




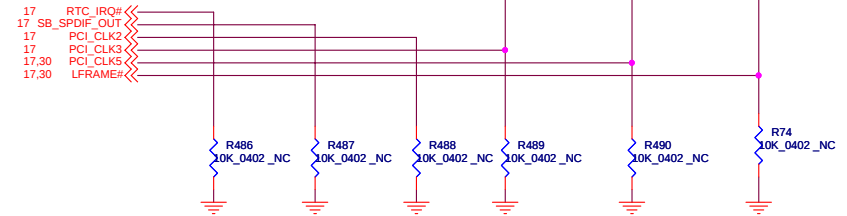


REQUIRED STRAPS

NPTE: FOR SB460, EXTERNAL PU/PD ARE REQUIRED



SPDIF_OUT Integrated 10K
PM2_Rg EAh. Default: PU/PD not enable
BIOS must confirm with AMI/ATI.

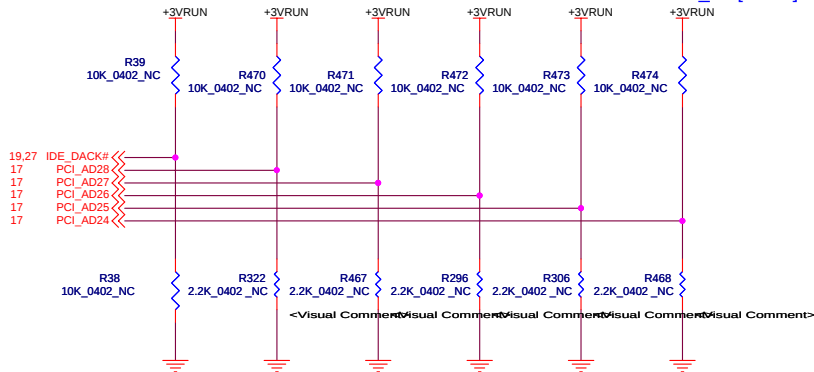


SB600						
PULL HIGH	AC_SDOUT	RTC_CLK	PCI_CLK4	PCI_CLK6	PCI_CLK0	PCI_CLK1
	USE DEBUG STRAPS DEFAULT	INTERNAL RTC DEFAULT	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM	DEFAULT
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ DEFAULT	CPU IF=P4		

	ACPWRON	SPDIF_OUT	PCI_CLK2	PCI_CLK3	PCI_CLK5	LFRAME#
PULL HIGH	MANUAL PWR ON DEFAULT	SIO 24MHz	XTAL MODE NOT SUPPORTED	USB PHY POWERDOWN DISABLE DEFAULT	PCIE_CM_SET LOW DEFAULT	ENABLE THERMTRIP# DEFAULT
PULL LOW	AUTO PWR ON	SIO 48MHz DEFAULT	48MHZ OSC MODE DEFAULT	USB PHY POWERDOWN ENABLE	PCIE_CM_SET HIGH	DISABLE THERMTRIP#

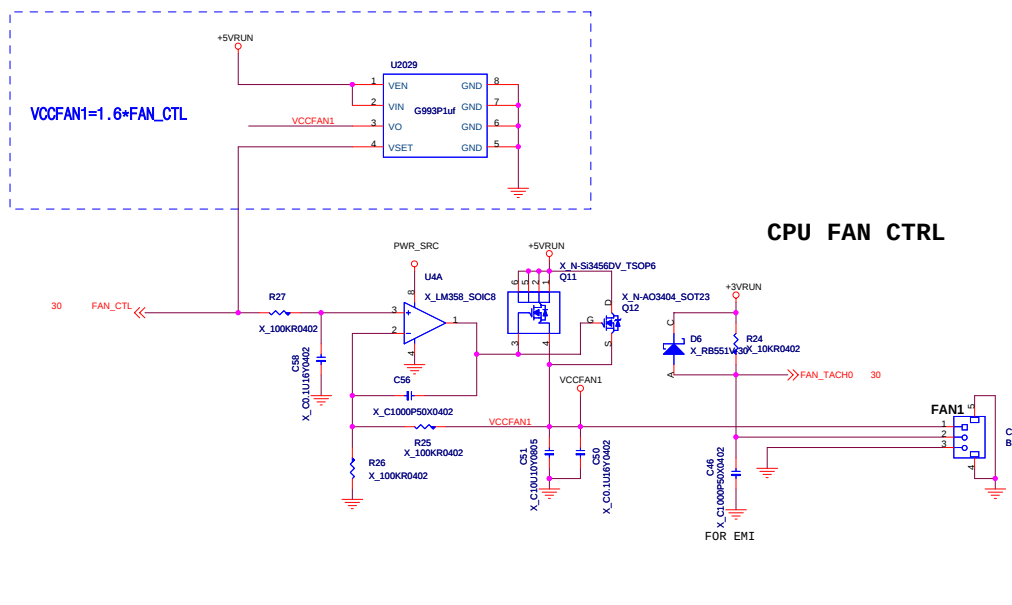
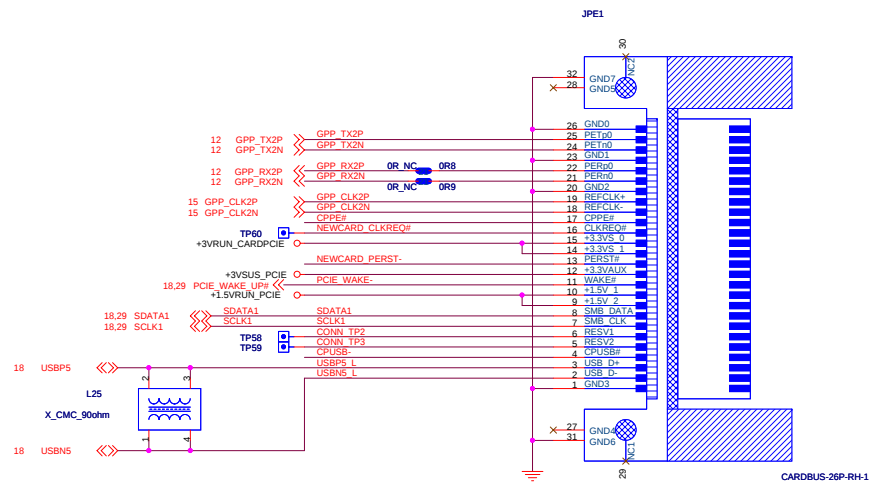
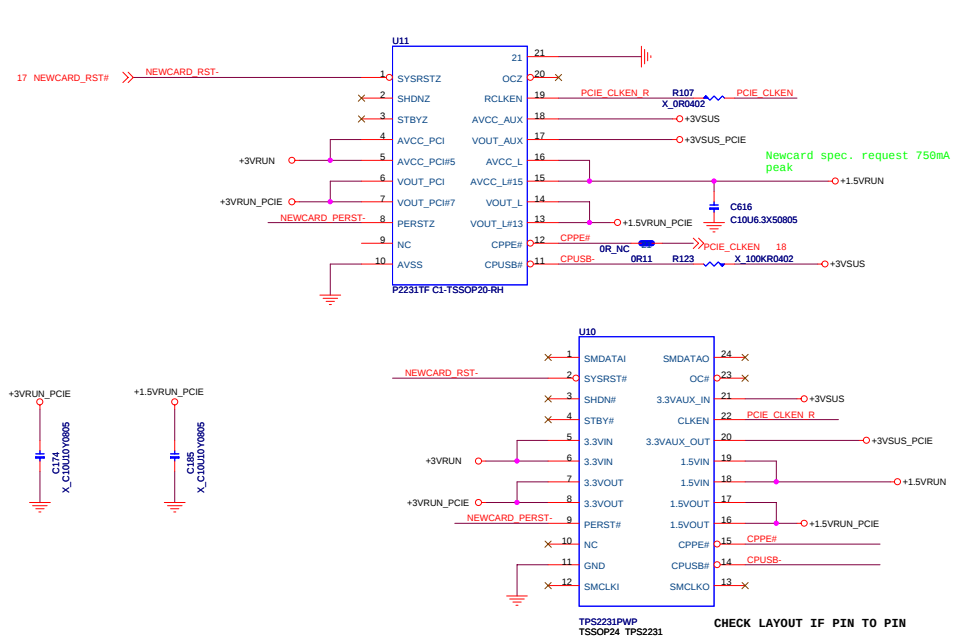
DEBUG STRAPS

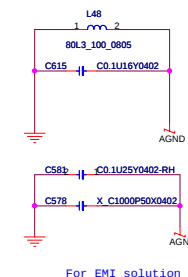
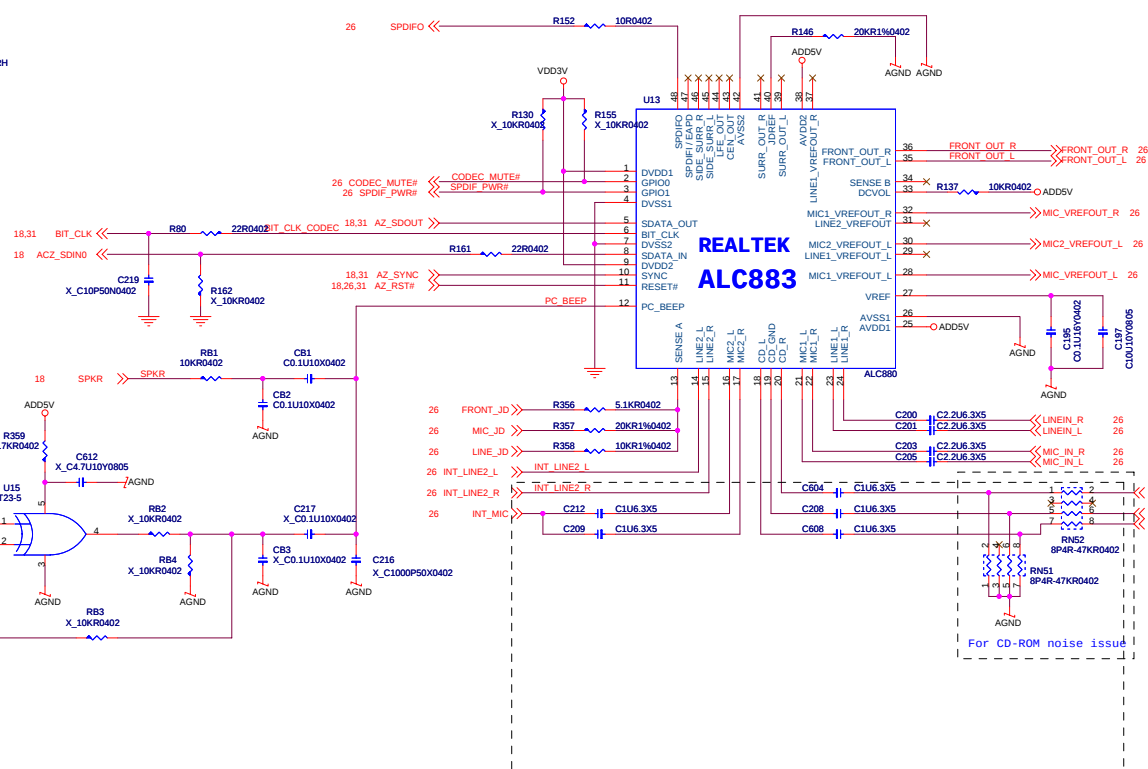
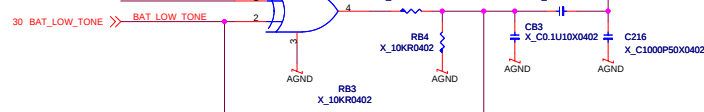
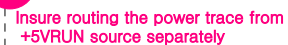
SB600 HAS 15K INTERNAL PU FOR PCI_AD[31:23]

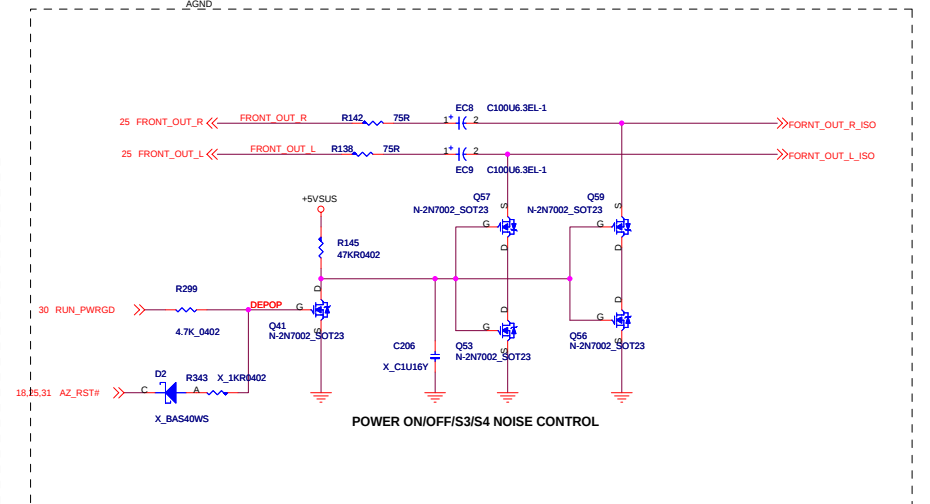
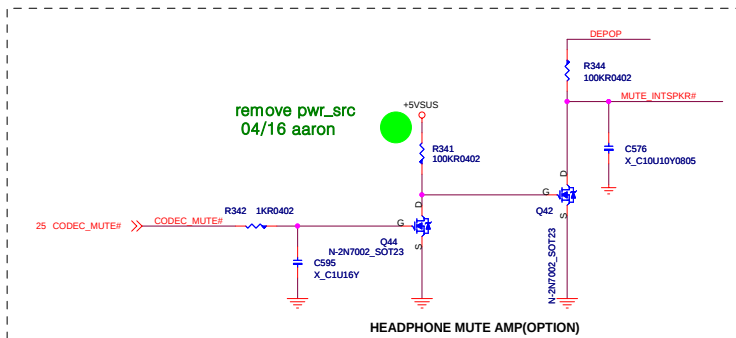
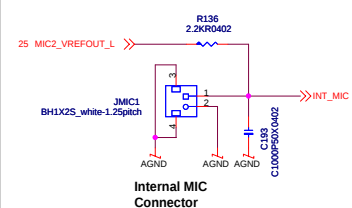
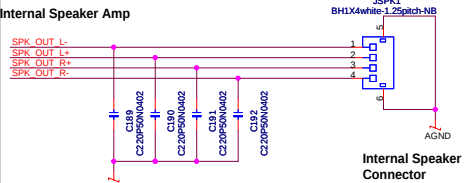
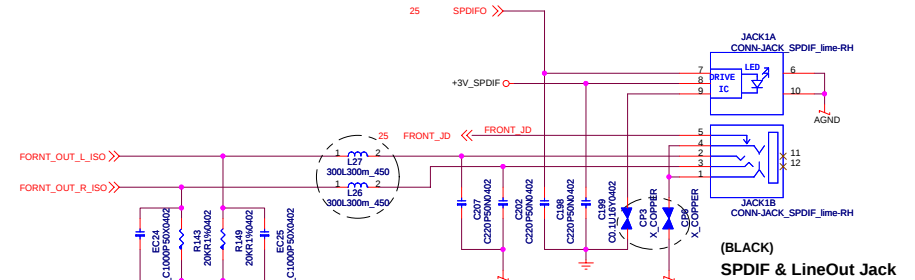
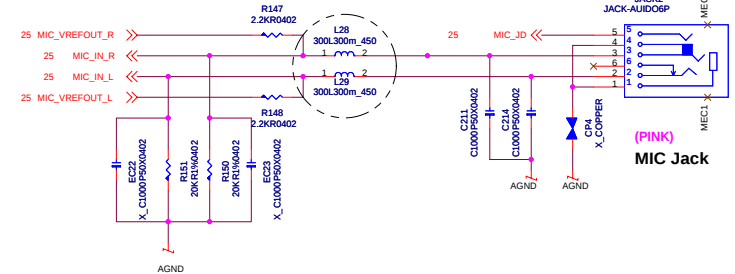
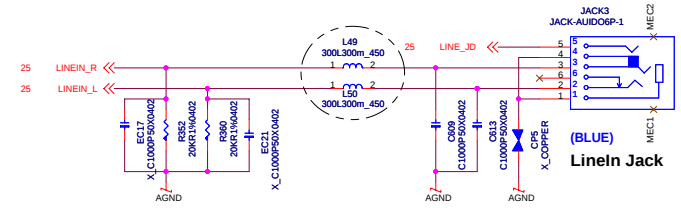
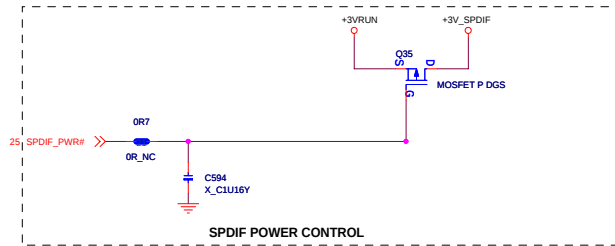
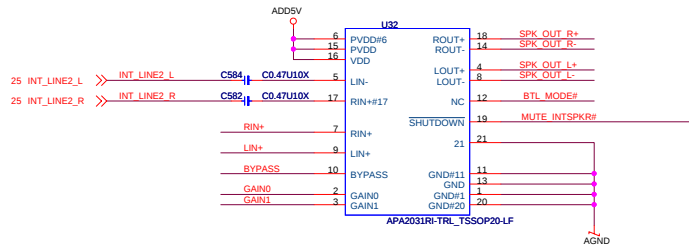
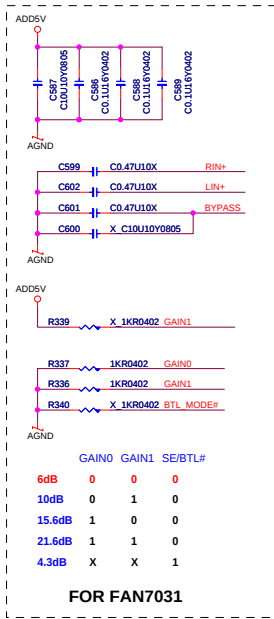


	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS

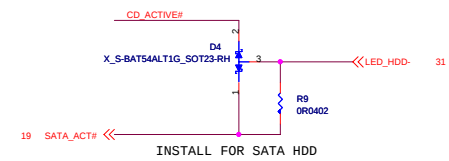
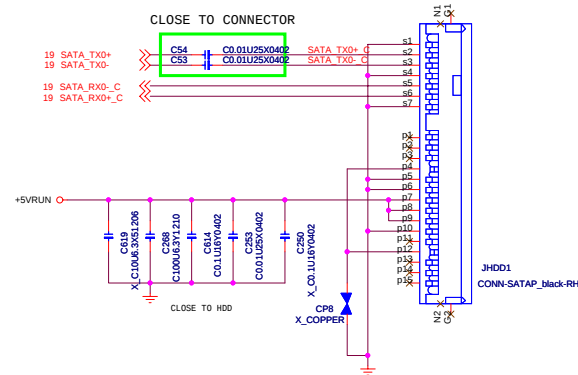
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



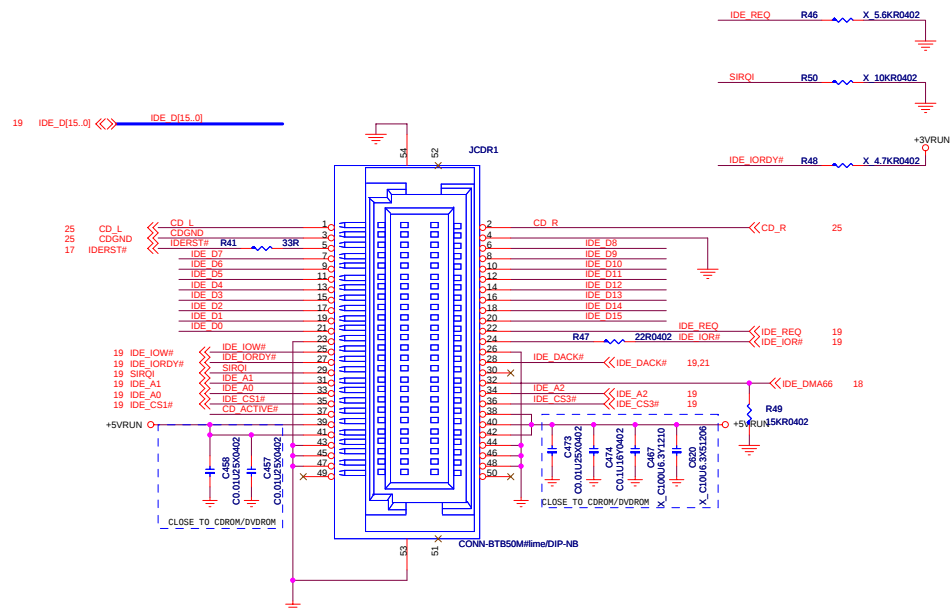




SATA HDD CONNECTOR



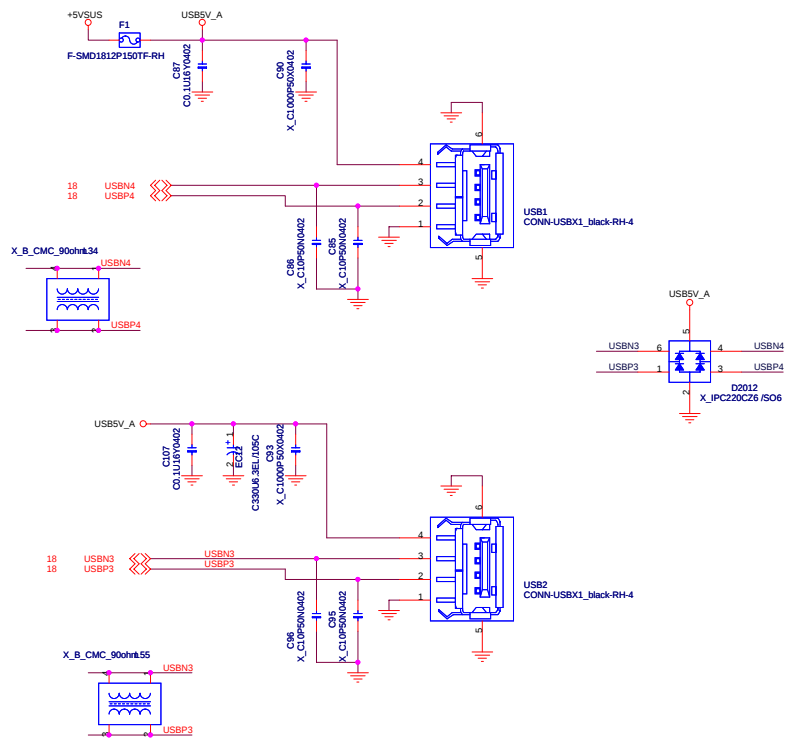
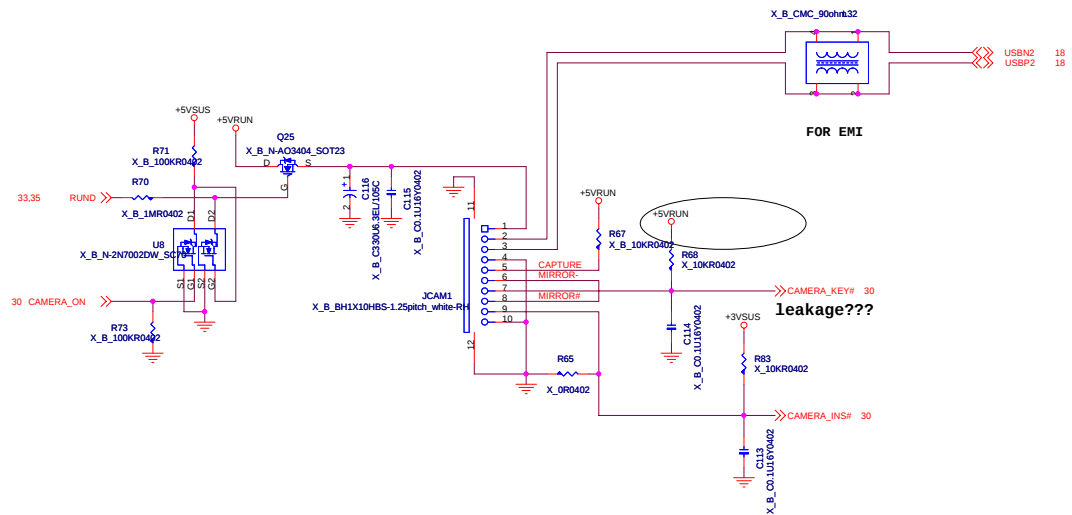
CD ROM CONNECTOR

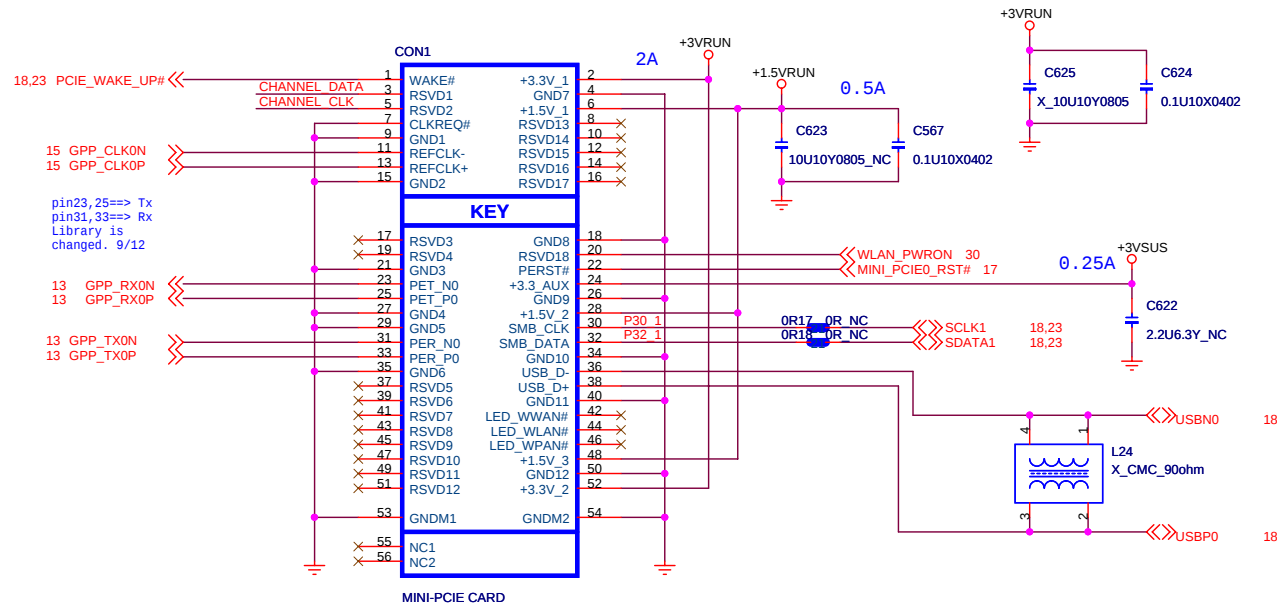


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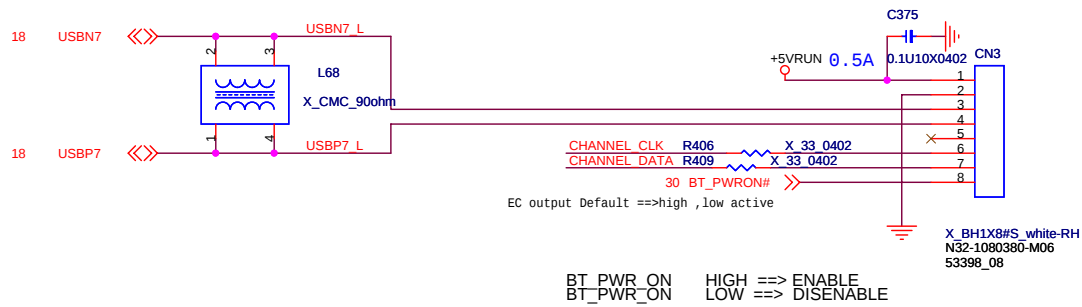
Size C	Document Description SATA & CDROM Connector	Rev 0A
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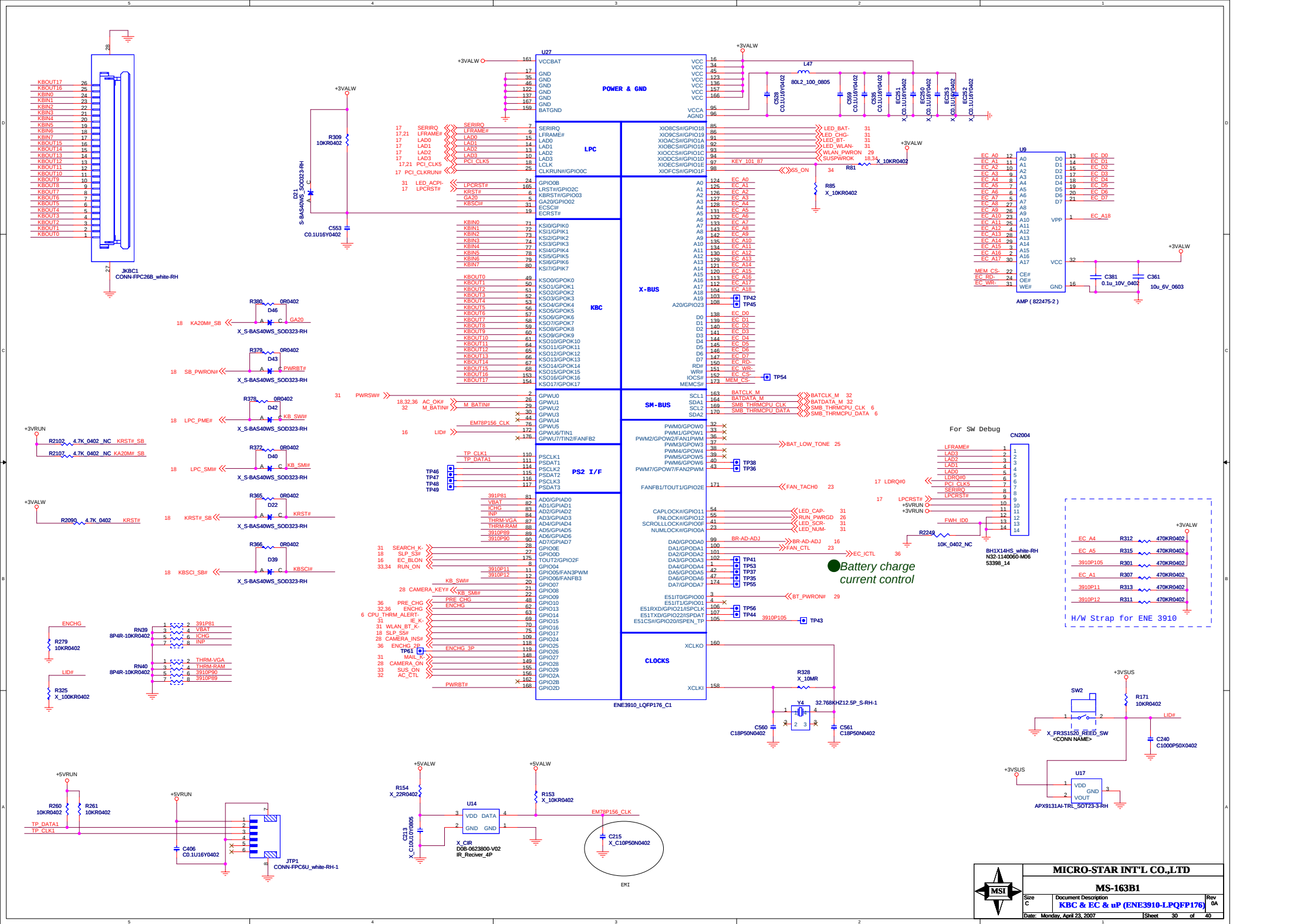


Wireless LAN

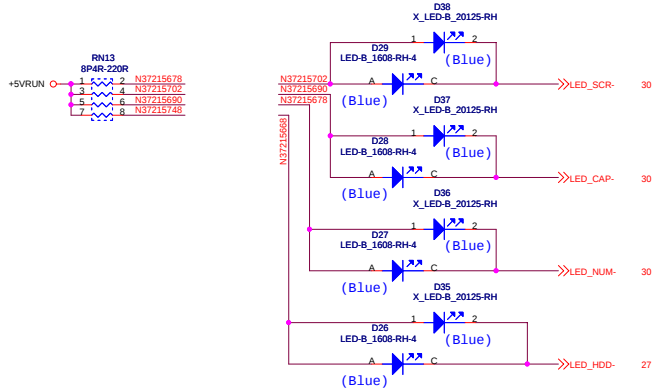
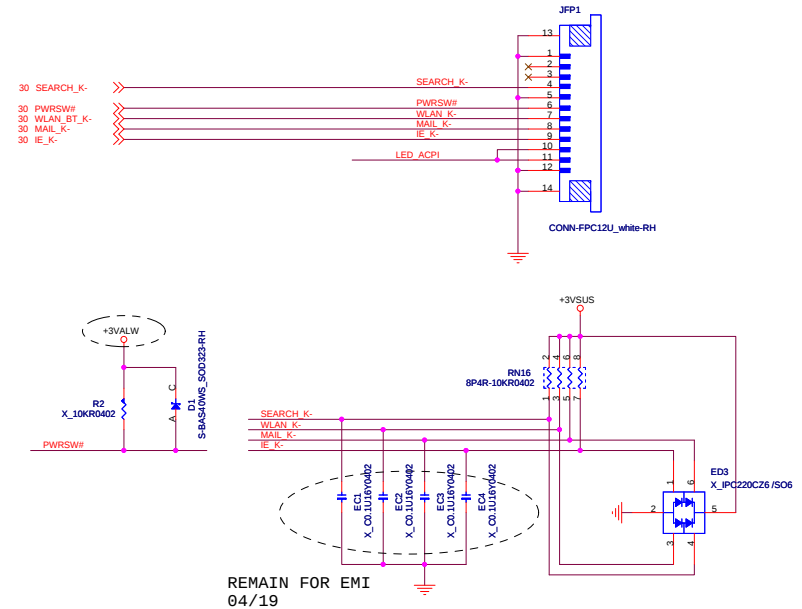
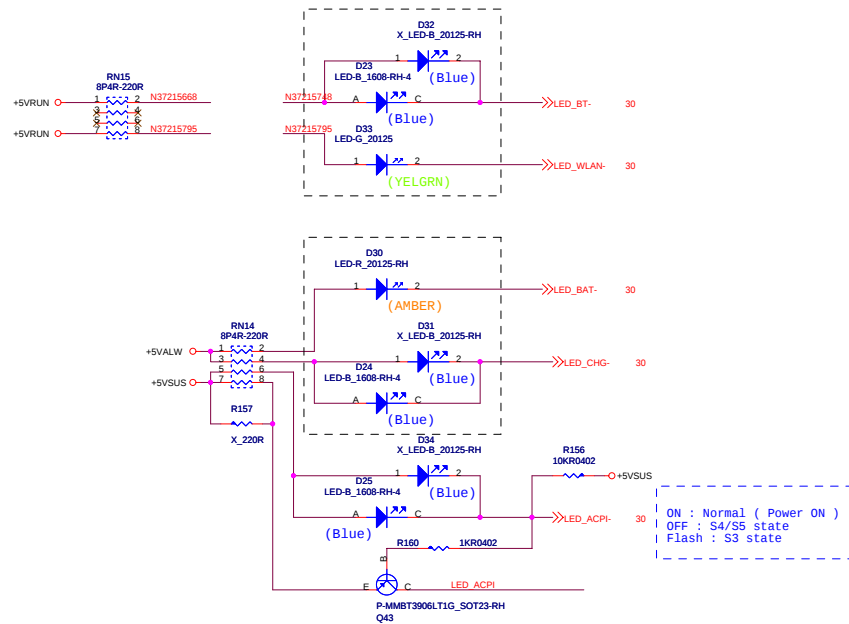
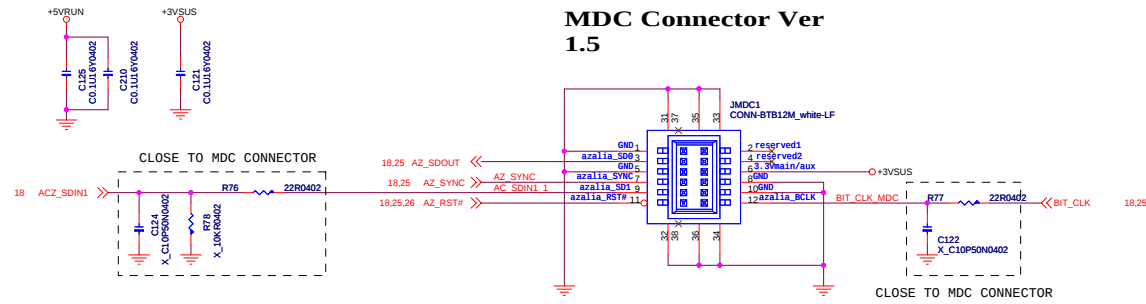
BLUETOOTH

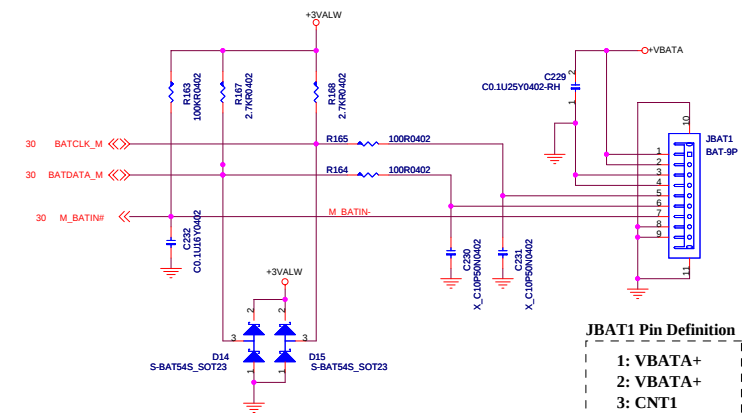
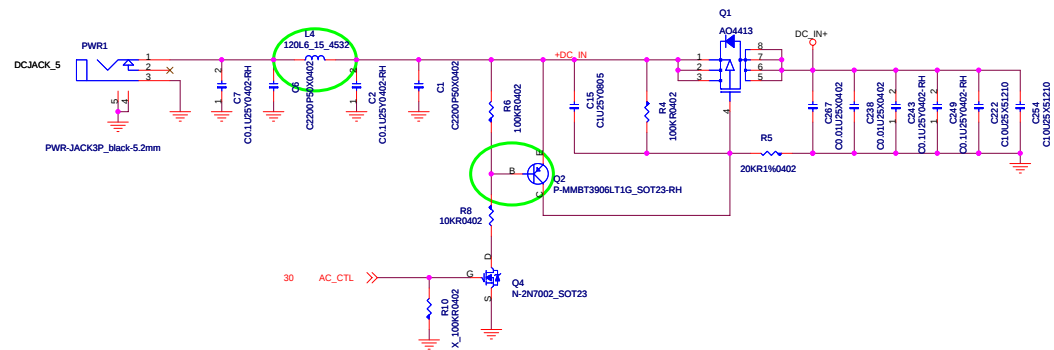


			MICRO-STAR INT'L CO.,LTD	
			MS-163B1	
Size B	Document Description		Rev 0A	
	Mini-PCI & WLAN/BT On/Off CTRL			
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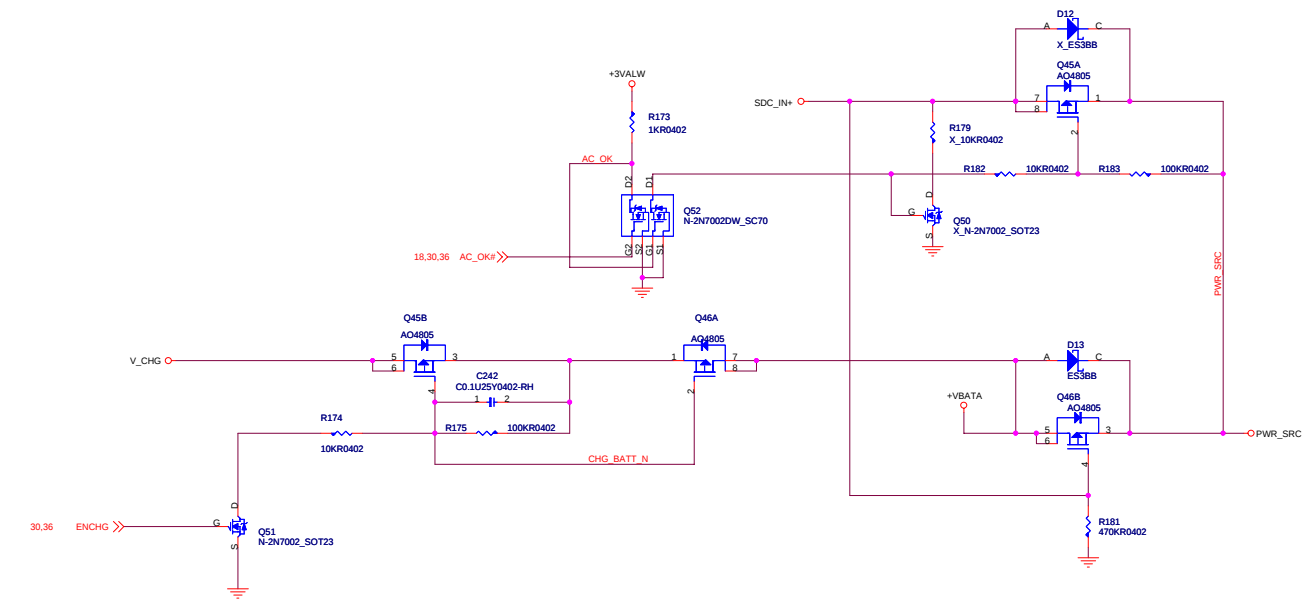
MDC Connector Ver 1.5

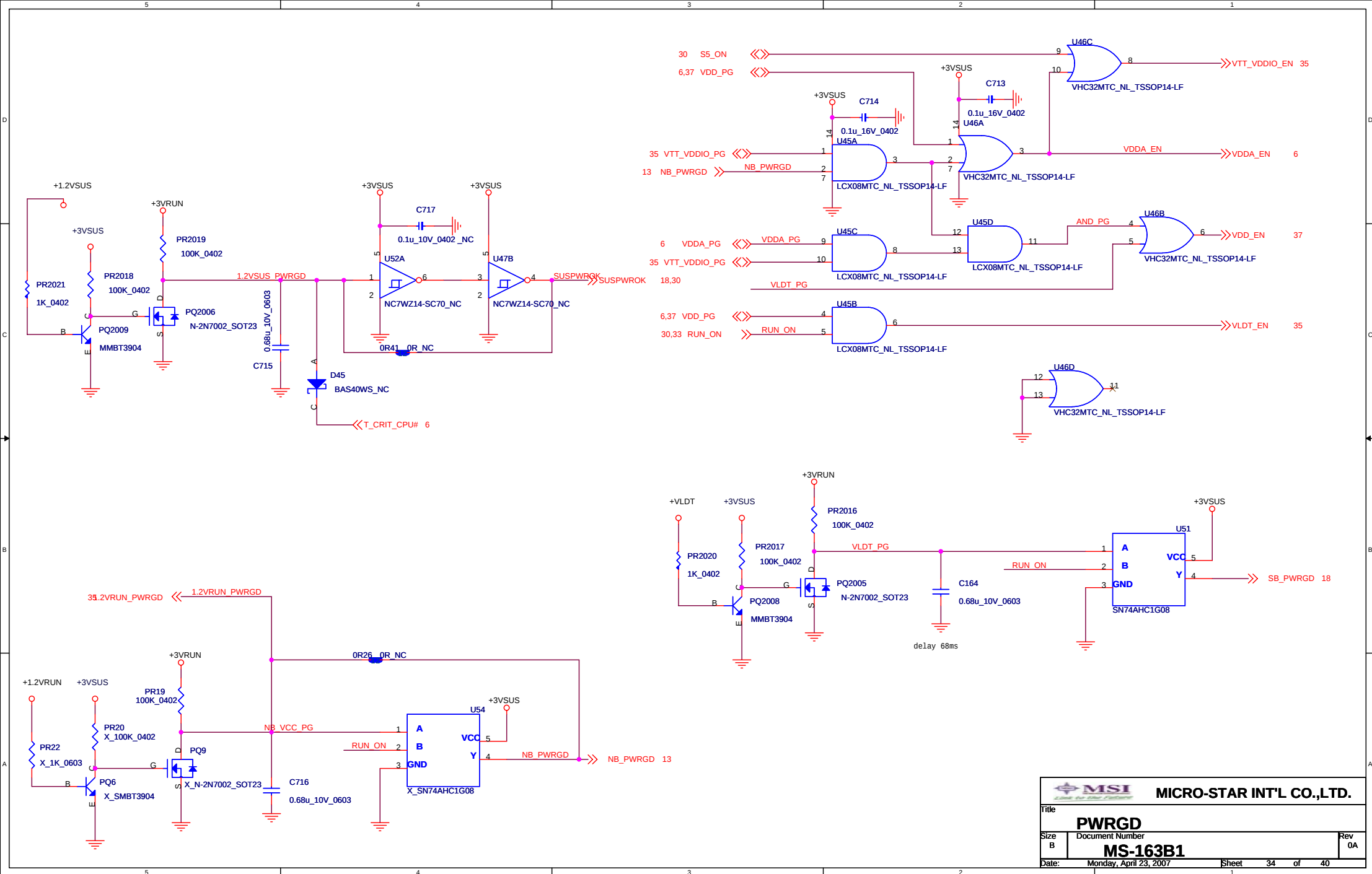


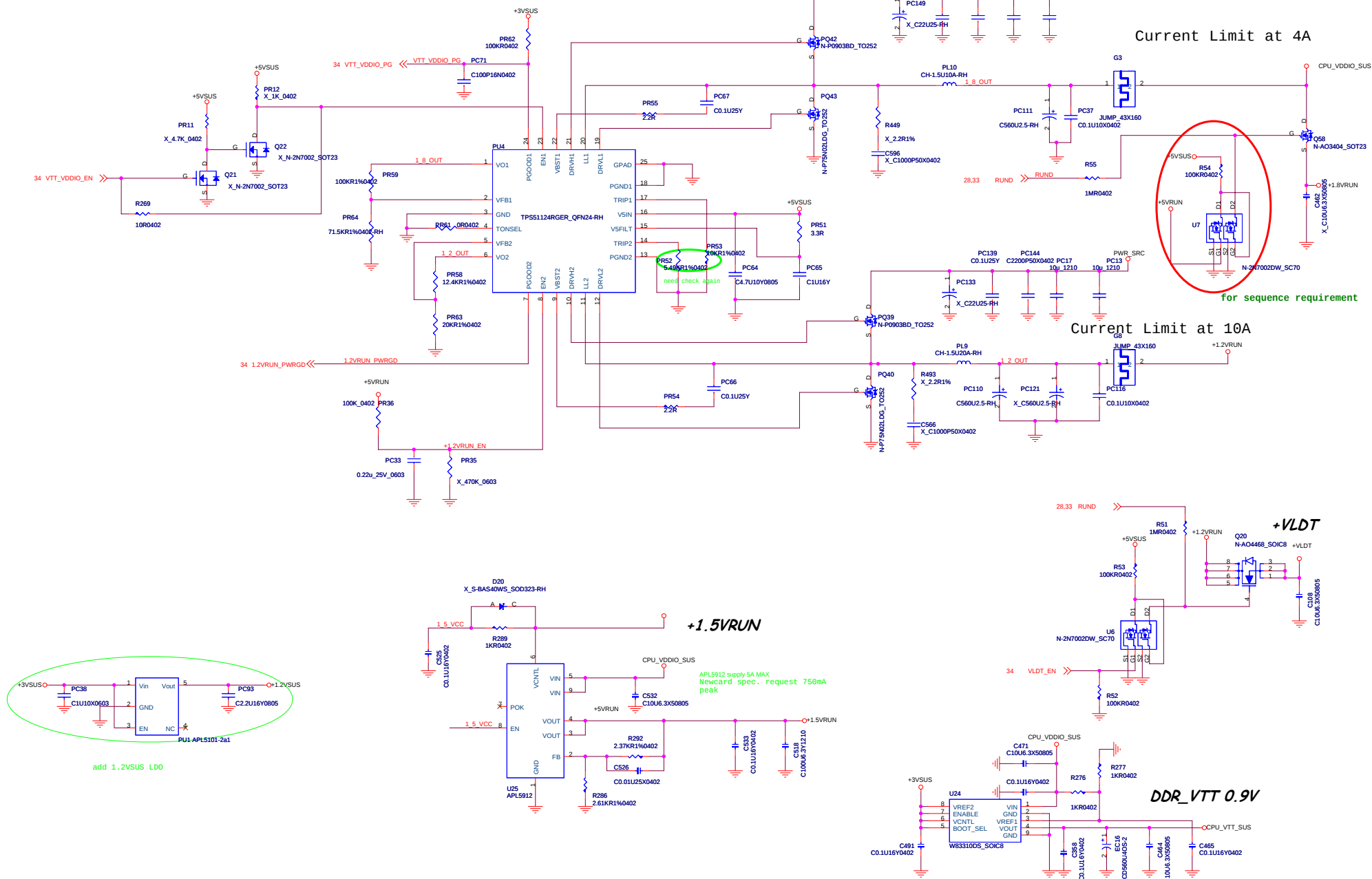


JBAT1 Pin Definition

- 1: VBATA+
- 2: VBATA+
- 3: CNT1
- 4: CNT2
- 5: SMBCLK
- 6: SMBDATA
- 7: THERMAL
- 8: VBATA-
- 9: VBATA-
- 10: GND
- 11: GND







Adapter= 65W
Adapter input voltage set 17.4 Voltage
 $2.048/7.15 \times (53.6+7.15)=17.4V$

Battery charge current ctrl,
if this signal is used, PR100
will be modified to 0.01 ohm
Aaron

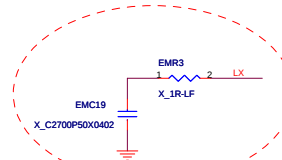
CELL GND=2 CELLS
FLOAT=3 CELLS
REFIN=4 CELLS

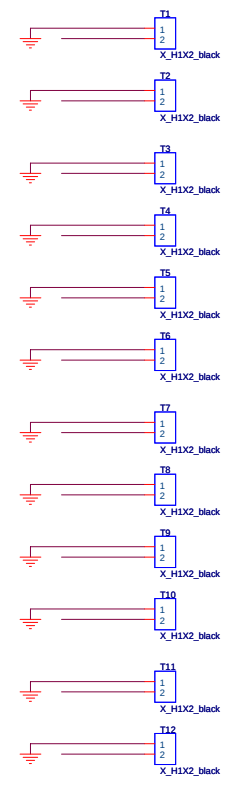
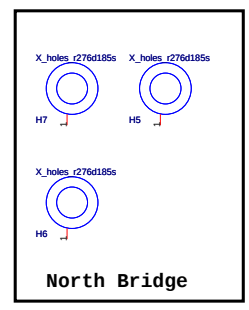
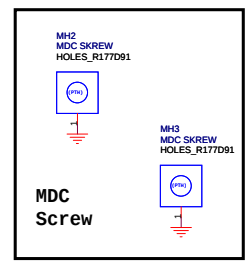
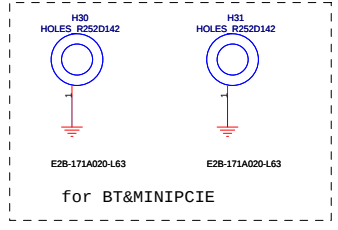
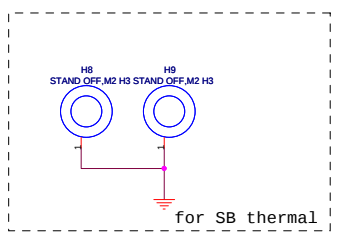
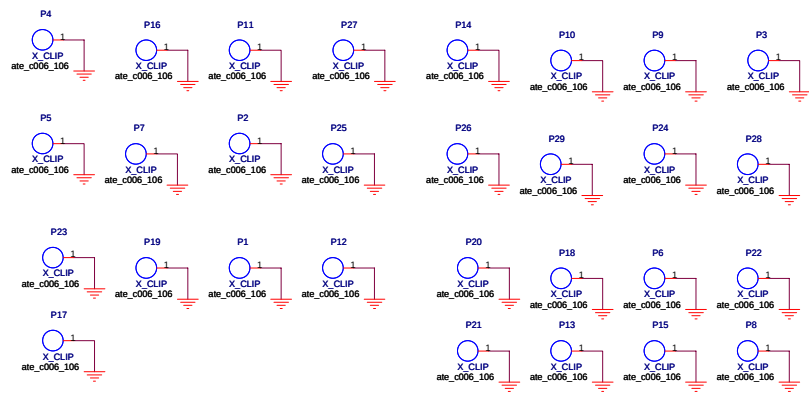
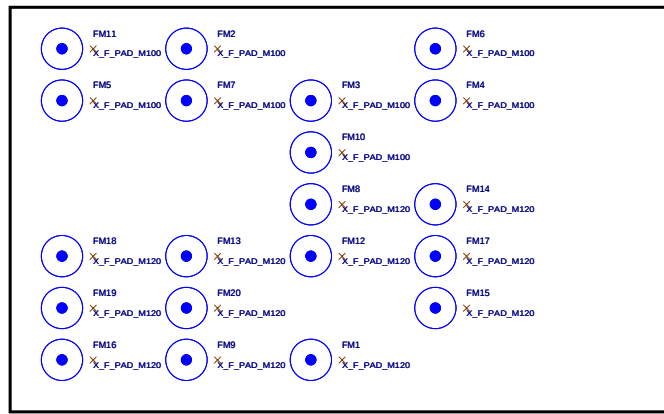
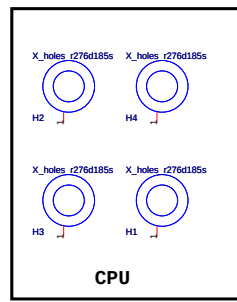
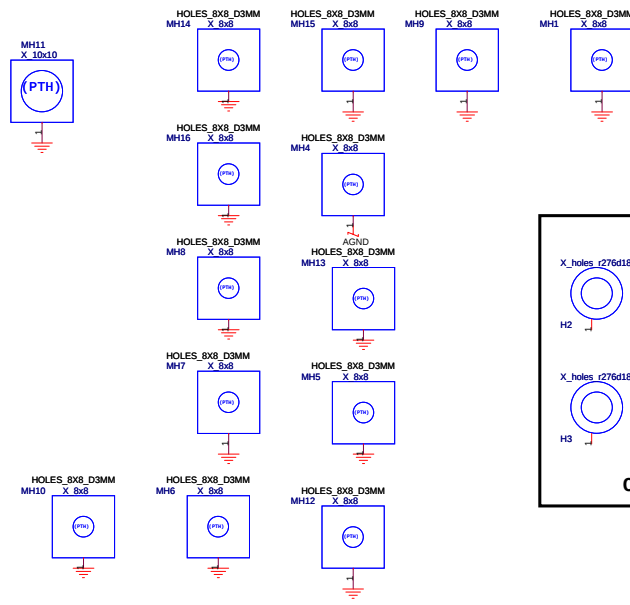
3S2P: Charge current set 3 Amp
3S3P: Charge current set 4.5 Amp
Pre-charger: Charge current set
220mA

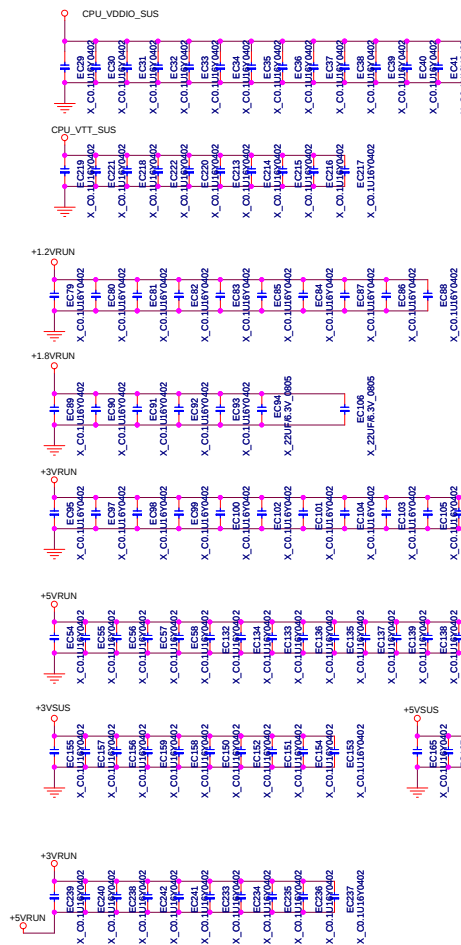
$$IC_{HG} = (V_{ICTL} / V_{REFIN}) \times (0.75 / R_{S2})$$

ENCHG_2P	PRE_CHG	ENCHG	
0	1	1	Pre-charge
1	0	1	3S2P-Fast charge
0	0	1	3S3P-Fast charge
0	0	0	STOP CHARGE

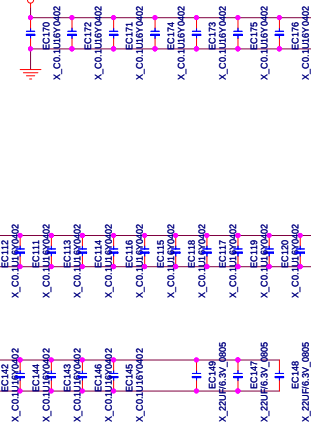
$$I_{in} = (V_{cls} / V_{ref}) \times (0.075 / R_{S1})$$



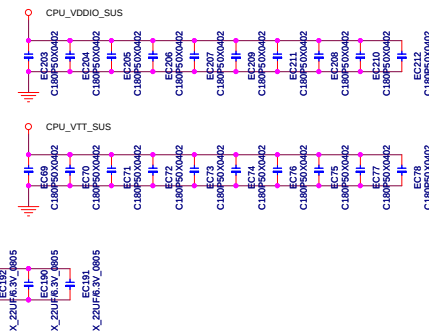
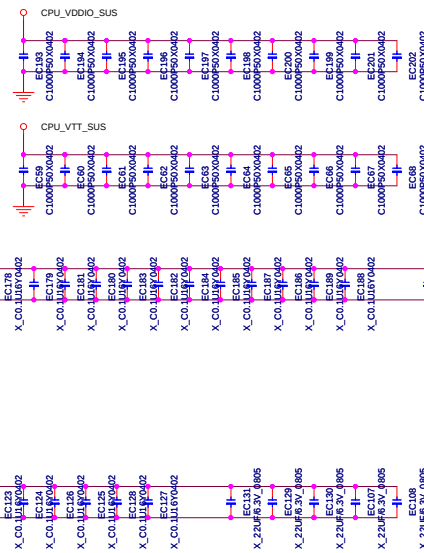




PWR_SRC



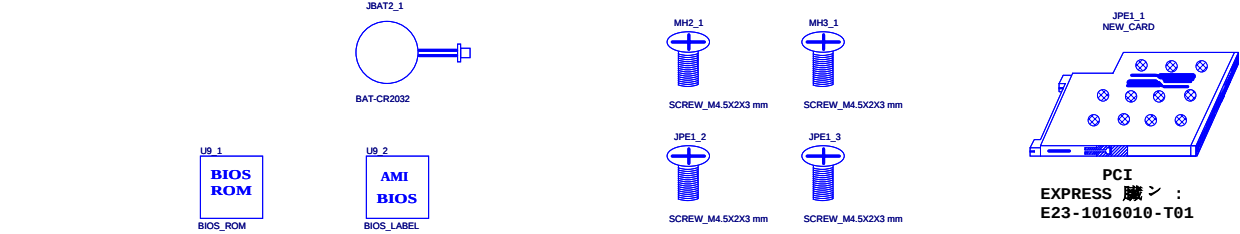
CPU_VDD_RUN



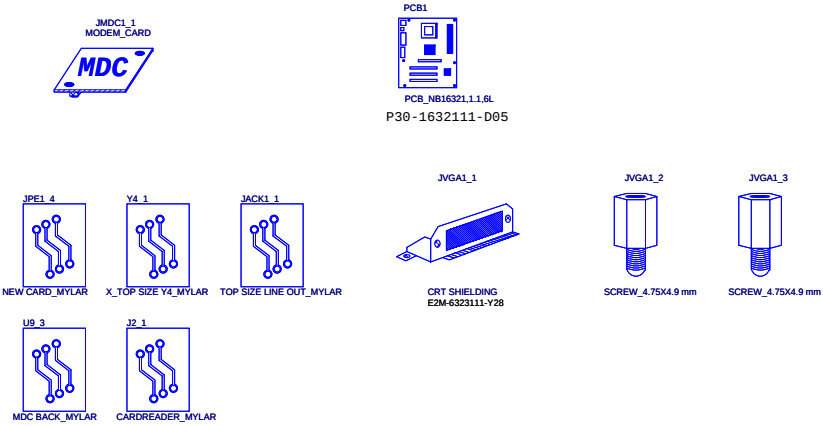
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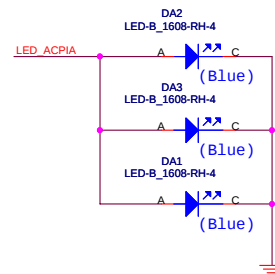
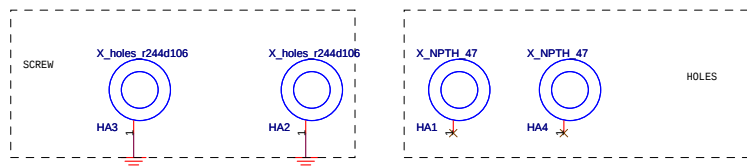
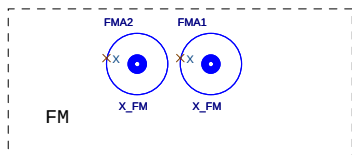
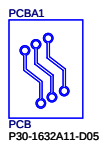
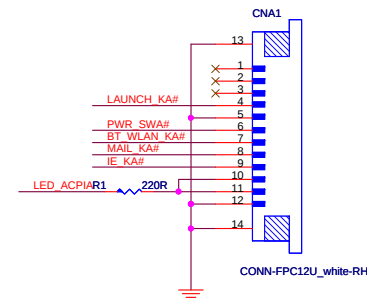
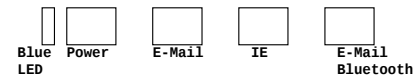
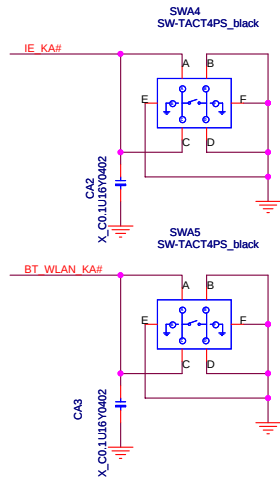
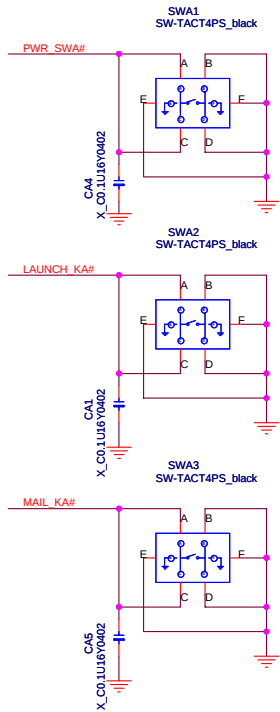
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