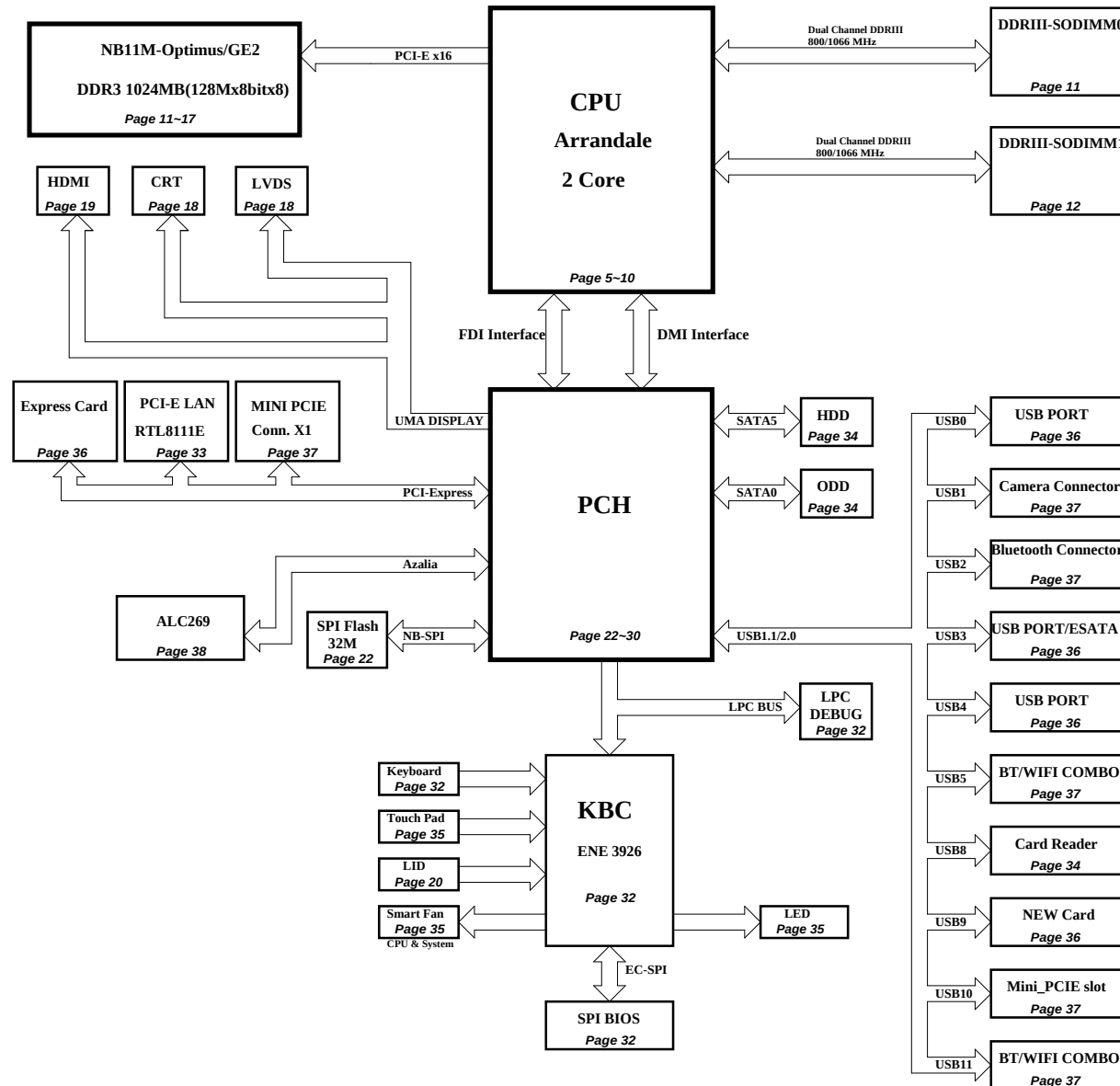
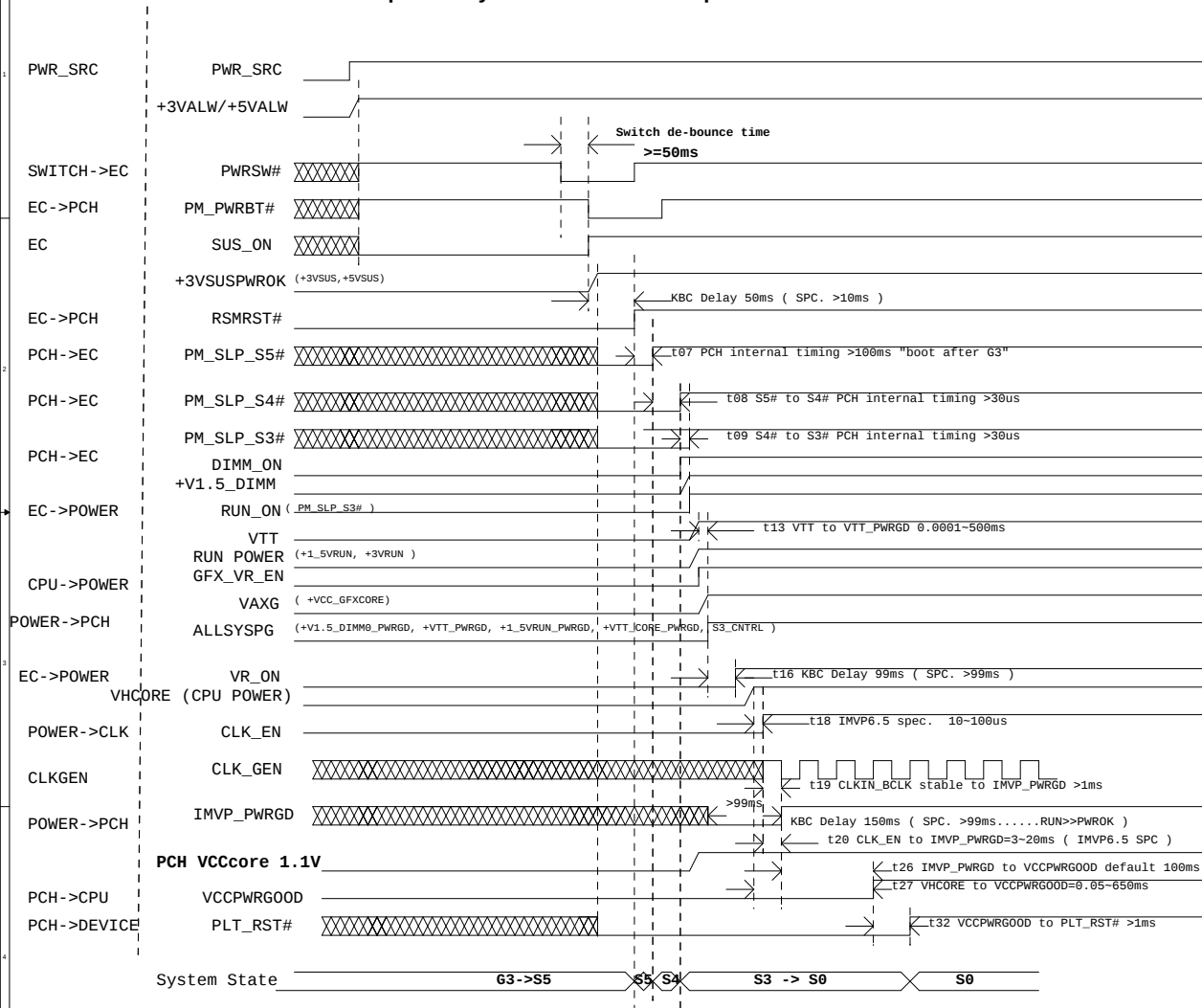


Table of Contents

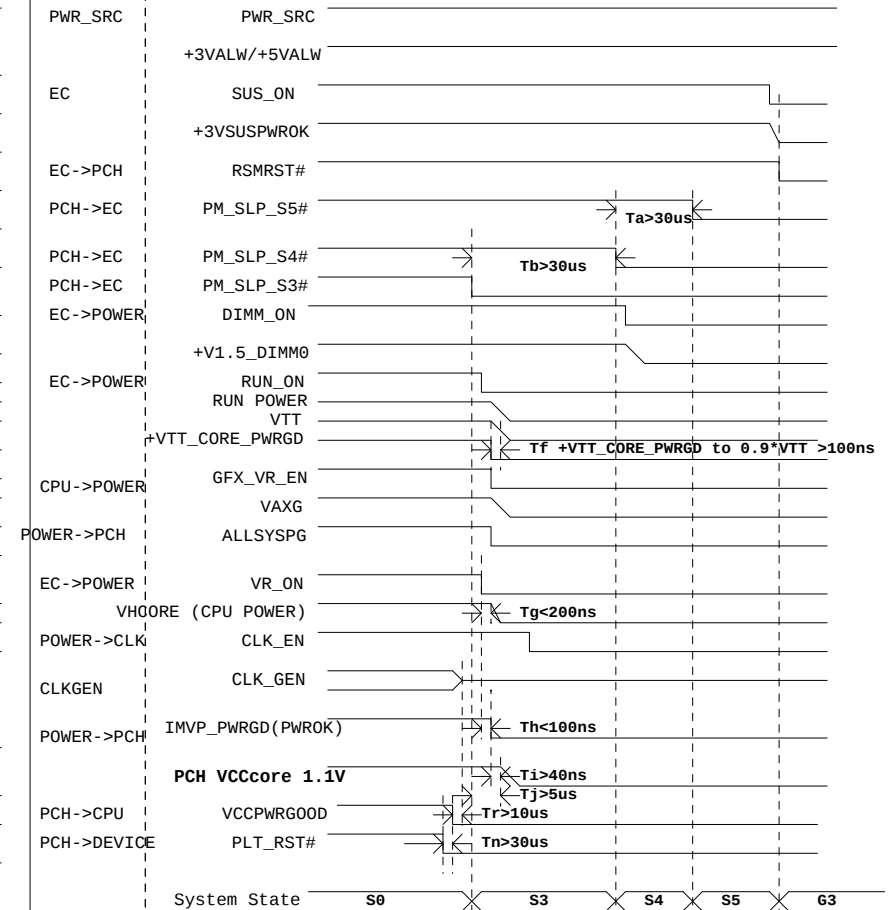
Page	Description
01	BLOCK DIAGRAM
02	Power Delivery
03	Power Sequency
04	Clock/SMBus Distribution
05	PROCESSOR-1 (HOST BUS)
06	PROCESSOR-2 (DDR3)
07	PROCESSOR-3 (POWER)
08	PROCESSOR-4 (GRAPHICS POWER)
09	PROCESSOR-5 (GND)
10	PROCESSOR-6 (RESERVE)
11	DDR3 SODIMM 0
12	DDR3 SODIMM 1
13	NB11M_GE2(PCIE Interface)
14	NB11M_GE2(FB interface)
15	NB11M_GE2(VRAM)
16	NB11M_GE2(VRAMB)
17	NB11M_GE2(CRT/LVDS)
18	NB11M_GE2(GPIO)
19	NB11M_GE2(STRAPS)
20	CRT,LVDS connector & LID
21	LEVEL SHIFT&HDMI
22	PCH-1 (HDA,JTAG,SATA)
23	PCH-2 (PCI-E,SMBUS,CLK)
24	PCH-3 (DMI,FDI,GPIO)
25	PCH-4 (LVDS,DDI)
26	PCH-5 (PCI,USB,NVRAM)
27	PCH-6 (GPIO,VSS_NCTF,RSVD)
28	PCH-7 (POWER)
29	PCH-8 (POWER)
30	PCH-9 (GND)
31	Clock Generator (9LRS3199AKL)
32	KBC/EC/uP (KB3926)
33	PCI-E Lan (RTL8111E)
34	Cardreader (UB6250)
35	FAN,Lauch board
36	HDD,CDROM,USB,NEWCARD,ESATA
37	MINIPICIE,CAMERA,BLUETOOTH,SW
38	CODEC(ALC269)
39	M_Battery select
40	M_Battery Charger
41	M_System Power
42	SMDDR_VTERM/1_5VRUN
43	VTT POWER,+1.8VRUN
44	M_CPU power
45	M_Graphic Core
46	NVVD, +1.03VRUN
47	Screw/ ME
48	168AA_USB BOARD
49	168AB_Lauch board
50	EMI
51	Change List

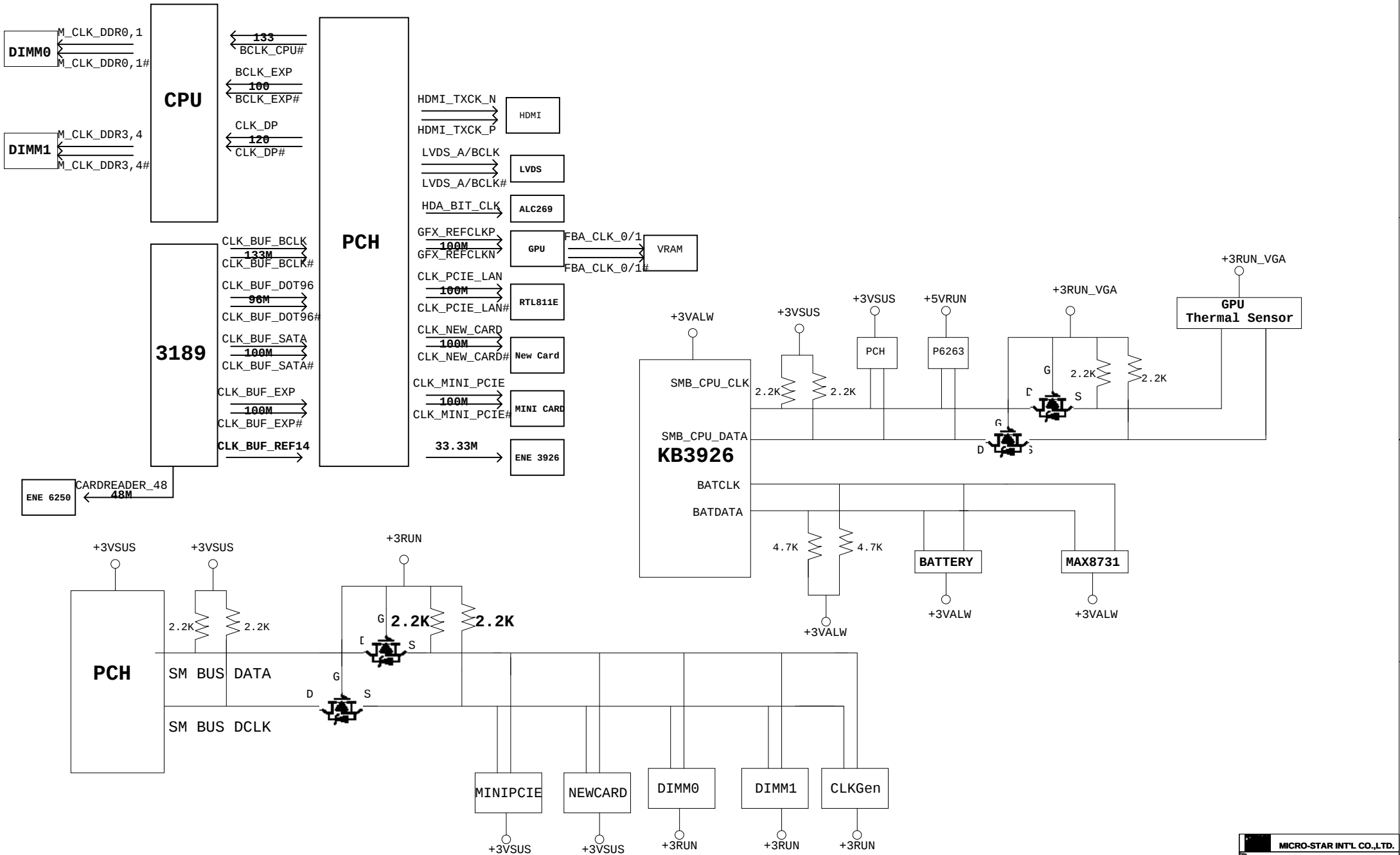


Calpella System Power on Sequence DC mode

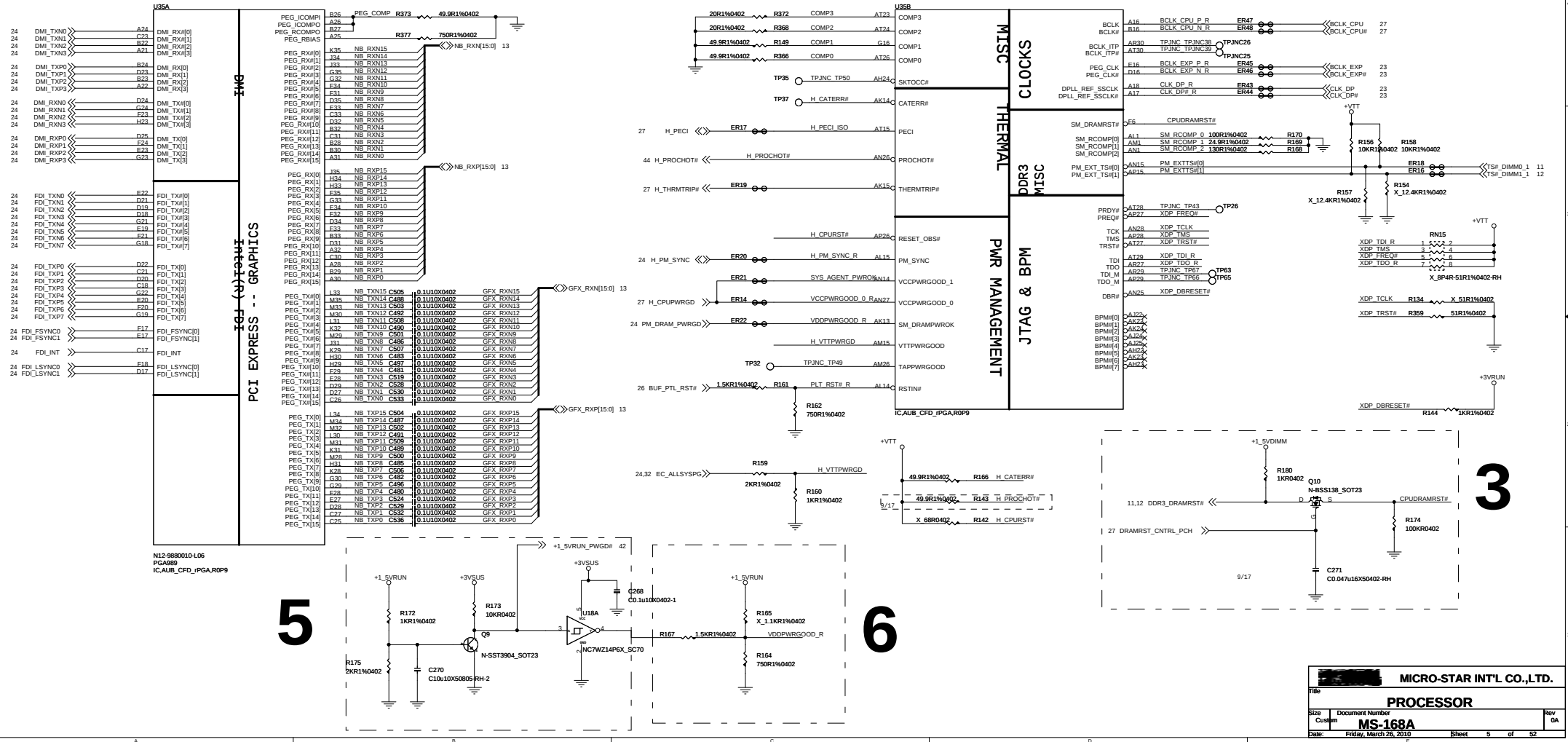


Power down Sequence DC mode S0 to G3

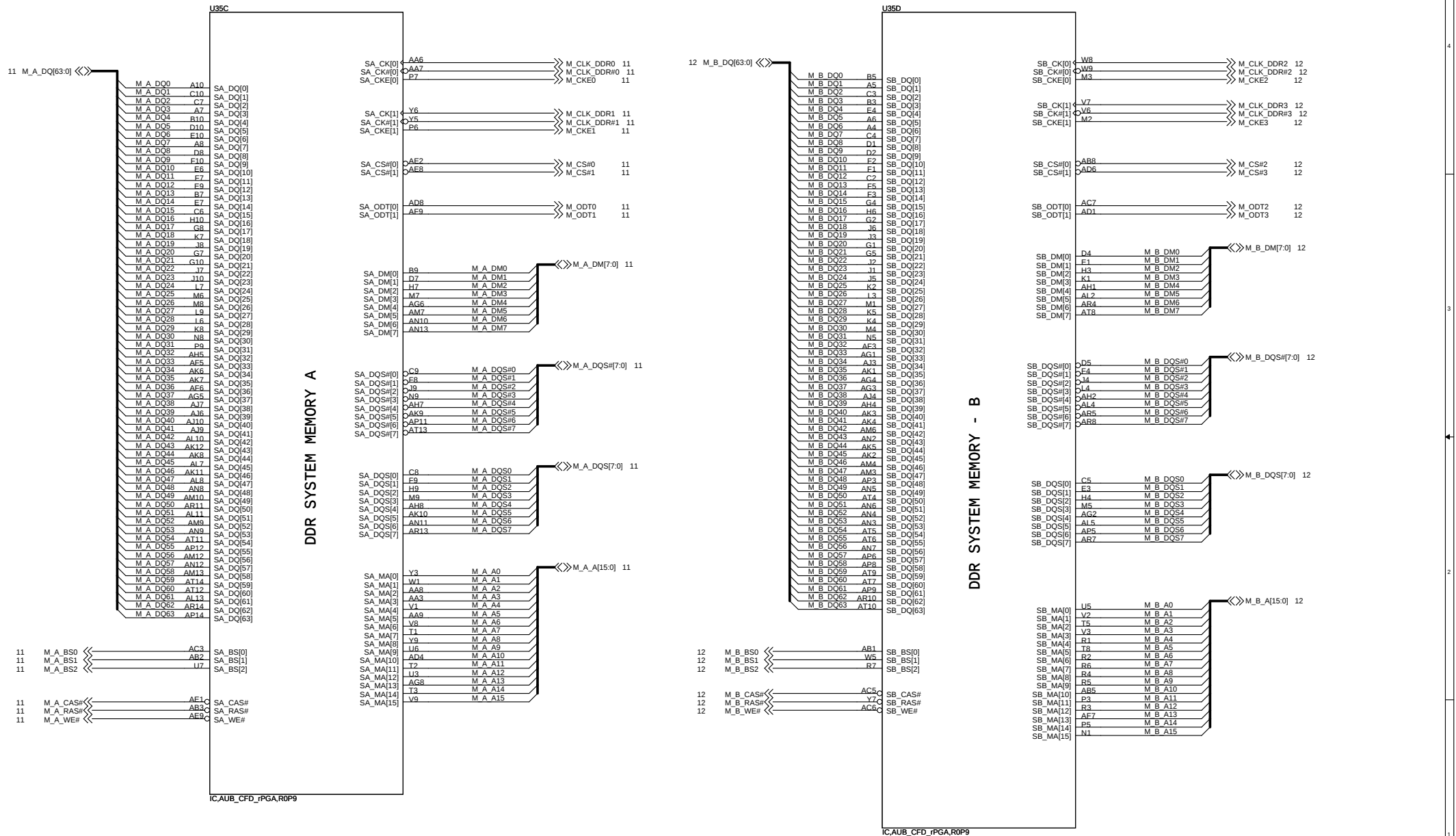




ARRANDALE PROCESSOR (CLK, MISC, JTAG)



ARRANDALE PROCESSOR (DDR3)



ARRANDALE PROCESSOR (POWER)

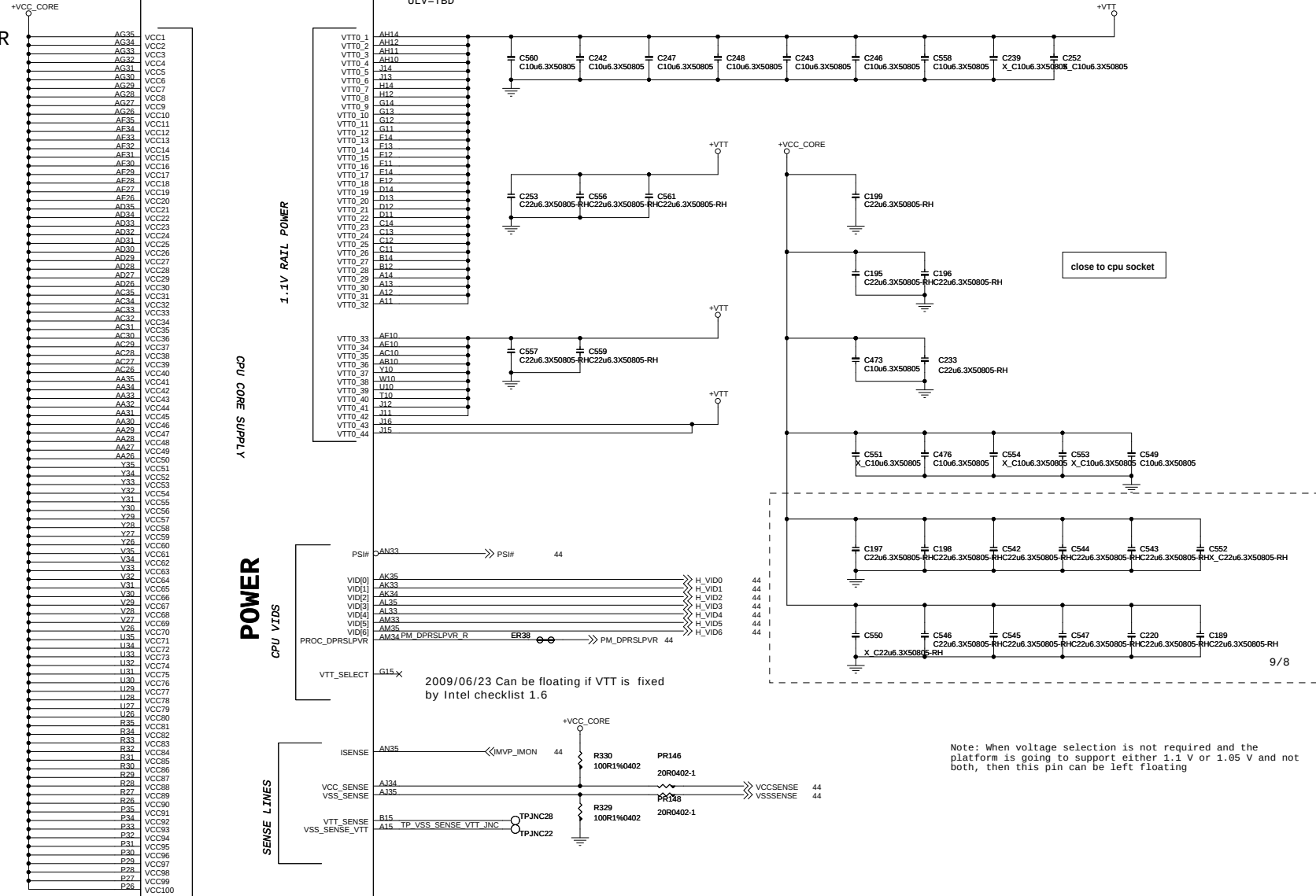
ARRANDALE:
SV=48A
LV=35A
ULV=27A

U35F

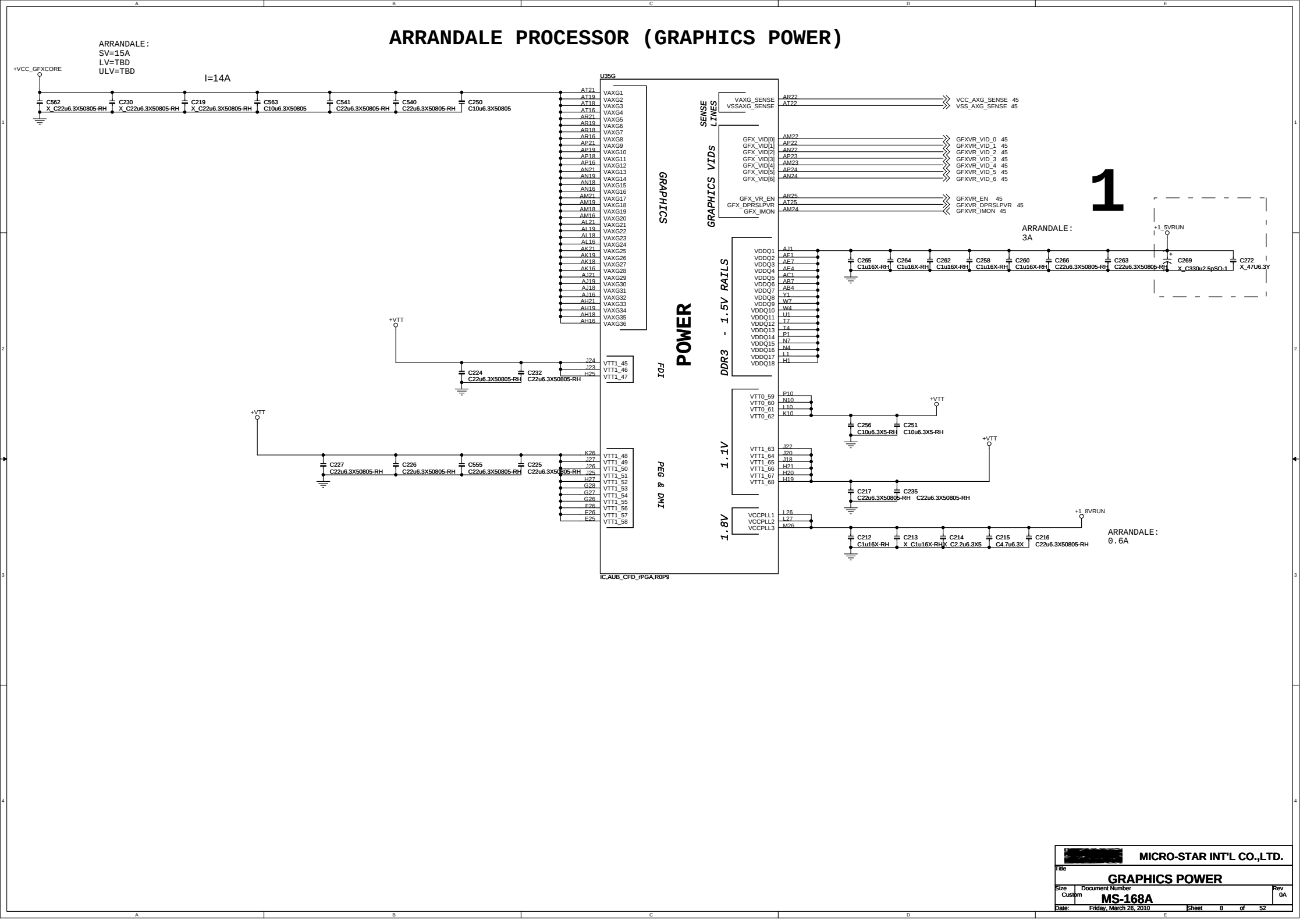
ARRANDALE:
SV=18A
LV=18A
ULV=TBD

PROCESSOR CORE POWER

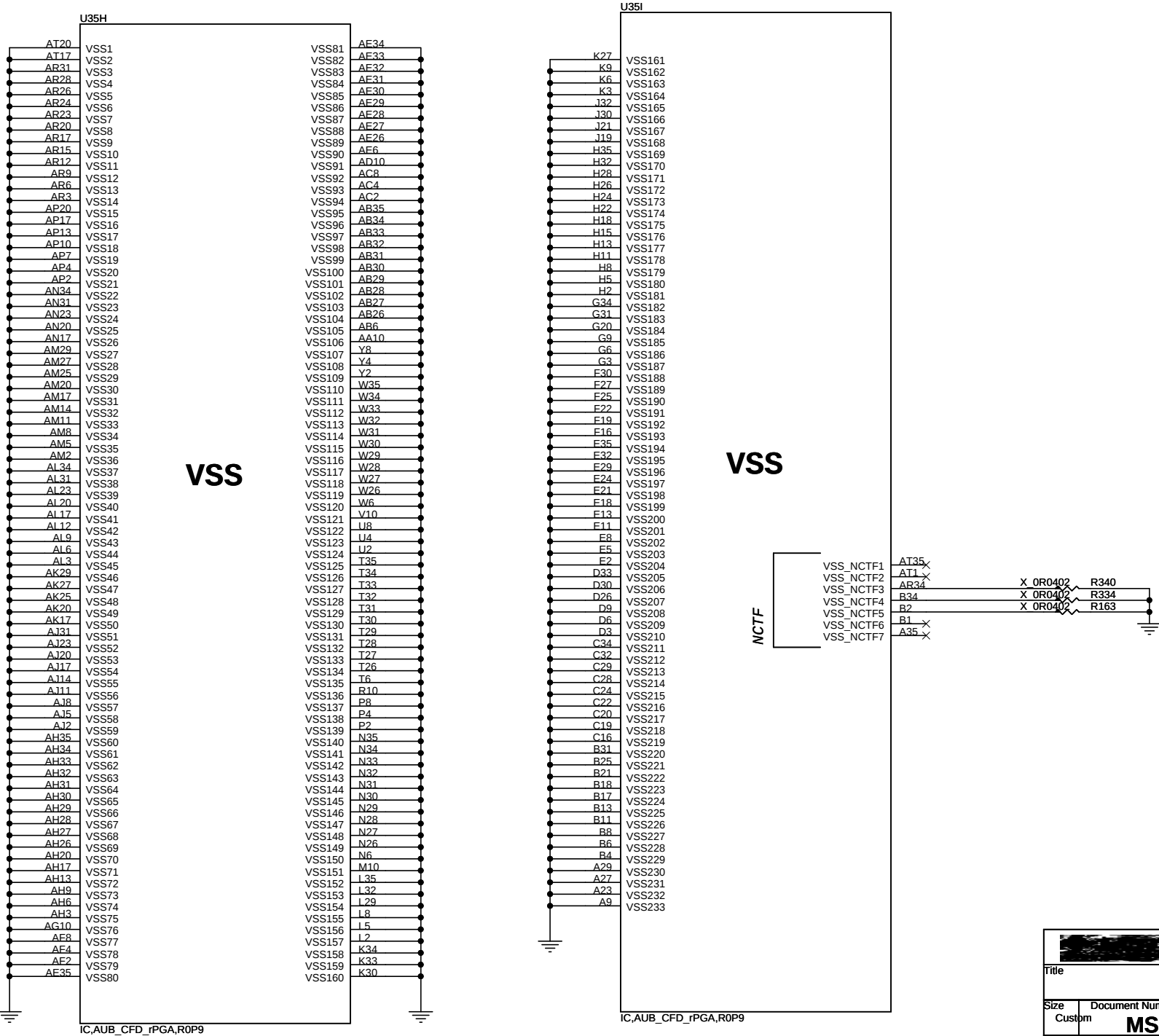
PROCESSOR CORE POWER



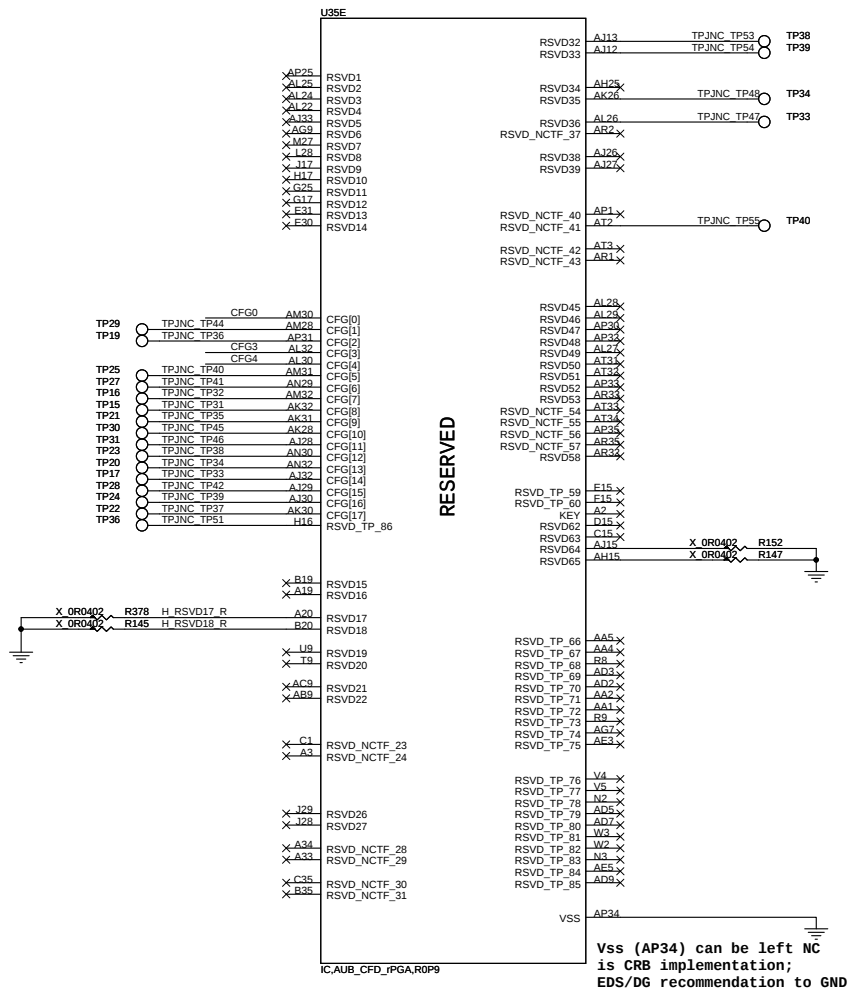
ARRANDALE PROCESSOR (GRAPHICS POWER)



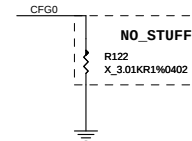
ARRANDALE PROCESSOR (GND)



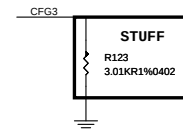
ARRANDALE PROCESSOR (RESERVED)



PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

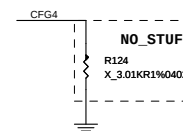


CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...



CFG3] PCI Express* Static Lane
Numbering Reversal. Lane Reversal will be
applied across all 16 Lanes.
1: No lane reversal
0: Reversal

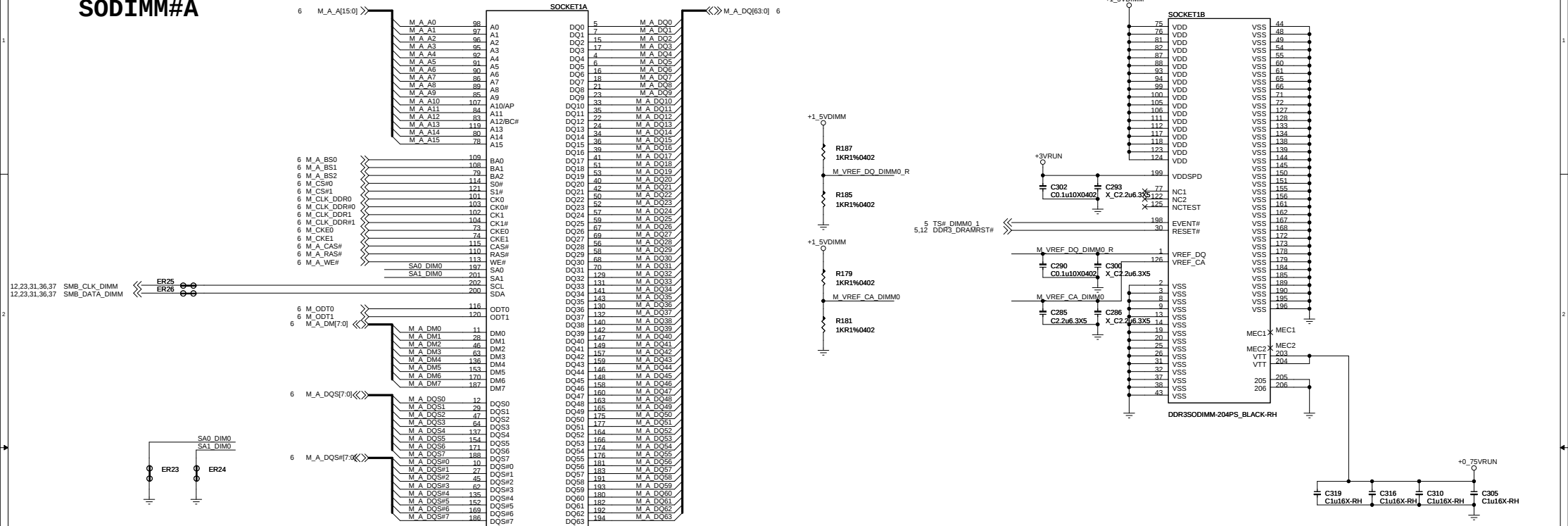
CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port



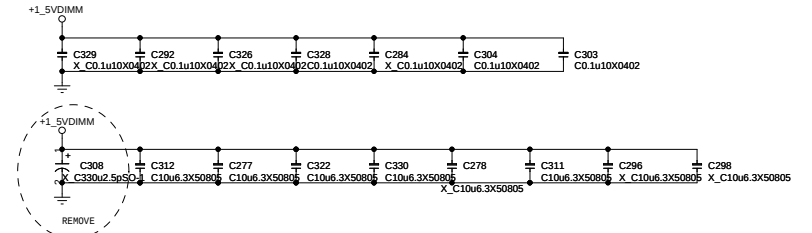
Layout Note:
Location of all CFG strap resistors needs
to be close to trace to minimize stub

Vss (AP34) can be left NC
is CRB implementation;
EDS/DG recommendation to GND

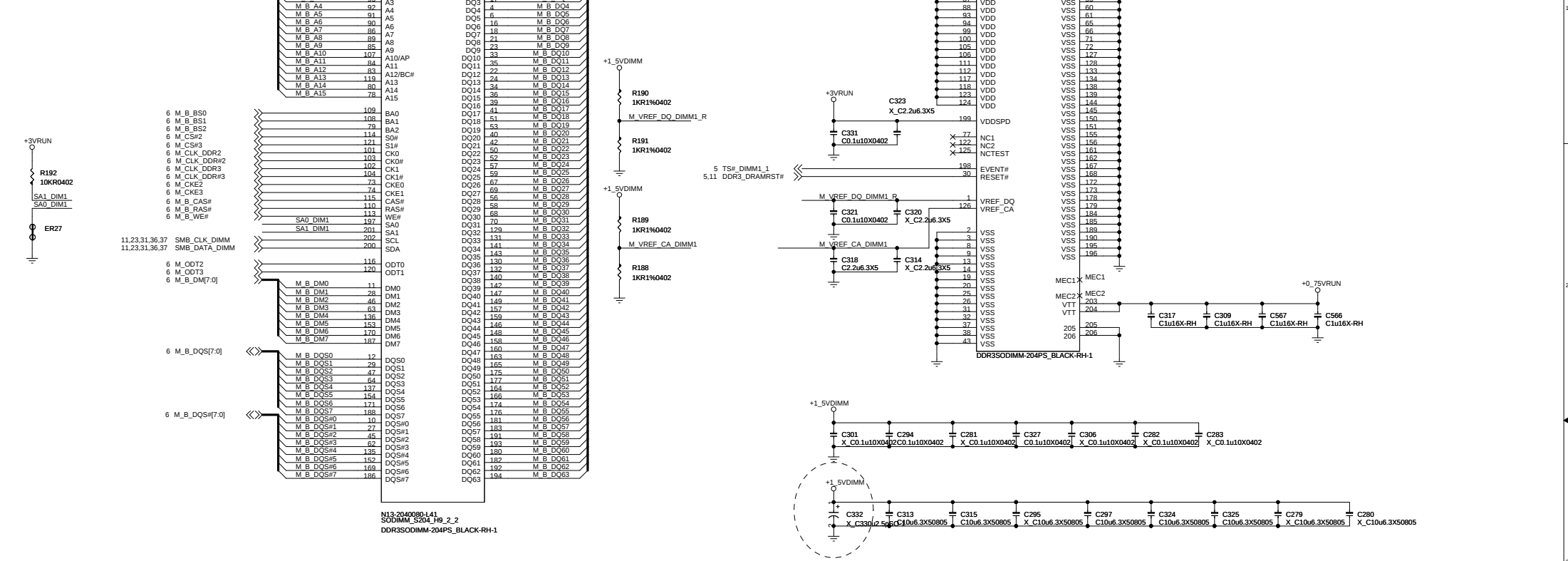
SODIMM#A

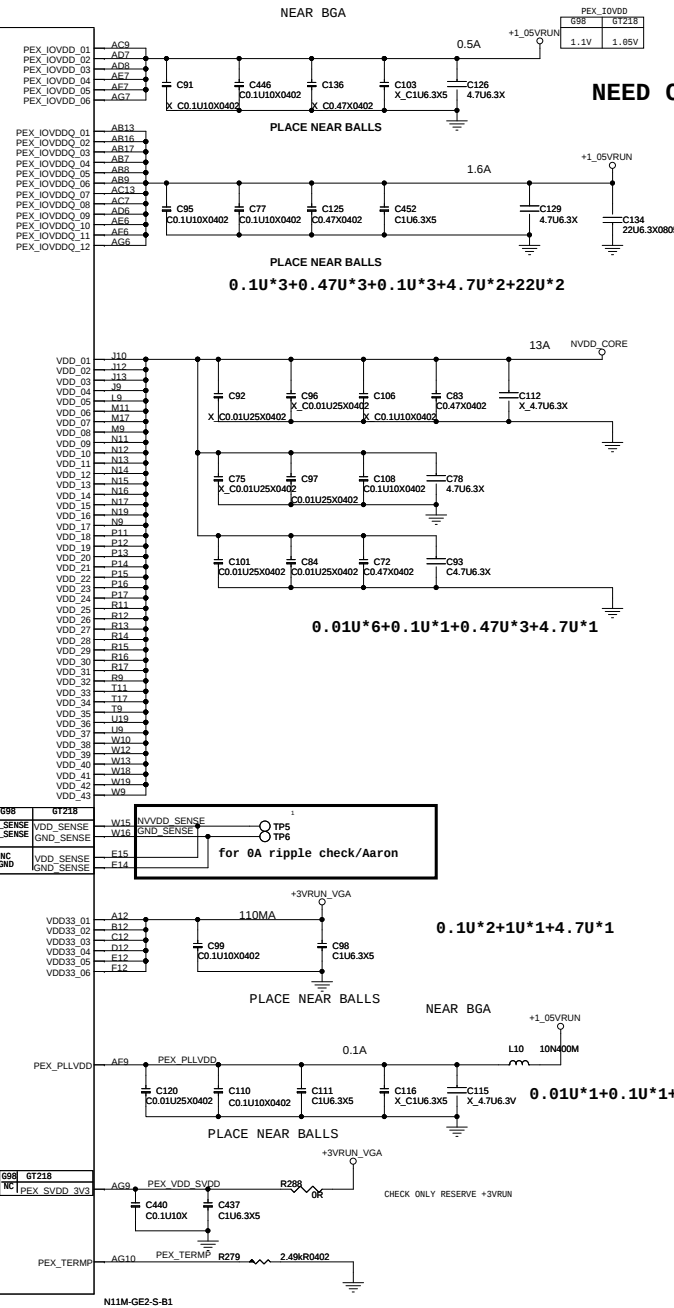
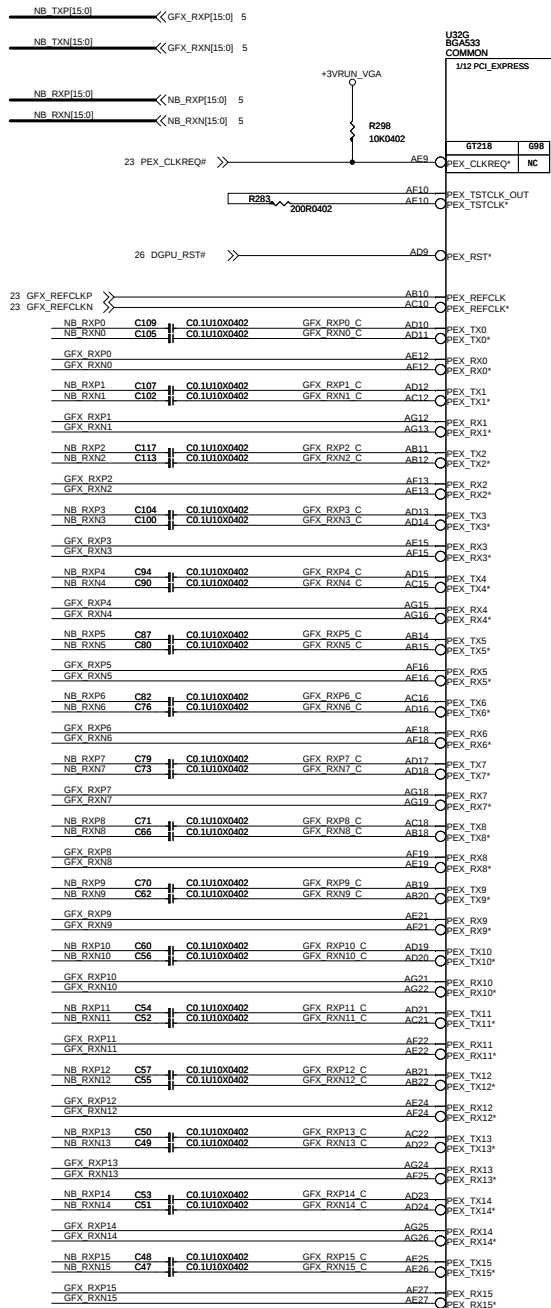


N13-2040060-L41
SODIMM_S204_P#5_2
DDR3SODIMM-204PS_BLACK-RH

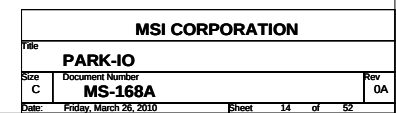


SODIMM#B

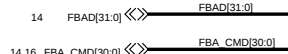




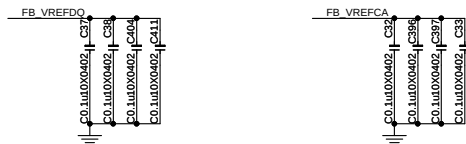
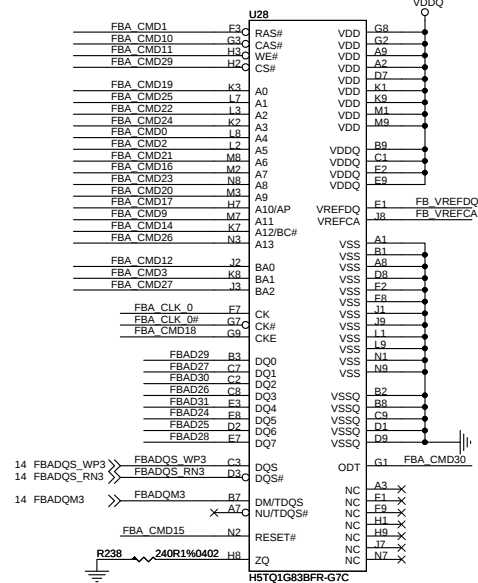
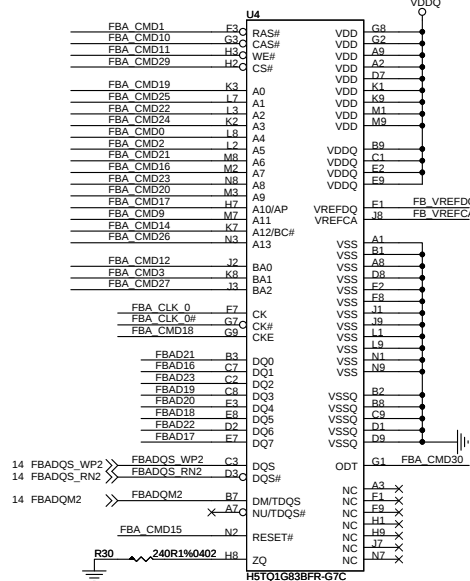
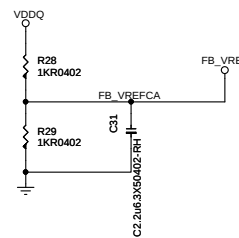
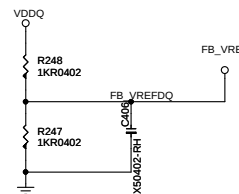
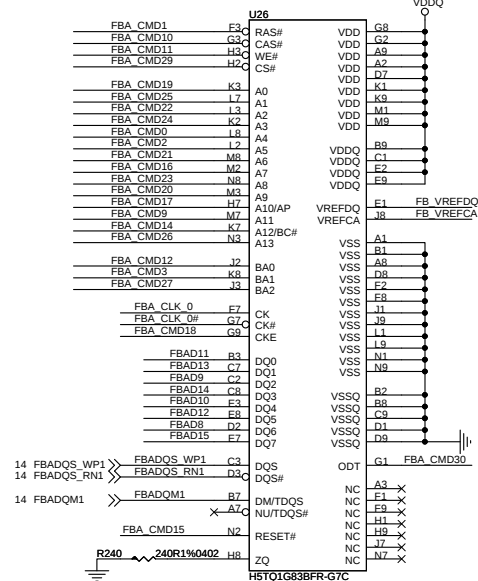
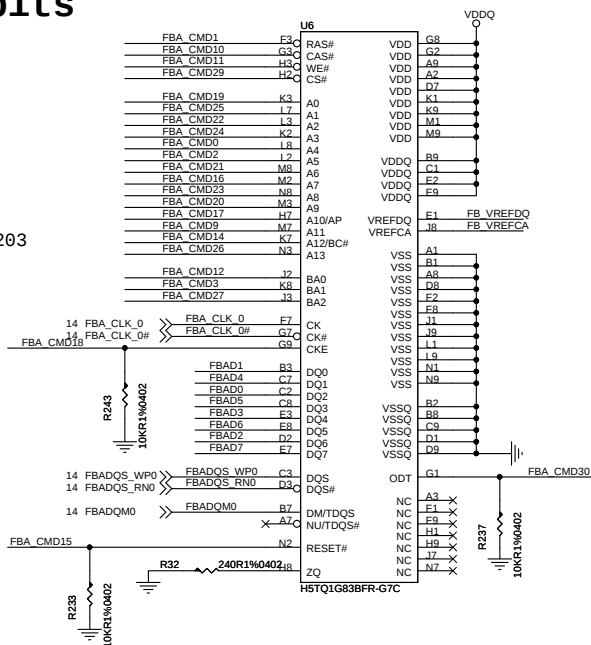
NEED CHANGE 1.1V to 1.05V 1130



DDR3 128Mx8bits



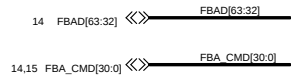
R252 need change to 242 ohm.1203



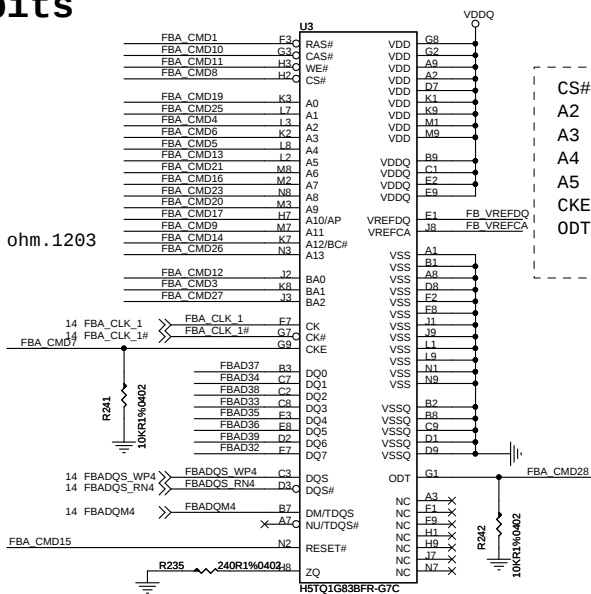
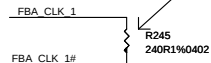
Each group(top & bottom) put a 0.1uF

MSI CORPORATION		
Title	PARK-POWER	
Size	Document Number	Rev
Custom	MS-168A	0A
Date:	Friday, March 26, 2010	Sheet 15 of 52

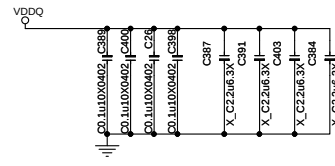
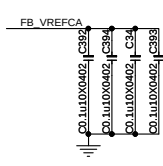
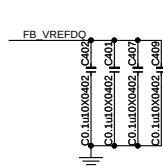
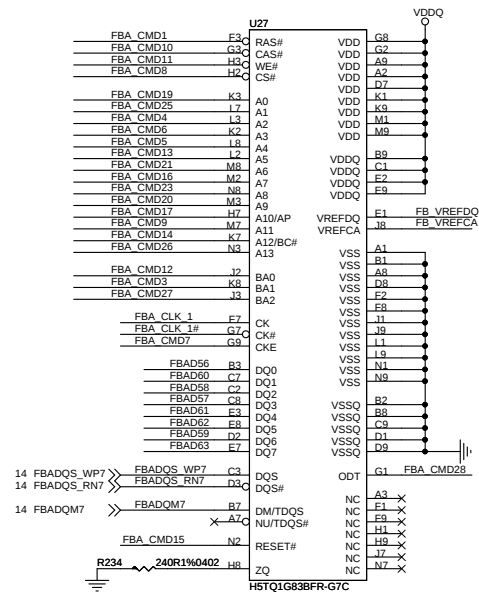
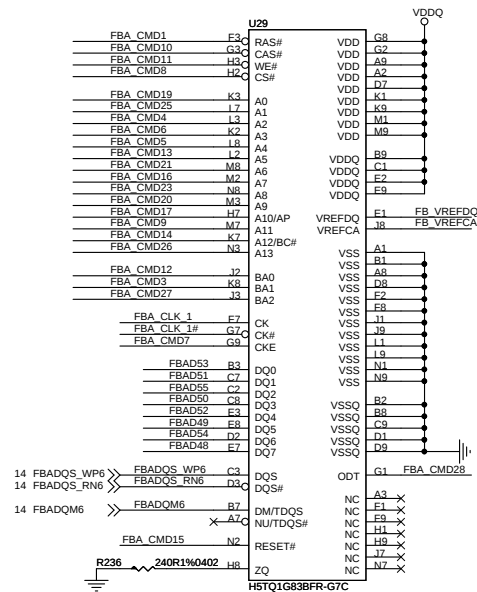
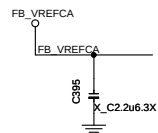
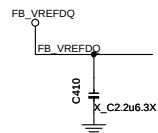
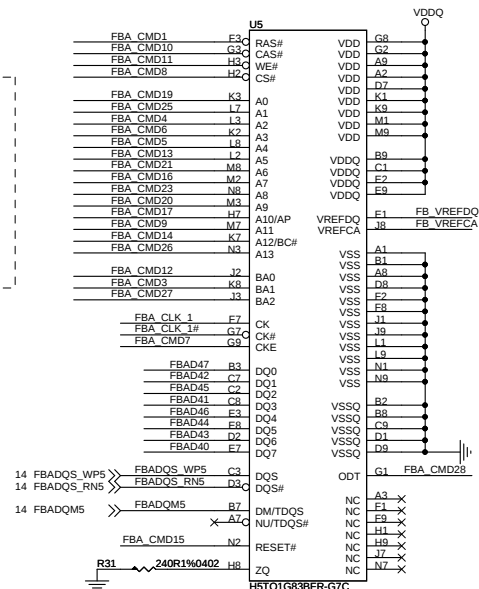
DDR3 128Mx8bits



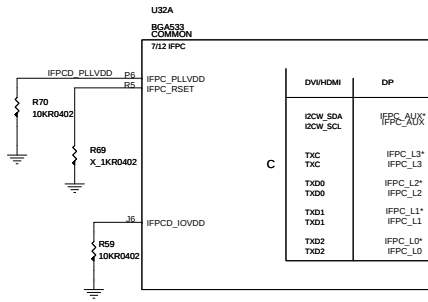
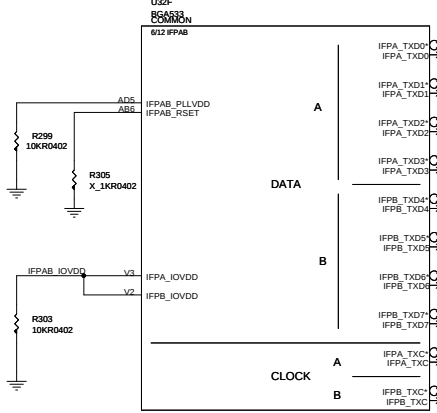
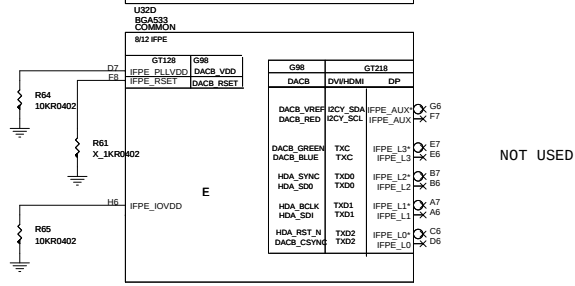
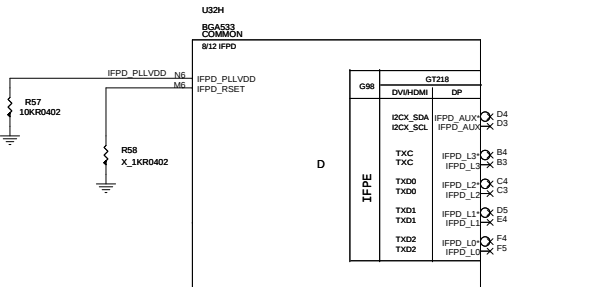
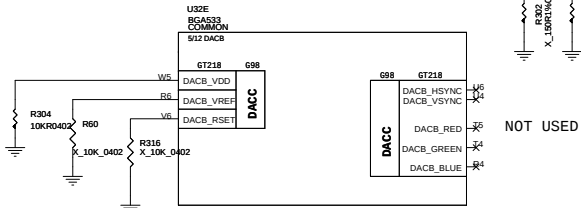
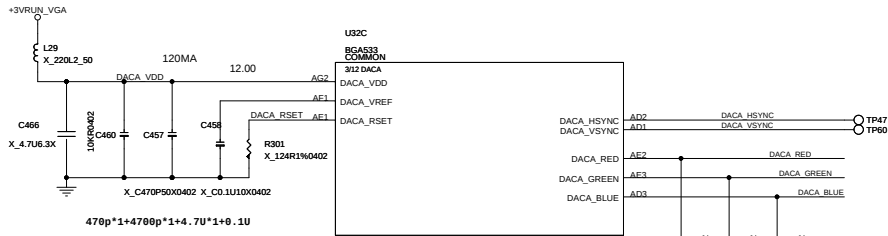
R264 need change to 242 ohm.1203



```
CS# 29; 8
A2 22; 4
A3 24; 6
A4 0; 5
A5 2; 13
CKE 18; 7
ODT 30; 28
```



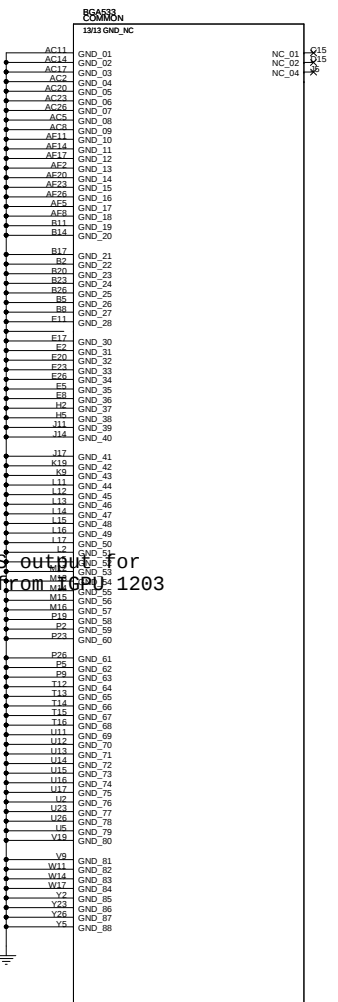
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Title PARK-power straps			
Size	Document Number		Rev
Custom	MS-168A		0
Date:	Friday, March 26, 2010	Sheet	16 of 52



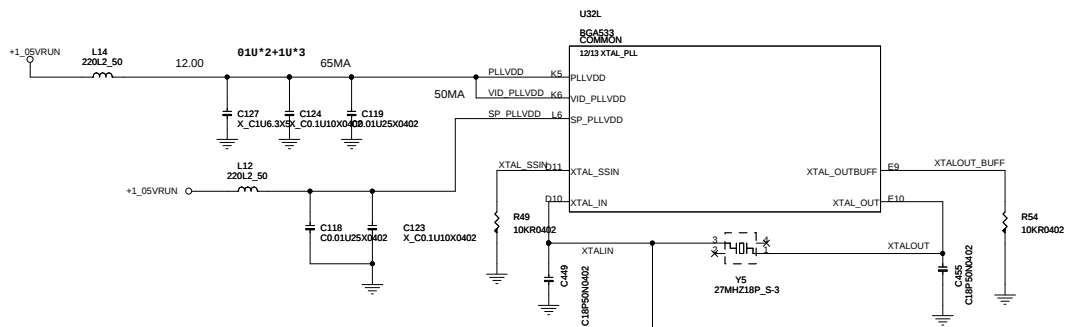
need delete DGPU output 1125

delete DGPU LVDS output for Optimus output from GPU 1203

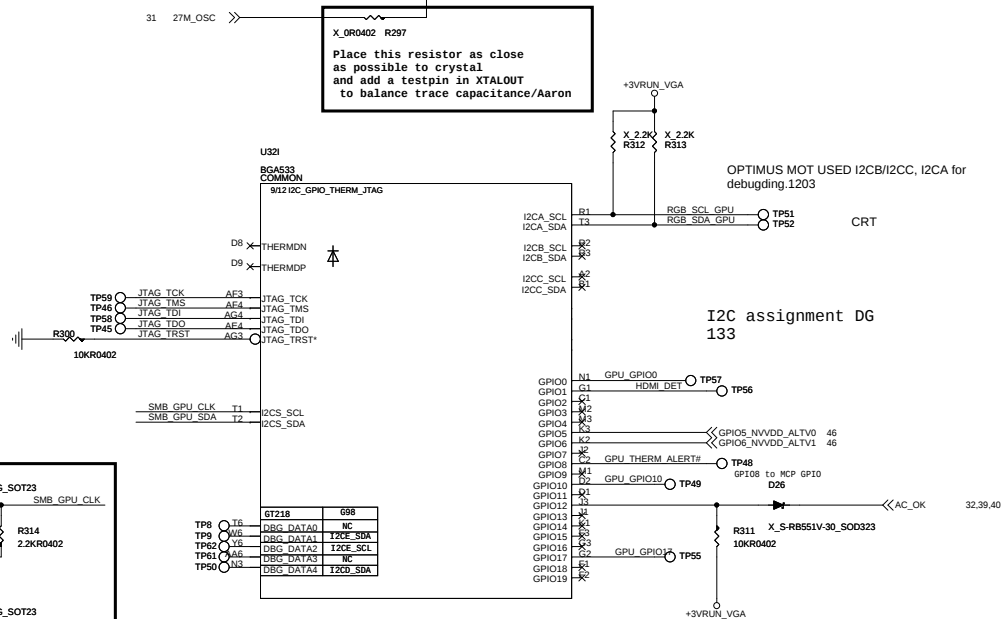
OPTIMUS not use GPU HDMI, delete 1203



MICRO-STAR INT'L CO., LTD.			
Title: PARK MEM I/F			
Size: Custom	Document Number: MS-168A	Rev: 0A	
Date: Friday, March 28, 2019	Sheet: 17	of 52	

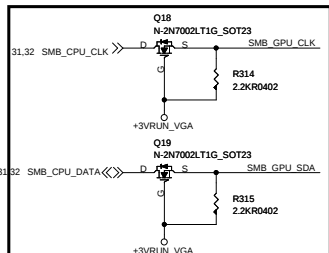


Place this resistor as close as possible to crystal and add a testpin in XTALOUT to balance trace capacitance/Aaron



I2C assignment DG 133

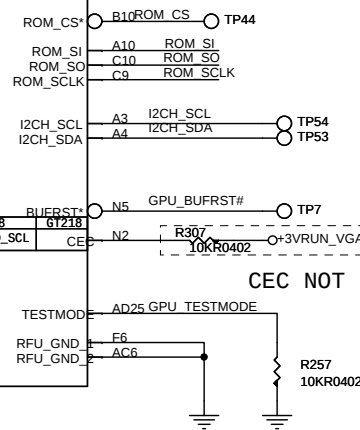
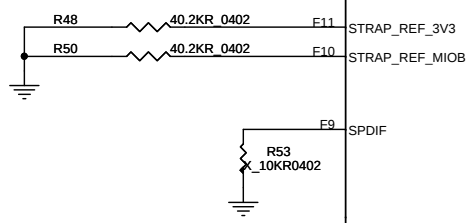
When use GPIO. Need Pull high or pull LOW.



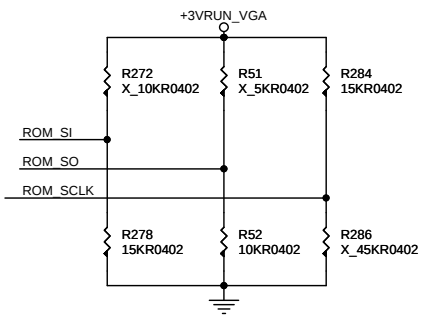
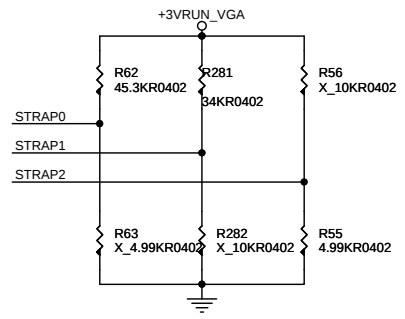
For Optimus system VGA no power @IGP mode 1203/ron

GPIO USAGE			
GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	HDMI HOTPLUG DETECT
1	IN	N/A	DVI/HDMI LINKC HOTPLUG DETECT
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	HIGH	NVDD ALT0
6	OUT	HIGH	NVDD ALT1
7	OUT	HIGH	FBVDD VDD0
8	IN	LOW	OVERTEMP ALERT
9	OUT	LOW	THERMAL ALERT
10	OUT	HIGH	DYNAMIC FB VREF GDDR3 (not used for DDR2)
11	OUT	HIGH	SLI SYNC0 (not used for GB1-64)
12	IN	N/A	AC DETECT
13	OUT	LOW	POWER SUPPLY CONTROL0
14	OUT	HIGH	POWER SUPPLY CONTROL1
15	IN	N/A	HPD_E
16	IN	N/A	DVI_E
17	IN	N/A	HDMI_E
18	IN	N/A	DVI_F (not used)
19	IN	N/A	HDMI_F (not used)

GPIO6	GPIO5	NVDD(N10M-SE1)
1	1	1.03V
1	0	0.85
0	1	TDB
0	0	0.85



CEC NOT USED 1130



N10M SE1

STRAP0	USER 3	1
	USER 2	1
	USER 1	1
	USER 0	1
STRAP1	3GIO_PADCFG 3	0
	3GIO_PADCFG 2	0
	3GIO_PADCFG 1	0
	3GIO_PADCFG 0	1
STRAP2	PCI_DEVID3	0
	PCI_DEVID2	0
	PCI_DEVID1	0
	PCI_DEVID0	0
ROM_SCLK	PCI DEVID 4	1
	SUBVENDOR	0
	SLOT_CLK	1
	PEX_PLL_EN	0
ROM_SI	RAMCFG 3	0
	RAMCFG 2	0
	RAMCFG 1	0
	RAMCFG 0	0
ROM_SO	XCLK_417	1
	FB_0_BAR_SIZE	0
	SMB_ALT_ADDR	0
	VGA_DEVICE	0

SM BUS define resolution 1111

PUN-04992-001-V01
NOTEBOOK 0001

0X0A70 0000
NB11M-GE2

VBIOS is in system bios
GPU and MCH do not share a common clock
disable pci express PLL termination

SEE PUN update 1130

Have 27M hz CRYSTAL

SPEC have no TV function

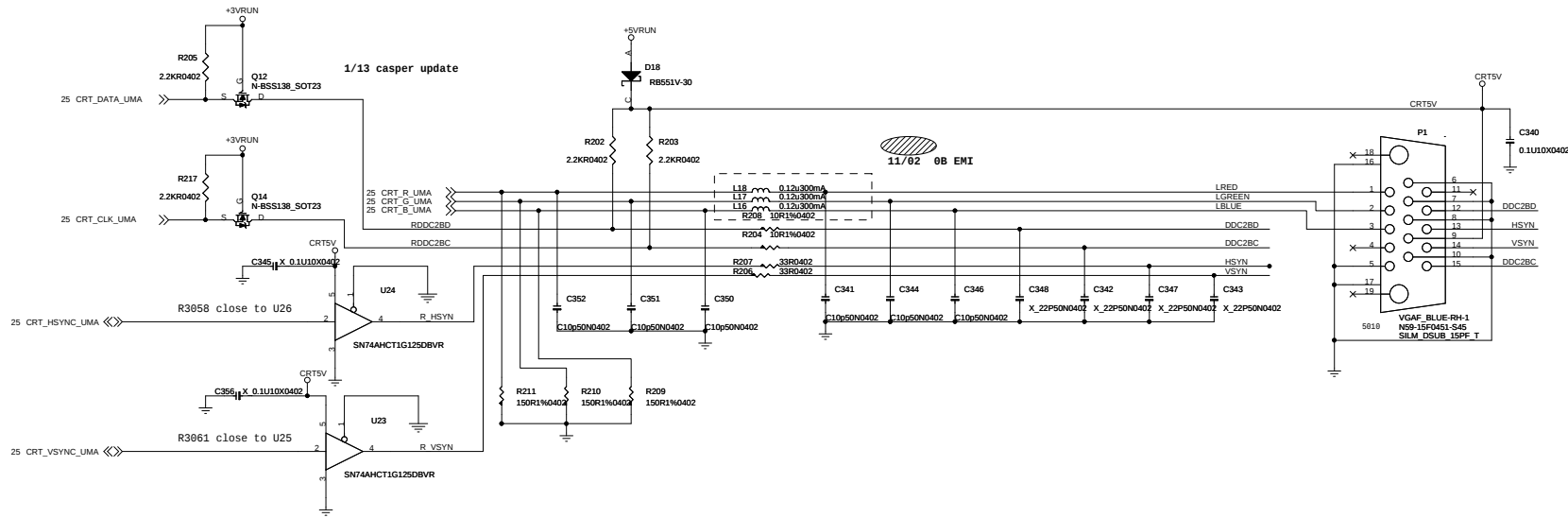
Rvalue	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

 MICRO-STAR INT'L CO.,LTD.

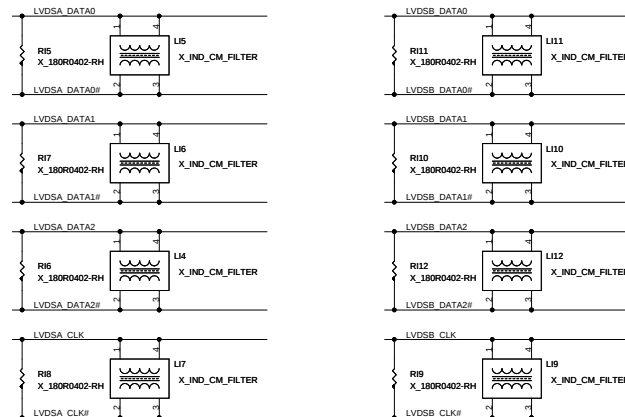
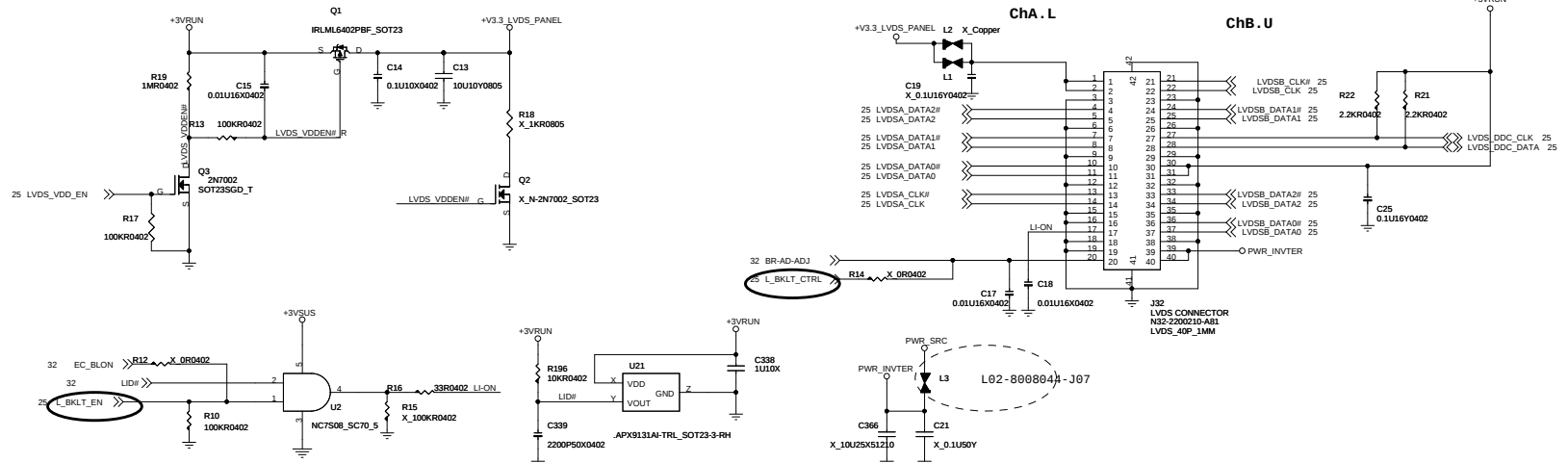
TitlePARK MEM DDR3 A1

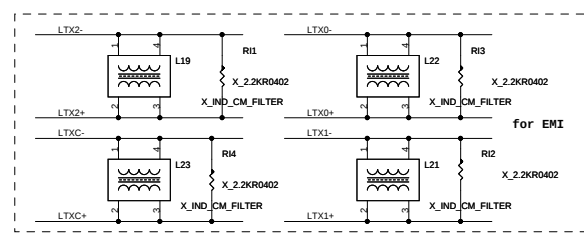
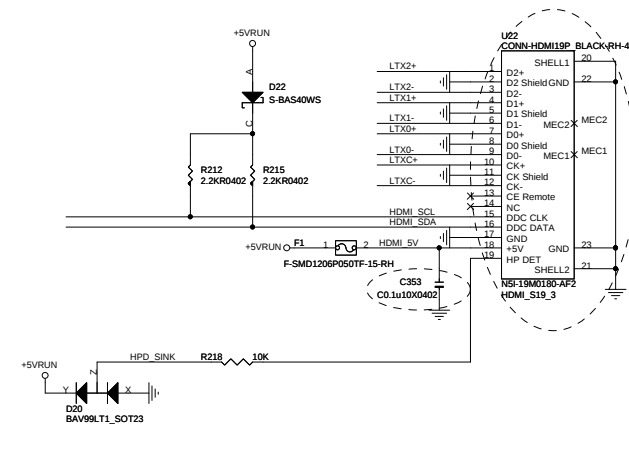
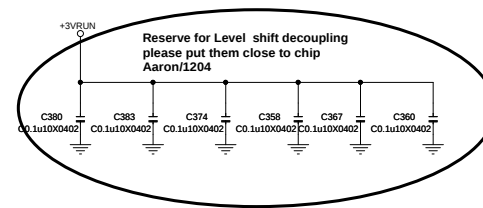
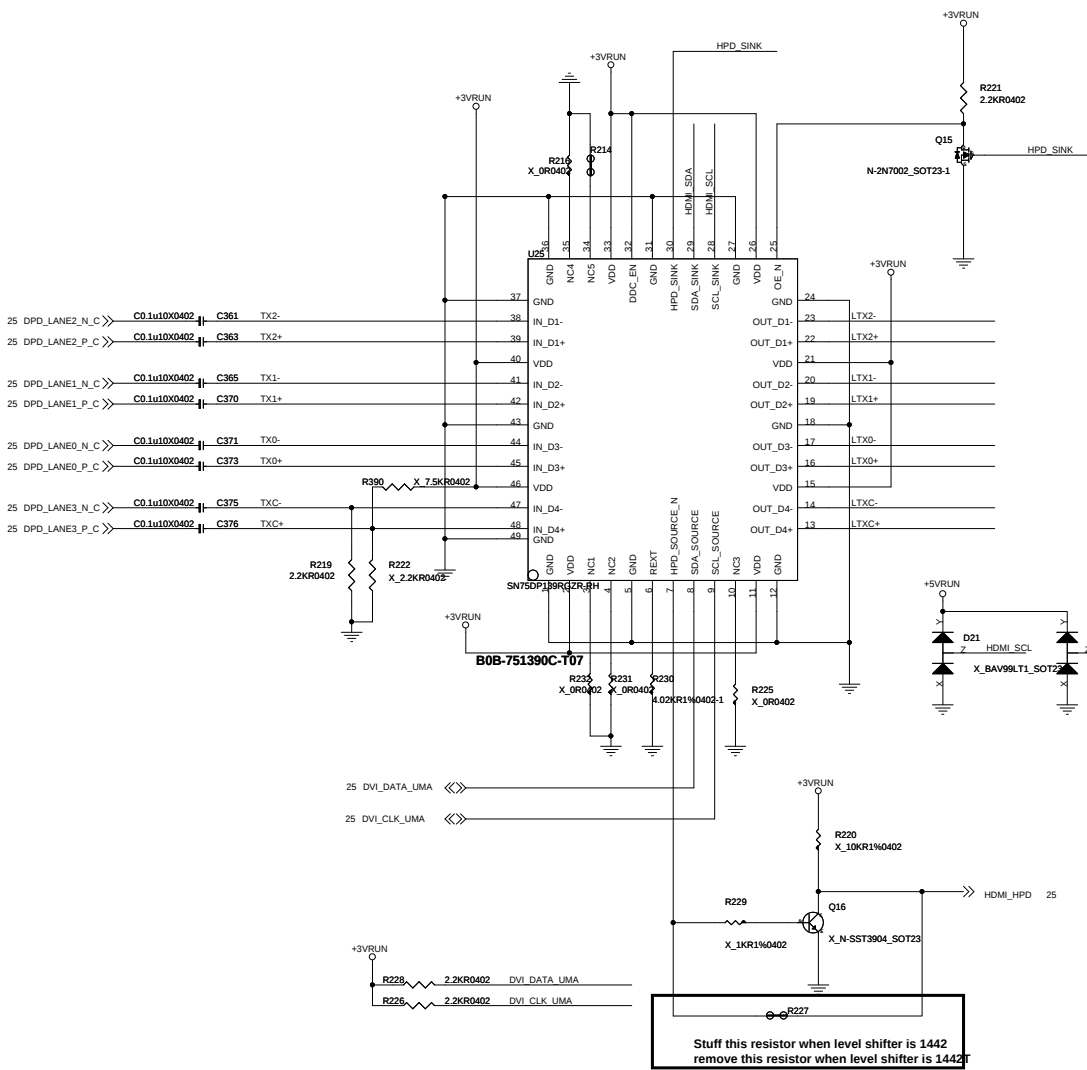
Size BDocument NumberMS-168ARev 0A

Date: Friday, March 26, 2010Sheet 19 of 52

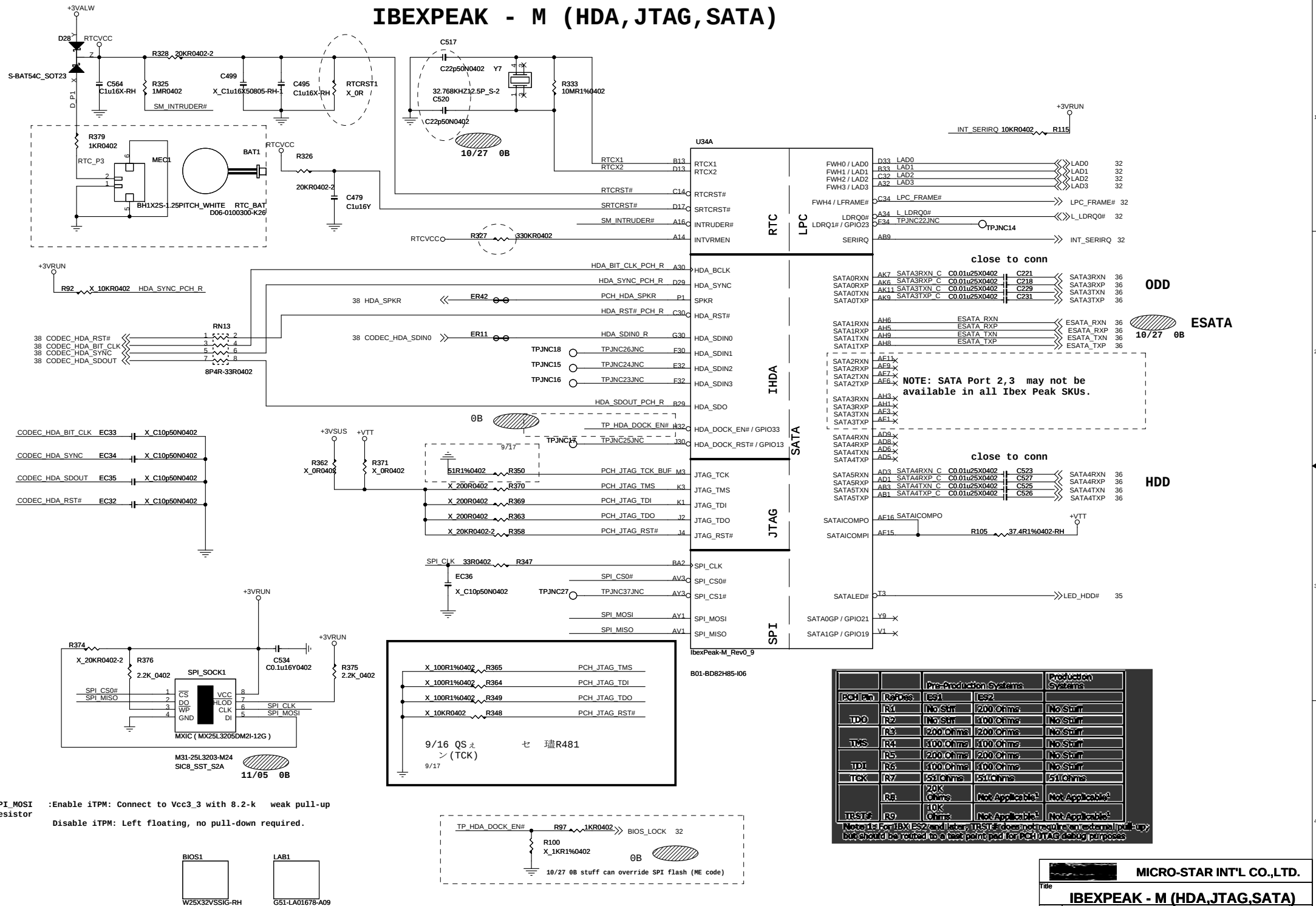


LVDS connector





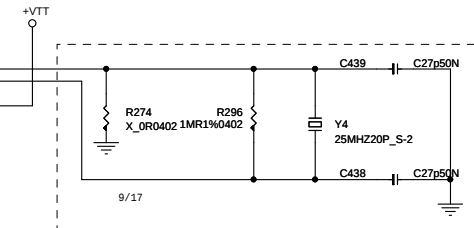
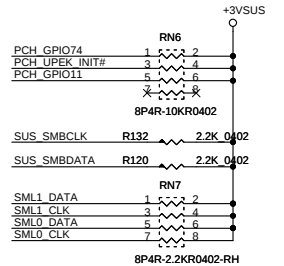
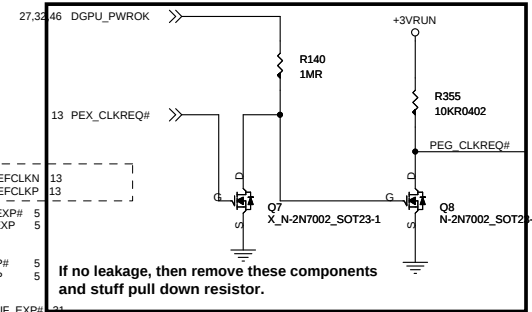
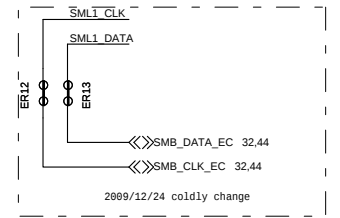
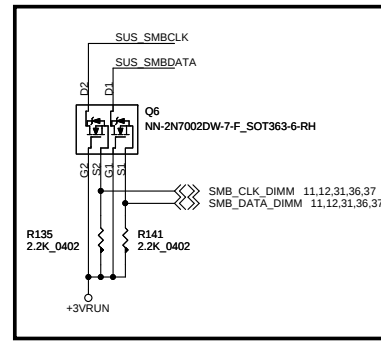
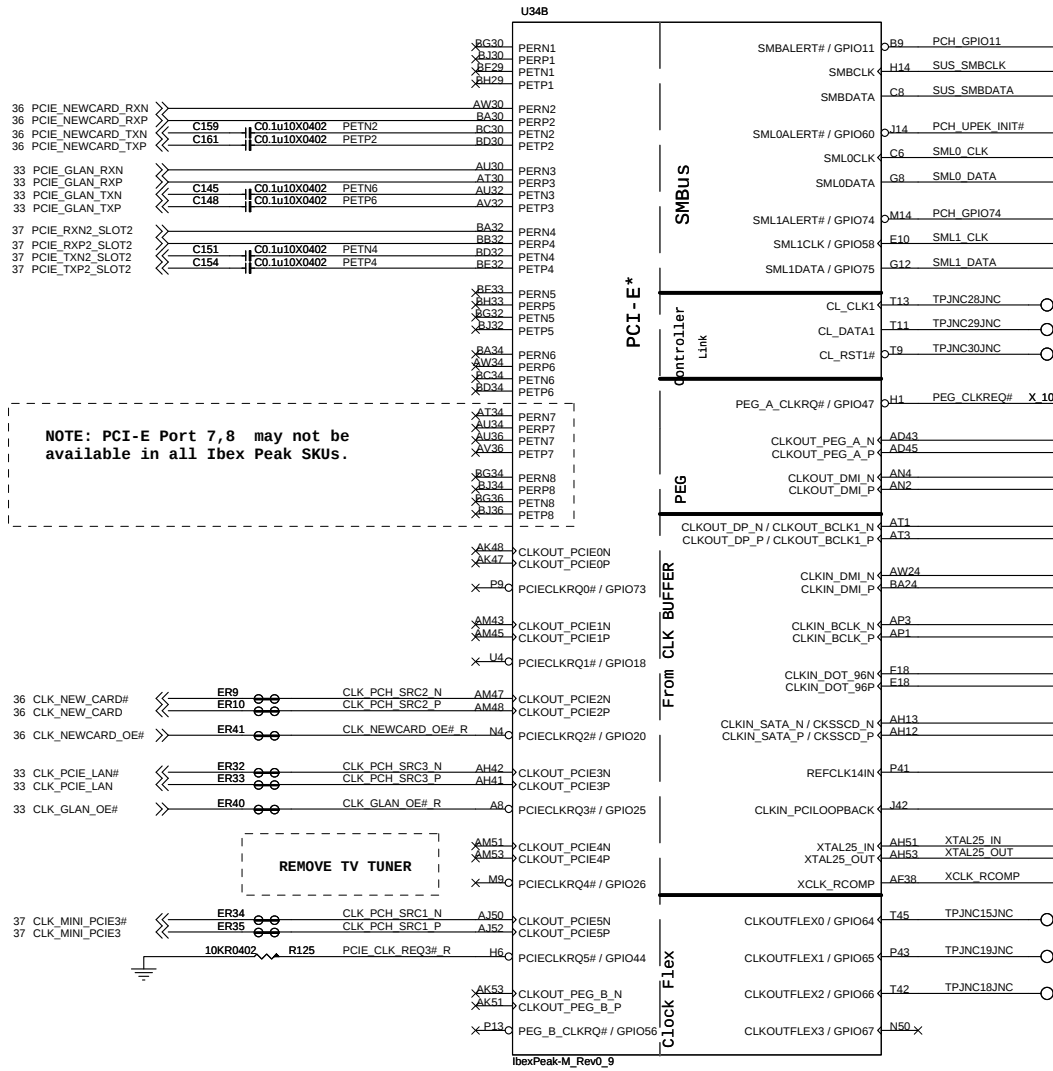
IBEXPEAK - M (HDA, JTAG, SATA)



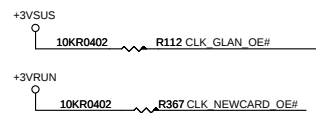
		Pre-Production Systems		Production Systems
POH Pin	RefDes	ES1	ES2	
TD0	R1	No Stn	200 Ohms	No Stn
	R2	No Stn	100 Ohms	No Stn
	R3	200 Ohms	200 Ohms	No Stn
TMS	R4	100 Ohms	100 Ohms	No Stn
	R5	200 Ohms	200 Ohms	No Stn
TD1	R6	100 Ohms	100 Ohms	No Stn
TCK	R7	551 Ohms	551 Ohms	551 Ohms
	R8	20K Ohms	Not Applicable ¹	Not Applicable ²
	R9	10K Ohms	Not Applicable ¹	Not Applicable ²

Notes: 1 For TBX ES2 and later, TRST# does not require an external pull-up but should be routed to a test point pad for PCB UTAG debug purposes

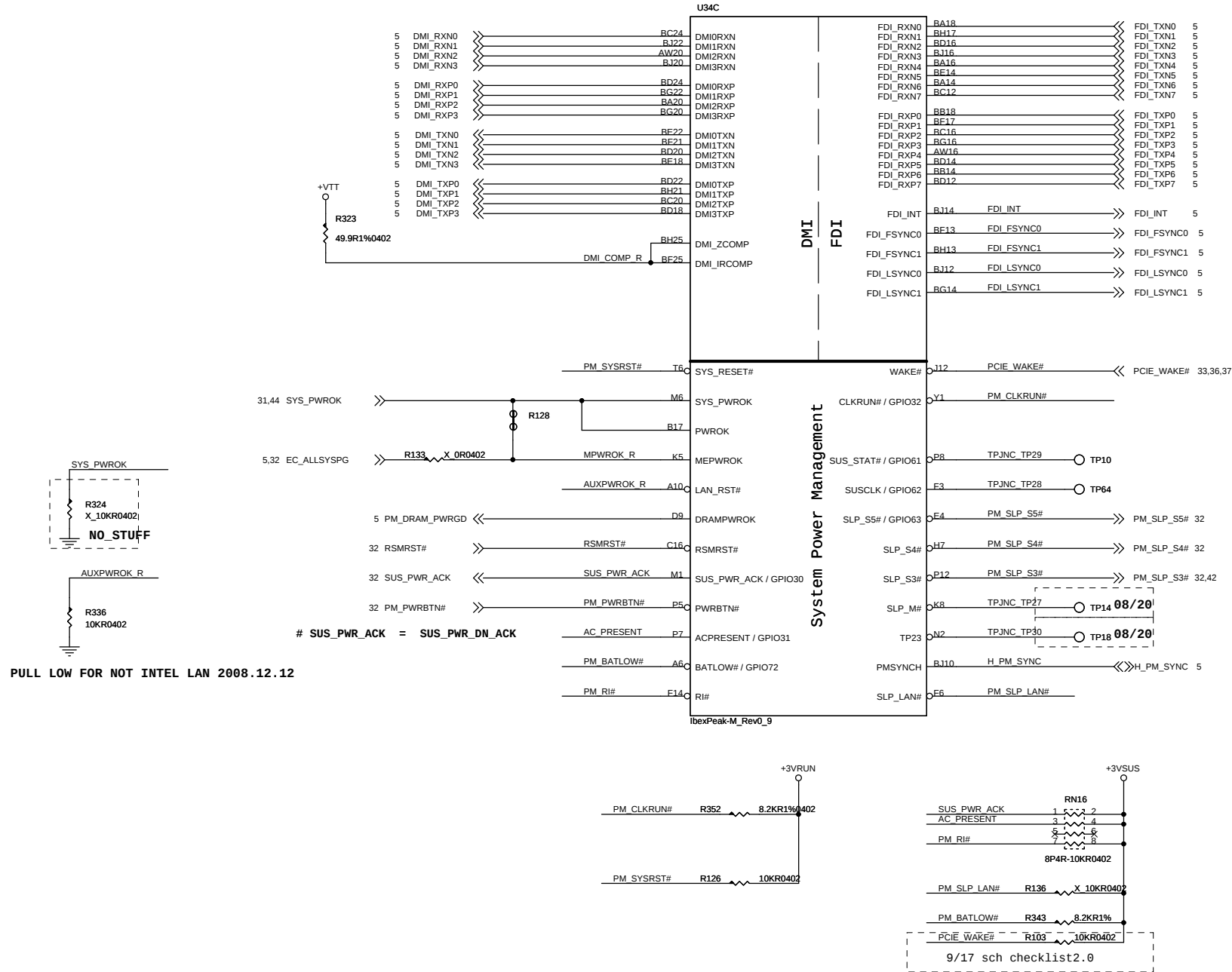
IBEXPEAK - M (PCI-E, SMBUS, CLK)



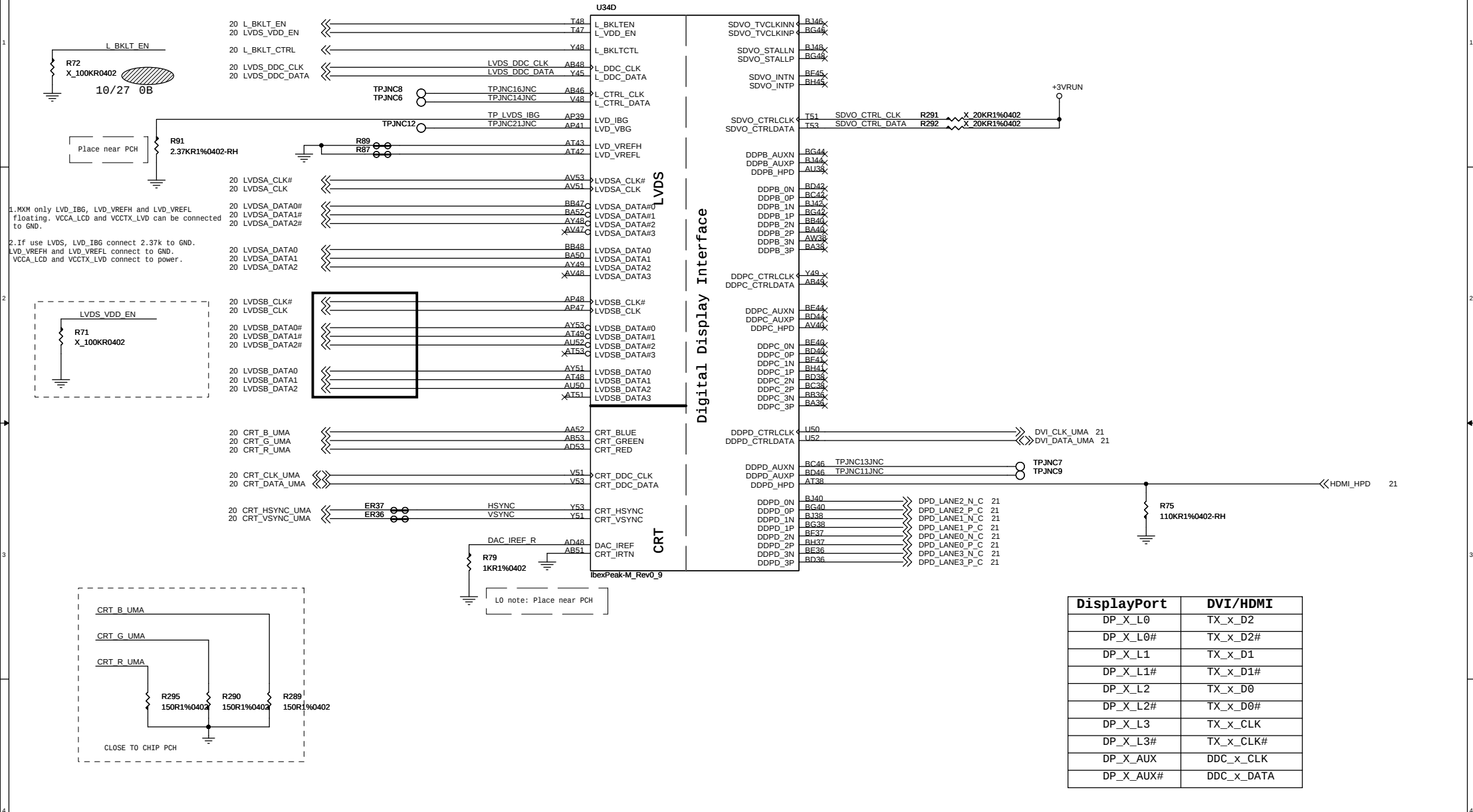
PCIECLKRQ1# / GPIO18 PCIECLKRQ1# / GPIO20	RUN Well
PCIECLKRQ0# and PCIECLKRQ3# ~ PCIECLKRQ7# PEG_A_CLKRQ# PEG_B_CLKRQ#	SUS Well



IBEXPEAK - M (DMI, FDI, GPIO)



IBEXPEAK - M (LVDS, DDI)

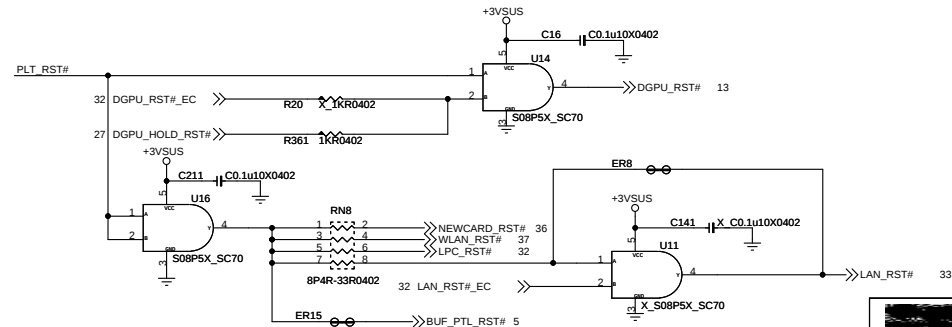
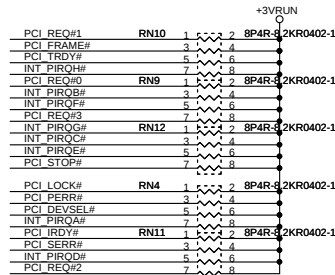
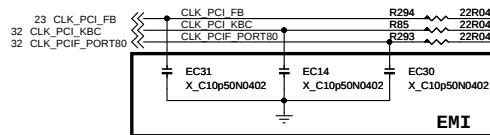
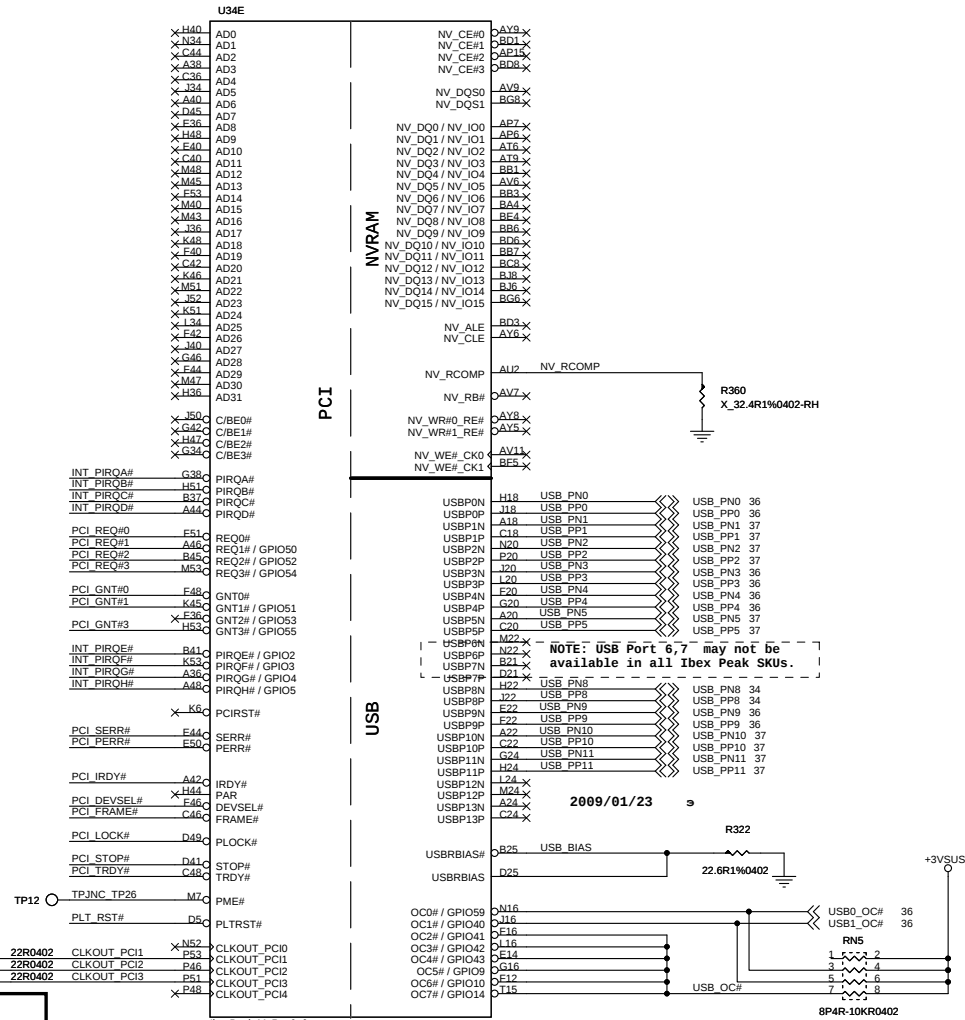
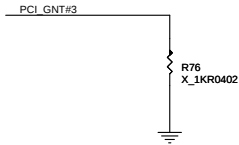
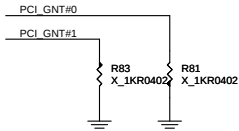


DisplayPort	DVI/HDMI
DP_X_L0	TX_x_D2
DP_X_L0#	TX_x_D2#
DP_X_L1	TX_x_D1
DP_X_L1#	TX_x_D1#
DP_X_L2	TX_x_D0
DP_X_L2#	TX_x_D0#
DP_X_L3	TX_x_CLK
DP_X_L3#	TX_x_CLK#
DP_X_AUX	DDC_x_CLK
DP_X_AUX#	DDC_x_DATA

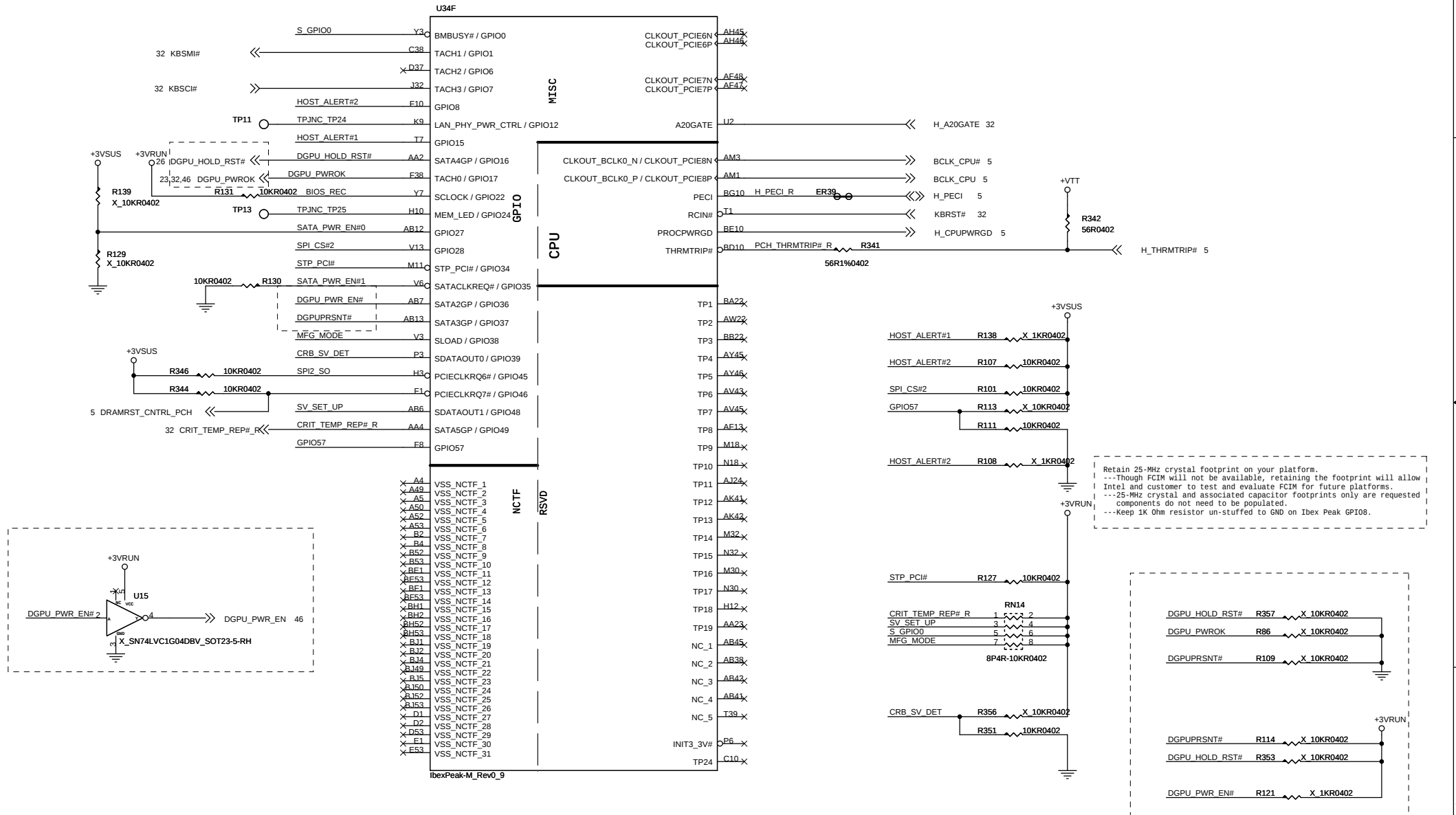
IBEXPEAK - M (PCI, USB, NVRAM)

Boot BIOS Strap		
PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI

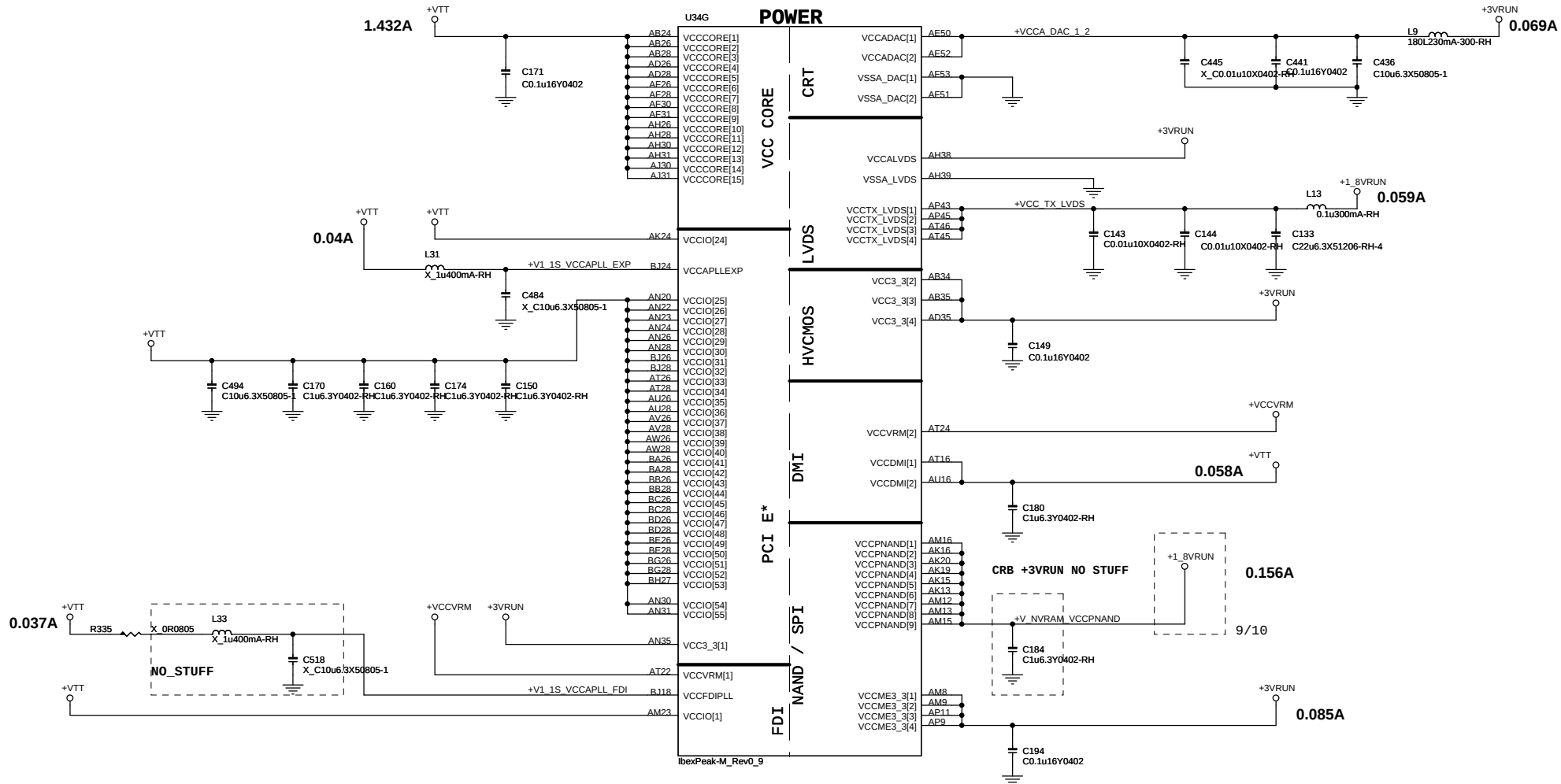
A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default



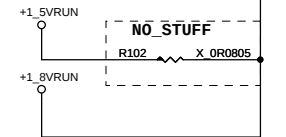
IBEXPEAK - M (GPIO, VSS_NCTF, RSVD)



IBEXPEAK - M (POWER)

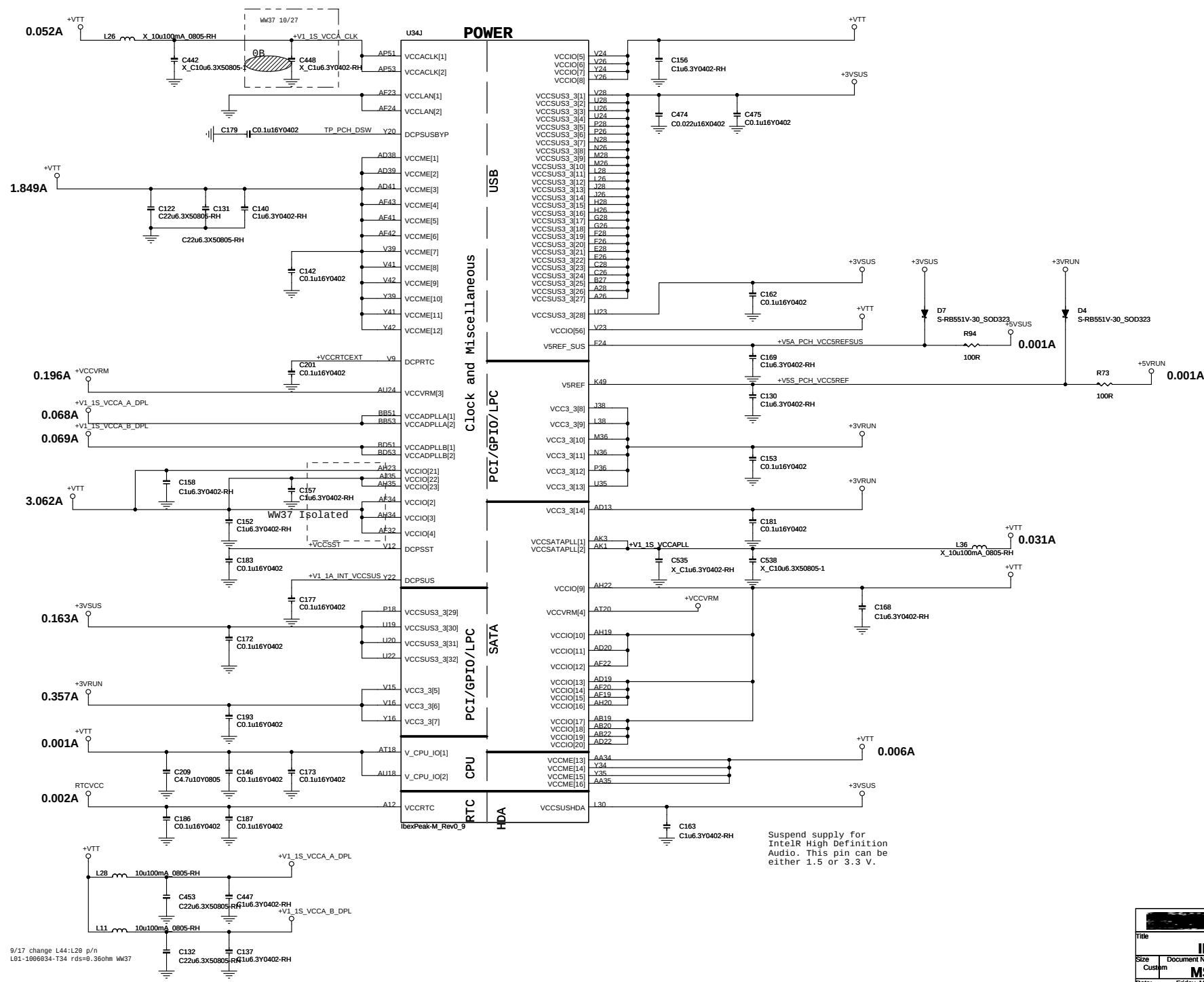


The VCCVPM rail (1.8 V/1.5 V) powers an internal voltage regulator module (VRM) that regulates clean 1.05-V voltage supply for analog rails (VCCACLK, VCCAPLLEX, VCCFDIPLL, and VCCSATAPLL). This solution will allow us to remove the LC filter requirements for those rails, thereby reducing platform BOM cost. VCCVPM is enabled by default via internal pull up to GPIO27, therefore GPIO27 should be left as No Connect. The following diagram shows implementation details on how to enable and disable VccVRM.



VccLAN may be grounded if Intel LAN is disabled.

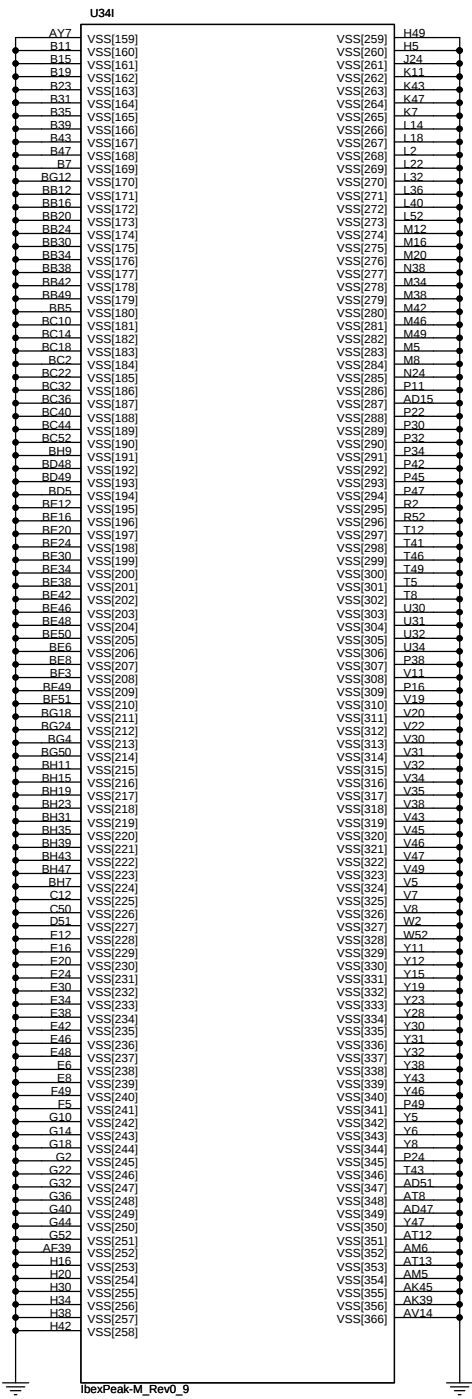
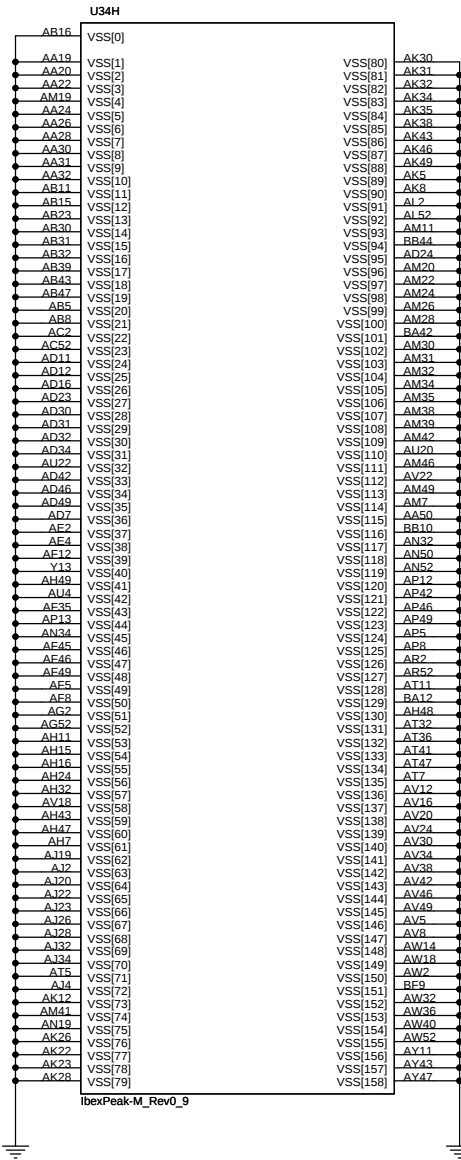
IBEXPEAK - M (POWER)



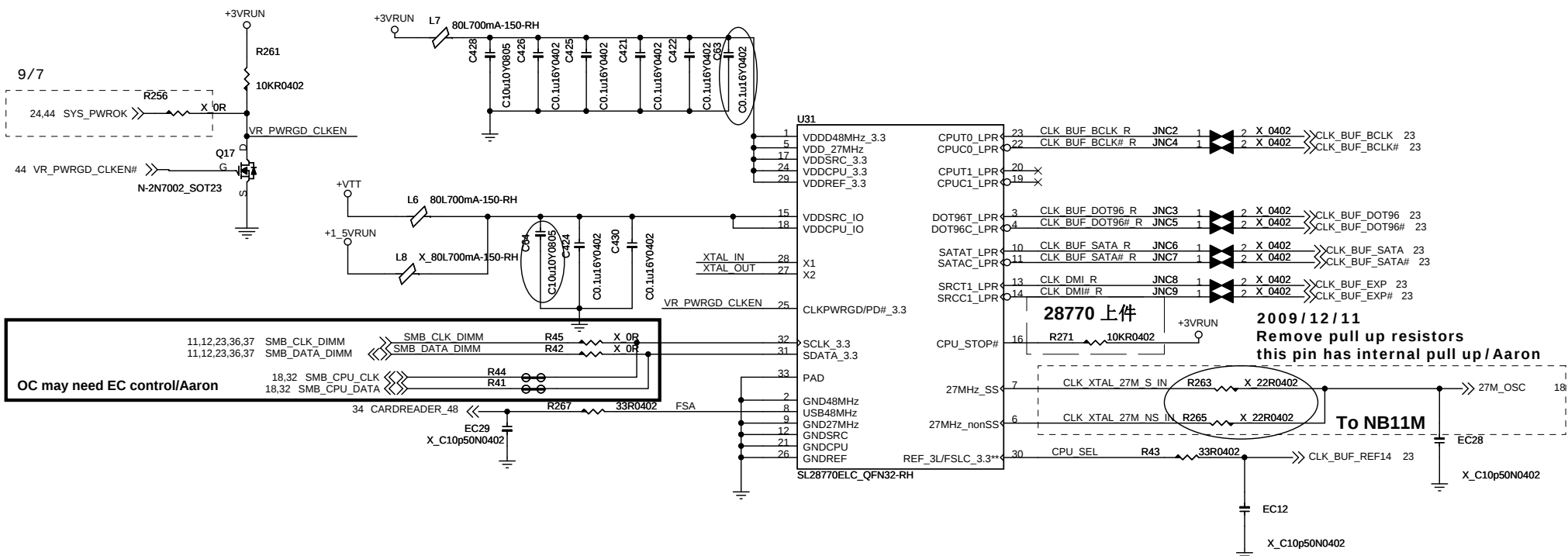
9/17 change L44:L20 p/n
L01-1006034-T34 rds=0.36ohm WW37

Suspend supply for
Intel High Definition
Audio. This pin can be
either 1.5 or 3.3 V.

IBEXPEAK - M (GND)

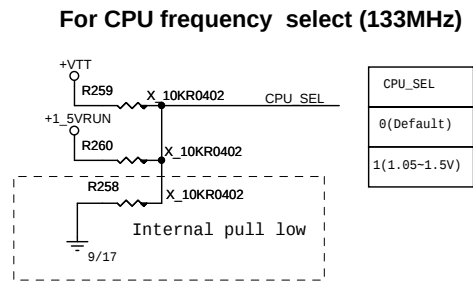
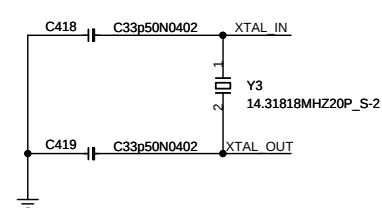


			MICRO-STAR INT'L CO.,LTD.		
Title					
IBEXPEAK - M (GND)					
Size	Document Number				Rev
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Date:	Friday, March 26, 2010		Sheet	30	of 52



OC may need EC control/Aaron

Capacity select
If LC=20pf C708/C709=33pf
If LC=32pf C708/C709=56pf



Co-Lay Note:

For IDT IC9IRS3199
R84,R73,R71=10Kohm

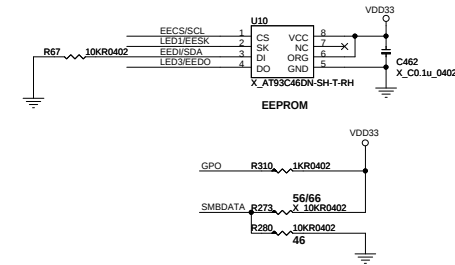
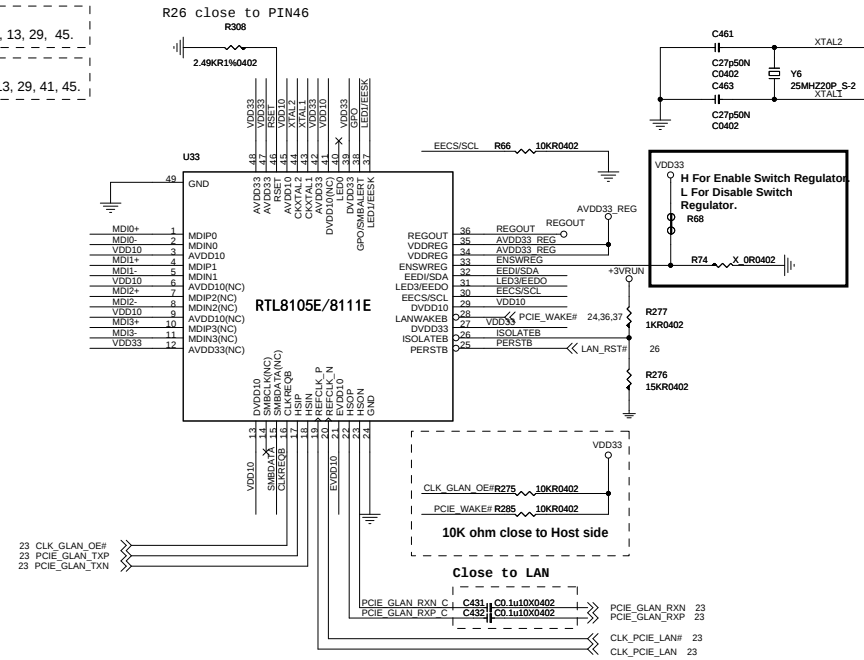
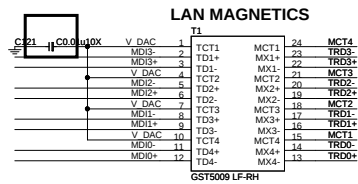
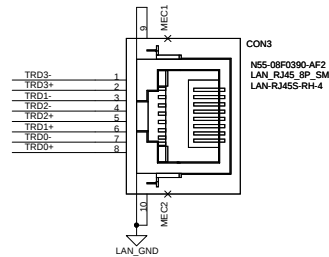
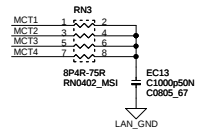
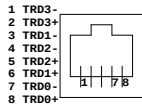
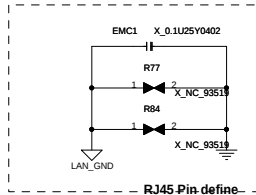
For Silego SLG8SP587
R84,R73,R600=4.7Kohm

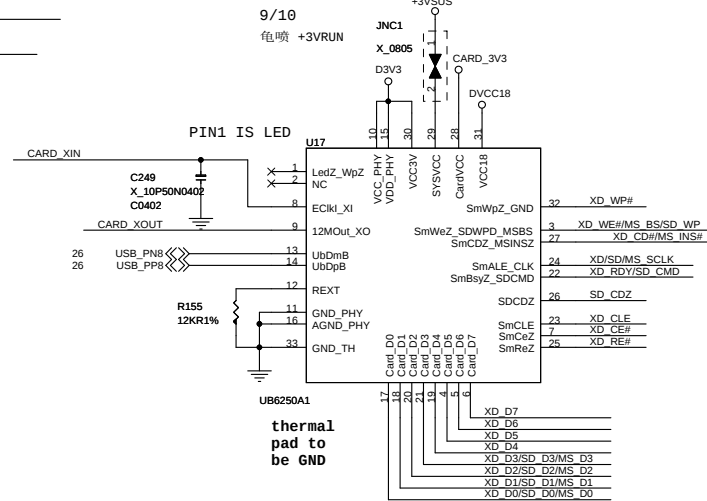
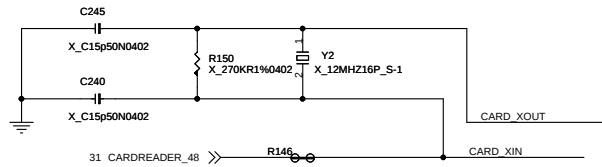
CPU_SEL	CPU0	CPU1
0(Default)	133MHz	133MHz
1(1.05-1.5V)	100MHz	100MHz

Need to modify L1 P/N to 2.2uH.

For RTL8105E
* C3 to C6 are for VDD10 pins-- 3, 13, 29, 45.

For RTL8111E
* C3 to C9 are for VDD10 pins-- 3, 6, 9, 13, 29, 41, 45.

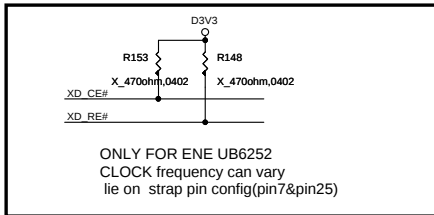




ENE UB6250 USB20 Flash Card Reader Controller

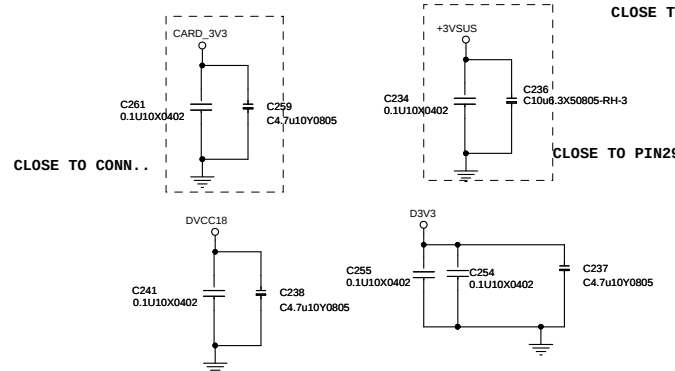
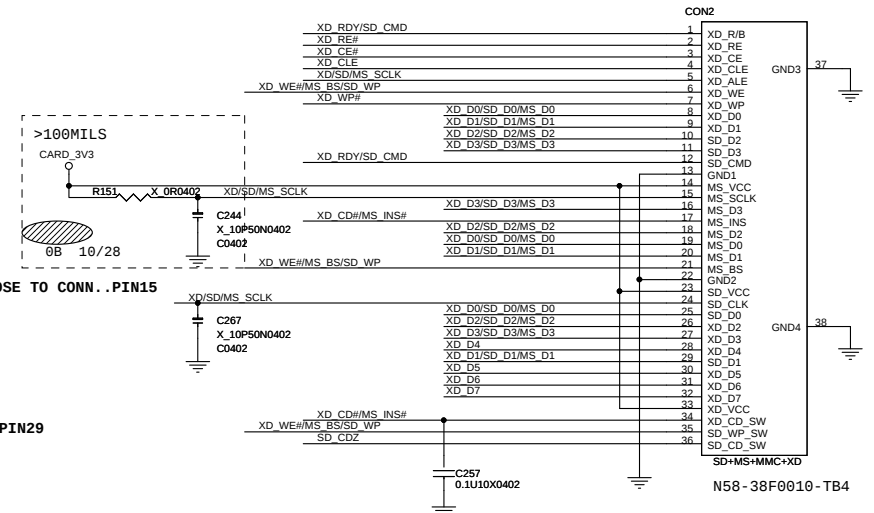
Pins for SD, MMC, MS, and xD memory cards

Name	No	I/O	SD	MMC	MS
xDCEZ	7	O	xD card EN		
xDClE	23	O	xD CMD latch EN		
xDAle	24	O	xD ADDR latch EN		
xDBsyZ	22	B	xD Ready/busy	SD clock	MMC clock
xDData0	17	B	SD D0	MMC D0	MS D0
xDData1	18	B	SD D1	MMC D1	MS D1
xDData2	20	B	SD D2	MMC D2	MS D2
xDData3	21	B	SD D3	MMC D3	MS D3
xDData4	19	B	SD D4	MMC D4	MS D4
xDData5	4	B	SD D5	MMC D5	MS D5
xDData6	6	B	SD D6	MMC D6	MS D6
xDData7	6	B	SD D7	MMC D7	MS D7
xDWeZ	3	B	xD W EN	SD WP	MS Busy
xDReZ	25	O	xD R EN		
xDWpZ	32	O	xD WP		
SDCdZ	26	I	SD CD	MMC CD	
xDCdZ	27	I	xD CD		MS CD



Configurations for Clock Source Selection:

4.7K Pull-high Resistor on		Frequency of external clock source to EClin pin
xDReZ	xDCEZ	
NC	NC	48MHz
NC	O	24MHz
O	NC	12MHz

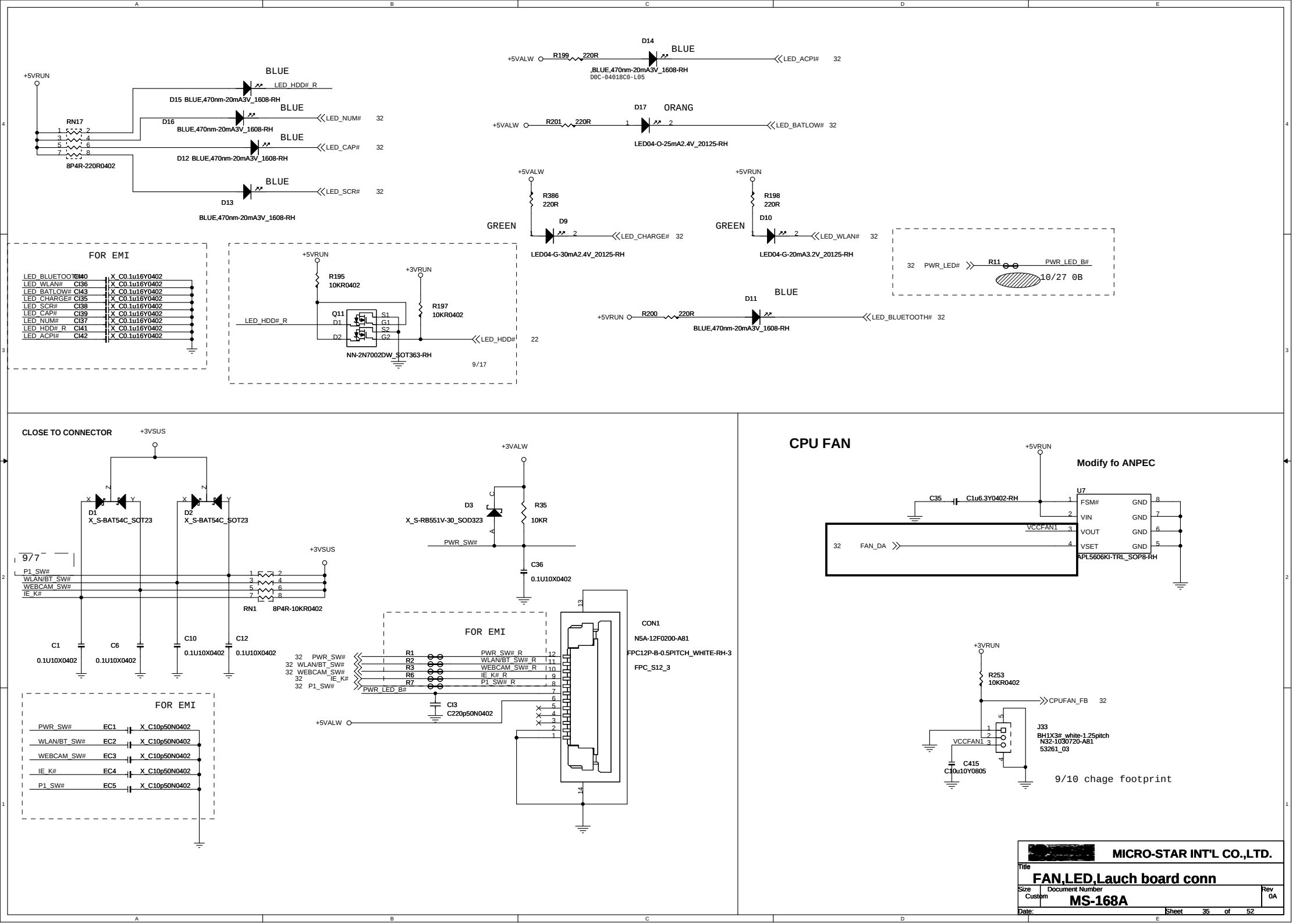


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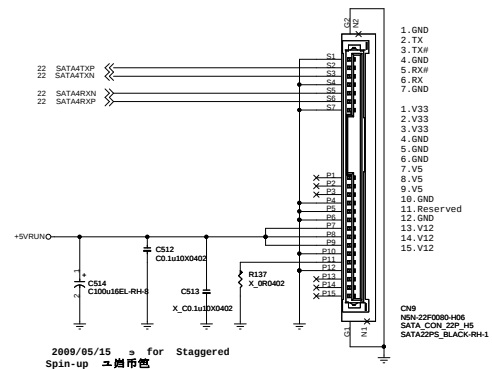
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Size: **Custom** Document Number: **MS-168A** Rev: **0A**

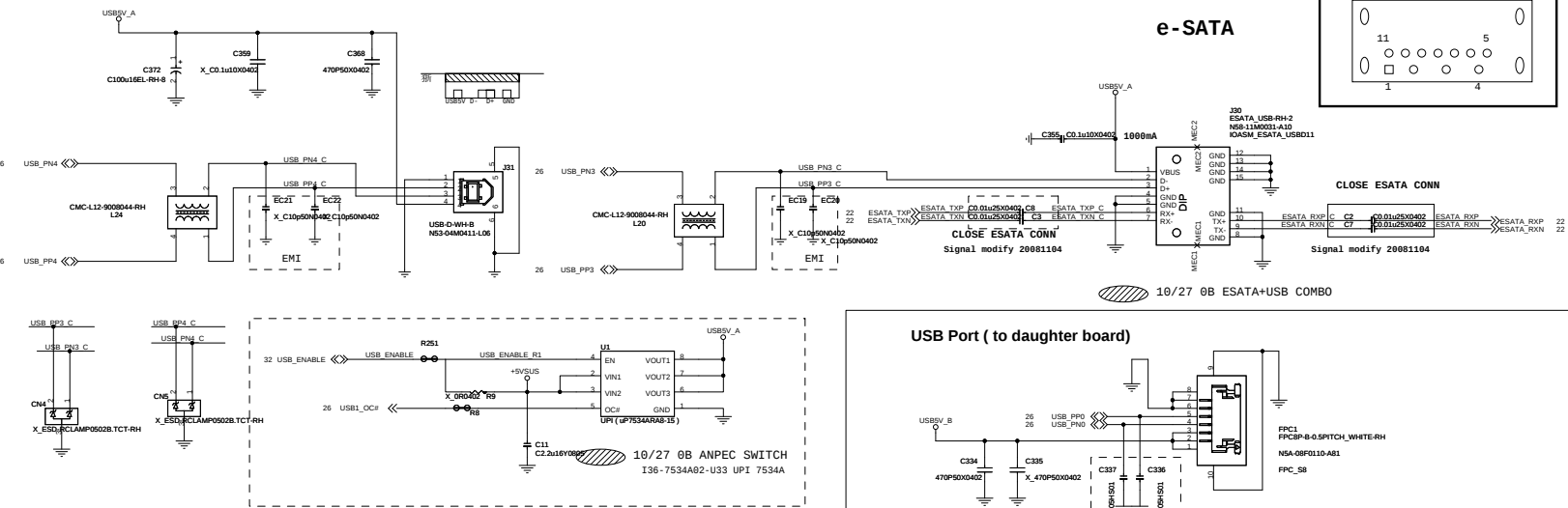
Date: _____ Sheet: **34** of **52**



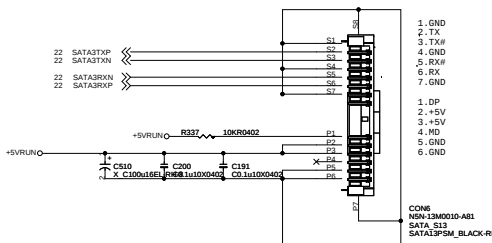
SATA HDD



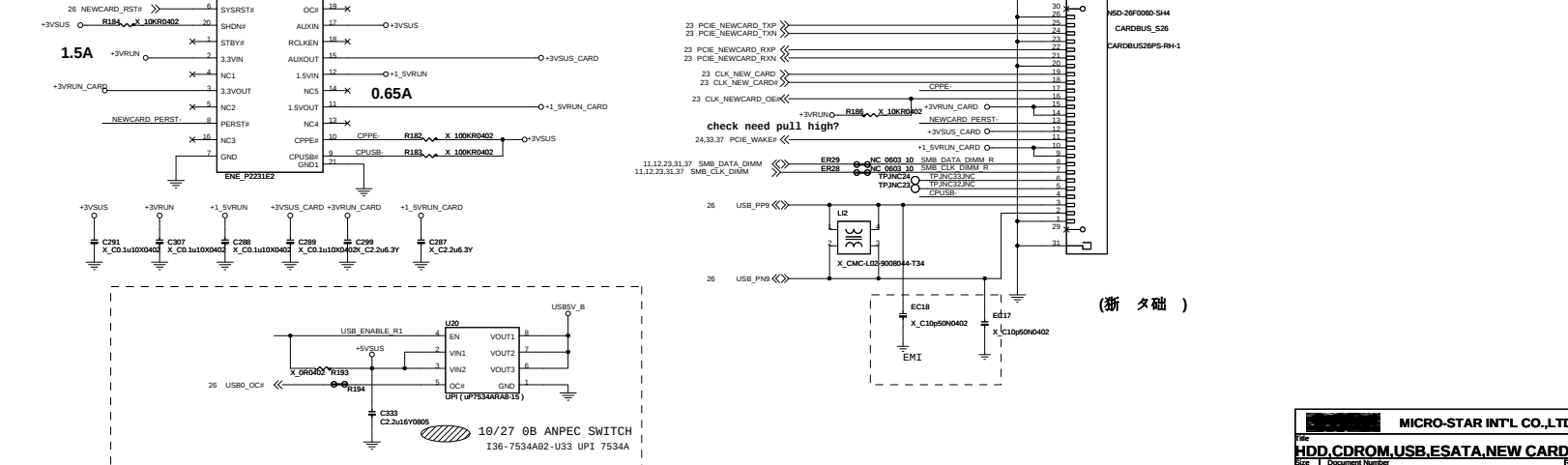
USB Port



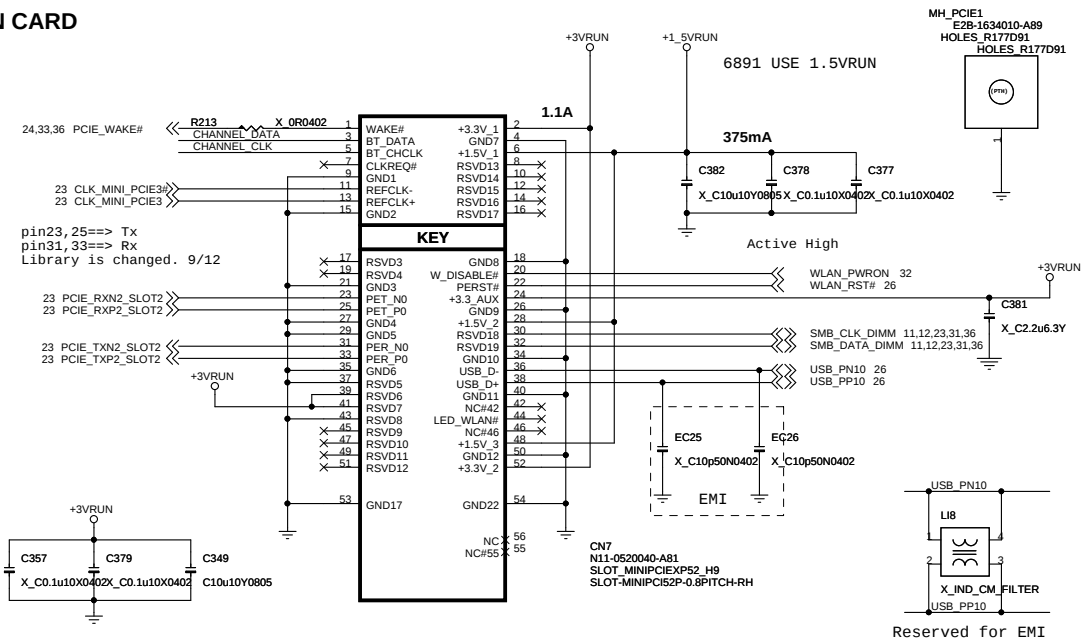
SATA ODD



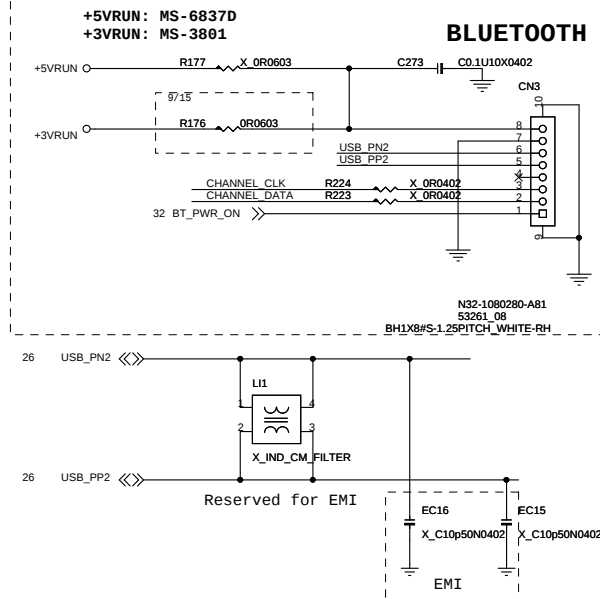
NEW CARD



WLAN CARD

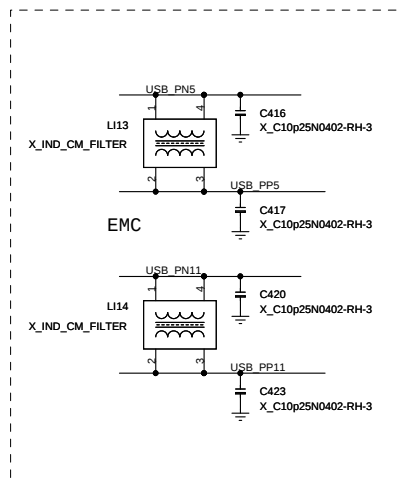
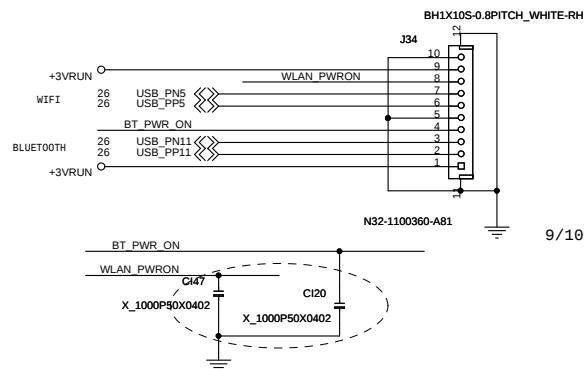


BLUETOOTH

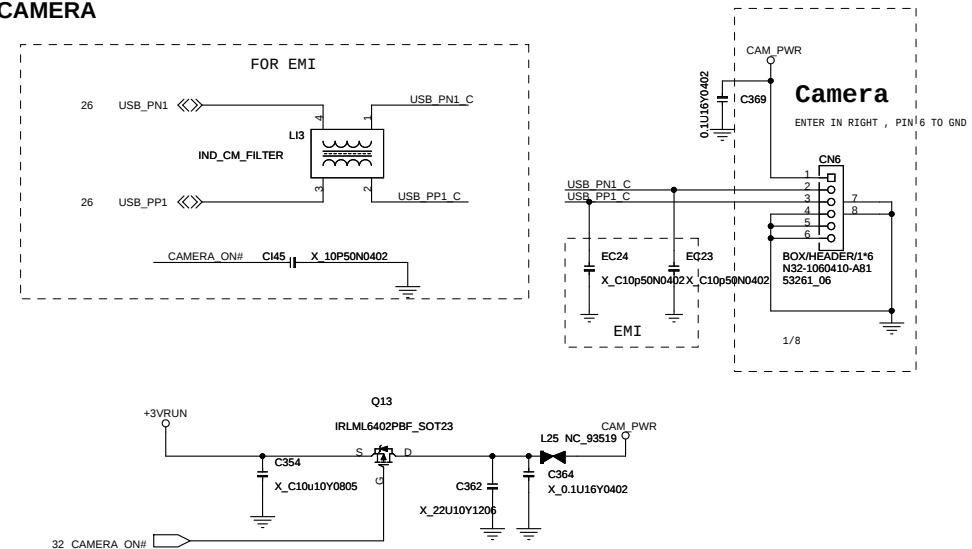


REMOVE TV TUNER

MS-3871



CAMERA

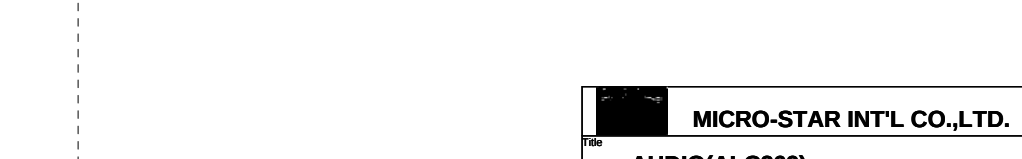
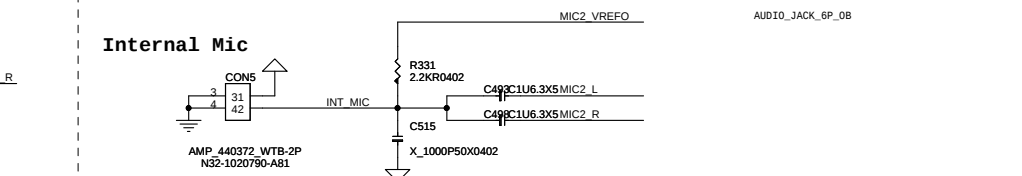
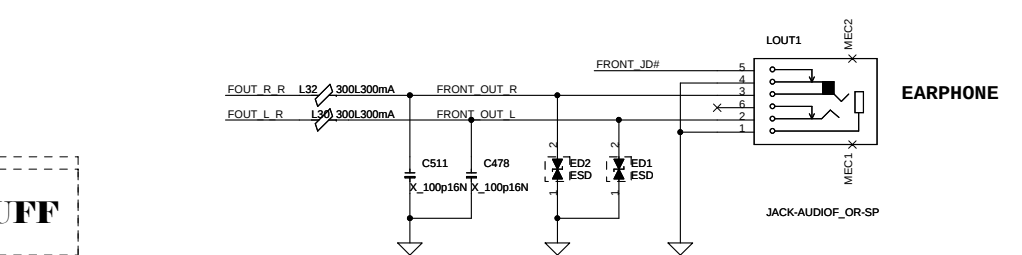
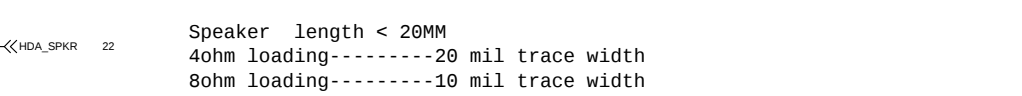
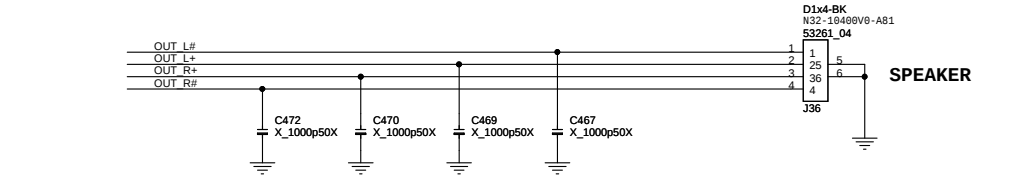
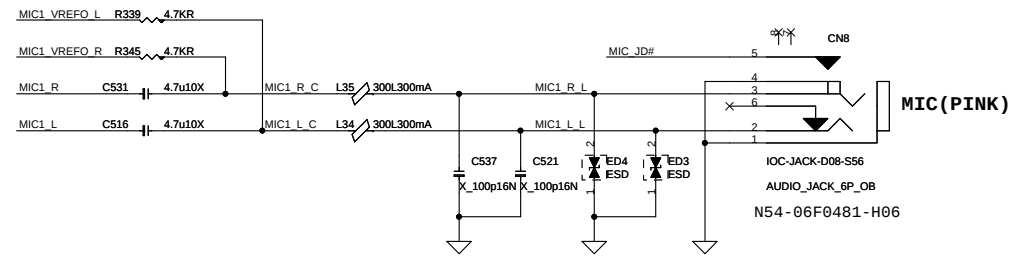
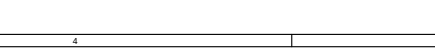
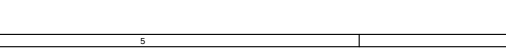
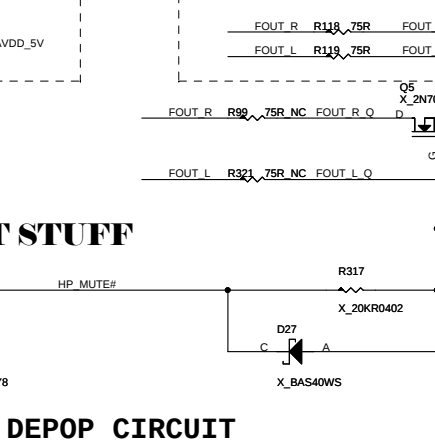
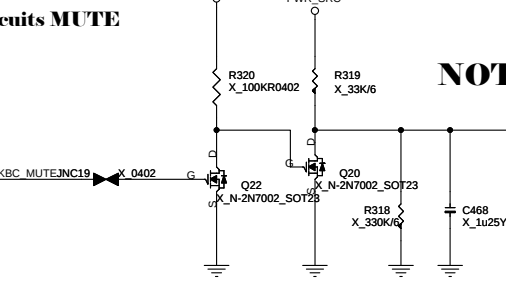
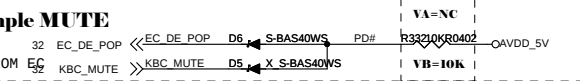
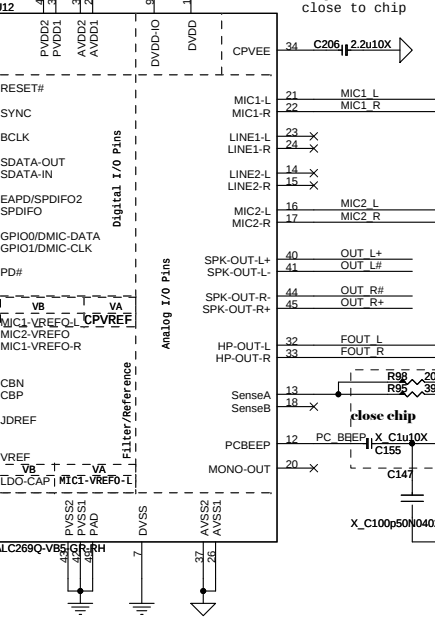
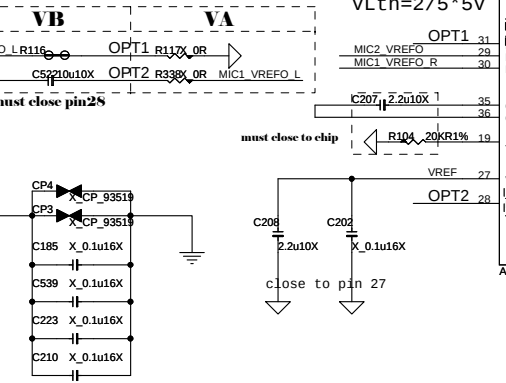
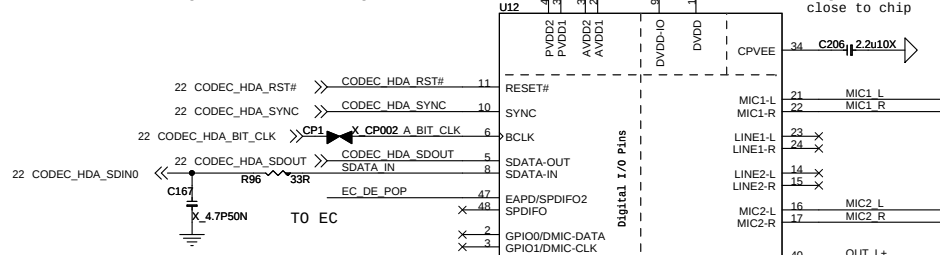
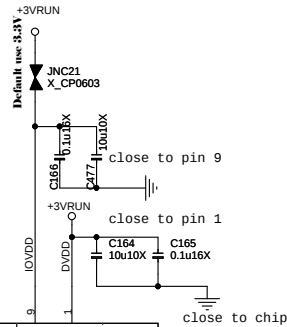
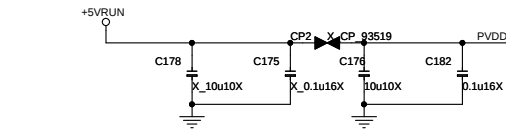
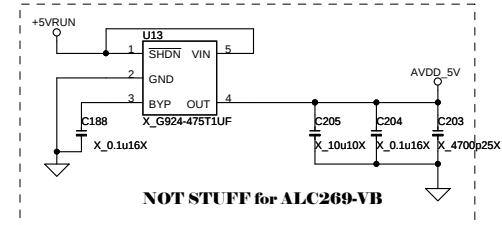
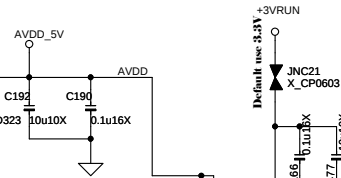
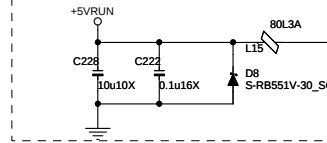


MSI CORPORATION

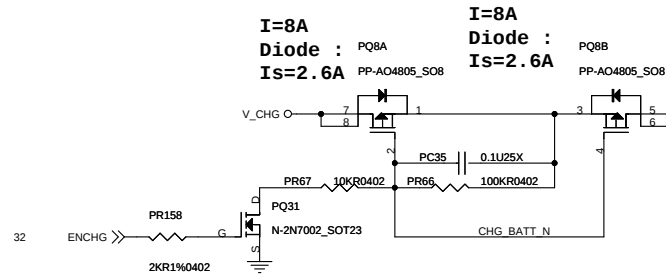
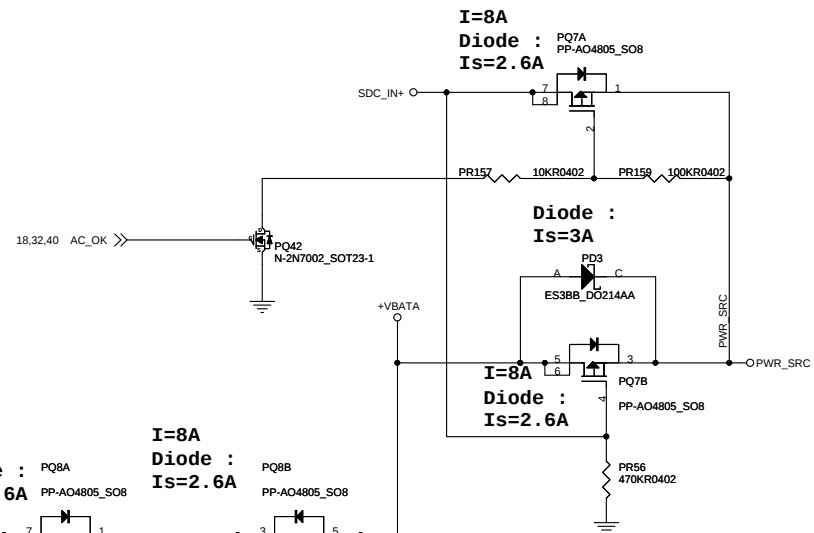
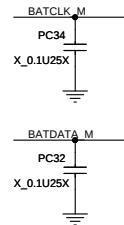
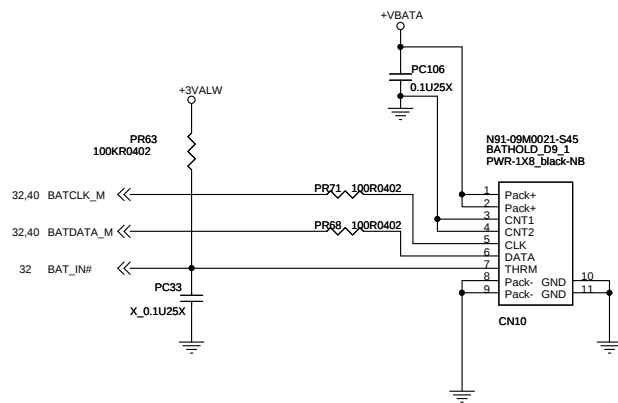
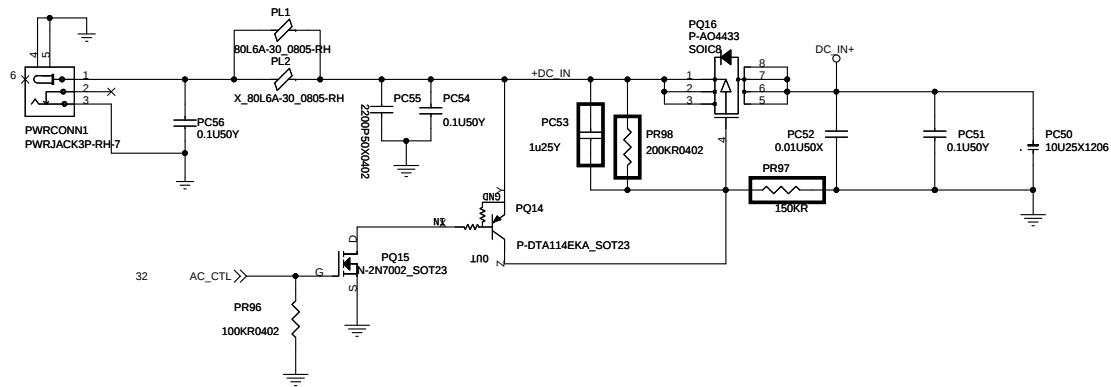
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Size	Document Number	Rev
Custom	MS-168A	0A
Date:	Friday, March 26, 2010	Sheet 37 of 52

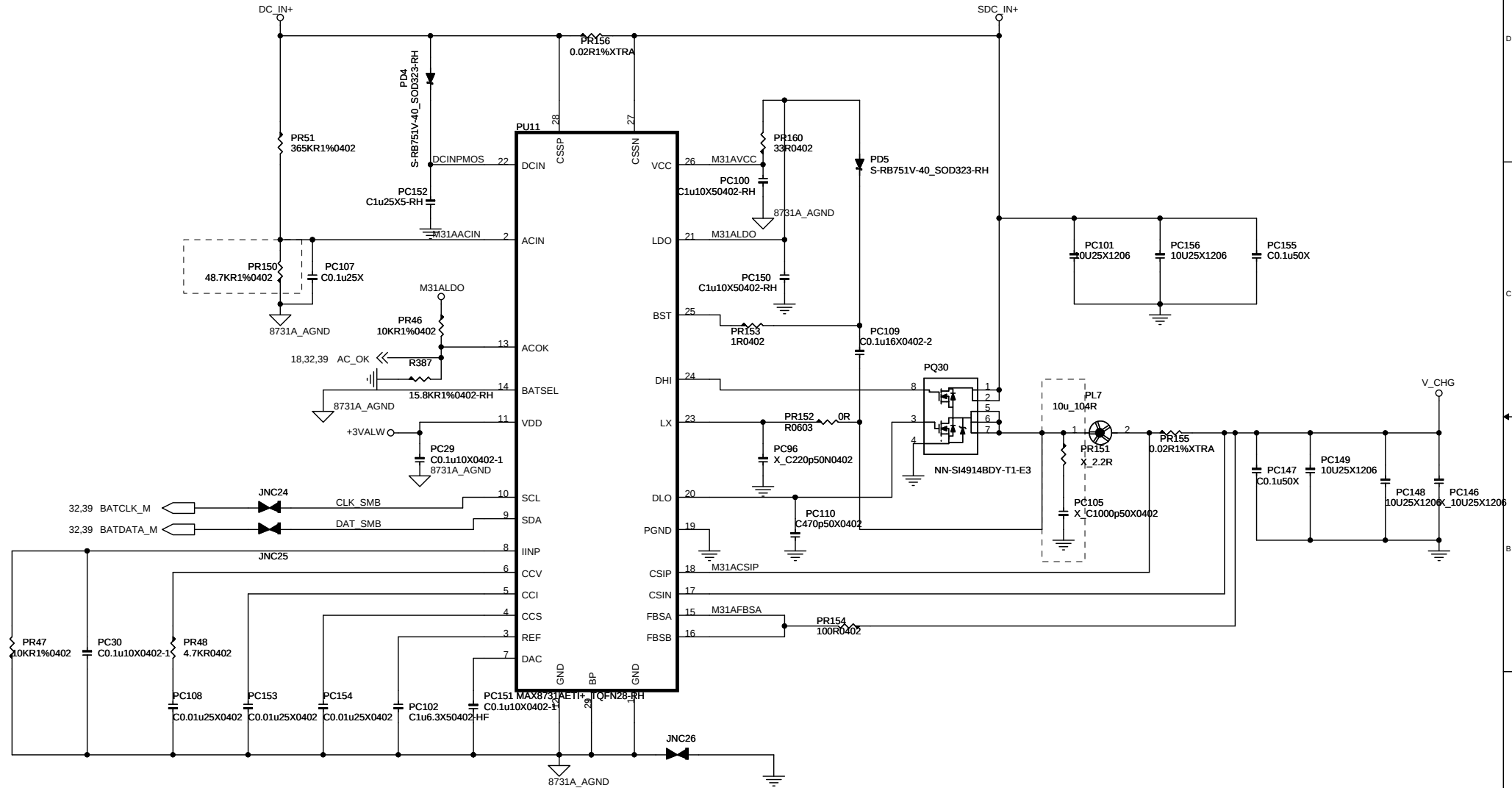
FOR ALC269-VB have internal LDO



Title		MICRO-STAR INT'L CO.,LTD.	
Size		Document Number	
Date		Rev	
Friday, March 26, 2010		0A	
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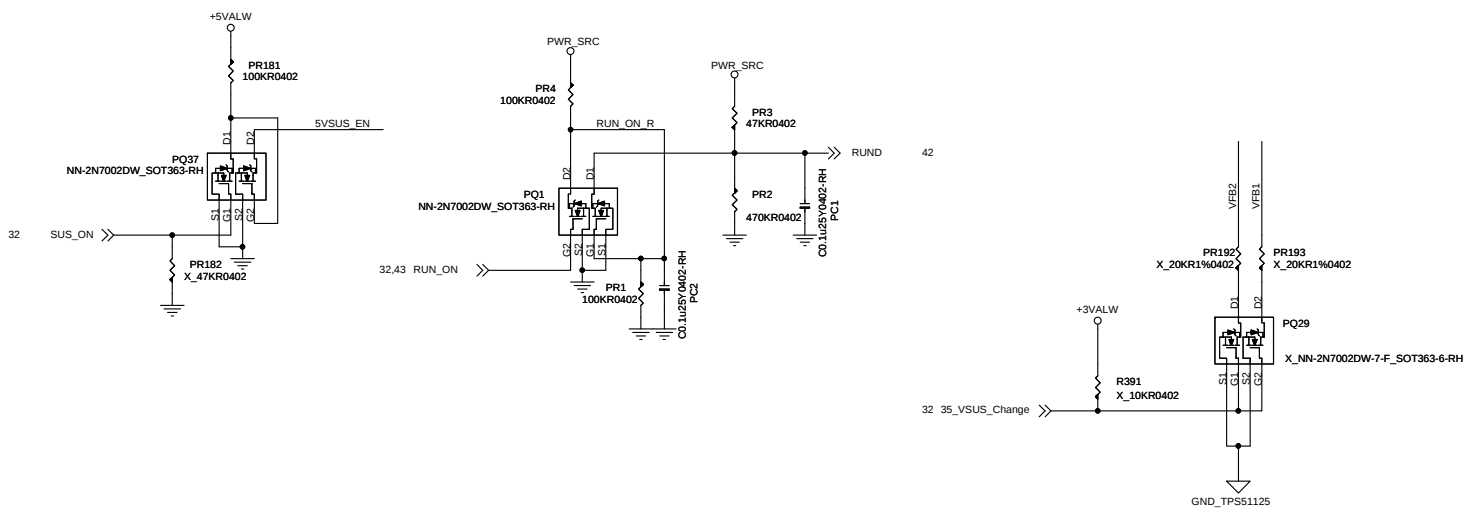
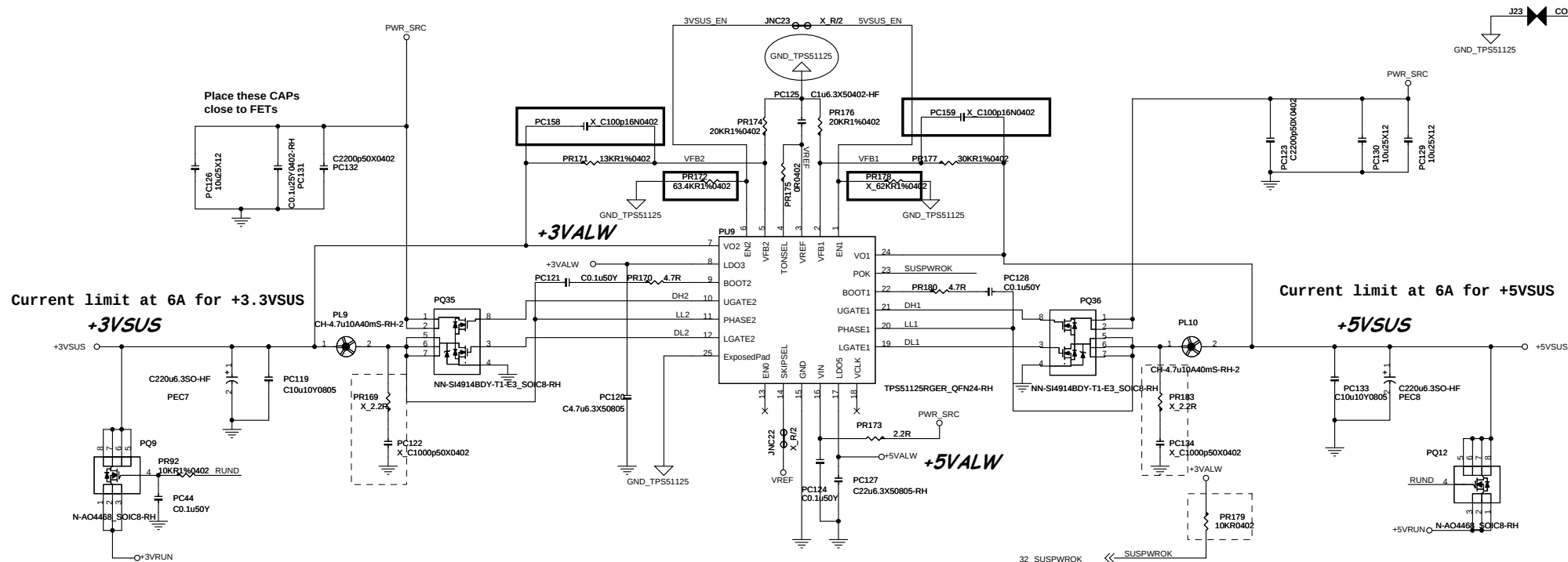
Adapter input voltage set 19 Voltage

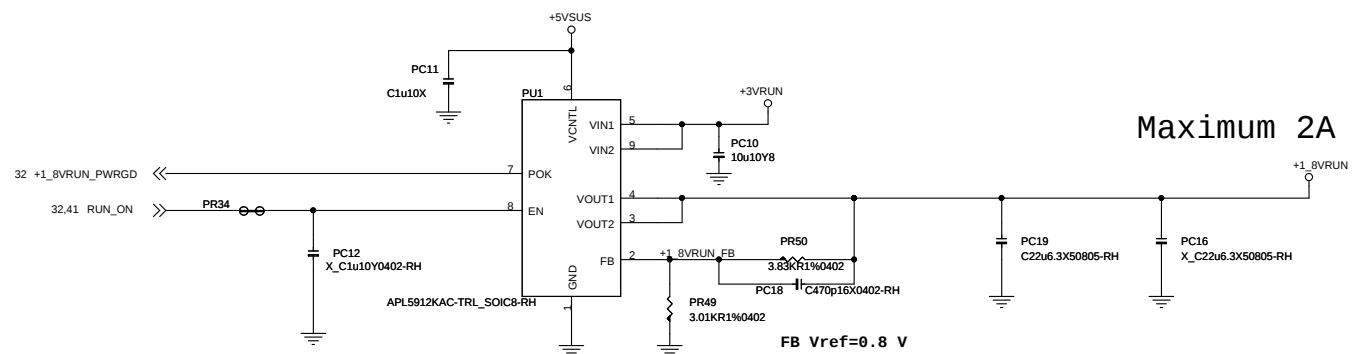
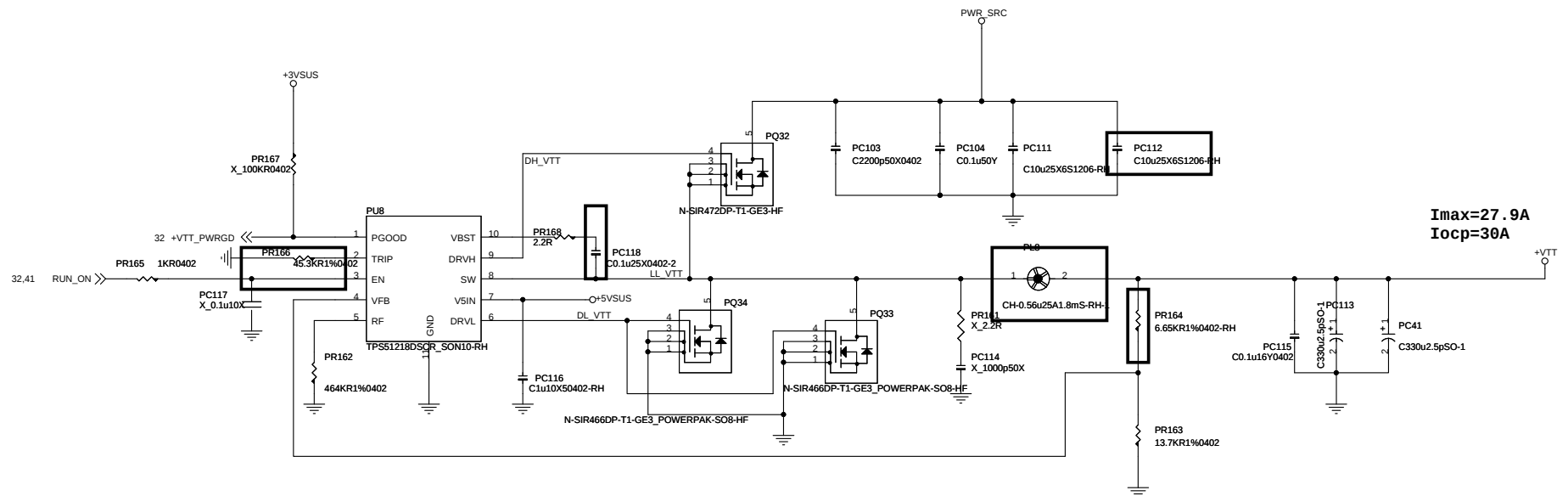


IINP :

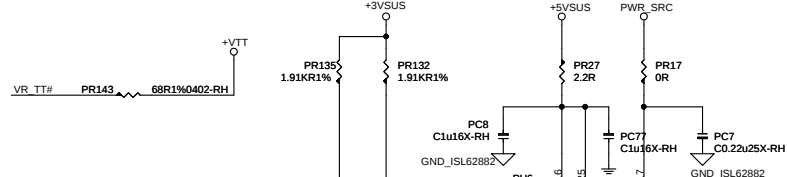
1. The transconductance from (CSSP - CSSN) to IINP is 3mA/V.
2. $V_{IINP} = IINP_{UT} \times RS1 \times 3mA/V \times PR25$

		MICRO-STAR INT'L CO.,LTD.	
Title		Battery Charger	
Size B	Document Number	E51/MQ	
	MS-168A	Rev 0A	
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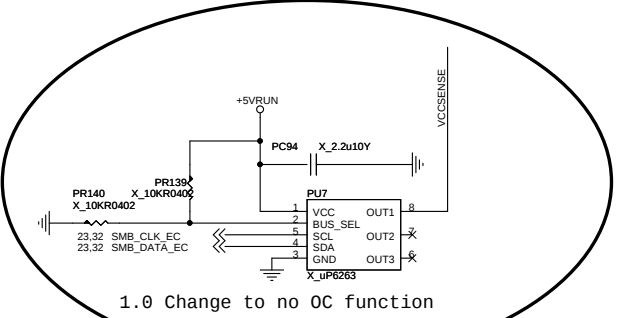
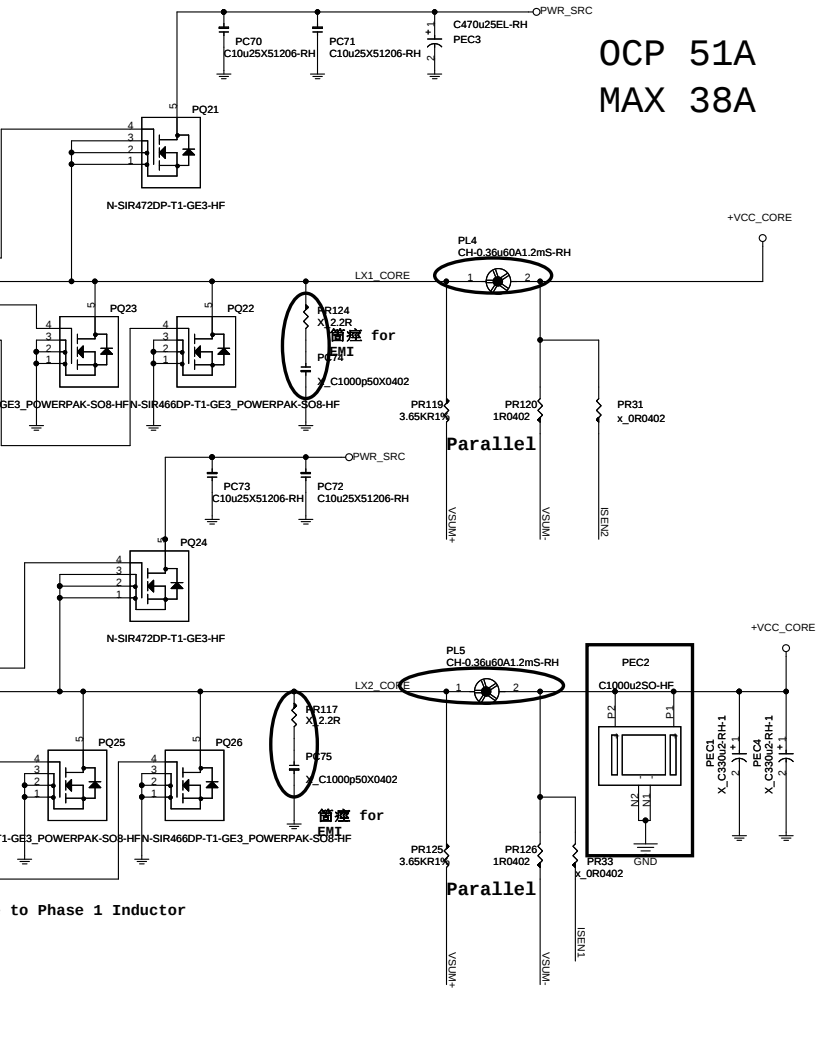
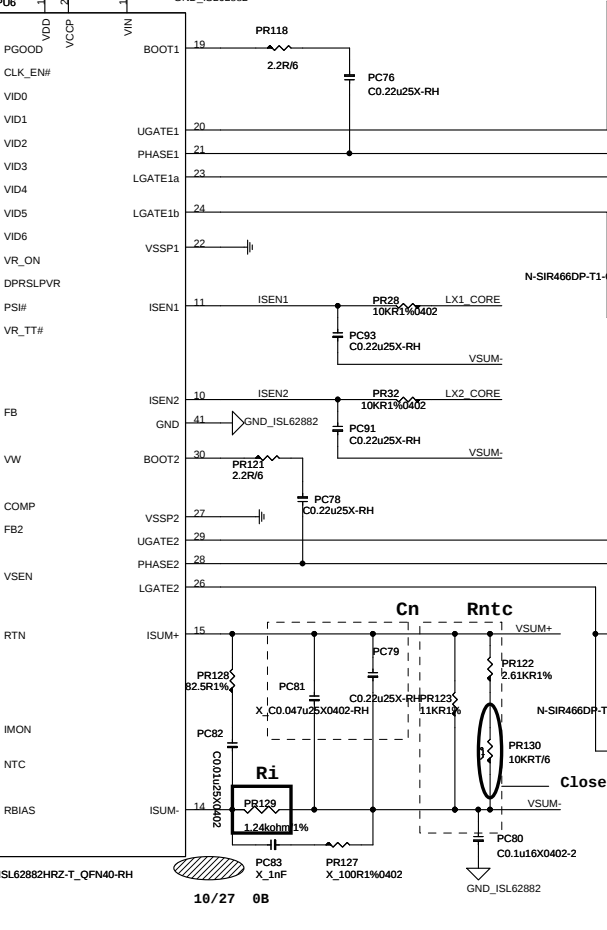
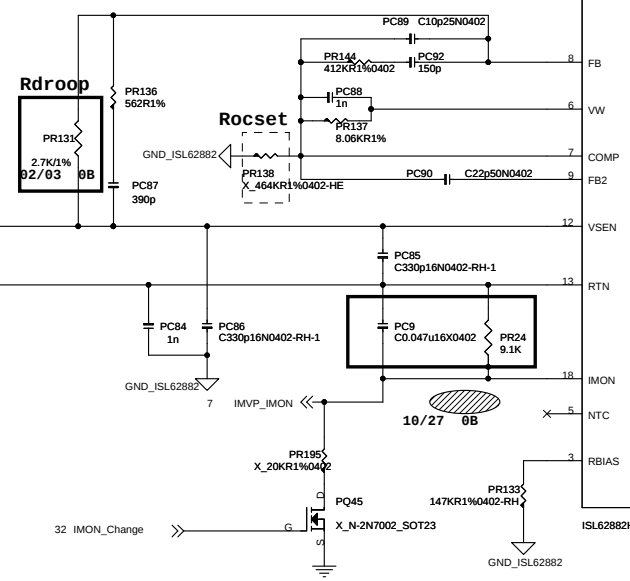
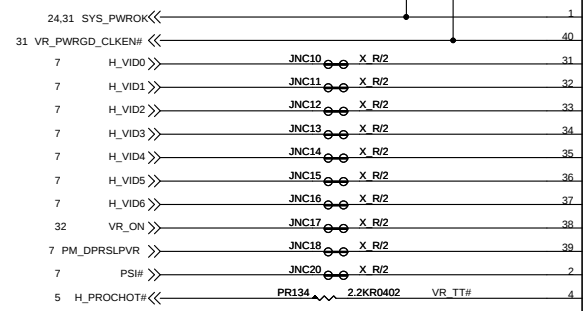




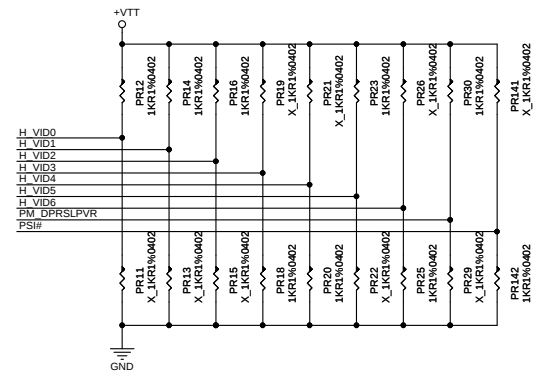
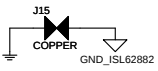
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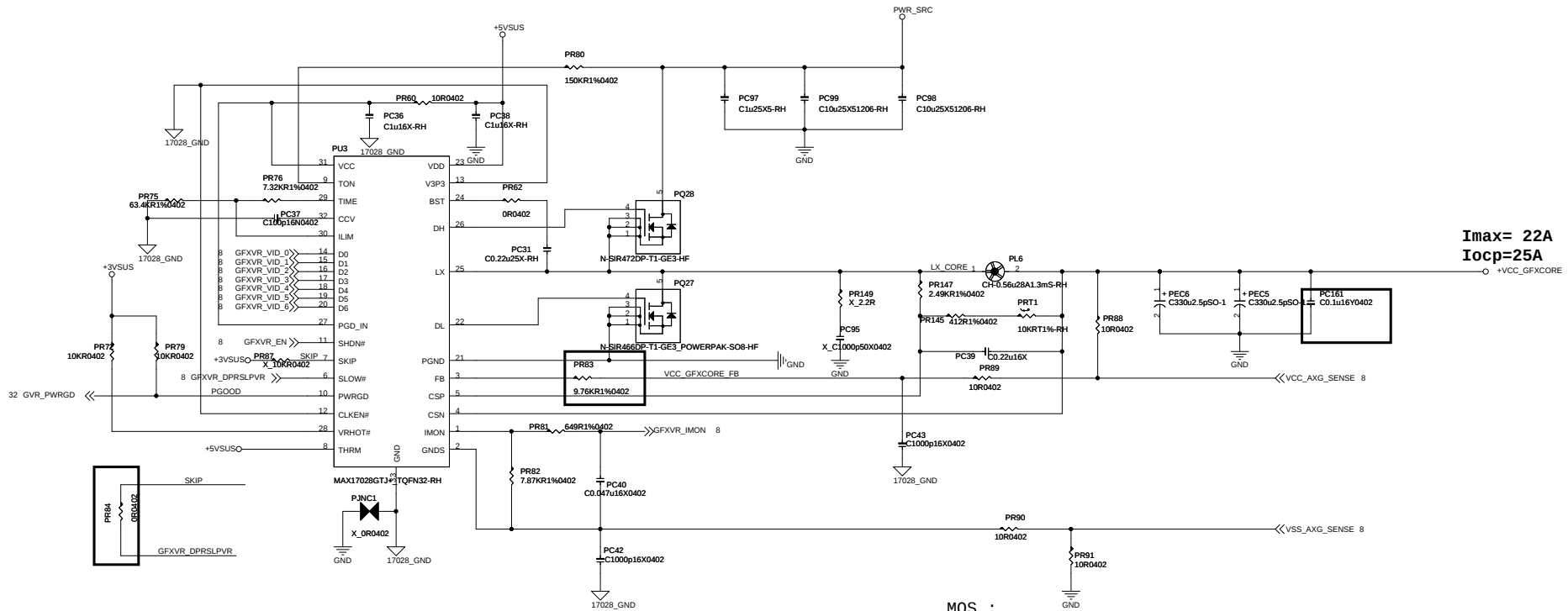


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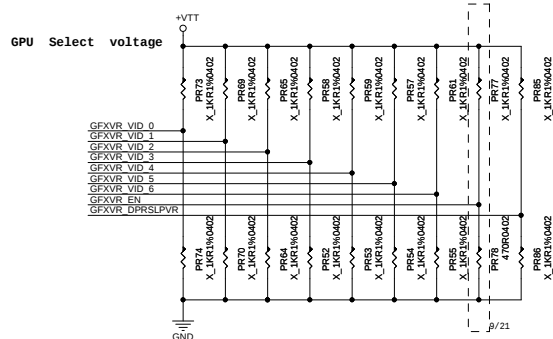
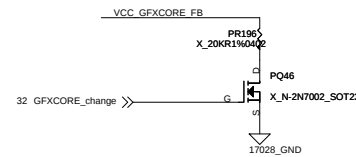


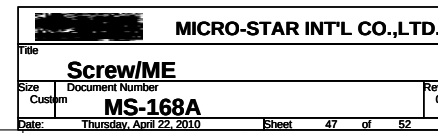
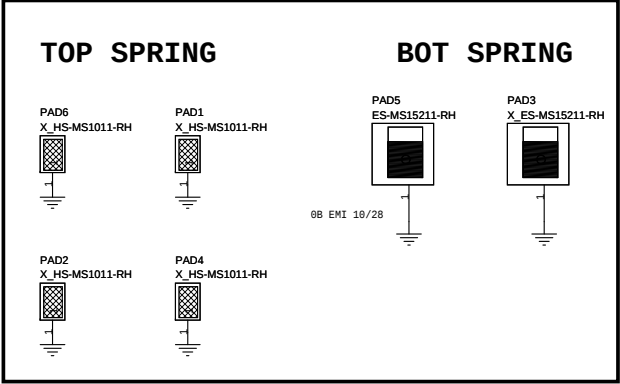
1.0 Change to no OC function

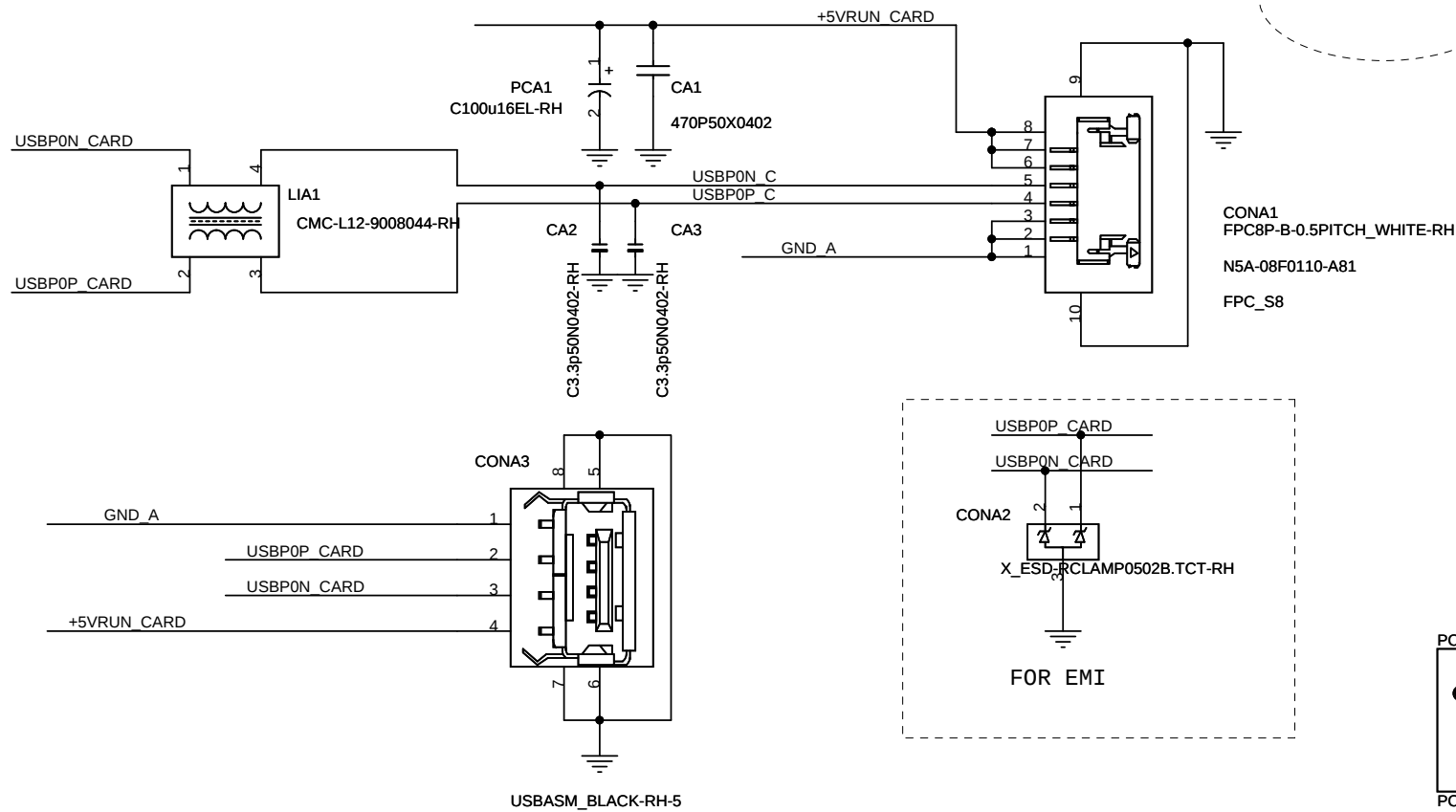




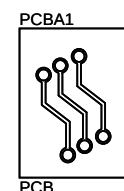
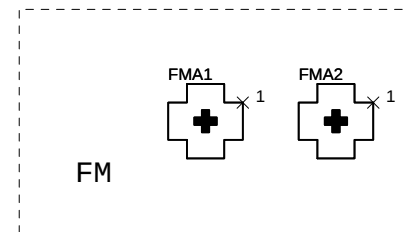
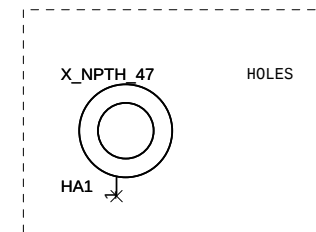
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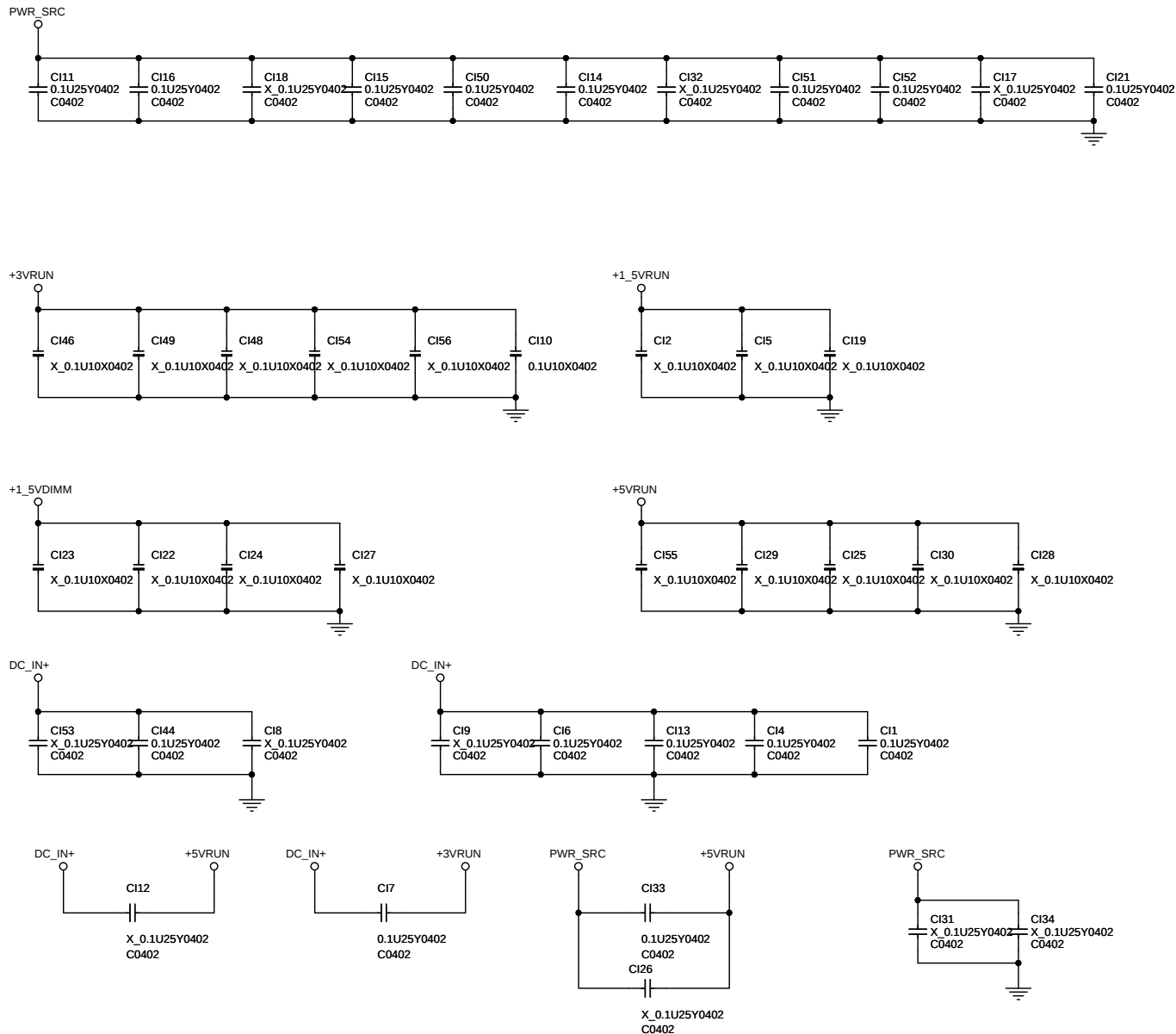


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