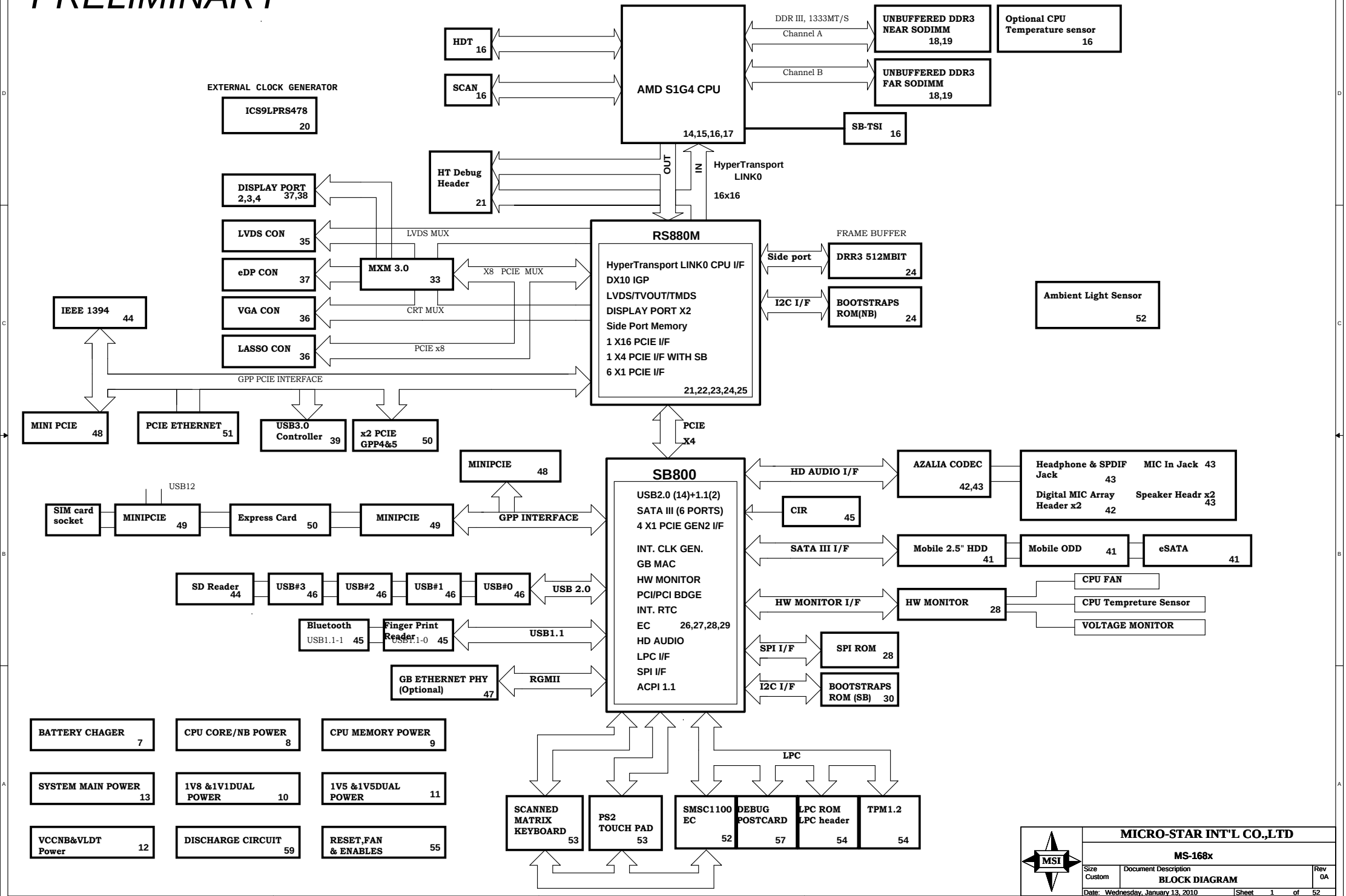
PRELIMINARY

GUAM S1G4 SCHEMATIC DESIGN



MICRO-STAR INT'L CO.,LTD

MS-168x

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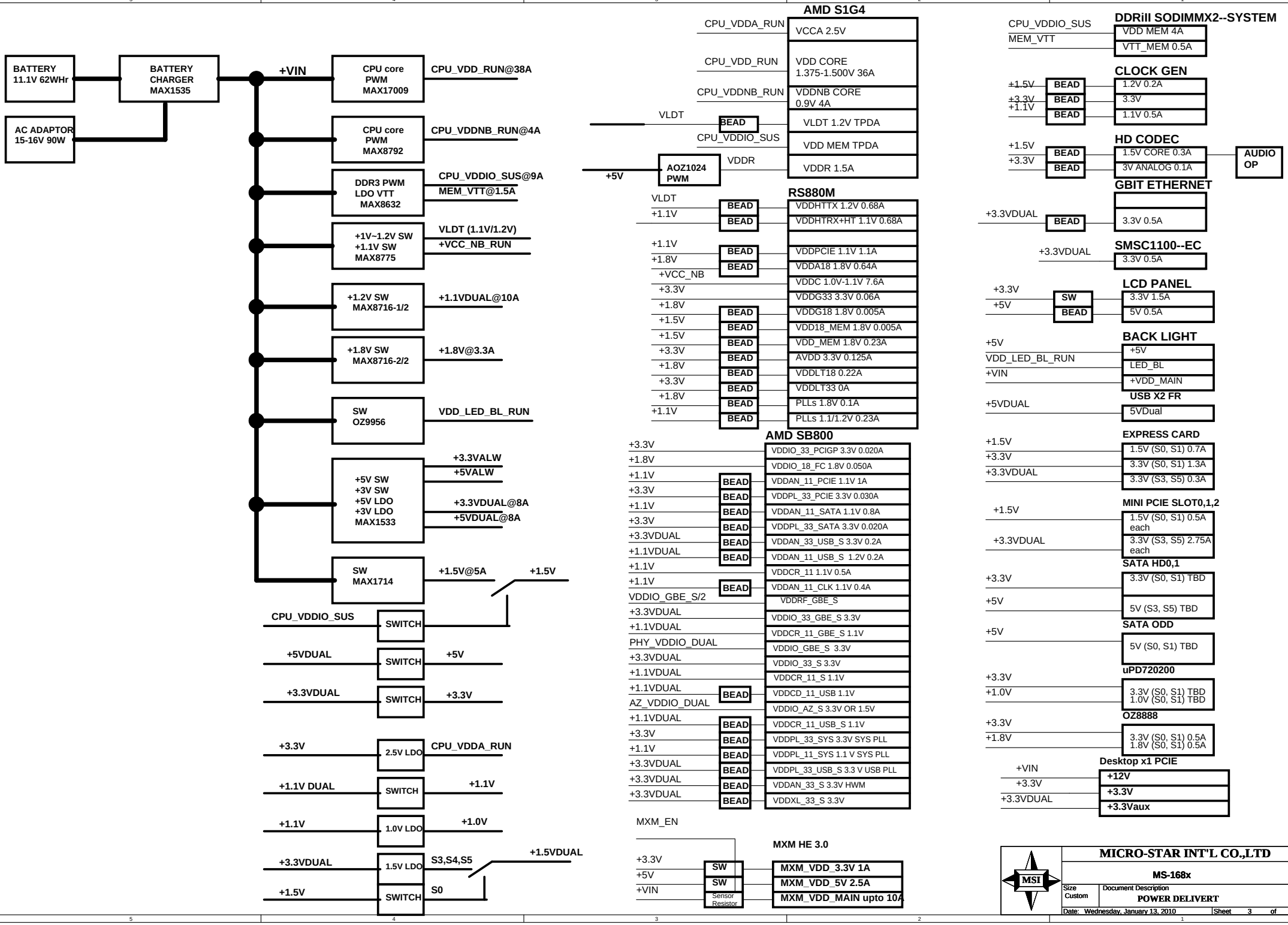
BATTERY 11.1V 62WHr
BATTERY CHARGER MAX1535
AC ADAPTOR 15-16V 90W
+VIN
CPU core PWM MAX17009
CPU_VDD_RUN@38A
CPU core PWM MAX8792
CPU_VDDNB_RUN@4A
DDR3 PWM LDO VTT MAX8632
CPU_VDDIO_SUS@9A
MEM_VTT@1.5A
+1V~1.2V SW +1.1V SW MAX8775
VLDT (1.1V/1.2V)
+VCC_NB_RUN
+1.2V SW MAX8716-1/2
+1.1VDUAL@10A
+1.8V SW MAX8716-2/2
+1.8V@3.3A
SW OZ9956
VDD_LED_BL_RUN
+5V SW +3V SW +5V LDO +3V LDO MAX1533
+3.3VALW
+5VALW
+3.3VDUAL@8A
+5VDUAL@8A
SW MAX1714
+1.5V@5A
+1.5V
CPU_VDDIO_SUS
SWITCH
+5VDUAL
SWITCH
+5V
+3.3VDUAL
SWITCH
+3.3V
+3.3V
2.5V LDO
CPU_VDDA_RUN
+1.1V DUAL
SWITCH
+1.1V
+1.1V
1.0V LDO
+1.0V
+3.3VDUAL
1.5V LDO
S3,S4,S5
+1.5VDUAL
+1.5V
SWITCH
S0
AMD S1G4
CPU_VDDA_RUN
VCCA 2.5V
CPU_VDD_RUN
VDD CORE 1.375-1.500V 36A
CPU_VDDNB_RUN
VDDNB CORE 0.9V 4A
VLDT
BEAD
VLDT 1.2V TPDA
CPU_VDDIO_SUS
VDD MEM TPDA
+5V
AOZ1024 PWM
VDDR
VDDR 1.5A
RS880M
VLDT
+1.1V
BEAD
VDDHTTX 1.2V 0.68A
VDDHTRX+HT 1.1V 0.68A
+1.1V
+1.8V
BEAD
VDDPCIE 1.1V 1.1A
VDDA18 1.8V 0.64A
+VCC_NB
VDDC 1.0V-1.1V 7.6A
+3.3V
VDDG33 3.3V 0.06A
+1.8V
+1.5V
+1.5V
+3.3V
+1.8V
+3.3V
+1.8V
+1.1V
BEAD
VDDG18 1.8V 0.005A
VDD18_MEM 1.8V 0.005A
VDD_MEM 1.8V 0.23A
AVDD 3.3V 0.125A
VDDLT18 0.22A
VDDLT33 0A
PLLs 1.8V 0.1A
PLLs 1.1/1.2V 0.23A
AMD SB800
+3.3V
+1.8V
+1.1V
+3.3V
+1.1V
+3.3V
+3.3VDUAL
+1.1VDUAL
+1.1V
+1.1V
VDDIO_GBE_S/2
+3.3VDUAL
+1.1VDUAL
PHY_VDDIO_DUAL
+3.3VDUAL
+1.1VDUAL
+1.1VDUAL
AZ_VDDIO_DUAL
+1.1VDUAL
+3.3V
+1.1V
+3.3VDUAL
+3.3VDUAL
+3.3VDUAL
BEAD
VDDIO_33_PCIGP 3.3V 0.020A
VDDIO_18_FC 1.8V 0.050A
VDDAN_11_PCIE 1.1V 1A
VDDPL_33_PCIE 3.3V 0.030A
VDDAN_11_SATA 1.1V 0.8A
VDDPL_33_SATA 3.3V 0.020A
VDDAN_33_USB_S 3.3V 0.2A
VDDAN_11_USB_S 1.2V 0.2A
VDDCR_11 1.1V 0.5A
VDDAN_11_CLK 1.1V 0.4A
VDDRF_GBE_S
VDDIO_33_GBE_S 3.3V
VDDCR_11_GBE_S 1.1V
VDDIO_GBE_S 3.3V
VDDIO_33_S 3.3V
VDDCR_11_S 1.1V
VDDCD_11_USB 1.1V
VDDIO_AZ_S 3.3V OR 1.5V
VDDCR_11_USB_S 1.1V
VDDPL_33_SYS 3.3V SYS PLL
VDDPL_11_SYS 1.1 V SYS PLL
VDDPL_33_USB_S 3.3 V USB PLL
VDDAN_33_S 3.3V HWM
VDDXL_33_S 3.3V
MXM_EN
+3.3V
+5V
+VIN
SW
SW
Sensor Resistor
MXM HE 3.0
MXM_VDD_3.3V 1A
MXM_VDD_5V 2.5A
MXM_VDD_MAIN upto 10A
DDRill SODIMMX2--SYSTEM
CPU_VDDIO_SUS
MEM_VTT
VDD MEM 4A
VTT_MEM 0.5A
CLOCK GEN
+1.5V
+3.3V
+1.1V
BEAD
1.2V 0.2A
3.3V
1.1V 0.5A
HD CODEC
+1.5V
+3.3V
BEAD
1.5V CORE 0.3A
3V ANALOG 0.1A
AUDIO OP
GBIT ETHERNET
+3.3VDUAL
BEAD
3.3V 0.5A
SMSC1100--EC
+3.3VDUAL
3.3V 0.5A
LCD PANEL
+3.3V
+5V
SW
BEAD
3.3V 1.5A
5V 0.5A
BACK LIGHT
+5V
VDD_LED_BL_RUN
+VIN
+5V
LED_BL
+VDD_MAIN
USB X2 FR
+5VDUAL
5VDual
EXPRESS CARD
+1.5V
+3.3V
+3.3VDUAL
1.5V (S0, S1) 0.7A
3.3V (S0, S1) 1.3A
3.3V (S3, S5) 0.3A
MINI PCIE SLOT0,1,2
+1.5V
+3.3VDUAL
1.5V (S0, S1) 0.5A each
3.3V (S3, S5) 2.75A each
SATA HD0,1
+3.3V
+5V
3.3V (S0, S1) TBD
5V (S3, S5) TBD
SATA ODD
+5V
5V (S0, S1) TBD
uPD720200
+3.3V
+1.0V
3.3V (S0, S1) TBD
1.0V (S0, S1) TBD
OZ8888
+3.3V
+1.8V
3.3V (S0, S1) 0.5A
1.8V (S0, S1) 0.5A
Desktop x1 PCIE
+VIN
+3.3V
+3.3VDUAL
+12V
+3.3V
+3.3Vaux
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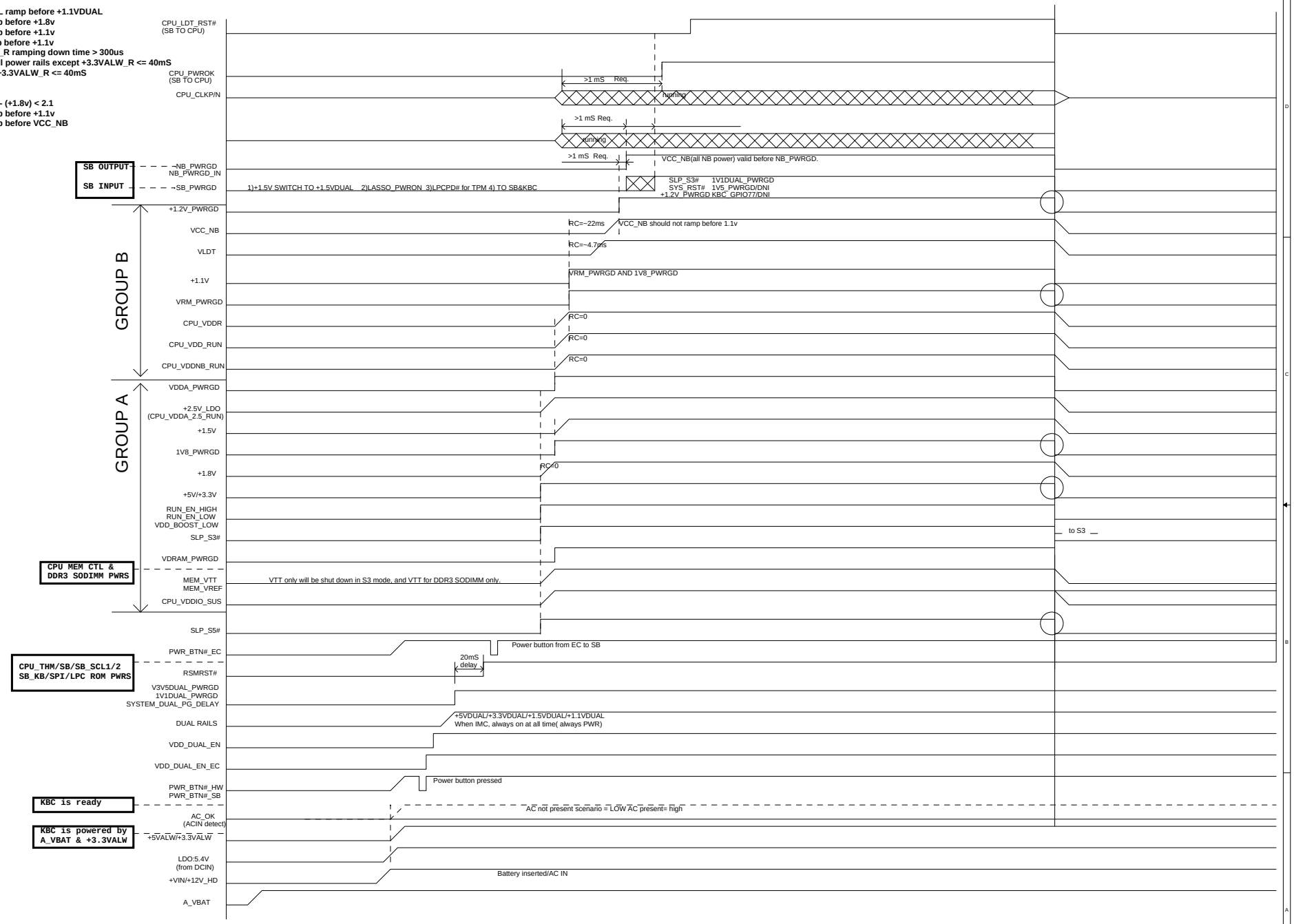
Power on Sequence required:

SB800:
1, +3.3VDUAL ramp before +1.1VDUAL
2, +3.3V ramp before +1.8v
3, +1.8V ramp before +1.1v
4, +3.3v ramp before +1.1v
5, +3.3VALW_R ramping down time > 300us
6, 50uS <= All power rails except +3.3VALW_R <= 40mS
7, 100uS <= +3.3VALW_R <= 40mS

RS880:
1, 0 <(+3.3V) - (+1.8v) < 2.1
2, +1.8V ramp before +1.1v
3. +1.1V ramp before VCC_NB



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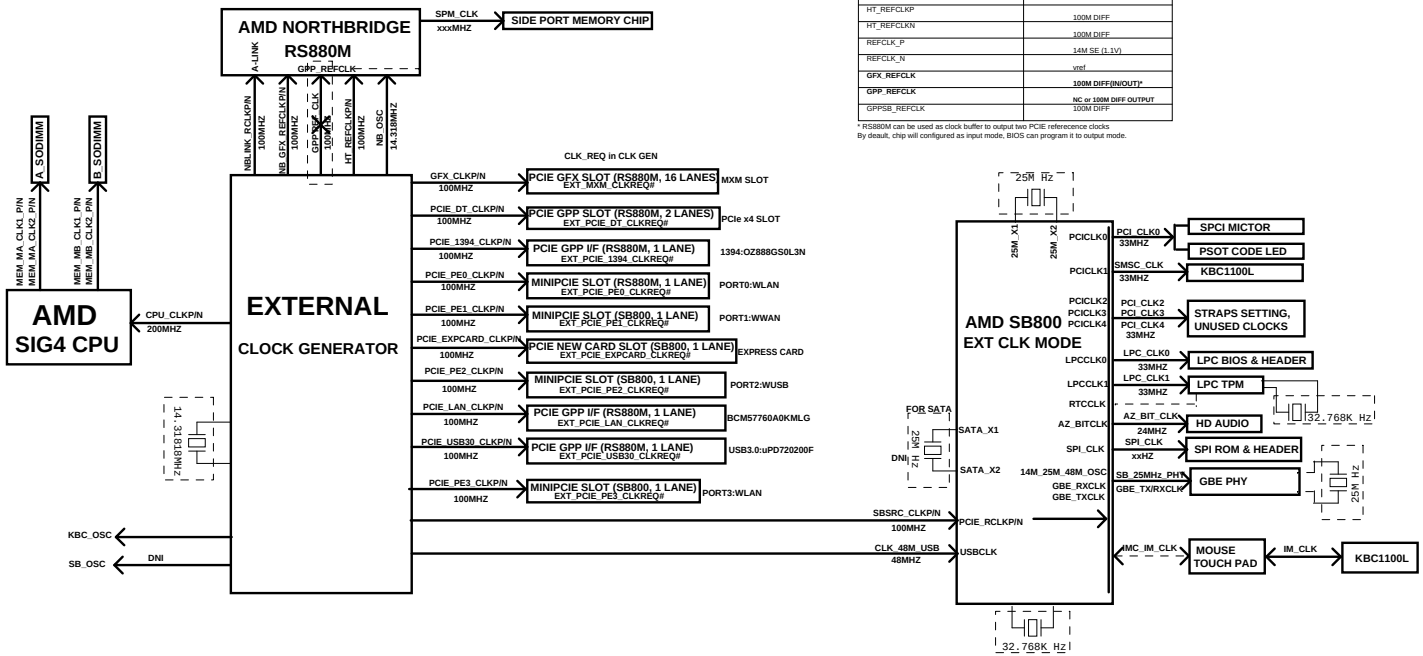
EXTERNAL CLOCK MODE

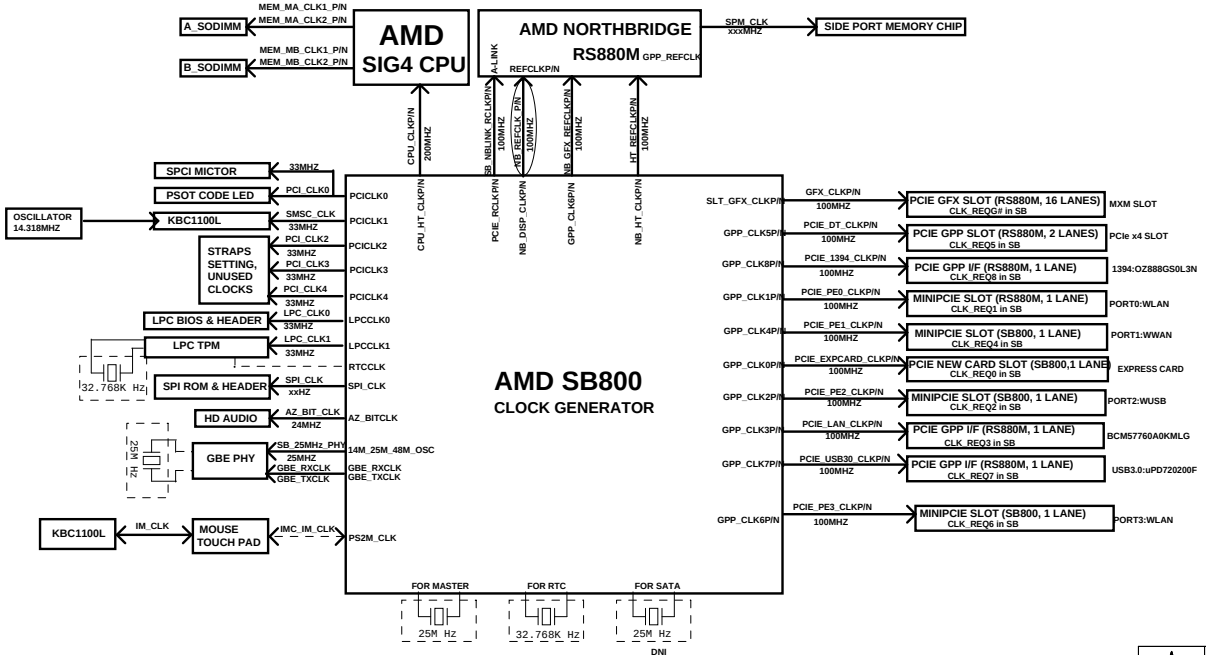
NB CLOCK INPUT TABLE

NB CLOCKS	RS880M
HT_REFCLKP	100M DIFF
HT_REFCLKN	100M DIFF
REFCLK_P	14M SE (1.1V)
REFCLK_N	vref
GFX_REFCLK	100M DIFF(IN/OUT)*
GPP_REFCLK	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF

* RS880M can be used as clock buffer to output two PCIE referecence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.



INTERNAL CLOCK MODE



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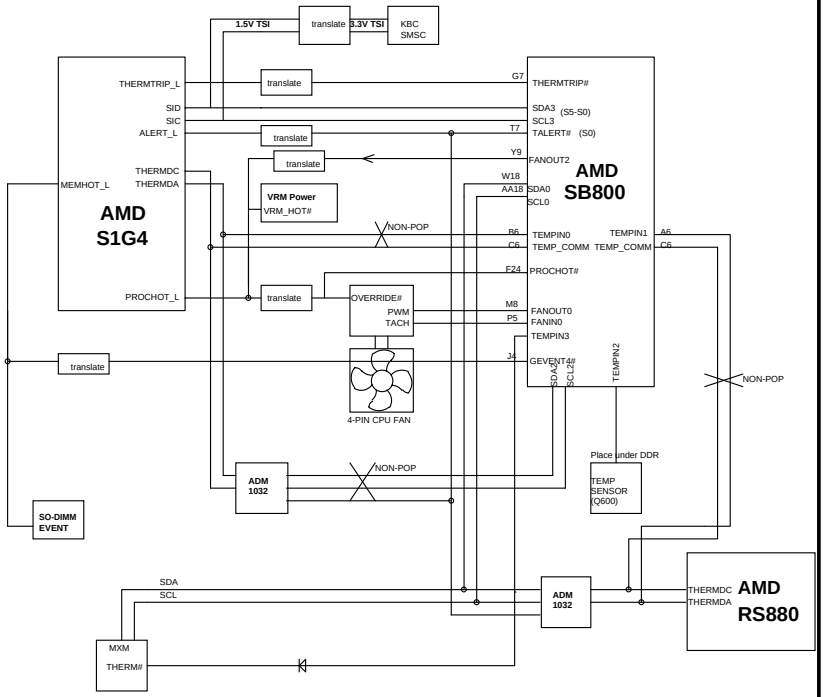
Thermal Systems
(Emergency Shutdown, Throttling, Fan Control)

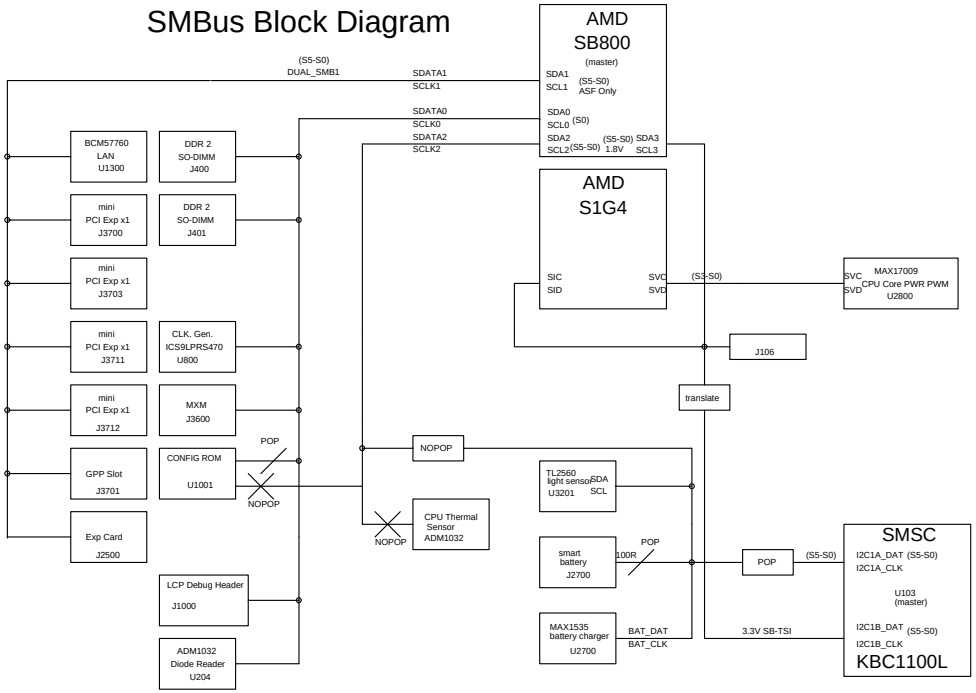


Thermal disaster prevention is implemented by PROCHOT_L and THERMTRIP_L with hardware non-system dependant functions. Fan speed control will only be implemented by SB TSI software based implementation

Power State / Voltage Rail Activity Summary

Global System State	Sleep State	Processor Power State	Description		RTC	ALW	DUAL	SUS	RUN
G0	S0	C0	Running		ON	ON	ON	ON	ON
G0	S0	C0	Running	P-state transitions under OS control	ON	ON	ON	ON	ON
G0	S0	C1		Halt	ON	ON	ON	ON	ON
G0	S0	C2		Stop grant, caches snoopable	ON	ON	ON	ON	ON
G0	S0	C3		TBD	ON	ON	ON	ON	ON
G0	S0	c4		TBD	ON	ON	ON	ON	ON
G1	S1	OFF	Sleeping	Powered on suspend	ON	ON	ON	ON	ON
G1	S3	OFF		Suspend to RAM	ON	ON	ON	ON	OFF
G2	S4	OFF		Suspend to diskON	ON	ON	ON	OFF	OFF
G2	S5	OFF	Soft-off		ON	ON	ON	OFF	OFF
G2/G3	S5 LOW	OFF	Battery IN		ON	ON	ON	OFF	OFF
G3		OFF	Mechanical off		ON	OFF	OFF	OFF	OFF

SMBus Block Diagram



Group Name Description

INT: Stuff when use internal clock generator
EXT: Stuff when use external clock generator
DNI: DO NOT INSTALL
KBC: Stuff when use external KBC
IMC: Stuff when use internal EC
A11:Resistors marked with "A11" is only for SB800A11 ONLY.

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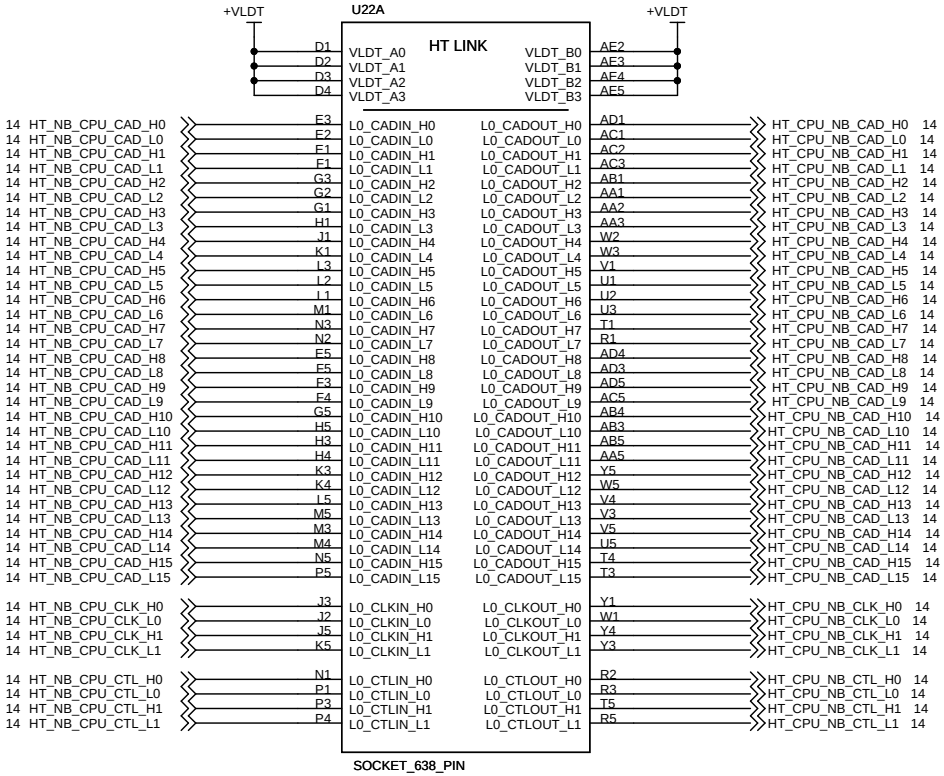
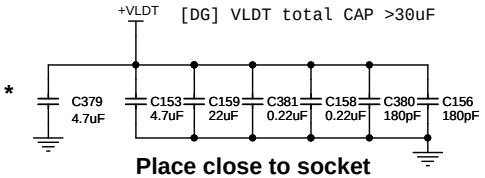
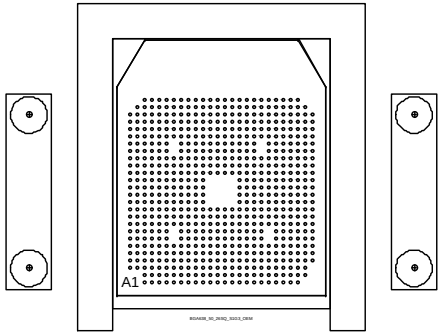


[CheckList] If the I/O device does not support the CTLIN1 pair, pull up 51ohm



[ChckList] Can change 22u*1/4.7u*2 to 10u*3



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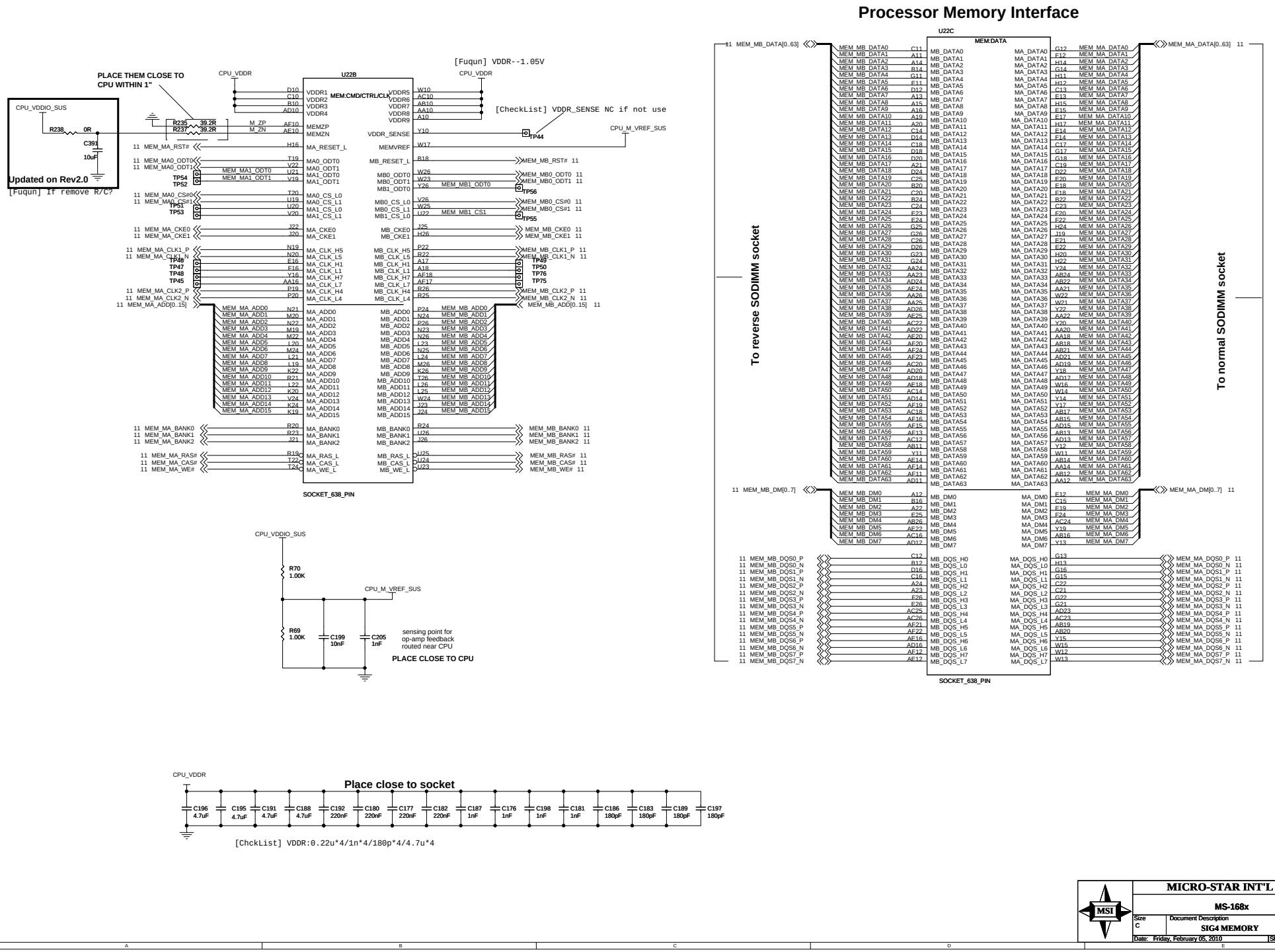
Processor Memory Interface



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[DG] BEAD: R<40mΩ(about 35), I>500mA
[ChckList] VDDA:100u*1/4.7u*1/0.22u0603*1/3300p0603*1

LAYOUT: ROUTE VDDA TRACE APPROX. 50 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

Keep net PWRGD, LDT_STOP#, LDT_RST# no stub

+1.5VRUN
R225 300R
19 CPU_PWRGD — R224 — PWRGD

+1.5VRUN
R213 300R
16,19 CPU_LDT_STOP# — R219 — LDT_STOP#

+1.5VRUN
R227 300R
19 CPU_LDT_RST# — R228 — LDT_RST#
C388 X_180pF

+VDDA
L12 26R_600mA
C175 22uF
C166 4.7UF
C167 220nF
C169 3.3NF
CPU_VDDA_RUN

200MHz
24 CPU_CLKP
24 CPU_CLKN
C390 3.9NF
C389 3.9NF
R232 169R
Keep trace from resisor to CPU within 0.6"
keep trace from caps to CPU within 1.2"

CPU_LDT_REQ# is NOT needed by S1G4
[Fuqun] Thermal
place them to CPU within 1.5"
TP28
20 CPU_SIC
20 CPU_SID
+VLDT
R63 44.2R
R62 44.2R

[CheckList} VDD1_FB_H/L NC if not use

U22D

F8	VDDA1	VSS	M11
F9	VDDA2	RSVD11	W18
A9	CLKIN_H	SVC	A6 CPU_SVC_R
A8	CLKIN_L	SVD	A4 CPU_SVD_R
B7	RESET_L		
A7	PWROK		
F10	LDTSTOP_L	THERMTRIP_L	AF6 CPU_THERMTRIP# VDDIO
C6	LDTREQ_L	PROCHOT_L	AC7
		MEMHOT_L	AA8 CPU_MEMHOT#_VDDIO
AF4	SIC		
AF5	SID		
AE6	ALERT_L	THERMDC	W7 CPU_THERMDC
		THERMDA	W8 CPU_THERMDA
R6	HT_REF0		
P6	HT_REF1		
F6	VDD0_FB_H	VDDIO_FB_H	W9
E6	VDD0_FB_L	VDDIO_FB_L	Y9
Y6	VDD1_FB_H	VDDNB_FB_H	H6
AB6	VDD1_FB_L	VDDNB_FB_L	G6
G10	DBRDY		
AA9	TMS	DBREQ_L	E10 CPU_DBREQ#
AC9	TCK		
AD9	TRST_L	TDO	AF9 CPU_TDO
AF9	TDI		
AD7	TEST23	TEST28_H	J7 CPU_TEST28_H_PLLCHRZ_P
		TEST28_L	H8 CPU_TEST28_L_PLLCHRZ_N
H10	TEST18	TEST17	D7 CPU_TEST17_BP3
G9	TEST19	TEST16	E7 CPU_TEST16_BP2
E9	TEST25_H	TEST15	F7 CPU_TEST15_BP1
E8	TEST25_L	TEST14	C7 CPU_TEST14_BP0
AB8	TEST21	TEST7	C3 CPU_TEST7_ANALOG_T
AF7	TEST20	TEST10	K8 CPU_TEST10_ANALOGOUT
AE7	TEST24		
AE8	TEST22	TEST8	C4 CPU_TEST8_DIG_T
AC8	TEST12		
AF8	TEST27		
C2	TEST9	TEST29_H	C9 CPU_TEST29_H_FBCLKOUT_P
AA6	TEST6	TEST29_L	C8 CPU_TEST29_L_FBCLKOUT_N
A3	RSVD1	RSVD10	H18
A5	RSVD2	RSVD9	H19
B3	RSVD3	RSVD8	AA7
B5	RSVD4	RSVD7	D5
C1	RSVD5	RSVD6	C5

SOCKET_638_PIN

CPU_VDDIO_SUS
R216 10K Q15
R210 1K
R200 300R
N-MMBT3904_NL_SOT23
R190 X_0R
CPU_THERMTRIP# 20
CPU_PROCHOT# 19
VRD_PROCHOT# 44
TP35
S1G4 does not support MEMHOT_L
TP36 TP39
Thermdc and Thermda should be routed away to VRM, crystal, etc. Customer should follow the MBDG. However, Guam is using TSI so this does not applies to Guam.

[CheckList] VDDIO_FB_H/L NC if not use
TP43 TP38
CPU_VDDNB_RUN_FB_H 44
TP28

TP42
route as differential as short as possible testpoint under package
TP30 TP34
TP26 TP24
For debug only
TP23
TP25

R65 80.6R
Route as 80ohm, diff R184's value is TBD.

[Fuqun] TEST23--R358 NC in ref schematic?

CPU_VDDIO_SUS
R236 510R
R234 510R
R208 0R
TP32

CPU_VDDIO_SUS
R203 1K
R204 2.2K
4.7K R194
Q13
N-MMBT3904_NL_SOT23
CPU_SID
SMB_THRMCPU_DATA 24,25
D10 BAS40WS

CPU_VDDIO_SUS
R202 1K
R201 2.2K
4.7K R193
Q12
N-MMBT3904_NL_SOT23
CPU_SIC
SMB_THRMCPU_CLK 24,25
D9 BAS40WS

CPU_VDDIO_SUS
R207 1K
R206 10K
4.7K R205
Q14
N-MMBT3904_NL_SOT23
CPU_ALERT
SMBALERT# 20

[Fuqun] Connect SB or EC?

THERMDA/THERMDC is not used;
CPU thermal control is based on TSI by default.

[Fuqun] RSVD/TEST6/7/8/10/28--NC
[Fuqun] TEST14/15/16/17--Test Point
[Fuqun] TEST23/25--Test Point
[Fuqun] TEST12/18~24--Pull down 1Kohn to VSS
[Fuqun] TEST27 pull-up 1Kohm to VDDIO
[Fuqun] TEST25_H pull-up 510ohm to VDDIO
[Fuqun] TEST25_L pull-down 510ohm to VSS
[Fuqun] TEST9 is tied to VSS
[Fuqun] There is a (±1%) differential termination between TEST29_L and TEST29_H
[Fuqun] CPU_DBRDY not need pull down in checklist

CPU_VDDIO_SUS
CPU_DBREQ# R218 300R
CPU_TEST27_SINGLECHAIN R231 1K
CPU_TEST21_SCANEN R226 1K
CPU_TEST20_SCANCLK2 R221 1K
CPU_TEST24_SCANCLK1 R222 1K
CPU_TEST22_SCANSHIFTEN R223 1K
CPU_TEST12_SCANSHIFTENB R229 1K
CPU_TEST15_BP1 R61 X_300R
CPU_TEST14_BP0 R64 X_300R
CPU_TEST18_PLLTEST1 R230 1K
CPU_TEST19_PLLTEST0 R223 1K
CPU_TEST23_TSTUPD R217 1K
CPU_DBRDY R67 X_300R
CPU_TEST10_ANALOGOUT R60 X_300R +VLDT

R147, R152 is installed ONLY when SCAN is enabled
R215, R185 internal ONLY
R162 is TBD

[DateSheet] Internal Termination:Systems that do not require use of these pins can rely on the internal termination to pull the signals to the proper inactive state. When these pins are used, they must not be driven with open-drain outputs,otherwise additional termination is required

[DateSheet] Internal pull_up 870~1250 ohm:
SSA[2;0], TCK, TMS, TRST_L, TDI, DBREQ_L, PLATFORM_TYPE, TEST27

[DateSheet] Internal pull_down 870~1250 ohm:
TEST12, TEST[20:24]

+1.5VRUN
1K R212
1K R209
2.2K R215
[Fuqun] PWRGD pull-up in 2 times (R187 and R163)?
CPU_SVC_R — R214
CPU_SVD_R — R211
PWRGD — R220
CPU_SVC 44
CPU_SVD 44
CPU_PWRGD_SVID_REG 44

Internal pull_up 870~1250 ohm:
SSA[2;0], TCK, TMS, TRST_L, TDI, DBREQ_L, PLATFORM_TYPE, TEST27

SVC	SVD	BOOT VOLTAGE(VDD) (CPUVRM_PRO# = VCC/GND)	BOOT VOLTAGE(VDD) (CPUVRM_PRO# = OPEN)
0	0	1.1	1.1
0	1	1.0	1.2
1	0	0.9	1.0
1	1	0.8	0.8

VID OVERIDE TABLE (VDD)

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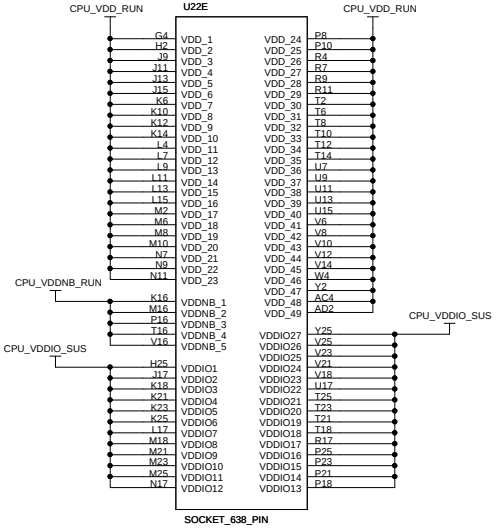
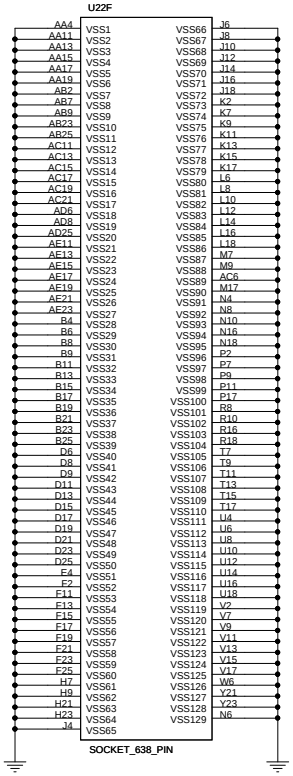
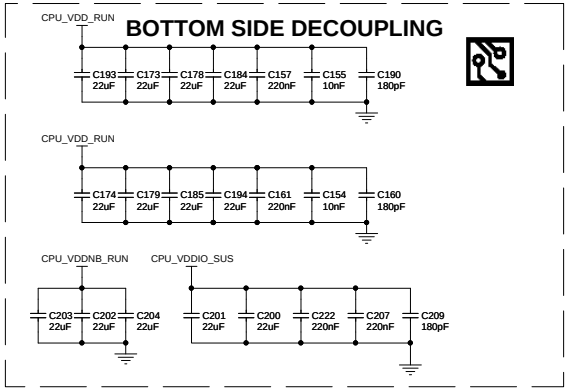
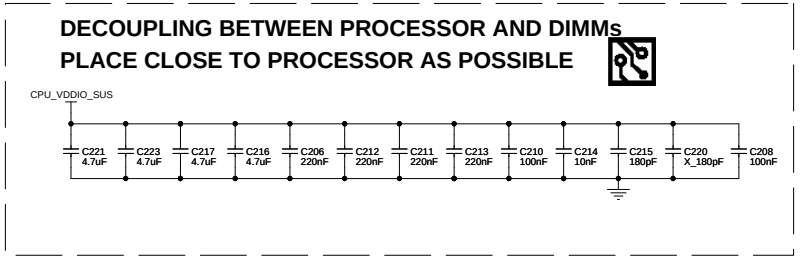






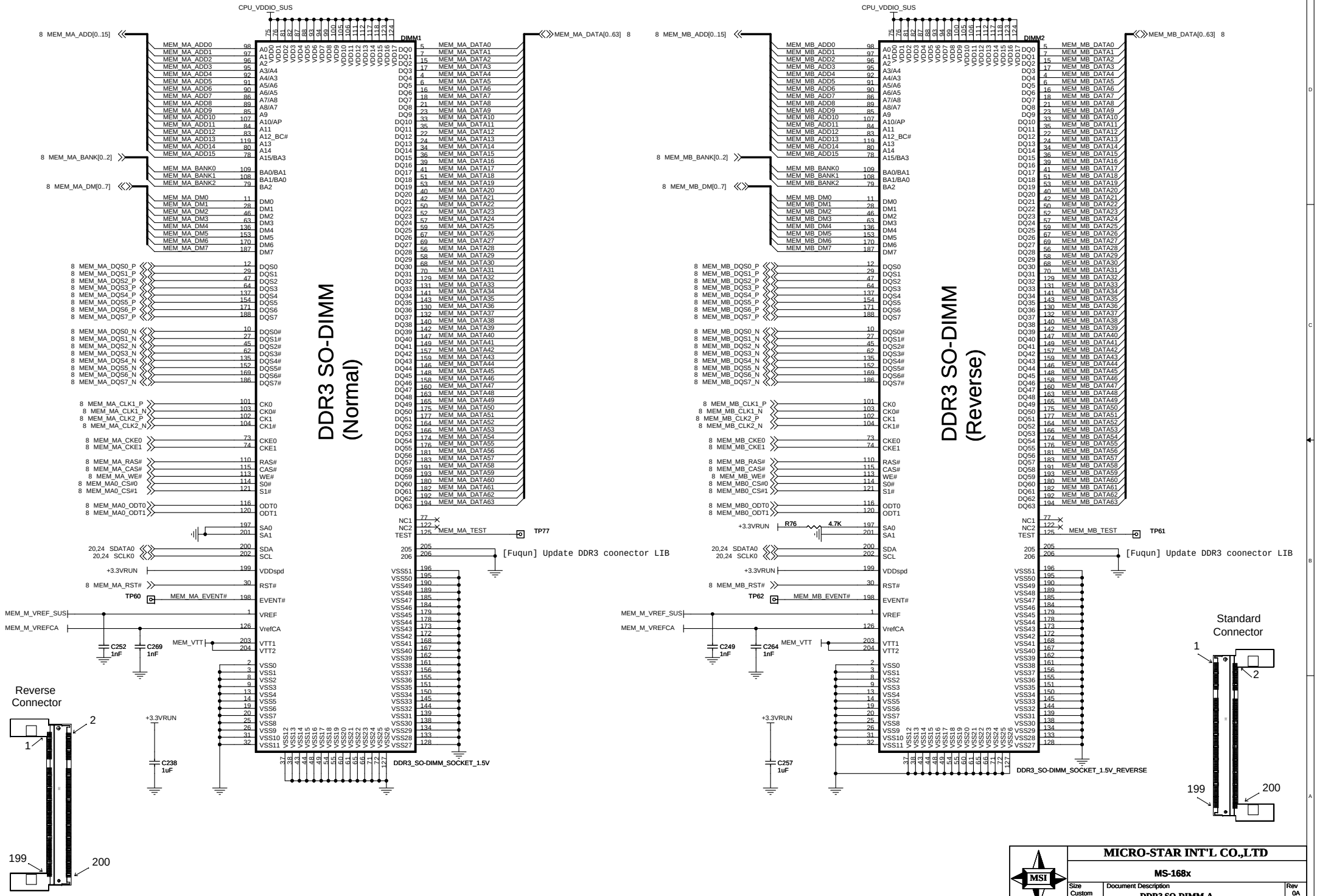
[ChckList] VDD:22u*8/0.22u*2/0.01u0603*2/180p*2
[ChckList] VDDNB:22u*3



[ChckList] VDDIO:22u*2/0.22u*6/0.1u0603*2/0.01u0603*1/180p*1/4.7u*4

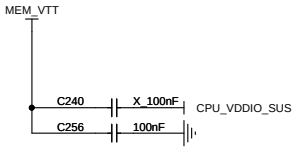
PROCESSOR POWER AND GROUND

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-168x	
Size: Custom	Document Description: SIG4 POWER and GND	Rev: 0A
Date: Friday, February 05, 2010	Sheet 10 of 52	

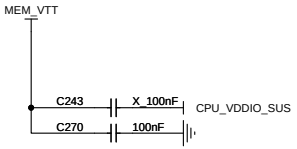


MICRO-STAR INT'L CO.,LTD	
MS-168x	
Size: Custom	Document Description: DDR3 SO-DIMM-A
Rev: 0A	
Date: Friday, February 05, 2010	Sheet 11 of 52

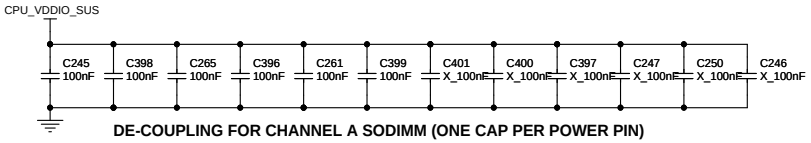
MICRO-STAR INT'L CO.,LTD	
MS-168x	
Size: A	Document Description: DDR3 SO-DIMM-B
Rev: 0A	
Date: Wednesday, January 13, 2010	Sheet 12 of 52



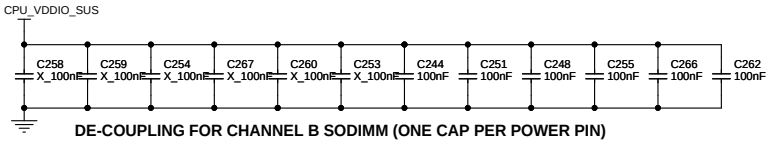
DE-COUPLING FOR CHANNEL A SODIMM



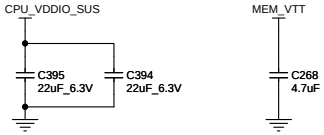
DE-COUPLING FOR CHANNEL B SODIMM

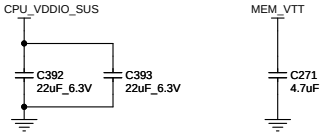


DE-COUPLING FOR CHANNEL A SODIMM (ONE CAP PER POWER PIN)

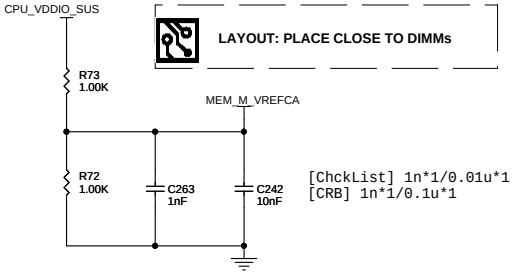


DE-COUPLING FOR CHANNEL B SODIMM (ONE CAP PER POWER PIN)

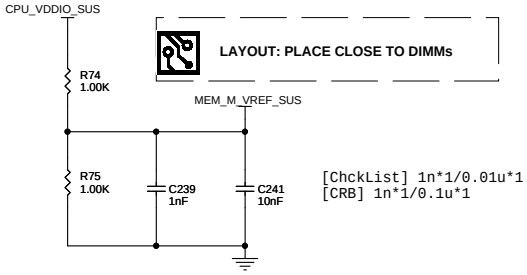




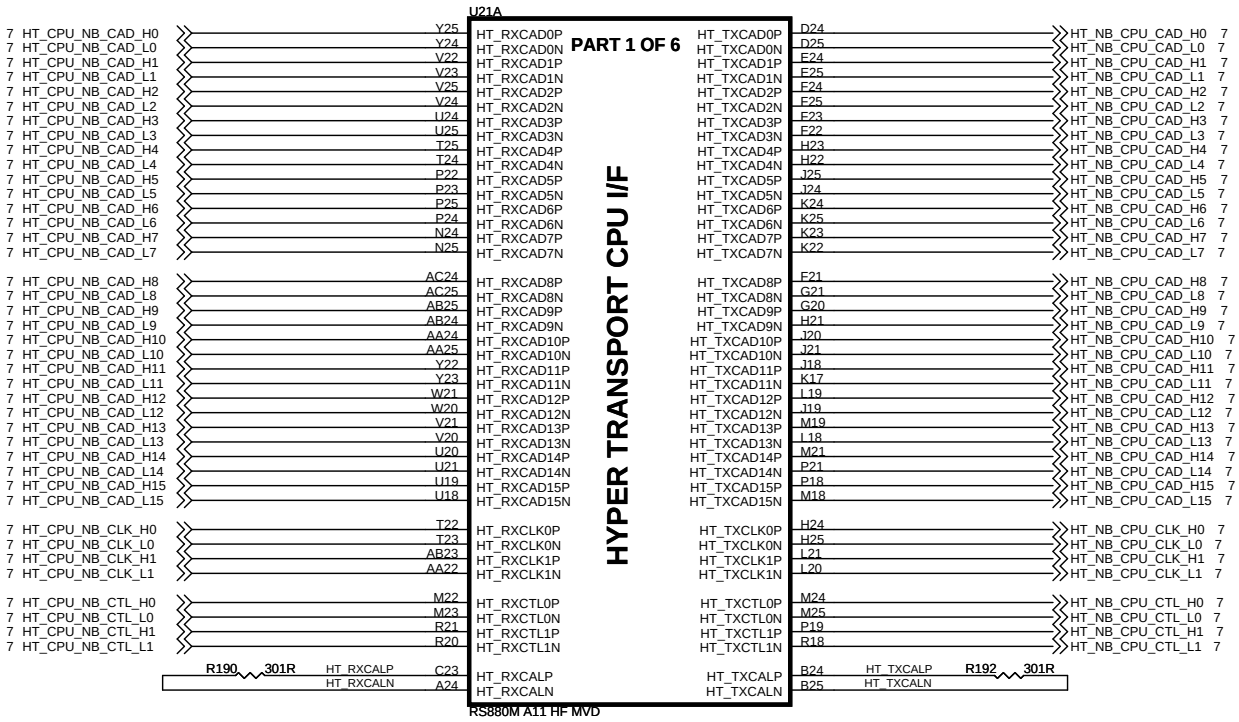
MEM_M_VREFCA



MEM_VREF_SUS



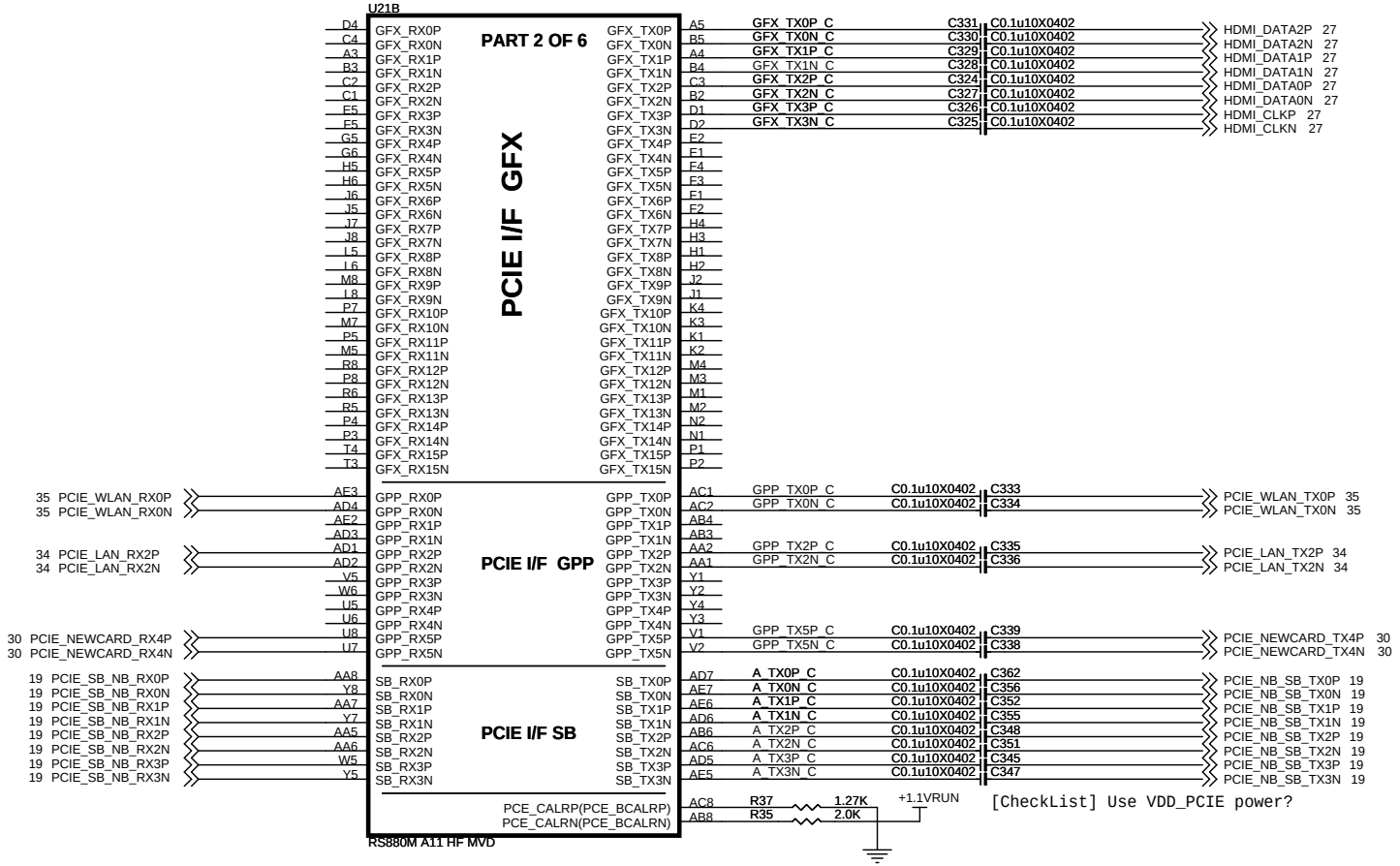
MICRO-STAR INT'L CO.,LTD		
MS-168x		
Size: Custom	Document Description: DDR3 DECOUPLING	Rev: 0A
Date: Friday, February 05, 2010	Sheet 13 of 52	



MICRO-STAR INT'L CO.,LTD			
MS-168x			
Size: B	Document Description: RS880M-HT		Rev: 0A
Date: Friday, February 05, 2010	Sheet 14 of 52		

MXM3.0 need put the CAP on the motherboard.
Close to the MXM Slot

MXM3.0 need put the CAP on the motherboard.
Close to the MXM Slot



RS880M Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

Keep the impendance of PCIE lane to 85ohm +/-15%
Including the A-link

All PCIe lane shou route 8" max for Gen2 connector and max 12" for Gen2 on board devices
Guam has the Lasso lane over 8" due to the large board, should use shorter lasso calbe for Guam.
Customer need to follow the MBDG.

MICRO-STAR INT'L CO.,LTD		
MS-168x		
Size: B	Document Description: RS880M-PCIE	Rev: 0A
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DDR3 based CPU and mobile platforms--Level shift to 1.8V

DDR2 based CPU mobile platforms--No need level shift

[CheckList] Change 1K to 2.2K for DDR3/NoteBook

+1.5VRUN +1.8VRUN R186 1K Q9 R168 2.2K N-MMBT3904_NL_SOT23

9,19 CPU_LDT_STOP# NB_LDT_STOP#

+1.8VRUN +1.8VRUN R167 300R R187 1K

19 ALLOW_LDTSTOP ALLOW_LDTSTOP

20 NB_PWRGD NB_PWRGD

18,19,24,25 A_RST# R151 X_NC NB_RST#_IN

[Fuqun] NBPWRGD:level shifterTto 1.8V if driven from a 3.3-V output?

[CheckList] 200ohm bead?

+1.1VRUN +1.8VRUN L5 220R 3.9R L7 L9 220R L4 220R C118 22uF

65mA 20mA 120mA

C93 2.2uF_4V C102 4.7uF_4V C111 2.2uF_4V C82 2.2uF_4V

[CheckList] 2.2uf?

Change B204/C262 for black screen issue in AMD 47329 document

+3.3VRUN L8 220R 110mA AVDD C105 2.2uF_4V

+1.8VRUN 20mA AVDDDI C104 0.1uF

+1.8VRUN L6 220R 4mA AVDDQ C103 2.2uF_4V

[Fuqun] TV--NC

Termination resstors < 1 inch trace

26 NB_VGA_R R49 140R 1% **

26 NB_VGA_G R48 150R 1%

26 NB_VGA_B R50 150R 1%

18,26 NB_HSYNC#

18,26 NB_VSYNC#

26 DAC_SCL

26 DAC_SDAT

R47 715R1%0402

U21C

PART 3 OF 6

CRT/TVOUT

AVDD1(NC) AVDD2(NC) AVDDDI(NC) AVSSDI(NC) AVDDQ(NC) AVSSQ(NC)

C_Pr(DFT_GPIO5) Y(DFT_GPIO2) COMP_Pb(DFT_GPIO4)

RED(DFT_GPIO0) REDb(NC) GREEN(DFT_GPIO1) GREENb(NC) BLUE(DFT_GPIO3) BLUEb(NC)

DAC_HSYNC(PWM_GPIO4) DAC_VSYNC(PWM_GPIO6) DAC_SCL(PCE_RCALRN) DAC_SDA(PCE_TCALRN)

DAC_RSET(PWM_GPIO1)

PLL PWR

PLLVDD(NC) PLLVDD18(NC) PLLVSS(NC)

VDDA18HTPLL

VDDA18PCIEPLL1 VDDA18PCIEPLL2

PLLVDD PLLVDD18 VDDA18HTPLL VDDA18PCIEPLL

LVTM

VDDLTP18(NC) VSSLTP18(NC)

VDDLT18_1(NC) VDDLT18_2(NC) VDDLT33_1(NC) VDDLT33_2(NC)

VSSLT1(VSS) VSSLT2(VSS) VSSLT3(VSS) VSSLT4(VSS) VSSLT5(VSS) VSSLT6(VSS) VSSLT7(VSS)

+1.8VRUN 15mA B10 220R

+1.8VRUN 300mA B8 220R_2A

C114 0.1uF C117 4.7uF C369 2.2uF_4V

PM

SYSRESETb POWERGOOD LDTSTOPb ALLOW_LDTSTOP

NB_RST# IN NB_PWRGD NB_LDT_STOP# ALLOW_LDTSTOP

CLOCKs

HT_REFCLKP HT_REFCLKN

24 HT_REFCLKP 24 HT_REFCLKN

REFCLK_P/OSCIN(OSCIN) REFCLK_N(PWM_GPIO3)

24 NB_OSC NB_REFCLKN

+1.1VRUN R39 4.7K R40 4.7K

GFX_REFCLKP GFX_REFCLKN

24 GFX_REFCLKP 24 GFX_REFCLKN

[Fuqun] NC or not?

GPP_REFCLKP GPP_REFCLKN

TP19 TP71

24 NBLINK_RCLKP 24 NBLINK_RCLKN

GPPSB_REFCLKP(SB_REFCLKP) GPPSB_REFCLKN(SB_REFCLKN)

LVDS_DIGON(PCE_TCALRP) LVDS_BLON(PCE_RCALRP) LVDS_ENA_BL(PWM_GPIO2)

TP21

[Fuqun] BIOS control for BLON or PWM function

MIS.

I2C_CLK I2C_DATA DDC_CLK0/AUX0P(NC) DDC_DATA0/AUX0N(NC) DDC_CLK1/AUX1P(NC) DDC_DATA1/AUX1N(NC)

26 LCD_I2C_CLK 26 LCD_I2C_DATA 27 NB_HDMI_CLK 27 NB_HDMI_DATA

R36 X_49.9R A11 R34 X_49.9R A11

STRP_DATA:
1. Strap function
2. Control NB_CORE power 1-0.95V;0-1.1V

18 STRP_DATA

STRP_DATA

RSVD

TP20

R155 150R RS880_AUX_CAL

AUX_CAL(NC)

TMDS_HPD(NC) HPD(NC)

HDMI_HPD 27

SUS_STAT#(PWM_GPIO5)

SUS_STAT# 18,20

THERMALDIODE_P THERMALDIODE_N

TESTMODE

TEST_EN

R41 1.8K

RS880M A11 HF MVD

PLACE R291, R292 CLOSE TO NB(R291, R292 IS FOR A11 SB800 ONLY)

[Fuqun] SUS_STAT#-->Not need connect to SB if Side-Port memory not implemented

TXOUT_L0P(NC) TXOUT_L0N(NC) TXOUT_L1P(NC) TXOUT_L1N(NC) TXOUT_L2P(NC) TXOUT_L2N(DBG_GPIO0) TXOUT_L3P(NC) TXOUT_L3N(DBG_GPIO2)

LVDS_TX_L0P 26 LVDS_TX_L0N 26 LVDS_TX_L1P 26 LVDS_TX_L1N 26 LVDS_TX_L2P 26 LVDS_TX_L2N 26

TP22

TXOUT_U0P(NC) TXOUT_U0N(NC) TXOUT_U1P(PCIE_RESET_GPIO3) TXOUT_U1N(PCIE_RESET_GPIO2) TXOUT_U2P(NC) TXOUT_U2N(NC) TXOUT_U3P(PCIE_RESET_GPIO5) TXOUT_U3N(NC)

TXCLK_LP(DBG_GPIO1) TXCLK_LN(DBG_GPIO3) TXCLK_UP(PCIE_RESET_GPIO4) TXCLK_UN(PCIE_RESET_GPIO1)

LVDS_TX_CLKLP 26 LVDS_TX_CLKLN 26

LVDS_VDDEN 26 LVDS_BLON 26

RS880M DEBUG PIN MAPPING

DEBUG_OUT0	LVDS_DIGON
DEBUG_OUT1	LVDS_ENA_BL
DEBUG_OUT2	LVDS_BLON
DEBUG_OUT3	TMDS_HPD
DEBUG_OUT4	AUX1N
DEBUG_OUT5	AUX1P
DEBUG_OUT6	HPD
DEBUG_OUT7	AUX_CAL

MICRO-STAR INT'L CO.,LTD

MS-168x

Size: Custom | Document Description: RS880M-I/F | Rev: 0A

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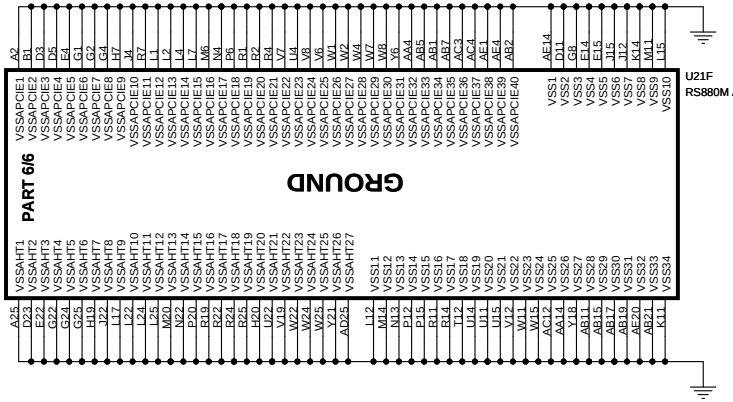


RS880M POWER TABLE

PIN NAME	RS880M	PIN NAME	RS880M
VDDHT	+1.1V	IOPLLVDD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVDD	+1.1V
VDD18_MEM	+1.8V	PLLVDD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.8V/1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDLT18	+1.8V
IOPLLVDD18	+1.8V	VDDLT33	NC

[CheckList] VDDHT can share with VDDC

[CheckList] VDDHTRX can share with VDDC

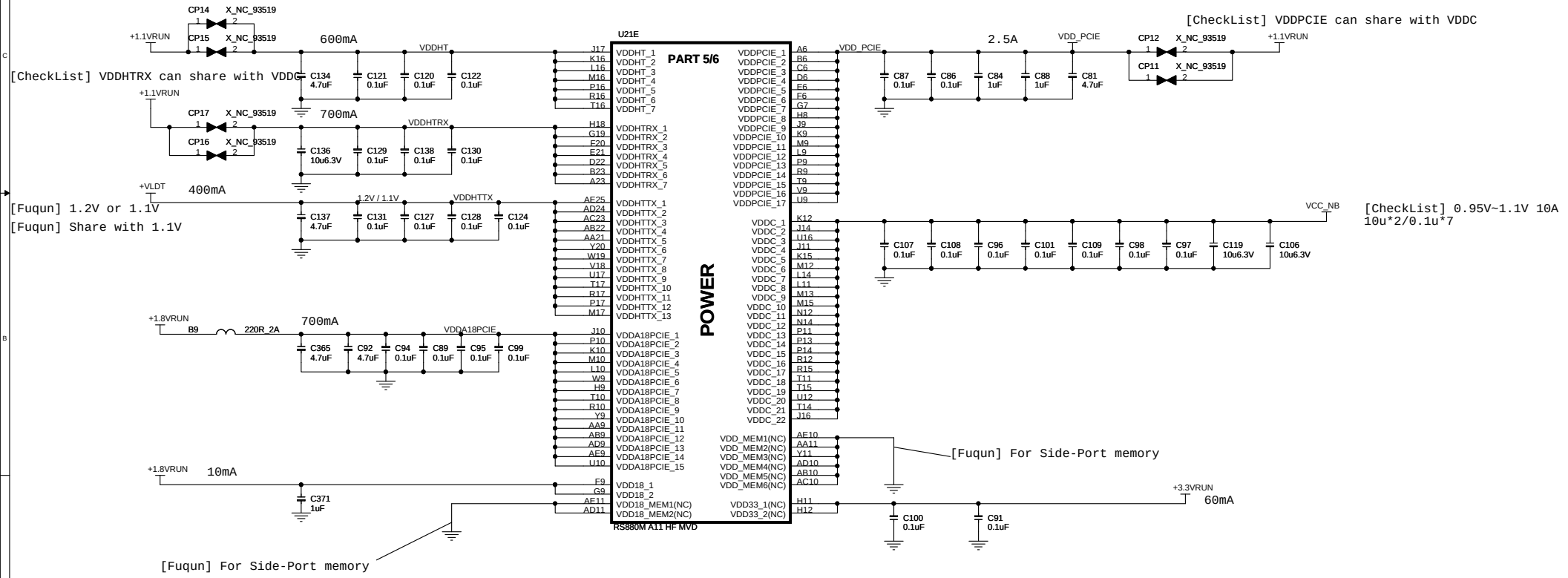
[Fuqun] 1.2V or 1.1V
[Fuqun] Share with 1.1V

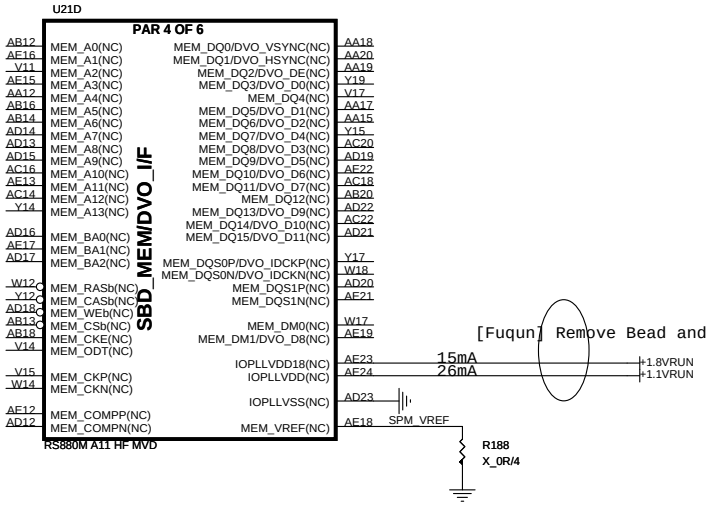
[CheckList] VDDPCIE can share with VDDC

[CheckList] 0.95V~1.1V 10A
10u*2/0.1u*7

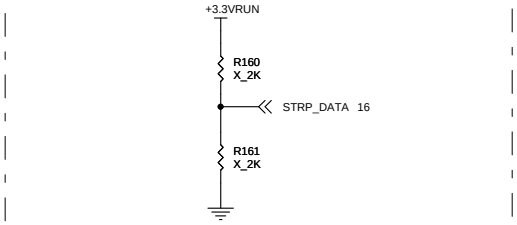
[Fuqun] For Side-Port memory

[Fuqun] For Side-Port memory



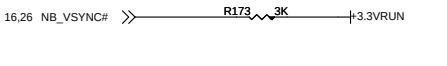


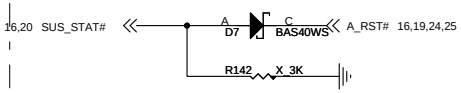
[Fuqun] Remove Bead and Cap follow CheckList



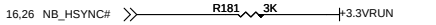
NOTE: Providing access to STRAP_DATA and I2C_CLK pins is MANDATORY.

[Fuqun] STRP_DATA pull down in Ref-schematic





[Fuqun] SUS_STAT# pull up in SB side



STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.

RS880M	
~~1 Disable~~	
~~0 Enable~~	

DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

RS880M: Enables Side port memory

RS880M:HSYNC#

Selects if Memory SIDE PORT is available or not
1 = Memory Side port Not available
0 = Memory Side port available
Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]

MICRO-STAR INT'L CO.,LTD		
MS-168x		
Size: Custom	Document Description: RS880M-STRAPS	Rev: 0A
Date: Friday, February 05, 2010	Sheet 18 of 52	

PLACE THESE PCIE AC COUPLING CAPS CLOSE TO U600

U16A

SB800 Part 1 of 5

PCI CLKS

PCI EXPRESS INTERFACES

PCI INTERFACE

CLOCK GENERATOR

LPC

CPU

RTC

SB800 A11

PEX_STD_SW#: Low - Standard(desktop) Swing Level
Input(3T) - Low Swing Level Mode (Default)

NOTE: SB8XX ONLY SUPPORTS 2 GPP PORT 2 AND 3 IS NOT SUPPORTED.

NOTE: The 0R serial resistor on SB CLK pair must share Pad with the serial resistor close to U800

[Fuqun] Y and C P/N?

SB_GPP GFX_CLK	DEVICE MXM3.0	CLKREQ# CLK_REQG#
0	EXPRESS	0
1	PE0	1
2	PE2	2
3	LAN	3
4	PE1	4
5	X4DT	5
6	PE3	6
7	USB3.0	7
8	1394	8

PLACE THESE COMPONENTS CLOSE TO U600, AND USE GROUND GUARD FOR 32K_X1 AND 32K_X2

[Fuqun] Y and C P/N?

POWER EXPRESS SUPPORT

PE_GPIO0 MXM RESET	H: Enable
PE_GPIO1 MXM POWER ENABLE	H: Enable
PE_GPIO2 MODE SWITCH(BY NB)	H:MXM L:NB
TMDS_HPD0 MXM HOT PLUG	

MICRO-STAR INT'L CO.,LTD

MS-168x

Size	Document Description	Rev
Custom	SB820-PCIE/PCI/CPU/LPC/CLK	0A

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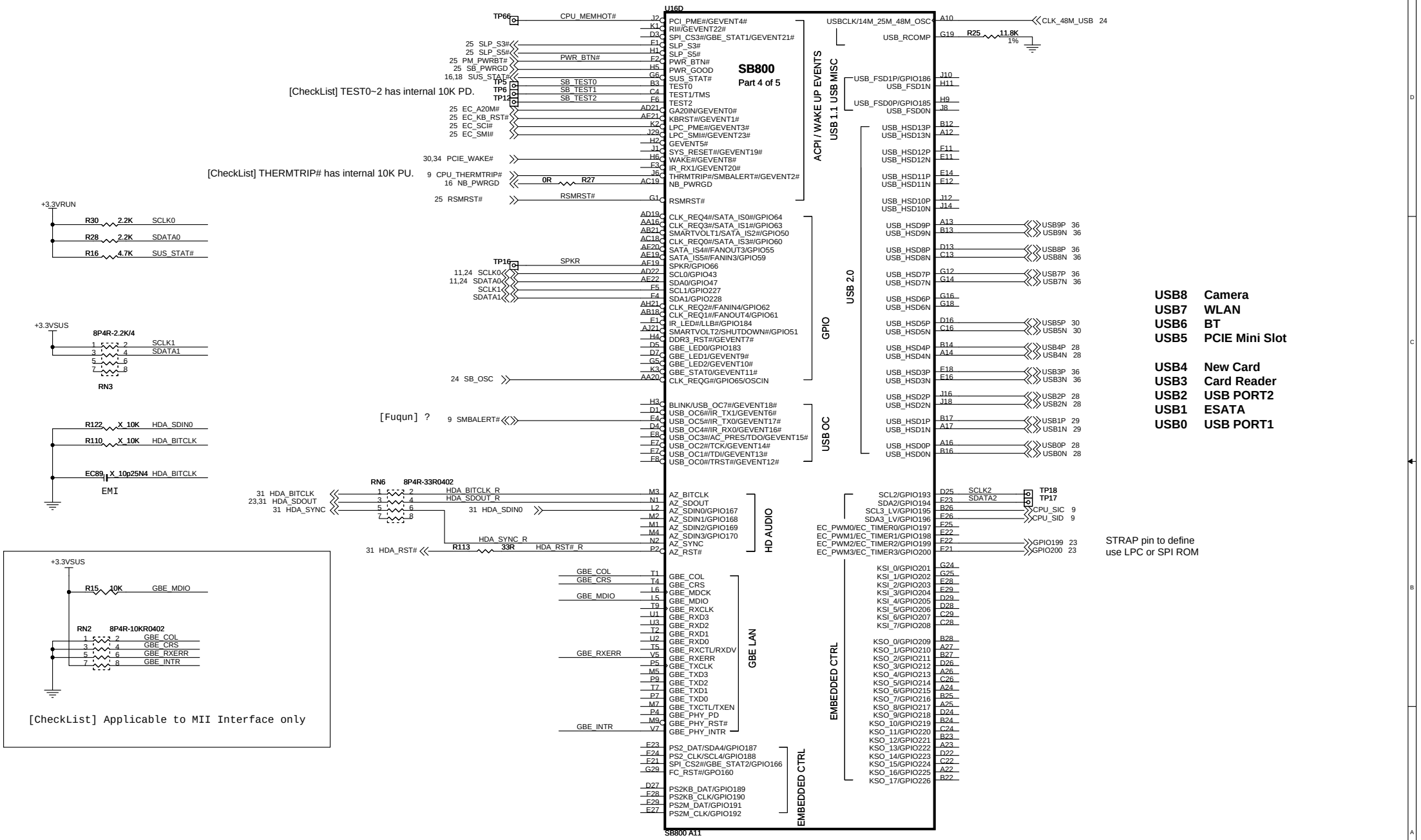

MICRO-STAR INT'L CO.,LTD	
MS-168x	
Size: Custom	Document Description: SB820-GPIO/USB/AZ
Rev: 0A	
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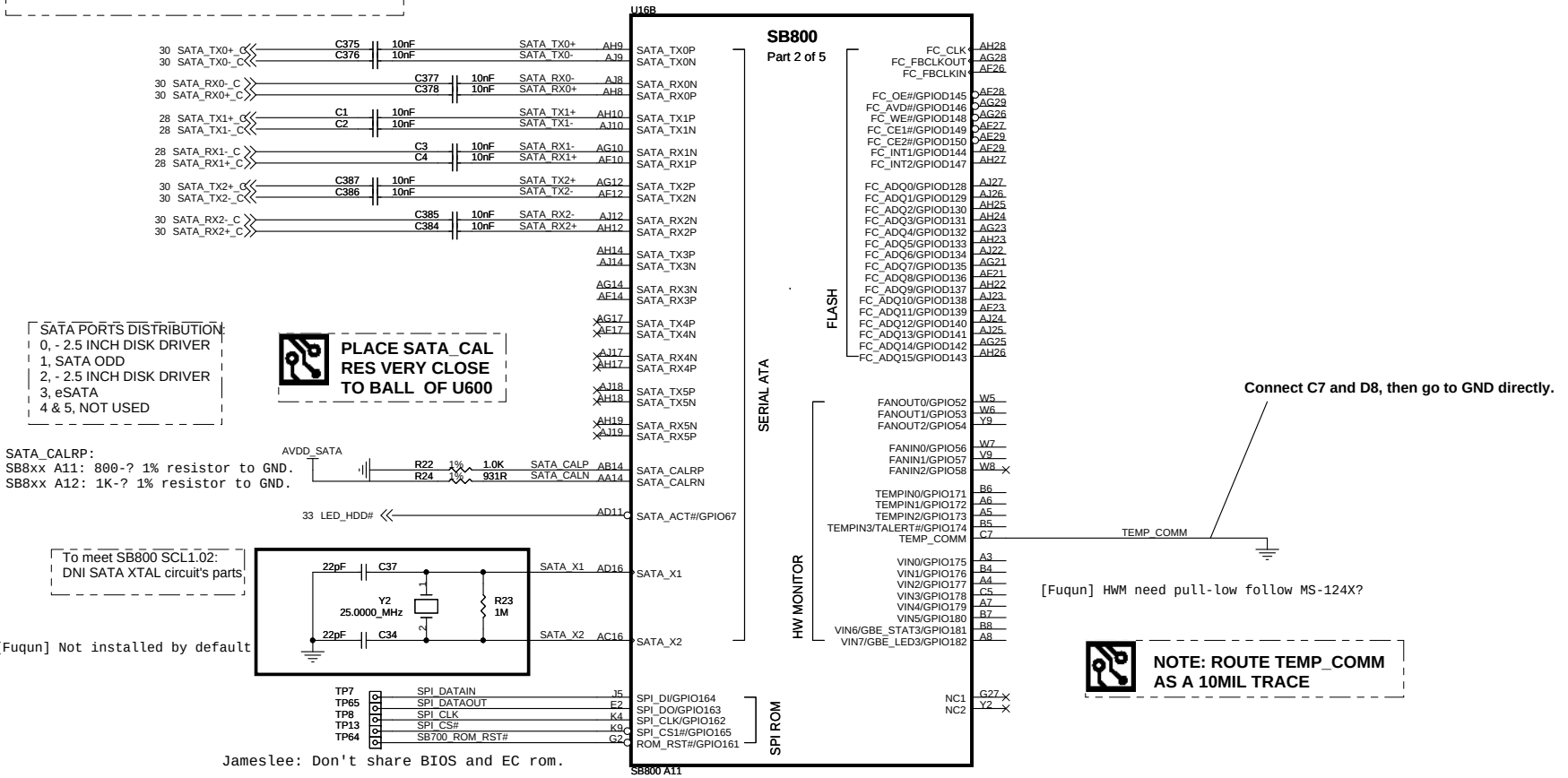
SATA trace should use only 1via on the trace. customers can use 2vias with GND via within 150mils of signal via as long as they can ensure that their platform meets SATA logo requirements. Return loss is expected to get affected with 2 vias. AMD platforms are validated with one via only



SATA PORTS DISTRIBUTION:
0, - 2.5 INCH DISK DRIVER
1, SATA ODD
2, - 2.5 INCH DISK DRIVER
3, eSATA
4 & 5, NOT USED

PLACE SATA_CAL RES VERY CLOSE TO BALL OF U600

SATA_CALRP:
SB8xx A11: 800-? 1% resistor to GND.
SB8xx A12: 1K-? 1% resistor to GND.

To meet SB800 SCL1.02:
DNI SATA XTAL circuit's parts

[Fuqun] Not installed by default

Jameslee: Don't share BIOS and EC rom.

Connect C7 and D8, then go to GND directly.

TEMP_COMM

[Fuqun] HWM need pull-low follow MS-124X?

NOTE: ROUTE TEMP_COMM AS A 10MIL TRACE

MICRO-STAR INT'L CO.,LTD		
MS-168x		
Size: Custom	Document Description: SB820-SATA/IDE/SPI/HWM	Rev: 0A
Date: Friday, February 05, 2010	Sheet 21 of 52	

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

1*22U/3*0.1u

1*10U/2*1U/2*0.1u

SB800 Part 3 of 5

POWER

GROUND

Part 5 of 5

[Fuqun] GPIOD not used-->Tied to GND

[Fuqun] No 42ohm bead, Use 30ohm

[CheckList] Bead-- 42 Ω @ 100 MHz/4A/ ≤ 0.01 Ω

[CheckList] Bead-- 42 Ω @ 100 MHz/4A/ ≤ 0.01 Ω

GbE Controller Not Enabled: Connected to GND

Updated on Rev2.0

[CheckList] No bead?

USB S3-S5 Wake Implemented: Tied to +3.3V_S5.
USB S3-only Wake Implemented: Tied to +3.3V_S3.
USB S3-S5 Wake Not Implemented: Tied to +3.3V_S3.

USB S3-S5 Wake Implemented: Tied to +1.1V_S5.
USB S3-only Wake Implemented: Tied to +1.1V_S3.
USB S3-S5 Wake Not Implemented: Tied to +1.1V_S3.

Wake on LAN supported: Tied to a +3.3V_S5 rail

To meet SB800 SCL1.02:
Separate ferrite bead is not required for VDDPL_33_USB_S, Del B603/600ohm bead.

HWM not Implemented and not used as GPIOs: Bead and Decoupling caps not used.

[CheckList] 1.5VSUS or 3.3VSUS

Company	MICRO-STAR INT'L CO.,LTD
Model	MS-168x
Size	Custom
Document Description	SB820-POWER
Rev	0A
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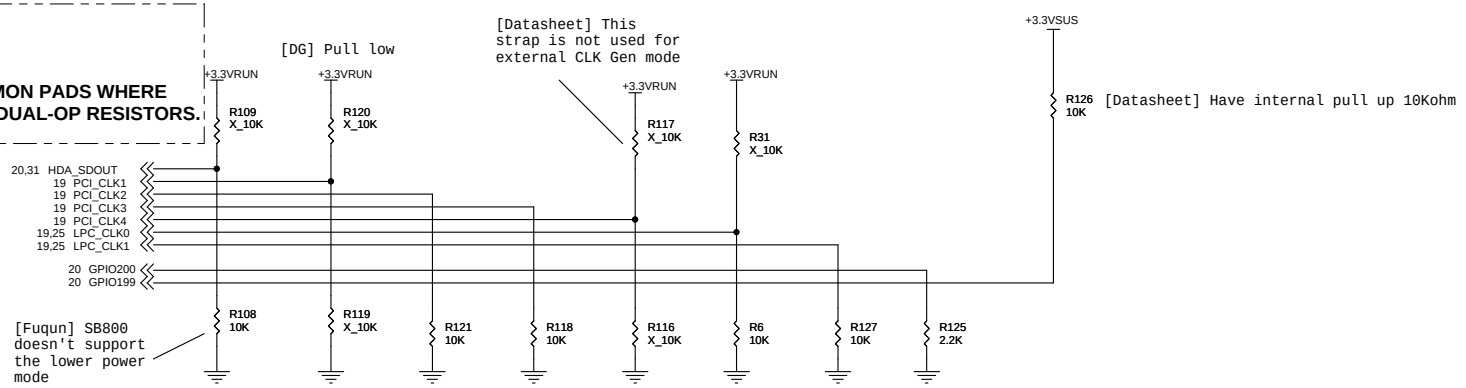
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



REQUIRED STRAPS

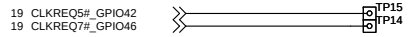
	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200 GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM (Default) L,L = FWH ROM

PCI_CLK1(SMSC_CLK)-->SB820M: Only provision for pull-down is required, not installed by default--checklist

[Fuqun] GPIO199 NC in checklist

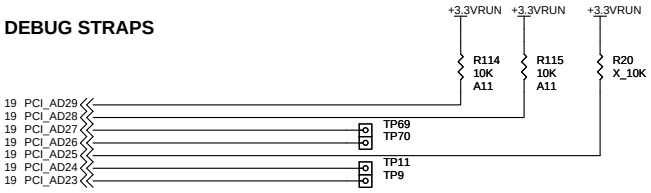
[Fuqun] PCI_CLK4 high or low?

SB PCIE EEPROM STRAPS



SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

DEBUG STRAPS



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

PCI23/24/26/27 have internal pull high 15kohm,But PCI25?
Why PCI28/29 pull high?

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MS-168x

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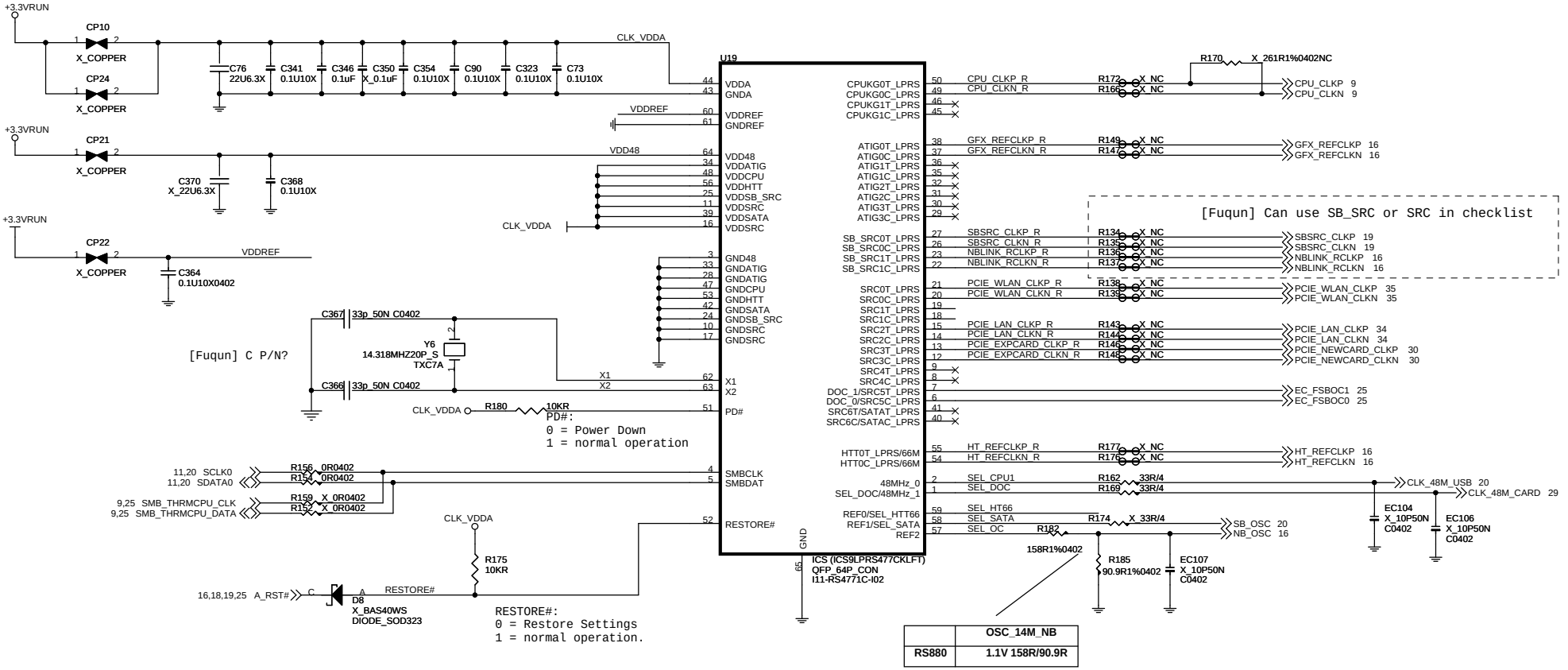
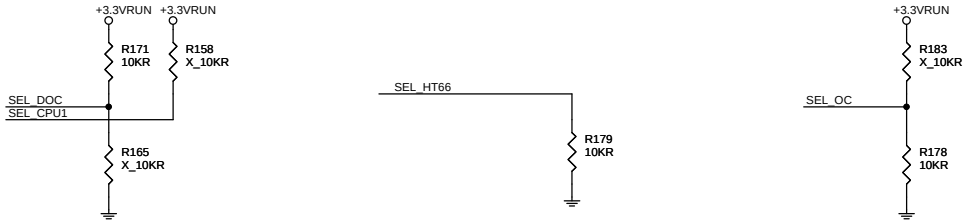
1- PLACE ALL SERIAL TERMINATION
RESISTORS CLOSE TO U11

2- PUT DECOUPLING CAPS CLOSE TO U11
POWER PIN



	OSC_14M_NB
RS880	1.1V 158R/90.9R



SEL_DOC/48MHz-1	1	DOC INPUT
	* 0	SRCCLK5
SEL_CPU1/48MHz-2	1	SRCCLK7
	* 0	CPUKG1

* default

SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0	100 MHz differential HTT clock
SEL_SATA	1	100MHz differential spreading SRC clock
	0	100 MHz spreading differential SATA clock

SEL_OC	1	Higher overclocking ability
	* 0	limited overclocking ability

* default

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

* RS780 can be used as clock buffer to output two PCIE referecence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.

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Custom	CLK GEN	0A

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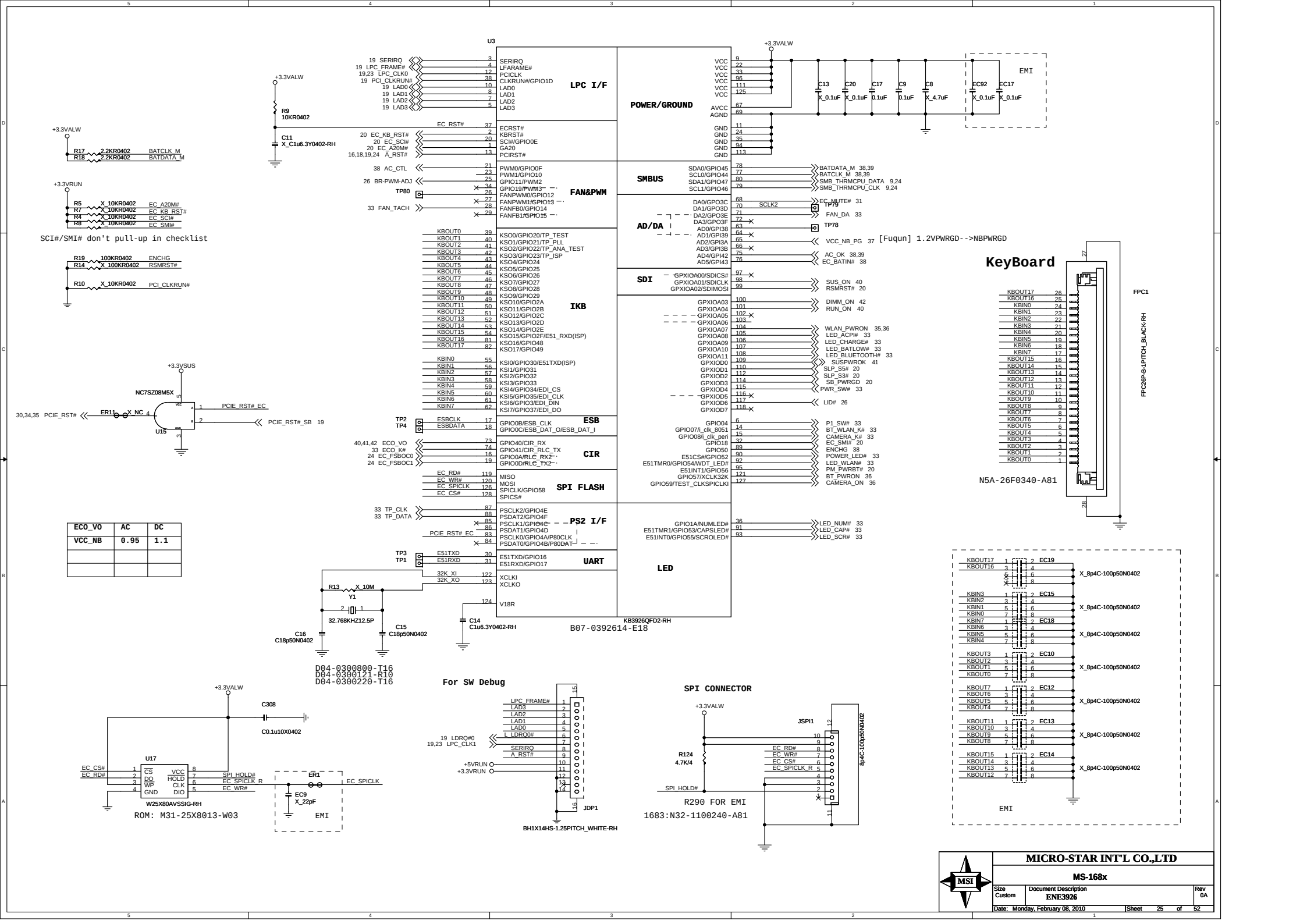
U3
LPC I/F
SERIRQ
LFRAME#
PCICLK
CLKRUN#/GPIO1D
LAD0
LAD1
LAD2
LAD3
ECRST#
KBRST#
SCI#/GPIO0E
GA20
PCIRST#
FAN&PWM
PWM0/GPIO0F
PWM1/GPIO10
GPIO11/PWM2
GPIO19/PWM3
FANPWM0/GPIO12
FANPWM1/GPIO13
FANFB0/GPIO14
FANFB1/GPIO15
IKB
KSO0/GPIO20/TP_TEST
KSO1/GPIO21/TP_PLL
KSO2/GPIO22/TP_ANA_TEST
KSO3/GPIO23/TP_ISP
KSO4/GPIO24
KSO5/GPIO25
KSO6/GPIO26
KSO7/GPIO27
KSO8/GPIO28
KSO9/GPIO29
KSO10/GPIO2A
KSO11/GPIO2B
KSO12/GPIO2C
KSO13/GPIO2D
KSO14/GPIO2E
KSO15/GPIO2F/E51_RXD(ISP)
KSO16/GPIO48
KSO17/GPIO49
KSI0/GPIO30/E51TXD(ISP)
KSI1/GPIO31
KSI2/GPIO32
KSI3/GPIO33
KSI4/GPIO34/EDI_CS
KSI5/GPIO35/EDI_CLK
KSI6/GPIO3/EDI_DIN
KSI7/GPIO37/EDI_DO
ESB
GPIO0B/ESB_CLK
GPIO0C/ESB_DAT_O/ESB_DAT_I
CIR
GPIO40/CIR_RX
GPIO41/CIR_RLC_TX
GPIO0A/RLC_RX2
GPIO0D/RLC_TX2
SPI FLASH
MISO
MOSI
SPICLK/GPIO58
SPICS#
PS2 I/F
PSCLK2/GPIO4E
PSDAT2/GPIO4F
PSCLK1/GPIO4C
PSDAT1/GPIO4D
PSCLK0/GPIO4A/P80CLK
PSDAT0/GPIO4B/P80DAT
UART
E51TXD/GPIO16
E51RXD/GPIO17
XCLKI
XCLKO
V18R
KB3926QFD2-RH
POWER/GROUND
VCC
AVCC
AGND
GND
SMBUS
SDA0/GPIO45
SCL0/GPIO44
SDA1/GPIO47
SCL1/GPIO46
AD/DA
DA0/GPO3C
DA1/GPO3D
DA2/GPO3E
DA3/GPO3F
AD0/GPI38
AD1/GPI39
AD2/GPI3A
AD3/GPI3B
AD4/GPI42
AD5/GPI43
SDI
GPXIOA00/SDICS#
GPXIOA01/SDICLK
GPXIOA02/SDIMOSI
GPXIOA03
GPXIOA04
GPXIOA05
GPXIOA06
GPXIOA07
GPXIOA08
GPXIOA09
GPXIOA10
GPXIOA11
GPXIOD0
GPXIOD1
GPXIOD2
GPXIOD3
GPXIOD4
GPXIOD5
GPXIOD6
GPXIOD7
LED
GPIO04
GPIO07/I_clk_8051
GPIO08/I_clk_peri
GPIO18
GPIO50
E51CS#/GPIO52
E51TMR0/GPIO54/WDT_LED#
E51INT1/GPIO56
GPIO57/XCLK32K
GPIO59/TEST_CLKSPICLKI
GPIO1A/NUMLED#
E51TMR1/GPIO53/CAPSLED#
E51INT0/GPIO55/SCROLED#
+3.3VALW
+3.3VRUN
+3.3VSUS
EMI
C13 X_0.1uF
C20 X_0.1uF
C17 0.1uF
C9 0.1uF
C8 X_4.7uF
EC92 X_0.1uF
EC17 X_0.1uF
R9 10KR0402
C11 X_C1u6.3Y0402-RH
R17 2.2KR0402 BATCLK_M
R18 2.2KR0402 BATDATA_M
R5 X_10KR0402 EC_A20M#
R7 X_10KR0402 EC_KB_RST#
R4 X_10KR0402 EC_SCI#
R8 X_10KR0402 EC_SMI#
SCI#/SMI# don't pull-up in checklist
R19 100KR0402 ENCHG
R14 X_100KR0402 RSMRST#
R10 X_10KR0402 PCI_CLKRUN#
[Fuqun] 1.2VPWRGD-->NBPWRGD
KeyBoard
FPC1
FPC28P-B-1PITCH_BLACK-RH
N5A-26F0340-A81
NC7SZ08M5X
U15
ER11 X_NC
PCIE_RST# EC
PCIE_RST#_SB 19
TP2
TP4
TP3
TP1
R13 X_10M
Y1
32.768KHZ12.5P
C16 C18p50N0402
C15 C18p50N0402
C14 C1u6.3Y0402-RH
B07-0392614-E18
D04-0300800-T16
D04-0300121-R10
D04-0300220-T16
ECO_VO | AC | DC
VCC_NB | 0.95 | 1.1
X_8p4C-100p50N0402
EC19
EC15
EC18
EC10
EC12
EC13
EC14
C308
C0.1u10X0402
U17
W25X80AVSSIG-RH
ROM: M31-25X8013-W03
ER1
EC9 X_22pF
EMI
For SW Debug
JDP1
BH1X14HS-1.25PITCH_WHITE-RH
SPI CONNECTOR
JSPI1
8p4C-100p50N0402
R124 4.7K/4
R290 FOR EMI
1683:N32-1100240-A81
MICRO-STAR INT'L CO.,LTD
MS-168x
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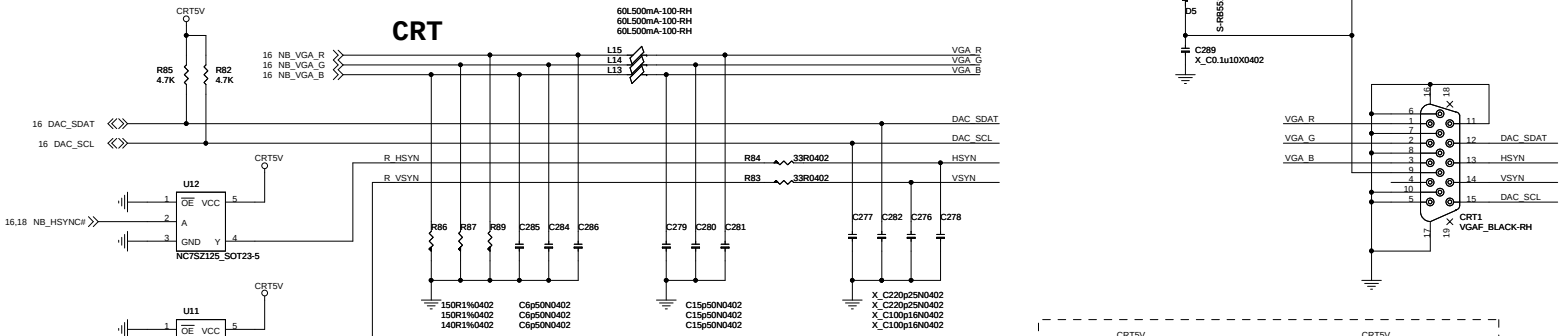
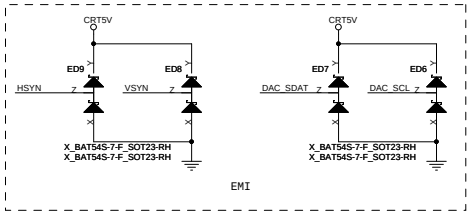
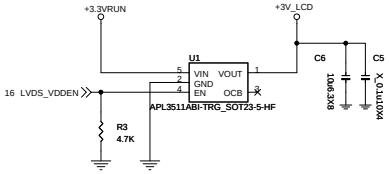
CRT



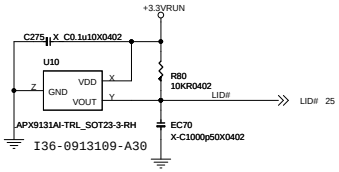


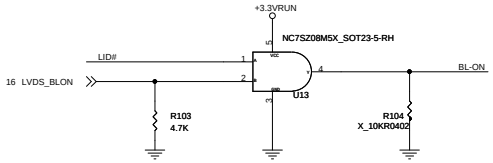
LVDS

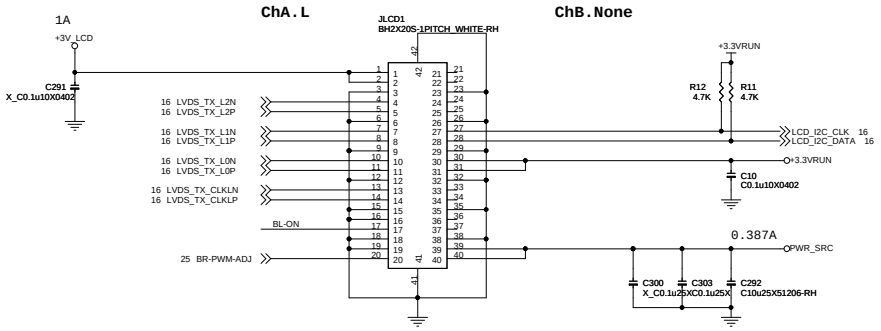
LVDS POWER 3.3V

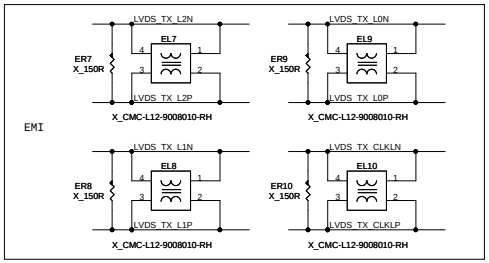


Hall Switch









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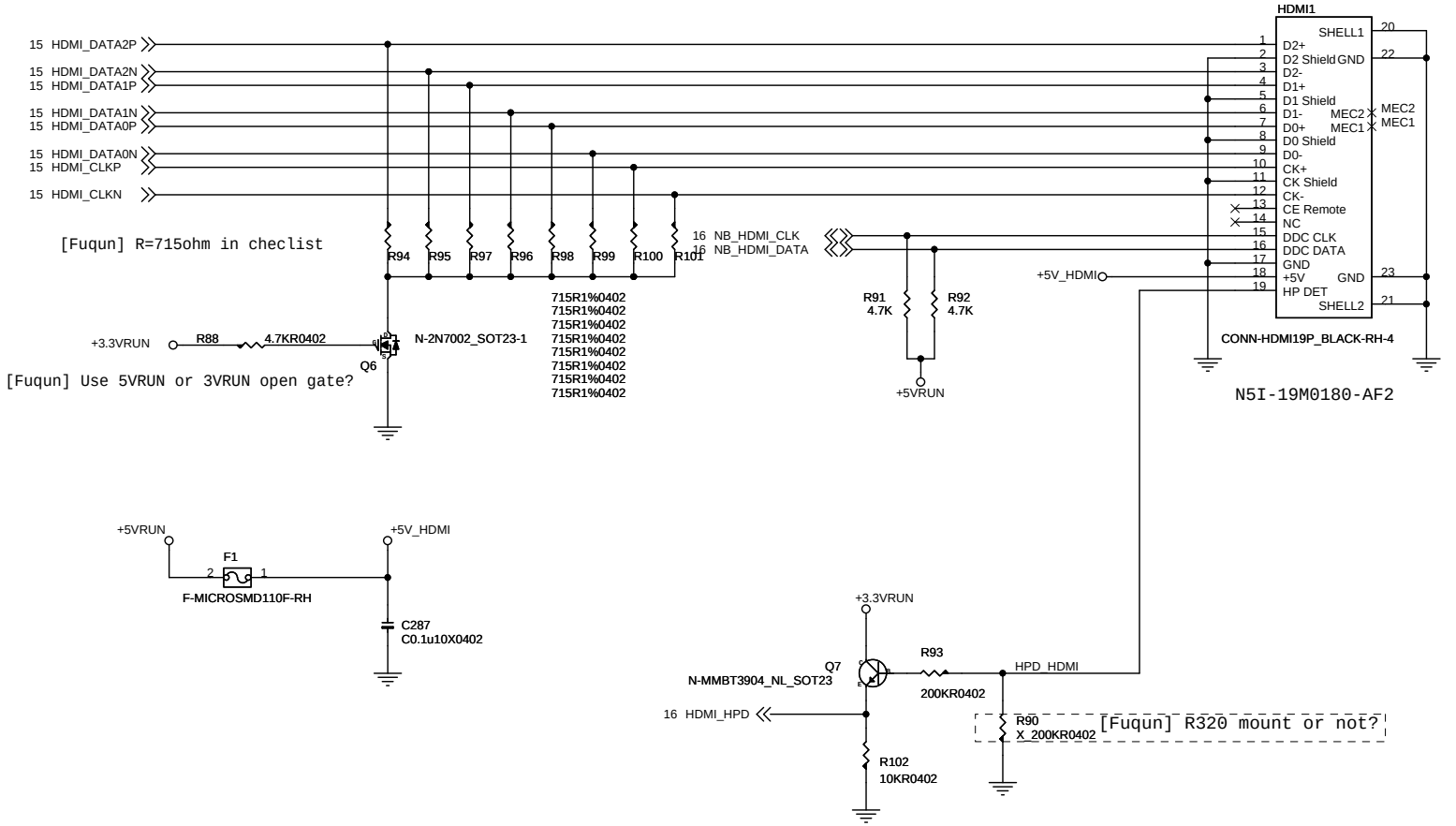
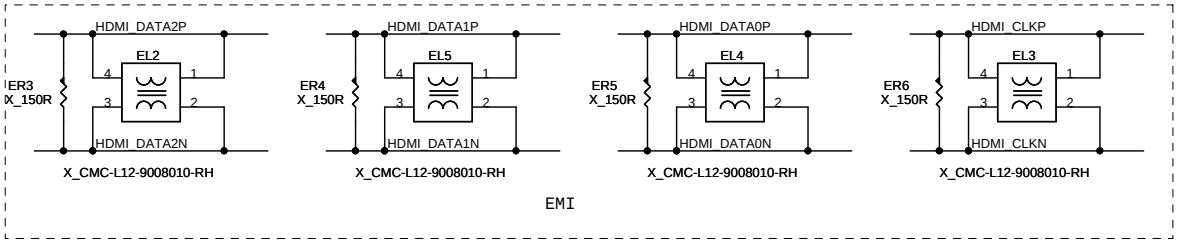
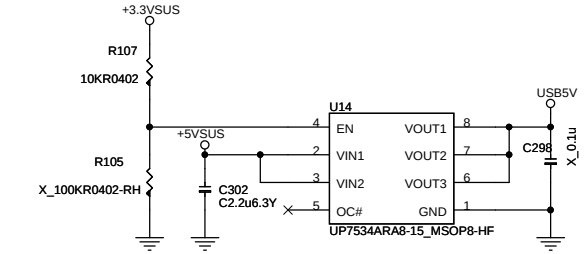
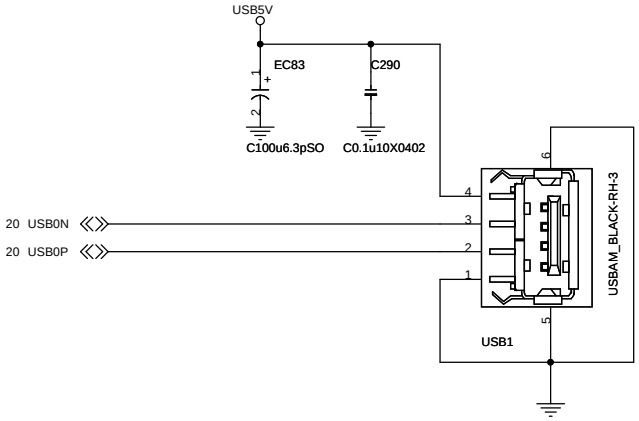
HDMI

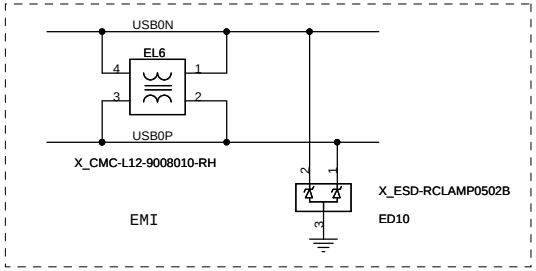


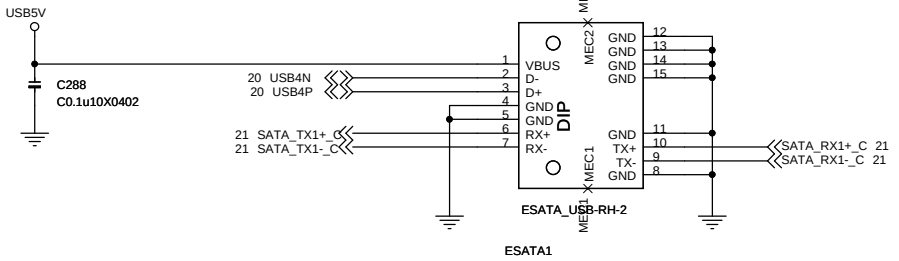


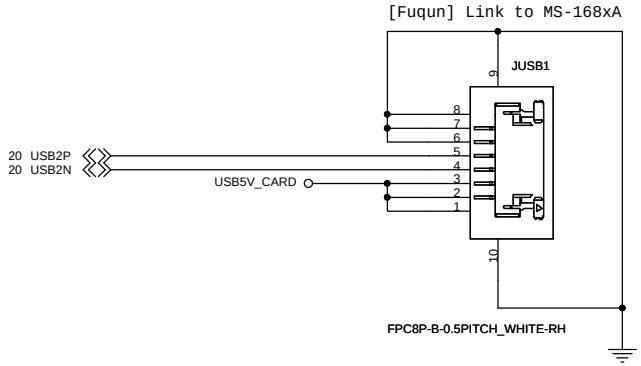
MSI	MICRO-STAR INT'L CO.,LTD		
	MS-168x		
Size B	Document Description HDMI		Rev 0A
Date: Saturday, February 20, 2010		Sheet 27 of 52	

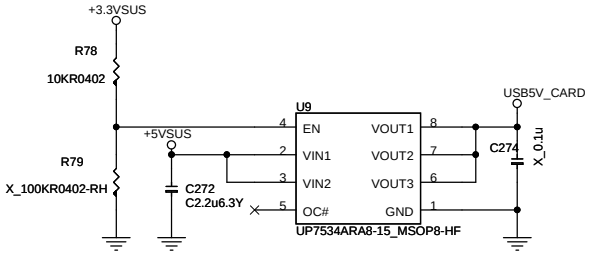












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	MS-168x	
Size: Custom	Document Description: USB and ESATA	Rev: 0A
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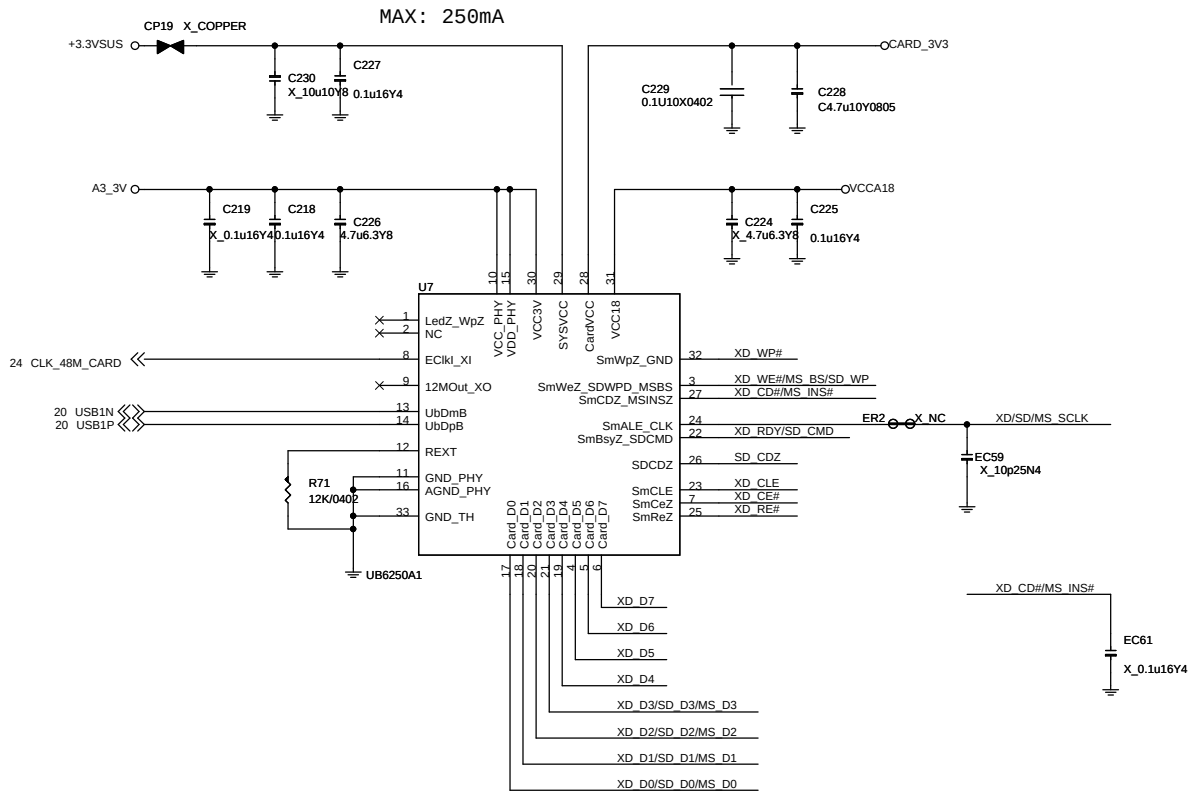
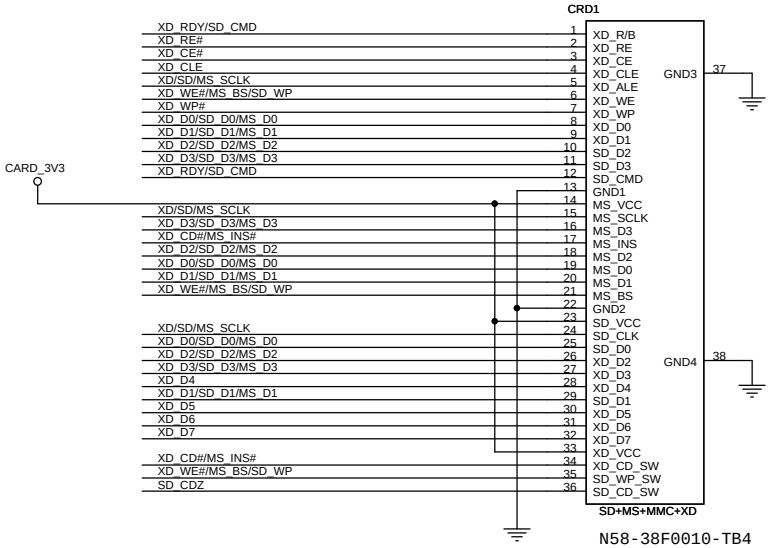
Card Reader controller

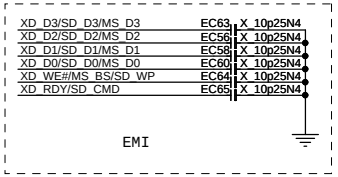


Flash Card Socket



N58-38F0010-TB4

ENE UB6250 USB20 Flash Card Reader Controller						
Pins for SD, MMC, MS, and xD memory cards						
Name	No	I/O	XD	SD	MMC	MS
xDCeZ	7	O	xD card EN			
xDCle	23	O	xD CMD latch EN			
xDAle	24	O	xD ADDR latch EN	SD clock	MMC clock	MS serial clock
xDBsyZ	22	B	xD Ready/busy	SD CMD/response	MMC CMD/response	
xDData0	17	B	xD D0	SD D0	MMC D0	MS D0
xDData1	18	B	xD D1	SD D1	MMC D1	MS D1
xDData2	20	B	xD D2	SD D2	MMC D2	MS D2
xDData3	21	B	xD D3	SD D3	MMC D3	MS D3
xDData4	19	B	xD D4		MMC D4	MS D4
xDData5	4	B	xD D5		MMC D5	MS D5
xDData6	5	B	xD D6		MMC D6	MS D6
xDData7	6	B	xD D7		MMC D7	MS D7
xDWeZ	3	B	xD W EN	SD WP		MS Busy
xDReZ	25	O	xD R EN			
xDWpZ	32	O	xD WP			
SdCdZ	26	I		SD CD	MMC CD	
xDCdZ	27	I	xD CD			MS CD



MICRO-STAR INT'L CO.,LTD

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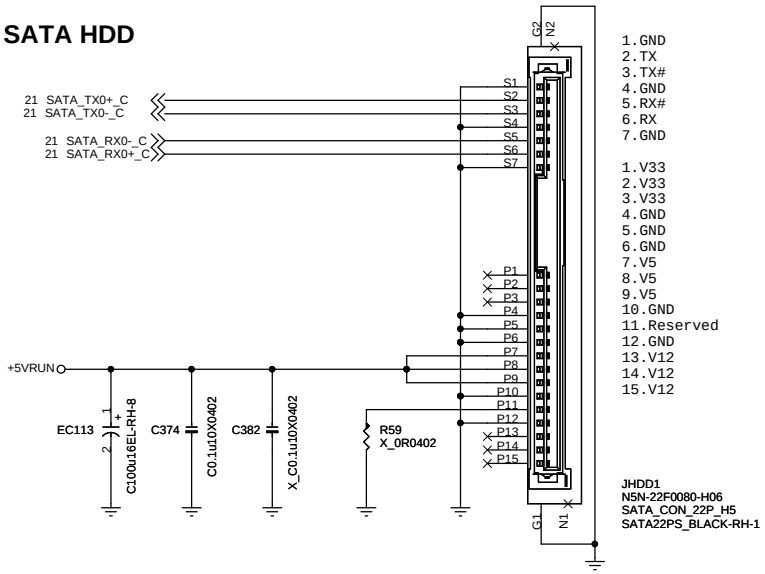
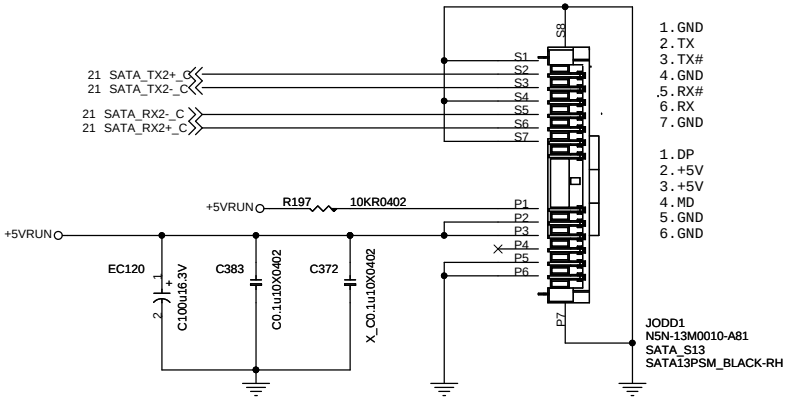
SATA HDD

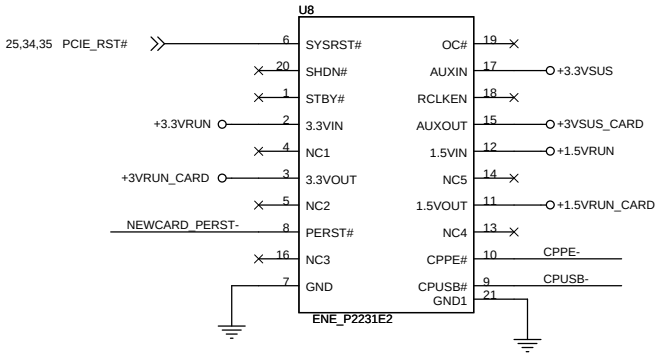


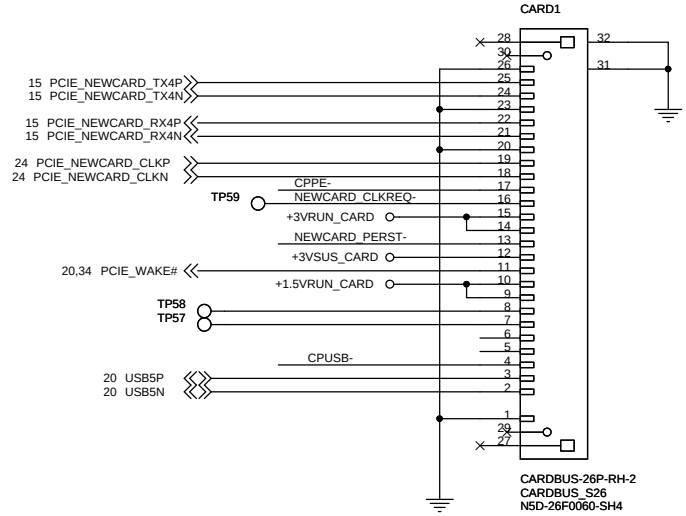
SATA ODD



NEW CARD

[CheckList] PCIE_RST# and GPIO_RST#-->PCIE device





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	MS-168x	
Size: Custom	Document Description: HDD/ODD/NEW CARD	Rev: 0A
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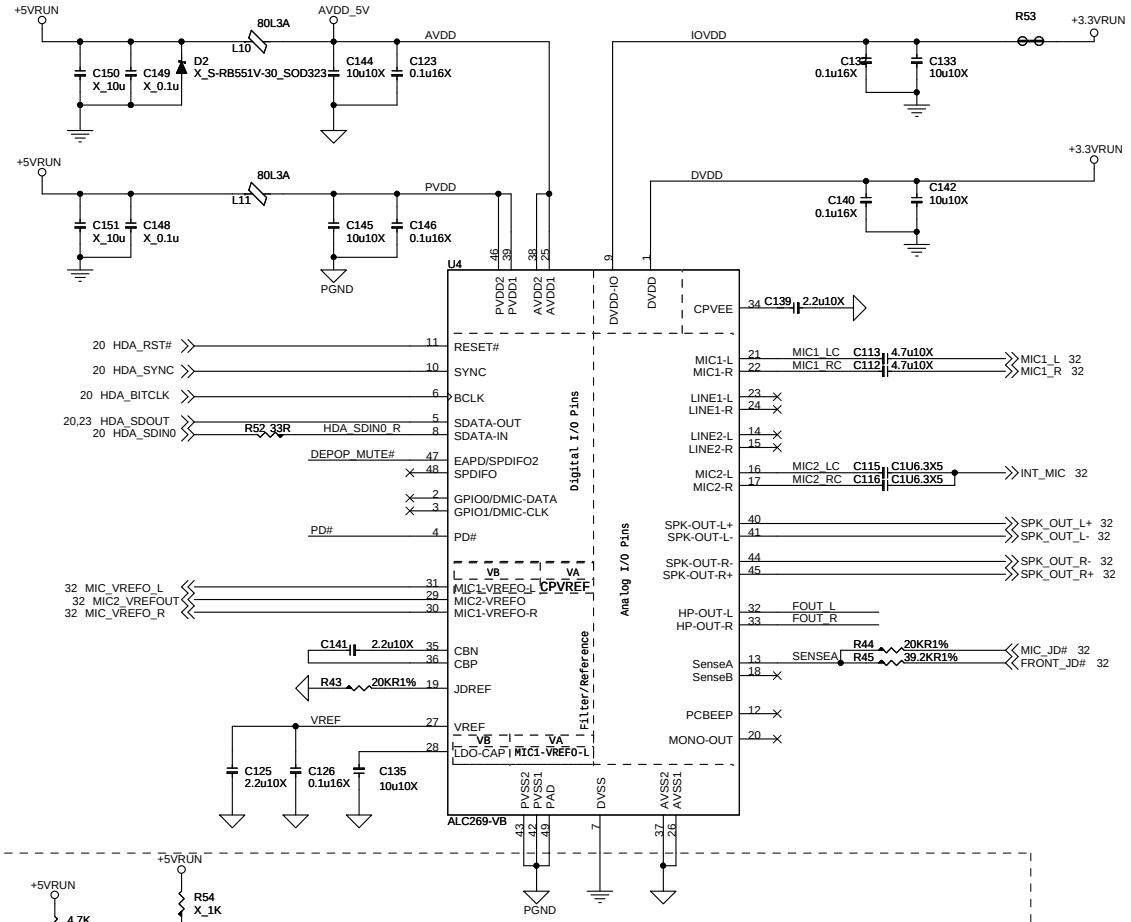

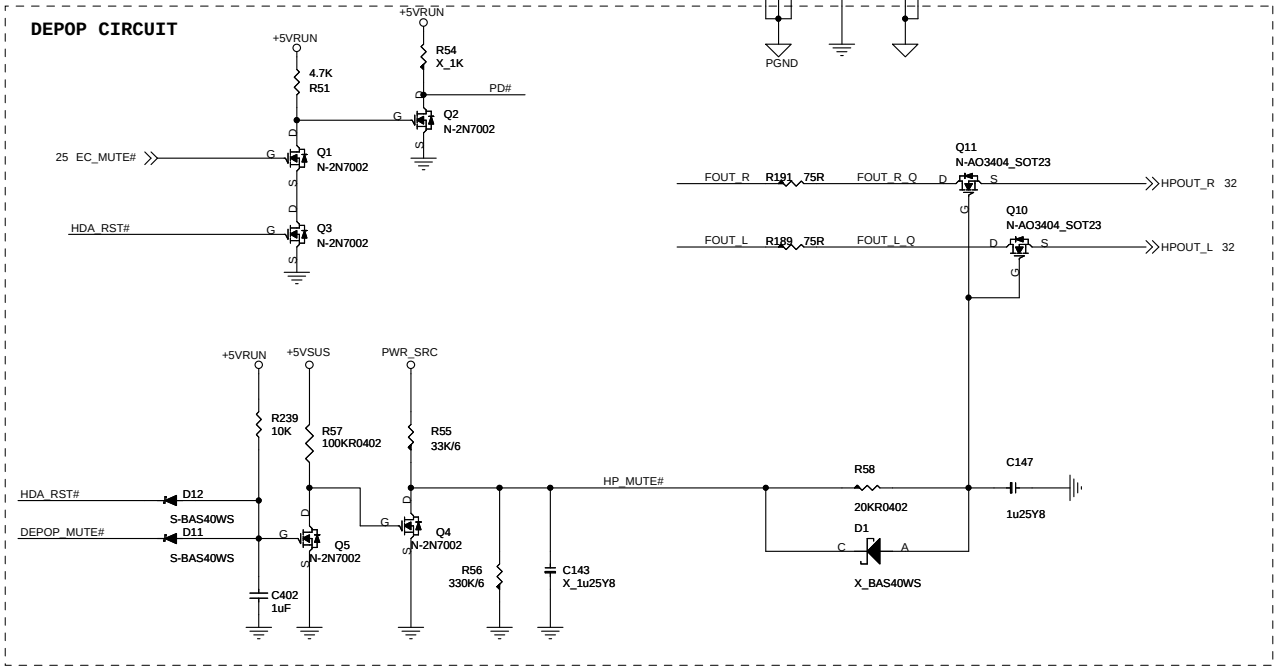

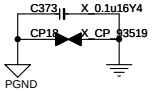

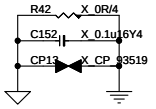

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-168x	
Size: Custom	Document Description: ALC662	Rev: 0A
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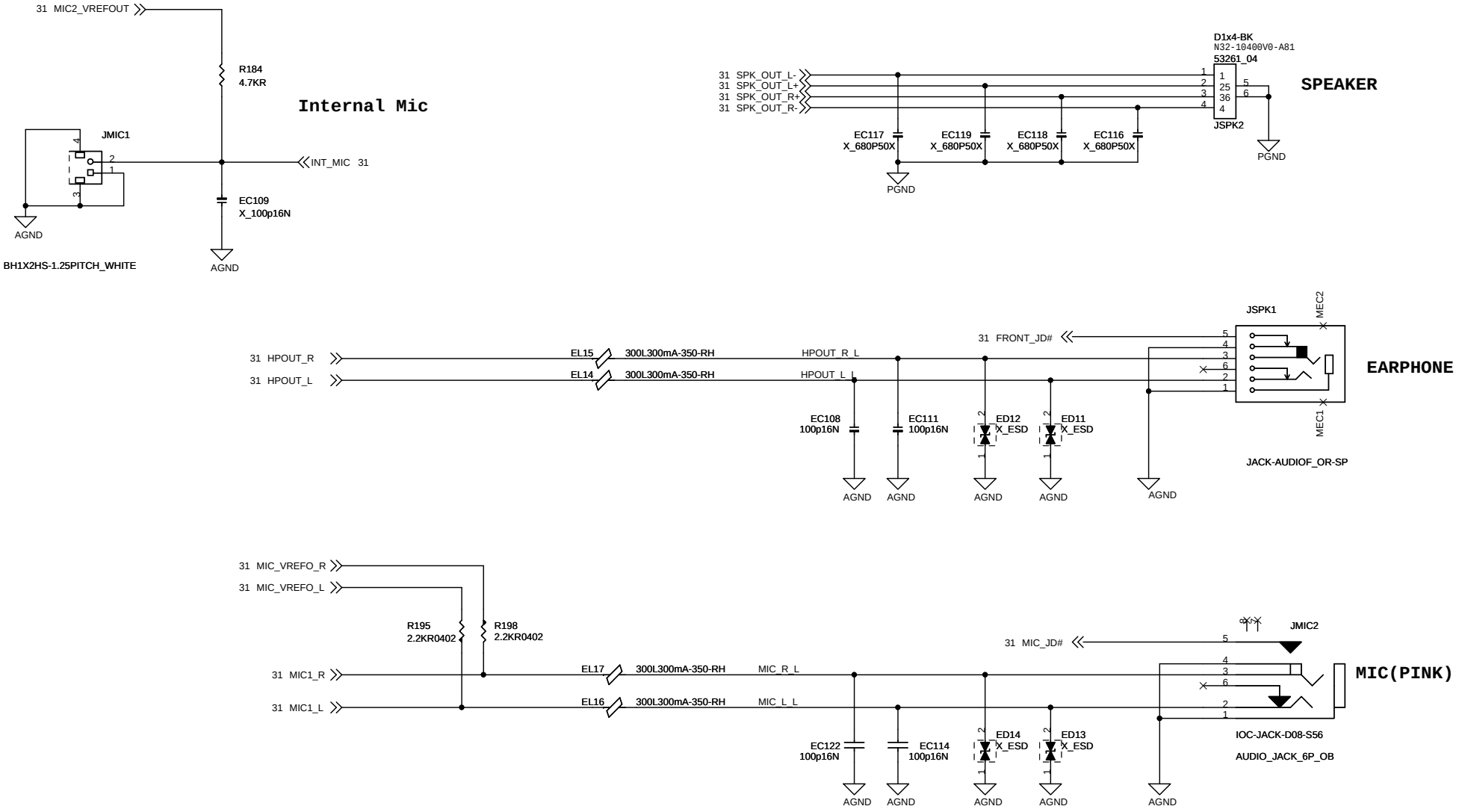

MSI	MICRO-STAR INT'L CO.,LTD		
	MS-168x		
Size B	Document Description SPK / HP / MIC		Rev 0A
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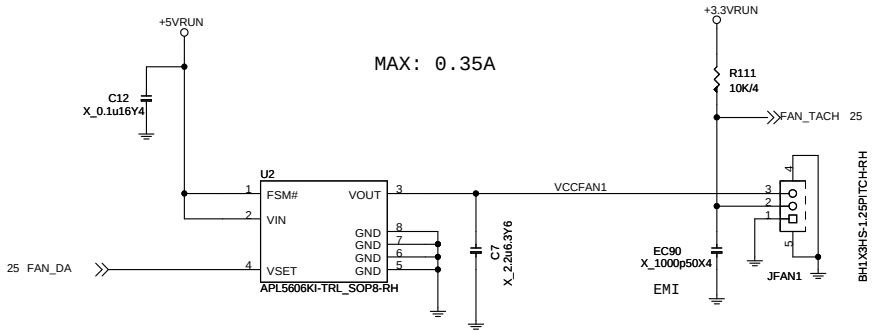
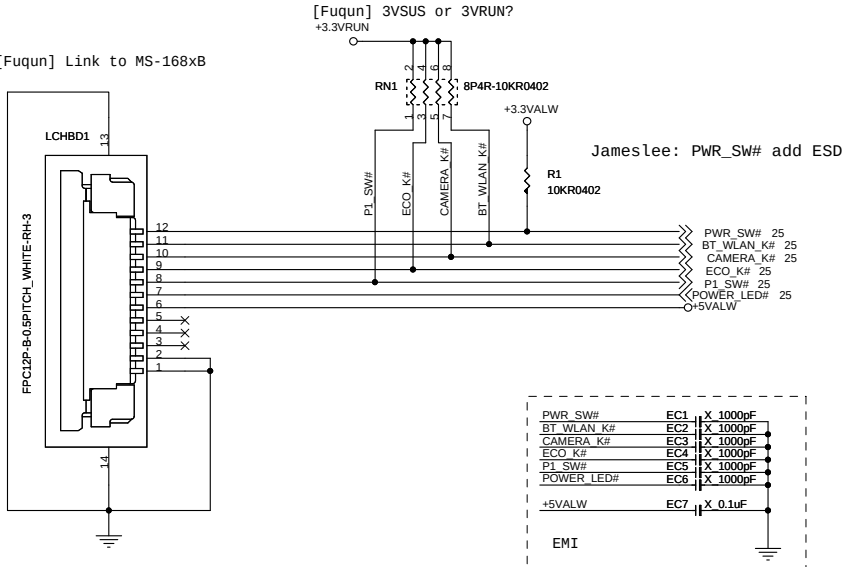
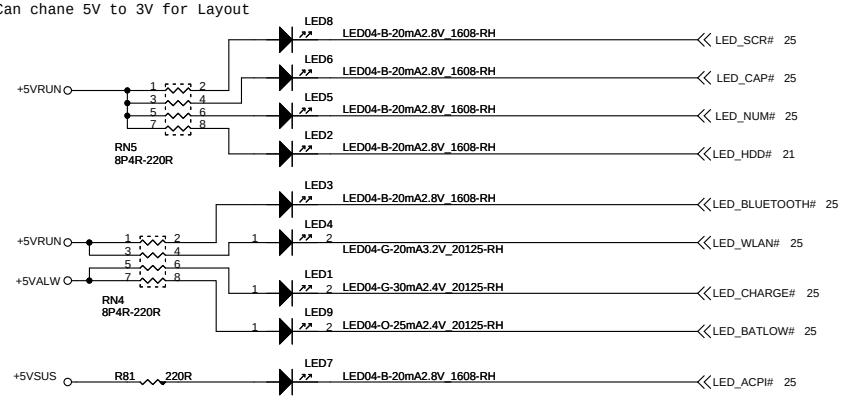
FAN

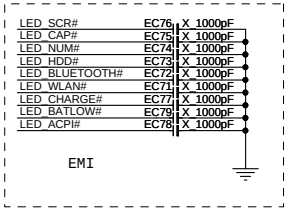


[Fuqun] P/N follow 1684 or 1688?

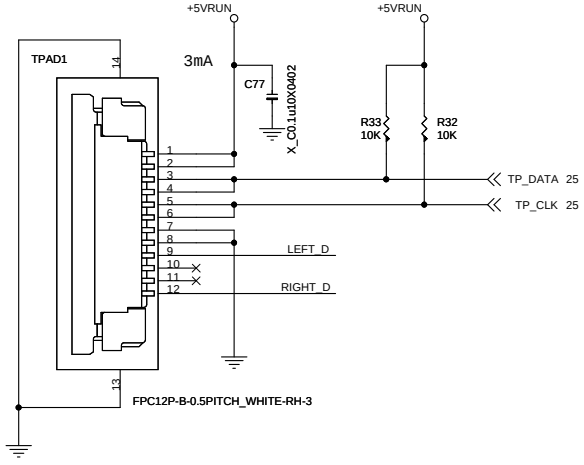


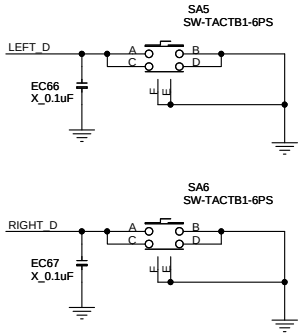
[Fuqun] Can chane 5V to 3V for Layout

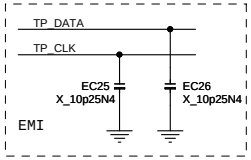




TOUCH PAD







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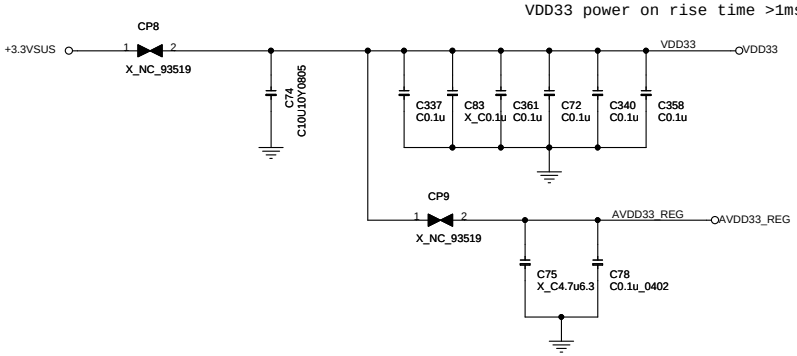
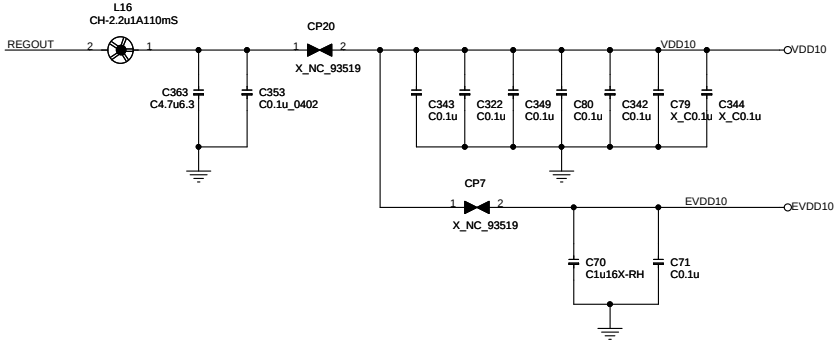
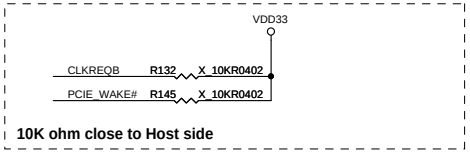
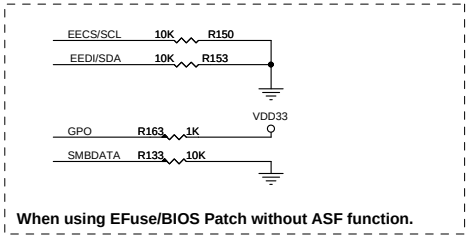
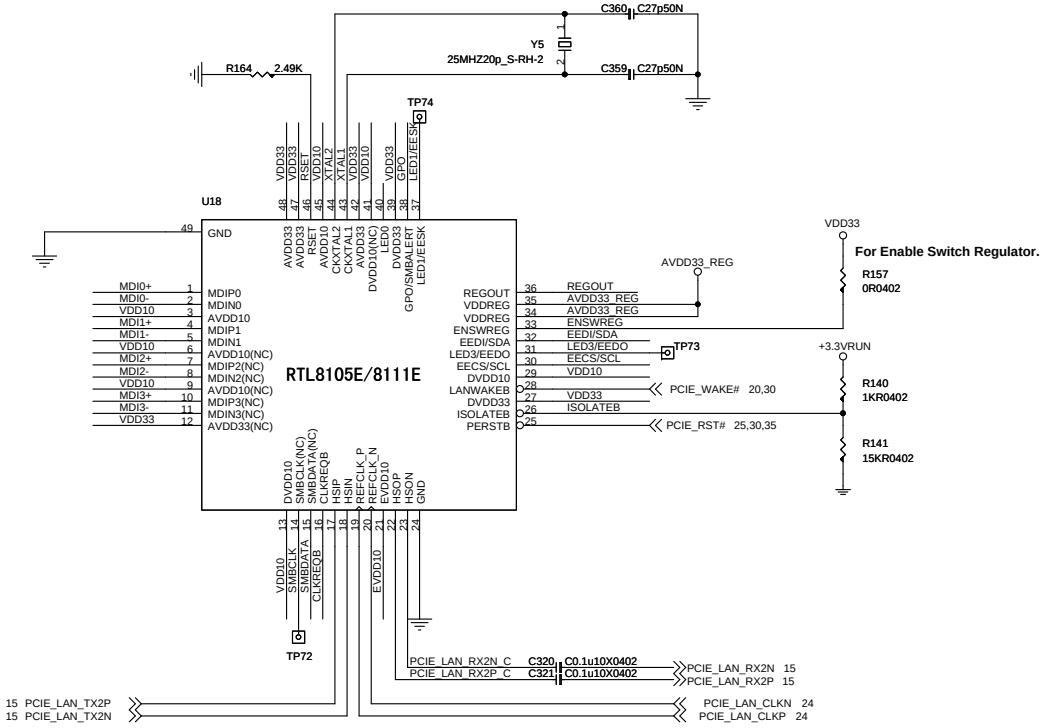
VDD33 power on rise time >1ms



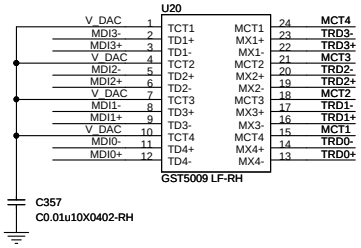


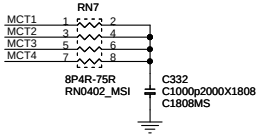




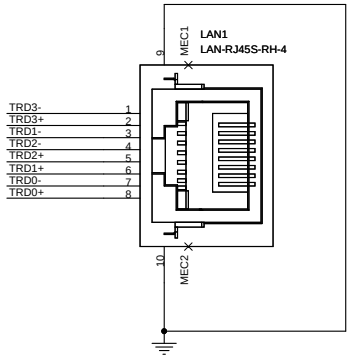


LAN MAGNETICS





[Fuqun] For P/N and pin define?
Follow 1684 or 1688?



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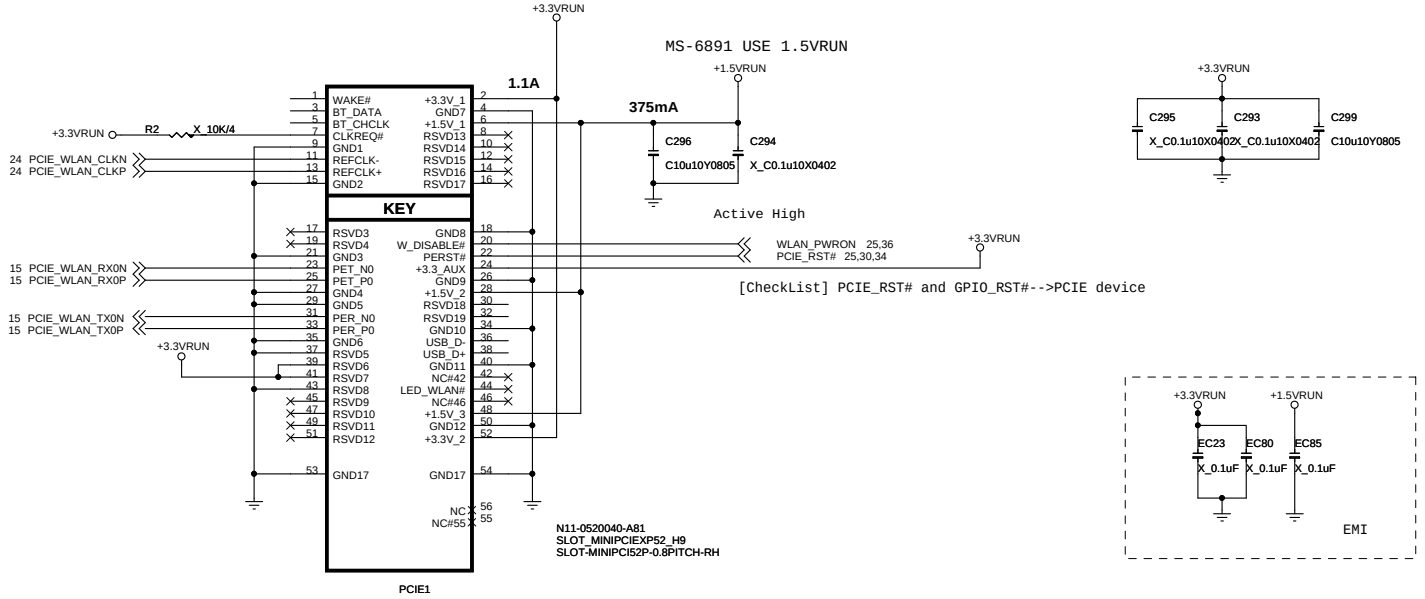
WLAN CARD



MICRO-STAR INT'L CO.,LTD		
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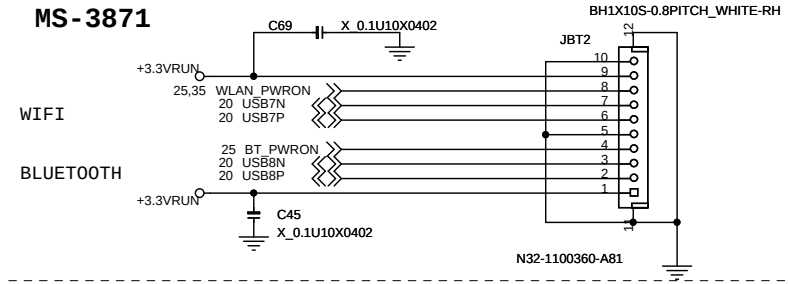
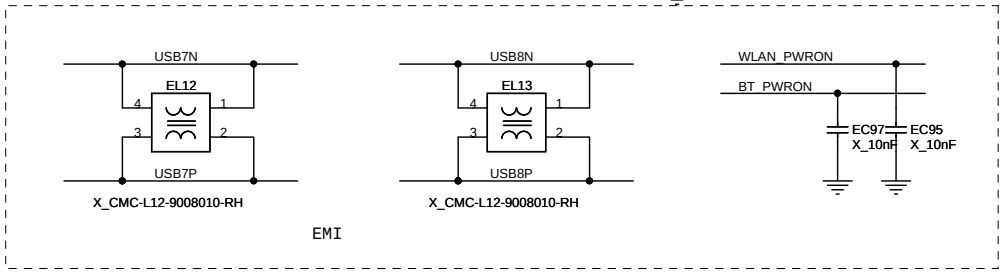
BLUETOOTH

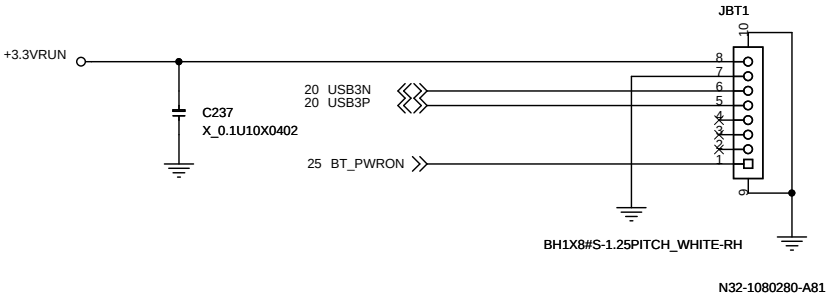
MS-3871





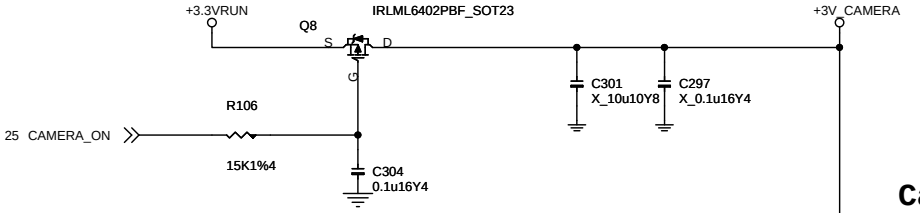
BLUETOOTH

MS-3801

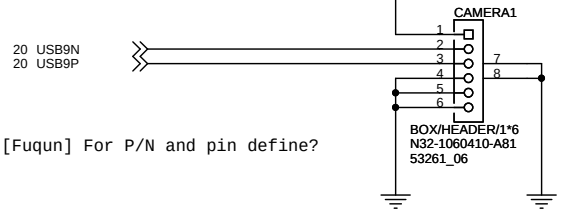


CAMERA

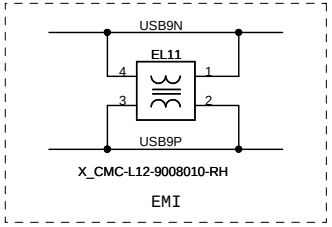
MAX: 130mA



Camera



[Fuqun] For P/N and pin define?



MICRO-STAR INT'L CO.,LTD		
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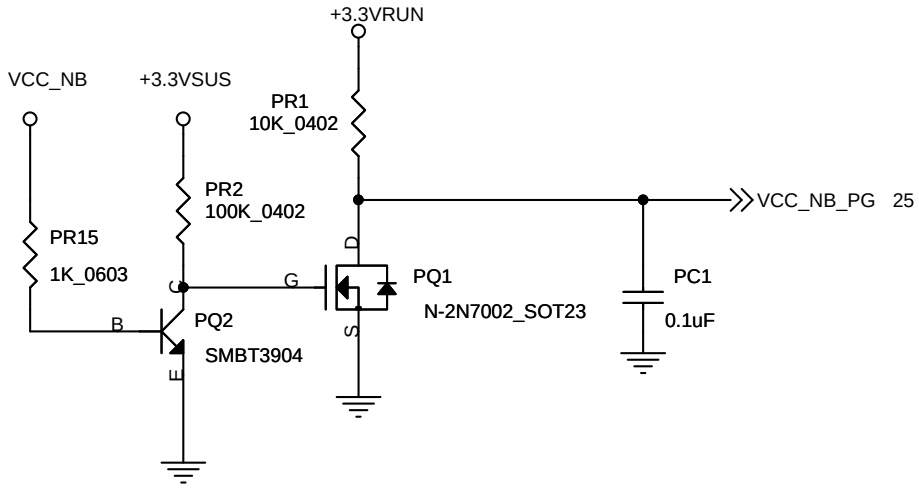

MICRO-STAR INT'L CO.,LTD		
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Size: A	Document Description: POWER LOGIC	Rev: 0A
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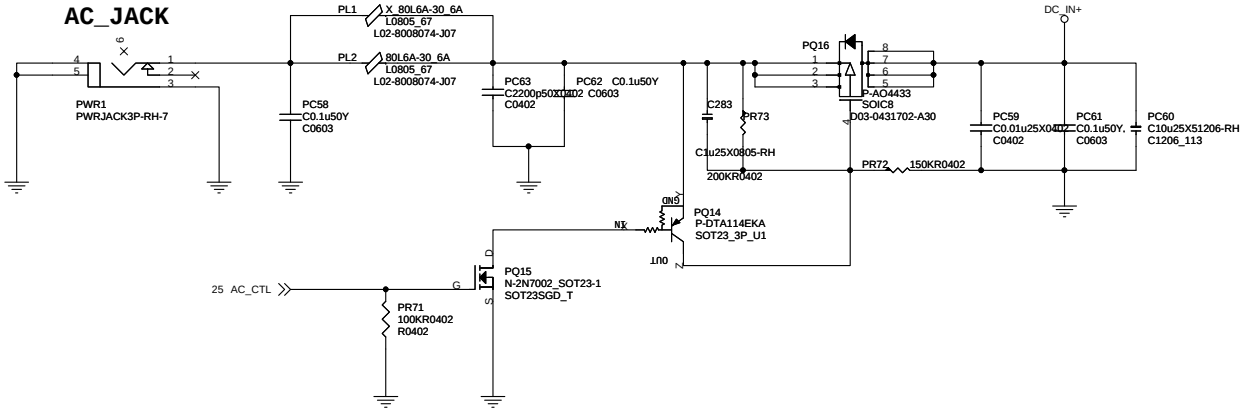

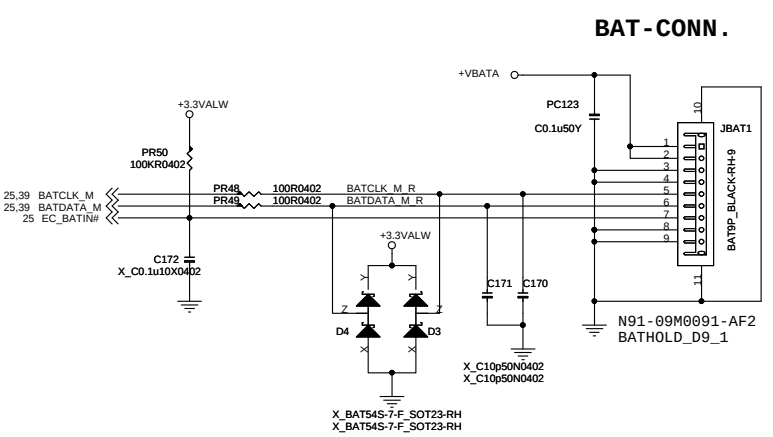

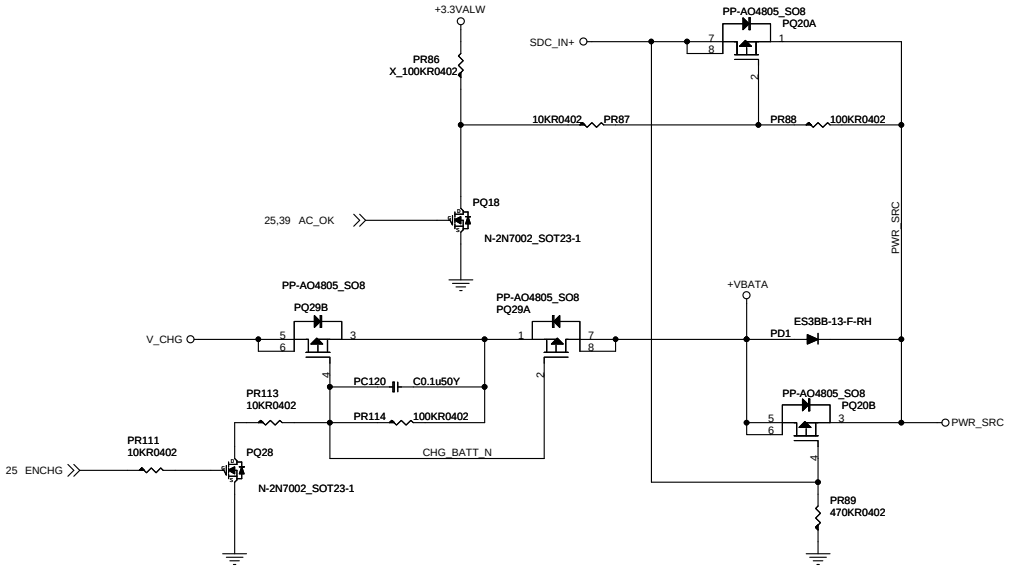

MICRO-STAR INT'L CO.,LTD		
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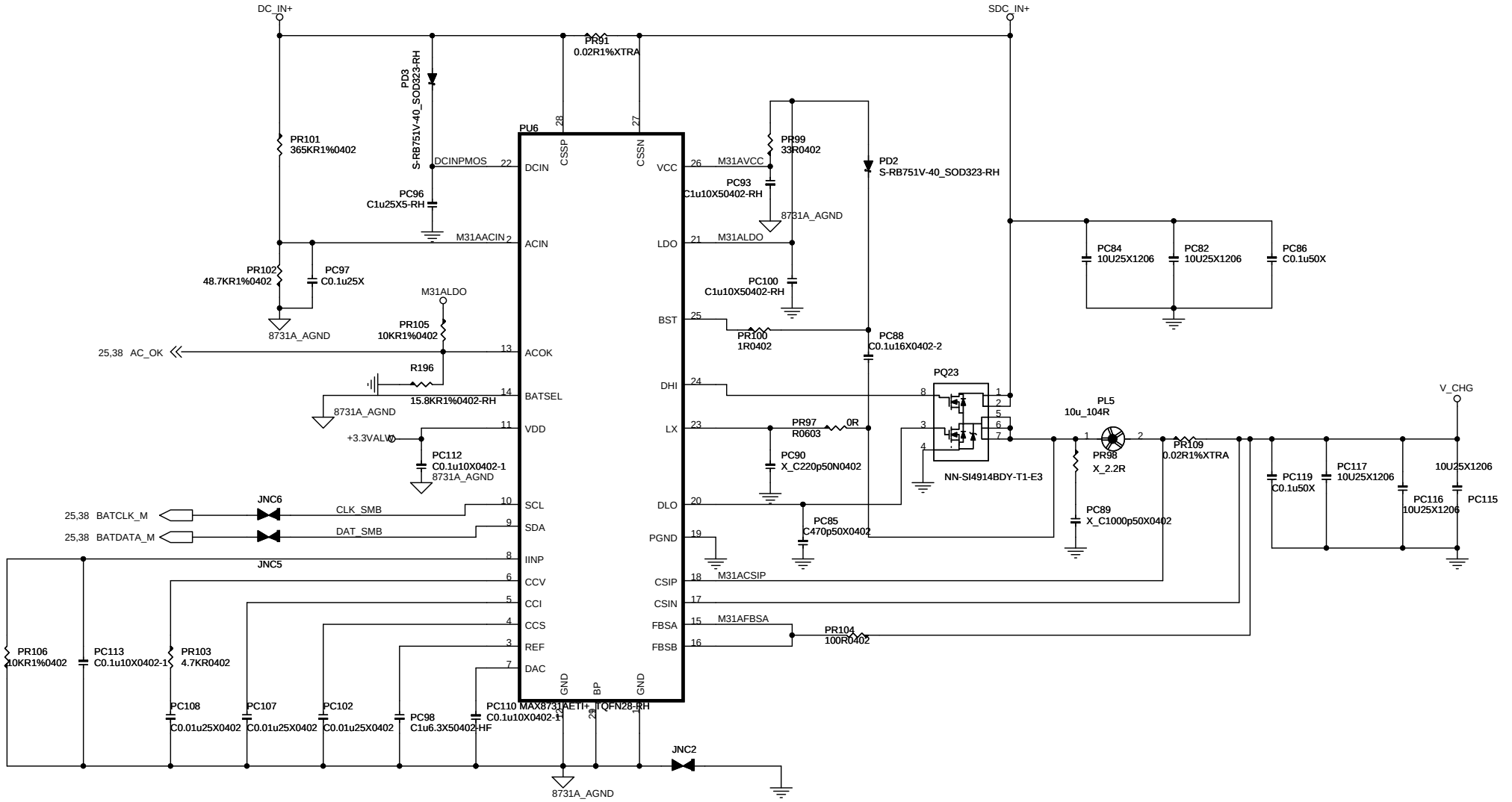
Adapter input voltage set 19 Voltage



IINP :

1. The transconductance from (CSSP - CSSN) to IINP is 3mA/V.

2. V_IINP = IINPUT x RS1 x 3mA/V x PR25

MSI	MICRO-STAR INT'L CO.,LTD		
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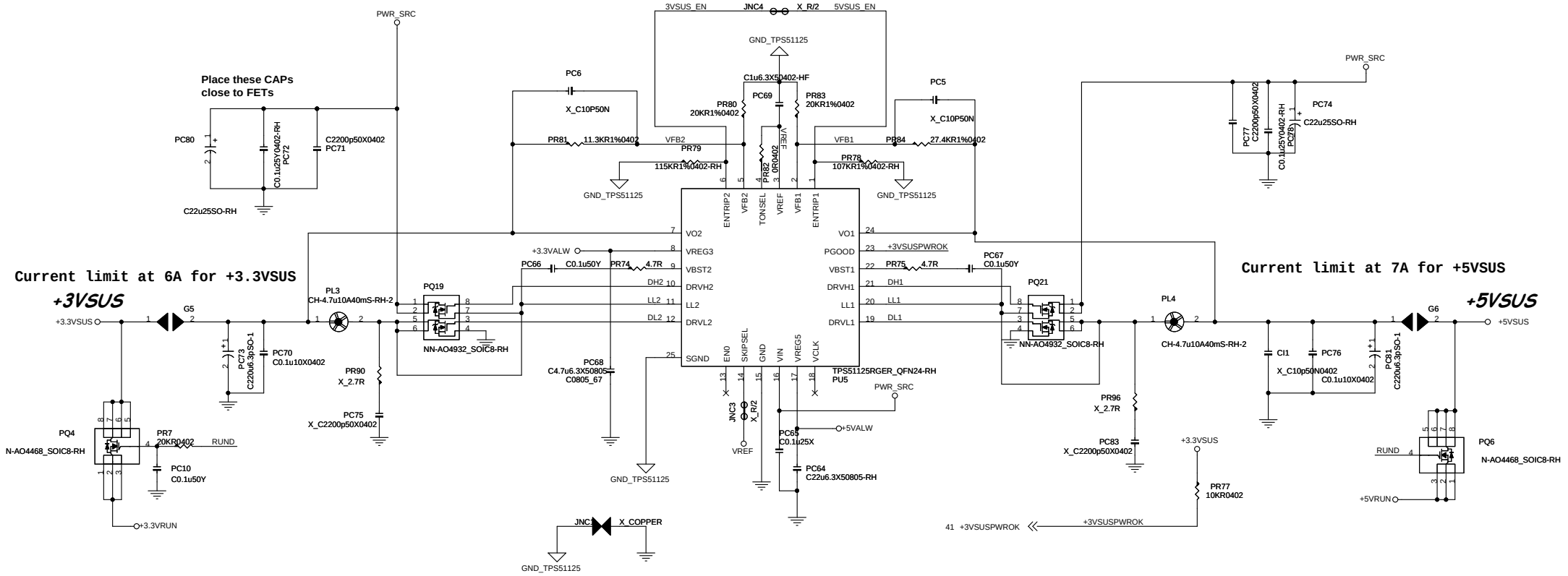
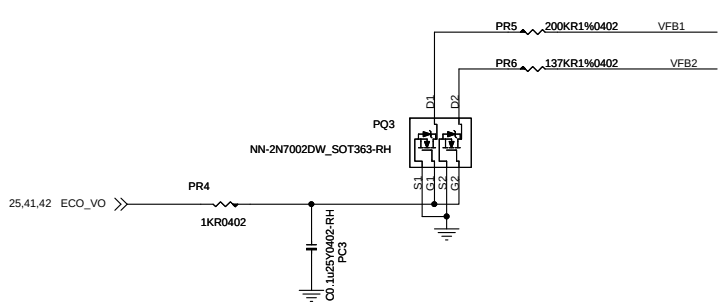


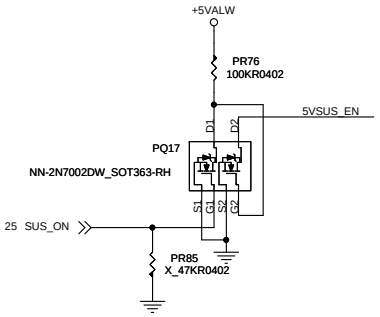


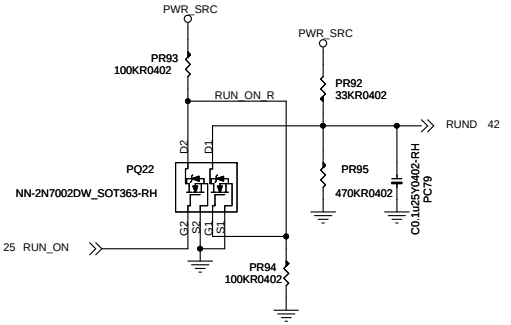
+3VSUS Voltage TABLE

ECO_VO	Voltage
HIGH	3.3V(default)
LOW	3.15V

+5VSUS Voltage TABLE

ECO_VO	Voltage
HIGH	5V(default)
LOW	4.8V





MICRO-STAR INT'L CO.,LTD		
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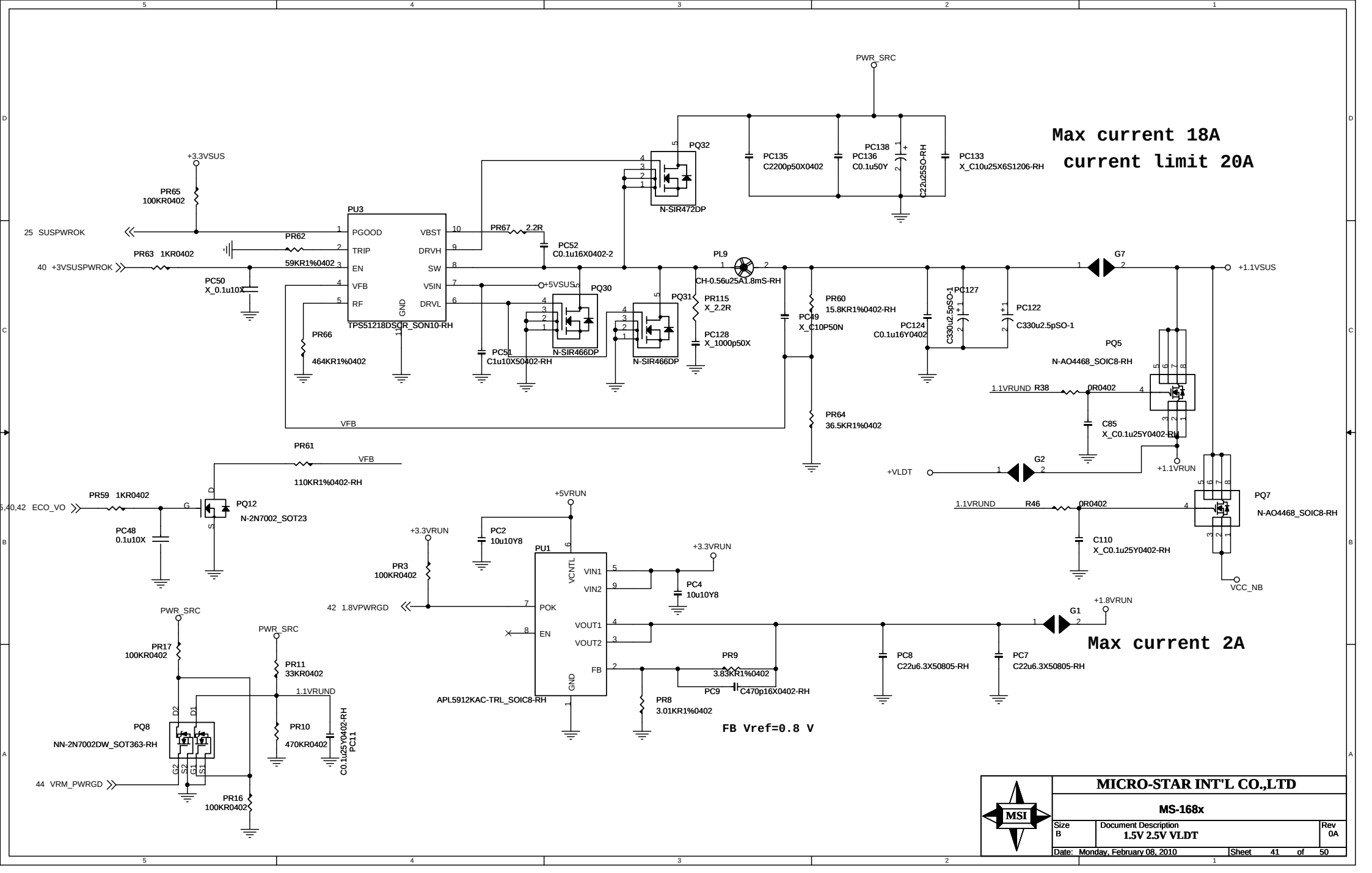

MSI	MICRO-STAR INT'L CO.,LTD	
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Size B	Document Description 1.5V 2.5V VLDT	Rev 0A
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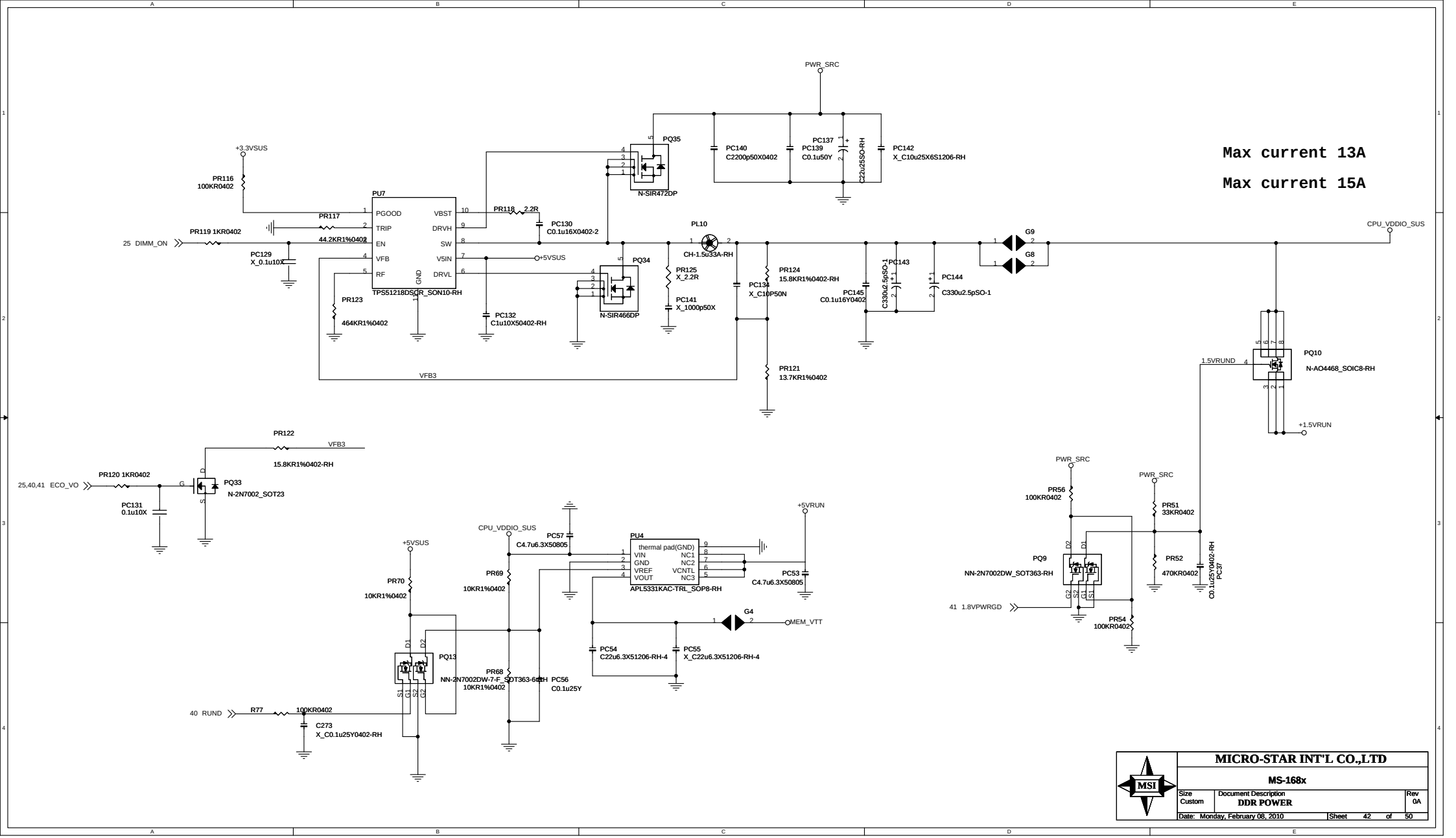

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Rev: 0A	
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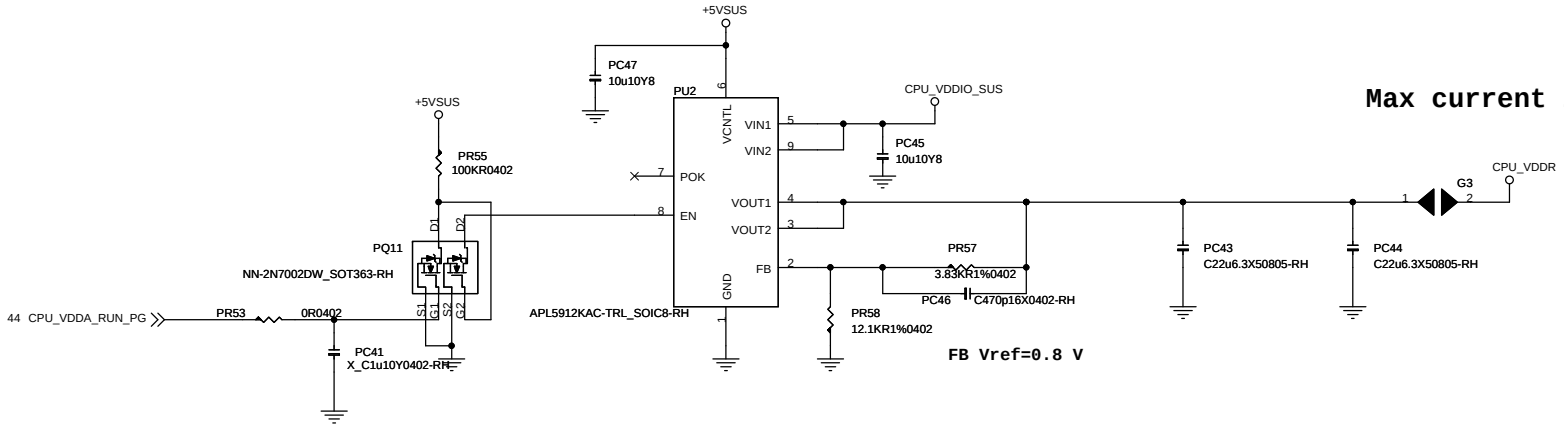

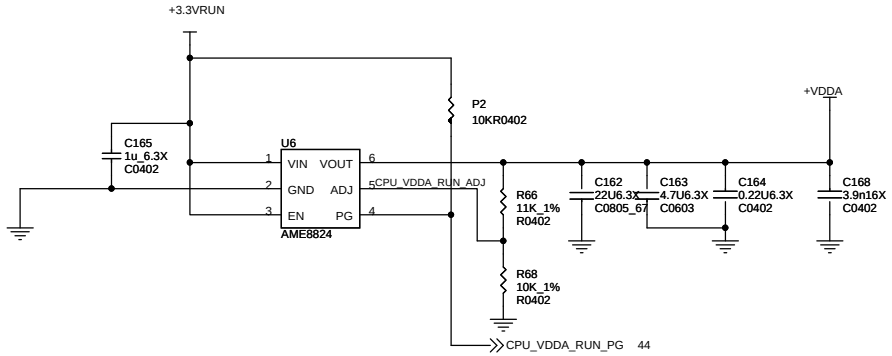

MICRO-STAR INT'L CO.,LTD		
MS-168x		
Size: Custom	Document Description: NB SB CORE PWR	Rev: 0A
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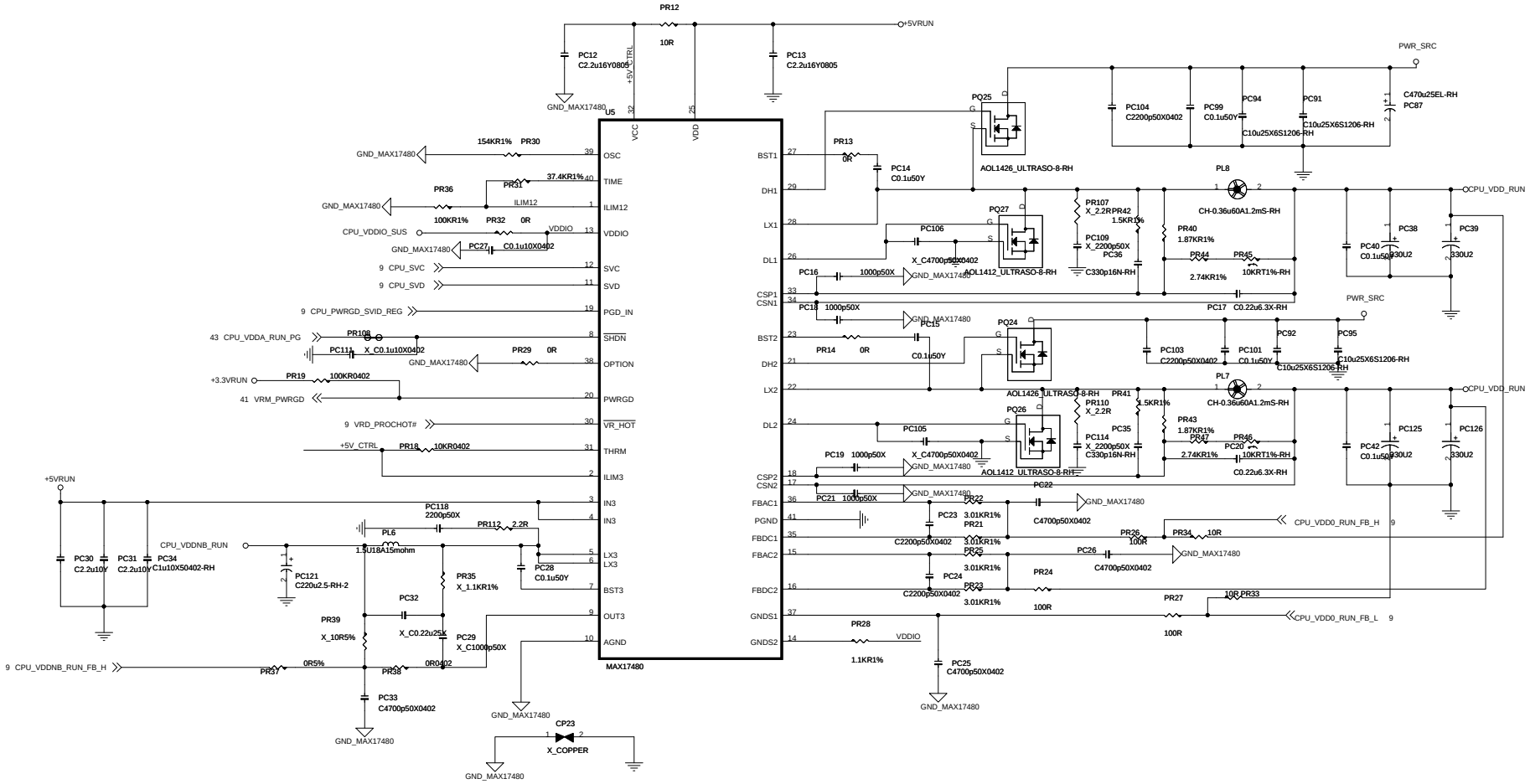

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Title	CPU CORE PWR	
Size: C	Document Number: MS-1684	Rev: 0A
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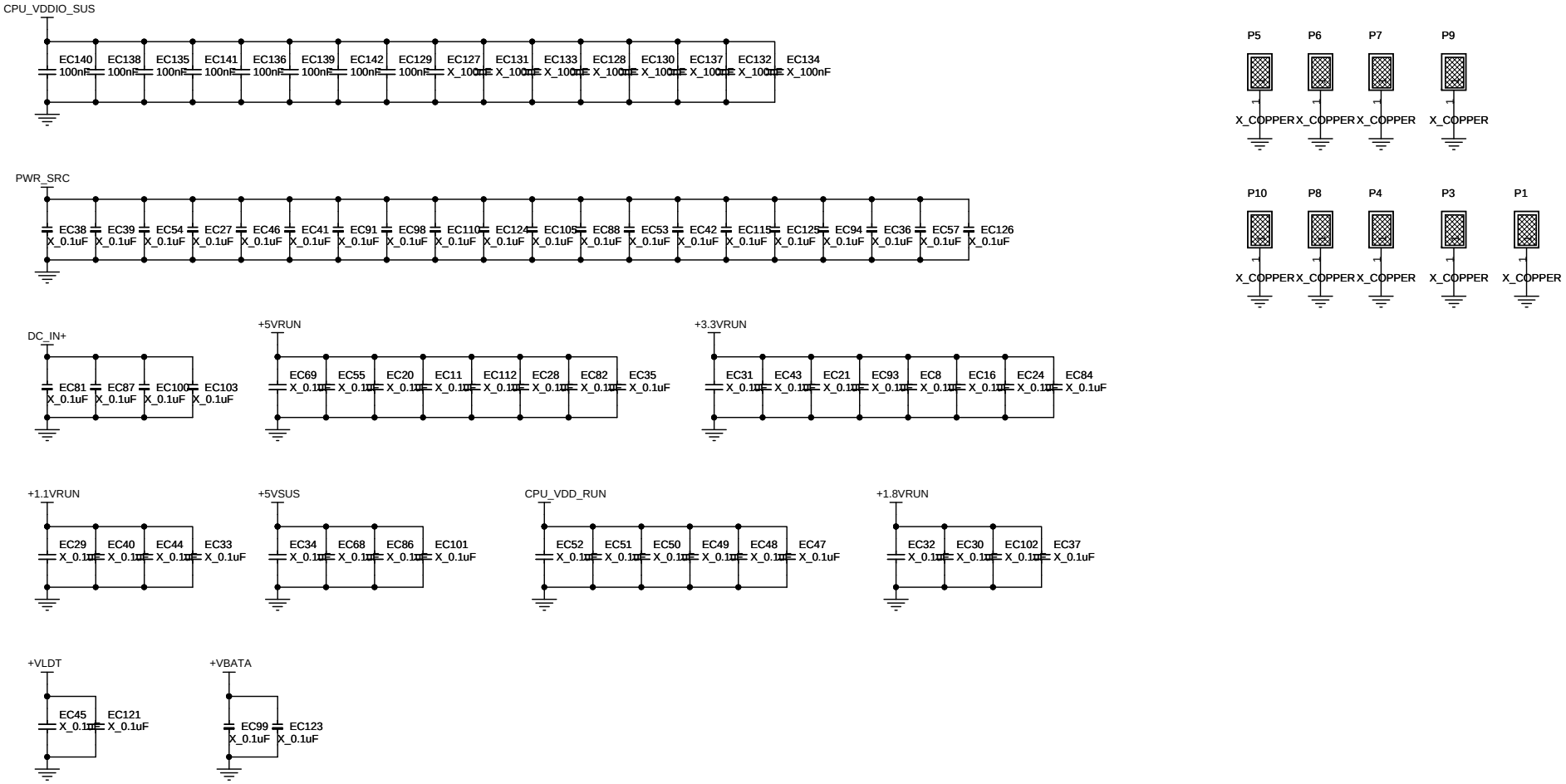

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-168x	
Size: B	Document Description: EMI	Rev: 0A
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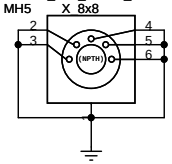
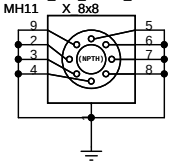
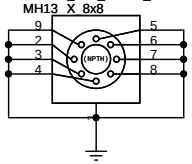
HOLES_8X8_D3MM_VIA5
MH5 X 8x8



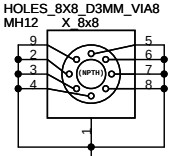
HOLES_8X8_D3MM_VIA8
MH11 X 8x8



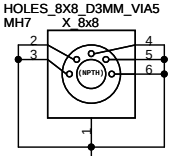
HOLES_8X8_D3MM_VIA8
MH13 X 8x8



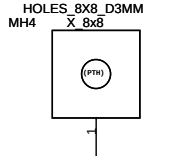
HOLES_8X8_D3MM_VIA8
MH12 X 8x8



HOLES_8X8_D3MM_VIA5
MH7 X 8x8



HOLES_8X8_D3MM
MH4 X 8x8



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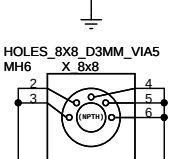
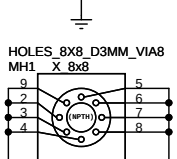
MH6 X 8x8



HOLES_8X8_D3MM_VIA8
MH1 X 8x8



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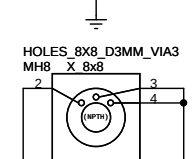
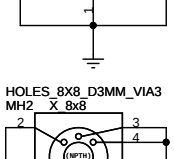
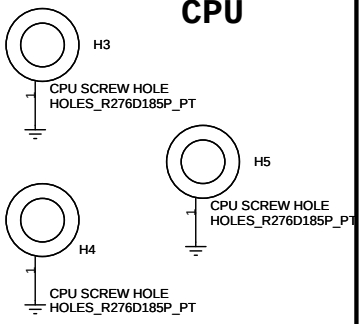
MH8 X 8x8

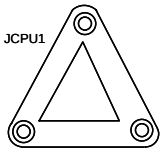


HOLES_8X8_D3MM_VIA3
MH2 X 8x8



CPU





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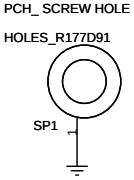
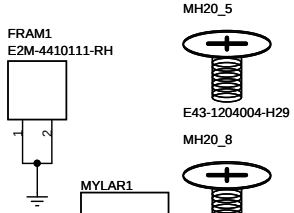
E2M-6710411-Y31

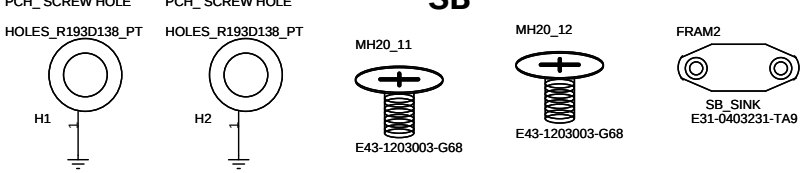
WLAN

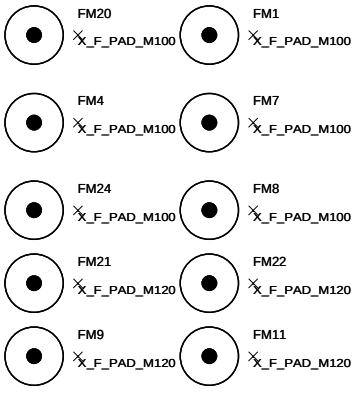


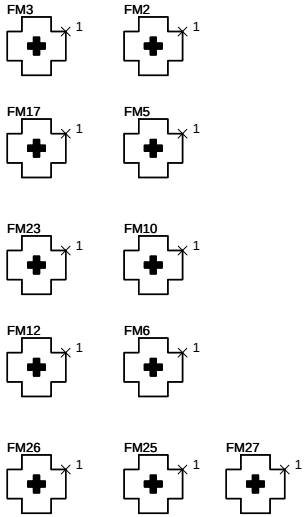
NEW CARD

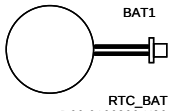


SB



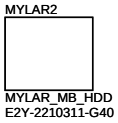




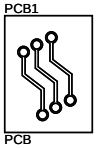


RTC_BAT
D06-0100300-K26

FOR HDD



MYLAR_MB_HDD
E2Y-2210311-G40



PCB

LABEL

LABEL

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Single ended

SIP25
L6_10mil_40ohm
X_PIN1*2

SIP23
L4_8.5mil_40ohm
X_PIN1*2

SIP11
L1_10mil_40ohm
X_PIN1*2

SIP16
L3_8.5mil_40ohm
X_PIN1*2

SIP28
L6_6.5mil_50ohm
X_PIN1*2

SIP21
L4_5.5mil_50ohm
X_PIN1*2

SIP9
L1_6.5mil_50ohm
X_PIN1*2

SIP1
L3_5.5mil_50ohm
X_PIN1*2

SIP27
L6_5mil_55ohm
X_PIN1*2

SIP20
L4_4.5mil_55ohm
X_PIN1*2

SIP12
L1_5mil_55ohm
X_PIN1*2

SIP13
L3_4.5mil_55ohm
X_PIN1*2

SIP26
L6_4mil_60ohm
X_PIN1*2

SIP22
L4_4mil_60ohm
X_PIN1*2

SIP14
L3_4mil_60ohm
X_PIN1*2

SIP8
L1_4mil_60ohm
X_PIN1*2

Differential signal

SIP15
L1_DIFF_5/4.5/5_85 Ohm-
L1_DIFF_5/4.5/5_85 Ohm+
X_H1X4_black-RH

SIP10
L3_DIFF_4.5/5.5/4.5_85 Ohm-
L3_DIFF_4.5/5.5/4.5_85 Ohm+
X_H1X4_black-RH

SIP32
L6_DIFF_5/4.5/5_85 Ohm-
L6_DIFF_5/4.5/5_85 Ohm+
X_H1X4_black-RH

SIP19
L4_DIFF_4.5/5.5/4.5_85 Ohm-
L4_DIFF_4.5/5.5/4.5_85 Ohm+
X_H1X4_black-RH

SIP6
L1_DIFF_5/5/5_90 Ohm-
L1_DIFF_5/5/5_90 Ohm+
X_H1X4_black-RH

SIP7
L3_DIFF_5/6/5_90 Ohm-
L3_DIFF_5/6/5_90 Ohm+
X_H1X4_black-RH

SIP29
L6_DIFF_5/5/5_90 Ohm-
L6_DIFF_5/5/5_90 Ohm+
X_H1X4_black-RH

SIP18
L4_DIFF_5/6/5_90 Ohm-
L4_DIFF_5/6/5_90 Ohm+
X_H1X4_black-RH

SIP2
L1_DIFF_4.5/5/4.5_93 Ohm-
L1_DIFF_4.5/5/4.5_93 Ohm+
X_H1X4_black-RH

SIP3
L3_DIFF_4.5/7/4.5_93 Ohm-
L3_DIFF_4.5/7/4.5_93 Ohm+
X_H1X4_black-RH

SIP31
L6_DIFF_4.5/5/4.5_93 Ohm-
L6_DIFF_4.5/5/4.5_93 Ohm+
X_H1X4_black-RH

SIP24
L4_DIFF_4.5/7/4.5_93 Ohm-
L4_DIFF_4.5/7/4.5_93 Ohm+
X_H1X4_black-RH

SIP4
L1_DIFF_4/7/4_100 Ohm-
L1_DIFF_4/7/4_100 Ohm+
X_H1X4_black-RH

SIP5
L3_DIFF_4/8/4_100 Ohm-
L3_DIFF_4/8/4_100 Ohm+
X_H1X4_black-RH

SIP30
L6_DIFF_4/7/4_100 Ohm-
L6_DIFF_4/7/4_100 Ohm+
X_H1X4_black-RH

SIP17
L4_DIFF_4/8/4_100 Ohm-
L4_DIFF_4/8/4_100 Ohm+
X_H1X4_black-RH

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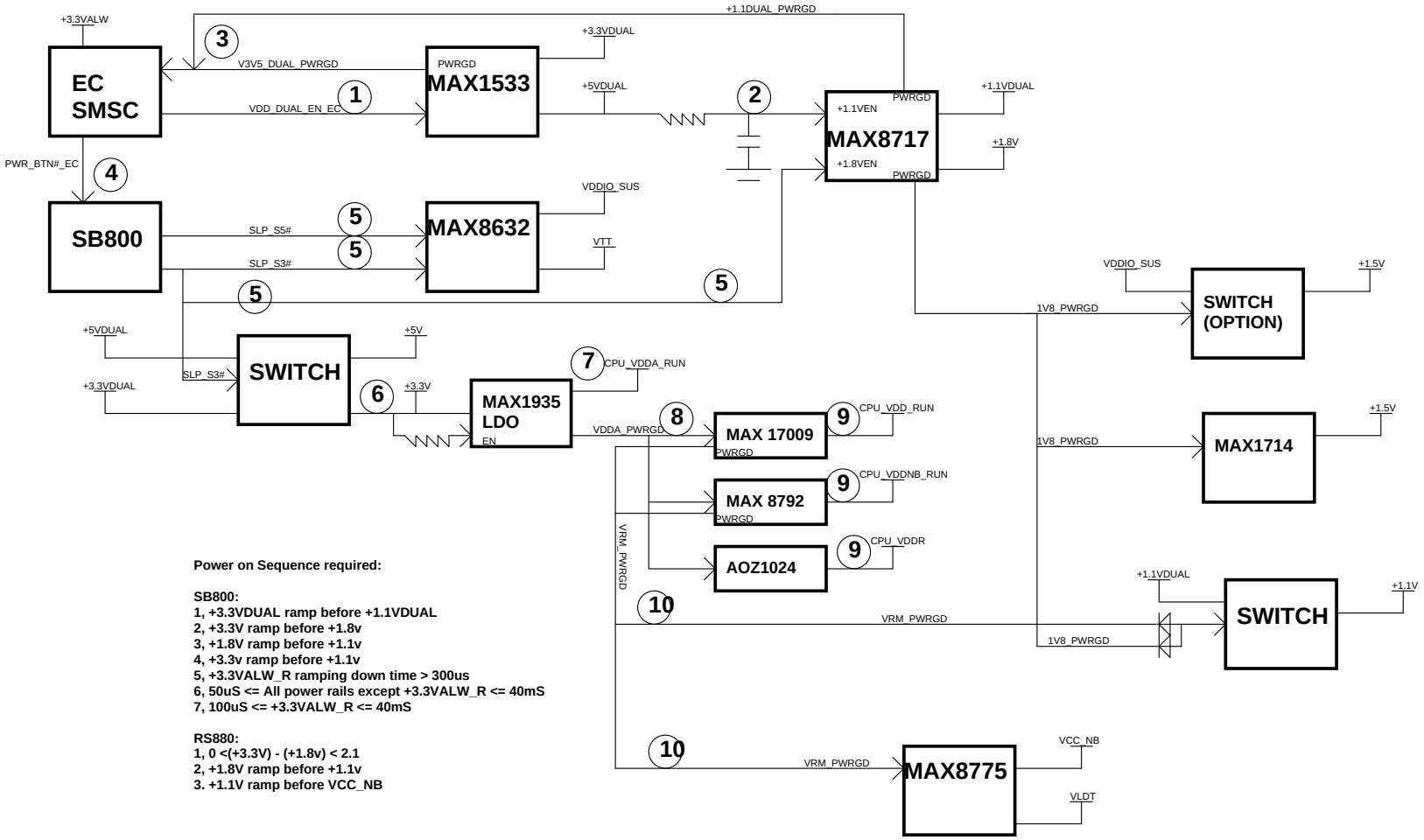

Power on Sequence required:

SB800:
1, +3.3VDUAL ramp before +1.1VDUAL
2, +3.3V ramp before +1.8v
3, +1.8V ramp before +1.1v
4, +3.3v ramp before +1.1v
5, +3.3VALW_R ramping down time > 300us
6, 50uS <= All power rails except +3.3VALW_R <= 40mS
7, 100uS <= +3.3VALW_R <= 40mS

RS880:
1, 0 <(+3.3V) - (+1.8v) < 2.1
2, +1.8V ramp before +1.1v
3. +1.1V ramp before VCC_NB

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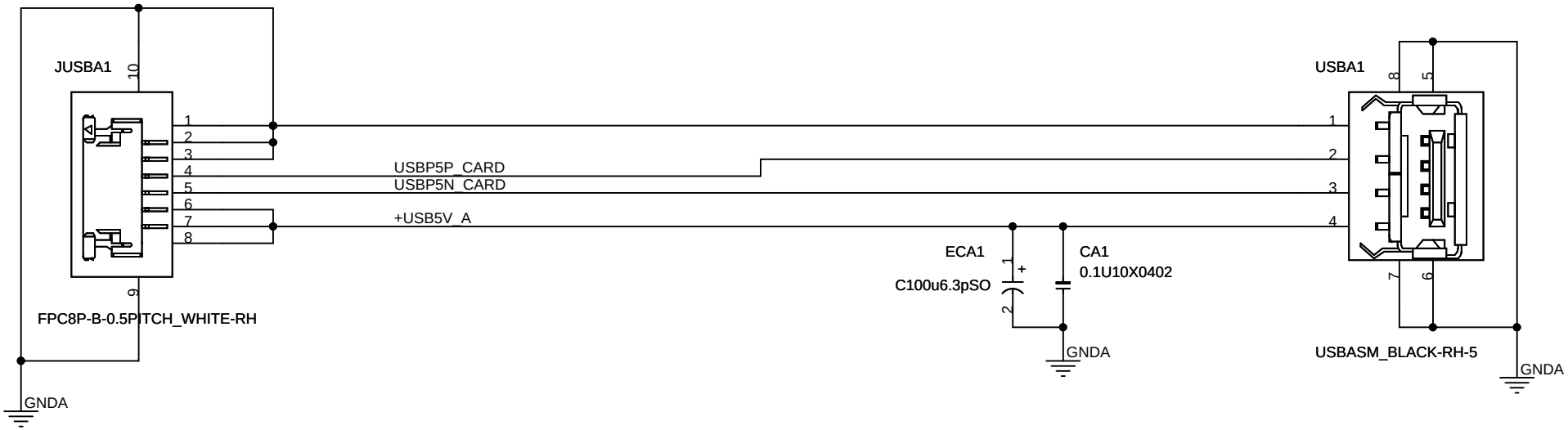

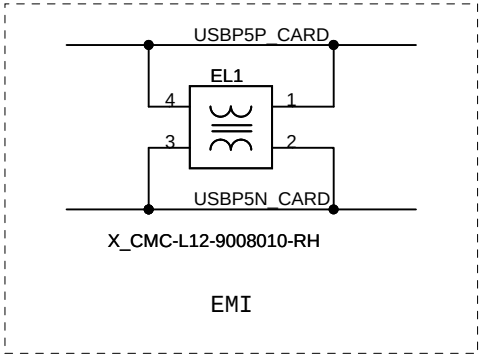

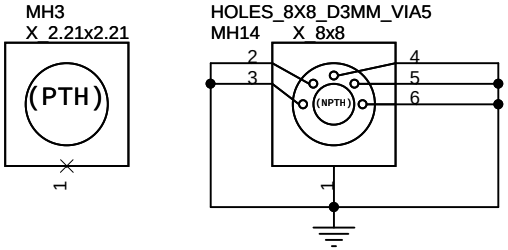

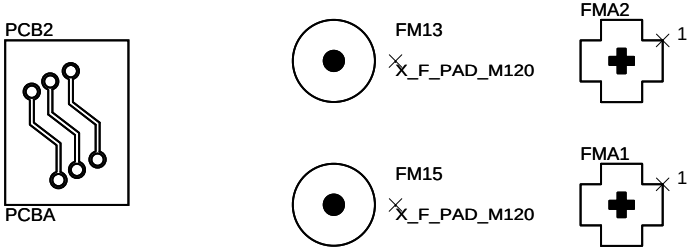

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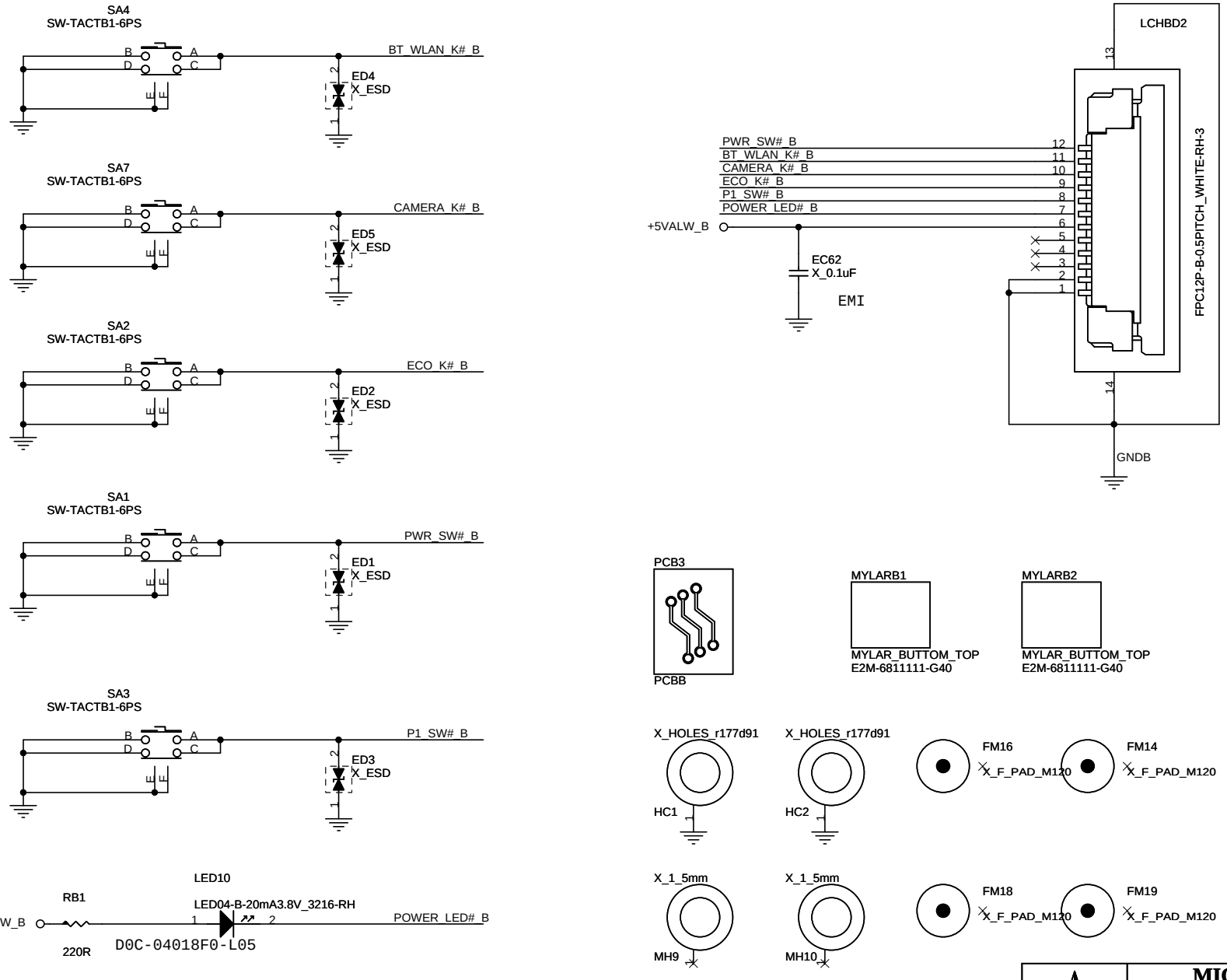
[Fuqun] Connector ORCad lib not same with MS-1688



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