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Intel mPGA478B CPU - Power	4
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MS-7024

**IBM
Wellfleet**

Version 130

Intel (R) Springdale (GMCH) + ICH5 Chipset
Intel Northwood & Prescott mPGA478B Processor

CPU:

Intel Northwood/Prescott - 3.0G & Above

System Chipset:

**Intel Springdale - GMCH (North Bridge)
Intel ICH5 (South Bridge)**

On Board Chipset:

**BIOS -- FWH EEPROM
AC'97 Codec -- AD1981B
LPC Super I/O -- LPC47M233
LAN -- I82562EZ(10/100) / I82541EI(Giga)
CLOCK -- Cypress CY28405**

Main Memory:

DDR * 2 (Max 2GB)

PCI Slots:

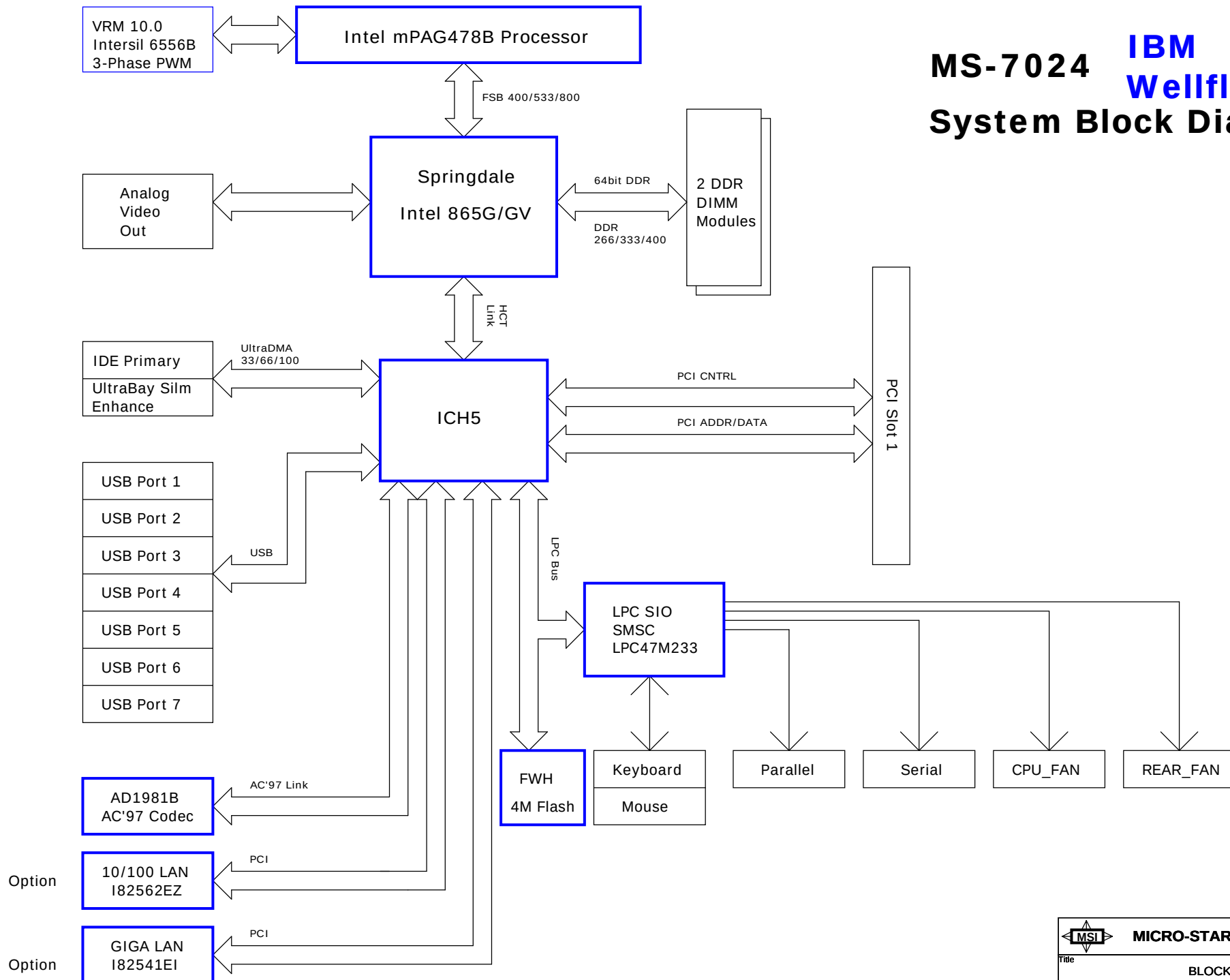
PCI2.3 SLOT * 1

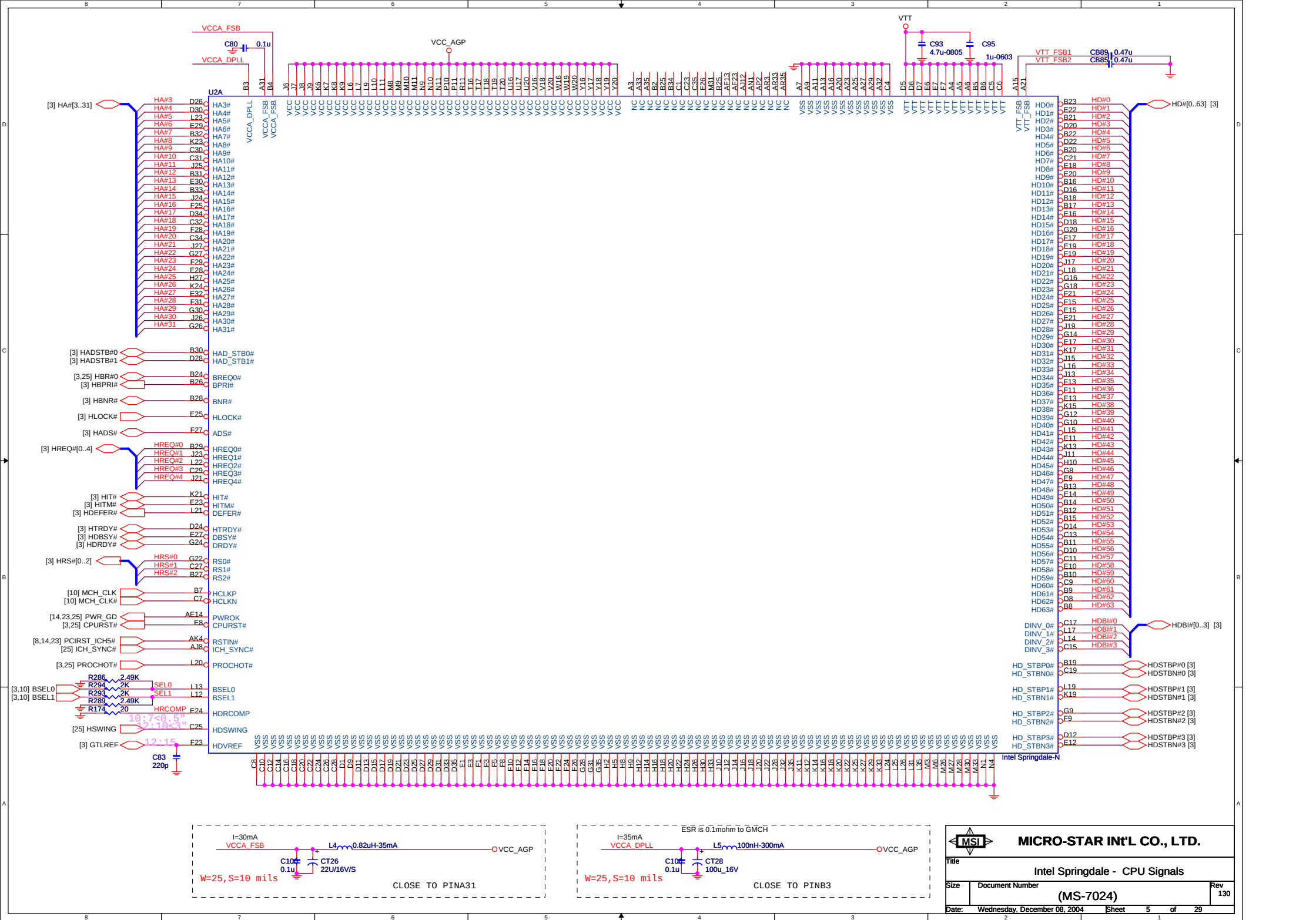
Intersil PWM:

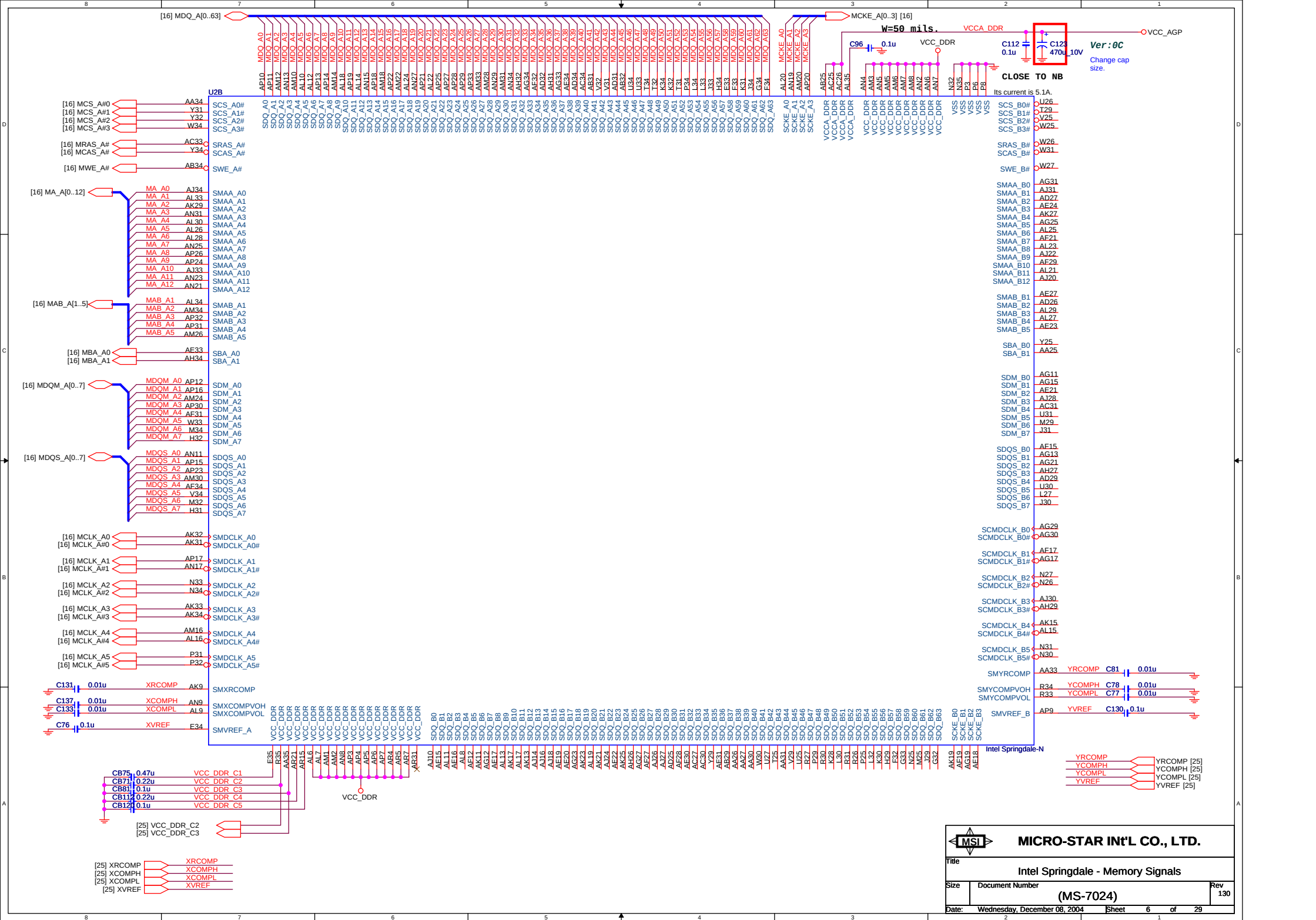
**Controller: HIP6556B (HIP6565)
Driver: HIP6602B *1 / HIP6601B * 1**

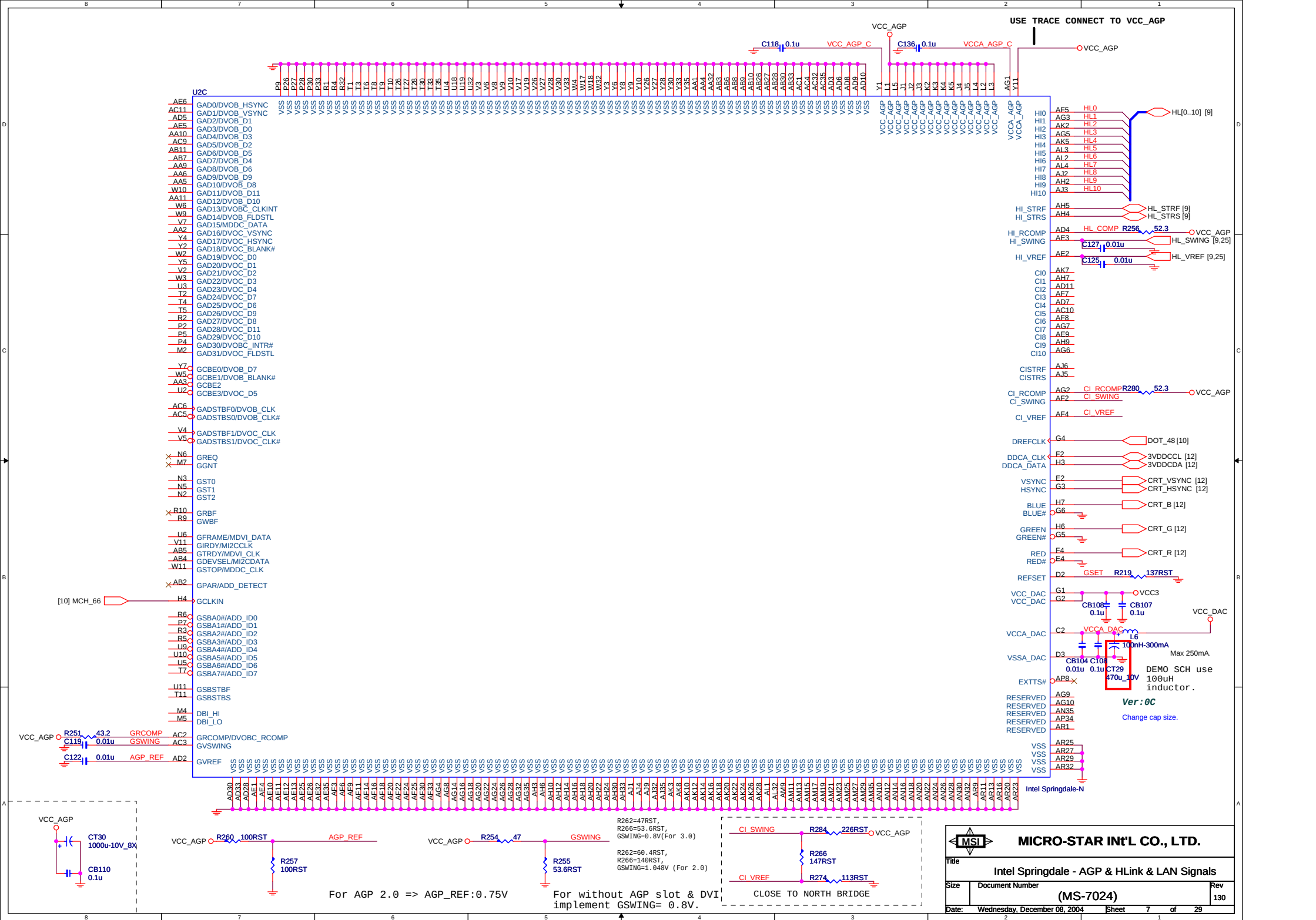
		MICRO-STAR INT'L CO., LTD.	
Title COVER SHEET			
Size	Document Number (MS-7024)		Rev 130
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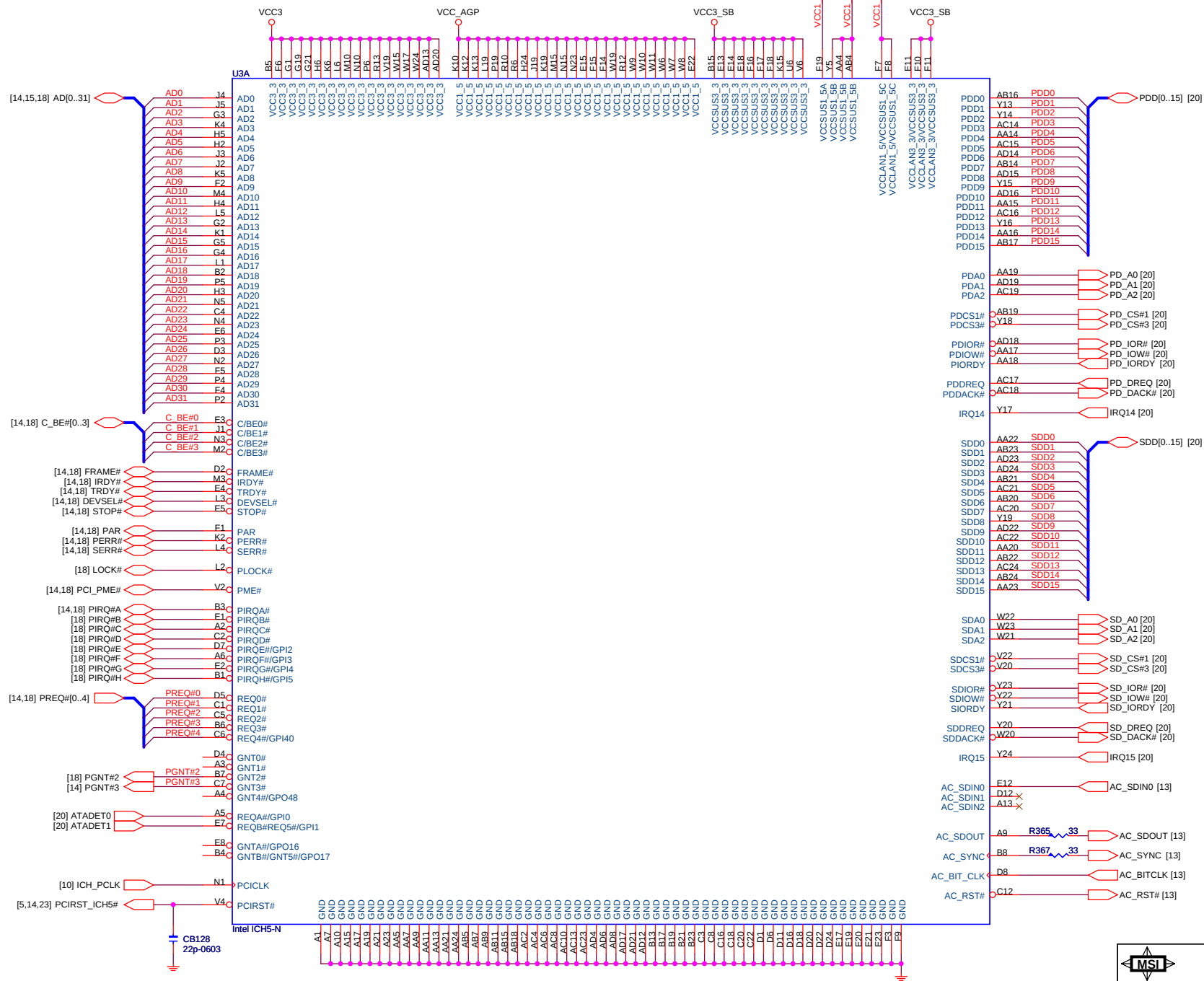
MS-7024 **IBM Wellfleet** System Block Diagram





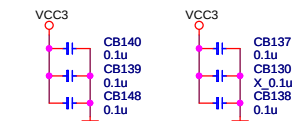




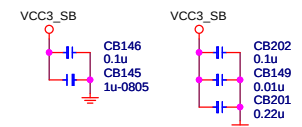


ICH5 Decoupling Capacitors

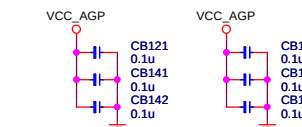
All caps be placed less than 100mils.



Close A1,A7,H1,P1,AD12 and AD21 of ICH5.



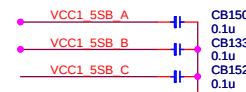
0.1uF close A15,A23, and V1 of ICH5.
Another close A17,A19 and A21 of ICH5.

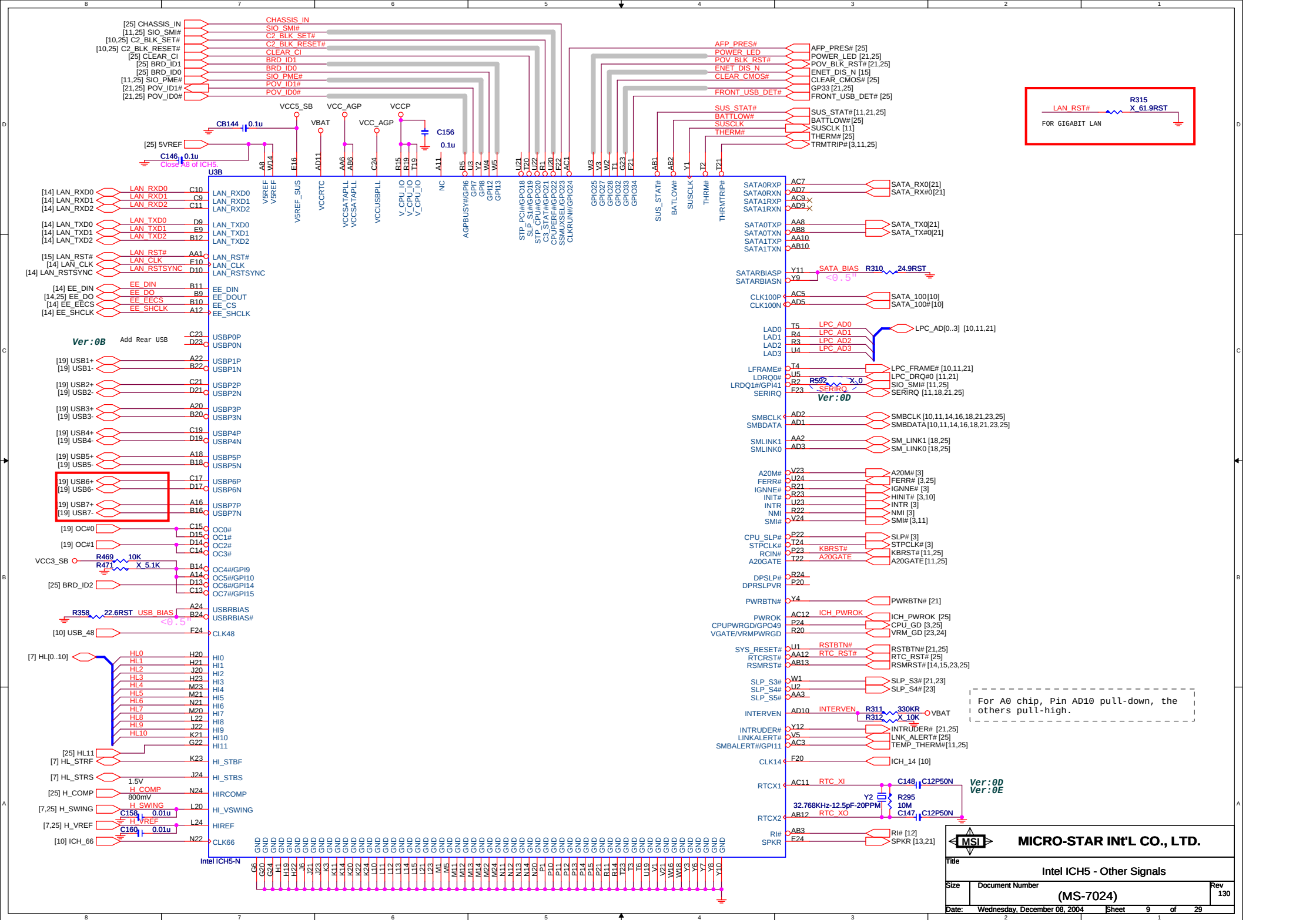


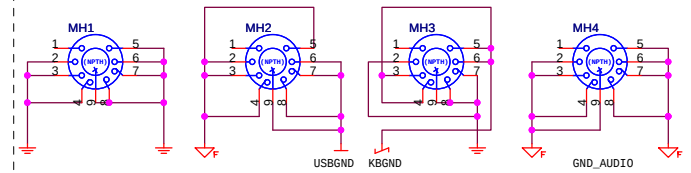
Close L24,C24,D8,G24,M24 and AD18 of ICH5.



Close AD18 of ICH5.







Ver:0C

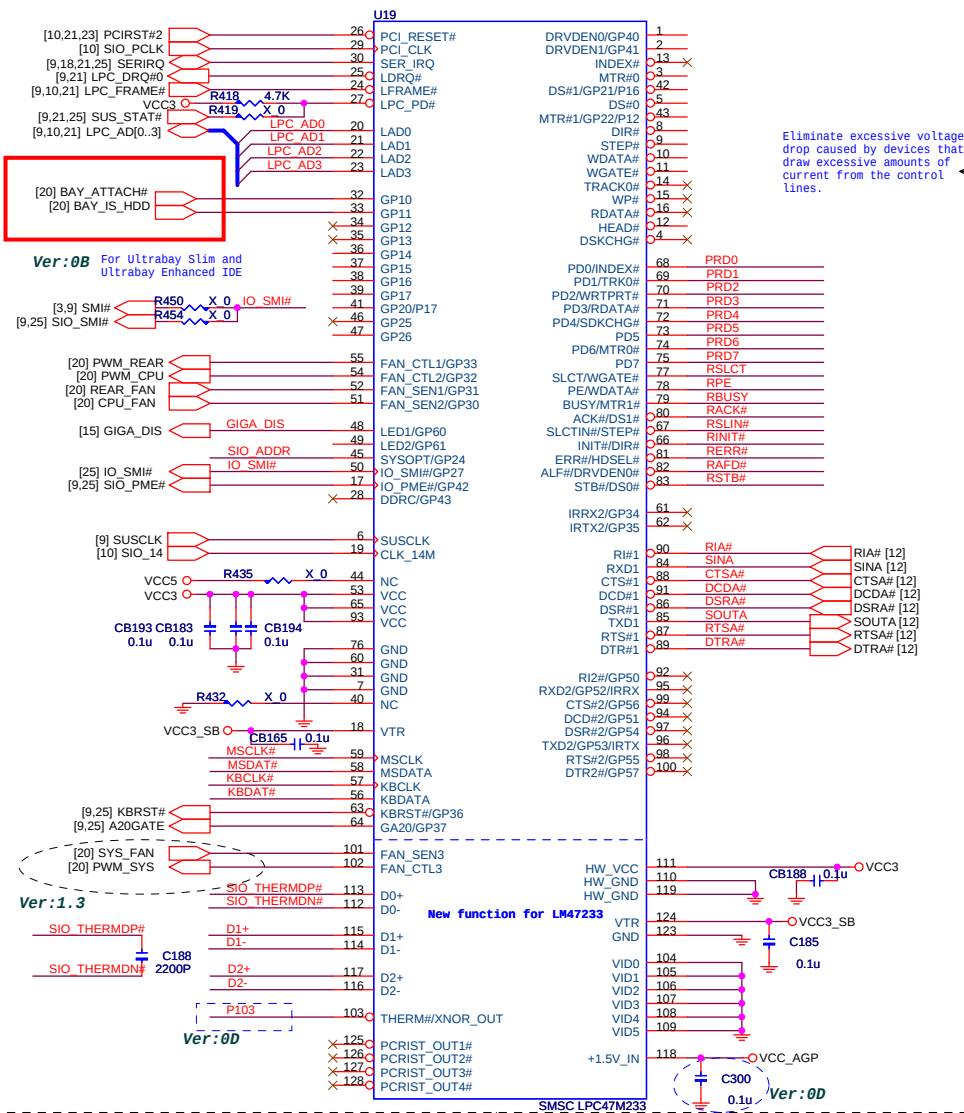
The schematic shows two input signals, [9,25] C2_BLK_RESET# and [9,25] C2_BLK_SET#, connected to a circuit. The RESET signal passes through a resistor R416 (10K) before reaching the gate of MOSFET Q51 (2N7002S). The SET signal also passes through a resistor R416 (10K) before reaching the gate of MOSFET Q52 (2N7002S). Both MOSFETs have their sources grounded and their drains connected to a common output node labeled FWH WP#. A label R1 is also present near the top right of the circuit.

10/100 ETHERNET
R386 1K
R385 X 1K
GIG ENET N VCC3
10/100 ETHERNET:H
GIGABIT ETHERNET: L

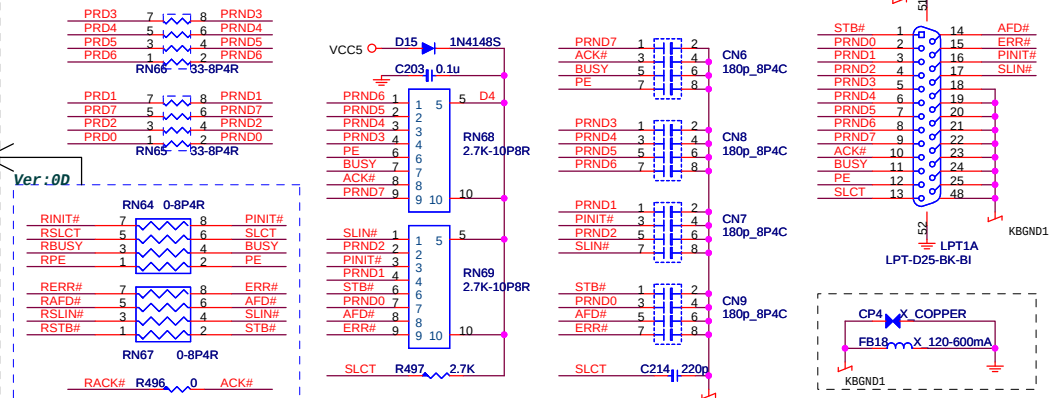
Ver:1.3 Change - the PCB Revision ID from 0000b to 0001b by pulling REV0 up (R414) instead of down (R413).

		MICRO-STAR INT'L CO., LTD.	
Title CY28405 & FWH			
Size	Document Number	(MS-7024)	Rev 130
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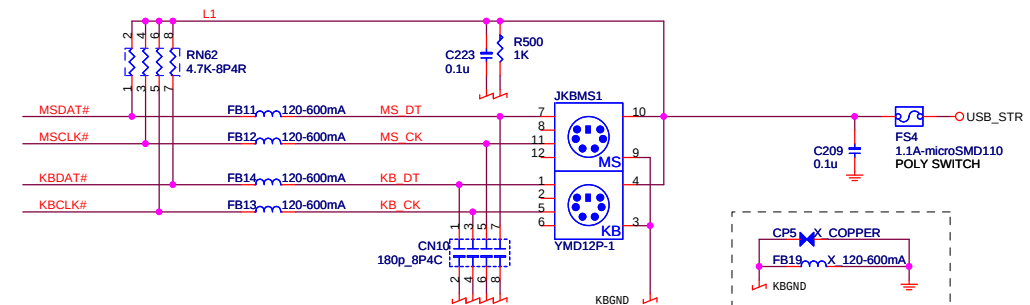
LPC SUPER I/O LPC47M233



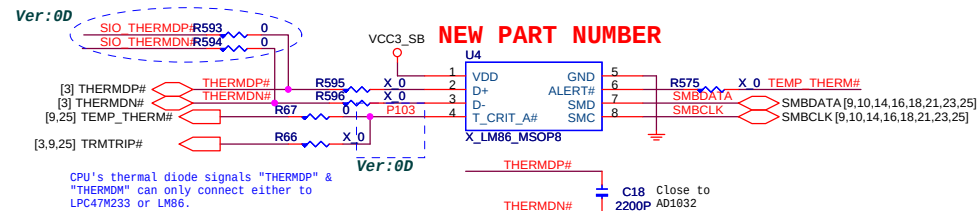
PARALLAL PORT



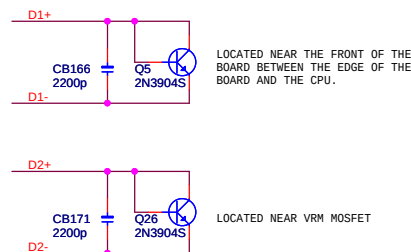
PS2 KEYBOARD & MOUSE CONNECTOR



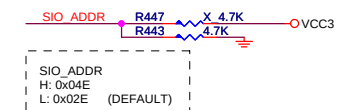
ADI 1032 TEMPERATURE SENSOR



REMOTE TEMPERATURE SENSOR



STRAPPING RESISTOR



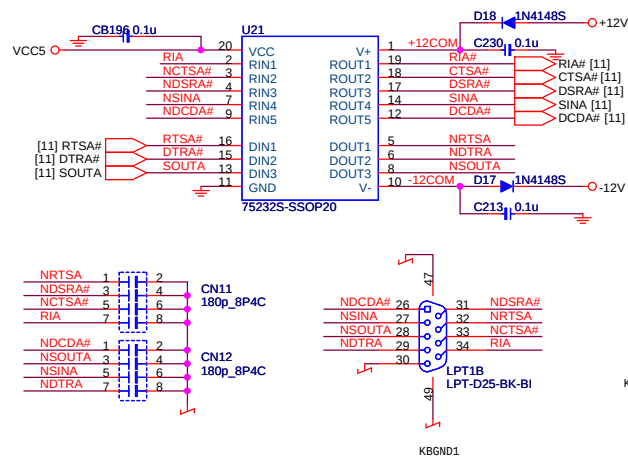
MICRO-STAR INT'L CO., LTD.

Title	LPC SUPER I/O & CONNECTORS
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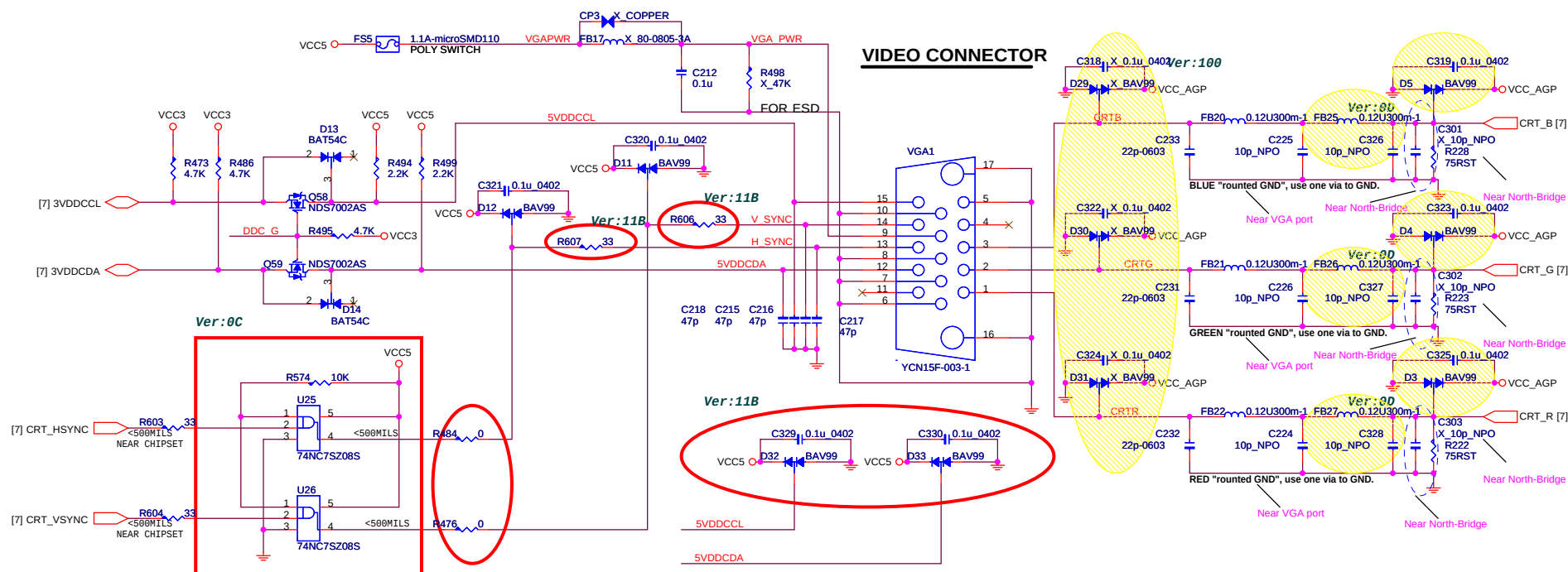
Size	Document Number
	(MS-7024)

Date: Wednesday, December 08, 2004 Sheet 11 of 29

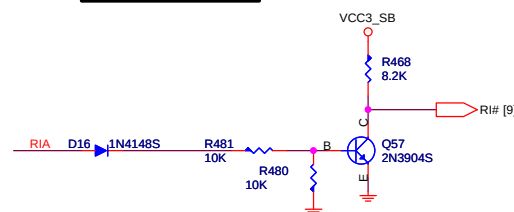
SERIAL PORT 1



VIDEO CONNECTOR



Wake On Ring



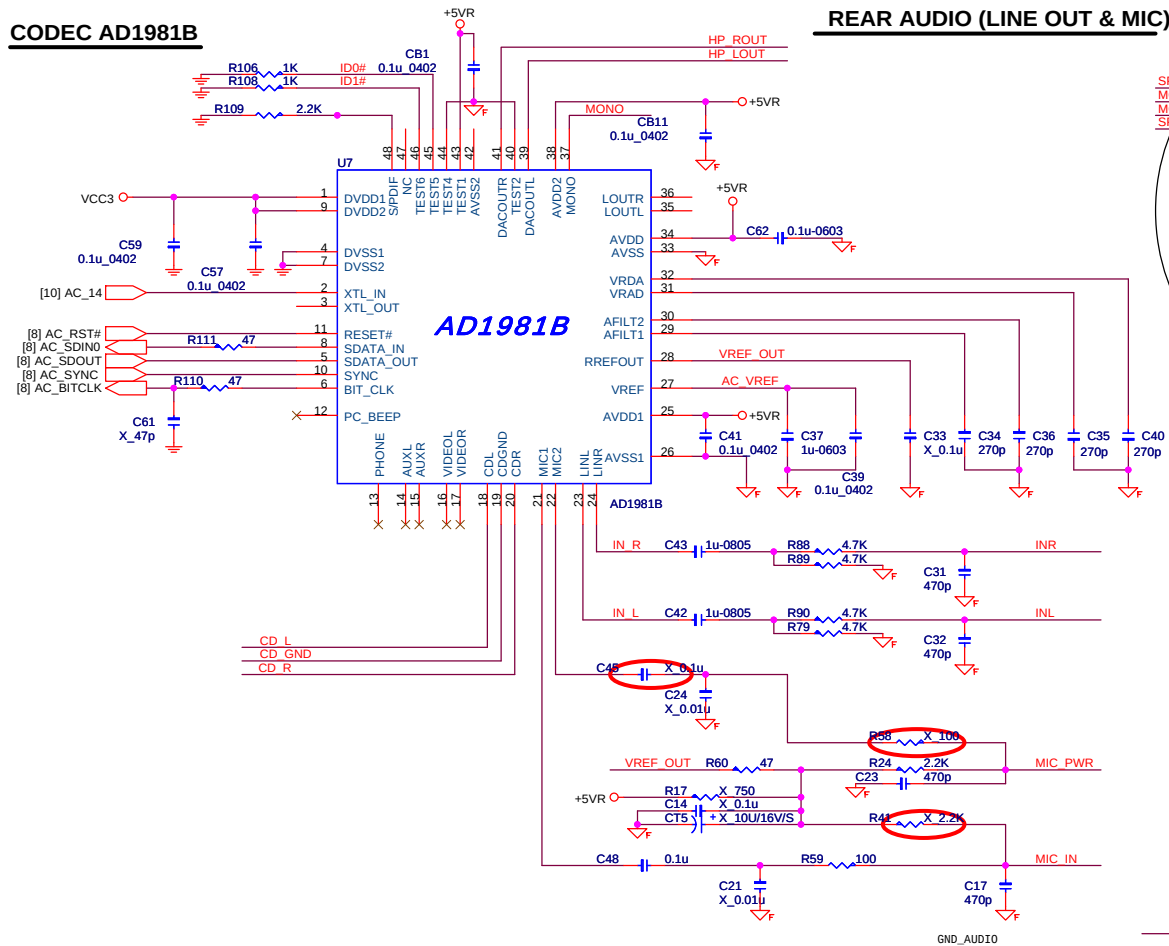
MICRO-STAR INT'L CO., LTD.

Title	COM PORT & VGA CONNECTORS
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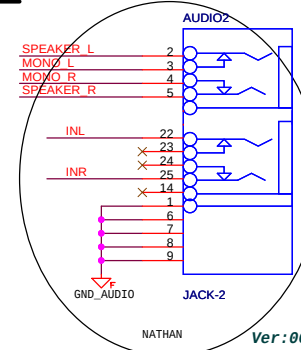
Size	Document Number	Rev
	(MS-7024)	130

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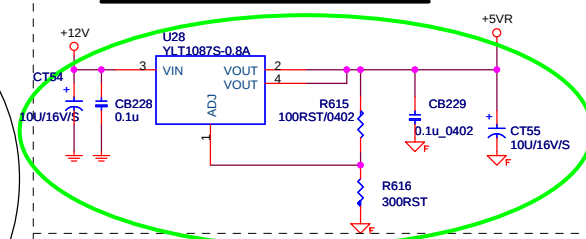
CODEC AD1981B



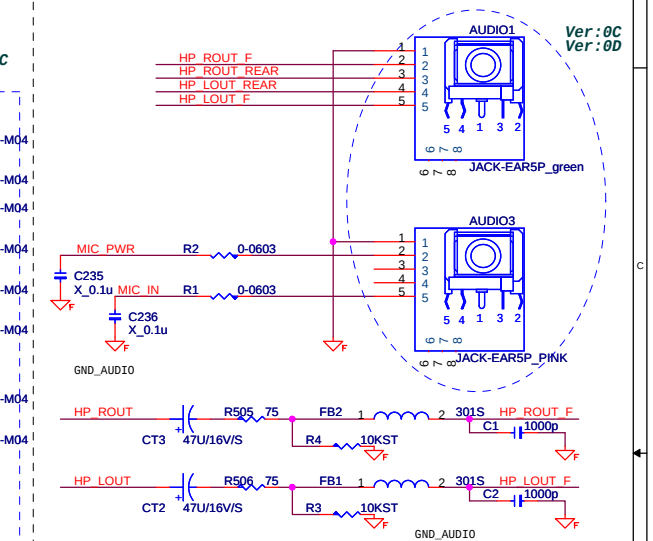
REAR AUDIO (LINE OUT & MIC)



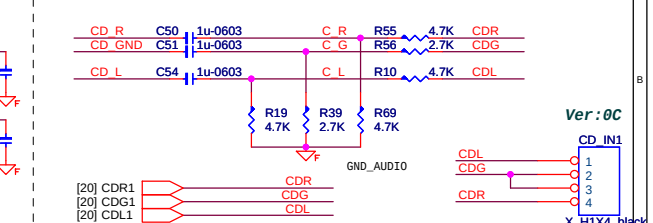
AUDIO CODE REGULATORS



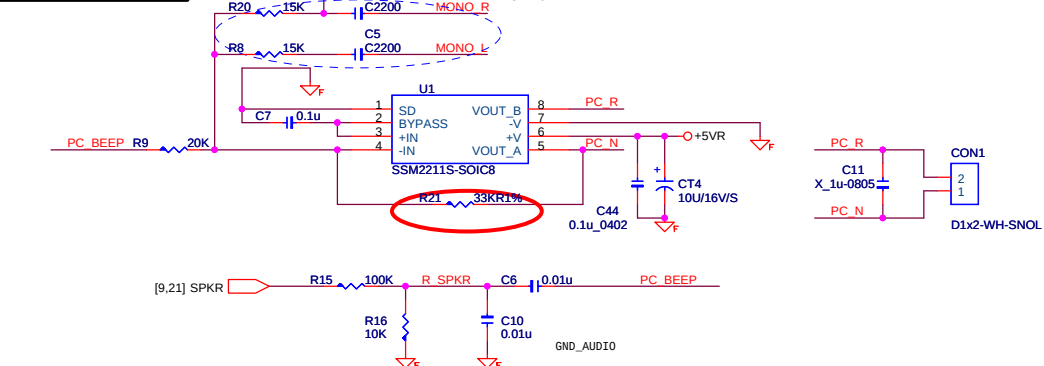
FRONT AUDIO CONNECTOR (LINE OUT & MIC)



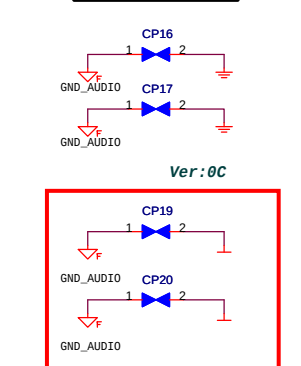
CD IN



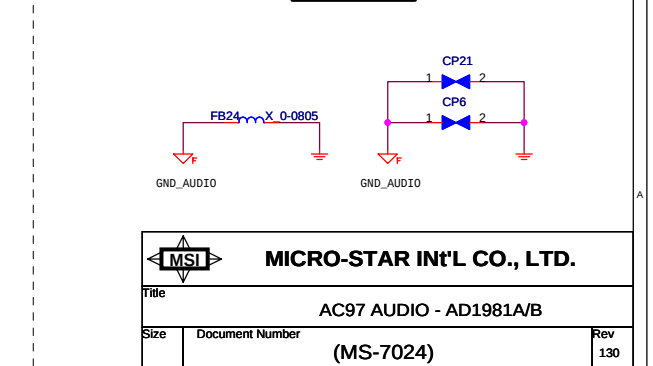
Internal Speaker



EMI COPPER



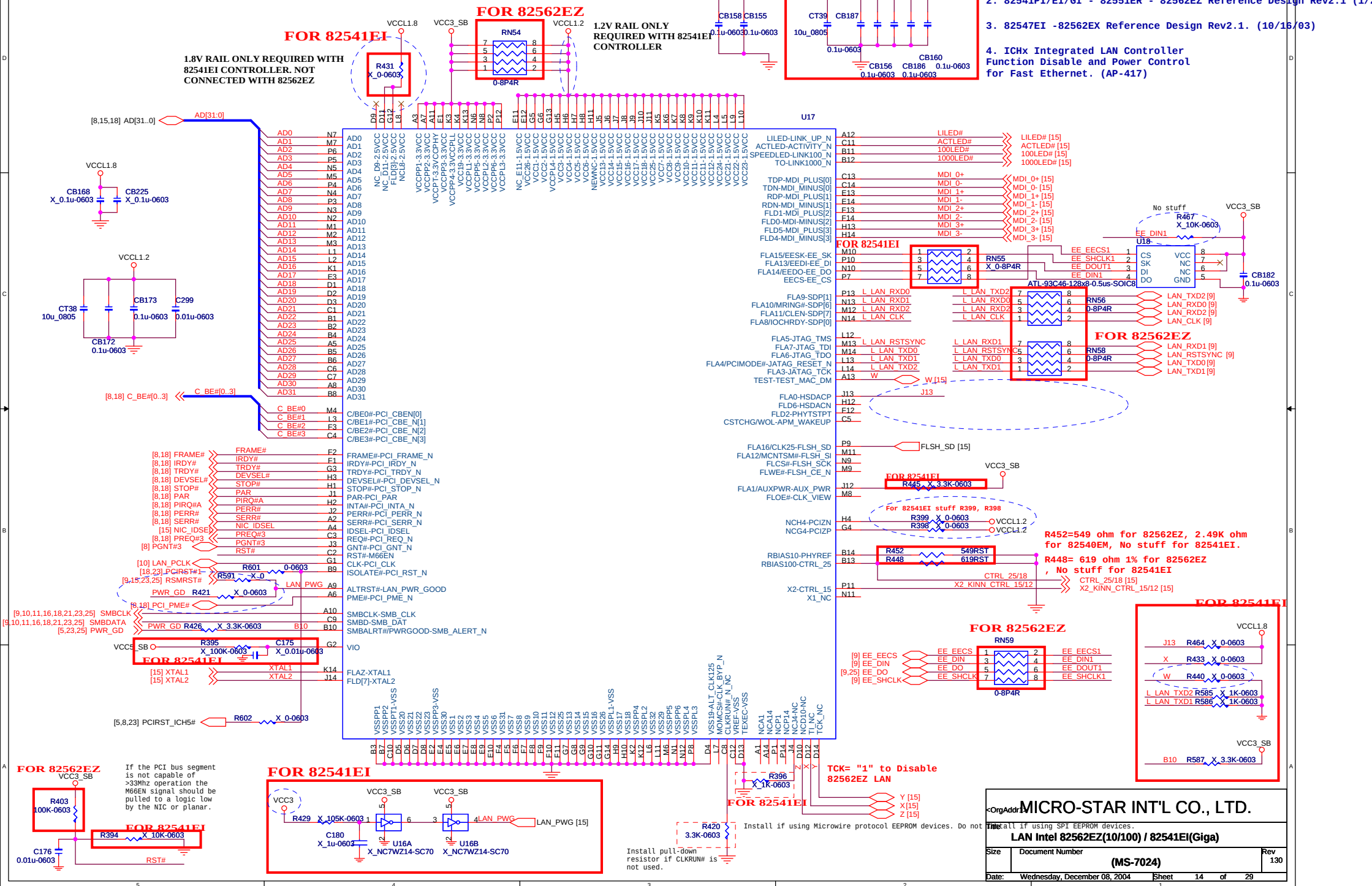
COPPER



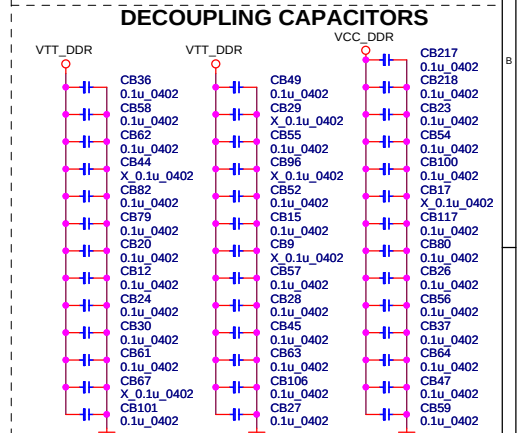
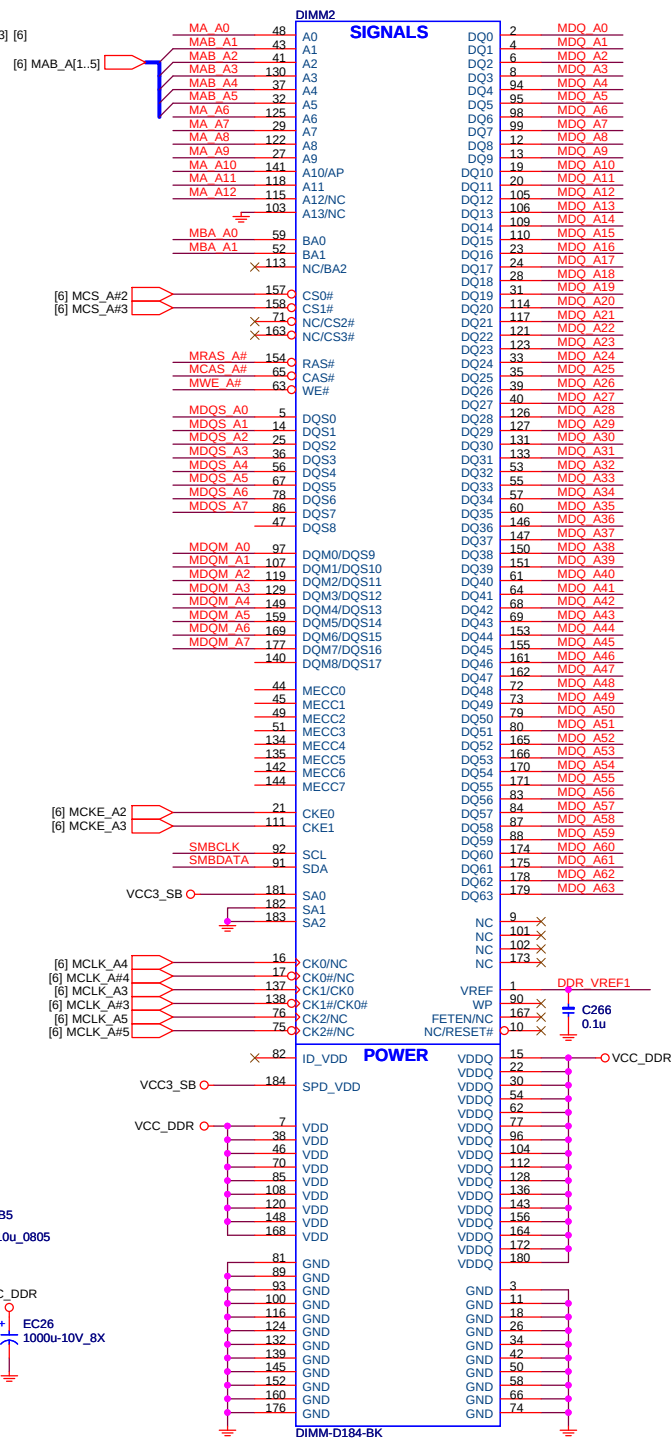
MICRO-STAR INT'L CO., LTD.			
Title			
AC97 AUDIO - AD1981A/B			
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B06-562EZ05-I06
Controller, LAN, INTEL/Kinnereth-R, BGA-196pin, 10/100 MBPS Ethernet Controller

B06-8254115-I06
CHIP, LAN, INTEL/82541EI, BGA-196, 1.2V/1.8V/3.3V, 10/100/1000 MBPS Gigabit Ethernet Controller



DDR Terminational Resisitors



Place these decoupling capacitors close to VTT_DDR termination resistors. One decoupling capacitor for each R-pack.



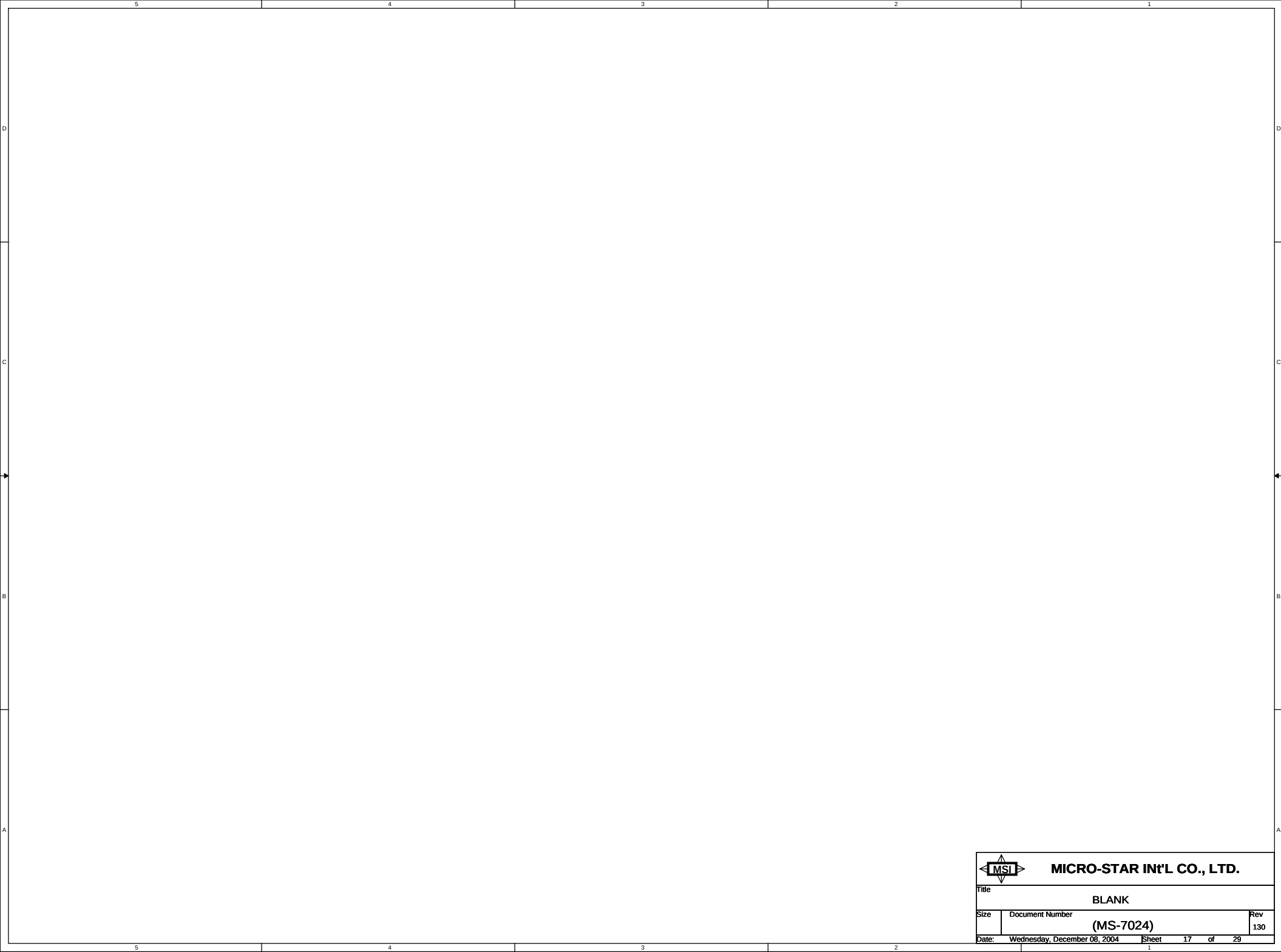
MICRO-STAR INT'L CO., LTD.

Title	DDR DIMM 1.2
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Size	Document Number	Rev
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	(MS-7024)	130
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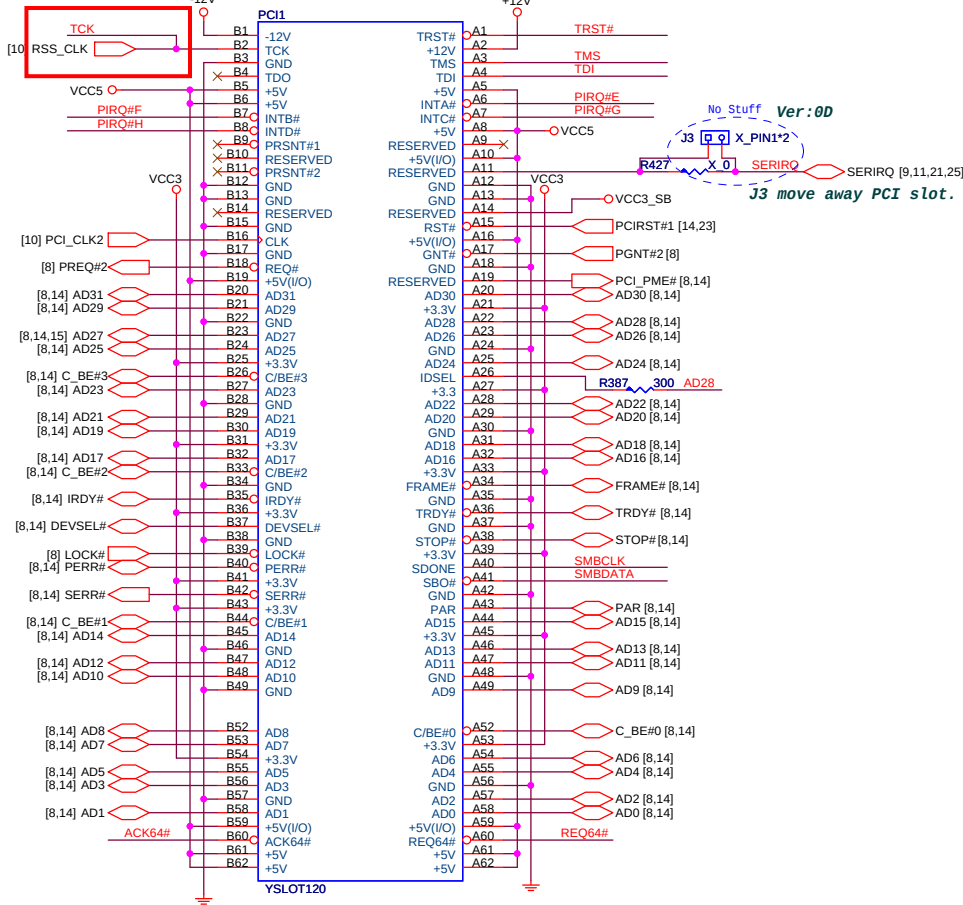
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		MICRO-STAR INT'L CO., LTD.	
Title			
BLANK			
Size	Document Number		Rev
	(MS-7024)		130
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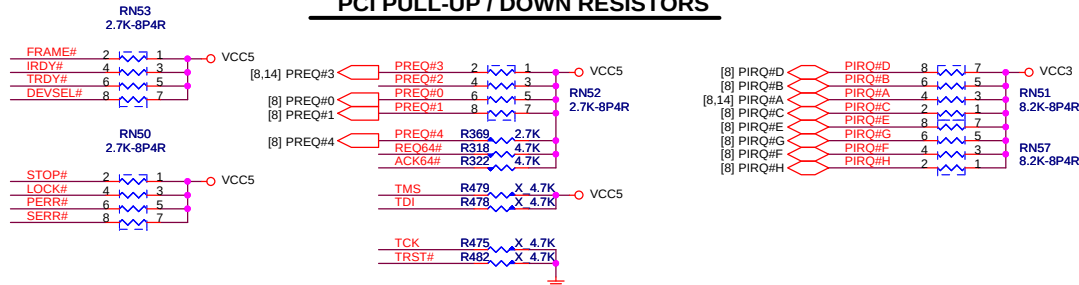
PCI RISER SLOT (PCI VER: 2.2 COMPLY)

Ver: 0D

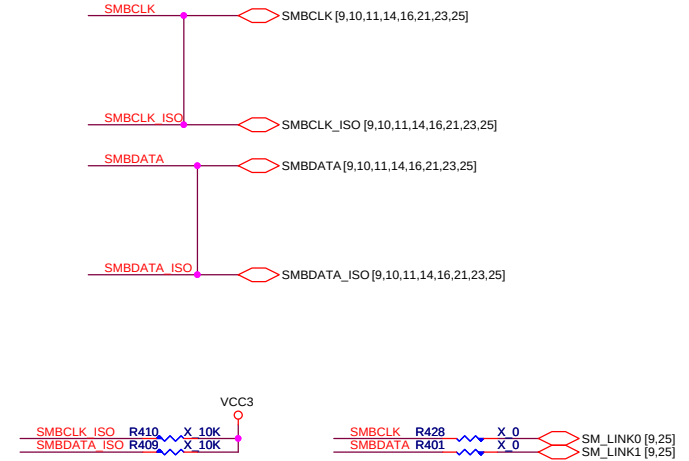


IDSEL = AD28
MASTER = PREQ#2
PIRQ#E

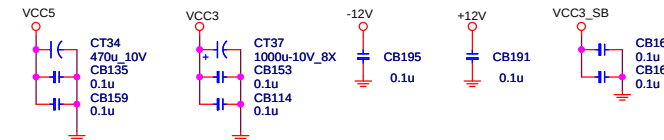
PCI PULL-UP / DOWN RESISTORS



SMBus Isolation



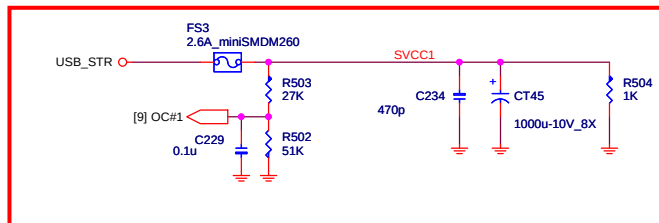
PCI SLOT DECOUPLING CAPACITORS



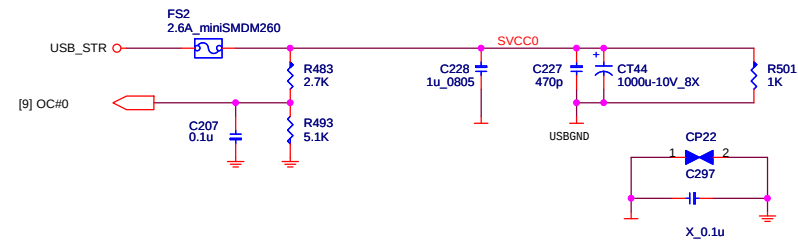
MICRO-STAR INT'L CO., LTD.		
Title: PCI Slot		
Size	Document Number: (MS-7024)	Rev: 130
Date: Wednesday, December 08, 2004	Sheet: 18	of 29

POWER CIRCUIT FOR USB PORT 4,5,6,7

Ver: 0B

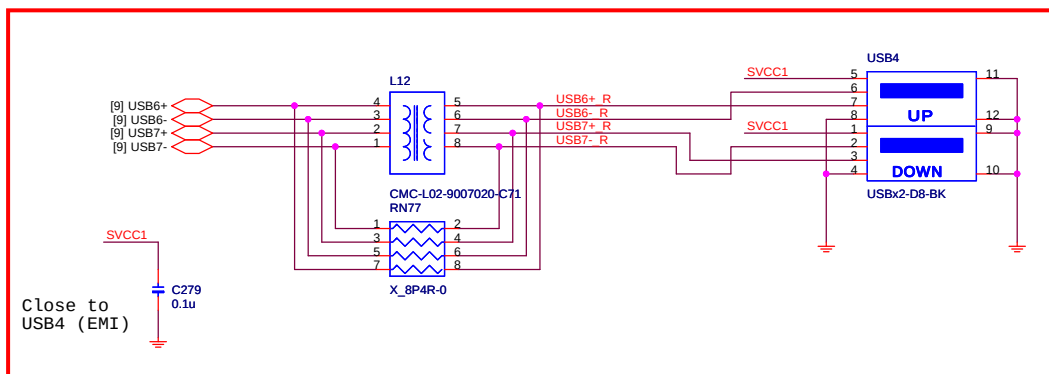


POWER CIRCUIT FOR USB PORT 0,1,2,3

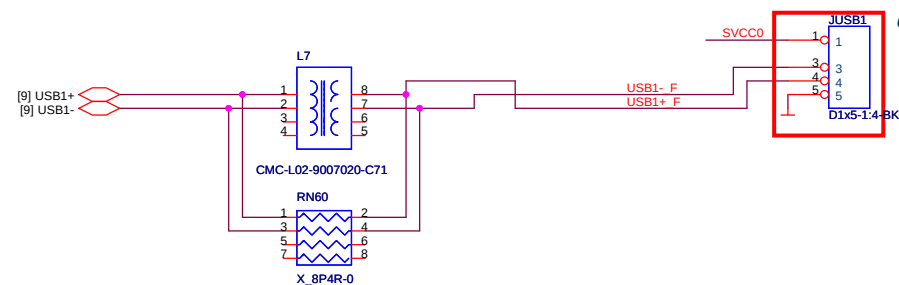


REAR PANEL USB CONNECTOR FOR USB PORT 6,7

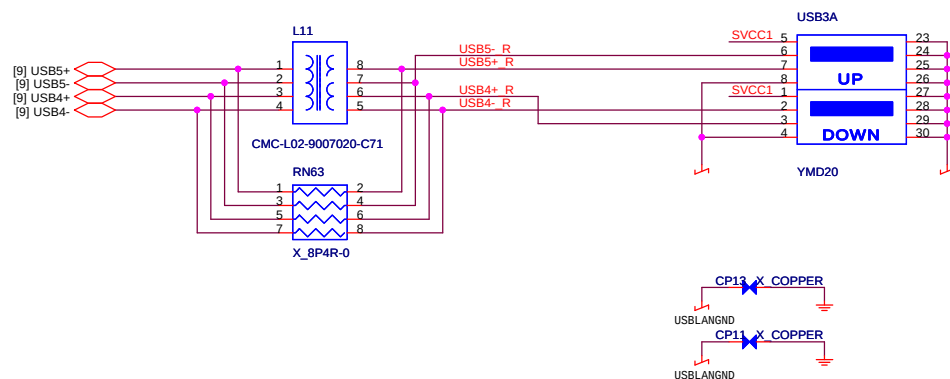
0B



FRONT PANEL USB CONNECTOR FOR USB PORT 0,1

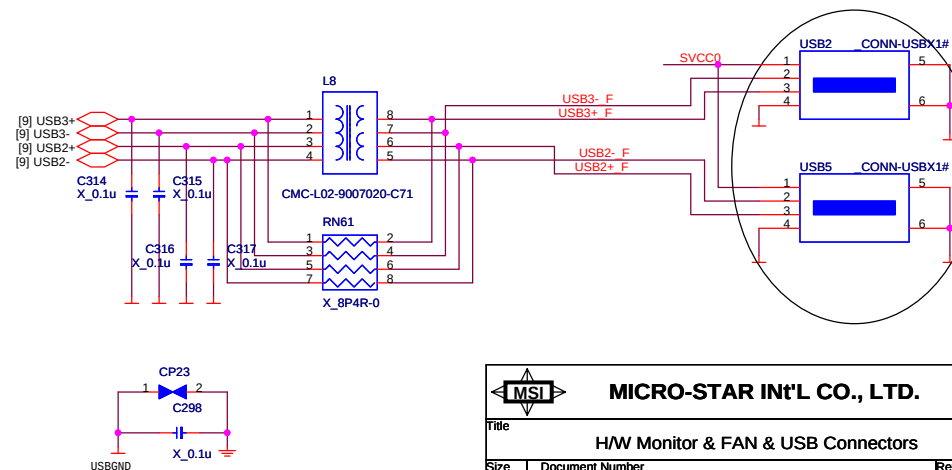


REAR PANEL USB CONNECTOR FOR USB PORT 4,5

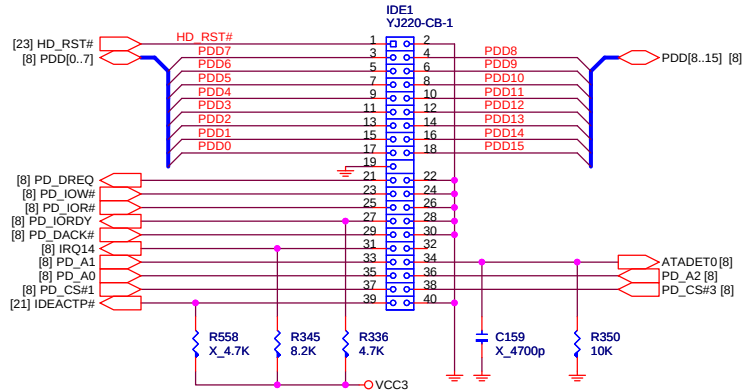


FRONT PANEL USB CONNECTOR FOR USB PORT 2,3

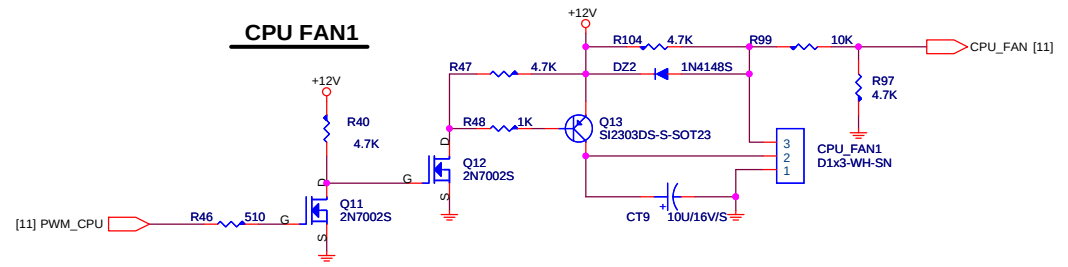
0C



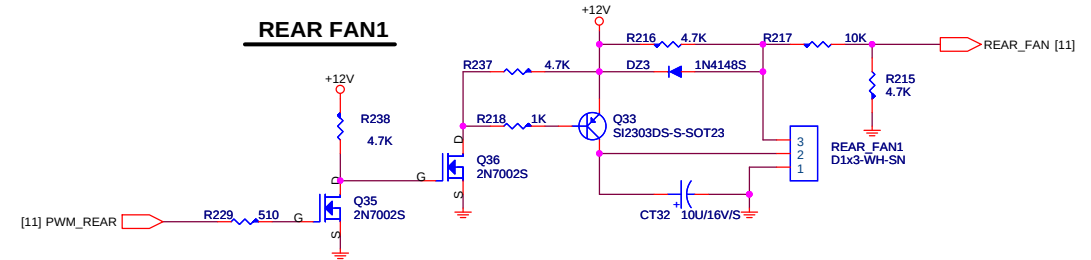
PRIMARY IDE BLOCK



CPU FAN1



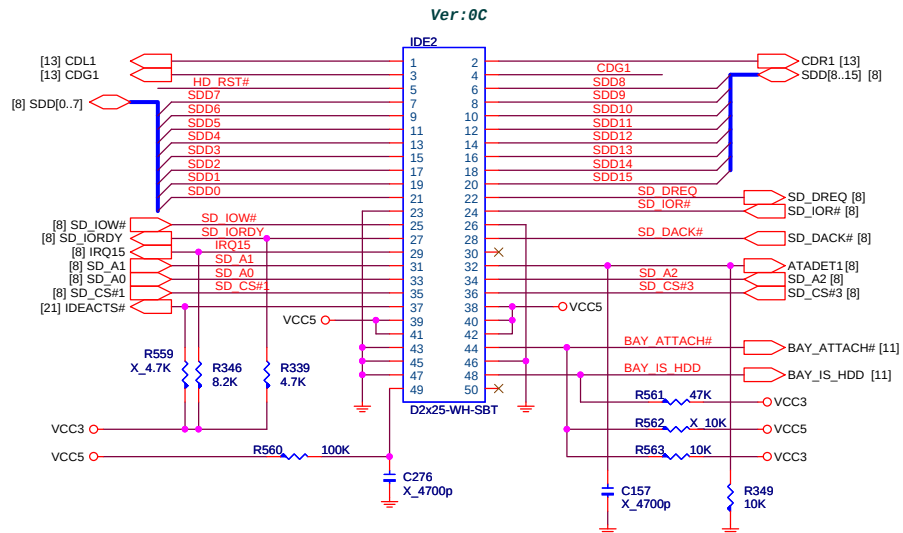
REAR FAN1



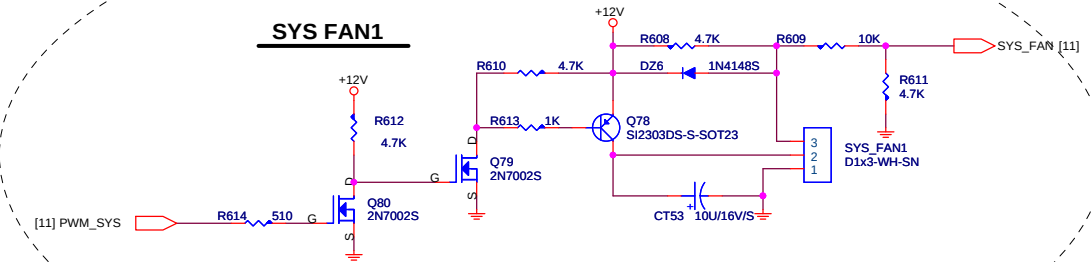
SECONDARY SLIME IDE

IBM Ultrabay Slim and Ultrabay Enhanced

Ver:0C



SYS FAN1



Ver:1.3



MICRO-STAR INT'L CO., LTD.

Title			ATA IDE & FAN CONNECTORS
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[illegible]

Ver: 0B

The diagram shows a 5V power plane (red) with six decoupling capacitors (C287-C291) connected to various signals. The signals and their corresponding capacitors are:

- SERIRQ (C287) X 0.1u
- LPC_DRQ#0 (C288) X 0.1u
- POV_ID0# (C289) X 0.1u
- POV_BLK_RST# (C290) X 0.1u
- POV_ID1# (C291) X 0.1u

The ground plane (green) is connected to the bottom of the capacitors.

Pinout diagram for the J_POV1 header of the LPC1114. The diagram shows connections for various signals including clocks, data buses, and control signals. A green circle highlights the connection for VCC3 to pin 25, which is labeled as VCC5 in the diagram.

Signal	Pin	Notes
VCC3	25	Also labeled as VCC5
POV_PCLK	1	[10]
LPC_FRAME#	2	[9,10,11]
RSTBT#	3	[9,25]
SB	4	
SBCLK	5	[9,10,11,14,16,18,23,25]
LPC_AD0	6	[9,10,11]
LPC_AD2	7	[9,10,11]
POV_ID0#	8	[9,25]
POV_ID0#	9	[9,25]
SUS_STAT#	10	[9,11,25]
LPC_DRQ#0	11	[9,11]
INTRUDER#	12	[9,25]
PCIRST#2	13	[10,11,23]
SMBDATA	14	[9,10,11,14,16,18,23,25]
LPC_AD1	15	[9,10,11]
LPC_AD3	16	[9,10,11]
POV_ID1#	17	[9,25]
SERIRQ	18	[9,11,18,25]
POV_BLK_RST#	19	[9,25]

Schematic diagram of the IDEACTS# signal path. The signal is a 20-bit bus (IDEACTS#[20]) that splits into two paths. One path goes through a BAT54A-S-SOT23 diode (D6) to the HDDLED pin. The other path goes through a 1N4148S diode (D7) to the GP33 pin [9,25].

SATA1

1 GND

2 HT+

3 HT-

4 GND

5 HR-

6 HR+

7 SDA

[9] SATA_TX0

[9] SATA_TX#

[9] SATA_RX#

[9] SATA_RX0

20:20:7:5:20<5"

Title			
ATX & FRONT PANEL & POV3			
Size	Document Number	Rev	
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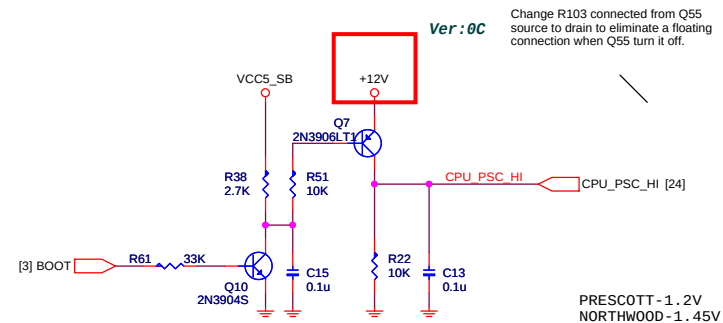
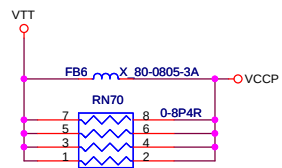
GMCH_VTT ON/OFF CIRCUIT

GMCH VCC_DAC Voltage Supplier

Intel reference GMCH VTT power circuit

GMCH VTT Generator

NW/ PSC Load Line Selection



3VSB MODE SELECT

3VSB MODE	3VOLDDEC#
SINGLE MOSFET	PULL HIGH
DUAL MOSFET	PULL LOW

Ver:0C

Ver:0C

5V DUAL Power

REAR

Low RDS ON MOSFET

INCREASE VCC5 COPPER & VIA HOLE

INCREASE GND COPPER & VIA HOLE

WIDE TRACE

3VDUAL MOS
APM2054N(SOT89)
P3055LL(SOT89)

Dual NMOS
D03-07D0303-N03
D03-0731303-A30

SWITCH:
D03-40N030B-A36
D03-20N030B-I14
D03-45N030B-P03
Regulator(T0-252)
D03-45N020B-N03
D03-40N030B-A36
D03-6530A0B-F01
Regulator(T0-263)
D03-50N034B-N03
D03-50N031B-P03
Dual NMOS
D03-07D0303-N03
D03-0731303-A30
3VDUAL MOS
APM2054N
P3055LL

SWITCH:
D03-40N030B-A36
D03-20N030B-I14
D03-45N030B-P03

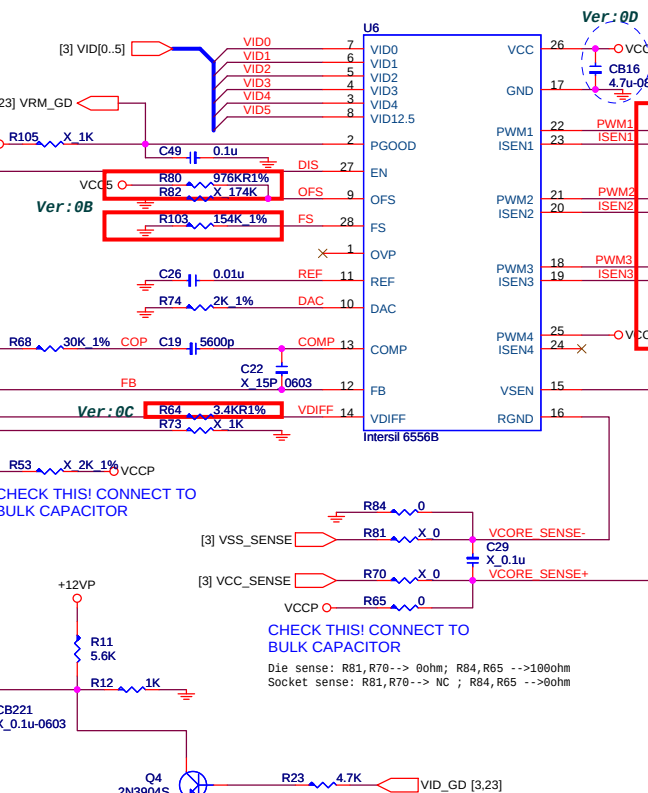
Regulator(T0-252)
D03-45N020B-N03
D03-40N030B-A36
D03-6530A0B-F01
Regulator(T0-263)
D03-50N034B-N03
D03-50N031B-P03

	VCCM
DDR400 & above	2.6V
DDR333	2.5V

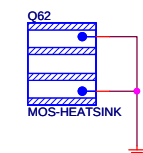
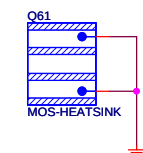
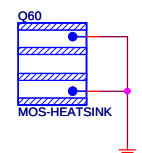
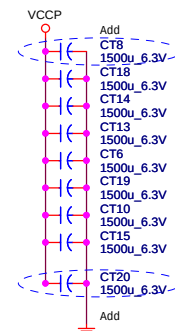
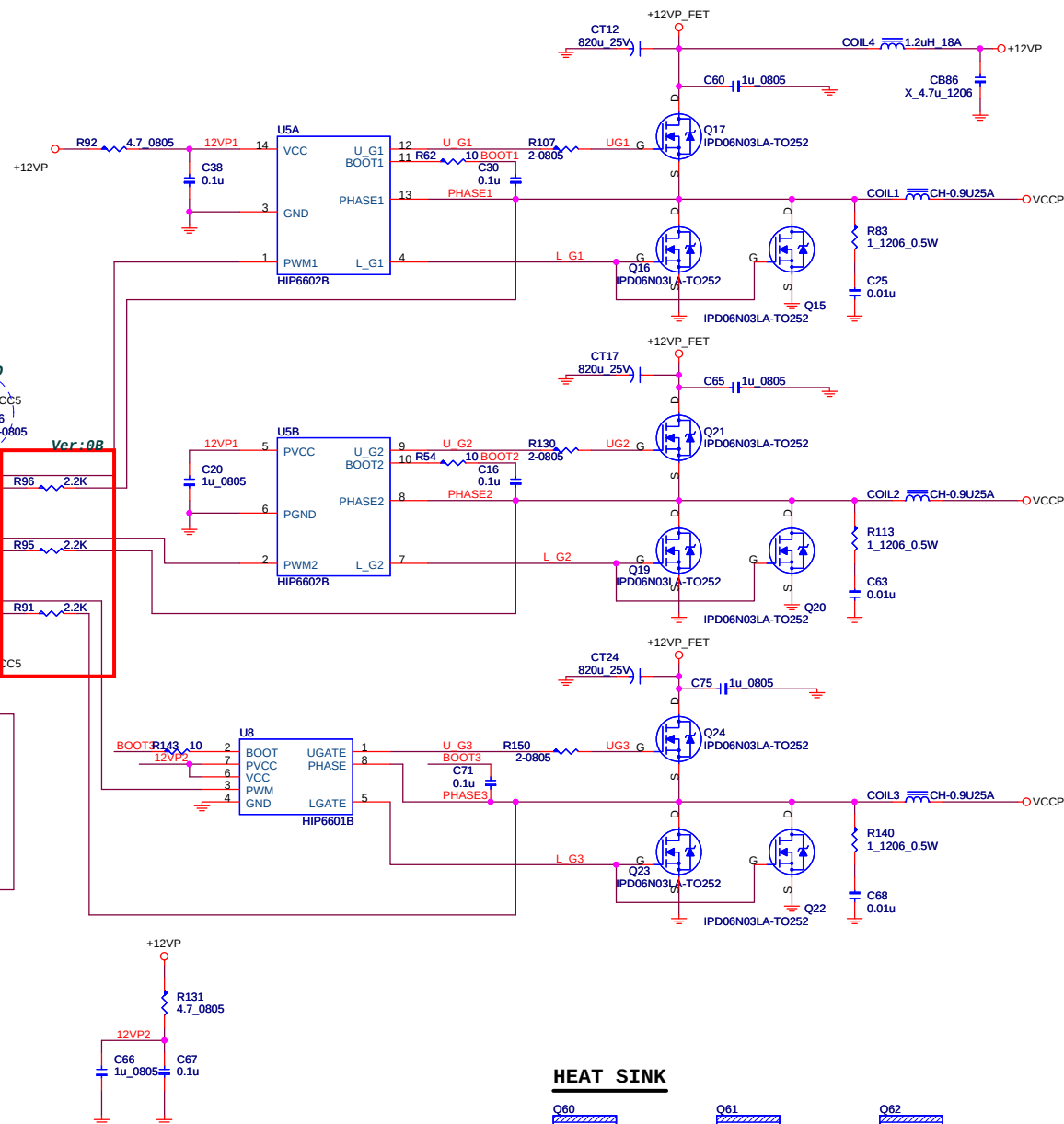
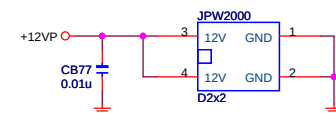
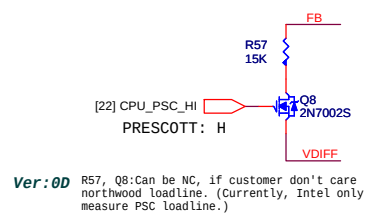
DDR VTT Power

VID Pull-Up Resistor

The diagram illustrates a VID pull-up resistor circuit. Five input lines, labeled VID1 through VID5, are shown on the left. VID1, VID2, VID3, and VID4 are each connected to a pull-up resistor (RN3, 1K_8P4R) that leads to a common node. VID5 is connected to a pull-up resistor (R86, 1K) that also leads to the same common node. This common node is connected to VCC3 and a capacitor C46 (0.1u) to ground.



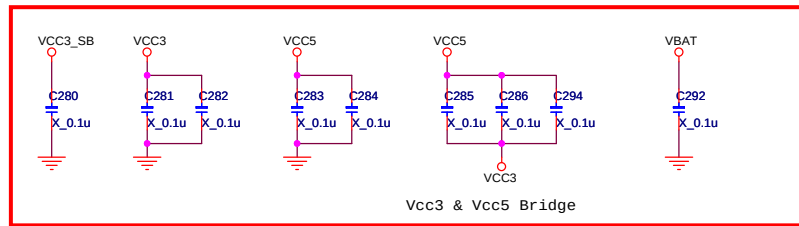
NORTHWOOD/PRESCOTT LOAD LINE SELECTOR



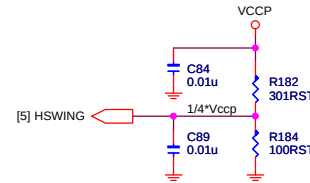
MICRO-STAR INT'L CO., LTD.

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VRM 10 - Intersil 6556B			
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EMI Decoupling CAP



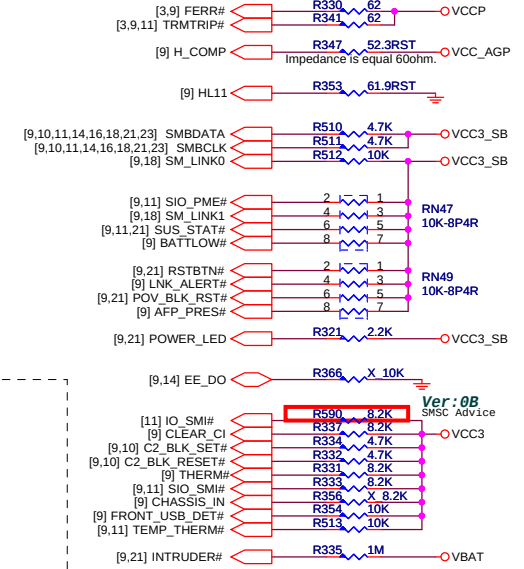
Ver:0B, 0C



ICH5 STRAPPING RESISTORS

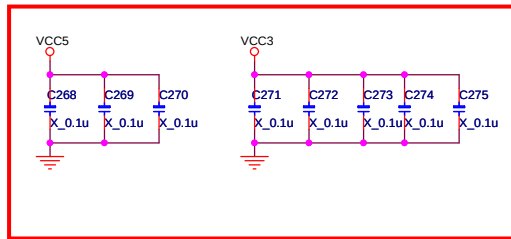
ALL COMPONENTS CLOSE TO ICH5

Trace length is less than 3inches to ICH5.



Decoupling CAP

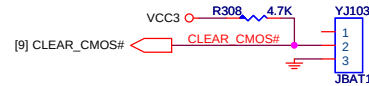
Ver:0B



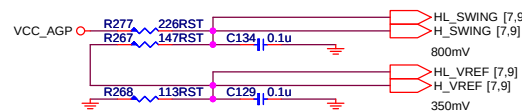
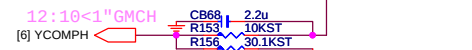
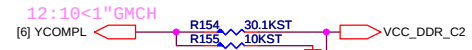
5VREF Sequencing Circuit



CLEAR CMOS JUMPER

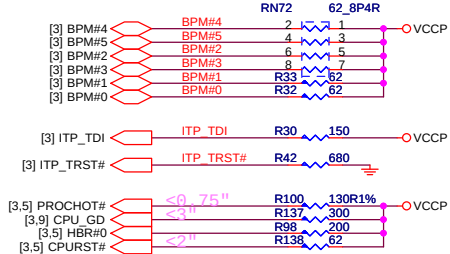


CMOS CLEAR	NORMAL	CLEAR
JBAT1	(1-2)	(2-3)

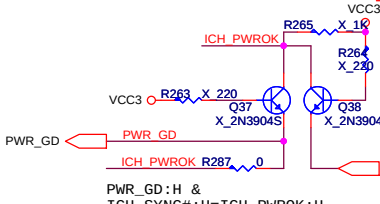
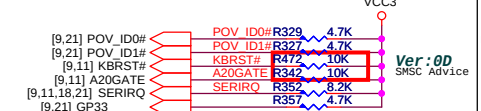
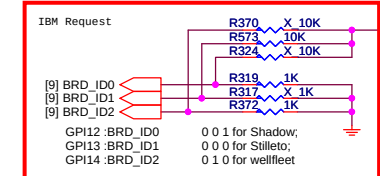
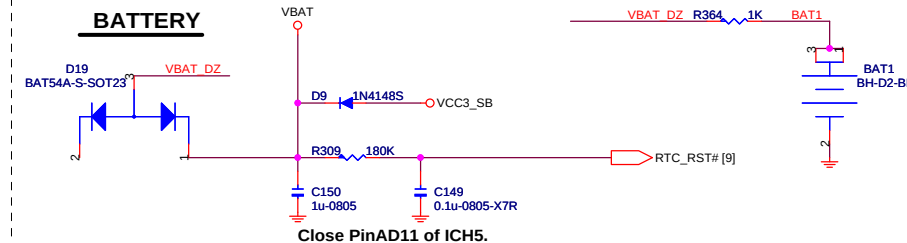


CPU STRAPPING RESISTORS

ALL COMPONENTS CLOSE TO CPU



BATTERY



ICH5

GPIO Pin	Type	Function
GPIO 0	I	ATADET0 (multifunction pin)
GPIO 1	I	Unused (multifunction pin)
GPIO 2	I	PCI_IRQ#E (multifunction pin)
GPIO 3	I	PCI_IRQ#F (multifunction pin)
GPIO 4	I	PCI_IRQ#G (multifunction pin)
GPIO 5	I	PCI_IRQ#H (multifunction pin)
GPIO 6	I	POV_ID0# (multifunction pin)
GPIO 7	I	POV_ID1# (multifunction pin)
GPIO 8	I	SIO_PME# (multifunction pin)
GPIO 9	I	USB_OC2# (multifunction pin)
GPIO 10	I	USB_OC2# (multifunction pin)
GPIO 11	I	TEMP_THERM# (multifunction pin)
GPIO 12	I	BRD_ID0 (multifunction pin)
GPIO 13	I	BRD_ID1 (multifunction pin)
GPIO 14	I	BRD_ID2 (multifunction pin)
GPIO 15	I	USB_OC3# (multifunction pin)
GPIO 16	O	Unused (multifunction pin)
GPIO 17	O	Unused (multifunction pin)
GPIO 18	O	Unused (multifunction pin)
GPIO 19	O	CLEAR_CI (multifunction pin)
GPIO 20	O	C2_BLK_RESET# (multifunction pin)
GPIO 21	O	C2_BLK_SET# (multifunction pin)
GPIO 22	O(OD)	SIO_SMI# (multifunction pin)
GPIO 23	O	CHASSIS_IN (multifunction pin)
GPIO 24	I/O	Unused (multifunction pin)
GPIO 25	I/O	POWER_LED (multifunction pin)
GPIO 27	I/O	POV_BLK_RST# (multifunction pin)
GPIO 28	I/O	ENET_DIS_N (multifunction pin)
GPIO 32	I/O	CLEAR_CMOS# (multifunction pin)
GPIO 33	I/O	Unused (multifunction pin)
GPIO 34	I/O	Unused (multifunction pin)
GPIO 40	I	PREQ#4 (multifunction pin)
GPIO 41	I	Unused (multifunction pin)
GPIO 48	O	PGNT#4 (multifunction pin)
GPIO 49	O	CPU_GD (multifunction pin)

Flash ROM(PCB REVISION ID)

GPIO Pin	Type	0A	0B	0C	
GPI 0	I	0	1	0	
GPI 1	I	0	0	1	
GPI 2	I	0	0	0	
GPI 3	I	0	0	0	
GPI 4	I	H:10/100 ETHERNET L:GIGABIT ETHERNET LAN			

PCI Config.

DEVICE	MCP1 INT Pin	REQ # / GNT #	IDSEL	CLOCK	CLK GEN PIN OUT
PCI Riser Slot	PIRQE	PCI_REQ#2	AD28	PCICLK2	7 (PCI_CLK2)
	PIRQF	PCI_GNT#2		PCICLK1	8 (PCI_CLK1)
	PIRQG	PCI_REQ#4			
	PIRQH	PCI_GNT#4			

LPC Super I/O

GPIO Pin	Type	Function
GPIO 10	I	BAY_ATTACH#
GPIO 11	I	BAY_IS_HDD
GPIO 12	I	Unused
GPIO 13	I	Unused
GPIO 14	I	Unused
GPIO 15	I	Unused
GPIO 16	I/O	Unused
GPIO 17	I/O	Unused
GPIO 20	I/O	Unused
GPIO 21	I/O	DSB#
GPIO 22	I/O	MOB#
GPIO 24	I/O	SIO_ADDR
GPIO 25	I/O	Unused
GPIO 26	I	Unused
GPIO 27	I	IO_SMI#
GPIO 30	O	CPU_FAN1
GPIO 31	O	REAR_FAN1
GPIO 32	I/O	PWM_CPU
GPIO 33	I/O	PWM_REAR
GPIO 34	O	Unused
GPIO 35	I/O	Unused
GPIO 36	O	KBRST#
GPIO 37	O	A20GATE
GPIO 40	O	DRVDE0
GPIO 41	I/O	DRVDE1
GPIO 42	O	SIO_PME#
GPIO 43	I	DDRC_LOCK_DIS
GPIO 50	I/O	RIB#
GPIO 51	I/O	DCDB#
GPIO 52	I	SINB
GPIO 53	I/O	SOUTB
GPIO 54	I/O	DSRB#
GPIO 55	I/O	RTSB#
GPIO 56	I/O	CTSB#
GPIO 57	I/O	DTRB#
GPIO 60	I/O	Unused
GPIO 61	I/O	Unused

DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	A0H	MCLK_A0/MCLK_A#0 MCLK_A1/MCLK_A#1 MCLK_A2/MCLK_A#2
DIMM 2	A2H	MCLK_B0/MCLK_B#0 MCLK_B1/MCLK_B#1 MCLK_B2/MCLK_B#2

PCI RESET DEVICE

Signals	Target
PCIRST#1	PCI slot, LAN
PCIRST#2	Super I/O, FWH, POV3
PCIRST_ICH5#	Northbridge , MS-5
HDDRST#	Primary IDE

JUMPER SETTING

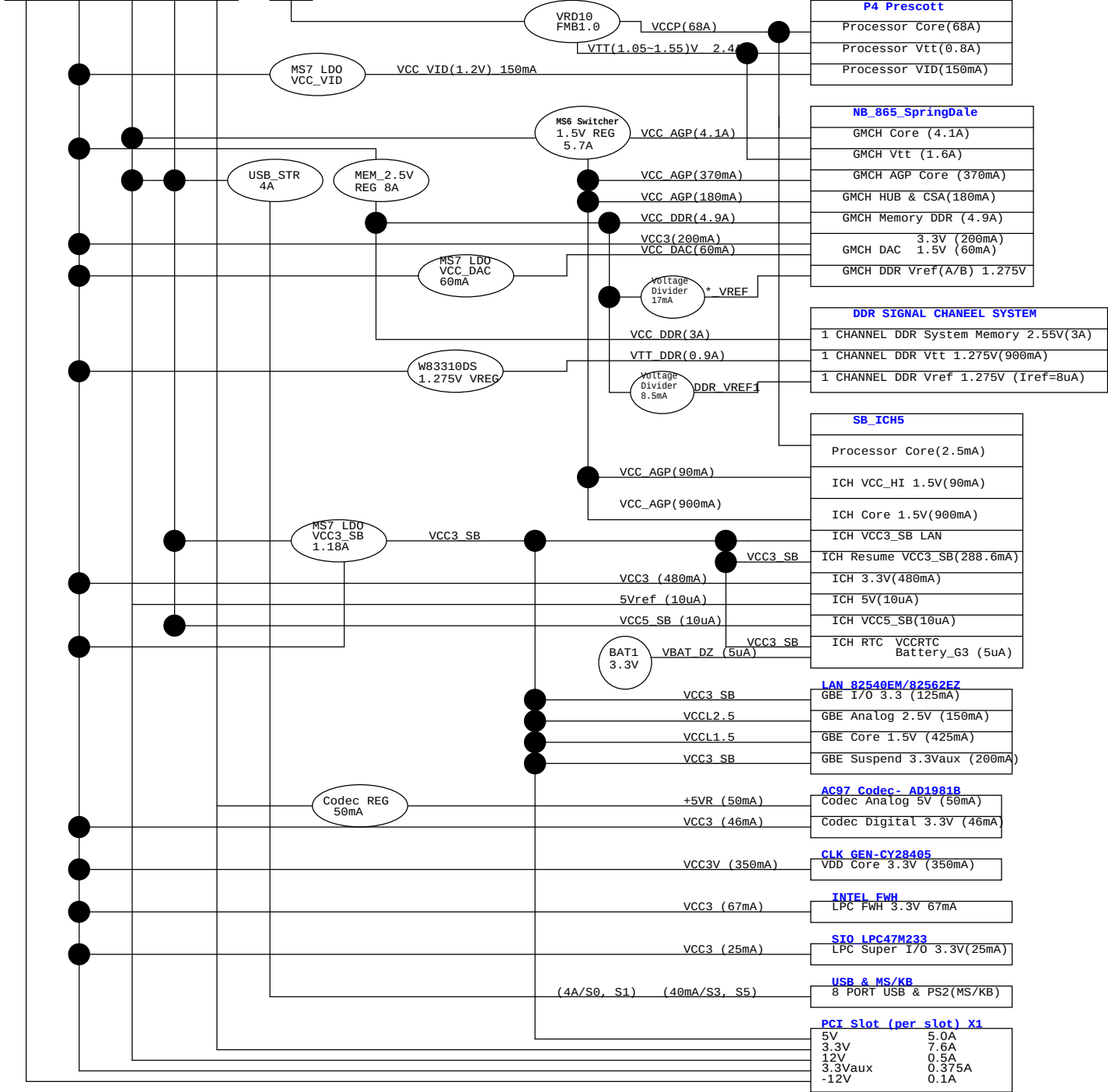
JBAT1	(1-2)NORMAL	(2-3)CLEAR
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ATX POWER Supply				
-12V	3.3V	5V	5VSB 2A	12V

12V POWER

12VP

POWER DELIVERY MAP



VRM SPEC		Transition	Sustain	Power Consumption
VRM9.0	FMB1.0	60A	50A	
	FMB2.0	70A	60A	
VRM10.0	FMB1.0	78A	68A	89W/69
	FMB1.5	91A	80A	103W/74

P4 Prescott	
Processor Core(68A)	
Processor Vtt(0.8A)	
Processor VID(150mA)	

NB_865_Springdale	
GMCH Core (4.1A)	
GMCH Vtt (1.6A)	
GMCH AGP Core (370mA)	
GMCH HUB & CSA(180mA)	
GMCH Memory DDR (4.9A)	
GMCH DAC 3.3V (200mA)	
GMCH DAC 1.5V (60mA)	
GMCH DDR Vref(A/B) 1.275V	

DDR SIGNAL CHANEEL SYSTEM	
1 CHANNEL DDR System Memory 2.55V(3A)	
1 CHANNEL DDR Vtt 1.275V(900mA)	
1 CHANNEL DDR Vref 1.275V (Iref=8uA)	

SB_ICH5	
Processor Core(2.5mA)	
ICH VCC_HI 1.5V(90mA)	
ICH Core 1.5V(900mA)	
ICH VCC3_SB LAN	
ICH Resume VCC3_SB(288.6mA)	
ICH 3.3V(480mA)	
ICH 5V(10uA)	
ICH VCC5_SB(10uA)	
ICH RTC VCCRTC Battery_G3 (5uA)	

LAN_82540EM/82562EZ	
GBE I/O 3.3 (125mA)	
GBE Analog 2.5V (150mA)	
GBE Core 1.5V (425mA)	
GBE Suspend 3.3Vaux (200mA)	

AC97 Codec- AD1981B	
Codec Analog 5V (50mA)	
Codec Digital 3.3V (46mA)	

CLK_GEN-CY28485	
VDD Core 3.3V (350mA)	

INTEL FW	
LPC FW 3.3V 67mA	

STO LPC47M233	
LPC Super I/O 3.3V(25mA)	

USB & MS/KB	
8 PORT USB & PS2(MS/KB)	

PCI Slot (per slot) X1	
5V 5.0A	
3.3V 7.6A	
12V 0.5A	
3.3Vaux 0.375A	
-12V 0.1A	



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MS-7024 Revision History List			
Ver .	DATE	Schematic Change List	Page
0A	2003.09.24	1. Create MS-7024 Project for IBM (Wellfleet) design.	
0B	2004.02.13	1. Front 4 port USB change to 2 port USB. 2. Add JUSB1 pin header (1x5) for card reader.. 3. Add Rear 2 port USB connector. 4. Secondary Silm IDE change to IBM Ultrabay Slim and Ultrabay Enhanced spec.	P.19 P.19 P.19 P.19
	2004.02.20	5. Add Front_FAN1 for thermal issue reserve. 6. EMI coupling cap reserve. 7. Intel LAN Kinnereth / Kenai 2 EMI issue update.	P.20 P.21 P.25 P.14
0C	2004.02.13	1. Front panel spec update: Line-Out, MIC, USB, USB 2. Rear panel spec update: Line-Out, Line-In. 3. IBM Wellfleet broad ID circuit update. 4. IBM Wellfleet Logo location update. 5. POV3 card mechanical issue with C128, JBAT1. 6. Video sink buffers circuit added in. 7. IEEE 10/100/1000 LAN solution update.	Layout P.13 Layout Layout P.12
0D	2004.03.31	1. Change LAN chipset for 82540EM to 82541EI. 2. Parallel port proposal from IBM suggestion change 33ohm to 0ohm. 3. Add RSS_CLK for IBM Retail Store Systems (RSS) group requirement. 4. Change H-sync and V-sync resistor value form 47ohm to 33ohm for EMI issue. 5. Add C301, C302, C303 cap at North-Bridge side for EMI concern.	P.14 P.15 P.11 P.10 P.11 P.12
0E	2004.04.30	1. Update 82541EI LAN Enable/Disable circuit. 2. Update component RSL0005 for IBM request. 3. Reserve SIO/GPIO pin for LAN enable/disable function used. 4. Change SATA connector with housing spec.	P.15 P.1 P.15 P.21
100	2004.05.20	1. Change R21 to 27Kohm for internal speaker small volume issue.	P.13
110	2004.06.25	1. Update mounting hole for EMI concern. 2. Reserve C314, C315, C316, C317 for USB EMI concern. 3. Change R8, R20 to 15Kohm, R21 to 33Kohm for internal speaker small olume issue.	P.19
11A	2004.07.21	1. Add RGB signal protection diode for No display issue. 2. Add L-C filter for RGB signal (Reference Intel Grantsdale suggestion).	P.12
11B	2004.07.23	1. Add DDCCL, DDCDA signal protection diode for No display issue. 2. Add serier resistor (R607, R606) on H-sync, Vsync signal at VGA connector and buffer side.	P.12
120	2004.08.27	1. Change to Ver.120	

Ver .	DATE	Schematic Change List
1.3	2004.11.12	1. Modify J_POV1 schematic (Slove password issue when using POV3), short pin 27 & 29 2. Change board ID (Just change the PCB Revision ID from 0000b to 0001b by pulling REV0 up (R414) instead of down (R413). 3. Add system FAN
1.3	2004.12.02	1. Change LM78L05-SOT89 to YLT1087S-0.8A for AUDIO regulator on page 13.

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REVISION HISTORY			
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