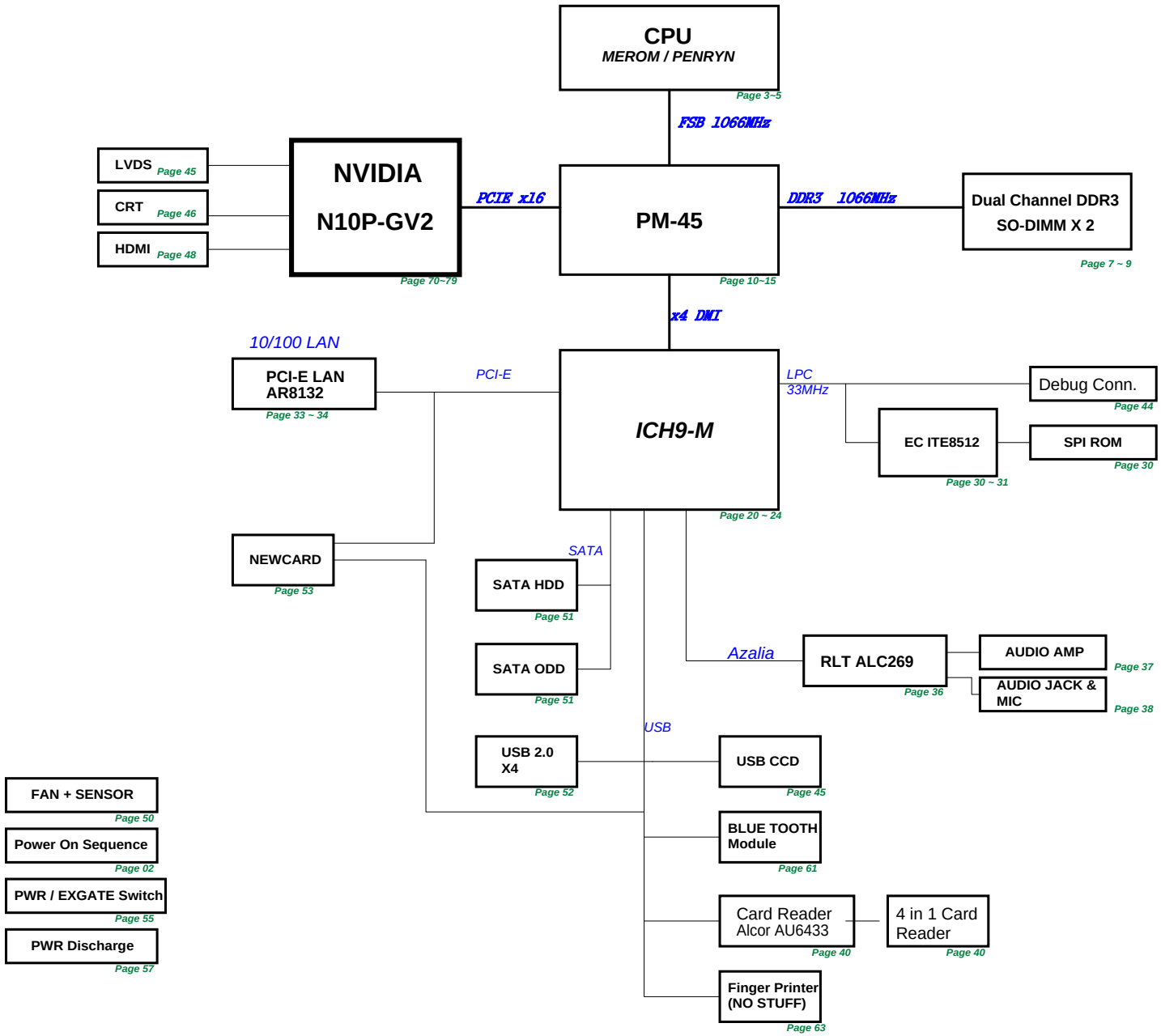
F83Vf MonteVina BLOCK DIAGRAM



Power

- VCORE — Page 80
- System — Page 81
- 1.5VS & 1.05VS — Page 82
- DDR & VTT — Page 83
- 1.8VS — Page 84
- VGA_VCORE — Page 85
- Charger — Page 88
- Detect — Page 90
- Load Switch — Page 91
- Power Protect — Page 92
- Power Protect — Page 93

PEGATRON

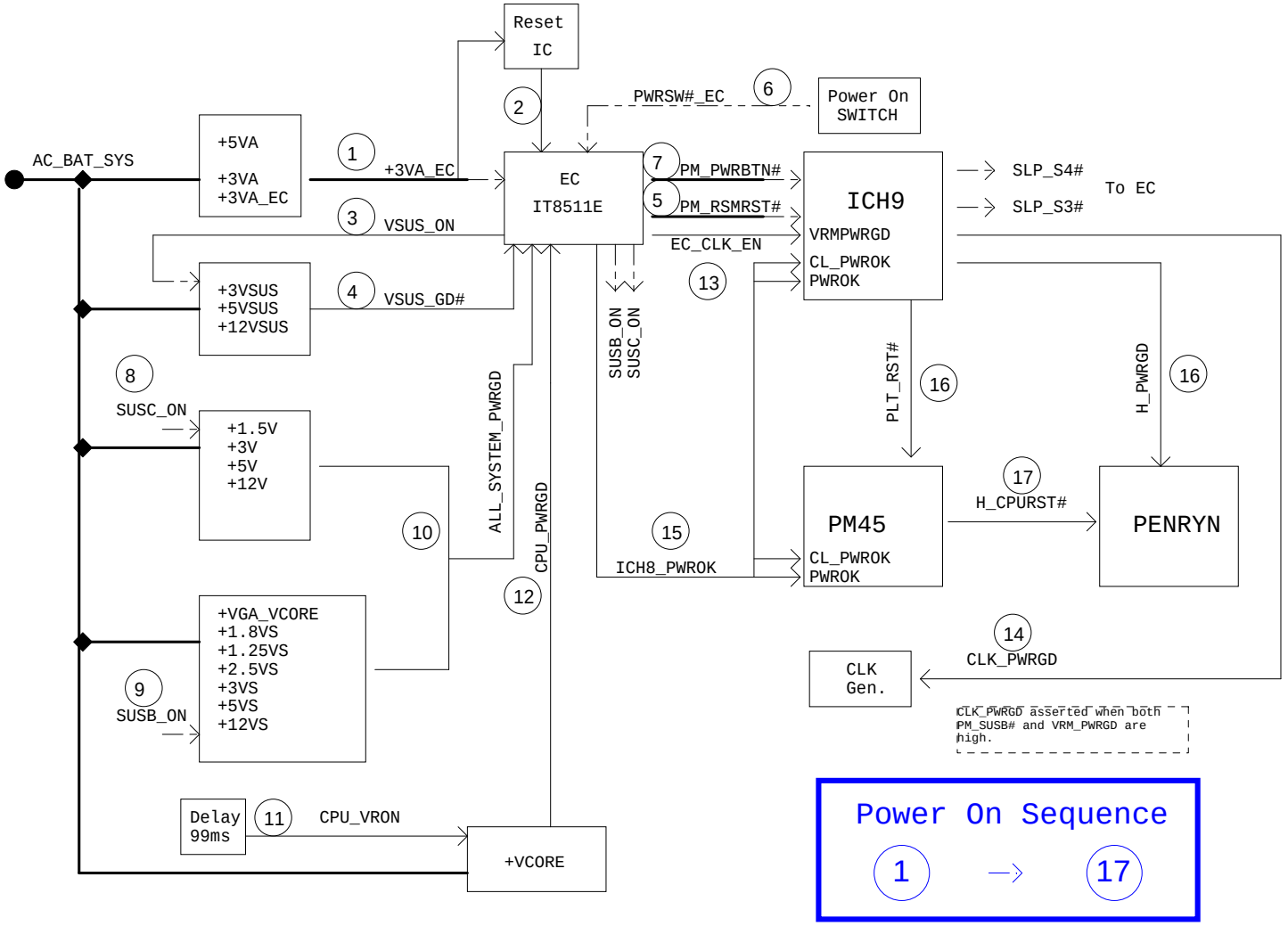
Title : Block Diagram

PEGATRON COMPUTER INC

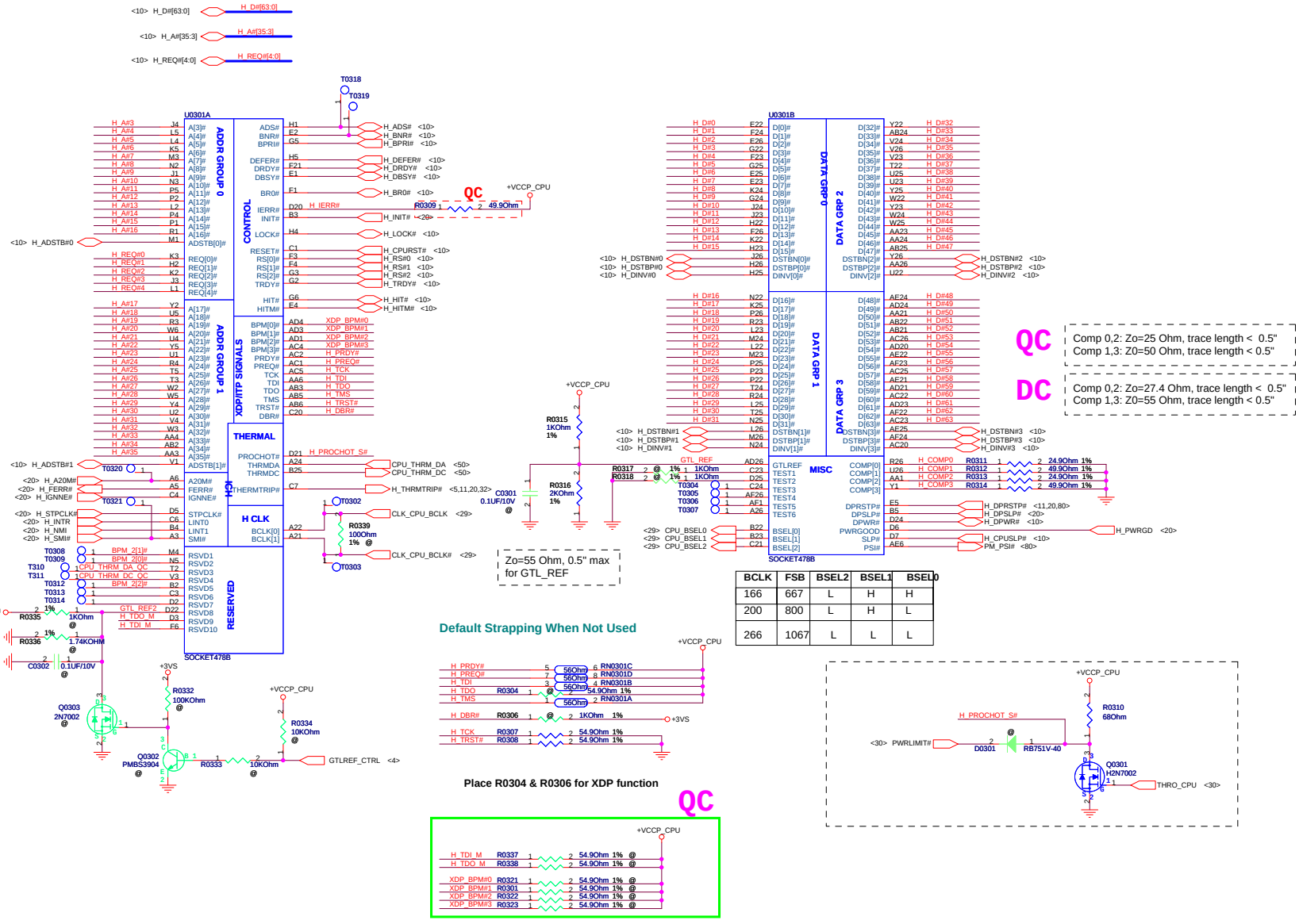
Engineer: Zack Kuo

Size	Project Name	Rev
C	F83Vf	1.1
	P/N <OrgAddr2>	

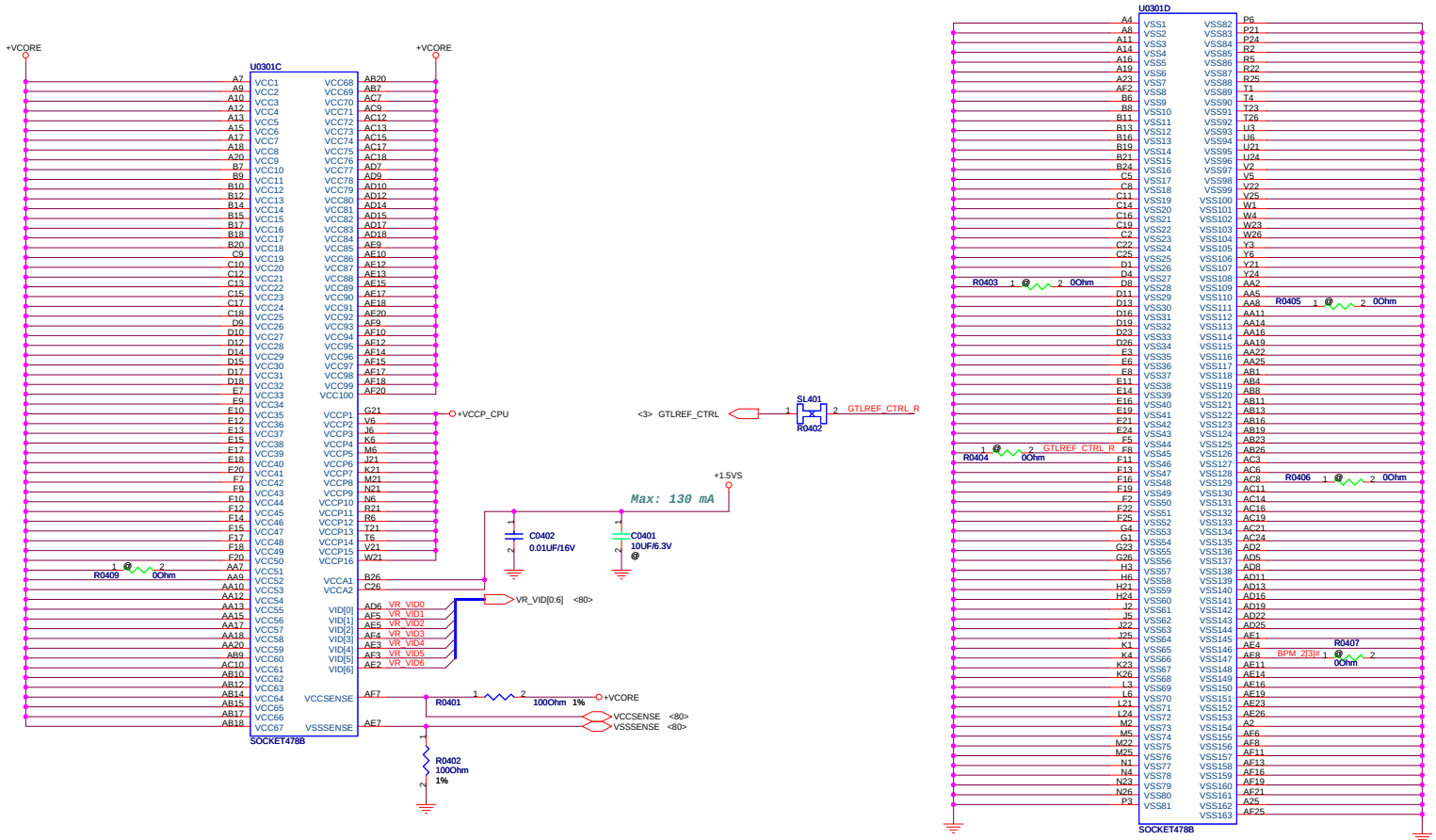
Date: Thursday, July 16, 2009 Sheet 1 of 100



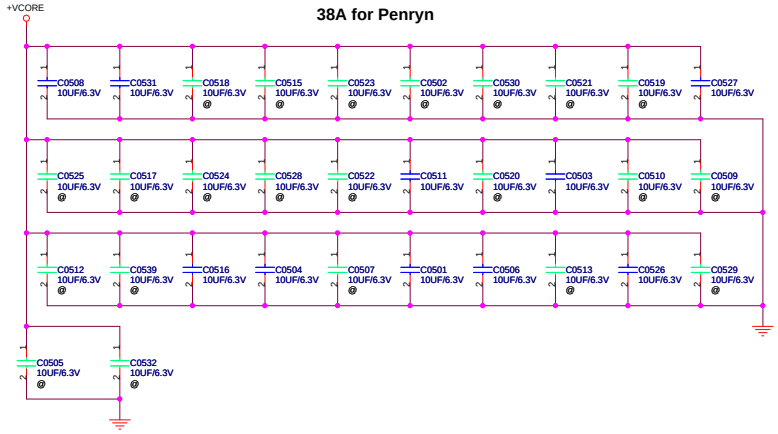
PEGATRON	Title : Power Sequence		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 2 of 100		

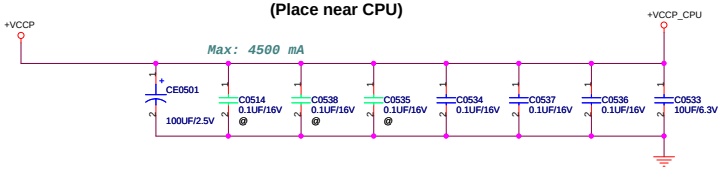


Title :	Penryn(1)		
PEGATRON COMPUTER INC	Engineer:	Zack Kuo	
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 3 of 100		



PEGATRON	Title :	Penryn(2)	
PEGATRON COMPUTER INC	Engineer:	Zack Kuo	
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 4 of 100		

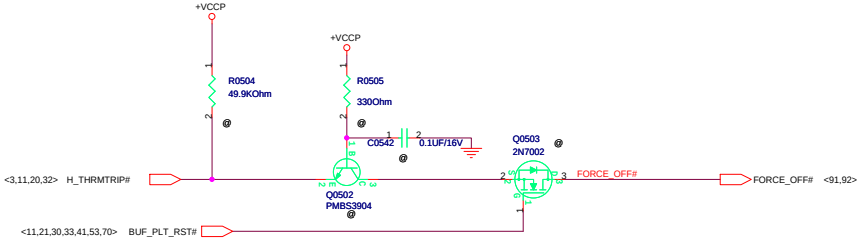




Decoupling guide from Intel

VCORE	22uF/10V r 10uF	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs
	150uF	* 1pcs ?
	10uF	* 1pcs ?

+VCORE Mid-Frequency Capacitor
*Intel: 22UF *32*
*F83Vf: 10UF*12*
+VCCP Decoupling Capacitor
*Intel: 270UF *1, 0.1UF *6*
*F3S: 100UF *1, 0.1UF *3*
V1V: ?



Thermal Trip signal (From CPU to ICH-9M and sequence)

PEGATRON	Title : CPU Decouple		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 5 of 100		

PEGATRON

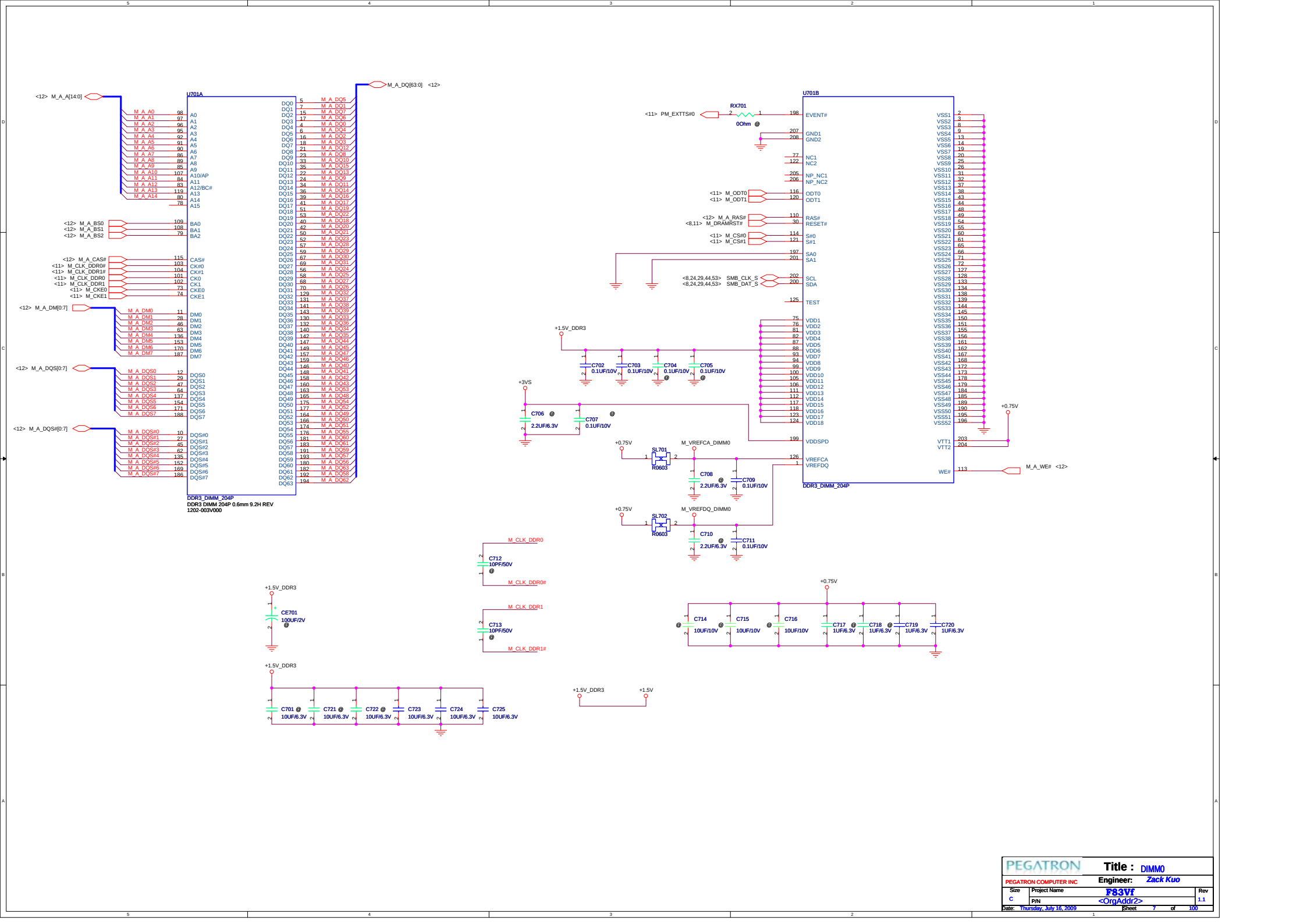
Title : CPU ***

PEGATRON COMPUTER INC

Engineer: Zack Kuo

Size	Project Name	Rev
C	F83Vf	1.1
	P/N <OrgAddr2>	

Date: Thursday, July 16, 2009 Sheet 6 of 100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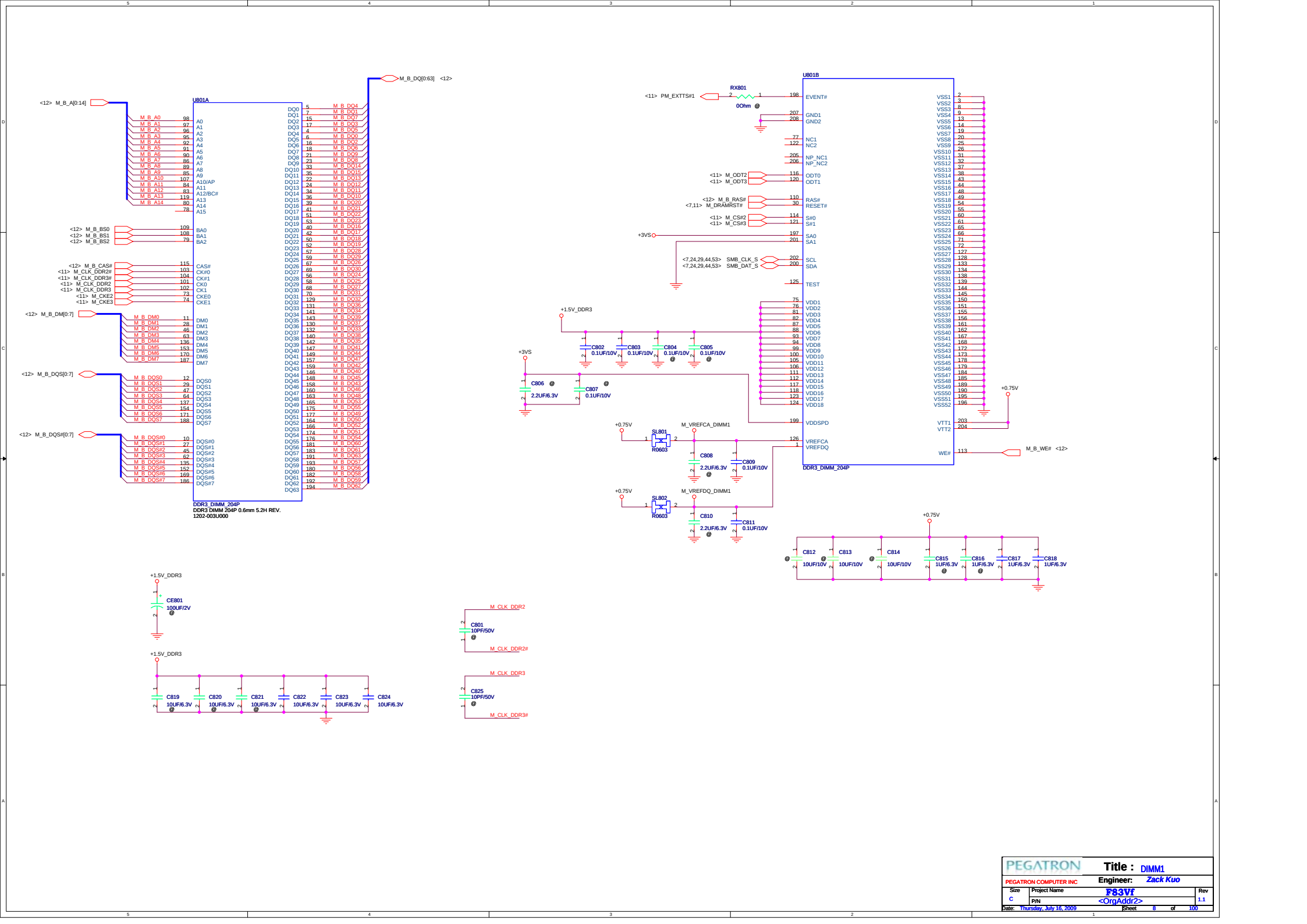
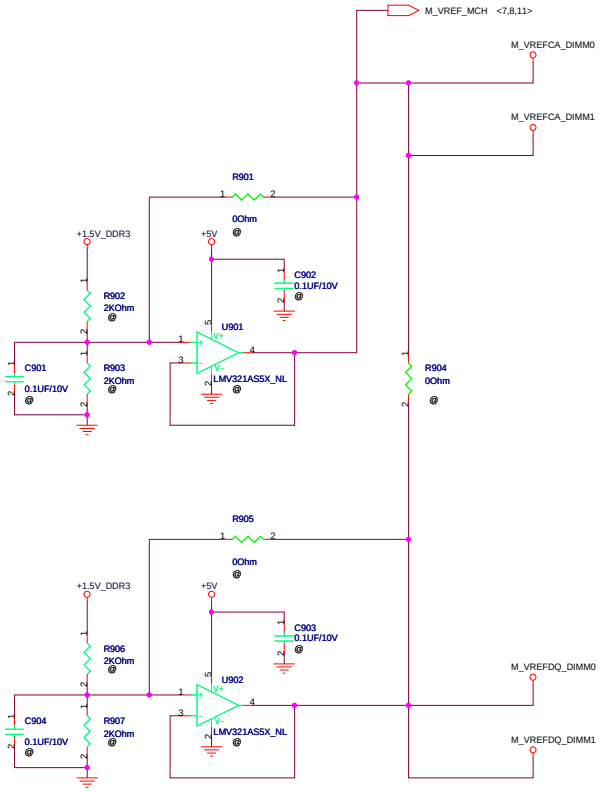
DDR3 DIMM 204P 0.6mm 9.2H REV
1202-003V000
U701B
DDR3_DIMM_204P
RX701
0Ohm @
M_A_DQ[63:0]
M_A_A[14:0]
M_A_BS0
M_A_BS1
M_A_BS2
M_A_CAS#
M_CLK_DDR0#
M_CLK_DDR1#
M_CLK_DDR0
M_CLK_DDR1
M_CKE0
M_CKE1
M_A_DM[0:7]
M_A_DQS[0:7]
M_A_DQS#[0:7]
PM_EXTTS#0
M_ODT0
M_ODT1
M_A_RAS#
M_DRAMRST#
M_CS#0
M_CS#1
SMB_CLK_S
SMB_DAT_S
M_A_WE#
+1.5V_DDR3
+3VS
+0.75V
M_VREFCA_DIMM0
M_VREFDQ_DIMM0
SL701
SL702
R0603
C702 0.1UF/10V
C703 0.1UF/10V
C704 0.1UF/10V
C705 0.1UF/10V
C706 @ 2.2UF/6.3V
C707 @ 0.1UF/10V
C708 @ 2.2UF/6.3V
C709 @ 0.1UF/10V
C710 @ 2.2UF/6.3V
C711 @ 0.1UF/10V
C712 10PF/50V @
C713 10PF/50V @
CE701 100UF/2V @
C701 @ 10UF/6.3V
C721 @ 10UF/6.3V
C722 @ 10UF/6.3V
C723 10UF/6.3V
C724 10UF/6.3V
C725 10UF/6.3V
C714 @ 10UF/10V
C715 @ 10UF/10V
C716 @ 10UF/10V
C717 @ 1UF/6.3V
C718 @ 1UF/6.3V
C719 1UF/6.3V
C720 1UF/6.3V
+1.5V
PEGATRON
PEGATRON COMPUTER INC
Title : DIMM0
Engineer: Zack Kuo
Size C
Project Name F83Vf
P/N <OrgAddr2>
Rev 1.1
Date: Thursday, July 16, 2009
Sheet 7 of 100



PEGATRON	Title : DIMM1		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 8 of 100		



PEGATRON

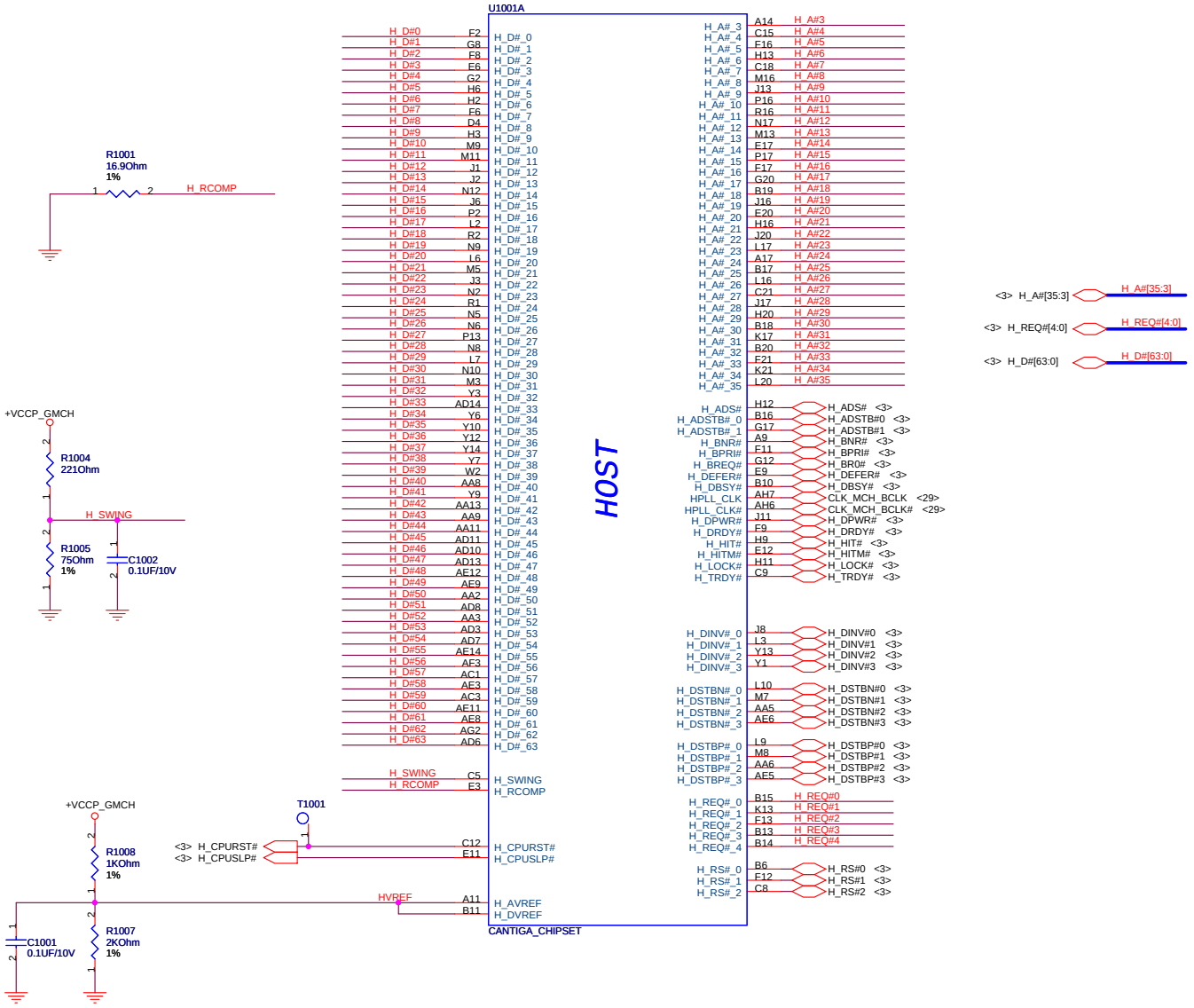
PEGATRON COMPUTER INC

Title : DIMM_TERM

Engineer: Zack Kuo

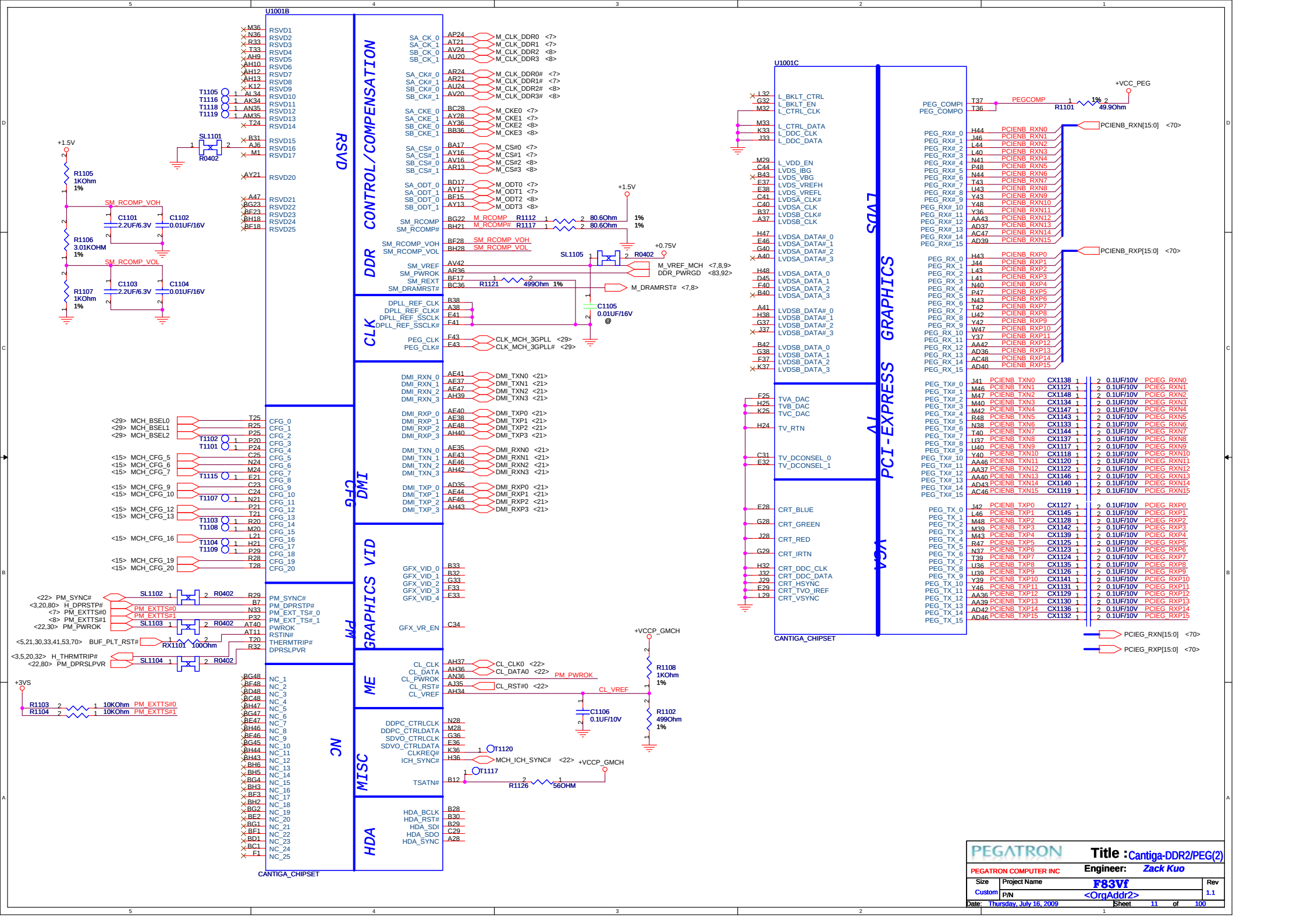
Size	Project Name	Rev
C	F83Vf	1.1
	P/N <OrgAddr2>	

Date: Thursday, July 16, 2009 Sheet 9 of 100



Cap 0.1uF within 100 mils from GMCH

PEGATRON	Title : Cantiga -- CPU (1)	
PEGATRON COMPUTER INC	Engineer: Zack Kuo	
Size: Custom	Project Name: F83Vf	Rev: 1.1
	P/N: <OrgAddr2>	
Date: Thursday, July 16, 2009	Sheet 10 of 100	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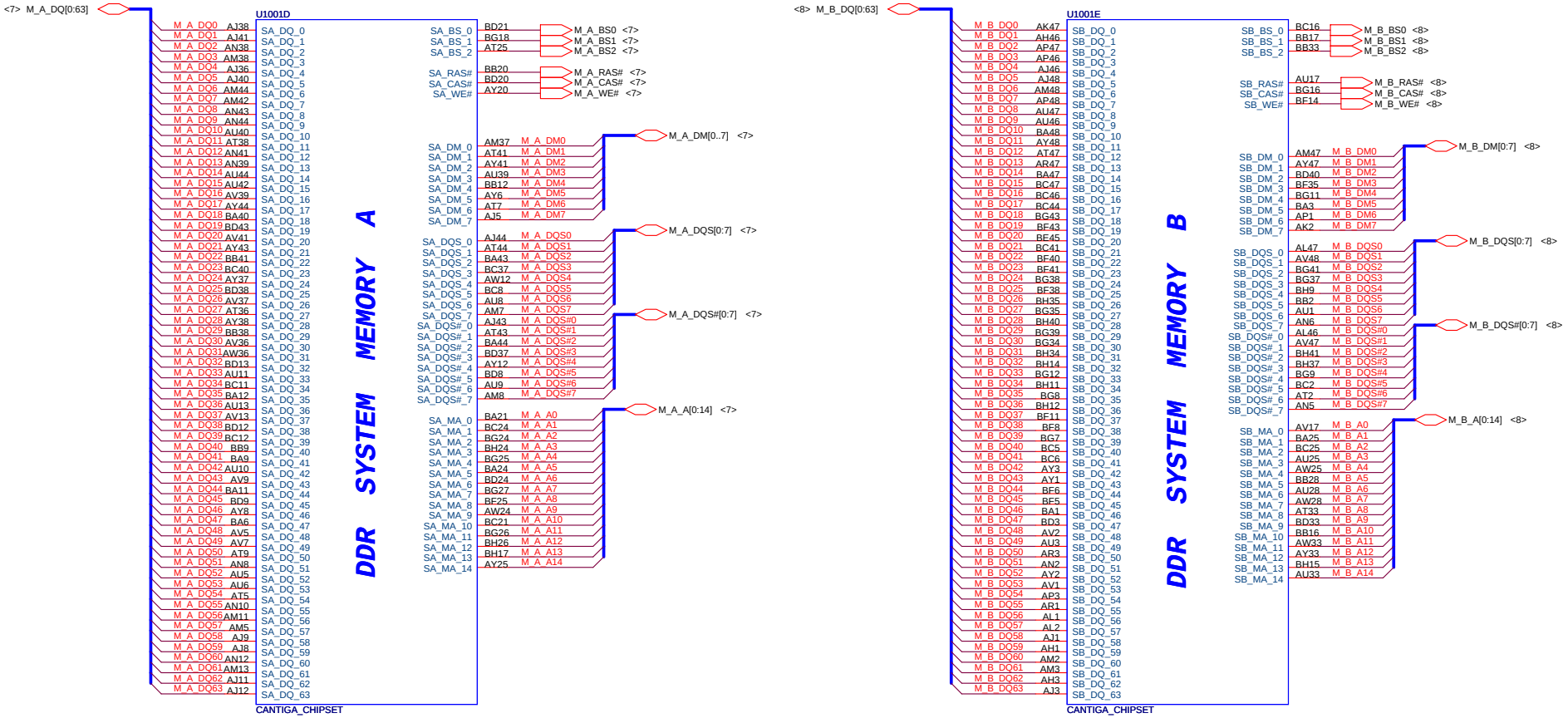
CONTROL/COMPENSATION
DDR
CLK
CFG
DMI
GRAPHICS VID
PM
ME
MISC
HDA
NC
CANTIGA_CHIPSET
U1001C
LVDS
PCI-EXPRESS GRAPHICS
VGA
CANTIGA_CHIPSET
PEGATRON
Title : Cantiga-DDR2/PEG(2)
PEGATRON COMPUTER INC
Engineer: Zack Kuo
Size: Custom
Project Name: F83Vf
Rev: 1.1
P/N: <OrgAddr2>
Date: Thursday, July 16, 2009
Sheet 11 of 100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M_A_DQ6 AM44
M_A_DQ7 AM42
M_A_DQ8 AN43
M_A_DQ9 AN44
M_A_DQ10 AU40
M_A_DQ11 AT38
M_A_DQ12 AN41
M_A_DQ13 AN39
M_A_DQ14 AU44
M_A_DQ15 AU42
M_A_DQ16 AV39
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M_A_DQ23 BC40
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M_A_DQ29 BB38
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M_B_DQ62 AH3
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M_B_DQS0 M_B_DQS1 M_B_DQS2 M_B_DQS3 M_B_DQS4 M_B_DQS5 M_B_DQS6 M_B_DQS7
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M_B_DQS#0 M_B_DQS#1 M_B_DQS#2 M_B_DQS#3 M_B_DQS#4 M_B_DQS#5 M_B_DQS#6 M_B_DQS#7
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AV17 BA25 BC25 AU25 AW25 BB28 AU28 AW28 AT33 BD33 BB16 AW33 AY33 BH15 AU33
M_B_A0 M_B_A1 M_B_A2 M_B_A3 M_B_A4 M_B_A5 M_B_A6 M_B_A7 M_B_A8 M_B_A9 M_B_A10 M_B_A11 M_B_A12 M_B_A13 M_B_A14
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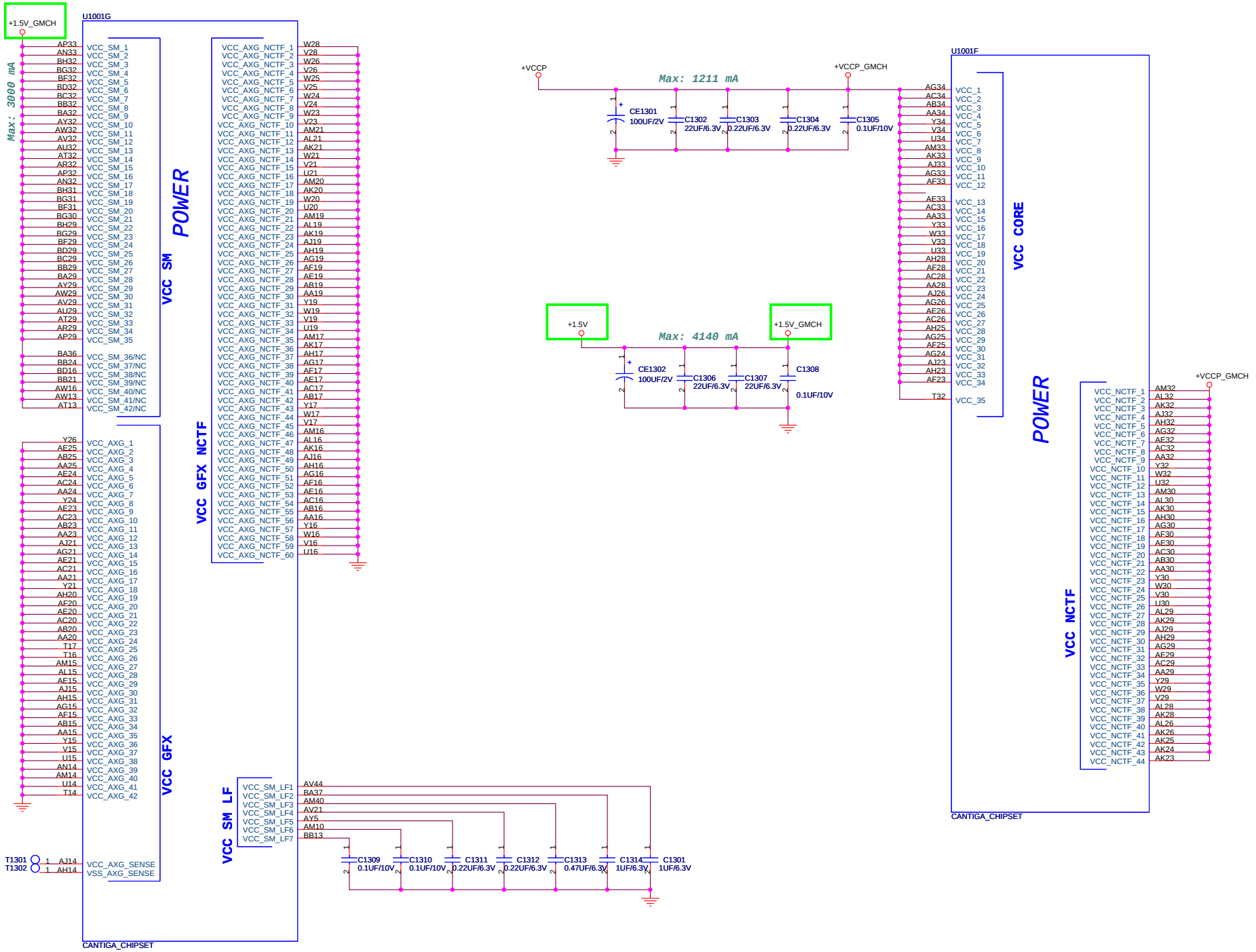
PEGATRON
Title : Cantiga--DDR2 bus (3)
PEGATRON COMPUTER INC
Engineer: Zack Kuo
Size Custom
Project Name F83Vf
Rev 1.1
P/N <OrgAddr2>
Date: Thursday, July 16, 2009
Sheet 12 of 100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Max: 3000 mA
U1001G
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VCC_SM_2
VCC_SM_3
VCC_SM_4
VCC_SM_5
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VCC_SM_7
VCC_SM_8
VCC_SM_9
VCC_SM_10
VCC_SM_11
VCC_SM_12
VCC_SM_13
VCC_SM_14
VCC_SM_15
VCC_SM_16
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VCC_SM_26
VCC_SM_27
VCC_SM_28
VCC_SM_29
VCC_SM_30
VCC_SM_31
VCC_SM_32
VCC_SM_33
VCC_SM_34
VCC_SM_35
VCC_SM_36/NC
VCC_SM_37/NC
VCC_SM_38/NC
VCC_SM_39/NC
VCC_SM_40/NC
VCC_SM_41/NC
VCC_SM_42/NC
VCC SM
POWER
VCC_AXG_1
VCC_AXG_2
VCC_AXG_3
VCC_AXG_4
VCC_AXG_5
VCC_AXG_6
VCC_AXG_7
VCC_AXG_8
VCC_AXG_9
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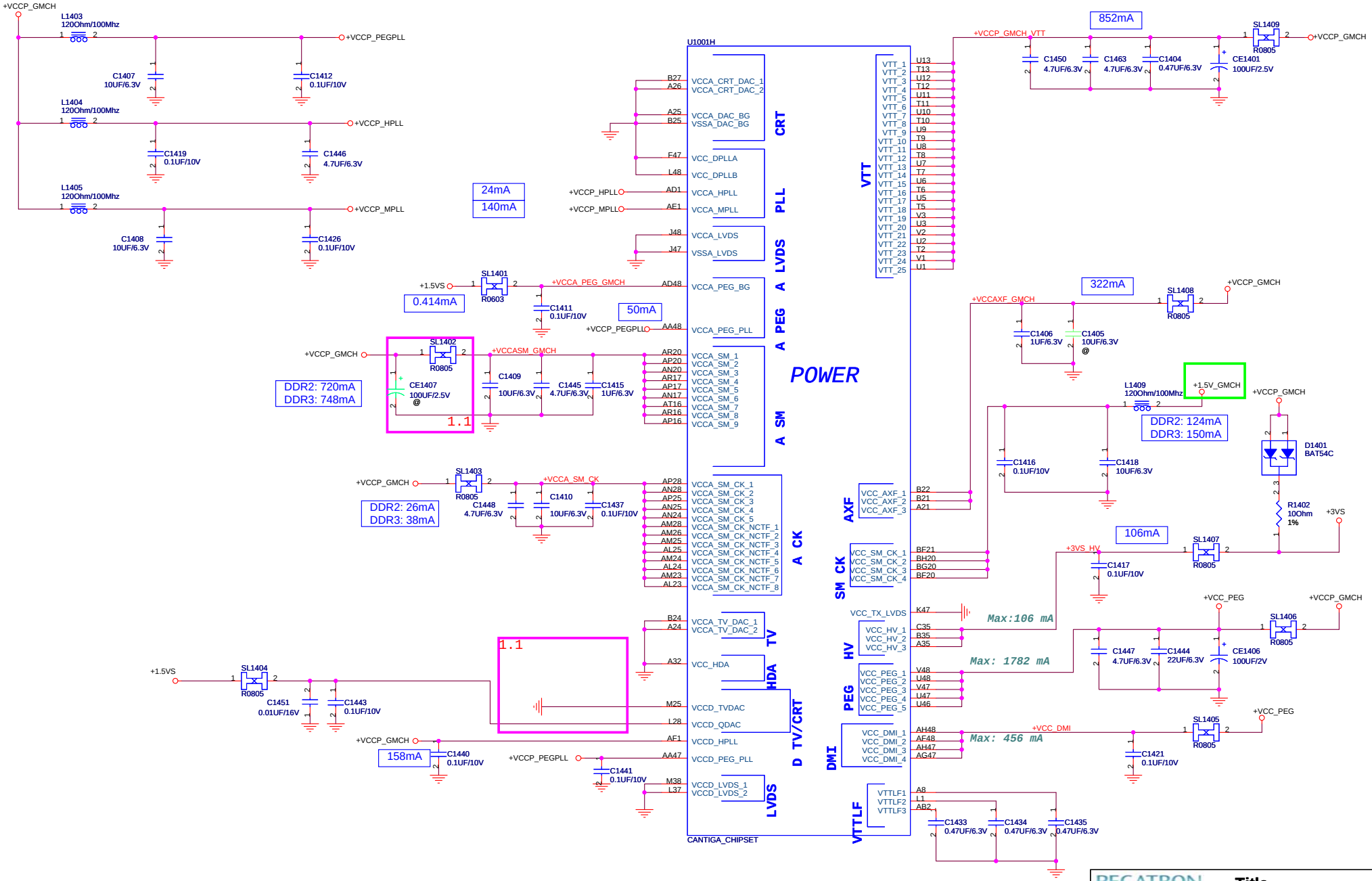
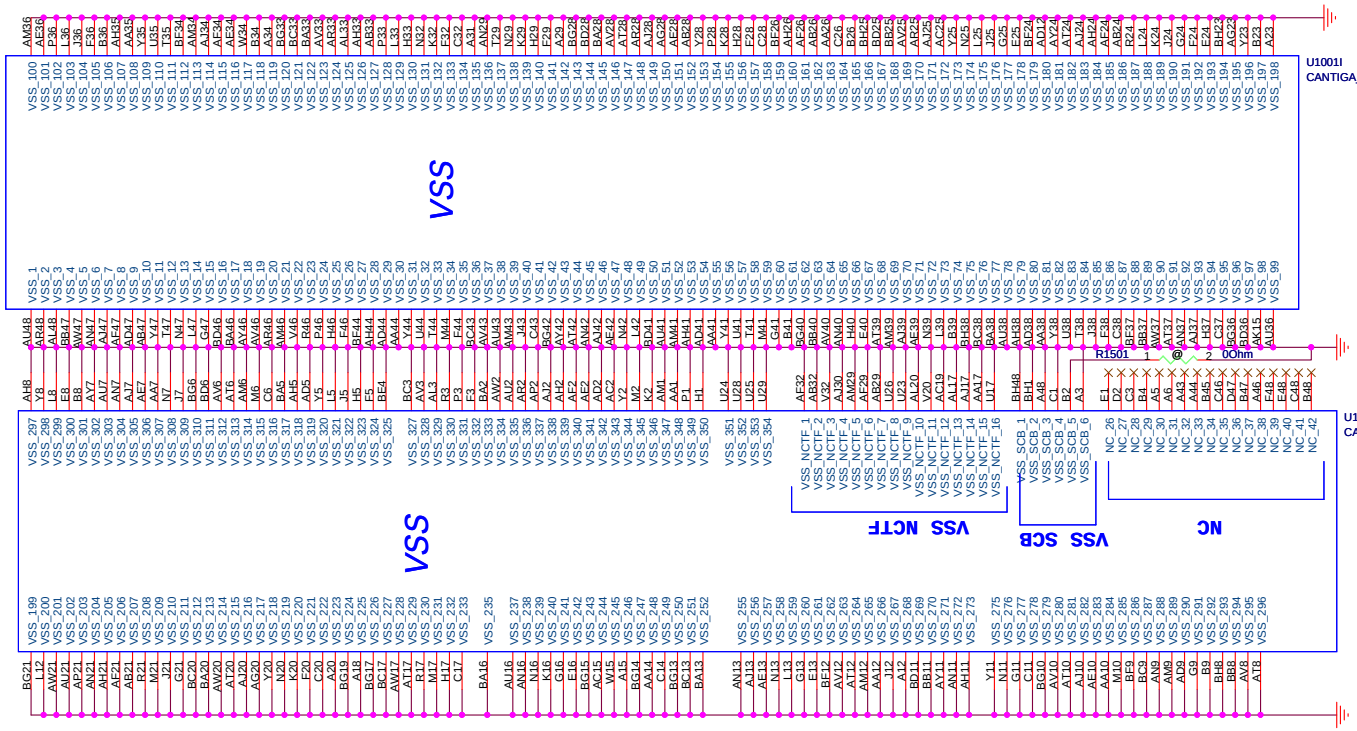
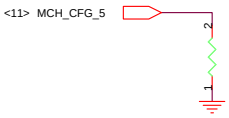
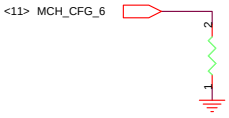
T1301
T1302
VCC_AXG_SENSE
VSS_AXG_SENSE
VCC_AXG_NCTF_1
VCC_AXG_NCTF_2
VCC_AXG_NCTF_3
VCC_AXG_NCTF_4
VCC_AXG_NCTF_5
VCC_AXG_NCTF_6
VCC_AXG_NCTF_7
VCC_AXG_NCTF_8
VCC_AXG_NCTF_9
VCC_AXG_NCTF_10
VCC_AXG_NCTF_11
VCC_AXG_NCTF_12
VCC_AXG_NCTF_13
VCC_AXG_NCTF_14
VCC_AXG_NCTF_15
VCC_AXG_NCTF_16
VCC_AXG_NCTF_17
VCC_AXG_NCTF_18
VCC_AXG_NCTF_19
VCC_AXG_NCTF_20
VCC_AXG_NCTF_21
VCC_AXG_NCTF_22
VCC_AXG_NCTF_23
VCC_AXG_NCTF_24
VCC_AXG_NCTF_25
VCC_AXG_NCTF_26
VCC_AXG_NCTF_27
VCC_AXG_NCTF_28
VCC_AXG_NCTF_29
VCC_AXG_NCTF_30
VCC_AXG_NCTF_31
VCC_AXG_NCTF_32
VCC_AXG_NCTF_33
VCC_AXG_NCTF_34
VCC_AXG_NCTF_35
VCC_AXG_NCTF_36
VCC_AXG_NCTF_37
VCC_AXG_NCTF_38
VCC_AXG_NCTF_39
VCC_AXG_NCTF_40
VCC_AXG_NCTF_41
VCC_AXG_NCTF_42
VCC_AXG_NCTF_43
VCC_AXG_NCTF_44
VCC_AXG_NCTF_45
VCC_AXG_NCTF_46
VCC_AXG_NCTF_47
VCC_AXG_NCTF_48
VCC_AXG_NCTF_49
VCC_AXG_NCTF_50
VCC_AXG_NCTF_51
VCC_AXG_NCTF_52
VCC_AXG_NCTF_53
VCC_AXG_NCTF_54
VCC_AXG_NCTF_55
VCC_AXG_NCTF_56
VCC_AXG_NCTF_57
VCC_AXG_NCTF_58
VCC_AXG_NCTF_59
VCC_AXG_NCTF_60
VCC GFX NCTF
VCC_SM_LF1
VCC_SM_LF2
VCC_SM_LF3
VCC_SM_LF4
VCC_SM_LF5
VCC_SM_LF6
VCC_SM_LF7
VCC SM LF
C1309 0.1UF/10V
C1310 0.1UF/10V
C1311 0.22UF/6.3V
C1312 0.22UF/6.3V
C1313 0.47UF/6.3V
C1314 1UF/6.3V
C1301 1UF/6.3V
CANTIGA_CHIPSET
+VCCP
Max: 1211 mA
+VCCP_GMCH
CE1301 100UF/2V
C1302 22UF/6.3V
C1303 0.22UF/6.3V
C1304 0.22UF/6.3V
C1305 0.1UF/10V
U1001F
VCC_1
VCC_2
VCC_3
VCC_4
VCC_5
VCC_6
VCC_7
VCC_8
VCC_9
VCC_10
VCC_11
VCC_12
VCC_13
VCC_14
VCC_15
VCC_16
VCC_17
VCC_18
VCC_19
VCC_20
VCC_21
VCC_22
VCC_23
VCC_24
VCC_25
VCC_26
VCC_27
VCC_28
VCC_29
VCC_30
VCC_31
VCC_32
VCC_33
VCC_34
VCC_35
VCC CORE
POWER
+1.5V
Max: 4140 mA
+1.5V_GMCH
CE1302 100UF/2V
C1306 22UF/6.3V
C1307 22UF/6.3V
C1308 0.1UF/10V
VCC_NCTF_1
VCC_NCTF_2
VCC_NCTF_3
VCC_NCTF_4
VCC_NCTF_5
VCC_NCTF_6
VCC_NCTF_7
VCC_NCTF_8
VCC_NCTF_9
VCC_NCTF_10
VCC_NCTF_11
VCC_NCTF_12
VCC_NCTF_13
VCC_NCTF_14
VCC_NCTF_15
VCC_NCTF_16
VCC_NCTF_17
VCC_NCTF_18
VCC_NCTF_19
VCC_NCTF_20
VCC_NCTF_21
VCC_NCTF_22
VCC_NCTF_23
VCC_NCTF_24
VCC_NCTF_25
VCC_NCTF_26
VCC_NCTF_27
VCC_NCTF_28
VCC_NCTF_29
VCC_NCTF_30
VCC_NCTF_31
VCC_NCTF_32
VCC_NCTF_33
VCC_NCTF_34
VCC_NCTF_35
VCC_NCTF_36
VCC_NCTF_37
VCC_NCTF_38
VCC_NCTF_39
VCC_NCTF_40
VCC_NCTF_41
VCC_NCTF_42
VCC_NCTF_43
VCC_NCTF_44
VCC NCTF
+VCCP_GMCH
CANTIGA_CHIPSET
PEGATRON
Title : Cantiga--POWER (4)
PEGATRON COMPUTER INC
Engineer: Zack Kuo
Size
Custom
Project Name
F83Vf
Rev
1.1
P/N
<OrgAddr2>
Date: Thursday, July 16, 2009
Sheet 13 of 100


+VCCP_GMCH
L1403 120Ohm/100Mhz
+VCCP_PEGPLL
C1407 10UF/6.3V
C1412 0.1UF/10V
L1404 120Ohm/100Mhz
+VCCP_HPLL
C1419 0.1UF/10V
C1446 4.7UF/6.3V
L1405 120Ohm/100Mhz
+VCCP_MPLL
C1408 10UF/6.3V
C1426 0.1UF/10V
U1001H
VCCA_CRT_DAC_1
VCCA_CRT_DAC_2
VCCA_DAC_BG
VSSA_DAC_BG
CRT
24mA
140mA
VCC_DPLLA
VCC_DPLLB
VCCA_HPLL
VCCA_MPLL
PLL
VCCA_LVDS
VSSA_LVDS
LVDS
+1.5VS
SL1401 R0603
+VCCA_PEG_GMCH
0.414mA
C1411 0.1UF/10V
50mA
VCCA_PEG_BG
VCCA_PEG_PLL
A PEG
+VCCP_GMCH
SL1402 R0805
+VCCASM_GMCH
DDR2: 720mA
DDR3: 748mA
CE1407 100UF/2.5V @
C1409 10UF/6.3V
C1445 4.7UF/6.3V
C1415 1UF/6.3V
1.1
VCCA_SM_1
VCCA_SM_2
VCCA_SM_3
VCCA_SM_4
VCCA_SM_5
VCCA_SM_6
VCCA_SM_7
VCCA_SM_8
VCCA_SM_9
A SM
POWER
SL1403 R0805
+VCCA_SM_CK
DDR2: 26mA
DDR3: 38mA
C1448 4.7UF/6.3V
C1410 10UF/6.3V
C1437 0.1UF/10V
VCCA_SM_CK_1
VCCA_SM_CK_2
VCCA_SM_CK_3
VCCA_SM_CK_4
VCCA_SM_CK_5
VCCA_SM_CK_NCTF_1
VCCA_SM_CK_NCTF_2
VCCA_SM_CK_NCTF_3
VCCA_SM_CK_NCTF_4
VCCA_SM_CK_NCTF_5
VCCA_SM_CK_NCTF_6
VCCA_SM_CK_NCTF_7
VCCA_SM_CK_NCTF_8
A CK
VCCA_TV_DAC_1
VCCA_TV_DAC_2
TV
VCC_HDA
HDA
1.1
+1.5VS
SL1404 R0805
C1451 0.01UF/16V
C1443 0.1UF/10V
VCCD_TVDAC
VCCD_QDAC
VCCD_HPLL
VCCD_PEG_PLL
D TV/CRT
+VCCP_GMCH
158mA
C1440 0.1UF/10V
+VCCP_PEGPLL
C1441 0.1UF/10V
VCCD_LVDS_1
VCCD_LVDS_2
LVDS
CANTIGA_CHIPSET
VTT_1
VTT_2
VTT_3
VTT_4
VTT_5
VTT_6
VTT_7
VTT_8
VTT_9
VTT_10
VTT_11
VTT_12
VTT_13
VTT_14
VTT_15
VTT_16
VTT_17
VTT_18
VTT_19
VTT_20
VTT_21
VTT_22
VTT_23
VTT_24
VTT_25
VTT
+VCCP_GMCH_VTT
852mA
C1450 4.7UF/6.3V
C1463 4.7UF/6.3V
C1404 0.47UF/6.3V
CE1401 100UF/2.5V
SL1409 R0805
+VCCP_GMCH
+VCCAXF_GMCH
322mA
C1406 1UF/6.3V
C1405 10UF/6.3V @
SL1408 R0805
+VCCP_GMCH
L1409 120Ohm/100Mhz
+1.5V_GMCH
+VCCP_GMCH
DDR2: 124mA
DDR3: 150mA
C1416 0.1UF/10V
C1418 10UF/6.3V
D1401 BAT54C
R1402 10Ohm 1%
+3VS
VCC_AXF_1
VCC_AXF_2
VCC_AXF_3
AXF
106mA
+3VS_HV
C1417 0.1UF/10V
SL1407 R0805
VCC_SM_CK_1
VCC_SM_CK_2
VCC_SM_CK_3
VCC_SM_CK_4
SM CK
VCC_TX_LVDS
Max:106 mA
VCC_HV_1
VCC_HV_2
VCC_HV_3
HV
Max: 1782 mA
+VCC_PEG
+VCCP_GMCH
SL1406 R0805
C1447 4.7UF/6.3V
C1444 22UF/6.3V
CE1406 100UF/2V
VCC_PEG_1
VCC_PEG_2
VCC_PEG_3
VCC_PEG_4
VCC_PEG_5
PEG
VCC_DMI_1
VCC_DMI_2
VCC_DMI_3
VCC_DMI_4
DMI
Max: 456 mA
+VCC_DMI
SL1405 R0805
+VCC_PEG
C1421 0.1UF/10V
VTTLF1
VTTLF2
VTTLF3
VTTLF
C1433 0.47UF/6.3V
C1434 0.47UF/6.3V
C1435 0.47UF/6.3V
PEGATRON
Title : Cantiga-POWER(5)
PEGATRON COMPUTER INC
Engineer: Zack Kuo
Size: Custom
Project Name: F83Vf
Rev: 1.1
P/N: <OrgAddr2>
Date: Thursday, July 16, 2009
Sheet 14 of 100

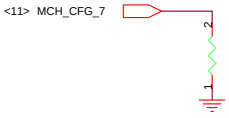




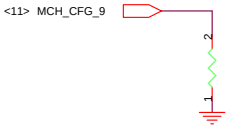
CFG5 : DMI STRAP
HIGH = DMI X 4 (Default)
LOW = DMI X 2



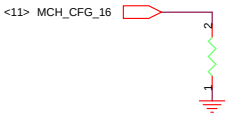
CFG6 : Integrated TPM Host Interface
HIGH = iTPM disable (Default)
LOW = iTPM enable



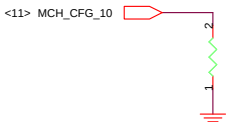
CFG7 : Intel ME Crypto Strap Transport Layer Security cipher suite
HIGH = With confidentiality (Default)
LOW = Without confidentiality



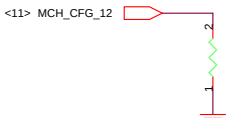
CFG9 : PCIE GRAPHIC LANE
HIGH = Normal Operation (Default)
LOW = Reverse Lanes



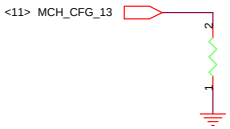
CFG16 : FSB Dynamic ODT
HIGH = Ensable (Default)
LOW = Disable

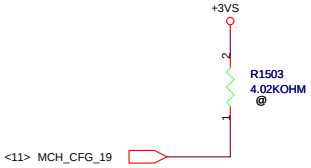


CFG10 : PCIe Loopback
HIGH = Disable (Default)
LOW = Enable

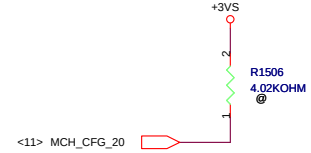


CFG [13:12] : XOR/ALL-Z
00 = Reserved
01= XOR Mode Enabled
10= All-Z Mode Enabled
11= Normal Operation (Default)





CFG19 : DMI Lane Reversal
LOW = NORMAL (default)
HIGH = Reverse Lanes



CFG20 : SDVO/PCIE CONCURRENT MODE
LOW = ONLY SDVO or PCIE is Operational (Default)
HIGH = SDVO and PCIE are operating simultaneously via the PEG port

PEGATRON	Title : Cantiga-GND		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: Custom	Project Name: F83Vf	P/N: <OrgAddr2>	Rev: 1.1
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PEGATRON	Title :		
PEGATRON COMPUTER INC	Engineer:	Zack Kuo	
Size: Custom	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 16 of 100		

Main Board

PEGATRON

Title :

PEGATRON COMPUTER INC

Engineer: Zack Kuo

Size	Project Name	Rev
Custom	F83Vf	1.1
	P/N <OrgAddr2>	

Date: Thursday, July 16, 2009 Sheet 17 of 100

Main Board

PEGATRON

Title :

PEGATRON COMPUTER INC

Engineer: Zack Kuo

Size	Project Name	Rev
Custom	F83Vf	1.1
	P/N <OrgAddr2>	

Date: Thursday, July 16, 2009 Sheet 18 of 100

PEGATRON

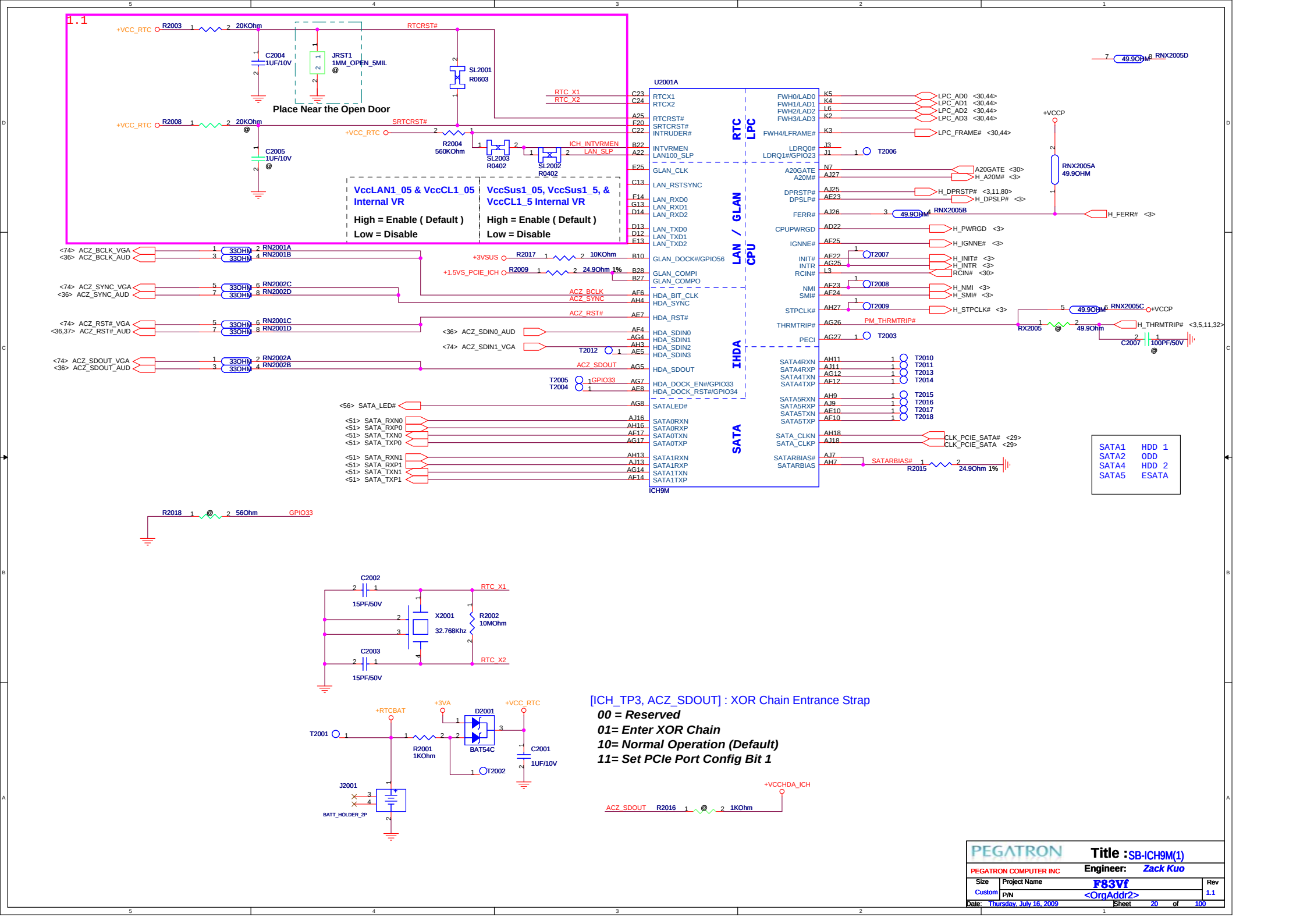
Title :

PEGATRON COMPUTER INC

Engineer: Zack Kuo

Size	Project Name	Rev
C	F83Vf	1.1
	P/N <OrgAddr2>	

Date: Thursday, July 16, 2009 Sheet 19 of 100


1.1
Place Near the Open Door
VccLAN1_05 & VccCL1_05 Internal VR
High = Enable (Default)
Low = Disable
VccSus1_05, VccSus1_5, & VccCL1_5 Internal VR
High = Enable (Default)
Low = Disable
U2001A
ICH9M
RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
SATA1 HDD 1
SATA2 ODD
SATA4 HDD 2
SATA5 ESATA
[ICH_TP3, ACZ_SDOUT] : XOR Chain Entrance Strap
00 = Reserved
01= Enter XOR Chain
10= Normal Operation (Default)
11= Set PCIe Port Config Bit 1
PEGATRON
PEGATRON COMPUTER INC
Title : SB-ICH9M(1)
Engineer: Zack Kuo
Size Custom
Project Name F83Vf
P/N <OrgAddr2>
Rev 1.1
Date: Thursday, July 16, 2009
Sheet 20 of 100

PCIE1	NC
PCIE2	MiniCard
PCIE3	NewCard
PCIE4	NC
PCIE5	NC
PCIE6	LAN

U2001B

PCI

Interrupt I/F

ICH9M

U2001D

PCI-Express

Direct Media Interface

SPI

USB

ICH9M

SPI_MOSI
iTPM Enable

High = Enable

Low = Disable(Default)

Place within 500 mils of ICH

Place within 500 mils of ICH

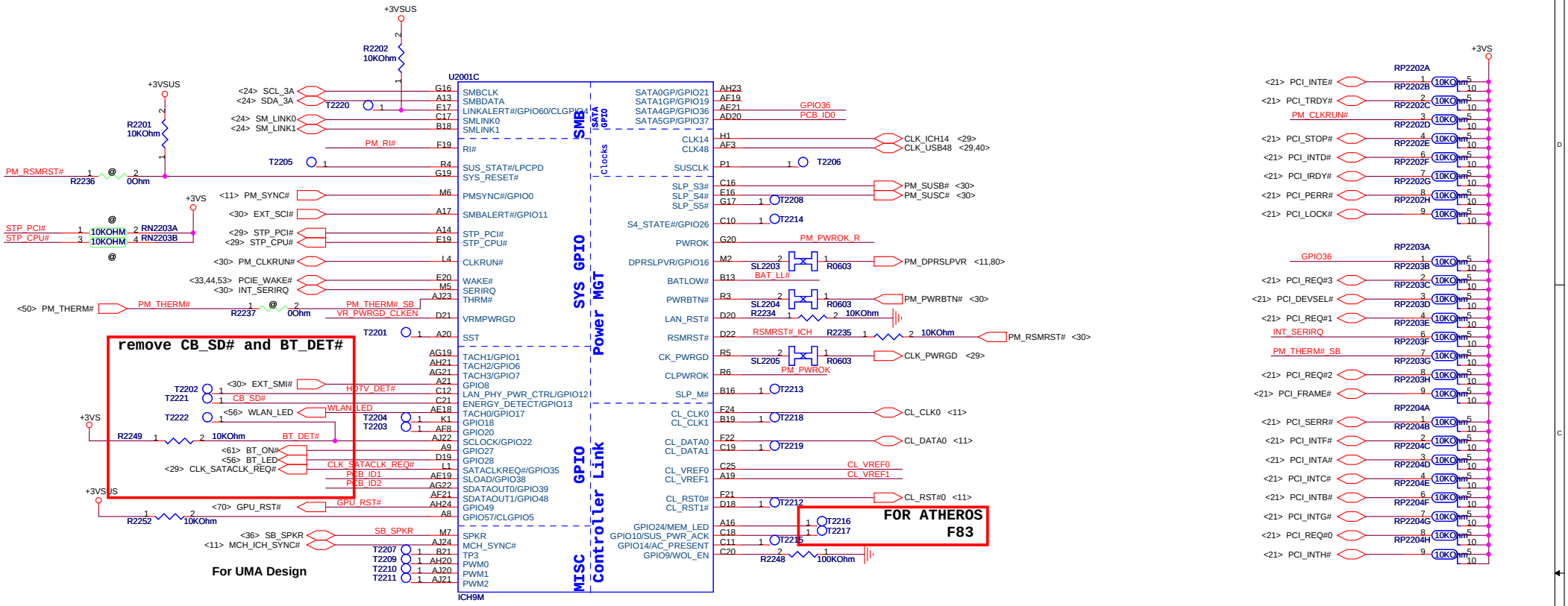
USB0	External Port 1
USB1	External Port 2
USB2	WLAN
USB3	External Port 3
USB4	CMOS Camera
USB5	BT
USB6	NEWCARD
USB7	CardReader
USB8	FREE
USB9	FREE
USB10	FREE
USB11	FingerPrinter

ICH9 Boot BIOS select

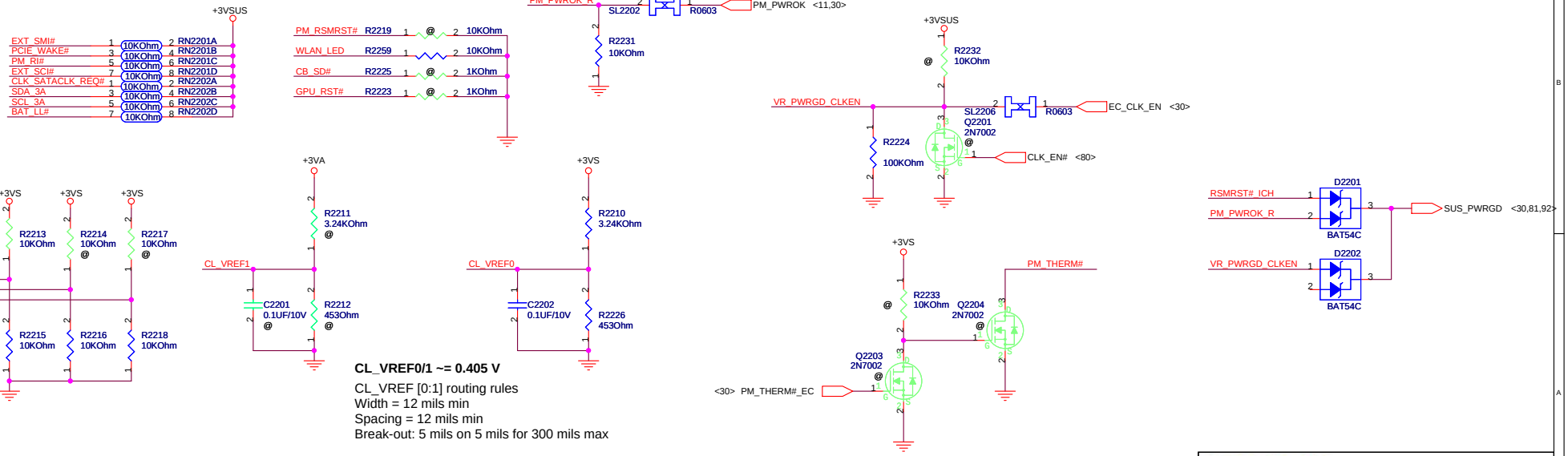
		GNT#0	CS#1
LPC	11	1	1
PCI	10	1	0
SPI	01	0	1

(default)

PEGATRON COMPUTER INC	Title : SB-ICH9M(2)
	Engineer: Zack Kuo
Size: Custom	Project Name: F83Vf
	P/N: <OrgAddr2>
	Rev: 1.1
Date: Thursday, July 16, 2009	Sheet 21 of 100



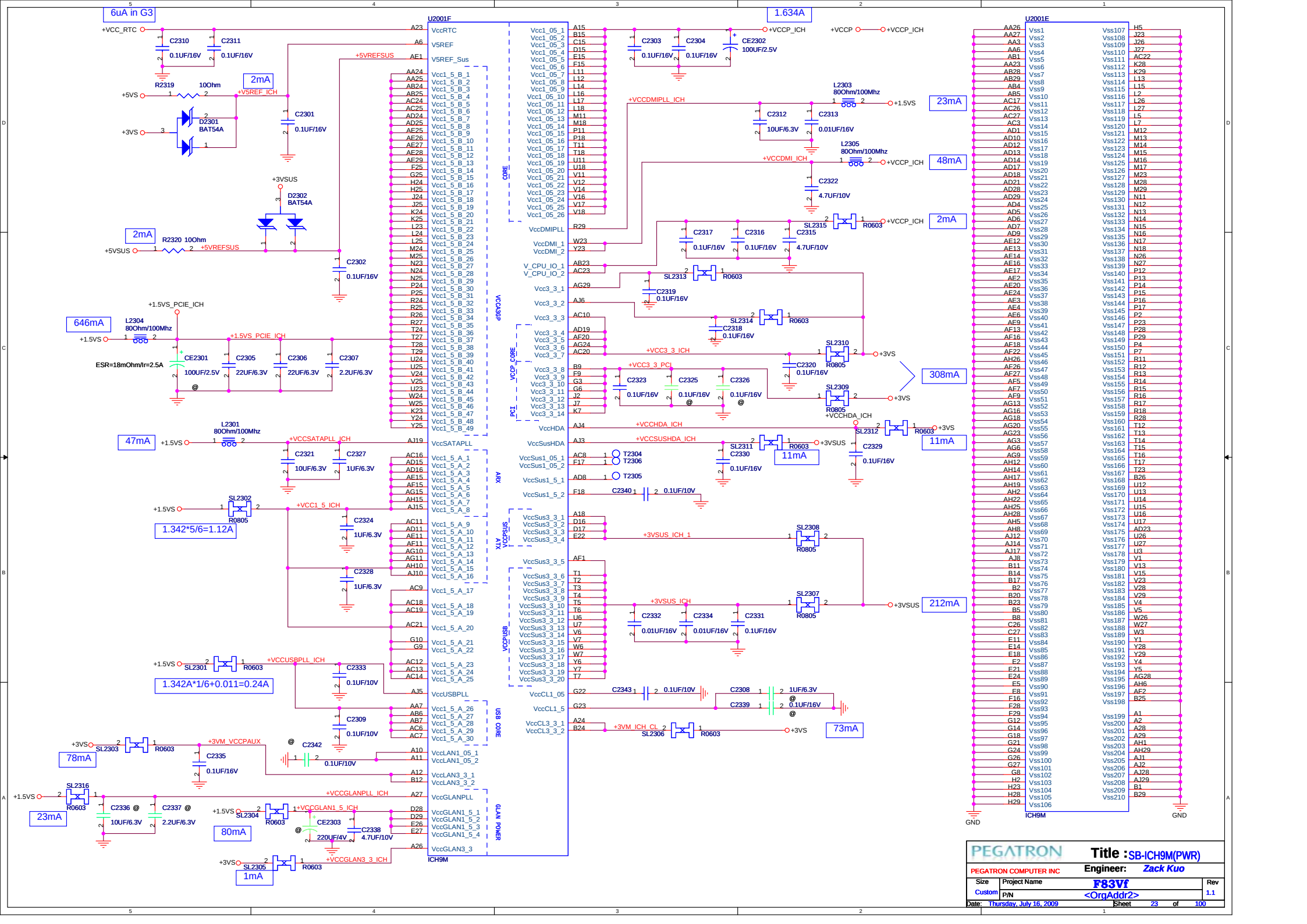
Mount/unmount as same R2236



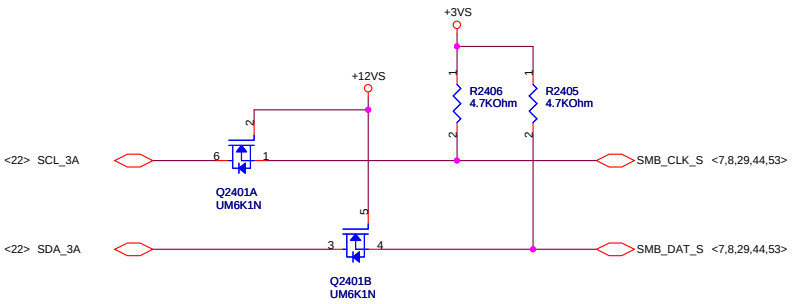
CL_VREF0/1 ~= 0.405 V

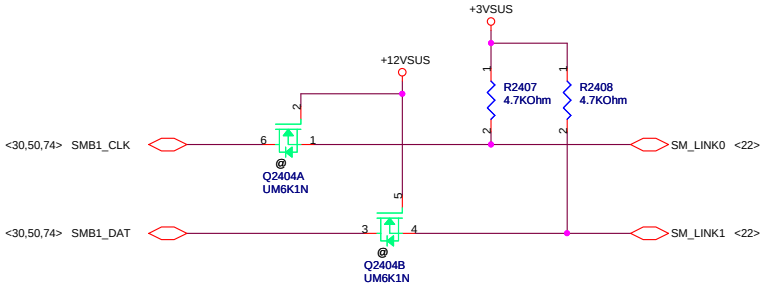
CL_VREF [0:1] routing rules
Width = 12 mils min
Spacing = 12 mils min
Break-out: 5 mils on 5 mils for 300 mils max

PEGATRON	Title : SB-ICH9M(3)		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: Custom	Project Name: F83Vf	P/N: <OrgAddr2>	Rev: 1.1
Date: Thursday, July 16, 2009	Sheet 22 of 100		


6uA in G3
1.634A
U2001F
U2001E
ICH9M
+VCC_RTC
C2310 0.1UF/16V
C2311 0.1UF/16V
R2319 10Ohm
+5VS
+3VS
D2301 BAT54A
2mA
+5VREFSUS
+V5REF_ICH
C2301 0.1UF/16V
+3VSUS
D2302 BAT54A
R2320 10Ohm
C2302 0.1UF/16V
+1.5VS_PCIE_ICH
646mA
L2304 80Ohm/100Mhz
CE2301 100UF/2.5V
ESR=18mOhm/Ir=2.5A
C2305 22UF/6.3V
C2306 22UF/6.3V
C2307 2.2UF/6.3V
47mA
L2301 80Ohm/100Mhz
+VCCSATAPLL_ICH
C2321 10UF/6.3V
C2327 1UF/6.3V
SL2302 R0805
+VCC1_5_ICH
1.342*5/6=1.12A
C2324 1UF/6.3V
C2328 1UF/6.3V
SL2301 R0603
+VCCUSBPLL_ICH
1.342A*1/6+0.011=0.24A
C2333 0.1UF/10V
C2309 0.1UF/10V
SL2303 R0603
+3VM_VCCPAUX
78mA
C2335 0.1UF/16V
C2342 0.1UF/10V
SL2316 R0603
23mA
C2336 10UF/6.3V
C2337 2.2UF/6.3V
SL2304 R0603
+VCCGLAN1_5_ICH
80mA
CE2303 220UF/4V
C2338 4.7UF/10V
SL2305 R0603
+VCCGLAN3_3_ICH
1mA
C2303 0.1UF/16V
C2304 0.1UF/16V
CE2302 100UF/2.5V
+VCCP
+VCCP_ICH
+VCCDMIPLL_ICH
L2303 80Ohm/100Mhz
+1.5VS
23mA
C2312 10UF/6.3V
C2313 0.01UF/16V
+VCCDMI_ICH
L2305 80Ohm/100Mhz
48mA
C2322 4.7UF/10V
C2317 0.1UF/16V
C2316 0.1UF/16V
C2315 4.7UF/10V
SL2315 R0603
2mA
SL2313 R0603
C2319 0.1UF/16V
SL2314 R0603
C2318 0.1UF/16V
+VCC3_3_ICH
SL2310 R0805
+3VS
308mA
C2320 0.1UF/16V
+VCC3_3_PCI
C2323 0.1UF/16V
C2325 0.1UF/16V
C2326 0.1UF/16V
SL2309 R0805
+VCCHDA_ICH
SL2312 R0603
C2329 0.1UF/16V
+VCCSUSHDA_ICH
SL2311 R0603
C2330 0.1UF/16V
+3VSUS
11mA
T2304
T2306
T2305
C2340 0.1UF/10V
+3VSUS_ICH_1
SL2308 R0805
+3VSUS_ICH
SL2307 R0805
212mA
C2332 0.01UF/16V
C2334 0.01UF/16V
C2331 0.1UF/16V
C2343 0.1UF/10V
C2308 1UF/6.3V
C2339 0.1UF/16V
+3VM_ICH_CL
SL2306 R0603
73mA
GND
CORE
VCCA3P
VCCP_CORE
PCI
AUX
VCCPSUS
VCCPUSB
USB CORE
GLAN POWER
Title : SB-ICH9M(PWR)
PEGATRON COMPUTER INC
Engineer: Zack Kuo
Size Custom
Project Name F83Vf
P/N <OrgAddr2>
Rev 1.1
Date: Thursday, July 16, 2009
Sheet 23 of 100

ICH9-M





PEGATRON

PEGATRON COMPUTER INC

Title : ICH9M-Other

Engineer: Zack Kuo

Size	Project Name	Rev
Custom	F83Vf	1.1
	P/N <OrgAddr2>	

Date: Thursday, July 16, 2009 Sheet 24 of 100

Main Board

PEGATRON

Title : SB_****

PEGATRON COMPUTER INC

Engineer: Zack Kuo

Size	Project Name	Rev
Custom	F83Vf	1.1
	P/N <OrgAddr2>	

Date: Thursday, July 16, 2009 Sheet 25 of 100

Main Board

PEGATRON

Title : SB_****

PEGATRON COMPUTER INC

Engineer: Zack Kuo

Size	Project Name	Rev
Custom	F83Vf	1.1
	P/N <OrgAddr2>	

Date: Thursday, July 16, 2009 Sheet 26 of 100

Main Board

PEGATRON

Title : SB_****

PEGATRON COMPUTER INC

Engineer: Zack Kuo

Size	Project Name	Rev
Custom	F83Vf	1.1
	P/N <OrgAddr2>	

Date: Thursday, July 16, 2009 Sheet 27 of 100

Main Board

PEGATRON

Title : SB_****

PEGATRON COMPUTER INC

Engineer: Zack Kuo

Size	Project Name	Rev
Custom	F83Vf	1.1
	P/N <OrgAddr2>	

Date: Thursday, July 16, 2009 Sheet 28 of 100

Main Board

U2901 — ICS9LPR362AGLF-T
0610-000C000

	R2903	R2904	R2925
363:VREF	1K	330	@
364:TURBO	@	10K	0
364:NO TURBO	@	@	@

Latched Input Select

0 : Pin 17/18 = LCD_SSCG
1 : Pin 17/18 = PCIe_L0
33PCI3 R2907 10KOhm

0 : Pin 43/44 = SRC CLK
1 : Pin 43/44 = CPU_ITP CLK
33PCIF4 R2908 10KOhm

0 : Pin 14/15 = PCIe_L9
Pin 17/18 = 27FIX/27SS
1 : Pin 14/15 = DOT_96MHz
Pin 17/18 = LCD_SSCG/PCIe_L0
33PCIF5 R2910 10KOhm

0 : Pin 40/41 = PCIe_L7
1 : Pin 40/41 = PEREQ#
33PCI0 R2928 10KOhm / R2911 @ 10KOhm

PEREQ1#: PEREQ1# R2922 10KOhm

PEREQ2#: PEREQ2# R2923 @ 10KOhm

PEREQ3# : PCIEX2/4
PEREQ4# : PCIEX3/5/7

For 364 Over-clocking

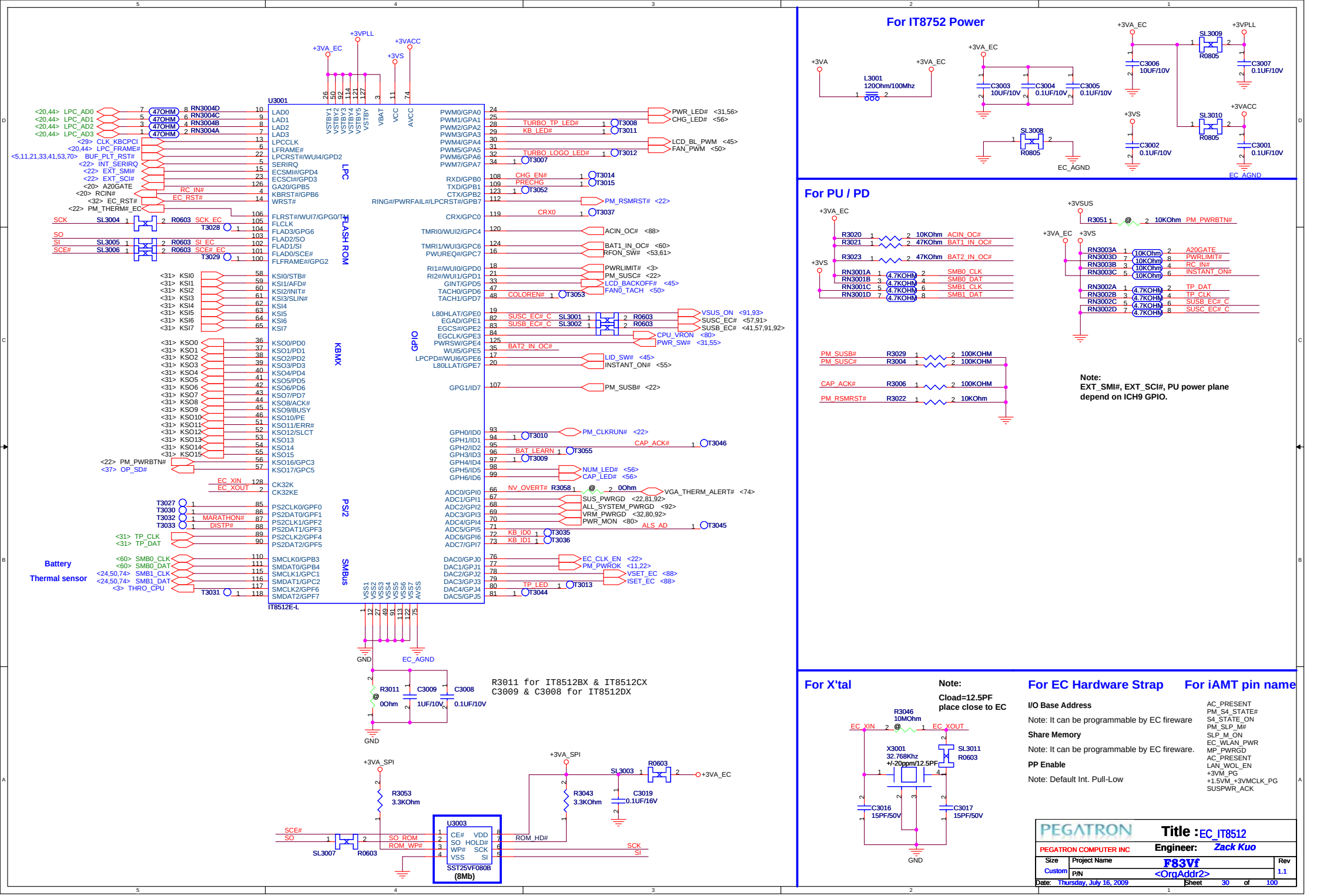
33PCI1 R2932 10KOhm / R2929 @ 10KOhm
REF0 R2931 10KOhm / R2930 @ 10KOhm

Reserved for R1.0 Debug

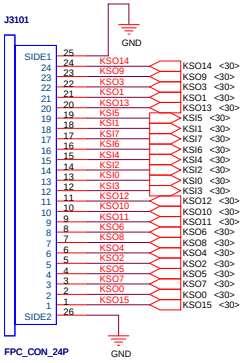
BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	0	1	1
200	800	0	1	0
266	1067	0	0	0

F83

PEGATRON COMPUTER INC
Title : CLK_ICS9LPR363
Engineer: Zack Kuo
Size: Custom | Project Name: F83Vf | Rev: 1.1
P/N: <OrgAddr2>
Date: Thursday, July 16, 2009 | Sheet 29 of 100


U3001
IT8512E-L
LPC
FLASH ROM
KBMX
GPIO
PS/2
SMBus
LAD0
LAD1
LAD2
LAD3
LPCCLK
LFRAME#
LPCRST#/WUI4/GPD2
SERIRQ
ECSMI#/GPD4
ECSCI#/GPD3
GA20/GPB5
KBRST#/GPB6
WRST#
FLRST#/WUI7/GPG0/TP
FLCLK
FLAD3/GPG6
FLAD2/SO
FLAD1/SI
FLAD0/SCE#
FLFRAME#/GPG2
KSI0/STB#
KSI1/AFD#
KSI2/INIT#
KSI3/SLIN#
KSI4
KSI5
KSI6
KSI7
KSO0/PD0
KSO1/PD1
KSO2/PD2
KSO3/PD3
KSO4/PD4
KSO5/PD5
KSO6/PD6
KSO7/PD7
KSO8/ACK#
KSO9/BUSY
KSO10/PE
KSO11/ERR#
KSO12/SLCT
KSO13
KSO14
KSO15
KSO16/GPC3
KSO17/GPC5
CK32K
CK32KE
PS2CLK0/GPF0
PS2DAT0/GPF1
PS2CLK1/GPF2
PS2DAT1/GPF3
PS2CLK2/GPF4
PS2DAT2/GPF5
SMCLK0/GPB3
SMDAT0/GPB4
SMCLK1/GPC1
SMDAT1/GPC2
SMCLK2/GPF6
SMDAT2/GPF7
PWM0/GPA0
PWM1/GPA1
PWM2/GPA2
PWM3/GPA3
PWM4/GPA4
PWM5/GPA5
PWM6/GPA6
PWM7/GPA7
RXD/GPB0
TXD/GPB1
CTX/GPB2
RING#/PWRFAIL#/LPCRST#/GPB7
CRX/GPC0
TMRI0/WUI2/GPC4
TMRI1/WUI3/GPC6
PWUREQ#/GPC7
RI1#/WUI0/GPD0
RI2#/WUI1/GPD1
GINT/GPD5
TACH0/GPD6
TACH1/GPD7
L80HLAT/GPE0
EGAD/GPE1
EGCS#/GPE2
EGCLK/GPE3
PWRSW/GPE4
WUI5/GPE5
LPCPD#/WUI6/GPE6
L80LLAT/GPE7
GPG1/ID7
GPH0/ID0
GPH1/ID1
GPH2/ID2
GPH3/ID3
GPH4/ID4
GPH5/ID5
GPH6/ID6
ADC0/GPI0
ADC1/GPI1
ADC2/GPI2
ADC3/GPI3
ADC4/GPI4
ADC5/GPI5
ADC6/GPI6
ADC7/GPI7
DAC0/GPJ0
DAC1/GPJ1
DAC2/GPJ2
DAC3/GPJ3
DAC4/GPJ4
DAC5/GPJ5
VSTBY1
VSTBY2
VSTBY3
VSTBY4
VSTBY5
VSTBY
VBAT
VCC
AVCC
VSS1
VSS2
VSS3
VSS4
VSS5
VSS6
VSS7
AVSS
+3VPLL
+3VA_EC
+3VACC
+3VS
GND
EC_AGND
Battery
Thermal sensor
R3011 for IT8512BX & IT8512CX
C3009 & C3008 for IT8512DX
U3003
SST25VF080B
(8Mb)
+3VA_SPI
ROM_HD#
SCE#
SO
SCK
SI
SO_ROM
ROM_WP#
SL3007
R0603
R3053
3.3KOhm
R3043
3.3KOhm
SL3003
C3019
0.1UF/16V
For IT8752 Power
L3001
120Ohm/100Mhz
C3003
10UF/10V
C3004
0.1UF/10V
C3005
0.1UF/10V
SL3008
R0805
EC_AGND
SL3009
C3006
10UF/10V
C3007
0.1UF/10V
SL3010
C3002
0.1UF/10V
C3001
0.1UF/10V
For PU / PD
R3020
10KOhm
ACIN_OC#
R3021
47KOhm
BAT1_IN_OC#
R3023
47KOhm
BAT2_IN_OC#
RN3001A
RN3001B
RN3001C
RN3001D
4.7KOHM
SMB0_CLK
SMB0_DAT
SMB1_CLK
SMB1_DAT
R3051
10KOhm
PM_PWRBTN#
RN3003A
RN3003D
RN3003B
RN3003C
10KOhm
A20GATE
PWRLIMIT#
RC_IN#
INSTANT_ON#
RN3002A
RN3002B
RN3002C
RN3002D
TP_DAT
TP_CLK
SUSB_EC# C
SUSC_EC# C
PM_SUSB#
PM_SUSC#
R3029
R3004
100KOHM
CAP_ACK#
R3006
PM_RSMRST#
R3022
10KOhm
Note:
EXT_SMI#, EXT_SCI#, PU power plane
depend on ICH9 GPIO.
For X'tal
Note:
Cload=12.5PF
place close to EC
R3046
10MOhm
X3001
32.768Khz
+/-20ppm/12.5PF
SL3011
R0603
C3016
15PF/50V
C3017
15PF/50V
For EC Hardware Strap
I/O Base Address
Note: It can be programmable by EC fireware
Share Memory
Note: It can be programmable by EC fireware.
PP Enable
Note: Default Int. Pull-Low
For iAMT pin name
AC_PRESENT
PM_S4_STATE#
S4_STATE_ON
PM_SLP_M#
SLP_M_ON
EC_WLAN_PWR
MP_PWRGD
AC_PRESENT
LAN_WOL_EN
+3VM_PG
+1.5VM_+3VMCLK_PG
SUSPWR_ACK
PEGATRON
PEGATRON COMPUTER INC
Title : EC_IT8512
Engineer: Zack Kuo
Size
Custom
Project Name
F83Vf
Rev
1.1
P/N
<OrgAddr2>
Date: Thursday, July 16, 2009
Sheet 30 of 100

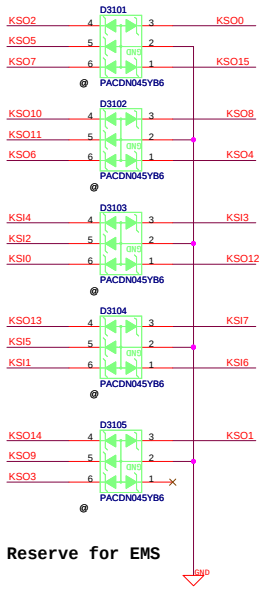
For Keyboard



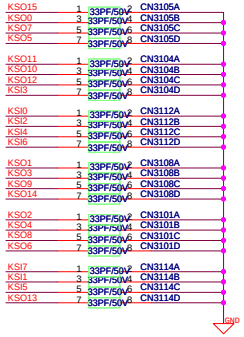
P/N:12G182002408

T53 KB MATRIX

Close to keyboard connect

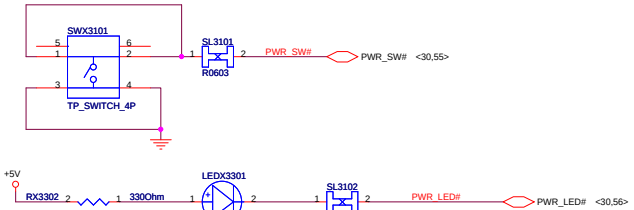


Reserve for EMS



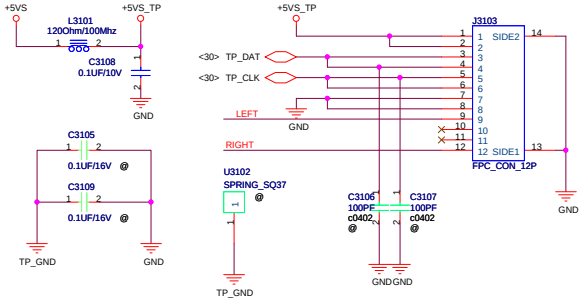
Reserve for EMI

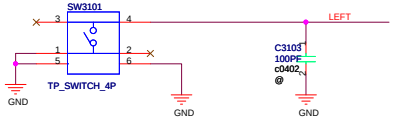
TEST



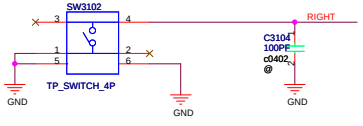
Touch-Pad

P/N:12G183301208



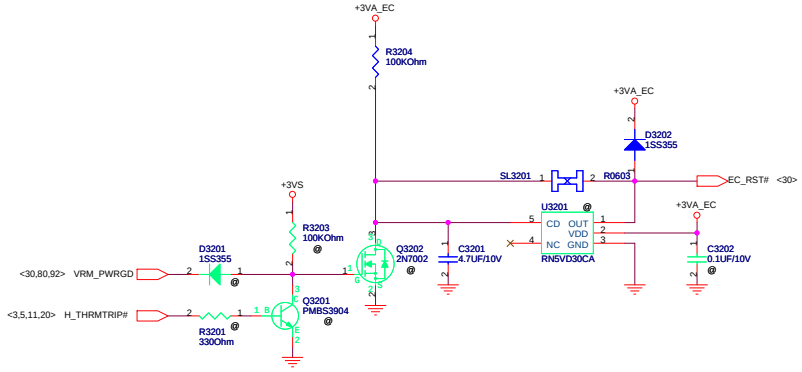


P/N:12G091031041



P/N:12G091031041

PEGATRON	Title :	EC_IT8512 (2/2)	
PEGATRON COMPUTER INC	Engineer:	Zack Kuo	
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 31 of 100		



PEGATRON	Title : EC_RESET		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 32 of 100		

+3VS +3VS <3,7,8,11,14,15,22,23,24,29,30,32,36,40,41,44,45,46,48,50,51,53,56,57,70,72,74,80,91,92>

+3VSUS +3VSUS <20,21,22,23,24,30,37,45,53,56,91,92>

GND <3,4,5,7,8,9,10,11,13,14,15,20,21,22,23,29,30,31,32,34,36,37,38,40,41,44,45,46,48,50,51,52,53,55,56,57,60,61,63,68,70,72,73,74,75,76,77,80,81,82,83,84,85,88,91,92>

LAN_GND <34>

LAN_GND

ground pad要打散熱孔

PCIE Tx,Rx方向是以南橋爲觀點
Chip pin Tx,Rx是以chip爲觀點

AR8121: Remove R3313
AR8131: Remove R3314

Close to U3301

For AR8131 : Remove R3309

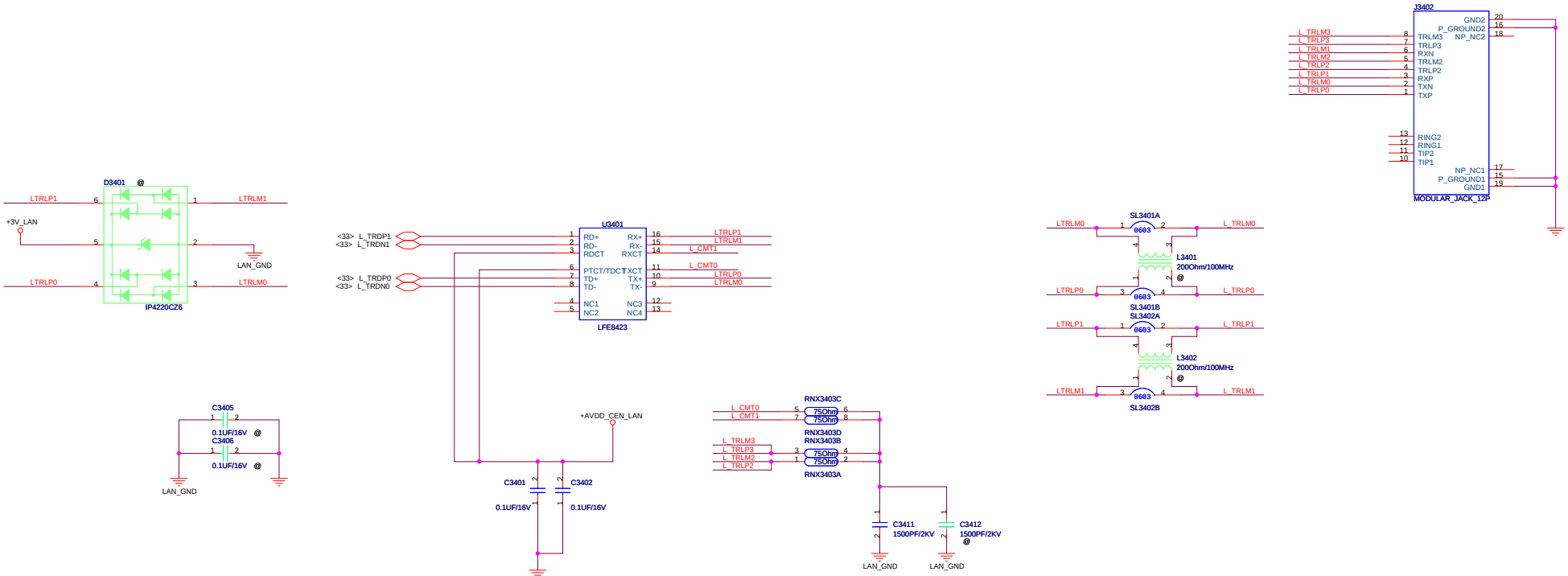
AR8121:Remove C3328
AR8131/25MHz: Remove C3328

With overclock:Remove SL3304, Add R3325
Not overclock:Add SL3304, Remove R3325

C3301 C3302 C3303 C3304 close to pin2

PEGATRON	Title : Atheros 8132		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 33 of 100		

LAN / MODEM PORT



PEGATRON	Title : RJ45		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 34 of 100		

PEGATRON

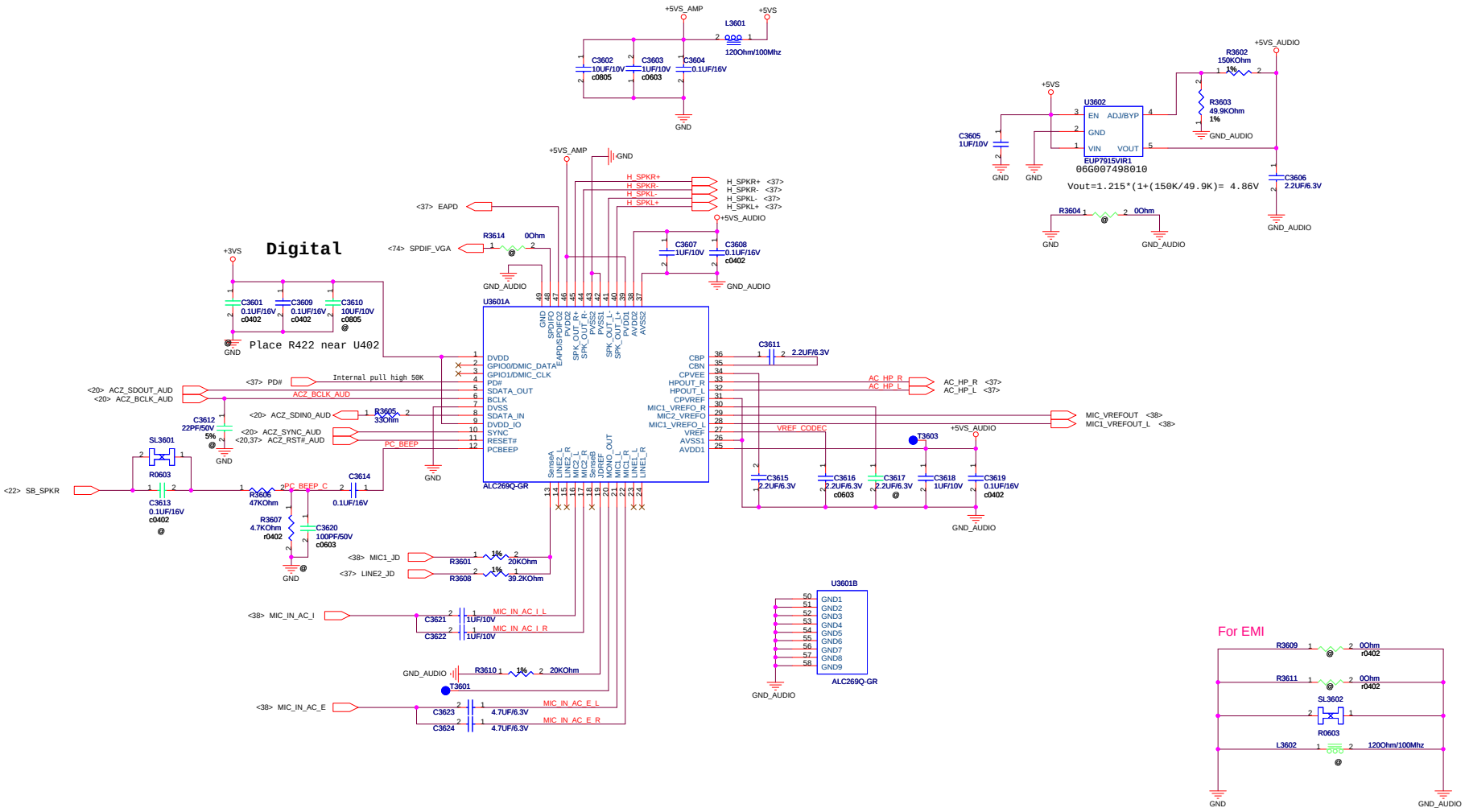
Title : <Title>

PEGATRON COMPUTER INC

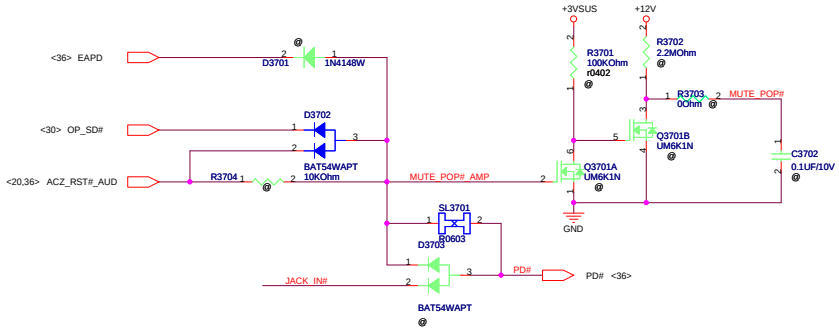
Engineer: Zack Kuo

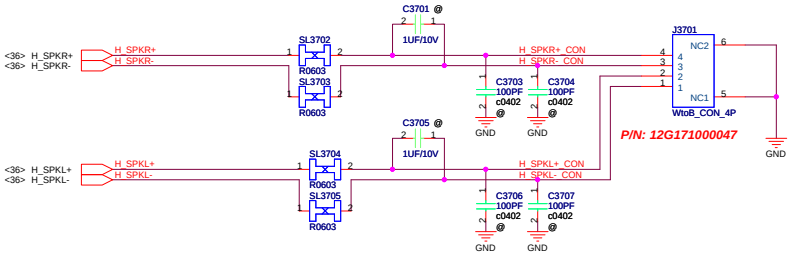
Size	Project Name	Rev
C	F83Vf	1.1
	P/N <OrgAddr2>	

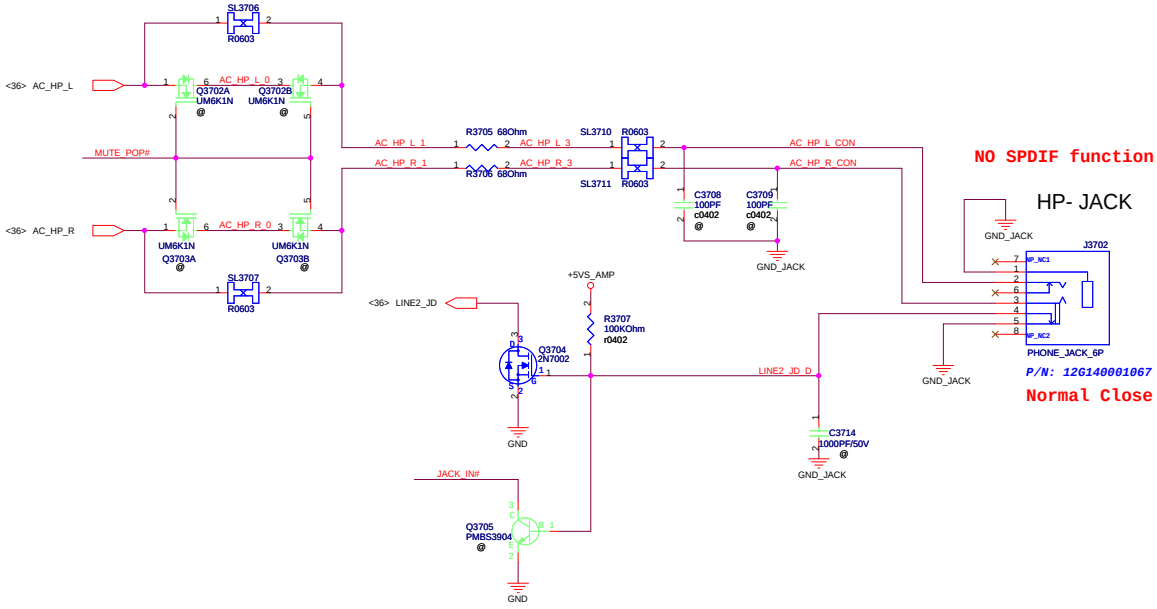
Date: Thursday, July 16, 2009 Sheet 35 of 100

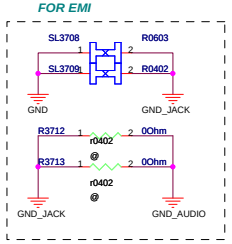


PEGATRON	Title : AUDIO		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 36 of 100		



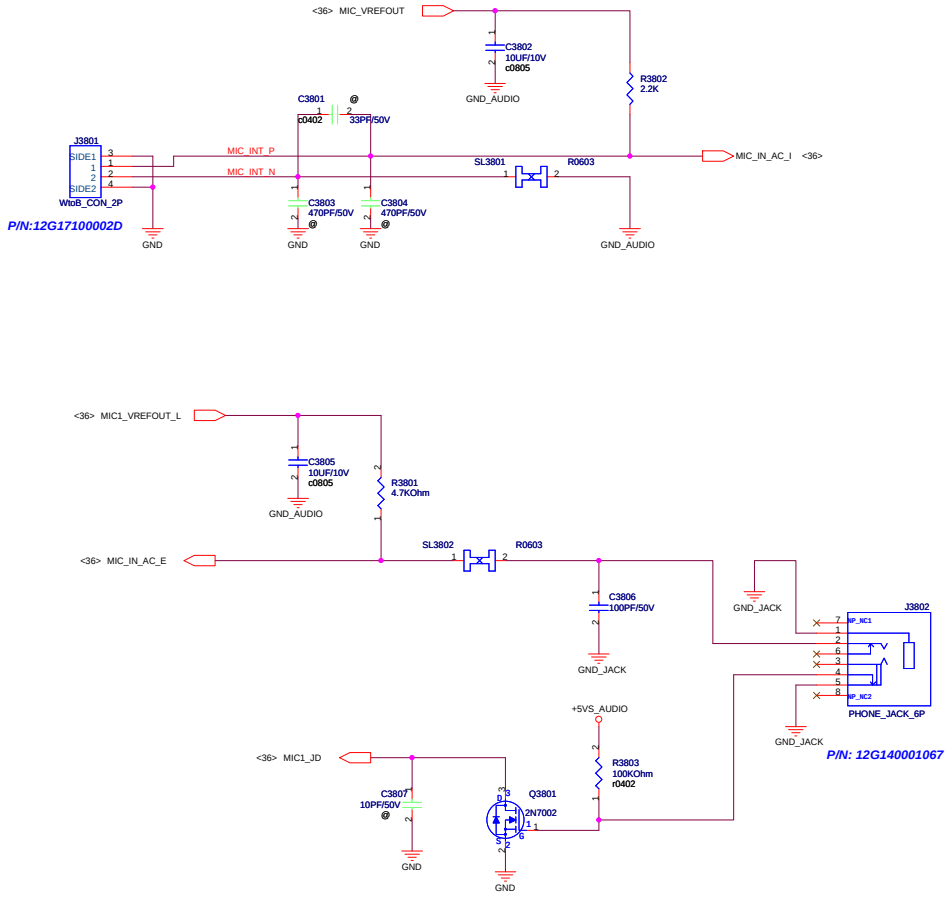






PEGATRON	Title : AUDIO		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 37 of 100		

Internal MIC Pre-Amplifier



PEGATRON	Title : AUDIO		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf	P/N: <OrgAddr2>	Rev: 1.1
Date: Thursday, July 16, 2009	Sheet 38 of 100		

PEGATRON

Title : <Title>

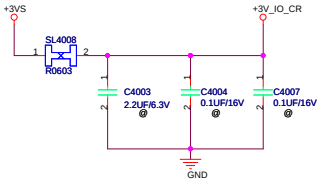
PEGATRON COMPUTER INC

Engineer: Zack Kuo

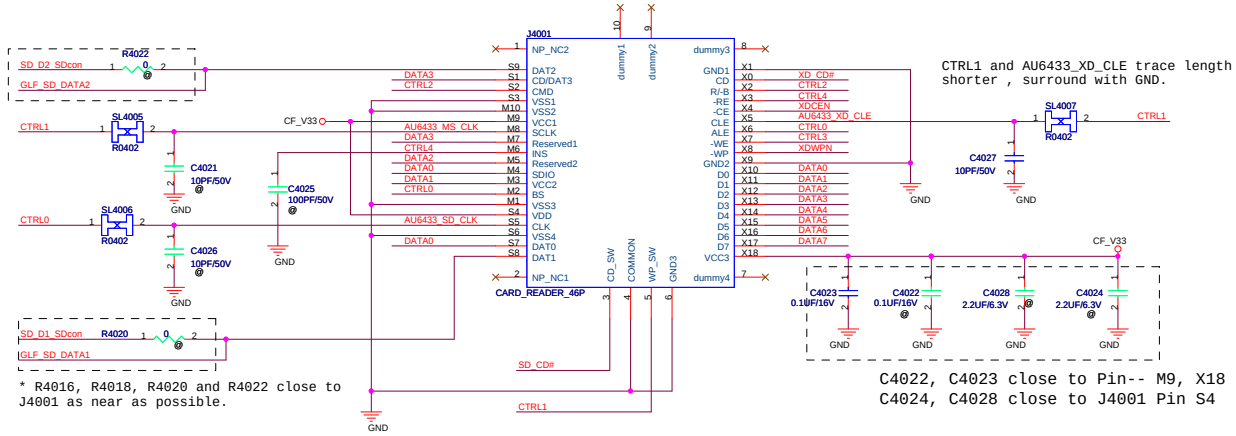
Size	Project Name	Rev
C	F83Vf	1.1
	P/N <OrgAddr2>	

Date: Thursday, July 16, 2009 Sheet 39 of 100

0304 for card reader chip via



CARD READER CONNECTOR

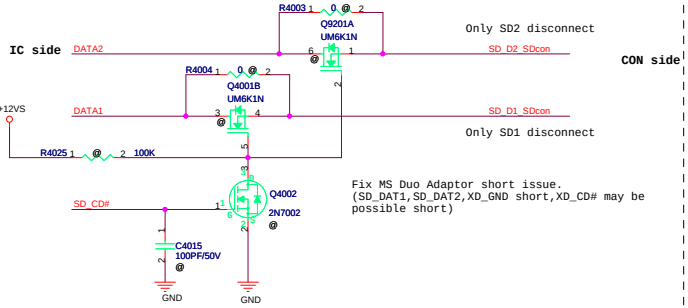


CTRL1 and AU6433_XD_CLE trace length shorter , surround with GND.

* R4016, R4018, R4020 and R4022 close to J4001 as near as possible.

C4022, C4023 close to Pin-- M9, X18
C4024, C4028 close to J4001 Pin S4

For AU6433-GEF

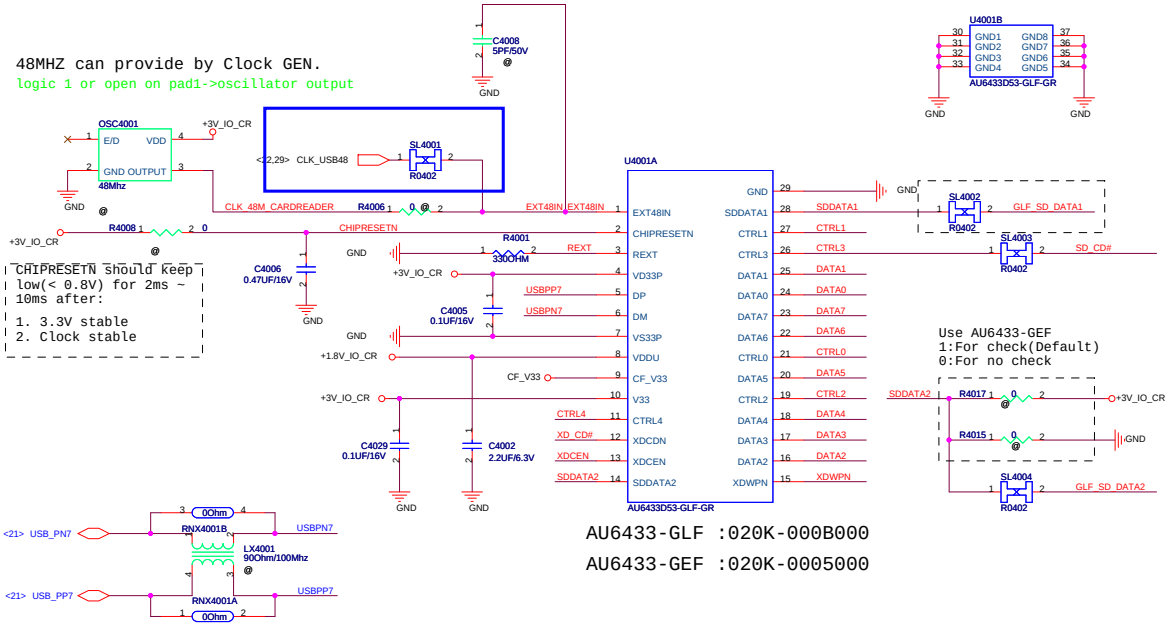


Only SD2 disconnect

Only SD1 disconnect

Fix MS Duo Adaptor short issue.
(SD_DAT1,SD_DAT2,XD_GND short,XD_CD# may be possible short)

0304 for card reader chip via



Use AU6433-GEF
1:For check(Default)
0:For no check

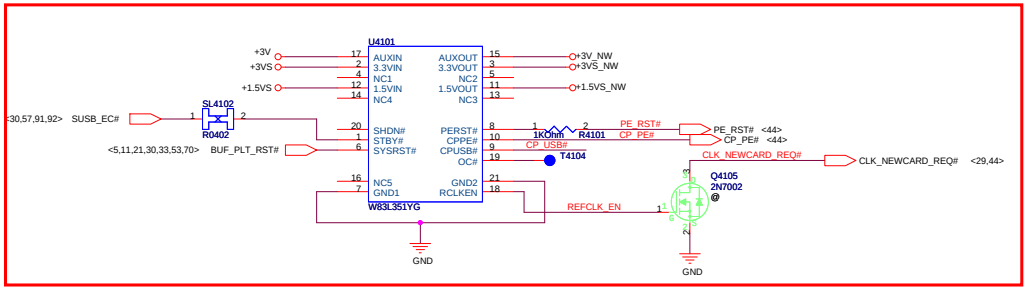
AU6433-GLF :020K-000B000
AU6433-GEF :020K-0005000

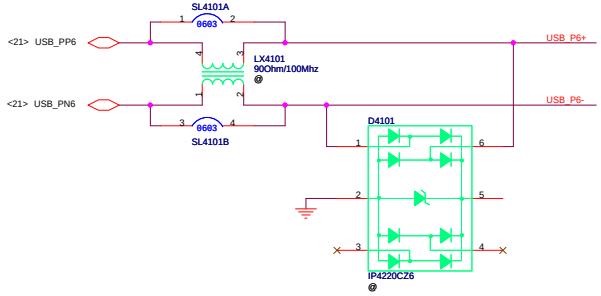
```
CTRL0->SDCLK/XDALE/MSBS
CTRL1->SDWP/XDCLE/MSCLK
CTRL2->SDCMD/XDRBN
CTRL3->SDCDN/XDWRN
CTRL4->XDRDN/MSINS

XDCDN->XDCDN
XDCEN->XDCEN
SDDATA2->SDDATA2/xD CIS check is disable
XDWPN->XDWPN

ADDATA1->SDDATA1

DATA0->SDDATA0/XDDATA0/MSDATA0
DATA1->XDDATA1/MSDATA1
DATA2->XDDATA2/MSDATA2
DATA3->SDDATA3/XDDATA3/MSDATA3
DATA4->SDDATA4/XDDATA4/MSDATA4
DATA5->SDDATA5/XDDATA5/MSDATA5
DATA6->SDDATA6/XDDATA6/MSDATA6
DATA7->SDDATA7/XDDATA7/MSDATA7
```

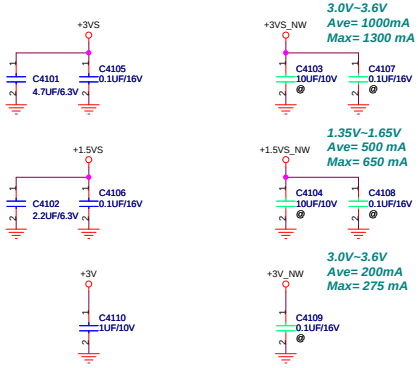
AU6433 GEF /GLF colay.

```
Option 1:AU6433-GEF
If use GEF package need:

unmount-> R4016,R4018
mount->R4017,R4020,R4022,R4025,Q4001,Q4002.


Option 2:AU6433-GLF
If use GLF package need:
unmount->
R4017,R4020,R4022,R4025,Q4001,Q4002.
mount->R4016,R4018
```

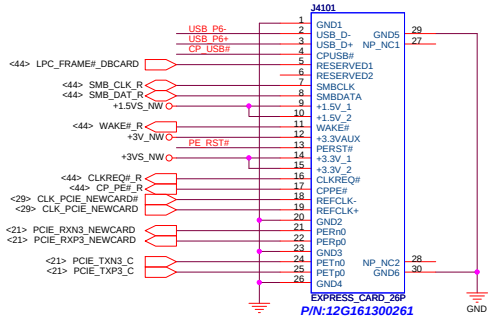
PEGATRON	Title : Card Reader AU8433		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 40 of 100		



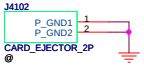




NewCard Header



NewCard Ejecter



PEGATRON	Title : CB_NEWCARD	
PEGATRON COMPUTER INC	Engineer: Zack Kuo	
Size: C	Project Name: F83Vf	Rev: 1.1
	P/N: <OrgAddr2>	
Date: Thursday, July 16, 2009	Sheet 41 of 100	

PEGATRON

Title : Connector, LED

PEGATRON COMPUTER INC

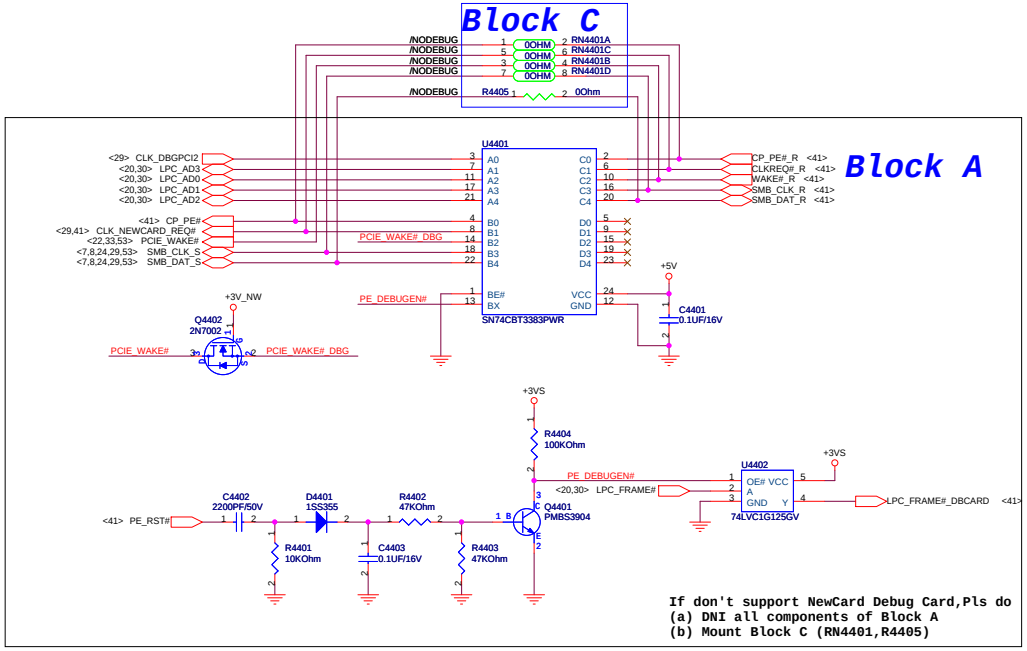
Engineer: Zack Kuo

Size	Project Name	Rev
C	F83Vf	1.1
	P/N <OrgAddr2>	

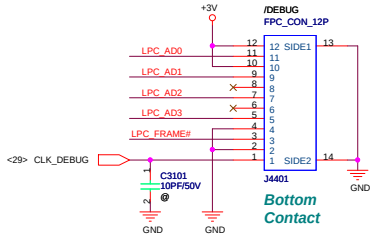
Date: Thursday, July 16, 2009 Sheet 42 of 100

PEGATRON	Title : Connector, LED		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 43 of 100		

For NewCard Debug Card

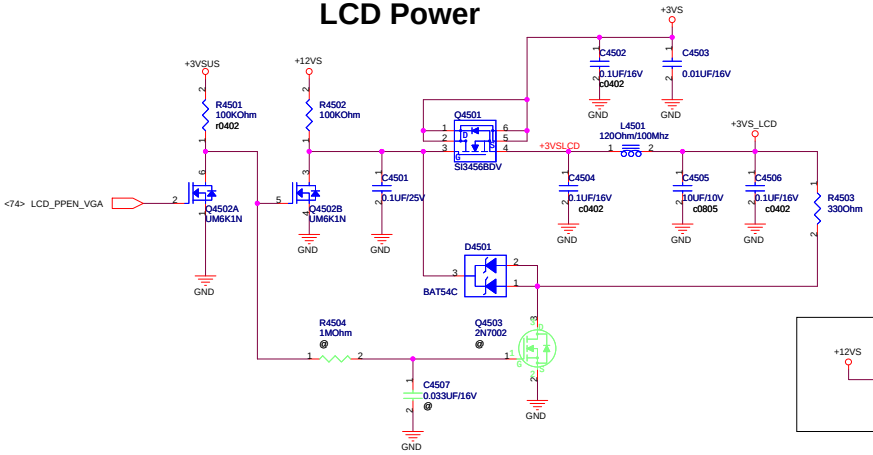


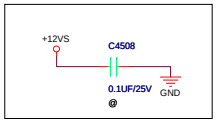
LPC Debug Port

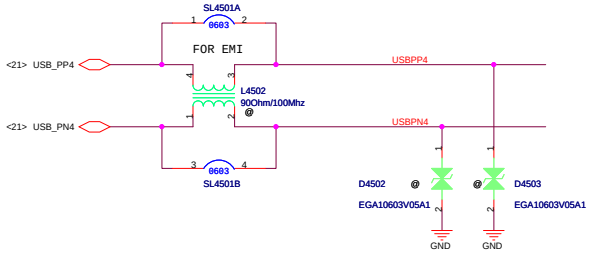


PEGATRON	Title : DEBUG		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 44 of 100		

LCD Power





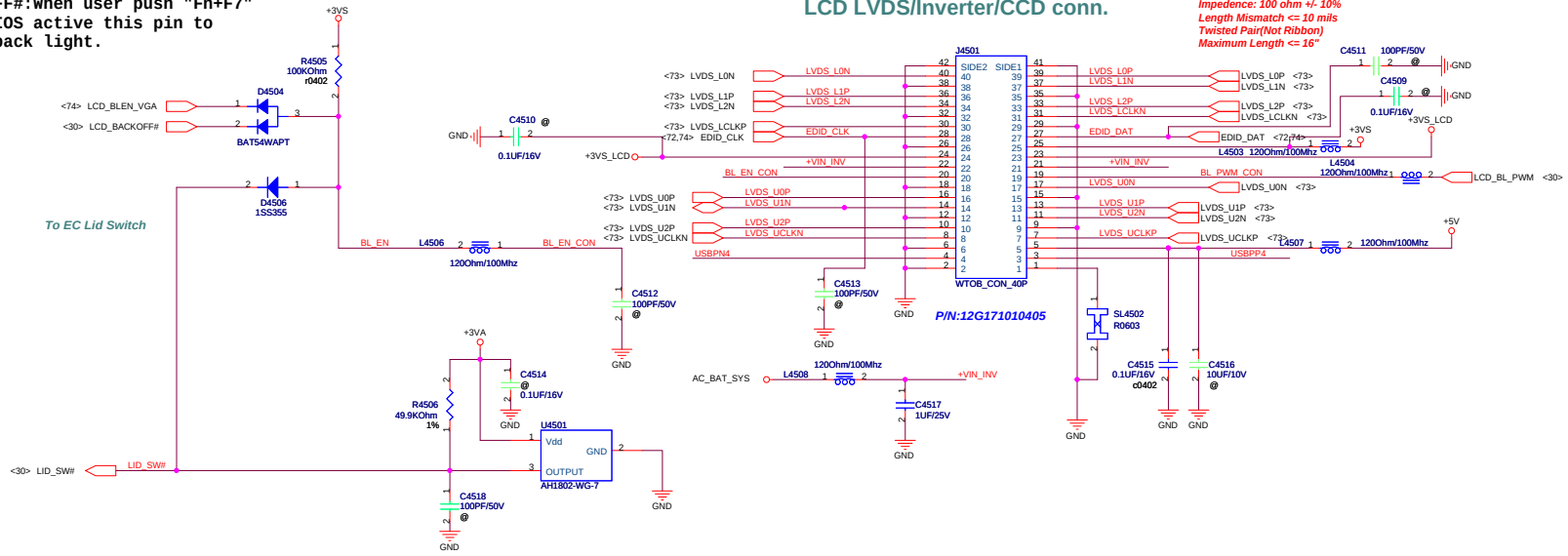


BIOS

LCD_BACKOFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.

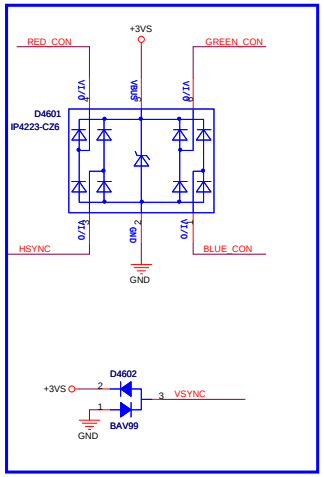
LCD LVDS/Inverter/CCD conn.

Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"



PEGATRON	Title : Connector, LED		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 45 of 100		

PLACE ESD Diodes near connector



37.5 ohm **50 ohm**

<72> CRT_RED — JP4601 SHORT_PIN @ — CRT_R_C — R4601 150Ohm 1% — L4601 47Ohm/100Mhz — C4601 10PF/50V c0402 — C4602 10PF/50V c0402 — GND

<72> CRT_GREEN — JP4602 SHORT_PIN @ — CRT_G_C — R4604 150Ohm 1% — L4602 47Ohm/100Mhz — C4603 10PF/50V c0402 — C4604 10PF/50V c0402 — GND

<72> CRT_BLUE — JP4603 SHORT_PIN @ — CRT_B_C — R4606 150Ohm 1% — L4603 47Ohm/100Mhz — C4605 10PF/50V c0402 — C4606 10PF/50V c0402 — GND

+3VS — SL4601 R0805

<72> CRT_VSYNC — U4601 74LVC1G125GV (OE# VCC A GND Y) — VSYNC_CRT — 33Ohm R4608 — C4607 47pF/50V C0402 — GND

<72> CRT_HSYNC — U4602 74LVC1G125GV (OE# VCC A GND Y) — HSYNC_CRT — 33Ohm R4609 — C4608 47pF/50V C0402 — GND

+5VS — D4603 1SS355 @ — +5VS_HDMI_CRT

RN4601A 4.7KOhm — RN4601B 4.7KOhm — RN4601D 4.7KOhm — RN4601C 4.7KOhm

Q4601A UM6K1N — Q4601B UM6K1N

<72> CRT_DDC_DAT

<72> CRT_DDC_CLK

D4604 @ EGA10603V05A1 — D4605 @ EGA10603V05A1 — GND GND

J4601 D_SUB_15P — P_GND1 — NP_NC1 — NP_NC2 — P_GND2 — GND

RED_CON — DDC2BD — BLUE_CON — VSYNC — GREEN_CON — HSYNC — DDC2BC

12G10110915K

PEGATRON	Title :	Connector, LED	
PEGATRON COMPUTER INC	Engineer:	Zack Kuo	
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 46 of 100		

PEGATRON

Title : Connector, LED

PEGATRON COMPUTER INC

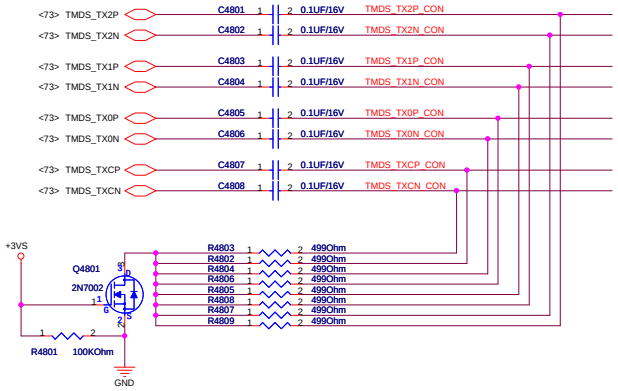
Engineer: Zack Kuo

Size	Project Name	Rev
C	F83Vf	1.1
	P/N <OrgAddr2>	

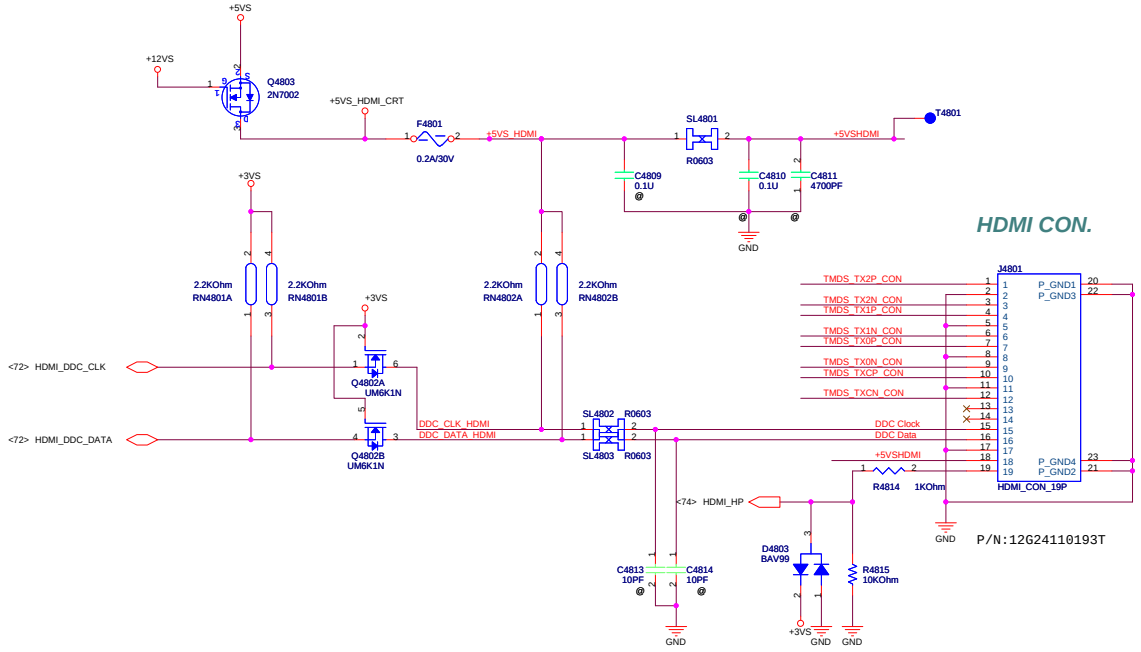
Date: Thursday, July 16, 2009 Sheet 47 of 100

HDMI

near the HDMI connector



Reference should be +5VS, but ATI answer that +3VS is fine. As long as it can turn the MOSFET on.



HDMI CON.

P/N:12G24110193T

Note: 1. L1805,L1806,L1807: For EMI.(defult=0 ohm)
2. DDC_CLK_HDMI,DDC_DATA_HDMI: +5V tolerant

PEGATRON	Title : Connector, LED		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 48 of 100		

PEGATRON

Title : Connector, LED

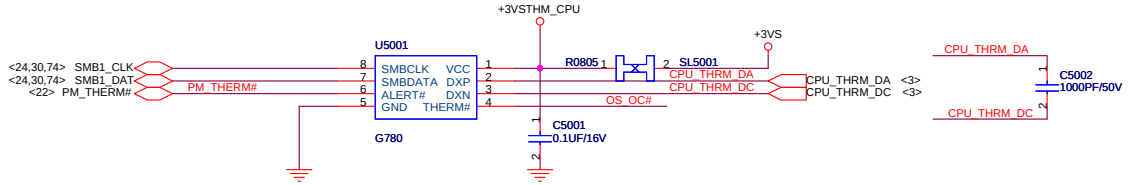
PEGATRON COMPUTER INC

Engineer: *Zack Kuo*

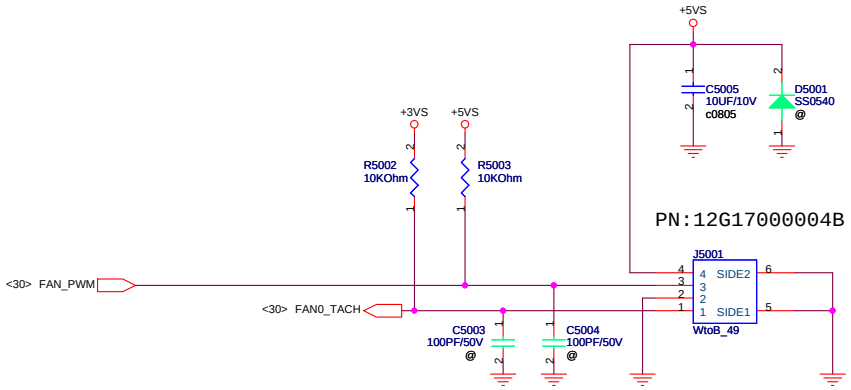
Size	Project Name	Rev
C	**F83Vf**	1.1
	P/N <OrgAddr2>	

Date: Thursday, July 16, 2009 Sheet 49 of 100

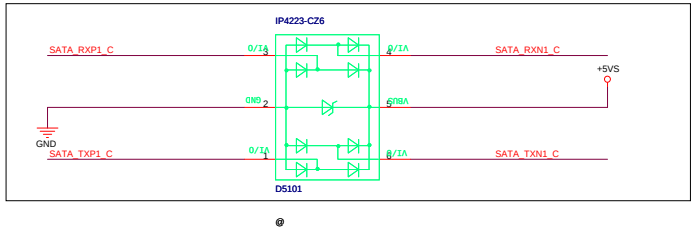
CPU Thermal Sensor



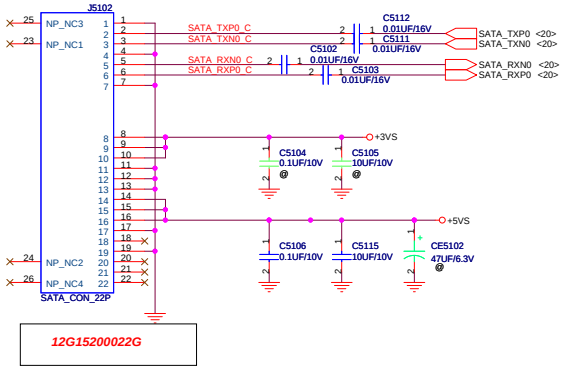
PWM Fan



ASUSTeK COMPUTER INC. NB4	Title : FAN_Fan & Sensor	
	Engineer: Zack Kuo	
Size: Custom	Project Name: F83Vf	Rev: 1.1
Date: Thursday, July 16, 2009	Sheet 50 of 100	



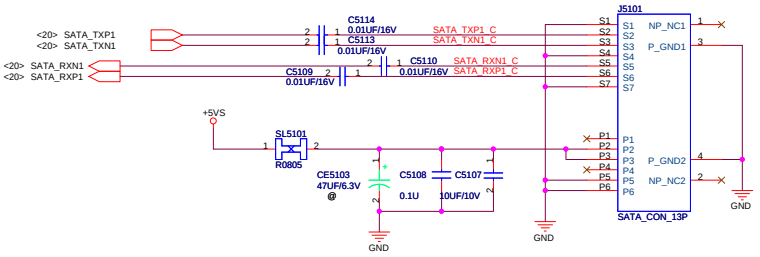
SATA HDD con.



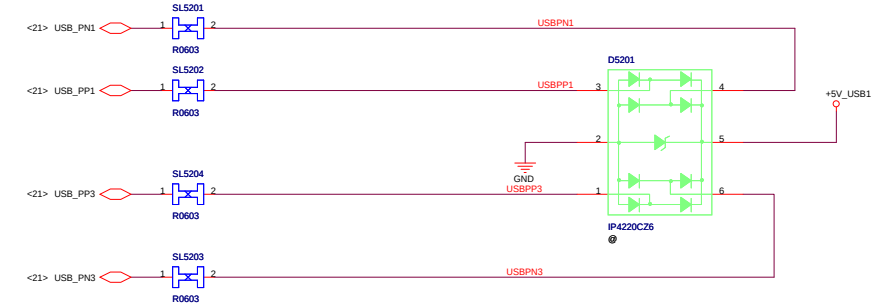
12G15200022G

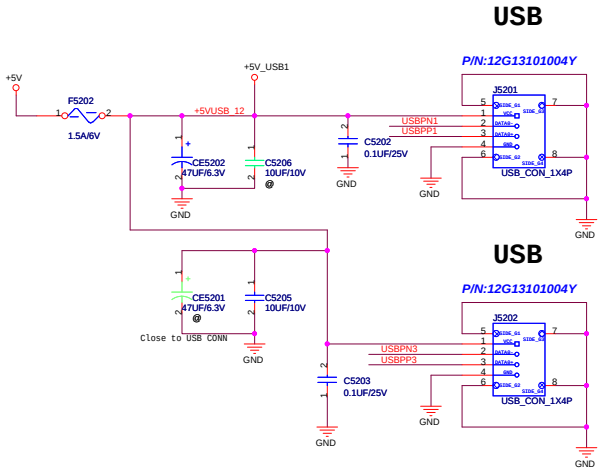
SATA CD-ROM con.

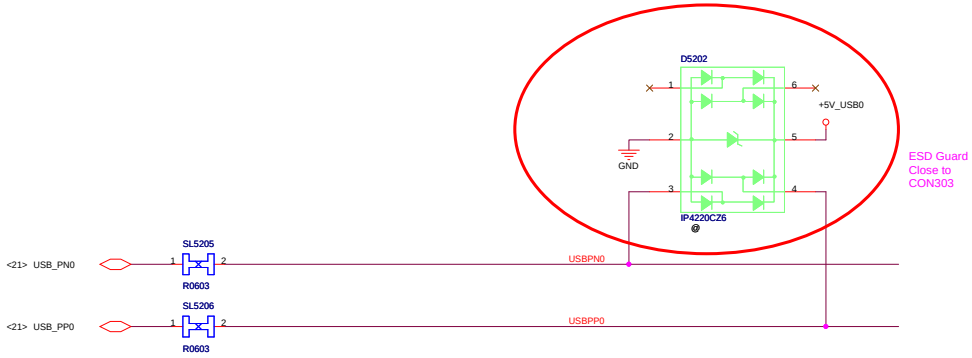
P/N:12G15100013J

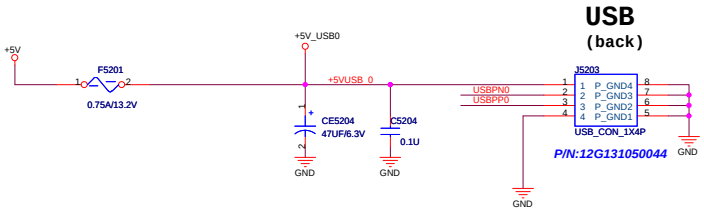


PEGATRON	Title : HDD/ODD CON		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 51 of 100		



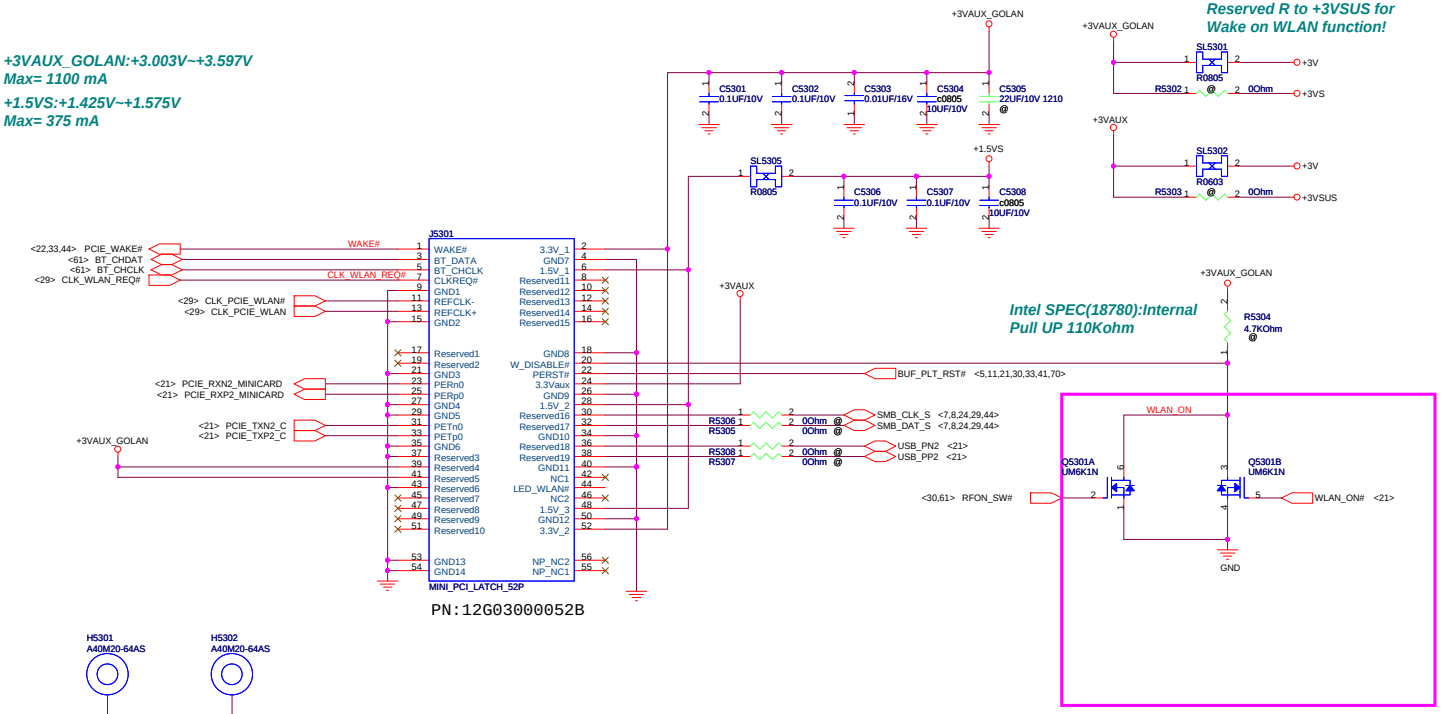






PEGATRON	Title : Connector, LED		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 52 of 100		

+3VAUX_GOLAN:+3.003V~+3.597V
Max= 1100 mA
+1.5VS:+1.425V~+1.575V
Max= 375 mA



PN:12G03000052B

PEGATRON	Title : Connector, LED		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 53 of 100		

PEGATRON

Title : Connector, LED

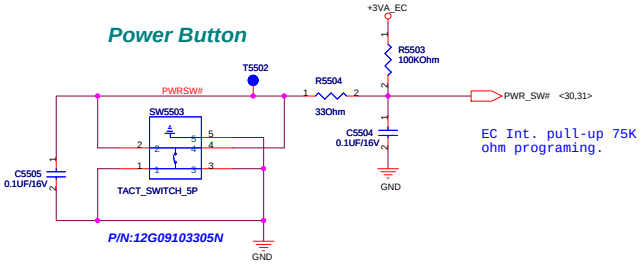
PEGATRON COMPUTER INC

Engineer: Zack Kuo

Size	Project Name	Rev
C	F83Vf	1.1
	P/N <OrgAddr2>	

Date: Thursday, July 16, 2009 Sheet 54 of 100

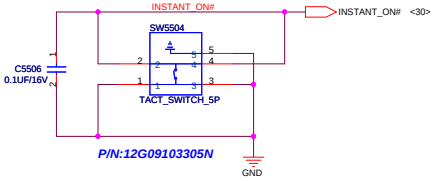
Power Button



EC Int. pull-up 75K ohm programing.

P/N:12G09103305N

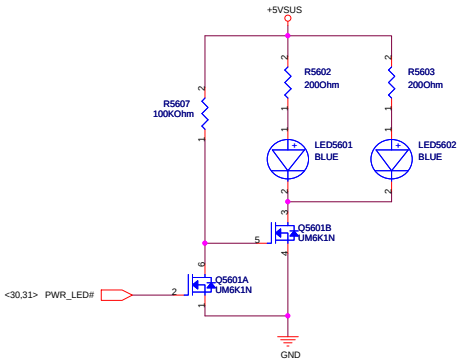
EXPRESS GATE



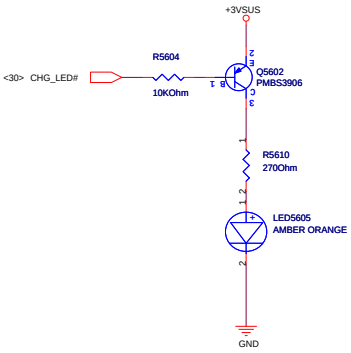
P/N:12G09103305N

PEGATRON	Title : SWITCH	
PEGATRON COMPUTER INC	Engineer: Zack Kuo	
Size: C	Project Name: F83Vf	Rev: 1.1
	P/N: <OrgAddr2>	
Date: Thursday, July 16, 2009	Sheet 55 of 100	

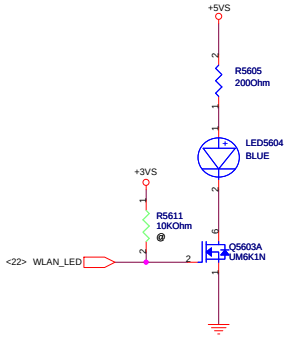
PWR LED



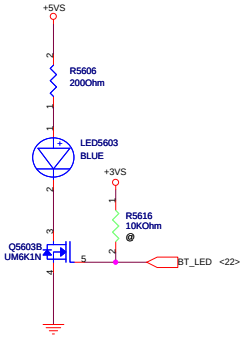
For BATTERY LED



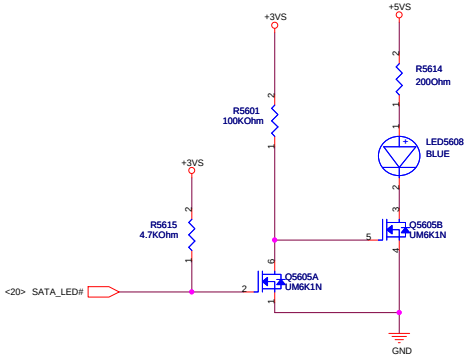
WireLess LED



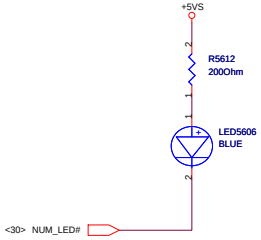
BT LED



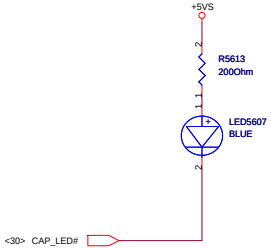
SATA LED



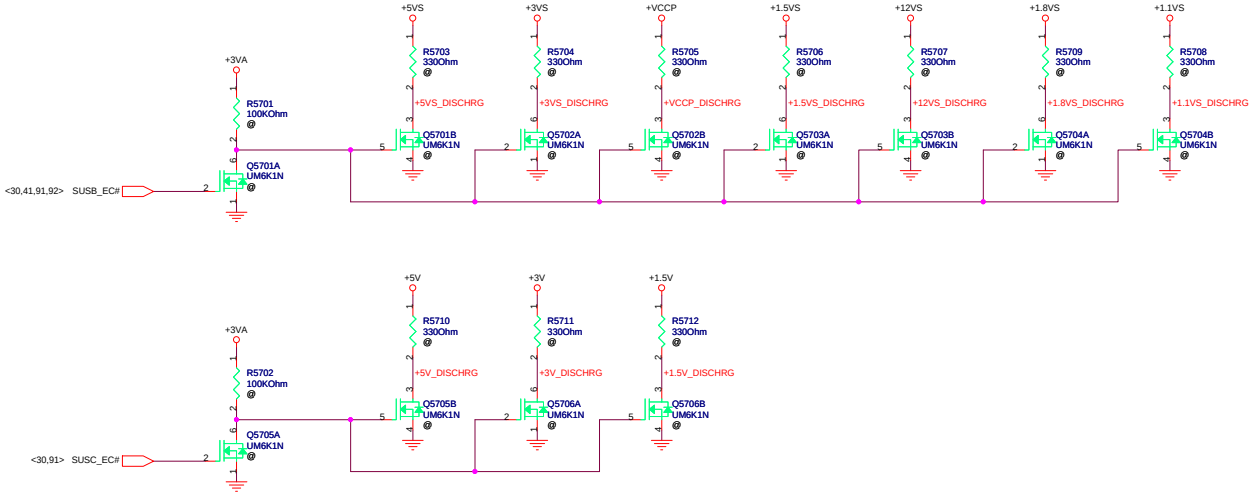
Num Lock



Cap. Lock



PEGATRON	Title : Connector, LED	
PEGATRON COMPUTER INC	Engineer: Zack Kuo	
Size: C	Project Name: F83Vf	Rev: 1.1
	P/N: <OrgAddr2>	
Date: Thursday, July 16, 2009	Sheet 56 of 100	



PEGATRON	Title : DISCHARGE		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 57 of 100		

PEGATRON

Title : Connector, LED

PEGATRON COMPUTER INC

Engineer: Zack Kuo

Size	Project Name	Rev
C	F83Vf	1.1
	P/N <OrgAddr2>	

Date: Thursday, July 16, 2009 Sheet 58 of 100

PEGATRON

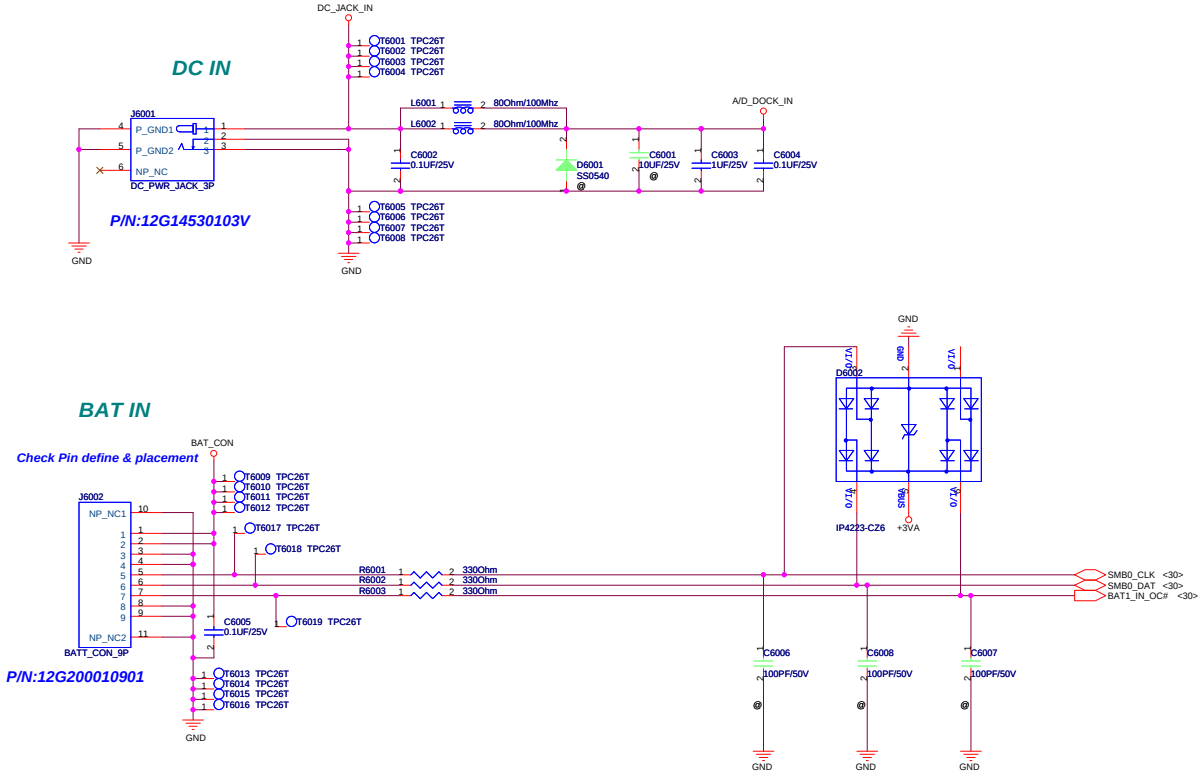
Title : Connector, LED

PEGATRON COMPUTER INC

Engineer: Zack Kuo

Size	Project Name	Rev
C	F83Vf	1.1
	P/N <OrgAddr2>	

Date: Thursday, July 16, 2009 Sheet 59 of 100

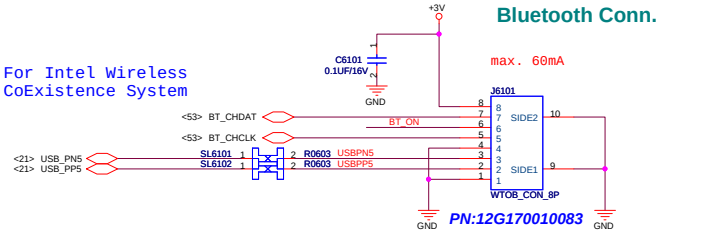


PEGATRON	Title : Connector, LED		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 60 of 100		

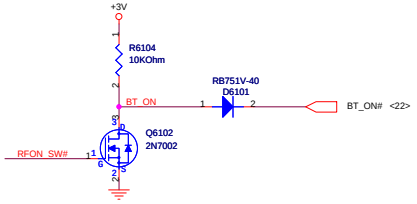
Bluetooth Conn.

For Intel Wireless
CoExistence System

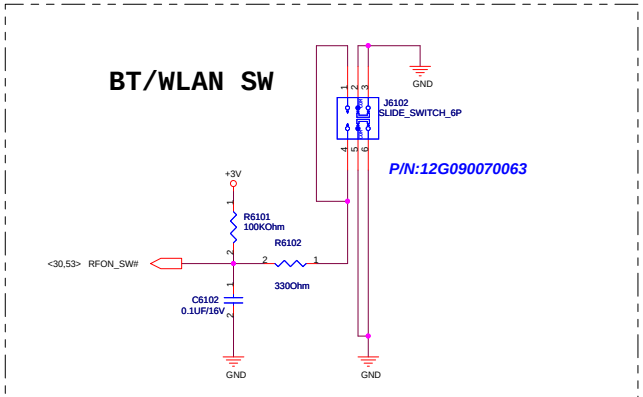
max. 60mA



P/N:12G170010083



BT/WLAN SW



P/N:12G090070063

PEGATRON	Title : Connector, LED		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 61 of 100		

PEGATRON

Title : Connector, LED

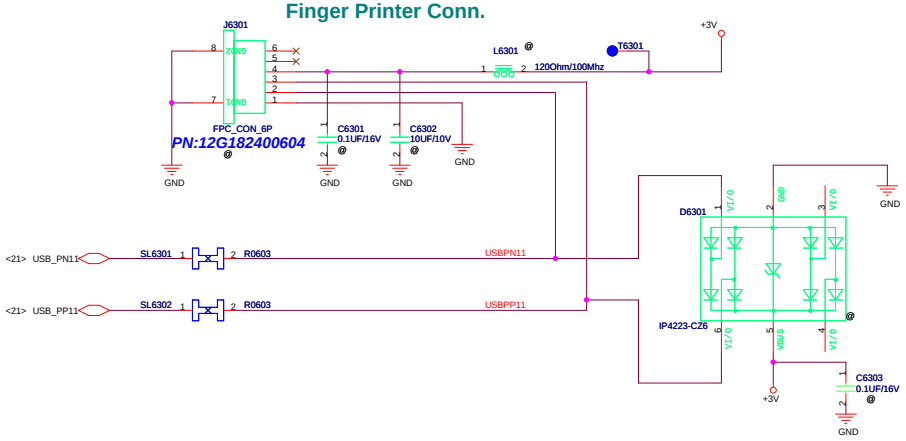
PEGATRON COMPUTER INC

Engineer: Zack Kuo

Size	Project Name	Rev
C	F83Vf	1.1
	P/N <OrgAddr2>	

Date: Thursday, July 16, 2009 Sheet 62 of 100

Finger Printer Conn.



PEGATRON	Title : Connector, LED		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 63 of 100		

PEGATRON

Title : Connector, LED

PEGATRON COMPUTER INC

Engineer: Zack Kuo

Size	Project Name	Rev
C	F83Vf	1.1
	P/N <OrgAddr2>	

Date: Thursday, July 16, 2009 Sheet 64 of 100

PEGATRON

Title : Connector, LED

PEGATRON COMPUTER INC

Engineer: Zack Kuo

Size	Project Name	Rev
C	F83Vf	1.1
	P/N <OrgAddr2>	

Date: Thursday, July 16, 2009 Sheet 65 of 100

PEGATRON

Title : Connector, LED

PEGATRON COMPUTER INC

Engineer: Zack Kuo

Size	Project Name	Rev
C	F83Vf	1.1
	P/N <OrgAddr2>	

Date: Thursday, July 16, 2009 Sheet 66 of 100

PEGATRON

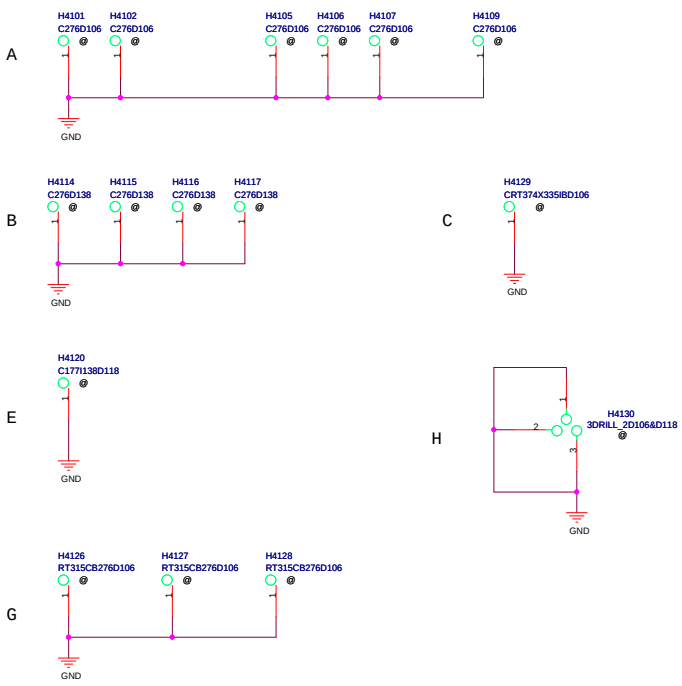
Title : Connector, LED

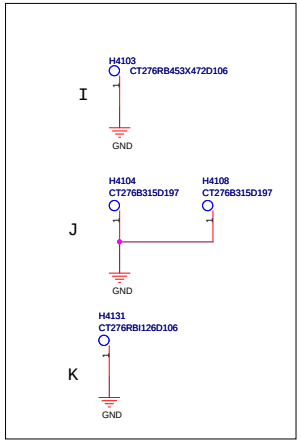
PEGATRON COMPUTER INC

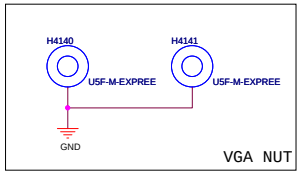
Engineer: Zack Kuo

Size	Project Name	Rev
C	F83Vf	1.1
	P/N <OrgAddr2>	

Date: Thursday, July 16, 2009 Sheet 67 of 100







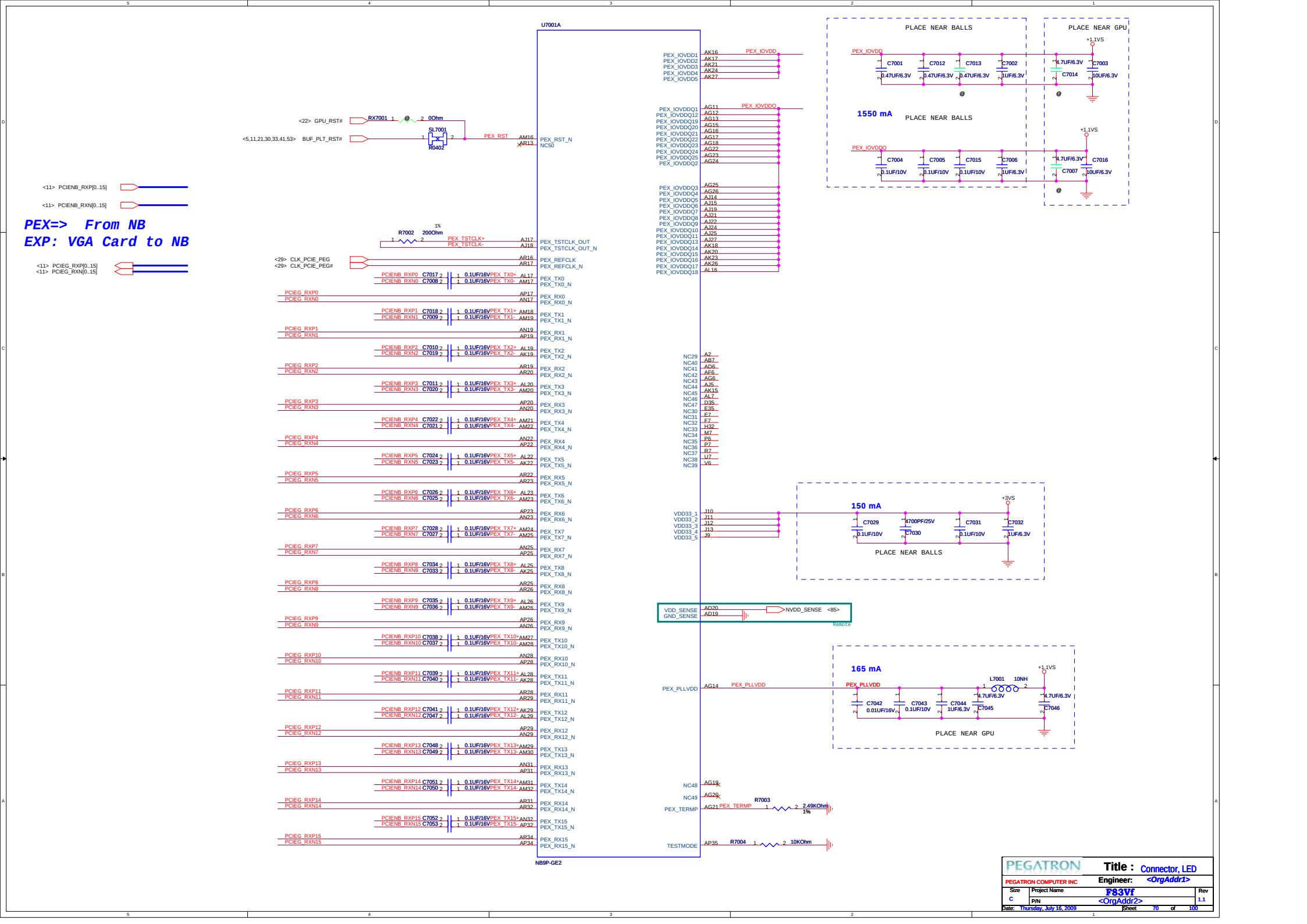
PEGATRON	Title : ScrewHole		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 68 of 100		

R1.1

2009/06/30

1. Set DDR3 VREF to 0.75V LDO output.
2. Change Card Reader to AU6433D53-GLF.
3. Change LAN to Atheros AR6132.
4. Change Transformer to 10/100 TAIMAG HA003
5. Change ClockGen to ICS9LPR363.
6. Remove ClockGen 3362 circuits.
7. Unstuff Finger Printer Connector.
8.

PEGATRON	Title : Connector, LED	
PEGATRON COMPUTER INC	Engineer: Zack Kuo	
Size: C	Project Name: F83Vf	Rev: 1.1
	P/N: <OrgAddr2>	
Date: Thursday, July 16, 2009	Sheet 69 of 100	


PEX=> From NB
EXP: VGA Card to NB
<11> PCIENB_RXP[0..15]
<11> PCIENB_RXN[0..15]
<11> PCIEG_RXP[0..15]
<11> PCIEG_RXN[0..15]
U7001A
NB9P-GE2
<22> GPU_RST#
<5,11,21,30,33,41,53> BUF_PLT_RST#
RX7001 0Ohm
SL7001
R0402
PEX_RST
PEX_RST_N
NC50
R7002 200Ohm 1%
PEX_TSTCLK+
PEX_TSTCLK-
PEX_TSTCLK_OUT
PEX_TSTCLK_OUT_N
<29> CLK_PCIE_PEG
<29> CLK_PCIE_PEG#
PEX_REFCLK
PEX_REFCLK_N
PEX_IOVDD1
PEX_IOVDD2
PEX_IOVDD3
PEX_IOVDD4
PEX_IOVDD5
PEX_IOVDD
PEX_IOVDDQ1
PEX_IOVDDQ12
PEX_IOVDDQ19
PEX_IOVDDQ20
PEX_IOVDDQ21
PEX_IOVDDQ22
PEX_IOVDDQ23
PEX_IOVDDQ24
PEX_IOVDDQ25
PEX_IOVDDQ2
PEX_IOVDDQ
PEX_IOVDDQ3
PEX_IOVDDQ4
PEX_IOVDDQ5
PEX_IOVDDQ6
PEX_IOVDDQ7
PEX_IOVDDQ8
PEX_IOVDDQ9
PEX_IOVDDQ10
PEX_IOVDDQ11
PEX_IOVDDQ13
PEX_IOVDDQ14
PEX_IOVDDQ15
PEX_IOVDDQ16
PEX_IOVDDQ17
PEX_IOVDDQ18
PLACE NEAR BALLS
PLACE NEAR GPU
1550 mA
+1.1VS
C7001 0.47UF/6.3V
C7012 0.47UF/6.3V
C7013 0.47UF/6.3V
C7002 1UF/6.3V
C7014 4.7UF/6.3V
C7003 10UF/6.3V
C7004 0.1UF/10V
C7005 0.1UF/10V
C7015 0.1UF/10V
C7006 1UF/6.3V
C7007 4.7UF/6.3V
C7016 10UF/6.3V
NC29
NC40
NC41
NC42
NC43
NC44
NC45
NC46
NC47
NC30
NC31
NC32
NC33
NC34
NC35
NC36
NC37
NC38
NC39
VDD33_1
VDD33_2
VDD33_3
VDD33_4
VDD33_5
150 mA
+3VS
C7029 0.1UF/10V
4700PF/25V
C7030
C7031 0.1UF/10V
C7032 1UF/6.3V
VDD_SENSE
GND_SENSE
NVDD_SENSE <85>
Remote
PEX_PLLVDD
165 mA
L7001 10NH
C7042 0.01UF/16V
C7043 0.1UF/10V
C7044 1UF/6.3V
C7045 4.7UF/6.3V
C7046 4.7UF/6.3V
NC48
NC49
PEX_TERMP
R7003 2.49KOhm 1%
TESTMODE
R7004 10KOhm
PEGATRON
PEGATRON COMPUTER INC
Title : Connector, LED
Engineer: <OrgAddr1>
Size C
Project Name F83Vf
P/N <OrgAddr2>
Rev 1.1
Date: Thursday, July 16, 2009
Sheet 70 of 100

PEGATRON

Title : Connector, LED

PEGATRON COMPUTER INC

Engineer: <OrgAddr1>

Size	Project Name	Rev
C	F83Vf	1.1
	P/N <OrgAddr2>	

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change 4.7uF to 1uF
C5001,C5005,C5015

CRT

+3VS
RN7205A 2.2KOhm
RN7205B 2.2KOhm
L7201 220Ohm/100Mhz
130 mA
I0603
Irat=600mA
C7201 4.7UF/6.3V
C7202 4700PF/25V
c0603
C7203 0.01UF/25V
R7201 1240Ohm 1%
DACA_VDD
DACA_VREF
DACA_RSET
U7001F
AJ12
AK12
AK13
DACA_VDD
DACA_VREF
DACA_RSET
I2CA_SCL
I2CA_SDA
DACA_HSYNC
DACA_VSYNC
DACA_RED
DACA_GREEN
DACA_BLUE
NB9P-GE2
G1 I2CA_CLK
G4 I2CA_DAT
33OHM RN7201B
33OHM RN7201A
CRT_DDC_CLK <46>
CRT_DDC_DAT <46>
AM13 CRT_HSYNC <46>
AL13 CRT_VSYNC <46>
AM15 DAC_VR
AM14 DAC_VG
AL14 DAC_VB
JP7201
JP7202
JP7203
CRT_RED <46>
CRT_GREEN <46>
CRT_BLUE <46>
R7202 150Ohm
R7203 150Ohm
R7204 150Ohm
near GPU

(180 mA)
DACB_VDD
U7001H
AC6
AC5
AB6
DACB_VDD
DACB_VREF
DACB_RSET
DACB_CSYNC
DACB_RED
DACB_GREEN
DACB_BLUE
AB5
AA4
AB4
Y4
NB9P-GE2
Composite
RN7219A 10KOHM

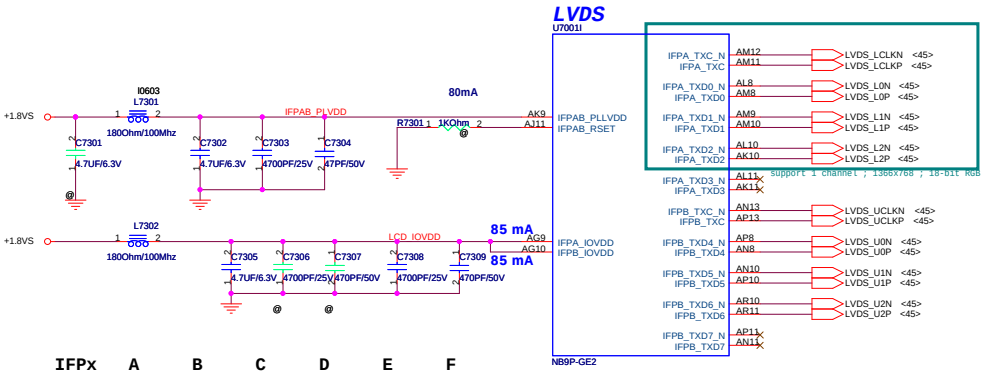
(130 mA)
DACC_VDD
U7001G
AG7
AK6
AH7
DACC_VDD
DACC_VREF
DACC_RSET
I2CB_SCL
I2CB_SDA
DACC_HSYNC
DACC_VSYNC
DACC_RED
DACC_GREEN
DACC_BLUE
AM1
AM2
AK4
AL4
AJ4
NB9P-GE2
G3 I2CB_CLK
G2 I2CB_DAT
33OHM RN7220B
33OHM RN7220A
HDMI_DDC_CLK <48>
HDMI_DDC_DATA <48>
RN7219B 10KOHM

XTAL_IN , XTAL_OUT
3.3V tolerance

correspondent BGA balls must be
12mils and 16 mil wide
near GPU

65 +25 +50 mA
+1.1VS
L7202 220Ohm/100Mhz
I0603
C7205 4.7UF/6.3V
C7204 1UF/6.3V
C7206 0.1UF/16V
C7207 0.1UF/16V
PLL_VDD
U7001E
AE9
AD9
AF9
PLLVDD
VID_PLLVDD
SP_PLLVDD
XTAL_SSIN
XTAL_IN
XTAL_OUTBUFF
XTAL_OUT
NB9P-GE2
<29> CLK_GFX_SSC
<29> CLK_GFX_NOSSC
R7216 @ 0Ohm
R7217 @ 0Ohm
XTALSSIN
D2
B1
D1
B2
XTAL_OUTB
near GPU
R7207 @
R7208 22Ohm
10KOhm
NOT SSC NEED PD 10K
R7209 10KOhm
R7218 @ 10KOhm
XTALIN
XTALOUT
X7201 27Mhz
10/10/5 PPM
C7208 18PF/50V
C7209 18PF/50V
SS_CLKIN
+3VS
RN7202A 10KOHM @
RN7202B 10KOHM @
+3VS
R7210 @ 4.7Ohm
+3VS_SSC
C7210 @ 1UF/6.3V
C7211 @ 0.1UF/16V
C7212 @ 470PF/50V
U7201 @ ICS91730AMLF
CLKIN
VDD
GND
CLKOUT/FS_IN0
REF_OUT/FS_IN1
PD#
SCLK
SDATA
SS_PD#
SS_REFOUT
EDID_CLK <45,74>
EDID_DAT <45,74>
R7211 @ 22Ohm
SS_CLKOUT
near ICS
EXTERNAL SPREAD SPECTRUM
Address: 0xD4H

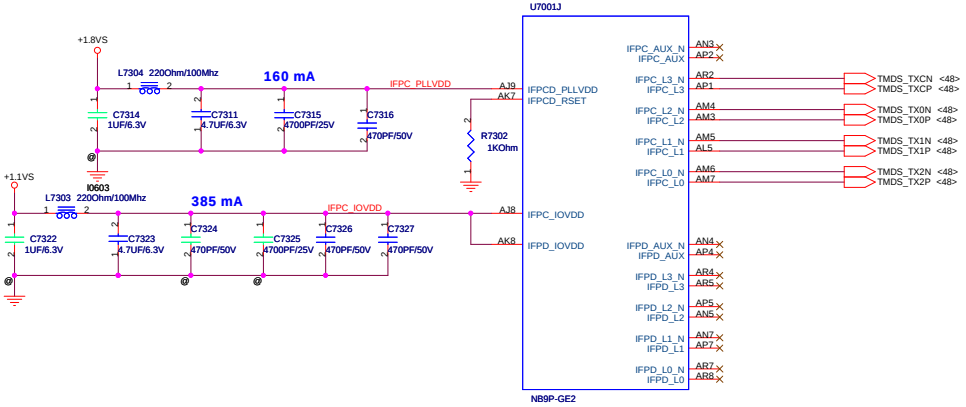
PEGATRON
PEGATRON COMPUTER INC
Title : Connector, LED
Engineer: <OrgAddr1>
Size C
Project Name F83Vf
P/N <OrgAddr2>
Rev 1.1
Date: Thursday, July 16, 2009
Sheet 72 of 100

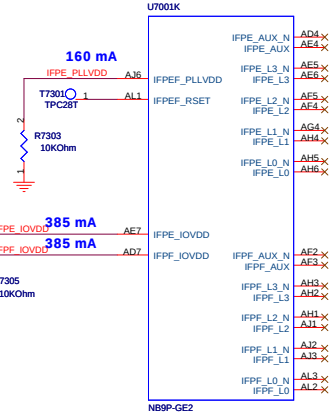


IFPx A B C D E F

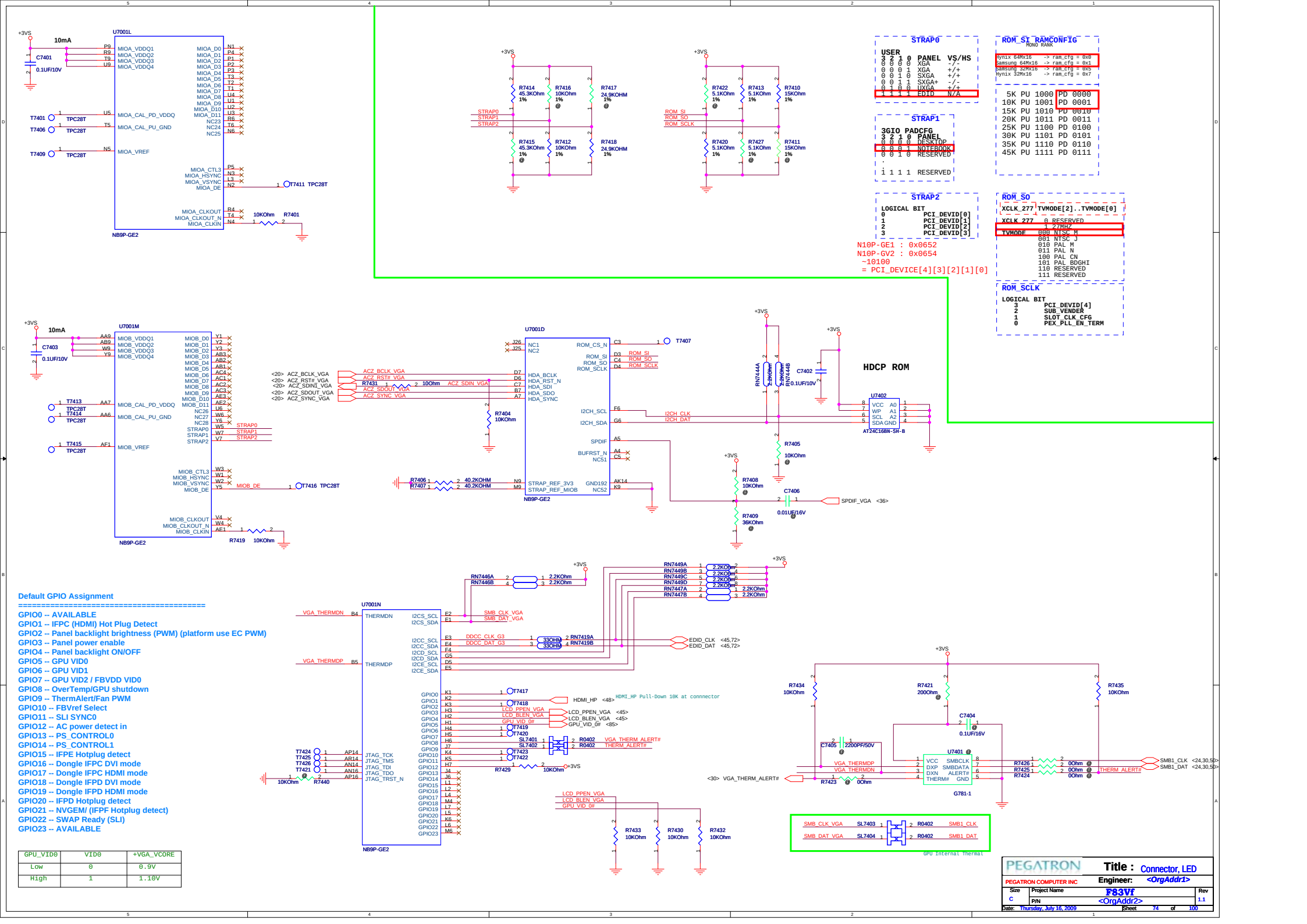
LVDS LVDS

HDMI HDMI HDMI
DVI DVI(S/D) DVI(S/D)





PEGATRON	Title : Connector, LED		
PEGATRON COMPUTER INC	Engineer: <OrgAddr1>		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 73 of 100		


U7001L
NB9P-GE2
U7001M
NB9P-GE2
U7001D
NB9P-GE2
U7001N
NB9P-GE2
HDCP ROM
AT24C16BN-SH-B
G781-1
STRAP0
USER
3 2 1 0 PANEL VS/HS
0 0 0 0 XGA -/-
0 0 0 1 XGA +/+
0 0 1 0 SXGA +/+
0 0 1 1 SXGA+ -/-
0 1 0 0 UXGA +/+
1 1 1 1 EDID N/A
STRAP1
3GIO PADCFG
3 2 1 0 PANEL
0 0 0 0 DESKTOP
0 0 0 1 NOTEBOOK
0 0 1 0 RESERVED
1 1 1 1 RESERVED
STRAP2
LOGICAL BIT
0 PCI_DEVID[0]
1 PCI_DEVID[1]
2 PCI_DEVID[2]
3 PCI_DEVID[3]
N10P-GE1 : 0x0652
N10P-GV2 : 0x0654
-10100
= PCI_DEVICE[4][3][2][1][0]
ROM_SI_RAMCONFIG
MONO RANK
Hynix 64Mx16 -> ram_cfg = 0x0
Samsung 64Mx16 -> ram_cfg = 0x1
Samsung 32Mx16 -> ram_cfg = 0x5
Hynix 32Mx16 -> ram_cfg = 0x7
5K PU 1000 PD 0000
10K PU 1001 PD 0001
15K PU 1010 PD 0010
20K PU 1011 PD 0011
25K PU 1100 PD 0100
30K PU 1101 PD 0101
35K PU 1110 PD 0110
45K PU 1111 PD 0111
ROM_SO
XCLK_277 TVMODE[2]..TVMODE[0]
XCLK_277 0 RESERVED
1 27MHZ
TVMODE 000 NTSC M
001 NTSC J
010 PAL M
011 PAL N
100 PAL CN
101 PAL_BDGHI
110 RESERVED
111 RESERVED
ROM_SCLK
LOGICAL BIT
3 PCI_DEVID[4]
2 SUB_VENDER
1 SLOT_CLK_CFG
0 PEX_PLL_EN_TERM
Default GPIO Assignment
GPIO0 -- AVAILABLE
GPIO1 -- IFPC (HDMI) Hot Plug Detect
GPIO2 -- Panel backlight brightness (PWM) (platform use EC PWM)
GPIO3 -- Panel power enable
GPIO4 -- Panel backlight ON/OFF
GPIO5 -- GPU VID0
GPIO6 -- GPU VID1
GPIO7 -- GPU VID2 / FBVDD VID0
GPIO8 -- OverTemp/GPU shutdown
GPIO9 -- ThermAlert/Fan PWM
GPIO10 -- FBVref Select
GPIO11 -- SLI SYNC0
GPIO12 -- AC power detect in
GPIO13 -- PS_CONTROL0
GPIO14 -- PS_CONTROL1
GPIO15 -- IFPE Hotplug detect
GPIO16 -- Dongle IFPC DVI mode
GPIO17 -- Dongle IFPC HDMI mode
GPIO18 -- Dongle IFPD DVI mode
GPIO19 -- Dongle IFPD HDMI mode
GPIO20 -- IFPD Hotplug detect
GPIO21 -- NVGEM/ (IFPF Hotplug detect)
GPIO22 -- SWAP Ready (SLI)
GPIO23 -- AVAILABLE
GPU_VID0 VID0 +VGA_VCORE
Low 0 0.9V
High 1 1.10V
PEGATRON
Title : Connector, LED
PEGATRON COMPUTER INC
Engineer: <OrgAddr1>
Size C
Project Name F83Vf
Rev 1.1
P/N <OrgAddr2>
Date: Thursday, July 16, 2009
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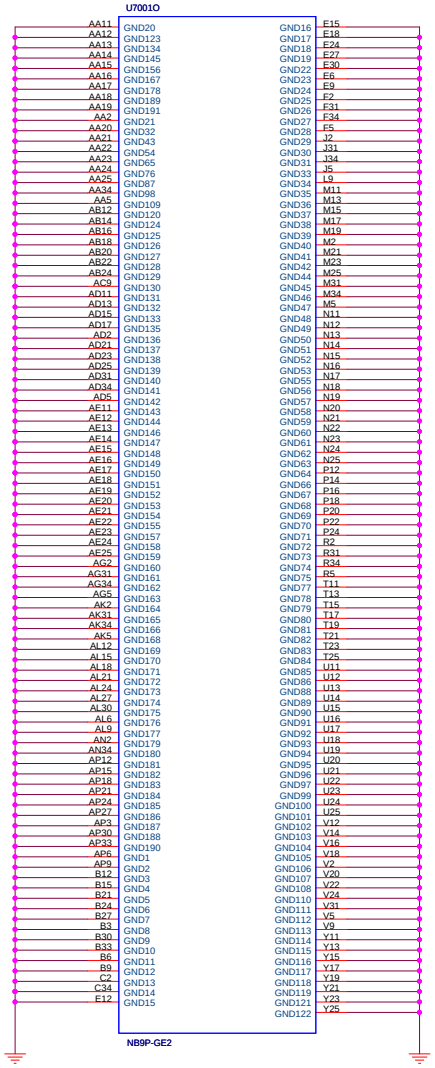
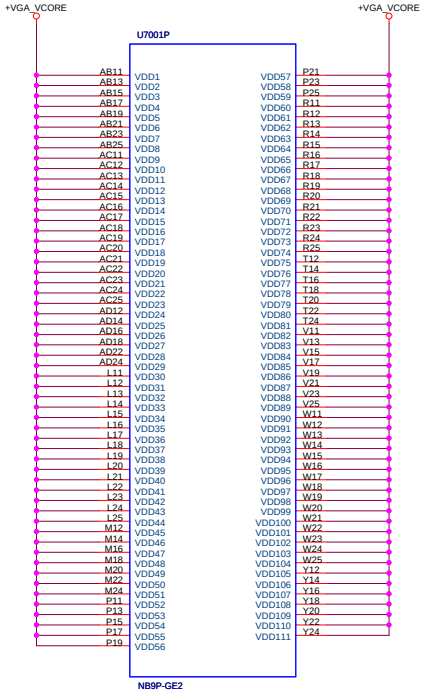
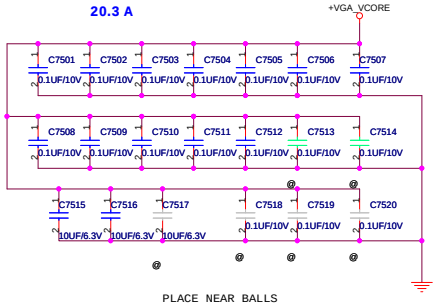




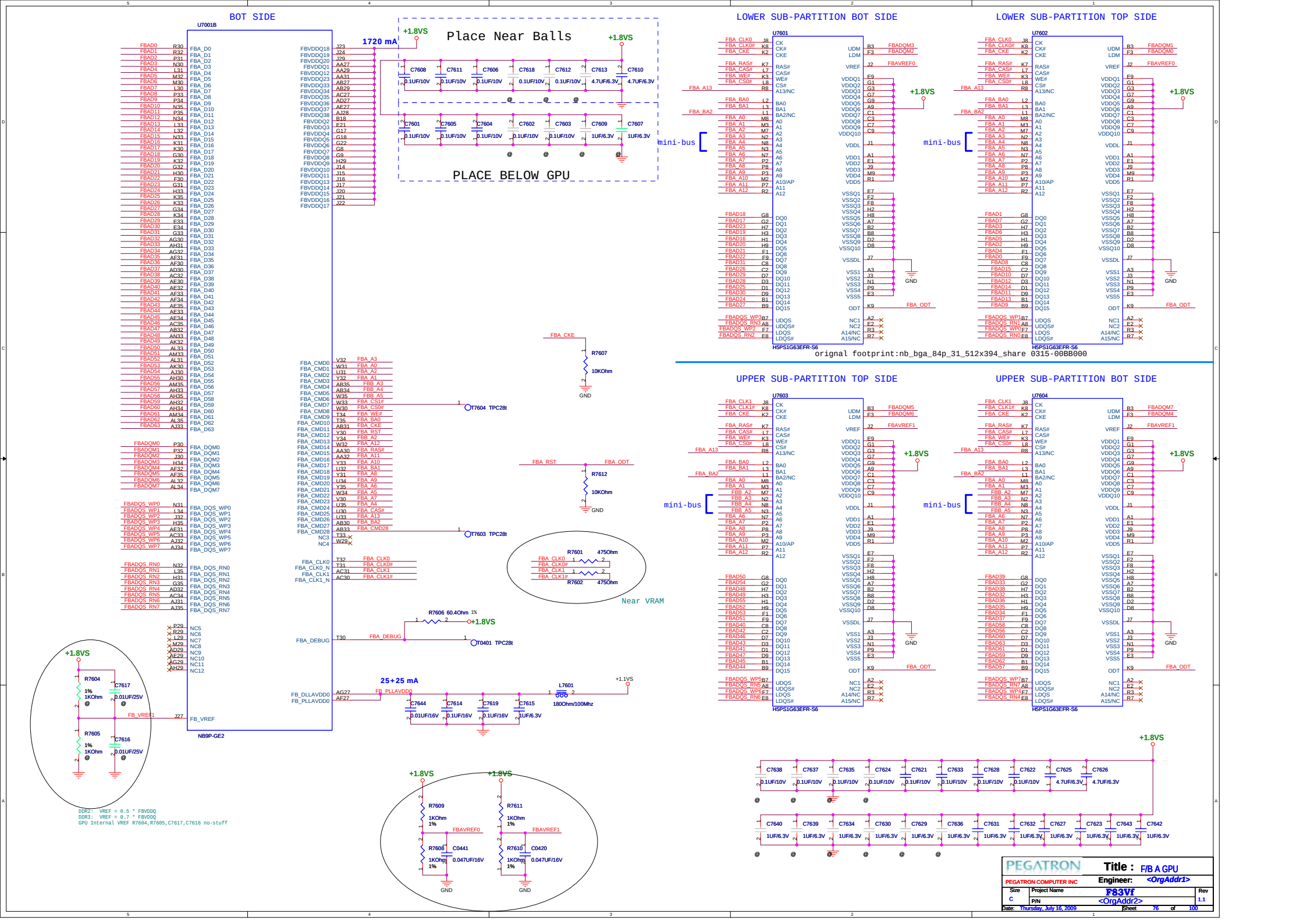


PLACE NEAR BALLS

17 0.1u

3 10u

PEGATRON	Title : Connector, LED		
PEGATRON COMPUTER INC	Engineer: <OrgAddr1>		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 75 of 100		


BOT SIDE
LOWER SUB-PARTITION BOT SIDE
LOWER SUB-PARTITION TOP SIDE
UPPER SUB-PARTITION TOP SIDE
UPPER SUB-PARTITION BOT SIDE
Place Near Balls
1720 mA
PLACE BELOW GPU
25+25 mA
Near VRAM
orignal footprint:nb_bga_84p_31_512x394_share 0315-00BB000
DDR2: VREF = 0.5 * FBVDDQ
DDR3: VREF = 0.7 * FBVDDQ
GPU Internal VREF R7604,R7605,C7617,C7616 no-stuff
PEGATRON
PEGATRON COMPUTER INC
Title : F/B A GPU
Engineer: <OrgAddr1>
Project Name F83Vf
P/N <OrgAddr2>
Rev 1.1
Date: Thursday, July 16, 2009
Sheet 76 of 100

BOT SIDE

1720 mA

+1.8VS

U7001C

NB9P-GE2

Main source：
Hynix DDR2 64M*16 500Hz/1.8V
H5PS1G63EFR-20L(0315-00AZ000)

Second source：
SAMSUNG DDR2 64M*16 500Hz/1.8V
K4N1G164QQ-HC20(0315-002E0AS)

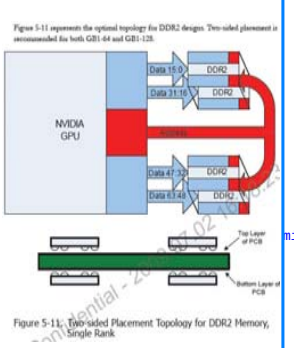


Figure 5-11. Two-sided Placement Topology for DDR2 Memory, Single Rank

Pins	Mapping Mode A	Pins	Mapping Mode A
FBx_CMD	CS0/CS1	FBx_CMD15	RAS
FBx_CMD0	A3[1] (low)	FBx_CMD16	A11
FBx_CMD1	A0	FBx_CMD17	A10
FBx_CMD2	A2 (low)	FBx_CMD18	BA1
FBx_CMD3	A1	FBx_CMD19	A8
FBx_CMD4	A3 (high)	FBx_CMD20	A9
FBx_CMD5	A4 (high)	FBx_CMD21	A6
FBx_CMD6	A5 (high)	FBx_CMD22	A5 (low)
FBx_CMD7	CS1/BA2	FBx_CMD23	A7
FBx_CMD8	CS0	FBx_CMD24	A4 (low)
FBx_CMD9	WE	FBx_CMD25	CAS
FBx_CMD10	BA0	FBx_CMD26	A13
FBx_CMD11	CKE	FBx_CMD27	BA2
FBx_CMD12	RST/ODT	FBx_CMD28	RFU0
FBx_CMD13	A2 (high)	FBx_CMD29	RFU1
FBx_CMD14	A12	FBx_CMD30	RFU2

LOWER SUB-PARTITION TOP SIDE

U7701

H5PS1G63EFR-S6

mini-bus

LOWER SUB-PARTITION BOT SIDE

orignal footprint:nb_bga_84p_31_512x394_share

U7702

H5PS1G63EFR-S6

mini-bus

UPPER SUB-PARTITION BOT SIDE

U7703

H5PS1G63EFR-S6

mini-bus

UPPER SUB-PARTITION TOP SIDE

U7704

H5PS1G63EFR-S6

mini-bus

25+25 mA

+1.1VS

L7701 180Ohm/100Mhz

Near VRAM

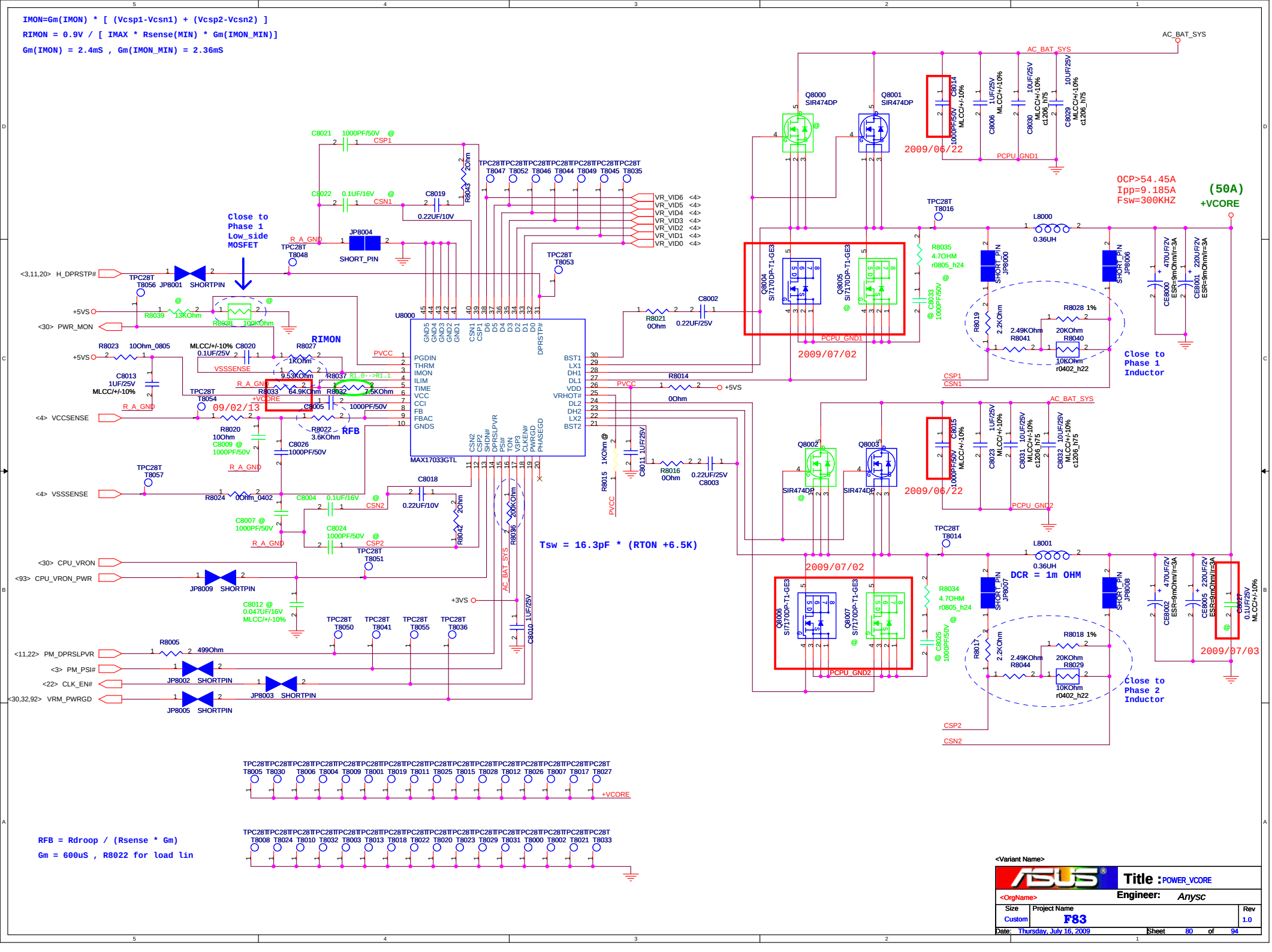
	FBVDDQ	FBCAL_PD_GND	FBCAL_PU_GND	FBCAL_thrm_GND
DDRII	1.8V	30.1 ohm	36.5 ohm	40.2 ohm

PEGATRON	Title :	F/B C GPU	
PEGATRON COMPUTER INC	Engineer:	<OrgAddr1>	
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 77 of 100		

IMON=Gm(IMON) * [(Vcsp1-Vcsn1) + (Vcsp2-Vcsn2)]

RIMON = 0.9V / [IMAX * Rsense(MIN) * Gm(IMON_MIN)]

Gm(IMON) = 2.4mS , Gm(IMON_MIN) = 2.36mS



RFB = Rdroop / (Rsense * Gm)

Gm = 600uS , R8022 for load lin

<Variant Name>

<OrgName>	Title : POWER_VCORE	
	Engineer: Anysc	
Size: Custom	Project Name: F83	Rev: 1.0
Date: Thursday, July 16, 2009	Sheet 80 of 94	

SKIP:
GND : DEM operation;
REF : Ultrasonic Mode operation;
VCC : PWM operation.

TON:(5V/3.3V)
VCC:(200kHz/250kHz)
REF:(300kHz/375kHz)
GND:(400kHz/500kHz)

VENLDO:
Rising Edge:Max:2V;Typ:1.6V;Min:1.2V
Falling Edge:Max:1.06V;Typ:1V;Min:0.94V

AC_BAT_SYS

<82,83,85,91,93> SUSB#_PWR
09/04/17
R8123 0Ohm r0402_h16
SKIP#
R8105 0Ohm r0402_h16 @

2009/06/22
R8128 10Ohm
+5VAO
R8139 0Ohm @
C8115 1UF/6.3V MLCC/+/-10% @
R8126 100KOhm 5%
R8114 0Ohm
GND_17020
R8141 0Ohm @
C8113 1UF/6.3V MLCC/+/-10%
R8122 @ 0Ohm
R8117 0Ohm
C8112 MLCC/+/-10% 0.1UF/25V
R8146 @ 150KOhm
C8108 4.7UF/6.3V MLCC/+/-10%
C8109 0.22UF/10V
R8142 0Ohm
C8102 0.1UF/25V
C8117 10UF/25V_1206
Q8102 SI4134DY-T1-GE3

Iin=2.99A
C8118 10UF/25V_1206
C8105 0.1UF/25V MLCC/+/-10%
Q8100 SI4134DY-T1-GE3
Iin=2.78A

OCP>8.7A
4.966V~~5.217V
Ipp=3.72A LIR=0.62
Fsw=300KHZ

OCP>7.9A
3.285V~~3.375V
Ipp=2.2A LIR=0.37
Fsw=375KHZ

+5VO
(Max:5.68A)
(5.99A)
DCR:Typ=28mOhm;Max=30mOhm
+5VSUS
(0.31A)
JP8100 @
1MM_OPEN_5MIL
L8100 3.3UH Irat=6A
40mil
10mil
Separate
U8100A
BYP VOUT1 FB1 ILIM1 PGOOD1 EN1 UGATE1 PHASE1
NC2 LDO NC3 NC1 ENLDO VCC TON REF
GND2 FB2 ILIM2 VOUT2 SKIP# PGOOD2 EN2 UGATE2 PHASE2
BOOT1 LGATE1 PGND SECFB GND1 LGATE2 BOOT2
+3VO_FB
R8124 330KOHM
R8125 330KOHM
SUS_PWRGD
ENBL
SKIP#
R8113 0Ohm
+5VAO
OCP Set
R8115 2.2Ohm 5% r1206
C8103 150UF/16V ESR=30mOHM/1400mA
CE8101 100UF/6.3V
C8103 1UF/10V
JP8105 SHORT_PIN
JP8109 SHORT_PIN
C8125 1500PF/50V MLCC/+/-10% @
C8110 0.1UF/25V MLCC/+/-10%
RT8206AGQW
R8120 0Ohm
R8119 0Ohm
C8111 MLCC/+/-10% 0.1UF/25V
DL1
(5V:300kHz)
(3.3V:375kHz)
Q8101 SI4134DY-T1-GE3
Q8103 SI4134DY-T1-GE3
R8116 2.2Ohm 5% r1206 @
JP8104 SHORT_PIN
C8126 1500PF/50V MLCC/+/-10% @
C8100 1UF/10V
2009/06/18
2009/06/22
2009/06/18
2009/06/18
2009/06/22

(Typ: Rdson = 14.5m OHM)
(Max: Rdson = 17.5m OHM)
FB1=2V(T=1.25%)
(Typ: Rdson = 14.5m OHM)
(Max: Rdson = 17.5m OHM)
FB1=2V(T=1.25%)

L8101 3.3UH Irat=6A
(6.432A)
+3VO
(MAX:5.712A)
JP8101 @
1MM_OPEN_5MIL
+3VA
(0.22A)

+5VAO
JP8108 @
1MM_OPEN_5MIL
+5VA
C8134 39PF/50V @
R8108 30.9KOhm 1%
C8136 0.1UF/25V @
R8109 20KOhm 1%
GND_17020
C8137 39PF/50V @
C8114 1UF/6.3V MLCC/+/-10%
SECFB
R8127 200KOhm
+15VO
*SECFB:2V(T=4%)
R8132 39KOHM
JP8110
SHORT_PIN
<22,30,92> SUS_PWRGD
<91> 5VO_ENBL
U8100B
GND3 GND4 GND5 GND6
RT8206AGQW
R8112 13.3KOhm 1%
C8135 39PF/50V
C8138 0.1UF/25V @
R8111 20KOhm 1% @
09/05/18

2009/07/02

+12VSUS
+5VO
D8104 BAT54S
C8121 0.1UF/25V MLCC/+/-10%
2009/06/22
20mil
DL1
C8120 0.1UF/25V MLCC/+/-10%
2009/06/22
D8103 BAT54S
C8122 1UF/25V MLCC/+/-10%
+10VO
C8123 1UF/25V MLCC/+/-10%
(Max:0.02A)
+15VO
JP8106 @
1MM_OPEN_5MIL
+12VSUS
C8124 1UF/25V MLCC/+/-10%
VOUT:Typ.=12.256V;Max.=12.962V;Min.=11.571V;T=5.76%

TPC26TPC26TPC26TPC26TPC26
+5VO TB110 TB103 TB114 TB120
+5VSUS TB134 TB132 TB135 TB121
+3VO TB117 TB107 TB109 TB122
TB104 TB108 TB116 TB126
TB112 TB119 TB101 TB130

TOTAL COUNT : 38 PCS

<Variant Name>
Title : POWER_SYSTEM
<OrgName>
Engineer: Anysc
Size Custom
Project Name F83
Rev 1.0
Date: Thursday, July 16, 2009
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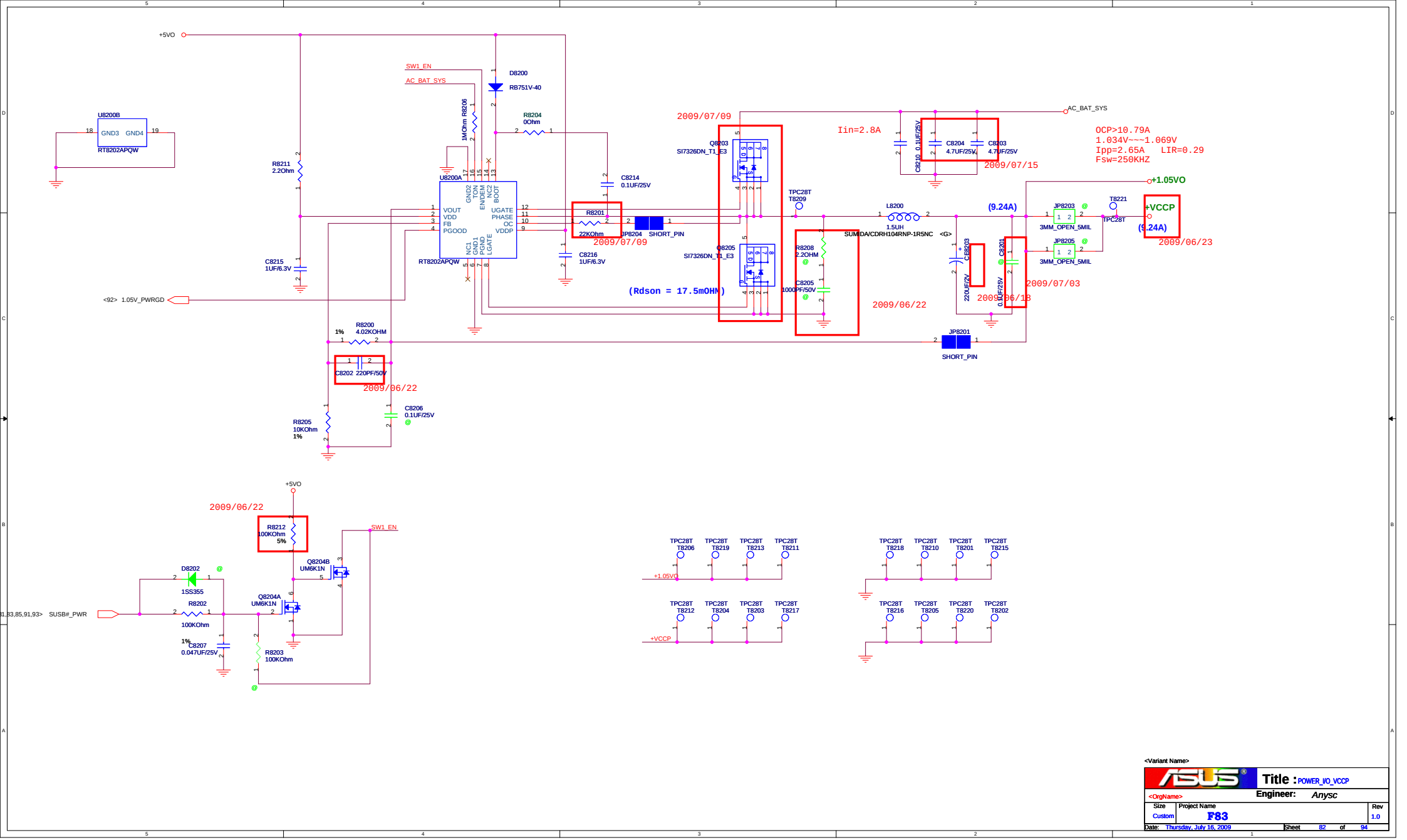
+5VO
SW1_EN
AC_BAT_SYS
D8200
RB751V-40
R8204
0Ohm
1MOhm R8206
U8200B
GND3 GND4
RT8202APQW
R8211
2.2Ohm
U8200A
VOUT
VDD
FB
PGOOD
GND2
TON
ENSOFT
NC2
BOOT
UGATE
PHASE
OC
VDDP
NC1
GND1
LGND
LGATE
RT8202APQW
C8214
0.1UF/25V
R8201
22KOhm
JP8204
SHORT_PIN
C8216
1UF/6.3V
C8215
1UF/6.3V
<92> 1.05V_PWRGD
2009/07/09
Q8203
SI7326DN_T1_E3
Q8205
SI7326DN_T1_E3
(Rdson = 17.5mOHM)
TPC28T
T8209
R8208
2.2OHM
C8205
1000PF/50V
2009/06/22
Iin=2.8A
C8210 0.1UF/25V
C8204
4.7UF/25V
C8203
4.7UF/25V
2009/07/15
AC_BAT_SYS
OCP>10.79A
1.034V~~~1.069V
Ipp=2.65A LIR=0.29
FSw=250KHZ
+1.05VO
L8200
1.5UH
SUMIDA/CDRH104RNP-1R5NC <G>
(9.24A)
C8209
220UF/2V
C8201
0.1UF/25V
2009/07/03
2009/06/18
JP8203
3MM_OPEN_5MIL
JP8205
3MM_OPEN_5MIL
T8221
TPC28T
+VCCP
(9.24A)
2009/06/23
JP8201
SHORT_PIN
R8200
1% 4.02KOHM
C8202 220PF/50V
2009/06/22
R8205
10KOhm
1%
C8206
0.1UF/25V
+5VO
2009/06/22
R8212
100KOhm
5%
SW1_EN
D8202
1SS355
Q8204B
UM6K1N
Q8204A
UM6K1N
R8202
100KOhm
1%
C8207
0.047UF/25V
R8203
100KOhm
<1,33,85,91,93> SUSB#_PWR
TPC28T T8206
TPC28T T8219
TPC28T T8213
TPC28T T8211
+1.05VO
TPC28T T8212
TPC28T T8204
TPC28T T8203
TPC28T T8217
+VCCP
TPC28T T8218
TPC28T T8210
TPC28T T8201
TPC28T T8215
TPC28T T8216
TPC28T T8205
TPC28T T8220
TPC28T T8202
<Variant Name>
Title : POWER_I/O_VCCP
<OrgName>
Engineer: Anysc
Size Custom
Project Name F83
Rev 1.0
Date: Thursday, July 16, 2009
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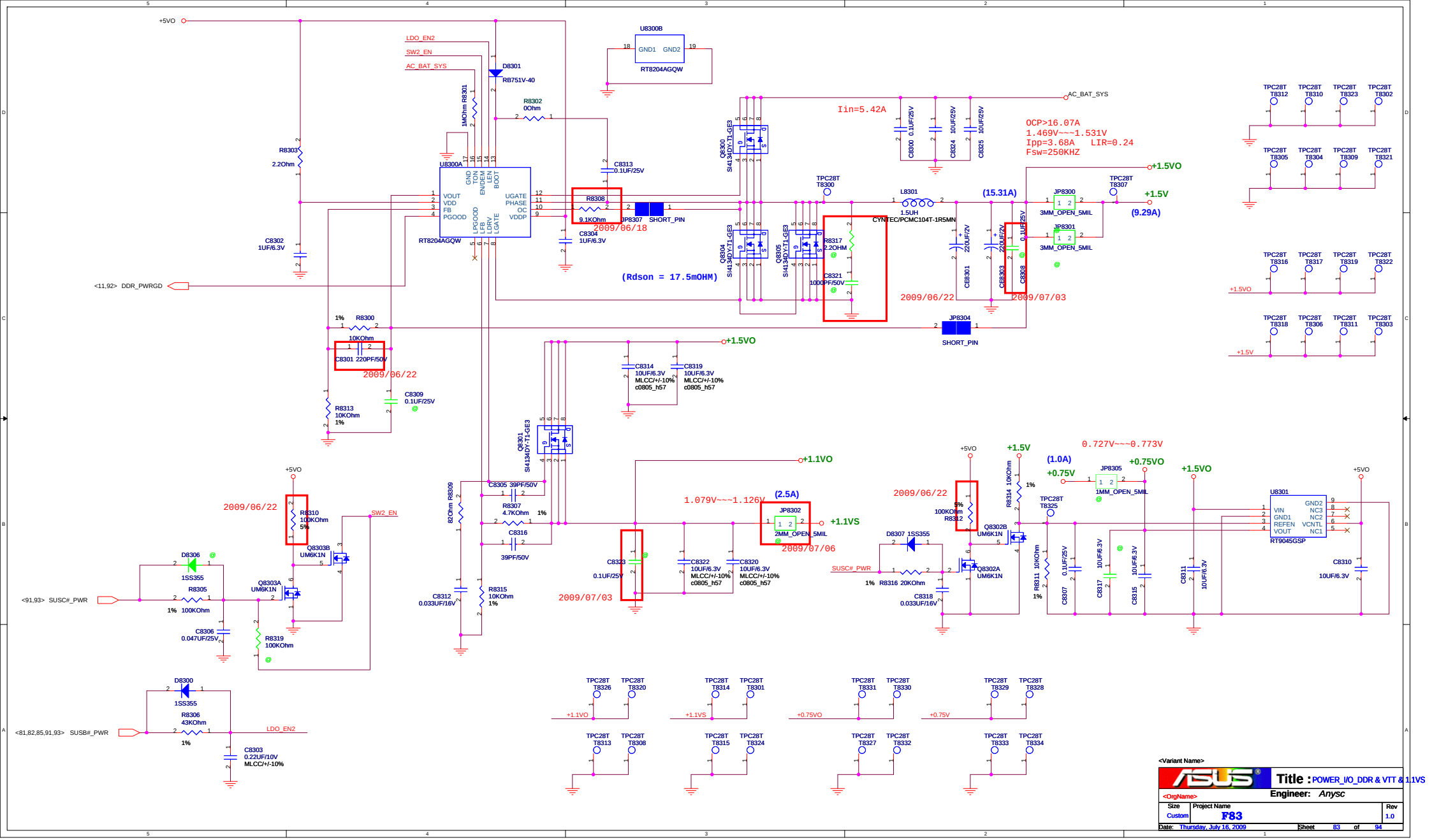
+5VO
LDO_EN2
SW2_EN
AC_BAT_SYS
D8301
RB751V-40
R8302
0Ohm
1MOhm R8301
R8303
2.2Ohm
U8300A
RT8204AGQW
VOUT
VDD
FB
PGOOD
GND
TON
ENDEM
LDRV
BOOT
UGATE
PHASE
OC
VDDP
LPGOOD
LDRV
LGATE
C8302
1UF/6.3V
C8313
0.1UF/25V
R8308
9.1KOhm
JP8307
SHORT_PIN
C8304
1UF/6.3V
2009/06/18
U8300B
GND1
GND2
RT8204AGQW
Q8300
SI4134DY-T1-GE3
Q8304
SI4134DY-T1-GE3
Q8305
SI4134DY-T1-GE3
Iin=5.42A
C8300 0.1UF/25V
C8324 10UF/25V
C8325 10UF/25V
OCP>16.07A
1.469V~~~1.531V
Ipp=3.68A LIR=0.24
Fsw=250KHZ
+1.5VO
TPC28T T8300
L8301
1.5UH
CYNTEC/PCMC104T-1R5MN
(15.31A)
JP8300
3MM_OPEN_5MIL
TPC28T T8307
+1.5V
(9.29A)
JP8301
3MM_OPEN_5MIL
C8303 220UF/2V
C8308 0.1UF/25V
C8301 220UF/2V
R8317
2.2OHM
C8321
1000PF/50V
2009/06/22
2009/07/03
(Rdson = 17.5mOHM)
JP8304
SHORT_PIN
<11,92> DDR_PWRGD
1% R8300
10KOhm
C8301 220PF/50V
2009/06/22
R8313
10KOhm
1%
C8309
0.1UF/25V
C8314
10UF/6.3V
MLCC/+/-10%
c0805_h57
C8319
10UF/6.3V
MLCC/+/-10%
c0805_h57
+1.5VO
Q8301
SI4134DY-T1-GE3
+1.1VO
C8305 39PF/50V
R8307
4.7KOhm 1%
C8316
39PF/50V
82Ohm R8309
C8312
0.033UF/16V
R8315
10KOhm
1%
1.079V~~~1.126V
(2.5A)
JP8302
2MM_OPEN_5MIL
+1.1VS
2009/07/06
C8333
0.1UF/25V
2009/07/03
C8322
10UF/6.3V
MLCC/+/-10%
c0805_h57
C8320
10UF/6.3V
MLCC/+/-10%
c0805_h57
+5VO
2009/06/22
R8310
100KOhm
5%
SW2_EN
Q8303B
UM6K1N
D8306
1SS355
<91,93> SUSC#_PWR
R8305
1% 100KOhm
Q8303A
UM6K1N
C8306
0.047UF/25V
R8319
100KOhm
D8300
1SS355
<81,82,85,91,93> SUSB#_PWR
R8306
43KOhm
1%
LDO_EN2
C8303
0.22UF/10V
MLCC/+/-10%
+5VO
+1.5V
0.727V~~~0.773V
(1.0A)
+0.75V
JP8305
1MM_OPEN_5MIL
+0.75VO
+1.5VO
2009/06/22
R8314 10KOhm
1%
100KOhm
5%
R8312
Q8302B
UM6K1N
D8307 1SS355
SUSC#_PWR
1% R8316 20KOhm
C8318
0.033UF/16V
Q8302A
UM6K1N
R8311 10KOhm
1%
C8307 0.1UF/25V
C8317 10UF/6.3V
C8315 10UF/6.3V
C8311 10UF/6.3V
U8301
RT9045GSP
VIN
GND1
REFEN
VOUT
GND2
NC3
NC2
VCNTL
NC1
C8310
10UF/6.3V
TPC28T T8312
TPC28T T8310
TPC28T T8323
TPC28T T8302
TPC28T T8305
TPC28T T8304
TPC28T T8309
TPC28T T8321
TPC28T T8316
TPC28T T8317
TPC28T T8319
TPC28T T8322
TPC28T T8318
TPC28T T8306
TPC28T T8311
TPC28T T8303
TPC28T T8326
TPC28T T8320
TPC28T T8313
TPC28T T8308
TPC28T T8314
TPC28T T8301
TPC28T T8315
TPC28T T8324
TPC28T T8331
TPC28T T8330
TPC28T T8327
TPC28T T8332
TPC28T T8329
TPC28T T8328
TPC28T T8333
TPC28T T8334
<Variant Name>
Title : POWER_I/O_DDR & VTT & 1.1VS
<OrgName>
Engineer: Anysc
Size Custom
Project Name F83
Rev 1.0
Date: Thursday, July 16, 2009
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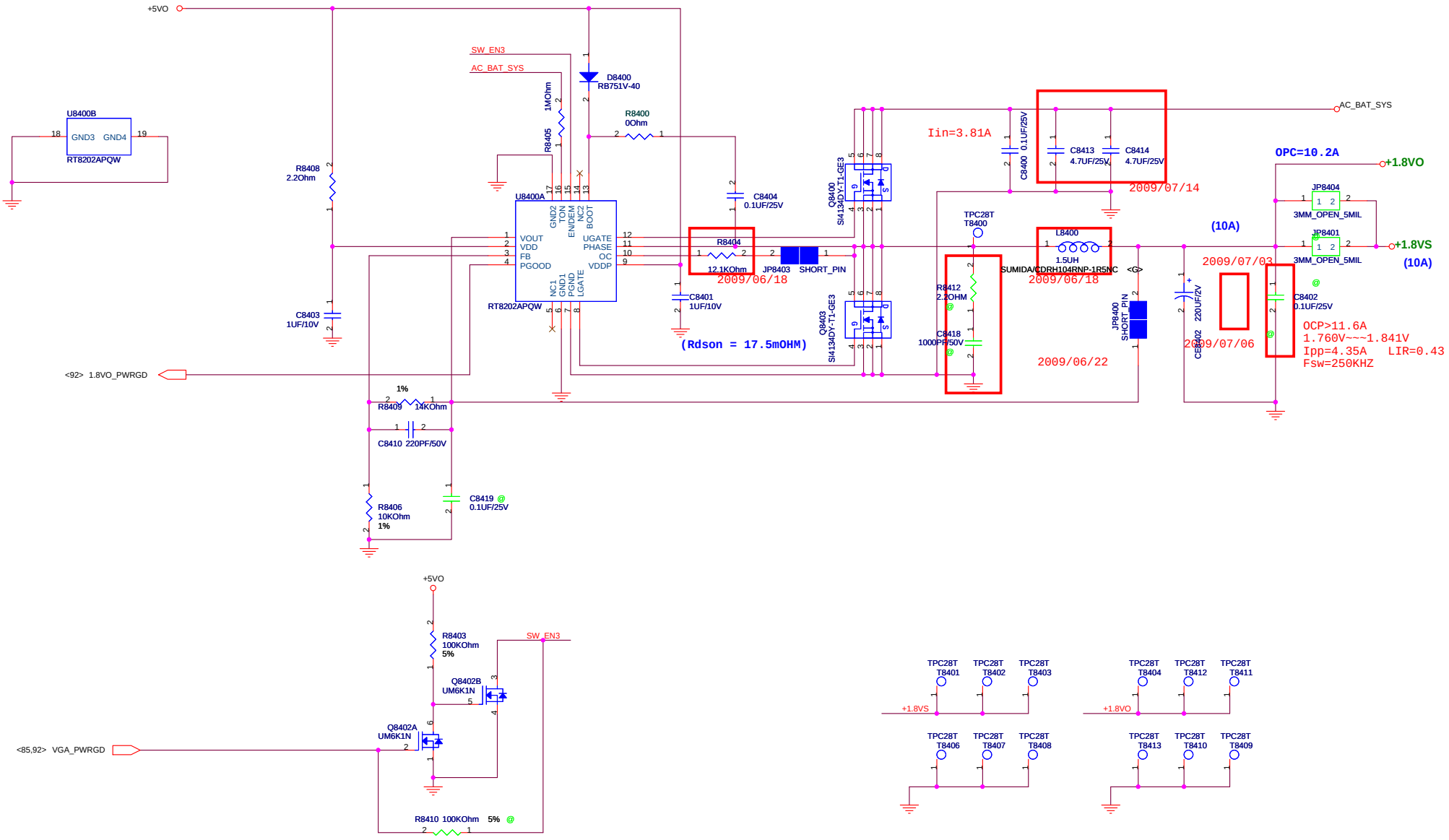
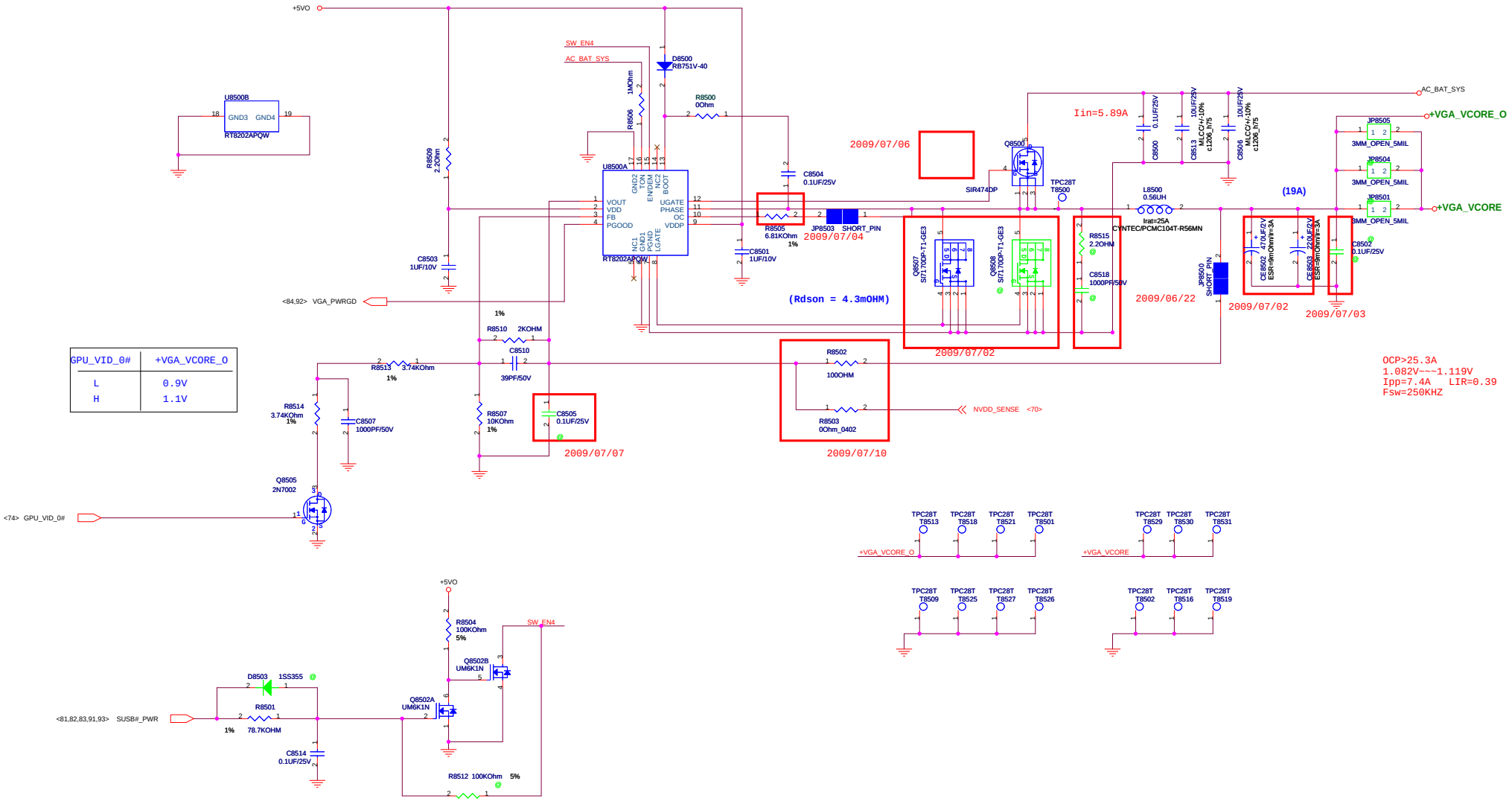


<Variant Name>

Title : POWER_I/O_1.8VS		
<OrgName>	Engineer: Anysc	
Size: Custom	Project Name: F83	Rev: 1.0
Date: Thursday, July 16, 2009	Sheet 84 of 94	



<Variant Name>

ASUS

Title : POWER_VGA_VCORE

<OrgName>

Engineer: Anysc

Size	Project Name	Rev
C	F83	1.0

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<Variant Name>

Title : N/A

<OrgName>

Engineer: Anysc

Size	Project Name	Rev
Custom	F83	1.0

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<Variant Name>

Title : N/A

<OrgName>

Engineer: Anysc

Size	Project Name	Rev
C	F83	1.0

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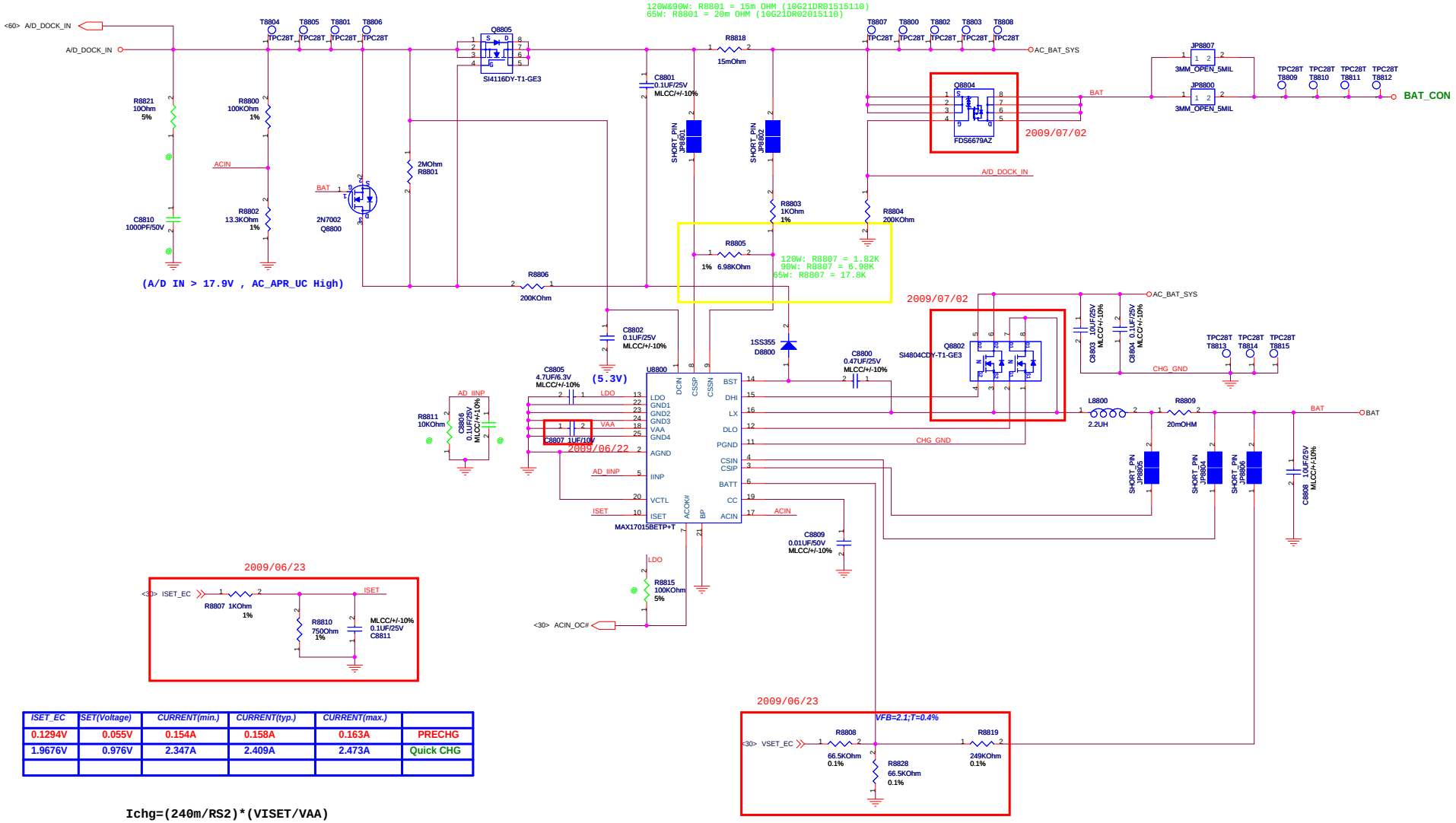

ISET_EC	ISET(Voltage)	CURRENT(min.)	CURRENT(typ.)	CURRENT(max.)	
0.1294V	0.055V	0.154A	0.158A	0.163A	PRECHG
1.9676V	0.976V	2.347A	2.409A	2.473A	Quick CHG

Ichg=(240m/RS2)*(VISET/VAA)
Ichg=(240m/20m)*(0.055/4.2)=0.157A
Ichg=(240m/20m)*(0.865/4.2)=2.4714A

VCTL connect to GND,VFB=2.1V
VBAT=2.1*(R8819+R8828)/R8828

VSET_EC	BAT(min.)	BAT(typ.)	BAT(max.)
1.3948V	12.511V	12.604V	12.696V

12.641V(min)<VBAT-12.515(Typ)<12.768V(Max)

<Variant Name>

Title : POWER_CHARGER
<OrgName>
Engineer: Anysc

Size	Project Name	Rev
C	F83	1.0

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<variant_name><Variant Name></variant_name>

Title : N/A

<OrgName>

Engineer: Anysc

Size	Project Name	Rev
Custom	F83	1.0

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BATTERY IN DETECT

2009/07/08
delete batt detect

<Variant Name>

Title : POWER_DETECT

<OrgName>

Engineer: Anysc

Size	Project Name	Rev
Custom	F83	1.0

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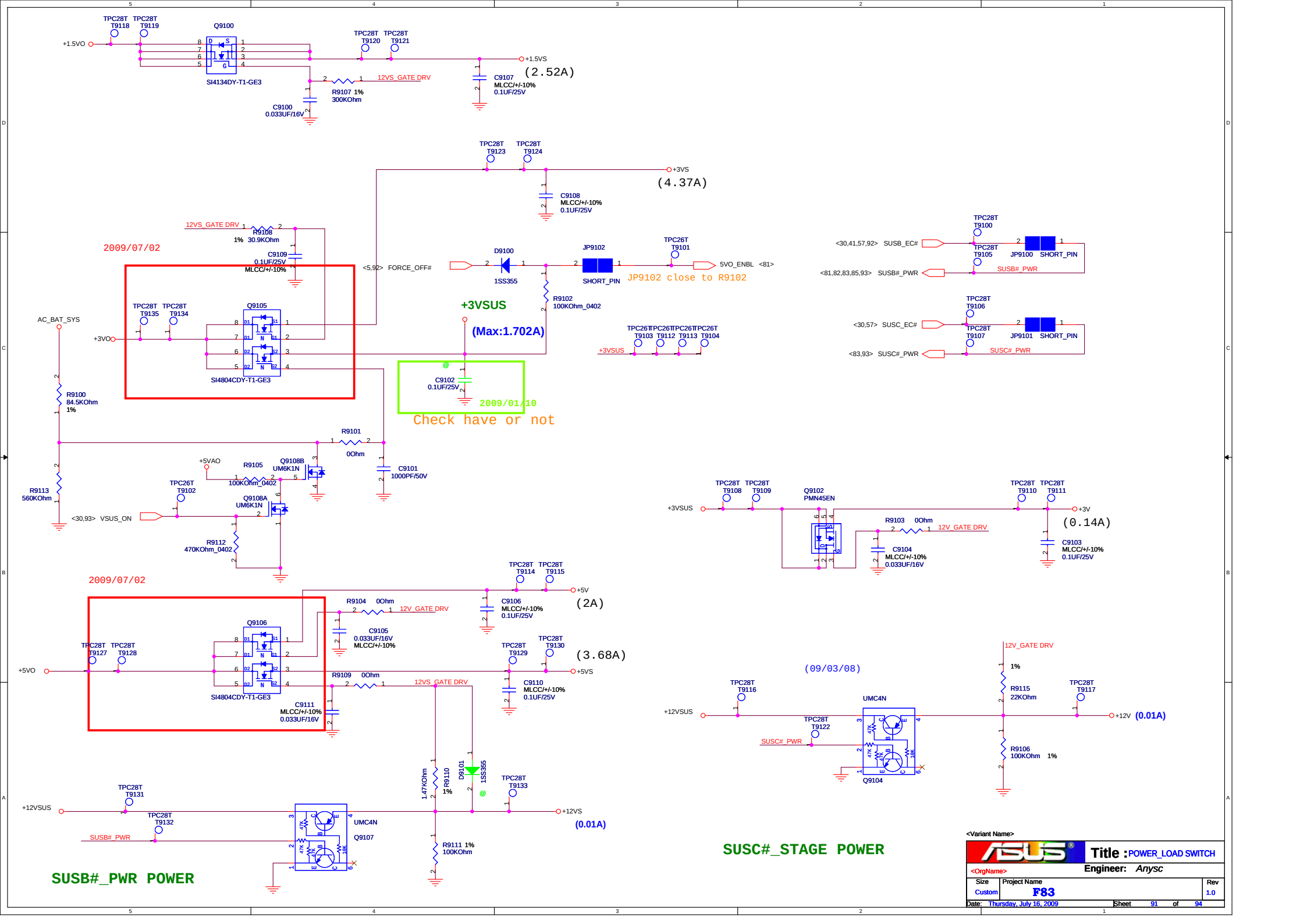
+1.5VO
TPC28T T9118
TPC28T T9119
Q9100
SI4134DY-T1-GE3
TPC28T T9120
TPC28T T9121
+1.5VS
(2.52A)
12VS_GATE DRV
R9107 1%
300KOhm
C9100
0.033UF/16V
C9107
MLCC/+/-10%
0.1UF/25V
+3VS
(4.37A)
TPC28T T9123
TPC28T T9124
C9108
MLCC/+/-10%
0.1UF/25V
2009/07/02
R9108
1% 30.9KOhm
C9109
0.1UF/25V
MLCC/+/-10%
<5,92> FORCE_OFF#
D9100
1SS355
JP9102
SHORT_PIN
TPC26T T9101
5VO_ENBL <81>
JP9102 close to R9102
R9102
100KOhm_0402
+3VSUS
(Max:1.702A)
TPC26T T9103
TPC26T T9112
TPC26T T9113
TPC26T T9104
+3VSUS
C9102
0.1UF/25V
2009/01/10
Check have or not
AC_BAT_SYS
+3VO
TPC28T T9135
TPC28T T9134
Q9105
SI4804CDY-T1-GE3
R9100
84.5KOhm
1%
R9101
0Ohm
C9101
1000PF/50V
+5VAO
R9105
100KOhm_0402
Q9108B
UM6K1N
Q9108A
UM6K1N
TPC26T T9102
<30,93> VSUS_ON
R9113
560KOhm
R9112
470KOhm_0402
<30,41,57,92> SUSB_EC#
TPC28T T9100
TPC28T T9105
JP9100
SHORT_PIN
SUSB# PWR
<81,82,83,85,93> SUSB#_PWR
<30,57> SUSC_EC#
TPC28T T9106
TPC28T T9107
JP9101
SHORT_PIN
SUSC# PWR
<83,93> SUSC#_PWR
+3VSUS
TPC28T T9108
TPC28T T9109
Q9102
PMN45EN
R9103 0Ohm
12V_GATE DRV
C9104
MLCC/+/-10%
0.033UF/16V
TPC28T T9110
TPC28T T9111
+3V
(0.14A)
C9103
MLCC/+/-10%
0.1UF/25V
2009/07/02
+5VO
TPC28T T9127
TPC28T T9128
Q9106
SI4804CDY-T1-GE3
R9104 0Ohm
12V_GATE DRV
C9105
0.033UF/16V
MLCC/+/-10%
TPC28T T9114
TPC28T T9115
+5V
(2A)
C9106
MLCC/+/-10%
0.1UF/25V
R9109 0Ohm
12VS_GATE DRV
C9111
MLCC/+/-10%
0.033UF/16V
TPC28T T9129
TPC28T T9130
+5VS
(3.68A)
C9110
MLCC/+/-10%
0.1UF/25V
+12VSUS
TPC28T T9131
TPC28T T9132
SUSB# PWR
UMC4N
Q9107
1.47KOhm
R9110
1%
D9101
1SS355
TPC28T T9133
+12VS
(0.01A)
R9111 1%
100KOhm
SUSB#_PWR POWER
(09/03/08)
+12VSUS
TPC28T T9116
TPC28T T9122
SUSC# PWR
UMC4N
Q9104
12V_GATE DRV
1%
R9115
22KOhm
TPC28T T9117
+12V
(0.01A)
R9106
100KOhm
1%
SUSC#_STAGE POWER
<Variant Name>
Title : POWER_LOAD SWITCH
<OrgName>
Engineer: Anysc
Size
Custom
Project Name
F83
Rev
1.0
Date: Thursday, July 16, 2009
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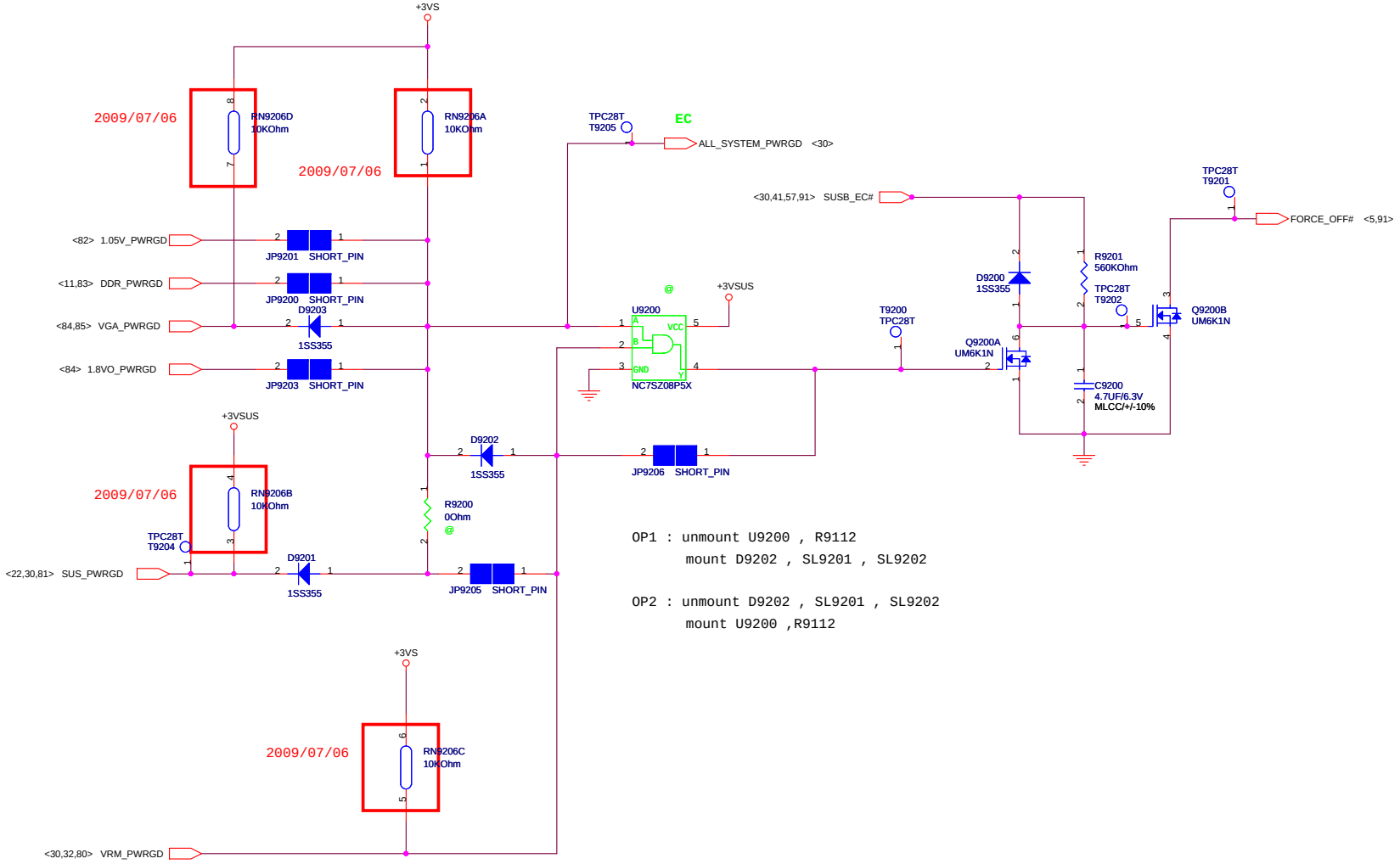
POWER GOOD DETECTER



OP1 : unmount U9200 , R9112
mount D9202 , SL9201 , SL9202

OP2 : unmount D9202 , SL9201 , SL9202
mount U9200 ,R9112

<Variant Name>

<OrgName>	Title : POWER_PROTECT	
	Engineer: Anysc	
Size: Custom	Project Name: F83	Rev: 1.0
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FOR POWER TEST

+3VA → +3VA <20,22,30,45,57,60,81>

+3VSUS → +3VSUS <20,21,22,23,24,30,33,37,45,53,56,91,92>

+5VSUS → +5VSUS <23,56,81>

+12VSUS → +12VSUS <24,81,91>

+5VO → +5VO <81,82,83,84,85,91>

+3VO → +3VO <81,91>

+1.05VO → +1.05VO <82>

+1.5VO → +1.5VO <83,91>

+0.75VO → +0.75VO <83>

+1.8VO → +1.8VO <84>

+1.1VO → +1.1VO <83>

+VGA_VCORE_O → +VGA_VCORE_O <85>

+3V → +3V <21,33,41,44,53,57,61,63,91>

+5V → +5V <9,31,44,45,52,57,91>

+12V → +12V <37,91>

+1.5V → +1.5V <7,8,9,11,13,14,57,83>

+3VS → +3VS <3,7,8,11,14,15,22,23,24,29,30,32,36,40,41,44,45,46,48,50,51,53,56,57,70,72,74,80,91,92>

+12VS → +12VS <24,40,45,48,57,91>

+5VS → +5VS <23,31,36,46,48,50,51,56,57,80,91>

+1.8VS → +1.8VS <57,73,76,77,84>

+1.5VS → +1.5VS <4,14,23,41,53,57,91>

+VCCP → +VCCP <3,4,5,10,11,13,14,20,23,29,57,82>

+0.75V → +0.75V <7,8,11,83>

+1.1VS → +1.1VS <57,70,72,73,76,77,83>

+VGA_VCORE → +VGA_VCORE <75,85>

+VCORE → +VCORE <4,5,80>

AC_BAT_SYS → AC_BAT_SYS <45,80,81,82,83,84,85,88,91>

BAT → BAT <88>

BAT_CON → BAT_CON <60,88>

+3VO → JP9300 @ (1 1 2 2) SGL_JUMP → CPU_VRON_PWR <80>

+3VO → JP9301 @ (1 1 2 2) SGL_JUMP → SUSB#_PWR → SUSB#_PWR <81,82,83,85,91>

+3VO → JP9302 @ (1 1 2 2) SGL_JUMP → SUSC#_PWR → SUSC#_PWR <83,91>

+3VO → JP9303 @ (1 1 2 2) SGL_JUMP → VSUS_ON <30,91>

<Variant Name>

<OrgName>	Title : POWER_SIGNAL	
	Engineer: Anysc	
Size: Custom	Project Name: F83	Rev: 1.0
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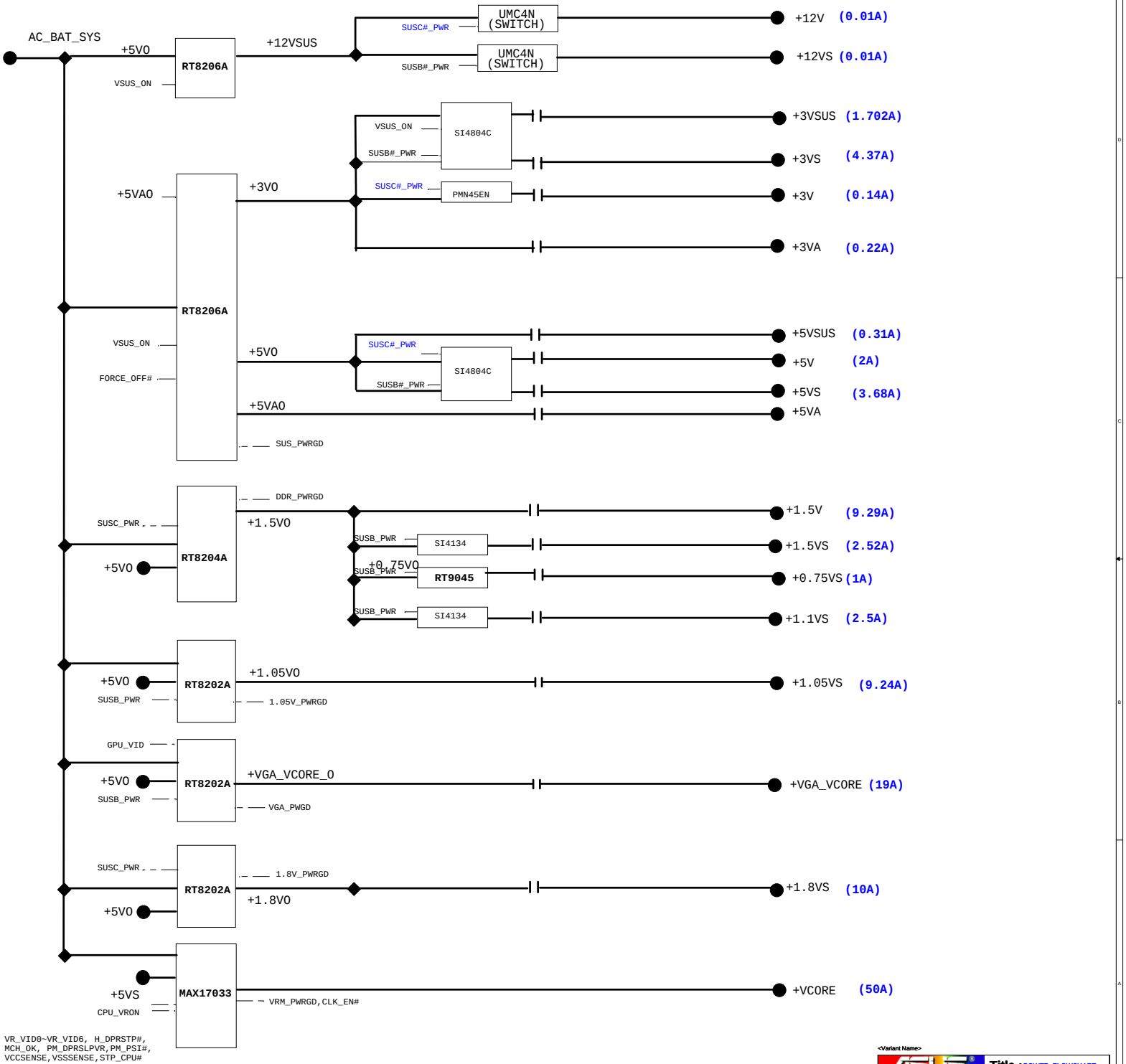

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Title : POWER_FLOWCHART

<OrgName>

Engineer: Anysc

Size	Project Name	Rev
Custom	F83	1.0

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