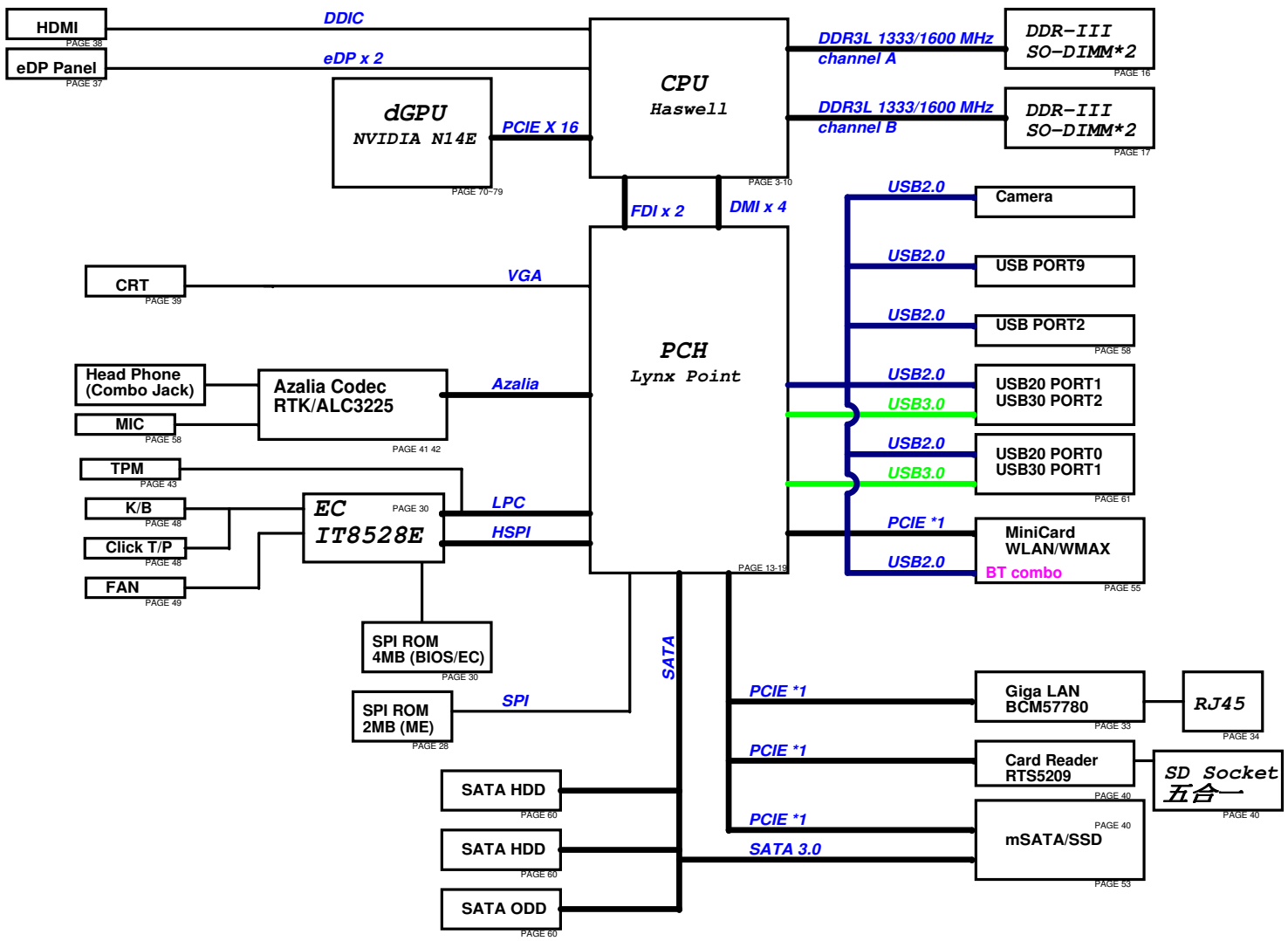
VA70HW BLOCK DIAGRAM



POWER

CPU VCORE PAGE 80
SYSTEM, +3V, +5V PAGE 81
+VCCP & +VCCP_VT PAGE 82
DDR & VTT PAGE 83
2.5V & 1.5VS &1.1VS PAGE 84
SMART CHARGER PAGE 88
POWER DETECT PAGE 90
LOAD SWITCH PAGE 91
POWER PROTECT PAGE 92

VGA POWER

GPU VCORE PAGE 80
+1.05VS_VGA
+3VS_VGA
+12VS_VGA
LOAD SWITCH PAGE 91
POWER PROTECT PAGE 92

Power Rails

Sleep State	RTC	VA	VSUS	VS
S0	ON	ON	ON	ON
S3	ON	ON	ON	OFF
S4	ON	ON	ON	OFF
S5/ AC	ON	ON	ON	OFF
S5/ DC	ON	ON	OFF	OFF

PCIe Port

PCIE_P1	CARDREADER
PCIE_P2	mSATA
PCIE_P3	Mini CARD (WLAN)
PCIE_P4	LAN
PCIE_P5	
PCIE_P6	

USB20 PORT

USB P00	External MB
USB P01	External MB
USB P02	External DB
USB P03	
USB P04	
USB P05	WiFi
USB P08	Camera
USB P09	External DB
USB P10	BT
USB P11	PCIE/mSATA
USB P12	
USB P13	

SATA PORT

SATA P0	HDD 1
SATA P1	
SATA P2	ODD
SATA P3	
SATA P4	mSATA
SATA P5	HDD 2

IO BOARD

USB PORT3	HP_OUT
USB PORT9	MIC IN

PWR BOARD

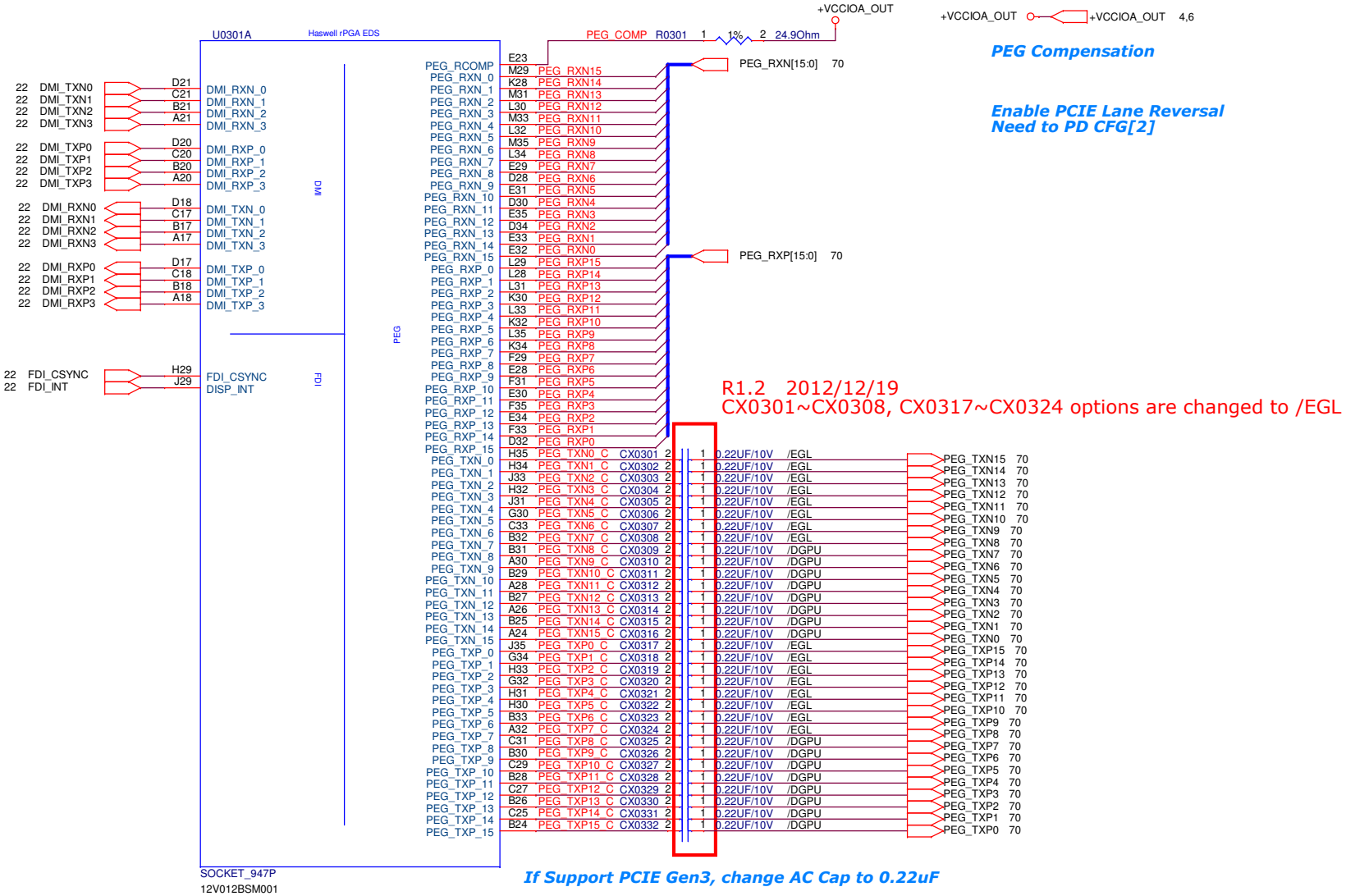
POWER Button
POWER LED
LID SW

PEGATRON Title : BLOCK DIAGRAM

BU1-RD Div.1-HW RD Dept.1 Engineer: Wing_Cheng

Size	Project Name	Rev
Custom	VA70_HW	1.0

Date: Monday, February 04, 2013 Sheet 1 of 96



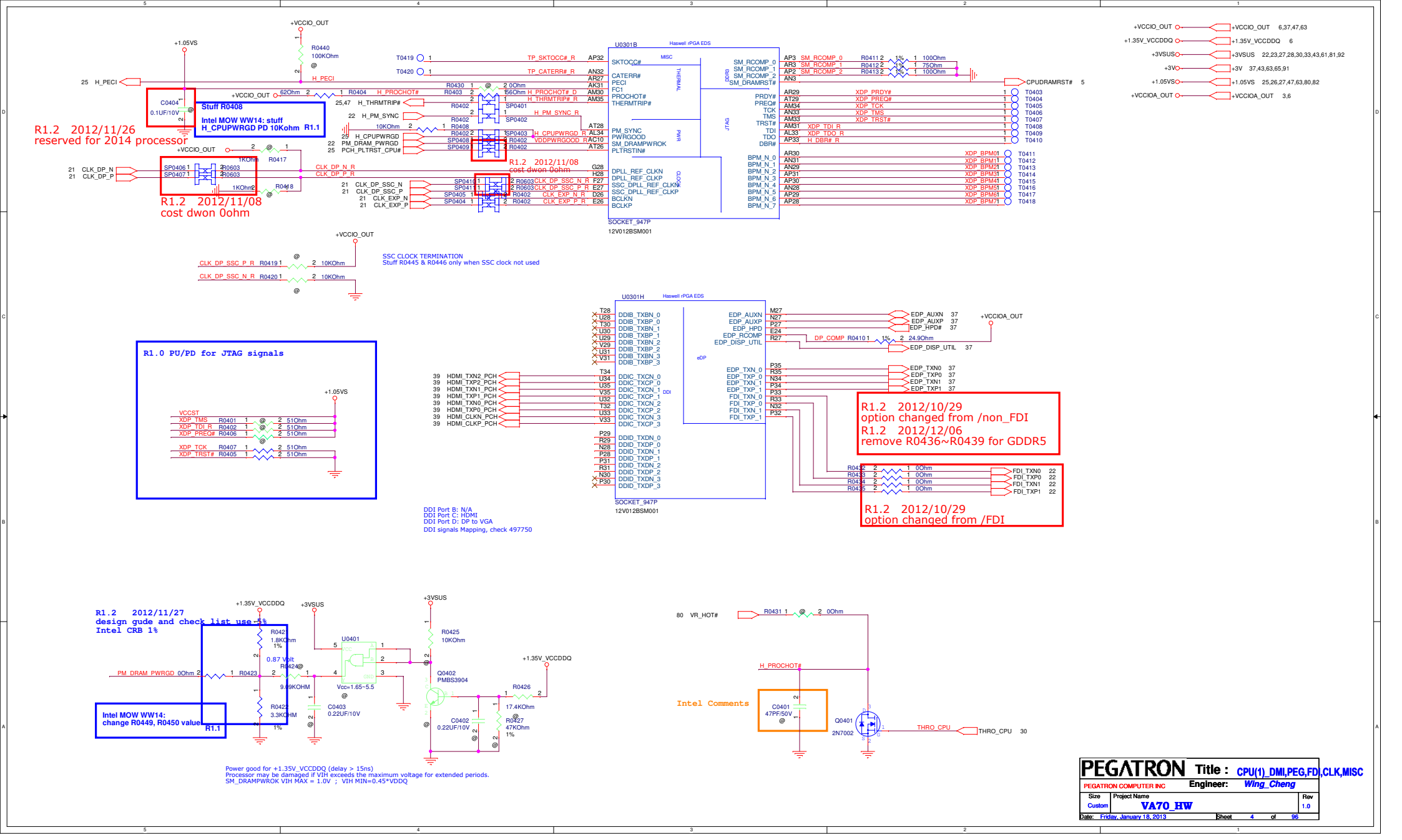
PEG Compensation

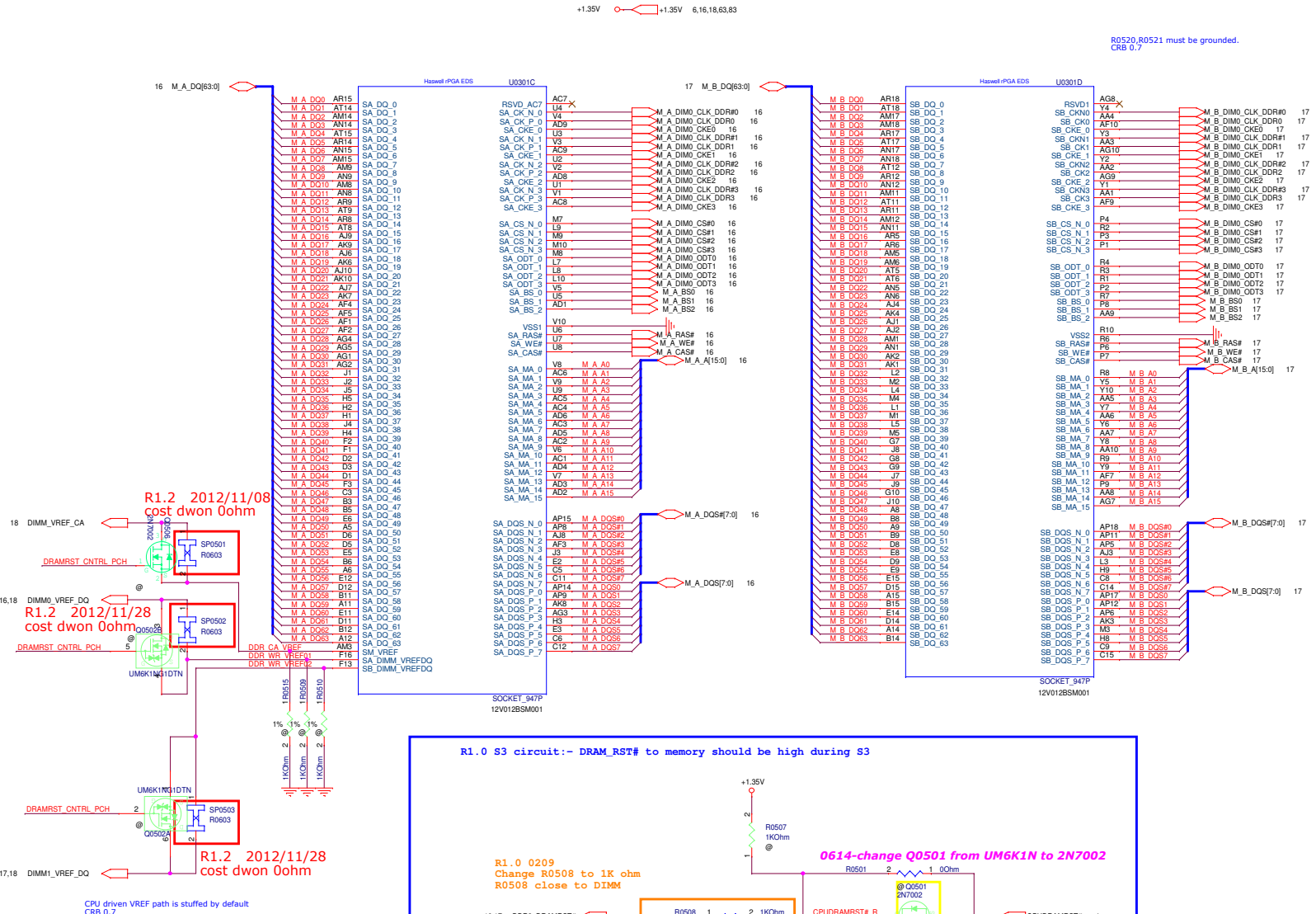
Enable PCIE Lane Reversal
Need to PD CFG[2]

R1.2 2012/12/19
CX0301~CX0308, CX0317~CX0324 options are changed to /EGL

If Support PCIE Gen3, change AC Cap to 0.22uF

PEGATRON	Title :	CPU(1)_DMI,PEG,FDI,CLK,MISC	
PEGATRON COMPUTER INC	Engineer:	*Wing_Cheng*	
Size: B	Project Name: VA70_HW		Rev: 1.0
Date: Friday, January 18, 2013	Sheet 3 of 96		


U0301B
Haswell rPGA EDS
SOCKET_947P
12V012BSM001
R1.2 2012/11/26
reserved for 2014 processor
Stuff R0408
Intel MOW WW14: stuff
H_CPUPWRGD PD 10Kohm R1.1
R1.2 2012/11/08
cost dwon 0ohm
R1.2 2012/11/08
cost dwon 0ohm
SSC CLOCK TERMINATION
Stuff R0445 & R0446 only when SSC clock not used
U0301H
Haswell rPGA EDS
SOCKET_947P
12V012BSM001
R1.0 PU/PD for JTAG signals
R1.2 2012/10/29
option changed from /non_FDI
R1.2 2012/12/06
remove R0436~R0439 for GDDR5
R1.2 2012/10/29
option changed from /FDI
DDI Port B: N/A
DDI Port C: HDMI
DDI Port D: DP to VGA
DDI signals Mapping, check 497750
R1.2 2012/11/27
design gude and check list use 5%
Intel CRB 1%
Intel MOW WW14:
change R0449, R0450 value
R1.1
Power good for +1.35V_VCCDDQ (delay > 15ns)
Processor may be damaged if VIH exceeds the maximum voltage for extended periods.
SM_DRAMPWROK VIH MAX = 1.0V ; VIH MIN=0.45*VDDQ
Intel Comments
PEGATRON
Title : CPU(1)_DMI,PEG,FDI,CLK,MISC
PEGATRON COMPUTER INC
Engineer: Wing_Cheng
Size Custom
Project Name VA70_HW
Rev 1.0
Date: Friday, January 18, 2013
Sheet 4 of 96



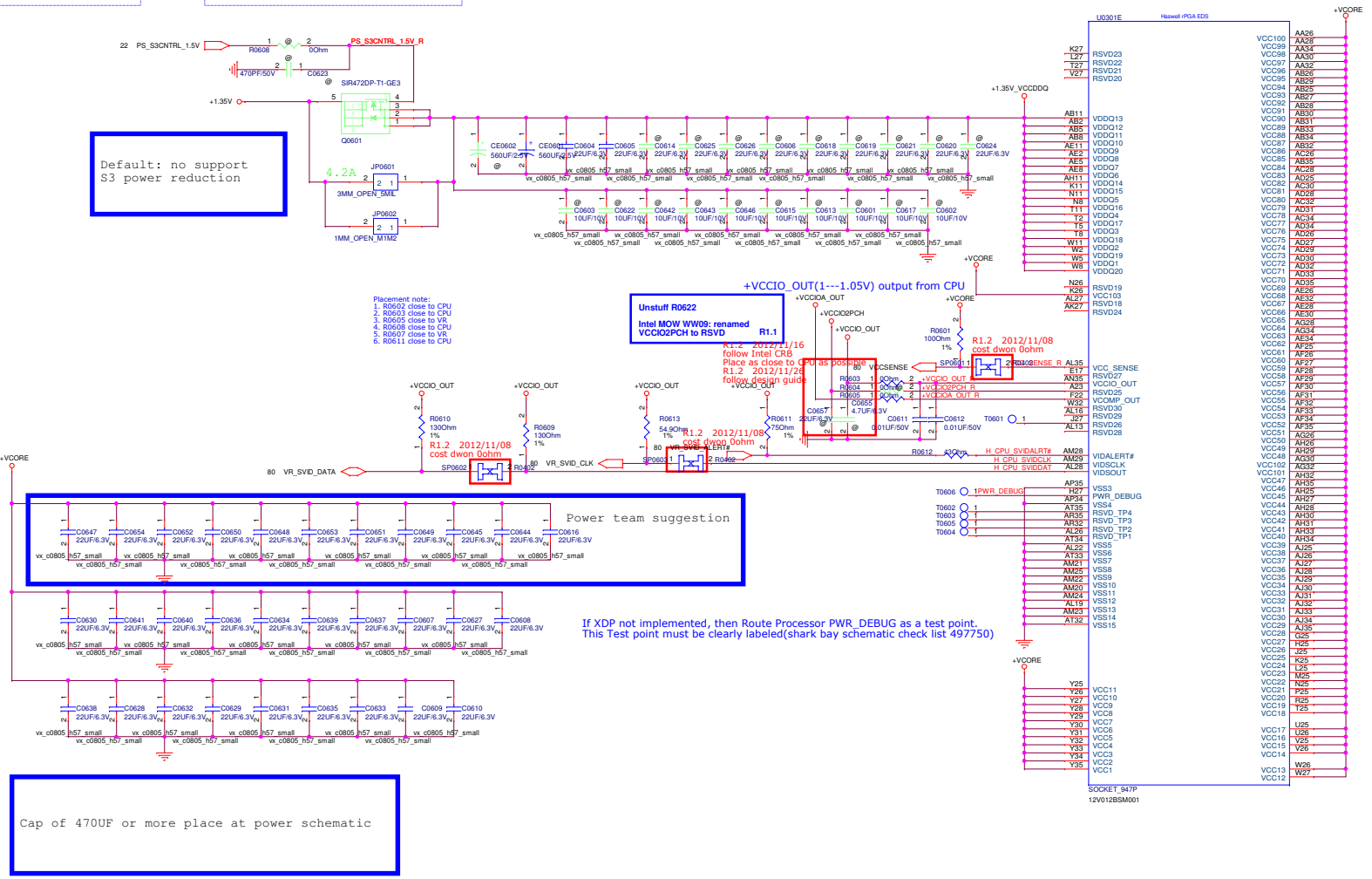
PEGATRON	Title : CPU(2)_DDR3		
PEGATRON COMPUTER INC	Engineer: Wing_Cheng		
Size C	Project Name VA70_HW		Rev 1.0
Date: Friday, January 18, 2013	Sheet 5 of 96		

Decoupling guide from Intel (SPEC)
VDDQ 22uF * 11 pcs (stuff)
10uF * 10 pcs (stuff)
330uF * 2 pcs (stuff)

Decoupling guide from Intel (EE)
VDDQ 22uF * 2pcs (stuff)
10uF * 2pcs (stuff)
330uF * 1pcs (stuff)

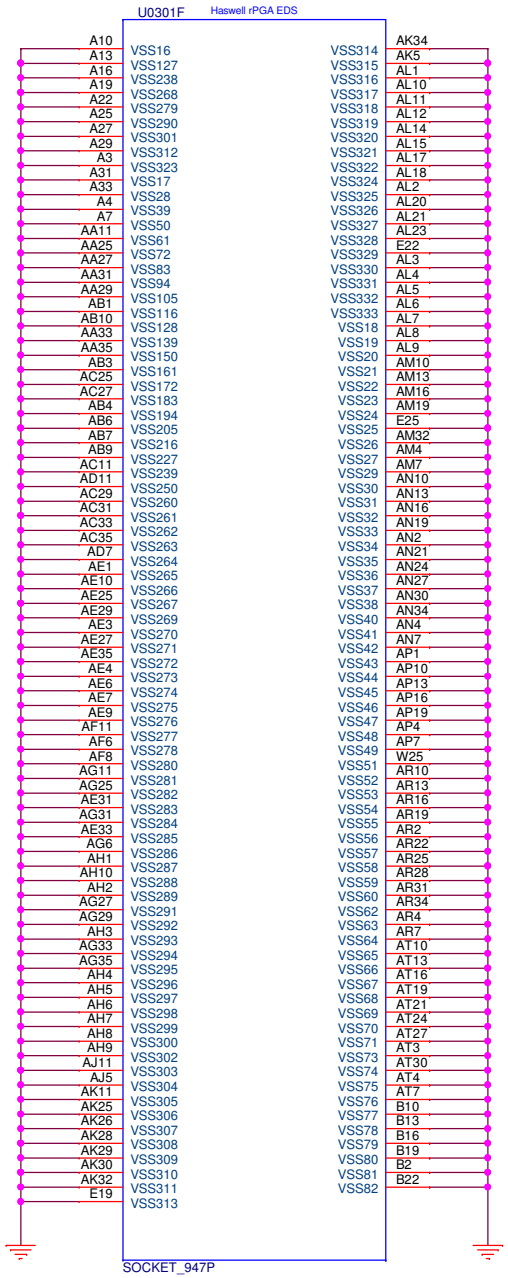
Decoupling guide from Intel (SPEC)
+VCORE 10uF * 11pcs (stuff)
22uF * 19pcs (stuff)
470uF * 4pcs (stuff)

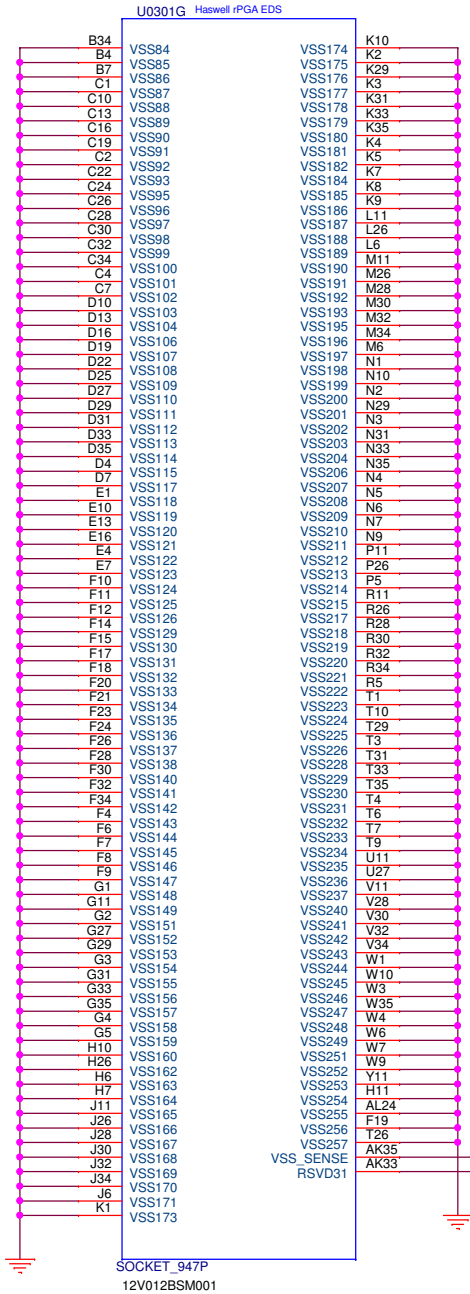
Decoupling guide from Intel (EE)
+VCORE 10uF * 11 pcs (stuff)
22uF * 19 pcs (stuff)
470uF * 5 pcs (stuff)

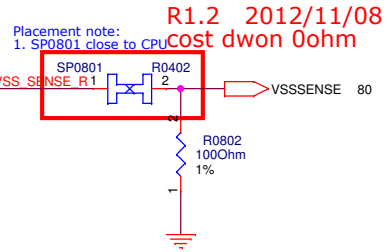


PEGATRON	Title : CPU(4)_PWR	
PEGATRON COMPUTER INC	Engineer: Wing_Cheng	
Size: Custom	Project Name: VA70_HW	Rev: 1.0
Date: Friday, January 18, 2013	Sheet 6 of 98	

PEGATRON	Title : CPU(4)_PWR		
PEGATRON COMPUTER INC	Engineer: Wing_Cheng		
Size C	Project Name VA70_HW		Rev 1.0
Date: Friday, January 18, 2013	Sheet 7 of 96		







PEGATRON	Title : CPU(3)_CFG,RSVD,GND		
PEGATRON COMPUTER INC	Engineer: Wing_Cheng		
Size B	Project Name VA70_HW		Rev 1.0
Date: Friday, January 18, 2013	Sheet 8 of 96		

CFG strapping information:

The CFG signals have a default value of '1'

CFG[1:0]: Reserved configuration lane.

CFG[2]: PCIE Static Numbering Lane Reversal- CFG[2] is for the 16x

- 1: (Default) Normal Operation, Lane # definition matches sockect pin map definition
- 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

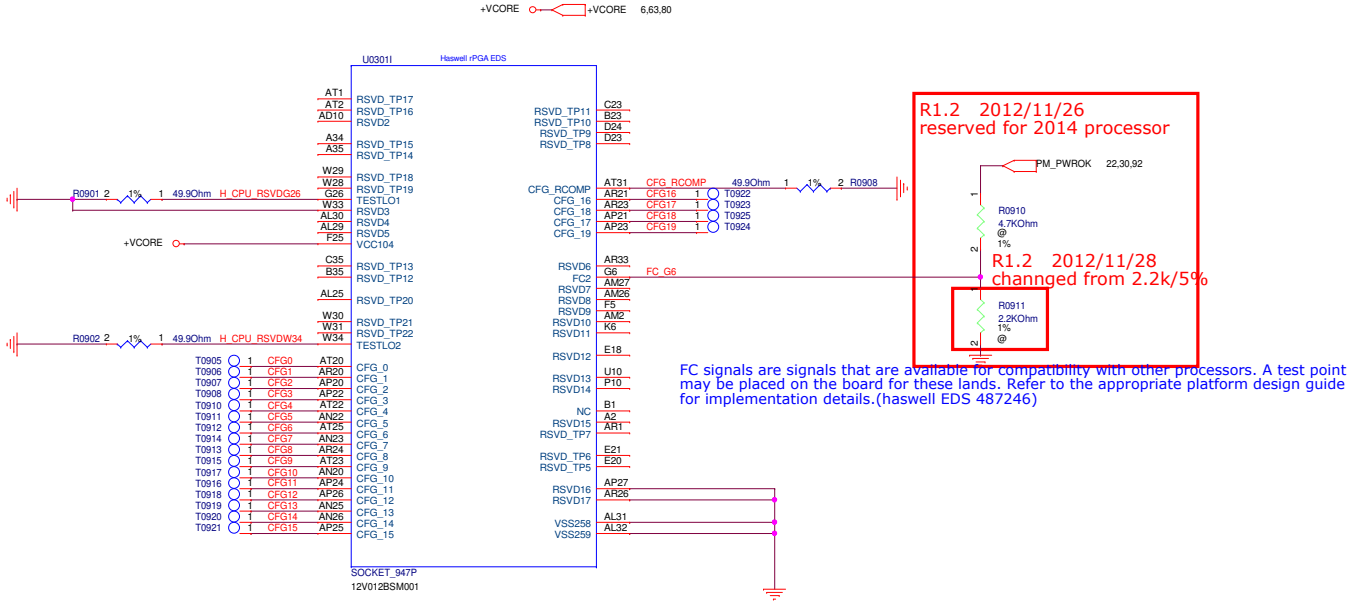
CFG[4]: eDP enable

-1 = Disabled
-0 = Enabled

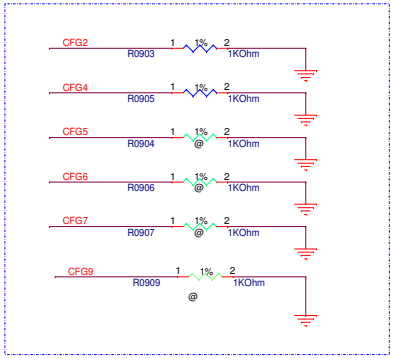
CFG[6:5]: PCI Express Port Bifurcation Straps

-00 = 1 x8, 2 x4 PCI Express*
-01 = reserved
-10 = 2 x8 PCI Express*
-11 = 1 x16 PCI Express*

CFG[19:7]: Reserved configuration lane.

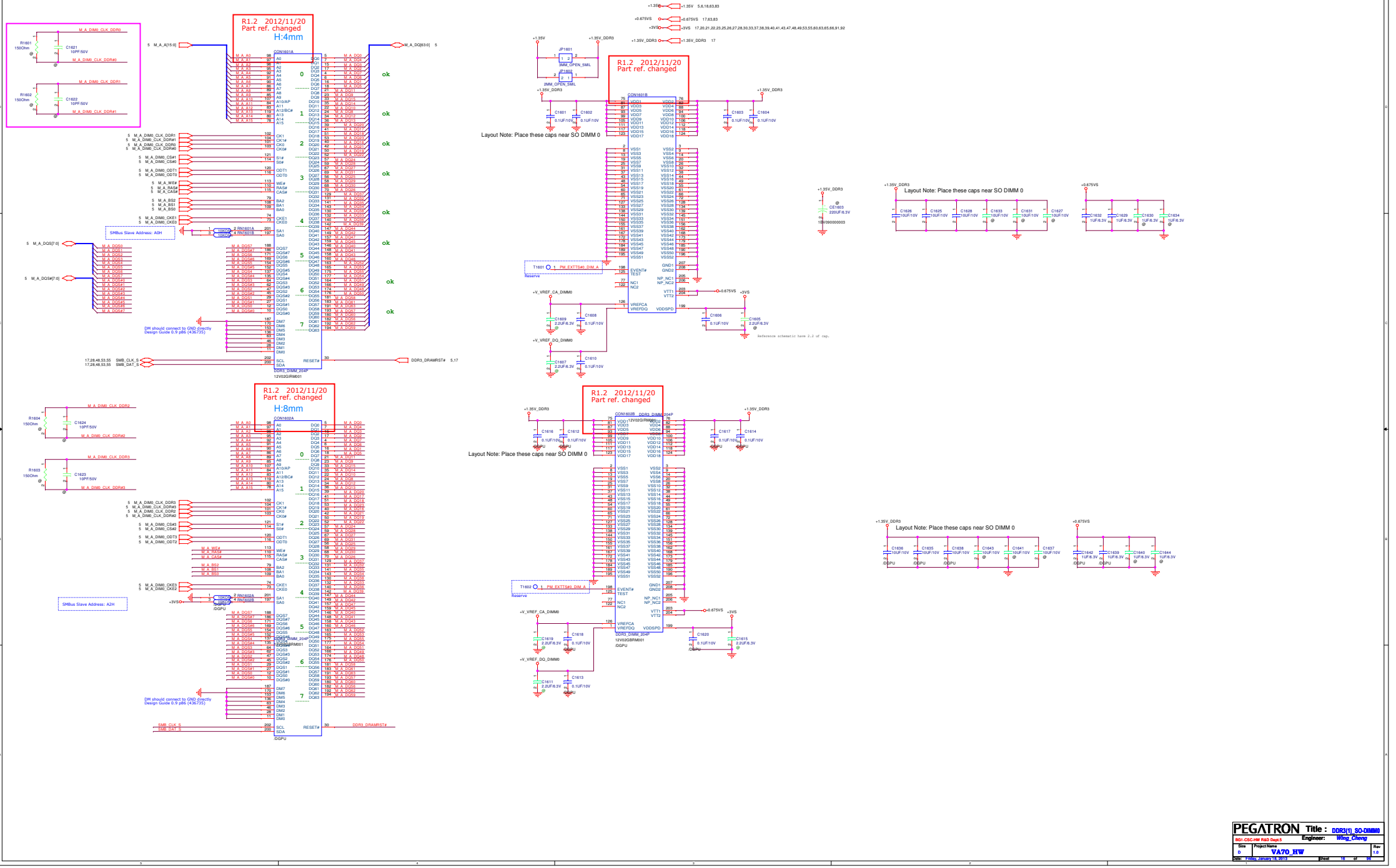


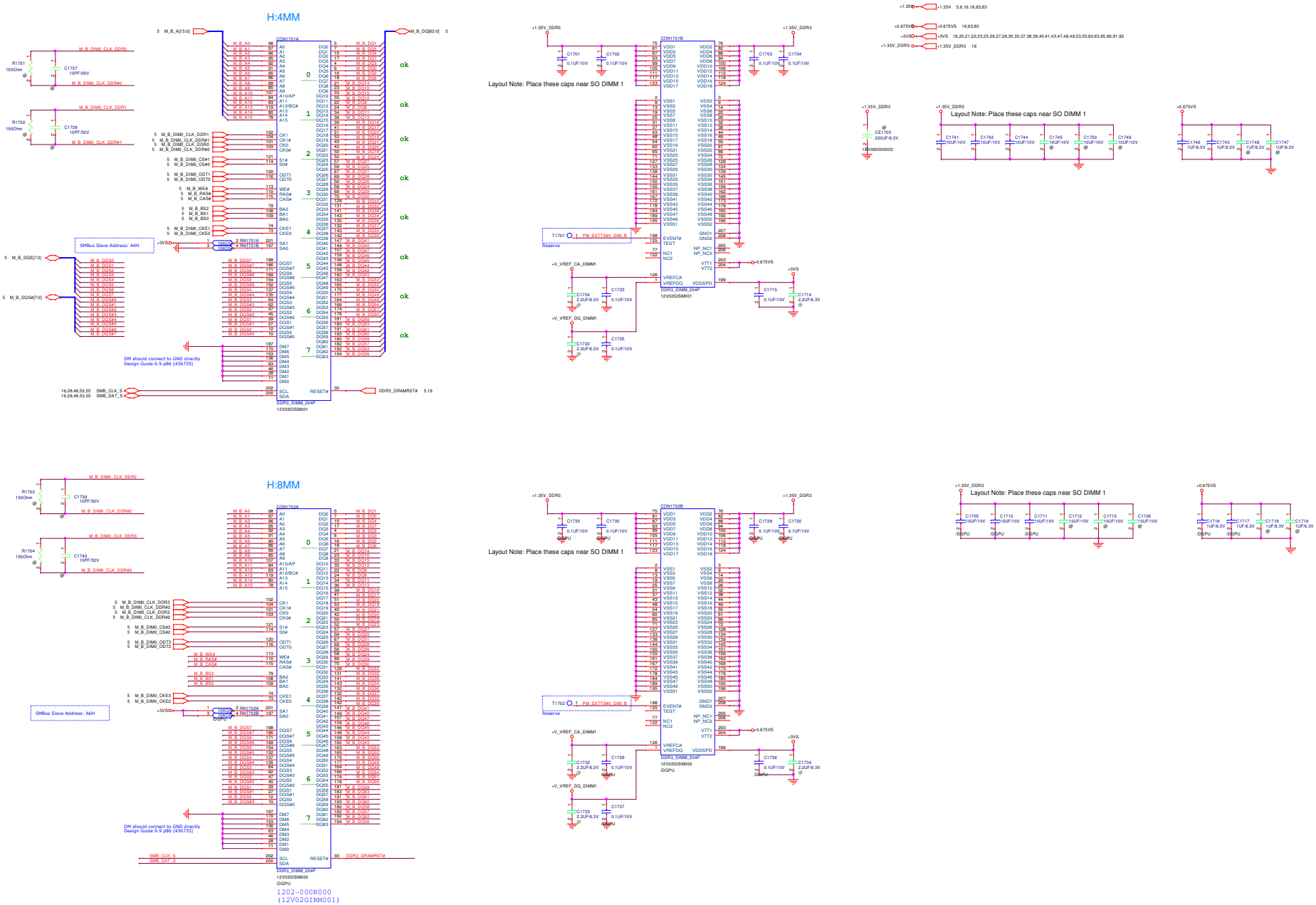
FC signals are signals that are available for compatibility with other processors. A test point may be placed on the board for these lands. Refer to the appropriate platform design guide for implementation details.(haswell EDS 487246)



PEGATRON	Title : CPU(3)_CFG,RSVD,GND	
PEGATRON COMPUTER INC	Engineer: Wing_Cheng	
Size: Custom	Project Name: VA70_HW	Rev: 1.0
Date: Friday, January 18, 2013	Sheet 9 of 96	

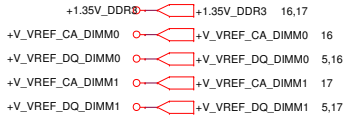
PEGATRON	Title : NB(3)_****		
PEGATRON COMPUTER INC	Engineer: Wing_Cheng		
Size C	Project Name VA70_HW		Rev 1.0
Date: Friday, January 18, 2013	Sheet 10 of 96		


R1.2 2012/11/20
Part ref. changed
H:4mm
CON1601A
DDR3_DIMM_204P
12V02GRM001
SMBus Slave Address: A0H
DM should connect to GND directly
Design Guide 0.9 p86 (436735)
R1.2 2012/11/20
Part ref. changed
CON1601B
Layout Note: Place these caps near SO DIMM 0
R1.2 2012/11/20
Part ref. changed
H:8mm
CON1602A
SMBus Slave Address: A2H
R1.2 2012/11/20
Part ref. changed
CON1602B
Layout Note: Place these caps near SO DIMM 0
Layout Note: Place these caps near SO DIMM 0
Layout Note: Place these caps near SO DIMM 0
Reference schematic have 2.2 uf cap.
PEGATRON
Title : DDR3(1)_SO-DIMM0
SQ1-CSC-HW R&D Dept.5
Engineer: Wing_Cheng
Size D
Project Name VA70_HW
Rev 1.0
Date: Friday, January 18, 2013
Sheet 16 of 96

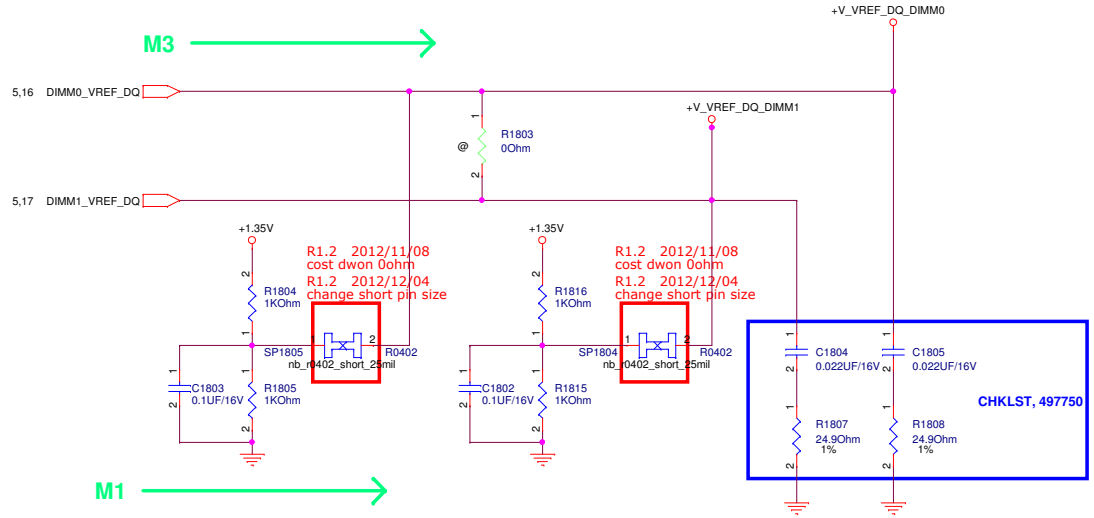


PEGATRON	Title : DDR3(2)_SO-DIMM1	
SQ1-C2C-HW R&D Dept.5	Engineer: Wing_Cheng	
Size D	Project Name VA70_HW	Rev 1.0
Date: Friday, January 18, 2013	Sheet 17 of 56	

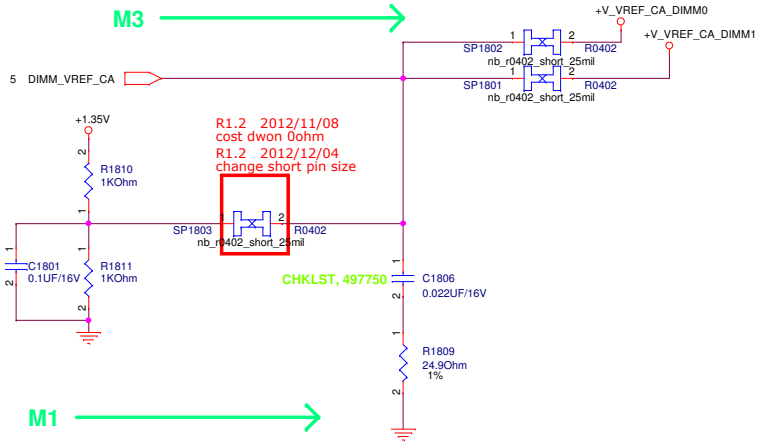
DDR3L Vref



M3: CPU driven VREF path is stuffed be default.
M1: VREF_DQ driven by a Voltage Divider Network during Processor power-off



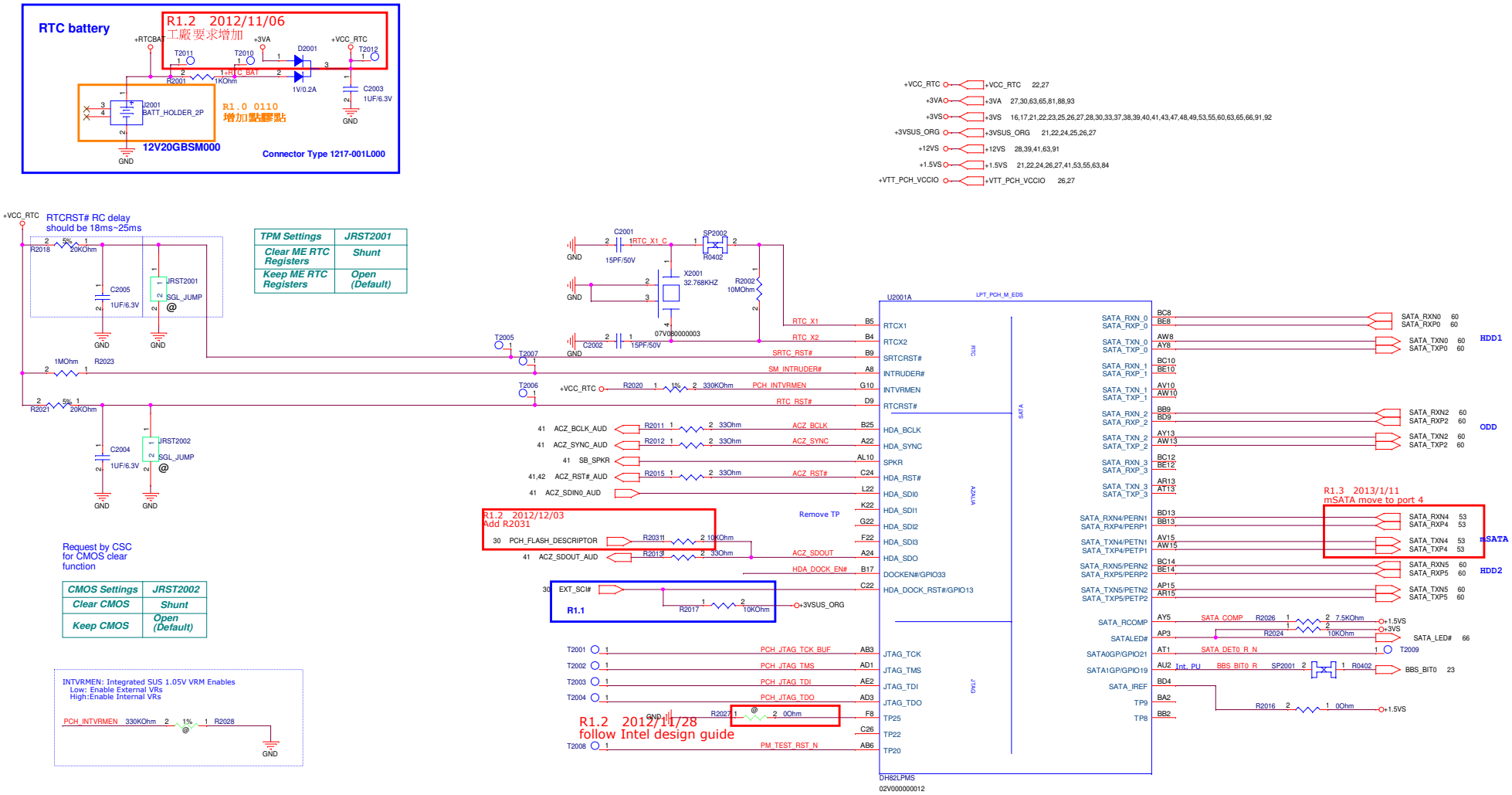

```
Intel 0203
M3+M1: Default Recommendation
```



PEGATRON	Title : DDR3(3)_CA/DQ Voltage	
PEGATRON COMPUTER INC	Engineer: Wing_Cheng	
Size: Custom	Project Name: VA70_HW	Rev: 1.0
Date: Friday, January 18, 2013	Sheet 18 of 96	

R1.4--2

PEGATRON	Title : VID Controller	
PEGATRON COMPUTER INC	Engineer: Wing_Cheng	
Size C	Project Name VA70_HW	Rev 1.0
Date: Friday, January 18, 2013	Sheet 19 of 96	

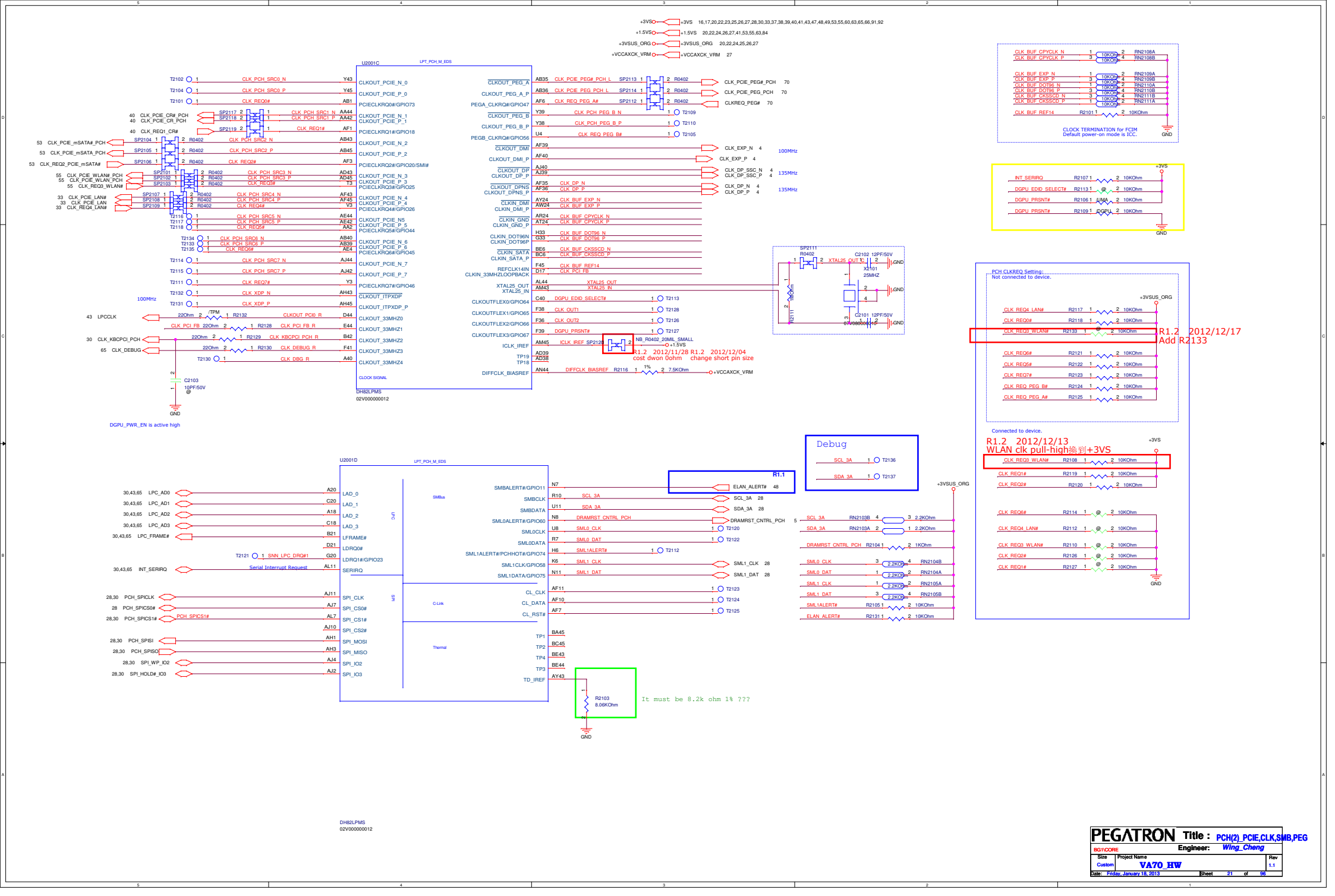


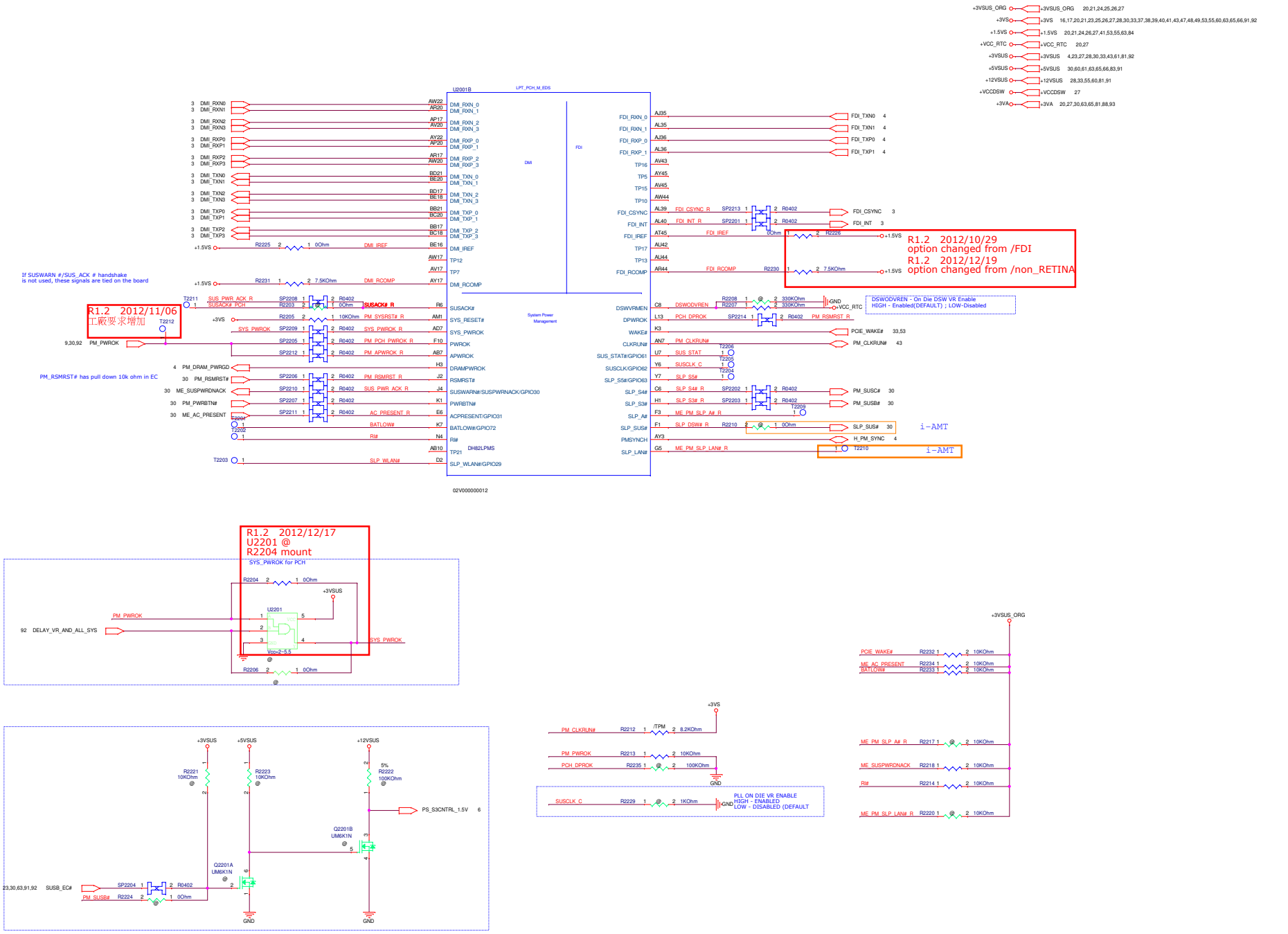
PEGATRON Title : PCH(1)_SATA,HDA,RTC,LPC

PEGATRON COMPUTER INC Engineer: Wing_Cheng

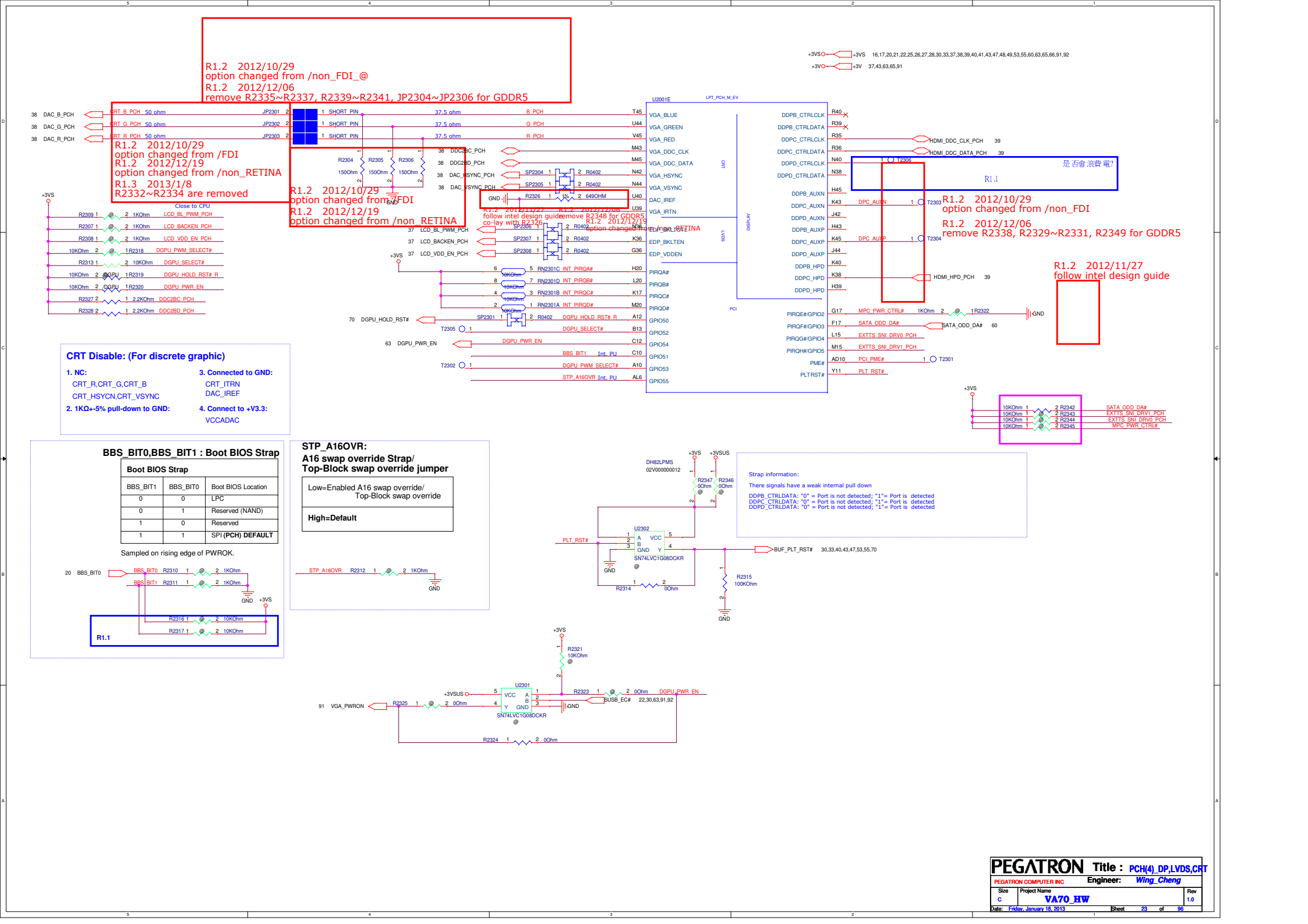
Size	Project Name	Rev
C	VA70_HW	1.0

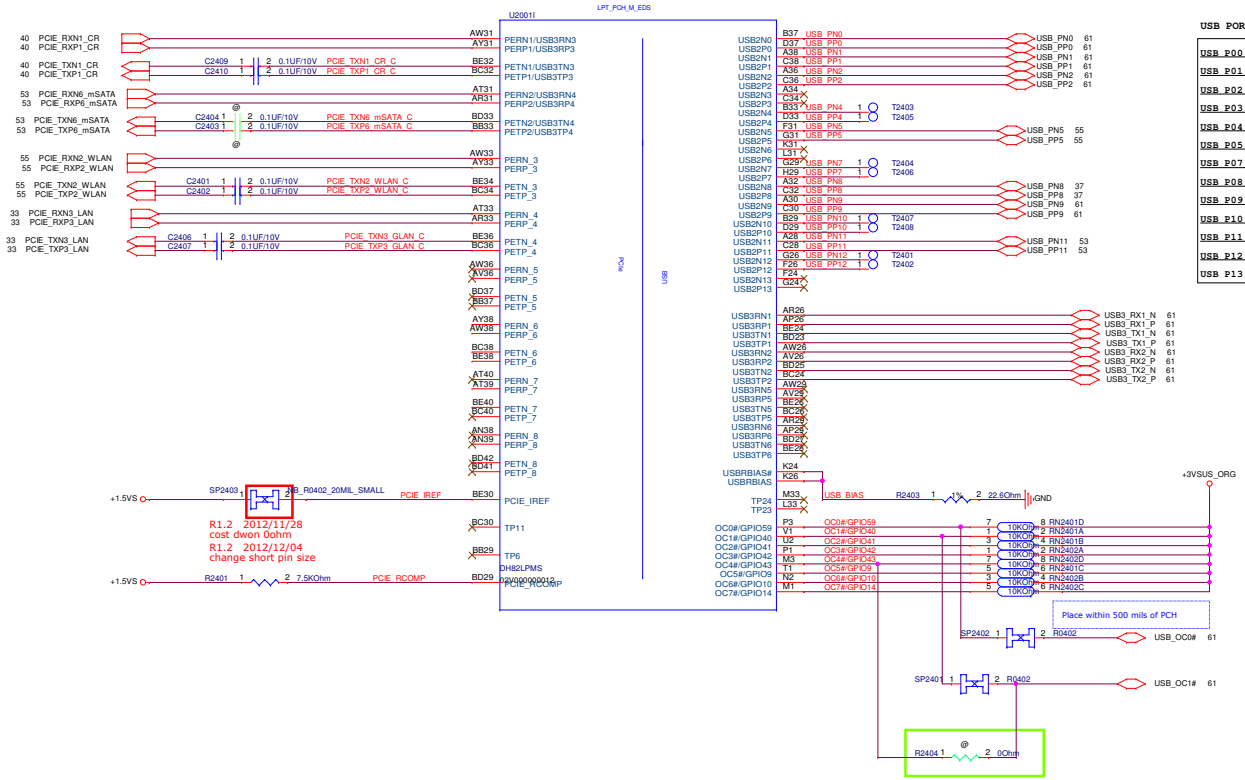
Date: Friday, January 18, 2013 Sheet 20 of 96


U2001C
LPT_PCH_M_EDS
DH82LPMS
02V000000012
CLOCK SIGNAL
DGPU_PWR_EN is active high
R1.2 2012/11/28 R1.2 2012/12/04
cost dwon 0ohm change short pin size
PCH CLKREQ Setting:
Not connected to device.
Connected to device.
R1.2 2012/12/17
Add R2133
R1.2 2012/12/13
WLAN clk pull-high換到+3VS
CLOCK TERMINATION for FCIM
Default power-on mode is ICC.
Debug
U2001D
LPT_PCH_M_EDS
SMBus
LPC
SPI
C-Link
Thermal
R1.1
It must be 8.2k ohm 1% ???
R2103
8.06KOhm
PEGATRON
Title : PCH(2)_PCIE,CLK,SMB,PEG
Engineer: Wing_Cheng
BG1CORE
Size Custom
Project Name VA70_HW
Rev 1.1
Date: Friday, January 18, 2013
Sheet 21 of 96



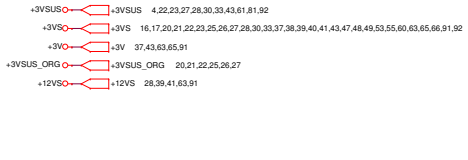
PEGATRON	Title : PCH(3)_FDI,DMI,SYS PWR		
PEGATRON COMPUTER INC	Engineer: Wing_Cheng		
Size: Custom	Project Name: VA70_HW		Rev: 1.0
Date: Friday, January 18, 2013	Sheet 22 of 96		


R1.2 2012/10/29
option changed from /non_FDI_@
R1.2 2012/12/06
remove R2335~R2337, R2339~R2341, JP2304~JP2306 for GDDR5
R1.2 2012/10/29
option changed from /FDI
R1.2 2012/12/19
option changed from /non_RETINA
R1.3 2013/1/8
R2332~R2334 are removed
R1.2 2012/10/29
option changed from /FDI
R1.2 2012/12/19
option changed from /non_RETINA
R1.2 2012/11/27
follow intel design guide
co-lay with R2326
R1.2 2012/12/06
remove R2348 for GDDR5
R1.2 2012/12/19
option changed from /non_RETINA
是否會浪費電?
R1.1
R1.2 2012/10/29
option changed from /non_FDI
R1.2 2012/12/06
remove R2338, R2329~R2331, R2349 for GDDR5
R1.2 2012/11/27
follow intel design guide
U2001E
LPT_PCH_M_EV
Close to CPU
CRT Disable: (For discrete graphic)
1. NC:
CRT_R,CRT_G,CRT_B
CRT_HSYCN,CRT_VSYNC
2. 1KΩ+-5% pull-down to GND:
3. Connected to GND:
CRT_ITRN
DAC_IREF
4. Connect to +V3.3:
VCCADAC
BBS_BIT0,BBS_BIT1 : Boot BIOS Strap
Boot BIOS Strap
BBS_BIT1 | BBS_BIT0 | Boot BIOS Location
0 | 0 | LPC
0 | 1 | Reserved (NAND)
1 | 0 | Reserved
1 | 1 | SPI (PCH) DEFAULT
Sampled on rising edge of PWROK.
R1.1
STP_A16OVR:
A16 swap override Strap/
Top-Block swap override jumper
Low=Enabled A16 swap override/
Top-Block swap override
High=Default
Strap information:
There signals have a weak internal pull down
DDPB_CTRLDATA: "0" = Port is not detected; "1"= Port is detected
DDPC_CTRLDATA: "0" = Port is not detected; "1"= Port is detected
DDPD_CTRLDATA: "0" = Port is not detected; "1"= Port is detected
U2302
SN74LVC1G08DCKR
U2301
SN74LVC1G08DCKR
PEGATRON
Title : PCH(4)_DP,LVDS,CRT
PEGATRON COMPUTER INC
Engineer: Wing_Cheng
Size C
Project Name VA70_HW
Rev 1.0
Date: Friday, January 18, 2013
Sheet 23 of 96



USB PORT

USB_P00	External 2.0/3.0
USB_P01	External 2.0/3.0
USB_P02	External 2.0
USB_P03	
USB_P04	
USB_P05	WiFi
USB_P07	
USB_P08	Camera
USB_P09	External 2.0
USB_P10	BT
USB_P11	PCIE/mSATA
USB_P12	
USB_P13	



Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

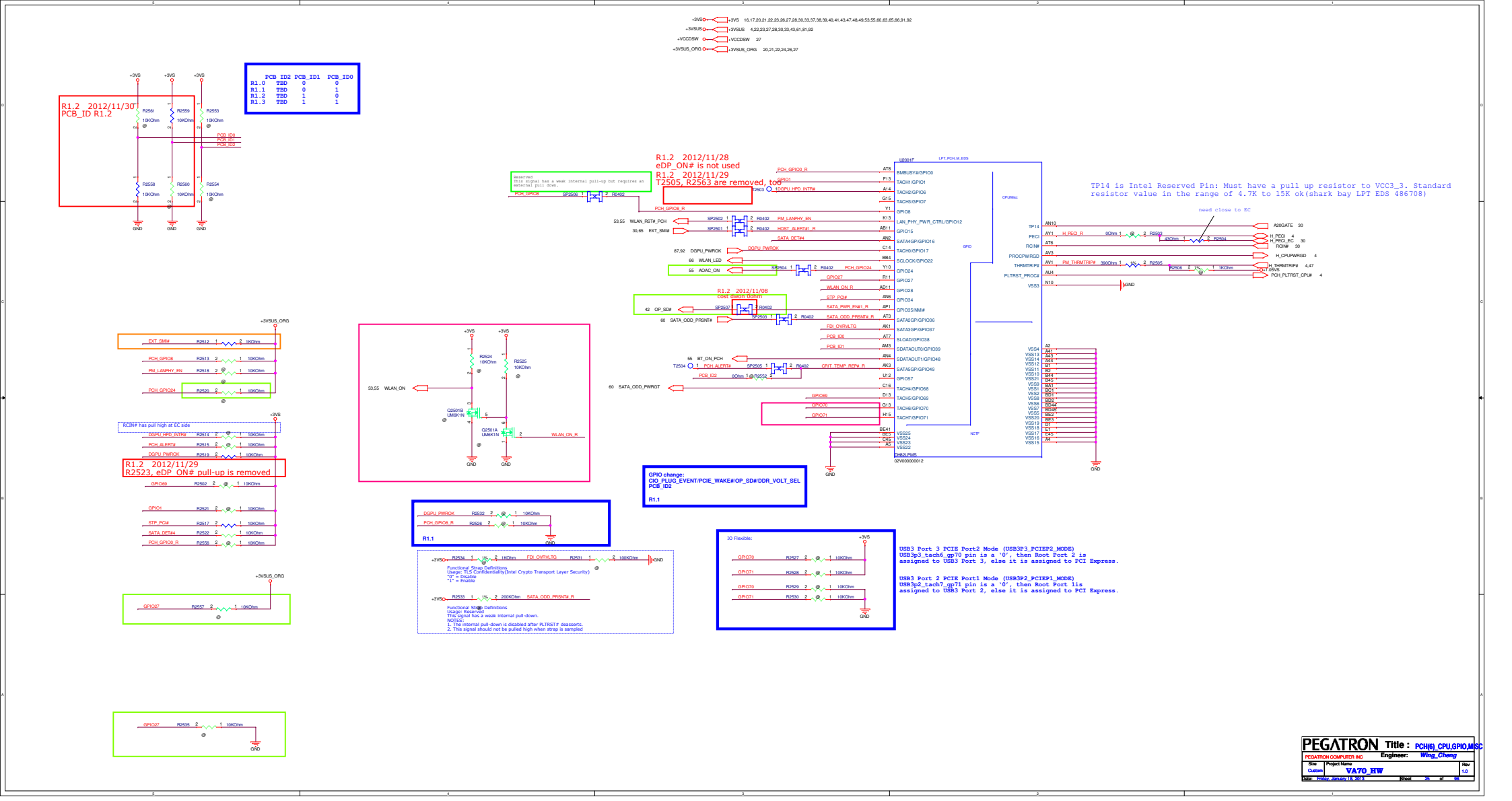
Table 1-5. Mobile Lynx Point SKUs Flexible I/O Map

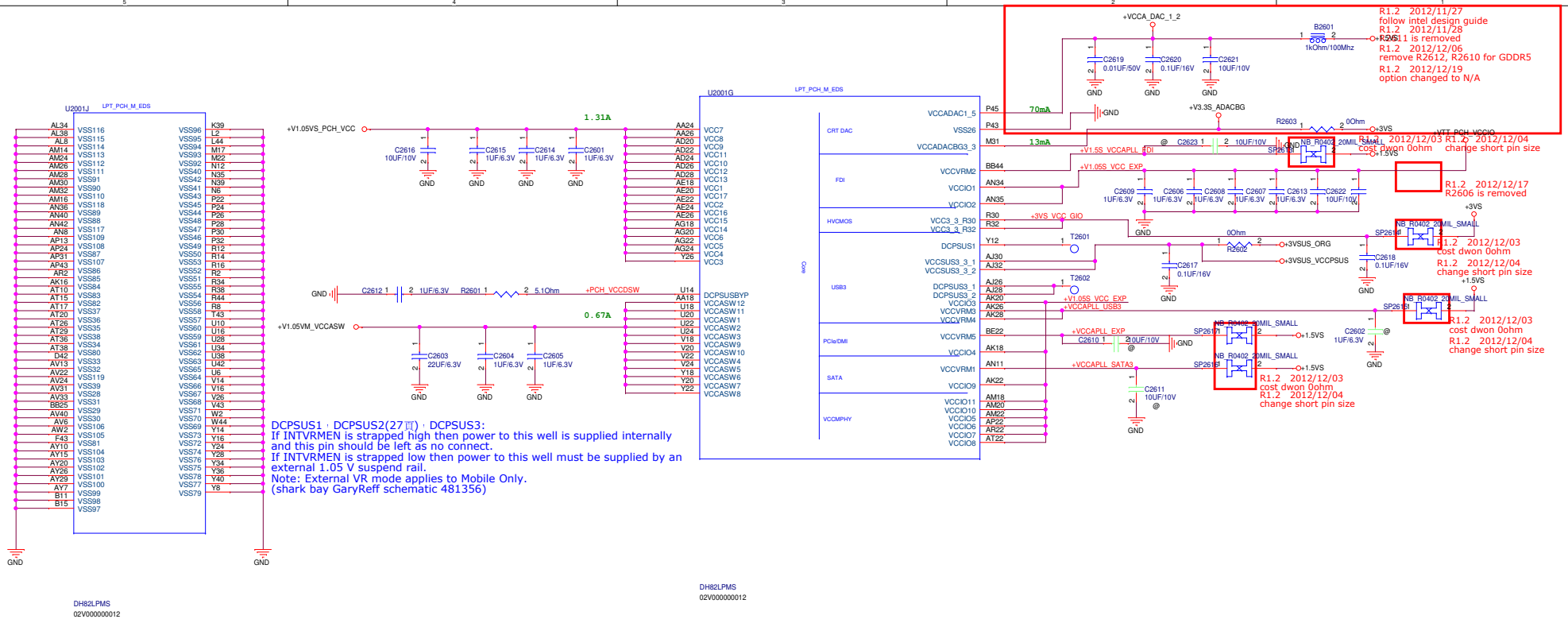
SKU	High Speed I/O Ports																	
	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7	Port 8	Port 9	Port 10	Port 11	Port 12	Port 13	Port 14	Port 15	Port 16	Port 17	Port 18
QM87	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 5	USB 3.0 Port 6	USB 3.0 Port 3 / PCIe* Port 1	USB 3.0 Port 4 / PCIe* Port 2	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5	PCIe* Port 6	PCIe* Port 7	PCIe* Port 8	SATA 6Gb/s Port 4 / PCIe* Port 1	SATA 6Gb/s Port 5 / PCIe* Port 2	SATA 6Gb/s Port 0	SATA 6Gb/s Port 1	SATA 3Gb/s Port 2	SATA 3Gb/s Port 3
HM87	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 5	USB 3.0 Port 6	USB 3.0 Port 3 / PCIe* Port 1	USB 3.0 Port 4 / PCIe* Port 2	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5	PCIe* Port 6	PCIe* Port 7	PCIe* Port 8	SATA 6Gb/s Port 4 / PCIe* Port 1	SATA 6Gb/s Port 5 / PCIe* Port 2	SATA 6Gb/s Port 0	SATA 6Gb/s Port 1	SATA 3Gb/s Port 2	SATA 3Gb/s Port 3
HM86	USB 3.0 Port 1	USB 3.0 Port 2	NA	NA	USB 3.0 Port 3 / PCIe* Port 1	USB 3.0 Port 4 / PCIe* Port 2	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5	PCIe* Port 6	PCIe* Port 7	PCIe* Port 8	SATA 6Gb/s Port 4	SATA 6Gb/s Port 5	SATA 3Gb/s Port 0	NA	SATA 3Gb/s Port 2	NA

NOTES:

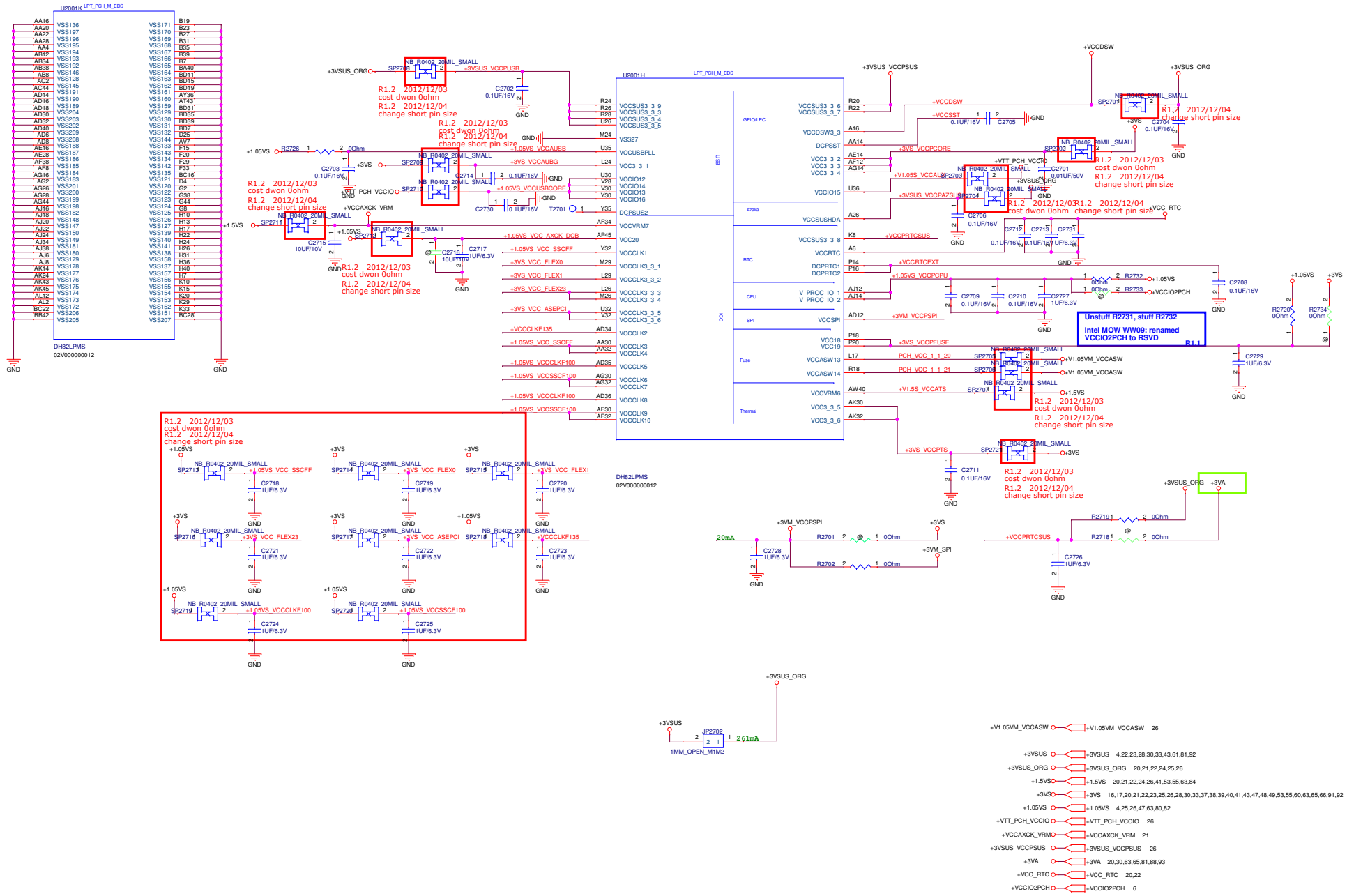
1. Ports listed with NA are not available and are disabled.

PEGATRON	Title : PCH(5)_PCI,NVRAM,USB		
PEGATRON COMPUTER INC	Engineer: Wing_Cheng		
Size: Custom	Project Name: VA70_HW		Rev: 1.0
Date: Friday, January 18, 2013	Sheet 24 of 96		


+3VSO +3VS 16,17,20,21,22,23,26,27,28,30,33,37,38,39,40,41,43,47,48,49,53,55,60,63,65,66,91,92
+3VSUS +3VSUS 4,22,23,27,28,30,33,43,61,81,92
+VCCDSW +VCCDSW 27
+3VSUS_ORG +3VSUS_ORG 20,21,22,24,26,27
PCB_ID2 PCB_ID1 PCB_ID0
R1.0 TBD 0 0
R1.1 TBD 0 1
R1.2 TBD 1 0
R1.3 TBD 1 1
R1.2 2012/11/30
PCB_ID R1.2
R2561 10KOhm
R2559 10KOhm
R2553 10KOhm
R2558 10KOhm
R2560 10KOhm
R2554 10KOhm
PCB_ID0
PCB_ID1
PCB_ID2
GND
R1.2 2012/11/28
eDP_ON# is not used
R1.2 2012/11/29
T2505, R2563 are removed, too
Reserved
This signal has a weak internal pull-up but requires an external pull down.
PCH_GPIO8
SP2506
R0402
PCH_GPIO8_R
53,55 WLAN_RST#_PCH
30,65 EXT_SMI#
SP2502
SP2501
PM_LANPHY_EN
HOST_ALERT#1_R
SATA_DET#4
87,92 DGPU_PWROK
DGPU_PWROK
66 WLAN_LED
55 AOAC_ON
SP2504
PCH_GPIO24
R1.2 2012/11/08
cost down DGPU
42 OP_SD#
60 SATA_ODD_PRSNT#
SP2507
SP2509
SATA_ODD_PRSNT#_R
55 BT_ON_PCH
T2504
PCH_ALERT#
SP2505
CRIT_TEMP_REPN_R
PCB_ID2
0Ohm
R2552
60 SATA_ODD_PWRGT
U2001F
LPT_PCH_M_EDS
BMBUSY#/GPIO0
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
LAN_PHY_PWR_CTRL/GPIO12
GPIO15
SATA4GP/GPIO16
TACH0/GPIO17
SCLOCK/GPIO22
GPIO24
GPIO27
GPIO28
GPIO34
GPIO55/NMI#
SATA2GP/GPIO36
SATA3GP/GPIO37
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48
SATA5GP/GPIO49
GPIO57
TACH4/GPIO68
TACH5/GPIO69
TACH6/GPIO70
TACH7/GPIO71
CPUMisc
GPIO
NCTF
VSS25
VSS24
VSS23
VSS22
DH82LPM6
02V0000000012
TP14 is Intel Reserved Pin: Must have a pull up resistor to VCC3_3. Standard resistor value in the range of 4.7K to 15K ok(shark bay LPT EDS 486708)
need close to EC
TP14
PECI
RCIN#
PROCPWRGD
THRMTRIP#
PLTRST_PROC#
VSS3
AN10
AY1
AT6
AV3
AV1
AU4
N10
H_PECI_R
0Ohm
R2503
43Ohm
R2504
PM_THRMTRIP#
390Ohm
R2505
R2508
1KOhm
A20GATE 30
H_PECI 4
H_PECI_EC 30
RCIN# 30
H_CPUPWRGD 4
H_THRMTRIP# 4,47
+3VS
PCH_PLTRST_CPU# 4
EXT_SMI#
PCH_GPIO8
PM_LANPHY_EN
PCH_GPIO24
R2512
R2513
R2518
R2520
10KOhm
RCIN# has pull high at EC side
DGPU_HPD_INTR#
PCH_ALERT#
DGPU_PWROK
R2514
R2515
R2519
R1.2 2012/11/29
R2523, eDP_ON# pull-up is removed
GPIO69
GPIO1
STP_PCI#
SATA_DET#4
PCH_GPIO0_R
R2502
R2521
R2517
R2522
R2556
R2524
R2525
53,55 WLAN_ON
Q2501B
UM6K1N
Q2501A
UM6K1N
WLAN_ON_R
GPIO68
GPIO70
GPIO71
DGPU_PWROK
PCH_GPIO8_R
R2532
R2526
R1.1
R2534
FDI_OVRVLTG
R2531
100KOhm
Functional Strap Definitions
Usage: TLS Confidentiality(Intel Crypto Transport Layer Security)
"0" = Disable
"1" = Enable
R2533
200KOhm
SATA_ODD_PRSNT#_R
Functional Strap Definitions
Usage: Reserved
This signal has a weak internal pull-down.
NOTES:
1. The internal pull-down is disabled after PLTRST# deasserts.
2. This signal should not be pulled high when strap is sampled
GPIO27
R2557
GPIO27
R2535
GPIO change:
CIO_PLUG_EVENT/PCIE_WAKE#/OP_SD#/DDR_VOLT_SEL
PCB_ID2
R1.1
IO Flexible:
GPIO70
GPIO71
R2527
R2528
R2529
R2530
USB3 Port 3 PCIE Port2 Mode (USB3P3_PCIEP2_MODE)
USB3p3_tach6_gp70 pin is a '0', then Root Port 2 is
assigned to USB3 Port 3, else it is assigned to PCI Express.
USB3 Port 2 PCIE Port1 Mode (USB3P2_PCIEP1_MODE)
USB3p2_tach7_gp71 pin is a '0', then Root Port 1is
assigned to USB3 Port 2, else it is assigned to PCI Express.
PEGATRON
Title : PCH(6)_CPU,GPIO,MISC
PEGATRON COMPUTER INC
Engineer: Wing_Cheng
Size Project Name Rev
Custom VA70_HW 1.0
Date: Friday, January 18, 2013 Sheet 25 of 96

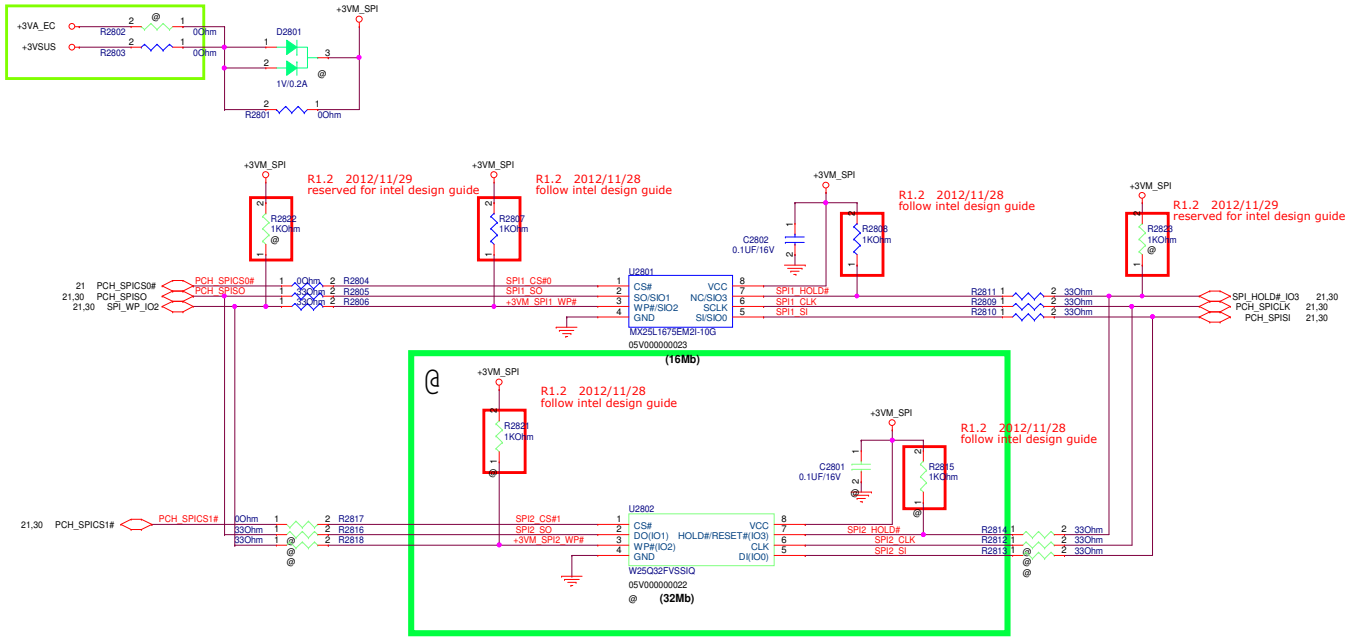


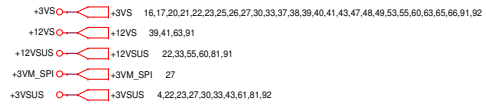
PEGATRON	Title : PCH(7)_POWER,GND	
BG1\CORE	Engineer: Wing_Cheng	
Size C	Project Name VA70_HW	Rev 1.1
Date: Friday, January 18, 2013	Sheet 26 of 96	

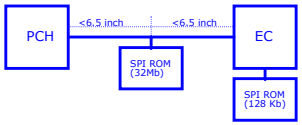


PEGATRON	Title : PCH(8)_POWER,GND		
PEGATRON COMPUTER INC	Engineer: Wing_Cheng		
Size: Custom	Project Name: VA70_HW		Rev: 1.0
Date: Friday, January 18, 2013	Sheet 27 of 96		

PCH SPI ROM





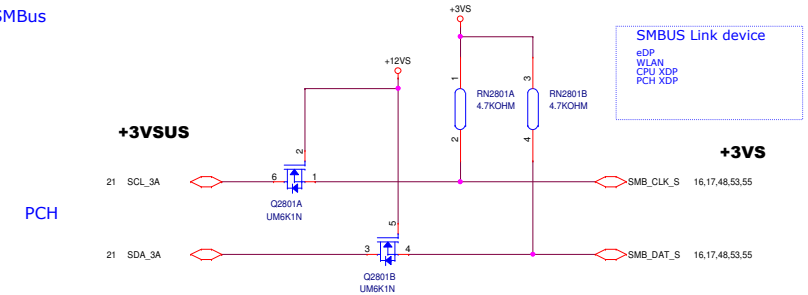


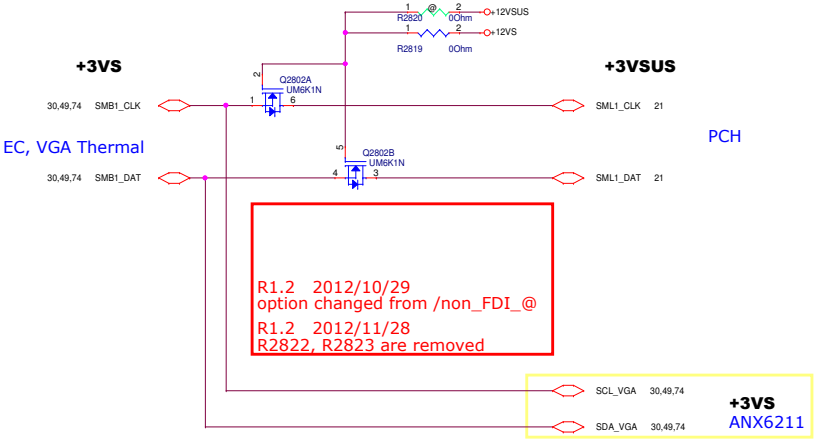

```
ROM setting:
Configuration 1. ITE HSPI -> short J2803 pin2 & 3
                 and no stuff U2801,U2802
Configuration 2. One ROM solution -> short J2803 pin1&2
                 and no stuff U2802 ; stuff U2801(BIOS+ME)
Configuration 3. Two ROM solution -> short J2803 pin1&2 , J2802 pin2&3
                 Stuff U2801(ME), Stuff U2802(BIOS)
```

```
Follow Intel setting:
U2801: ME
U2802: BIOS
```

SPI Debug Connector

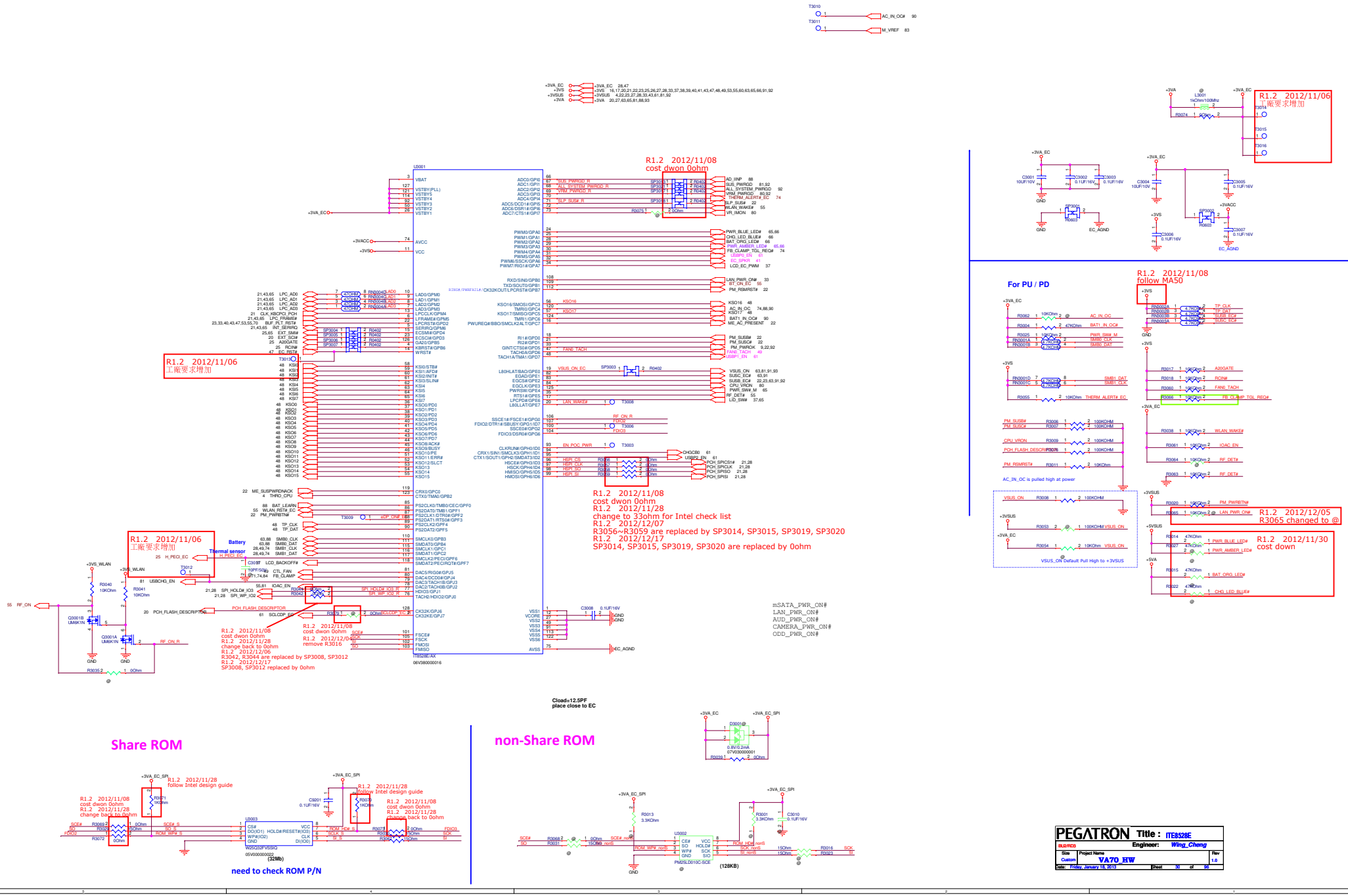
PCH SMBus

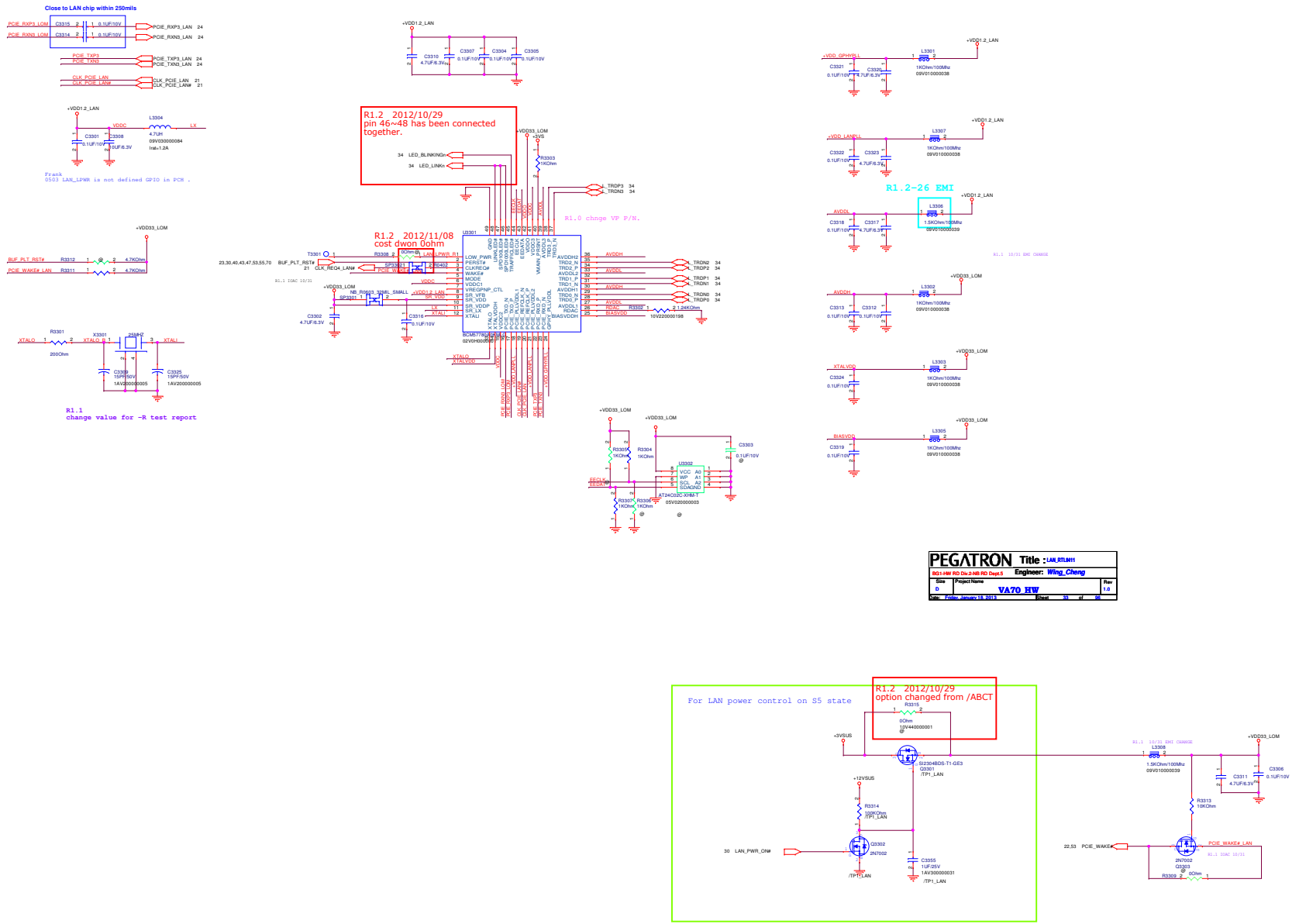




PEGATRON	Title : PCH(9)_SPI,SMB		
PEGATRON COMPUTER INC	Engineer: Wing_Cheng		
Size C	Project Name VA70_HW		Rev 1.0
Date: Friday, January 18, 2013	Sheet 28 of 96		

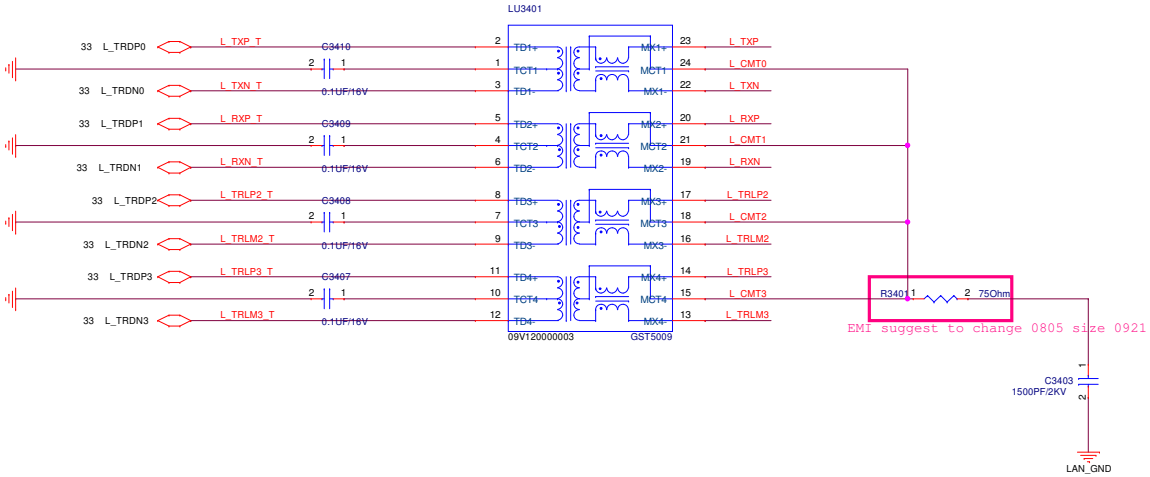
PEGATRON	Title : CLK_ICS9LRS3197		
PEGATRON COMPUTER INC	Engineer: Wing_Cheng		
Size: Custom	Project Name: VA70_HW		Rev: 1.0
Date: Friday, January 18, 2013	Sheet 29 of 96		

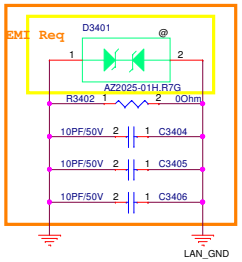

R1.2 2012/11/08
cost dwon 0ohm
R1.2 2012/11/06
工廠要求增加
R1.2 2012/11/08
cost dwon 0ohm
R1.2 2012/11/28
change to 33ohm for Intel check list
R1.2 2012/12/07
R3056~R3059 are replaced by SP3014, SP3015, SP3019, SP3020
R1.2 2012/12/17
SP3014, SP3015, SP3019, SP3020 are replaced by 0ohm
R1.2 2012/11/06
follow MA50
For PU / PD
R1.2 2012/12/05
R3065 changed to @
R1.2 2012/11/30
cost down
mSATA_PWR_ON#
LAN_PWR_ON#
AUD_PWR_ON#
CAMERA_PWR_ON#
ODD_PWR_ON#
Share ROM
R1.2 2012/11/08
cost dwon 0ohm
R1.2 2012/11/28
change back to 0ohm
R1.2 2012/12/06
R3042, R3044 are replaced by SP3008, SP3012
R1.2 2012/12/17
SP3008, SP3012 replaced by 0ohm
R1.2 2012/11/28
follow Intel design guide
R1.2 2012/11/08
cost dwon 0ohm
R1.2 2012/11/28
change back to 0ohm
(32Mb)
need to check ROM P/N
Cload=12.5PF
place close to EC
non-Share ROM
(128KB)
PEGATRON
Title : ITE8528E
Engineer: Wing_Cheng
Size Custom
Project Name VA70_HW
Rev 1.0
Date: Friday, January 18, 2013
Sheet 30 of 90

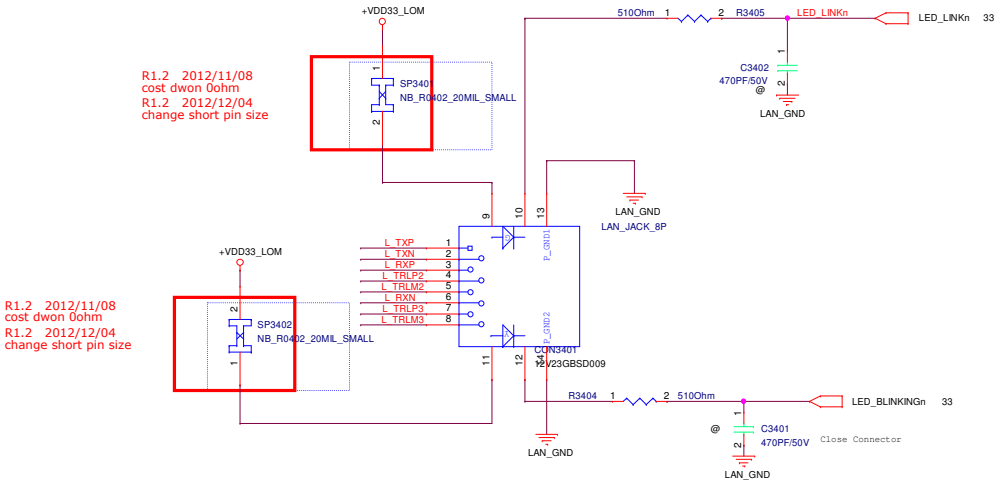

Close to LAN chip within 250mils
PCIE_RXP3_LOM
PCIE_RXN3_LOM
C3315 0.1UF/10V
C3314 0.1UF/10V
PCIE_RXP3_LAN 24
PCIE_RXN3_LAN 24
PCIE_TXP3
PCIE_TXN3
PCIE_TXP3_LAN 24
PCIE_TXN3_LAN 24
CLK_PCIE_LAN
CLK_PCIE_LAN#
CLK_PCIE_LAN 21
CLK_PCIE_LAN# 21
+VDD1.2_LAN
C3310 4.7UF/6.3V
C3307 0.1UF/10V
C3304 0.1UF/10V
C3305 0.1UF/10V
+VDD_GPHYPLL
L3301
C3321 0.1UF/10V
C3320 4.7UF/6.3V
1KOhm/100Mhz
09V010000038
+VDD_LANPLL
L3307
C3322 0.1UF/10V
C3323 4.7UF/6.3V
VDDC
L3304
LX
C3301 0.1UF/10V
C3308 10UF/6.3V
4.7UH
09V030000084
Irat=1.2A
Frank
0503 LAN_LPWR is not defined GPIO in PCM .
R1.2 2012/10/29
pin 46~48 has been connected together.
+VDD33_LOM
+3VS
R3303 1KOhm
34 LED_BLINKING#
34 LED_LINK#
L_TRDP3 34
L_TRDN3 34
R1.0 chnge VP P/N.
R1.2 2012/11/08
cost down 0ohm
LU301
+VDD33_LOM
BUF_PLT_RST# R3312 4.7KOhm
PCIE_WAKE#_LAN R3311 4.7KOhm
23,30,40,43,47,53,55,70 BUF_PLT_RST#
T3301
R3308 0Ohm
LAN_LPWR_R1
SP3301
PCIE_WAKE#_LAN
R1.1 IOAC 10/31
+VDD33_LOM
NB_R0603_10MIL_SMALL
SP3301
+VDD1.2_LAN
SR_VDD
C3302 4.7UF/6.3V
C3316 0.1UF/10V
LOW_PWR
PERST#
CLKREQ#
WAKE#
MODE
VDDCI
VREGPNP_CTL
SR_VFB
SR_VDD
SR_VDDP
SR_LX
XTALI
XTALO
XTALVDD
AVDDH2
TRDx2_N
TRDx2_P
AVDDL2
TRD1_P
TRD1_N
AVDDH1
TRDx_N
TRDx_P
AVDDL1
RDAC
BIASVDD
AVDDH
AVDDL
L_TRDN2 34
L_TRDP2 34
L_TRDP1 34
L_TRDN1 34
L_TRDN0 34
L_TRDP0 34
R3302 2.2.84KOhm
15V220000198
BCM57785A1KFBG
02V0600000
R3301
X3301
XTALO
XTALI
200Ohm
25MHZ
C3309 15PF/50V
C3325 15PF/50V
1AV200000005
R1.1
change value for -R test report
+VDD33_LOM
R3305 1KOhm
R3304 1KOhm
C3303 0.1UF/10V
U3302
VCC A0
WP A1
SCL A2
SDA GND
AT24C02C-XHM-T
05V020000003
R3307 1KOhm
R3306 1KOhm
+VDD33_LOM
L3302
C3318 0.1UF/10V
C3317 4.7UF/6.3V
1.5KOhm/100Mhz
09V010000039
R1.2-26 EMI
R1.1 10/31 EMI CHANGE
C3313 0.1UF/10V
C3312 0.1UF/10V
L3302
XTALVDD
C3324 0.1UF/10V
L3303
BIASVDD
C3319 0.1UF/10V
L3305
PEGATRON
Title : LAN_RTL8411
BG1-HW RD Div.2-NB RD Dept.5
Engineer: Wing_Cheng
Size D
Project Name VA70_HW
Rev 1.0
Date: Friday, January 18, 2013
Sheet 33 of 48
For LAN power control on S5 state
R1.2 2012/10/29
option changed from /ABCT
R3315 0Ohm 10V440000001
+3VSUS
Si2304BDS-T1-GE3
Q3301
/TP1_LAN
+12VSUS
R3314 100KOhm
/TP1_LAN
30 LAN_PWR_ON#
Q3302 2N7002
/TP1_LAN
C3355 1UF/25V 1AV300000031
/TP1_LAN
R1.1 10/31 EMI CHANGE
L3308 1.5KOhm/100Mhz 09V010000039
+VDD33_LOM
C3311 4.7UF/6.3V
C3306 0.1UF/10V
R3313 10KOhm
22,53 PCIE_WAKE#
PCIE_WAKE# LAN
R1.1 IOAC 10/31
2N7002
Q3303
R3309 0Ohm

FAE suggestion 1003

Co-Layout







R1.2 2012/10/29
All components options changed from /non_FDI

R1.2 2012/12/06
remove U3501 for GDDR5

<Variant Name>

PEGATRON	Title : DP to VGA	
BG1-CSC-HW R&D Dept.5	Engineer: Wing_Cheng	
Size: Custom	Project Name: VA70_HW	Rev: 1.0
Date: Friday, January 18, 2013	Sheet 35 of 86	

Initial Code EEPROM

PEGATRON	Title : LVDS CONN	
BU1-PD Div.1-HW RD Dept.1	Engineer: *Wing_Cheng*	
Size: Custom	Project Name: VA70_HW	Rev: 1.0
Date: Friday, January 18, 2013	Sheet 36 of 96	

LVDS

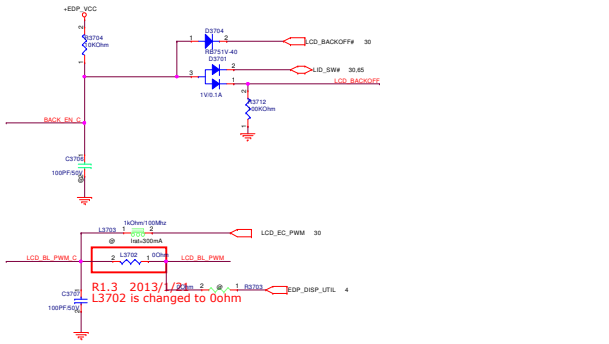
CH A

CH B

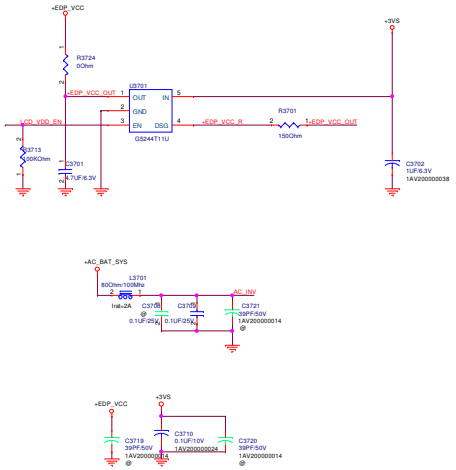
LVDS/eDP control signal

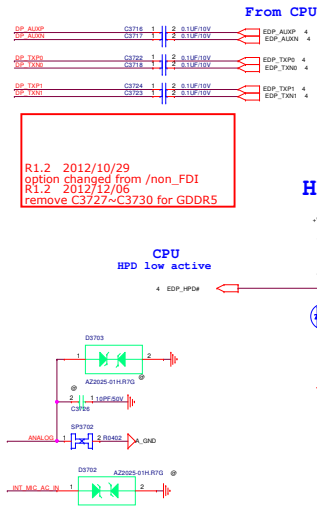
LVDS/EDP共用pin

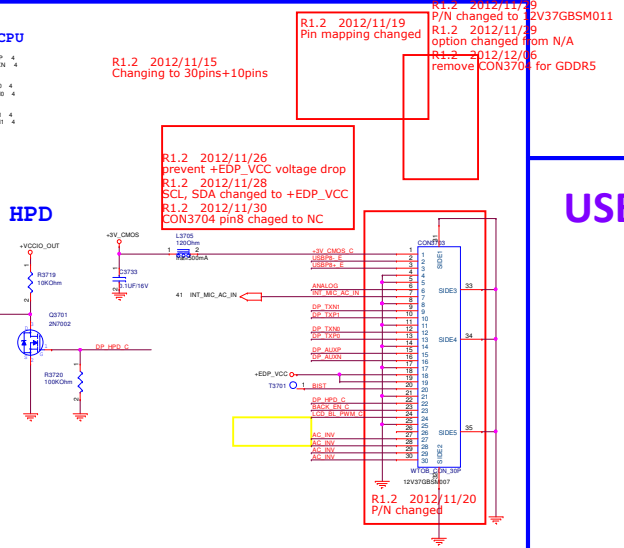
LVDS/EDP共用pin



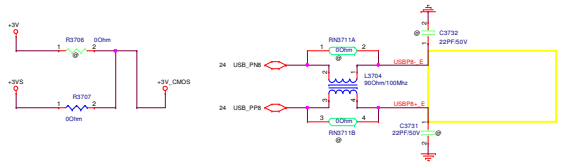
eDP



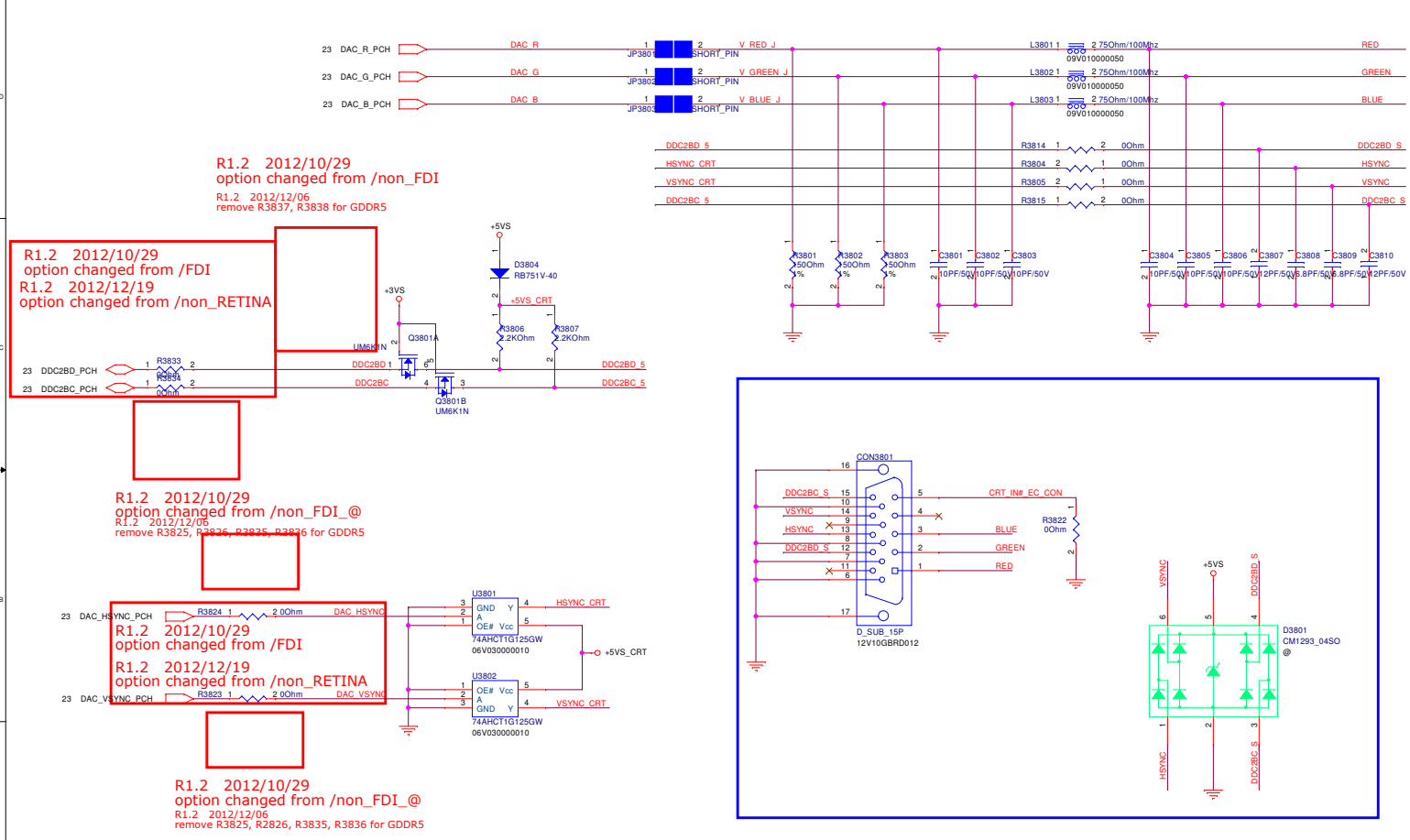


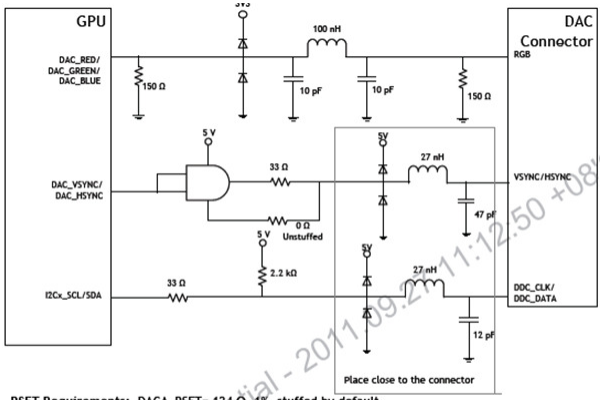


USB Camera



PEGATRON	Title : LVDS CONN	
BU1-RD Div.1-HW RD Dept.1	Engineer: Wing_Cheng	
Size / Custom	Project Name / VA70_HW	Rev / 1.0
Date: Monday, January 21, 2013	Sheet 37 of 38	





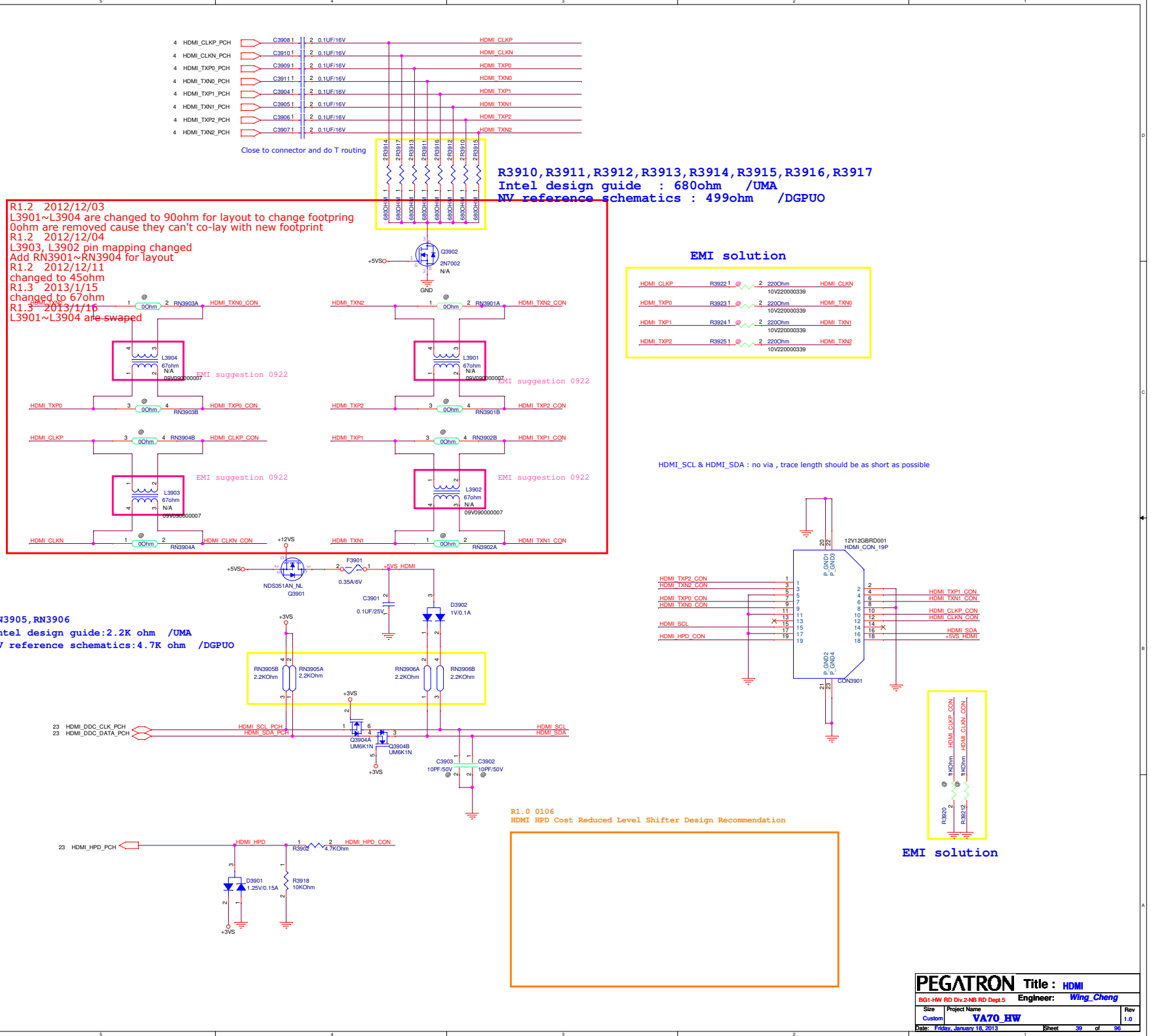
RSET Requirements: DACA_RSET= 124 Ω, 1%, stuffed by default.

Figure 71. GPU-DAC Connections

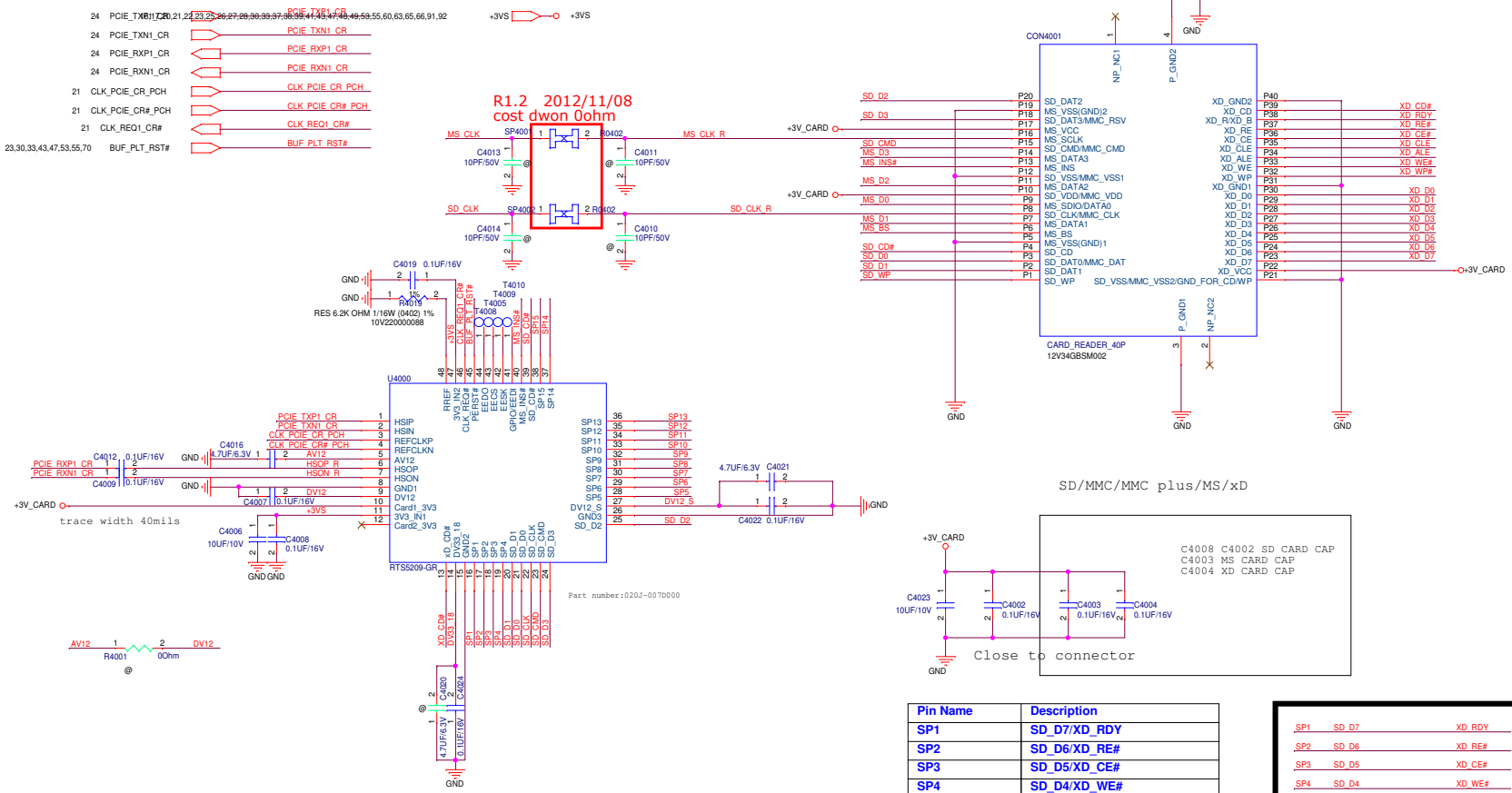
Confidential - 2011.09.27 11:12:50 +08

The LC filter circuit(NV DSC only)
DDC:L=27nH,C=12PF
HSYNC/VSYNC:L=27nH,C=47PF
RGB:L=100nH,C=10PF

PEGATRON	Title : CRT	
BU1-RD Div.1-HW RD Dept.1	Engineer: Wing_Cheng	
Size: Custom	Project Name: VA70_HW	Rev: 1.0
Date: Friday, January 18, 2013	Sheet 38 of 96	


HDMI_CLKP_PCH
HDMI_CLKN_PCH
HDMI_TXP0_PCH
HDMI_TXN0_PCH
HDMI_TXP1_PCH
HDMI_TXN1_PCH
HDMI_TXP2_PCH
HDMI_TXN2_PCH
C3908 0.1UF/16V
C3910 0.1UF/16V
C3909 0.1UF/16V
C3911 0.1UF/16V
C3904 0.1UF/16V
C3905 0.1UF/16V
C3906 0.1UF/16V
C3907 0.1UF/16V
HDMI_CLKP
HDMI_CLKN
HDMI_TXP0
HDMI_TXN0
HDMI_TXP1
HDMI_TXN1
HDMI_TXP2
HDMI_TXN2
Close to connector and do T routing
R3914 R3917 R3913 R3911 R3916 R3912 R3910 R3915
680OHM
R3910,R3911,R3912,R3913,R3914,R3915,R3916,R3917
Intel design guide : 680ohm /UMA
NV reference schematics : 499ohm /DGPUO
R1.2 2012/12/03
L3901~L3904 are changed to 90ohm for layout to change footpring
0ohm are removed cause they can't co-lay with new footprint
R1.2 2012/12/04
L3903, L3902 pin mapping changed
Add RN3901~RN3904 for layout
R1.2 2012/12/11
changed to 45ohm
R1.3 2013/1/15
changed to 67ohm
R1.3 2013/1/16
L3901~L3904 are swaped
Q3902
2N7002
N/A
+5VS
GND
HDMI_TXN0
RN3903A
HDMI_TXN0_CON
HDMI_TXN2
RN3901A
HDMI_TXN2_CON
L3904
67ohm
N/A
09V090000007
EMI suggestion 0922
L3901
HDMI_TXP0
RN3903B
HDMI_TXP0_CON
HDMI_TXP2
RN3901B
HDMI_TXP2_CON
HDMI_CLKP
RN3904B
HDMI_CLKP_CON
HDMI_TXP1
RN3902B
HDMI_TXP1_CON
L3903
L3902
HDMI_CLKN
RN3904A
HDMI_CLKN_CON
HDMI_TXN1
RN3902A
HDMI_TXN1_CON
EMI solution
HDMI_TXP0 R3923 220Ohm HDMI_TXN0
HDMI_TXP1 R3924 220Ohm HDMI_TXN1
HDMI_TXP2 R3925 220Ohm HDMI_TXN2
10V220000339
HDMI_SCL & HDMI_SDA : no via , trace length should be as short as possible
12V12GBRD001
HDMI_CON_19P
P_GND1
P_GND3
P_GND2
P_GND4
CON3901
HDMI_TXP2_CON
HDMI_TXN2_CON
HDMI_TXP0_CON
HDMI_TXN0_CON
HDMI_SCL
HDMI_HPD_CON
HDMI_TXP1_CON
HDMI_TXN1_CON
HDMI_CLKP_CON
HDMI_CLKN_CON
HDMI_SDA
+5VS_HDMI
+12VS
NDS351AN_NL
Q3901
F3901
0.35A/6V
C3901
0.1UF/25V
D3902
1V/0.1A
RN3905,RN3906
Intel design guide:2.2K ohm /UMA
NV reference schematics:4.7K ohm /DGPUO
+3VS
RN3905B 2.2KOhm
RN3905A 2.2KOhm
RN3906A 2.2KOhm
RN3906B 2.2KOhm
23 HDMI_DDC_CLK_PCH
23 HDMI_DDC_DATA_PCH
HDMI_SCL_PCH
HDMI_SDA_PCH
HDMI_SCL
HDMI_SDA
Q3904A UM6K1N
Q3904B UM6K1N
C3903 10PF/50V
C3902 10PF/50V
R1.0 0106
HDMI HPD Cost Reduced Level Shifter Design Recommendation
23 HDMI_HPD_PCH
HDMI_HPD
R3902 4.7KOhm
HDMI_HPD_CON
D3901 1.25V/0.15A
R3918 10KOhm
R3920 1KOhm HDMI_CLKP_CON
R3921 1KOhm HDMI_CLKN_CON
EMI solution
PEGATRON
Title : HDMI
BG1-HW RD Div.2-NB RD Dept.5
Engineer: Wing_Cheng
Size Custom
Project Name VA70_HW
Rev 1.0
Date: Friday, January 18, 2013
Sheet 39 of 96

From System's PCIE interface



Pin Name	Description
SP1	SD_D7/XD_RDY
SP2	SD_D6/XD_RE#
SP3	SD_D5/XD_CE#
SP4	SD_D4/XD_WE#
SP5	MS_BS/XD_CLE
SP6	MS_D5/XD_ALE
SP7	MS_D1/XD_WP#
SP8	MS_D4/XD_D0
SP9	MS_D0/XD_D1
SP10	MS_D2/XD_D2
SP11	MS_D6/XD_D3
SP12	MS_D3/XD_D4
SP13	MS_D7/XD_D5
SP14	MS_CLK/XD_D6
SP15	SD_WP/XD_D7

SP1	SD_D7		XD_RDY
SP2	SD_D6		XD_RE#
SP3	SD_D5		XD_CE#
SP4	SD_D4		XD_WE#
SP5		MS_BS	XD_CLE
SP6		MS_D5	XD_ALE
SP7		MS_D1	XD_WP#
SP8		MS_D4	XD_D0
SP9		MS_D0	XD_D1
SP10		MS_D2	XD_D2
SP11		MS_D6	XD_D3
SP12		MS_D3	XD_D4
SP13		MS_D7	XD_D5
SP14		MS_CLK	XD_D6
SP15	SD_WP		XD_D7

Share Pin

Remove Serial Flash

Reserve for BIOS boot function

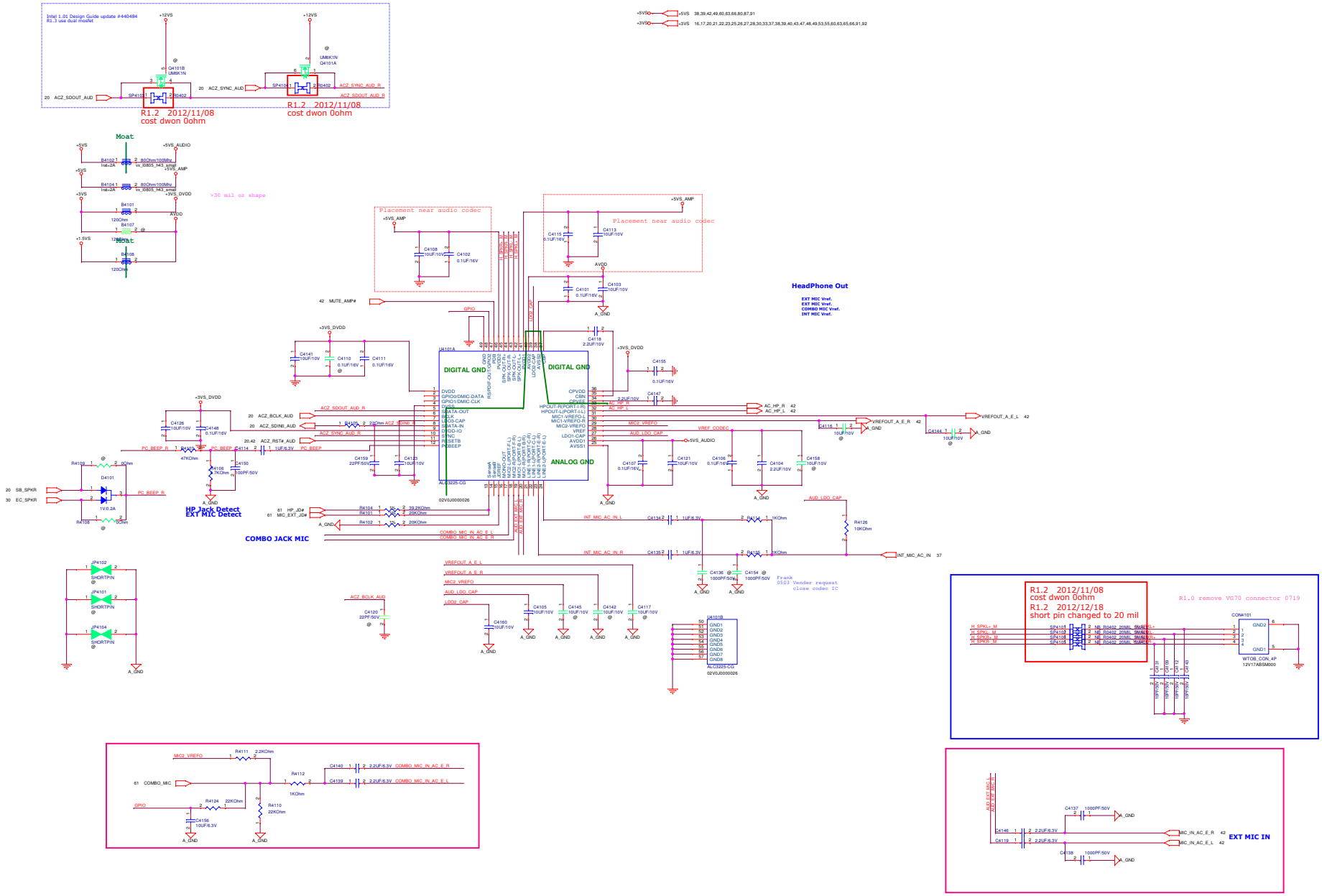
When EECS switch to be D3-Delink sideband signal, Serial Flash function is disabled.

PEGATRON Title : RTS5209

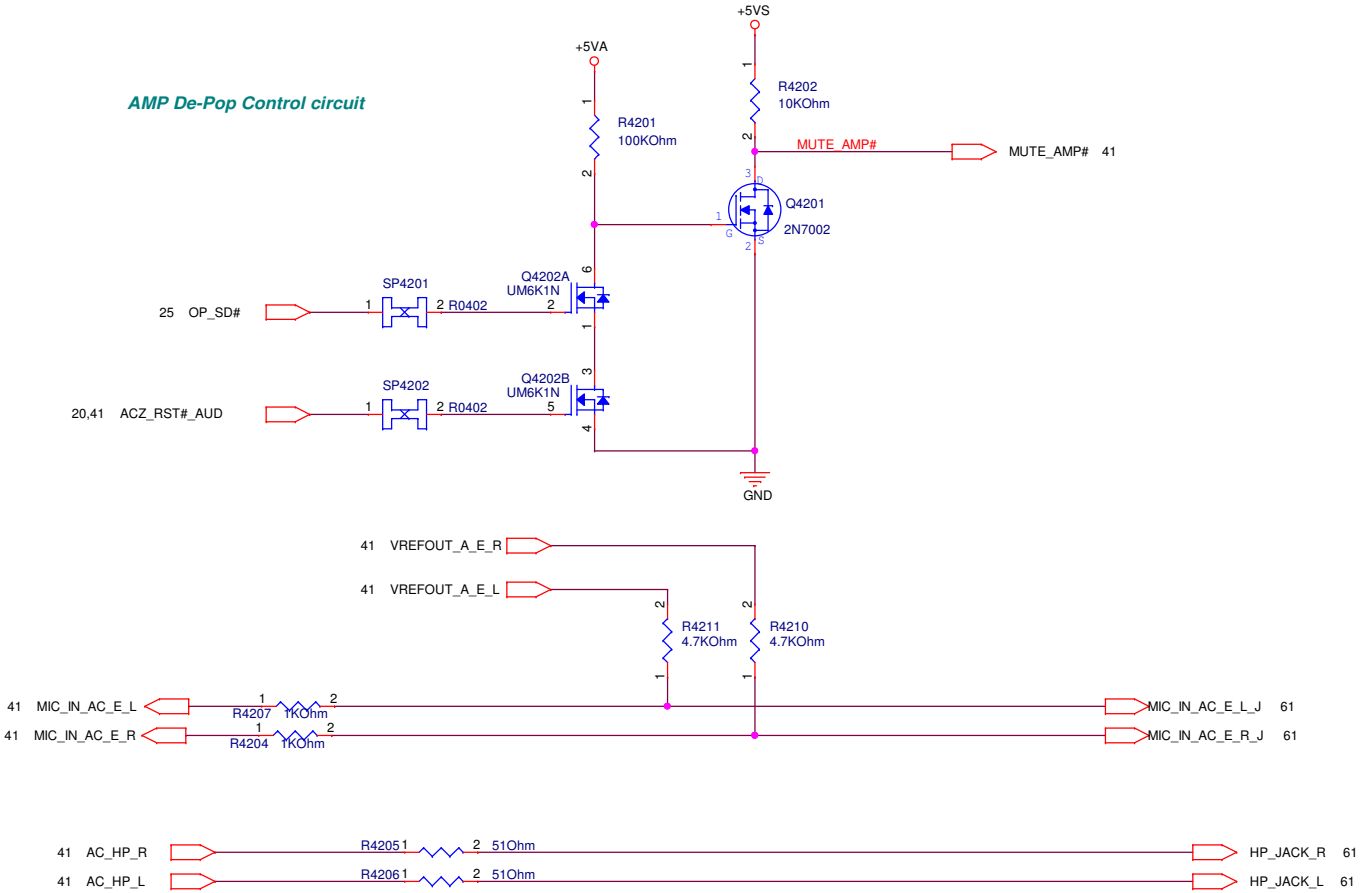
BG1/CSC/HW5 Engineer: Wing_Cheng

Size	Project Name	Rev
C	VA70_HW	1.0

Date: Friday, January 18, 2013 Sheet 40 of 96



PEGATRON	Title : CODEC-ALC3225	
ASUSTeK COMPUTER INC. NB1	Engineer: Wing_Cheng	
Size: D	Project Name: VA70_HW	Rev: 1.0
Date: Friday, January 18, 2013	Sheet 41 of 86	

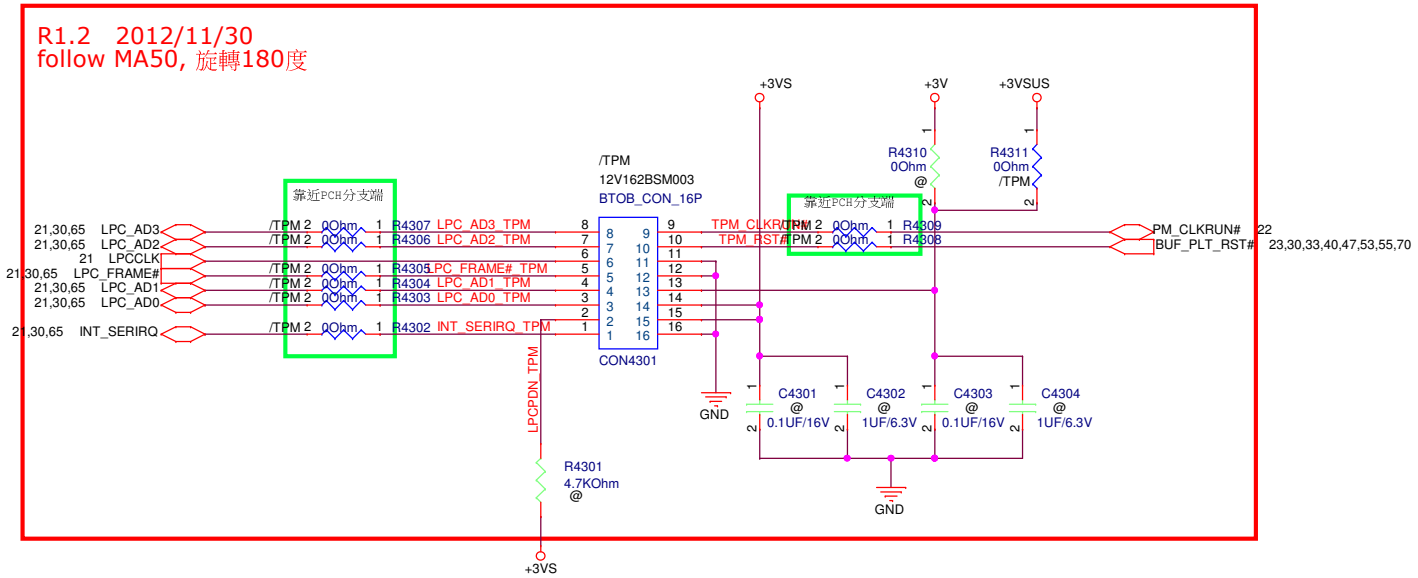


PEGATRON Title : AUDIO ALC269

BU1-RD Div.1-HW RD Dept.1 Engineer: Wing_Cheng

Size	Project Name	Rev
B	VA70_HW	1.0

Date: Friday, January 18, 2013 Sheet 42 of 96



PEGATRON	Title : TPM CONN		
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Wing_Cheng		
Size B	Project Name VA70_HW		Rev 1.0
Date: Friday, January 18, 2013	Sheet 43 of 96		

Del Entry audio circuit

SR-8
0121-11

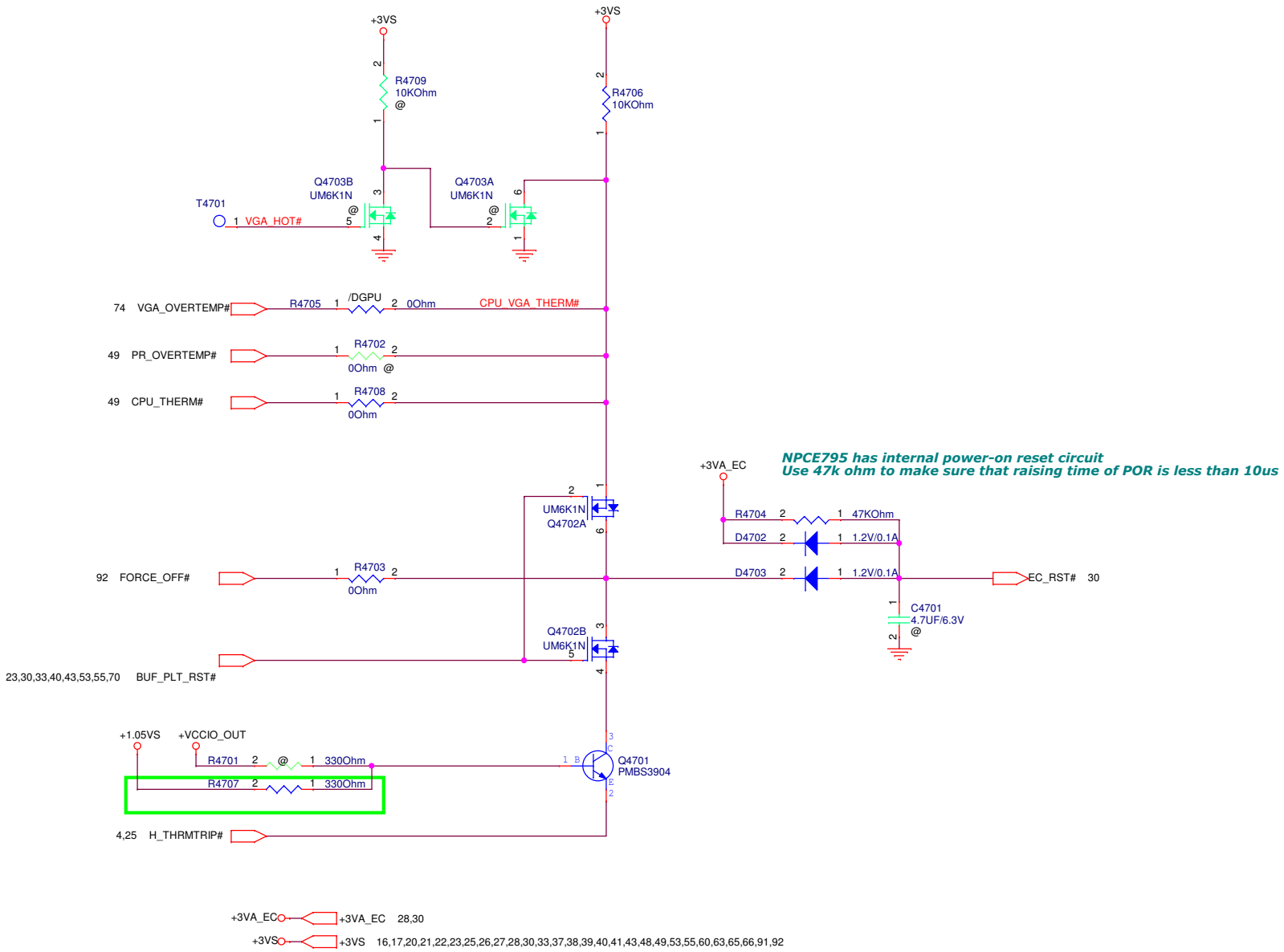
PEGATRON	Title : CODEC-ALC269		
ASUSTeK COMPUTER INC. NB1	Engineer: Wing_Cheng		
Size: Custom	Project Name: VA70_HW		Rev: 1.0
Date: Friday, January 18, 2013	Sheet 44 of 96		

Del Entry audio circuit

SR-8
0121-11

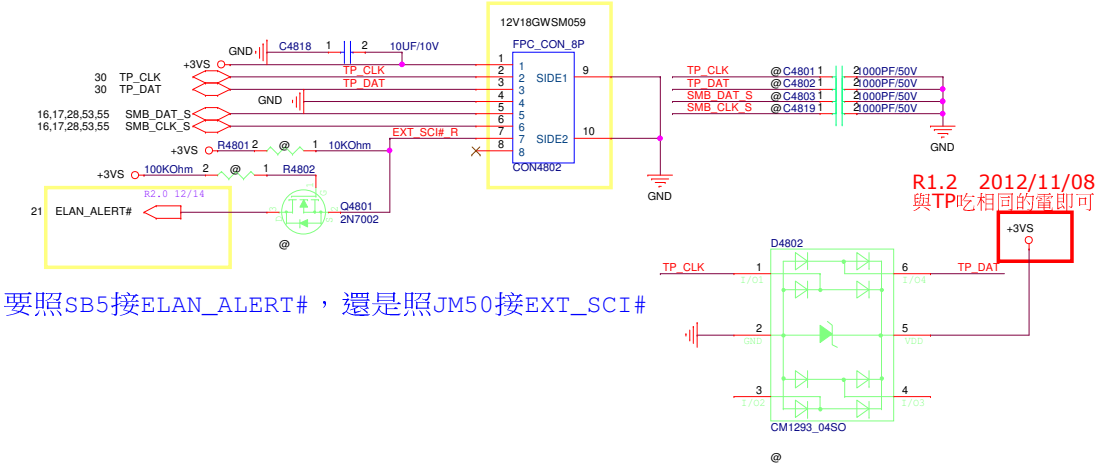
PEGATRON	Title : AUDIO ALC269	
BU1-RD Div.1-HW RD Dept.1	Engineer: Wing_Cheng	
Size: Custom	Project Name: VA70_HW	Rev: 1.0
Date: Friday, January 18, 2013	Sheet 45 of 96	

Thermal Policy



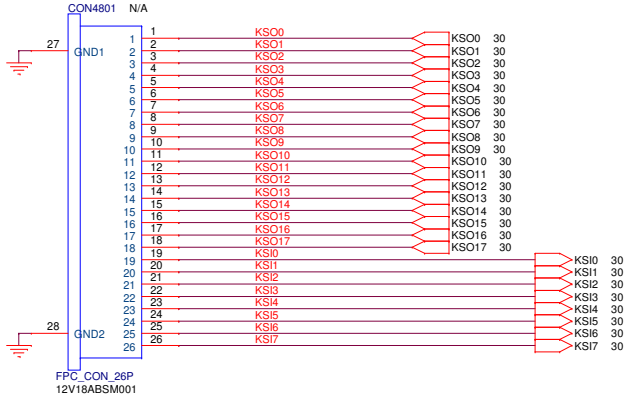
PEGATRON	Title : RST_Reset Circuit	
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Wing_Cheng	
Size B	Project Name VA70_HW	Rev 1.0
Date: Friday, January 25, 2013	Sheet 47 of 96	

Touch Pad Button

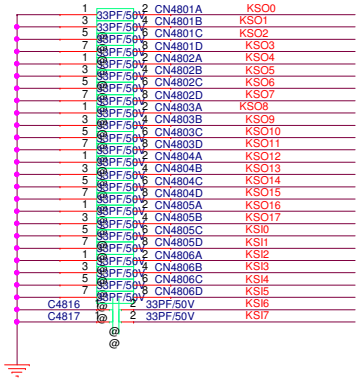


要照SB5接ELAN_ALERT#，還是照JM50接EXT_SCI#

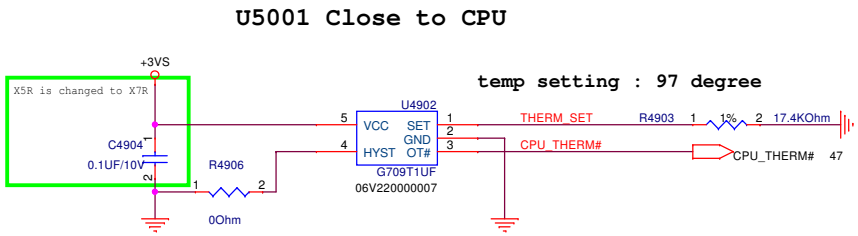
Keyboard

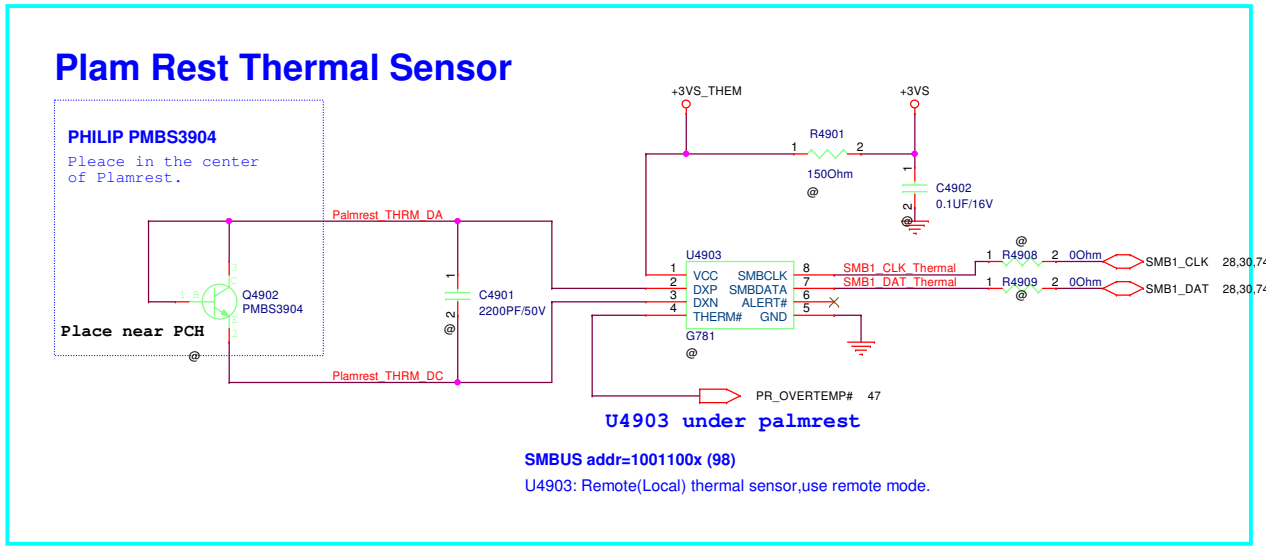


1218-00MW000



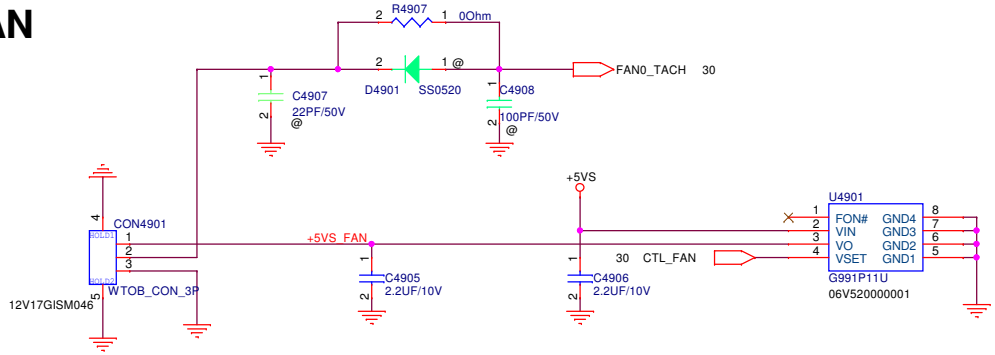
PEGATRON	Title : KB/ TP/ FLASH	
BU1-RD Div.1-HW RD Dept.1	Engineer: Wing_Cheng	
Size: Custom	Project Name: VA70_HW	Rev: 1.0
Date: Friday, January 18, 2013	Sheet 48 of 96	





R1.2-10

FAN



PEGATRON	Title : THERMAL/ FAN	
BU1-RD Div.1-HW RD Dept.1	Engineer: Wing_Cheng	
Size: Custom	Project Name: VA70_HW	Rev: 1.0
Date: Friday, January 18, 2013	Sheet 49 of 96	

PEGATRON	Title : Realtek_RTS5138		
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Wing_Cheng		
Size C	Project Name VA70_HW		Rev 1.0
Date: Friday, January 18, 2013	Sheet 50 of 96		

PEGATRON	Title : USB3.0 uPD720200		
BG1\HW1	Engineer: Wing_Cheng		
Size C	Project Name VA70_HW		Rev 1.0
Date: Friday, January 18, 2013		Sheet 51 of 96	

PEGATRON

Title : PCIE NEW CARD

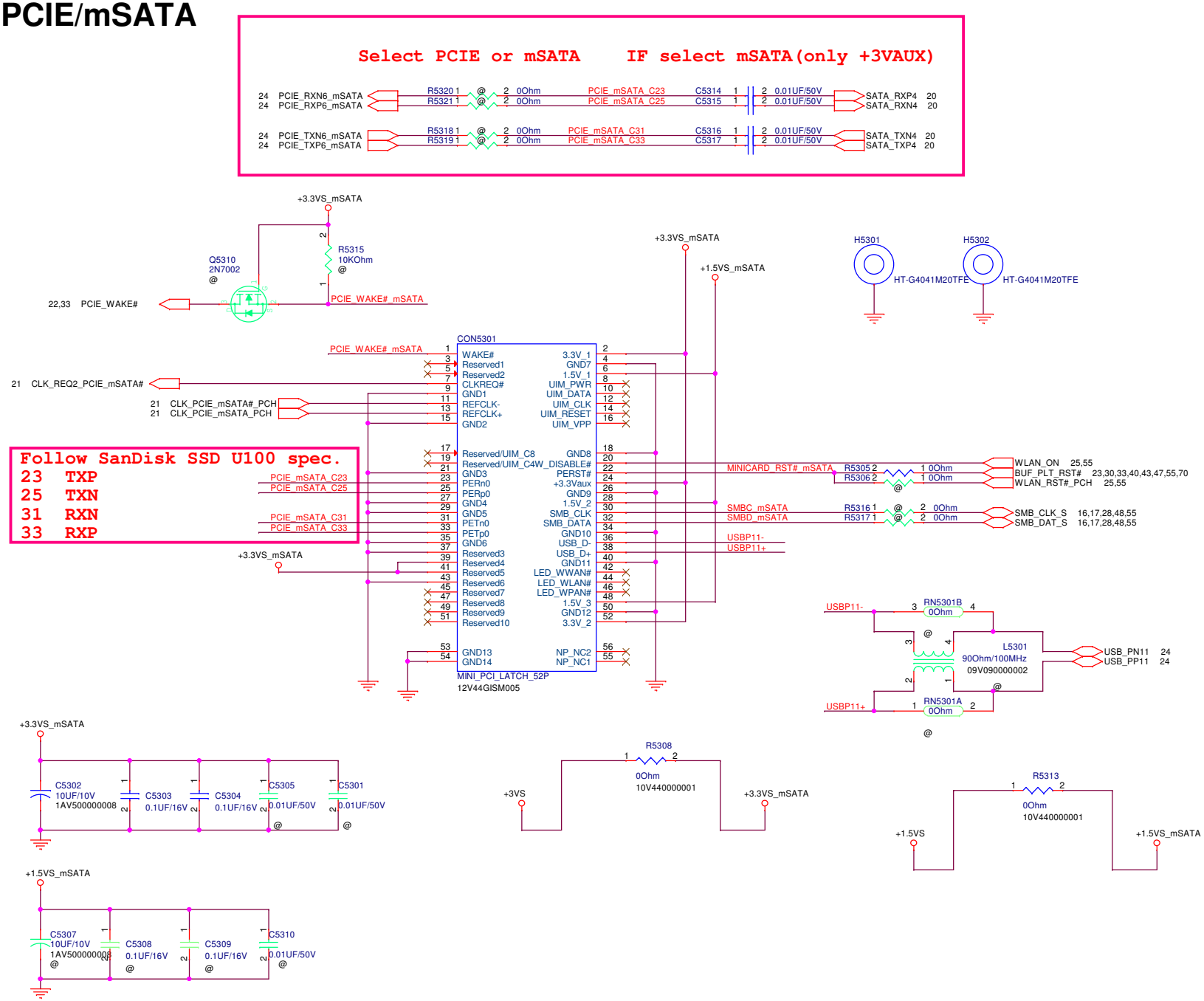
BU1-RD Div.1-HW RD Dept.1

Engineer: *Wing_Cheng*

Size	Project Name	Rev
Custom	VA70_HW	1.0

Date: Friday, January 18, 2013 Sheet 52 of 96

PCIE/mSATA



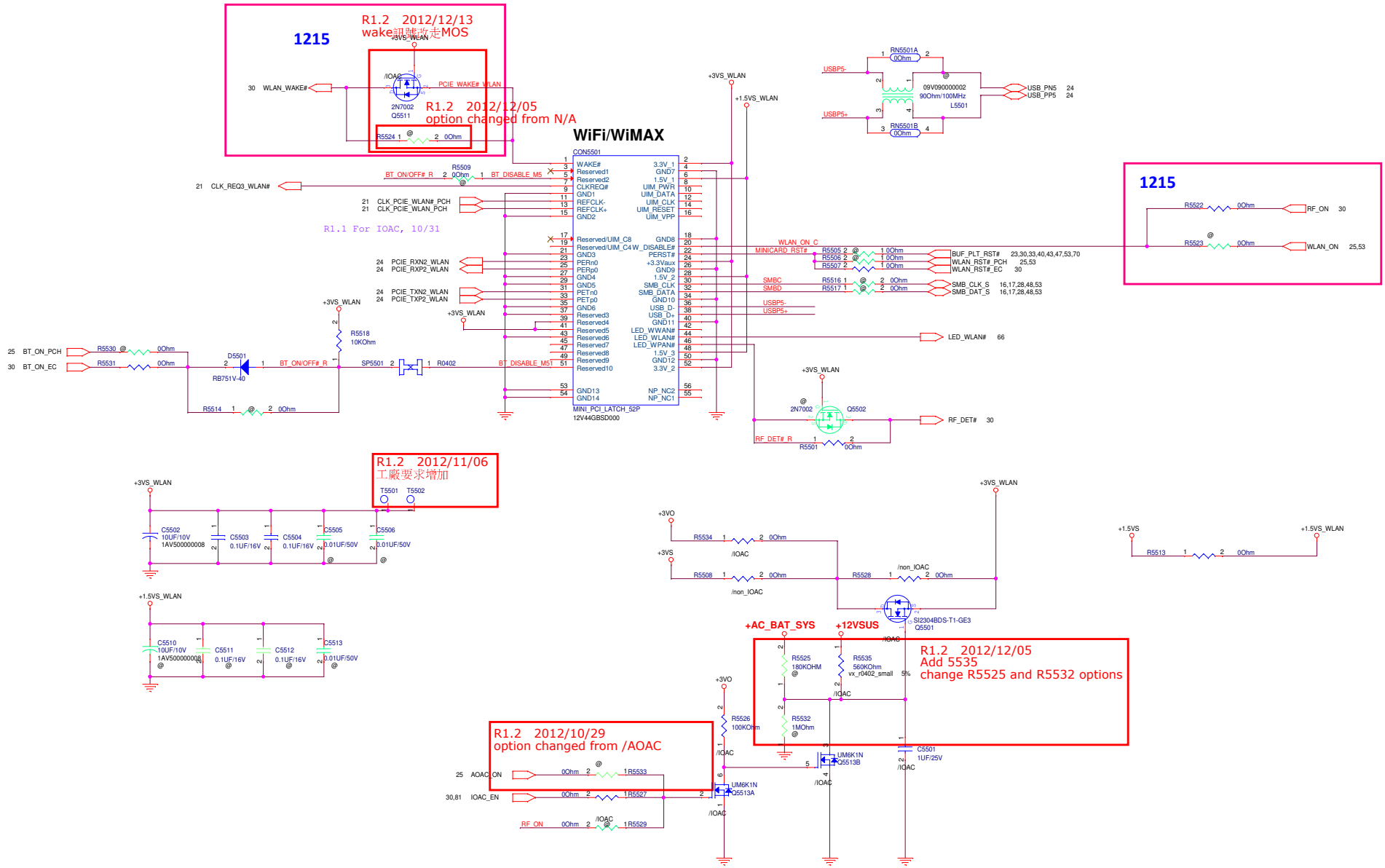
PEGATRON	Title : WiFi/WiMAX	
BU1-RD Div.1-HW RD Dept.1	Engineer:	
Size: Custom	Project Name: VA70_HW	Rev: 1.0
Date: Friday, January 18, 2013	Sheet 53 of 96	

PEGATRON Title : MINICARD (WUSB /UPCONVERT)

BU1-RD Div.1-HW RD Dept.1 Engineer: *Wing_Cheng*

Size	Project Name	Rev
Custom	VA70_HW	1.0

Date: Friday, January 18, 2013 Sheet 54 of 96



PEGATRON Title : WIFIWIMAX

BU1-RD Div.1-HW RD Dept.1 Engineer:

Size	Project Name	Rev
C	VA70_HW	1.0

Date: Friday, January 18, 2013 Sheet 55 of 96

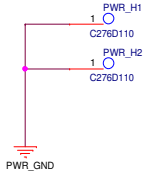
PEGATRON Title : TP_M

BG1-HW RD Div.2-NB RD Dept.5 Engineer: Wing_Cheng

Size	Project Name	Rev
B	VA70_HW	1.0

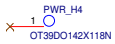
Date: Friday, January 18, 2013 Sheet 56 of 96

Screw G x 2

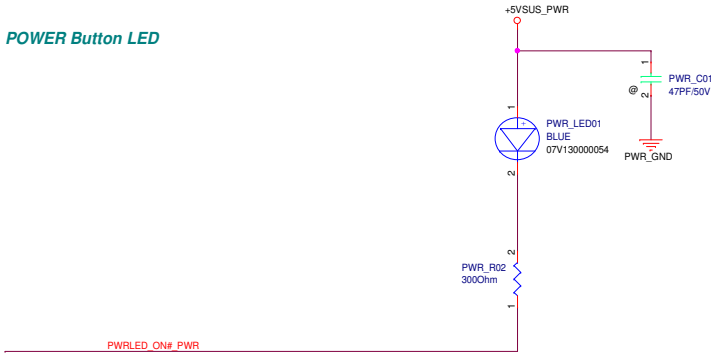


Fix Hole H x 1

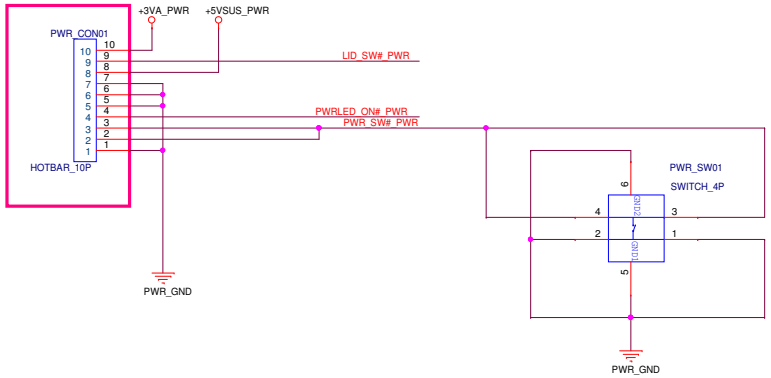
Fix Hole I x 1



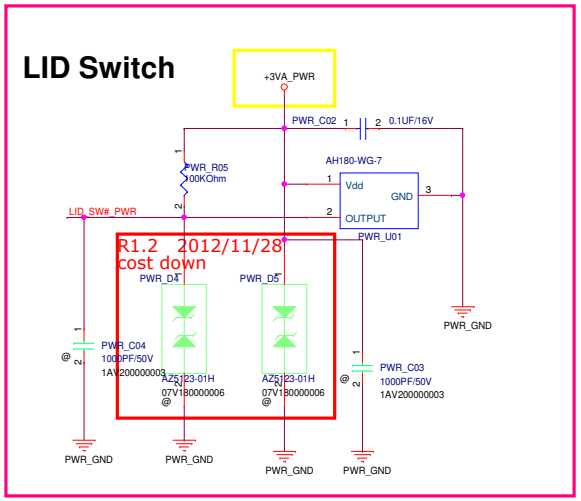
POWER Button LED



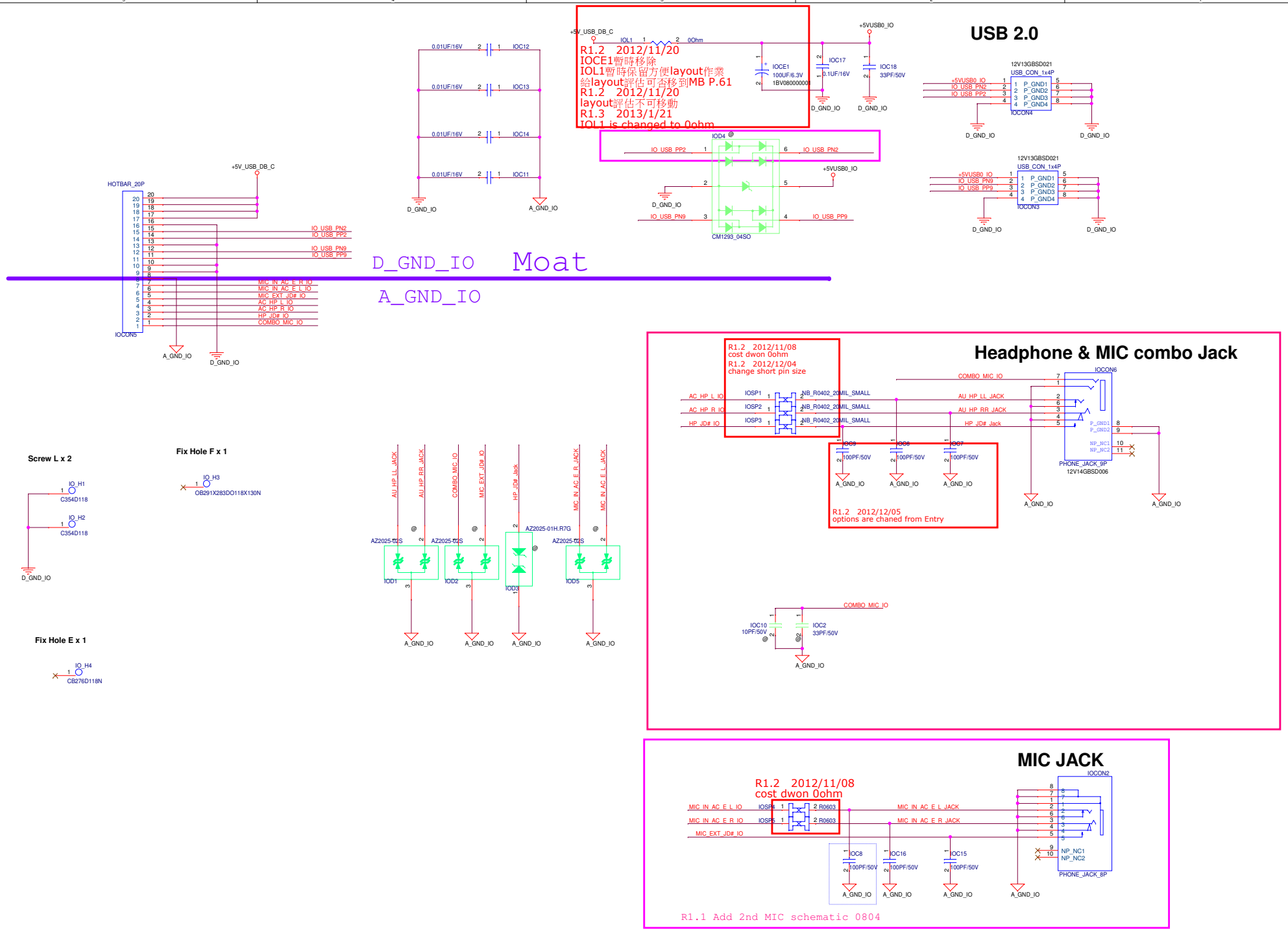
R1.1 reverse PWR_CON01 and change pin 1~4 pin define 1024



LID Switch



PEGATRON	Title : PWR BTN	
BU1-RD Div.1-HW RD Dept.1	Engineer: Wing_Cheng	
Size: Custom	Project Name: VA70_HW	Rev: 1.0
Date: Friday, January 18, 2013	Sheet 57 of 96	



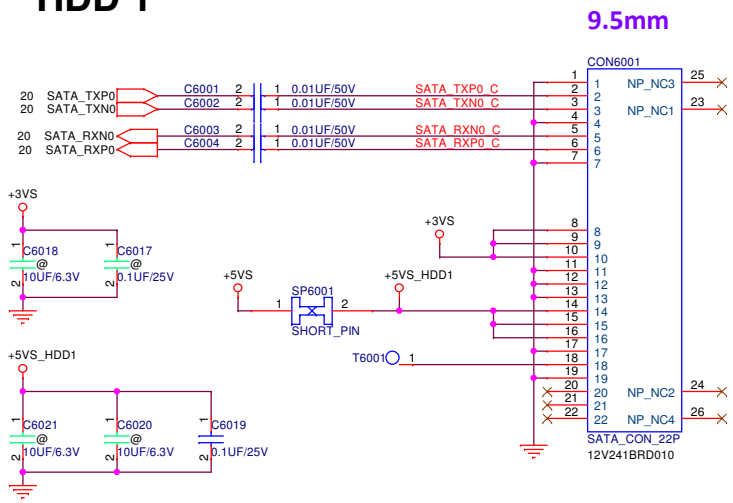
PEGATRON Title : IO

BG1-NB1-HW-NB5 Engineer: Wing_Cheng

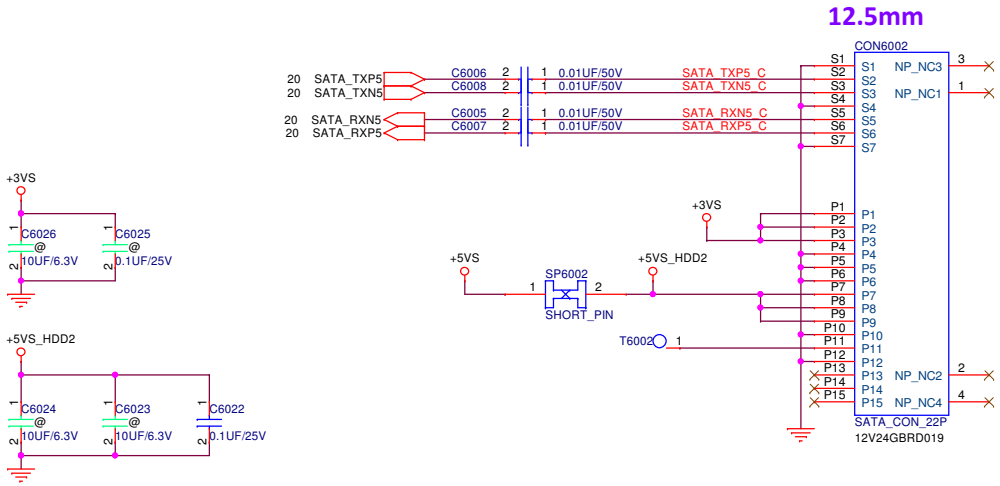
Size	Project Name	Rev
C	VA70_HW	1.0

Date: Monday, January 21, 2013 Sheet 58 of 96

HDD 1



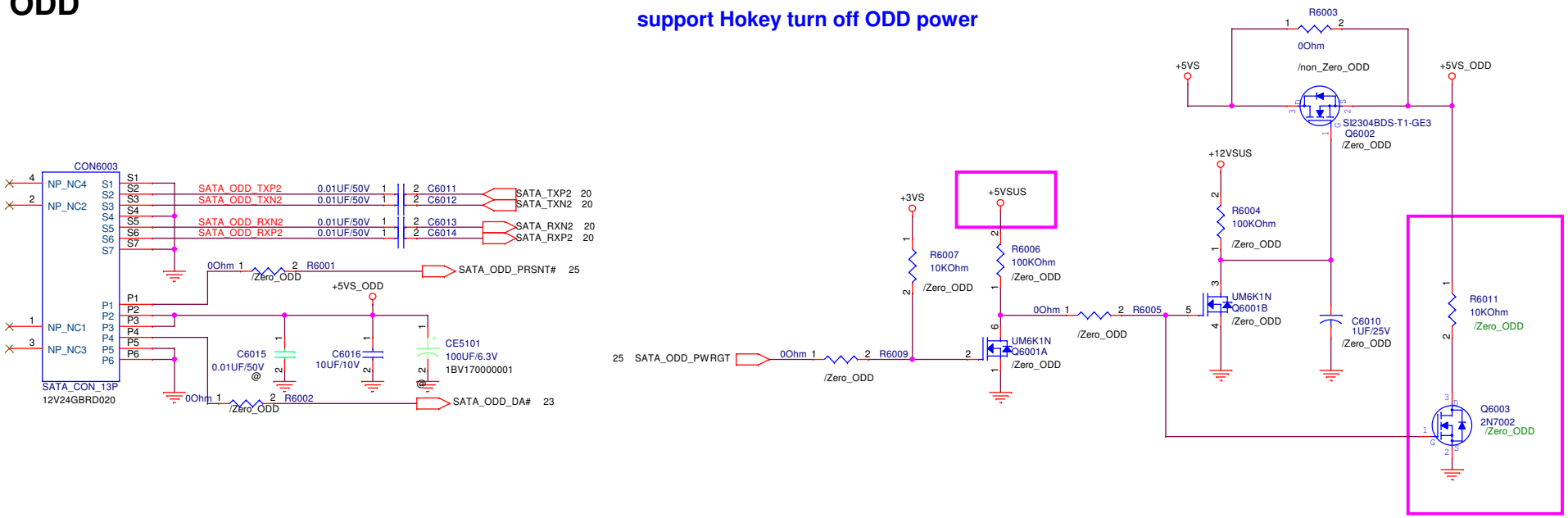
HDD 2



ODD

ZERO POWER ODD SUPPORT

support Hokey turn off ODD power



PEGATRON	Title : SATA HDD/ ODD	
BU1-RD Div.1-HW RD Dept.1	Engineer: Wing_Cheng	
Size: Custom	Project Name: VA70_HW	Rev: 1.0
Date: Friday, January 18, 2013	Sheet 60 of 96	

MB USB

R1.3 2013/1/21
L6110 is changed to 0ohm

USB 3.0

R1.2 2012/11/20
Changed from 560UF/2.5V

Sleep & Charge

no sleep & charge

R1.3 2013/1/21
L6111 is changed to 0ohm

PLACE ESD Diodes 0700-0014000 near Connector

USB 3.0

R1.2 2012/11/20
Changed from 100UF/6.3V
R1.2 2012/11/23
changed from 220UF/6.3V

IO Board

USB Power Switch for USB DB Main

BIOS debug port

AUDIO BOARD/w USB2.0 x2

R1.2 2012/11/20
Add 560UF/2.5V for layout to estimate
R1.2 2012/11/23
changed from 560/2.5V
R1.2 2012/11/27
L6115, CE6105 are removed

A_GND

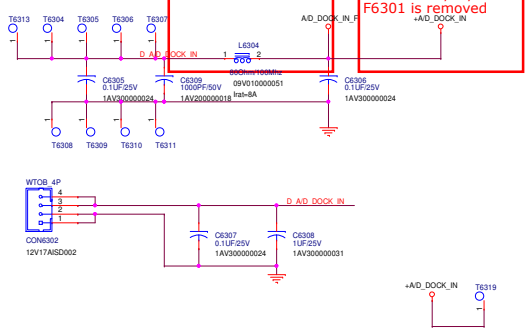
PEGATRON Title : USB PORTS eSATA
Engineer: Wing_Cheng
Size: Custom | Project Name: VA70_HW | Rev: 1.0
Date: Monday, January 21, 2013 | Sheet 61 of 68

PEGATRON	Title : Camera/ BT/ FL CONN		
BU1-RD Div.1-HW RD Dept.1	Engineer: *Wing_Cheng*		
Size	Project Name		Rev
Custom	VA70_HW		1.0
Date: Friday, January 18, 2013		Sheet 62 of 96	

DC IN

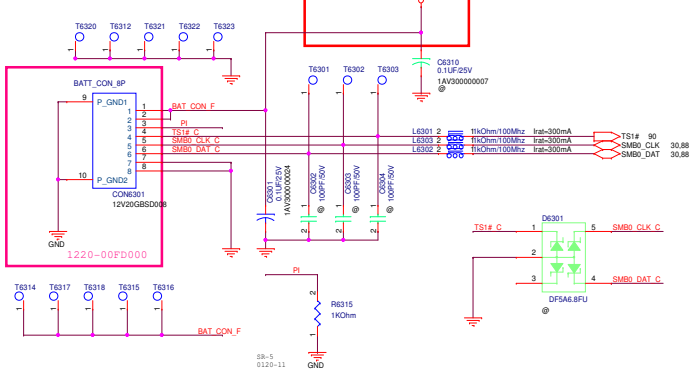
R1.3 2013/1/4
L6304 is changed to Irat=8A

R1.2 2012/11/21
F6301 is removed



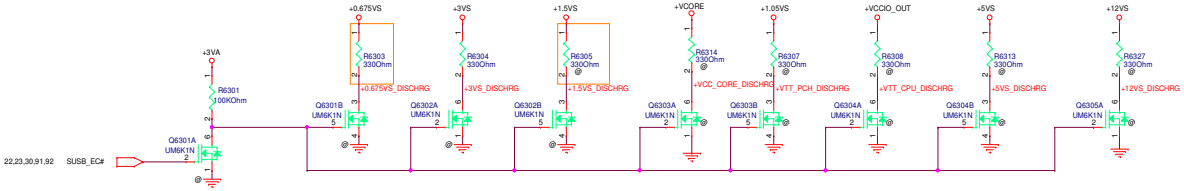
Battery Connector

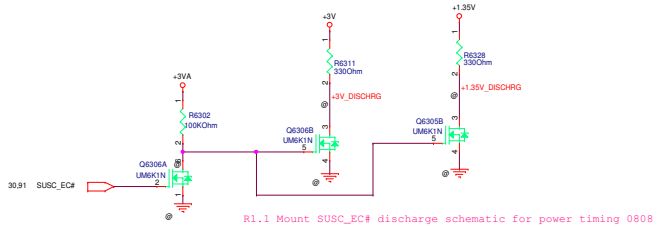
R1.2 2012/11/21
F6301 is removed



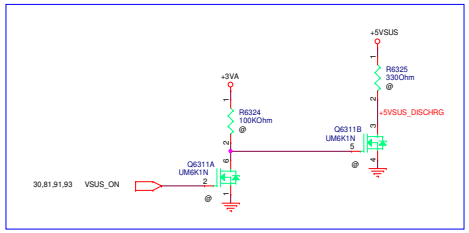
Discharge Circuit

Frank
0505 Follow EVEREST





R1.1 Mount SUSC_EC# discharge schematic for power timing 0808



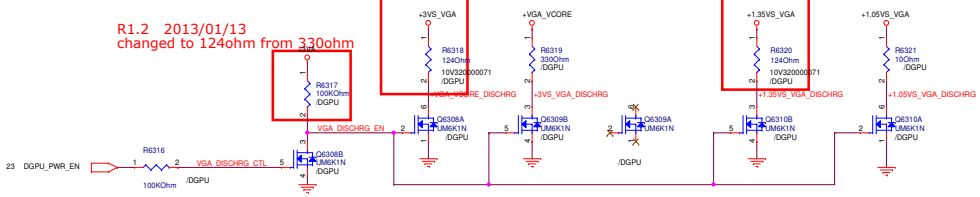
VGA Discharge Circuit

R1.2 2013/01/13
changed to 124ohm from 330ohm

R1.2 2013/01/02
changed to 124ohm from 330ohm

R1.2 2012/12/10
changed to +1.35VS_VGA

R1.2 2013/01/02
changed to 124ohm from 330ohm

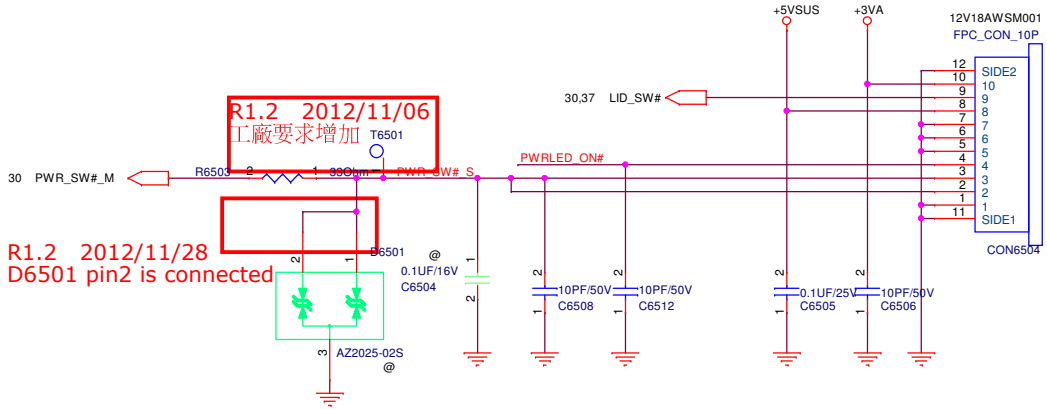


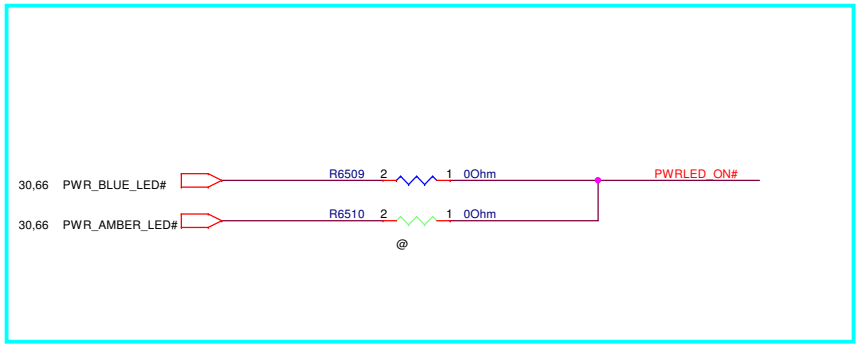
Unmount +VGA_Vcore discharg

PEGATRON	Title : DC-IN/ DISCHARGE		
BU1-RD Div.1-HW RD Dept.1	Engineer: Wing_Cheng		
Size: Custom	Project Name: VA70_HW		Rev: 1.0
Date: Friday, January 18, 2013	Sheet 63 of 96		

PEGATRON	Title: 2SC-IN DISCHARGE		
Size: A	Project Name: VA70_HW	Engineer: Wing_Chang	Rev: 1.0
Date: Friday, January 18, 2013		Sheet 1 of 1	

PWR BRD/ AMBIENT/ HALL CONN.



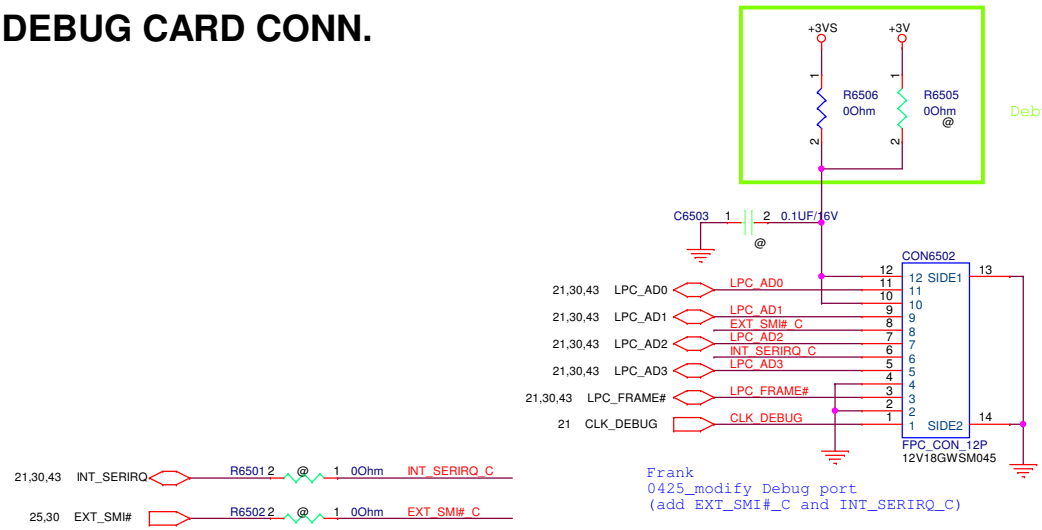


R1.2-28

change Power LED CON6503 circuit

R1.0 remove VG70 POWER connector CON6503 0719

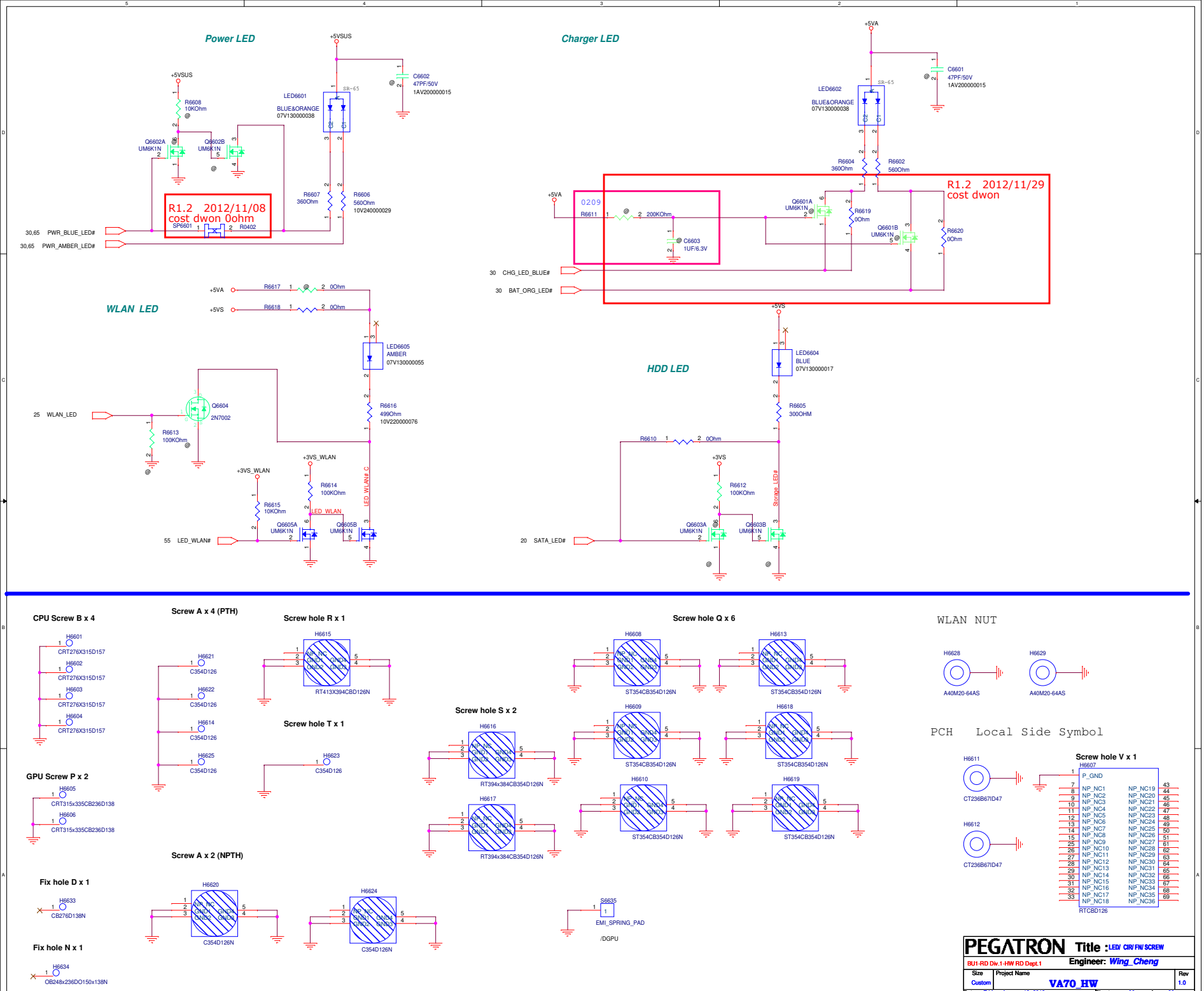
DEBUG CARD CONN.



Frank
0425_modify Debug port
(add EXT_SMI#_C and INT_SERIRQ_C)

CR R1.0 change part for EOL. Joyoung0803
PS. Pin define is reverse.

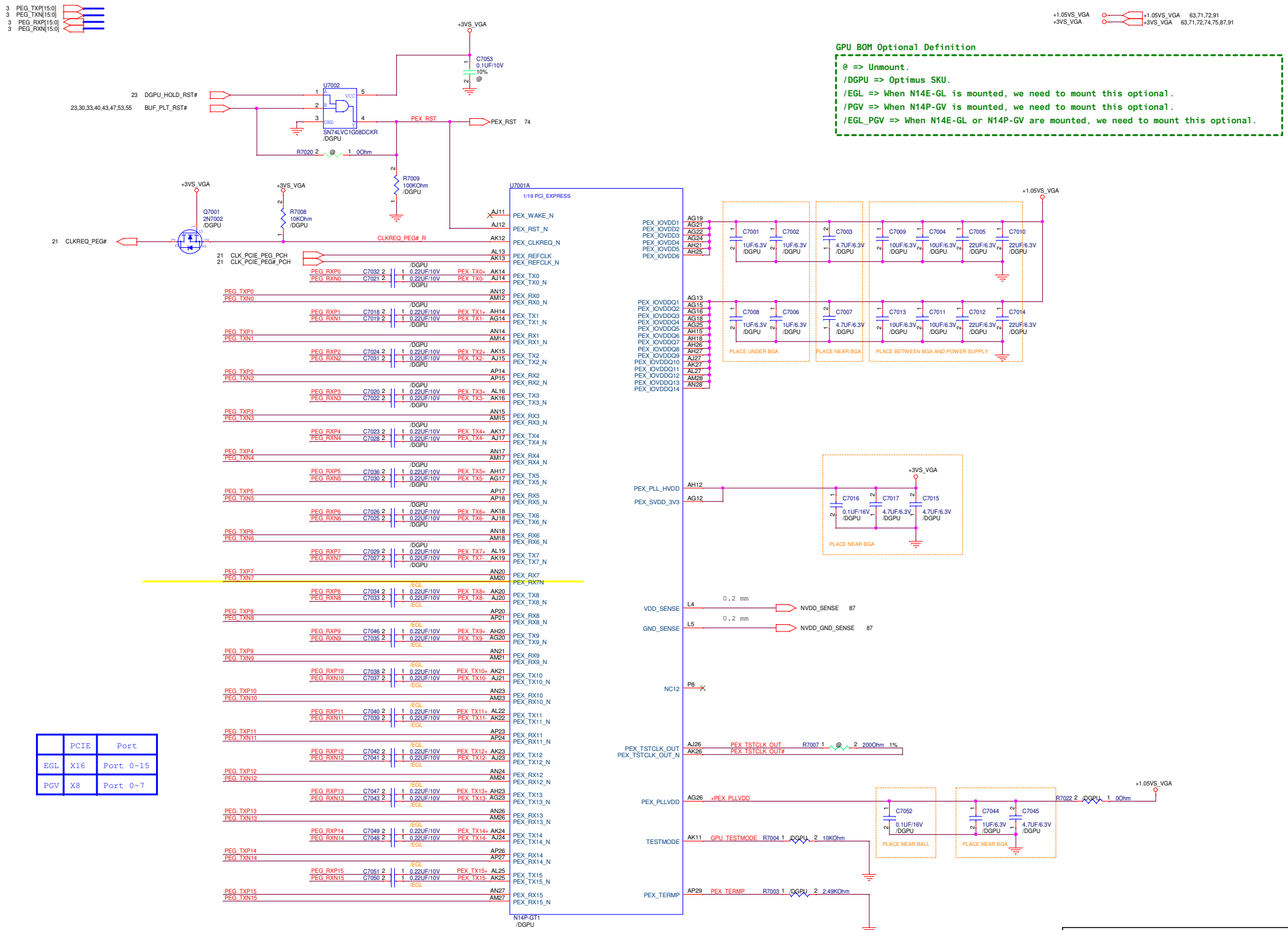
PEGATRON	Title : MDC/ PWR SW/ Debug		
BU1-RD Div.1-HW RD Dept.1	Engineer: Wing_Cheng		
Size: Custom	Project Name: VA70_HW		Rev: 1.0
Date: Friday, January 18, 2013	Sheet 65 of 96		


Power LED
+5VSUS
R6608
10KOhm
Q6602A
UM6K1N
Q6602B
UM6K1N
LED6601
BLUE&ORANGE
07V130000038
C6602
47PF/50V
1AV200000015
R6607
360Ohm
R6606
560Ohm
10V240000029
R1.2 2012/11/08
cost dwon 0ohm
SP6601
R0402
30,65 PWR_BLUE_LED#
30,65 PWR_AMBER_LED#
Charger LED
+5VA
C6601
47PF/50V
1AV200000015
LED6602
BLUE&ORANGE
07V130000038
R6604
360Ohm
R6602
560Ohm
R1.2 2012/11/29
cost dwon
0209
R6611
200KOhm
C6603
1UF/6.3V
Q6601A
UM6K1N
R6619
0Ohm
Q6601B
UM6K1N
R6620
0Ohm
30 CHG_LED_BLUE#
30 BAT_ORG_LED#
WLAN LED
+5VA
+5VS
R6617
0Ohm
R6618
0Ohm
LED6605
AMBER
07V130000055
Q6604
2N7002
25 WLAN_LED
R6613
100KOhm
R6616
499Ohm
10V220000076
+3VS_WLAN
R6615
10KOhm
R6614
100KOhm
LED_WLAN
LED_WLAN# C
Q6605A
UM6K1N
Q6605B
UM6K1N
55 LED_WLAN#
HDD LED
+5VS
LED6604
BLUE
07V130000017
R6605
300OHM
R6610
0Ohm
+3VS
R6612
100KOhm
Storage_LED#
Q6603A
UM6K1N
Q6603B
UM6K1N
20 SATA_LED#
CPU Screw B x 4
H6601
CRT276X315D157
H6602
CRT276X315D157
H6603
CRT276X315D157
H6604
CRT276X315D157
GPU Screw P x 2
H6605
CRT315x335CB236D138
H6606
CRT315x335CB236D138
Fix hole D x 1
H6633
CB276D138N
Fix hole N x 1
H6634
OB248x236DO150x138N
Screw A x 4 (PTH)
H6621
C354D126
H6622
C354D126
H6614
C354D126
H6625
C354D126
Screw A x 2 (NPTH)
H6620
C354D126N
H6624
C354D126N
Screw hole R x 1
H6615
RT413X394CBD126N
Screw hole T x 1
H6623
C354D126
Screw hole S x 2
H6616
RT394x384CB354D126N
H6617
RT394x384CB354D126N
Screw hole Q x 6
H6608
ST354CB354D126N
H6613
ST354CB354D126N
H6609
ST354CB354D126N
H6618
ST354CB354D126N
H6610
ST354CB354D126N
H6619
ST354CB354D126N
S6635
EMI_SPRING_PAD
/DGPU
WLAN NUT
H6628
A40M20-64AS
H6629
A40M20-64AS
PCH Local Side Symbol
H6611
CT236B67ID47
H6612
CT236B67ID47
Screw hole V x 1
H6607
P_GND
NP_NC1
NP_NC2
NP_NC3
NP_NC4
NP_NC5
NP_NC6
NP_NC7
NP_NC8
NP_NC9
NP_NC10
NP_NC11
NP_NC12
NP_NC13
NP_NC14
NP_NC15
NP_NC16
NP_NC17
NP_NC18
NP_NC19
NP_NC20
NP_NC21
NP_NC22
NP_NC23
NP_NC24
NP_NC25
NP_NC26
NP_NC27
NP_NC28
NP_NC29
NP_NC30
NP_NC31
NP_NC32
NP_NC33
NP_NC34
NP_NC35
NP_NC36
RTCBD126
PEGATRON
Title : LED/ CIR/ FN/ SCREW
BU1-RD Div.1-HW RD Dept.1
Engineer: Wing_Cheng
Size Custom
Project Name VA70_HW
Rev 1.0
Date: Friday, January 18, 2013
Sheet 66 of 96

PEGATRON	Title : TPM		
Pegatron Corp.	Engineer: Wing_Cheng		
Size B	Project Name VA70_HW		Rev 1.0
Date: Friday, January 18, 2013	Sheet 67 of 96		

PEGATRON	Title : Finger Printer		
Pegatron Corp.	Engineer:	Wing_Cheng	
Size	Project Name		Rev
A	VA70_HW		1.0
Date: Friday, January 18, 2013	Sheet 68 of 96		

PEGATRON	Title : G-Sensor TSH35TR		
BU1-RD Div.1-HW RD Dept.1	Engineer: Wing_Cheng		
Size A	Project Name		Rev 1.0
Date: Friday, January 18, 2013		Sheet 69 of 96	



GPU BOM Optional Definition

@ => Unmount.
/DGPU => Optimus SKU.
/EGL => When N14E-GL is mounted, we need to mount this optional.
/PGV => When N14P-GV is mounted, we need to mount this optional.
/EGL_PGV => When N14E-GL or N14P-GV are mounted, we need to mount this optional.

	PCIE	Port
EGL	X16	Port 0~15
PGV	X8	Port 0~7

PEGATRON
PEGATRON COMPUTER INC
Title : N14xxx-PCIE
Engineer: Panda_Wang
Size C
Project Name VA70_HW
Rev 1.3
P/N
Date: Friday, January 18, 2013
Sheet 70 of 99

76,77 FBAD[0..63]
76,77 FBA_DBI[0..7]
76,77 FBA_EDC[0..7]
76,77 FBA_CMD[0..31]

78,79 FBBD[0..63]
78,79 FBB_DBI[0..7]
78,79 FBB_EDC[0..7]
78,79 FBB_CMD[0..31]

+1.05VS_VGA 63,70,72,91
+1.35VS_VGA 63,75,76,77,78,79,84
+3VS_VGA 63,70,72,74,75,87,91

U7001B
2/19 FBA

BOT SIDE

FBAD0	L28	FBA_D0	
FBAD1	M29	FBA_D1	
FBAD2	L29	FBA_D2	
FBAD3	M28	FBA_D3	
FBAD4	N31	FBA_D4	
FBAD5	P29	FBA_D5	
FBAD6	R29	FBA_D6	
FBAD7	P28	FBA_D7	
FBAD8	J28	FBA_D8	
FBAD9	H29	FBA_D9	
FBAD10	J29	FBA_D10	
FBAD11	H28	FBA_D11	
FBAD12	G29	FBA_D12	
FBAD13	E31	FBA_D13	
FBAD14	E32	FBA_D14	
FBAD15	F30	FBA_D15	
FBAD16	C34	FBA_D16	
FBAD17	D32	FBA_D17	
FBAD18	B33	FBA_D18	
FBAD19	C33	FBA_D19	
FBAD20	F33	FBA_D20	
FBAD21	F32	FBA_D21	
FBAD22	H33	FBA_D22	
FBAD23	H32	FBA_D23	
FBAD24	P34	FBA_D24	
FBAD25	P32	FBA_D25	
FBAD26	P31	FBA_D26	
FBAD27	P33	FBA_D27	
FBAD28	L31	FBA_D28	
FBAD29	L34	FBA_D29	
FBAD30	L32	FBA_D30	
FBAD31	L33	FBA_D31	
FBAD32	AG28	FBA_D32	
FBAD33	AF29	FBA_D33	
FBAD34	AG29	FBA_D34	
FBAD35	AF28	FBA_D35	
FBAD36	AD30	FBA_D36	
FBAD37	AD29	FBA_D37	
FBAD38	AC29	FBA_D38	
FBAD39	AD28	FBA_D39	
FBAD40	AJ29	FBA_D40	
FBAD41	AK29	FBA_D41	
FBAD42	AJ30	FBA_D42	
FBAD43	AK28	FBA_D43	
FBAD44	AM29	FBA_D44	
FBAD45	AM31	FBA_D45	
FBAD46	AN29	FBA_D46	
FBAD47	AM30	FBA_D47	
FBAD48	AN31	FBA_D48	
FBAD49	AN32	FBA_D49	
FBAD50	AP30	FBA_D50	
FBAD51	AP32	FBA_D51	
FBAD52	AM33	FBA_D52	
FBAD53	AL31	FBA_D53	
FBAD54	AK33	FBA_D54	
FBAD55	AK32	FBA_D55	
FBAD56	AD34	FBA_D56	
FBAD57	AD32	FBA_D57	
FBAD58	AC30	FBA_D58	
FBAD59	AD33	FBA_D59	
FBAD60	AF31	FBA_D60	
FBAD61	AG34	FBA_D61	
FBAD62	AG32	FBA_D62	
FBAD63	AG33	FBA_D63	

FBA_DBI0	P30	FBA_DQM0	
FBA_DBI1	F31	FBA_DQM1	
FBA_DBI2	F34	FBA_DQM2	
FBA_DBI3	M32	FBA_DQM3	
FBA_DBI4	AD31	FBA_DQM4	
FBA_DBI5	AL29	FBA_DQM5	
FBA_DBI6	AM32	FBA_DQM6	
FBA_DBI7	AF34	FBA_DQM7	

FBA_EDC0	M31	FBA_DQS_WP0	
FBA_EDC1	G31	FBA_DQS_WP1	
FBA_EDC2	E33	FBA_DQS_WP2	
FBA_EDC3	M33	FBA_DQS_WP3	
FBA_EDC4	AE31	FBA_DQS_WP4	
FBA_EDC5	AK30	FBA_DQS_WP5	
FBA_EDC6	AN33	FBA_DQS_WP6	
FBA_EDC7	AF33	FBA_DQS_WP7	

M30		FBA_DQS_RN0	
H30		FBA_DQS_RN1	
E34		FBA_DQS_RN2	
M34		FBA_DQS_RN3	
AF30		FBA_DQS_RN4	
AK31		FBA_DQS_RN5	
AM34		FBA_DQS_RN6	
AF32		FBA_DQS_RN7	

T7101 1 H26 FBA_VREF

N14P-GT1
/DGPU

FB_CLAMP — E1 FB_CLAMP_R — R7121 2 /DGPU 1 0Ohm — FB_CLAMP — FB_CLAMP 30,74,84

R7130 2 /DGPU 1 10KOhm — GND

FB_DLL_AVDD — K27 +FB_DLL_AVDD_R — GND — L7102 1 /DGPU 2 30Ohm/100Mhz — +1.05VS_VGA

50mA C7115 0.1UF/10V 10% /DGPU

C7121 22UF/6.3V /DGPU

FB_DLL_AVDD		
EGL	1.05V	50mA
PGV		35mA

20121212(Eli)
FB_DLL_AVDD table follow NV
SPEC DG_06246_001_V04
Page121

FBA_CMD0	U30	FBA_CMD0	
FBA_CMD1	T31	FBA_CMD1	
FBA_CMD2	U29	FBA_CMD2	
FBA_CMD3	R34	FBA_CMD3	
FBA_CMD4	R33	FBA_CMD4	
FBA_CMD5	U32	FBA_CMD5	
FBA_CMD6	U33	FBA_CMD6	
FBA_CMD7	U28	FBA_CMD7	
FBA_CMD8	V28	FBA_CMD8	
FBA_CMD9	V29	FBA_CMD9	
FBA_CMD10	V30	FBA_CMD10	
FBA_CMD11	U34	FBA_CMD11	
FBA_CMD12	U31	FBA_CMD12	
FBA_CMD13	V34	FBA_CMD13	
FBA_CMD14	V33	FBA_CMD14	
FBA_CMD15	Y32	FBA_CMD15	
FBA_CMD16	AA31	FBA_CMD16	
FBA_CMD17	AA29	FBA_CMD17	
FBA_CMD18	AA28	FBA_CMD18	
FBA_CMD19	AC34	FBA_CMD19	
FBA_CMD20	AC33	FBA_CMD20	
FBA_CMD21	AA32	FBA_CMD21	
FBA_CMD22	AA33	FBA_CMD22	
FBA_CMD23	Y28	FBA_CMD23	
FBA_CMD24	Y29	FBA_CMD24	
FBA_CMD25	W31	FBA_CMD25	
FBA_CMD26	Y30	FBA_CMD26	
FBA_CMD27	AA34	FBA_CMD27	
FBA_CMD28	Y31	FBA_CMD28	
FBA_CMD29	Y34	FBA_CMD29	
FBA_CMD30	Y33	FBA_CMD30	
FBA_CMD31	V31	FBA_CMD31	

+1.35VS_VGA

FBA_CMD14 R7124 2 /DGPU 1 10KOhm

FBA_CMD30 R7123 2 /DGPU 1 10KOhm

FBA_CMD29 R7125 2 /DGPU 1 10KOhm

FBA_CMD13 R7126 2 /DGPU 1 10KOhm

GND

FBA_CMD_RFU0 R32
FBA_CMD_RFU1 AC32

+1.35VS_VGA

FBA_DEBUG0 R28 FBA_DEBUG0 R7101 1 @ 2 60.4Ohm 1%
FBA_DEBUG1 AC28 FBA_DEBUG1 R7102 1 @ 2 60.4Ohm 1%

FBA_CLK0	R30	FBA_CLK0	76
FBA_CLK0_N	R31	FBA_CLK0#	76
FBA_CLK1	AB31	FBA_CLK1	77
FBA_CLK1_N	AC31	FBA_CLK1#	77

FBA_WCK01	K31	FBA_WCK01	76
FBA_WCK01_N	L30	FBA_WCK01#	76
FBA_WCK23	H34	FBA_WCK23	76
FBA_WCK23_N	J34	FBA_WCK23#	76
FBA_WCK45	AG30	FBA_WCK45	77
FBA_WCK45_N	AG31	FBA_WCK45#	77
FBA_WCK67	AJ34	FBA_WCK67	77
FBA_WCK67_N	AK34	FBA_WCK67#	77

FBA_WCKB01	J30	
FBA_WCKB01_N	J31	
FBA_WCKB23	J32	
FBA_WCKB23_N	J33	
FBA_WCKB45	AH31	
FBA_WCKB45_N	AJ31	
FBA_WCKB67	AJ32	
FBA_WCKB67_N	AJ33	

FBA_PLL_AVDD U27 +FB_PLL_AVDD

120mA C7109 0.1UF/10V /DGPU C7119 22UF/6.3V /DGPU

Place Close to BALL Place Close to BGA

+FB_PLL_AVDD +1.05VS_VGA

C7112 1UF/6.3V 10% /DGPU L7101 30Ohm/100Mhz /PGV C7113 1UF/6.3V 10% /PGV

+3VS_VGA

L7103 30Ohm/100Mhz /EGL C7122 1UF/6.3V 10% /EGL

FBx_PLL_AVDD		
EGL	3.3V	120mA
PGV	1.05V	62mA

Place Close to BGA

20121214(Eli)
R7129 change to bead type
30ohm(ESR=0.01ohm) follow
NV FAE recommend

U7001C
3/19 FBB

FBBD0	G9	FBB_D0	
FBBD1	E9	FBB_D1	
FBBD2	G8	FBB_D2	
FBBD3	F9	FBB_D3	
FBBD4	F11	FBB_D4	
FBBD5	G11	FBB_D5	
FBBD6	F12	FBB_D6	
FBBD7	G12	FBB_D7	
FBBD8	G6	FBB_D8	
FBBD9	F5	FBB_D9	
FBBD10	E6	FBB_D10	
FBBD11	F6	FBB_D11	
FBBD12	F4	FBB_D12	
FBBD13	G4	FBB_D13	
FBBD14	E2	FBB_D14	
FBBD15	F3	FBB_D15	
FBBD16	C2	FBB_D16	
FBBD17	D4	FBB_D17	
FBBD18	D3	FBB_D18	
FBBD19	C1	FBB_D19	
FBBD20	B3	FBB_D20	
FBBD21	C4	FBB_D21	
FBBD22	B5	FBB_D22	
FBBD23	C5	FBB_D23	
FBBD24	A11	FBB_D24	
FBBD25	C11	FBB_D25	
FBBD26	D11	FBB_D26	
FBBD27	B11	FBB_D27	
FBBD28	D8	FBB_D28	
FBBD29	A8	FBB_D29	
FBBD30	C8	FBB_D30	
FBBD31	B8	FBB_D31	
FBBD32	F24	FBB_D32	
FBBD33	G23	FBB_D33	
FBBD34	E24	FBB_D34	
FBBD35	G24	FBB_D35	
FBBD36	D21	FBB_D36	
FBBD37	E21	FBB_D37	
FBBD38	G21	FBB_D38	
FBBD39	F21	FBB_D39	
FBBD40	G27	FBB_D40	
FBBD41	D27	FBB_D41	
FBBD42	G26	FBB_D42	
FBBD43	E27	FBB_D43	
FBBD44	E29	FBB_D44	
FBBD45	F29	FBB_D45	
FBBD46	E30	FBB_D46	
FBBD47	D30	FBB_D47	
FBBD48	A32	FBB_D48	
FBBD49	C31	FBB_D49	
FBBD50	C32	FBB_D50	
FBBD51	B32	FBB_D51	
FBBD52	D29	FBB_D52	
FBBD53	A29	FBB_D53	
FBBD54	C29	FBB_D54	
FBBD55	B29	FBB_D55	
FBBD56	B21	FBB_D56	
FBBD57	C23	FBB_D57	
FBBD58	A21	FBB_D58	
FBBD59	C21	FBB_D59	
FBBD60	B24	FBB_D60	
FBBD61	C24	FBB_D61	
FBBD62	B26	FBB_D62	
FBBD63	C26	FBB_D63	

FBB_DBI0	E11	FBB_DQM0	
FBB_DBI1	E3	FBB_DQM1	
FBB_DBI2	A3	FBB_DQM2	
FBB_DBI3	C9	FBB_DQM3	
FBB_DBI4	F23	FBB_DQM4	
FBB_DBI5	F27	FBB_DQM5	
FBB_DBI6	C30	FBB_DQM6	
FBB_DBI7	A24	FBB_DQM7	

FBB_EDC0	D10	FBB_DQS_WP0	
FBB_EDC1	D5	FBB_DQS_WP1	
FBB_EDC2	C3	FBB_DQS_WP2	
FBB_EDC3	B9	FBB_DQS_WP3	
FBB_EDC4	E23	FBB_DQS_WP4	
FBB_EDC5	E28	FBB_DQS_WP5	
FBB_EDC6	B30	FBB_DQS_WP6	
FBB_EDC7	A23	FBB_DQS_WP7	

D9		FBB_DQS_RN0	
E4		FBB_DQS_RN1	
B2		FBB_DQS_RN2	
A9		FBB_DQS_RN3	
D22		FBB_DQS_RN4	
D28		FBB_DQS_RN5	
A30		FBB_DQS_RN6	
B23		FBB_DQS_RN7	

N14P-GT1
/DGPU

FBB_CMD0	D13	FBB_CMD0	
FBB_CMD1	E14	FBB_CMD1	
FBB_CMD2	F14	FBB_CMD2	
FBB_CMD3	A12	FBB_CMD3	
FBB_CMD4	B12	FBB_CMD4	
FBB_CMD5	G14	FBB_CMD5	
FBB_CMD6	B14	FBB_CMD6	
FBB_CMD7	G15	FBB_CMD7	
FBB_CMD8	F15	FBB_CMD8	
FBB_CMD9	E15	FBB_CMD9	
FBB_CMD10	D15	FBB_CMD10	
FBB_CMD11	A14	FBB_CMD11	
FBB_CMD12	D14	FBB_CMD12	
FBB_CMD13	A15	FBB_CMD13	
FBB_CMD14	B15	FBB_CMD14	
FBB_CMD15	C17	FBB_CMD15	
FBB_CMD16	D18	FBB_CMD16	
FBB_CMD17	E18	FBB_CMD17	
FBB_CMD18	F18	FBB_CMD18	
FBB_CMD19	A20	FBB_CMD19	
FBB_CMD20	B20	FBB_CMD20	
FBB_CMD21	C18	FBB_CMD21	
FBB_CMD22	B18	FBB_CMD22	
FBB_CMD23	G18	FBB_CMD23	
FBB_CMD24	G17	FBB_CMD24	
FBB_CMD25	F17	FBB_CMD25	
FBB_CMD26	D16	FBB_CMD26	
FBB_CMD27	A18	FBB_CMD27	
FBB_CMD28	D17	FBB_CMD28	
FBB_CMD29	A17	FBB_CMD29	
FBB_CMD30	B17	FBB_CMD30	
FBB_CMD31	E17	FBB_CMD31	

+1.35VS_VGA

FBB_CMD30 R7119 2 /DGPU 1 10KOhm

FBB_CMD14 R7122 2 /DGPU 1 10KOhm

FBB_CMD29 R7120 2 /DGPU 1 10KOhm

FBB_CMD13 R7127 2 /DGPU 1 10KOhm

GND

FBB_CMD_RFU0 C12
FBB_CMD_RFU1 C20

+1.35VS_VGA

FBB_DEBUG0 G14 FBC_DEBUG0 R7103 1 @ 2 60.4Ohm 1%
FBB_DEBUG1 G20 FBC_DEBUG1 R7104 1 @ 2 60.4Ohm 1%

FBB_CLK0	D12	FBB_CLK0	78
FBB_CLK0_N	E12	FBB_CLK0#	78
FBB_CLK1	E20	FBB_CLK1	79
FBB_CLK1_N	F20	FBB_CLK1#	79

FBB_WCK01	F8	FBB_WCK01	78
FBB_WCK01_N	E8	FBB_WCK01#	78
FBB_WCK23	A5	FBB_WCK23	78
FBB_WCK23_N	A6	FBB_WCK23#	78
FBB_WCK45	D24	FBB_WCK45	79
FBB_WCK45_N	D25	FBB_WCK45#	79
FBB_WCK67	B27	FBB_WCK67	79
FBB_WCK67_N	C27	FBB_WCK67#	79

FBB_WCKB01	D6	
FBB_WCKB01_N	D7	
FBB_WCKB23	C6	
FBB_WCKB23_N	B6	
FBB_WCKB45	F26	
FBB_WCKB45_N	E26	
FBB_WCKB67	A26	
FBB_WCKB67_N	A27	

FBB_PLL_AVDD H17 +FB_PLL_AVDD

120mA C7120 0.1UF/10V 10% /DGPU

Place Close to BALL

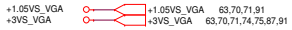
PEGATRON
PEGATRON COMPUTER INC

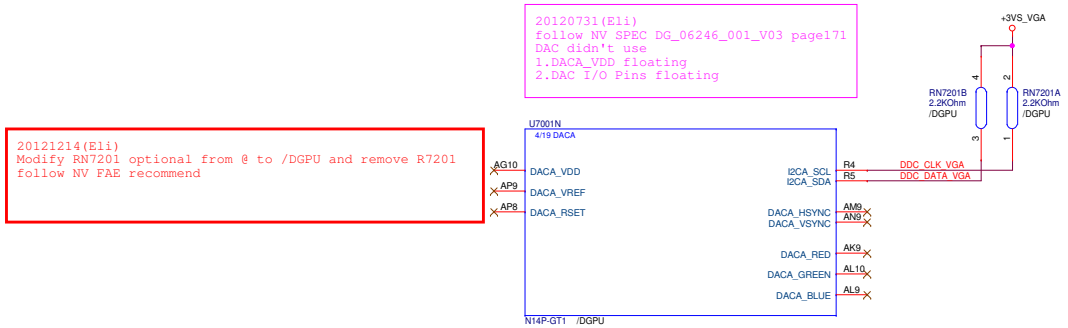
Title : N14xxx BUFFER
Engineer: Panda_Wang

Size	Project Name	Rev
C	VA70_HW	1.3
	P/N	

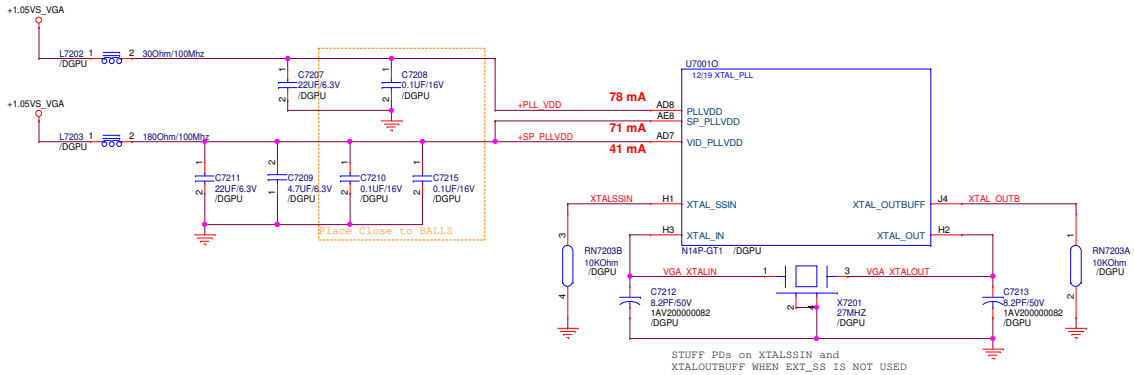
Date: Friday, January 18, 2013 Sheet 71 of 99

VGA



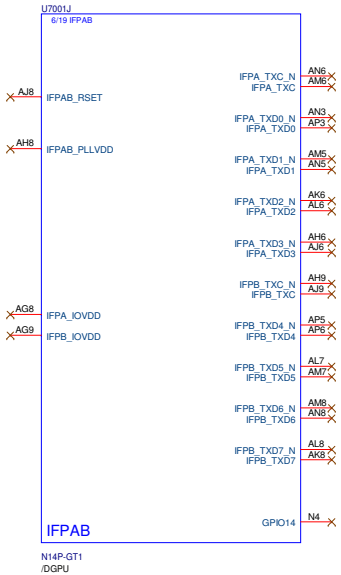


X'TAL



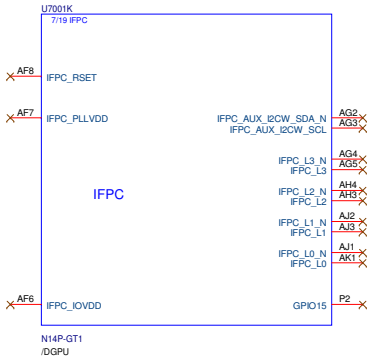
PEGATRON	Title : N14xxx_RGB,XTAL		
PEGATRON COMPUTER INC	Engineer: Panda_Wang		
Size C	Project Name VA70_HW		Rev 1.3
	P/N		
Date: Friday, January 18, 2013	Sheet 72 of 99		

LVDS

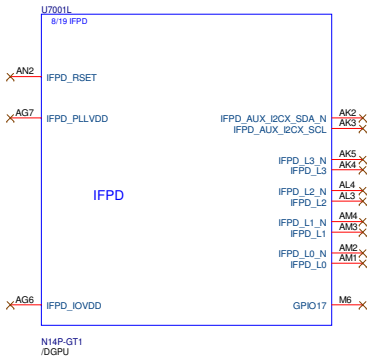


20121214(Eli)
Remove R7303, R7304, R7305, R7306, R7308, R7309, R7310, R7312, RN7301, RN7302 follow NV FAE recommend

HDMI

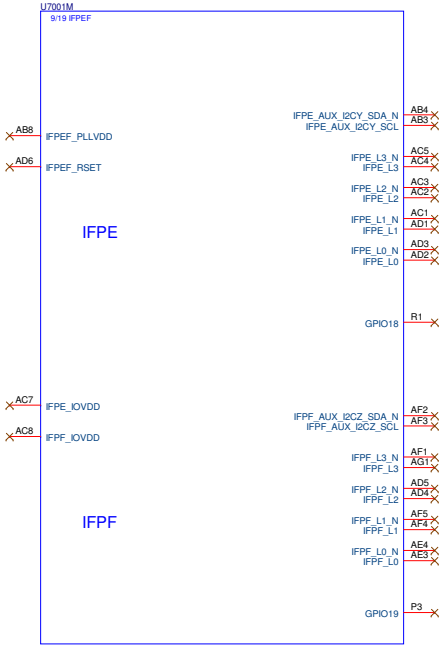


eDP



DVI

+3VS_VGA +3VS_VGA 63,70,71,72,74,75,87,91



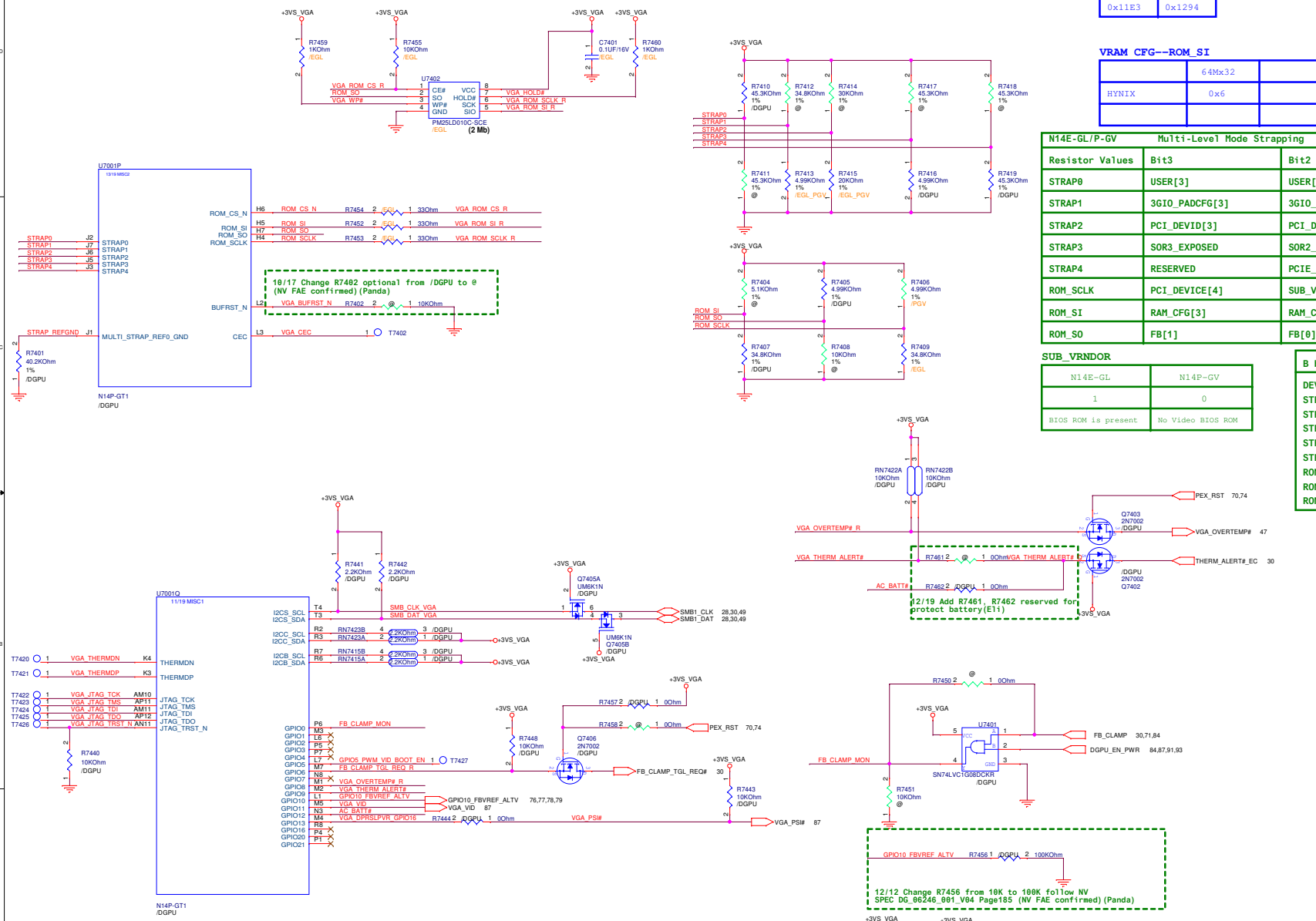
20121221(Eli)
Remove T7301, T7302, T7303, T7304 follow NV FAE recommend

IFPX channel

	N14E-GL Standard Mode	N14P-GV Combined Mode
IFPA	LVDS	LVDS(DP/DVI)
IFPB	LVDS	LVDS(DP/DVI)
IFPC	DP/HDMI	DP/HDMI
IFPD	DP/eDP	DP/eDP
IFPE	DP/DVI	X
IFPF	DP/DVI	X

GPIO Definition

	NV SPEC Standard mode DG_06246_001_V03	VA70_HW
GPIO14	IFPAB_HPD(LVDS)	NC
GPIO15	IFPC_HPD(HDMI)	NC
GPIO17	IFPD_HPD(eDP)	NC
GPIO18	IFPE_HPD(DVI)	NC
GPIO19	IFPF_HPD(DVI)	NC



+3VS_VGA +3VS_VGA 63,70,71,72,75,87,91

GPU DEVICE ID

N14E-GL	N14P-GV
0x11E3	0x1294

VRAM CFG--ROM_SI

	64Mx32	
HYNIX	0x6	

SUB_VRNDOR

N14E-GL	N14P-GV
1	0
BIOS ROM is present	No Video BIOS ROM

N14E-GL/P-GV Strap Resistance Mapping to Hex Values

Resistor Values	Pull-up to VDD33	Pull-down to GND
4.99K	1000	0000
10.0K	1001	0001
15.0K	1010	0010
20.0K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

N14E-GL/P-GV Multi-Level Mode Strapping

Resistor Values	Bit3	Bit2	Bit1	Bit0
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V
ROM_SCLK	PCI_DEVICE[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE

B build	N14E-GL	N14P-GV
DEVICE ID	0x11E3	0x1294
STRAP0	45K PU	45K PU
STRAP1	5K PD	45K PD
STRAP2	20K PD	25K PD
STRAP3	5K PD	5K PD
STRAP4	45K PD	45K PD
ROM_SCLK	35K PD	5K PU
ROM_SI	35K PD	35K PD
ROM_SO	5K PU	5K PU

GPIO Definition

	NV SPEC Standard mode DG_06246_001_V03	VA70_HW
GPIO0	FB_CLAMP_MON	FB_CLAMP_MON
GPIO1	MEM_VDD_CTL	NC
GPIO2	LCD_BL_PWM	NC
GPIO3	LCD_VCC	NC
GPIO4	LCD_BLEN	NC
GPIO5	Reserved	Reserved
GPIO6	FB_CLAMP_TGL_REQ	FB_CLAMP_TGL_REQ#
GPIO7	3DVision	NC
GPIO8	OVERT	VGA_OVERTEMP#
GPIO9	ALERT	VGA_THERM_ALERT#
GPIO10	MEM_VREF_CTL	MEM_VREF_CTL
GPIO11	PWM_VID	VGA_VID
GPIO12	PWR_LEVEL	AC_BATT#
GPIO13	PSI	VGA_PSI#
GPIO16	FRM_LCK	NC
GPIO20	Reserved	NC
GPIO21	Reserved	NC

PEGATRON

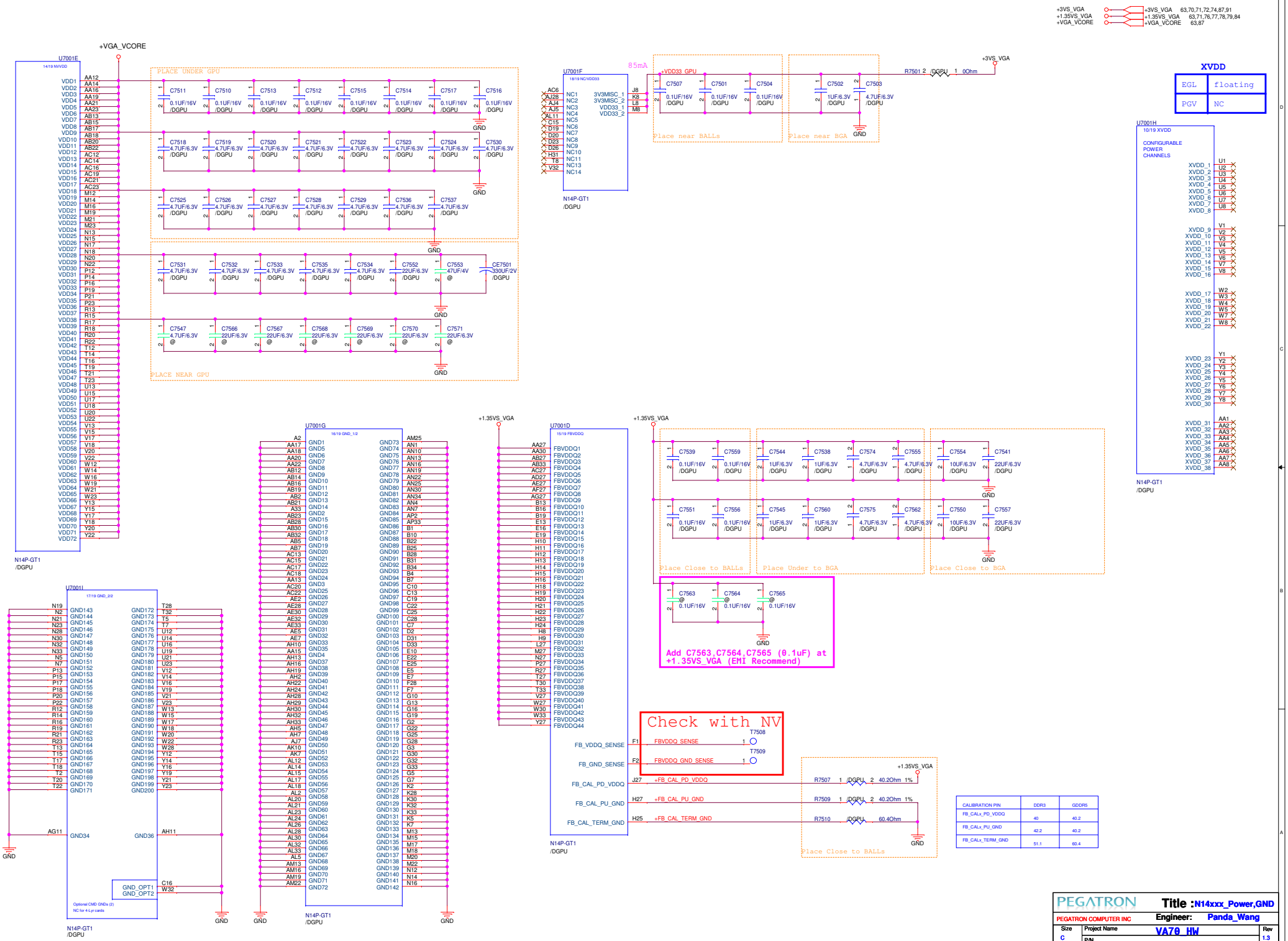
Title : N14xxx_GPIO,STRAP

PEGATRON COMPUTER INC Engineer: Panda_Wang

Size	Project Name	Rev
A2	VA70_HW	1.3

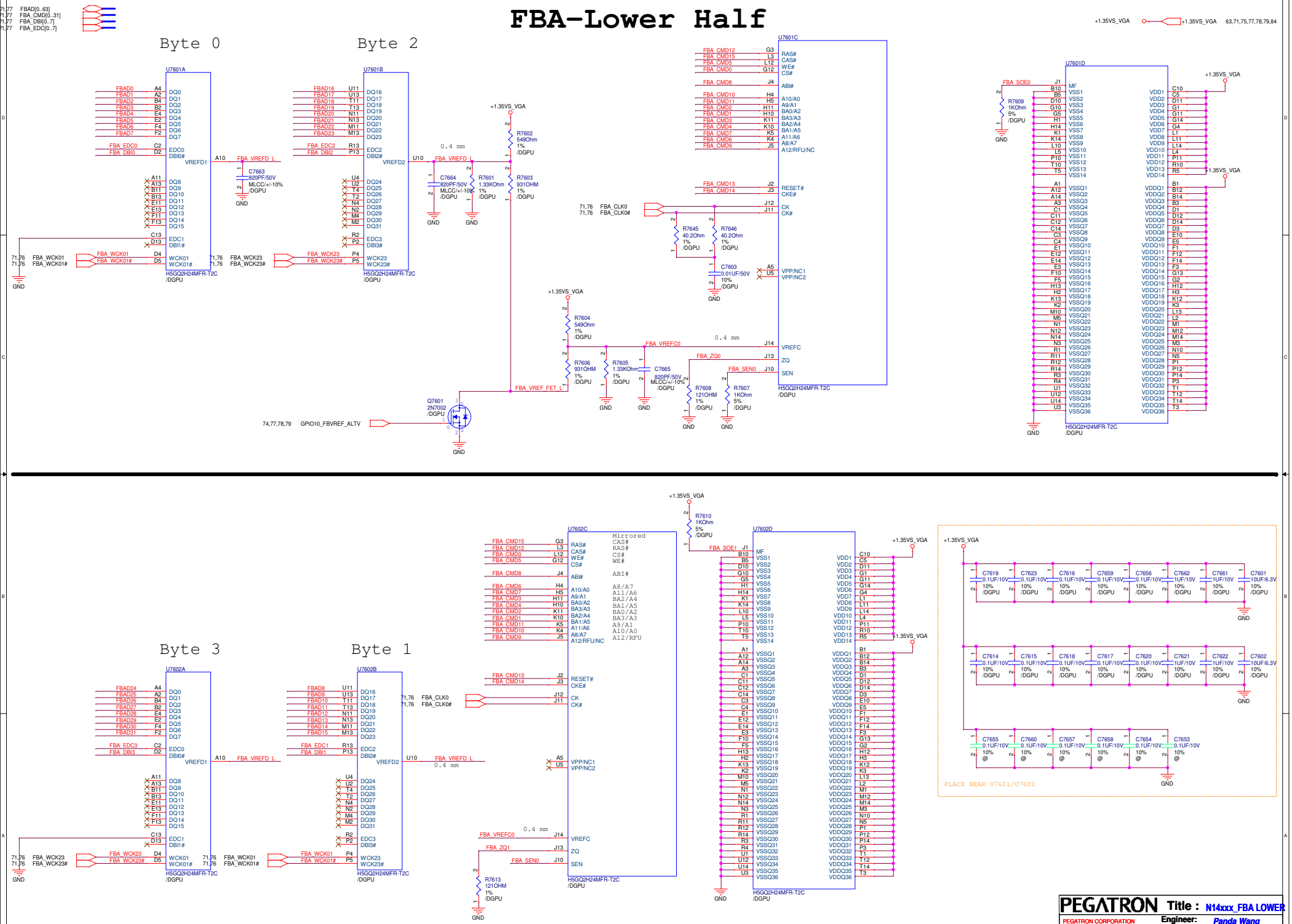
P/N

Date: Friday, January 18, 2013 Sheet 74 of 89



CALIBRATION PIN	DDR3	GDDR5
FB_CALx_PD_VDDQ	40	40.2
FB_CALx_PU_GND	42.2	40.2
FB_CALx_TERM_GND	51.1	60.4

FBA-Lower Half



PEGATRON CORPORATION

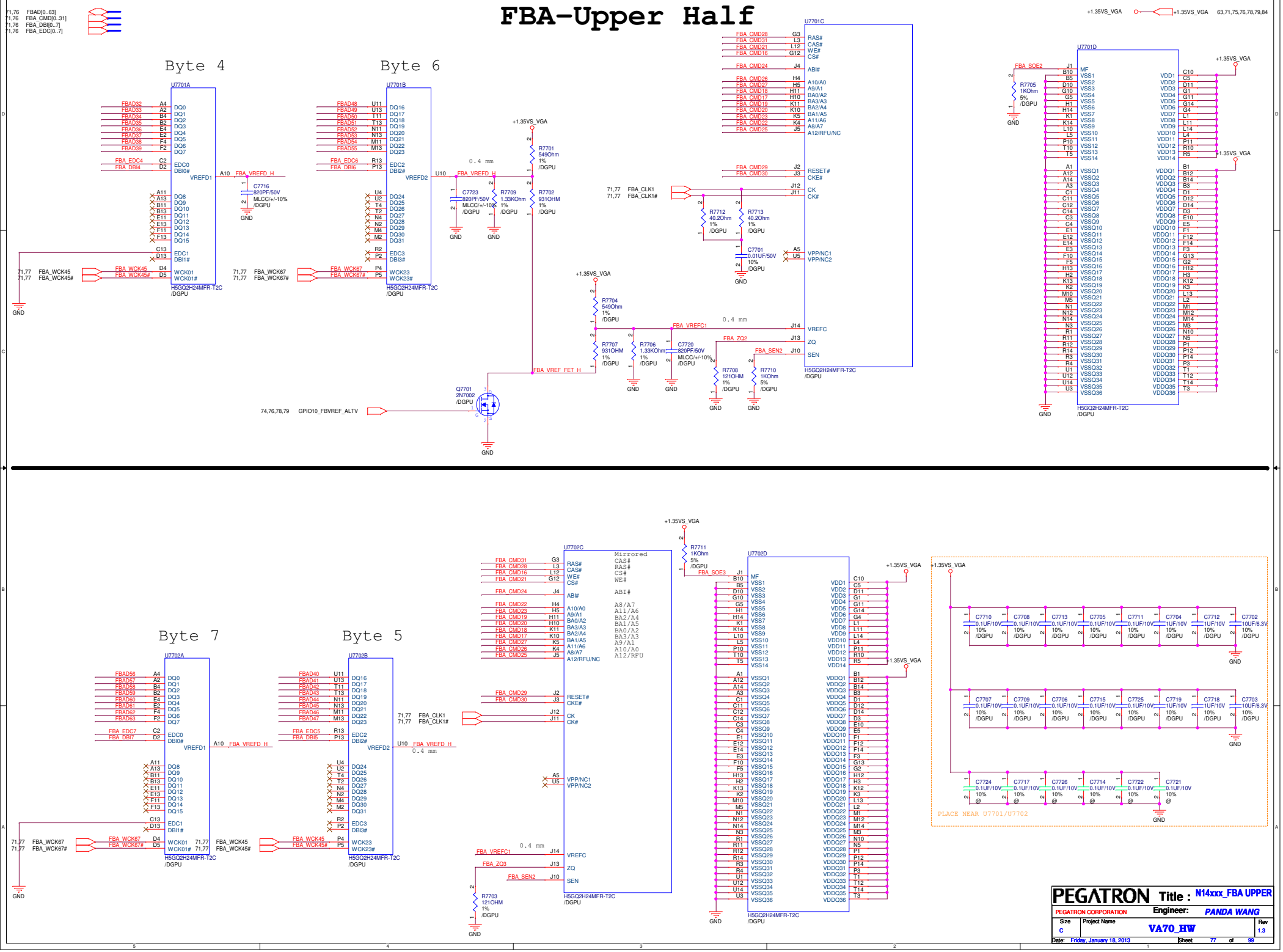
Title : N14xxx_FBA LOWER

Engineer: Panda Wang

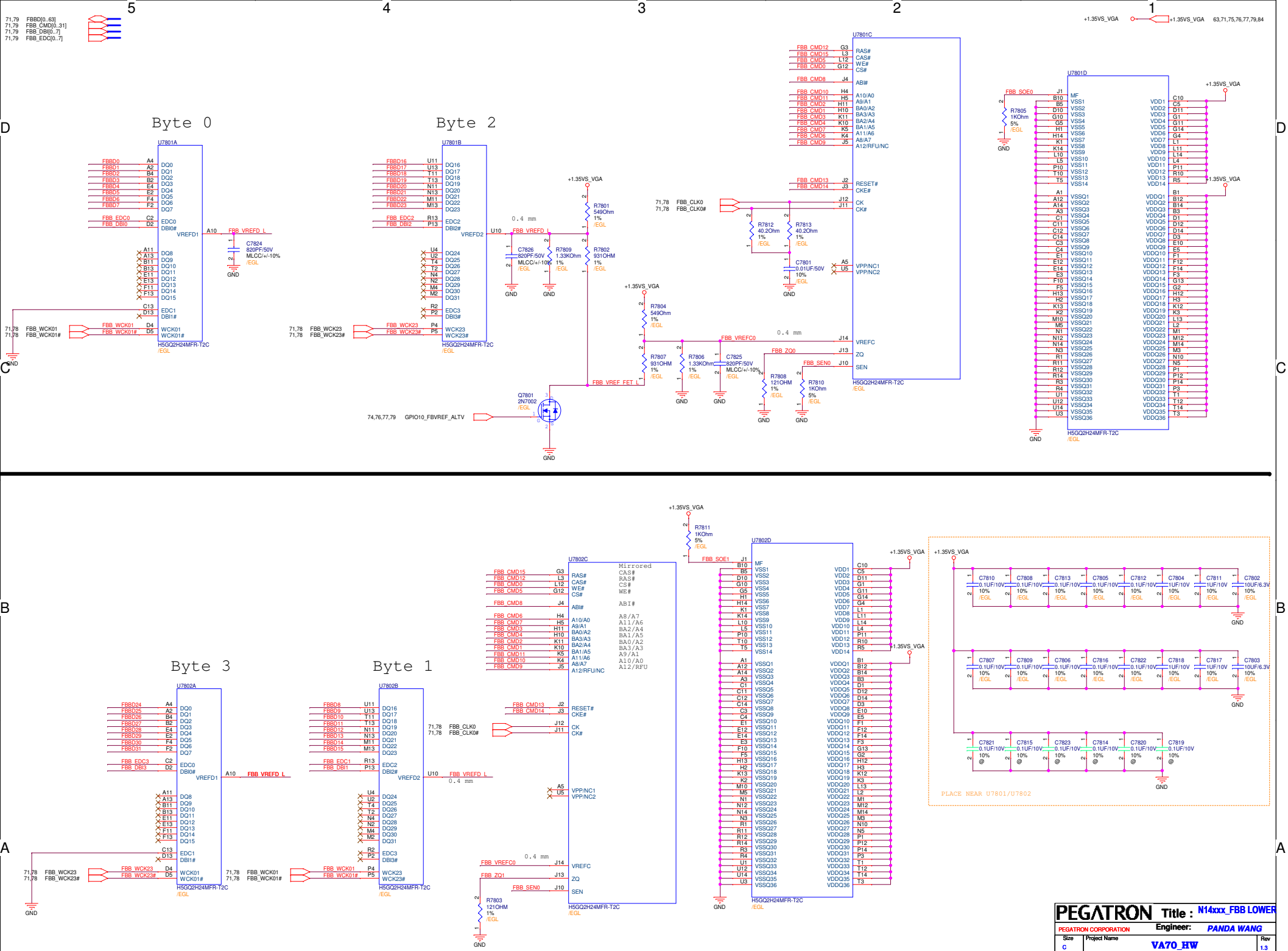
Size	Project Name	Rev
C	VA70_HW	1.3

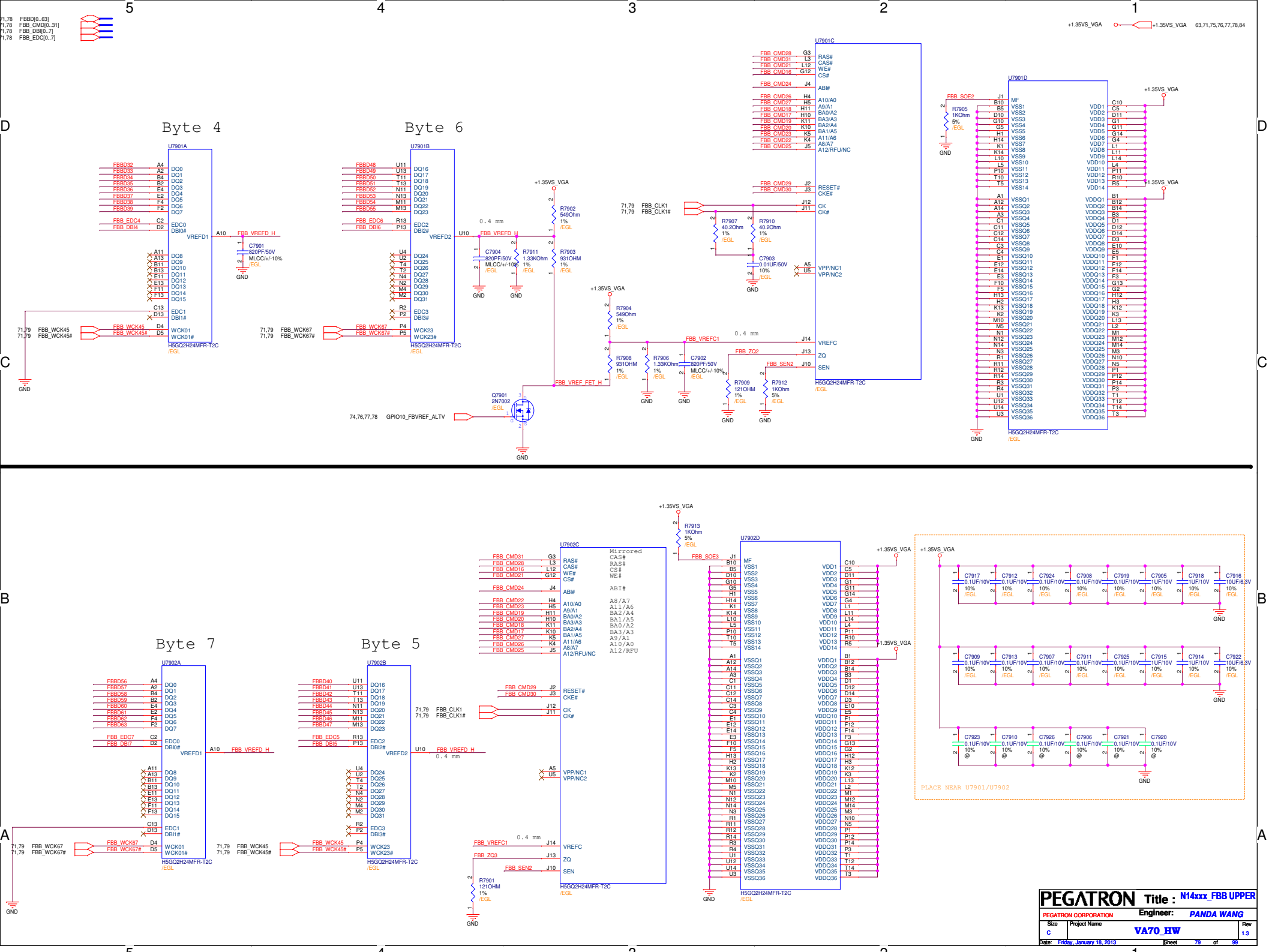
Date: Friday, January 18, 2013 Sheet 76 of 99

FBA-Upper Half



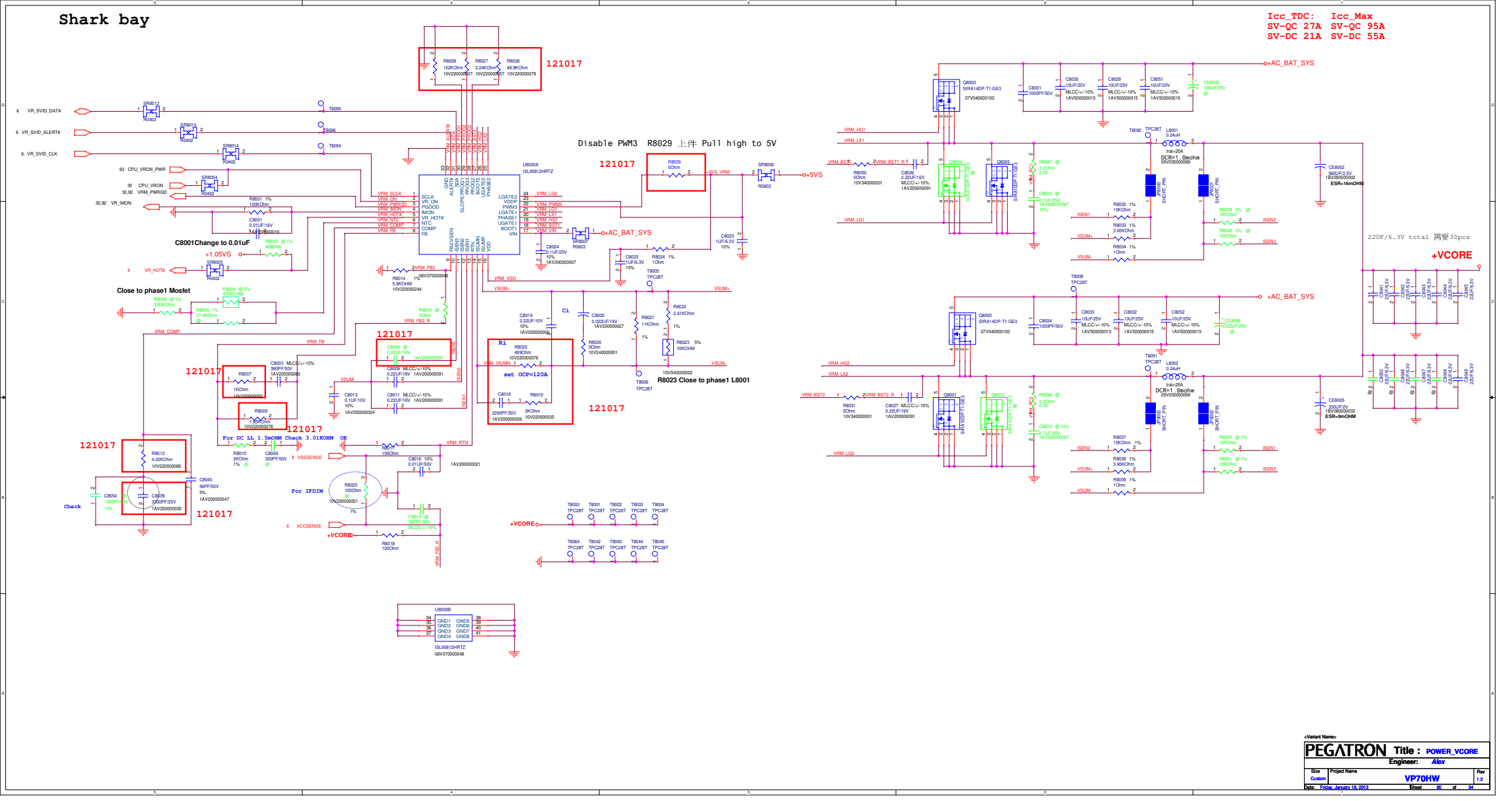
PEGATRON	Title :	N14xxx_FBA UPPER
PEGATRON CORPORATION	Engineer:	PANDA WANG
Size: C	Project Name: VA70_HW	Rev: 1.3
Date: Friday, January 18, 2013	Sheet 77 of 99	


Byte 0
Byte 2
Byte 3
Byte 1
U7801A
U7801B
U7801C
U7801D
U7802A
U7802B
U7802C
U7802D
H5GQ2H24MFR-T2C
PLACE NEAR U7801/U7802
PEGATRON
Title : N14xxx_FBB LOWER
PEGATRON CORPORATION
Engineer: PANDA WANG
Size C
Project Name VA70_HW
Rev 1.3
Date: Friday, January 18, 2013
Sheet 78 of 99

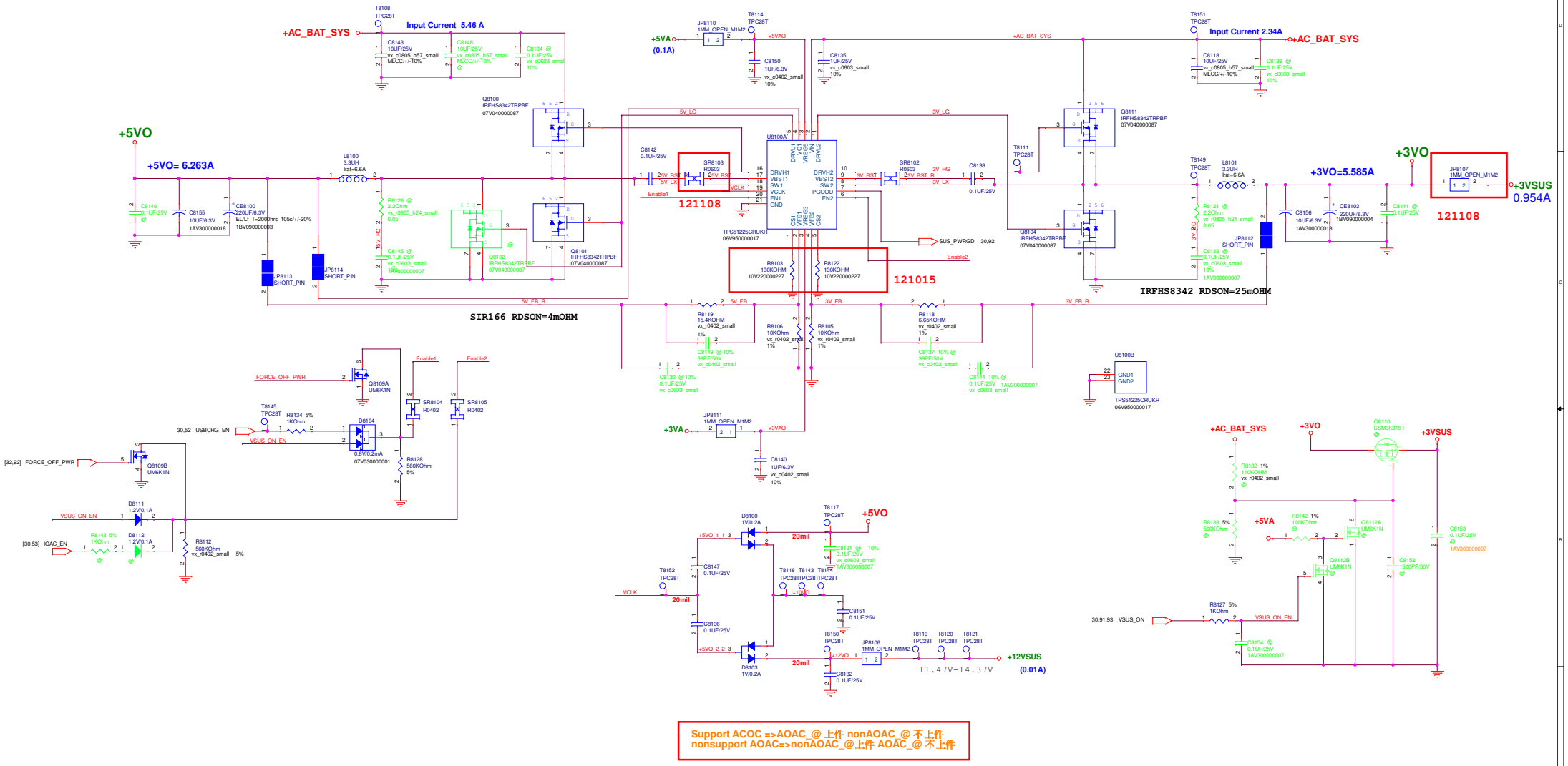

Byte 4
Byte 6
Byte 7
Byte 5
U7901A
U7901B
U7901C
U7901D
U7902A
U7902B
U7902C
U7902D
H5GQ2H24MFR-T2C
Q7901
2N7002
PLACE NEAR U7901/U7902
PEGATRON
Title : N14xxx_FBB UPPER
PEGATRON CORPORATION
Engineer: PANDA WANG
Size C
Project Name VA70_HW
Rev 1.3
Date: Friday, January 18, 2013
Sheet 79 of 99

Shark bay

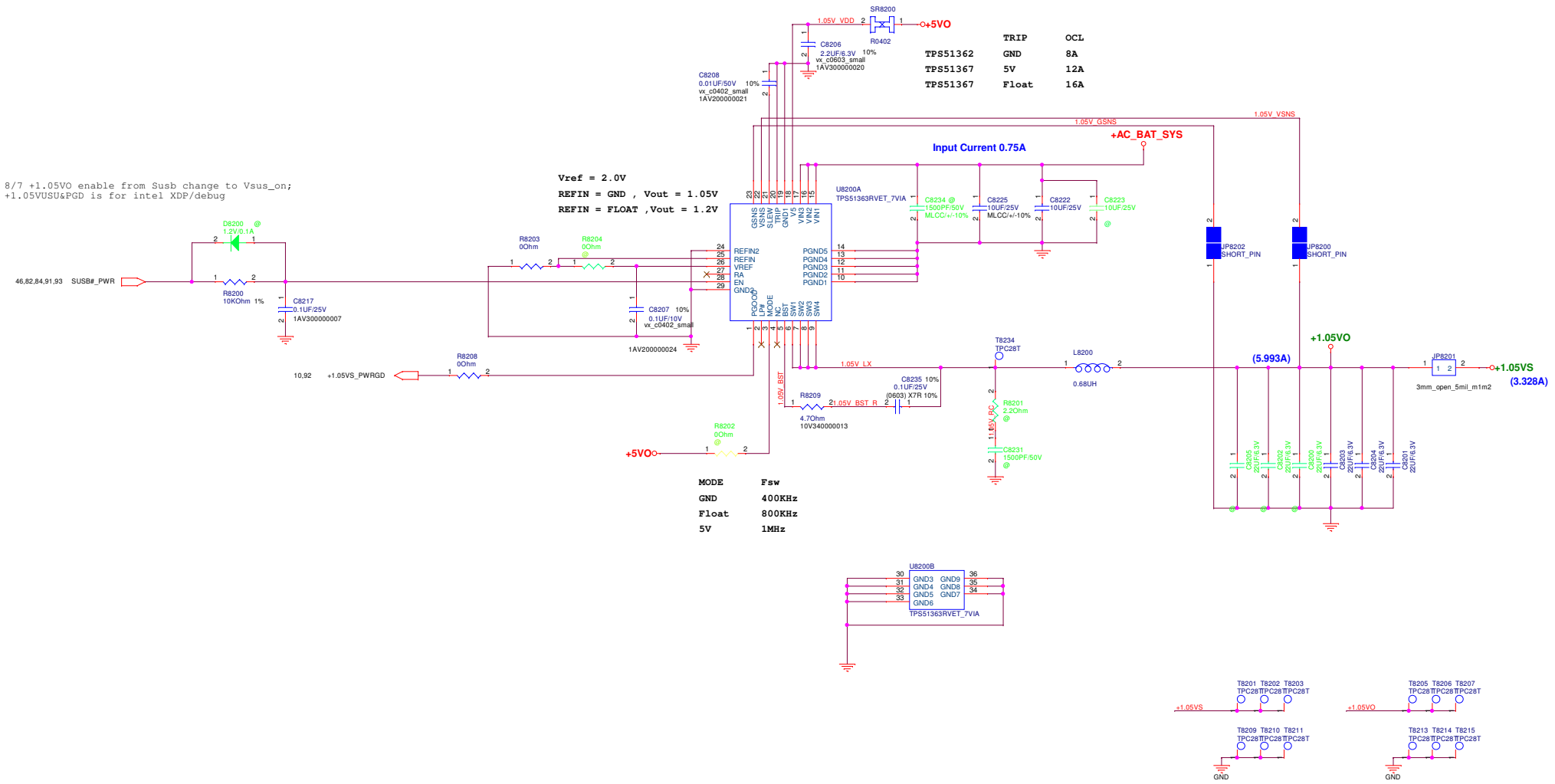
Icc_TDC: Icc_Max
SV-QC 27A SV-QC 95A
SV-DC 21A SV-DC 55A



+5VO & +3VO POWER SUPPLY



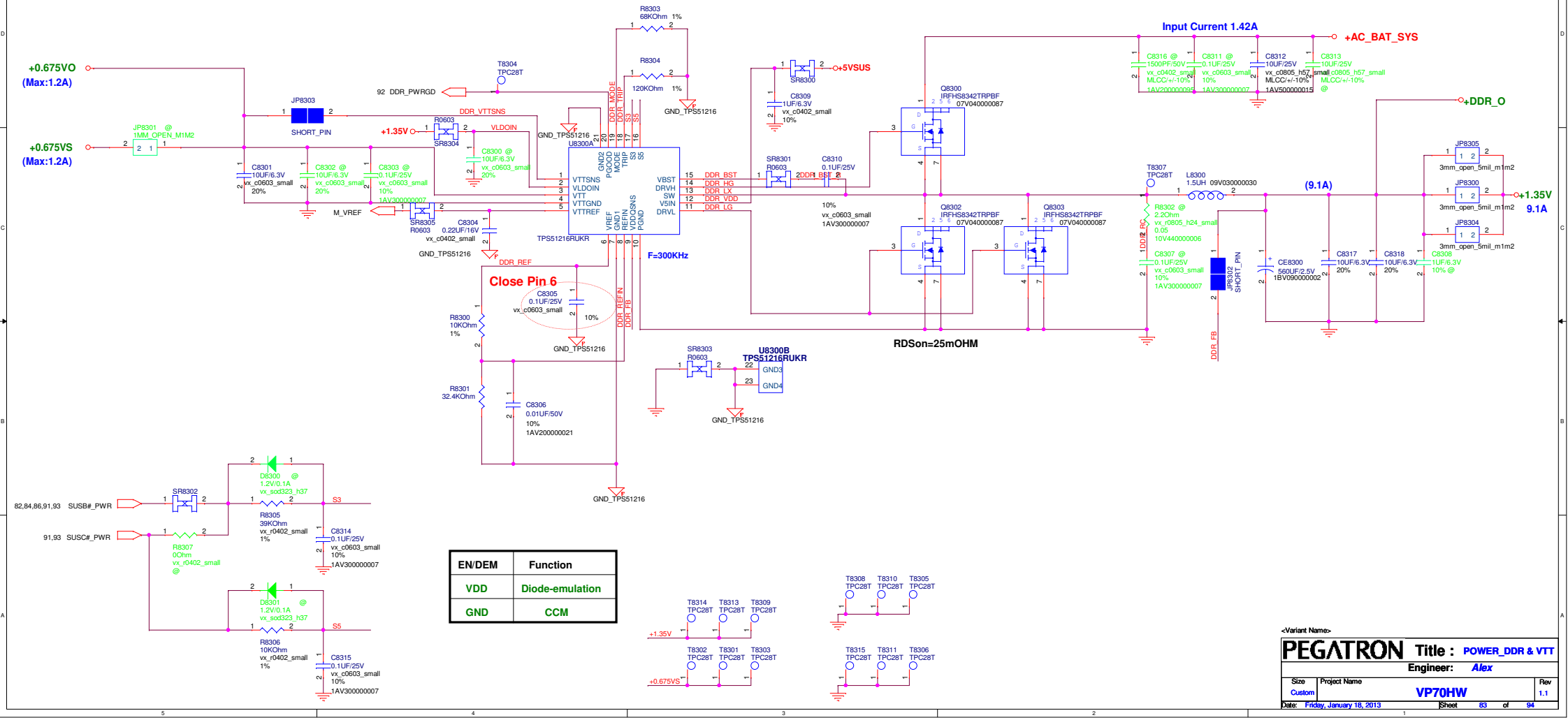
+1.05VS POWER SUPPLY



<Variant Name>

PEGATRON	Title : POWER_+1.05VS	
	Engineer: Alex	
Size: Custom	Project Name: VP70HW	Rev: 1.1
Date: Friday, January 18, 2013	Sheet 82 of 94	

DDR & VTT POWER SUPPLY



EN/DEM	Function
VDD	Diode-emulation
GND	CCM

<Variant Name>

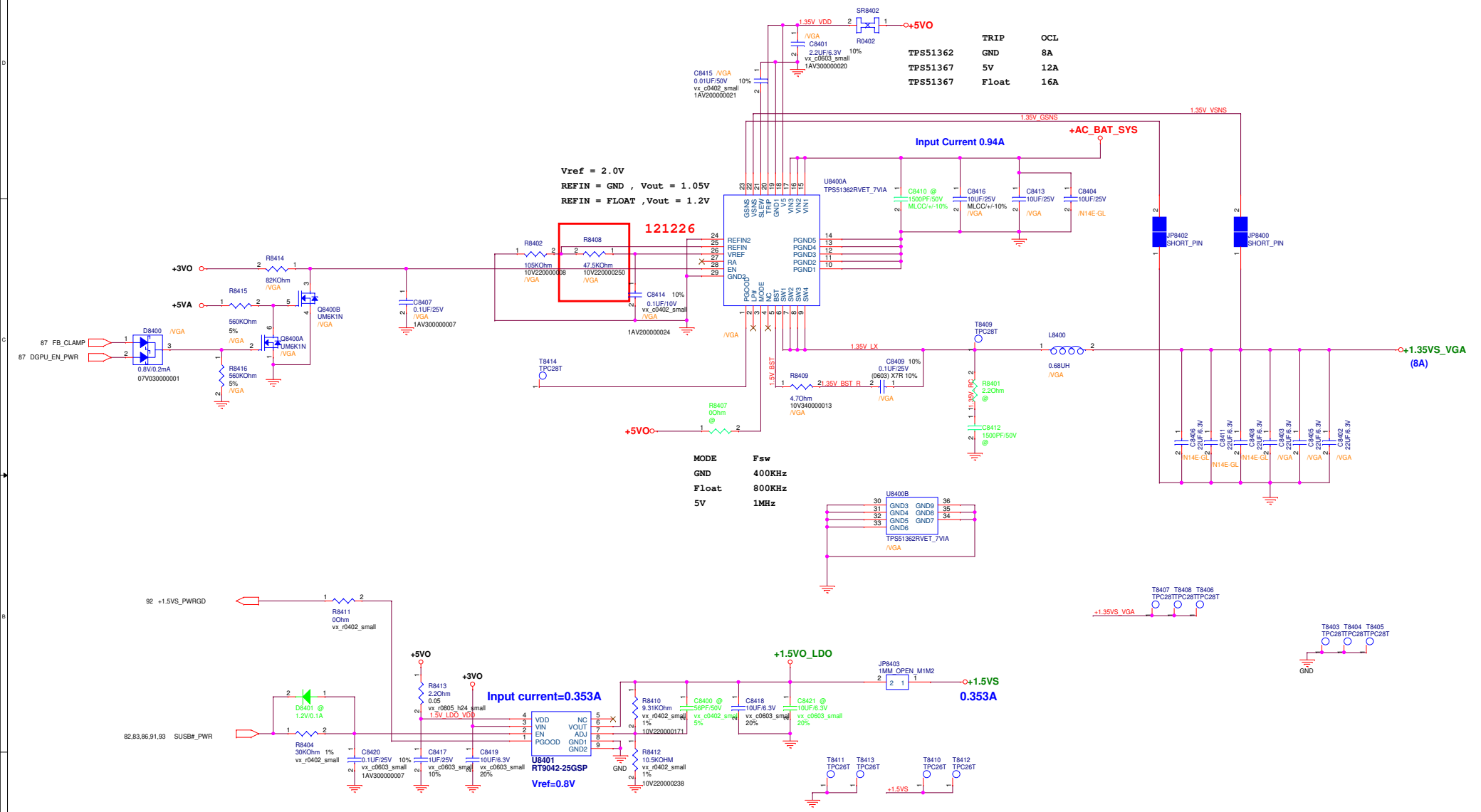
PEGATRON Title : POWER_DDR & VTT

Engineer: Alex

Size	Project Name	Rev
Custom	VP70HW	1.1

Date: Friday, January 18, 2013 Sheet 83 of 94

+1.35VS POWER SUPPLY



<Variant Name>

PEGATRON Title : POWER_1.5VS

Engineer: Alex

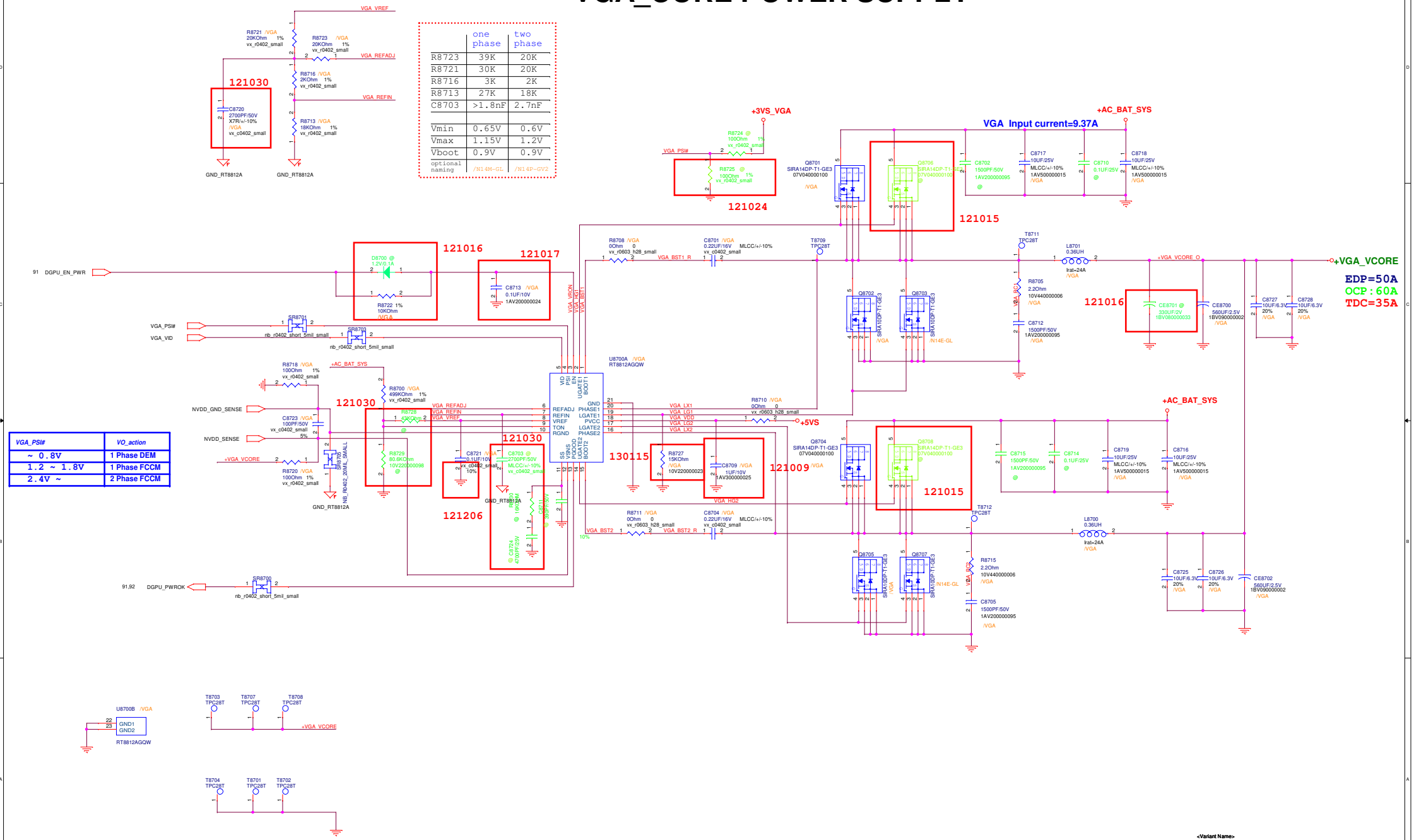
Size	Project Name	Rev
C	VP70HW	1.1

Date: Friday, January 18, 2013 Sheet 84 of 94

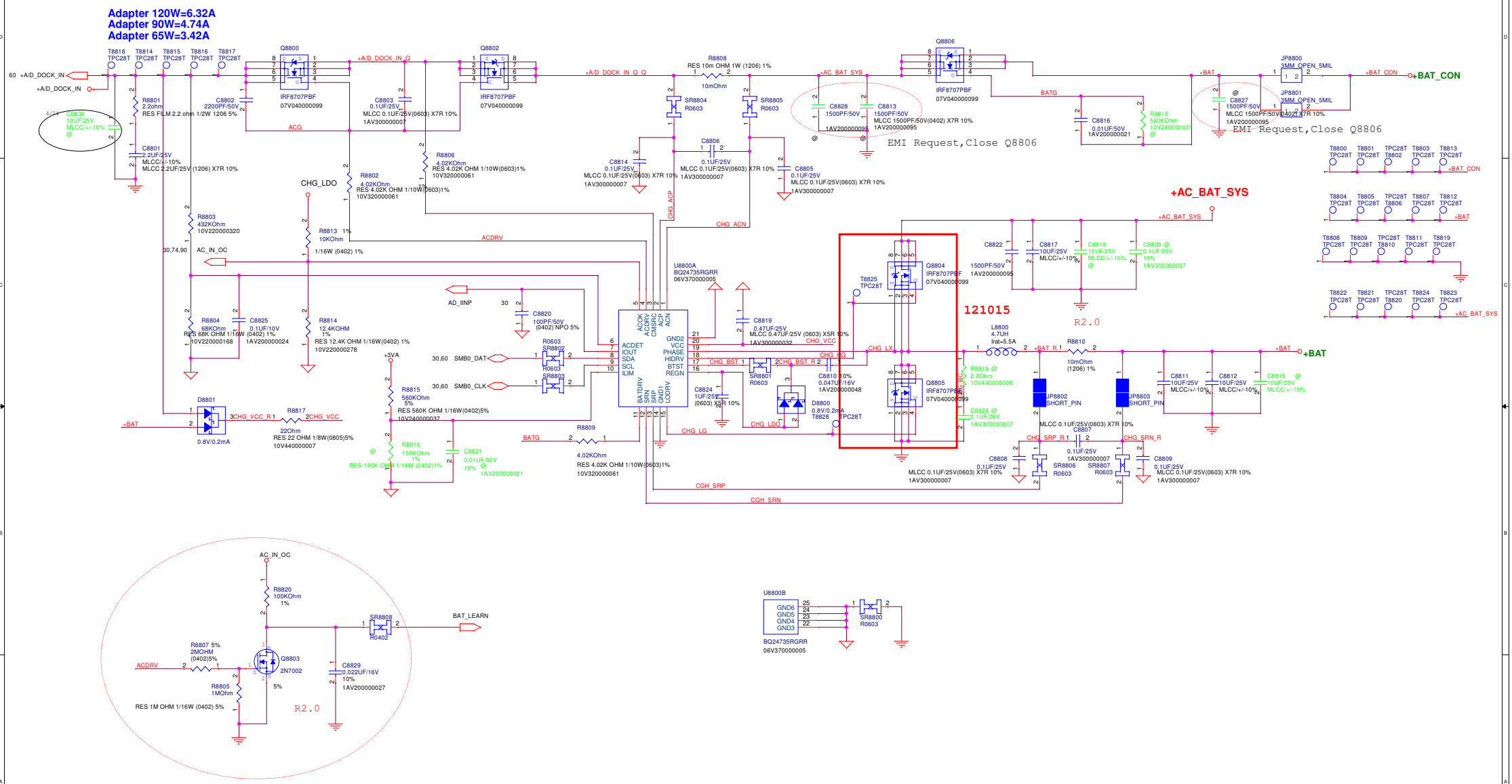
VGA_CORE POWER SUPPLY

	one phase	two phase
R8723	39K	20K
R8721	30K	20K
R8716	3K	2K
R8713	27K	18K
C8703	>1.8nF	2.7nF
Vmin	0.65V	0.6V
Vmax	1.15V	1.2V
Vboot	0.9V	0.9V
optional naming	/N14M-GL	/N14P-GV2

VGA_PSI#	VO_action
~ 0.8V	1 Phase DEM
1.2 ~ 1.8V	1 Phase FCCM
2.4V ~	2 Phase FCCM

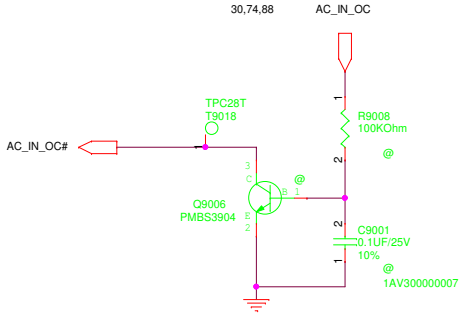


BATTERY CHARGER



BATTERY IN DETECT

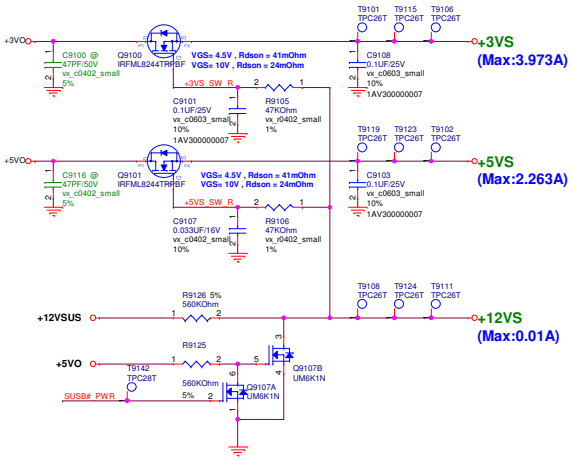
ADAPTER IN DETECT



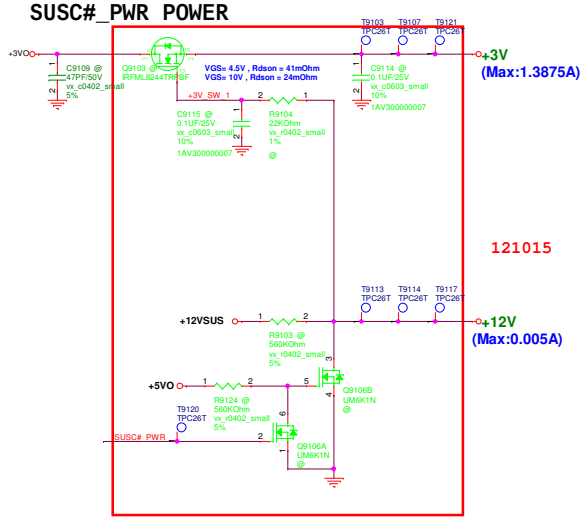
<Variant Name>

PEGATRON	Title : POWER_DETECT	
	Engineer: *Alex*	
Size: Custom	Project Name: VP70HW	Rev: 1.1
Date: Friday, January 18, 2013	Sheet 90 of 99	

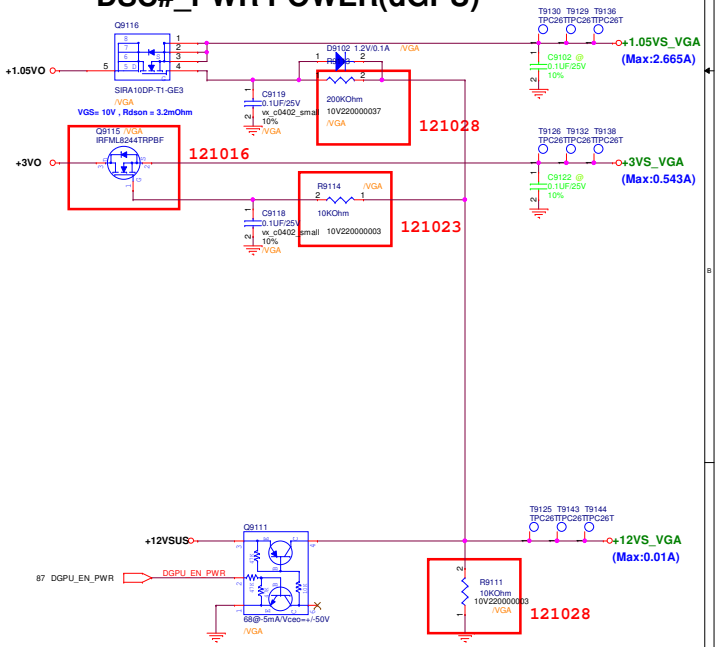
SUSB#_PWR POWER



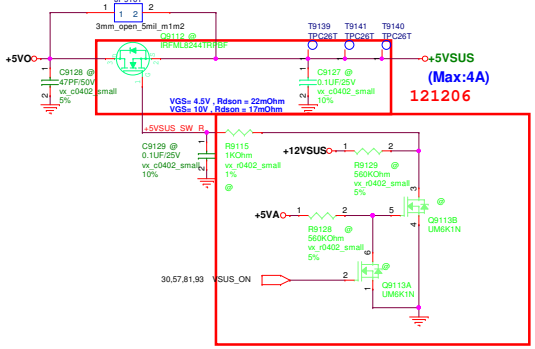
SUSC#_PWR POWER

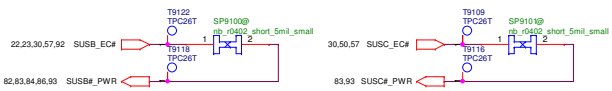


DSC#_PWR POWER(dGPU)

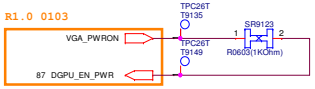


VSUS_ON POWER

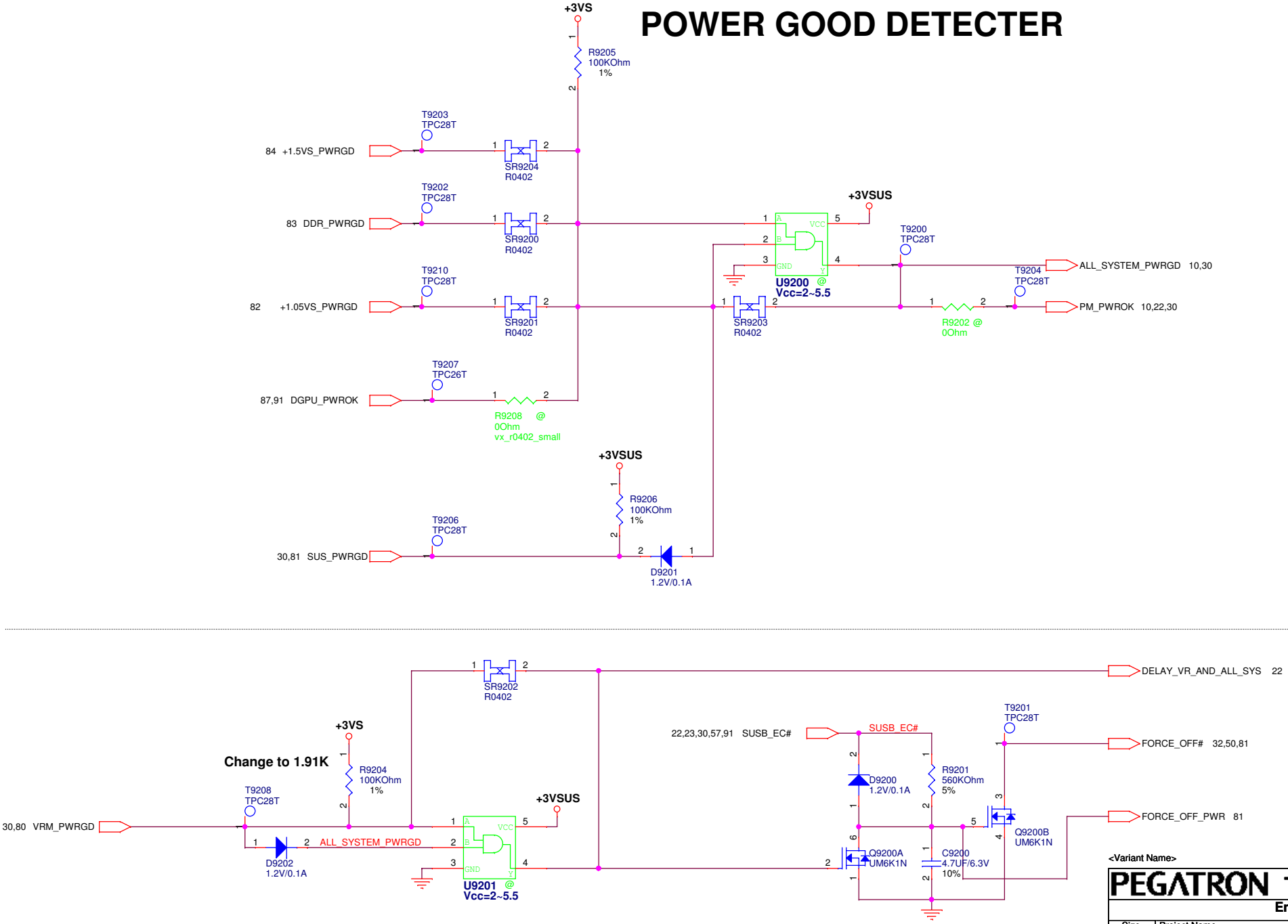




DSC_VGA_PWR POWER Control



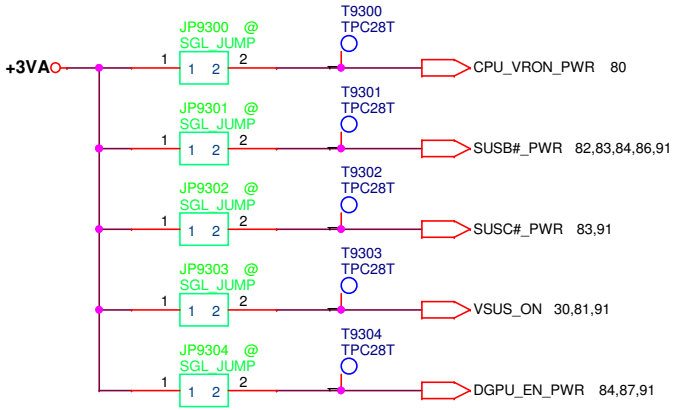
POWER GOOD DETECTER



<Variant Name>

PEGATRON	Title : POWER_PROTECT	
	Engineer: Alex	
Size: Custom	Project Name: VP70HW	Rev: 1.1
Date: Friday, January 18, 2013	Sheet 92 of 94	

FOR POWER TEST



<Variant Name>

PEGATRON	Title : POWER_SIGNAL	
	Engineer: Alex	
Size: Custom	Project Name: VP70HW	Rev: 1.1
Date: Friday, January 18, 2013	Sheet 93 of 94	