

Aegis M/B

MS14-Additional
2010.12.10

A01 Build

INVENTEC

TITLE
Aegis

SIZE Custom	CODE ES	DOC.NUMBER CS-131	REV A01
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CHANGE by IEC	DATE Friday, December 10, 2010
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SHEET 1	of 61
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Friday, December 10, 2010		
DATE	CHANGE NO.	REV

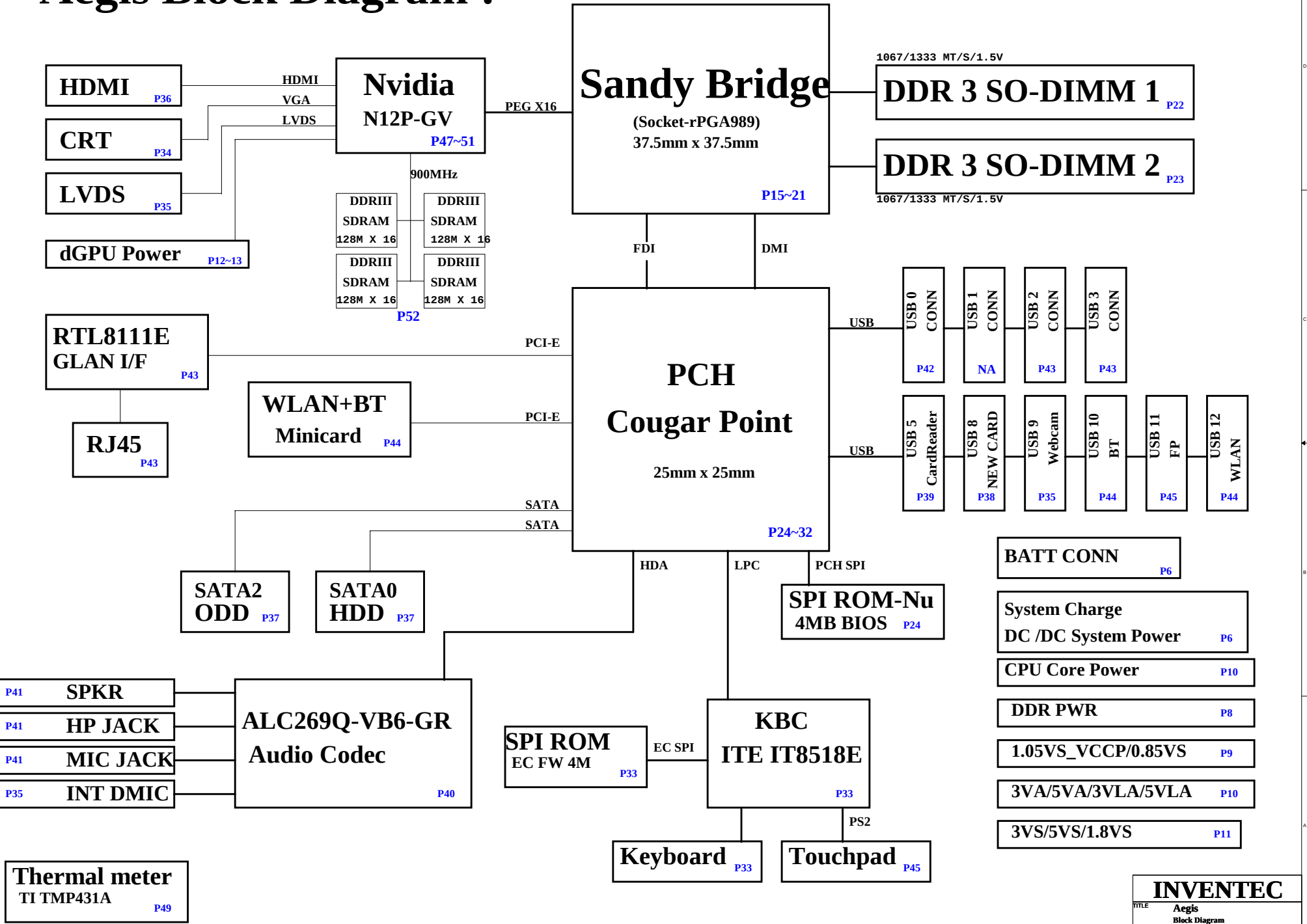
Schematic Page Description :

- | | |
|----------------------------|----------------------|
| 01. Title | 32. PCH (9/9) |
| 02. Schematic Page DESCR | 33. KBC |
| 03. Block Diagram | 34. CRT CONN |
| 04. Power Block Diagram | 35. LCD CONN |
| 05. Annotations | 36. HDMI CONN |
| 06. PWR_Adaptor in/Charge | 37. SATA HDD /ODD |
| 07. PWR_3VA/5VA/3VLA/5VLA | 38. New Card |
| 08. PWR_1.5V/0.75V | 39. Card Reader |
| 09. PWR_0.85VS/1.05VS_VCCP | 40. Audio Codec |
| 10. PWR_CPU Core Power | 41. Audio Jack |
| 11. PWR_3VS/5VS/1.8VS | 42. PWR OFF Charge |
| 12. GPU Power-1 | 43. RJ45 I/F USB I/F |
| 13. GPU Power-2 | 44. WLAN / BT |
| 14. POWER SEQUENCE | 45. PSW/LID/ TP |
| 15. Processor(1/6) | 46. LED / SCREW |
| 16. Processor(2/6) | 47. N12P-GV (1/5) |
| 17. Processor(3/6) | 48. N12P-GV (2/5) |
| 18. Processor(4/6) | 49. N12P-GV (3/5) |
| 19. Processor(5/6) | 50. N12P-GV (4/5) |
| 20. Processor(6/6) | 51. N12P-GV (5/5) |
| 21. Fan/Thermal | 52. DDR3 VRAM |
| 22. DDR3 DIMM0 | 53. USB Board Title |
| 23. DDR3 DIMM1 | 54. RTL8111E-VL-CG |
| 24. PCH (1/9) | 55. USB Port |
| 25. PCH (2/9) | 56. SW Board Title |
| 26. PCH (3/9) | 57. SW_Board |
| 27. PCH (4/9) | 58. FP Board Title |
| 28. PCH (5/9) | 59. FP Board |
| 29. PCH (6/9) | 60. GP Board Title |
| 30. PCH (7/9) | 61. GP Board |
| 31. PCH (8/9) | |

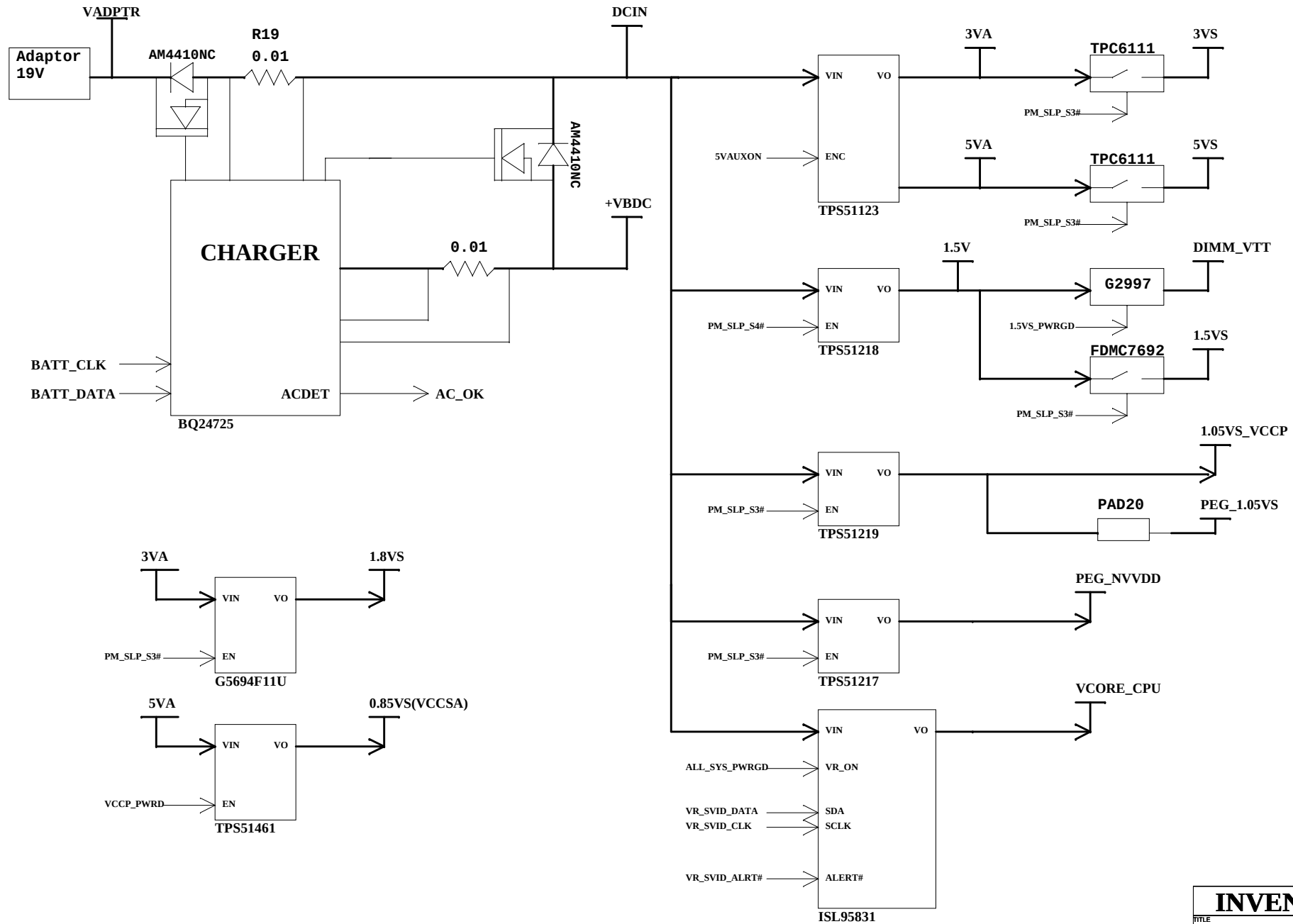
INVENTEC

TITLE Aegis schematics page DESCR			
SIZE C	CODE ES	DOC NUMBER CS-131	REV A01
SHEET 2 of 61			

Aegis Block Diagram :



Power Block Diagram :



Net name Description :

Board Stack up Description

Voltage Rails

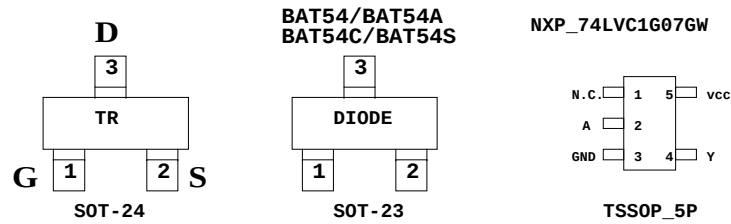
DCIN	Primary DC system power supply
3VLA	3.3V always on power rail by DCIN
5VLA	5.0V always on power rail by DCIN
3VLA_EC	3.3V always on power rail by 5VAUXON
3VA	3.3V always on power rail by LATCH_ON
5VA	5.0V always on power rail by LATCH_ON
5VACP	5.0V always on power rail by 5VAUXON
1.5V	1.5V switched power rail by PM_SLP_S4#
1.8V	1.8V power rail by PM_SLP_S4#
3VS	3.3V power rail by PM_SLP_S3#
5VS	5.0V power rail by PM_SLP_S3#
1.5VS	1.5V power rail by PM_SLP_S3#
1.05VS_VCCP	1.05V power rail by PM_SLP_S3#
DIMM_VTT	0.75V DDR Termination Voltage by 1.5VS_PWRGD
PEG_1.5VS	1.5V switched power rail for N12P-GV by PM_SLP_S3#
PEG_1.05VS	1.05V switched power rail for N12P-GV by PM_SLP_S3#
PEG_NVVDD	Variable switched power rail for N12P-GV by PM_SLP_S3#
VCORE_CPU	Core switched power rail for CPU by ALL_SYS_PWRGD
1.8VS	1.8V power rail by PM_SLP_S3#

Part Naming Conventions

C	= Capacitor	Q	= Transistor
CN	= Connector	R	= Resistor
D	= Diode	RP	= Resistor Pack
F	= Fuse	U	= Arbitrary Logic Device
L	= Inductor	Y	= Crystal and Osc

Name Suffix

#	= Active Low signal
NU	= No Stuff



PCB Layers

Layer 1		Component Side, Microstrip signal Layer
Layer 2		Ground Plane
Layer 3		Stripline Layer
Layer 4		Power Plane
Layer 5		Stripline Layer
Layer 6		Stripline Layer
Layer 7		Ground Plane
Layer 8		Solder Side, Microstrip signal Layer

	Differential Impedance for Microstrip(5-mils)	Differential Impedance for Stripline(4-mils)
Host Clock	95 ohm +/- 20%	100 ohm +/- 20%
PCI-E Clock	95 ohm +/- 20%	100 ohm +/- 20%
DDR2 CLK	70 ohm +/- 20%	70 ohm +/- 20%
DDR2 Strobe	85 ohm +/- 20%	90 ohm +/- 20%
DMI Bus	95 ohm +/- 20%	100 ohm +/- 20%
PCI-E Bus	95 ohm +/- 20%	100 ohm +/- 20%
SDVO	95 ohm +/- 20%	100 ohm +/- 20%
SATA	95 ohm +/- 20%	100 ohm +/- 20%
USB	90 ohm +/- 20%	95 ohm +/- 20%
LVDS		100 ohm +/- 20%
Lan	95 ohm +/- 20%	100 ohm +/- 20%

Mother Board ID setting by PCH

FJ Mother Board ID setting by PCH			
Project	MB_ID2	MB_ID1	MB_ID0
	0	0	0
Aegis (Discrete)	0	0	1
Neuron (UMA)	0	1	0
Neuron-V (Optimus)	0	1	1
Strike (UMA)	1	0	0
Strike-V (Optimus)	1	0	1
Silk (UMA)	1	1	0
Silk-V (Optimus)	1	1	1
PCH ----->	GPIO41	GPIO40	GPIO59

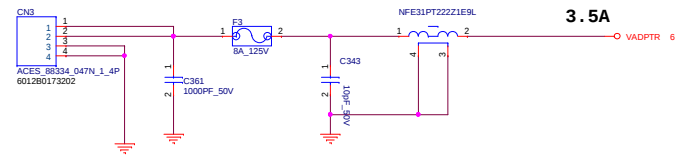
Mother Board ID setting by EC

FJ Mother Board ID setting by EC	
Project	EC_ID0
Aegis (Discrete)	1
Neuron (UMA)	0
Neuron-V (Optimus)	1
Strike (UMA)	0
Strike-V (Optimus)	1
Silk (UMA)	0
Silk-V (Optimus)	1
EC ----->	GPC0 (pin 119)

Please pull up 10k for "1". Pull down 10k for "0"

INVENTEC

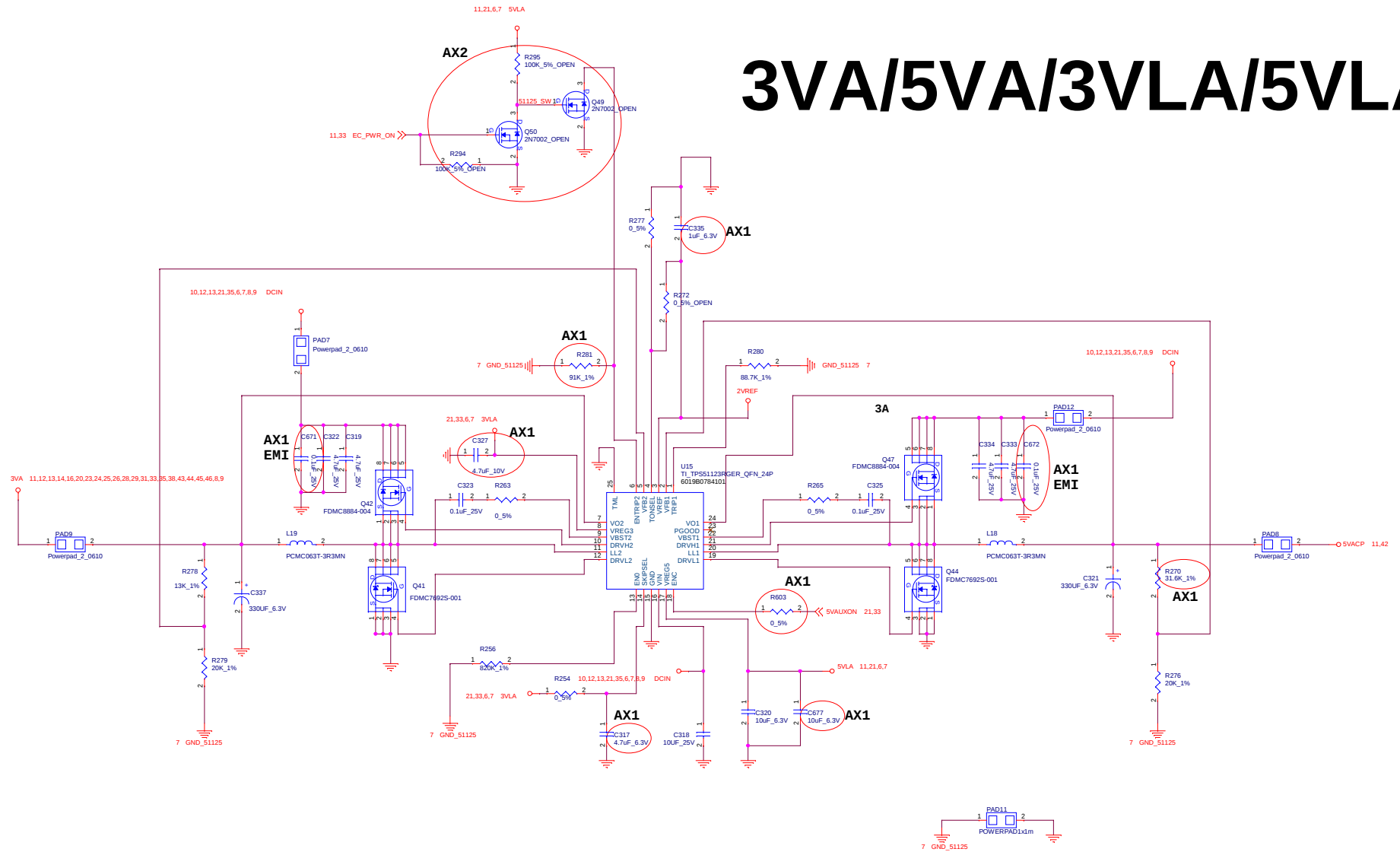
Aegis Annotations			
SIZE	CODE	DOC NUMBER	REV
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3VA/5VA/3VLA/5VLA

3.395V@5A

5.16V@5A

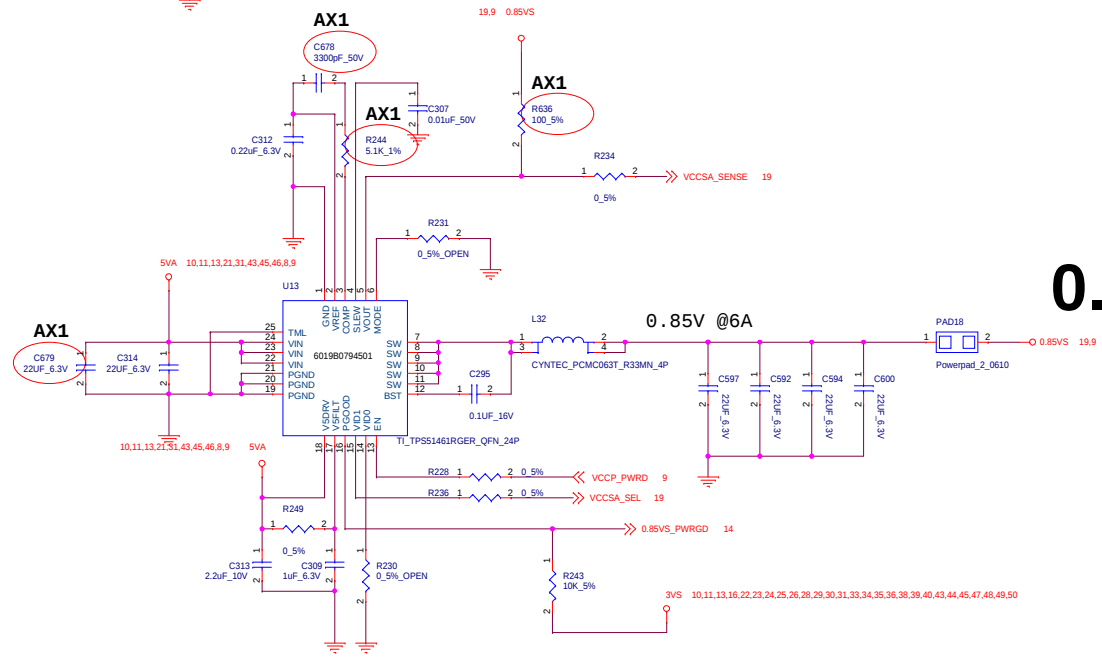
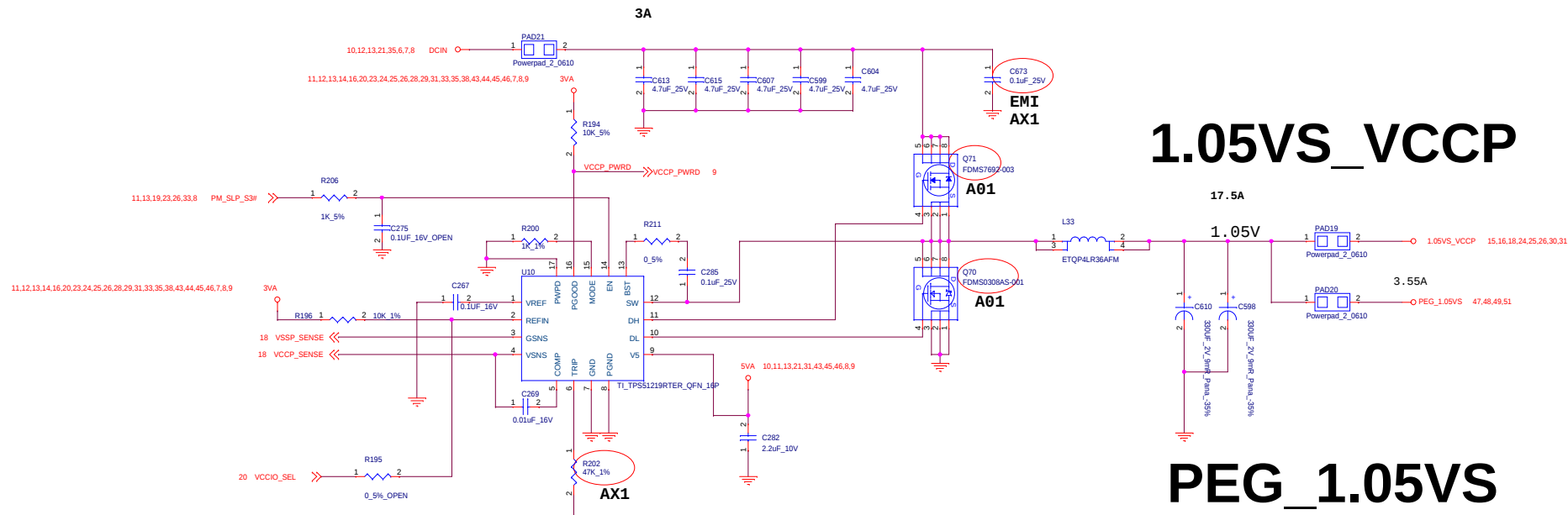


INVENTEC			
TITLE Aegis			
3VA/5VA/3VLA/5VLA			
SIZE	CODE	DOC NUMBER	REV
Custom	CS	CS-131	A01
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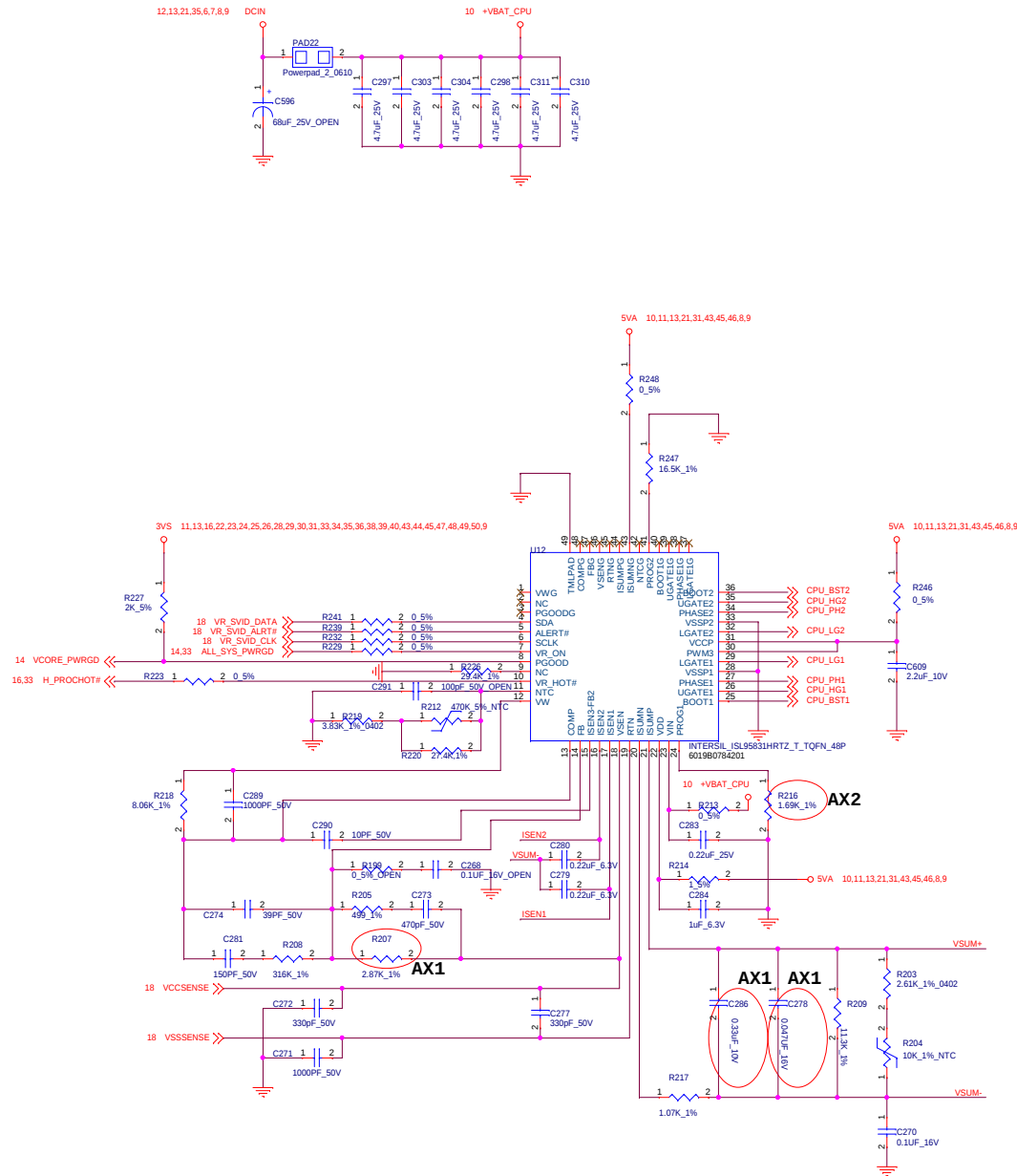


CHANGE by IEC		DATE Friday, December 10, 2010	C	ES	CS-131	A01
			SHEET 8 of 61			



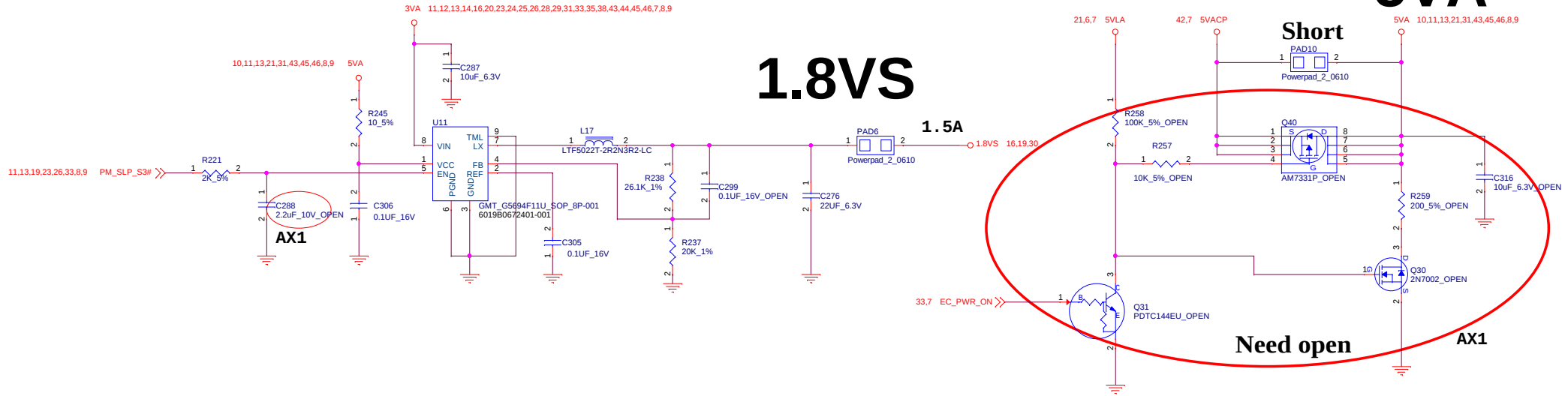
INVENTEC				
Aegis				
0.85VS/1.05VS_VCCP				
SIZE	CODE	DOC NUMBER	REV	
C	ES	CS-131	A01	
SHEET		9	of	61

The schematic diagram illustrates the CPU power supply section of the Razer Blade 15 (2019). It shows three distinct power planes: CPU_BST1, CPU_HG1, and CPU_PH1. Each plane is regulated by an A01 MOSFET (Q27, Q28, Q26) driven by an AX1 gate driver (C669, C670). The diagram includes input capacitors (C601, C614), sense resistors (R568, R570, R569), and output capacitors (C579, C139, C265, C580).

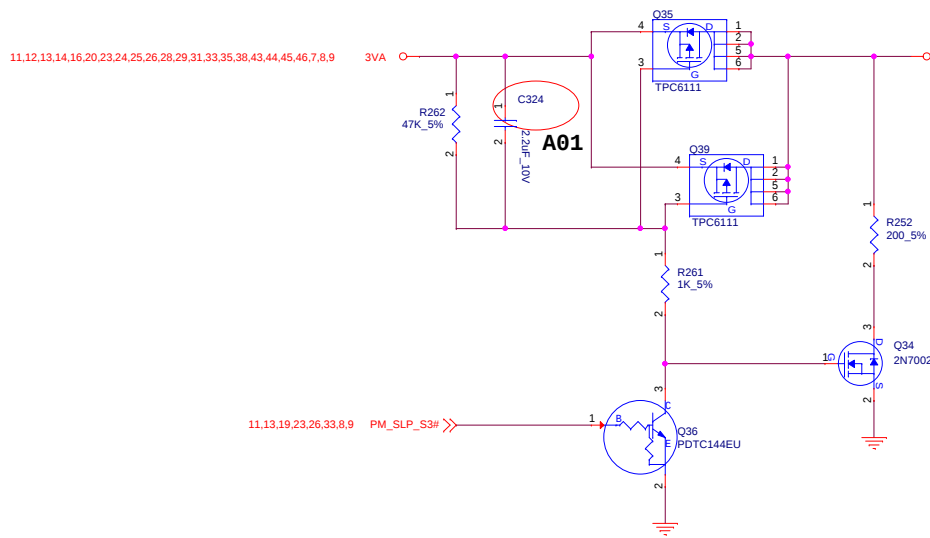


TITLE			
Aegis PWR_CPU Core Power			
SIZE	CODE	DOC.NUMBER	REV
C	ES	CS-131	A01
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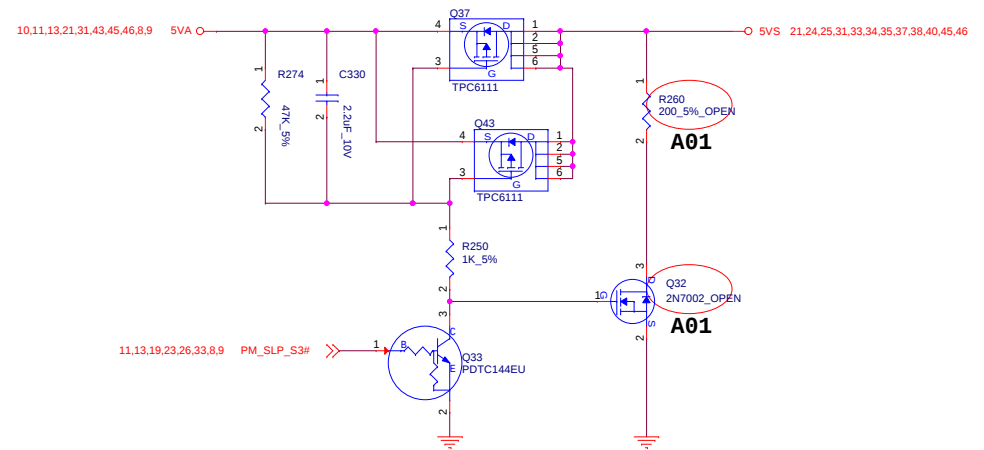
1.8VS



3VS



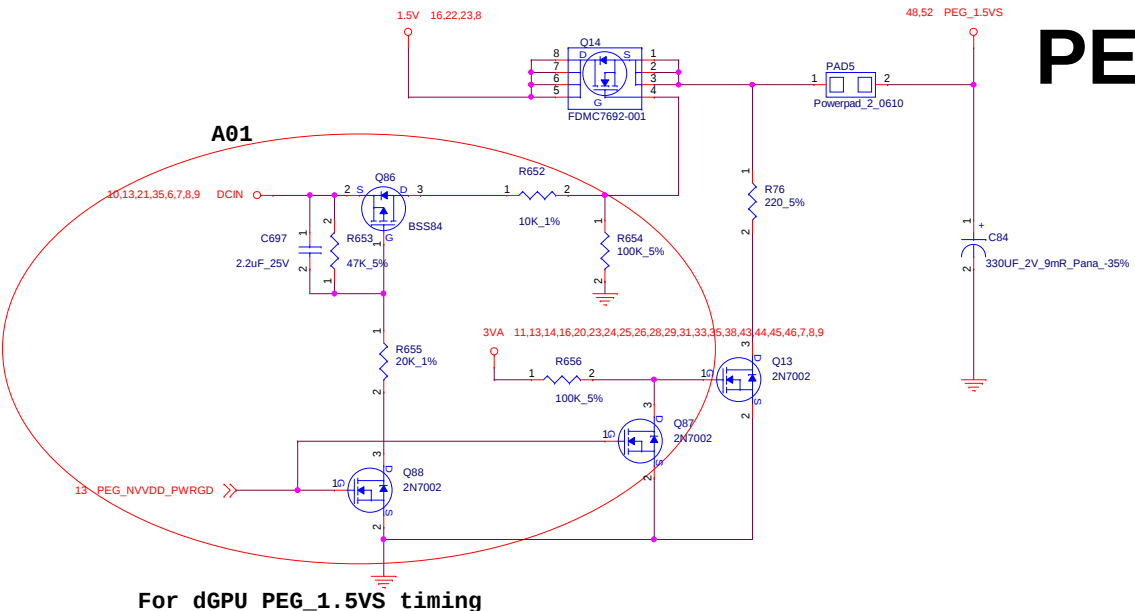
5VS



INVENTEC

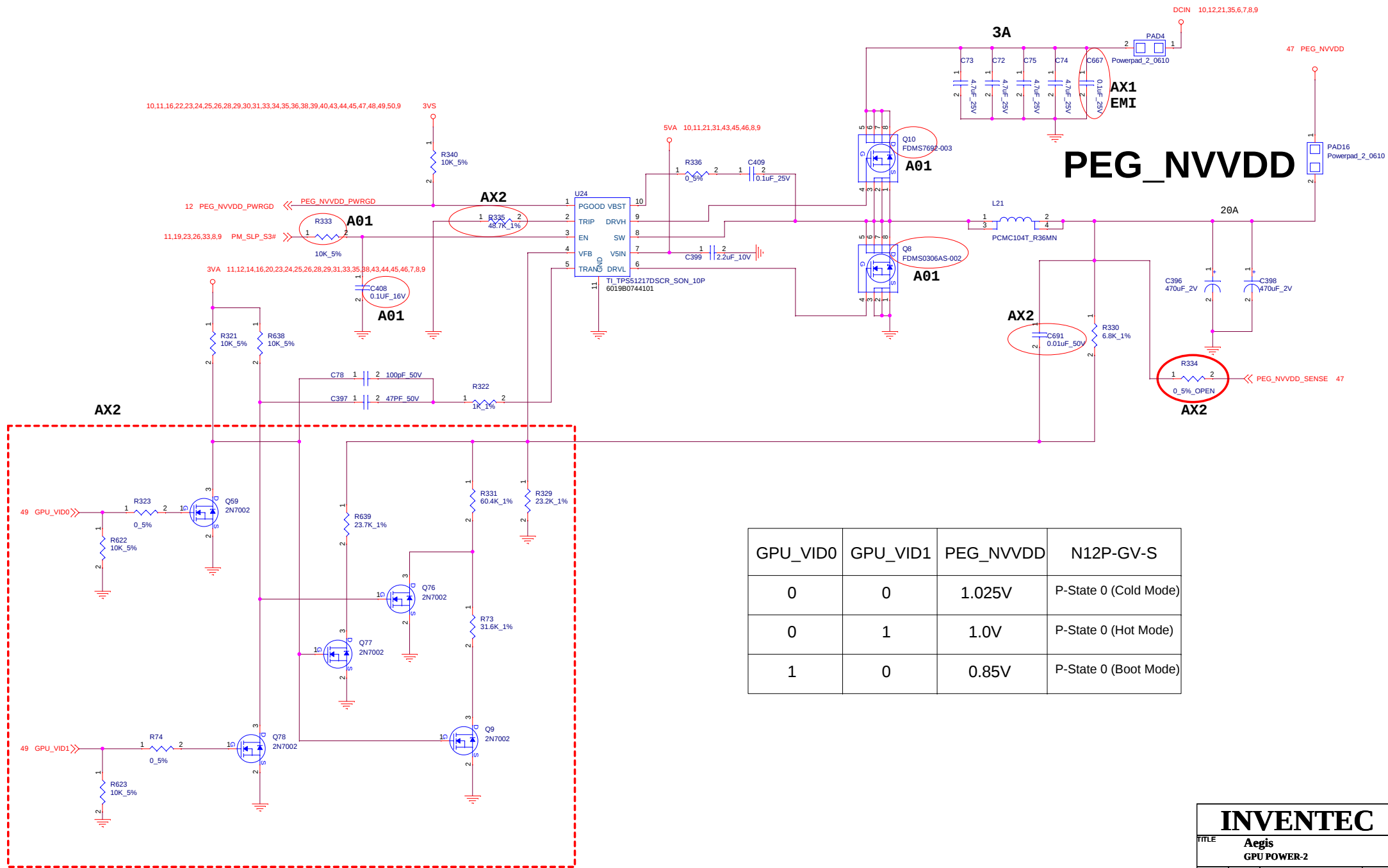
TITLE			
Aegis			
3VS/5VS/1.8VS			
SIZE	CODE	DOC NUMBER	REV
Custom	ES	CS-131	A01
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PEG_1.5VS

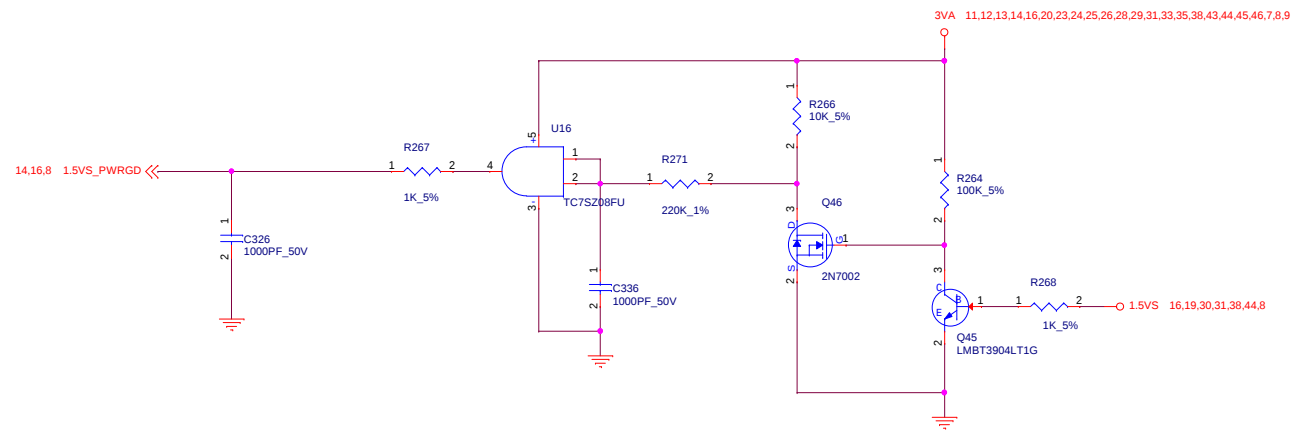
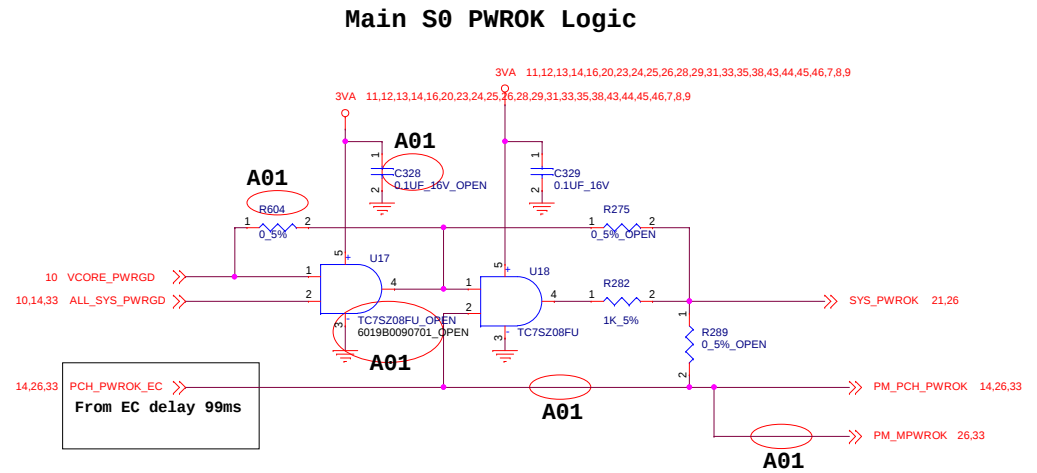
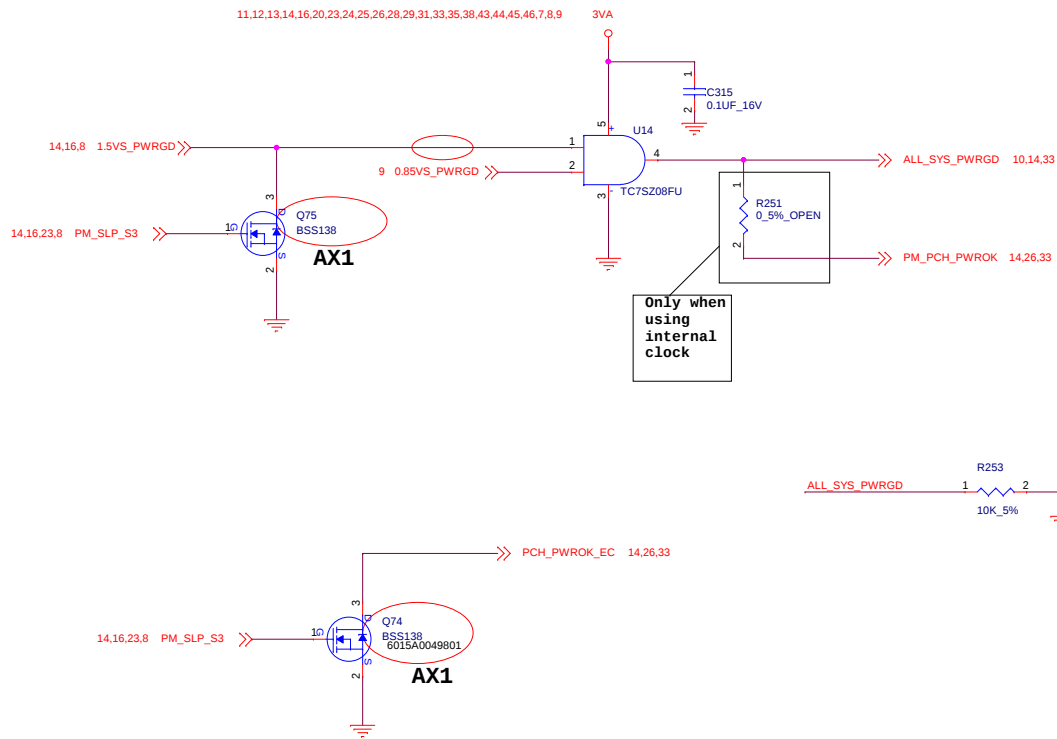


INVENTEC			
TITLE			
Aegis			
GPU Power-1			
SIZE	CODE	DOC.NUMBER	REV
Custom	ES	CS-131	A01
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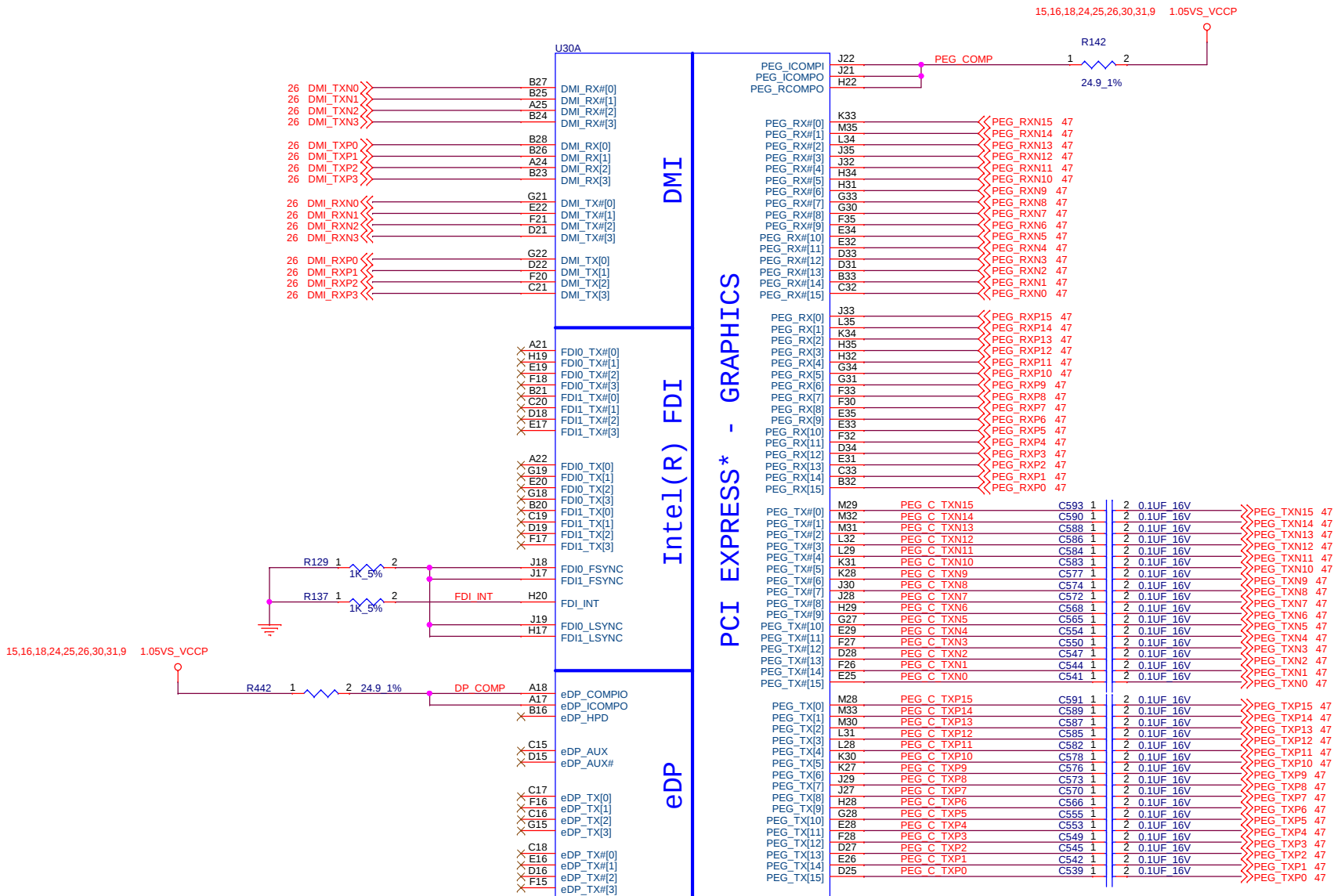
CHANGE by	IEC	DATE	Friday, December 10, 2010
2			



GPU_VID0	GPU_VID1	PEG_NVVDD	N12P-GV-S
0	0	1.025V	P-State 0 (Cold Mode)
0	1	1.0V	P-State 0 (Hot Mode)
1	0	0.85V	P-State 0 (Boot Mode)



INVENTEC				
TITLE Aegis Power Sequence				
SIZE Custom	CODE ES	DOC.NUMBER CS-131	REV A01	
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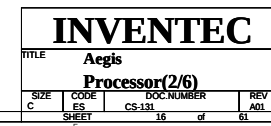


FOX PZ98927_3641_41F_Huronriver_989P
6026B0154901

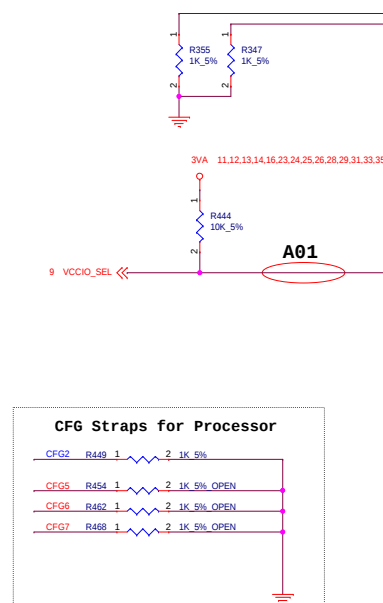
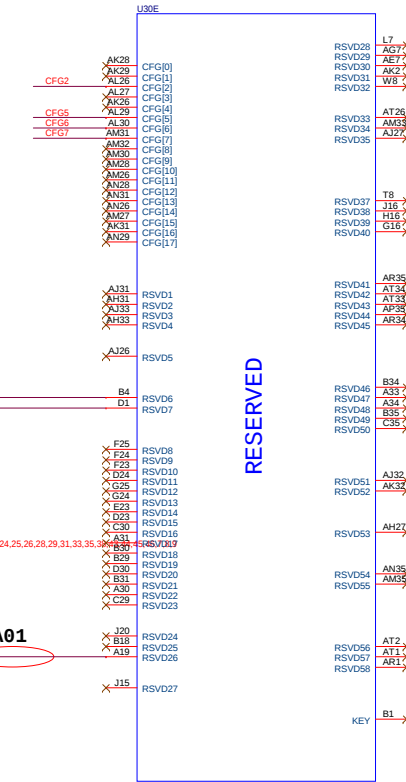
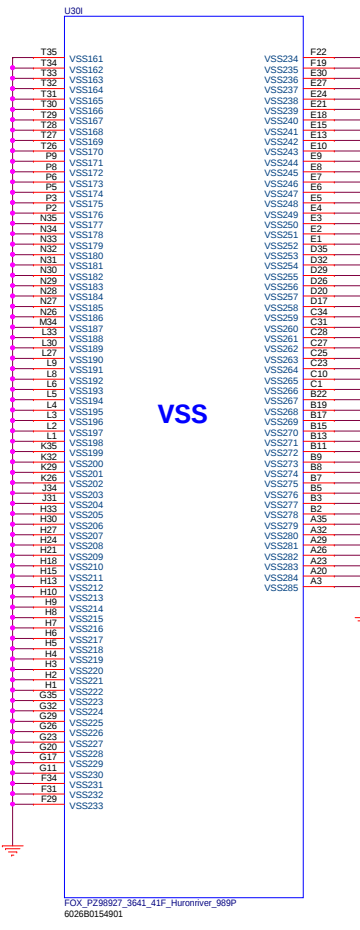
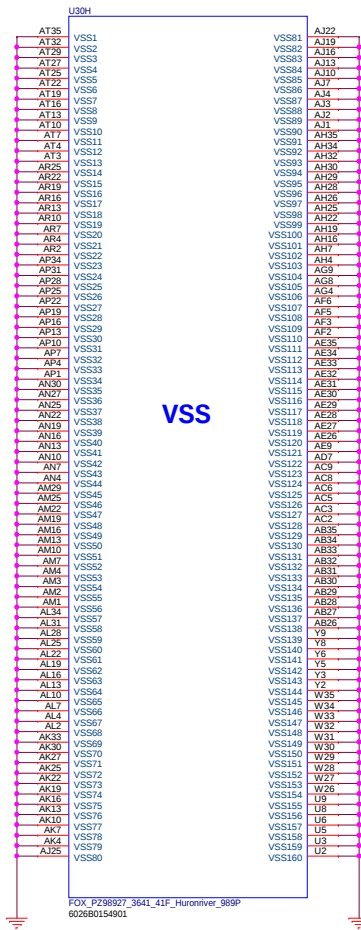
CLOSED TO CPU

INVENTEC				
TITLE Aegis				
Processor(1/6)				
SIZE B	CODE ES	DOC.NUMBER CS-131	REV A01	
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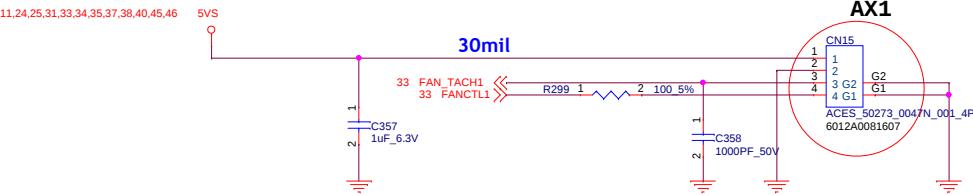
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1:(Default) Normal operation; Line # definition matches socket pin map definition 0:Lane Reversed

PCIe Port Bifurcation Straps	
CFG[6:5]	11:(Default)x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

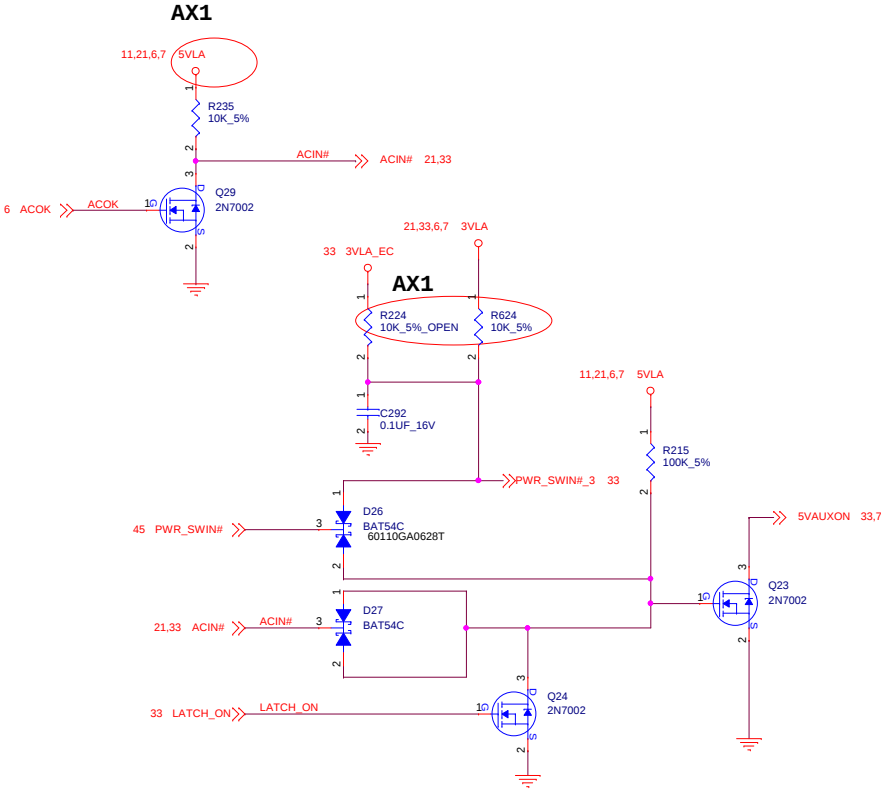
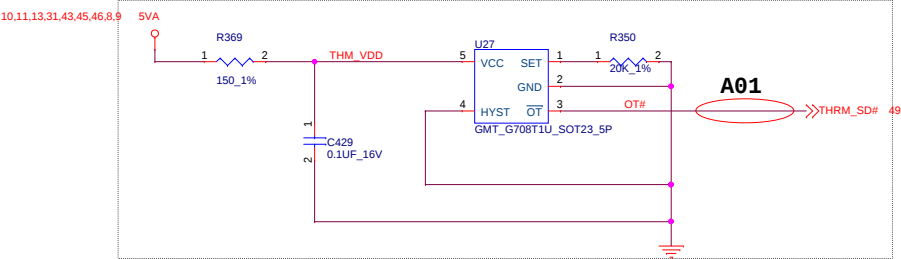
PEG DEFER TRAINING	
CFG7	1:(Default) PEG Train immediately following RESETB de assertion 0:PEG Wait for BIOS for training

INVENTEC			
Aegis			
Processor(6/6)			
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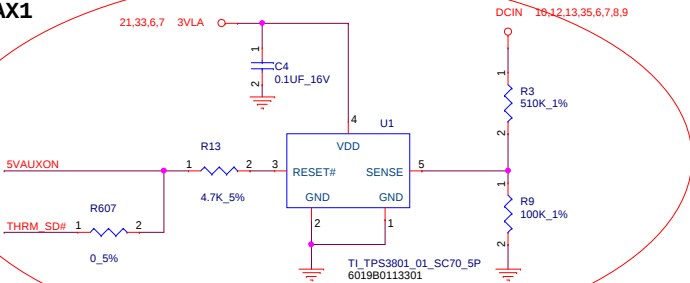
Fan control



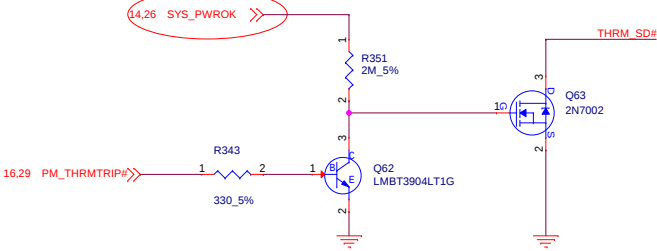
Temperature Security



AX1



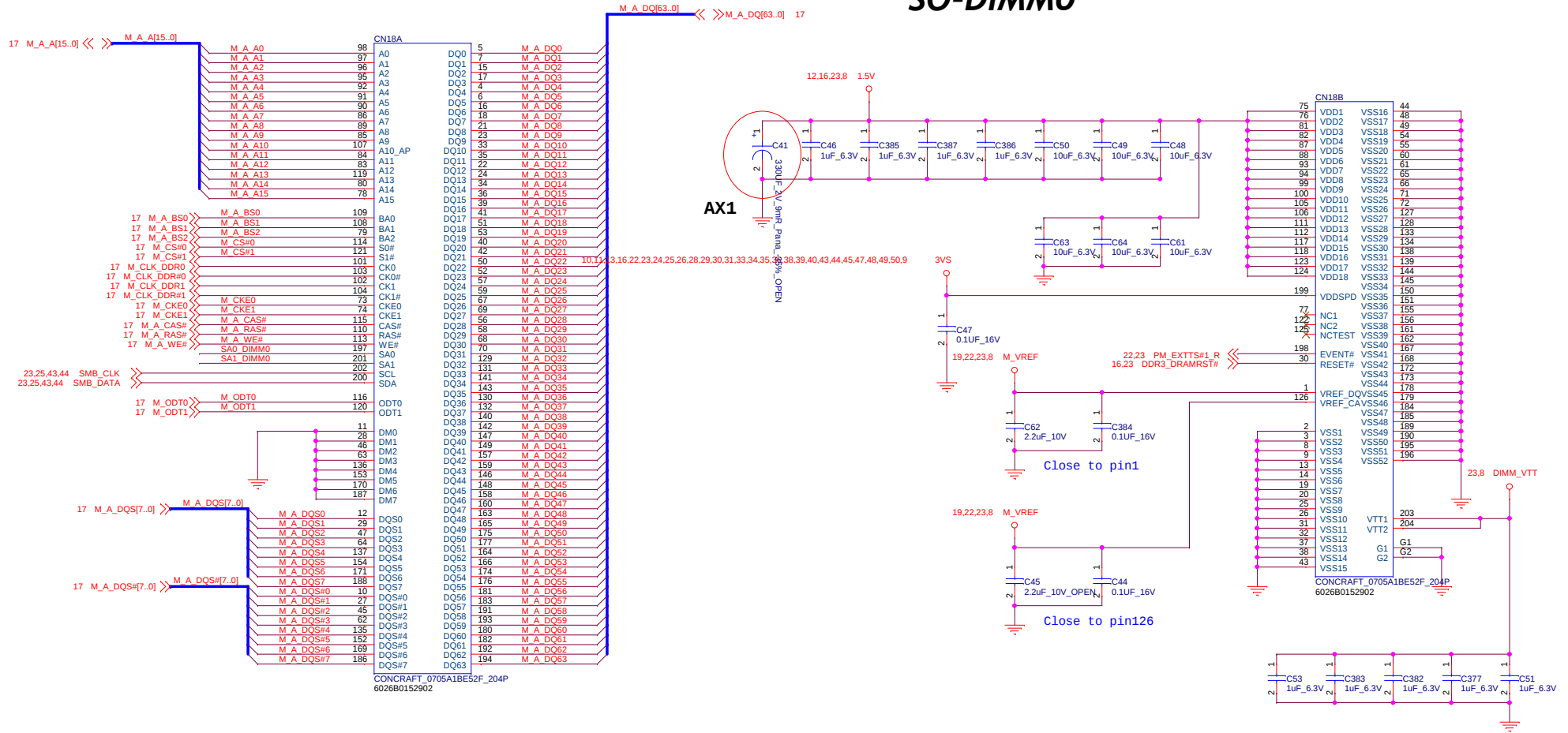
AX1



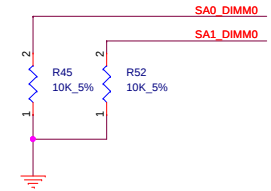
INVENTEC				
TITLE Aegis FAN / THERMAL				
SIZE Custom	CODE ES	DOC.NUMBER CS-131	REV A01	
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Need change for layout

SO-DIMM0

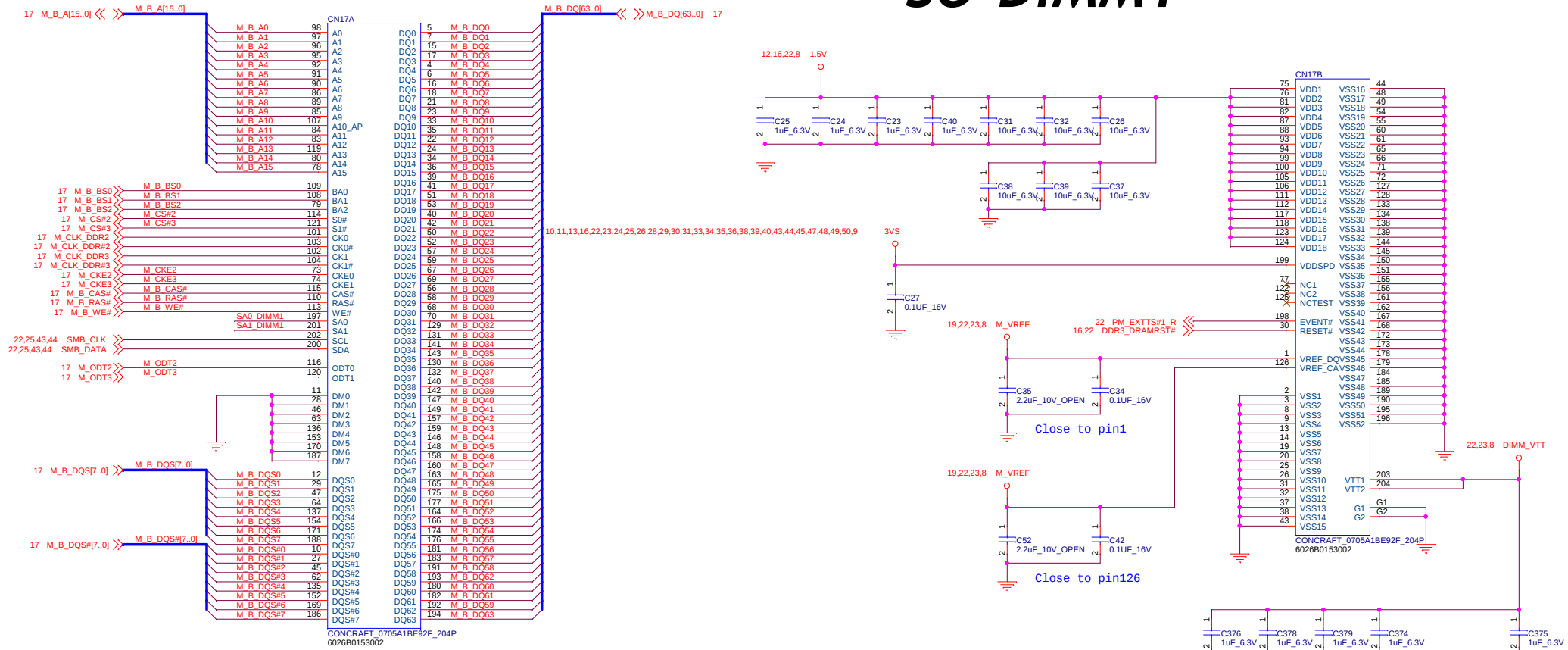


NOTE:
 IF SA0 DIMM0=0, SA1 DIMM0=0
 SO-DIMMA SPD ADDRESS IS 0XA0
 SO-DIMMA TS ADDRESS IS 0X30
 IF SA0 DIMM0=1, SA1 DIMM0=0
 SO-DIMMA SPD ADDRESS IS 0XA2
 SO-DIMMA TS ADDRESS IS 0X32

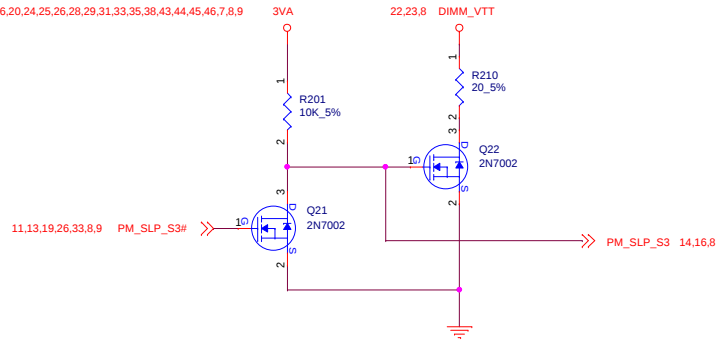


INVENTEC			
Aegis			
DDR3 SODIMM-A			
SIZE	CODE	DOC.NUMBER	REV
Custom	ES	CS-131	A01
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SO-DIMM1



NOTE:
 IF SA0 DIMM0=0, SA1 DIMM0=0
 SO-DIMMA SPD ADDRESS IS 0XA0
 SO-DIMMA TS ADDRESS IS 0X30
 IF SA0 DIMM0=1, SA1 DIMM0=0
 SO-DIMMA SPD ADDRESS IS 0XA2
 SO-DIMMA TS ADDRESS IS 0X32



INVENTEC

TITLE			
Aegis			
DDR3 SODIMM-B			
SIZE	CODE	DOC.NUMBER	REV
Custom	ES	CS-131	A01
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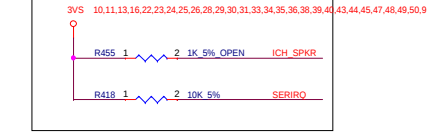
FJ request

RTC Circuit

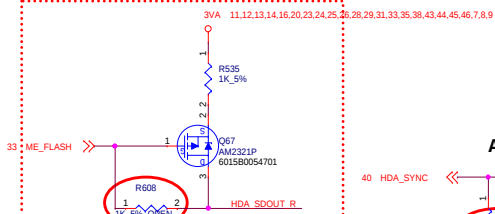
(HDA, JTAG, SPI, SATA)

located on DIMM window area.
CL1 CL2

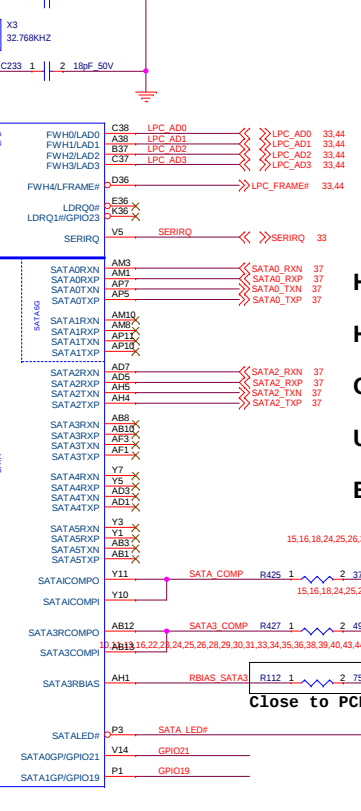
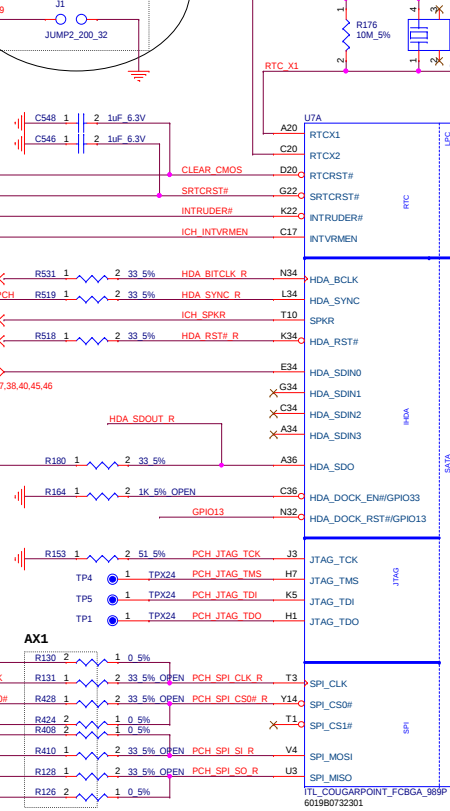
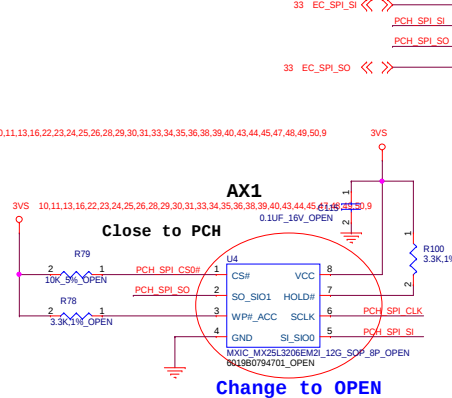
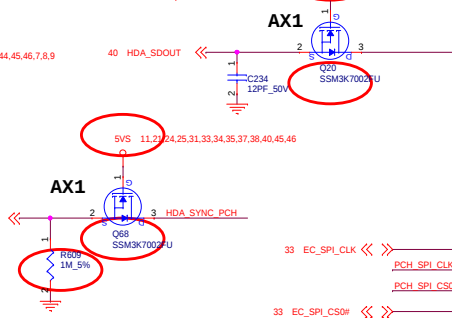
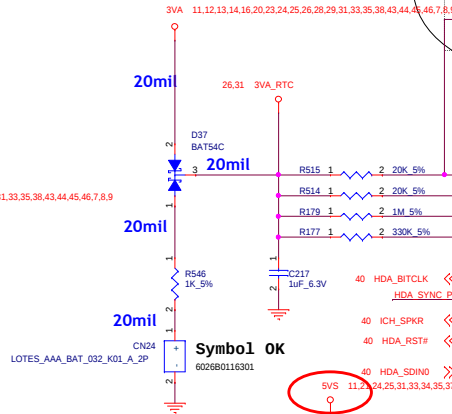
NO Reboot Strap



AX1



Flash Descriptor Security Override	
HDA_SDOUT_R	High : Enable Low : Disable



HDD I/F

HDD I/F for 17"

ODD I/F

USB3.0 for 17"

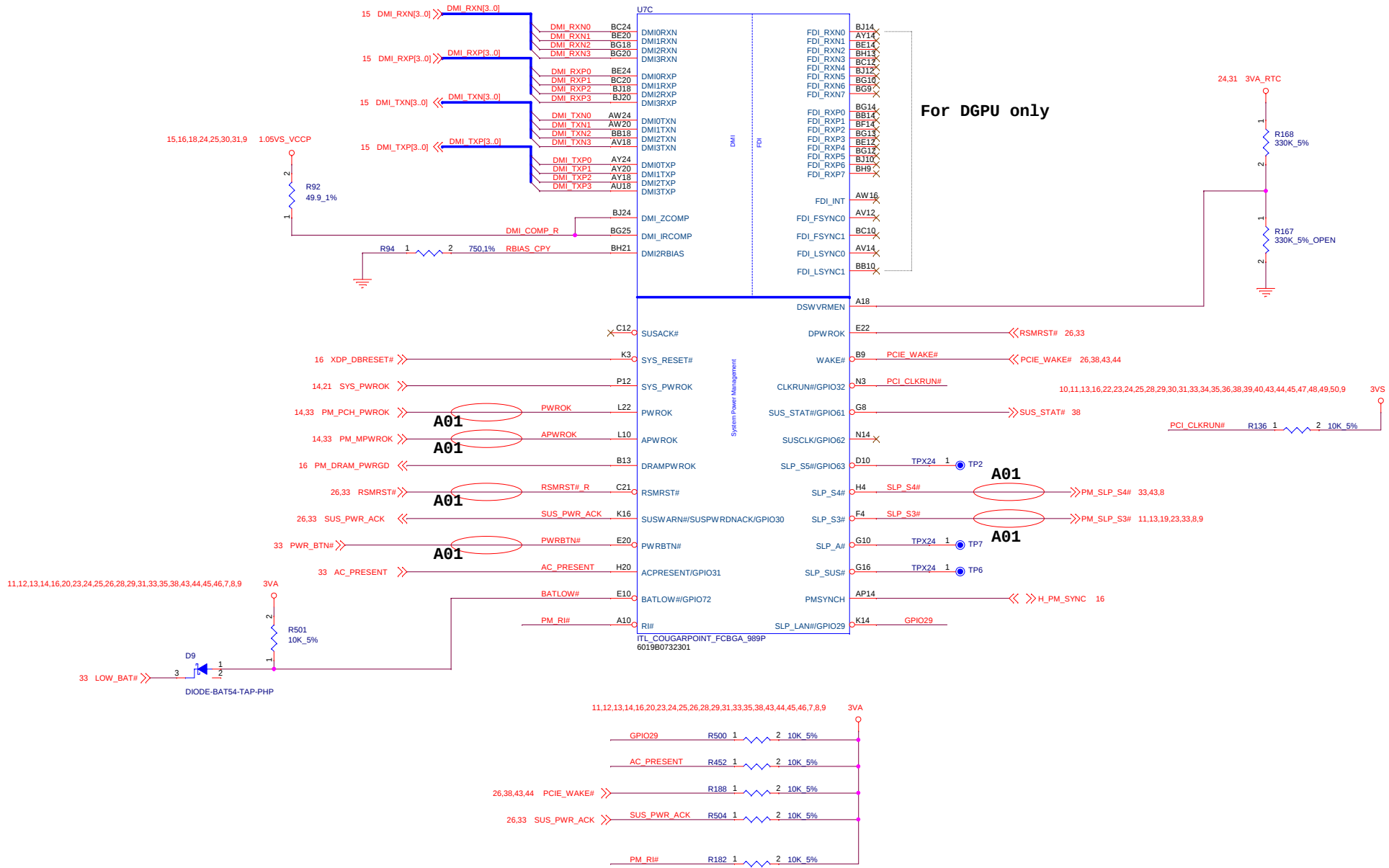
ESATA I/F

Close to PCH

INVENTEC

TITLE			
Aegis			
PCH (I/O)-(HDA,JTAG,SATA)			
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(DMI, FDI, GPIO)



INVENTEC

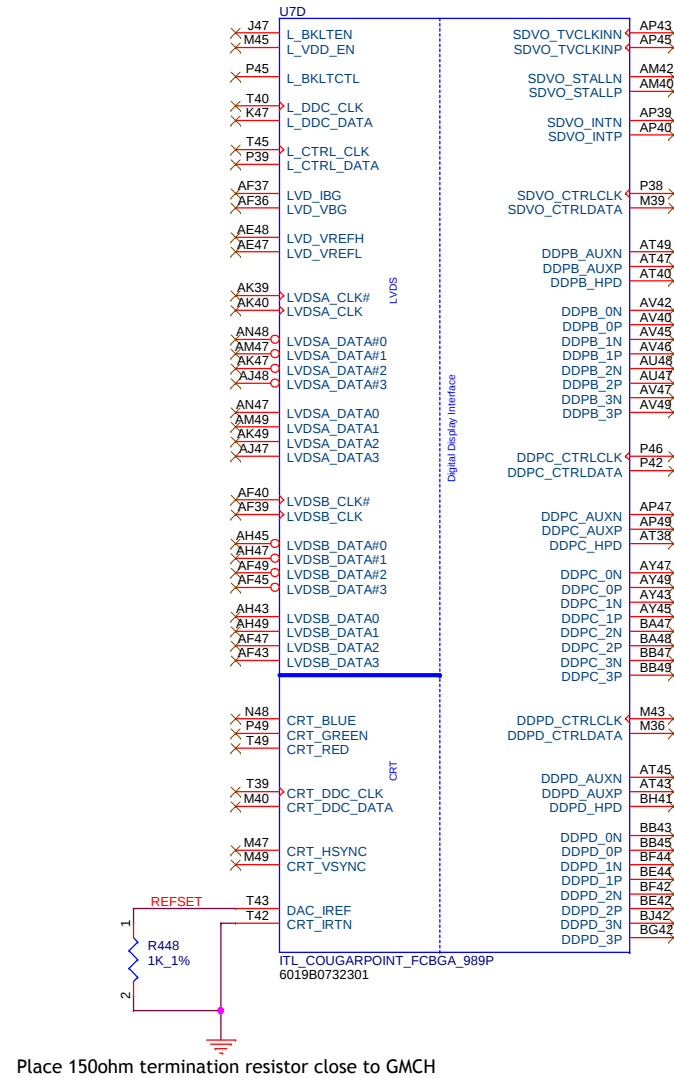
TITLE
Aegis
PCH (3/9)-(DMI,FDI,GPIO)

SIZE Custom	CODE ES	DOC.NUMBER CS-131	REV A01
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(LVDS, DDI)



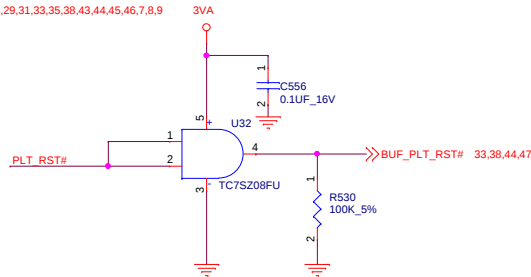
Place 150ohm termination resistor close to GMCH

INVENTEC

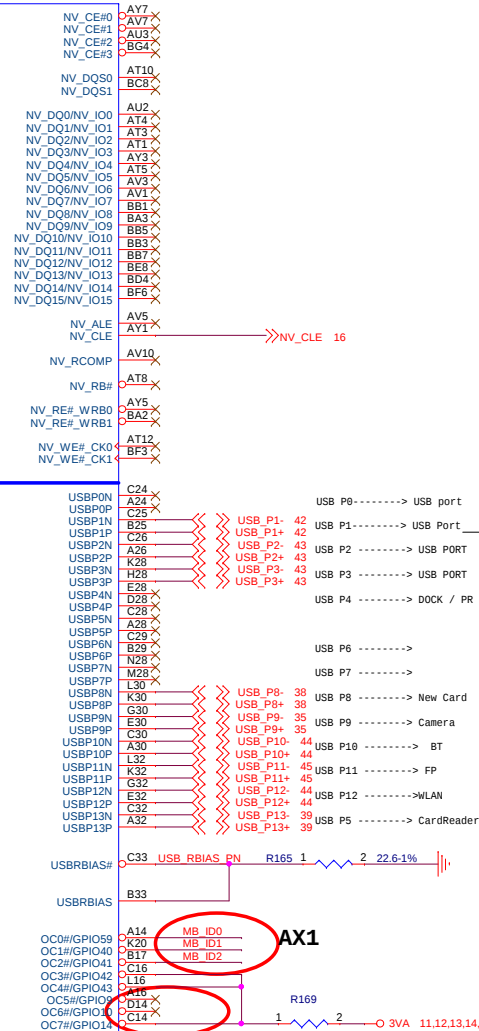
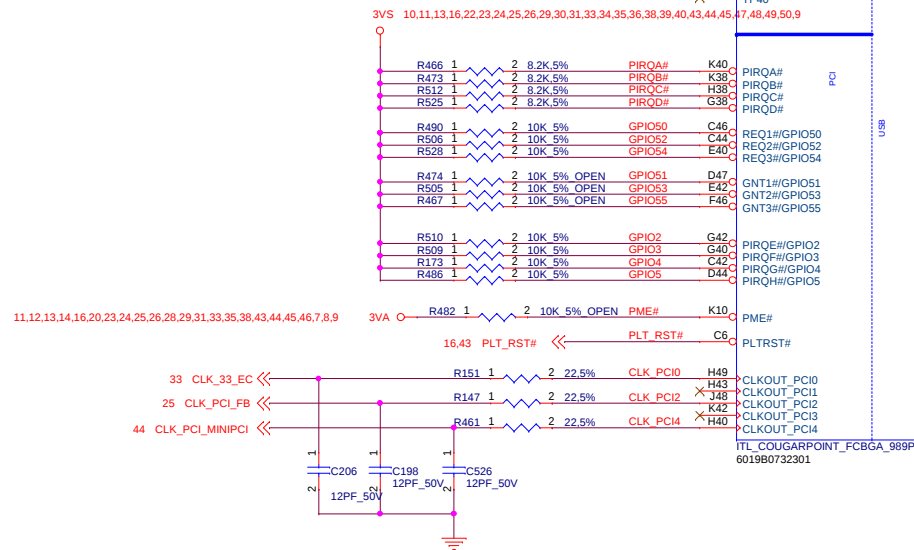
TITLE			
Aegis PCH (4/9)-(LVDS,DDI)			
SIZE B	CODE ES	DOC.NUMBER CS-131	REV A01
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(PCI, USB, NVRAM)



Buffer to reduce loading on PLT_RST#

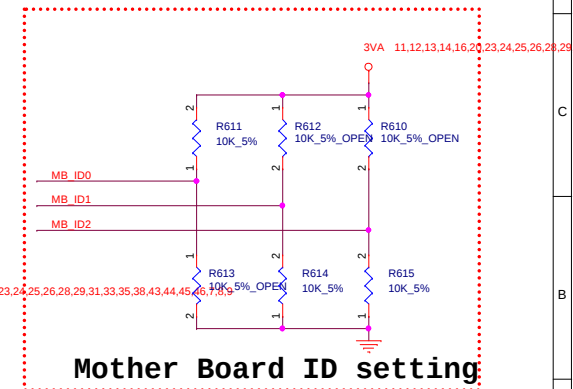


FJ Mother Board ID setting

Project	MB_ID2	MB_ID1	MB_ID0
	0	0	0
Aegis (Discrete)	0	0	1
Neurron (UMA)	0	1	0
Neuron-V (Optimus)	0	1	1
Strike (UMA)	1	0	0
Strike-V (Optimus)	1	0	1
Silk (UMA)	1	1	0
Silk-V (Optimus)	1	1	1
PCH ----->	GPIO41	GPIO40	GPIO59

For Debug

AX1

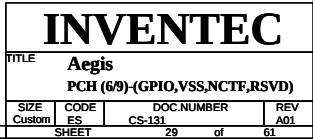


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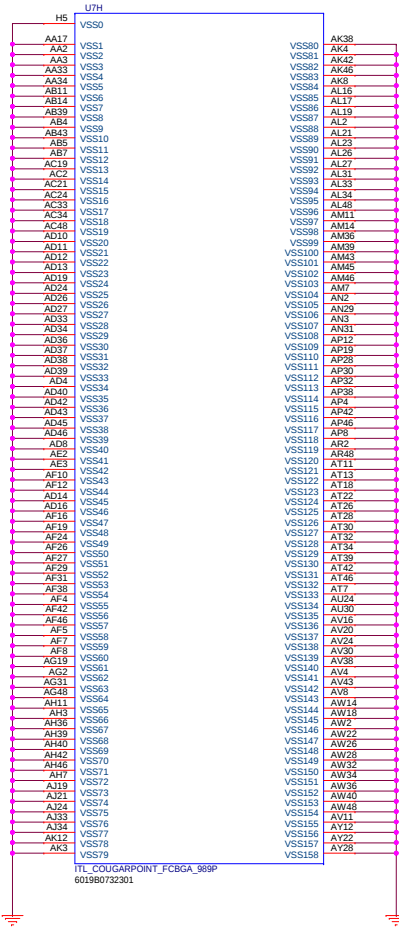
TITLE	Aegis PCH (5/9)-(PCI,USB,NVRAM)
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SIZE Custom	CODE ES	DOC.NUMBER CS-131	REV A01
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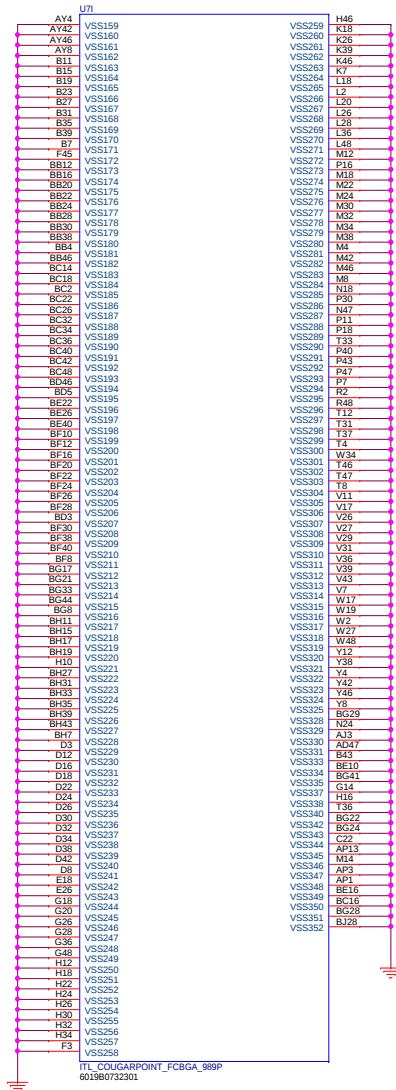
CHANGE by	IEC	DATE	Friday, December 10, 2010
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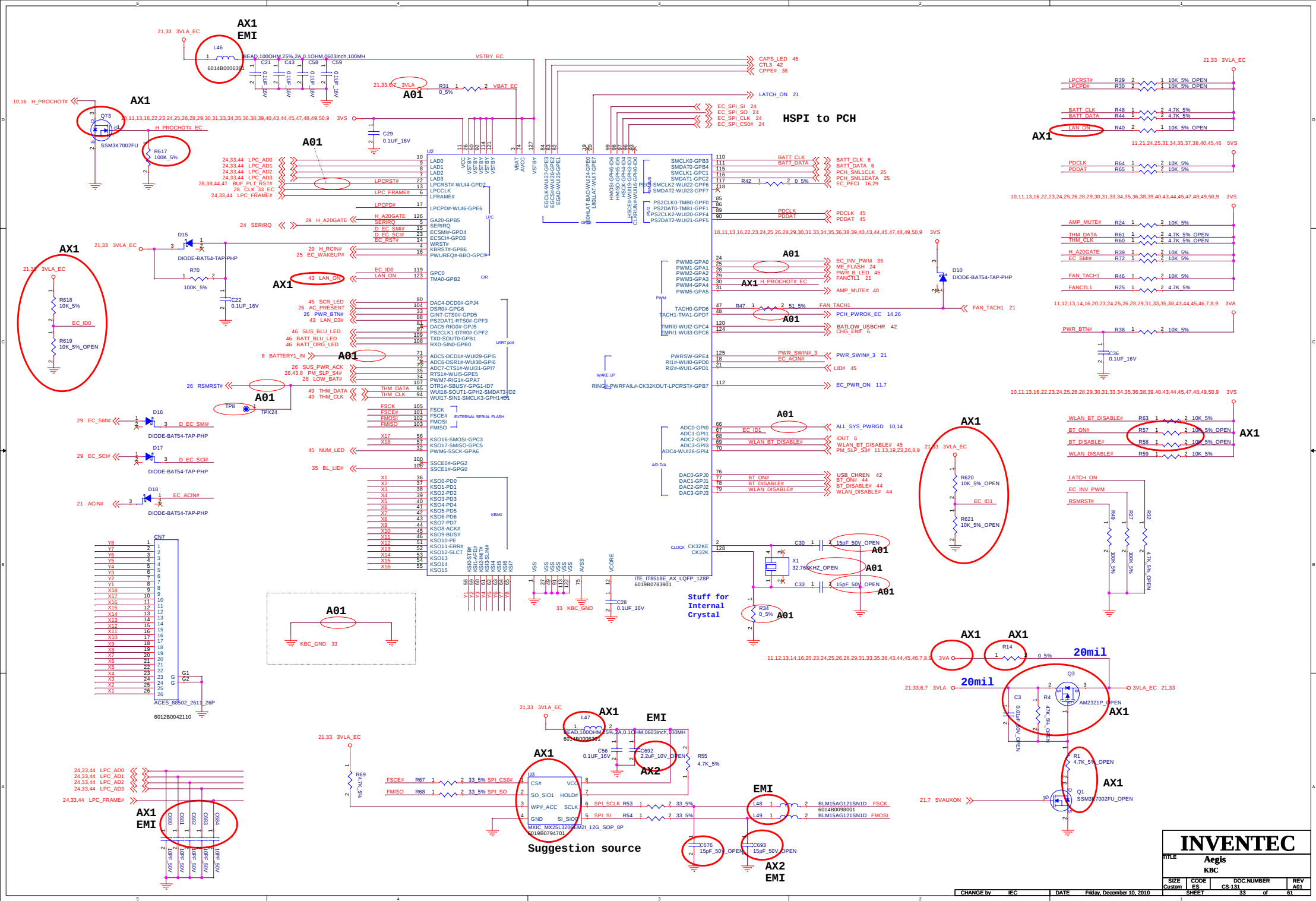


(GND)

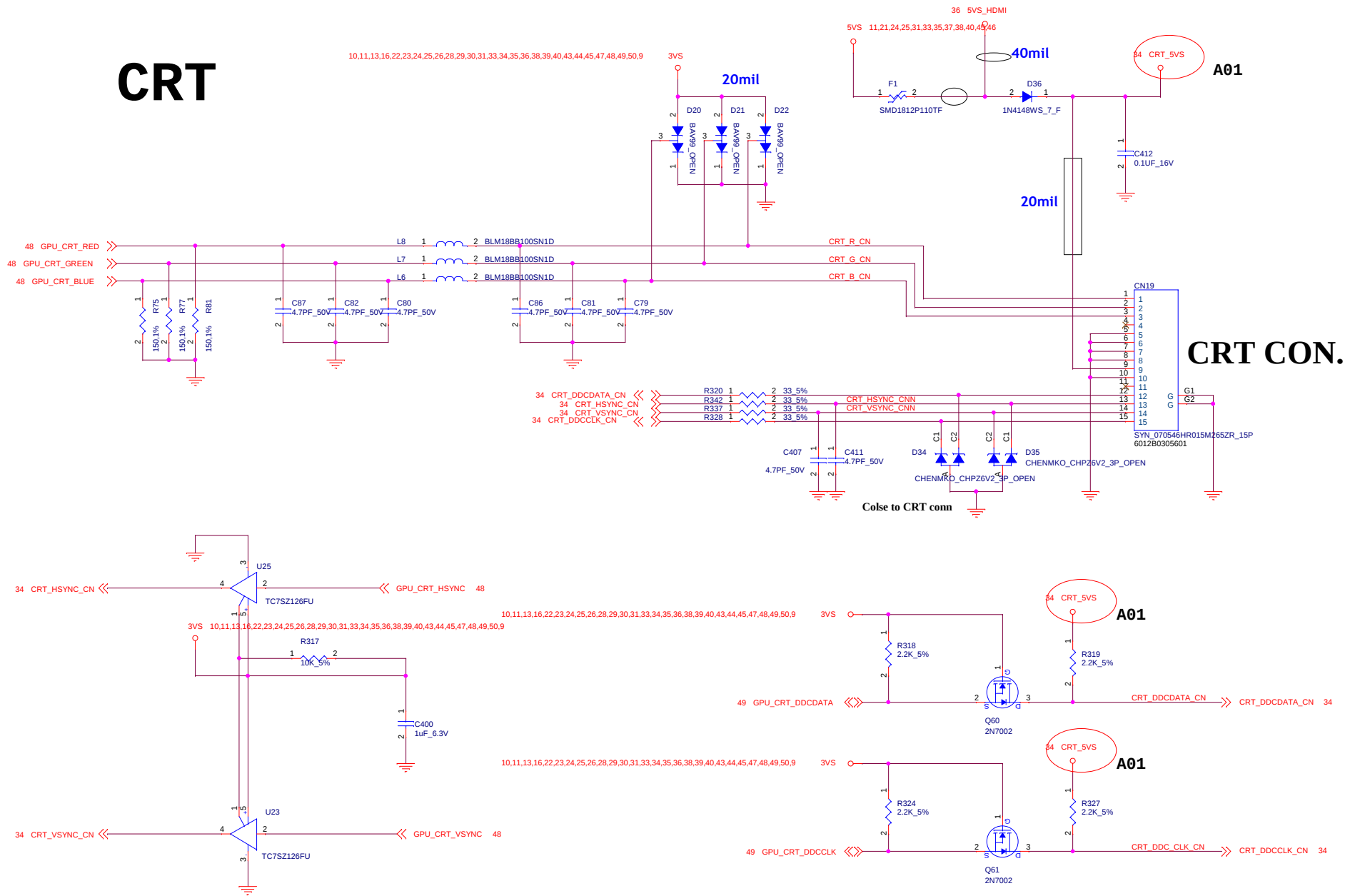


(GND)





CRT



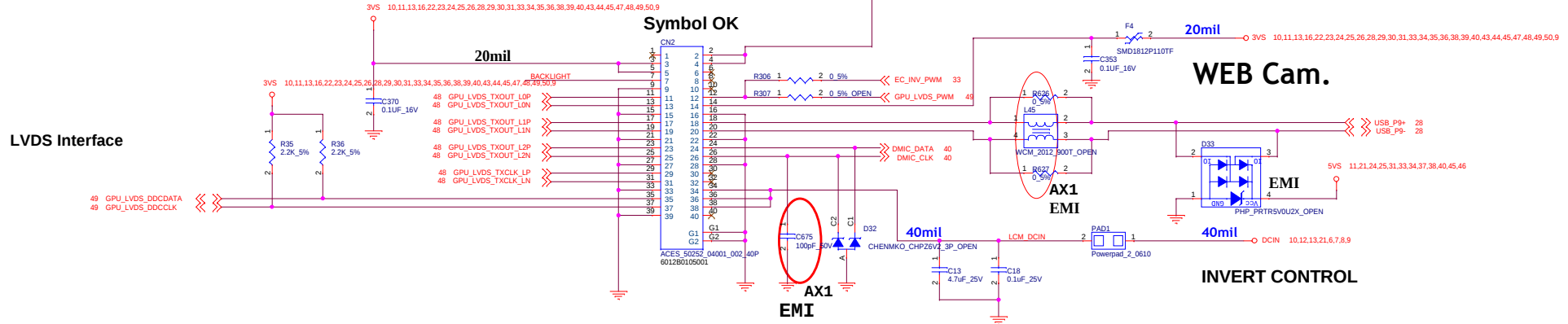
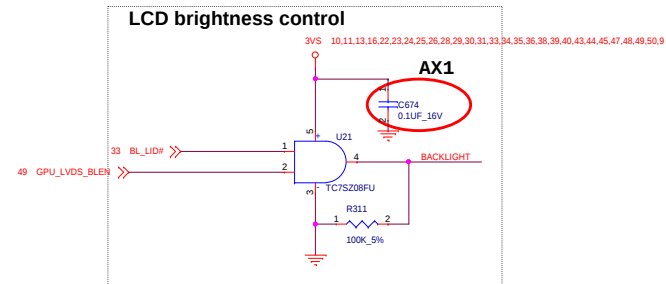
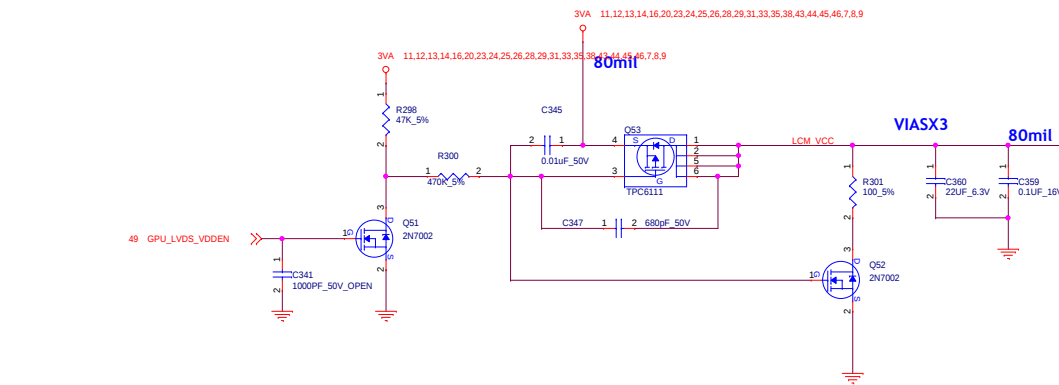
INVENTEC

TITLE **Aegis CRT**

SIZE Custom	CODE ES	DOC.NUMBER CS-131	REV A01
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CHANGE by IEC DATE Friday, December 10, 2010

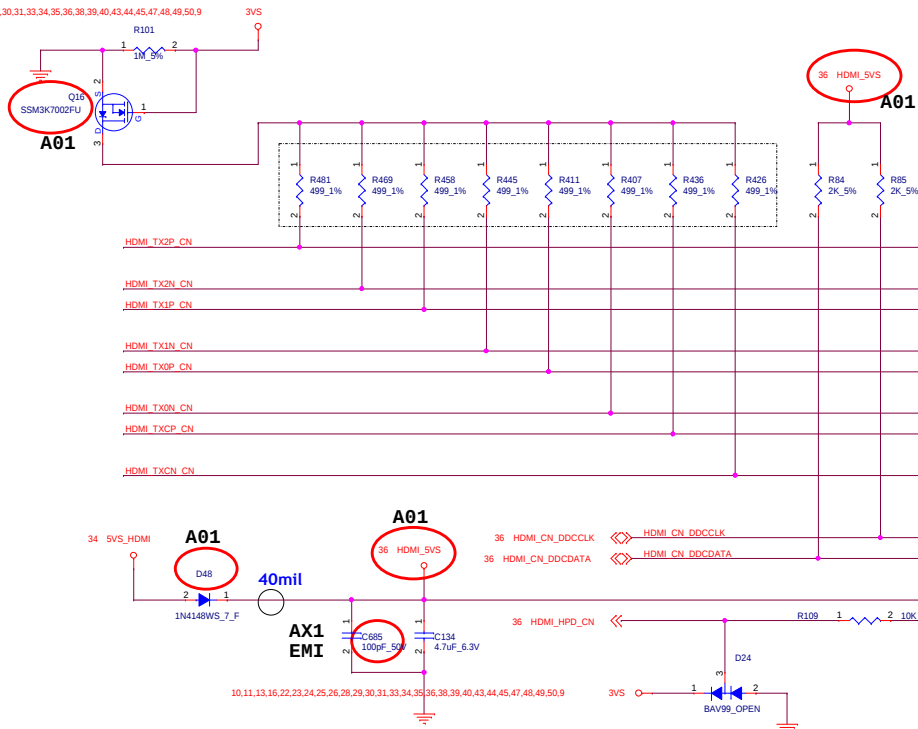
SHEET 34 of 61



Please as close as possible to the LVDS CONN

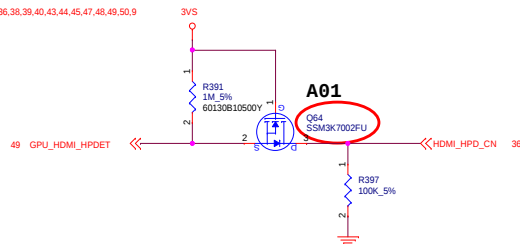
INVENTEC			
TITLE Aegis LVDS			
SIZE C	CODE ES	DOC.NUMBER CS-131	REV A01
SHEET 35		of 61	

10.11.13.16.22.23.24.25.26.28.29.30.31.33.34.35.36.38.39.40.43.44.45.47.48.49.50.9

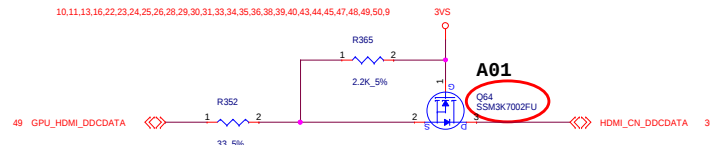


49 GPU_HDMI_TX2P	>>	C536	1	2	0.1uF 16V	HDMI_C_TX2P
49 GPU_HDMI_TX2N	>>	C535	1	2	0.1uF 16V	HDMI_C_TX2N
49 GPU_HDMI_TX1P	>>	C521	1	2	0.1uF 16V	HDMI_C_TX1P
49 GPU_HDMI_TX1N	>>	C511	1	2	0.1uF 16V	HDMI_C_TX1N
49 GPU_HDMI_TX0P	>>	C471	1	2	0.1uF 16V	HDMI_C_TX0P
49 GPU_HDMI_TX0N	>>	C463	1	2	0.1uF 16V	HDMI_C_TX0N
49 GPU_HDMI_TXCP	>>	C489	1	2	0.1uF 16V	HDMI_C_TXCP
49 GPU_HDMI_TXCN	>>	C485	1	2	0.1uF 16V	HDMI_C_TXCN

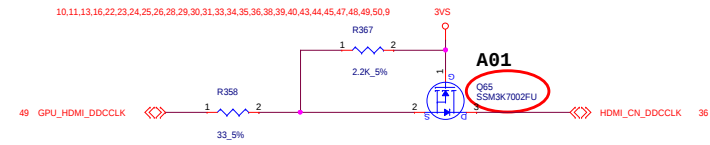
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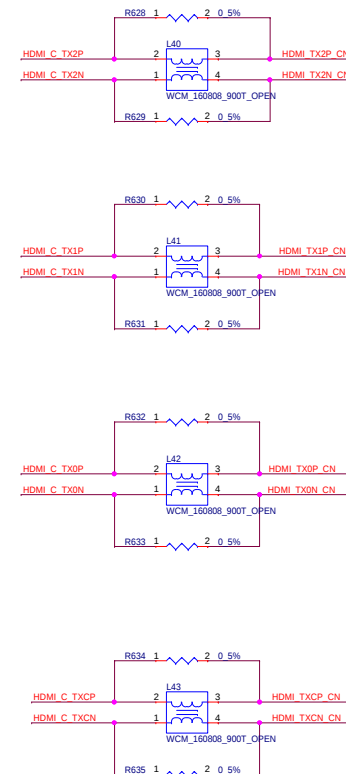
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10.11.13.16.22.23.24.25.26.28.29.30.31.33.34.35.36.38.39.40.43.44.45.47.48.49.50.9



AX1

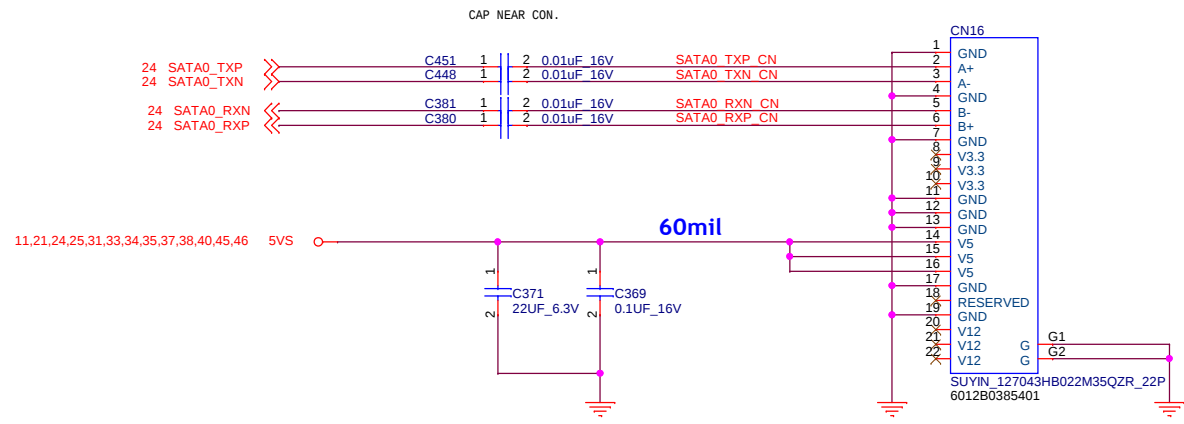


EMI

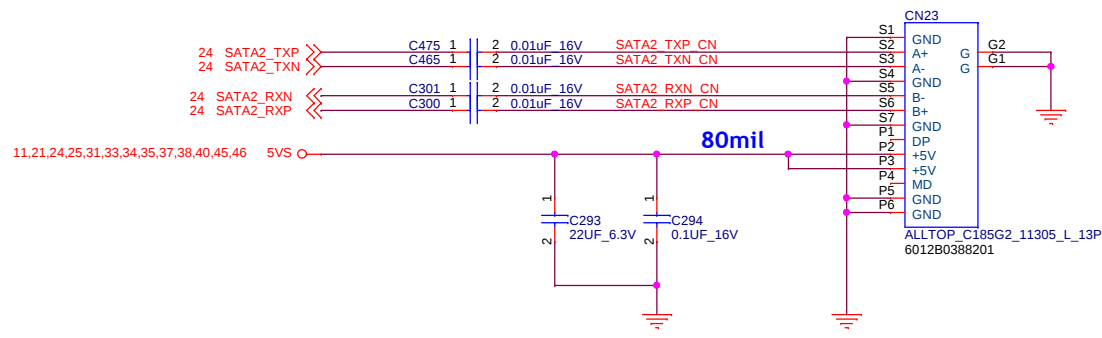
INVENTEC

TITLE				Aegis
				HDMI
SIZE	CODE	DOC NUMBER	REV	
C	ES	CS-131	A01	
SHEET				61

HDD I/F



ODD I/F

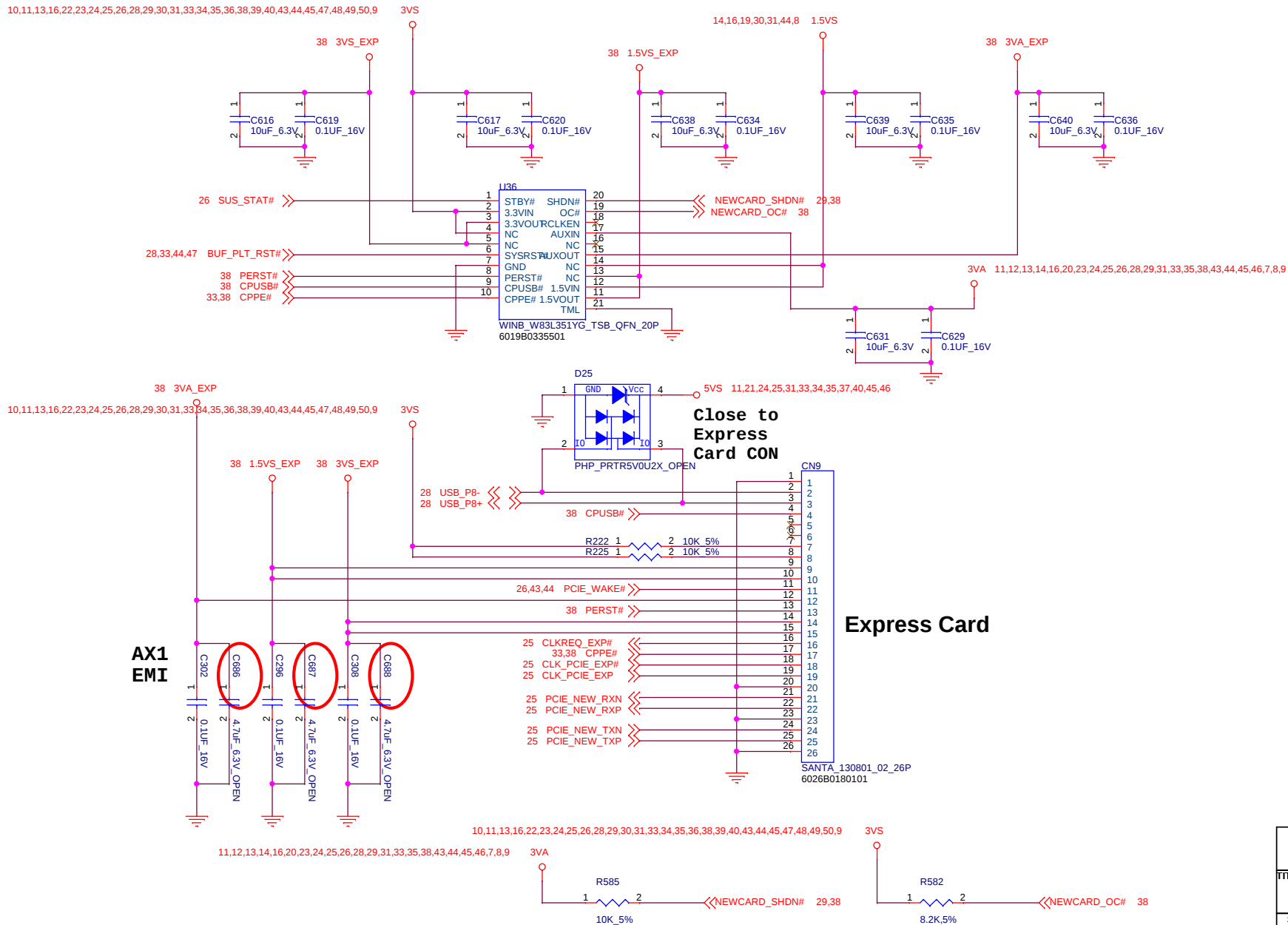


INVENTEC

TITLE			
Aegis			
SATA HDD/ODD			
SIZE	CODE	DOC.NUMBER	REV
B	ES	CS-131	A01
SHEET 37 of 61			

CHANGE by IEC DATE Friday, December 10, 2010

New Card Board

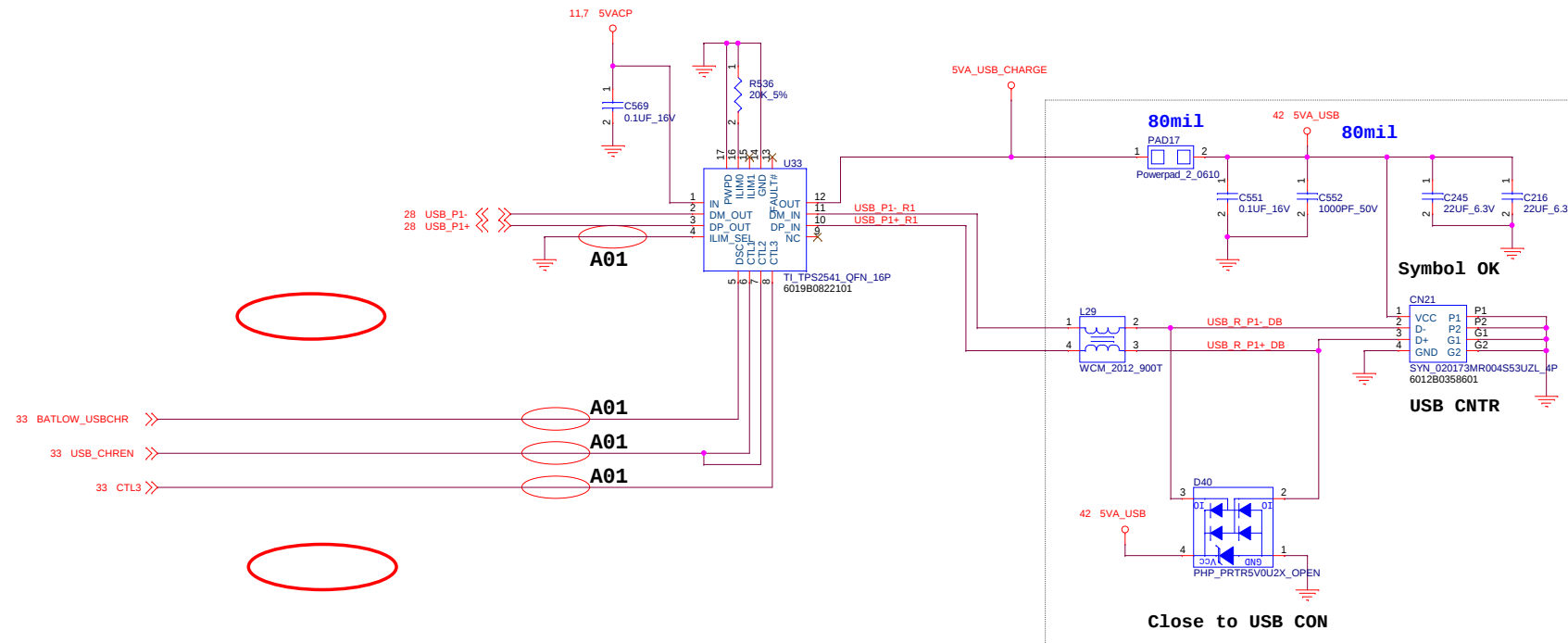


INVENTEC

TITLE			
Aegis			
Express Card			
SIZE	CODE	DOC.NUMBER	REV
B	ES	CS-131	A01
SHEET		38	of 61

CHANGE by IEC DATE Friday, December 10, 2010

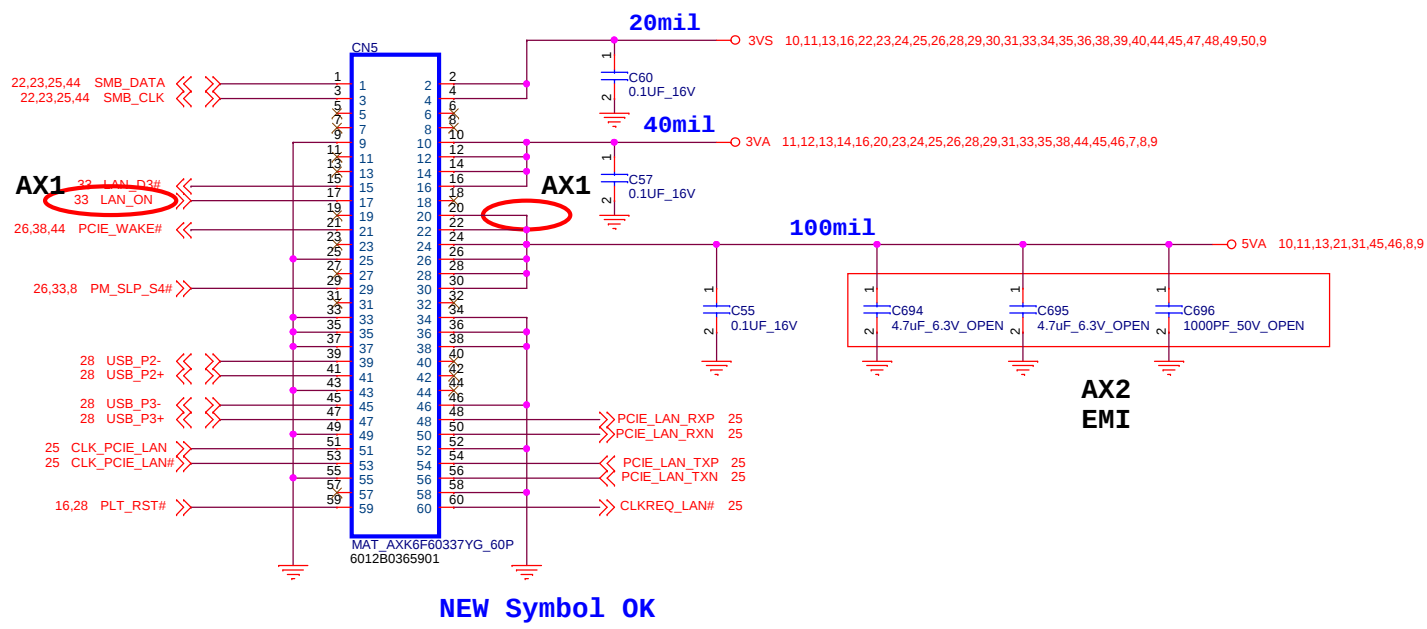
Power OFF Charge USB



INVENTEC			
TITLE Aegis USB power off charger			
SIZE Custom	CODE ES	DOC.NUMBER CS-131	REV A01
SHEET		42	of 61

Symbol Ok

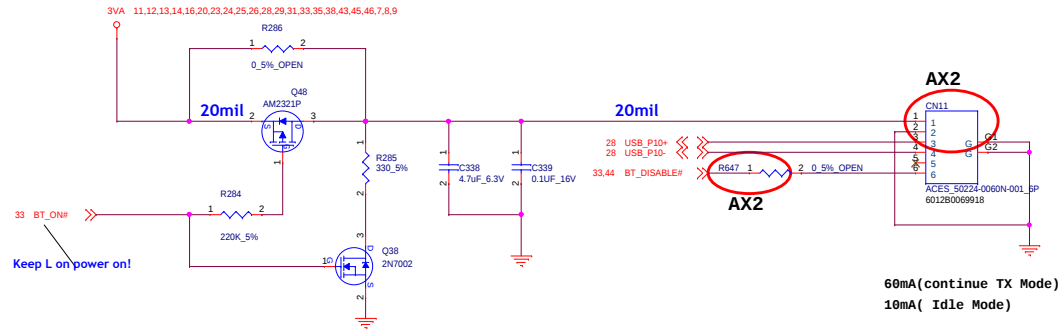
TO USB/LAN BOARD



INVENTEC			
TITLE Aegis USB/LAN I/F			
SIZE B	CODE ES	DOC.NUMBER CS-131	REV A01
SHEET 43 of 61			

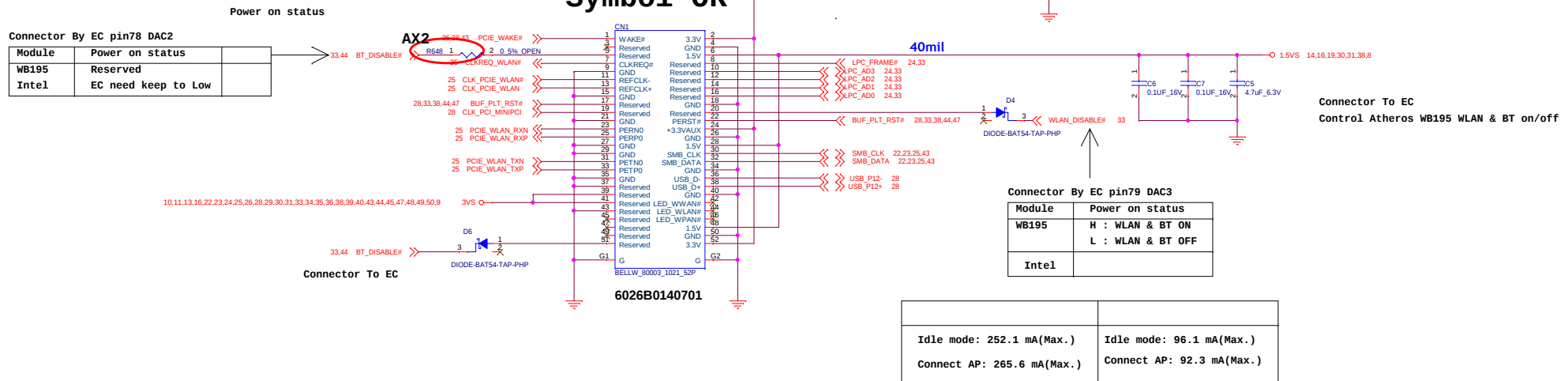
CHANGE by IEC DATE Friday, December 10, 2010

Bluetooth CNN.



PCIE Mini Card(WLAN)

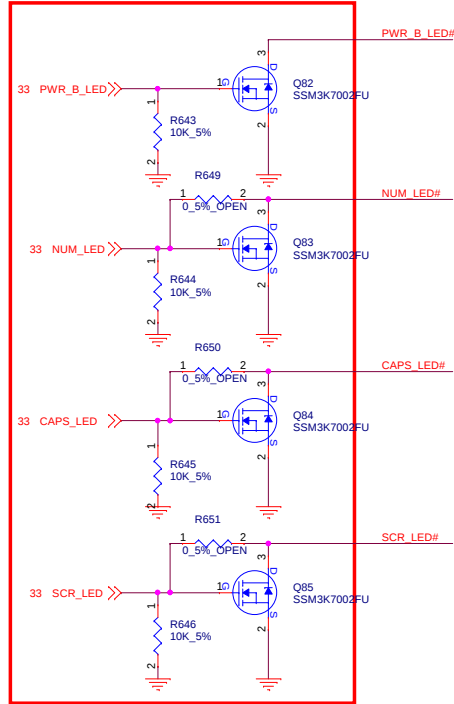
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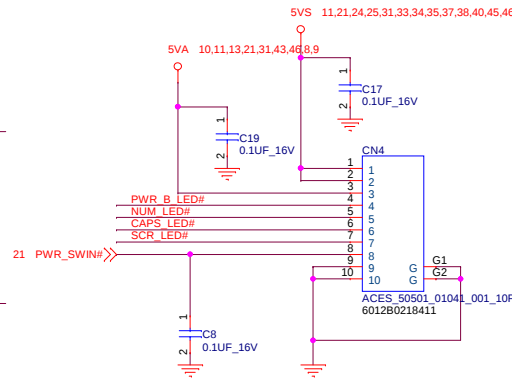
INVENTEC

TITLE			
Aegis			
WLAN/BT			
SIZE	CODE	DOC NUMBER	REV
C	ES	CS-131	A01
SHEET		44	of 61

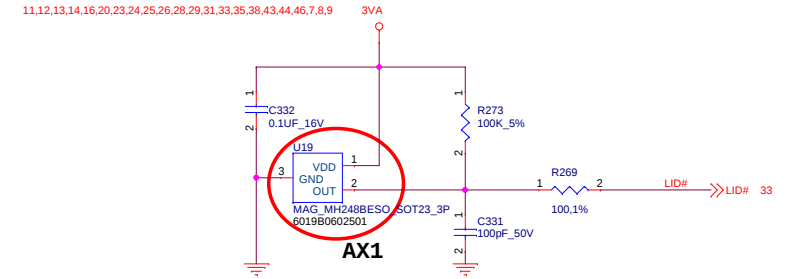
AX2



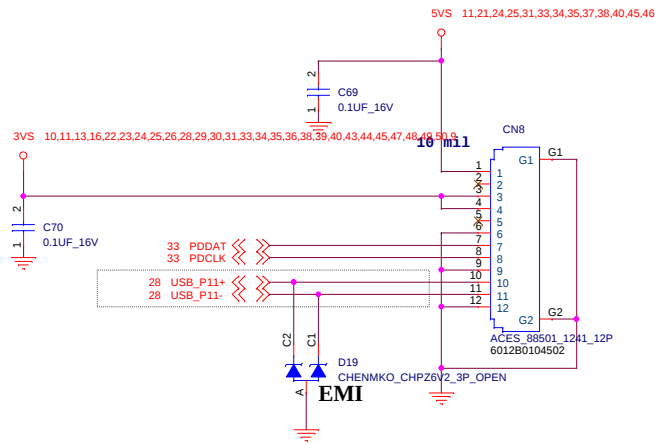
PWS + LED CNN.



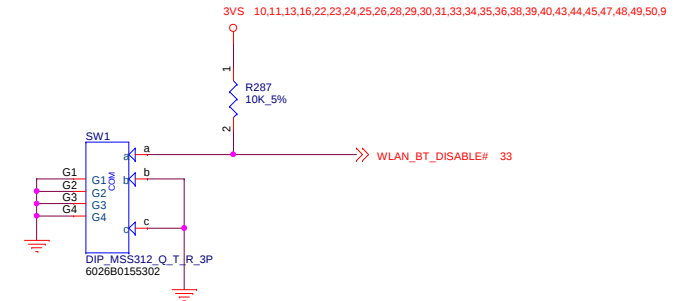
HALL Switch



GP + FP CNN.



(W-LAN, BT) sliding switch



INVENTEC

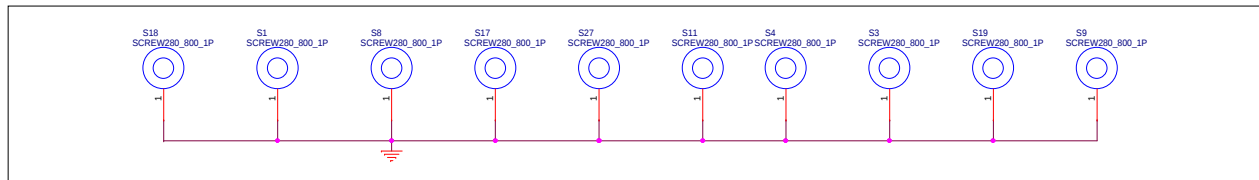
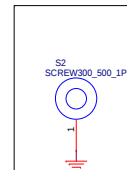
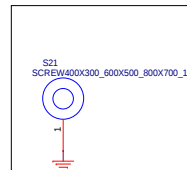
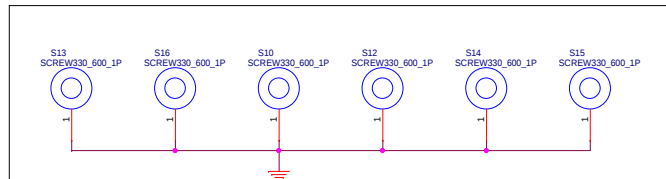
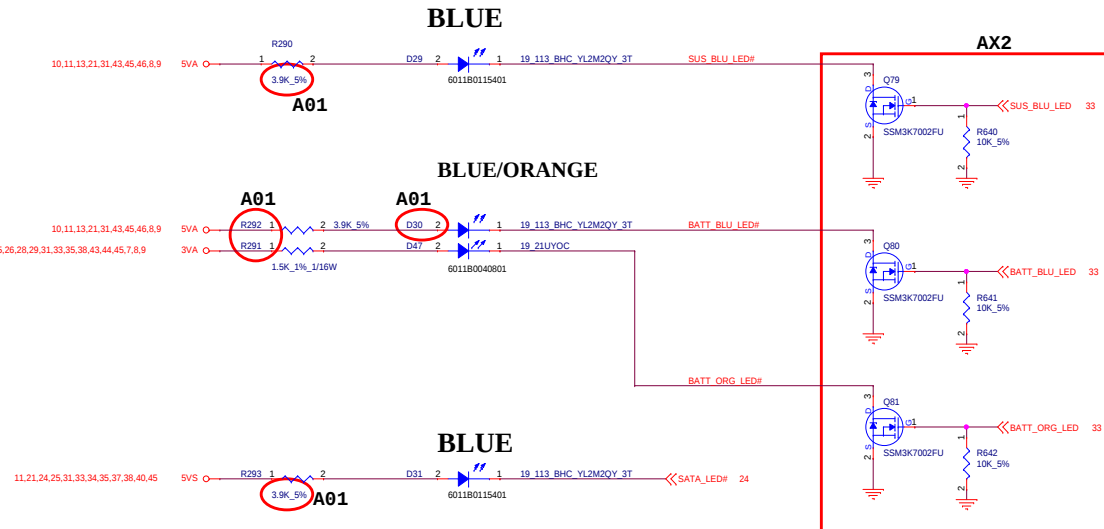
TITLE			
Aegis			
PSW/LID/ GP/FP/SL SW			
SIZE	CODE	DOC.NUMBER	REV
Custom	ES	CS-131	A01
SHEET		45	of 61

CHANGE by IEC DATE Friday, December 10, 2010

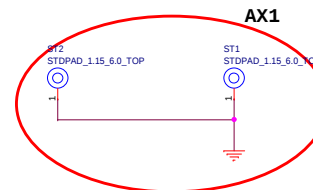
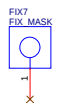
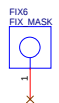
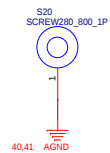
BLUE **BLUE/ORANGE** **BLUE**

Power **Charge** **HDD/ODD**

LEFT **RIGHT**



SCREW

**INVENTEC**

TITLE			
Aegis LED / SCREW			
SIZE	CODE	DOC. NUMBER	REV
C	ES	CS-131	A01
SHEET		46 of	61

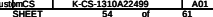
Aegis

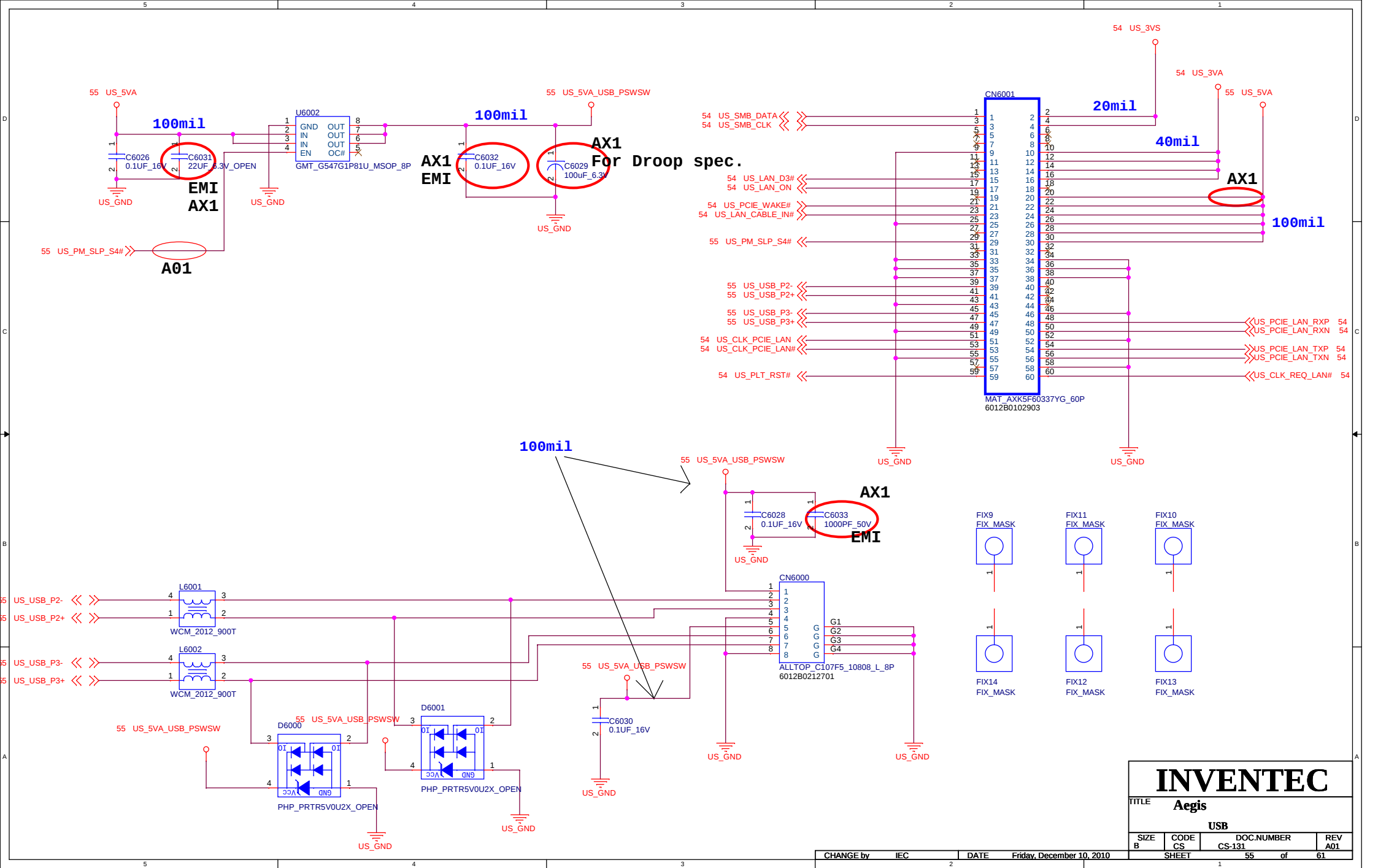
USB Board

2010.12.10 A01 Build

Thursday, Jun 26, 2008	3rd Issue	A01
Monday, May 26, 2008	Second Issue	AX1
Thursday, April 17, 2008	First Issue	A01
DATE	CHANGE NO.	REV

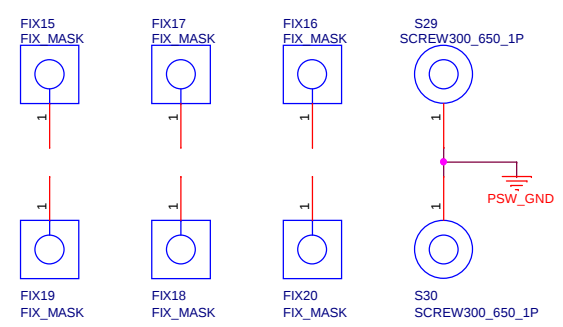
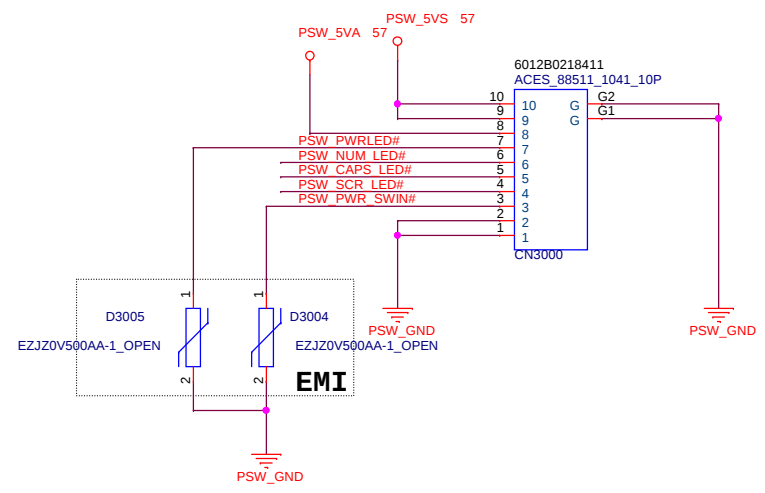
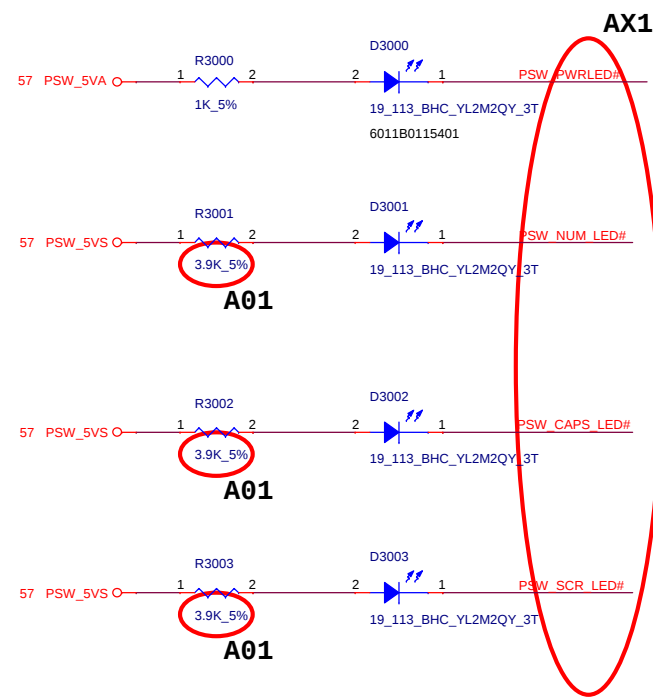
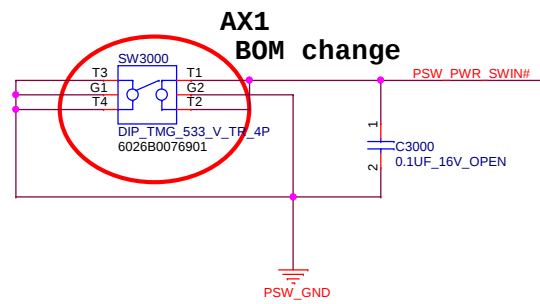
	EE	DATE	POWER	DATE	INVENTEC			
DRAWER					TITLE USB Board			
DESIGN								
CHECK								
RESPONSIBLE								
SIZE=				VER:	SIZE	CODE	DOC NUMBER	REV
FILE NAME: XXXX-XXXXXX-XX					C	CS	K-CS-1310A2221S-ALG	A01
PIN: XXXXXXXXXX					SHEET	53	of	51





2010.12.10 A01 Build

EE		DATE		POWER		DATE		INVENT TITLE PWR SW BOARD			
DRAWER											
DESIGN											
CHECK											
RESPONSIBLE											
SIZE=				VER:				SIZE	CODE	DOC NUMBER	REV
FILE NAME: XXXX-XXXXXX-XX								CustomCS	K-CS-1310A22219-ALG		A01
PIN		XXXXXXXXXXXXXX						SHEET	56	of	61



INVENTEC			
TITLE Aegis			
Power Switch			
SIZE B	CODE CS	DOC NUMBER K-CS-1310A22219-ALG	REV A01
SHEET	57	of	61

CHANGE by	BEN LEE	DATE	Friday, December 10, 2010

Aegis

Finger Print board

2010.12.10

A01 Build

Friday, December 10, 2010		
DATE	CHANGE NO.	REV

	EE	DATE	POWER	DATE	INVENTEC			
DRAWER					TITLE			
DESIGN								
CHECK					Finger Print board			
RESPONSIBLE								
SIZE=				VER:	SIZE	CODE	DOC NUMBER	REV
FILE NAME: XXXX-XXXXXX-XX					CustomCS		K-CS-1310A22499	A01
P/N	XXXXXXXXXXXX				SHEET	58	of	61

Aegis GP board

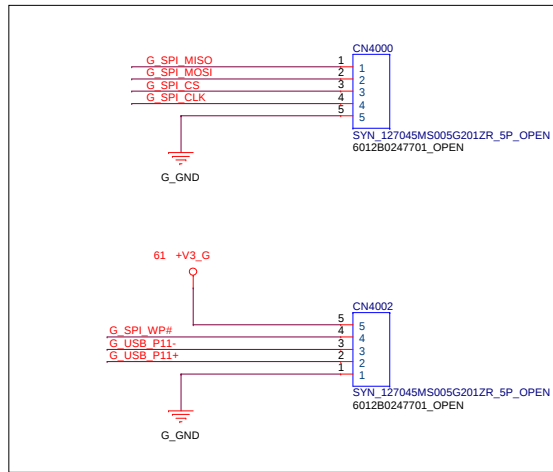
2010.12.10

A01 Build

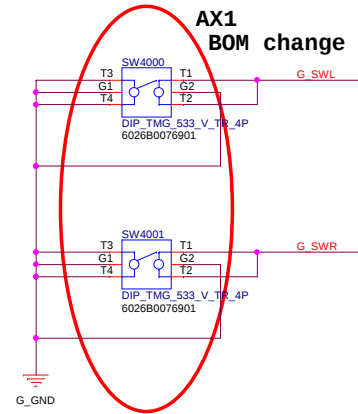
Friday, December 10, 2010		
DATE	CHANGE NO.	REV

	EE	DATE	POWER	DATE	INVENTEC			
DRAWER					TITLE			
DESIGN								
CHECK					GP Board			
RESPONSIBLE								
SIZE=				VER:	SIZE	CODE	DOC NUMBER	REV
FILE NAME: XXXX-XXXXXX-XX					CustomCS		K-CS-1310A22499	A01
P/N	XXXXXXXXXXXX				SHEET	60	of	61

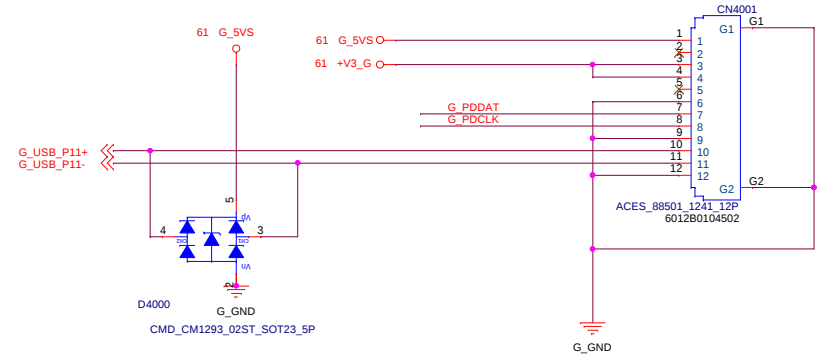
TO FP PIN HEADER



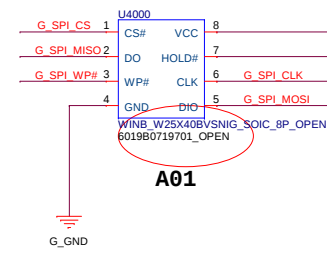
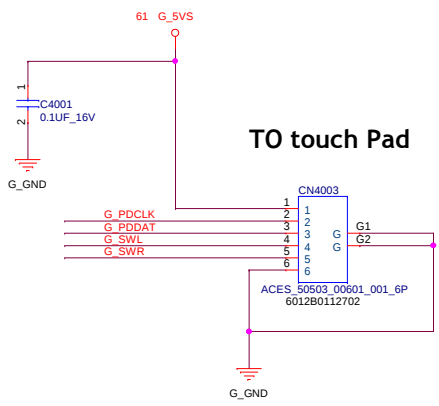
GP Button



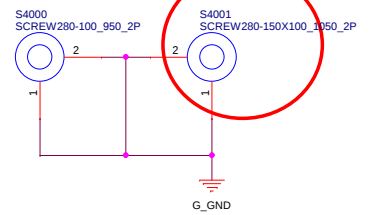
TO MB



TO touch Pad



AX2



INVENTEC

TITLE			
Aegis			
USB Board/GP			
SIZE	CODE	DOC NUMBER	REV
CustomCS		K-CS-1310A22499	A01