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EVEREST-M

WS BULID

2010.01.04

INVENTEC

TITLE			
EVEREST-M COVER PAGE			
SIZE	CODE	DOC.NUMBER	REV
C	CS	CS_1310AXXXXX-MTR	A01

CHANGE by Frank Hu DATE Tue Jan 04 11:08:28 2011

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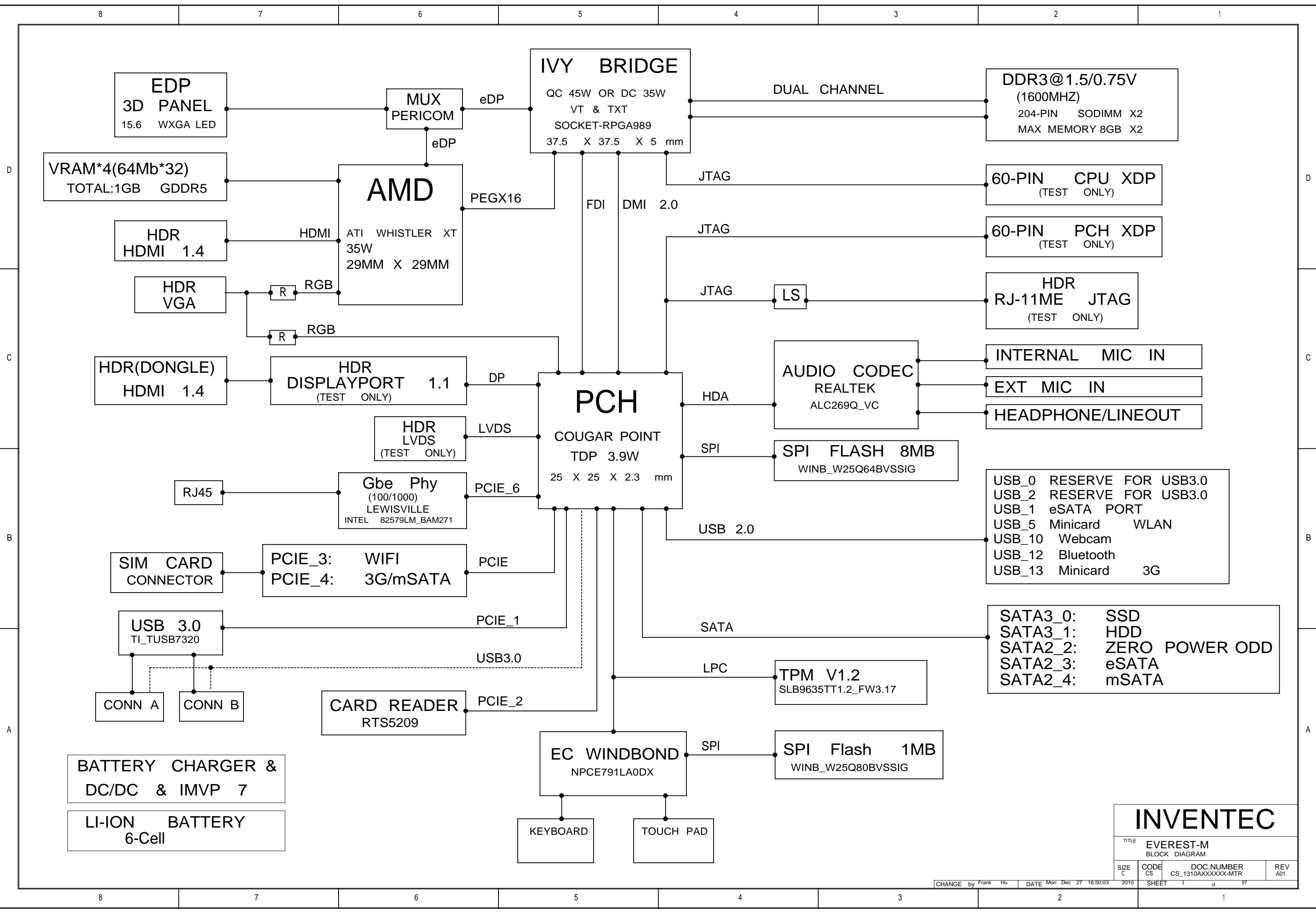
PAGE		PAGE		PAGE	
1.	COVER PAGE	28.	PCCH 1	55.	MINI1 WLAN/Debug Card
2.	INDEX	29.	PCCH 2	56.	MINI2 3G
3.	BLOCK DIAGRAM	30.	PCCH 3	57.	HALL SENSOR
4.	SMB DIAGRAM	31.	PCCH 4 AXG	58.	LED
5.	POWER SEQUENCE BLOCK	32.	PCCH 5 USB	59.	CLOCK GENERATOR
6.	POWER FLOW	33.	PCCH 6 MISC	60.	XDP
7.	PCB SCREW	34.	PCCH 7 POWER	61.	ME JTAG
8.	POWER CHARGER	35.	PCCH 8 POWER	62.	PICK BUTTON BOARD
9.	POWER BATTERY	36.	PCCH 9 GND	63.	TOUCH PAD SW BOARD
10.	POWER +3A/+5A	37.	EC	64.	POWER BUTTON BOARD
11.	POWER +V1.5/+V0.75S	38.	FAN & THERMAL	65.	CARDREADER & USB BOARD
12.	POWER VCCP/+V1.05 LAN_M	39.	LAN	66.	EMI
13.	POWER +V0.85S/+V1.8S	40.	RJ45 & TRANSFORMER	67.	GPU SW/POWER
14.	POWER VCORE	41.	AUDIO CODEC	68.	GPU-1
15.	POWER VCORE	42.	AUDIO AMP	69.	GPU-2
16.	POWER GPU NVVDD	43.	TPM	70.	GPU-3
17.	POWER +V3S/+V5S/+V1.5S	44.	LCM CONN	71.	GPU-4
18.	POWER SEQ	45.	CRT CONN	72.	GPU-5
19.	POWER SEQ	46.	HDMI CONN	73.	VRAM
20.	CPU 1	47.	DP CONN	74.	VRAM
21.	CPU 2	48.	eDP CONN	75.	VRAM
22.	CPU 3 DRAM	49.	DB CONN USB & CARDREADER	76.	VRAM
23.	CPU 4 POWER	50.	SATA HDD/SSD & ODD CONN		
24.	CPU 5 POWER	51.	E-SATA CONN		
25.	CPU 6 GND	52.	USB CONN		
26.	DDR3 DIMM0	53.	K/B & TP/B CONN		
27.	DDR3 DIMM1	54.	BLUETOOTH CONN		

INVENTEC

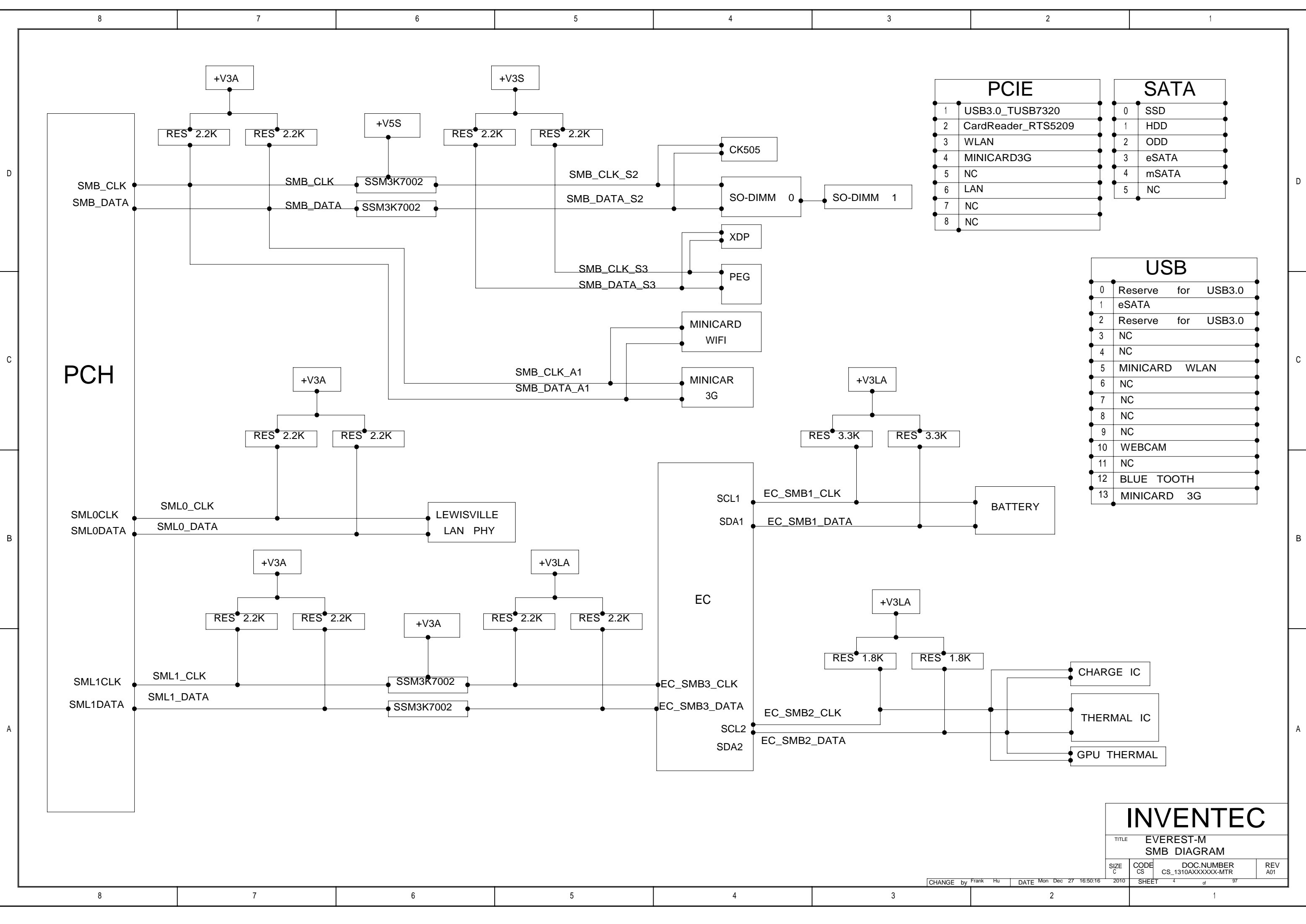
TITLE EVEREST-M
INDEX

SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01
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CHANGE by Frank Hu DATE Mon Dec 27 16:49:48 2010 SHEET 2 of 97



INVENTEC			
TITLE EVEREST-M BLOCK DIAGRAM			
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01



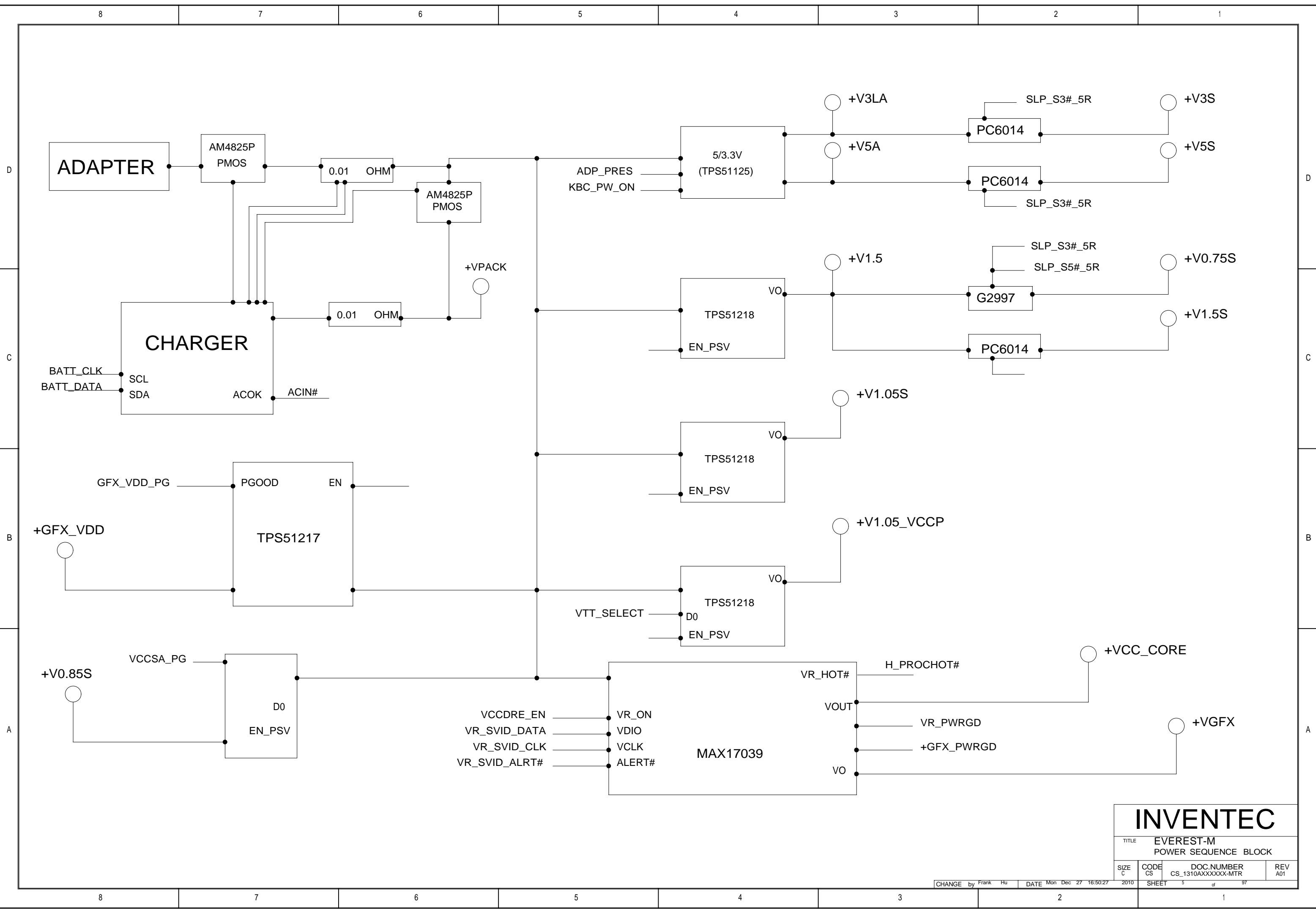
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1	USB3.0_TUSB7320
2	CardReader_RTS5209
3	WLAN
4	MINICARD3G
5	NC
6	LAN
7	NC
8	NC

SATA	
0	SSD
1	HDD
2	ODD
3	eSATA
4	mSATA
5	NC

USB	
0	Reserve for USB3.0
1	eSATA
2	Reserve for USB3.0
3	NC
4	NC
5	MINICARD WLAN
6	NC
7	NC
8	NC
9	NC
10	WEBCAM
11	NC
12	BLUE TOOTH
13	MINICARD 3G

INVENTEC			
TITLE EVEREST-M SMB DIAGRAM			
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01

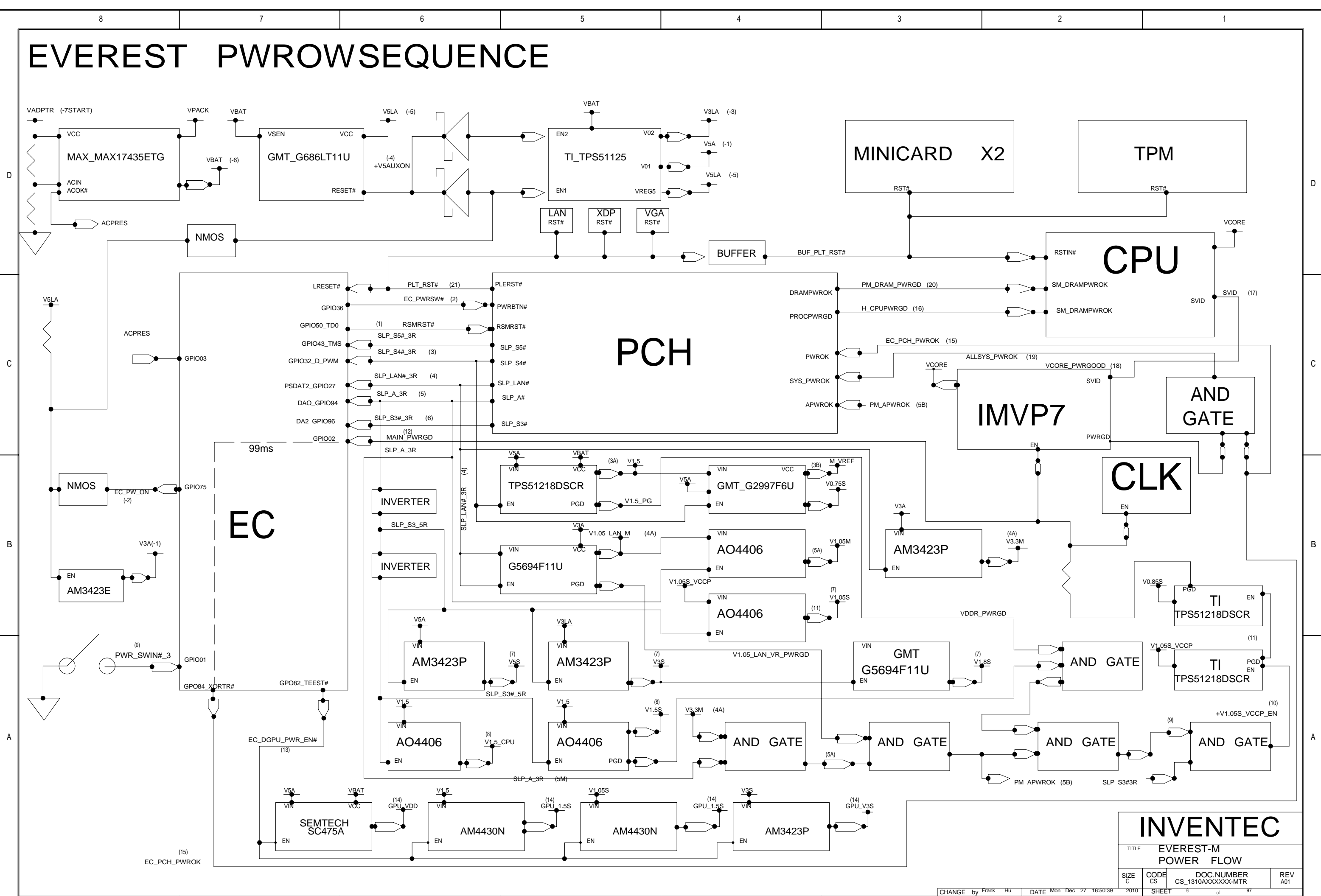
CHANGE by Frank Hu DATE Mon Dec 27 16:50:16 2010 SHEET 4 of 97



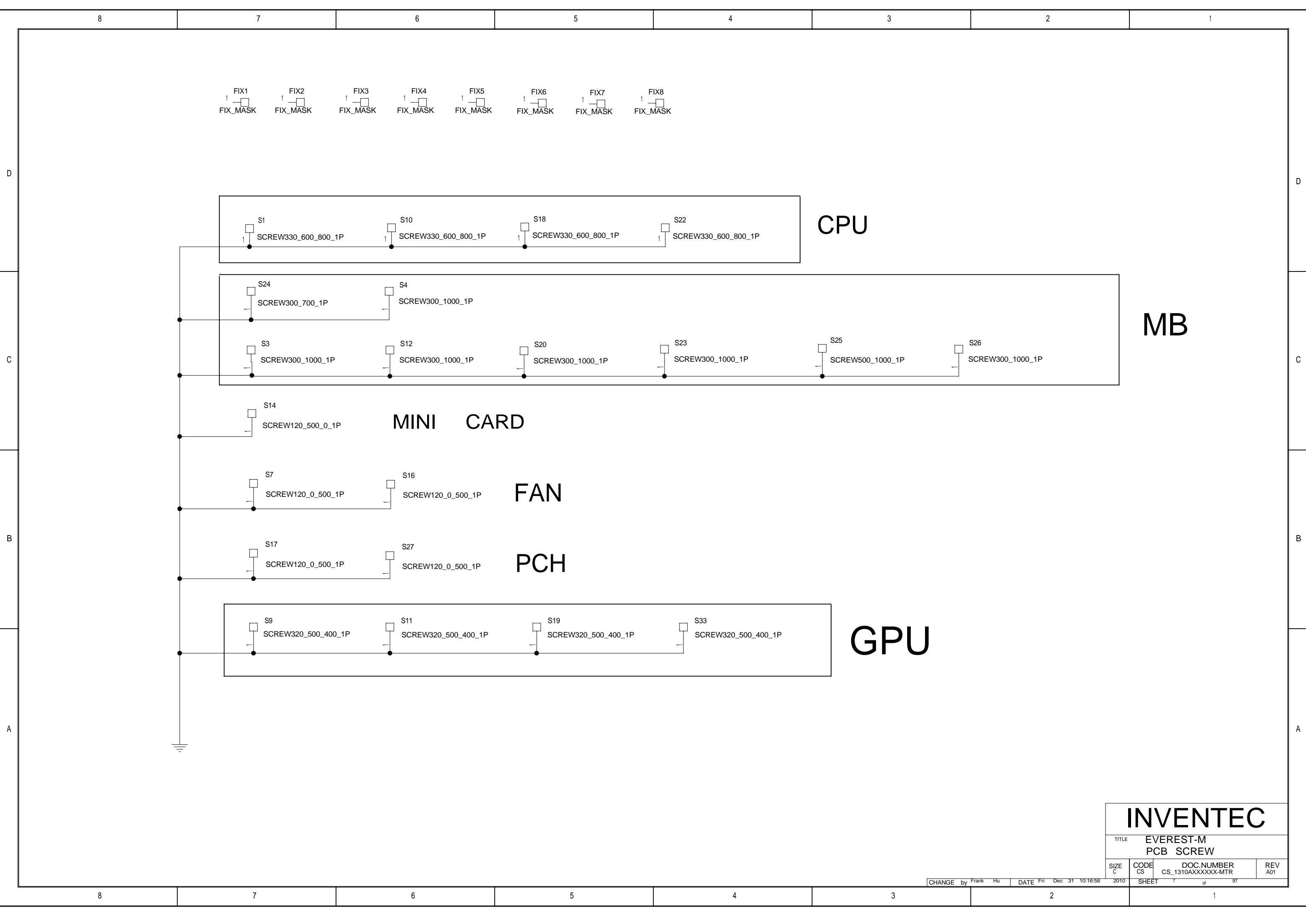
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TITLE EVEREST-M POWER SEQUENCE BLOCK			
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01

CHANGE by Frank Hu DATE Mon Dec 27 16:50:27 2010 SHEET 5 of 97

EVEREST PWROWSEQUENCE

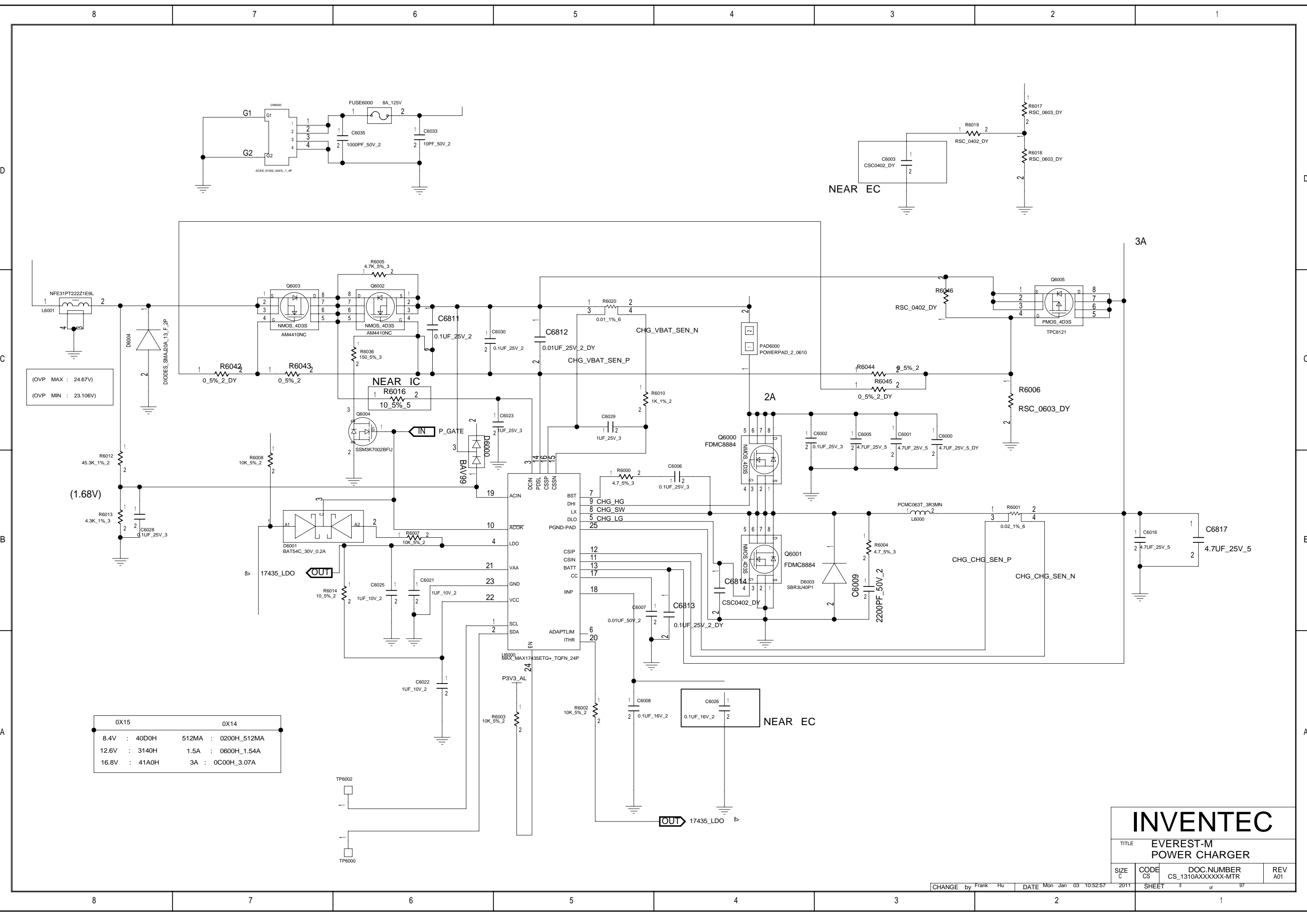


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TITLE EVEREST-M POWER FLOW			
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01
CHANGE by Frank Hu		DATE Mon Dec 27 16:50:39 2010	SHEET 6 of 97



INVENTEC			
TITLE EVEREST-M PCB SCREW			
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01

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(OVP MAX : 24.67V)
(OVP MIN : 23.106V)

(1.68V)

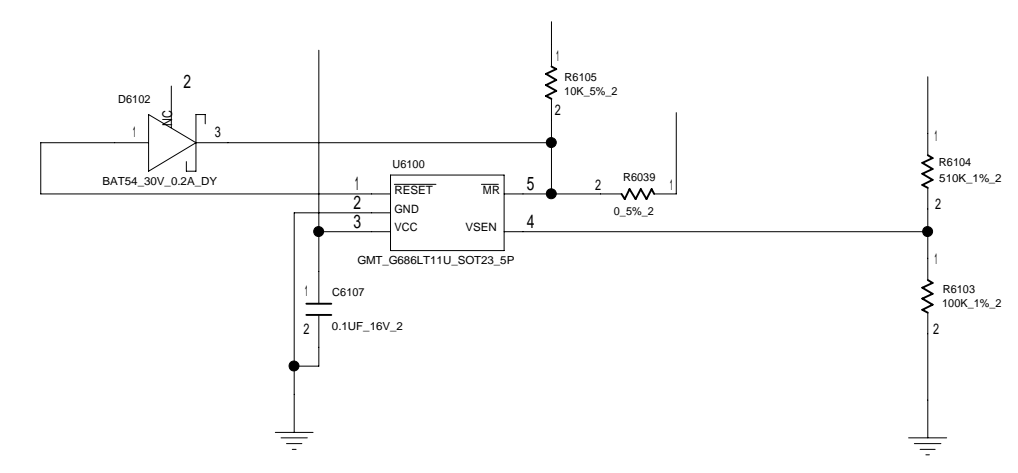
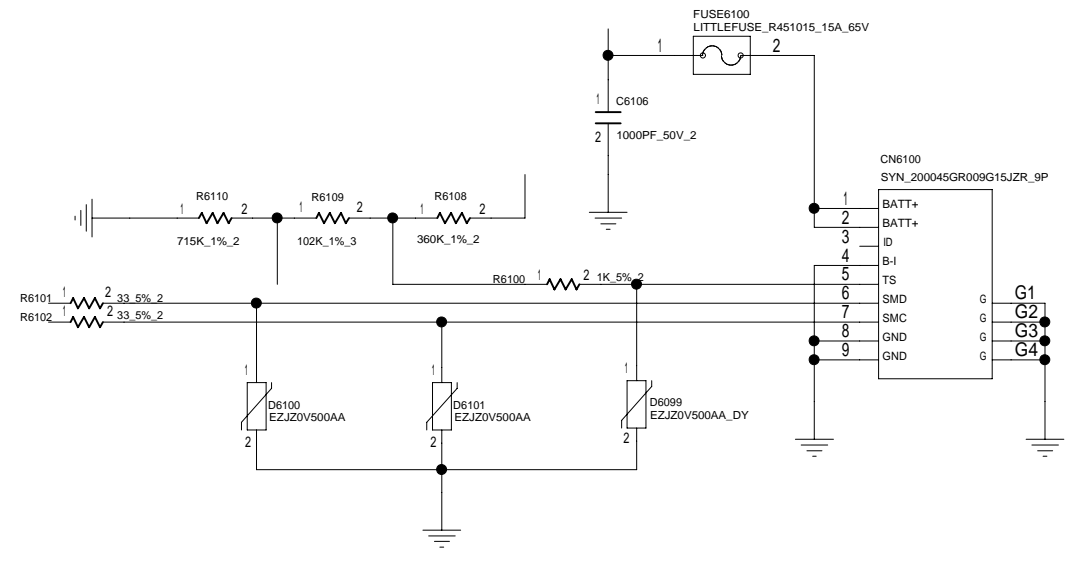
0X15	0X14
8.4V : 40D0H	512MA : 0200H_512MA
12.6V : 3140H	1.5A : 0600H_1.54A
16.8V : 41A0H	3A : 0C00H_3.07A

INVENTEC

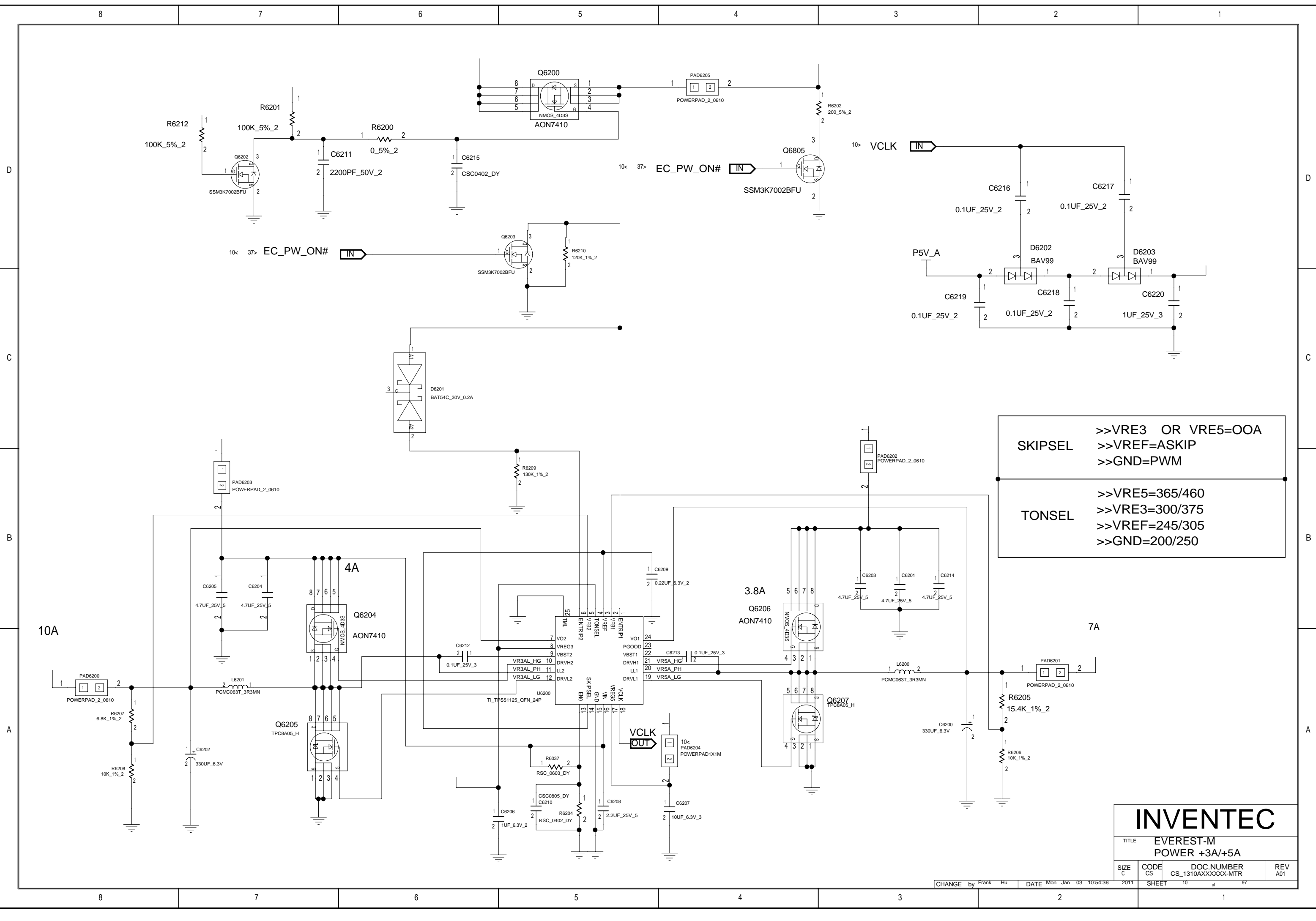
TITLE EVEREST-M
POWER CHARGER

SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01
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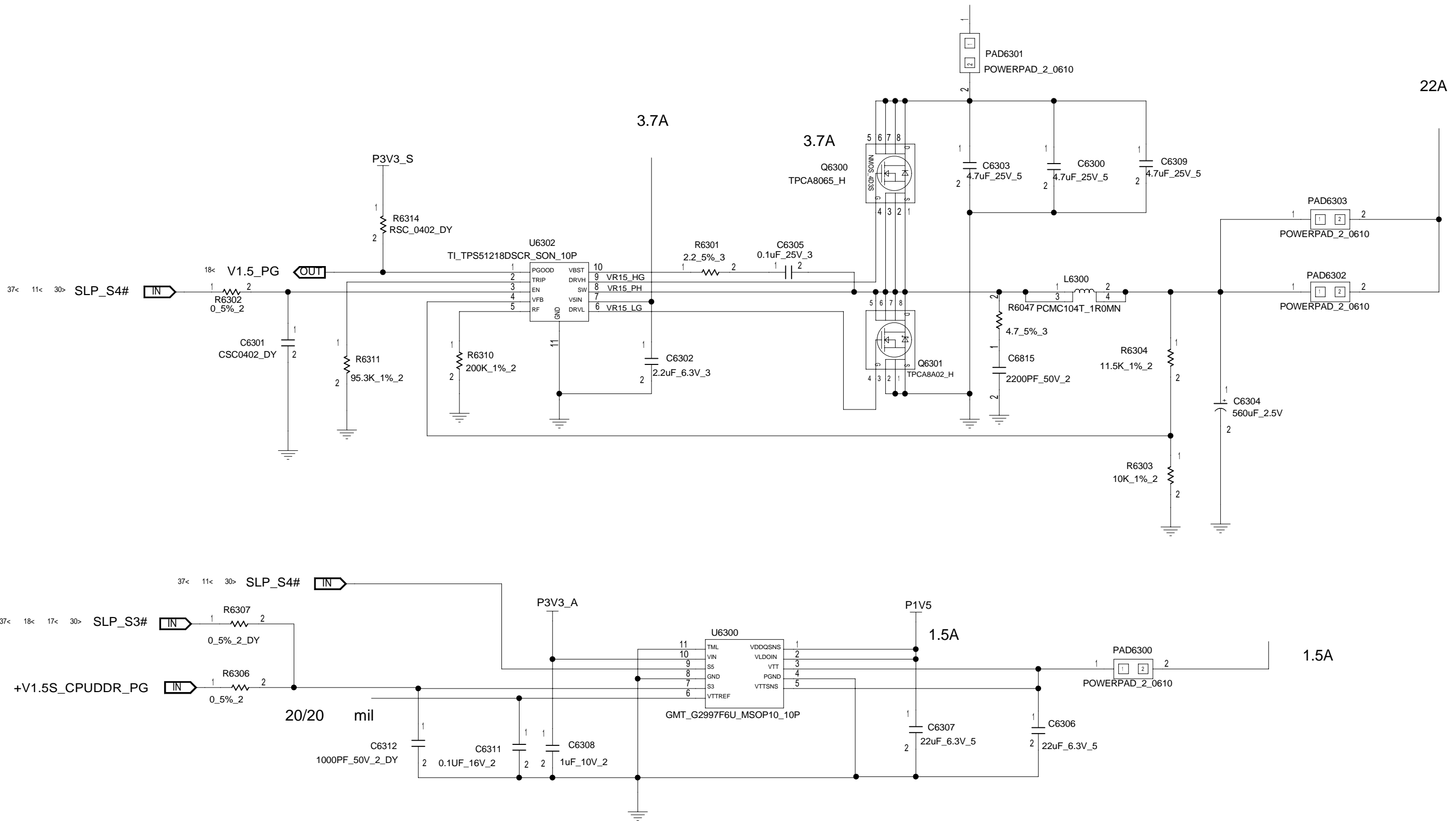
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TITLE EVEREST-M POWER BATTERY				
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01	



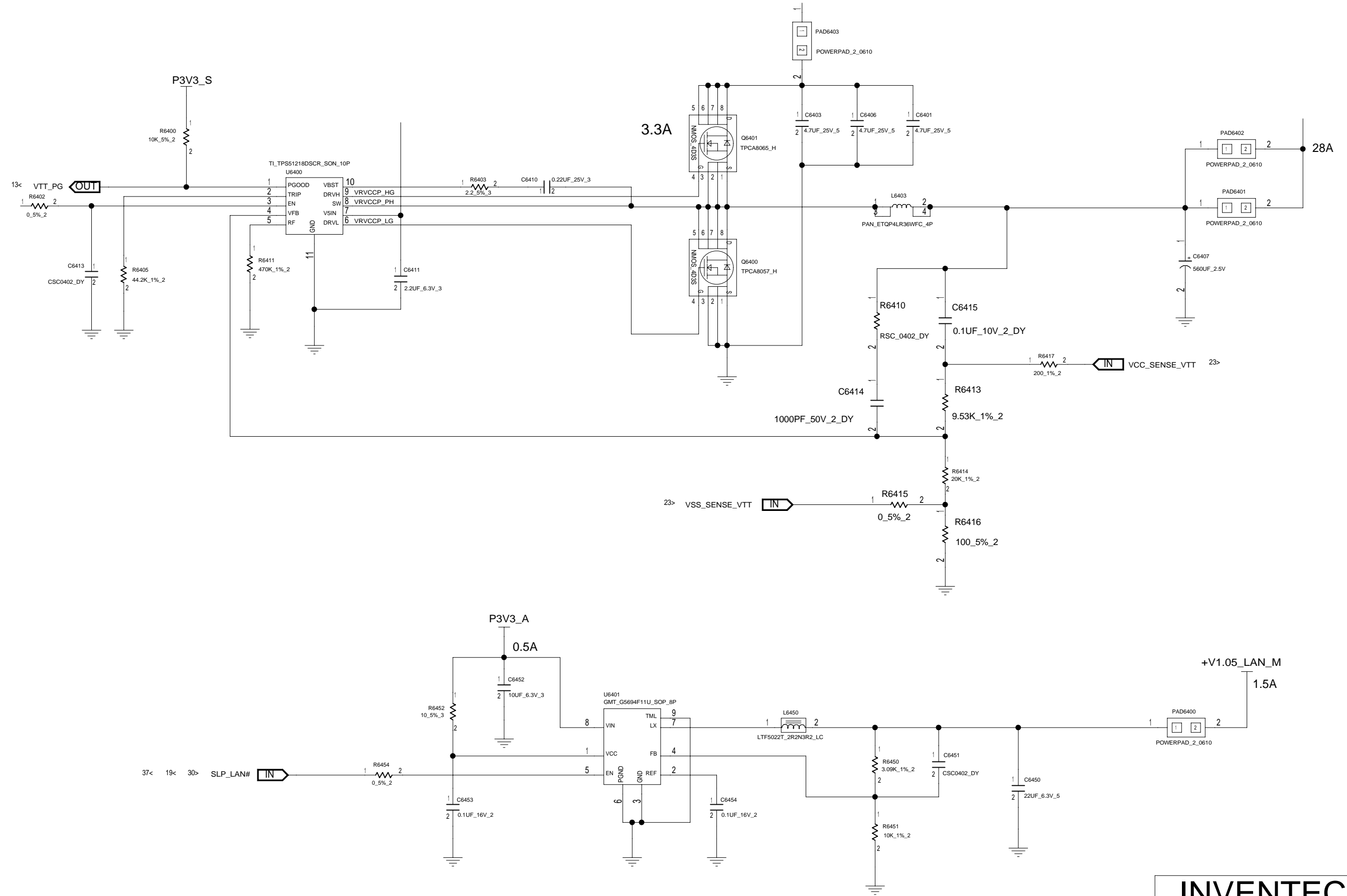
SKIPSEL >>VRE3 OR VRE5=OOA
 >>VREF=ASKIP
 >>GND=PWM

TONSEL >>VRE5=365/460
 >>VRE3=300/375
 >>VREF=245/305
 >>GND=200/250

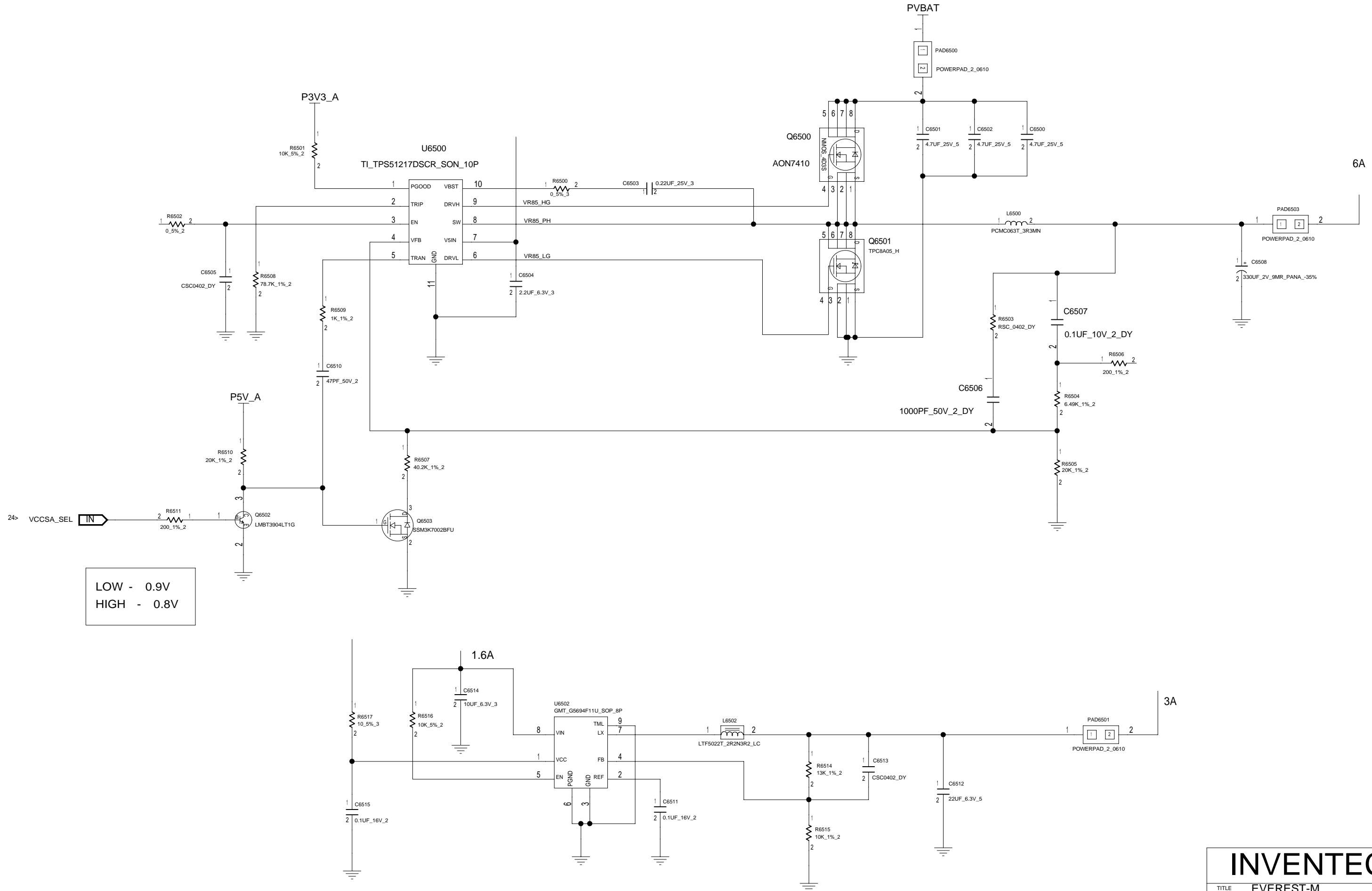
INVENTEC				
TITLE EVEREST-M POWER +3A/+5A				
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01	



INVENTEC				
TITLE EVEREST-M POWER +V1.5/+V0.75S				
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01	

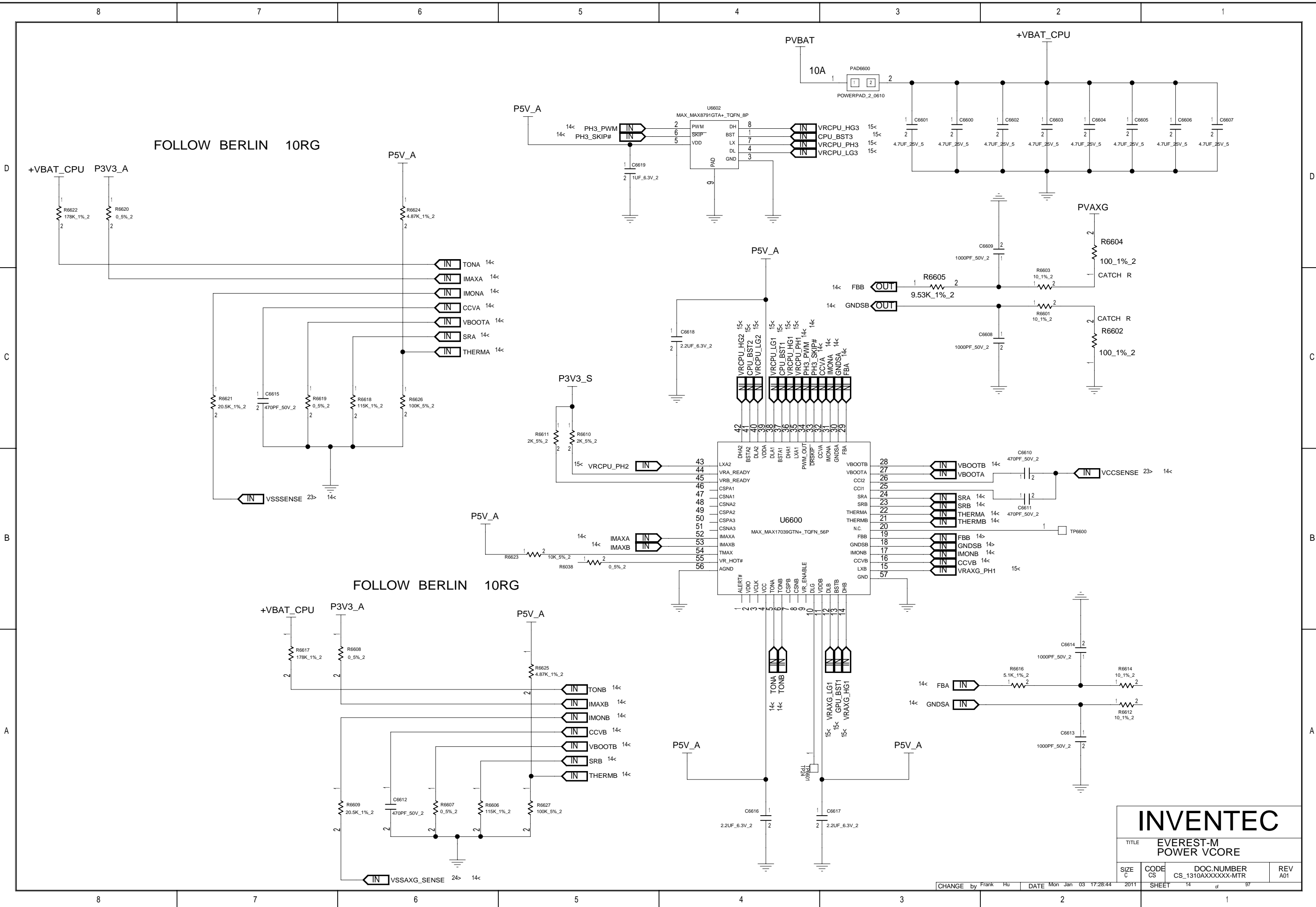


INVENTEC				
TITLE EVEREST-M POWER VCCP/+V1.05_LAN_M				
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01	
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LOW - 0.9V
HIGH - 0.8V

INVENTEC			
TITLE EVEREST-M POWER +V0.85S/+V1.8S			
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01
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INVENTEC				
TITLE EVEREST-M POWER VCORE				
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01	

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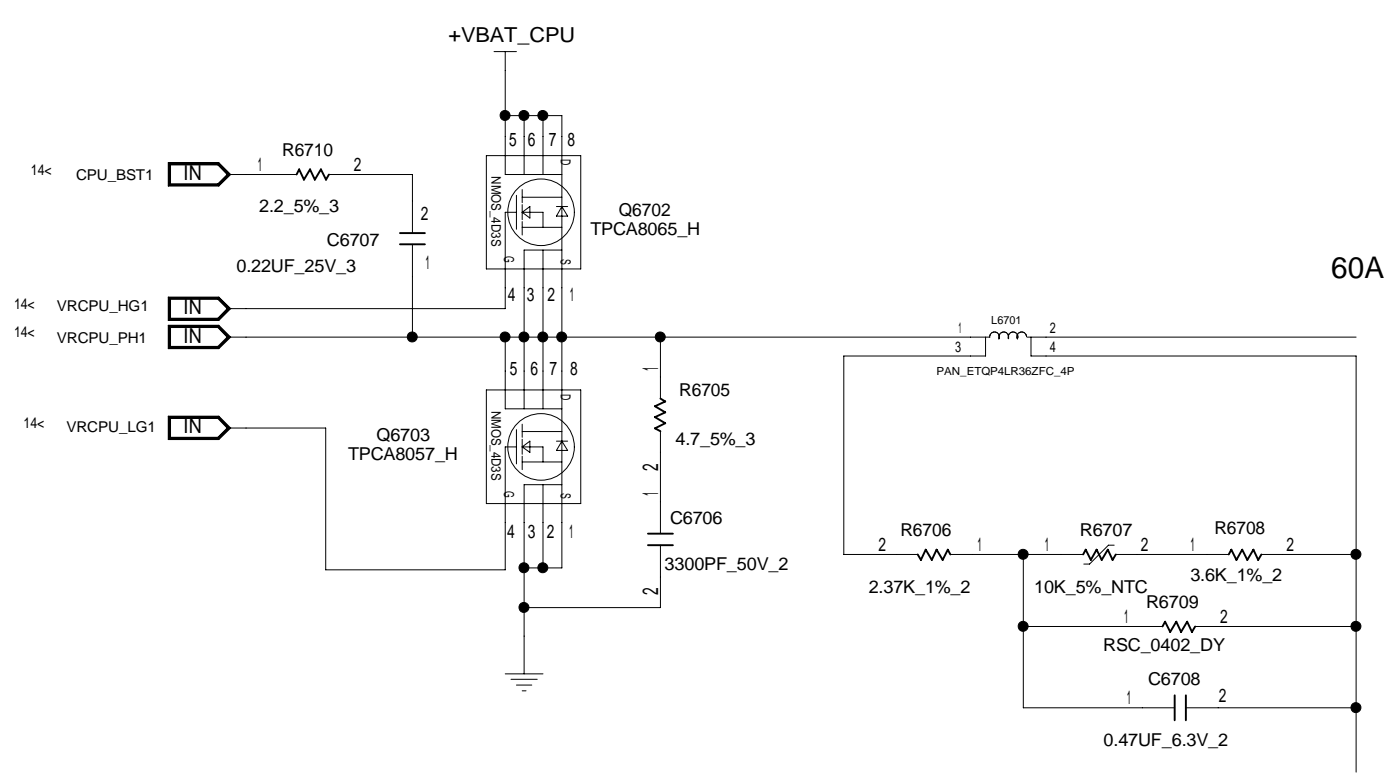
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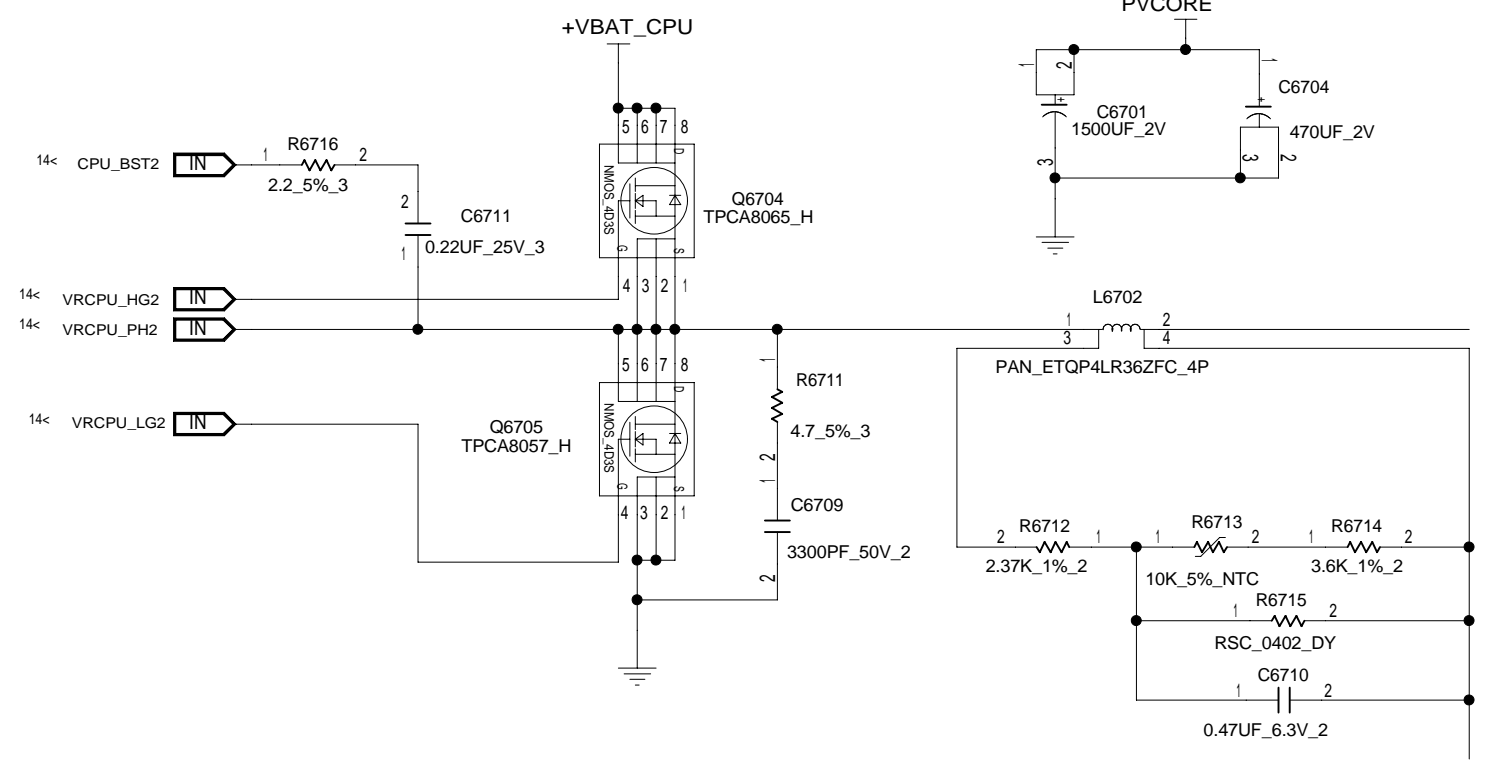
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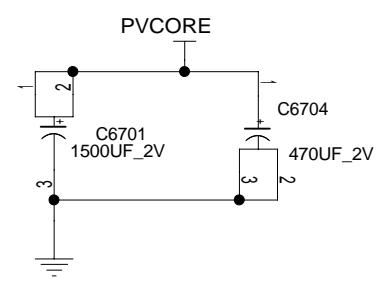
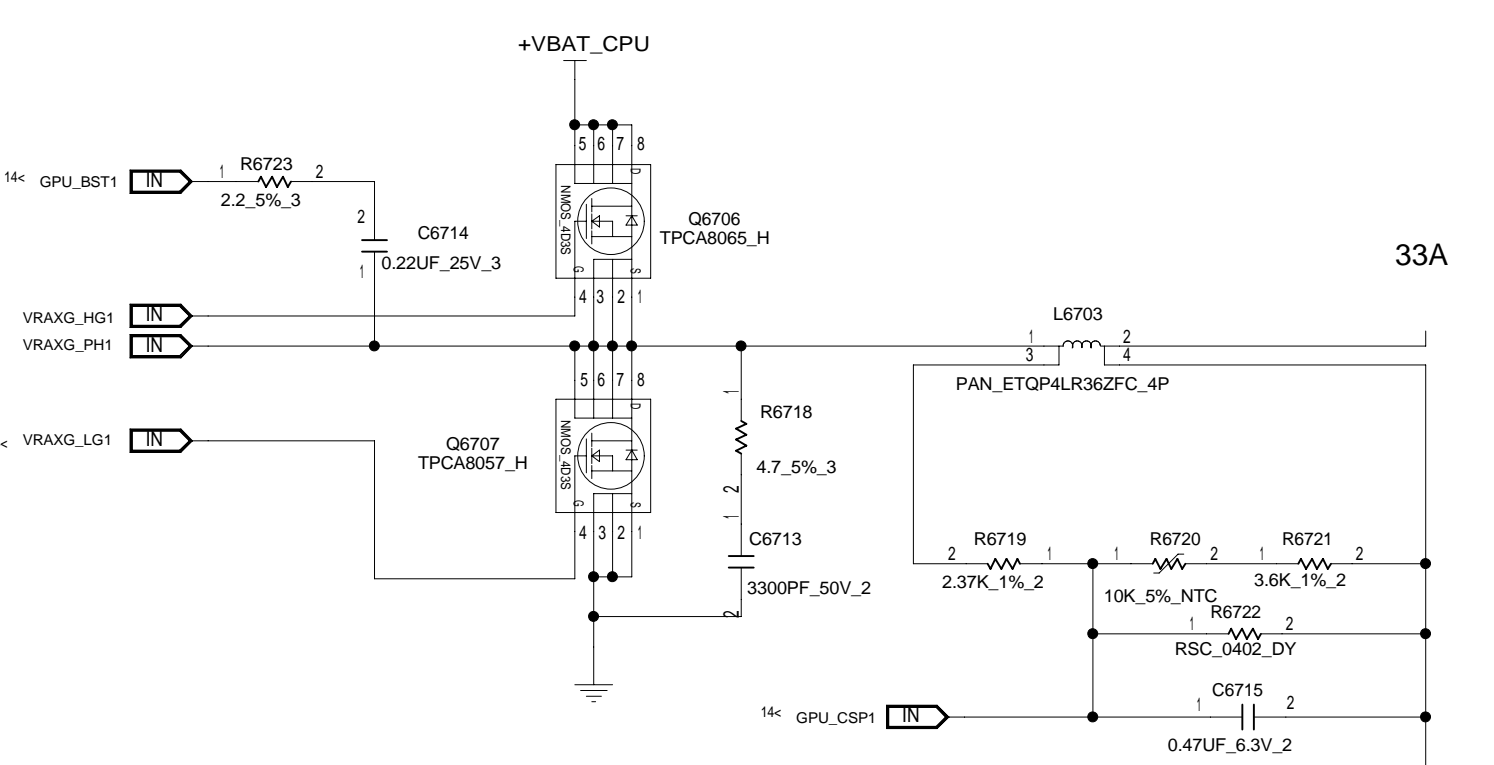
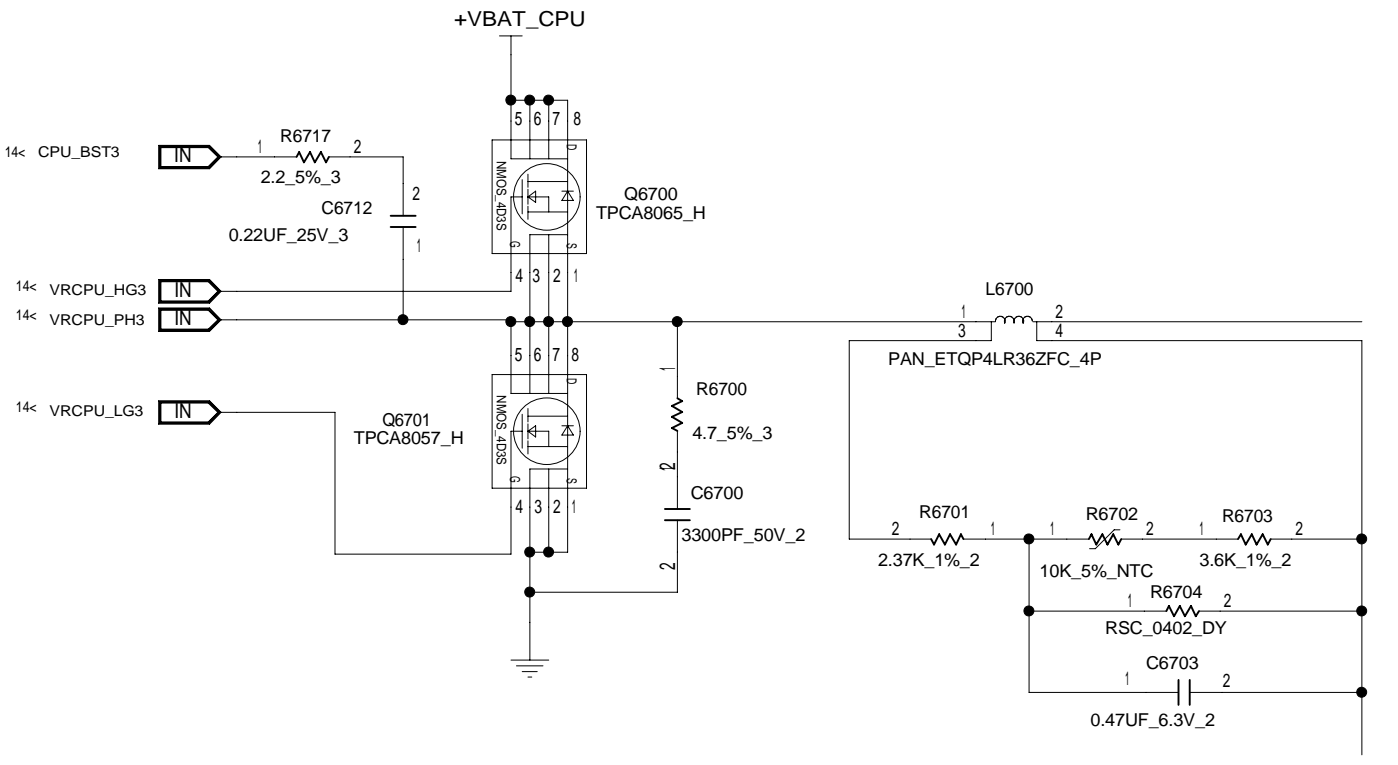
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60A



33A

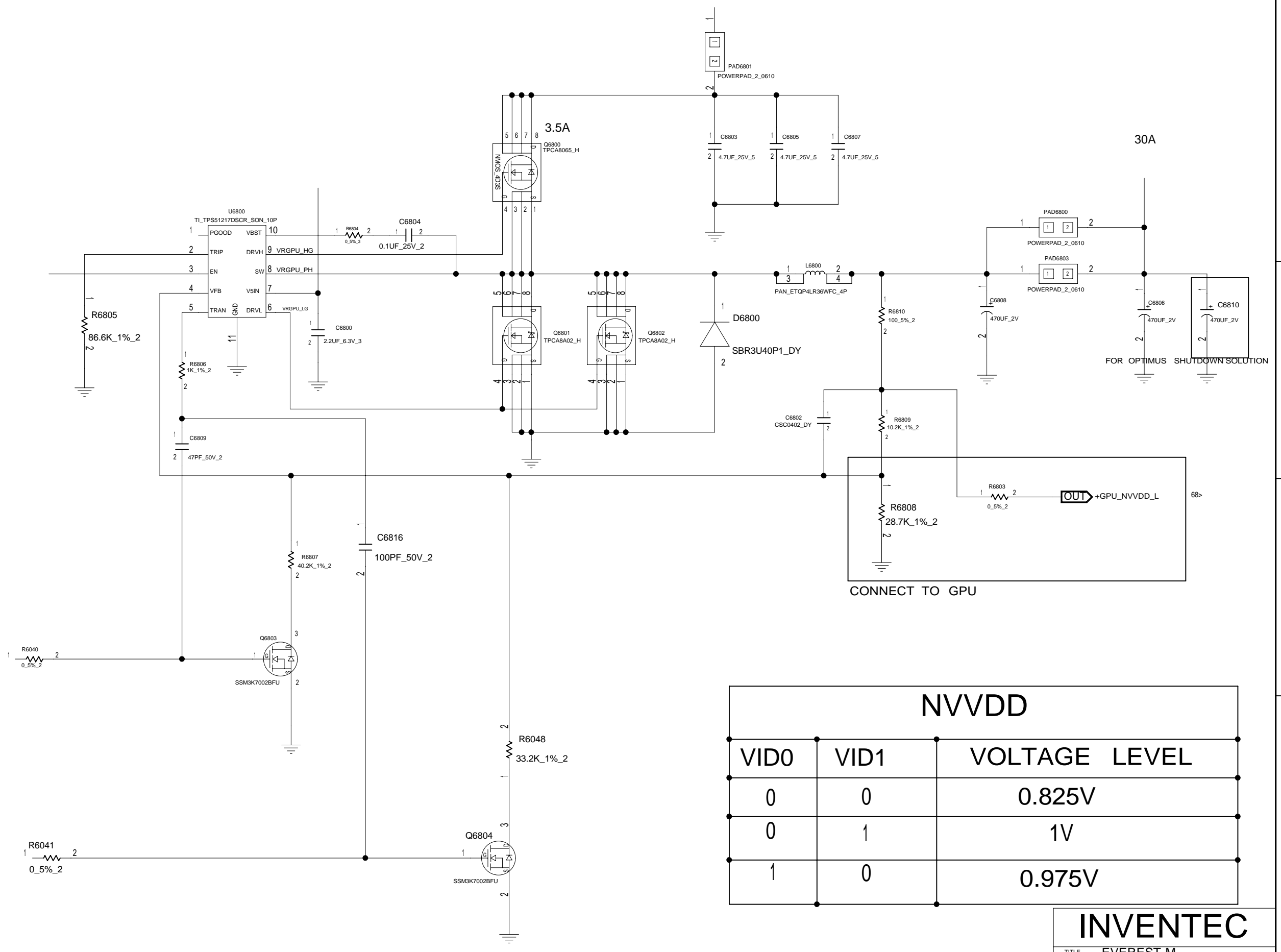


INVENTEC

TITLE EVEREST-M
POWER VCORE

SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01
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NVVDD		
VID0	VID1	VOLTAGE LEVEL
0	0	0.825V
0	1	1V
1	0	0.975V

INVENTEC

TITLE EVEREST-M
POWER GPU NVVDD

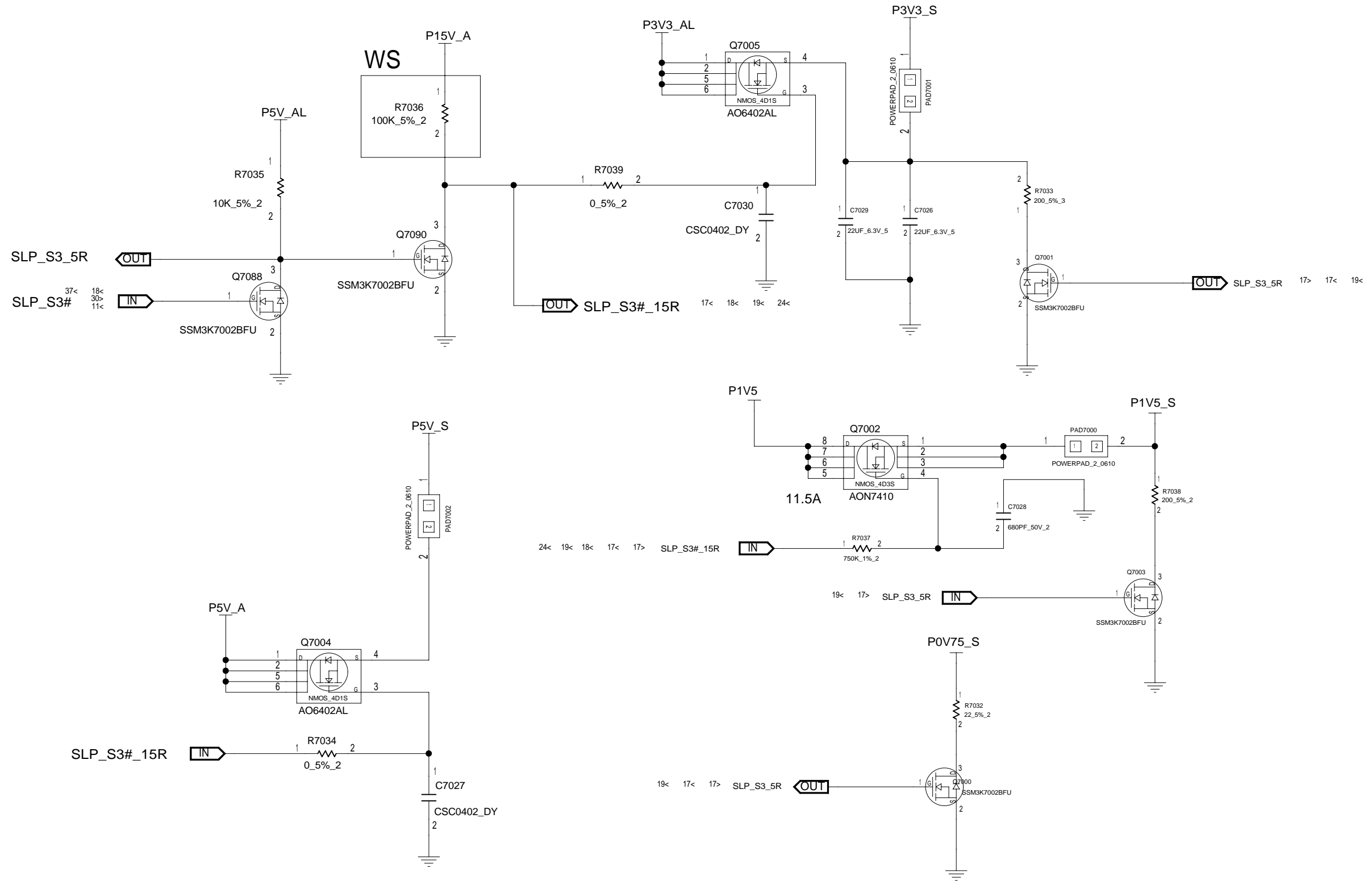
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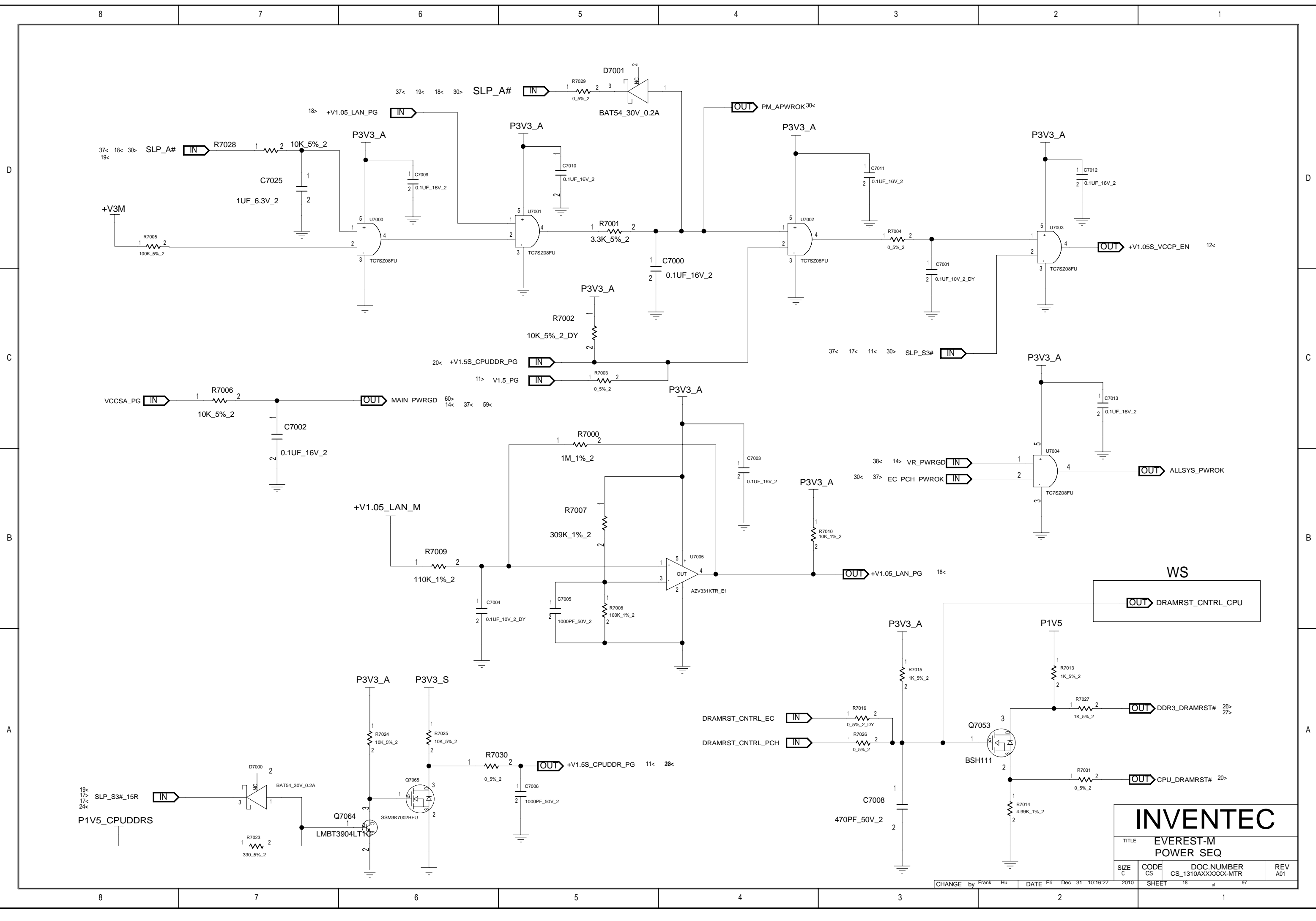
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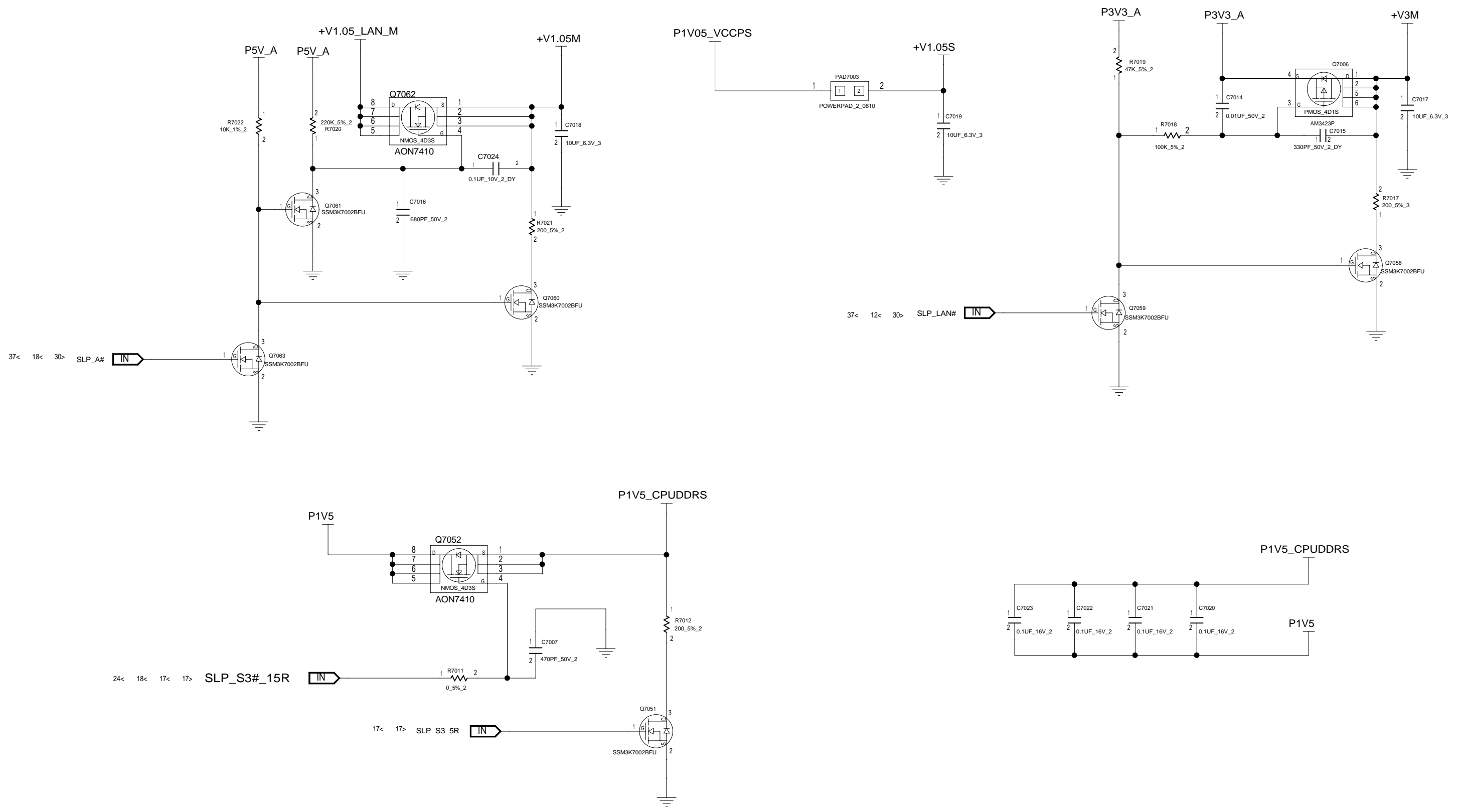


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TITLE EVEREST-M POWER +V3S/+V5S/+V1.5S				
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01	
CHANGE by Frank Hu		DATE Fri Dec 31 10:16:26	2010	SHEET 17 of 97



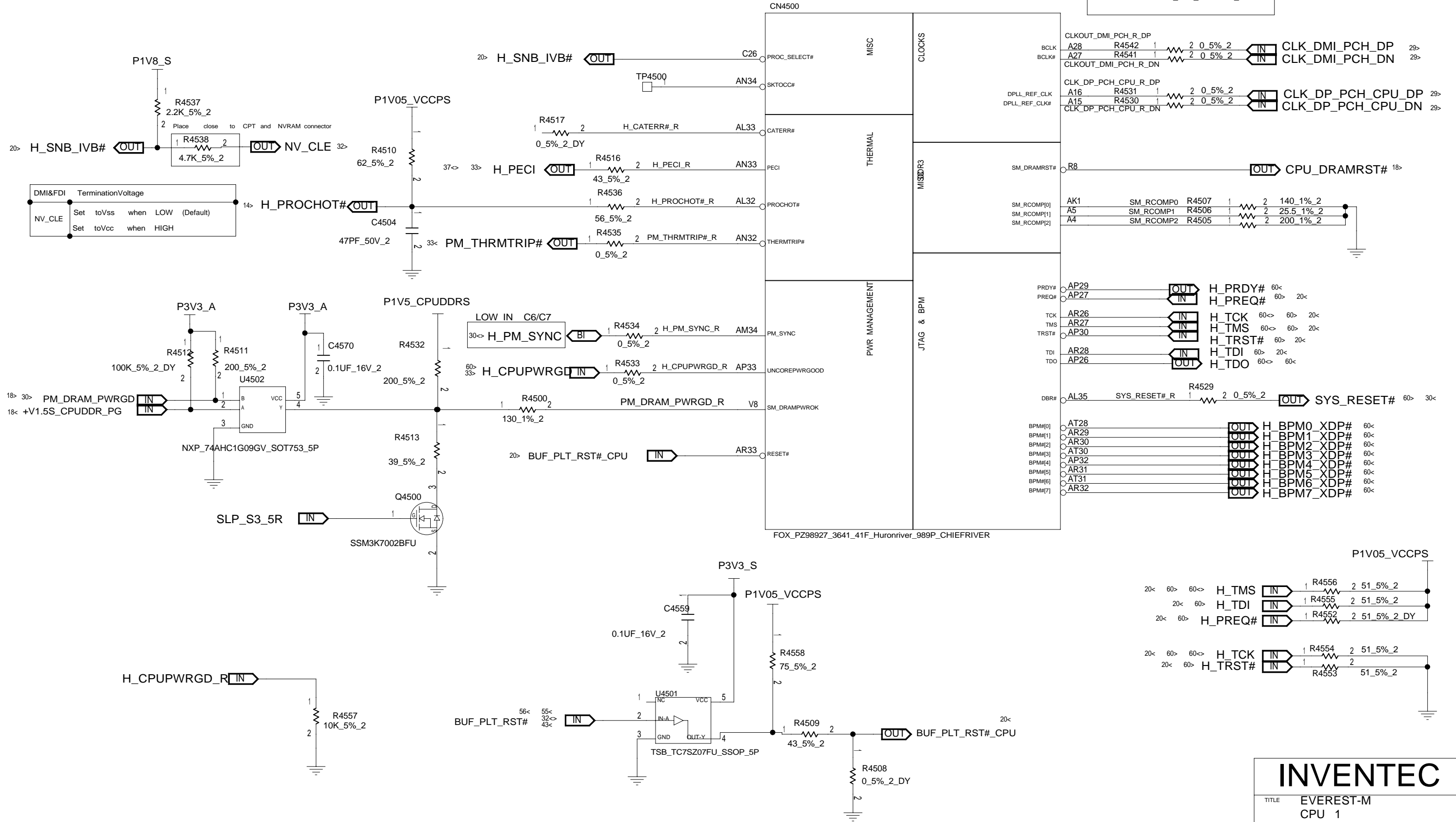
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TITLE EVEREST-M POWER SEQ			
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01

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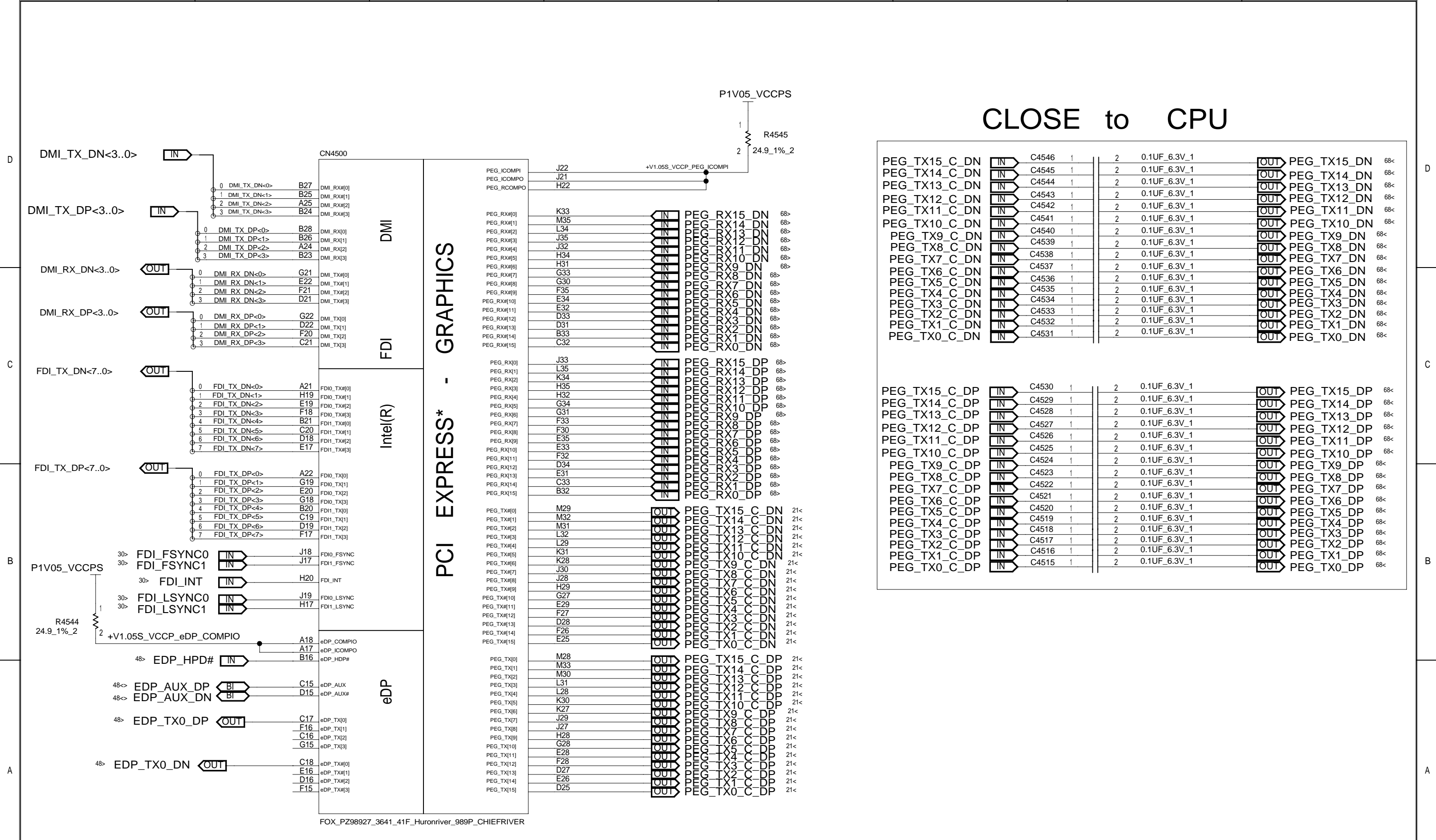
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SIZE C	CODE CS	DOC. NUMBER CS_1310AXXXXX-MTR	REV A01	
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REMOVE CLKOUT_DMI_CLKGEN_DP
 CLKOUT_DMI_CLKGEN_DN WS



INVENTEC
 TITLE EVEREST-M
 CPU 1
 SIZE C CODE CS DOC.NUMBER CS_1310AXXXXX-MTR REV A01
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CLOSE to CPU

PEG_TX15_C_DN	IN	C4546	1	2	0.1UF_6.3V_1	OUT	PEG_TX15_DN	68<
PEG_TX14_C_DN	IN	C4545	1	2	0.1UF_6.3V_1	OUT	PEG_TX14_DN	68<
PEG_TX13_C_DN	IN	C4544	1	2	0.1UF_6.3V_1	OUT	PEG_TX13_DN	68<
PEG_TX12_C_DN	IN	C4543	1	2	0.1UF_6.3V_1	OUT	PEG_TX12_DN	68<
PEG_TX11_C_DN	IN	C4542	1	2	0.1UF_6.3V_1	OUT	PEG_TX11_DN	68<
PEG_TX10_C_DN	IN	C4541	1	2	0.1UF_6.3V_1	OUT	PEG_TX10_DN	68<
PEG_TX9_C_DN	IN	C4540	1	2	0.1UF_6.3V_1	OUT	PEG_TX9_DN	68<
PEG_TX8_C_DN	IN	C4539	1	2	0.1UF_6.3V_1	OUT	PEG_TX8_DN	68<
PEG_TX7_C_DN	IN	C4538	1	2	0.1UF_6.3V_1	OUT	PEG_TX7_DN	68<
PEG_TX6_C_DN	IN	C4537	1	2	0.1UF_6.3V_1	OUT	PEG_TX6_DN	68<
PEG_TX5_C_DN	IN	C4536	1	2	0.1UF_6.3V_1	OUT	PEG_TX5_DN	68<
PEG_TX4_C_DN	IN	C4535	1	2	0.1UF_6.3V_1	OUT	PEG_TX4_DN	68<
PEG_TX3_C_DN	IN	C4534	1	2	0.1UF_6.3V_1	OUT	PEG_TX3_DN	68<
PEG_TX2_C_DN	IN	C4533	1	2	0.1UF_6.3V_1	OUT	PEG_TX2_DN	68<
PEG_TX1_C_DN	IN	C4532	1	2	0.1UF_6.3V_1	OUT	PEG_TX1_DN	68<
PEG_TX0_C_DN	IN	C4531	1	2	0.1UF_6.3V_1	OUT	PEG_TX0_DN	68<

PEG_TX15_C_DP	IN	C4530	1	2	0.1UF_6.3V_1	OUT	PEG_TX15_DP	68<
PEG_TX14_C_DP	IN	C4529	1	2	0.1UF_6.3V_1	OUT	PEG_TX14_DP	68<
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PEG_TX12_C_DP	IN	C4527	1	2	0.1UF_6.3V_1	OUT	PEG_TX12_DP	68<
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PEG_TX9_C_DP	IN	C4524	1	2	0.1UF_6.3V_1	OUT	PEG_TX9_DP	68<
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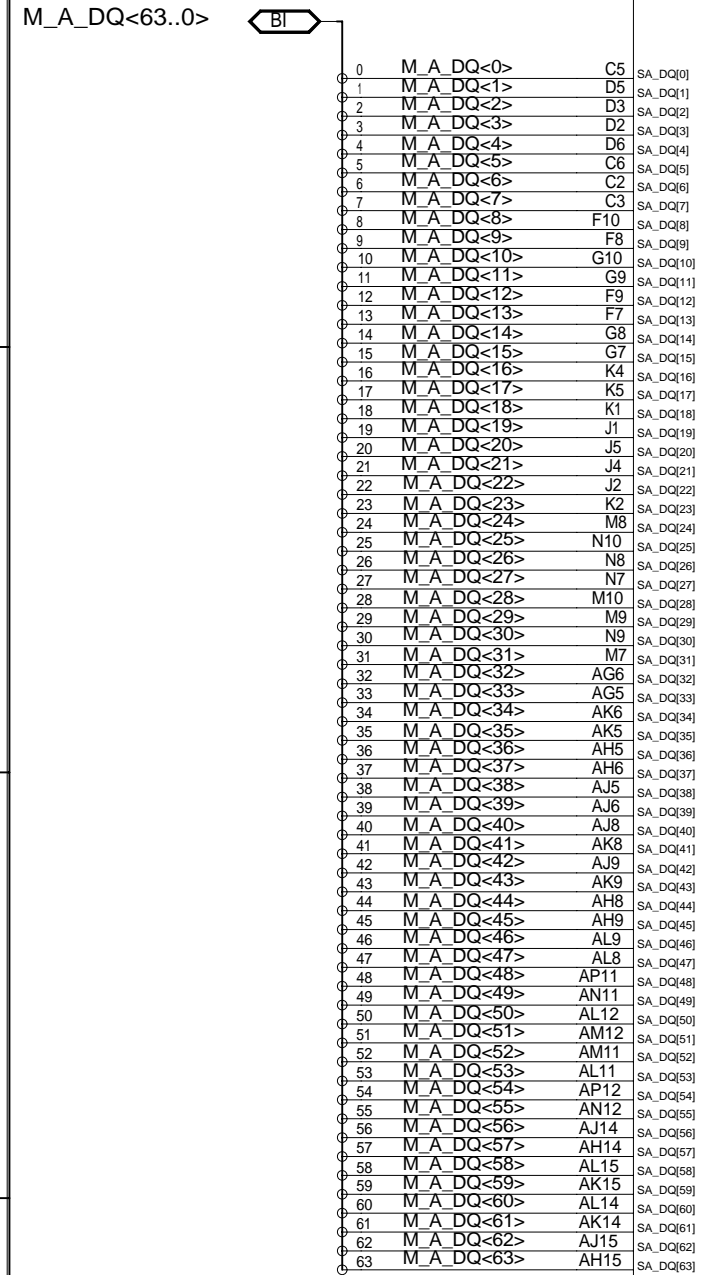
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TITLE EVEREST-M CPU 2				
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01	

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SOCKET,CPU,989P,TIN,3.0MM,STR,SMD,TR

CN4500

DDR SYSTEM MEMORY A



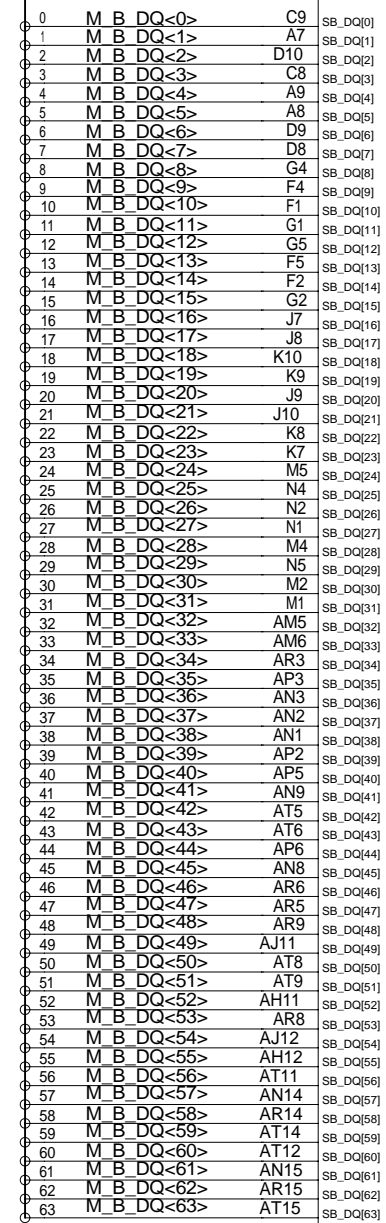
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BI

CN4500

DDR SYSTEM MEMORY B



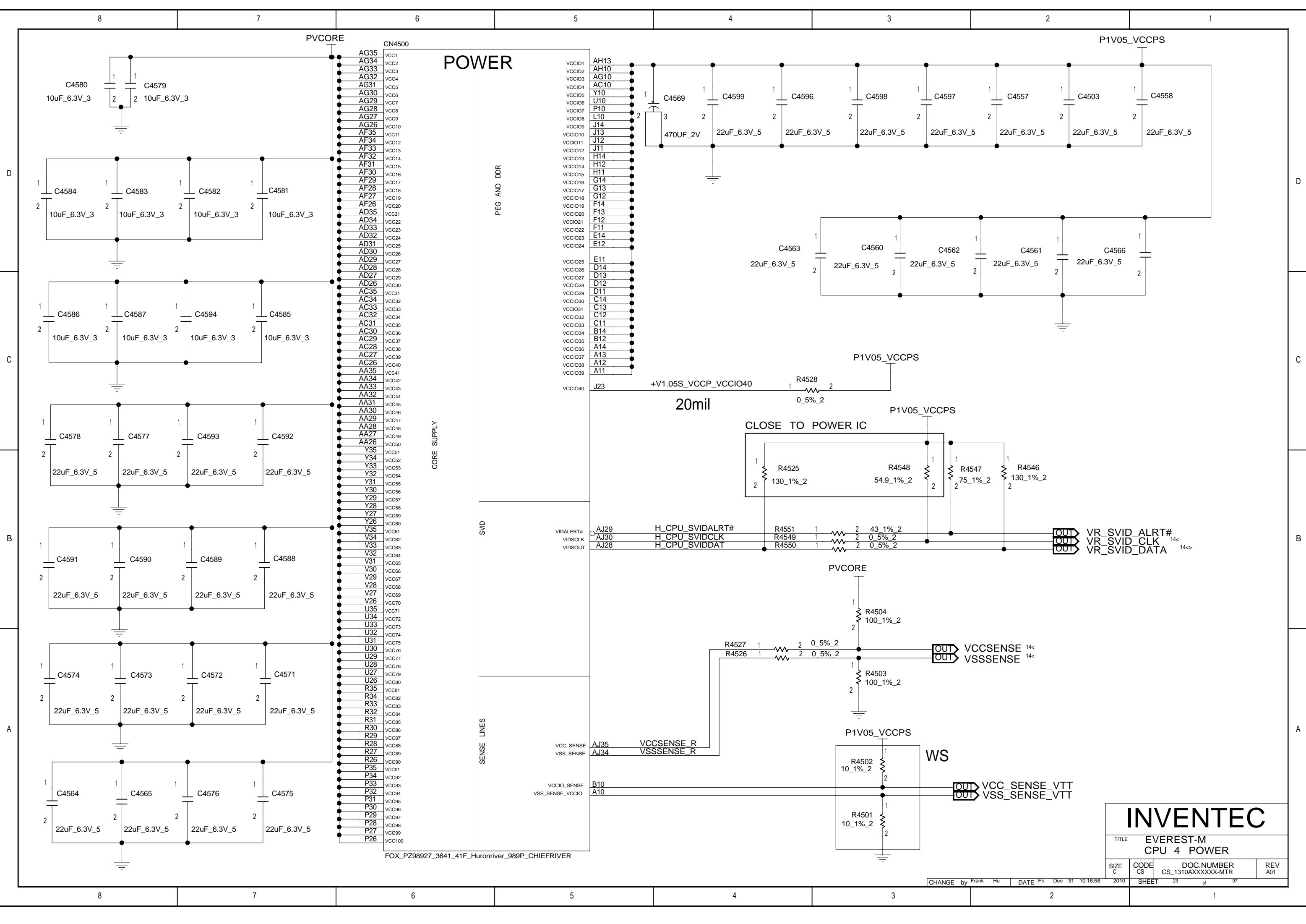
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INVENTEC

TITLE EVEREST-M
CPU 3 DRAM

SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01
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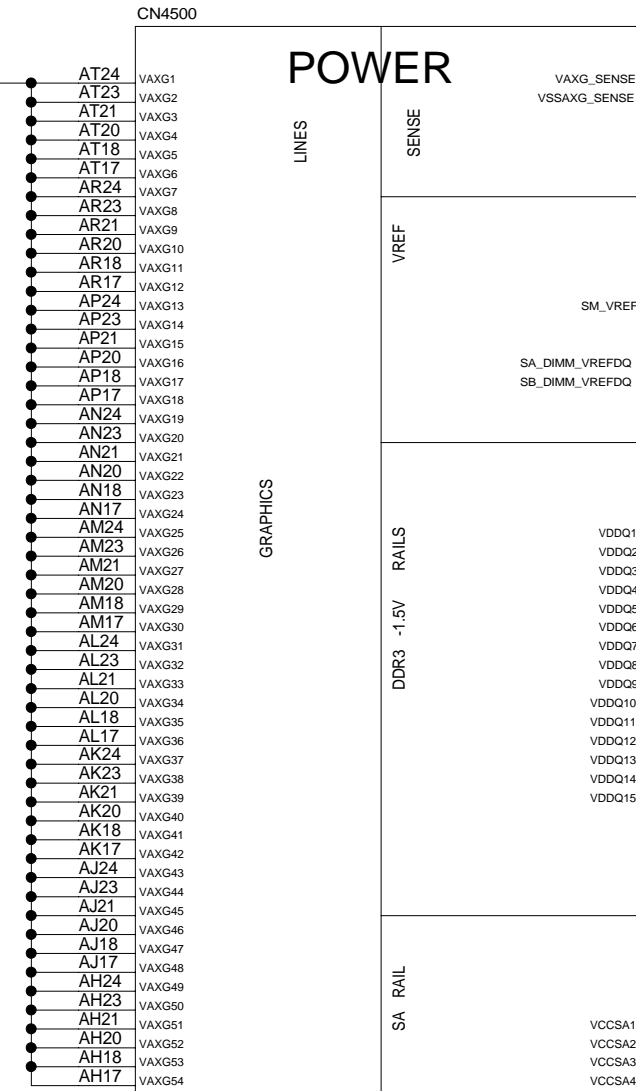
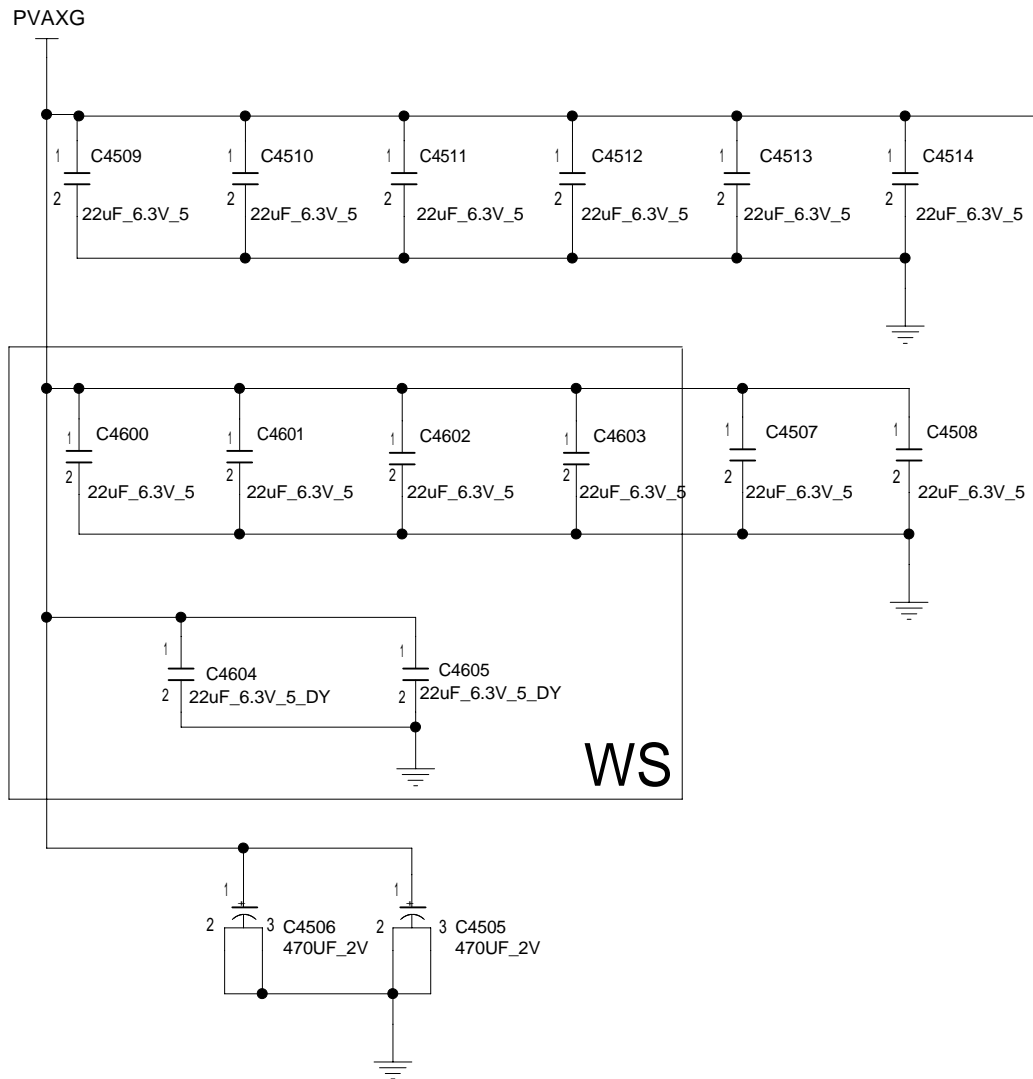
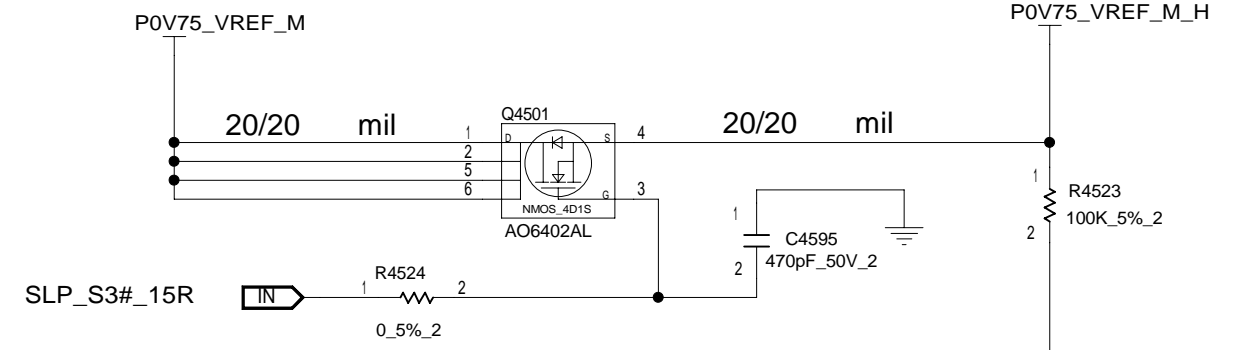


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 - VCC5
 - VCC6
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 - VCC11
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 - VCC99
 - VCC100

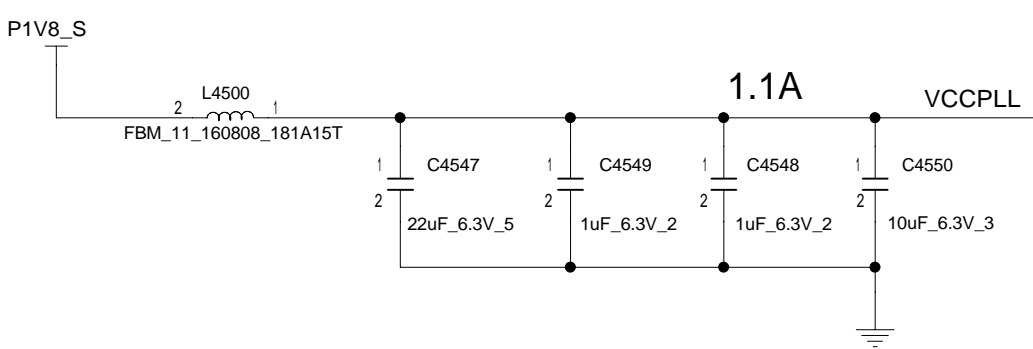
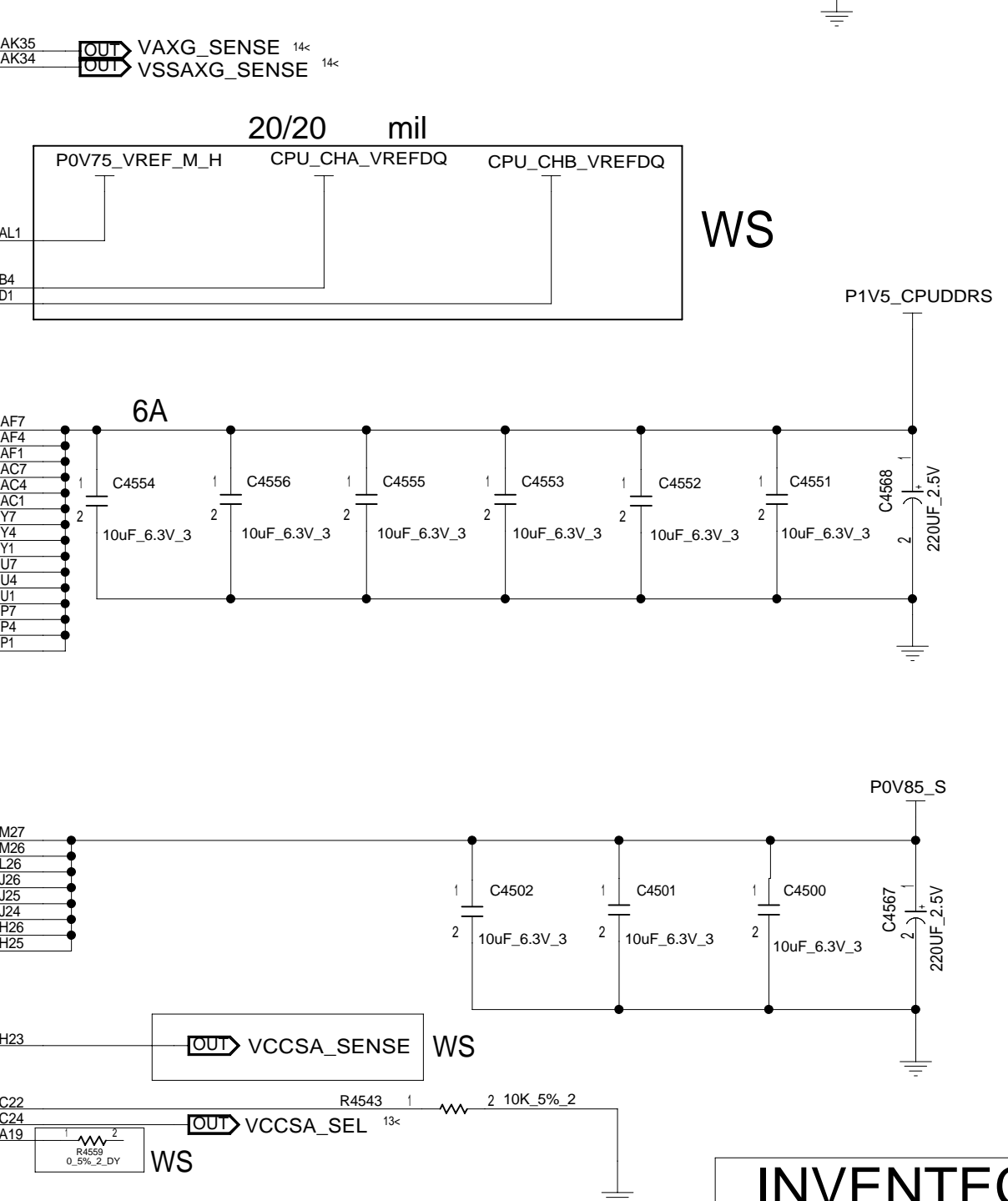
- POWER**
- AH13
 - AH10
 - AG10
 - AC10
 - Y10
 - U10
 - P10
 - L10
 - J14
 - J13
 - J12
 - J11
 - H14
 - H12
 - H11
 - G14
 - G13
 - G12
 - F14
 - F13
 - F12
 - F11
 - E14
 - E12
 - E11
 - D14
 - D13
 - D12
 - D11
 - C14
 - C13
 - C12
 - C11
 - B14
 - B12
 - A14
 - A13
 - A12
 - A11
- PEG AND DDR**
- VCCIO1
 - VCCIO2
 - VCCIO3
 - VCCIO4
 - VCCIO5
 - VCCIO6
 - VCCIO7
 - VCCIO8
 - VCCIO9
 - VCCIO10
 - VCCIO11
 - VCCIO12
 - VCCIO13
 - VCCIO14
 - VCCIO15
 - VCCIO16
 - VCCIO17
 - VCCIO18
 - VCCIO19
 - VCCIO20
 - VCCIO21
 - VCCIO22
 - VCCIO23
 - VCCIO24
 - VCCIO25
 - VCCIO26
 - VCCIO27
 - VCCIO28
 - VCCIO29
 - VCCIO30
 - VCCIO31
 - VCCIO32
 - VCCIO33
 - VCCIO34
 - VCCIO35
 - VCCIO36
 - VCCIO37
 - VCCIO38
 - VCCIO39
 - VCCIO40
- CORE SUPPLY**
- VCC1
 - VCC2
 - VCC3
 - VCC4
 - VCC5
 - VCC6
 - VCC7
 - VCC8
 - VCC9
 - VCC10
 - VCC11
 - VCC12
 - VCC13
 - VCC14
 - VCC15
 - VCC16
 - VCC17
 - VCC18
 - VCC19
 - VCC20
 - VCC21
 - VCC22
 - VCC23
 - VCC24
 - VCC25
 - VCC26
 - VCC27
 - VCC28
 - VCC29
 - VCC30
 - VCC31
 - VCC32
 - VCC33
 - VCC34
 - VCC35
 - VCC36
 - VCC37
 - VCC38
 - VCC39
 - VCC40
 - VCC41
 - VCC42
 - VCC43
 - VCC44
 - VCC45
 - VCC46
 - VCC47
 - VCC48
 - VCC49
 - VCC50
 - VCC51
 - VCC52
 - VCC53
 - VCC54
 - VCC55
 - VCC56
 - VCC57
 - VCC58
 - VCC59
 - VCC60
 - VCC61
 - VCC62
 - VCC63
 - VCC64
 - VCC65
 - VCC66
 - VCC67
 - VCC68
 - VCC69
 - VCC70
 - VCC71
 - VCC72
 - VCC73
 - VCC74
 - VCC75
 - VCC76
 - VCC77
 - VCC78
 - VCC79
 - VCC80
 - VCC81
 - VCC82
 - VCC83
 - VCC84
 - VCC85
 - VCC86
 - VCC87
 - VCC88
 - VCC89
 - VCC90
 - VCC91
 - VCC92
 - VCC93
 - VCC94
 - VCC95
 - VCC96
 - VCC97
 - VCC98
 - VCC99
 - VCC100

INVENTEC				
TITLE EVEREST-M CPU 4 POWER				
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01	
CHANGE by Frank Hu		DATE Fri Dec 31 10:16:58	2010	SHEET 23 of 97

Function	xxVccSA_Select[1] [[CPU PIN# C24 VID0 of VR]]	xxVccSA_Select[0] [[CPU PIN# C22 VID1 of VR]]	VCCSA VR Vout
SNB HIGH	0	0	0.90V
IVB HIGH	0	1	0.725V
SNB LOW	1	0	0.80V
IVB LOW	1	1	0.675V

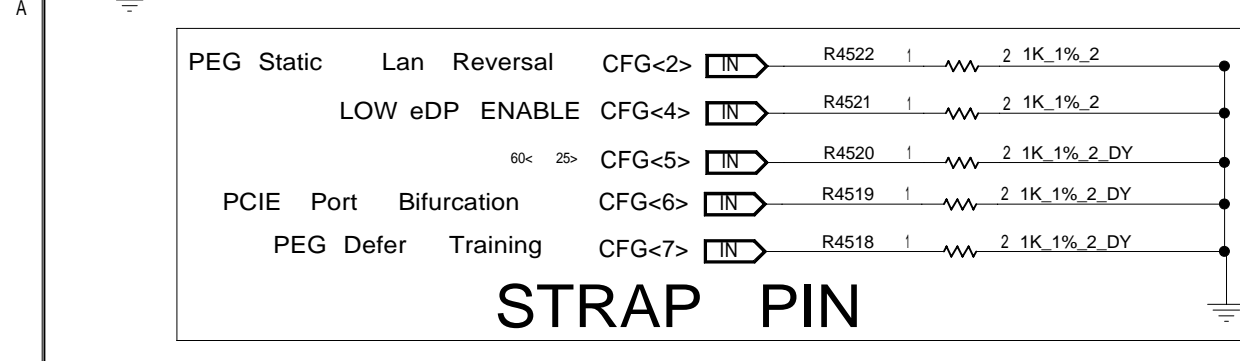
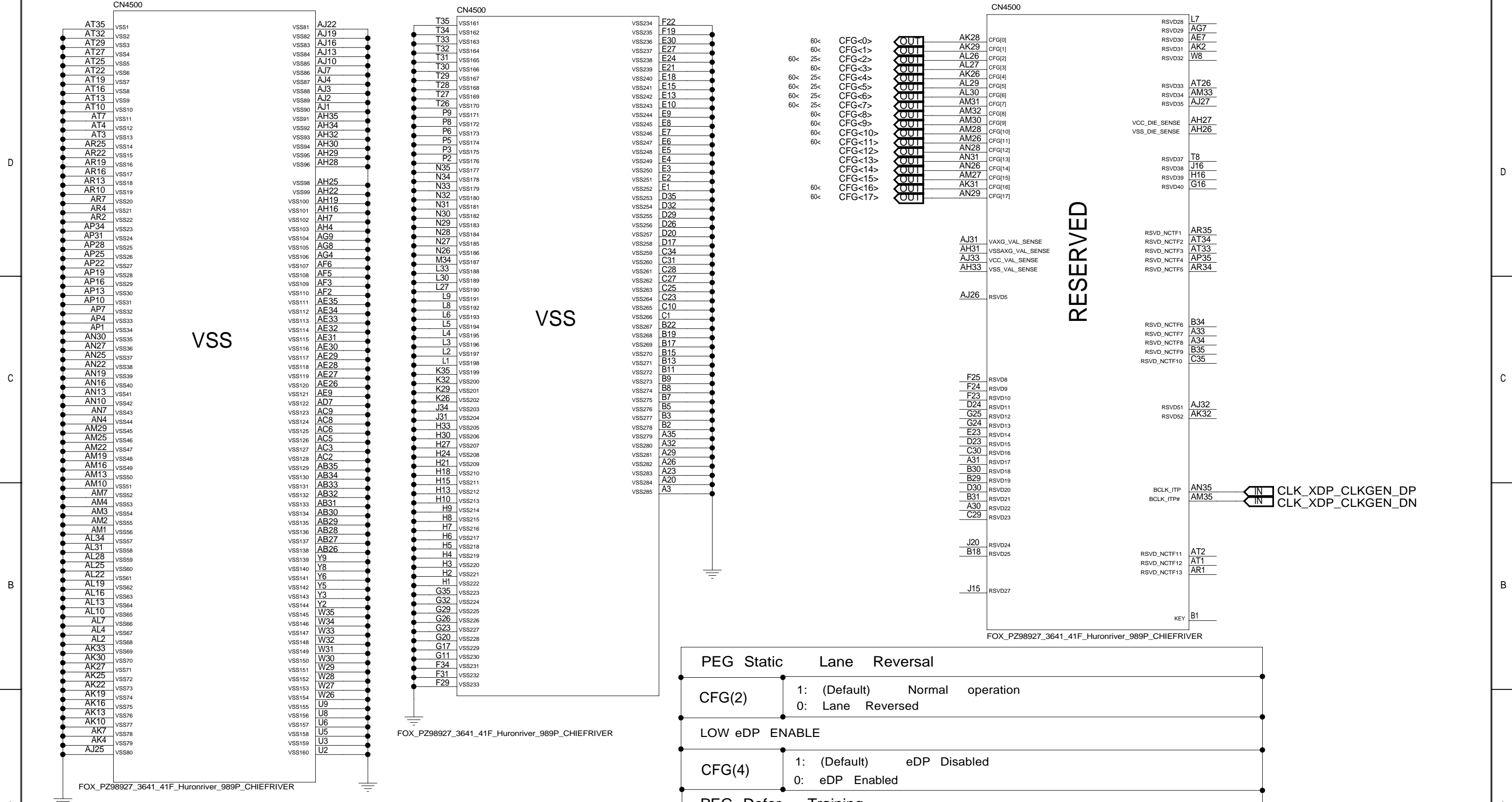


POWER



INVENTEC				
TITLE EVEREST-M CPU 5 POWER				
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01	

CHANGE by Frank Hu DATE Mon Jan 03 17:28:06 2011 SHEET 24 of 97



PEG Static	Lane Reversal	CFG(2)	1: (Default) Normal operation 0: Lane Reversed
LOW eDP ENABLE		CFG(4)	1: (Default) eDP Disabled 0: eDP Enabled
PEG Defer Training		CFG(7)	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training
PCIE Port Bifurcation Straps		CFG[6:5]	11: (Default) x16 - Device 1 function 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8, x4, x4 - Device 1 function 1 and 2 enabled

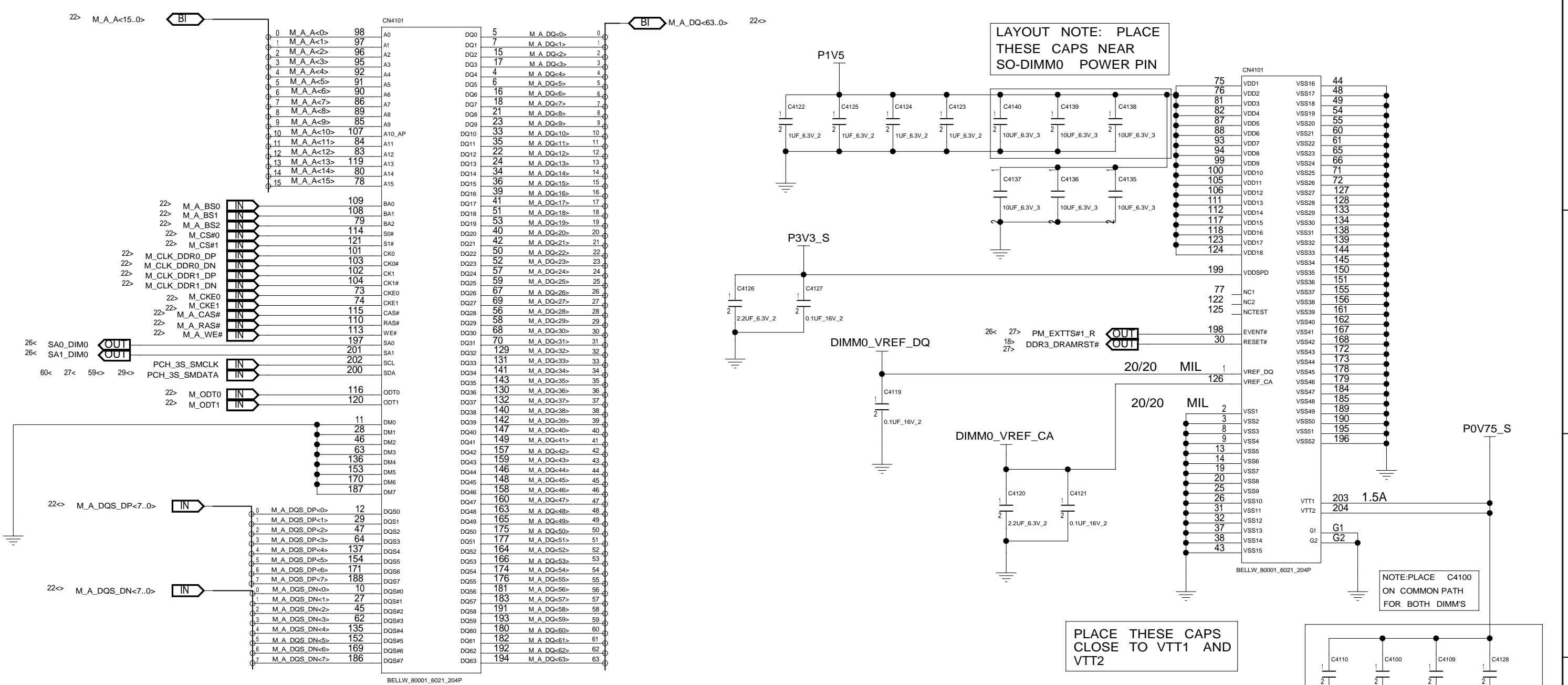
INVENTEC

TITLE EVEREST-M
CPU 6 GND

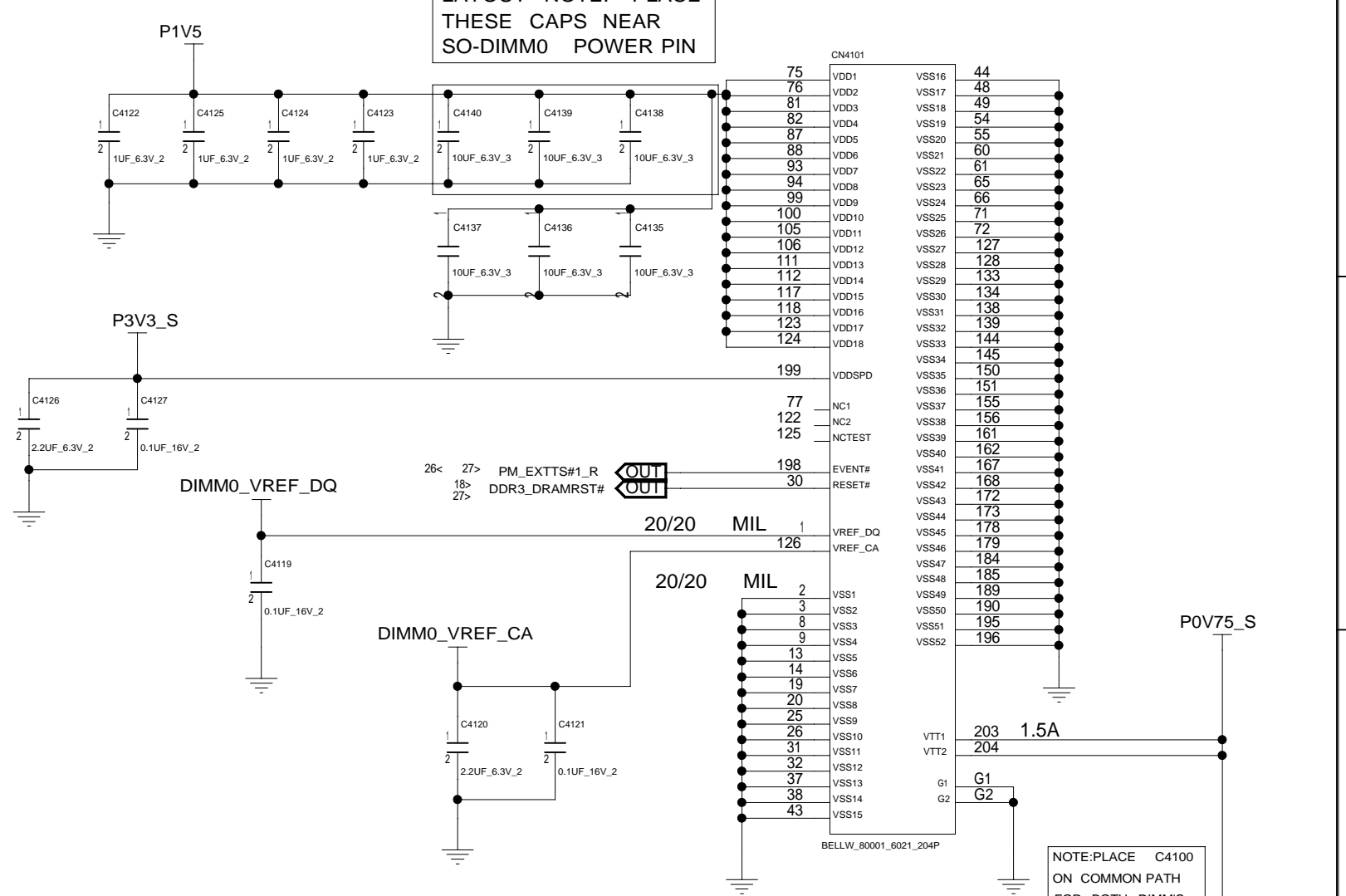
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01
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CHANGE by Frank Hu DATE Fri Dec 31 10:16:59 2010 SHEET 25 of 97

CHA

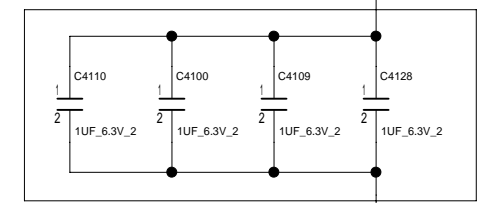


LAYOUT NOTE: PLACE THESE CAPS NEAR SO-DIMM0 POWER PIN

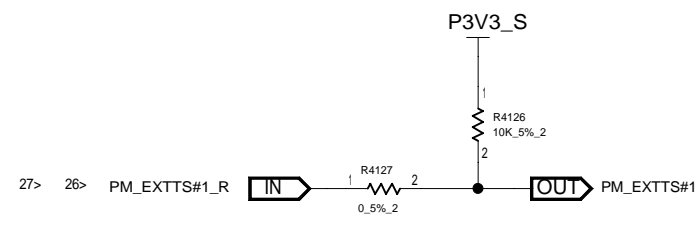
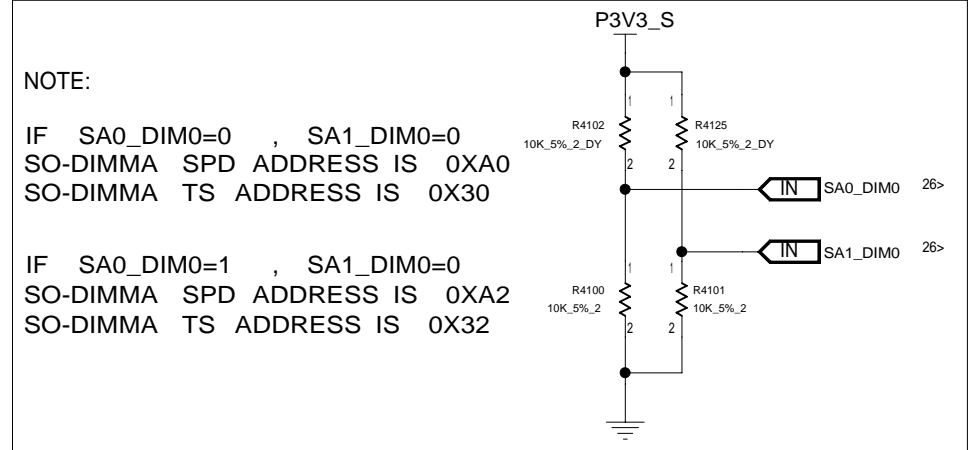


PLACE THESE CAPS CLOSE TO VTT1 AND VTT2

NOTE: PLACE C4100 ON COMMON PATH FOR BOTH DIMM'S

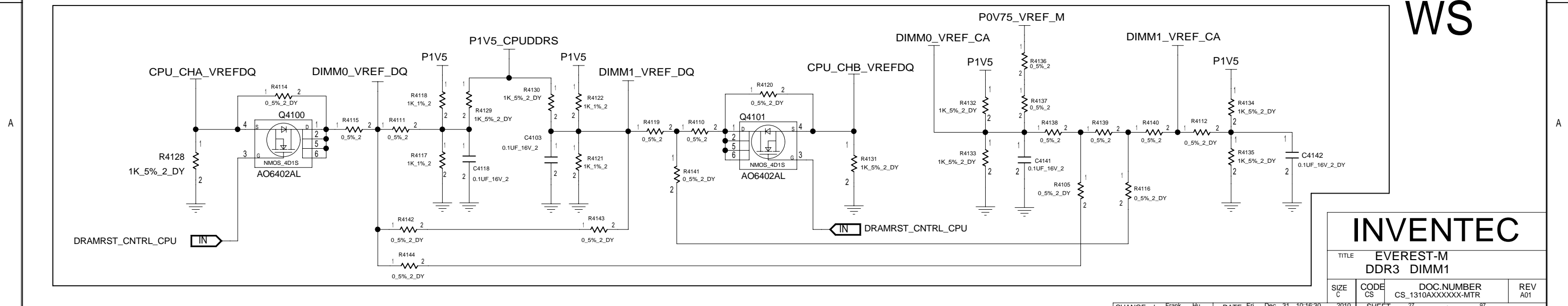
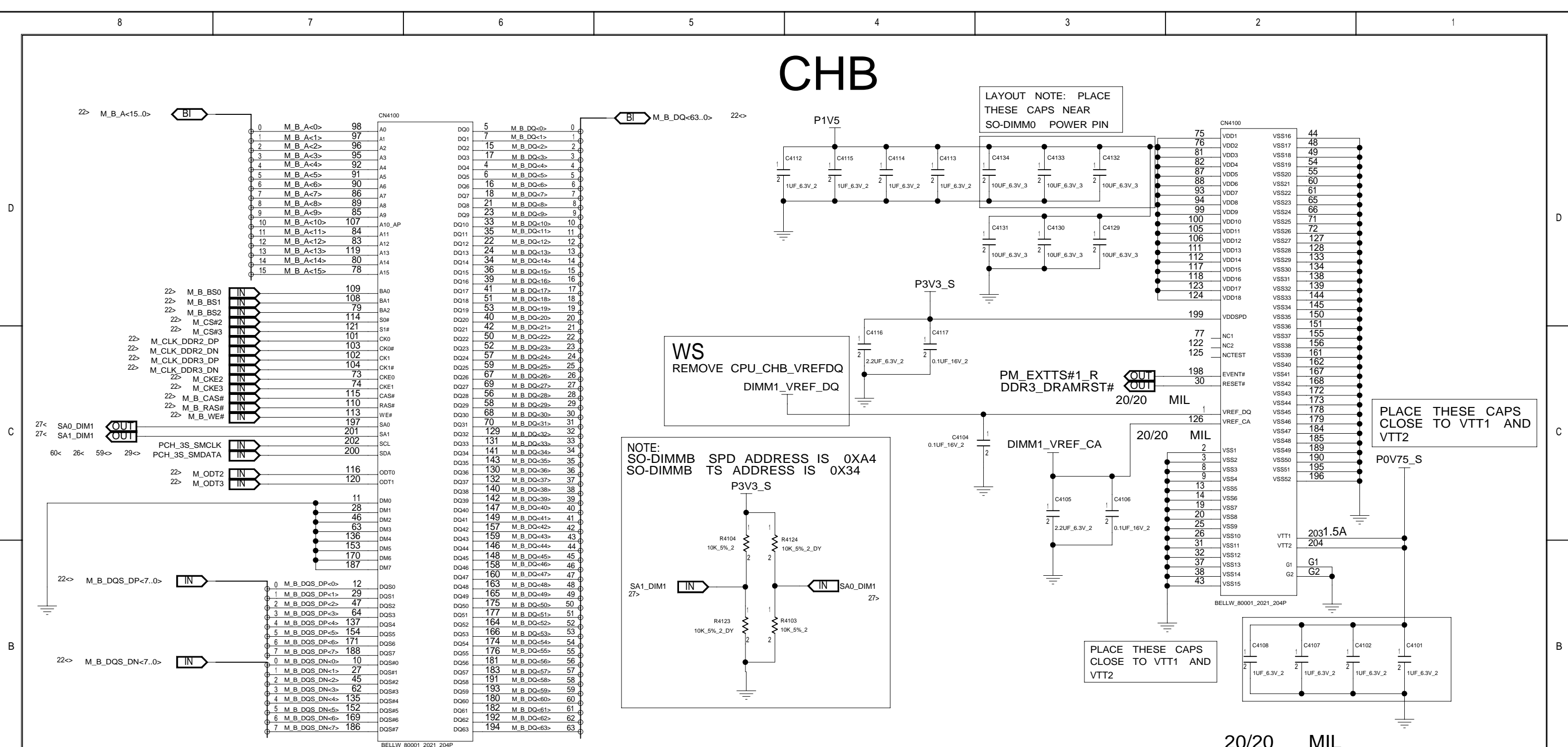


WS REMOVE 1UF CAP 1PCS

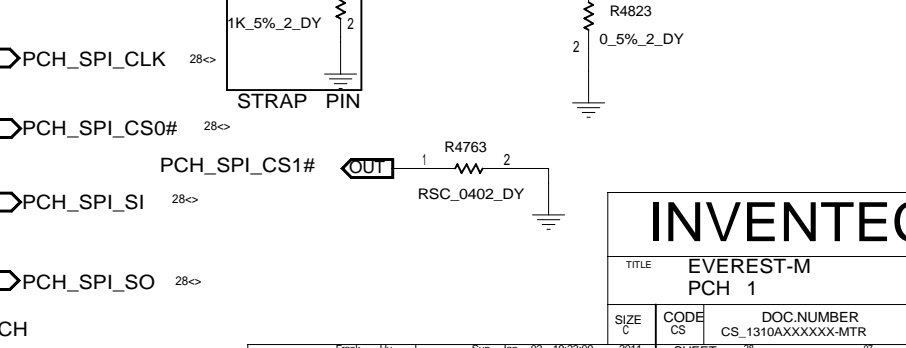
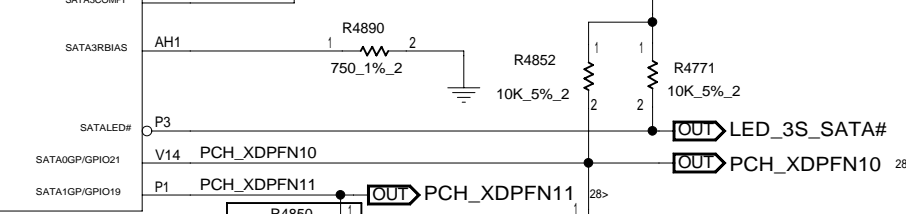
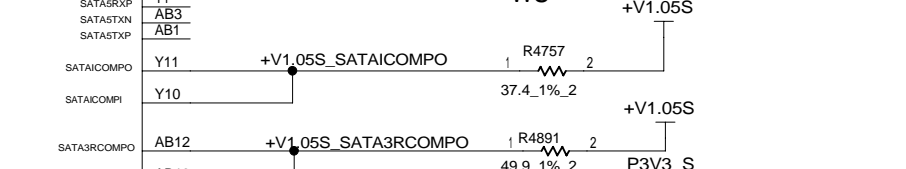
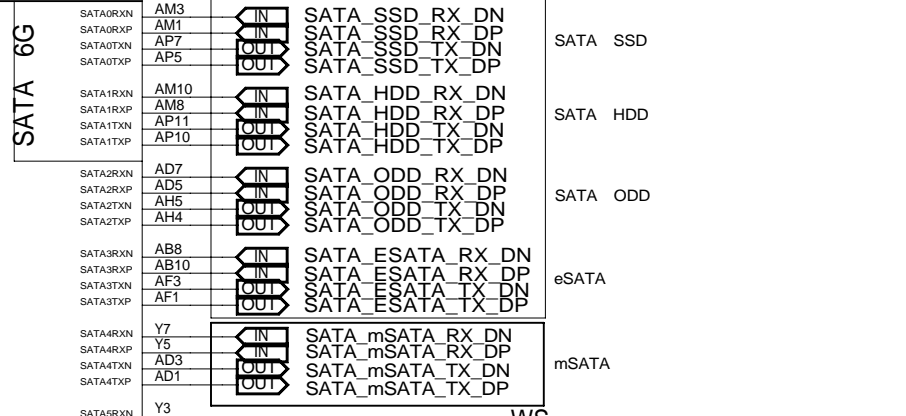
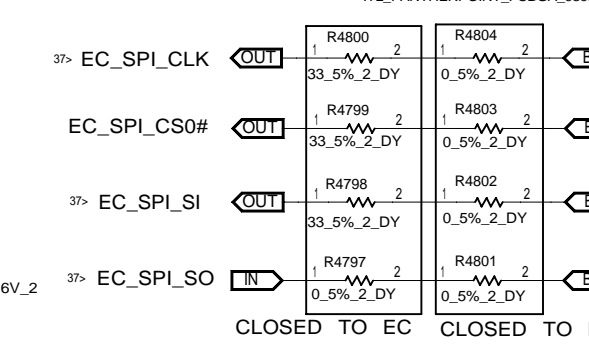
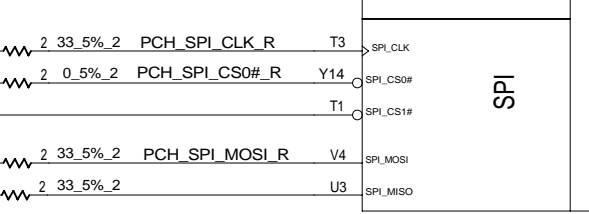
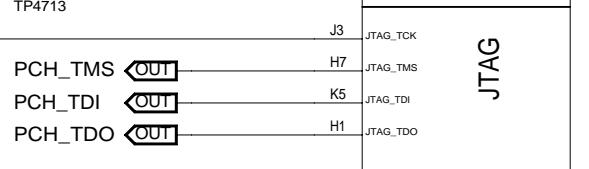
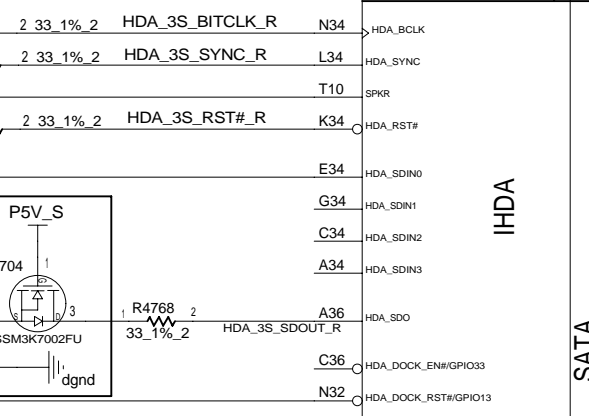
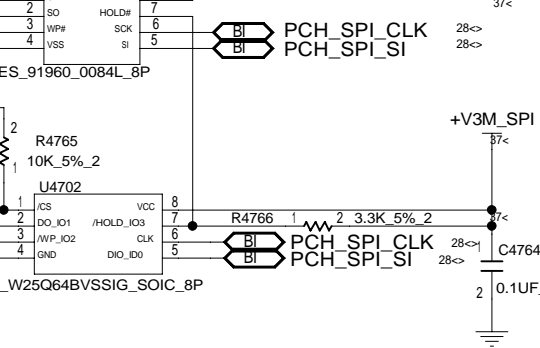
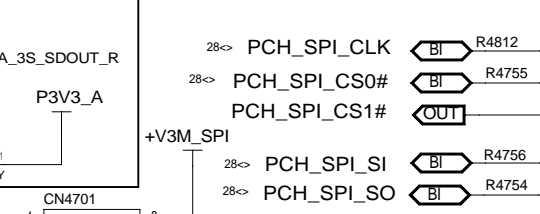
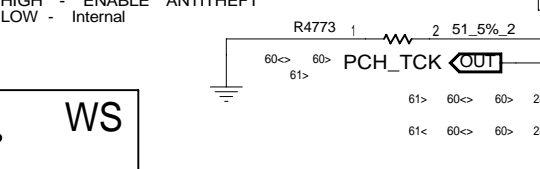
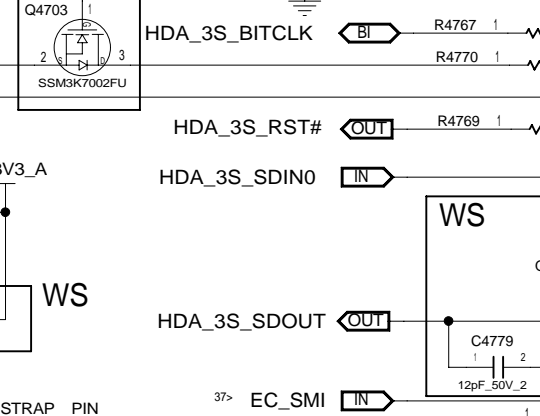
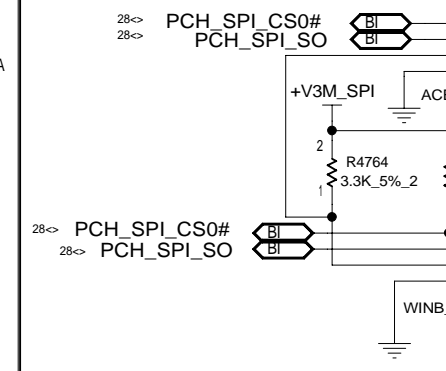
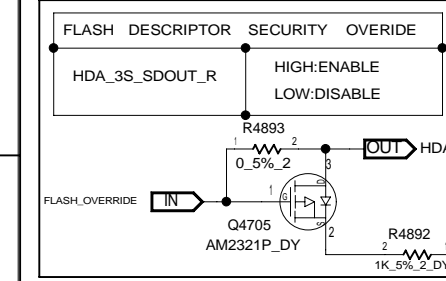
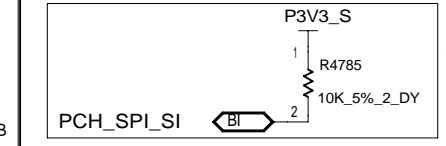
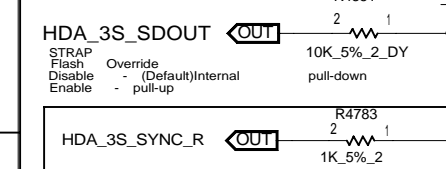
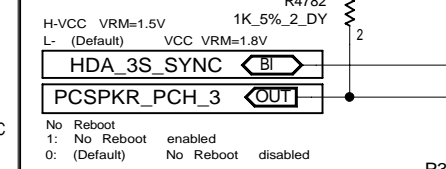
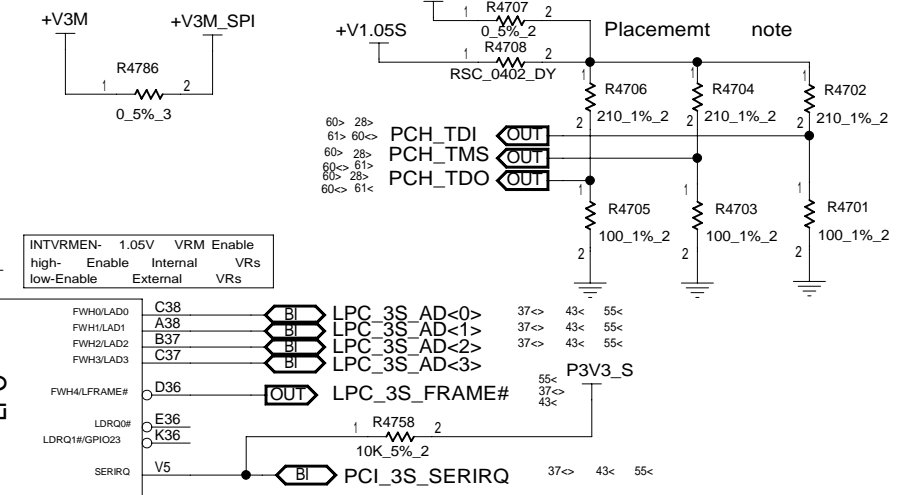
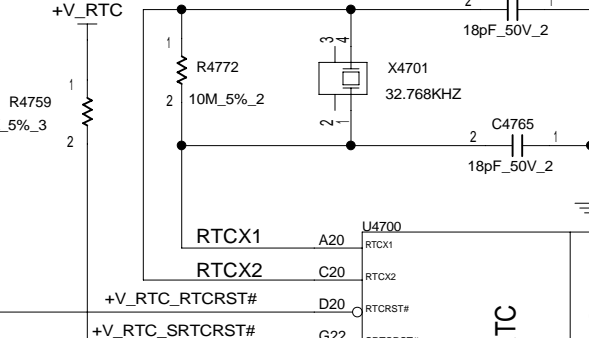
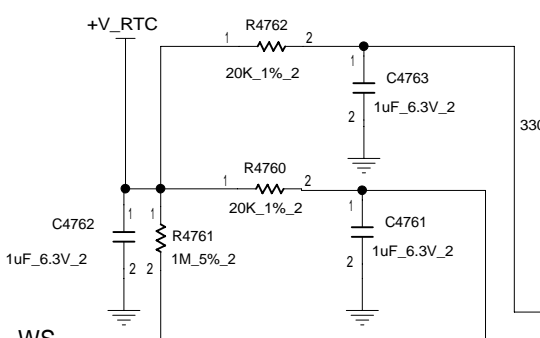
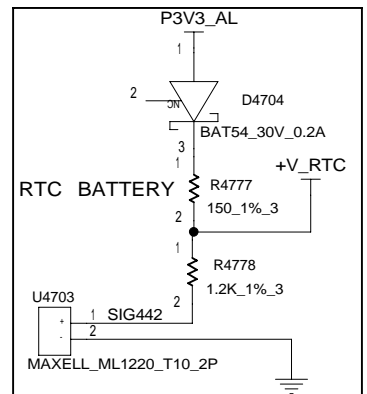


INVENTEC				
TITLE EVEREST-M DDR3 DIMM0				
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01	

CHB



INVENTEC				
TITLE EVEREST-M DDR3 DIMM1				
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01	
CHANGE by Frank Hu			DATE Fri Dec 31 10:16:30 2010	SHEET 27 of 97

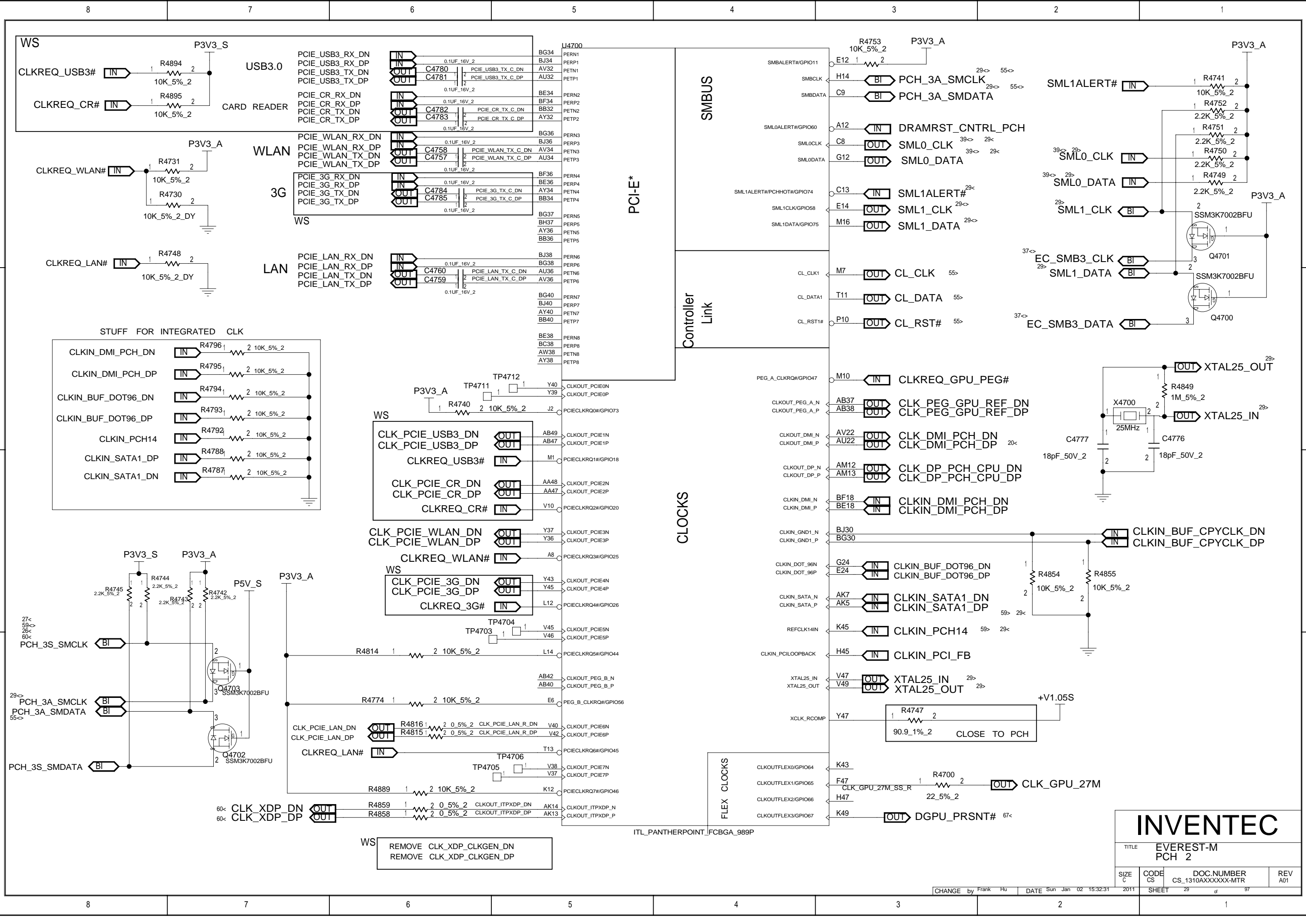


Distance between the PCH and cap on the "P" signal should be identical distance between the PCH and cap on the "N" signal for same pair

INVENTEC

TITLE EVEREST-M			
PCH 1			
SIZE C	CODE CS	DOC.NUMBER CS_1310AAXXXXX-MTR	REV A01
CHANGE by Frank Hu		DATE Sun Jan 02 19:22:09 2011	SHEET 28 of 97

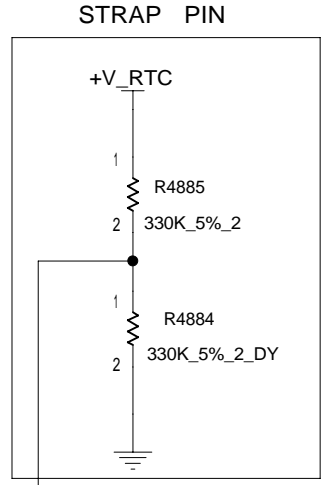
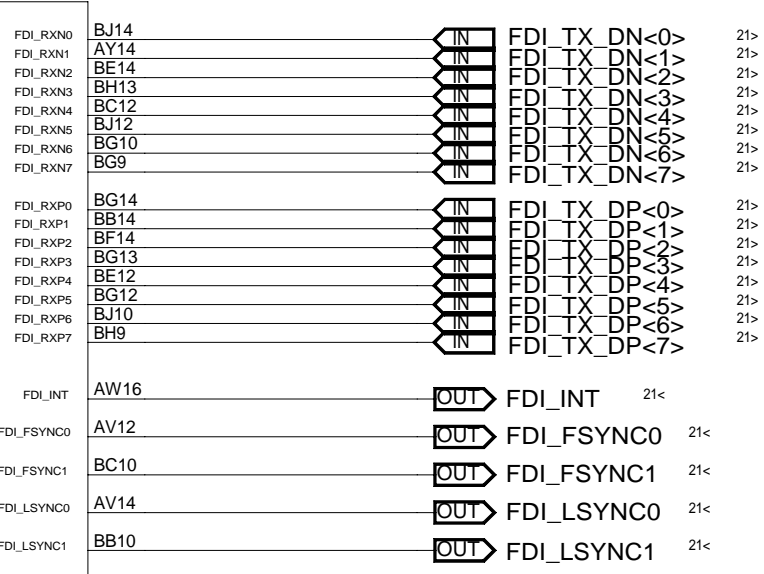
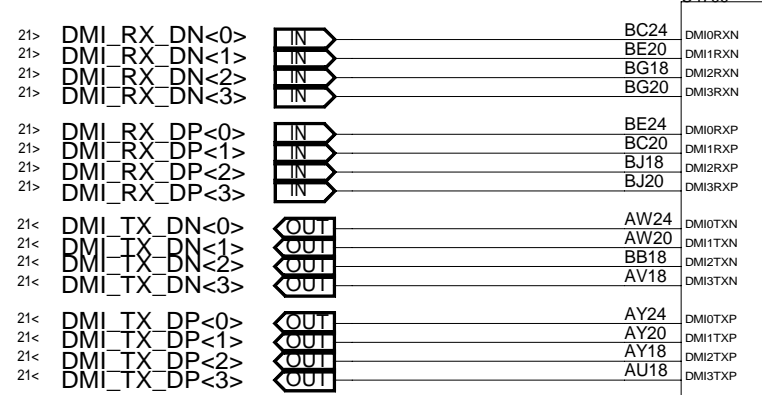
CLOSED TO EC CLOSED TO PCH



WS REMOVE CLK_XDP_CLKGEN_DN
REMOVE CLK_XDP_CLKGEN_DP

INVENTEC			
TITLE EVEREST-M PCH 2			
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01
CHANGE by Frank Hu		DATE Sun Jan 02 15:32:31	2011 SHEET 29 of 97

DSWVRMEN - Deep S4/S5 Well On-Die Voltage Regulator Enable
 high-Enabled(Default)
 low-Disabled



D

C

B

A

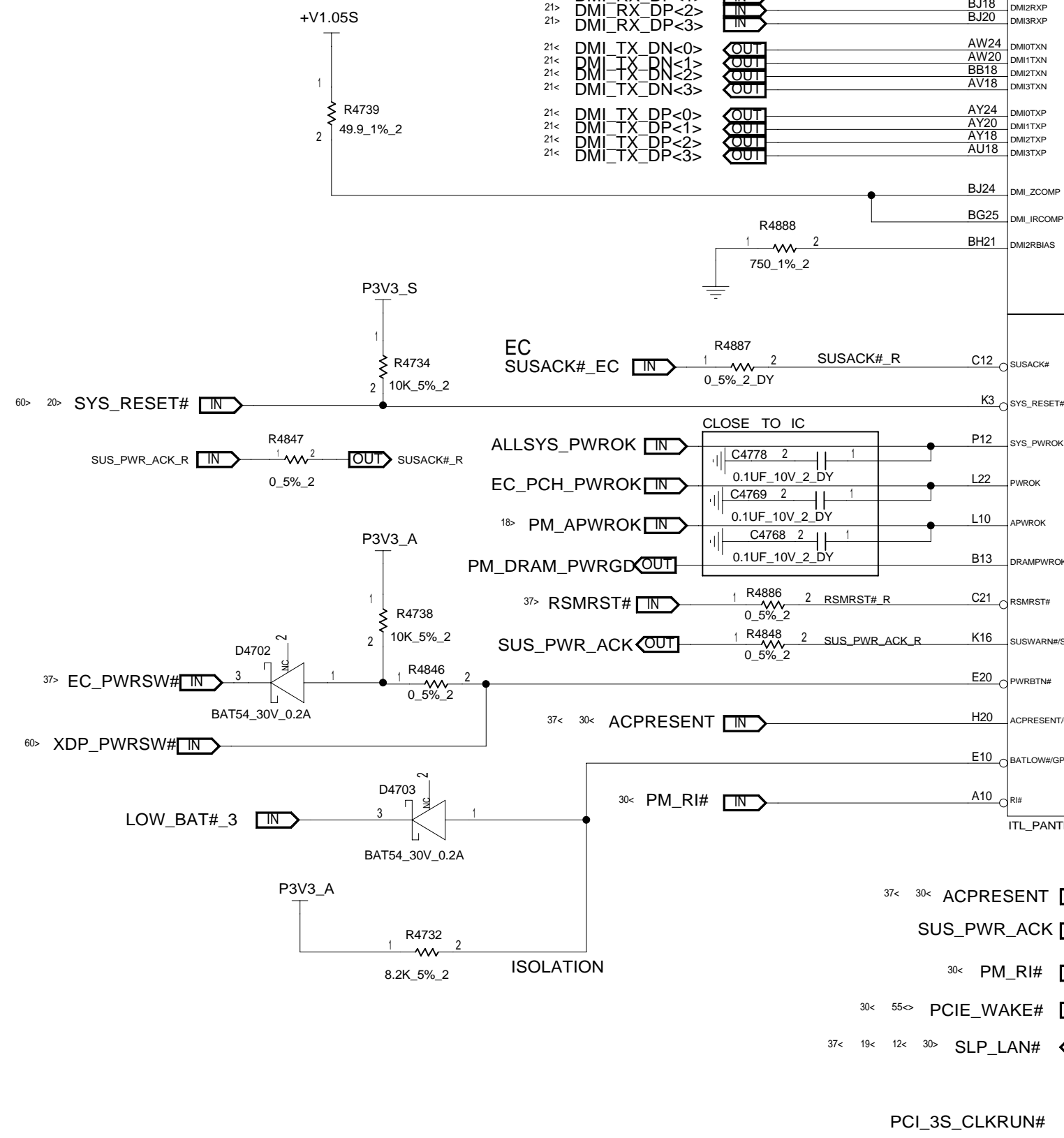
D

C

B

A

System Power Management



INVENTEC			
TITLE EVEREST-M PCH 3			
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01
2011	SHEET 30	of 97	

D

C

B

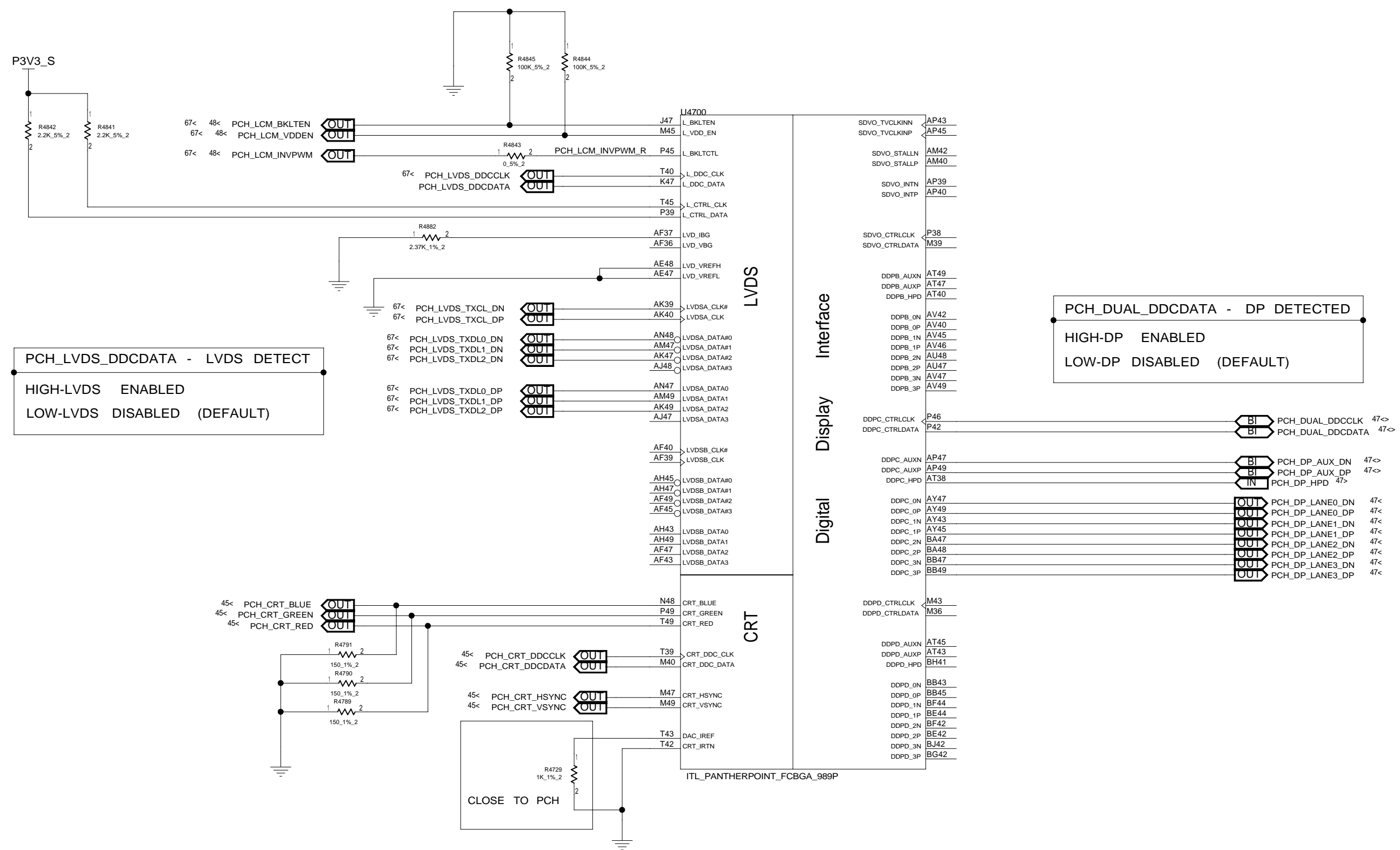
A

D

C

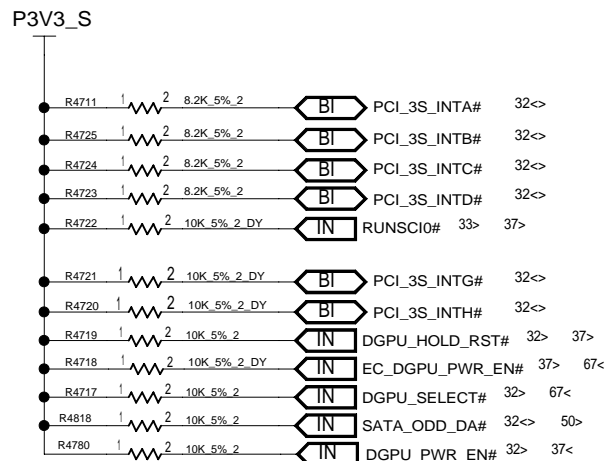
B

A

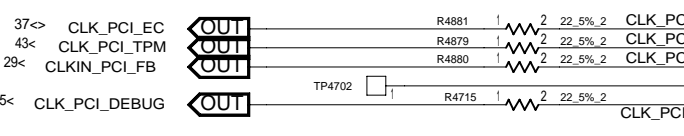
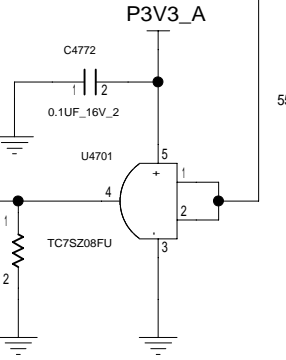
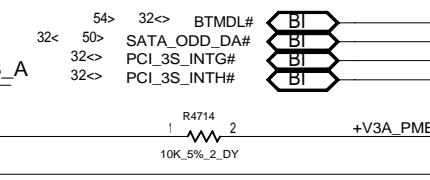
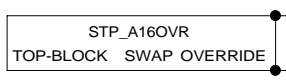
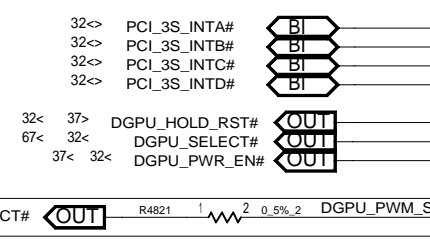
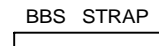
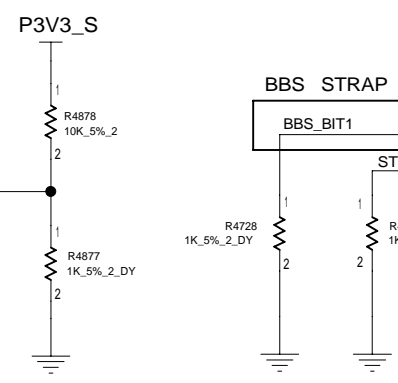
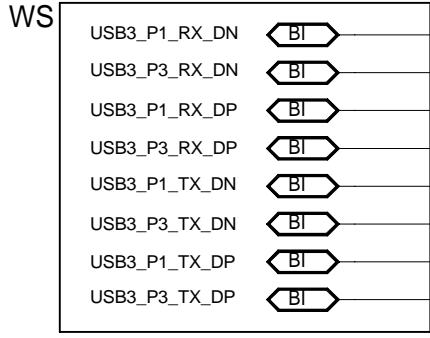


INVENTEC				
TITLE EVEREST-M PCH 4 AXG				
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01	

GPIO51		GPIO19		BOOT BIOS	
BBS_BIT1	BBS_BIT0	DESTINATION			
0	1	RESERVED(NAND)			
1	0	-			
1	1	SPI (DEFAULT)			
0	0	LPC			



Routed with 90 ohms impedance
 Total length no longer than 11 inches



- U4700
- BG26 TP1
- BJ26 TP2
- BH25 TP3
- BJ16 TP4
- BG16 TP5
- AH38 TP6
- AH37 TP7
- AK43 TP8
- AK45 TP9
- C18 TP10
- N30 TP11
- H3 TP12
- AH12 TP13
- AM4 TP14
- AM5 TP15
- Y13 TP16
- K24 TP17
- L24 TP18
- AB46 TP19
- AB45 TP20
- B21 TP21
- M20 TP22
- AY16 TP23
- BG46 TP24

- RSVD1 AY7
- RSVD2 AY7
- RSVD3 AU3
- RSVD4 BG4
- RSVD5 AT10
- RSVD6 BC8
- RSVD7 AU2
- RSVD8 AT4
- RSVD9 AT3
- RSVD10 AT1
- RSVD11 AY3
- RSVD12 AT5
- RSVD13 AV3
- RSVD14 AV1
- RSVD15 BB1
- RSVD16 BA3
- RSVD17 BB5
- RSVD18 BB3
- RSVD19 BB7
- RSVD20 BE8
- RSVD21 BD4
- RSVD22 BF6
- RSVD23 AV5
- RSVD24 AV10
- RSVD25 AT8
- RSVD26 AY5
- RSVD27 BA2
- RSVD28 AT12
- RSVD29 BF3

- USB3R1
- USB3R2
- USB3R3
- USB3R4
- USB3RP1
- USB3RP2
- USB3RP3
- USB3RP4
- USB3TN1
- USB3TN2
- USB3TN3
- USB3TN4
- USB3TP1
- USB3TP2
- USB3TP3
- USB3TP4

- PIRQA# K40
- PIRQB# K38
- PIRQC# H38
- PIRQD# G38
- REQ1#/GPIO51 D47
- REQ2#/GPIO52 C44
- REQ3#/GPIO54 E40
- GNT1#/GPIO51 D47
- GNT2#/GPIO53 E42
- GNT3#/GPIO55 F46
- PIRQE#/GPIO2 G42
- PIRQF#/GPIO3 G40
- PIRQG#/GPIO4 C42
- PIRQH#/GPIO5 D44
- PME# K10
- PLTRST# C6
- CLKOUT_PCI0 H49
- CLKOUT_PCI1 H43
- CLKOUT_PCI2 J48
- CLKOUT_PCI3 K42
- CLKOUT_PCI4 H40

- OC0#/GPIO59 A14
- OC1#/GPIO40 K20
- OC2#/GPIO41 B17
- OC3#/GPIO42 C16
- OC4#/GPIO43 L16
- OC5#/GPIO9 A16
- OC6#/GPIO10 D14
- OC7#/GPIO14 C14

- PCH_XDPFN0 IN
- PCH_XDPFN1 IN
- PCH_XDPFN2 IN
- PCH_XDPFN3 IN
- PCH_XDPFN4 IN
- PCH_XDPFN5 IN
- PCH_XDPFN6 IN
- PCH_XDPFN7 IN

- USBP0N C24
- USBP0P A24
- USBP1N C25
- USBP1P B25
- USBP2N C26
- USBP2P A26
- USBP3N K28
- USBP3P H28
- USBP4N E28
- USBP4P D28
- USBP5N A28
- USBP5P C29
- USBP6N B29
- USBP7N N28
- USBP7P M28
- USBP8N L30
- USBP8P K30
- USBP9N G30
- USBP9P E30
- USBP10N C30
- USBP10P A30
- USBP11N L32
- USBP11P K32
- USBP12N G32
- USBP12P E32
- USBP13N C32
- USBP13P A32

- USB_P0_DN BI
- USB_P0_DP BI
- USB_P1_DN BI
- USB_P1_DP BI
- USB_P2_DN BI
- USB_P2_DP BI
- USB_P5_DN BI
- USB_P5_DP BI
- USB_P10_DN BI
- USB_P10_DP BI
- USB_P12_DN BI
- USB_P12_DP BI
- USB_P13_DN BI
- USB_P13_DP BI

- USB_OC#_0 IN
- USB_OC#_1 IN
- USB_OC#_2 IN
- SMC_WAKE_SCI# IN

- SMC_WAKE_SCI# OUT

INVENTEC

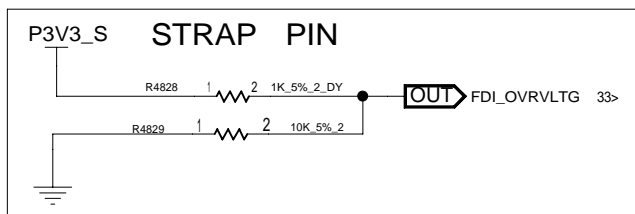
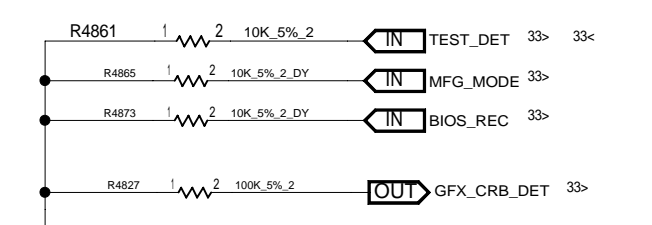
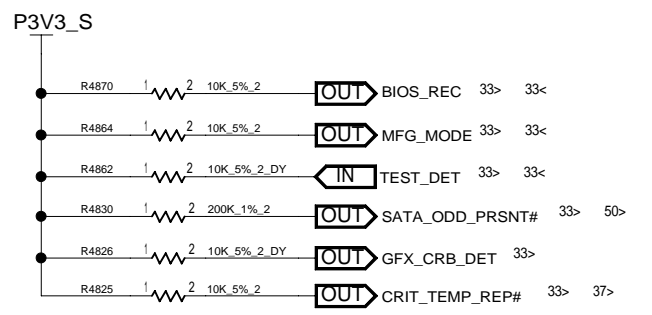
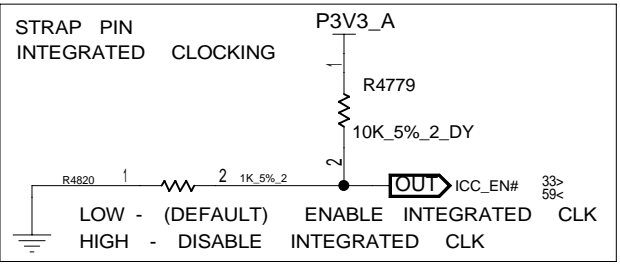
TITLE EVEREST-M
 PCH 5 USB

SIZE	CODE	DOC.NUMBER	REV
C	CS	CS_1310AXXXXX-MTR	A01

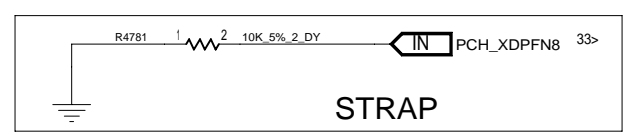
CHANGE by Frank Hu DATE Sun Jan 02 17:15:21 2011 SHEET 32 of 97



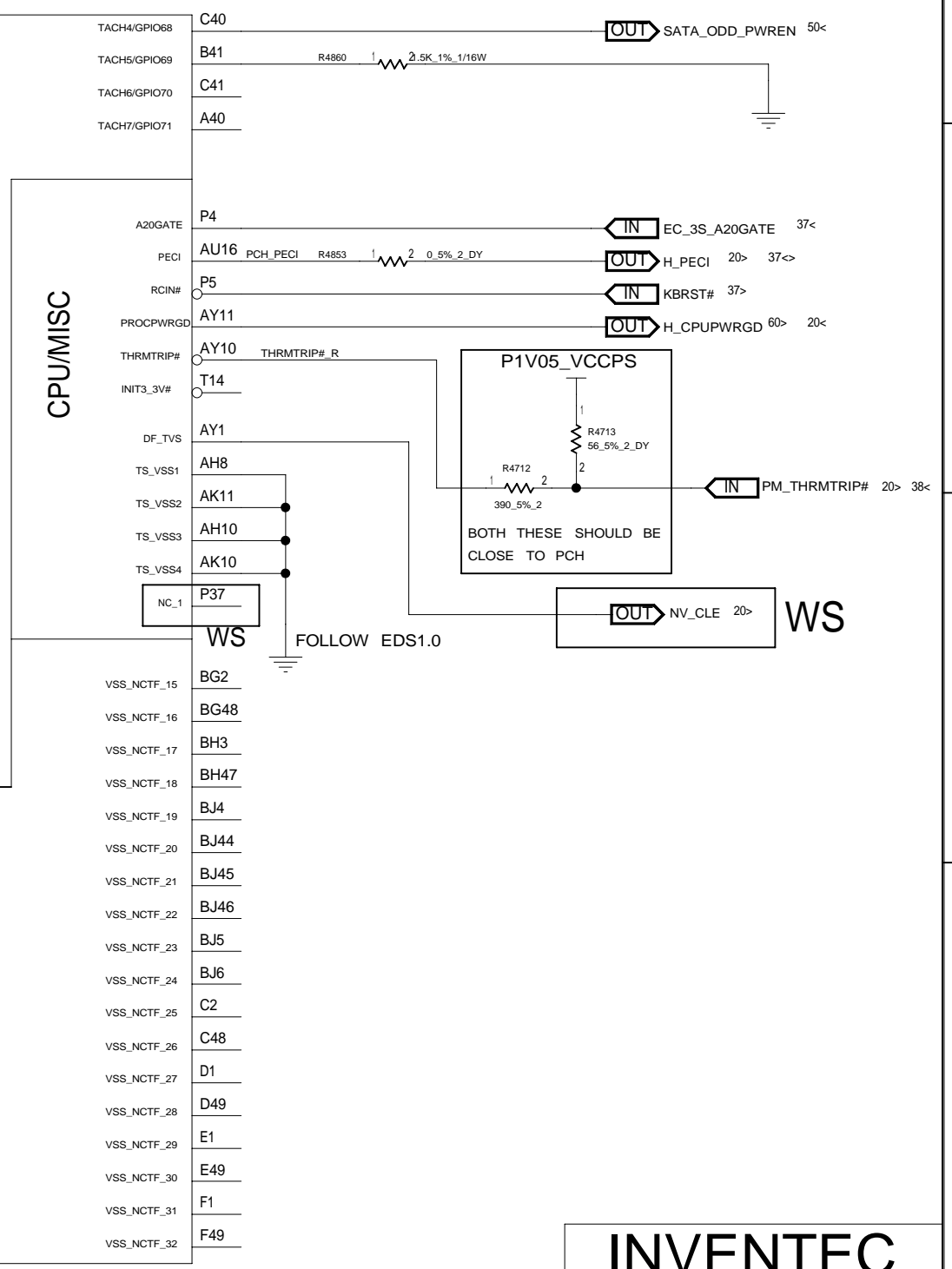
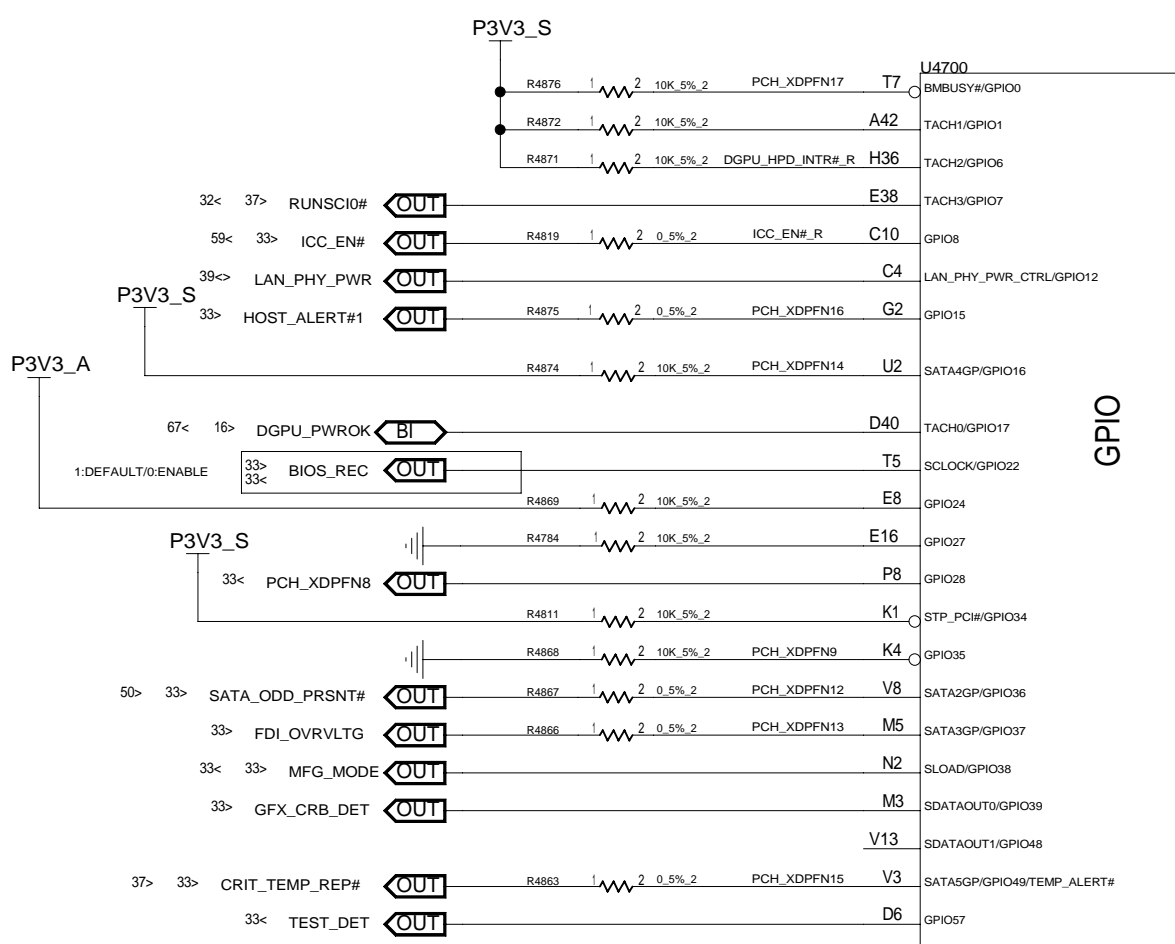
STRAP PIN
HOST_ALERT#1 - TLS CONFIDENTIALITY
 LOW - (DEFAULT) INTEL ME CRYPTO TRANSPORT LAYER SECURITY(TLS) CIPHER SUITE WITH NO CONFIDENTIALITY
 HIGH - INTEL ME CRYPTO TLS CIPHER SUITE WITH CONFIDENTIALITY



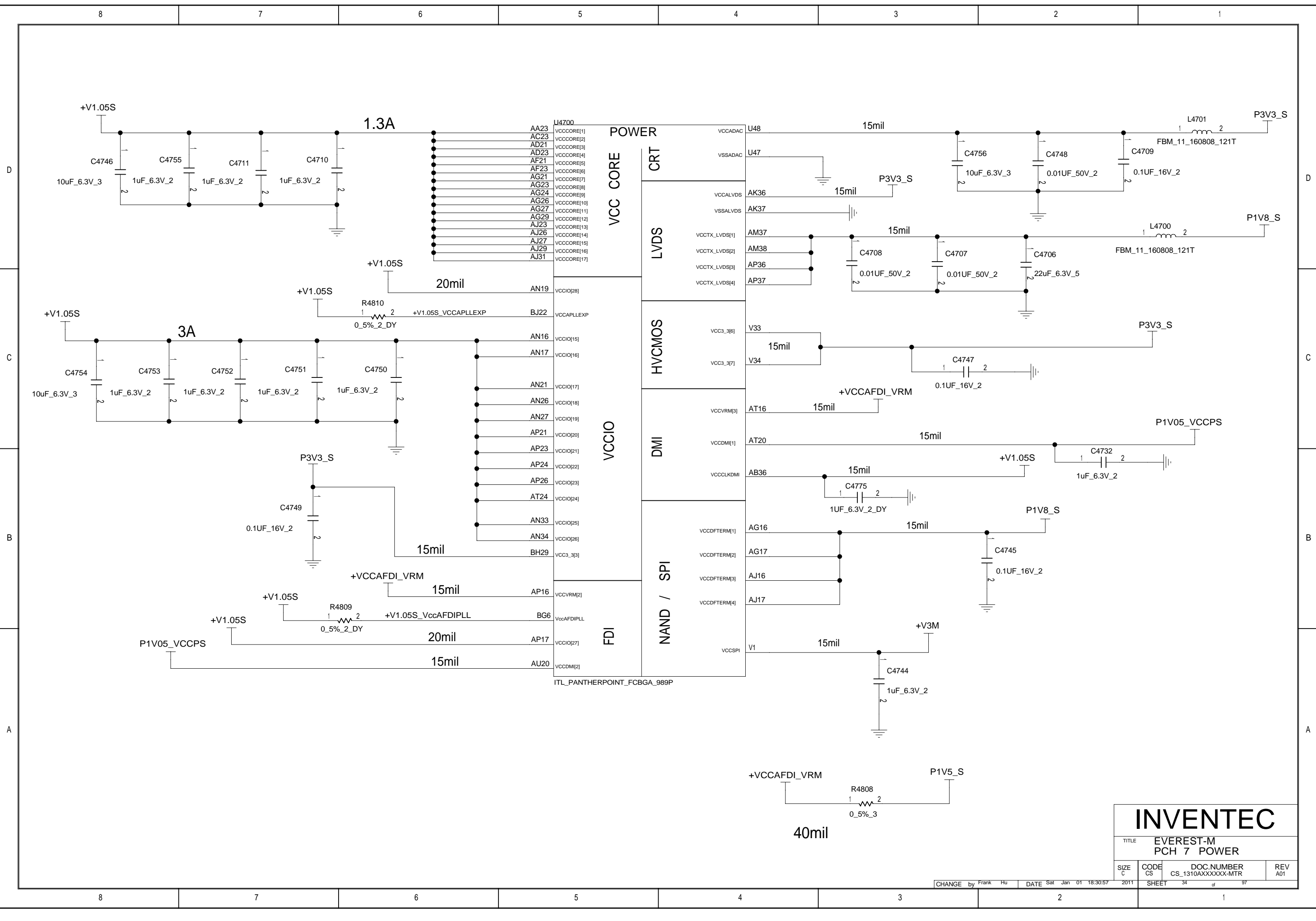
FDI_OVRVLTG
 LOW- TX,RXTERMINATED TO SAME VOLTAGE
 (DC COUPLING MODE) DEFAULT



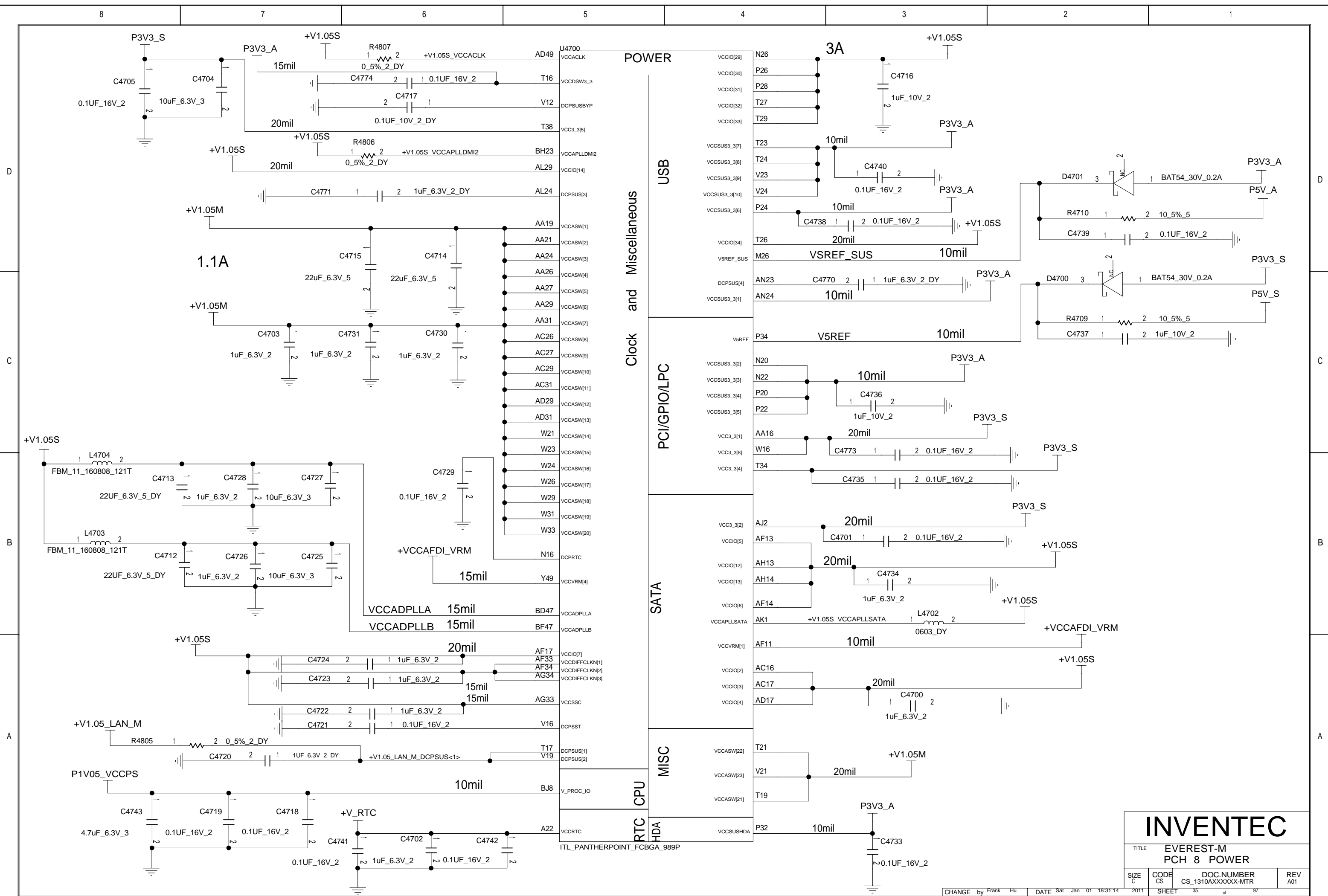
PCH_XDPFN8 - ON DIE PLL VOLTAGE REGULATOR
 HIGH-ENABLED (DEFAULT)
 LOW-DISABLED



INVENTEC			
TITLE EVEREST-M PCH 6 MISC			
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01
CHANGE by Frank Hu		DATE Sun Jan 02 17:58:29 2011	SHEET 33 of 97



INVENTEC			
TITLE EVEREST-M PCH 7 POWER			
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01
CHANGE by Frank Hu		DATE Sat Jan 01 18:30:57 2011	SHEET 34 of 97



INVENTEC			
TITLE EVEREST-M PCH 8 POWER			
SIZE C	CODE CS	DOC. NUMBER CS_1310AXXXXX-MTR	REV A01

CHANGE by Frank Hu DATE Sat Jan 01 18:31:14 2011 SHEET 35 of 97

D

C

B

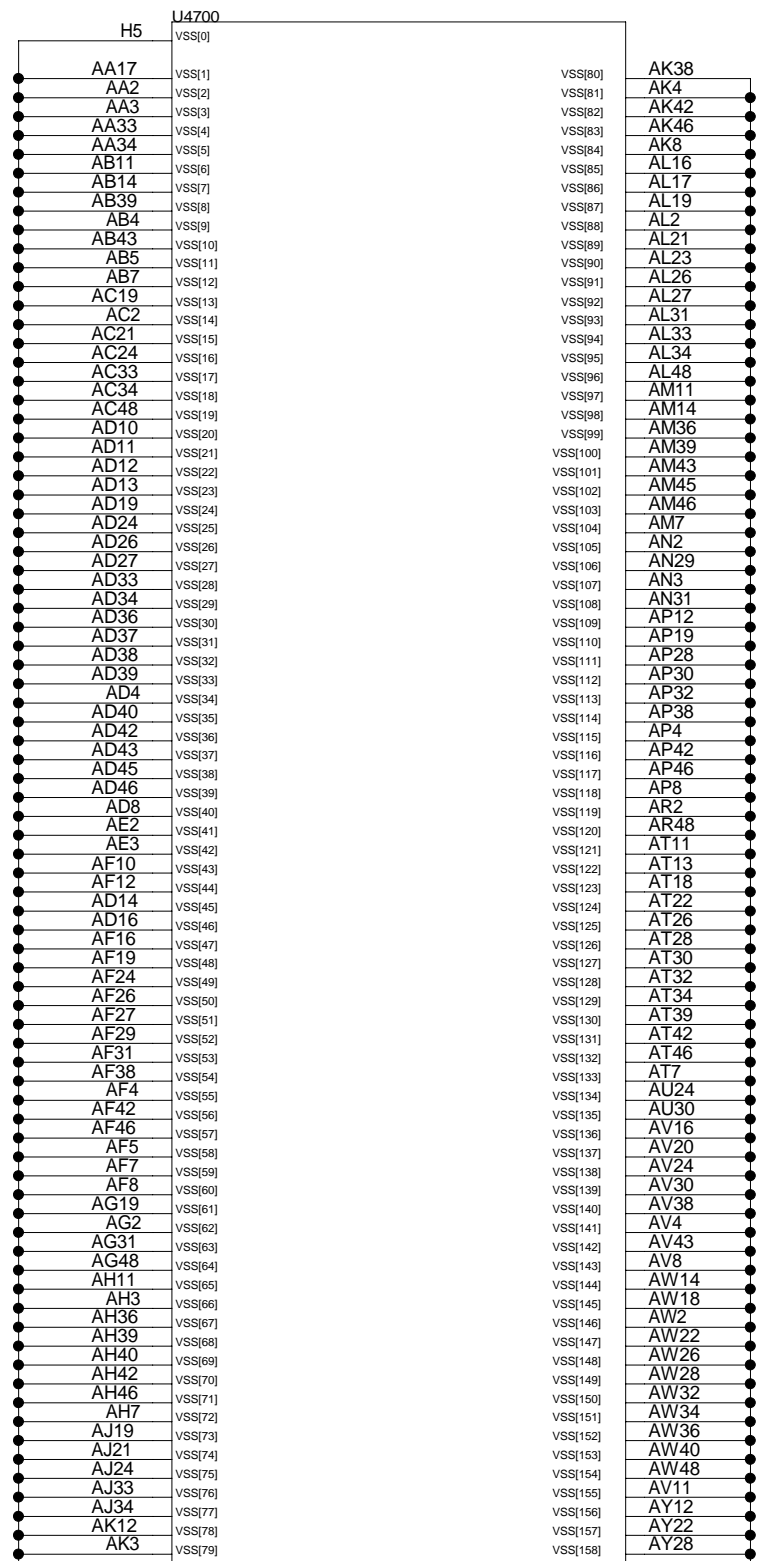
A

D

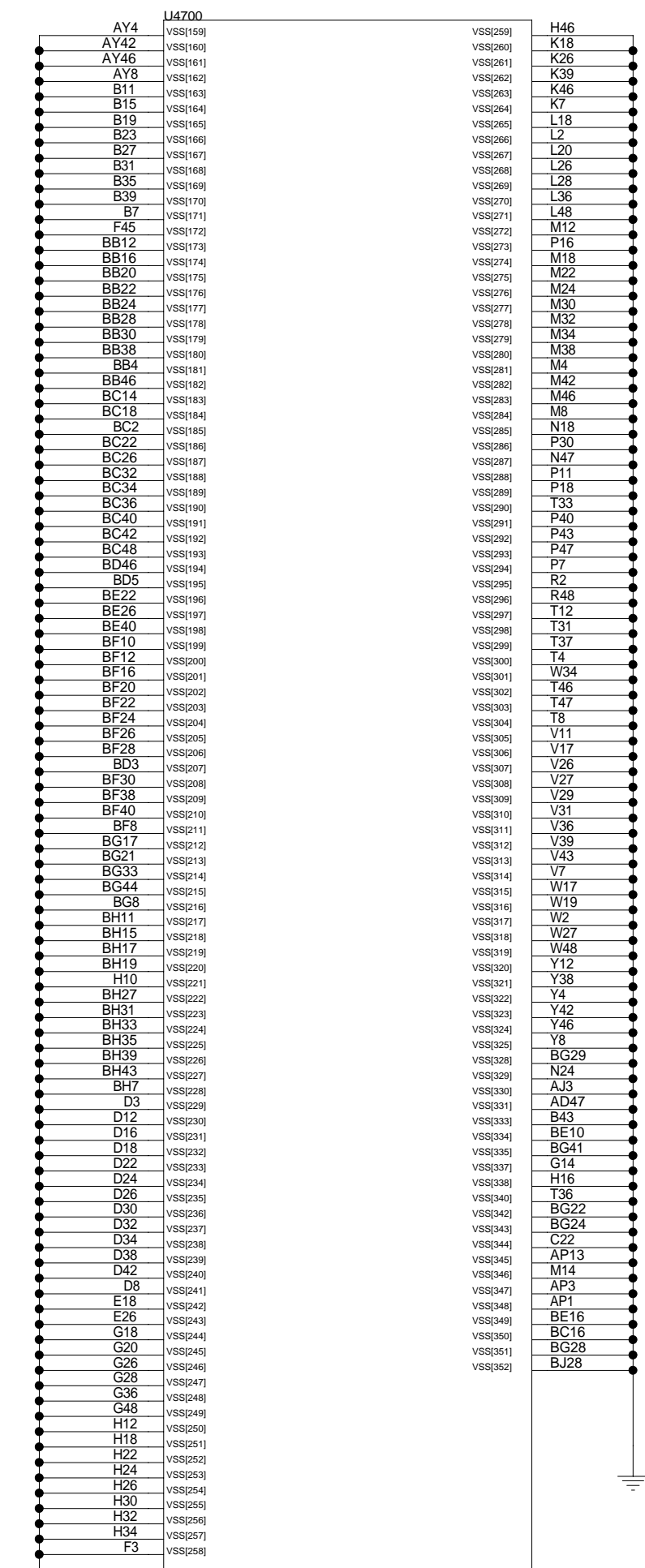
C

B

A



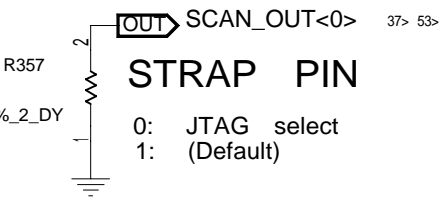
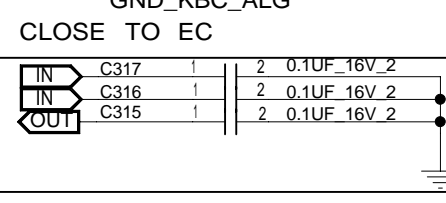
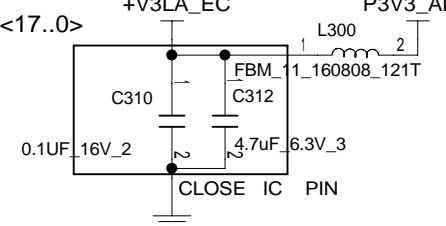
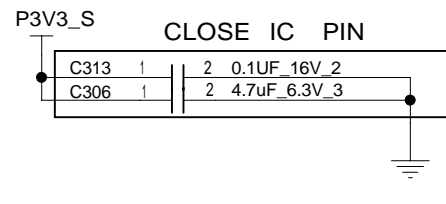
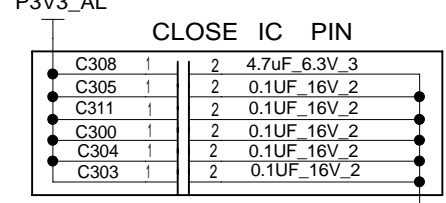
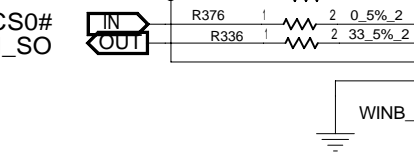
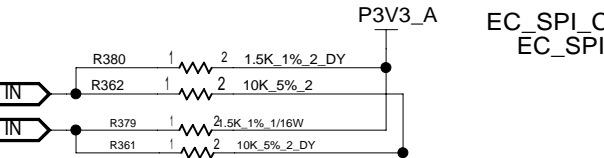
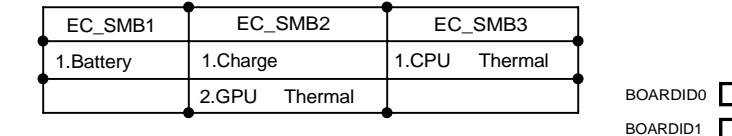
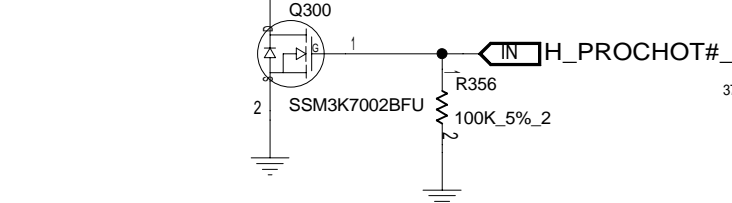
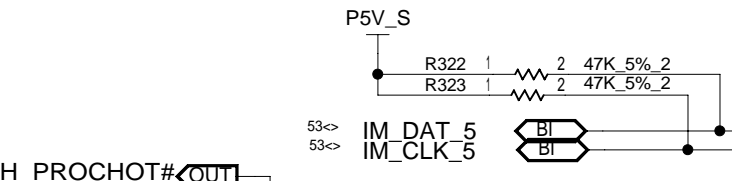
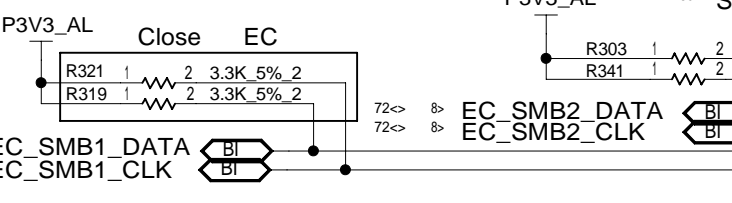
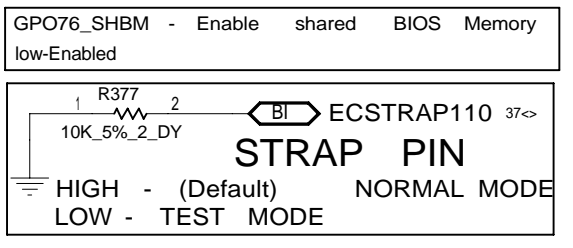
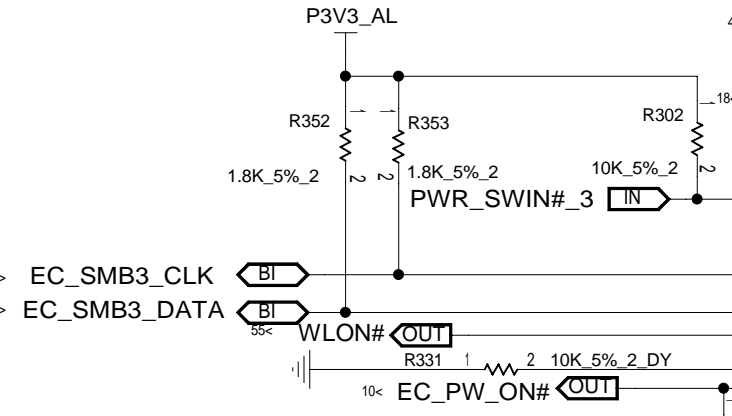
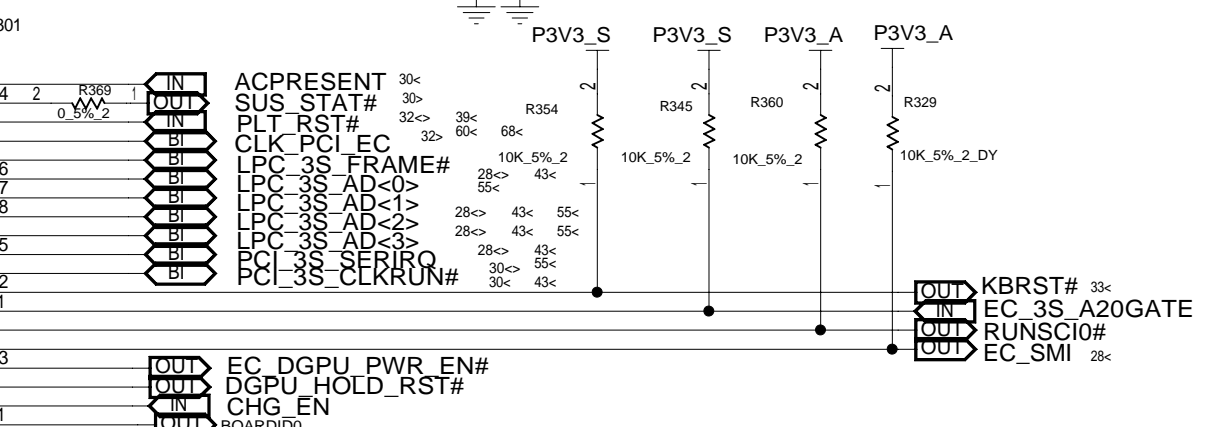
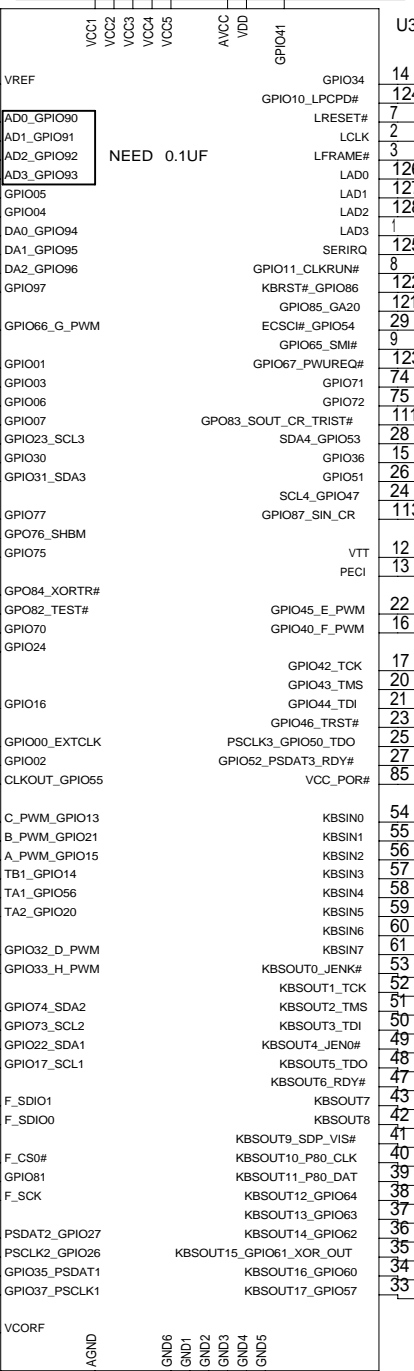
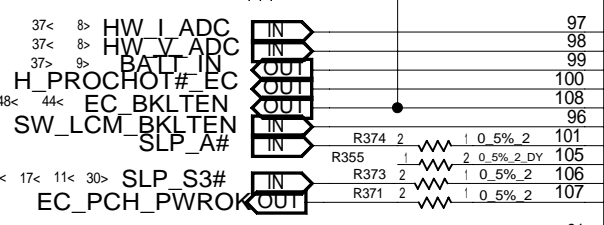
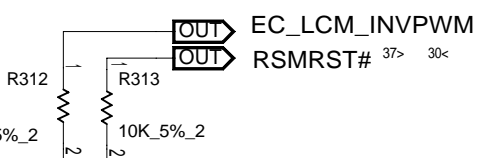
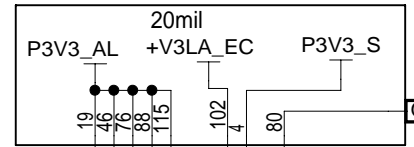
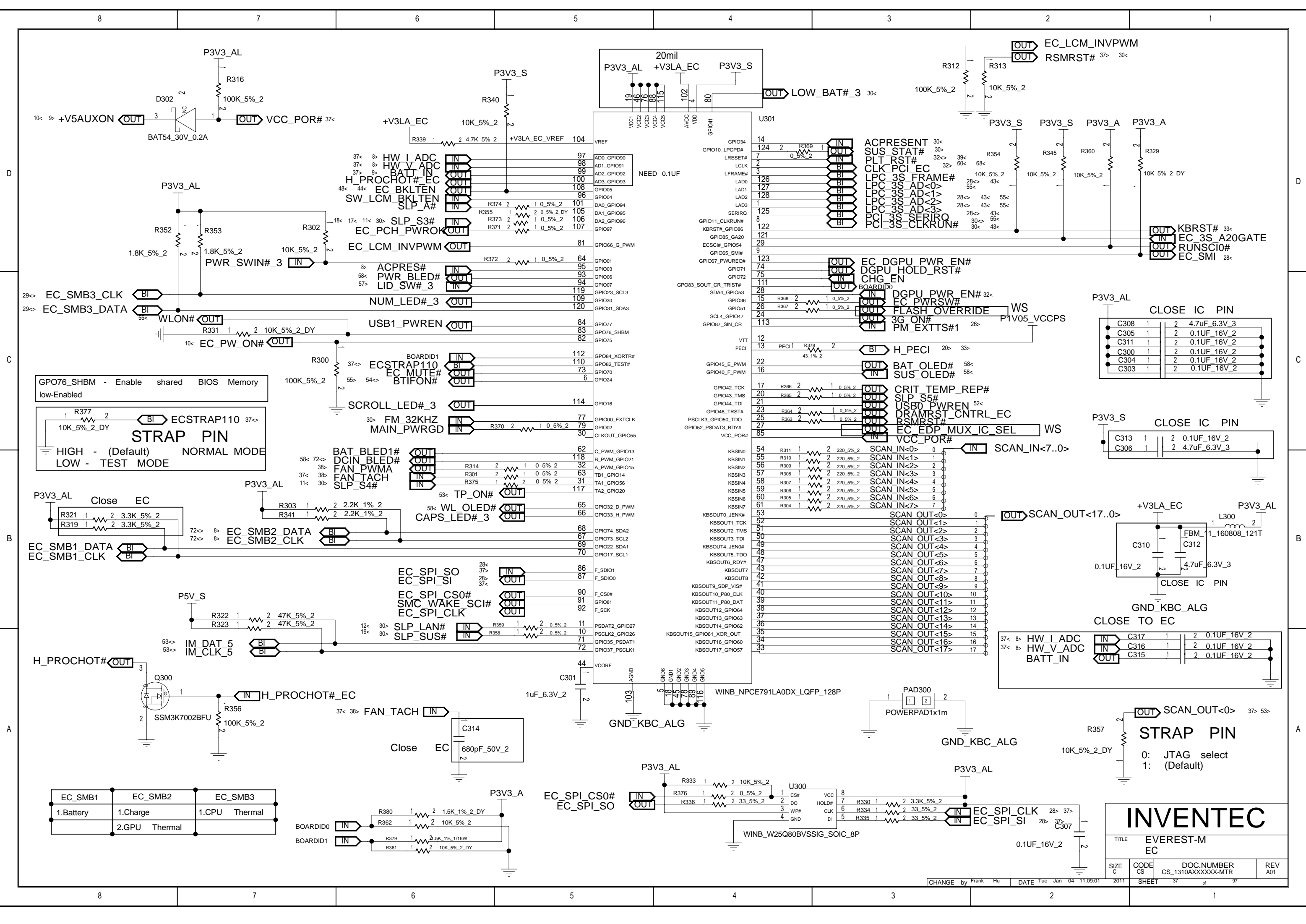
ITL_PANTHERPOINT_FCBGA_989P



ITL_PANTHERPOINT_FCBGA_989P

INVENTEC

TITLE EVEREST-M PCH 9 GND			
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01
CHANGE by Frank Hu		DATE Sun Jan 02 18:04:06 2011	SHEET 36 of 97



INVENTEC			
TITLE EVEREST-M EC			
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01
CHANGE by Frank Hu		DATE Tue Jan 04 11:09:01 2011	SHEET 37 of 97

D

C

B

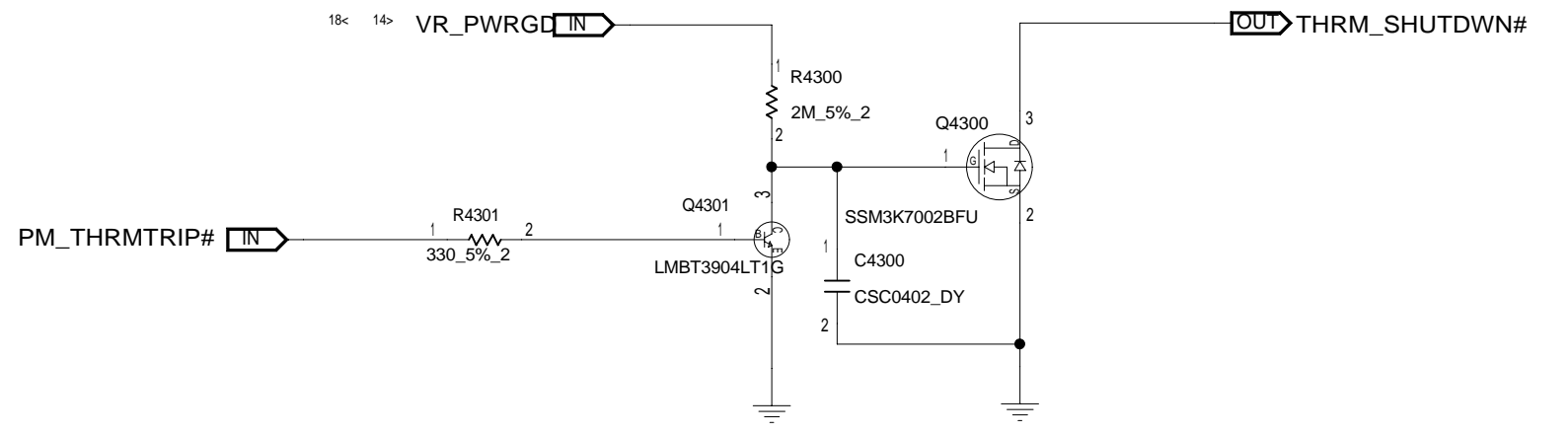
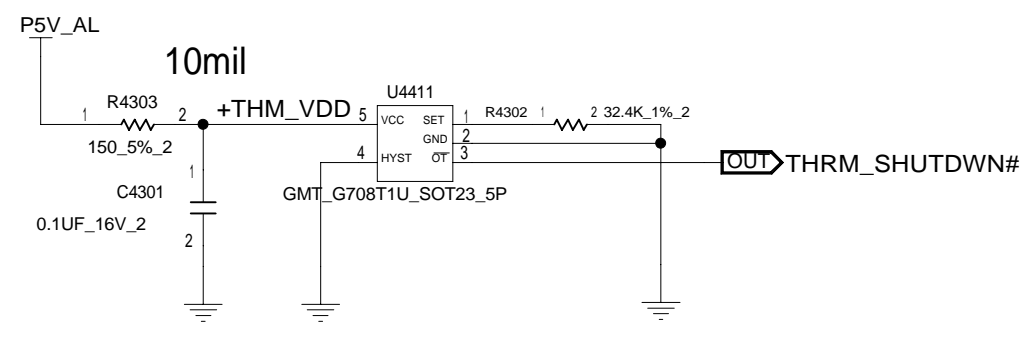
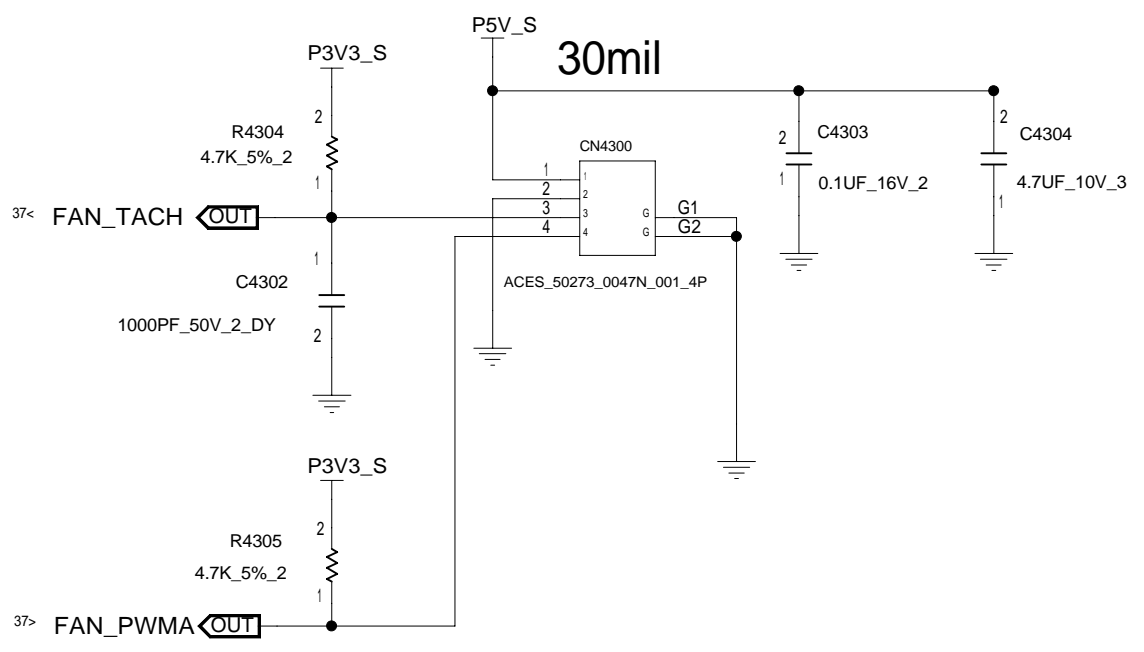
A

D

C

B

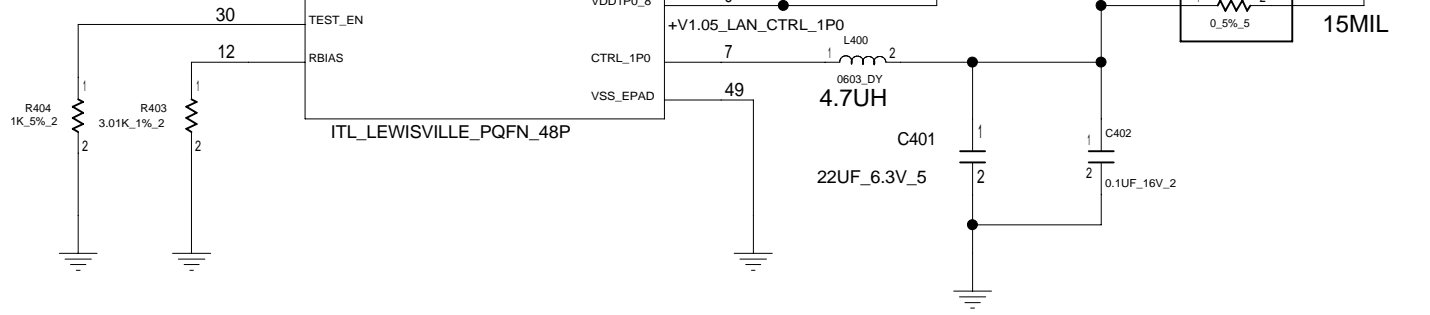
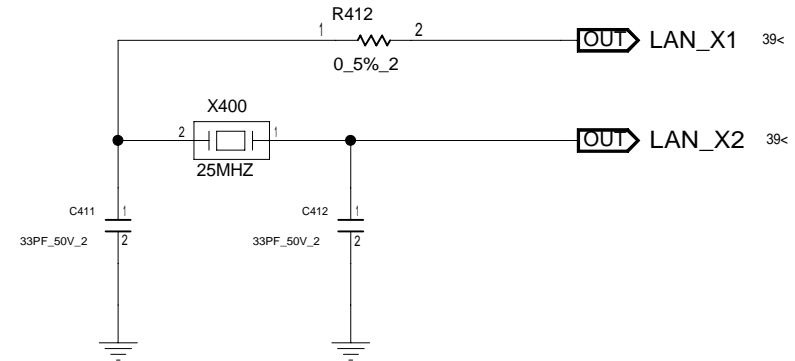
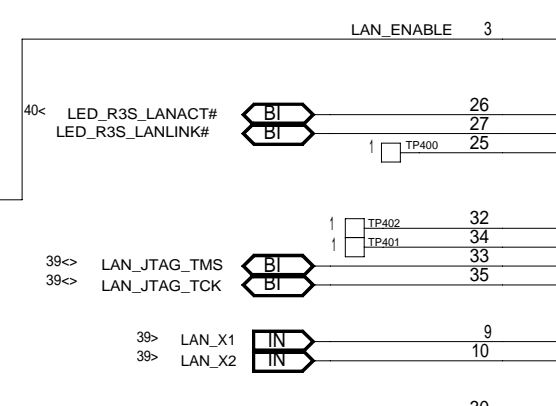
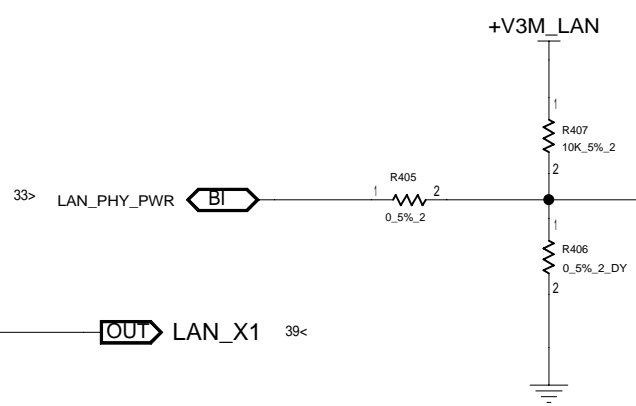
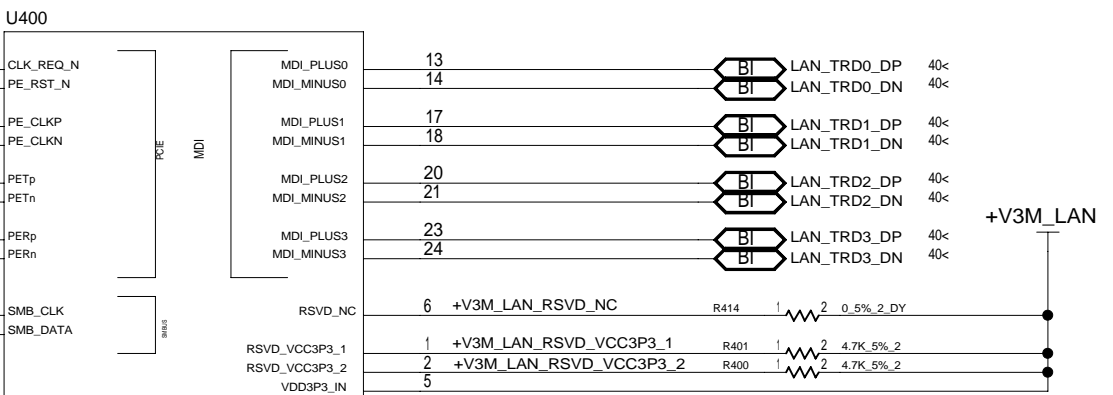
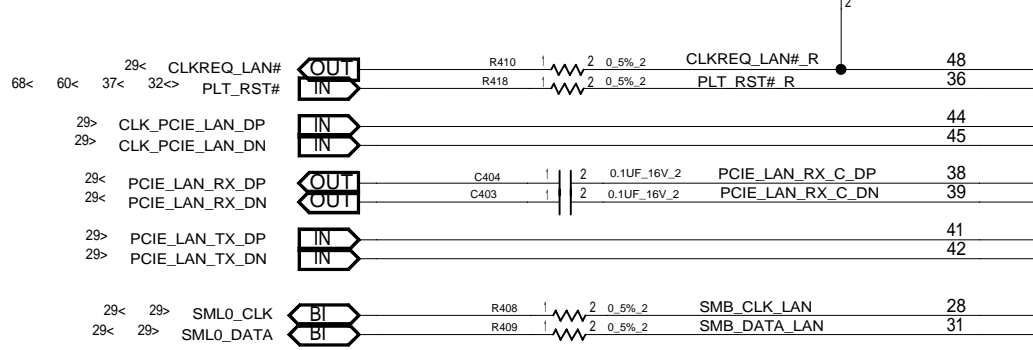
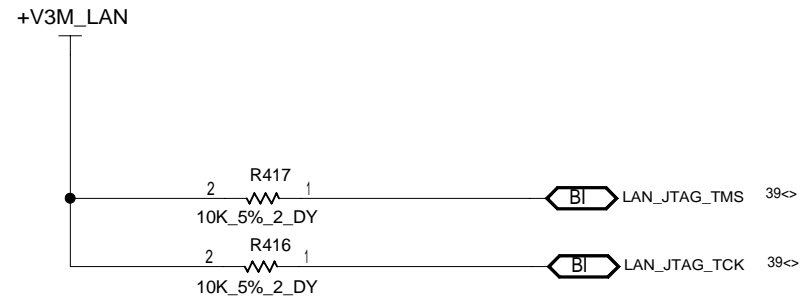
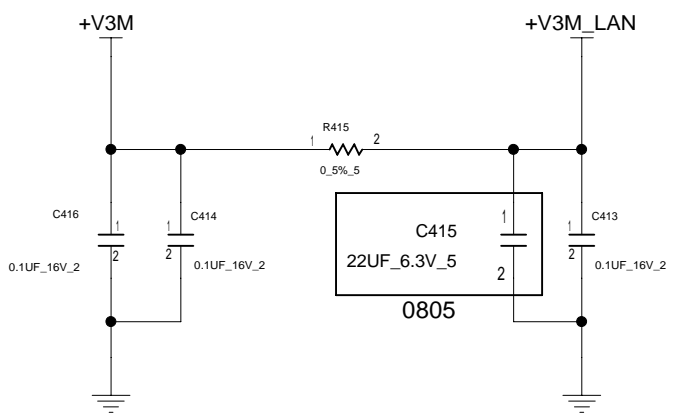
A



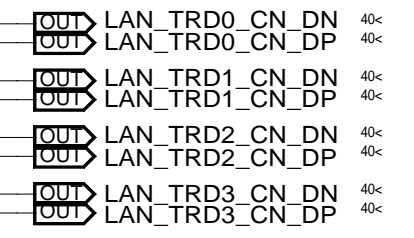
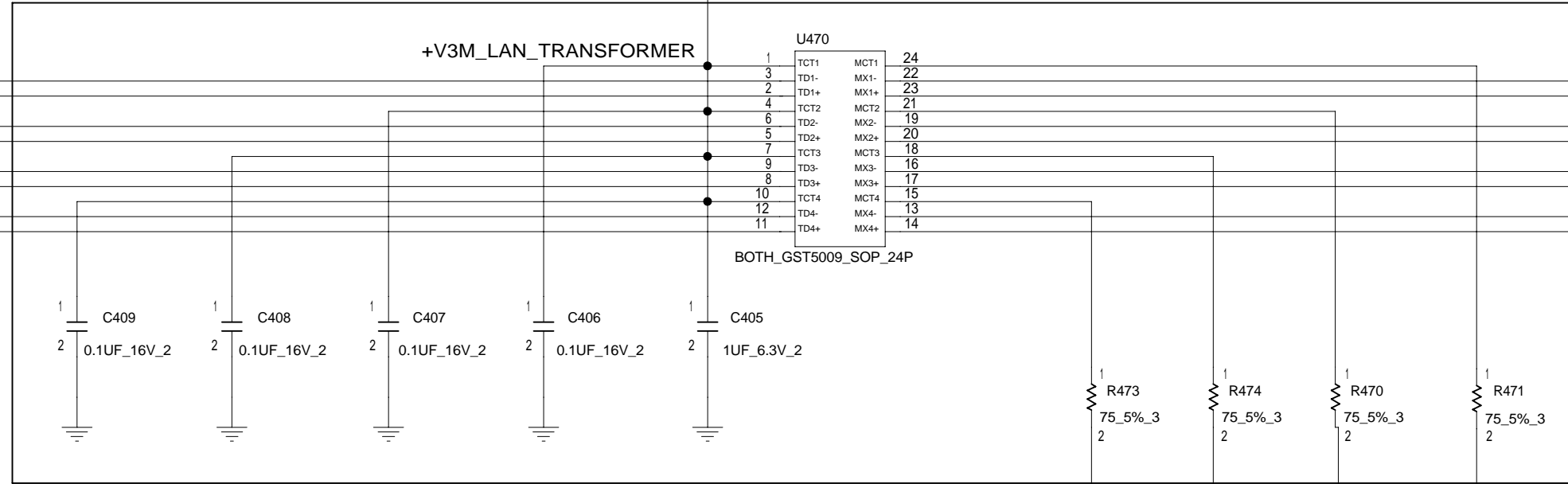
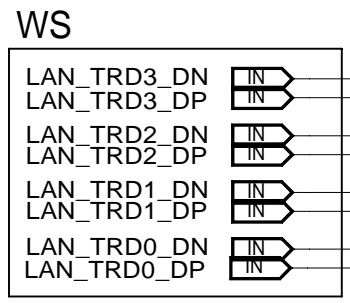
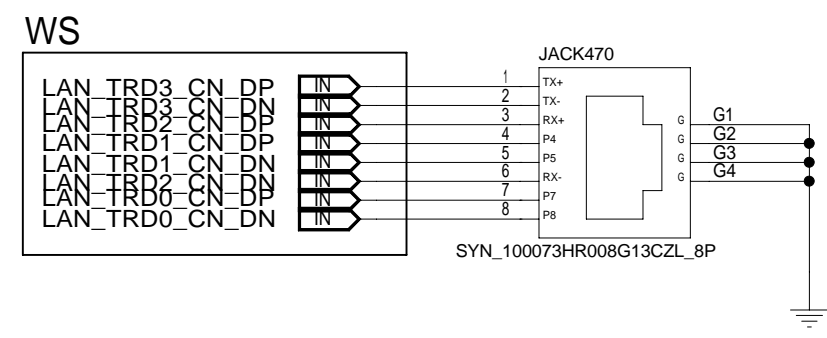
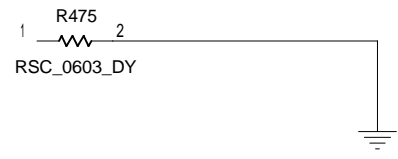
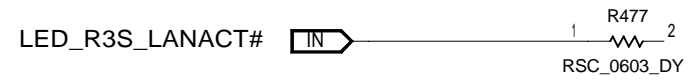
GM Thermal shutdown at 80.8°C +/-3°C from 60°C to 100°C
 PM Thermal shutdown at 86°C +/-3°C from 60°C to 100°C
 $RSET=0.0012*T^2-0.9308*T+96.147$
 Hysteresis is 30C

INVENTEC			
TITLE EVEREST-M FAN & THERMAL			
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01

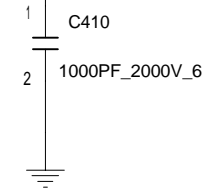
30MIL



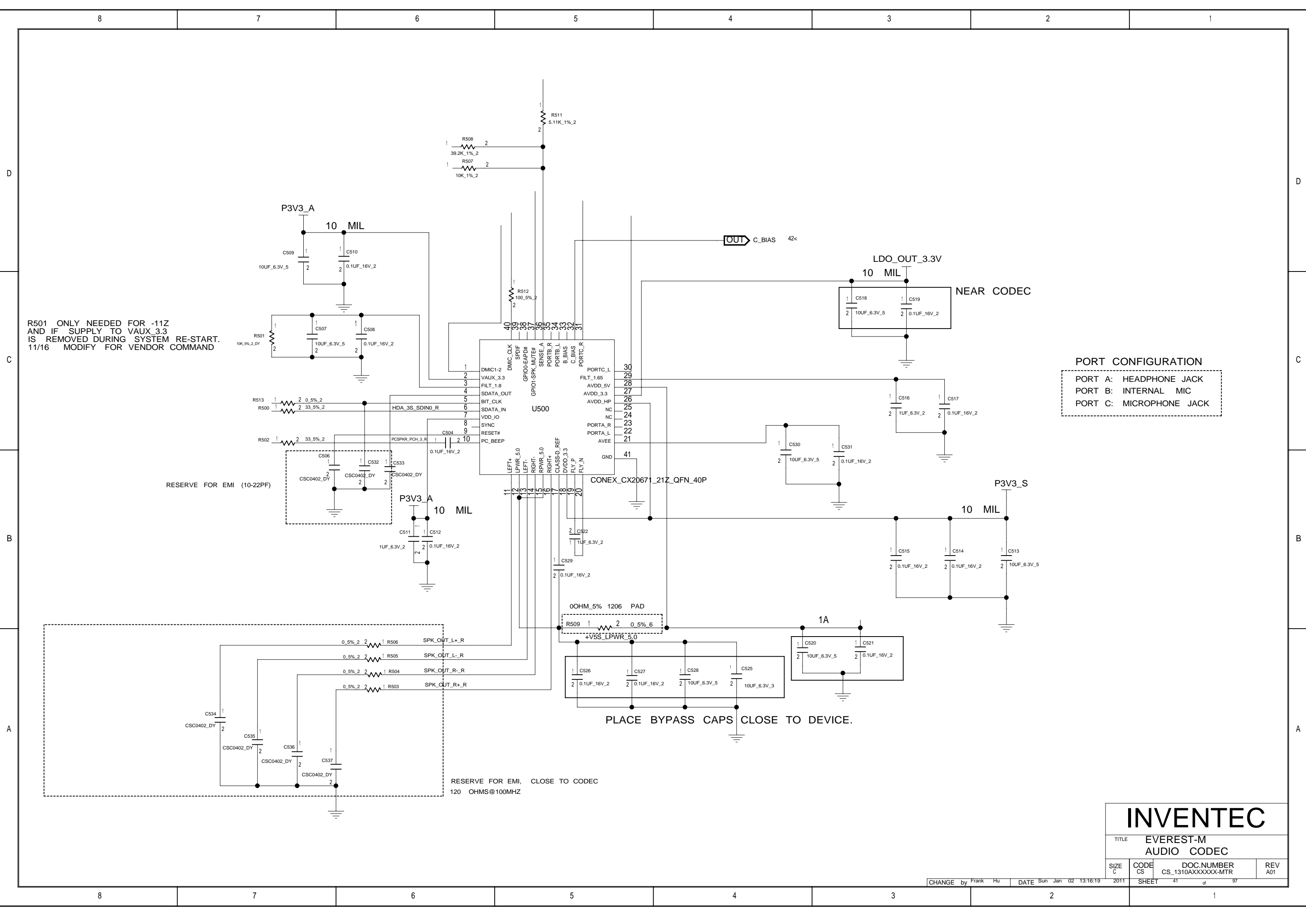
INVENTEC			
TITLE EVEREST-M LAN			
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01



8152 OPEN



INVENTEC			
TITLE EVEREST-M RJ45 & TRANSFORMER			
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01
CHANGE by Frank Hu		DATE Tue Jan 04 00:15:14 2011	SHEET 40 of 97



R501 ONLY NEEDED FOR -11Z
AND IF SUPPLY TO VAUX_3.3
IS REMOVED DURING SYSTEM RE-START.
11/16 MODIFY FOR VENDOR COMMAND

RESERVE FOR EMI (10-22PF)

RESERVE FOR EMI, CLOSE TO CODEC
120 OHMS@100MHZ

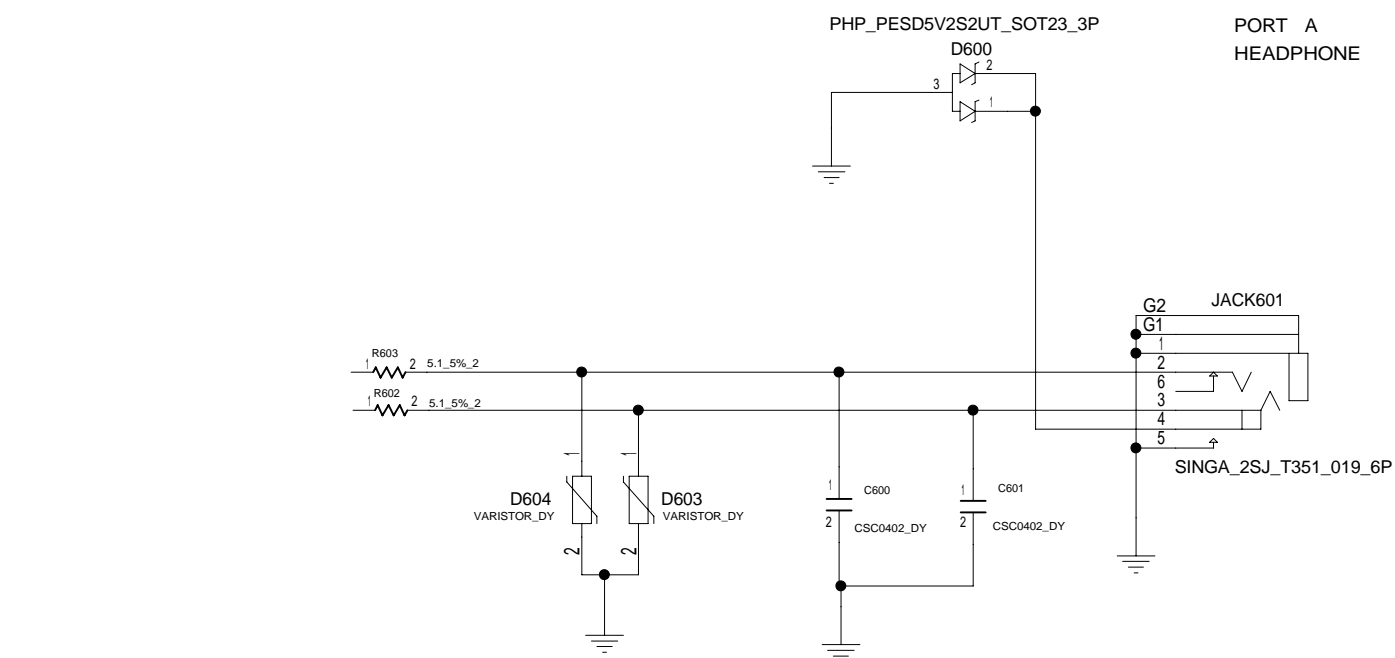
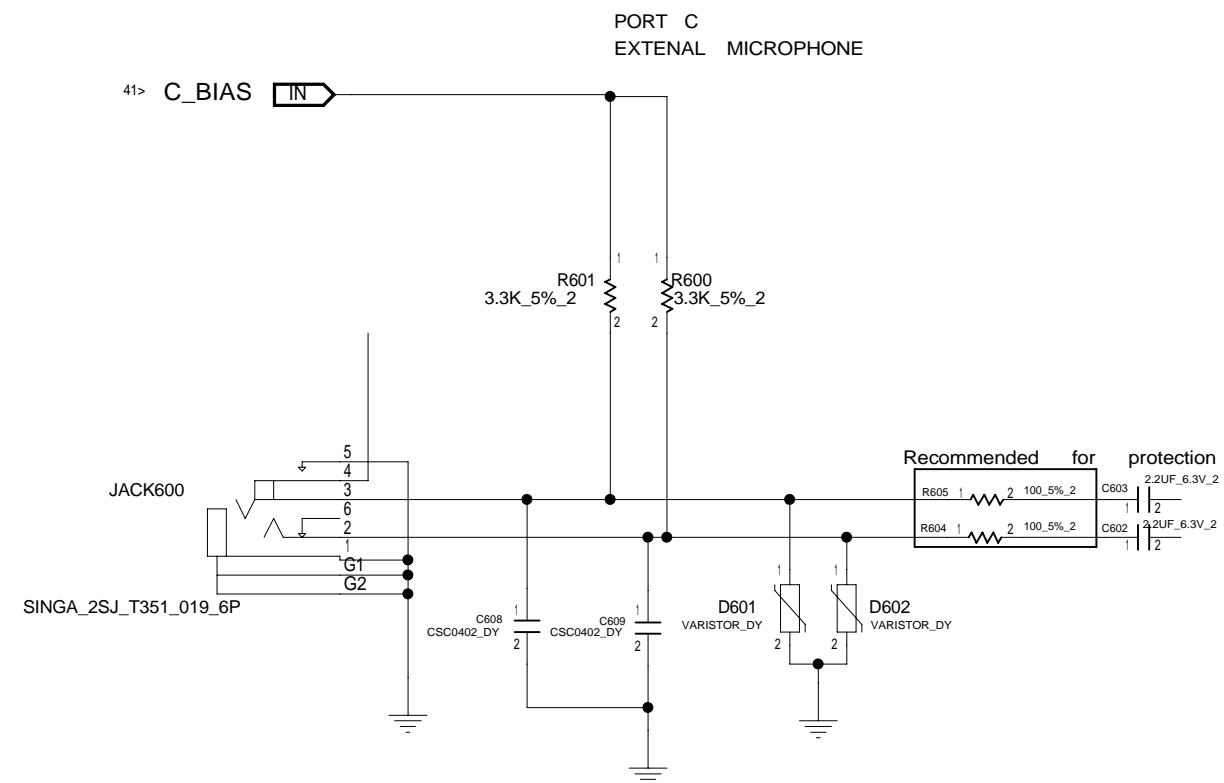
PLACE BYPASS CAPS CLOSE TO DEVICE.

PORT CONFIGURATION

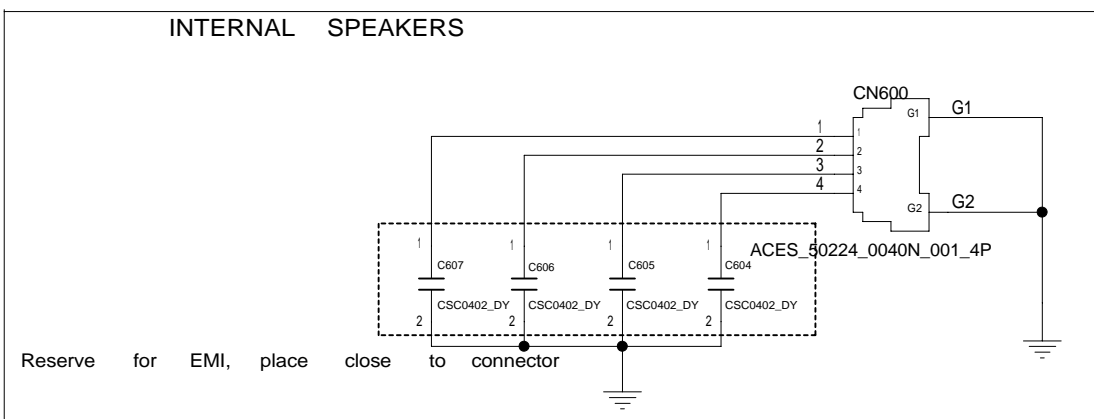
PORT A:	HEADPHONE JACK
PORT B:	INTERNAL MIC
PORT C:	MICROPHONE JACK

INVENTEC			
TITLE EVEREST-M AUDIO CODEC			
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01
CHANGE by Frank Hu		DATE Sun Jan 02 13:16:19 2011	SHEET 41 of 97

AUDIO JACKS

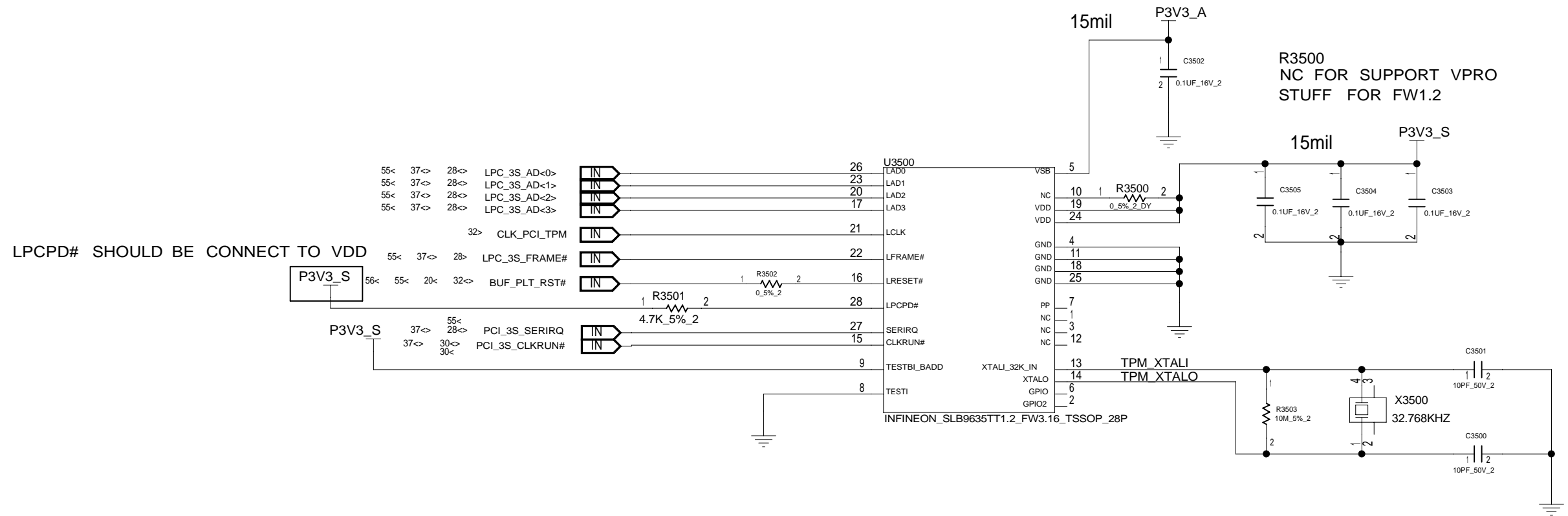


INTERNAL SPEAKERS



INVENTEC

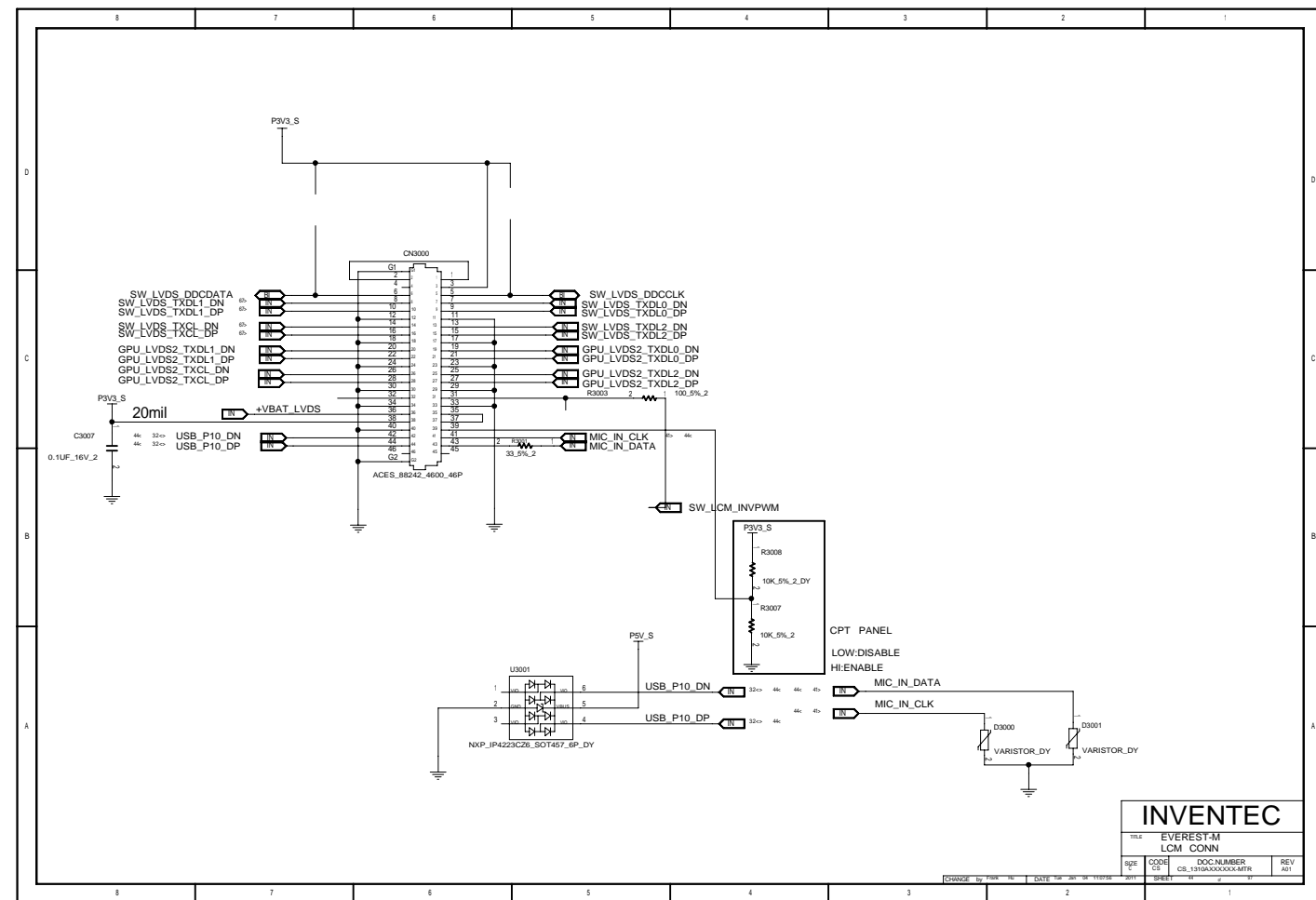
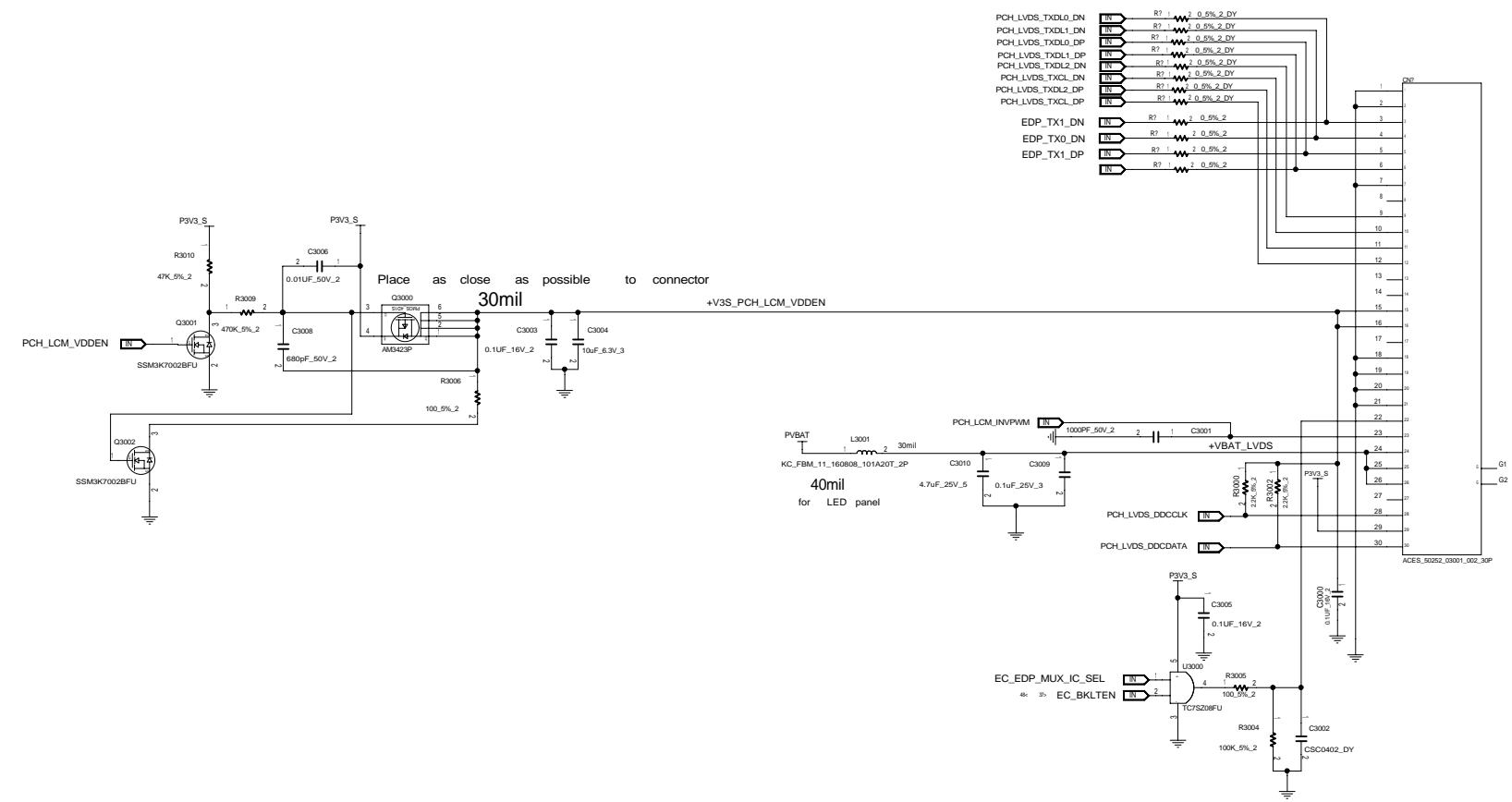
TITLE				EVEREST-M AUDIO AMP
SIZE	CODE	DOC.NUMBER	REV	
C	CS	CS_1310AXXXXX-MTR	A01	

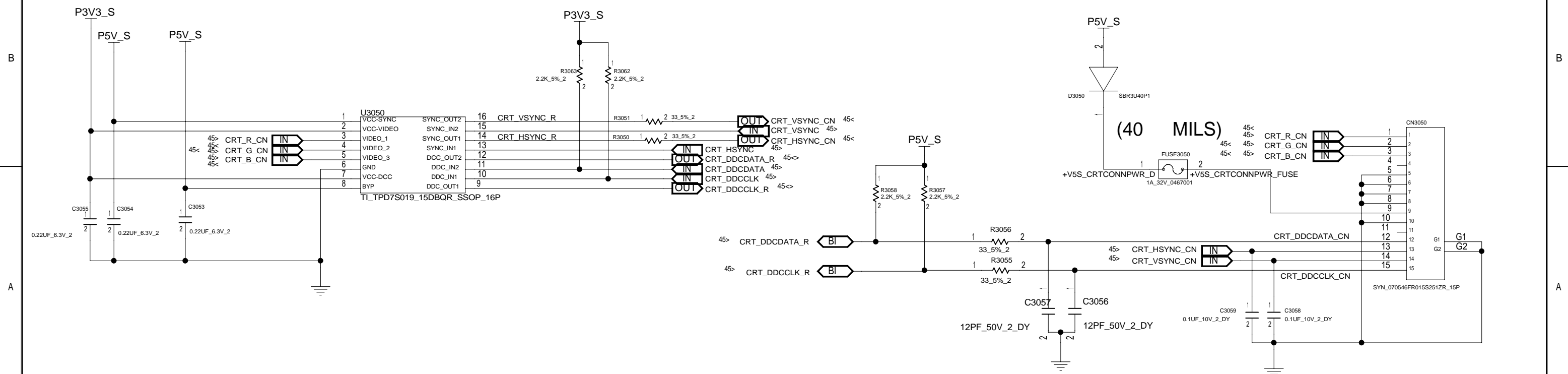
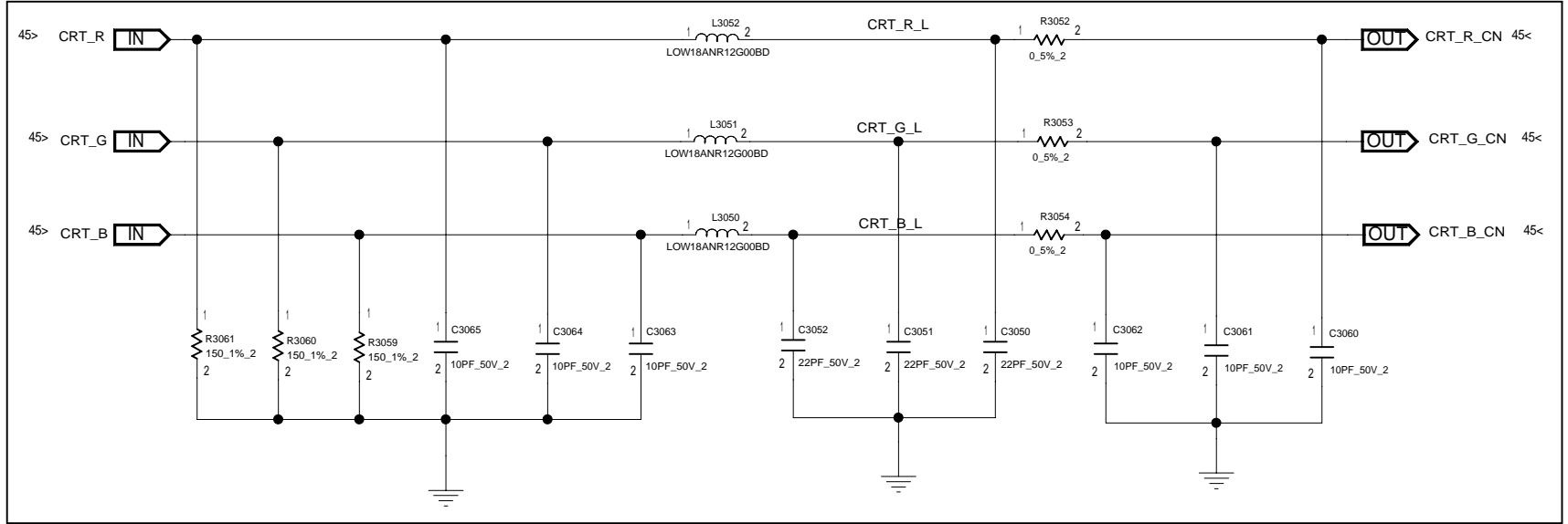
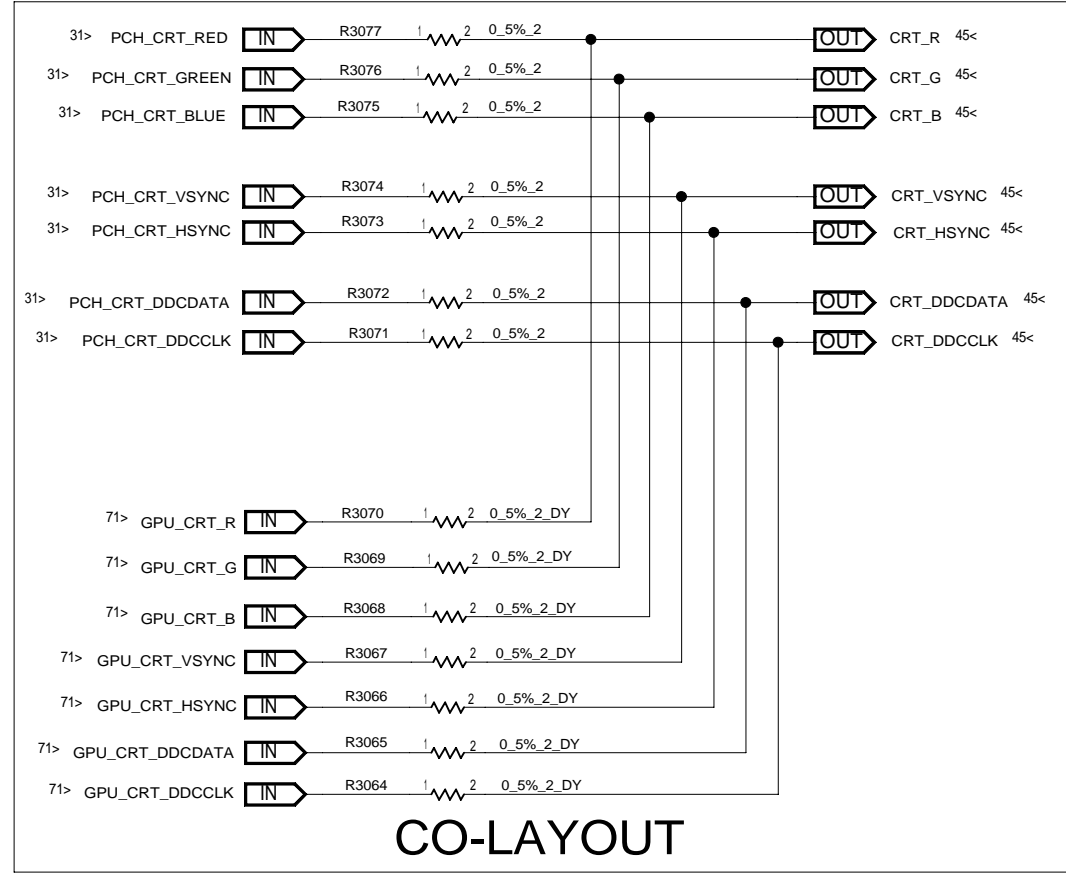


TPM1.2

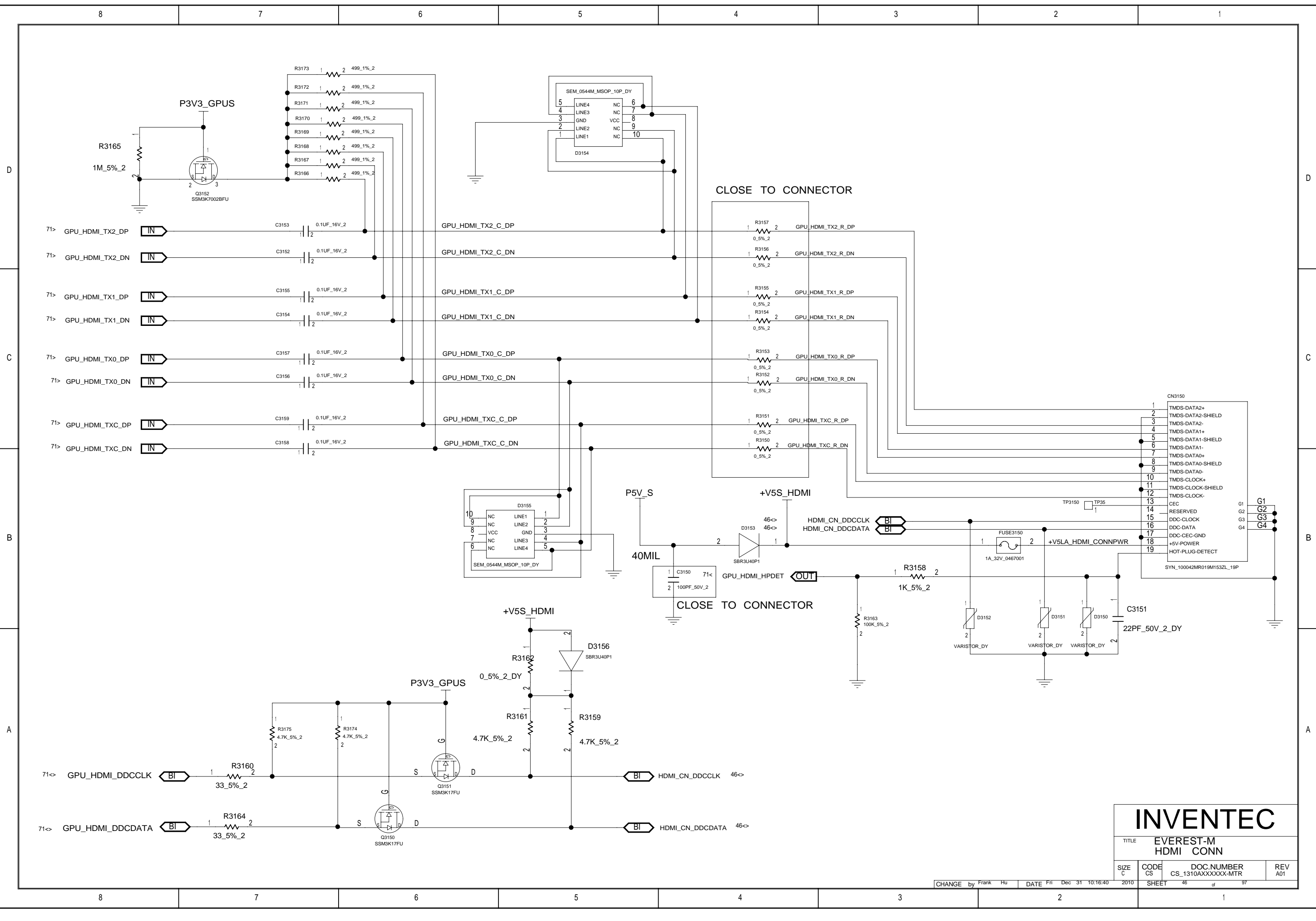
FW VERSION	P/N
1.02	6019B0101801
3.16	6019B0761601 (SUPPORT VPRO)

INVENTEC			
TITLE EVEREST-M TPM			
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01

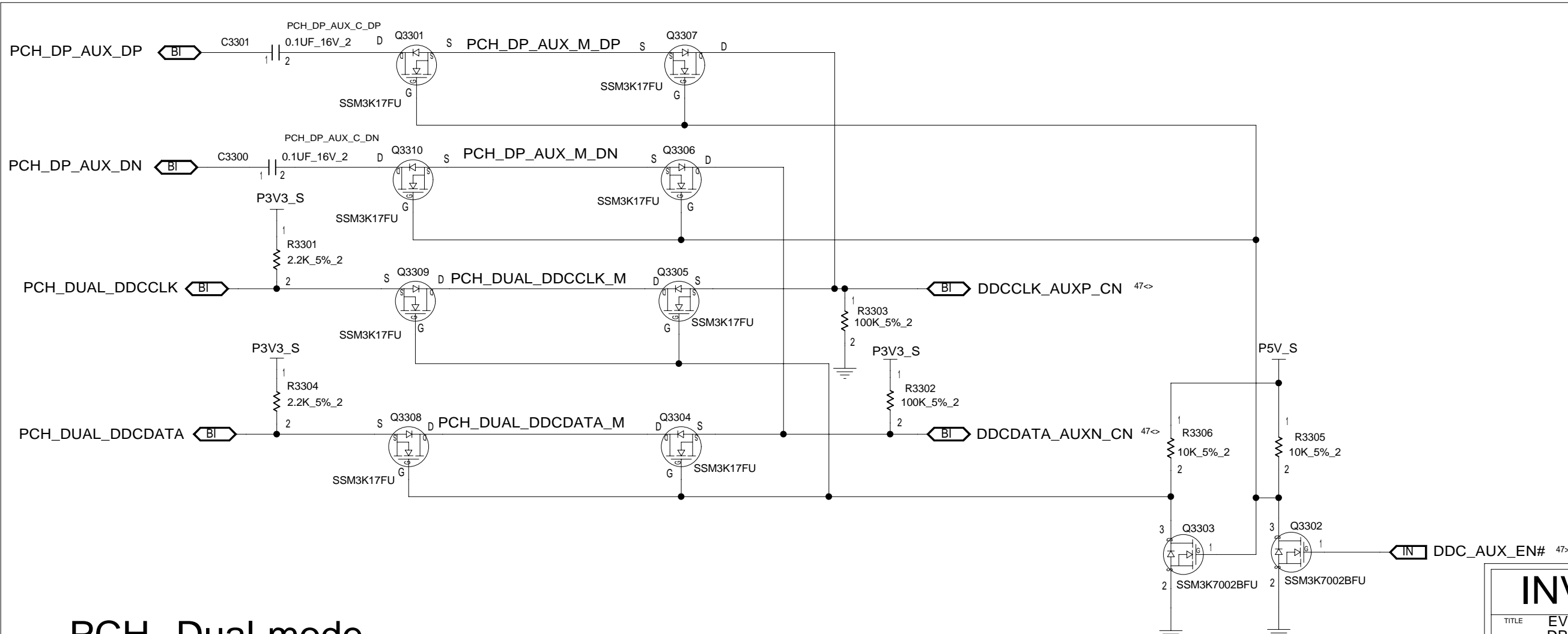
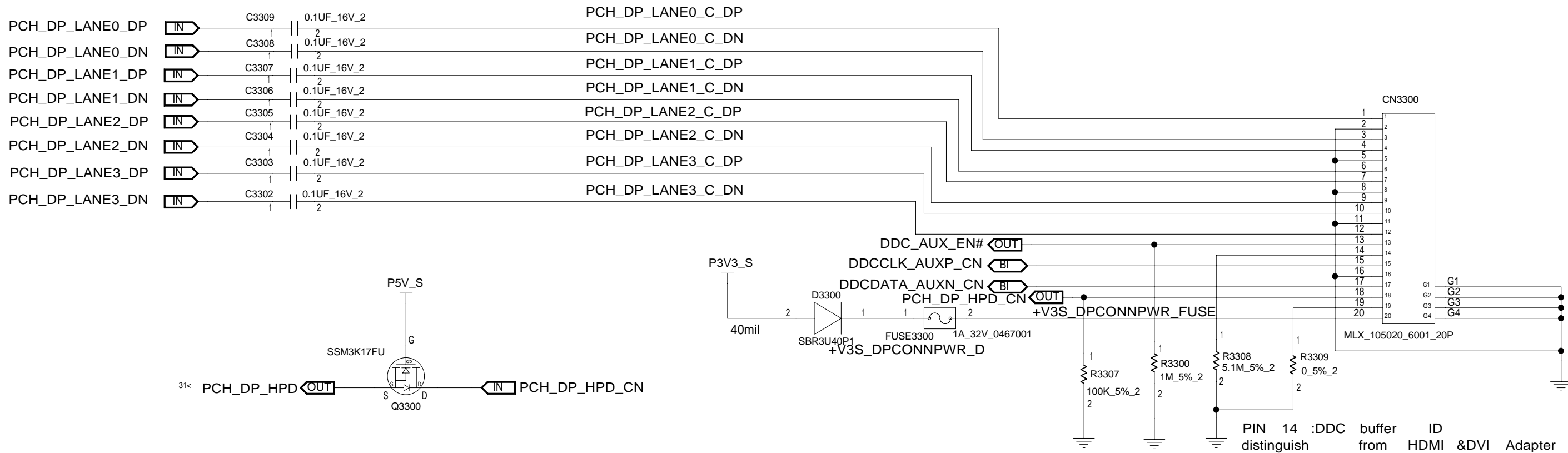




INVENTEC				
TITLE EVEREST-M CRT CONN				
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01	

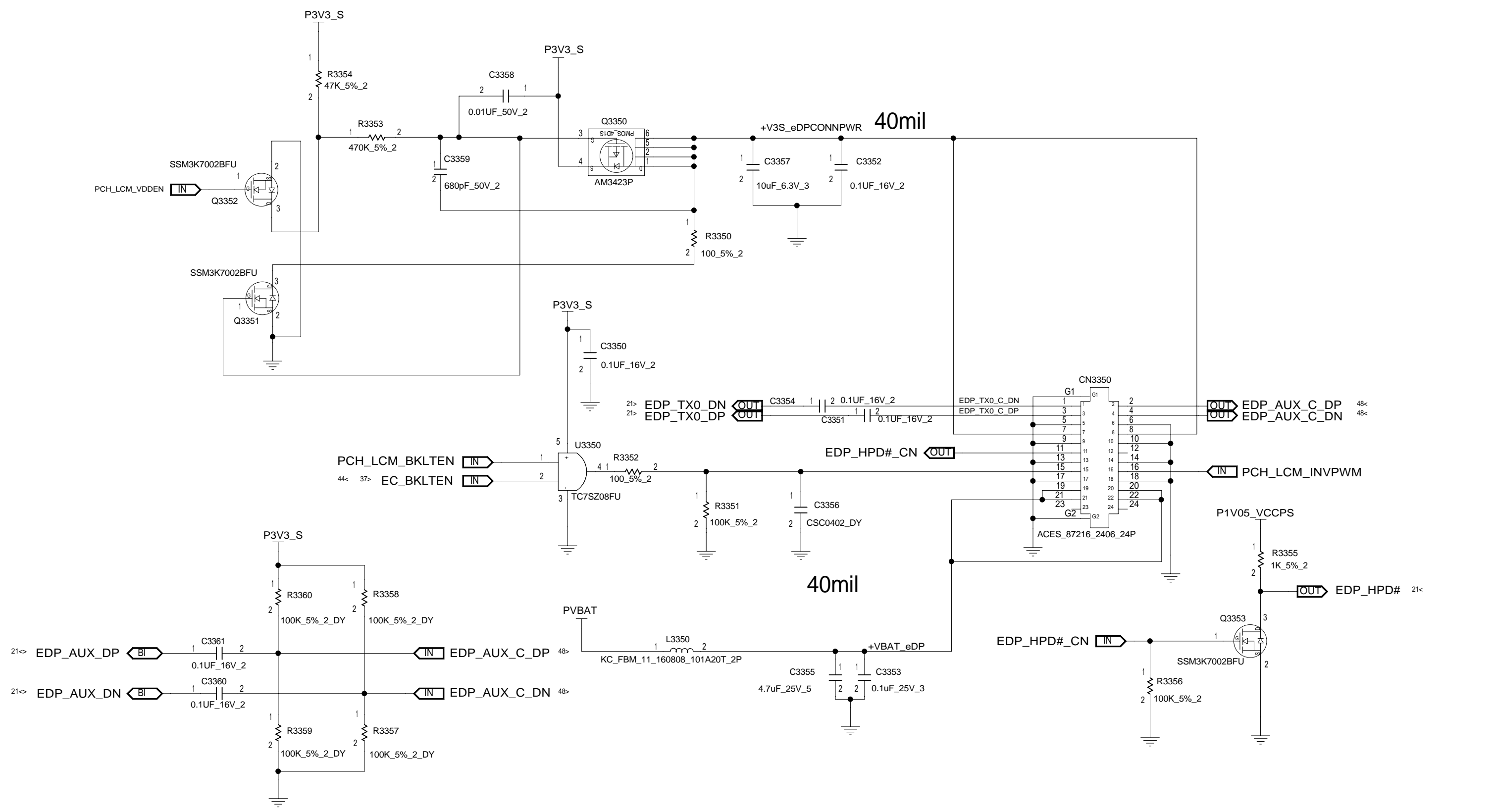


INVENTEC				
TITLE EVEREST-M HDMI CONN				
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01	
CHANGE by Frank Hu		DATE Fri Dec 31 10:16:40	2010	SHEET 46 of 97



PCH Dual-mode

INVENTEC			
TITLE EVEREST-M DP CONN			
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01



INVENTEC				
TITLE EVEREST-M EDP CONN				
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01	
CHANGE by Frank Hu		DATE Tue Jan 04 11:08:43	2011	SHEET 48 of 97

D

D

C

C

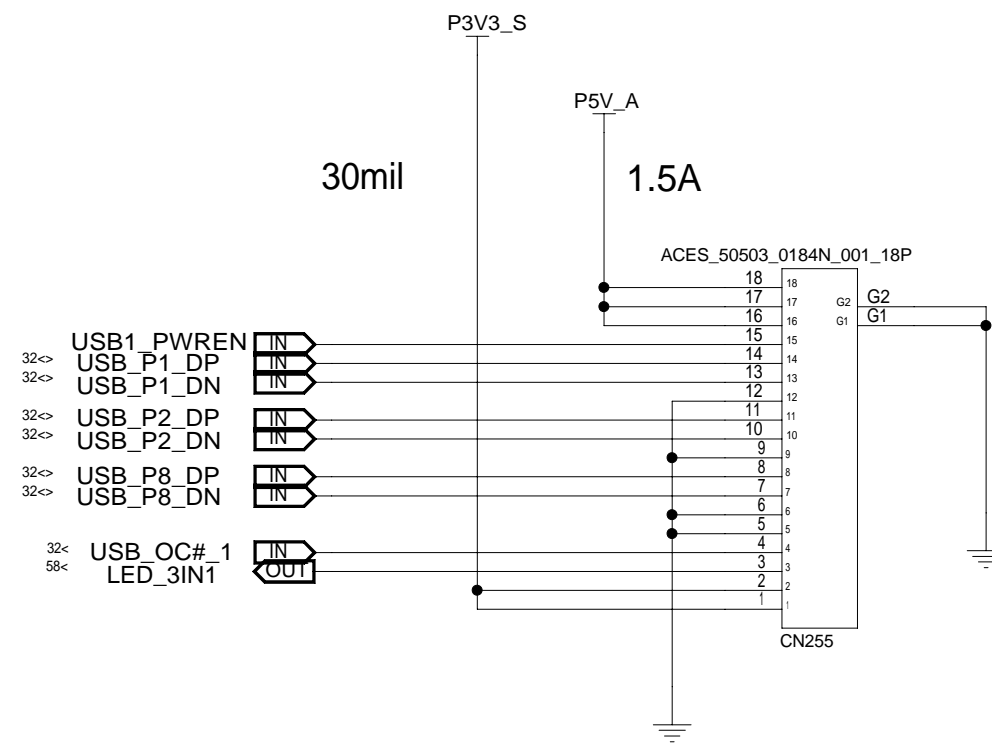
B

B

A

A

CARDREADER/USB CONNECTOR



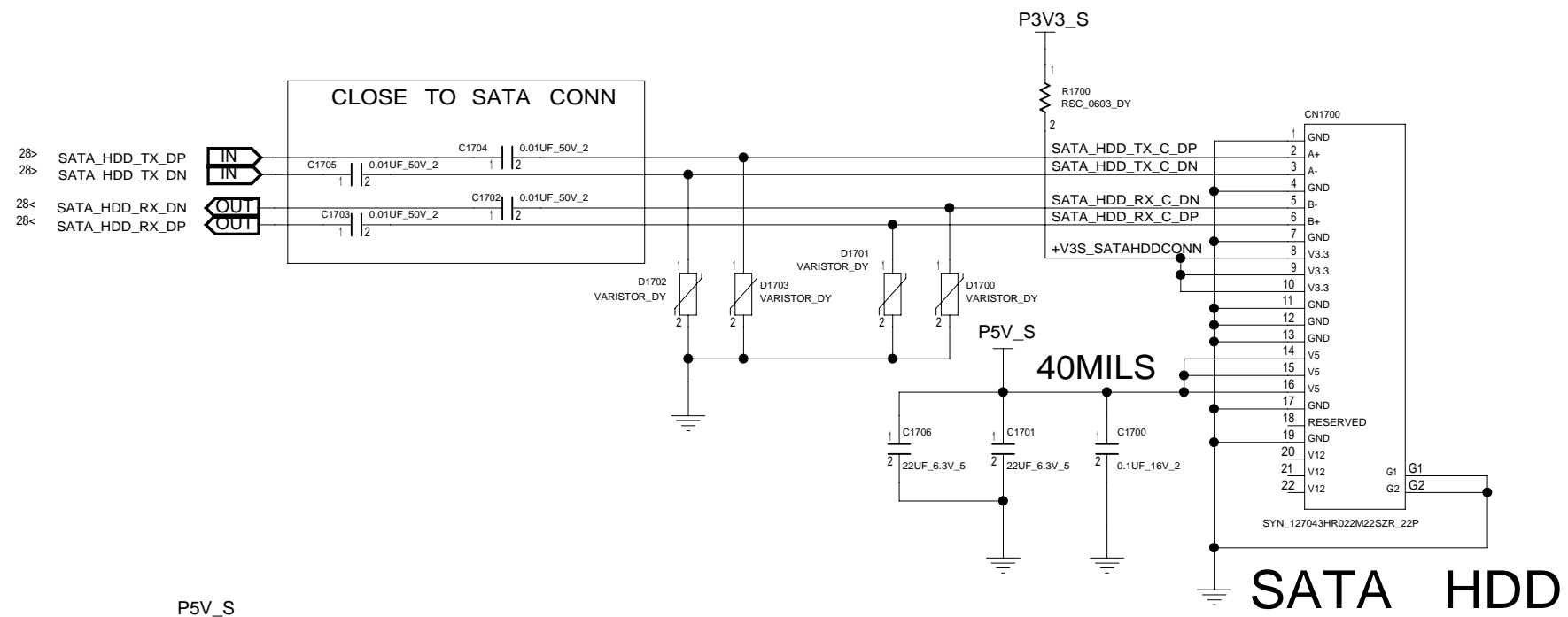
INVENTEC			
TITLE EVEREST-M			
DB CONN USB & CARDREADER			
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01

D

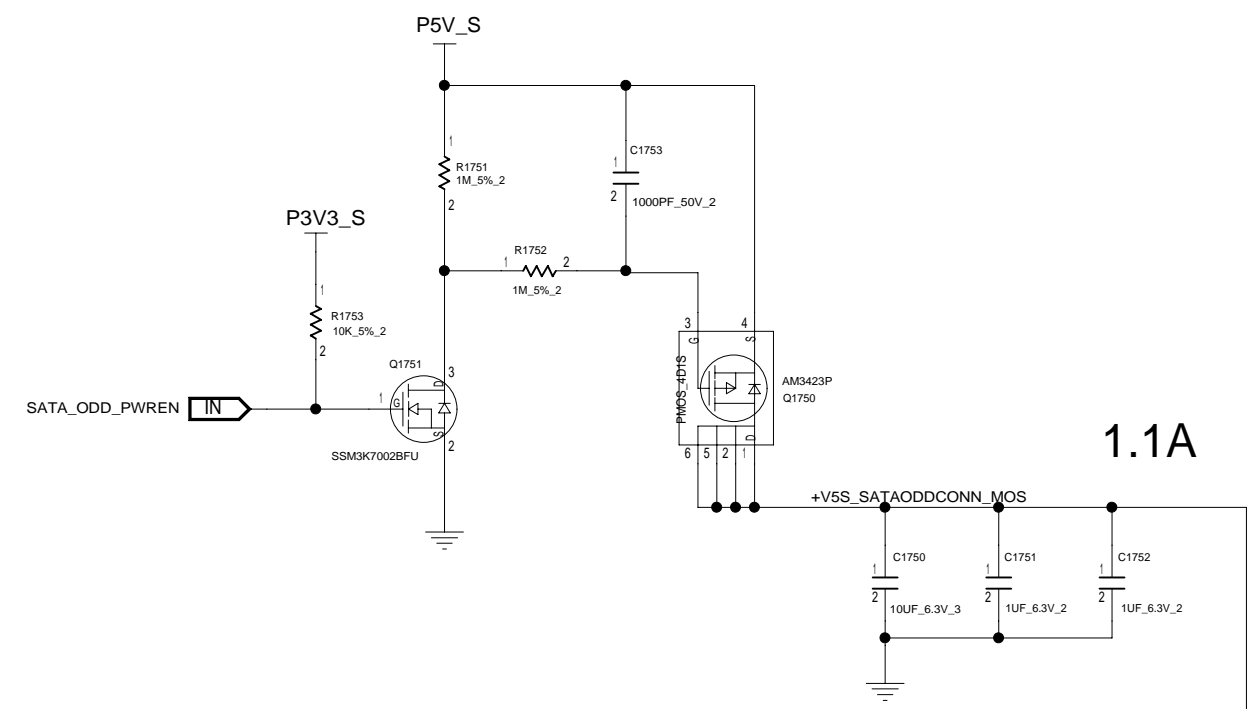
C

B

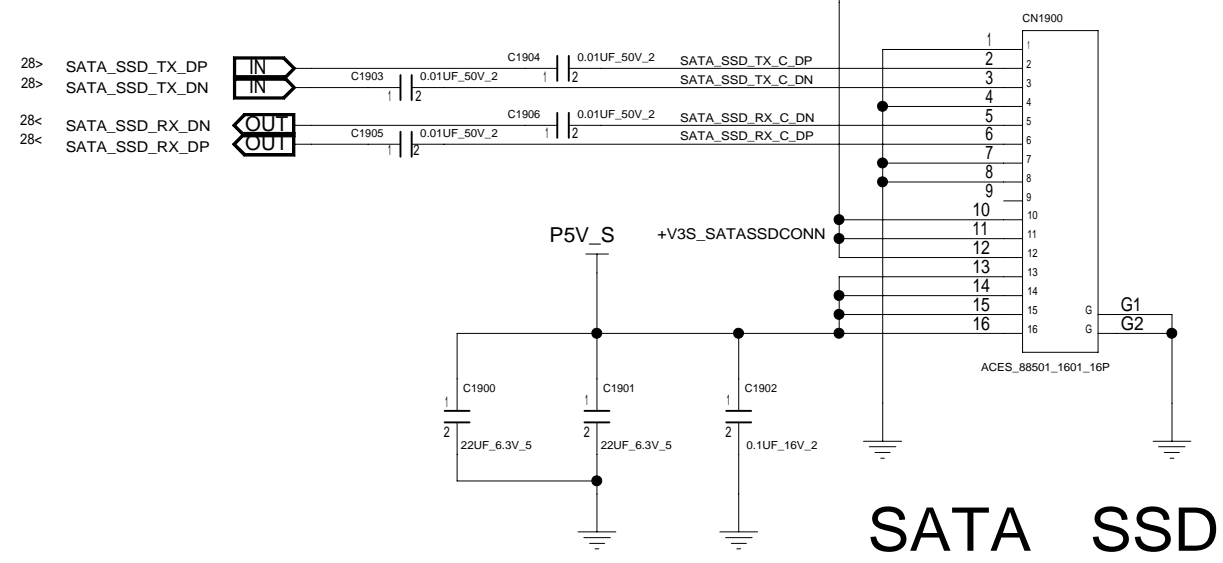
A



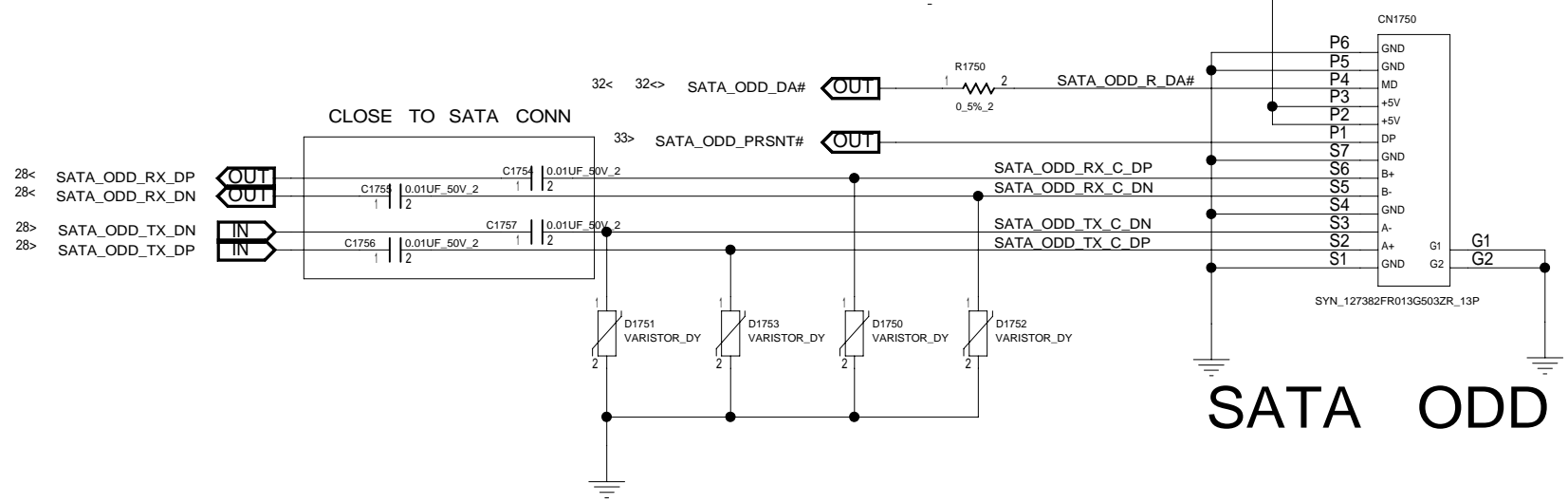
SATA HDD



SATA ODD

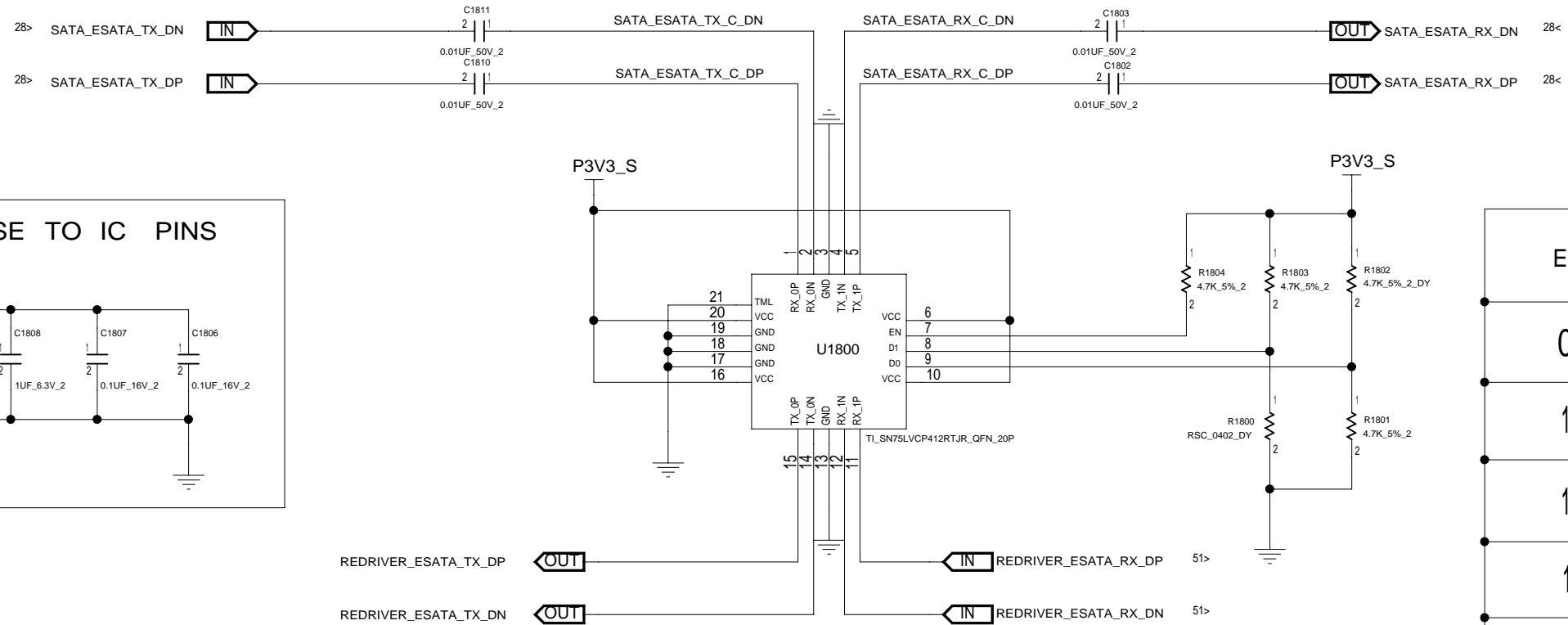


SATA SSD

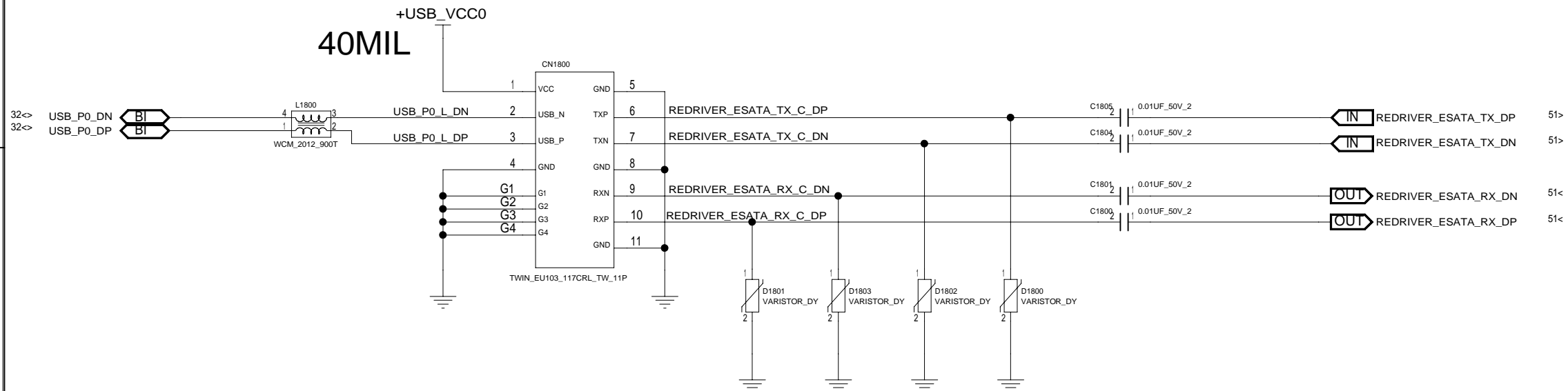


INVENTEC				
TITLE EVEREST-M SATA HDD/SSD & ODD CONN				
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01	
CHANGE by Frank Hu DATE Sun Jan 02 18:54:06 2011 SHEET 50 of 97				

E-SATA



EN	D0	D1	FUNCTION
0	X	X	STANDBY
1	0	0	DEFAULT
1	1	0	CH0->5DB
1	0	1	CH1->5DB
1	1	1	CH0,1->5DB



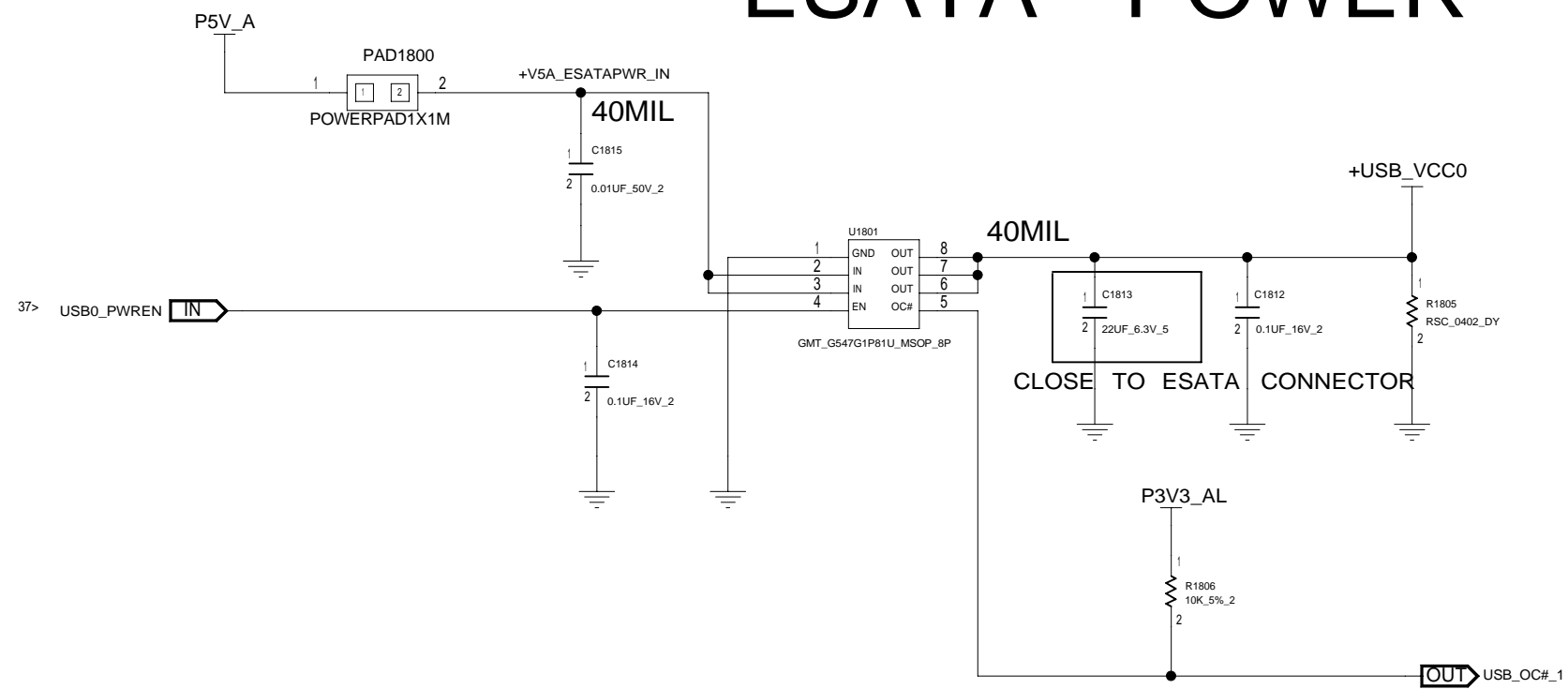
INVENTEC

TITLE EVEREST-M
E-SATA CONN

SIZE C CODE CS DOC.NUMBER CS_1310AXXXXX-MTR REV A01

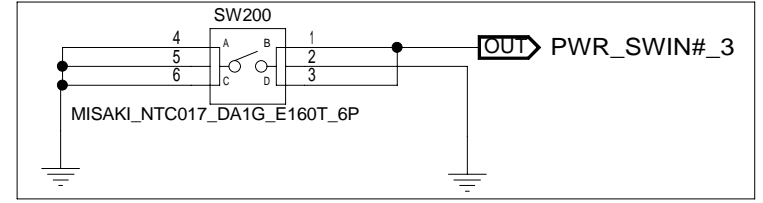
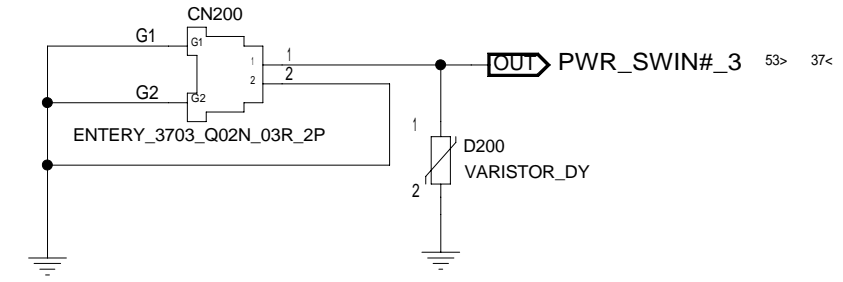
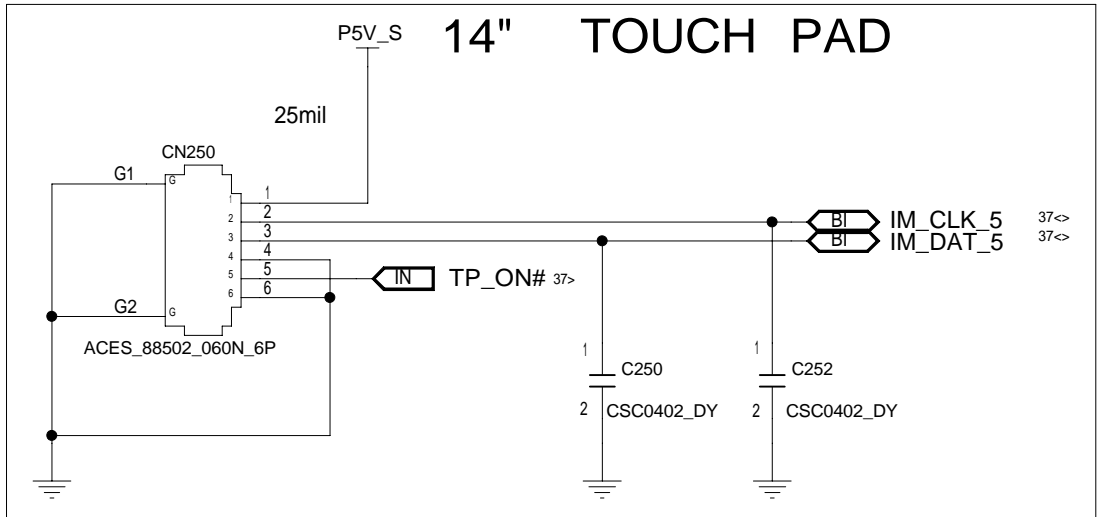
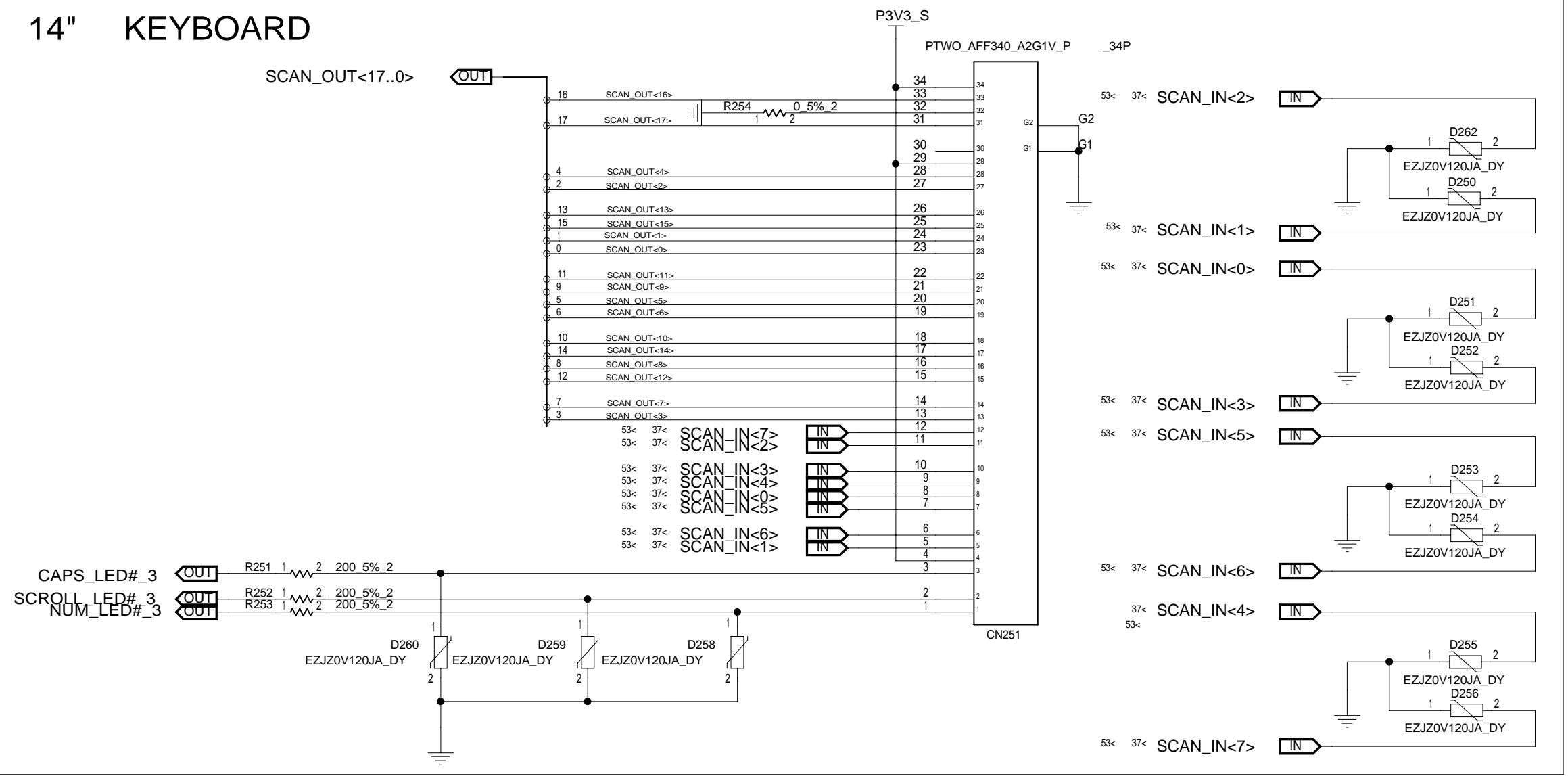
CHANGE by Frank Hu DATE Fri Dec 31 10:16:42 2010 SHEET 51 of 97

ESATA POWER



INVENTEC			
TITLE EVEREST-M USB CONN			
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01

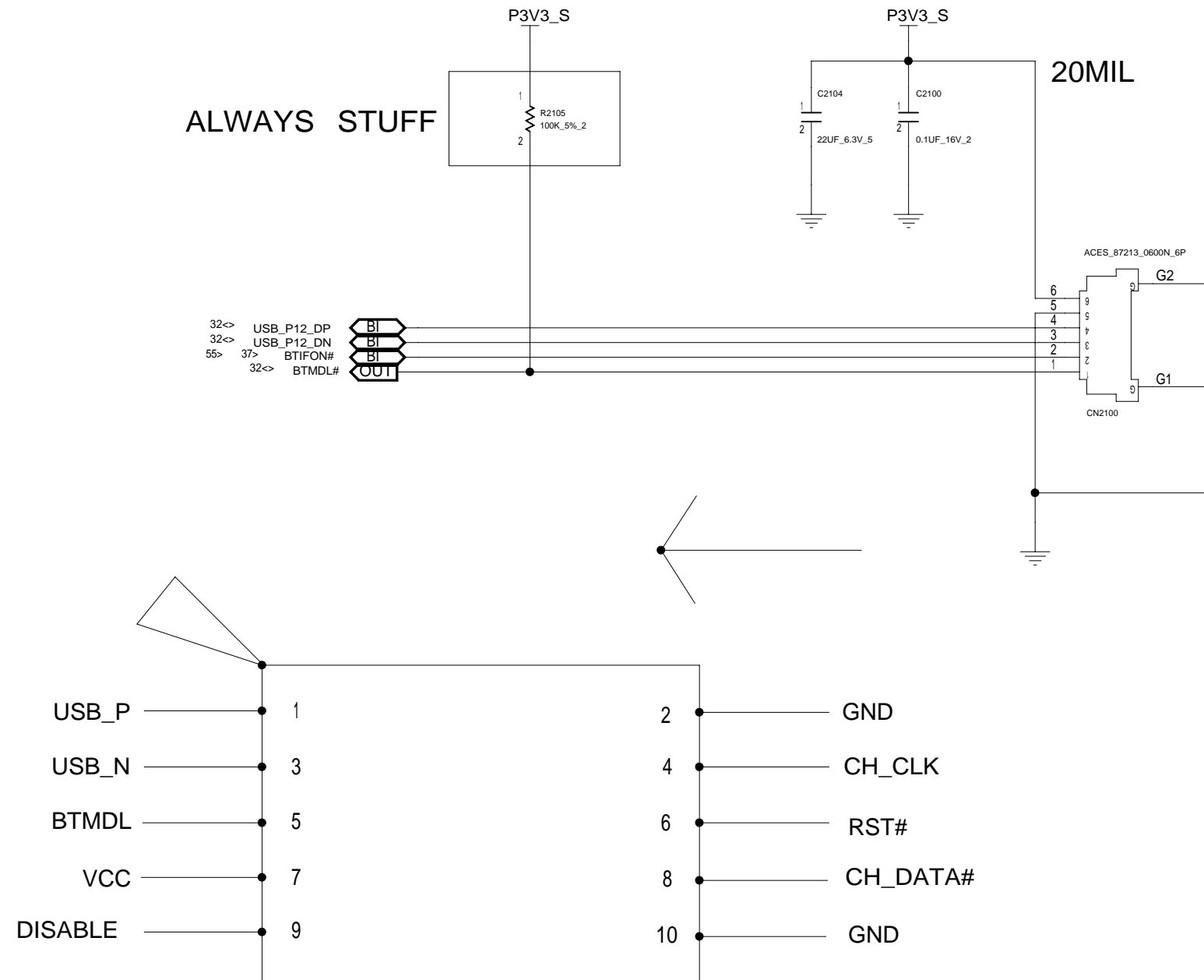
14" KEYBOARD



PUT ON BOTTOM SIDE

INVENTEC				
TITLE EVEREST-M K/B & TP/B CONN				
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01	
CHANGE by Frank Hu		DATE Fri Dec 31 10:16:43	2010	SHEET 53 of 97

BLUETOOTH



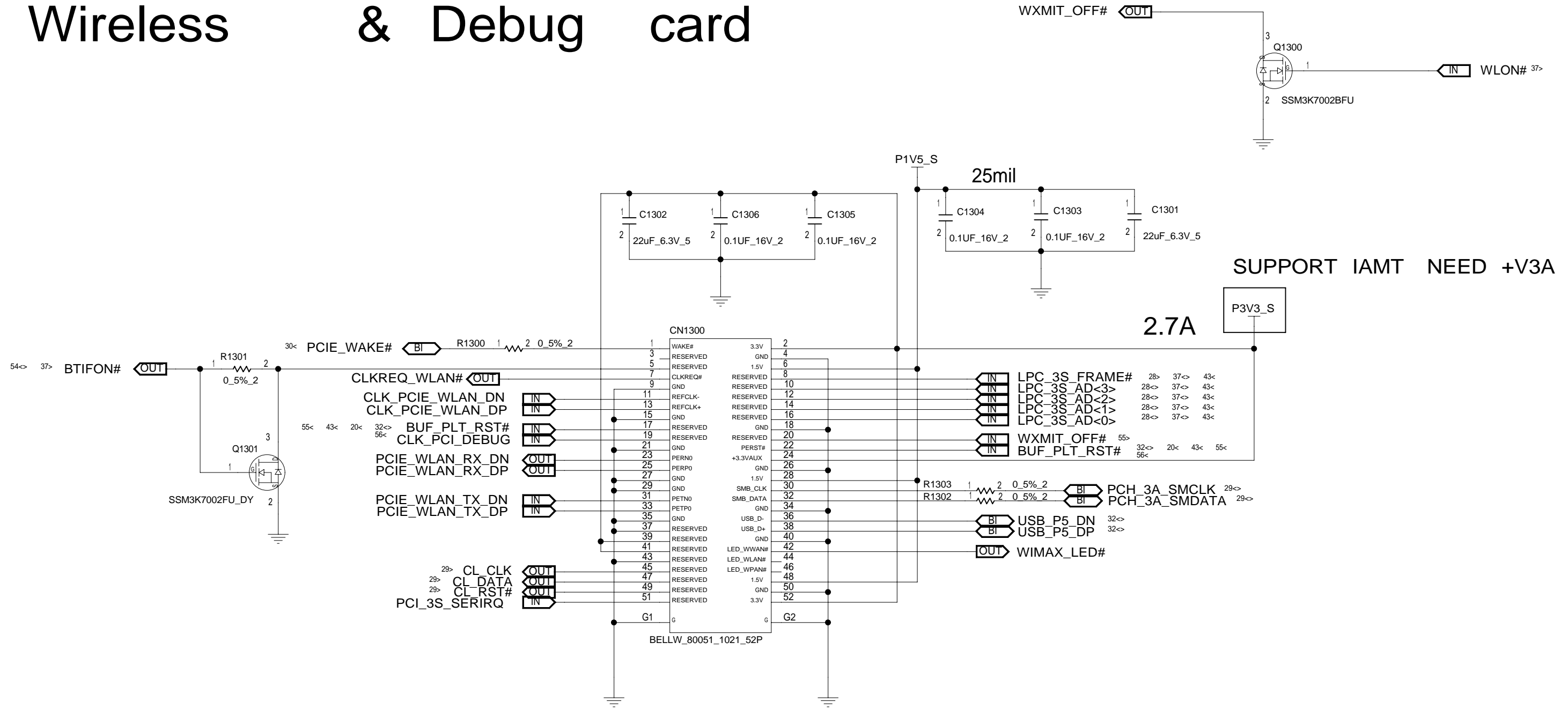
INVENTEC

TITLE EVEREST-M
BLUETOOTH CONN

SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01
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Wireless & Debug card



SUPPORT IAMT NEED +V3A

2.7A

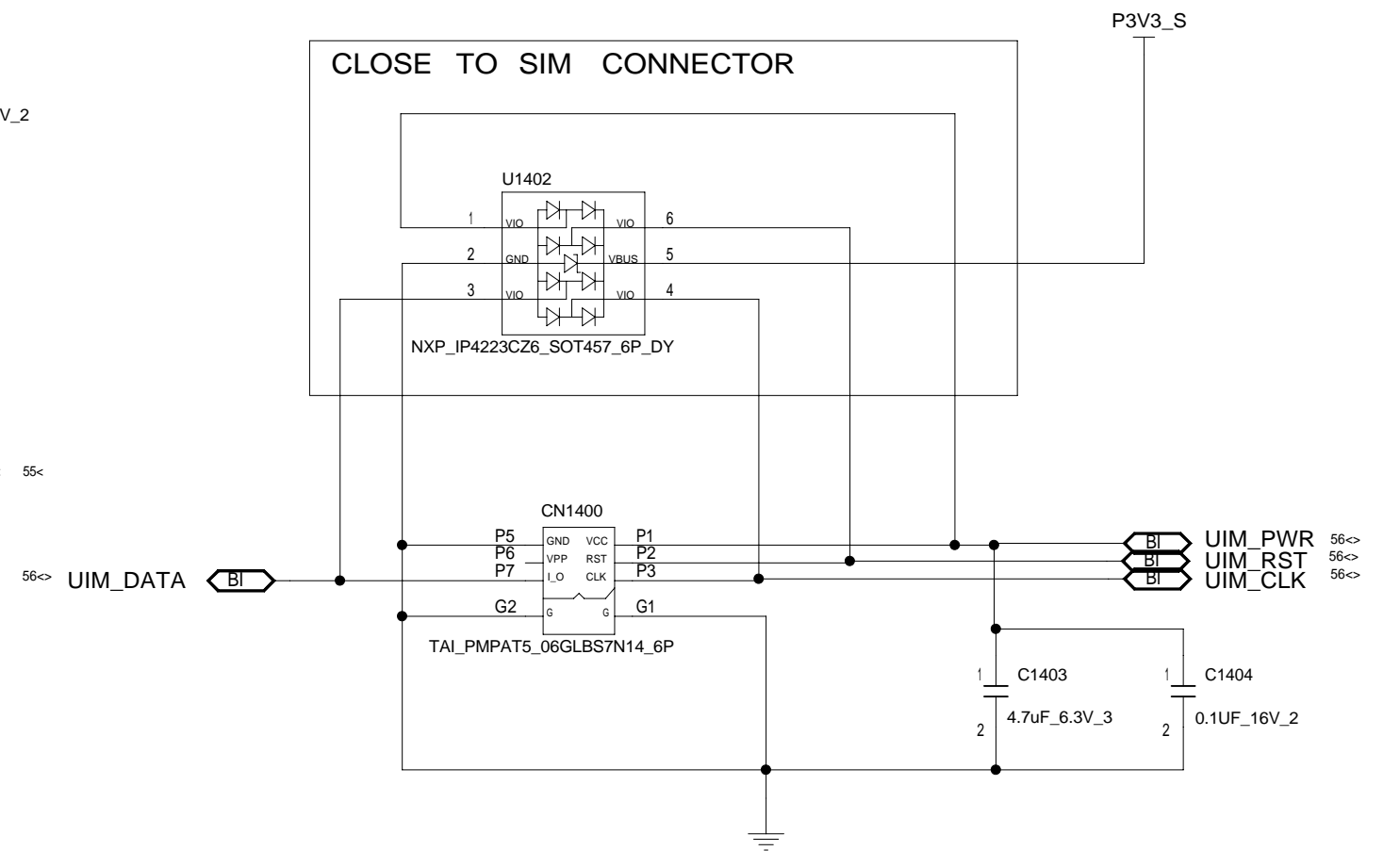
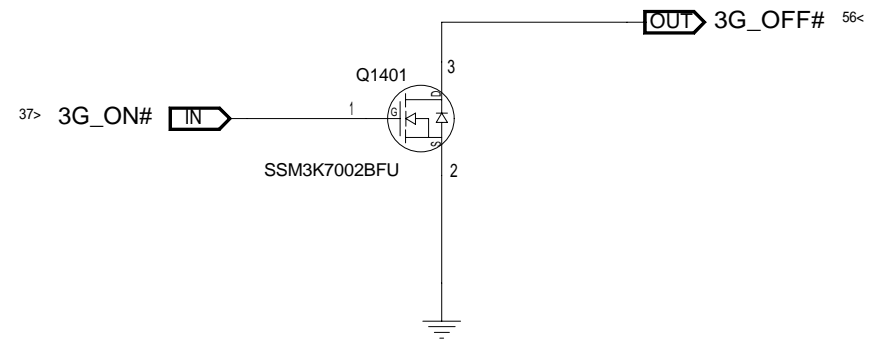
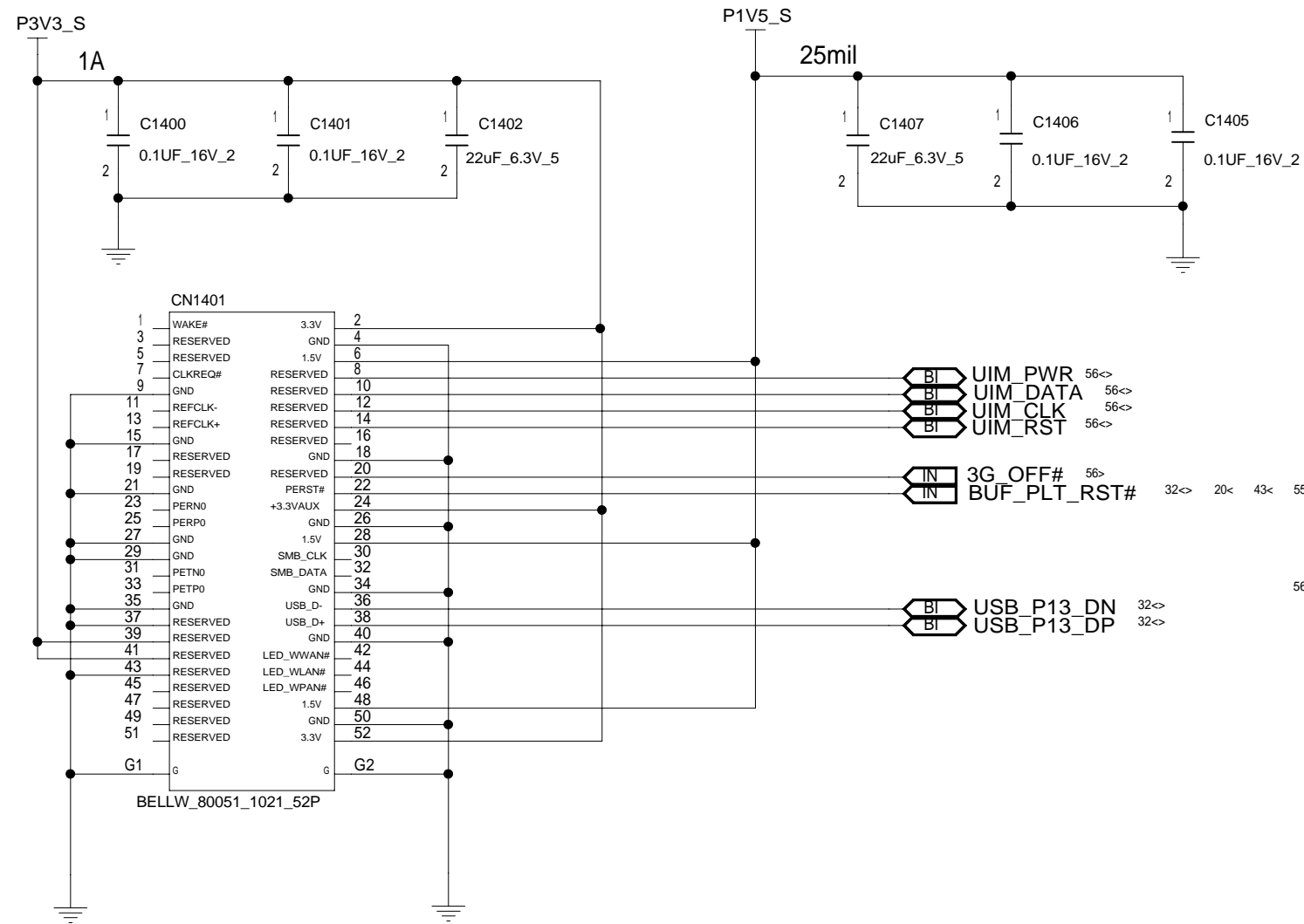
MINI CARD 1

Note:

	Peak(max)mA	Normal(max)mA
3.3V	2,750mA	1,100mA
1.5V	500mA	375mA

INVENTEC			
TITLE EVEREST-M			
MINI1 WLAN/DEBUG CARD			
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01

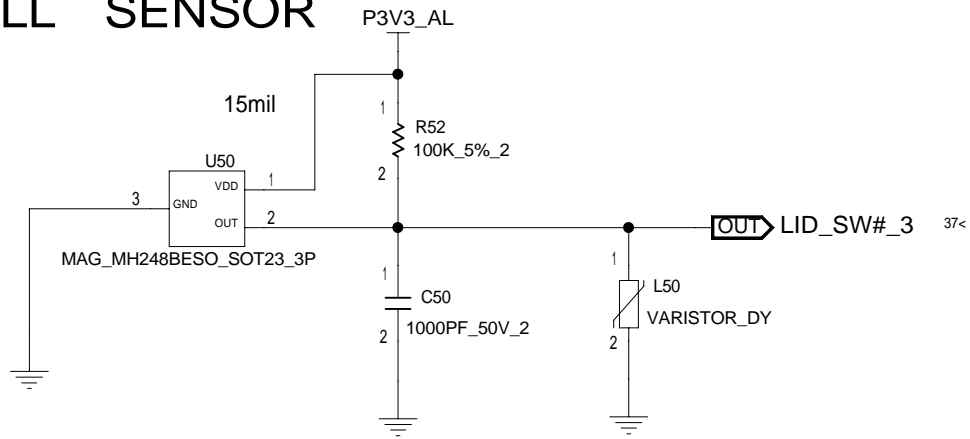
3G/GPS



MINI CARD 2

INVENTEC			
TITLE EVEREST-M MINI2 3G			
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01

HALL SENSOR

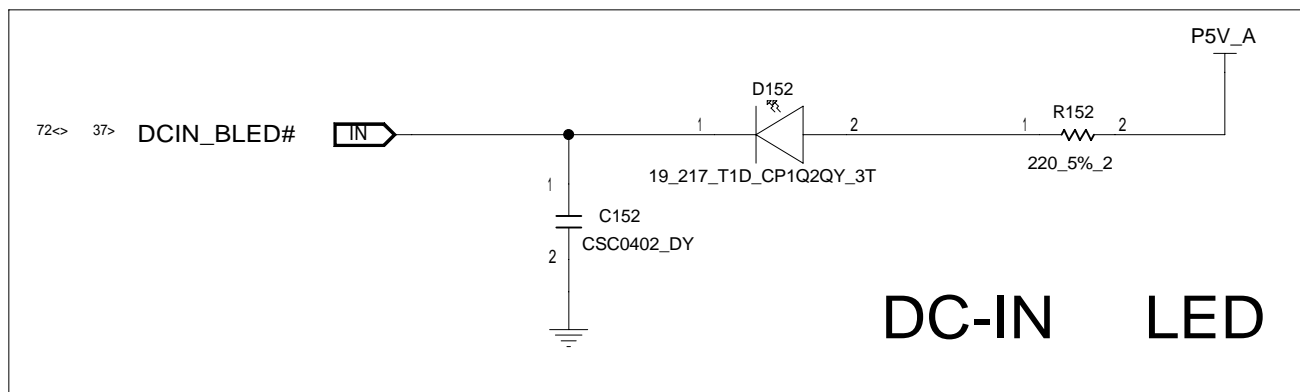
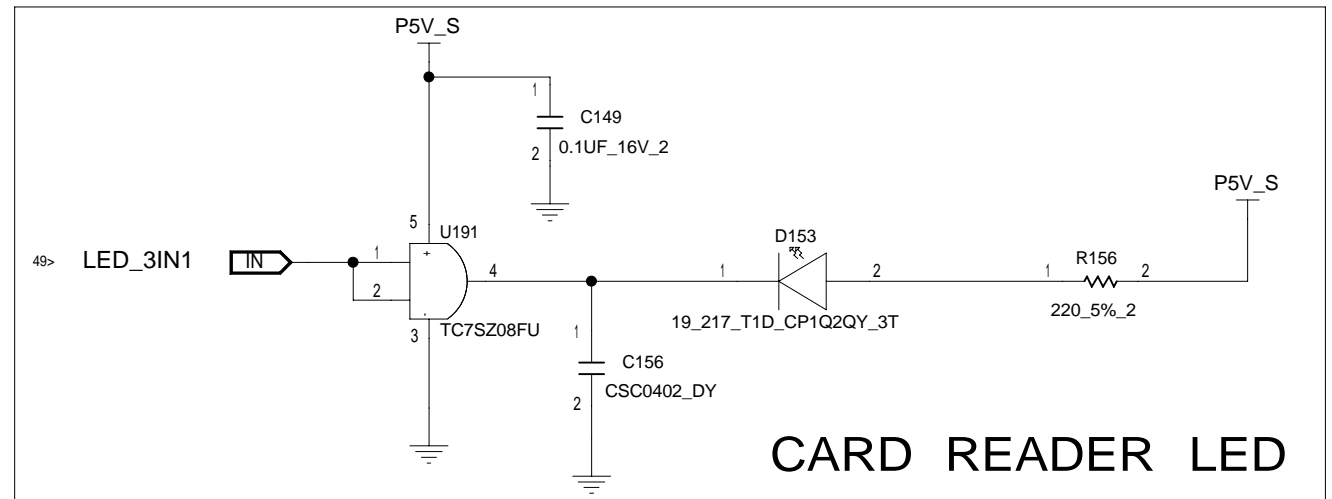
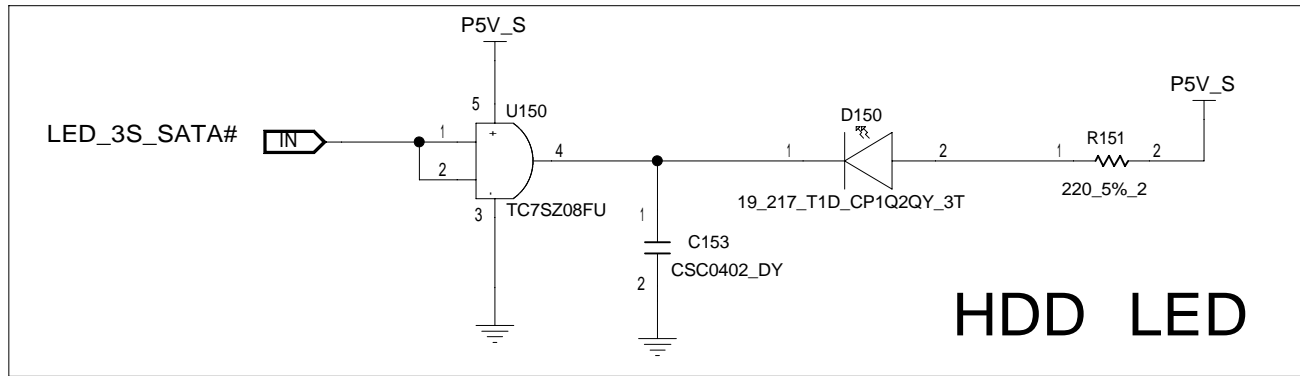
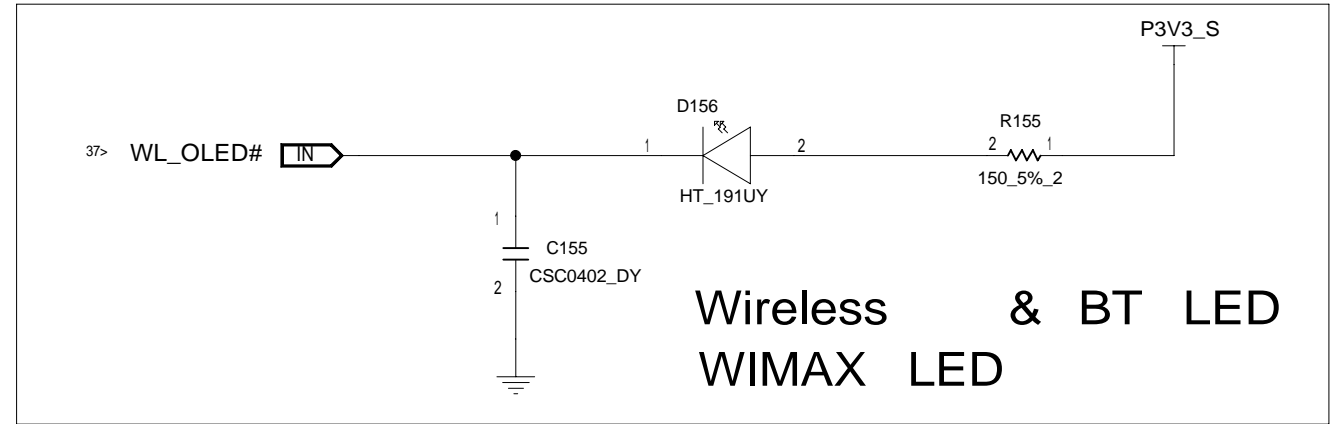
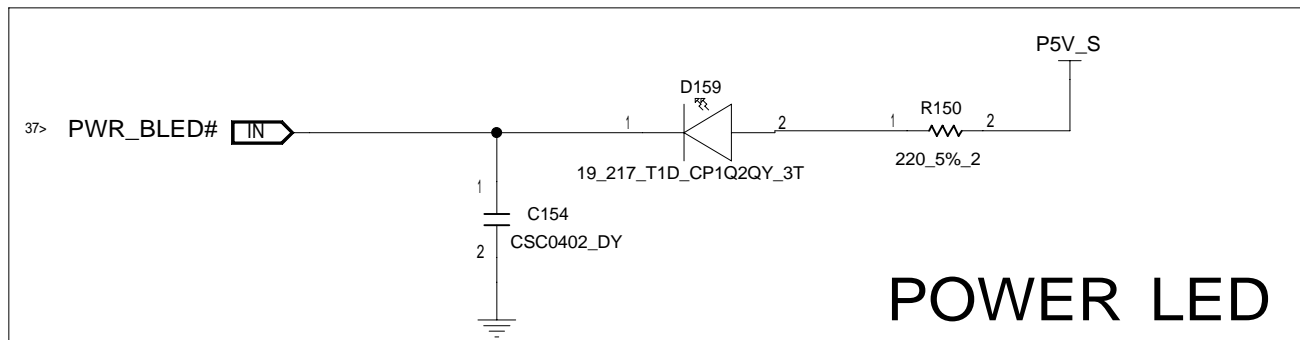
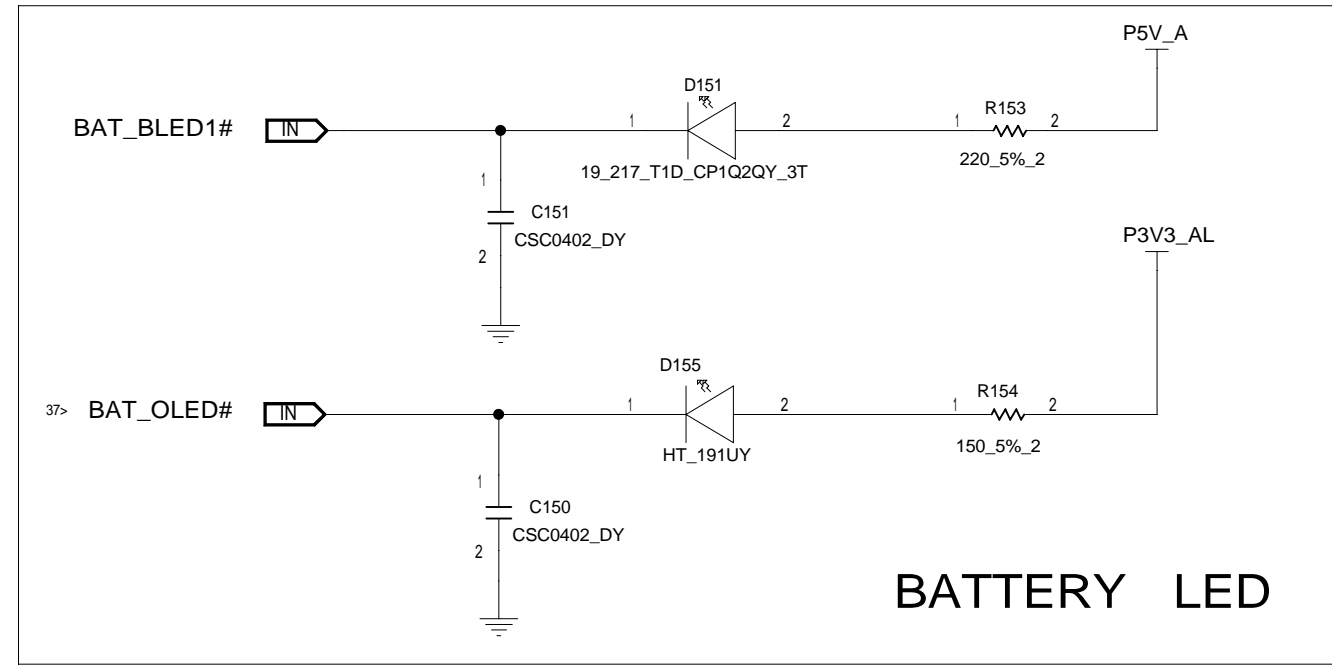
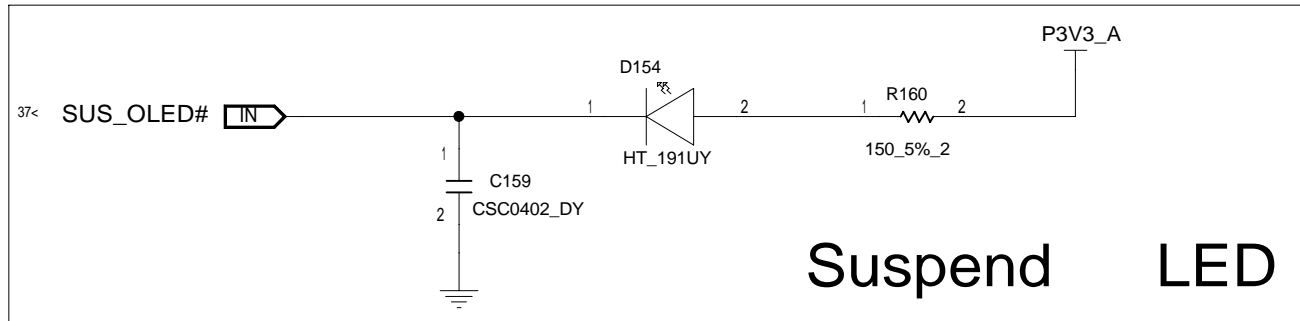


INVENTEC

TITLE EVEREST-M
HALL SENSOR

SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01
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INVENTEC				
TITLE EVEREST-M LED				
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01	

D

C

B

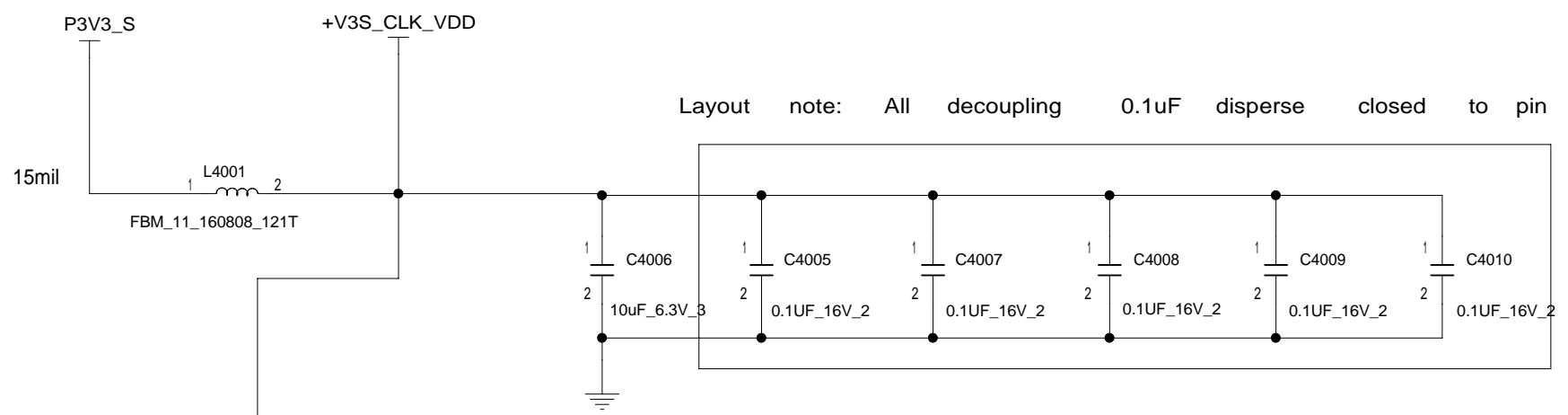
A

D

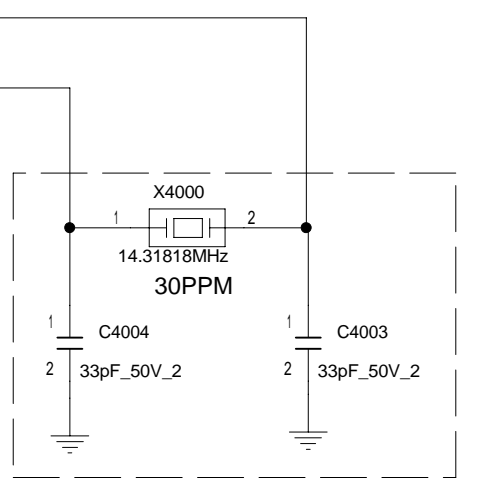
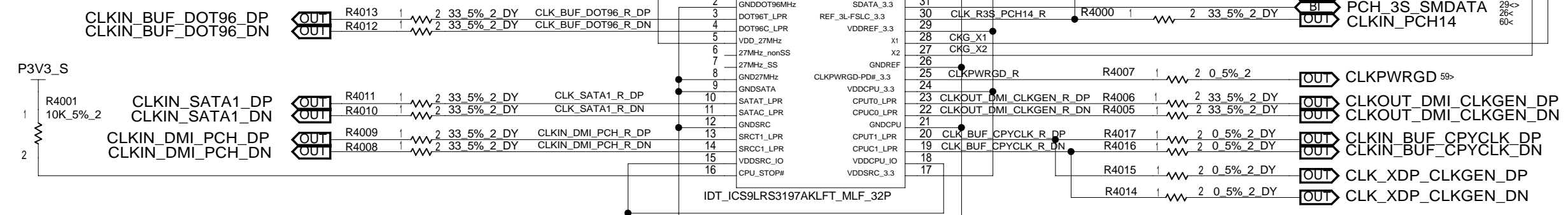
C

B

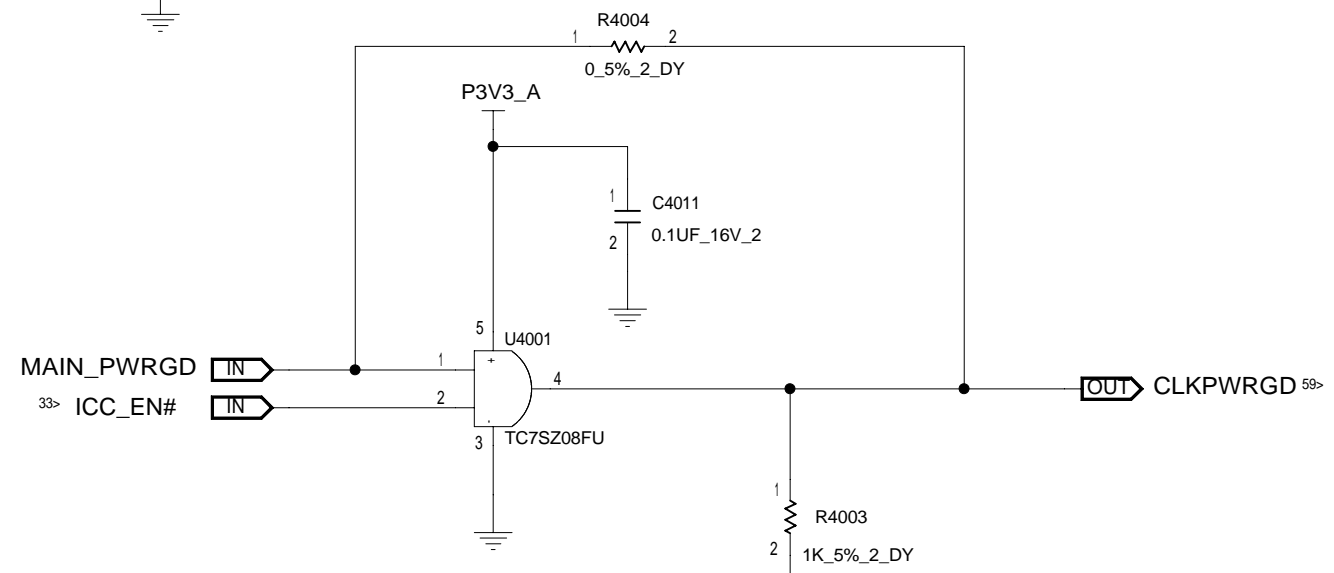
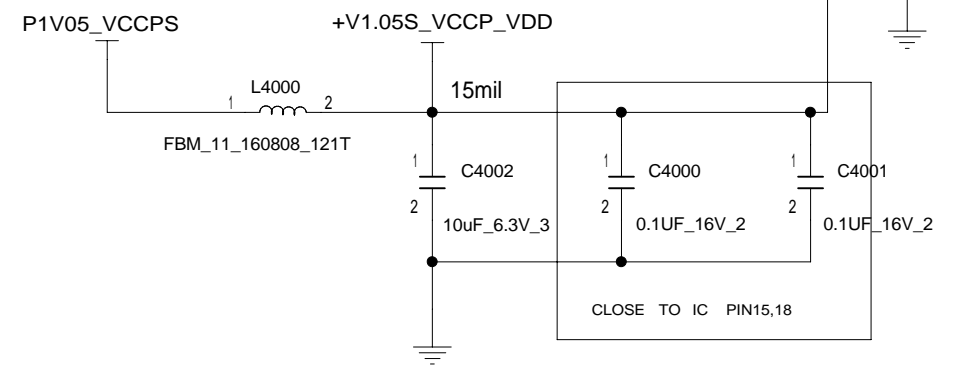
A



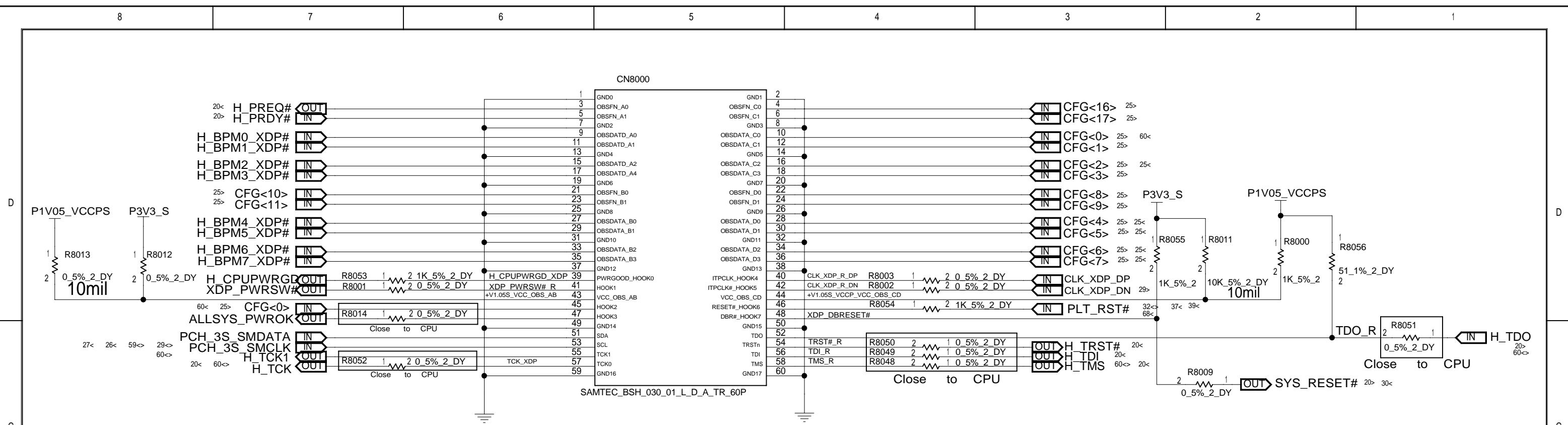
Layout note: All decoupling 0.1uF disperse closed to pin



Please place close to CLKGEN within 500mils

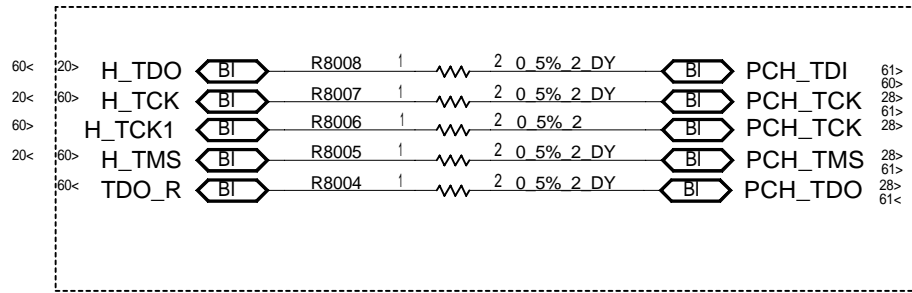


INVENTEC				
TITLE EVEREST-M CLOCK GENERATOR				
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01	
CHANGE by Frank Hu DATE Tue Jan 04 00:18:17 2011 SHEET 59 of 97				

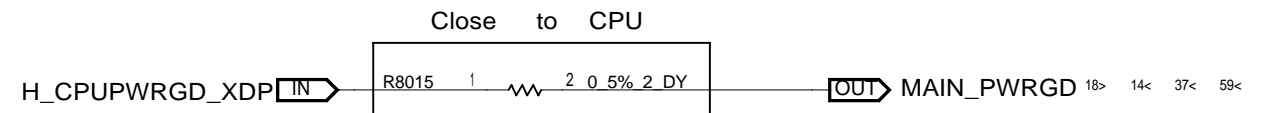
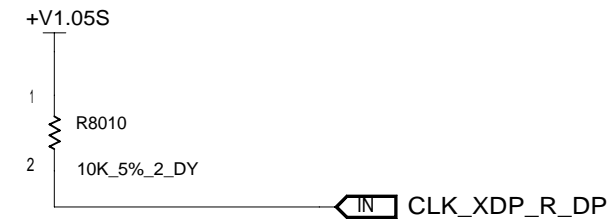
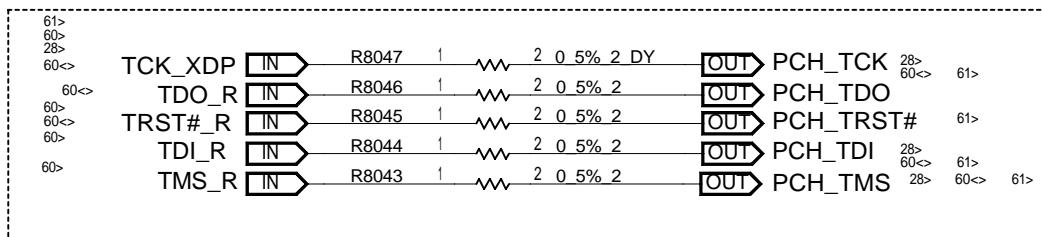


XDP CONNECTOR

SERIES



PCH ONLY

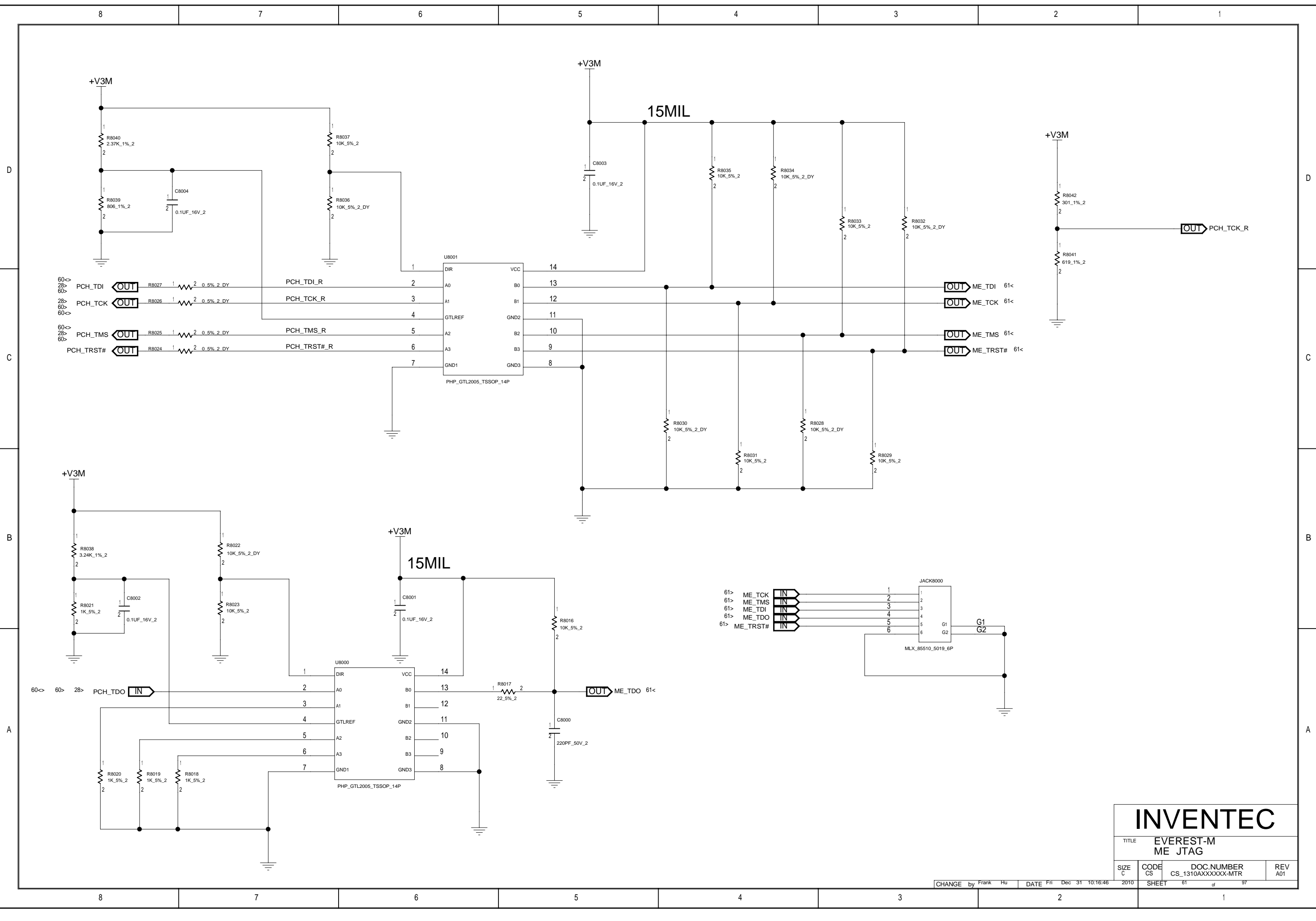


INVENTEC

TITLE EVEREST-M
XDP

SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01
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CHANGE by Frank Hu DATE Fri Dec 31 10:16:45 2010 SHEET 60 of 97



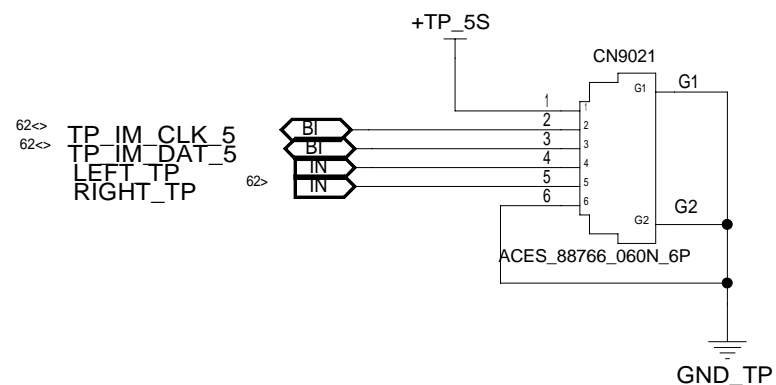
INVENTEC			
TITLE EVEREST-M ME JTAG			
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01

CHANGE by Frank Hu DATE Fri Dec 31 10:16:46 2010 SHEET 61 of 97

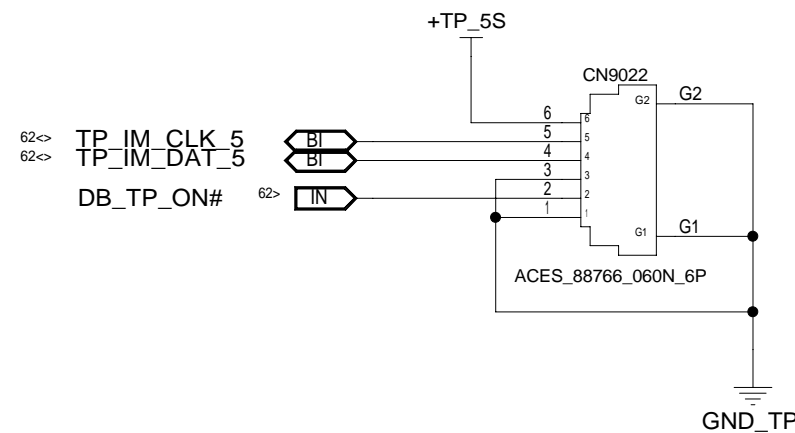
PICK BUTTON BOARD

(FOR - TOUCHPAD MODULE, TOUCHPAD SWITCH BOARD, FINGERPRINT MODULE)

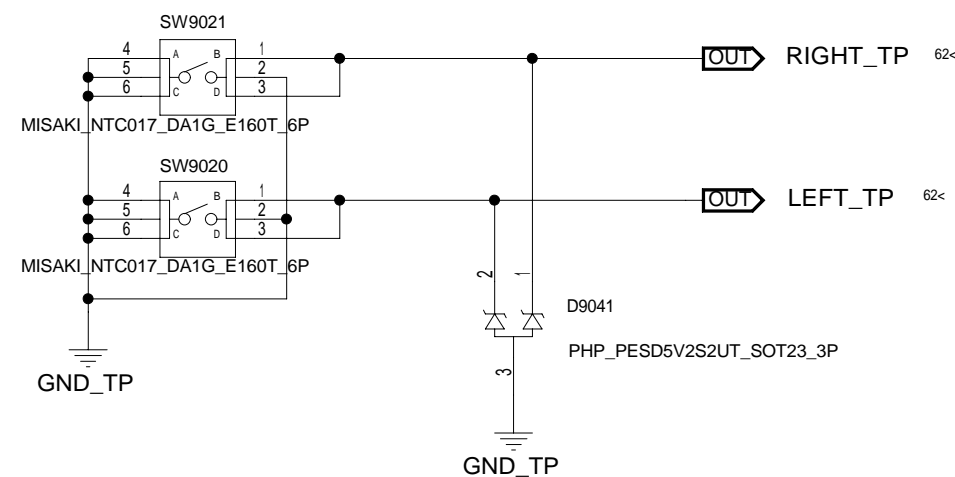
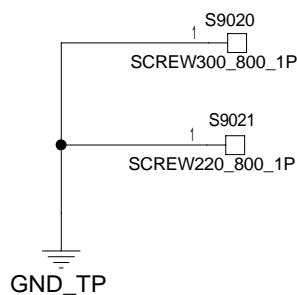
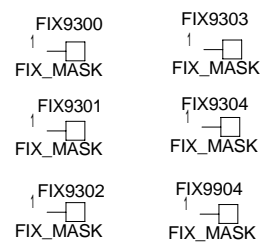
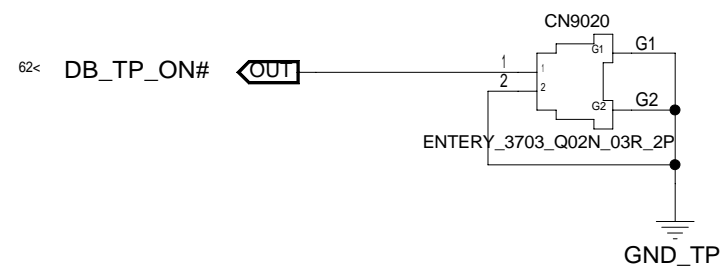
CONNECT TO TOUCHPAD MODULE



CONNECT TO MAINBOARD'S TP CONNECTOR



CONNECT TO TOUCHPAD SWITCH BOARD



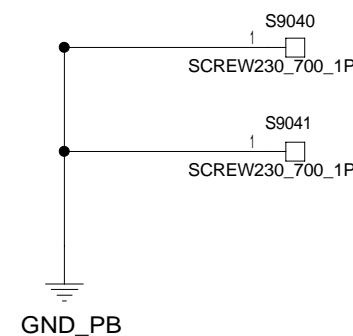
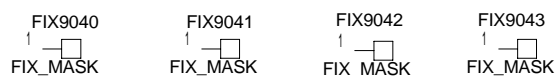
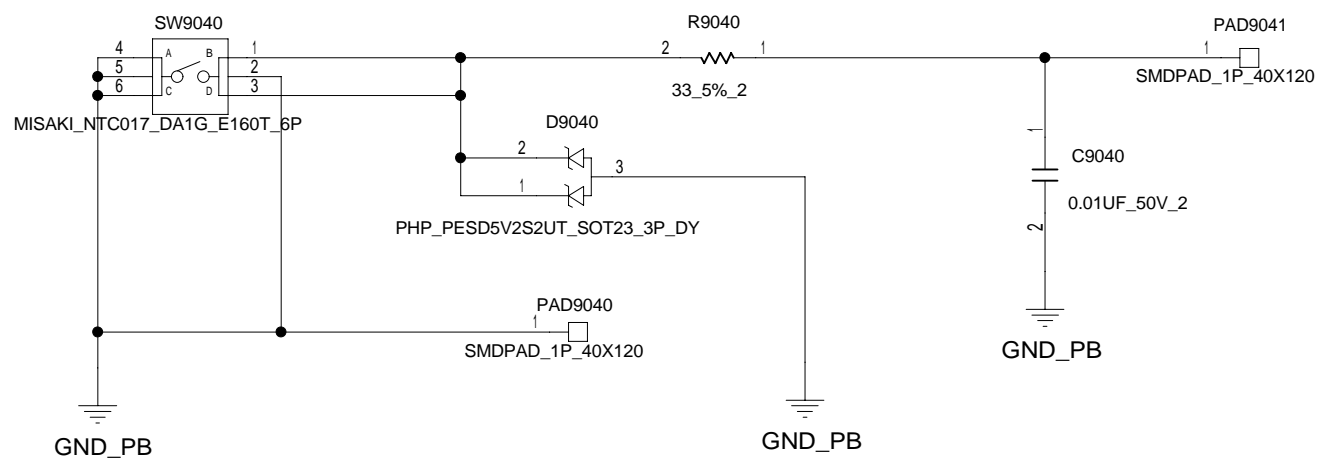
INVENTEC

TITLE EVEREST-M
PICK BUTTON BOARD

SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01
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CHANGE by Frank Hu DATE Fri Dec 31 10:17:03 2010 SHEET 62 of 97

TOUCHPAD SWITCH BOARD



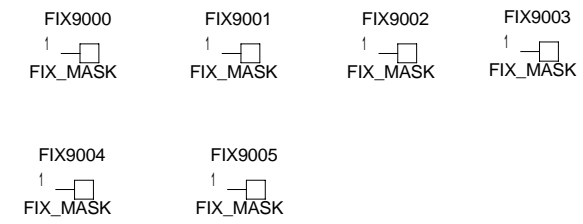
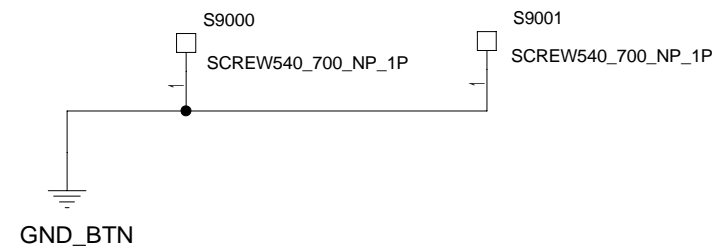
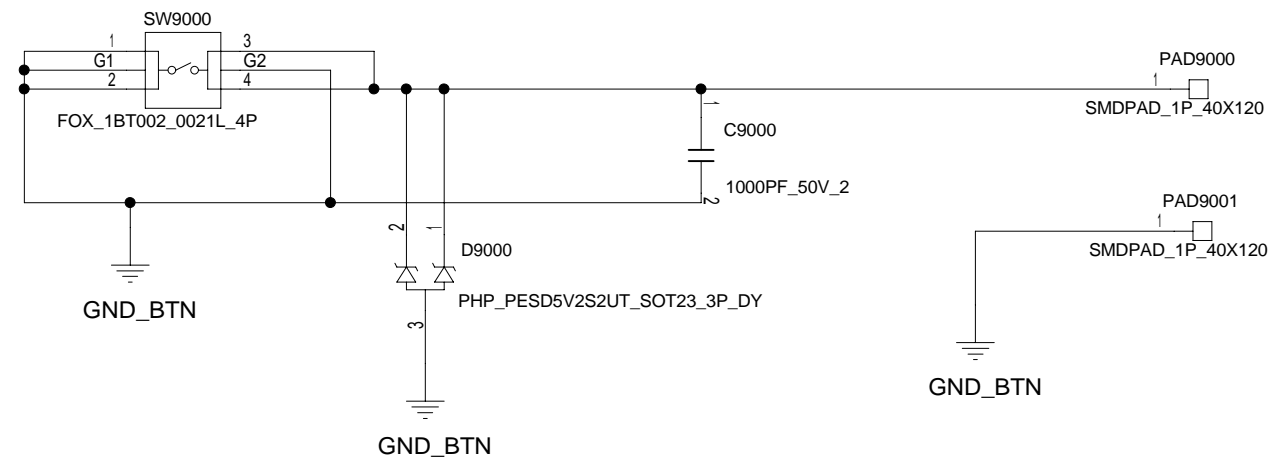
INVENTEC

TITLE EVEREST-M
TOUCH PAD SW BOARD

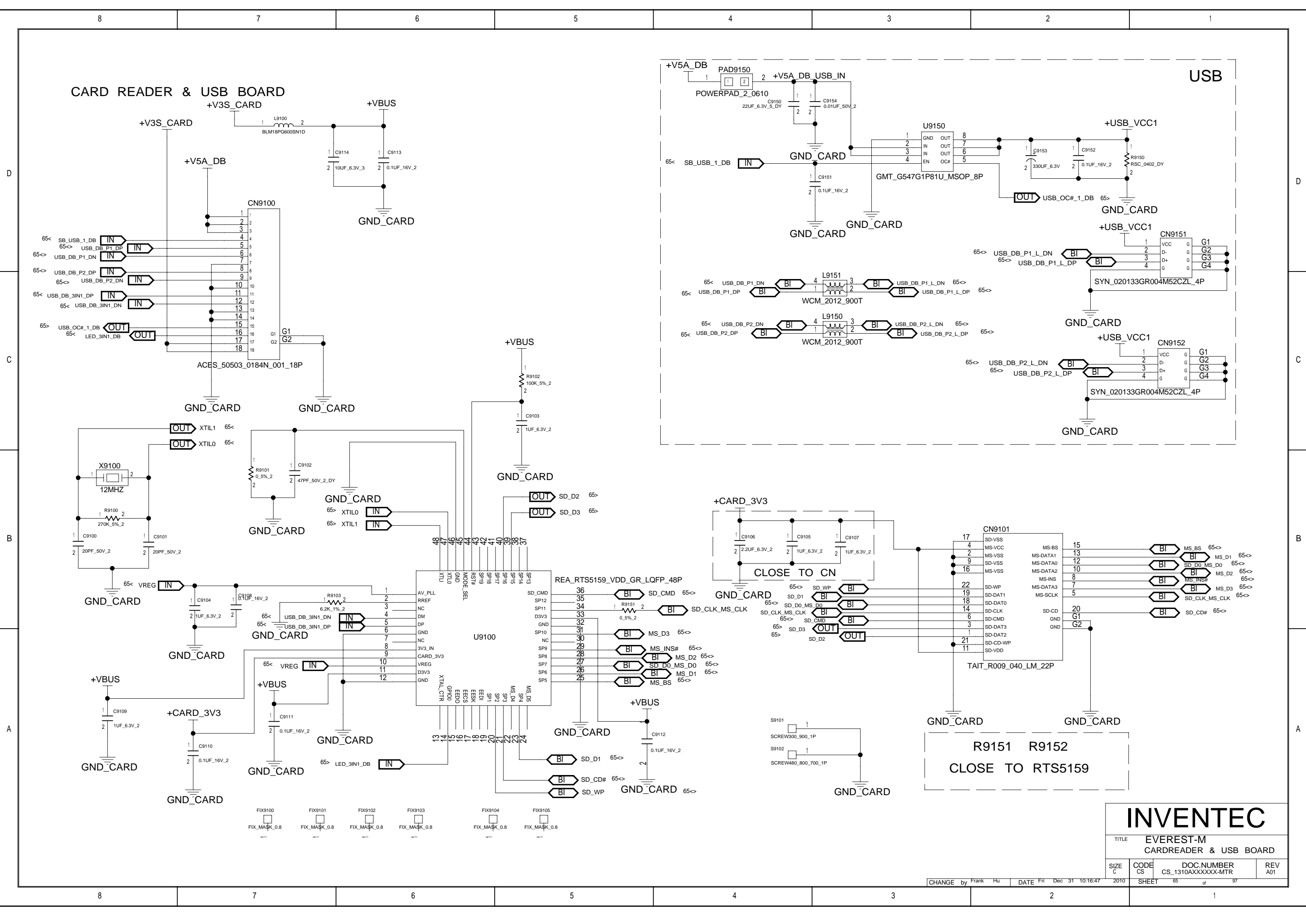
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01
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POWER BUTTON



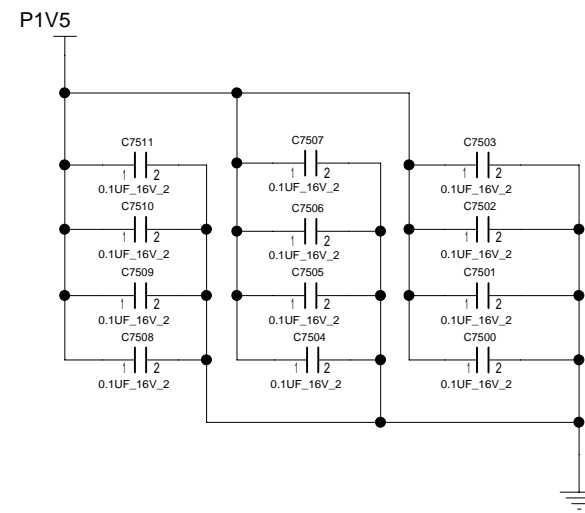
INVENTEC			
TITLE EVEREST-M POWER BUTTON BOARD			
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01



INVENTEC			
TITLE EVEREST-M CARDREADER & USB BOARD			
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01

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EMI

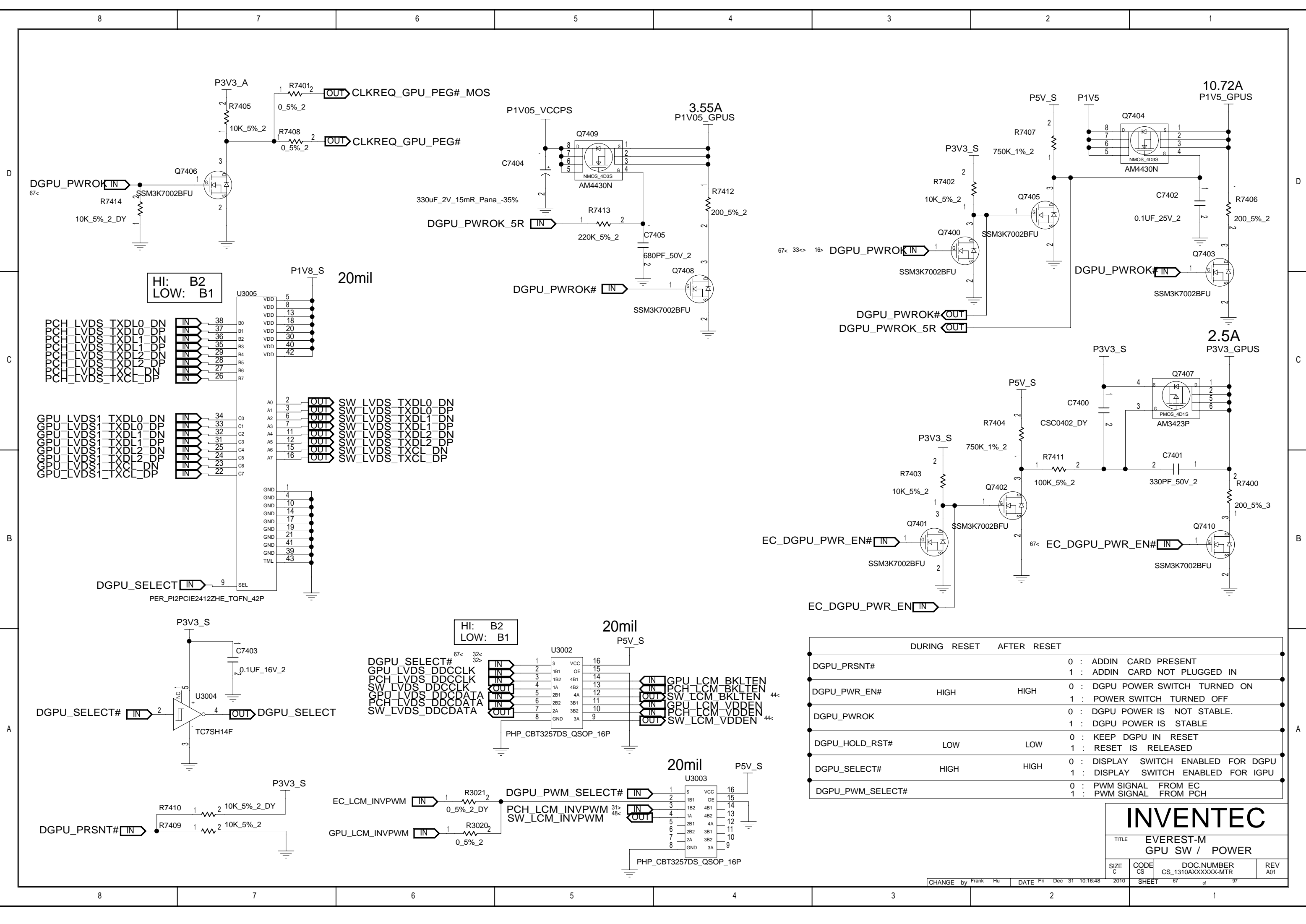


INVENTEC

TITLE EVEREST-M
EMI

SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01
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CHANGE by Frank Hu DATE Fri Dec 31 10:17:04 2010 SHEET 66 of 97



HI: B2
LOW: B1

20mil

HI: B2
LOW: B1

20mil

20mil

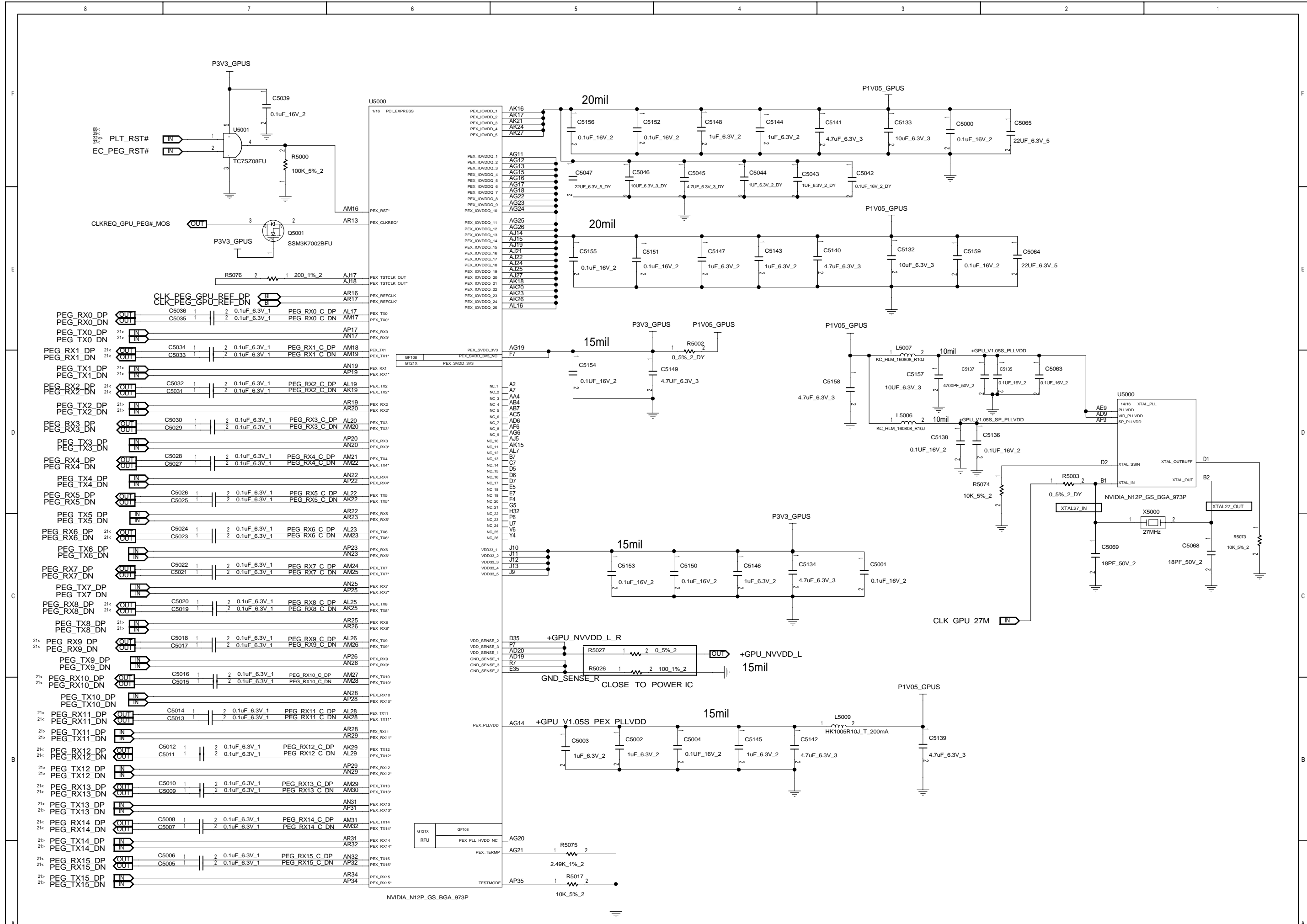
	DURING RESET	AFTER RESET	
DGPU_PRST#			0 : ADDIN CARD PRESENT 1 : ADDIN CARD NOT PLUGGED IN
DGPU_PWR_EN#	HIGH	HIGH	0 : DGPU POWER SWITCH TURNED ON 1 : POWER SWITCH TURNED OFF
DGPU_PWROK			0 : DGPU POWER IS NOT STABLE. 1 : DGPU POWER IS STABLE
DGPU_HOLD_RST#	LOW	LOW	0 : KEEP DGPU IN RESET 1 : RESET IS RELEASED
DGPU_SELECT#	HIGH	HIGH	0 : DISPLAY SWITCH ENABLED FOR DGPU 1 : DISPLAY SWITCH ENABLED FOR IGPU
DGPU_PWM_SELECT#			0 : PWM SIGNAL FROM EC 1 : PWM SIGNAL FROM PCH

INVENTEC

TITLE EVEREST-M
GPU SW / POWER

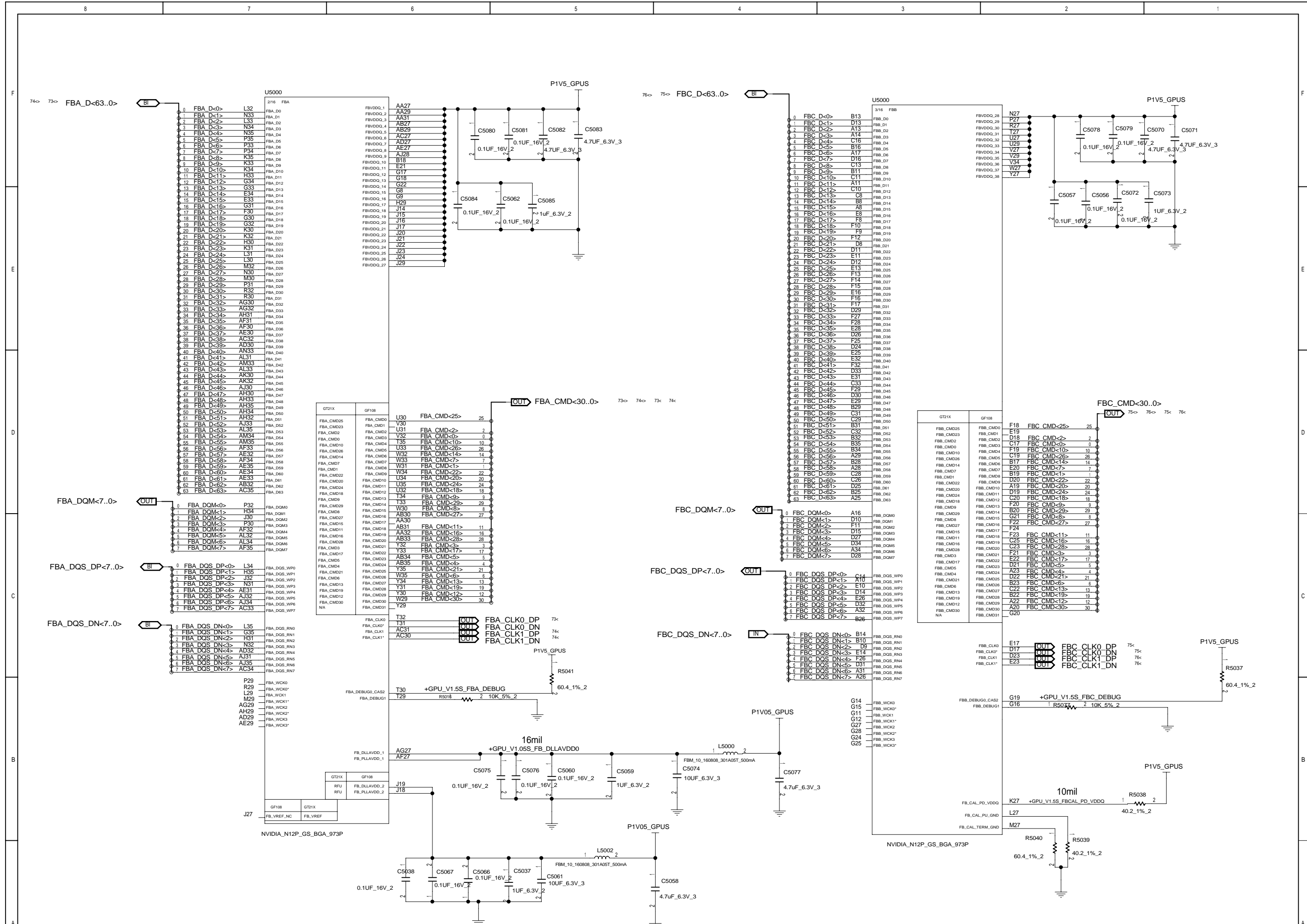
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01
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CHANGE by Frank Hu DATE Fri Dec 31 10:16:48 2010 SHEET 67 of 97



INVENTEC			
TITLE EVEREST GPU-1			
SIZE C	CODE ES	DOC NUMBER CS_1310AXXXX-MTR	REV A01
SHEET 68		# 97	

CHANGE by Frank Hu DATE Fri Dec 31 10:16:49 2010



INVENTEC

TITLE
EVEREST
GPU-2

SIZE C	CODE ES	DOC NUMBER CS_1310AXXXX-MTR	REV A01
SHEET 69		# 97	

CHANGE by Frank Hu DATE Fri Dec 31 10:16:50 2010

D

C

B

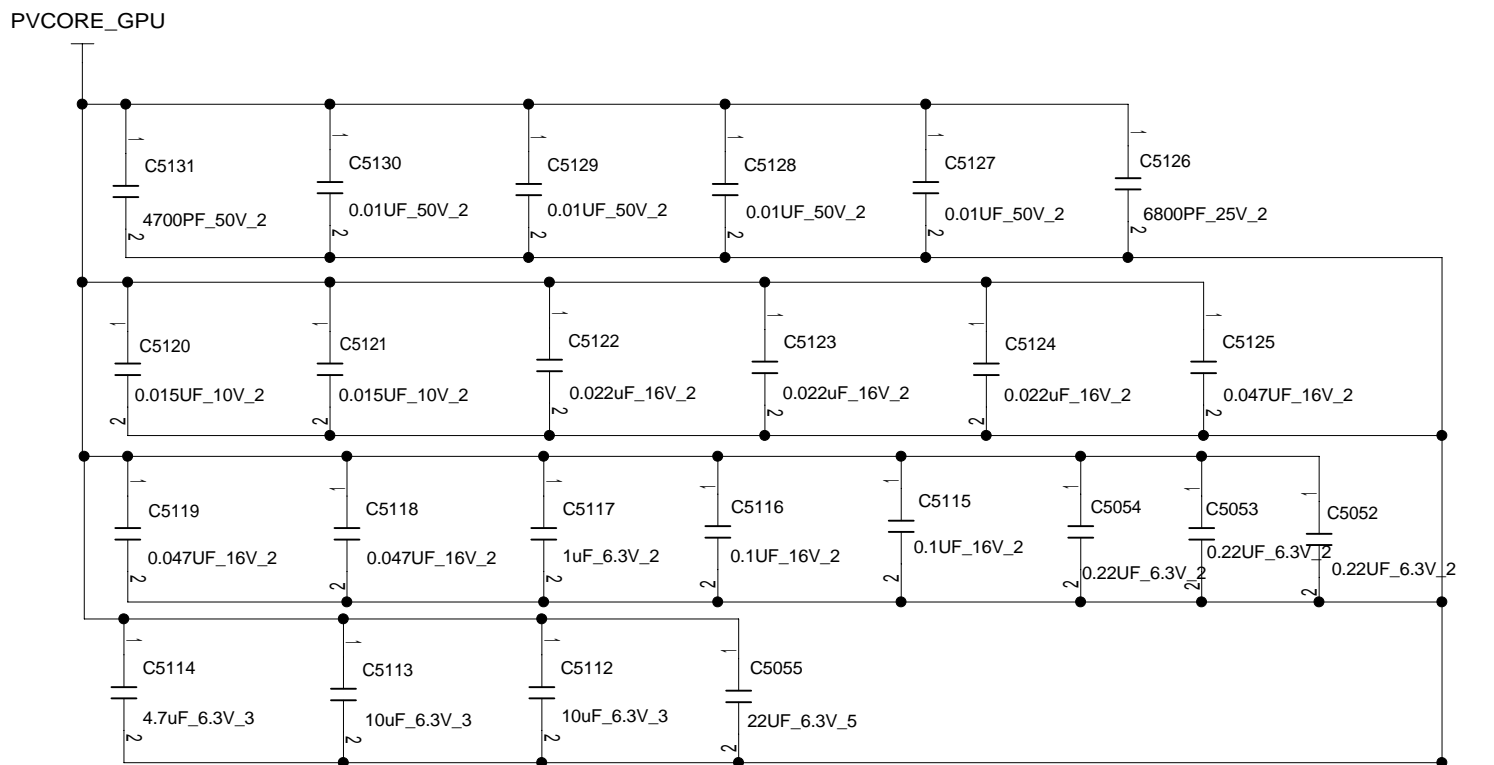
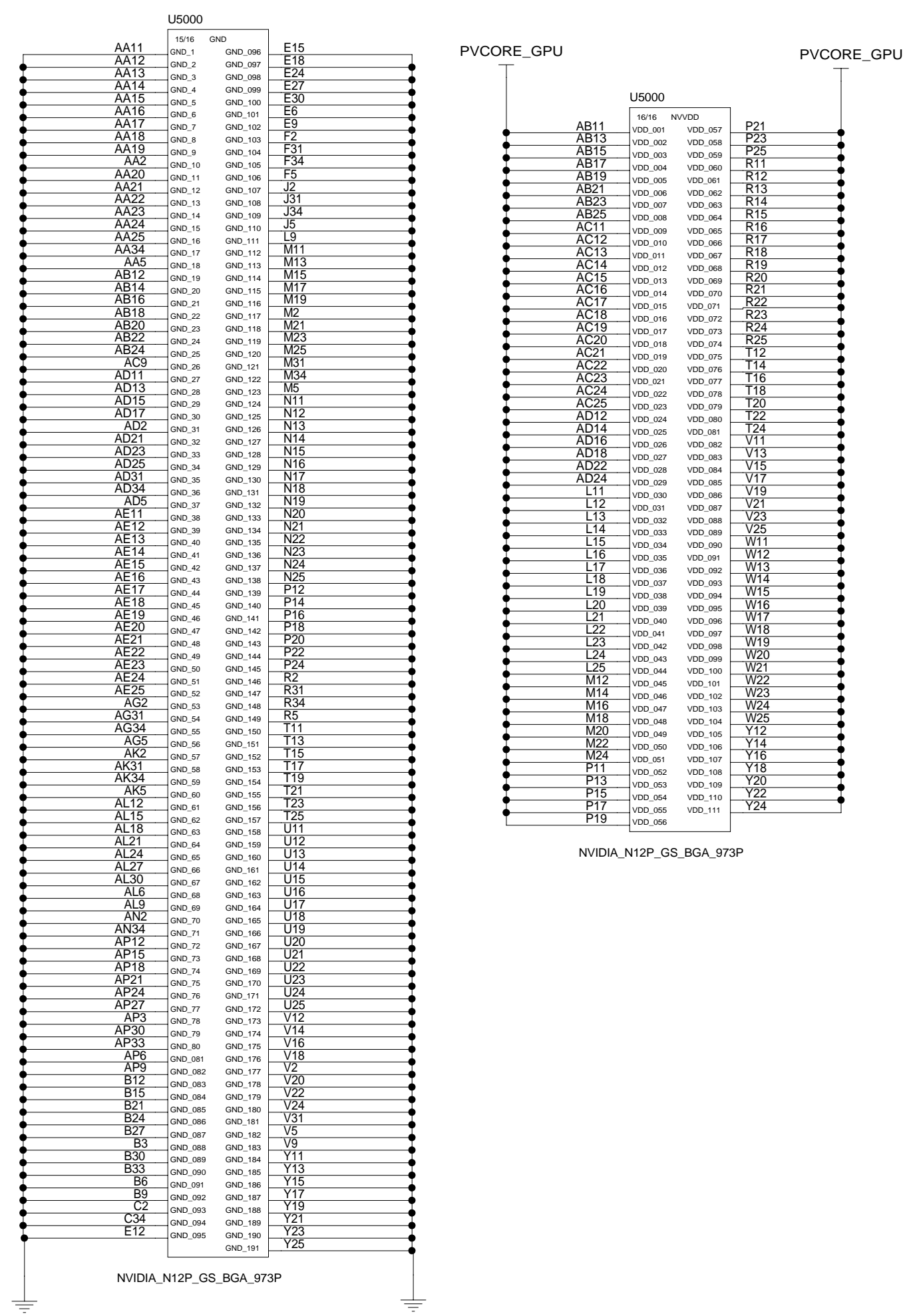
A

D

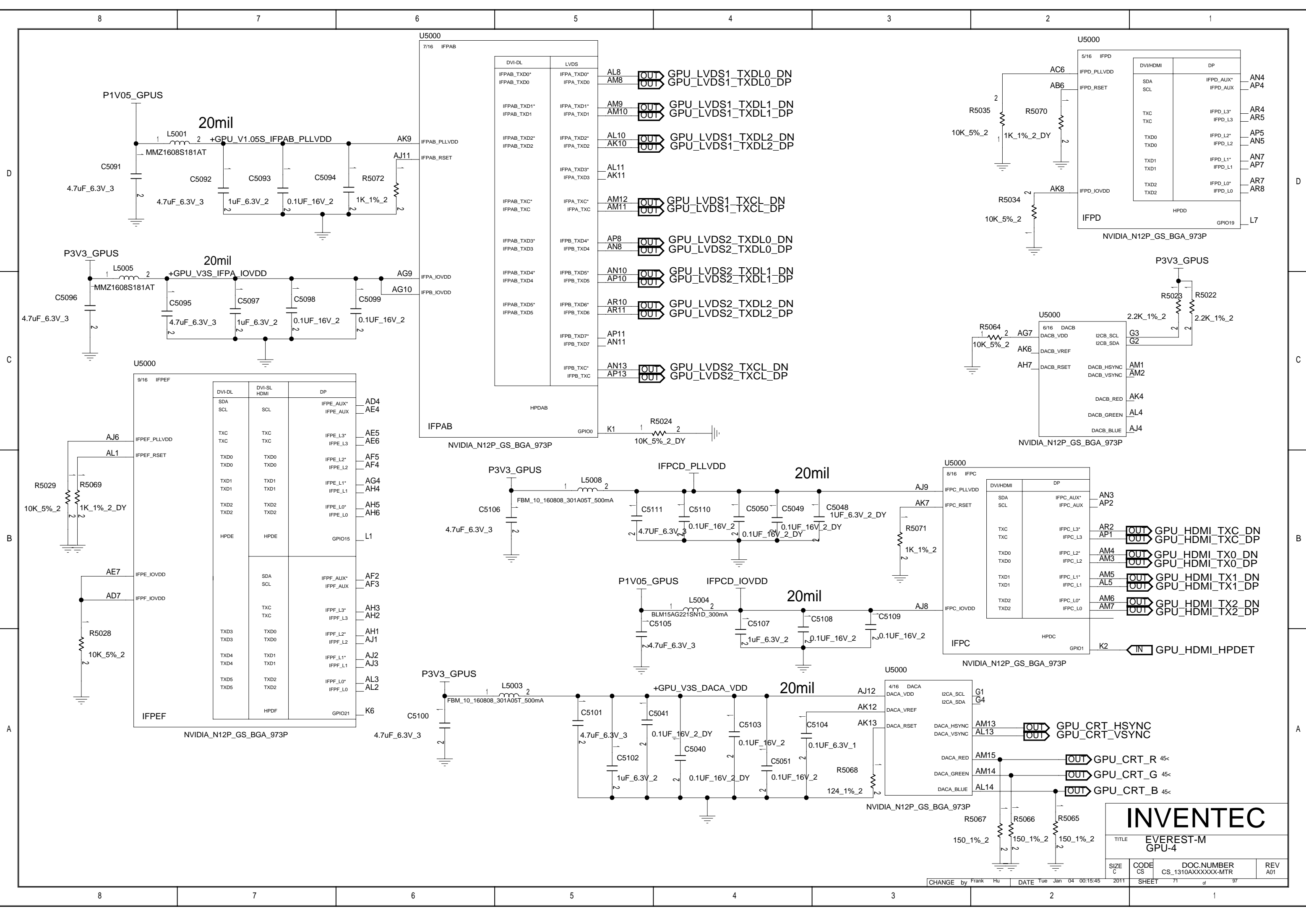
C

B

A



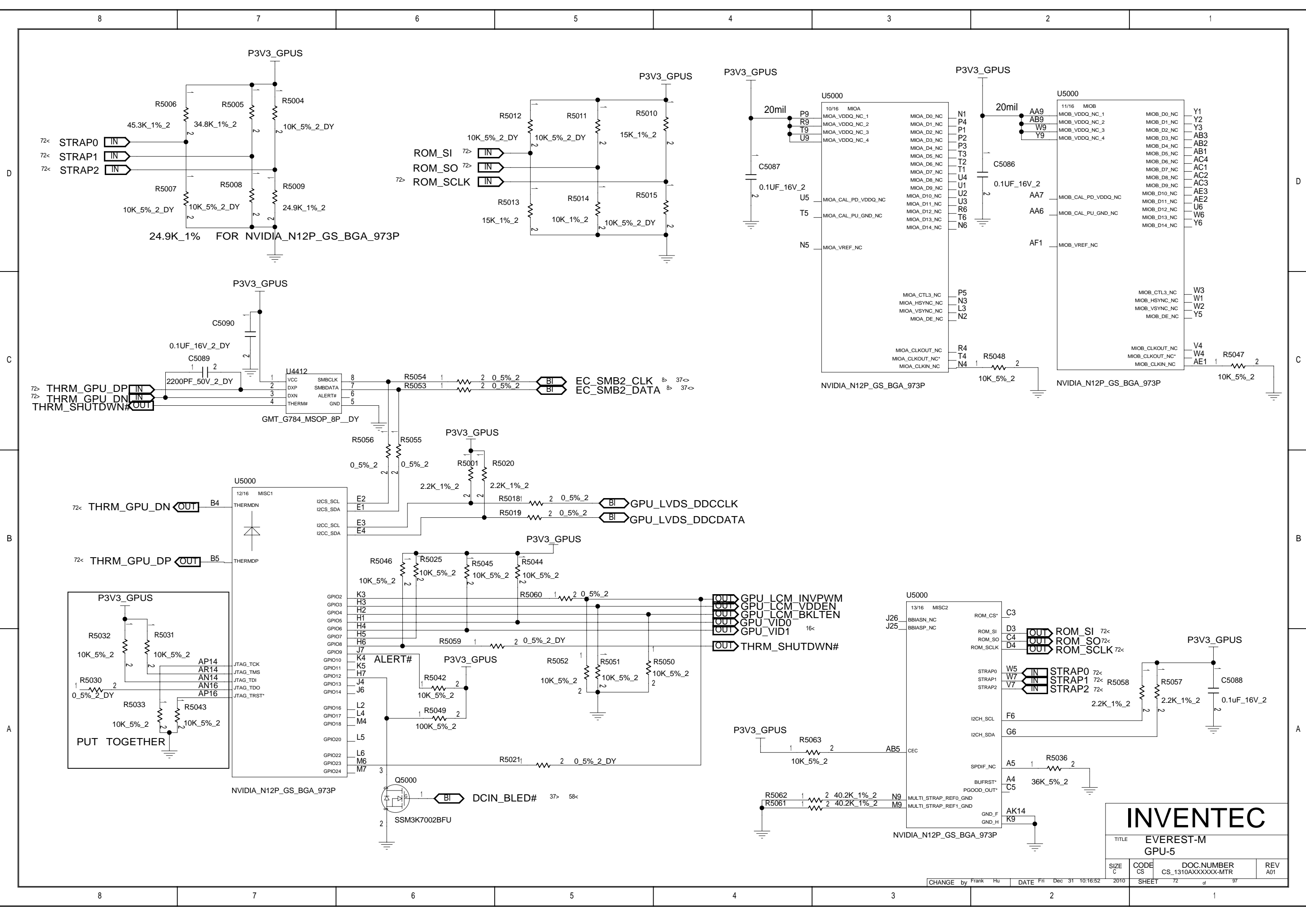
INVENTEC				
TITLE EVEREST-M GPU-3				
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01	
CHANGE by Frank Hu		DATE Fri Dec 31 10:17:04 2010	SHEET 70	of 97



INVENTEC

TITLE EVEREST-M GPU-4

SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01
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INVENTEC				
TITLE EVEREST-M GPU-5				
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01	

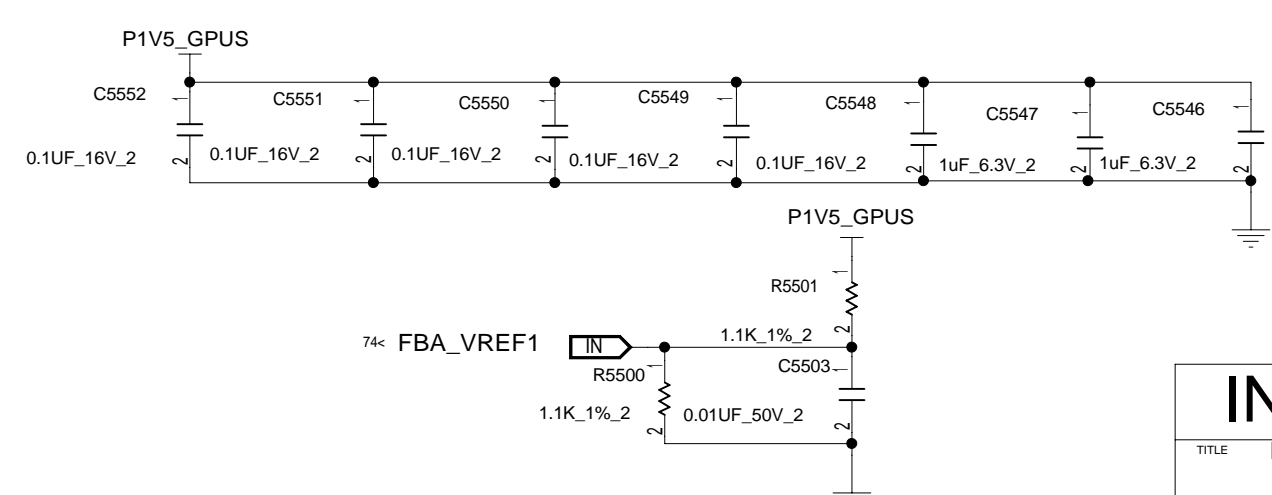
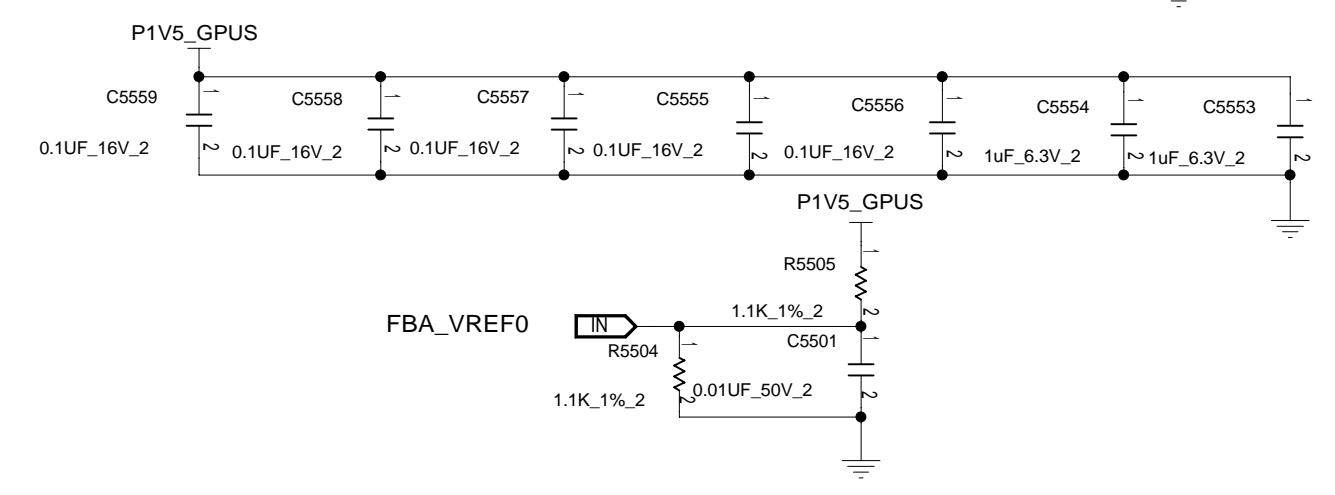
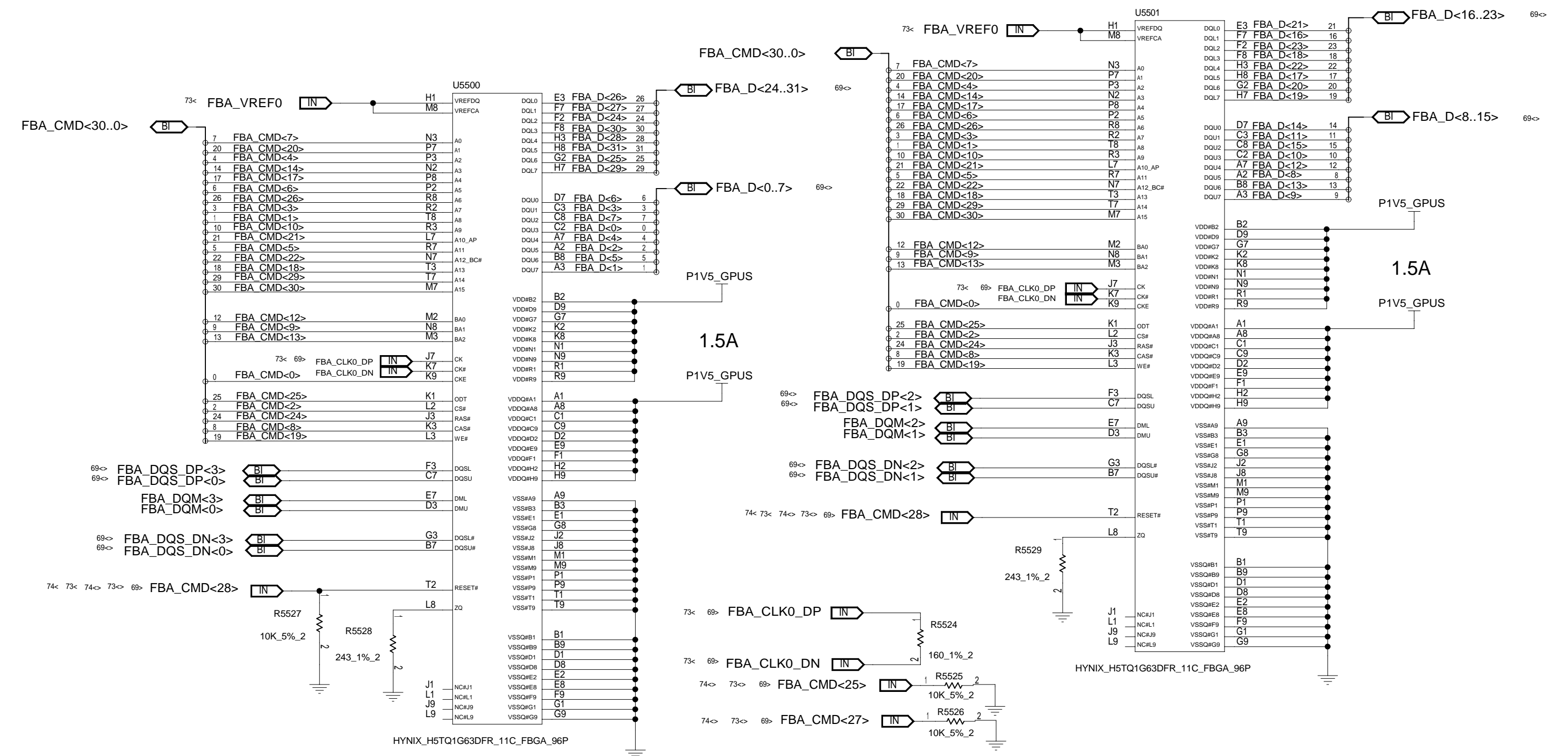
CHANGE by Frank Hu DATE Fri Dec 31 10:16:52 2010 SHEET 72 of 97

D

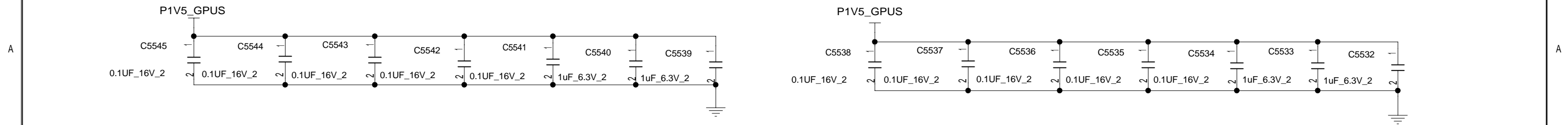
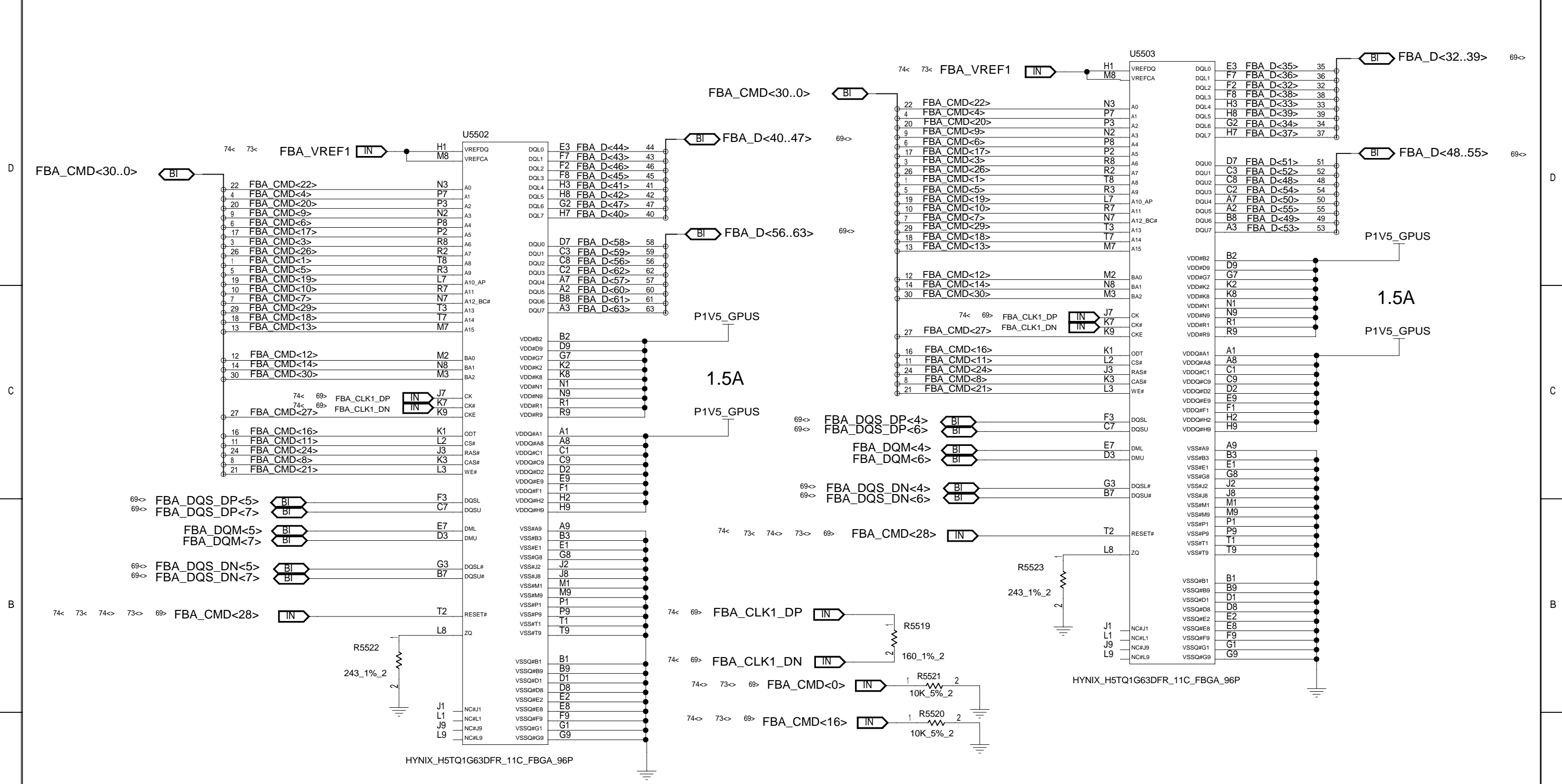
C

B

A



INVENTEC				
TITLE EVEREST-M VRAM				
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01	
CHANGE by Frank Hu DATE Fri Dec 31 10:16:52 2010 SHEET 73 of 97				



INVENTEC

TITLE EVEREST-M
VRAM

SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01
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CHANGE by Frank Hu DATE Fri Dec 31 10:16:53 2010 SHEET 74 of 97

D

C

B

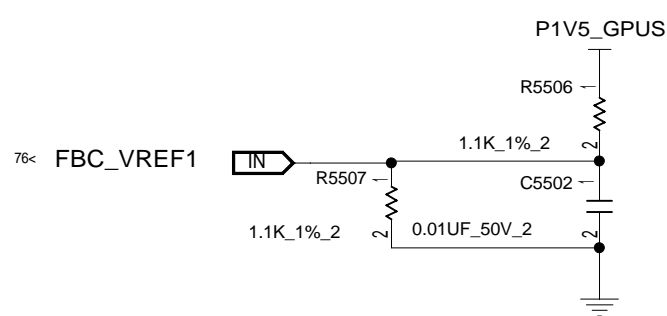
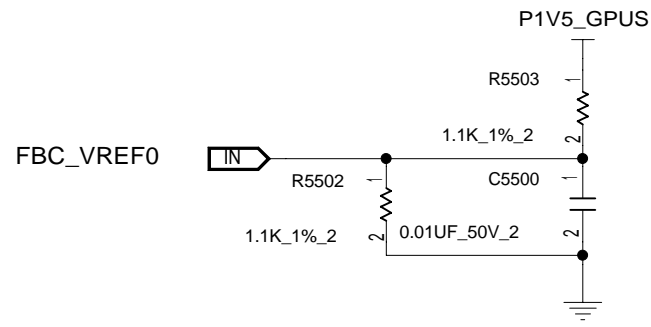
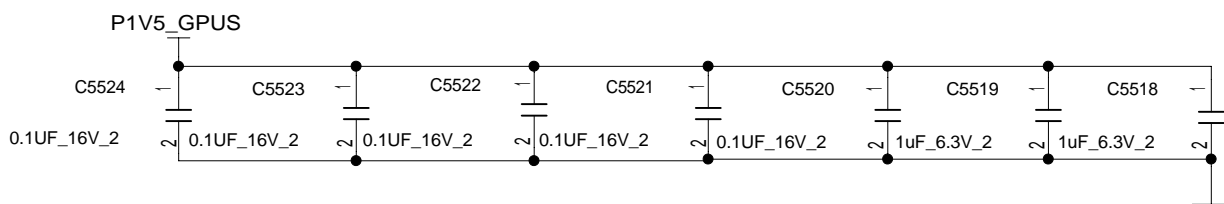
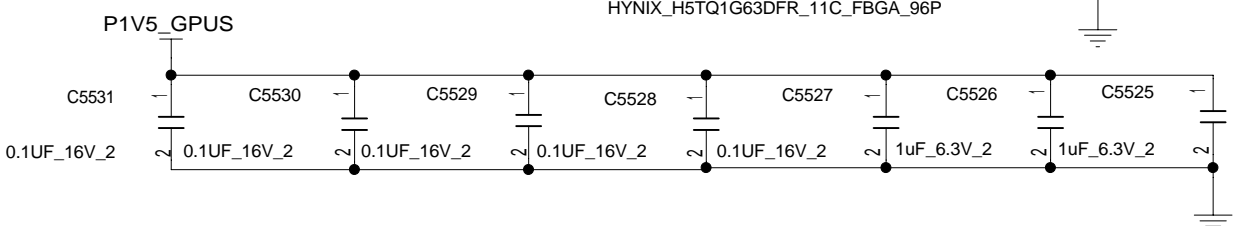
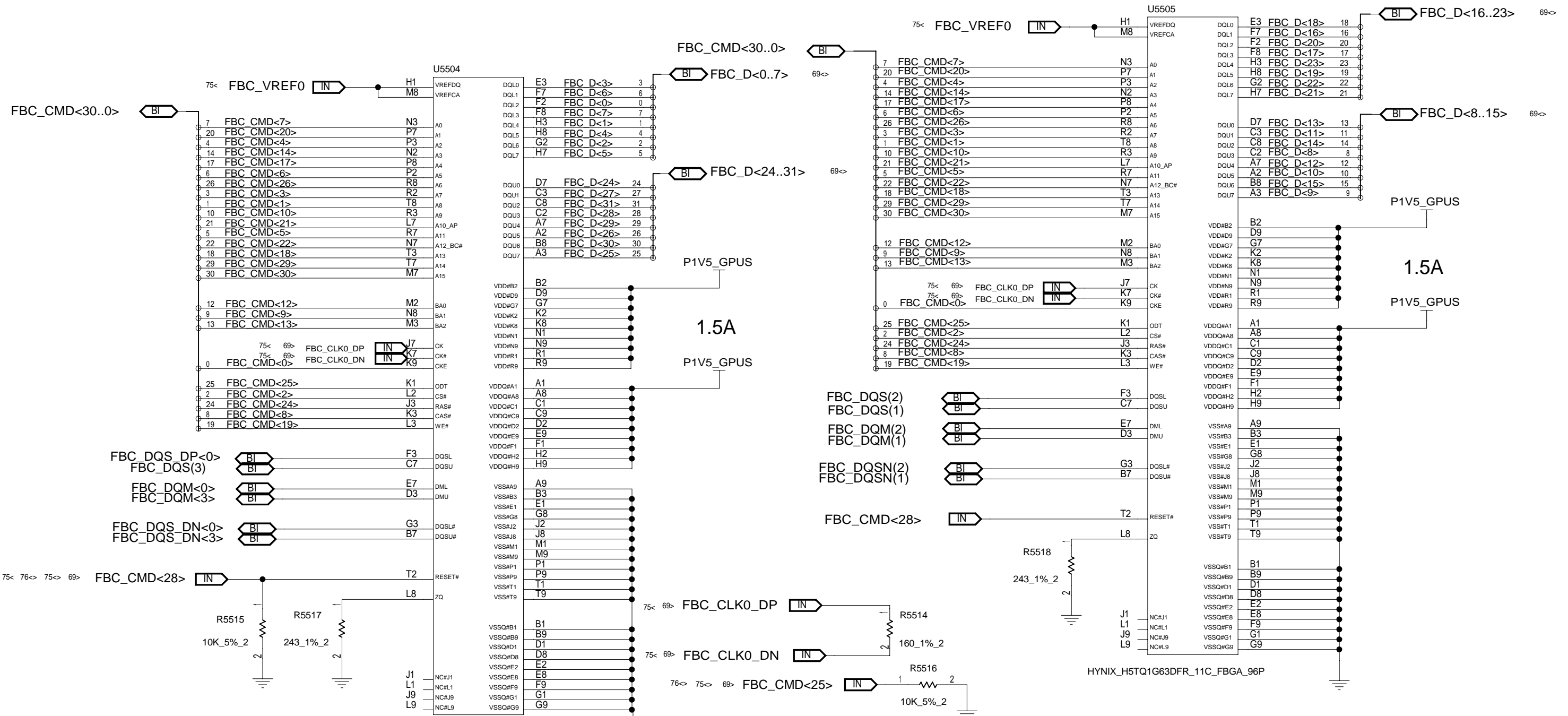
A

D

C

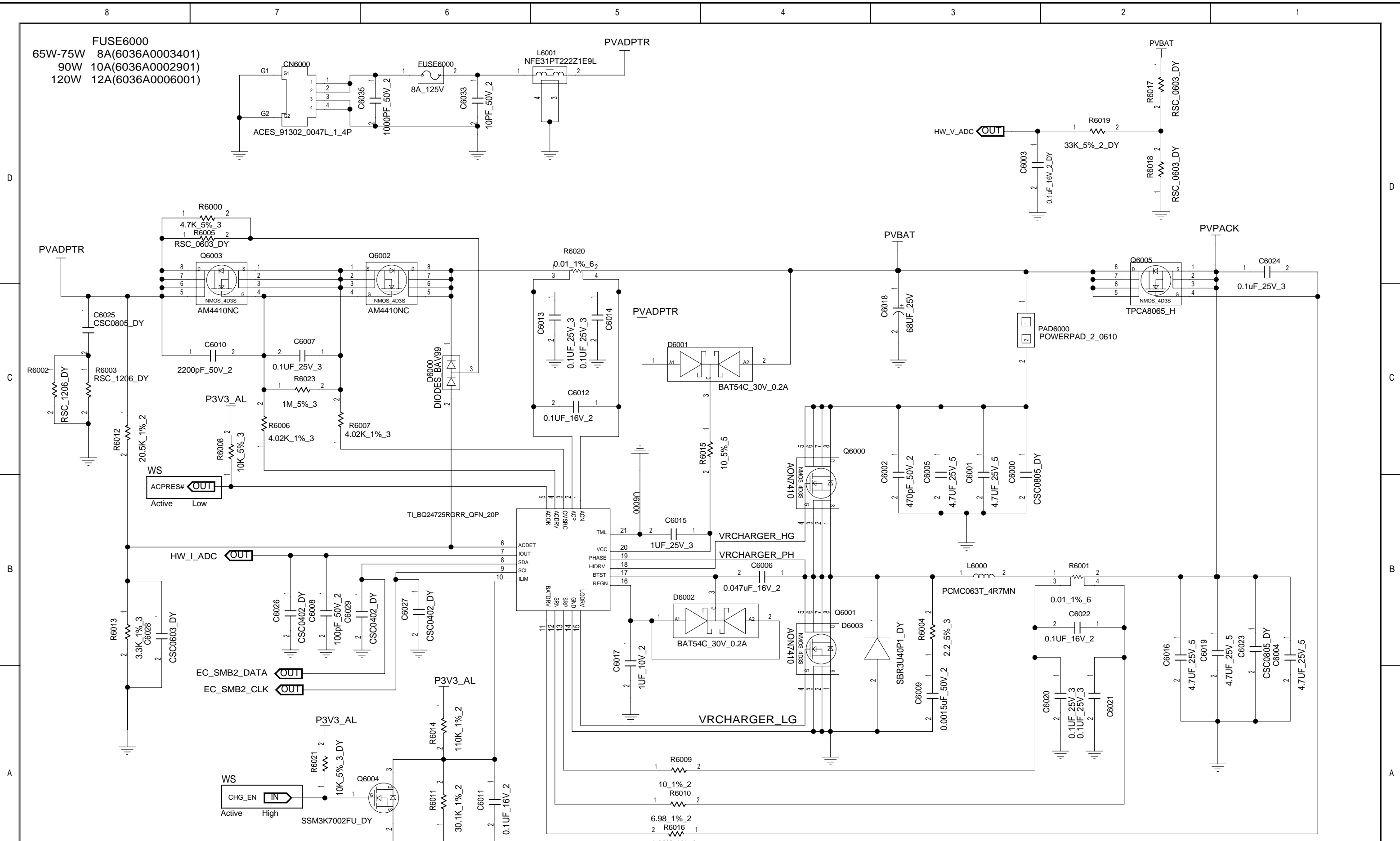
B

A



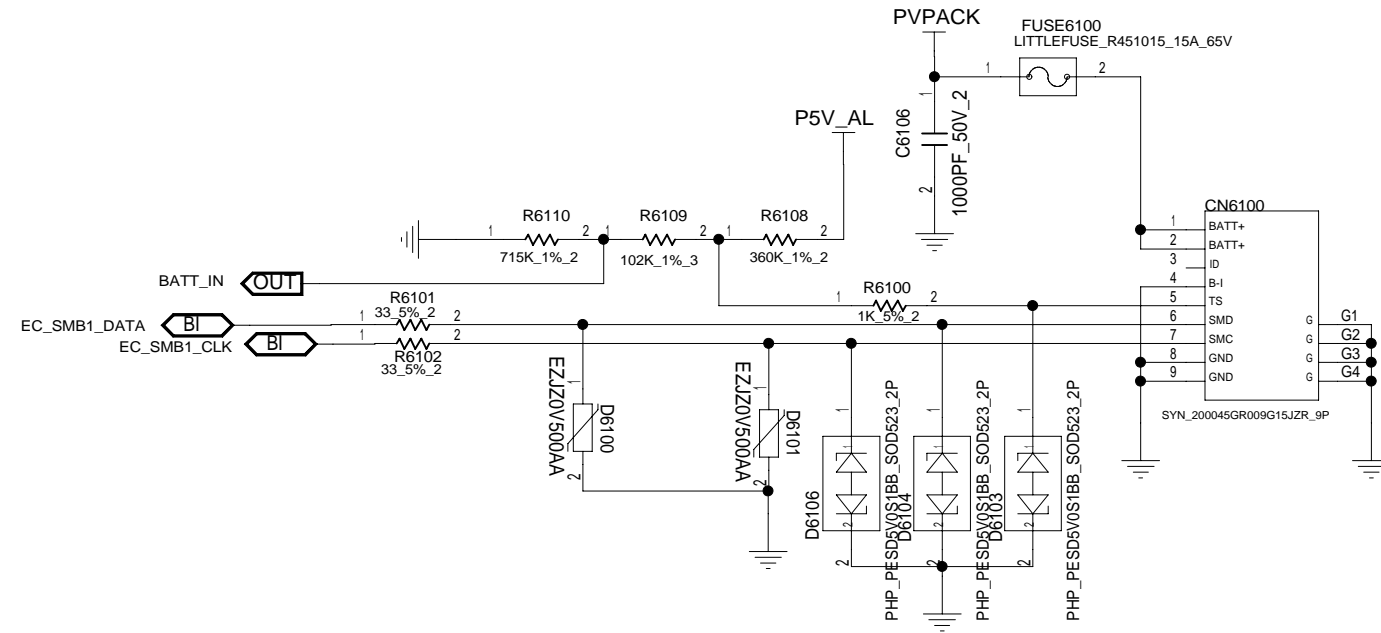
INVENTEC				
TITLE EVEREST-M VRAM				
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01	
CHANGE by Frank Hu		DATE Fri Dec 31 10:16:54	2010	SHEET 75 of 97

FUSE6000
 65W-75W 8A(6036A0003401)
 90W 10A(6036A0002901)
 120W 12A(6036A0006001)

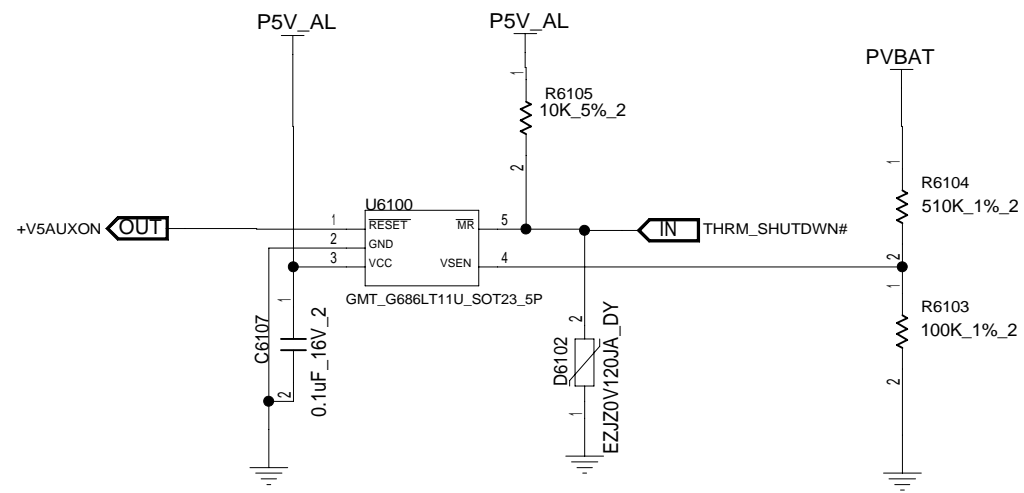
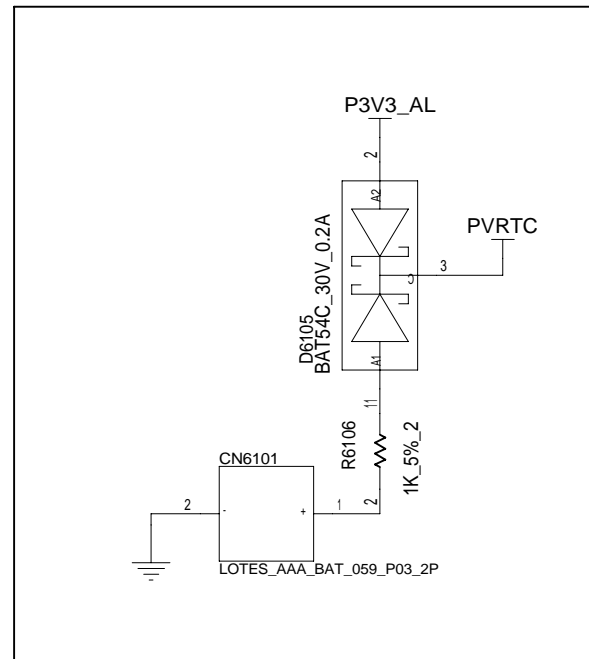


INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION Block Diagram			
SIZE C	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01



REMOVE ?



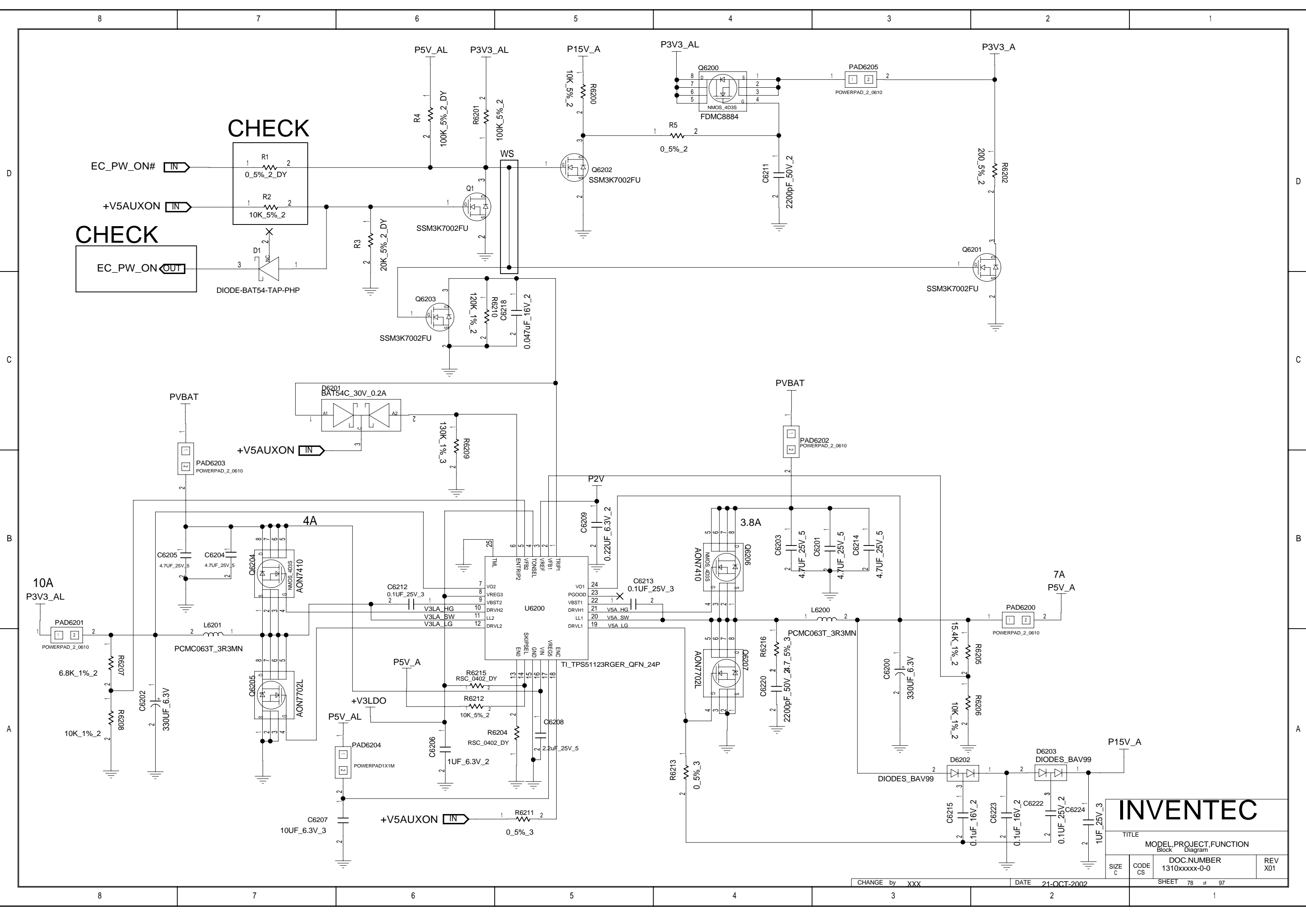
INVENTEC

TITLE MODEL,PROJECT,FUNCTION
Block Diagram

SIZE CODE DOC.NUMBER REV
C CS 1310xxxx-0-0 X01

CHANGE by XXX DATE 21-OCT-2002

SHEET 77 of 97



INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC. NUMBER	REV
C	CS	1310xxxx-0-0	X01
DATE 21-OCT-2002			SHEET 78 of 97

CHANGE by XXX DATE 21-OCT-2002

D

C

B

A

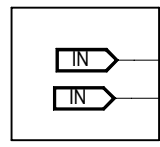
D

C

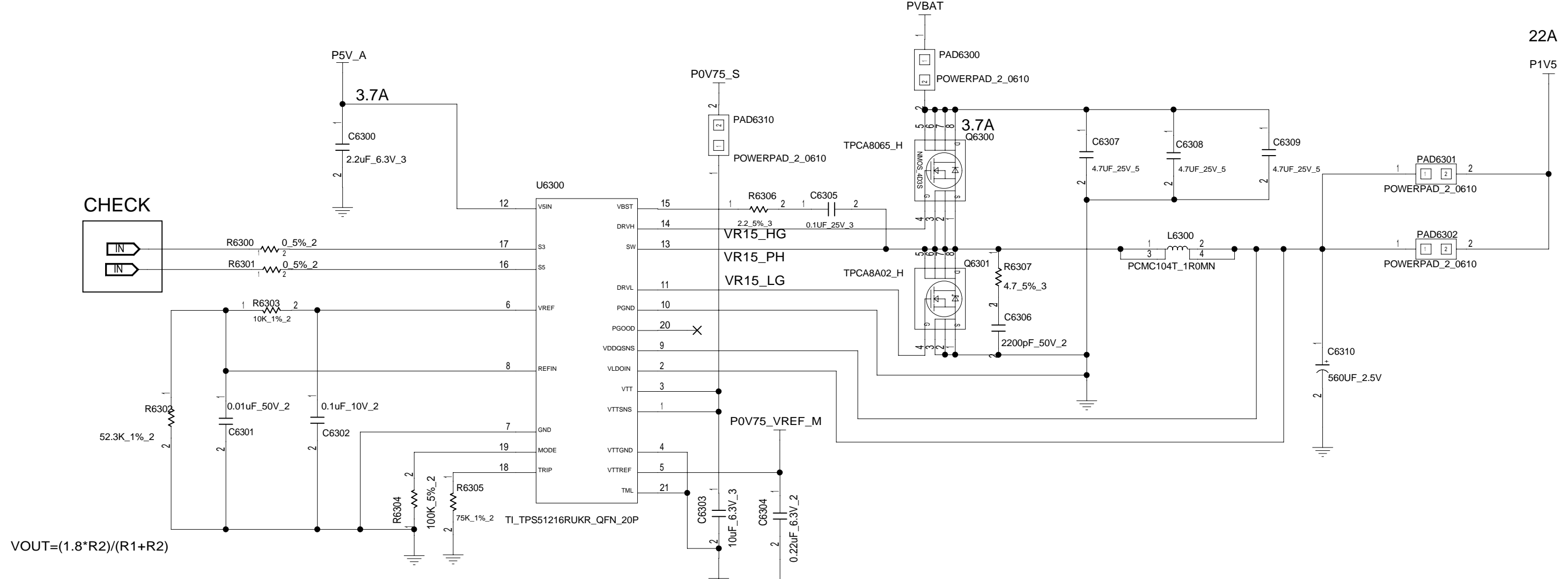
B

A

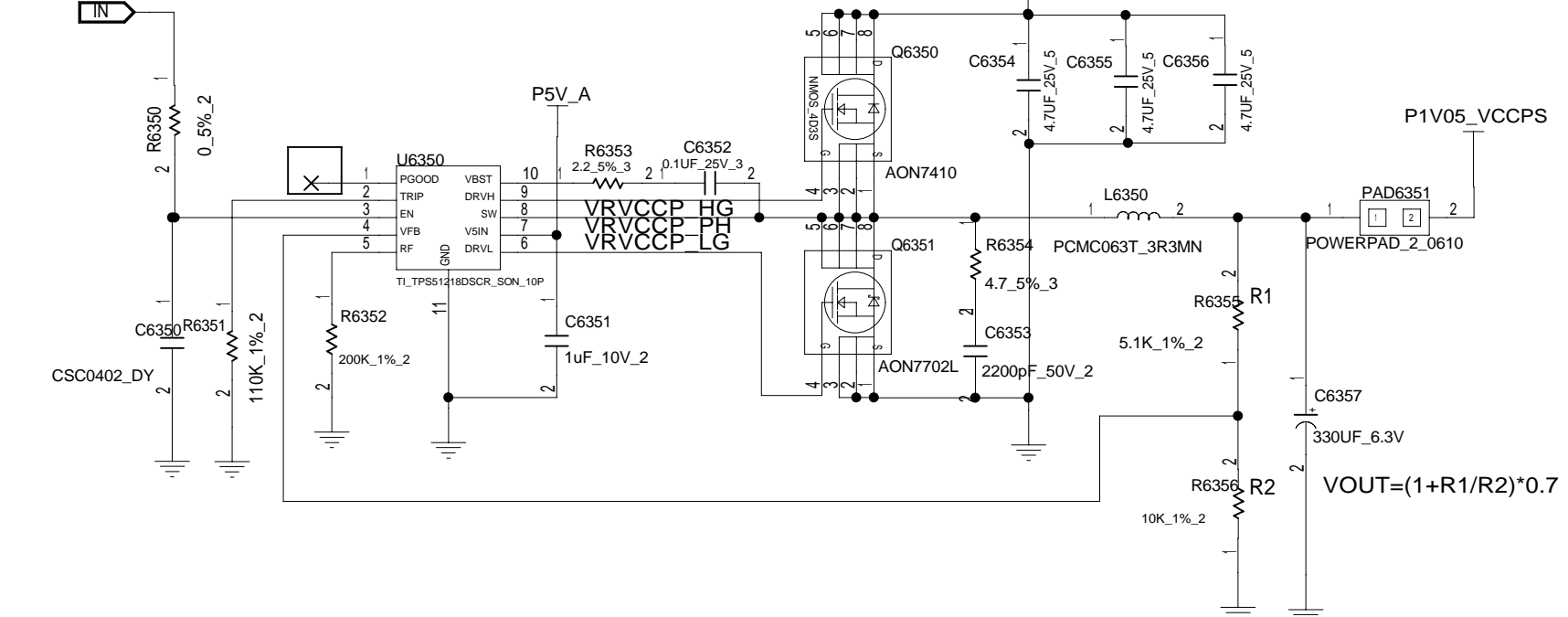
CHECK



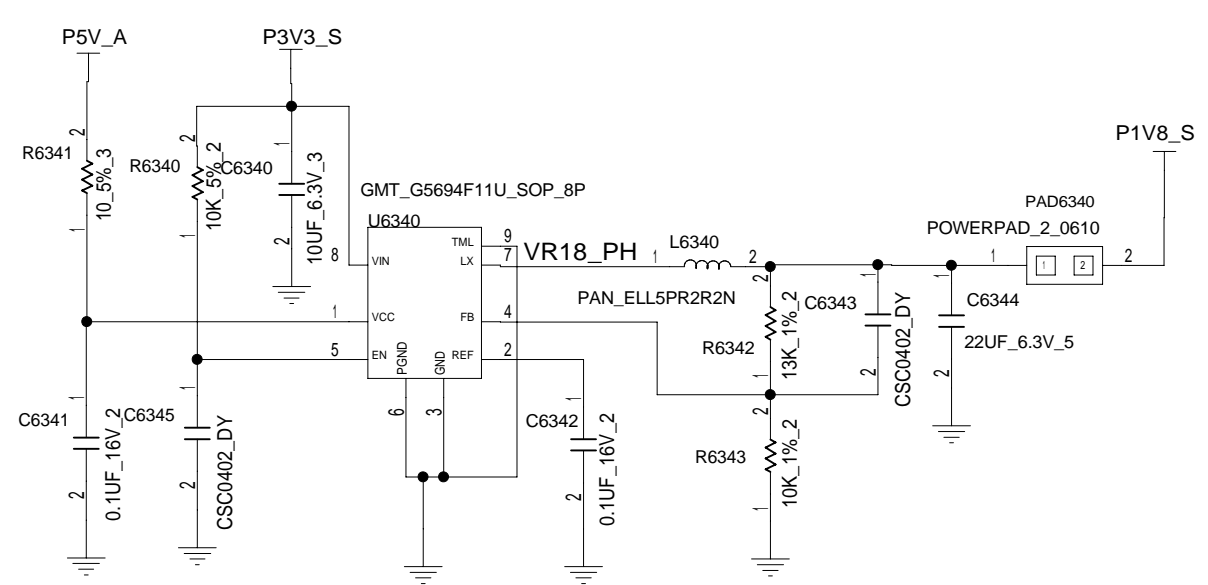
$$V_{OUT} = (1.8 * R_2) / (R_1 + R_2)$$



+V1.05S_VCCP_EN

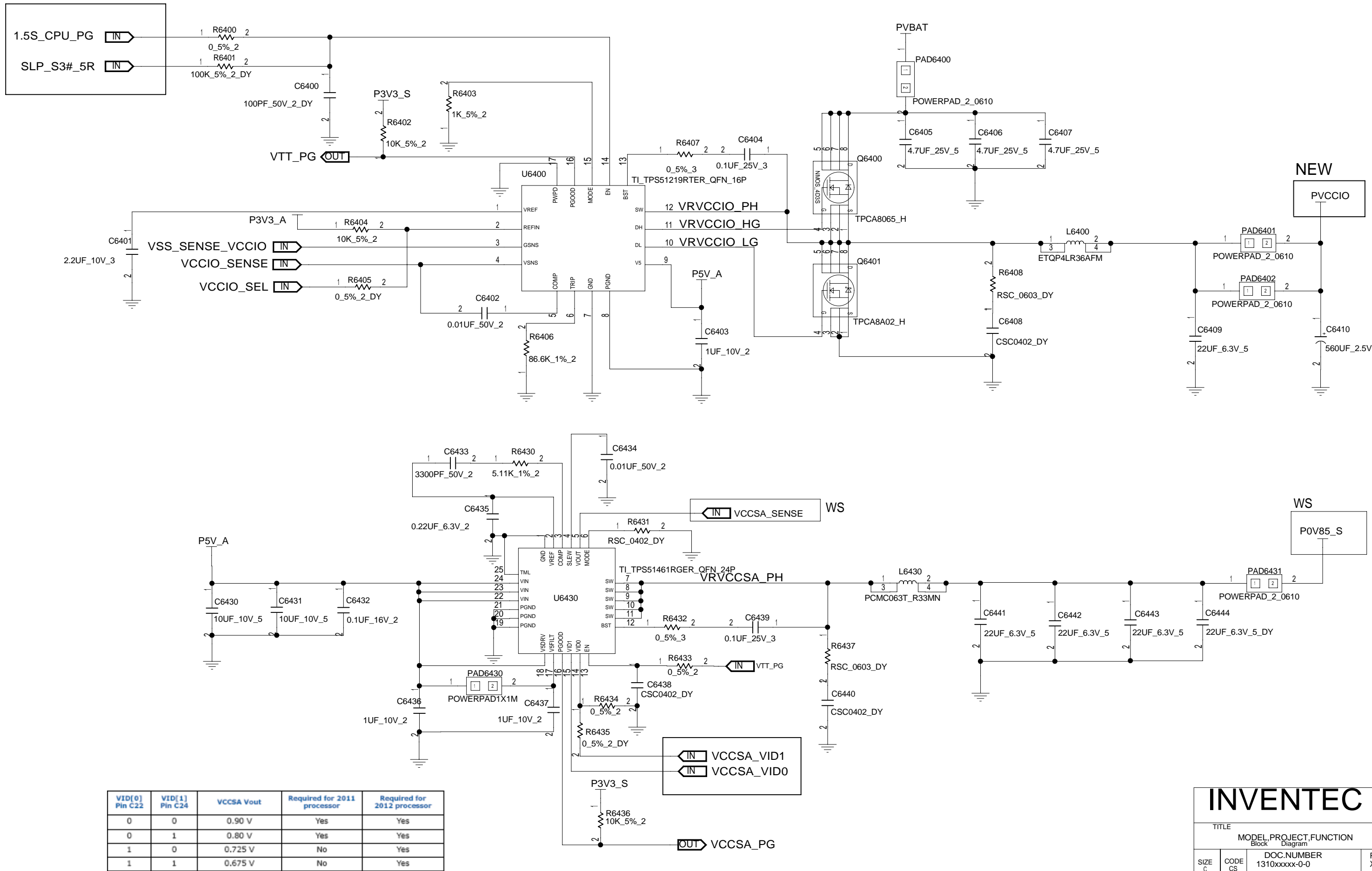


$$V_{OUT} = (1 + R_1/R_2) * 0.7$$



INVENTEC

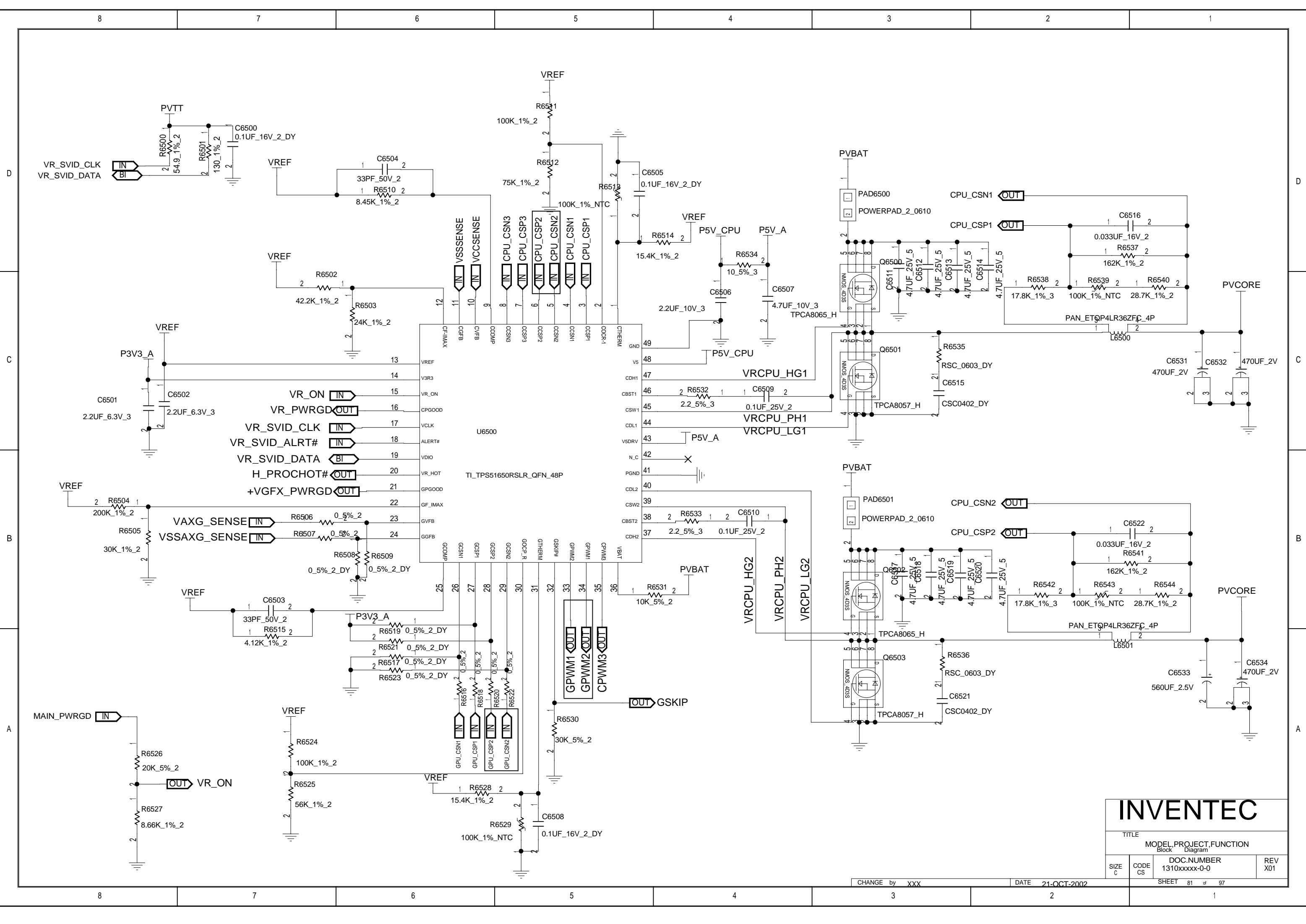
TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC. NUMBER	REV
C	CS	1310xxxx-0-0	X01



VID[0] Pin C22	VID[1] Pin C24	VCCSA Vout	Required for 2011 processor	Required for 2012 processor
0	0	0.90 V	Yes	Yes
0	1	0.80 V	Yes	Yes
1	0	0.725 V	No	Yes
1	1	0.675 V	No	Yes

INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE C	CODE CS	DOC.NUMBER 1310xxxx-0-0	REV X01
CHANGE by XXX		DATE 21-OCT-2002	SHEET 80 of 97

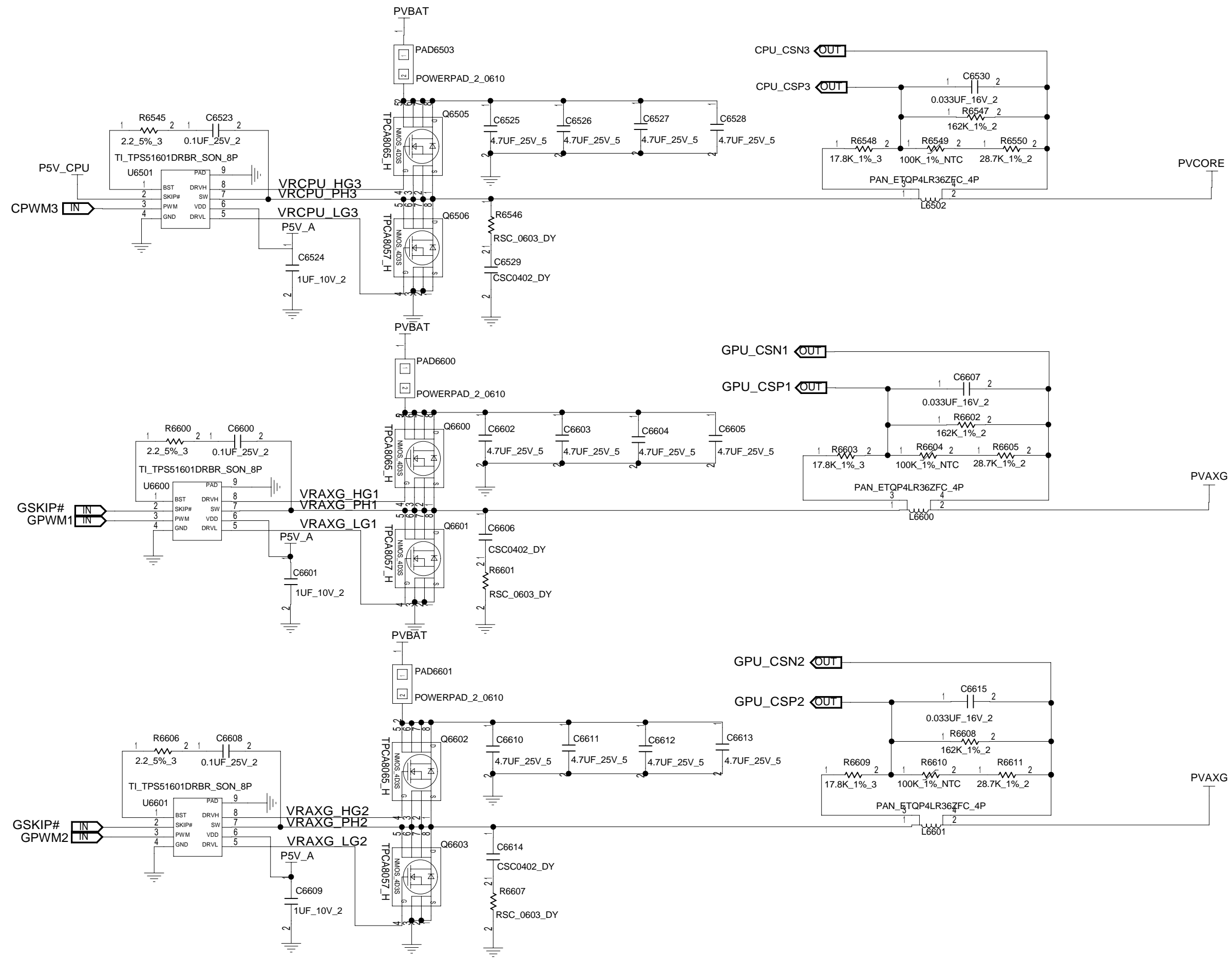


INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

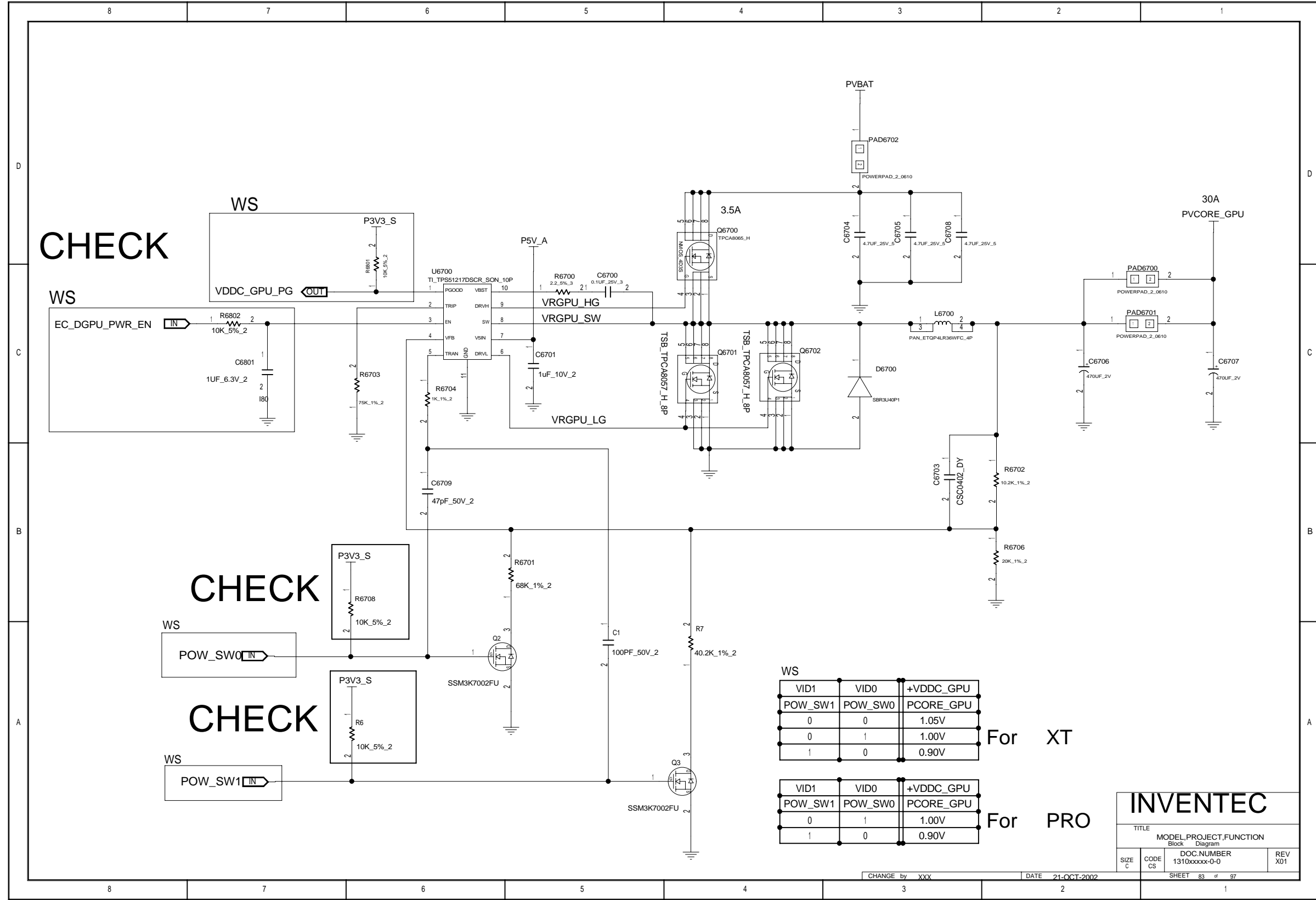
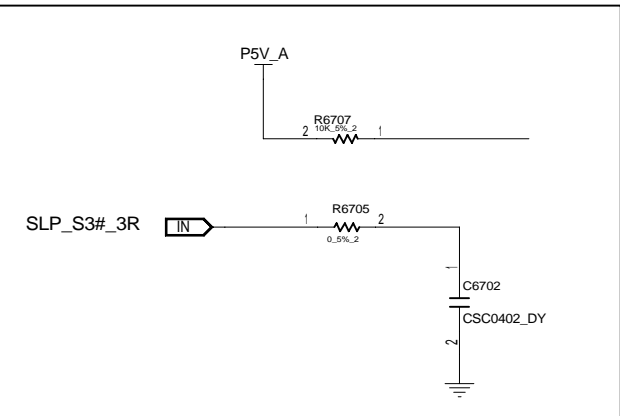
SIZE C	CODE CS	DOC.NUMBER 1310xxxx-0-0	REV X01
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CHANGE by XXX DATE 21-OCT-2002 SHEET 81 of 97



INVENTEC			
TITLE MODEL,PROJECT,FUNCTION Block Diagram			
SIZE C	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
CHANGE by XXX		DATE 21-OCT-2002	
SHEET 82 of 97			

Original Sch



CHECK

CHECK

CHECK

VID1	VID0	+VDDC_GPU
0	0	1.05V
0	1	1.00V
1	0	0.90V

For XT

VID1	VID0	+VDDC_GPU
0	1	1.00V
1	0	0.90V

For PRO

INVENTEC

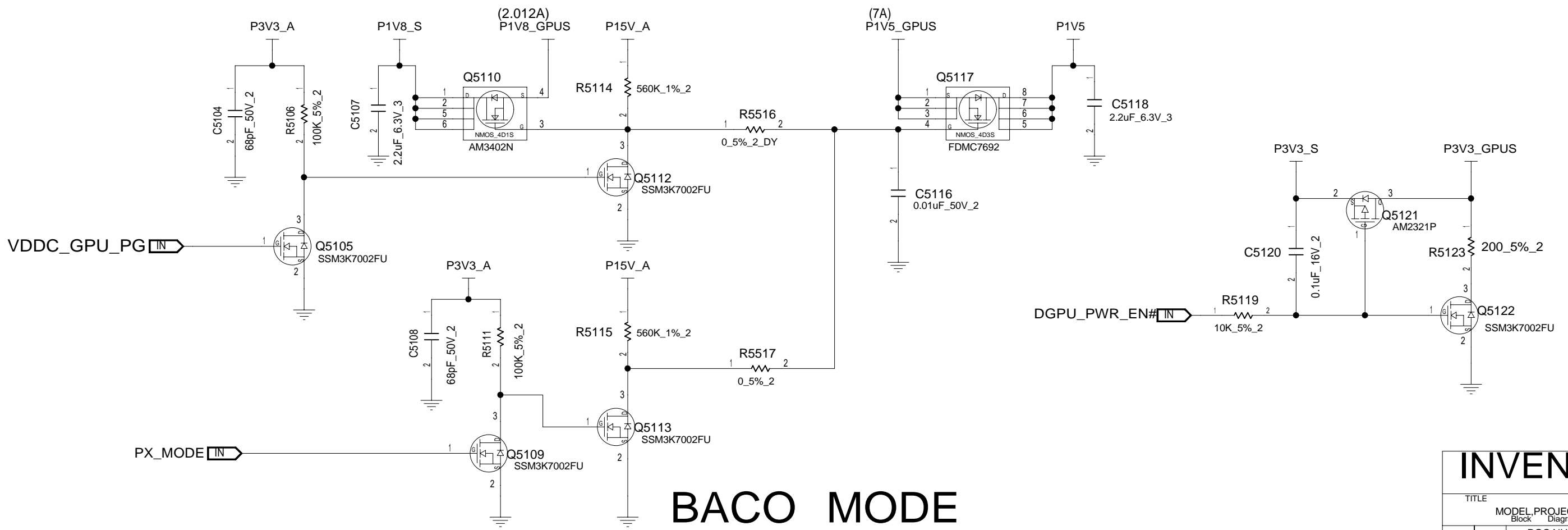
TITLE MODEL,PROJECT,FUNCTION
Block Diagram

SIZE CODE DOC.NUMBER REV
C CS 1310xxxxx-0-0 X01

CHANGE by XXX DATE 21-OCT-2002 SHEET 83 of 97

CONFIGURATION STRAPS: Pin-Based Straps		
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS
TX_PWRS_ENB	GPIO_0	Full Tx output swing=1 (Default) 50% Tx output swing=0
TX_DEEMPH_EN	GPIO_1	Tx De-emphasis enabled=1 (Default) Tx De-emphasis disabled=0
RESERVED	GPIO_2	Advertises the PCIe device as 2.5 GT/s capable at power on=0 Advertises the PCIe device as 5.0 GT/s capable at power on=1 (ASIC Internal pull down, and PCB Default is 0)
RESERVED	GPIO_8	Must be low during reset PCB default is left unconnected
RESERVED	GPIO_21	Must be low during reset (PCB default is 0) Voltage control signal for the memory-voltage regulator.
BIF_VGA_DIS	GPIO_9	VGA controller capacity enabled=0 (Default) VGA controller capacity disabled=1
BIOS_ROM_EN	GPIO_22	Disable the external BIOS ROM device=0 (Default) Enable the external BIOS ROM device=1
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO_13 GPIO_12 GPIO_11	If GPIO_22 = 0, then CONFIG [2:0] defines the primary memory-aperture size. Default is 0 0 1
AUD[0] AUD[1]	HSYNC VSYNC	AUD [1:0]: 0 0 = No audio function 0 1 = Audio for DisplayPort only 1 0 = Audio for DisplayPort and HDMI, if dongle is detected 1 1 = Audio for both DisplayPort and HDMI. (Default is 1 1)
RESERVED	GENLK_CLK	Must be low during reset PCB default is left unconnected

GPU Whistler



BACO MODE

INVENTEC			
TITLE MODEL,PROJECT,FUNCTION Block Diagram			
SIZE C	CODE CS	DOC. NUMBER 1310xxxx-0-0	REV X01
CHANGE by XXX		DATE 21-OCT-2002	SHEET 84 of 97

WHISTLER XT TDP: 30~35 W
 WHISTLER PRO TDP: 20~25 W

U5124

CLOSE TO GPU

D

C

B

A

D

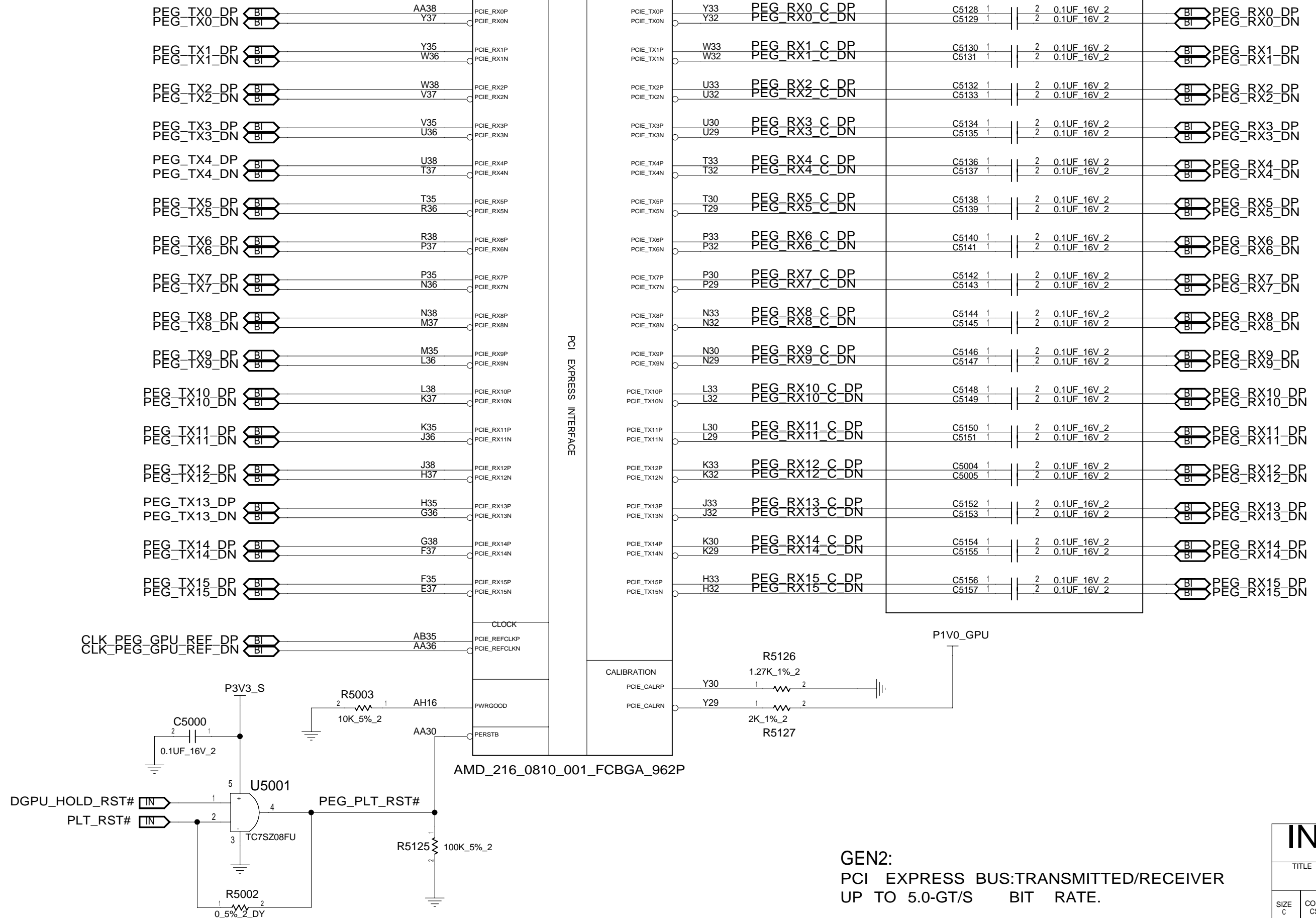
C

B

A

PCI EXPRESS INTERFACE

AMD_216_0810_001_FCBGA_962P



GEN2:
 PCI EXPRESS BUS:TRANSMITTED/RECEIVER
 UP TO 5.0-GT/S BIT RATE.

INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC.NUMBER	REV
C	CS	1310xxxx-0-0	X01
SHEET 85 of 97			

CHANGE by XXX DATE 21-OCT-2002

IF GPU_GPIO22 = 0, THEN GPIO[13:11] DEFINES THE PRIMARY MEMORY APERTURE SIZE

GPU_GPIO13	GPU_GPIO12	GPU_GPIO11	MEMORY APERTURE SIZE
0	0	1	256 MB (DEFAULT)
0	0	0	128 MB
0	1	0	64 MB
0	1	1	32 MB

VID1	VID0	+VDDC_GPU
POW_SW1	POW_SW0	PCORE_GPU
0	0	1.05V
0	1	1.00V
1	0	0.90V

For XT

VID1	VID0	+VDDC_GPU
POW_SW1	POW_SW0	PCORE_GPU
0	1	1.00V
1	0	0.90V

For PRO

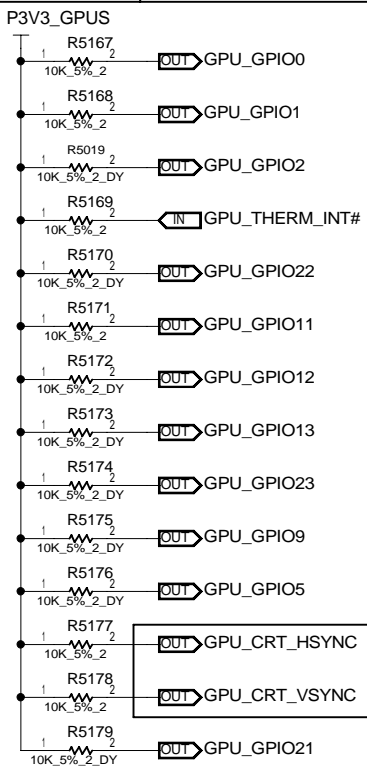
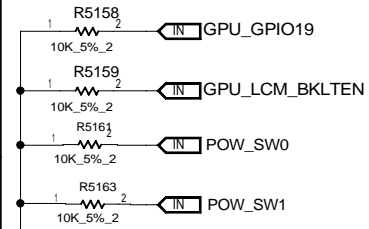
MEM_ID3	MEM_ID2	MEM_ID1	MEM_ID0	Vendor (GDDR5)
0	0	1	1	HYNIX (1GB)
0	0	0	1	SAMSUNG (1GB)

U5124

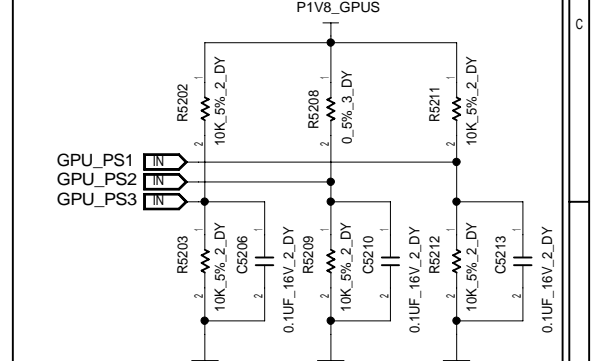
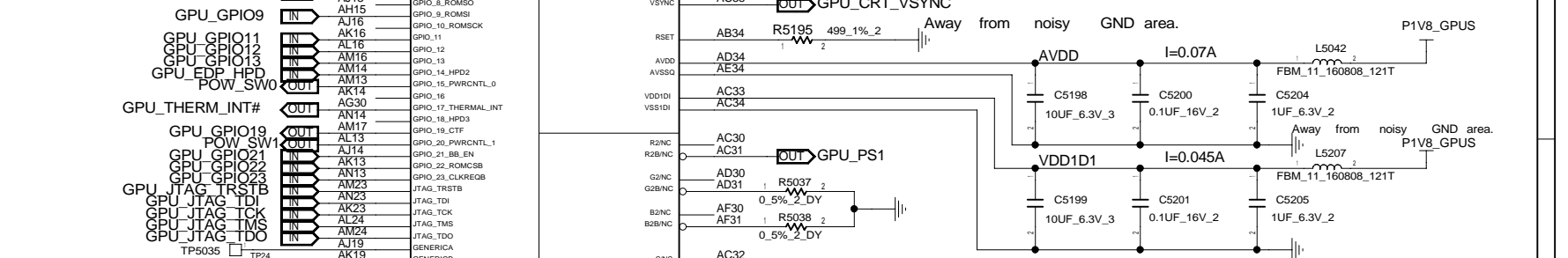
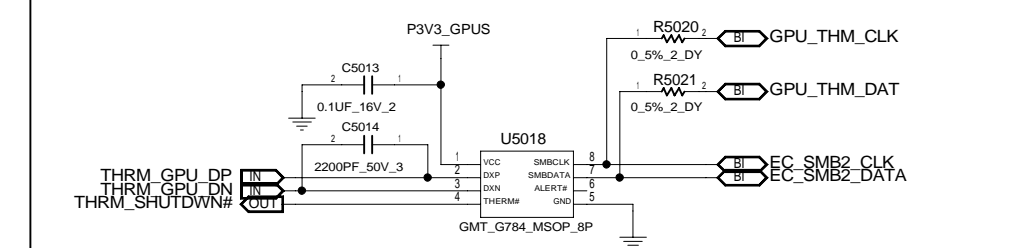
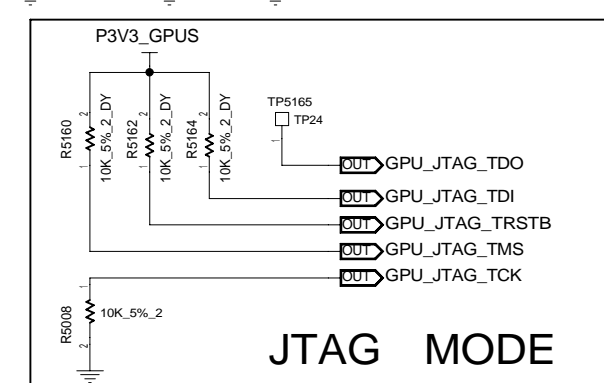
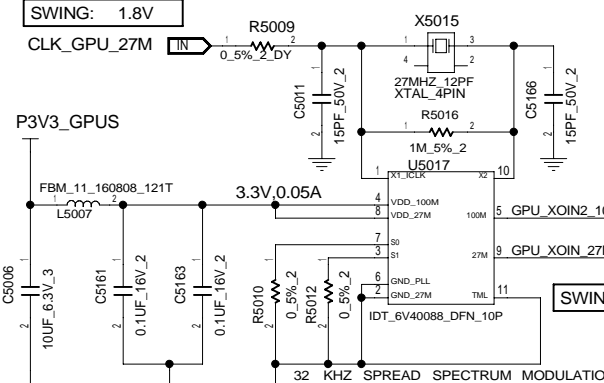
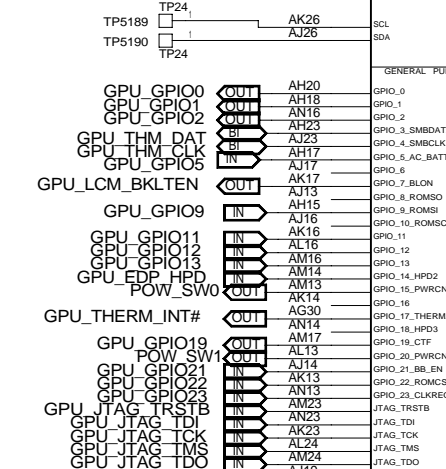
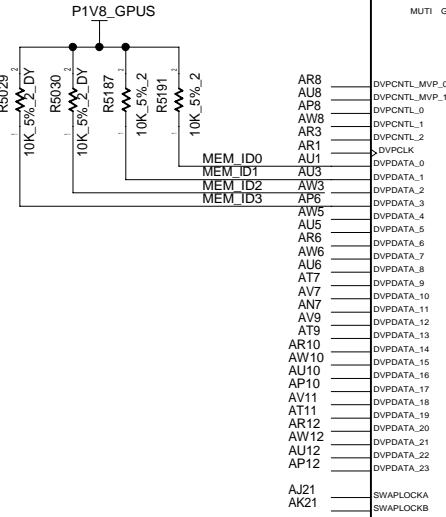
HDMI

EDP DUAL CHANNEL FOR 3D FUNCTION

CRT



HDMI&DP Audio



FUTURE ASIC
GPU Multi Level Pin Straps feature

AMD_216_0810_001_FCBGA_962P

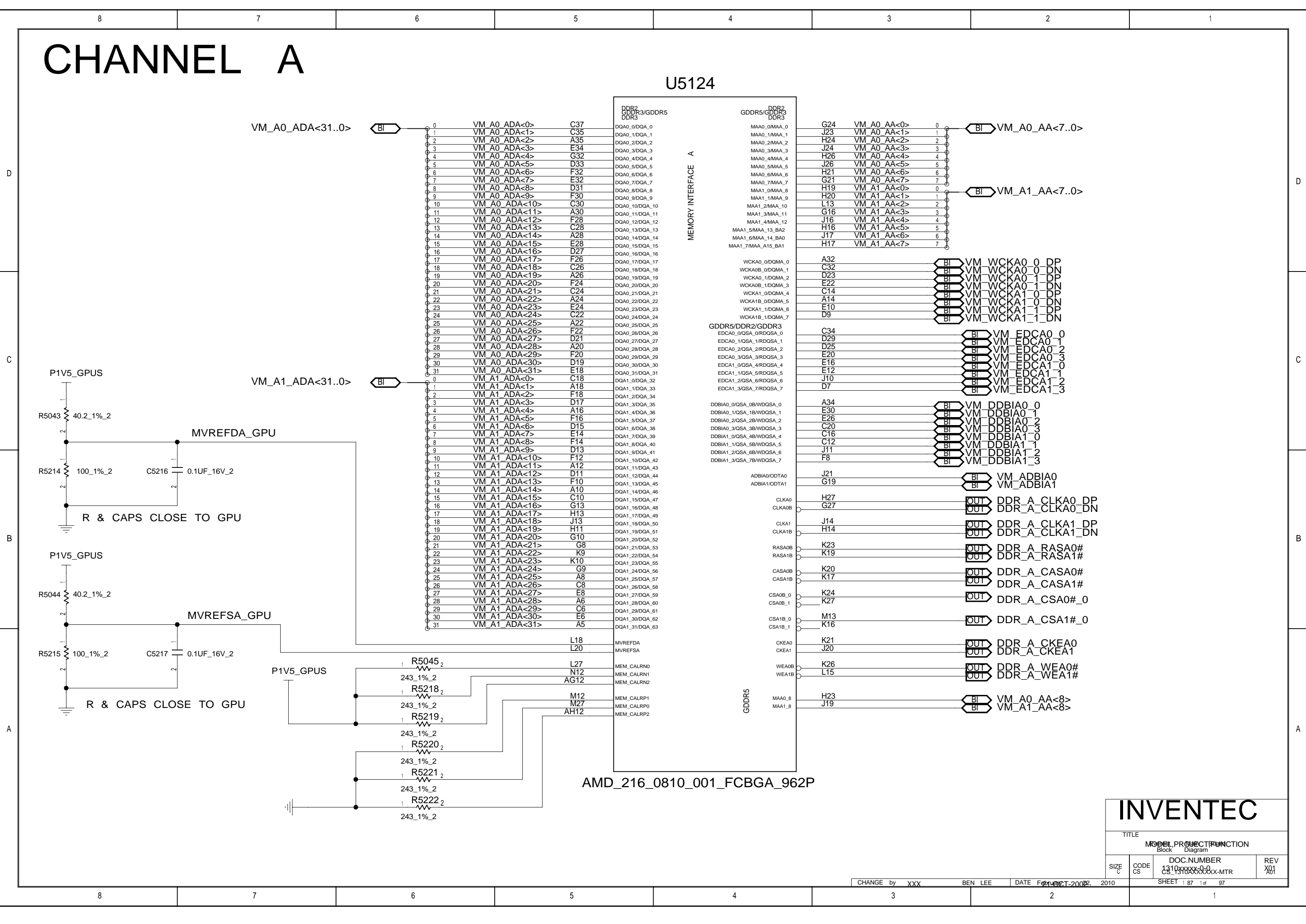
INVENTEC

TITLE	MODEL	PROJECT	FUNCTION
	Block	Diagram	
SIZE	CODE	DOC NUMBER	REV
C	CS	CS_1319XXXXX-MTR	V01
SHEET	86	1 of 97	

CHANGE BY XEN LEE DATE 21/01/2022

CHANNEL A

U5124



AMD_216_0810_001_FCBGA_962P

INVENTEC

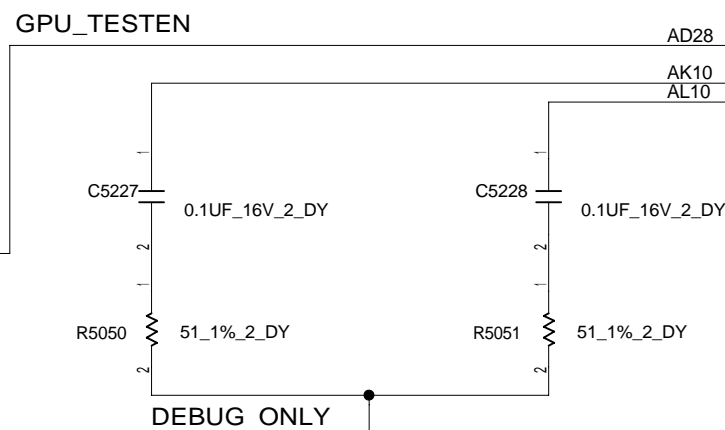
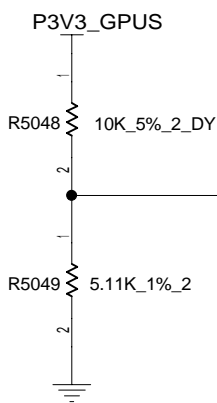
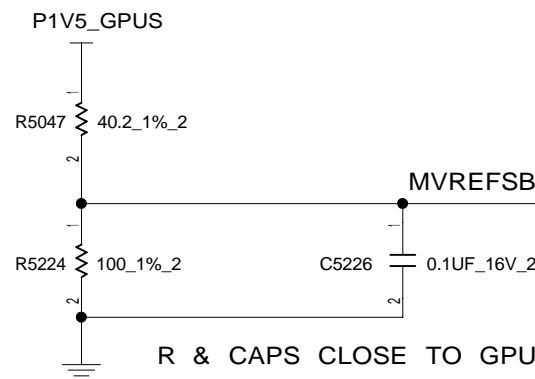
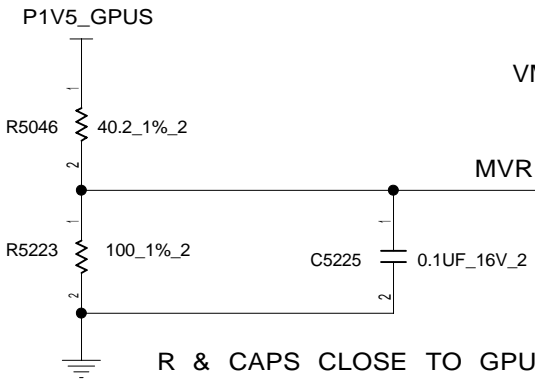
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MODEL PROJECT FUNCTION			
Block Diagram			
SIZE	CODE	DOC. NUMBER	REV
C	CS	1310xxxx-00	X01
CS_1310XXXX-MTR			

CHANNEL B

U5124

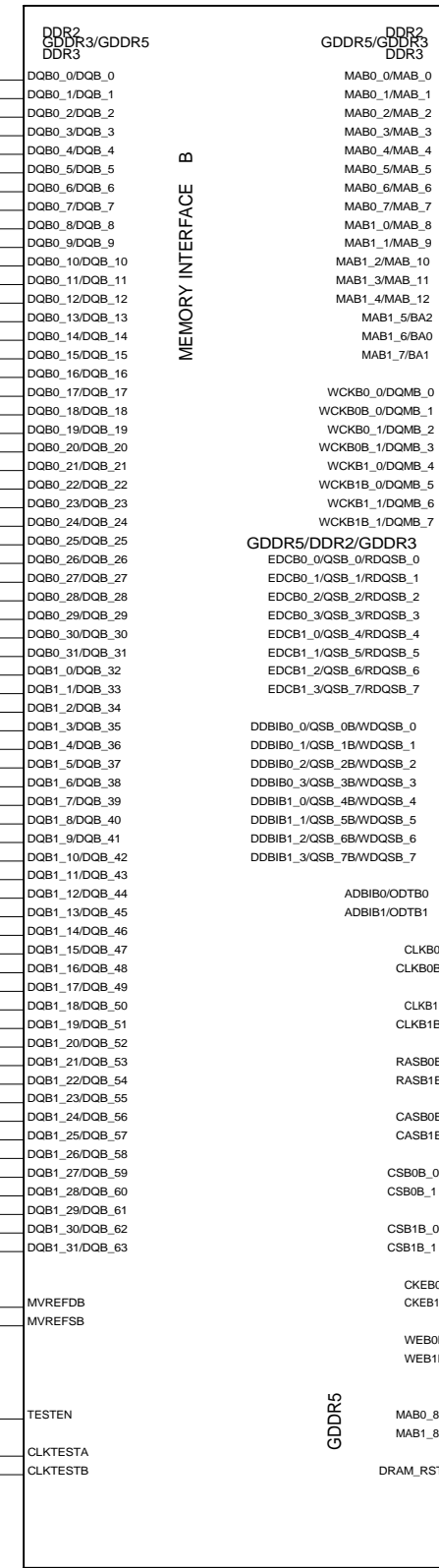
VM_B0_ADA<31..0>

VM_B1_ADA<31..0>



JTAG SIGNAL	STUFF	OPTION
SIGNALS	NORMAL MODE	JTAG MODE
GPU_TESTEN	0	1

Pin	Signal	Pin	Signal
0	VM B0 ADA<0>	C5	VM B0 ADA<0>
1	VM B0 ADA<1>	C3	VM B0 ADA<1>
2	VM B0 ADA<2>	E3	VM B0 ADA<2>
3	VM B0 ADA<3>	E1	VM B0 ADA<3>
4	VM B0 ADA<4>	F1	VM B0 ADA<4>
5	VM B0 ADA<5>	F3	VM B0 ADA<5>
6	VM B0 ADA<6>	F5	VM B0 ADA<6>
7	VM B0 ADA<7>	G4	VM B0 ADA<7>
8	VM B0 ADA<8>	H5	VM B0 ADA<8>
9	VM B0 ADA<9>	H6	VM B0 ADA<9>
10	VM B0 ADA<10>	J4	VM B0 ADA<10>
11	VM B0 ADA<11>	K6	VM B0 ADA<11>
12	VM B0 ADA<12>	K5	VM B0 ADA<12>
13	VM B0 ADA<13>	L4	VM B0 ADA<13>
14	VM B0 ADA<14>	M6	VM B0 ADA<14>
15	VM B0 ADA<15>	M1	VM B0 ADA<15>
16	VM B0 ADA<16>	M3	VM B0 ADA<16>
17	VM B0 ADA<17>	M5	VM B0 ADA<17>
18	VM B0 ADA<18>	N4	VM B0 ADA<18>
19	VM B0 ADA<19>	P6	VM B0 ADA<19>
20	VM B0 ADA<20>	P5	VM B0 ADA<20>
21	VM B0 ADA<21>	R4	VM B0 ADA<21>
22	VM B0 ADA<22>	T6	VM B0 ADA<22>
23	VM B0 ADA<23>	T1	VM B0 ADA<23>
24	VM B0 ADA<24>	U4	VM B0 ADA<24>
25	VM B0 ADA<25>	V6	VM B0 ADA<25>
26	VM B0 ADA<26>	V1	VM B0 ADA<26>
27	VM B0 ADA<27>	V3	VM B0 ADA<27>
28	VM B0 ADA<28>	Y6	VM B0 ADA<28>
29	VM B0 ADA<29>	Y1	VM B0 ADA<29>
30	VM B0 ADA<30>	Y3	VM B0 ADA<30>
31	VM B0 ADA<31>	Y5	VM B0 ADA<31>
0	VM B1 ADA<0>	AA4	VM B1 ADA<0>
1	VM B1 ADA<1>	AB6	VM B1 ADA<1>
2	VM B1 ADA<2>	AB1	VM B1 ADA<2>
3	VM B1 ADA<3>	AB3	VM B1 ADA<3>
4	VM B1 ADA<4>	AD6	VM B1 ADA<4>
5	VM B1 ADA<5>	AD1	VM B1 ADA<5>
6	VM B1 ADA<6>	AD3	VM B1 ADA<6>
7	VM B1 ADA<7>	AD5	VM B1 ADA<7>
8	VM B1 ADA<8>	AF1	VM B1 ADA<8>
9	VM B1 ADA<9>	AF3	VM B1 ADA<9>
10	VM B1 ADA<10>	AF6	VM B1 ADA<10>
11	VM B1 ADA<11>	AG4	VM B1 ADA<11>
12	VM B1 ADA<12>	AH5	VM B1 ADA<12>
13	VM B1 ADA<13>	AH6	VM B1 ADA<13>
14	VM B1 ADA<14>	AJ4	VM B1 ADA<14>
15	VM B1 ADA<15>	AK3	VM B1 ADA<15>
16	VM B1 ADA<16>	AF8	VM B1 ADA<16>
17	VM B1 ADA<17>	AF9	VM B1 ADA<17>
18	VM B1 ADA<18>	AG8	VM B1 ADA<18>
19	VM B1 ADA<19>	AG7	VM B1 ADA<19>
20	VM B1 ADA<20>	AK9	VM B1 ADA<20>
21	VM B1 ADA<21>	AL7	VM B1 ADA<21>
22	VM B1 ADA<22>	AM8	VM B1 ADA<22>
23	VM B1 ADA<23>	AM7	VM B1 ADA<23>
24	VM B1 ADA<24>	AK1	VM B1 ADA<24>
25	VM B1 ADA<25>	AL4	VM B1 ADA<25>
26	VM B1 ADA<26>	AM6	VM B1 ADA<26>
27	VM B1 ADA<27>	AM1	VM B1 ADA<27>
28	VM B1 ADA<28>	AN4	VM B1 ADA<28>
29	VM B1 ADA<29>	AP3	VM B1 ADA<29>
30	VM B1 ADA<30>	AP1	VM B1 ADA<30>
31	VM B1 ADA<31>	AP5	VM B1 ADA<31>



AMD_216_0810_001_FCBGA_962P

PLACE ALL THESE COMPONENTS VERY CLOSE TO GPU (WITHIN 25MM) AND KEEP ALL COMPONENT CLOSE TO EACH OTHER. (WITHIN 5MM) EXCEPT RSER2

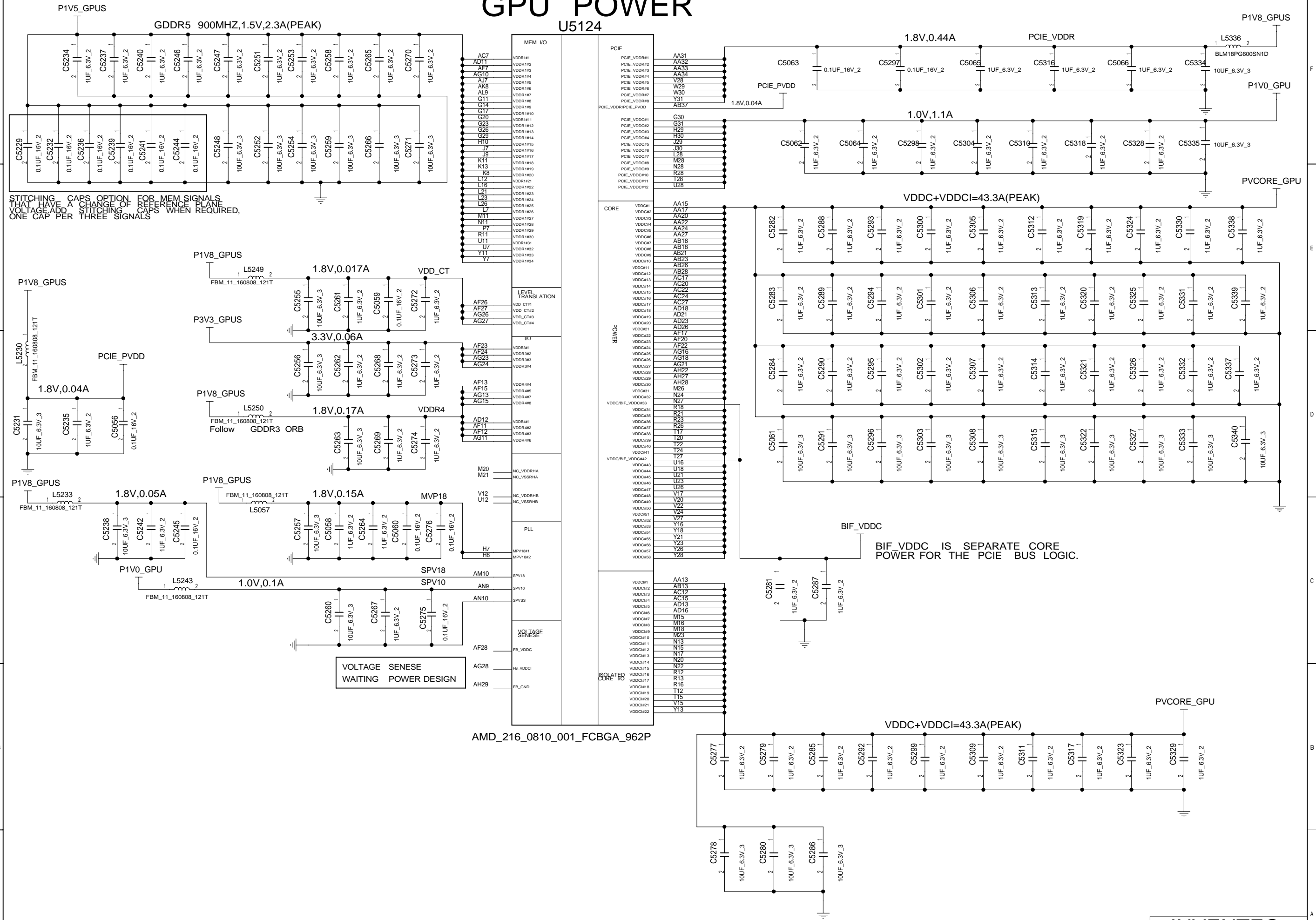
INVENTEC

TITLE			
MODEL PROJECT FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
C	CS	1310xxxx-00	X01
CS-1310XXXXXX-MTR			

GPU POWER

U5124

AMD_216_0810_001_FCBGA_962P



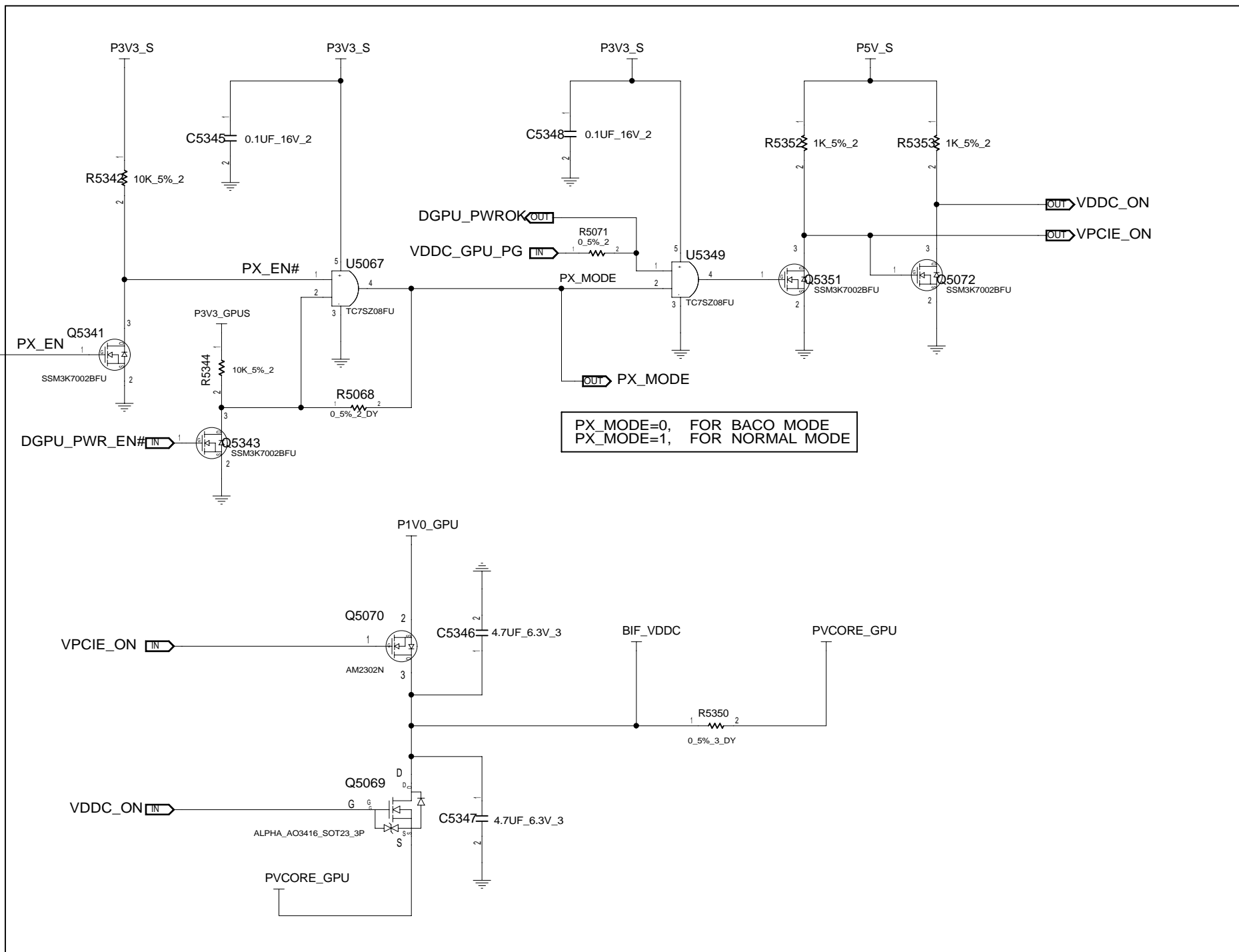
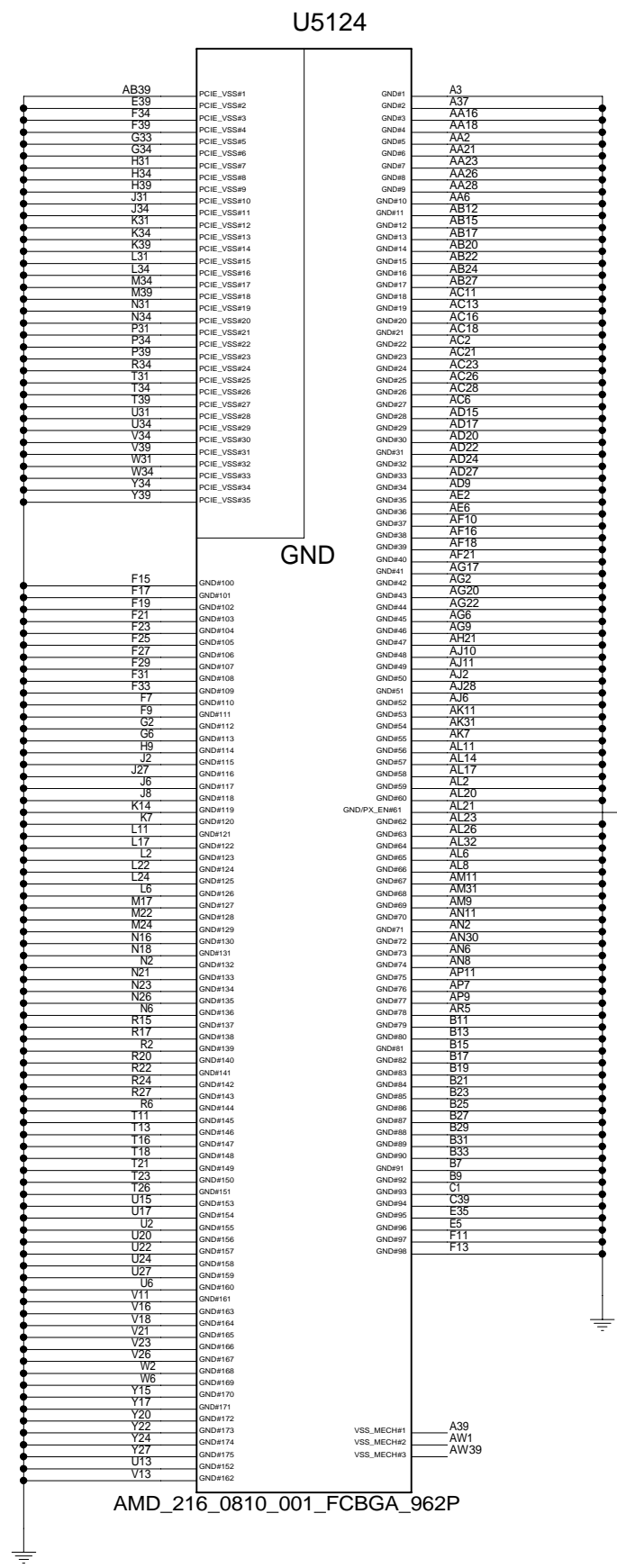
STITCHING CAPS OPTION FOR MEM SIGNALS THAT HAVE A CHANGE OF REFERENCE PLANE. VOLTAGE ADD SWITCHING CAPS WHEN REQUIRED. ONE CAP PER THREE SIGNALS

VOLTAGE SENESE WAITING POWER DESIGN

BIF VDDC IS SEPARATE CORE POWER FOR THE PCIE BUS LOGIC.

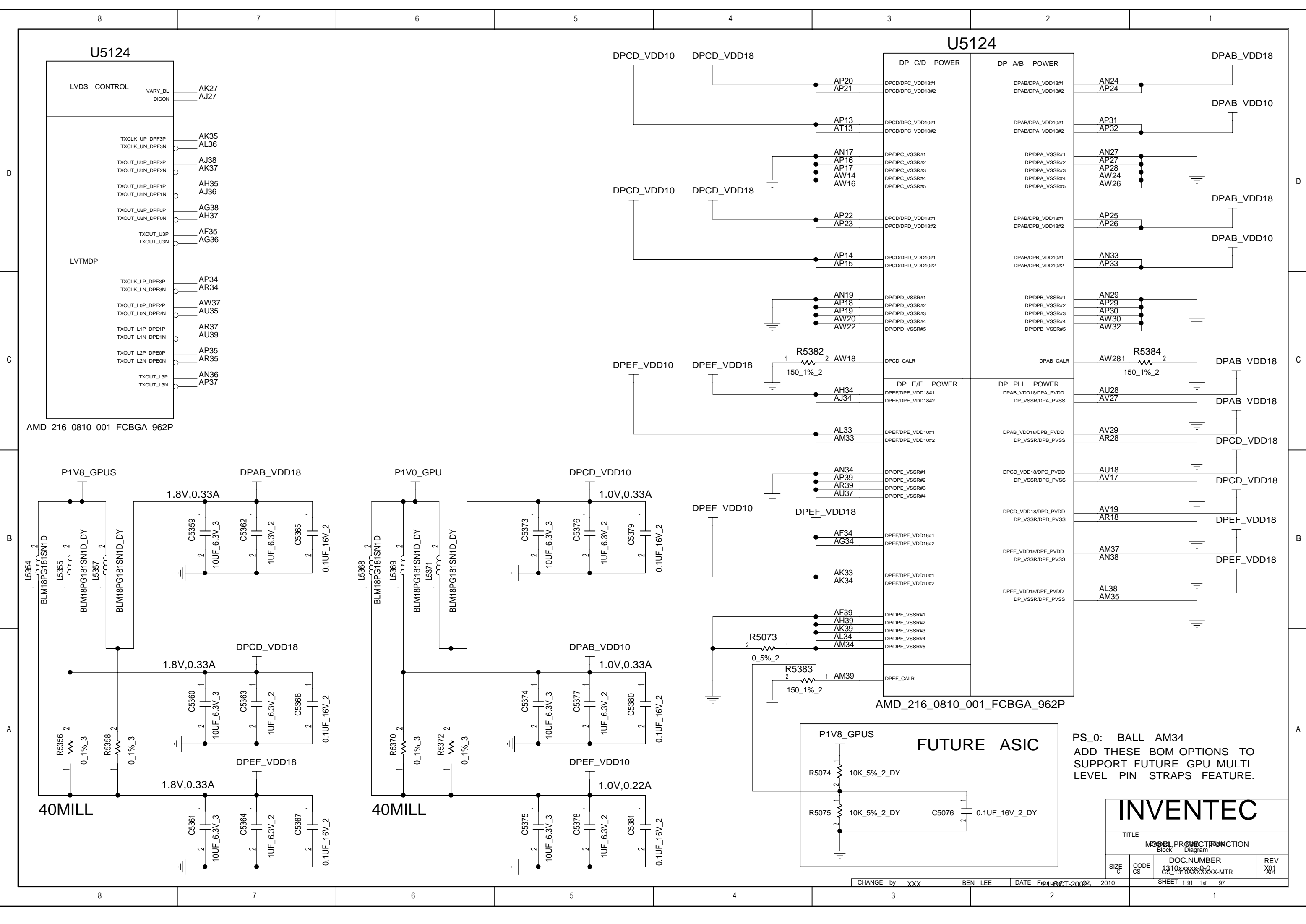
INVENTEC			
MODEL PROJECT FUNCTION Block Diagram			
SIZE C	CODE CS	DOC NUMBER CS_13194XXXX-MTR	REV 1.0
SHEET 89		of 97	

BACO



INVENTEC			
TITLE: MODEL PROTECTION FUNCTION			
Block Diagram			
SIZE: C	CODE: CS	DOC NUMBER: CS_1314XXXX-MTR	REV: 1
SHEET: 90		of 97	

CHANGE by: X BEN LEE DATE: 21/09/2022



U5124

LVDS CONTROL		VARY_BL	AK27
		DIGON	AJ27
TXCLK_UP_DPF3P	AK35		
TXCLK_UN_DPF3N	AL36		
TXOUT_U0P_DPF2P	AJ38		
TXOUT_U0N_DPF2N	AK37		
TXOUT_U1P_DPF1P	AH35		
TXOUT_U1N_DPF1N	AJ36		
TXOUT_U2P_DPF0P	AG38		
TXOUT_U2N_DPF0N	AH37		
TXOUT_U3P	AF35		
TXOUT_U3N	AG36		
LVTMDP			
TXCLK_LP_DPE3P	AP34		
TXCLK_LN_DPE3N	AR34		
TXOUT_L0P_DPE2P	AW37		
TXOUT_L0N_DPE2N	AU35		
TXOUT_L1P_DPE1P	AR37		
TXOUT_L1N_DPE1N	AU39		
TXOUT_L2P_DPE0P	AP35		
TXOUT_L2N_DPE0N	AR35		
TXOUT_L3P	AN36		
TXOUT_L3N	AP37		

U5124

DP C/D POWER		DPAB/DPA_VDD18#1	AN24
		DPAB/DPA_VDD18#2	AP24
		DPAB/DPA_VDD10#1	AP31
		DPAB/DPA_VDD10#2	AP32
		DPAB/DPA_VDD18	AN27
		DPAB/DPA_VDD18	AP27
		DPAB/DPA_VDD18	AP28
		DPAB/DPA_VDD18	AW24
		DPAB/DPA_VDD18	AW26
		DPAB/DPB_VDD18#1	AP25
		DPAB/DPB_VDD18#2	AP26
		DPAB/DPB_VDD10#1	AN33
		DPAB/DPB_VDD10#2	AP33
		DP/DPB_VSSR#1	AN29
		DP/DPB_VSSR#2	AP29
		DP/DPB_VSSR#3	AP30
		DP/DPB_VSSR#4	AW30
		DP/DPB_VSSR#5	AW32
DPAB_CALR		AW28	AW28
		AW27	AW27
		AV29	AV29
		AR28	AR28
		AU18	AU18
		AV17	AV17
		AV19	AV19
		AR18	AR18
		AM37	AM37
		AN38	AN38
		AL38	AL38
		AM35	AM35
DP E/F POWER		DP/DPE_VSSR#1	AN34
		DP/DPE_VSSR#2	AP39
		DP/DPE_VSSR#3	AR39
		DP/DPE_VSSR#4	AU37
DPAB_CALR		AM39	AM39

PS_0: BALL AM34
 ADD THESE BOM OPTIONS TO SUPPORT FUTURE GPU MULTI LEVEL PIN STRAPS FEATURE.

INVENTEC

TITLE			
MODEL PROJECT FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
C	CS	1310xxxx-00	X01
SHEET 1 of 97			

GDDR5 CHANNEL A MEMORY

U5089

U5094

P1V5_GPUS

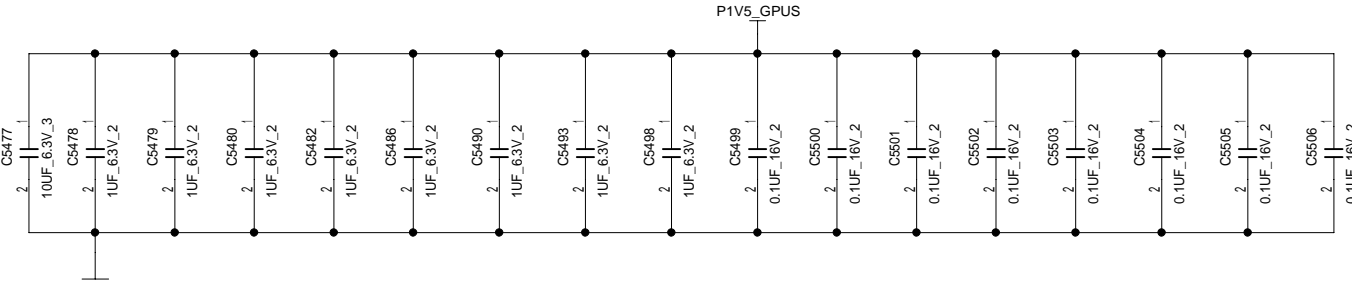
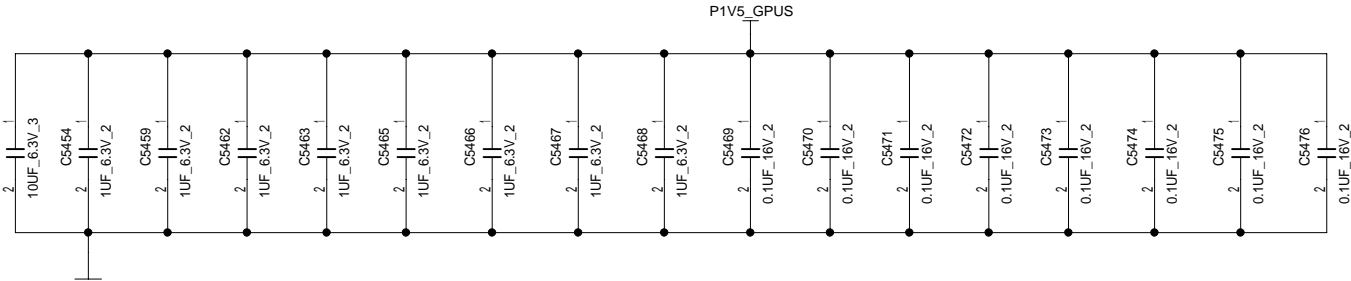
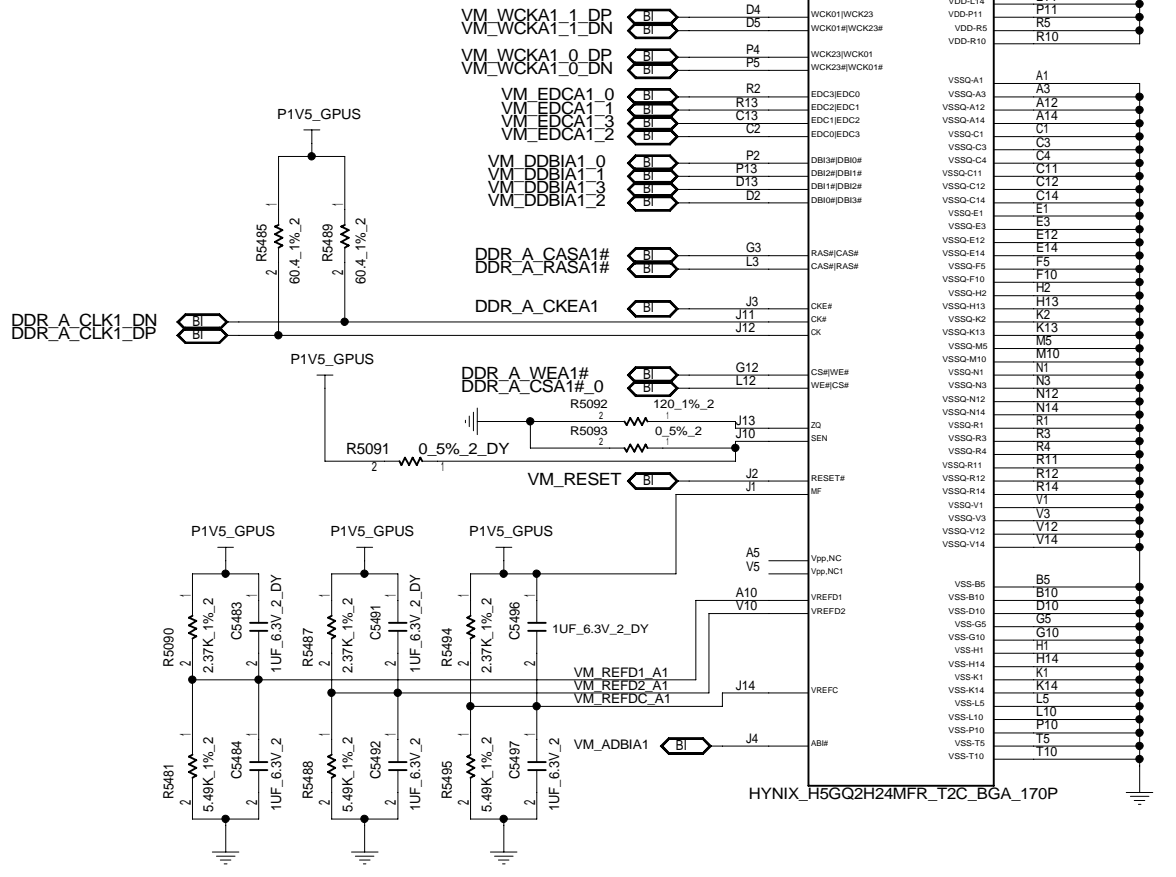
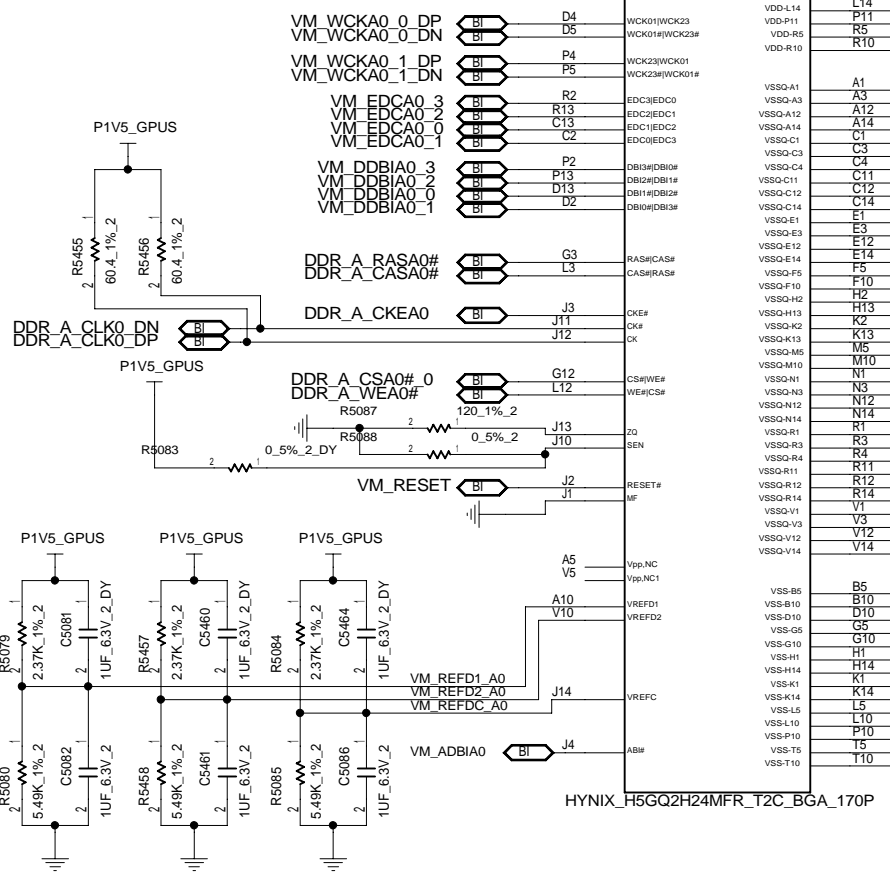
P1V5_GPUS

VM_A0_ADA<31..0>

VM_A1_ADA<31..0>

VM_A0_AA<8>
VM_A0_AA<7..0>

VM_A1_AA<8>
VM_A1_AA<7..0>

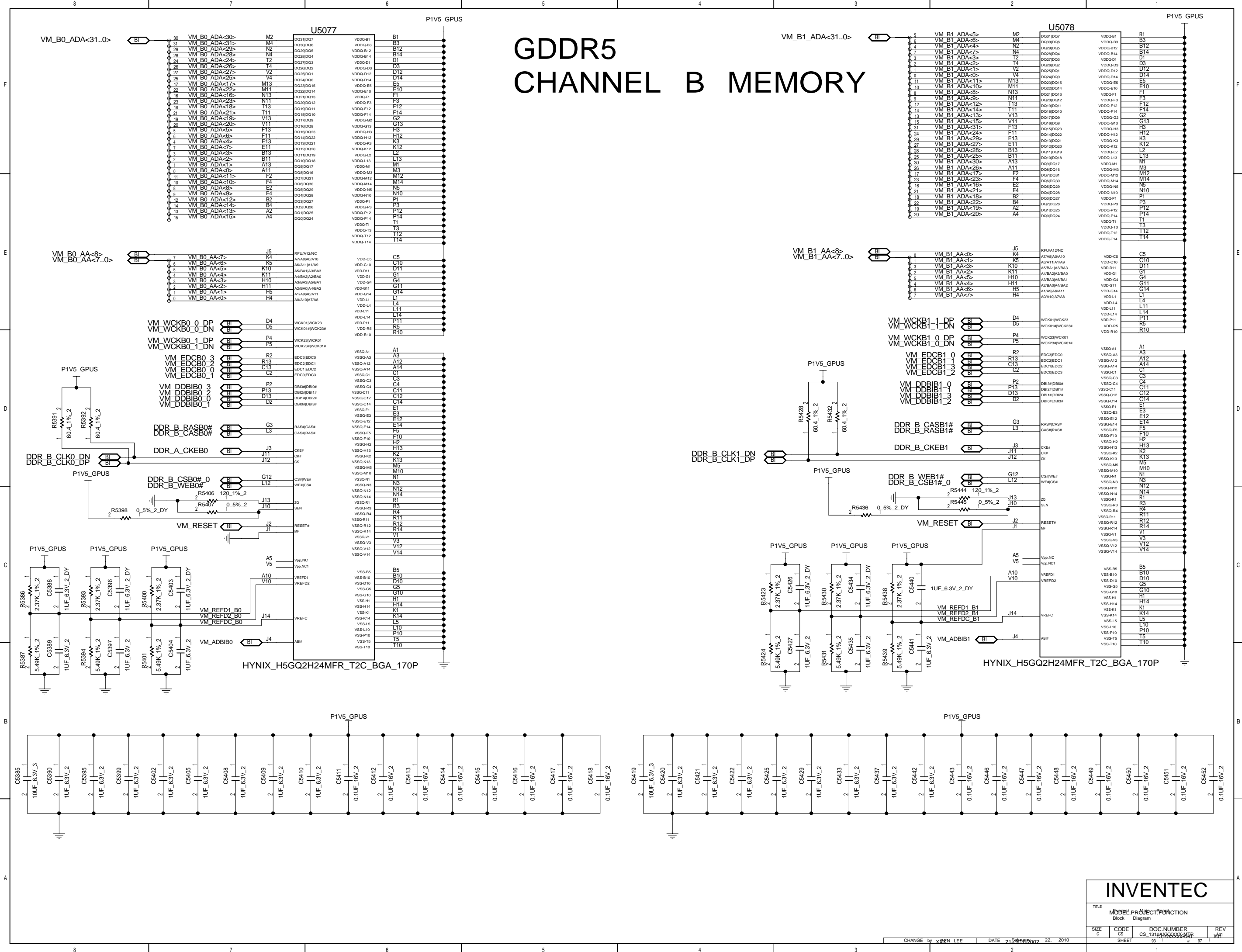


INVENTEC

TITLE	MODEL PROJECT FUNCTION			
Block	Diagram			
SIZE	CODE	DOC NUMBER	REV	
C	CS	CS_1314XXXX-MTR	1	01
SHEET		92	of 97	

CHANGE by: X BEN LEE DATE: 21/04/2022

GDDR5 CHANNEL B MEMORY



INVENTEC

TITLE			
MODEL PROJECT FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
C	CS	CS_1319XXXX-MTR	01
SHEET		93	of 97

CHANGE by XEN LEE DATE 21/04/2022 22, 2020

D

C

B

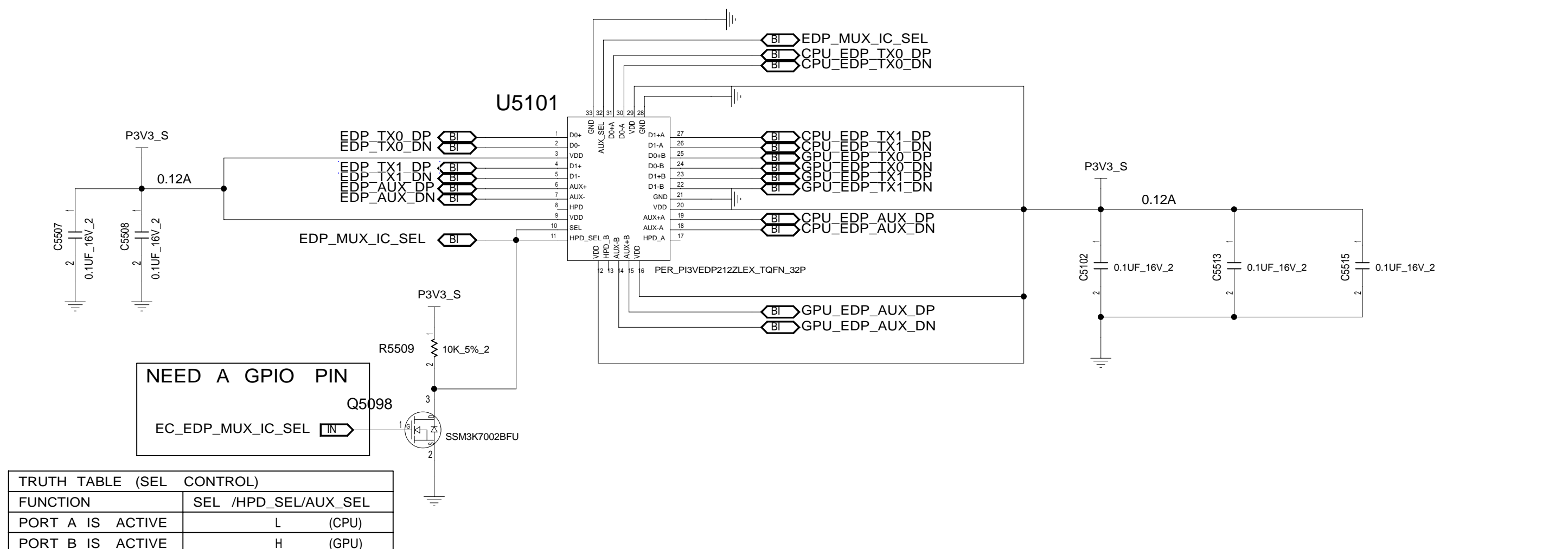
A

D

C

B

A



NEED A GPIO PIN

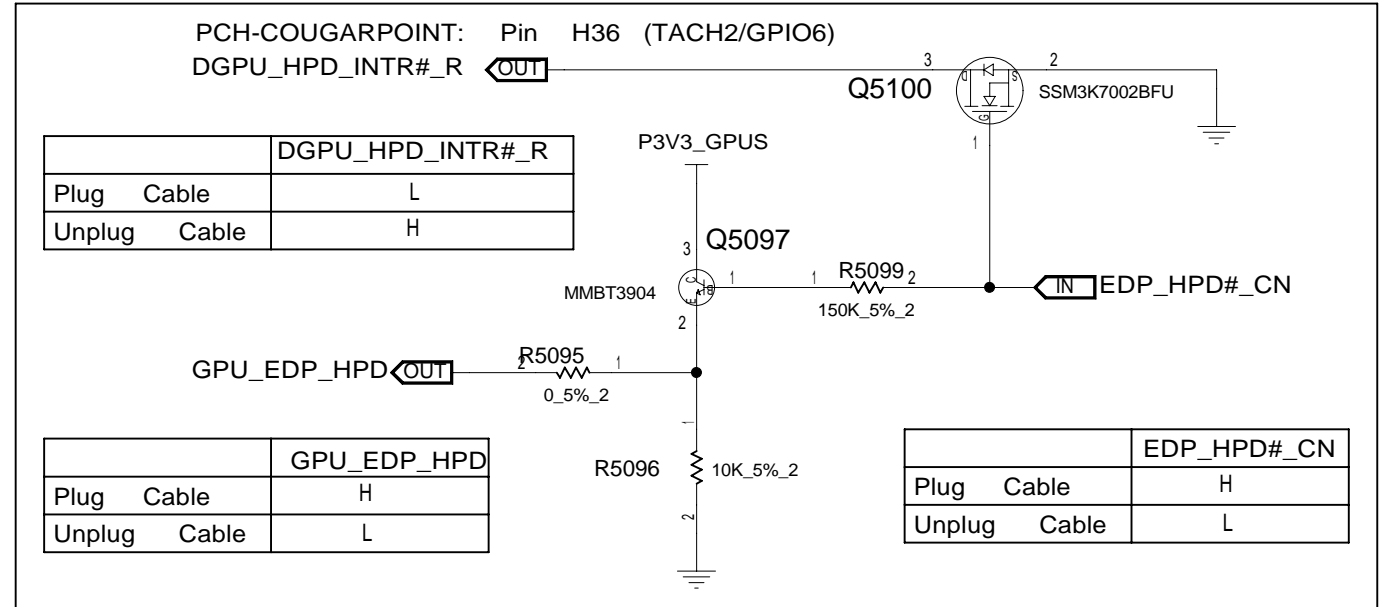
EC_EDP_MUX_IC_SEL IN

Q5098

SSM3K7002BFU

TRUTH TABLE (SEL CONTROL)

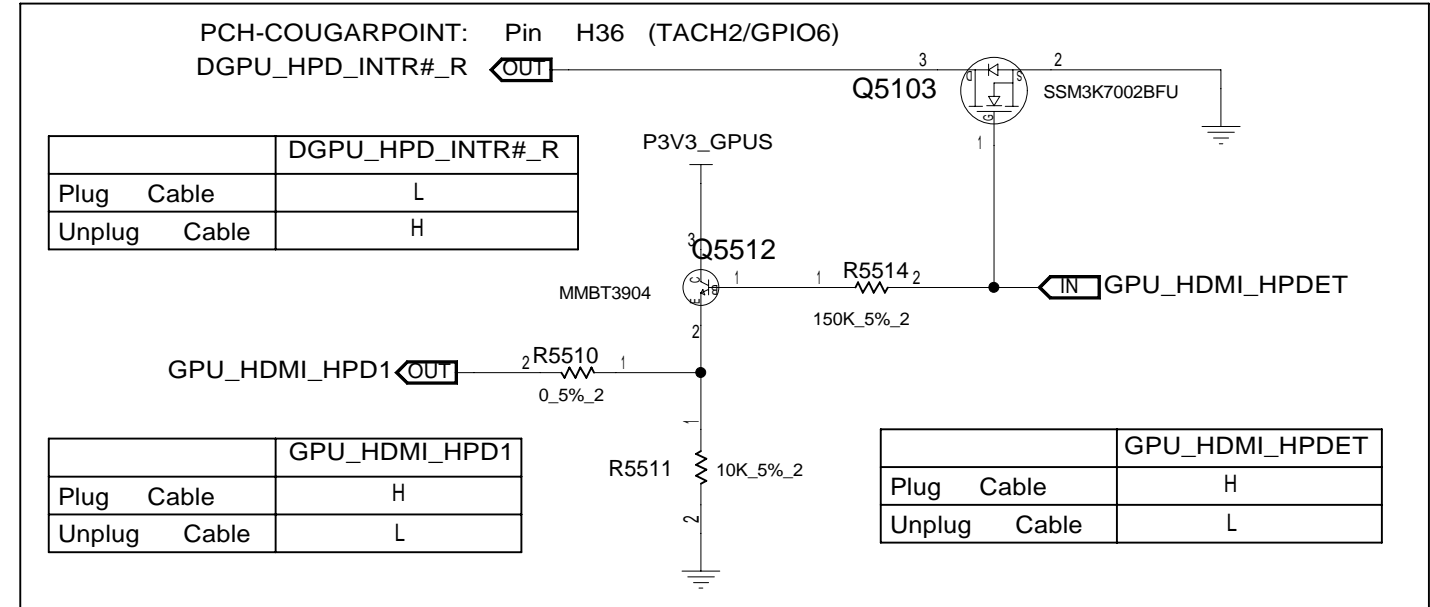
FUNCTION	SEL /HPD_SEL/AUX_SEL
PORT A IS ACTIVE	L (CPU)
PORT B IS ACTIVE	H (GPU)



	DGPU_HPD_INTR#_R
Plug Cable	L
Unplug Cable	H

	GPU_EDP_HPDP
Plug Cable	H
Unplug Cable	L

	EDP_HPD#_CN
Plug Cable	H
Unplug Cable	L



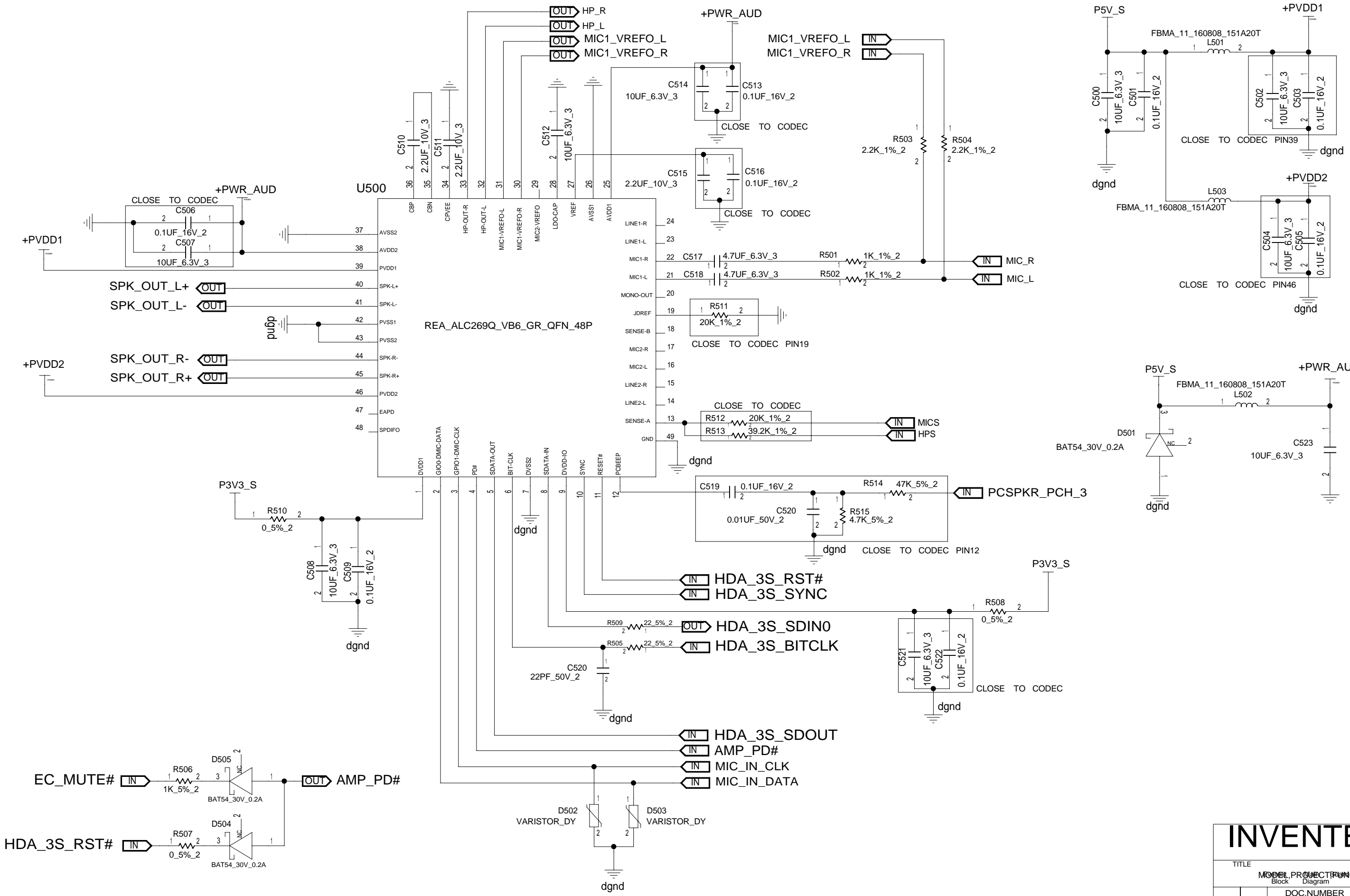
	DGPU_HPD_INTR#_R
Plug Cable	L
Unplug Cable	H

	GPU_HDMI_HPDP1
Plug Cable	H
Unplug Cable	L

	GPU_HDMI_HPDET
Plug Cable	H
Unplug Cable	L

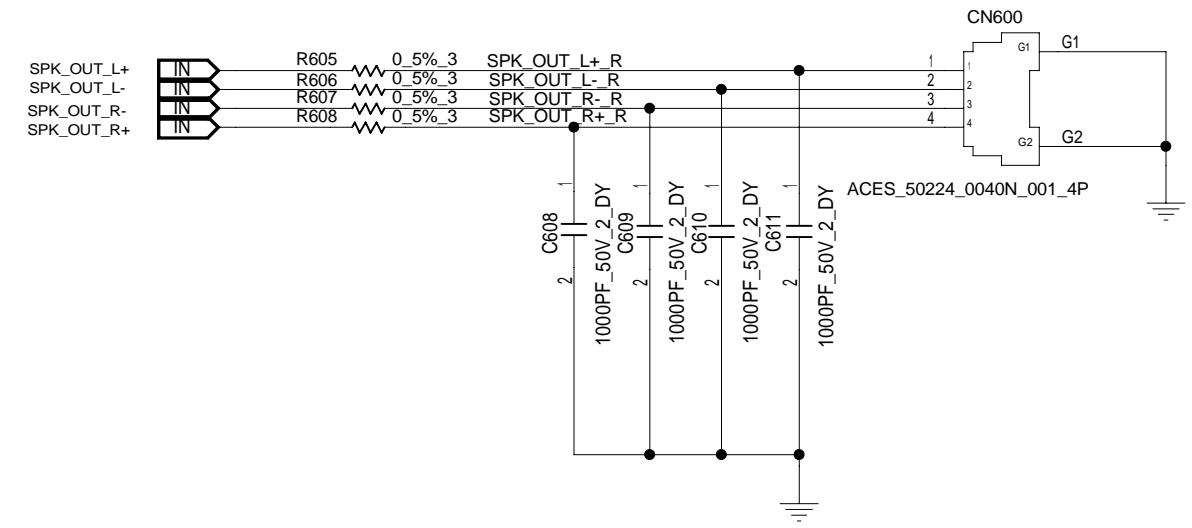
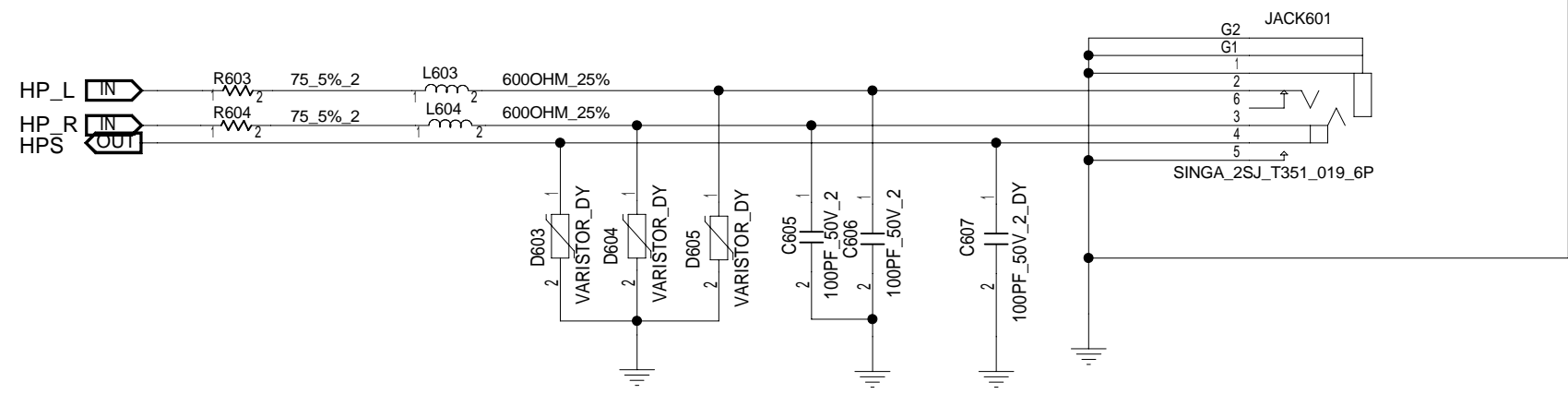
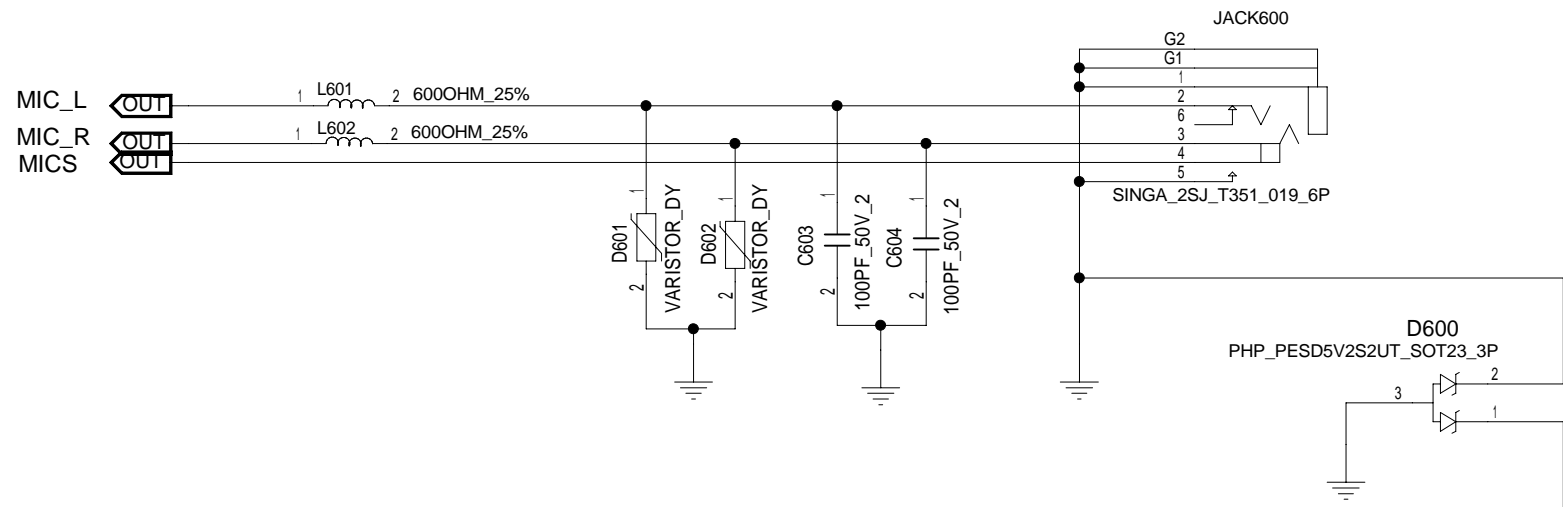
INVENTEC

TITLE			
MODEL PROJECT FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
C	CS	1310xxxx00	X01
CS-1310XXXXXX-MTR			



INVENTEC

TITLE			
MODEL PROJECT FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
C	CS	1310xxxxx-00	X01
SHEET 1 of 97			CS-1310XXXXXX-MTR



INVENTEC			
TITLE MODEL PROTECTION Block Diagram			
SIZE C	CODE CS	DOC NUMBER 1310xxxx-00 CS-1310XXXXXX-MTR	REV X01
CHANGE by XXX		DATE Feb 2002	2010
		BEN LEE	SHEET 1 of 97

D

C

B

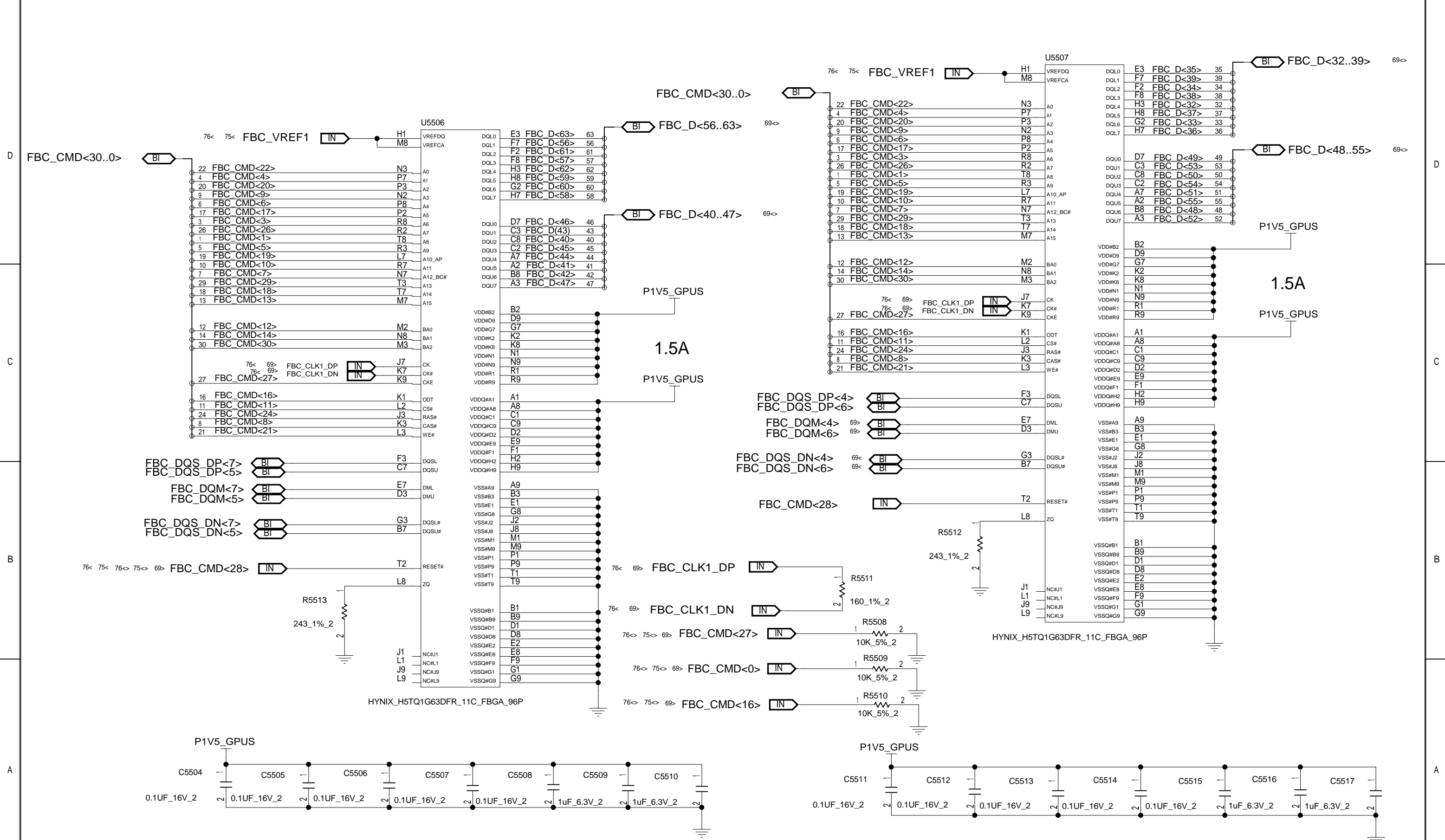
A

D

C

B

A



INVENTEC				
TITLE EVEREST-M VRAM				
SIZE C	CODE CS	DOC.NUMBER CS_1310AXXXXX-MTR	REV A01	
CHANGE by Frank Hu		DATE Fri Dec 31 10:16:55	2010	SHEET 97 of 97