

Inventec Corporation

R&D Division

Board name : Mother Board Schematic
Project : J11Eagle (Santa Rosa)
Version : 0.4
Initial Date : January 05, 2007

1. Schematic Page Description :

J11Eagle (Santa Rosa) Schematic Ver : 0.4

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53. STICK SW BOARD

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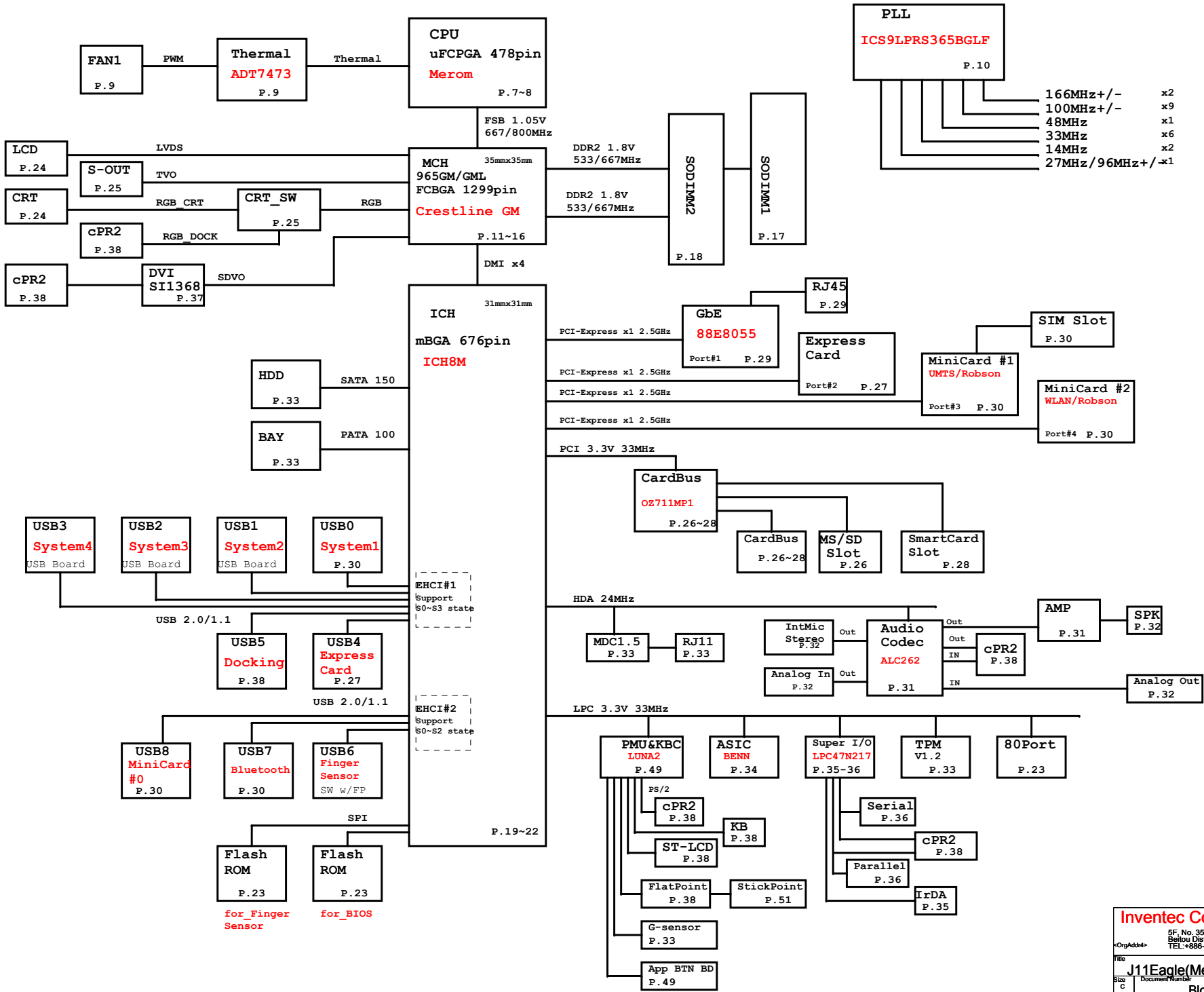
2. PCI & IRQ & DMA Description :

IDSEL	CHIP
AD19	OZ711MP1

PCIINT	CHIP
PCI_INT#0	OZ711MP1
PCI_INT#1	N/A
PCI_INT#2	N/A
PCI_INT#3	N/A

BUSMASTER	
REQ	CHIP
REQ0 / GNT0	N/A
REQ1 / GNT1	OZ711MP1
REQ2 / GNT2	N/A
REQ3 / GNT3	N/A

3. Block Diagram :



4. Nat name Description :

Voltage Rails

PWR DCIN	Primary DC system power supply
+5VIA	5.0V always on power rail by LATCH or ACIN
PWR 3VSTD	3.3V always on power rail by LATCH or ACIN
PWR PMU	3.3V always on power rail by ECPWON
PWR 5VSUS	5.0V power rail by SLP_S5#_3R
PWR 3VSUS	3.3V power rail by SLP_S5#_3R
PWR 5VMAIN	5.0V switched power rail by SLP_S3#_3R
PWR_3VMAIN	3.3V switched power rail by SLP_S3#_3R

PWR_CPUCORE	Core Voltage for CPU
PWR 1.05VMAIN	1.05V power rail for AGTL+ termination/Core for GMCH by SLP_S3#_3R
PWR_1.5VMAIN	1.5V power rail for CPU PLL/DMI/PCIE;DDRII DLLs for GMCH/CoRe;PCIE for ICH7m by SLP_S3#_3R

PWR 1.8VSUS	1.8V power rail for DDRII by SLP_S5#_3R
PWR_DIMM_VTT	0.9V DDRII Termination Voltage by SLP_S3#_3R

Part Naming Conventions

C	=	Capacitor
CN	=	Connector
D	=	Diode
F	=	Fuse
L	=	Inductor
Q	=	Transistor
R	=	Resistor
RP	=	Resistor Pack
U	=	Arbitrary Logic Device
Y	=	Crystal and Osc

Net Name Suffix

#	=	Active Low signal
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5. Board Stack up Description

PCB Layers

Layer 1		Component Side, Microstrip signal Layer
Layer 2		Ground Plane
Layer 3		Stripline Layer
Layer 4		Power Plane
Layer 5		Stripline Layer
Layer 6		Stripline Layer
Layer 7		Ground Plane
Layer 8		Solder Side, Microstrip signal Layer

	Single End Impedance	Differential Impedance for Microstrip	Differential Impedance for Stripline
Host Clock	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
SRC Clock	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
Host Bus	55 ohm +/- 15%		
DDR2 CLK	42 ohm +/- 15%	70 ohm +/- 20%	70 ohm +/- 20%
DDR2 Strobe	55 ohm +/- 15%		85 ohm +/- 20%
DDR2 Bus	55 ohm +/- 15%		
DMI Bus	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
PCIE Bus	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
SATA		95 ohm +/- 15%	100 ohm +/- 15%
SDVO	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
LVDS		100 ohm +/- 15%	100 ohm +/- 15%
USB		90 ohm +/- 15%	90 ohm +/- 15%
IEEE1394		110 ohm +/- 15%	110 ohm +/- 15%
Lan	50 ohm +/- 15%		

Power Rail	Destination	Voltage	S0 Current
PWR_CPUCORE	MeromHFM: LFM:	1.3319V-1.4375V-1.4591V 0.9221V-0.9625V-0.9739V	36A
PWR_1.05VMAIN	Merom: AGTL+ termination 965GM: Core	0.997V-1.05V-1.102V 1.0V-1.05V-1.1V	2.5A 4.6A
	965GM: AGTL+ termination ICH8m:	0.9475V-1.05V-1.1025V	1.4A
PWR_1.5VMAIN	Merom PLL 965GM: PCIE 965GM: LVDS 965GM: TVDAC 965GM: Various PLLS analog supply 965GM: DDR DLLS,DDRII,FSB HSIO ICH8m: ICH8m: ICH8m: Mini Card: Express Card:	1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V	120mA 1.5A 60mA 24mA 320mA 1.885A
PWR_1.8VSUS	965GM: DDRII System Memory SO-DIMM: 965GM: LVDS analog 965GM: LVDS I/O 965GM: PCIE analog CLOCK GEN.	1.7V-1.8V-1.9V 1.7V-1.8V-1.9V 1.7V-1.8V-1.9V	3.1A 10mA 60mA 2mA
PWR_DIMM_VTT	DDRII Terminator:	0.855V-0.9V-0.945V	1.0A
PWR_3VSUS	965GM: HV CMOS 965GM: TVDAC analog ICH8m: ICH8m: ICH8m: ICH8m: ICH8m: Mini Card: Express Card: CLK Generator: ICS9LPRS365AGLF Mini PCie: WirelessLan Azalia Codec: ALC262 Azalia MDC: HDD: SATA 965GM: CRT DAC	3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.0V-3.3V-3.6V	40mA 120mA 400mA
PWR_3VMAIN	CardBus: OZ711MP1 CardBus: Slot voltage Lan: Broadcom 88E8055 Card Reader: SD/MMC/MS Azalia MDC: For wake up Mini PCI: For wake up	3.0V-3.3V-3.6V	
PWR_3VSTD	ICH8m: ICH8m: ICH8m: LCD:	 3.0V-3.3V-3.6V	 1.0A
PWR_3VMAIN	Azalia Codec: ALC262 Azalia MDC: HDD: SATA ODD: PATA Audio AMP: G1412 Woofer AMP: G1432 Inverter:	3.0V-3.3V-3.6V 4.75V-5.0V-5.25V 4.75V-5.0V-5.25V	Max: 1.0A ; R/W: 460mA ; STDBY: 70mA Max: 1.8A ; R/W: 900mA ; STDBY: 45mA
PWR_5VMAIN	CardBus: Slot voltage USB: x 4 ports	 5V	 2.0A
PWR_3VSTD	EC: ICH8m: RTC Flash ROM: BIOS		

Inventec Corporation

5F, No. 35, Section 2, Zhongyang South Road
Beitou District, Taipei 11270, Taiwan
TEL: +886-2-2881-0721

File: J11Eagle(Merom+Crestline+ICH8M)
Size: C Document Number: ANNOTATIONS Rev: 0.3

Date: Monday, April 09, 2007 Sheet: 4 of 55

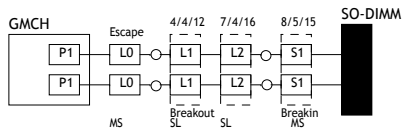
8. Layout Guideline :

Crestline DDRII Layout Guidelines

DDRII Signal Groups

Group	Signal Name	Length Matching and Length Formulas															
Data	M_A_DQ[63..0]/M_B_DQ[63..0] M_A_DM[7..0]/M_B_DM[7..0] M_A_DSQ[7..0]/M_A_DSQ[7..0] M_B_DSQ[7..0]/M_B_DSQ[7..0]	<table><tr><th>Signal Group</th><th>Minimum Length</th><th>Maximum Length</th></tr><tr><td>Control-to-Clock</td><td>Clock - 1.0"</td><td>Clock - 0.0"</td></tr><tr><td>Command-to-Clock</td><td>Clock - 1.0"</td><td>Clock + 1.0"</td></tr><tr><td>Strobe-to-Clock</td><td>Clock - 0.5"</td><td>Clock + 1.0"</td></tr><tr><td>Data-to-Strobe</td><td>Strobe - 220mils</td><td>Strobe - 180mils</td></tr></table>	Signal Group	Minimum Length	Maximum Length	Control-to-Clock	Clock - 1.0"	Clock - 0.0"	Command-to-Clock	Clock - 1.0"	Clock + 1.0"	Strobe-to-Clock	Clock - 0.5"	Clock + 1.0"	Data-to-Strobe	Strobe - 220mils	Strobe - 180mils
Signal Group	Minimum Length	Maximum Length															
Control-to-Clock	Clock - 1.0"	Clock - 0.0"															
Command-to-Clock	Clock - 1.0"	Clock + 1.0"															
Strobe-to-Clock	Clock - 0.5"	Clock + 1.0"															
Data-to-Strobe	Strobe - 220mils	Strobe - 180mils															
Address	M_A_A[13..0]/M_B_A[13..0] M_A_BS[2..0]/M_B_BS[2..0] M_A_RAS#/M_B_RAS# M_A_CAS#/M_B_CAS# M_A_WE#/M_B_WE#																
Control	M_CS[3..0] M_CKE[3..0] M_ODT[3..0]																
Clock	M_CLK_DDR[3..0] M_CLK_DDR[3..0]																
Feedback	SA_RCVEN#/SB_RCVEN#																

CLK group : M_CLK_DDR[3..0],M_CLK_DDR[3..0]



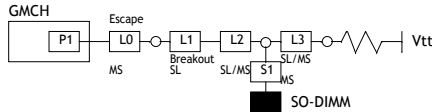
Topology	Differential Pair Point-to-Point
Reference Plane	Ground
Single Ended Trace Impedance	42 +/- 15%
Differential Mode Impedance	70 +/- 20%
Package Length Range - P1	350 mils - 625 mils
Min. Serpentine Spacing	25 mils
Trace Length Limit - L0 (MS)	Length Limit: Max = 50 mils (Escape)
Trace Length Limit - L1 (SL) (Breakout length segment)	Length Limit: Max = 700 mils Min. Trace Spacing (Other) : 12 mils
Trace Length Limit - L2 (SL)	Min. Trace Spacing (Other) : 16 mils Nominal Trace Width : Outer: 8.5/4/8.5 Inner: L3= 7/4/7, L5/L6=8/4/8 Min. Trace Spacing (pair) : 4mils
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1	Min = 500 mils Max = 4000 mils
Total Length - P1 + L0 + L1 + L2 + S1	Max = 4500 mils Total Length for Channel A : X0 Total Length for Channel B : X1
Maximim Via Count	2 (Per side)
CK to SCK# Length Matching	Match total length to within 5 mils
Clock to Clock Length Match (Total Length)	Match Channel A clocks to X0 +/- 20mils Match Channel A clocks to X1 +/- 20mils
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 4/12 mils to other DDR2 Outer Layer : 5/15 mils to other DDR2 Max. breakout length is 500 mils
Breakin Exceptions (Reduce geometries for SO-DIMM break-in region)	CK to CK# spacing rule waived at connector spacing of 15 mils to other DDR2 Max. breakin length is 200 mils

Feedback group :

M_RCVENIN#,M_A_RCVENOUT#,M_B_RCVENIN#,M_B_RCVENOUT#

These signals are routed internally on the GMCH package and don't require any routing on the MB. As a result, can be left as NC.

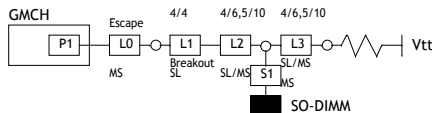
Control group : M_CKE[3..0],M_CS#[3..0],M_ODT[3..0]



Topology	Point-to-Point with parallel termination
Reference Plane	Ground
Characteristic Trace Impedance	55 +/- 15% L2 Seg. = 450ohm +/- 15%
Nominal Trace Width	Inner Layer : L3=5.5 mils, L5/L6= 7 mils Outer Layer : 5 mils
Minimum CTRL Trace Spacing	Inner Layer : 6 mils Outer Layer : 8 mils
Minimum Spacing to Other DDR2	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length P1	400-800 mils
Trace Length Limit - L0	Max = 250 mils (Escape)
Trace Length Limit - L1	Max = 700 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 250 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1 - From GMCH ball to SO-DIMM pad	Min = 500 mils Max = 4500 mils
Total Length - P1 + L0 + L1 + L2 + S1 - From GMCH die to SO-DIMM pad	Max = 5000 mils
Trace Length L3	Max = 1500 mils
Parallel Termination Resistor	56 +/- 5%
Maximim Via Count	3
CTRL to SCK/SCK# Length Matching (Total Length including package)	(CLK-1.0") <= CTRL <= (CLK-0.0")
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 4 mils spacing allowed Outer Layer : 5 mils spacing allowed Max. breakout length is 500 mils

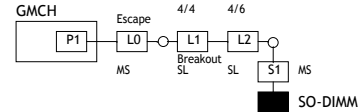
Command group :

M_A_A[13..0],M_B_A[13..0],M_A_BS[2..0],M_B_BS[2..0],M_A_RAS#,
M_B_RAS#,M_A_CAS#,M_B_CAS#,M_A_WE#,M_B_WE#



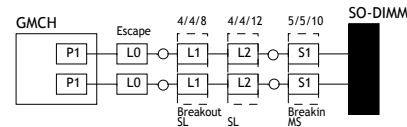
Topology	Point-to-Point with parallel termination
Reference Plane	Ground
Characteristic Trace Impedance	55 +/- 15%
Nominal Trace Width	Inner Layer : L5/L6= 4.5 mils Outer Layer : 5 mils
Minimum CMD Bus Trace Spacing	Inner Layer : 6 mils Outer Layer : 8 mils
Minimum Spacing to Other DDR2	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length P1	250-750 mils
Trace Length Limit - L0	Max = 250 mils (Escape)
Trace Length Limit - L1	Max = 700 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 250 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1 - From GMCH ball to SO-DIMM pad	Min = 500 mils Max = 4500 mils
Total Length - P1 + L0 + L1 + L2 + S1 - From GMCH die to SO-DIMM pad	Max = 5000 mils
Trace Length L3	Max = 1500 mils
Parallel Termination Resistor	56 +/- 5%
Maximim Via Count	3
CTRL to SCK/SCK# Length Matching (Total Length including package)	(CLK-1.0") <= CMD <= (CLK+1.0")
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 4 mils spacing allowed Outer Layer : 5 mils spacing allowed Max. breakout length is 500 mils

Data group : M_A_DQ[63..0],M_B_DQ[63..0],M_A_DM[7..0],M_B_DM[7..0]



Topology	Point-to-Point
Reference Plane	Ground
Characteristic Trace Impedance	55 +/- 15%
Nominal Trace Width	Inner Layer : L5/L6= 4.5 mils Outer Layer : 5 mils
Minimum DQ Bus Trace Spacing	Inner Layer : 6 mils Outer Layer : 8 mils
Minimum Serpentine Spacing	Same as DQ-to-DQ routing
Minimum Spacing to Other DDR2	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length P1	750 mils +/- 350 mils
Trace Length Limit - L0	Max = 250 mils (Escape)
Trace Length Limit - L1	Max = 700 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 250 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1 - From GMCH ball to SO-DIMM pad	Min = 500 mils Max = 4500 mils
Total Length - P1 + L0 + L1 + L2 + S1 - From GMCH die to SO-DIMM pad	Max = 4800 mils
Trace Length L3	Max = 1500 mils
Maximim Via Count	2
DQ/DM to DQS Length Matching (Total Length including package)	Match DQ/DM to [SDQS - 200mils] +/- 20mils, per byte lane
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 4 mils spacing allowed Outer Layer : 5 mils spacing allowed Max. breakout length is 500 mils

Data Strobe group : M_A_DSQ[7..0],M_A_DSQ[7..0],M_B_DSQ[7..0],M_B_DSQ[7..0]

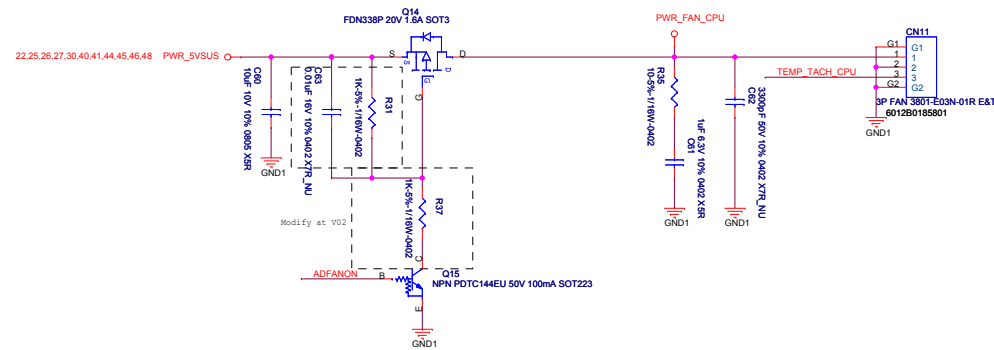
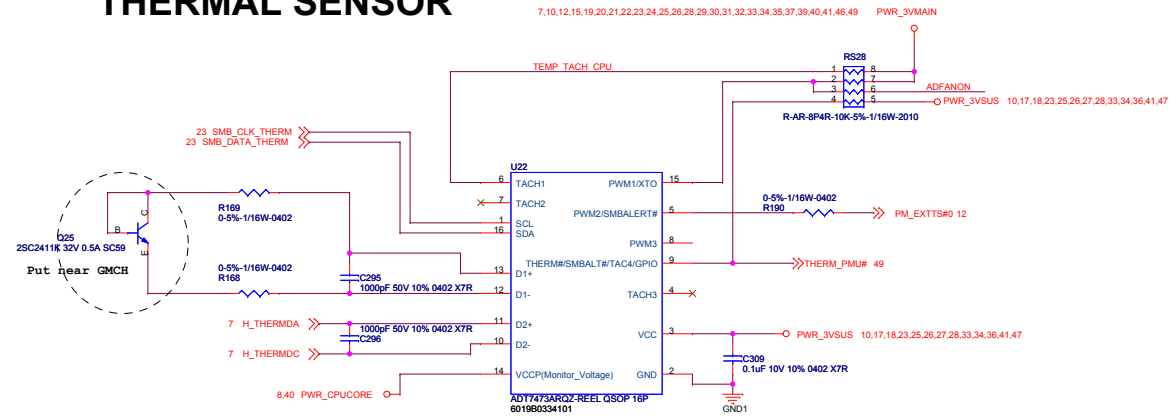


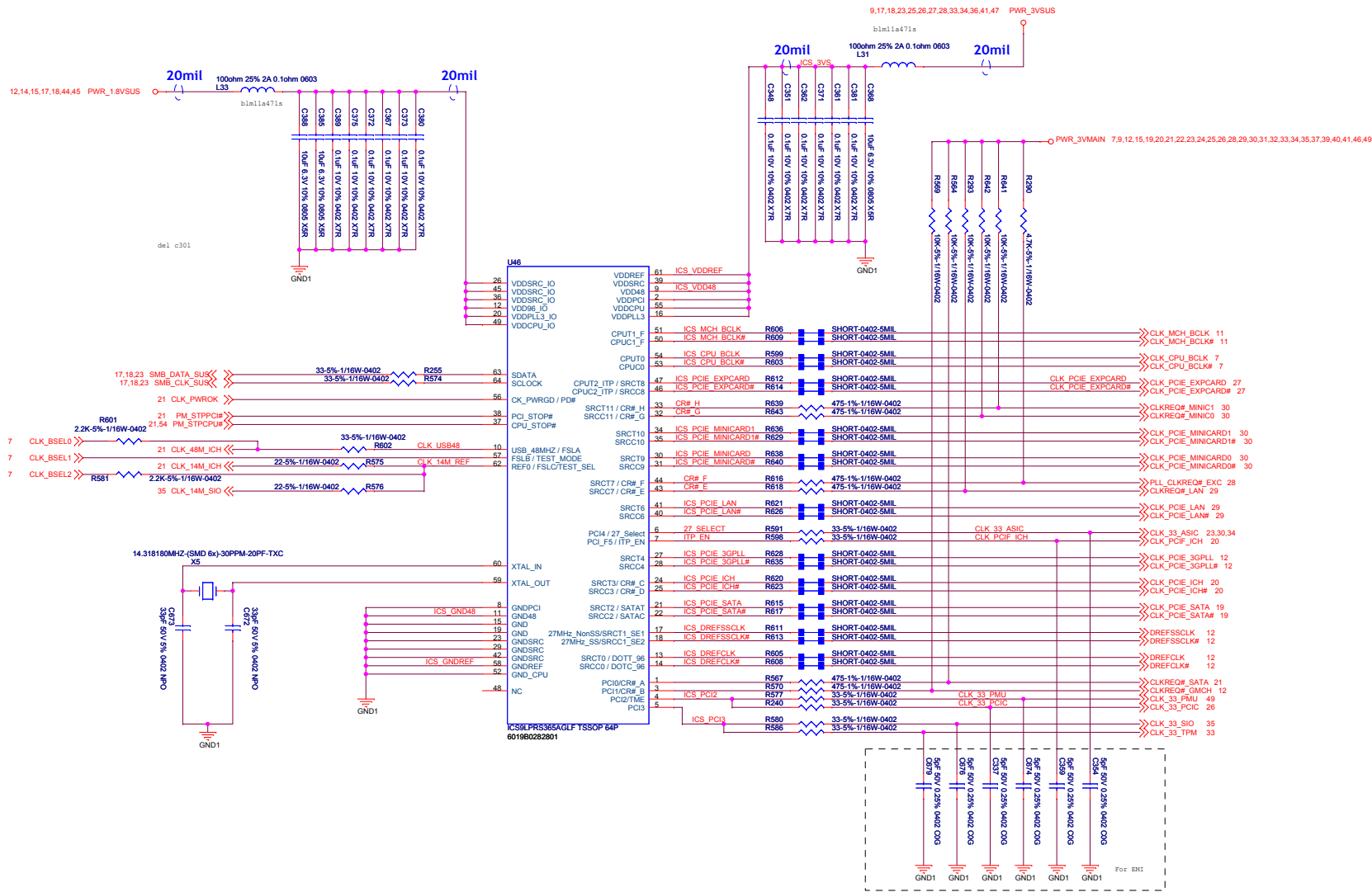
Topology	Differential Pair Point-to-Point
Reference Plane	Ground
Single Ended Trace Impedance	55 +/- 15%
Differential Mode Impedance	85 +/- 20%
Nominal Trace Width	Inner Layer : L3:5/5/5, L5/L6= 5/4/5 mils Outer Layer : 6/5/6 mils
Nominal DQS to DQS# Spacing (edge to edge)	Inner Layer : 4 mils Outer Layer : 5 mils
Minimum DQS to DQ Spacing	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Serpentine Spacing	Inner Layer : 8 mils Outer Layer : 10 mils
Minimum Spacing to Other DDR2	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length Range - P1	425-925 mils
Trace Length Limit - L0	Max = 250 mils (Escape)
Trace Length Limit - L1	Max = 500 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 250 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1 - From GMCH ball to SO-DIMM pad	Min = 500 mils Max = 4500 mils
Total Length - P1 + L0 + L1 + L2 + S1 - From GMCH die to SO-DIMM pad	Max = 5000 mils
Maximim Via Count	2 (Per side)
DQS to DQS# Length Matching	Match total length to within 5 mils
Clock to Clock Length Match (Total Length include package)	(CLK-0.5") <= DQS <= (CLK+1.0")
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 8 mils to other DDR2 Outer Layer : 10 mils to other DDR2 Max. breakout length is 500 mils
Breakin Exceptions (Reduce geometries for SO-DIMM break-in region)	DQS to DQS# spacing rule waived at connector spacing of 10 mils to other DDR2 Max. breakin length is 200 mils

Inventec Corporation

5F, No. 35, Section 2, Zhongyang South Road
Beitou District, Taipei 11270, Taiwan
TEL: +886-2-2881-0721

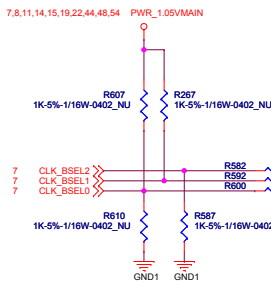
THERMAL SENSOR



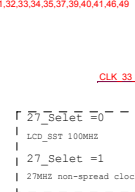
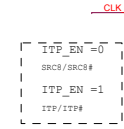
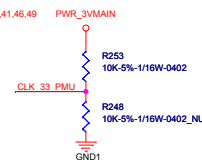


Clock Request table

CLKREQ#_pin	Clocks	Select	
CR#_A	SRCCLK0 SRCCLK2	V	Byte 5, bit 7=1 Byte 5, bit 6=1
CR#_B	SRCCLK1 SRCCLK4	V	Byte 5, bit 5=1 Byte 5, bit 4=1
CR#_E	SRCCLK6	V	Byte 6, bit 7=1
CR#_F	SRCCLK8	V	Byte 6, bit 6=1
CR#_G	SRCCLK9	V	Byte 6, bit 5=1
CR#_H	SRCCLK10	V	Byte 6, bit 4=1



FSA	F5B	F5C	F5B CLOCK FREQUENCY	HOST CLOCK FREQUENCY
1	1	0	667	166
0	1	0	800	200 *



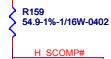
Inventec Corporation
5F, No. 35, Section 2, Zhongyang South Road
Beitou District, Taipei 11270, Taiwan
TEL: +886-2-2881-0721

File: J11Eagle(Merom+Crestline+ICH8M)
Docu: J11Eagle(Merom+Crestline+ICH8M)
Rev: 0.4

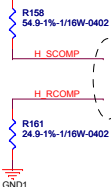
Clock Generator

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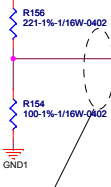
7,8,10,14,15,19,22,44,48,54 PWR_1.05VMMAIN



7,8,10,14,15,19,22,44,48,54 PWR_1.05VMMAIN



7,8,10,14,15,19,22,44,48,54 PWR_1.05VMMAIN

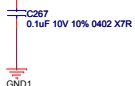
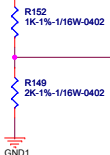


Trace should be 10-mil wide with 20-mil spacing

H_SWING
H_RCOMP
H_SCOMP
H_SCOMP#

7.54 H_CPURST#
7 H_CPUSLP#

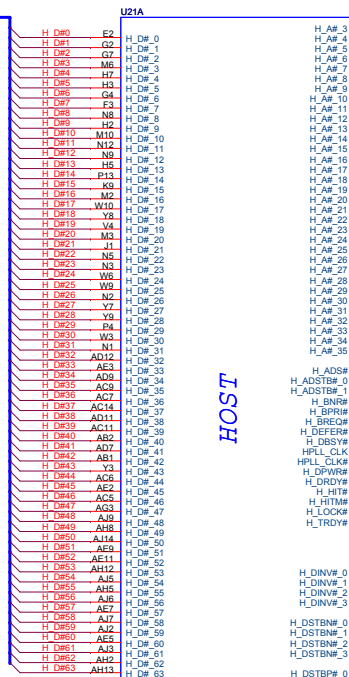
7,8,10,14,15,19,22,44,48,54 PWR_1.05VMMAIN



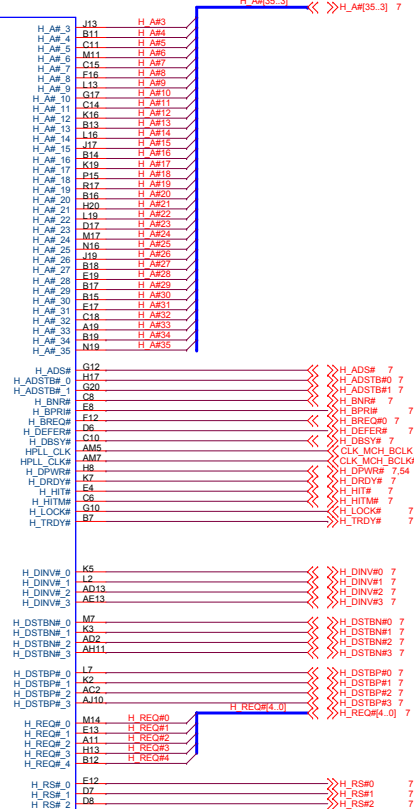
0.1uF 10V 10% 0402 X7R

0.5%-1/16W-0402

H_DVREF



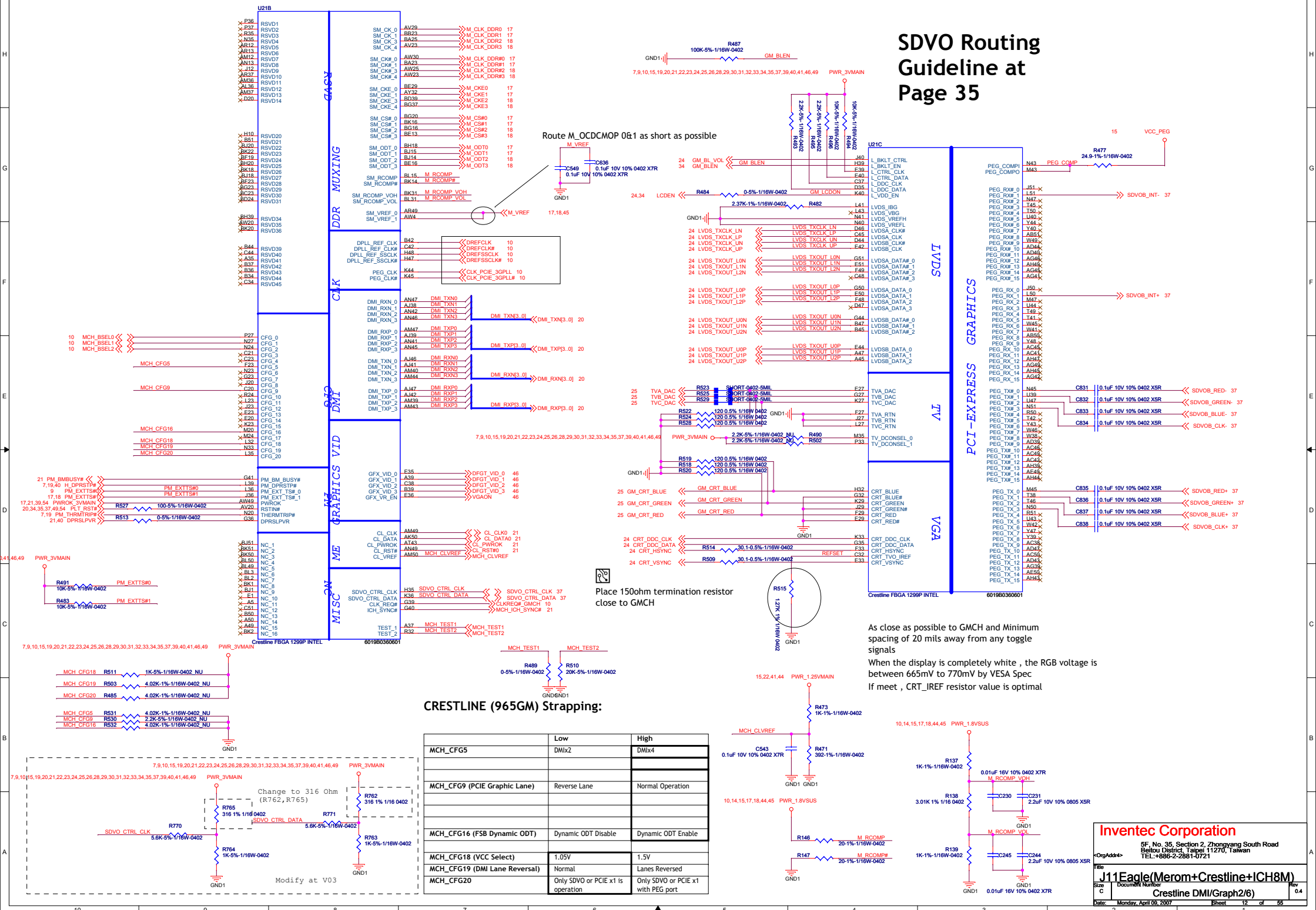
HOST

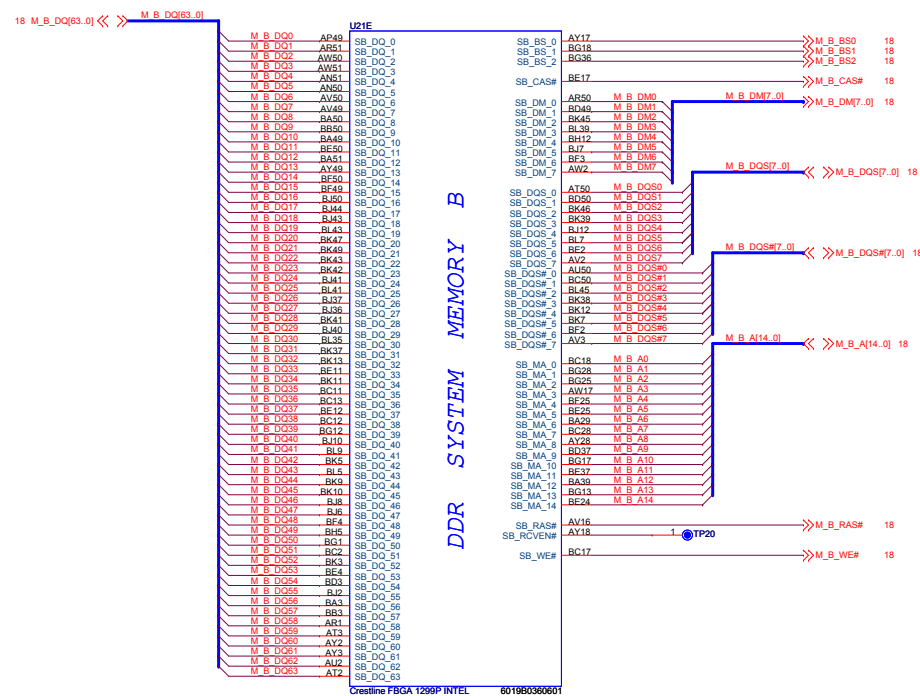
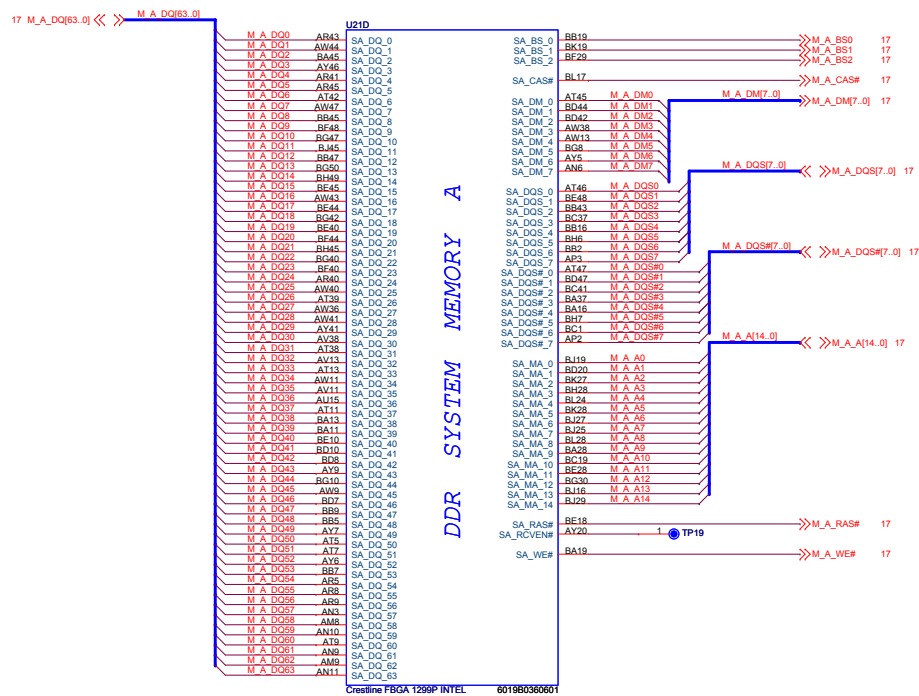


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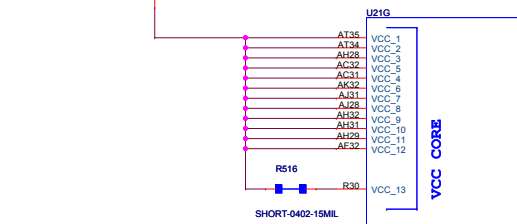
5F, No. 35, Section 2, Zhongyang South Road
Beitou District, Taipei 11270, Taiwan
TEL:+886-2-2881-0721

File
J11Eagle(Merom+Crestline+ICH8M)
Size C Document Number
Crestline Host(1/6)
Date: Monday, April 09, 2007 Sheet 11 of 55

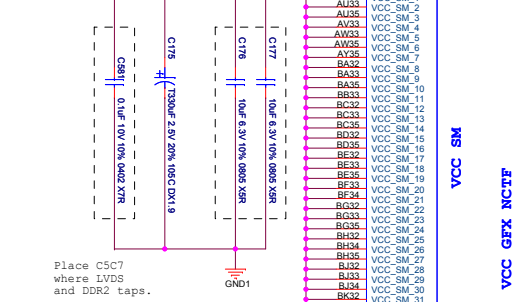
SDVO Routing
Guideline at
Page 35



7,8,10,11,15,19,22,44,48,54 PWR_1.05VMAIN

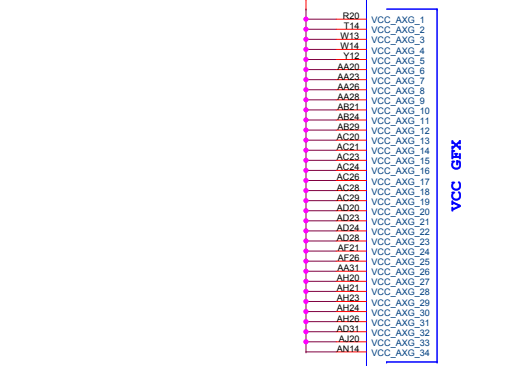


PLACE C176, C177, C178, C179 2.0V, 20%, 10% DIX 9 THE EDGE



Place C176, C177, C178, C179 2.0V, 20%, 10% DIX 9 and DDR2 taps.

46 PWR_1.05VMAIN



Crestline FBGA 1299P INTEL 601960360601

601960360601

601960360601

601960360601

601960360601

601960360601

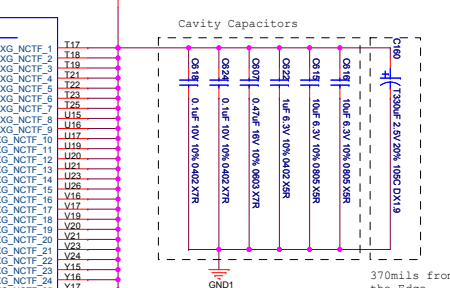
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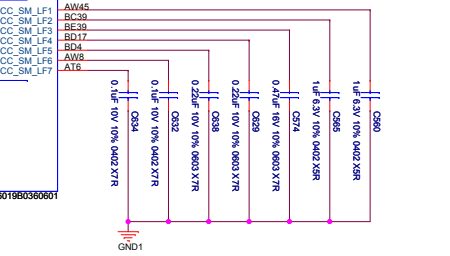
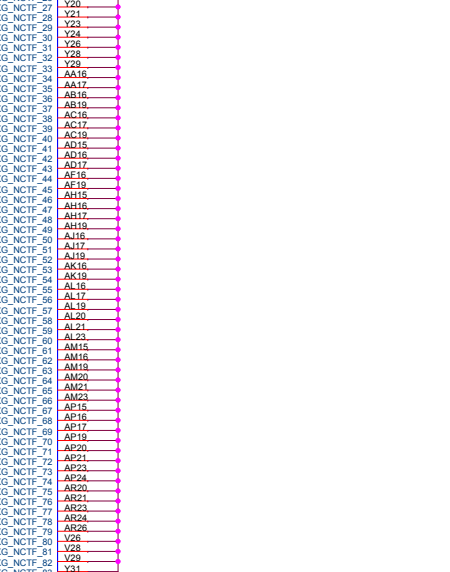
601960360601

601960360601

46 PWR_1.05VMAIN



370mils from the Edge



601960360601

601960360601

601960360601

601960360601

601960360601

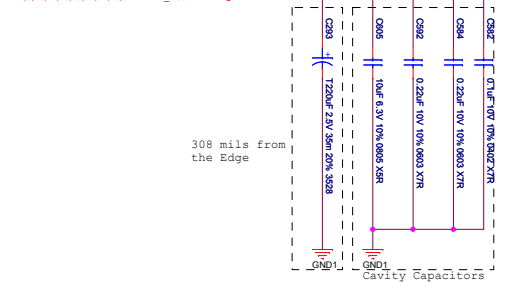
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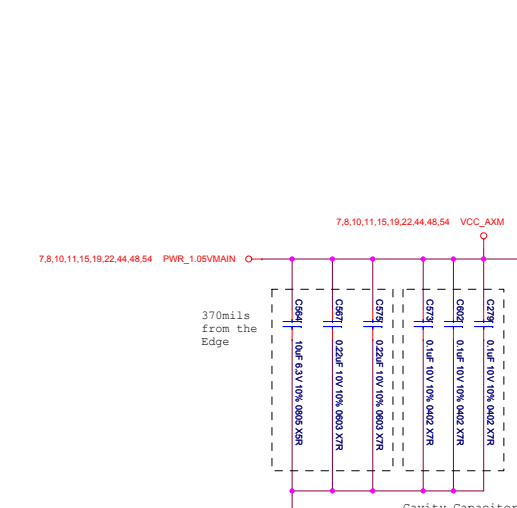
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601960360601

7,8,10,11,15,19,22,44,48,54 PWR_1.05VMAIN



308 mils from the Edge



370mils from the Edge



601960360601

601960360601

601960360601

601960360601

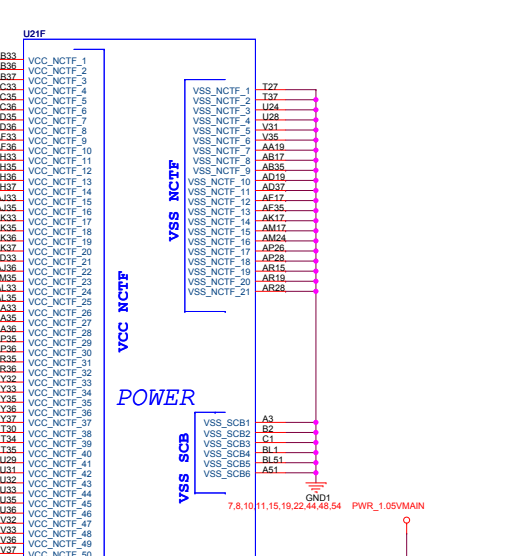
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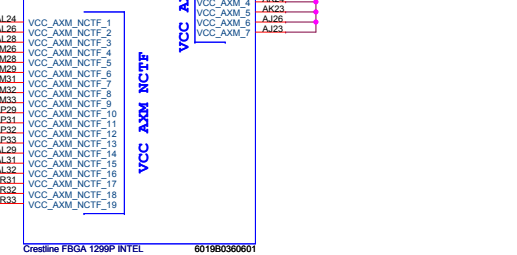
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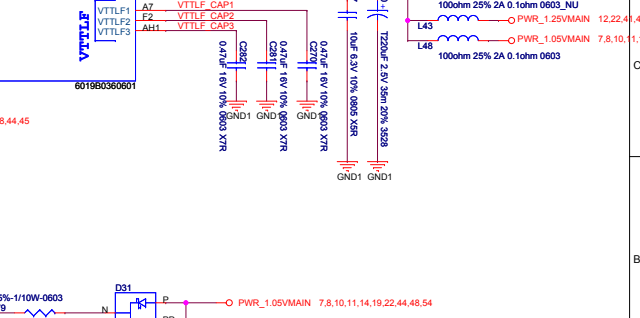
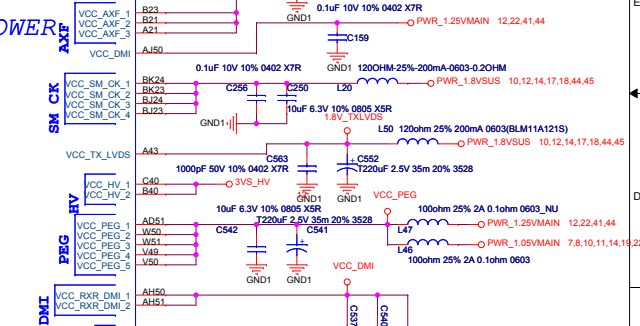
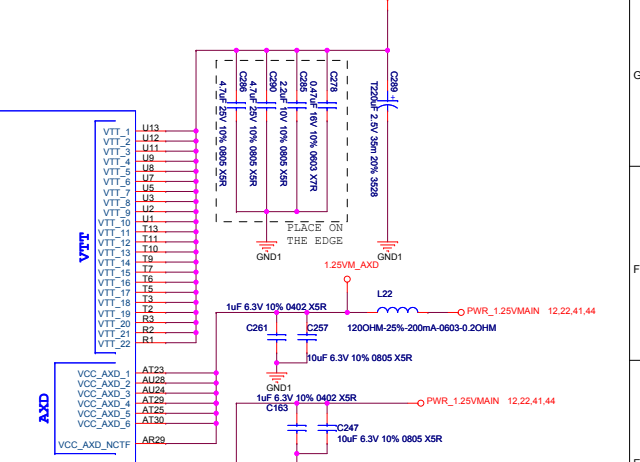
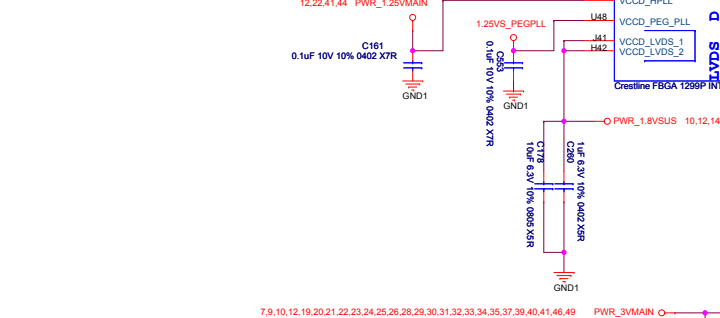
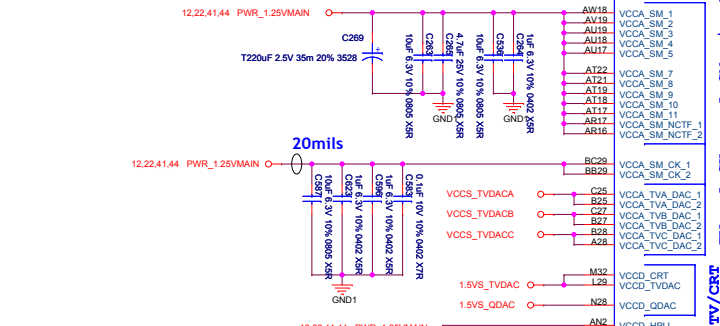
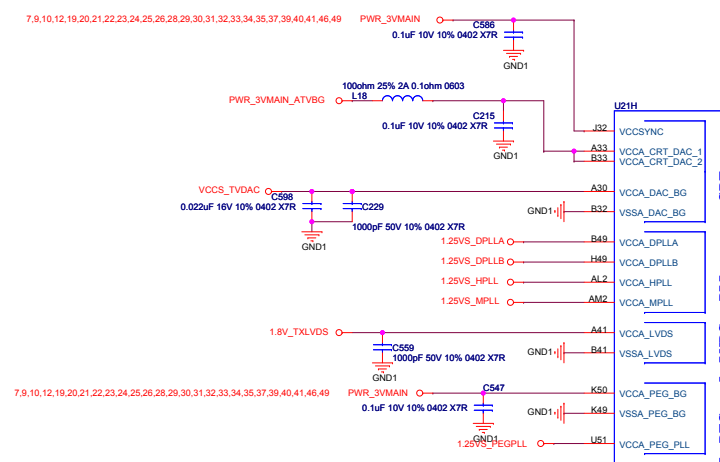
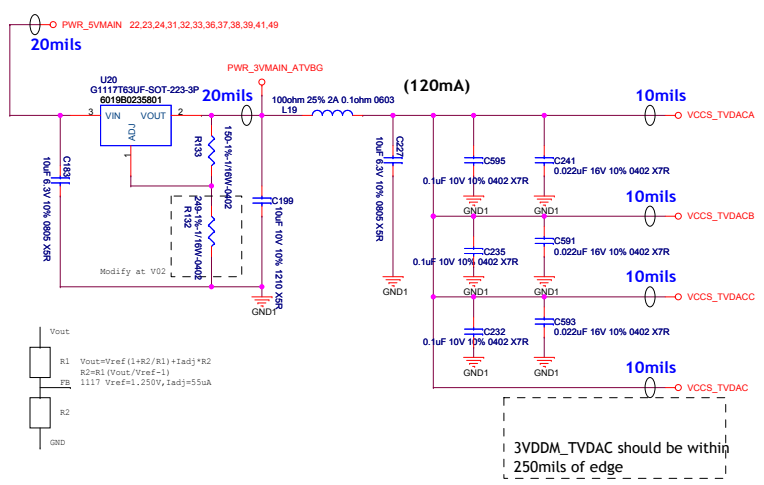
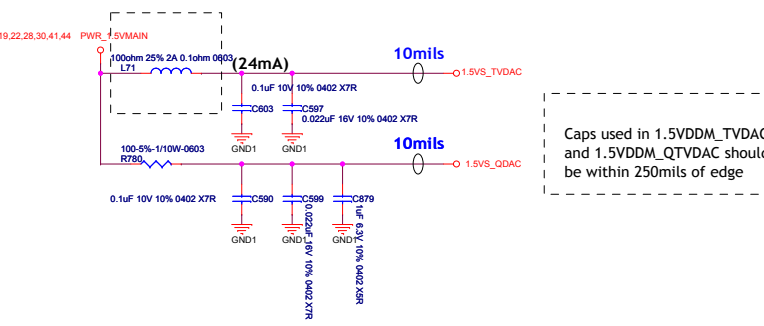
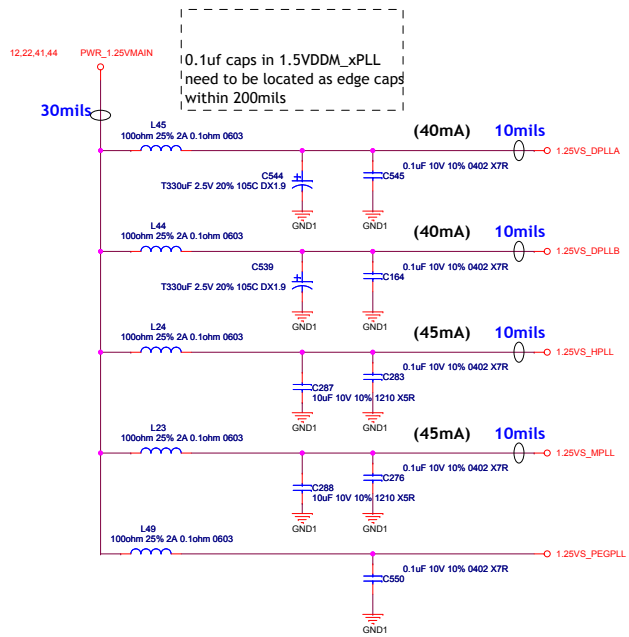
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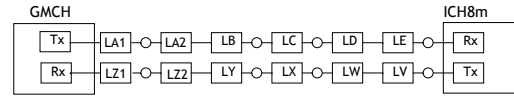
7,8,10,11,15,19,22,44,48,54 PWR_1.05VMAIN



601960360601



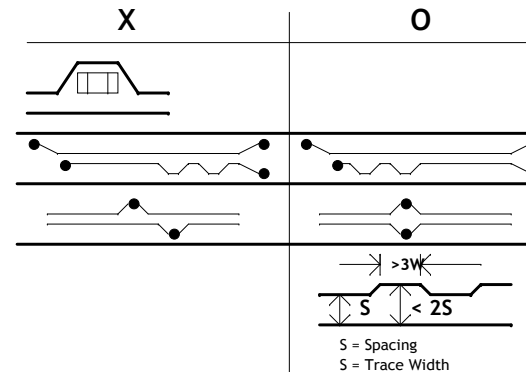
DMI Routing Guideline



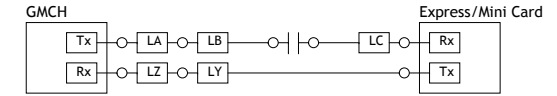
Breakout/in LA/LZ	Main Route LB/LY	Breakout/in LE/LV
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV

Parameter	Main Route Guideline	Breakout Guideline
Uncoupled Single End Impedance	55 +/- 15%	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils	
Nominal Differential Pair-Pitch	Inner Layer : 7 mils Outer Layer : 7 mils	Inner Layer : 4 mils Outer Layer : 5 mils
Pair-to-Pair Pitch	Inner Layer : 37 mils Outer Layer : 37 mils	Inner Layer : 27 mils Outer Layer : 27 mils
Bus-to-Bus Pitch	Inner Layer : 22 mils Outer Layer : 20 mils	Inner Layer : 15 mils Outer Layer : 12 mils
Reference Plane	Ground	Ground
Splits/Voids	No routing over plane splits No routing over voids	
Trace Length-LA (GMCH Breakout)	Max = 250 mils	
Trace Length-LB (GMCH Breakout to Via2)	Max = 3600 mils	
Trace Length-LC (Via2 to Via3)	Max = 5900 mils	
Trace Length-LD (Via3 to ICH7m Breakout)	Max = 3600 mils	
Trace Length-LE (ICH7m Breakout)	Max = 400 mils	
Trace Length-L1 (LA+LB+LC+LD+LE)	Max = 8000 mils	
Trace Length-LV (ICH7m Breakout)	Max = 400 mils	
Trace Length-LW (ICH7m Breakout to Via2)	Max = 3600 mils	
Trace Length-LX (Via2 to Via3)	Max = 5900 mils	
Trace Length-LY (Via3 to GMCH Breakout)	Max = 3600 mils	
Trace Length-LZ (GMCH Breakout)	Max = 400 mils	
Trace Length-L2 (LV+LW+LY+LZ)	Max = 8000 mils	

*** When routing near the edge of their reference plane , trace should maintain at least 40 mils space to the edge of the plane
*** Match the trace lengths of the complementary signals within each differential pair to +/- 5 mils

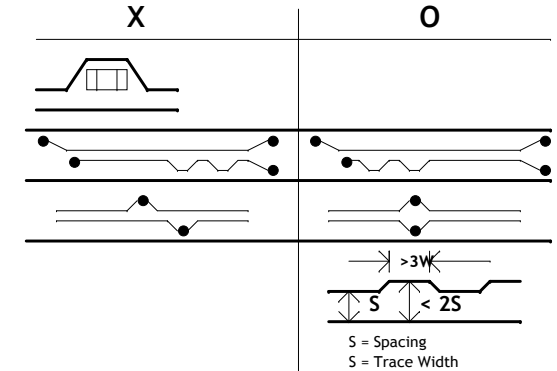


PCIE Routing Guideline



Breakout/in LA/LZ	Main Route LB/LC/LY	Main Route LD/LW	Breakout/in LE/LV
Stripline	Microstrip	Same Routing layer as LE/LV	Microstrip
Parameter	Main Route Guideline		Breakout Guideline
Uncoupled Single End Impedance	55 +/- 15%		55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils		
Nominal Differential Trace Space	Inner Layer : 7 mils Outer Layer : 7 mils		Inner Layer : 4 mils Outer Layer : 5 mils
Pair-to-Pair Pitch	Inner Layer : 37 mils Outer Layer : 37 mils		Inner Layer : 27 mils Outer Layer : 27 mils
Bus-to-Bus Pitch	Inner Layer : 20 mils Outer Layer : 20 mils		Inner Layer : 15 mils Outer Layer : 12 mils
Reference Plane	Ground		Ground
Splits/Voids	No routing over plane splits No routing over voids		
Trace Length-LA (ICH7m Breakout)	Max = 400 mils		
Trace Length-LB (ICH7m Breakout to AC cap)	Max = 10750 mils		
Trace Length-LC (AC cap to PCIe CN)	Max = 10750 mils		
Trace Length-L1 (LA+LB+LC)	Max = 12000 mils		
Trace Length-LY (PCIe CN to ICH7m Breakout)	Max = 11950 mils		
Trace Length-LZ (ICH7m Breakout)	Max = 400 mils		
Trace Length-L2 (LY+LZ)	Max = 12000 mils		

*** When routing near the edge of their reference plane , trace should maintain at least 40 mils space to the edge of the plane
*** Match the trace lengths of the complementary signals within each differential pair to +/- 5 mils



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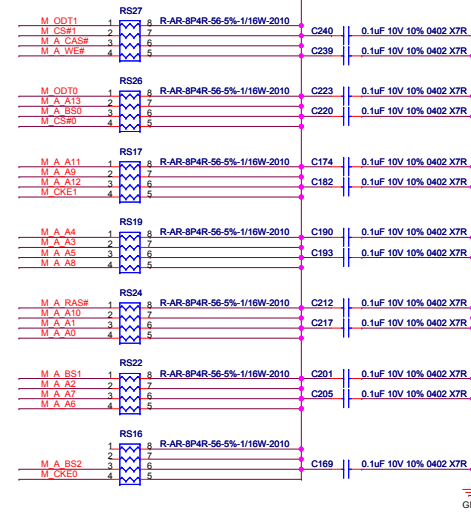
5F, No. 35, Section 2, Zhongyang South Road
Beitou District, Taipei 11270, Taiwan
TEL: +886-2-2881-0721

File: J11Eagle(Merom+Crestline+ICH8M)
Size: C Document Number: Crestline Ground(6/6)
Date: Monday, April 08, 2007 Sheet: 16 of 55

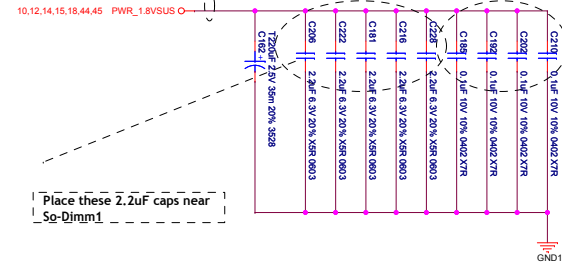
SO-DIMMO

Place one cap close to every 2 pullup resistors terminated to 0.9VDDT_DDRII

400 mils

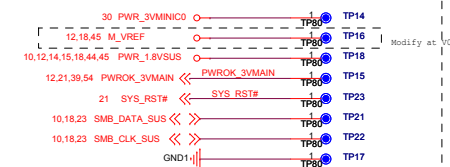


Place these 0.1uF caps near So-Dimm0 pin79~pin115 area



Place these 2.2uF caps near So-Dimm1

For Margin test

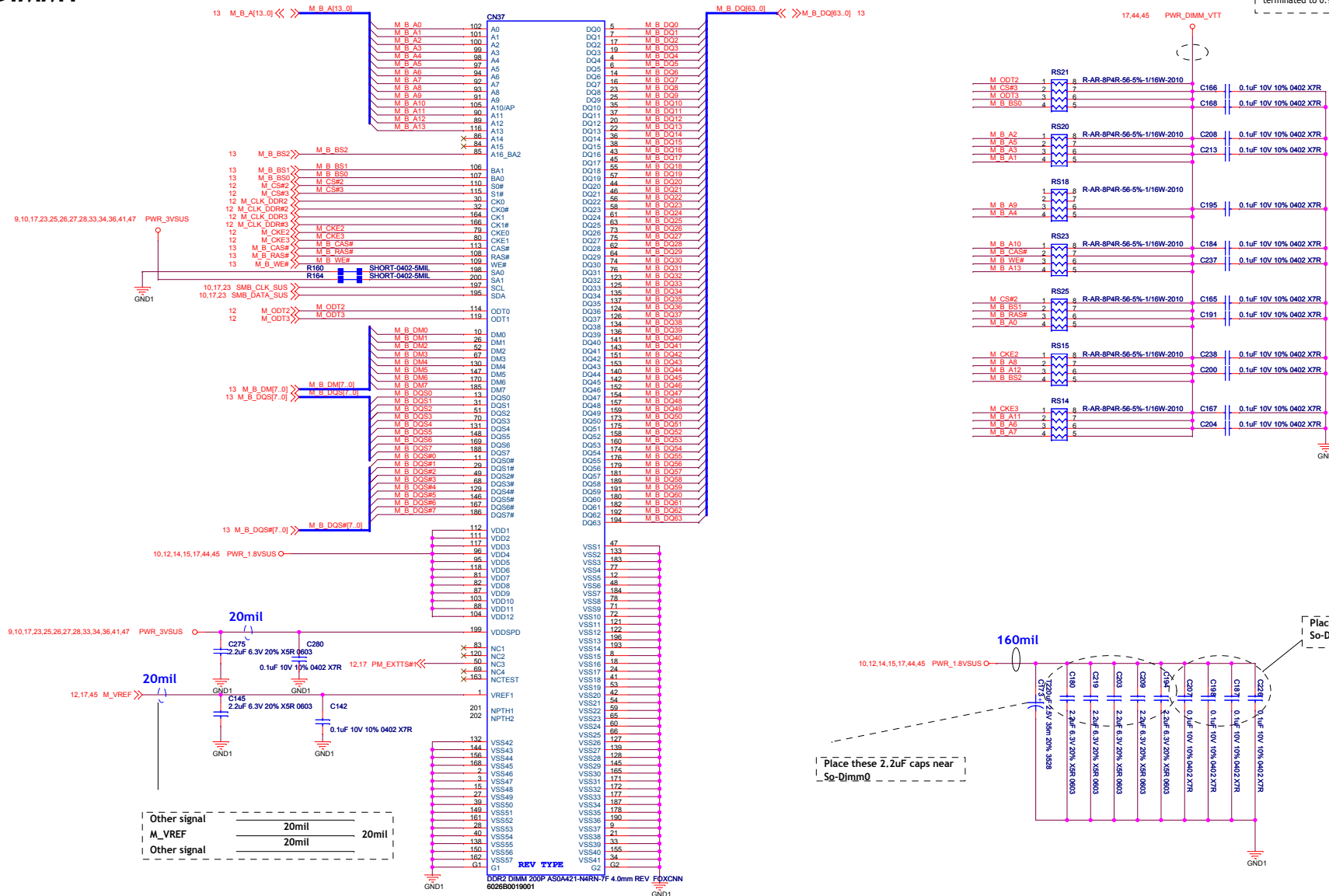


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SO-DIMM 1

- | Place one cap close to every 2 pullup resistors
- | terminated to 0.9VDDT_DDR11



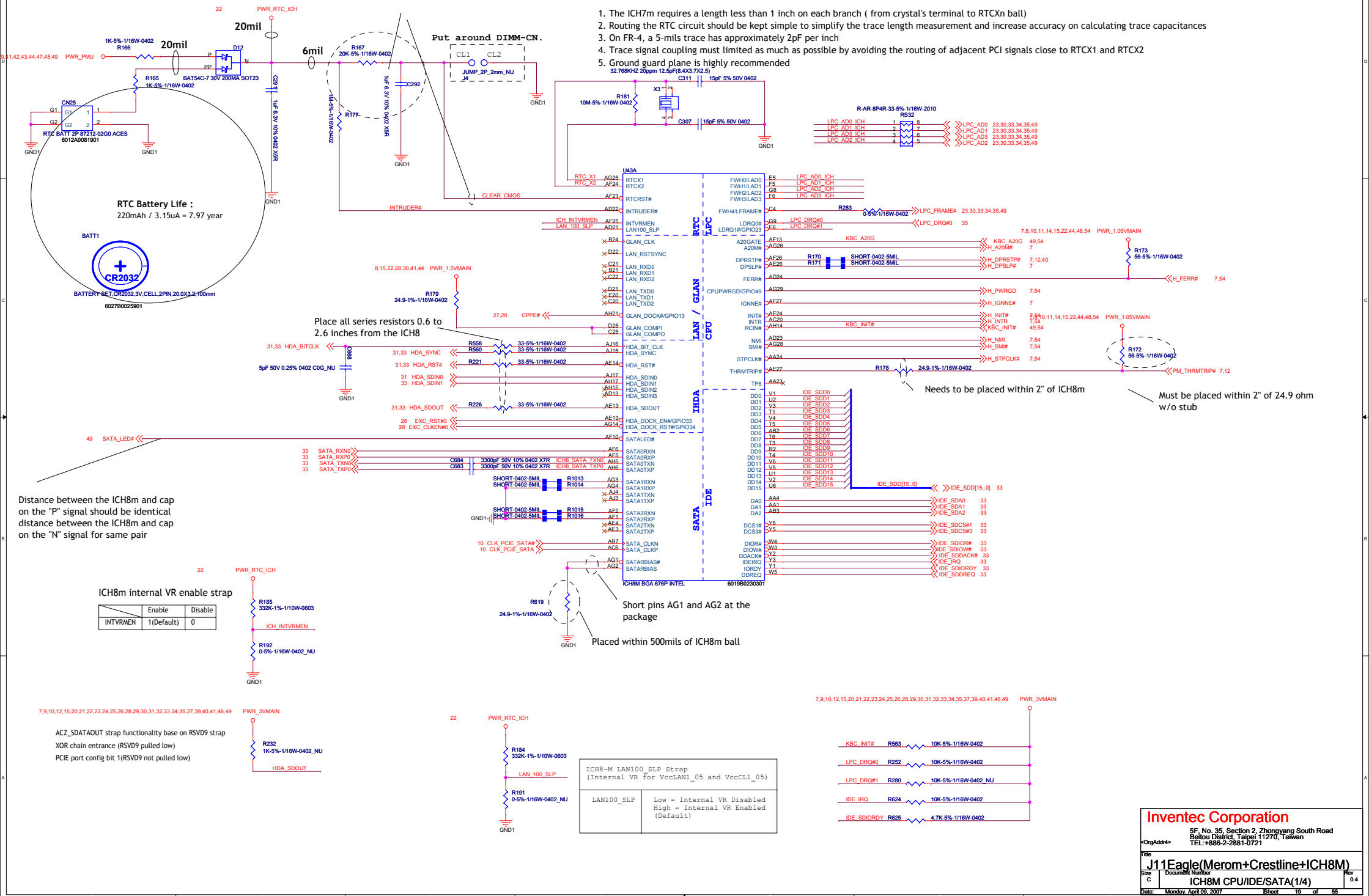
Place these 0.1uF caps near
So-Dimm1 pin79-pin115 area

Place these 2.2uF caps near
So-Dimm0

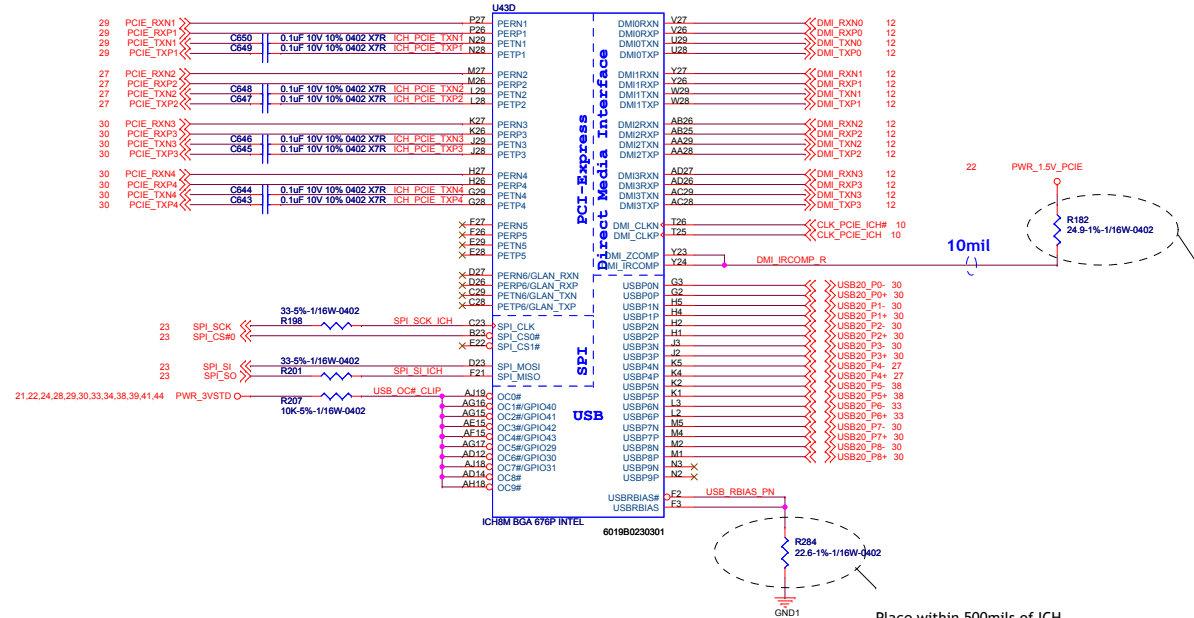
RTC Circuit

1. RC delay time should be in the range of 18-25ms
2. It is recommended that this larger capacitor and small resistor value in order to reduce the likelihood of glitching of RTCRST#

1. The ICH7m requires a length less than 1 inch on each branch (from crystal's terminal to RTCn ball)
2. Routing the RTC circuit should be kept simple to simplify the trace length measurement and increase accuracy on calculating trace capacitances
3. On FR-4, a 5-mils trace has approximately 2pF per inch
4. Trace signal coupling must limited as much as possible by avoiding the routing of adjacent PCI signals close to RTCX1 and RTCX2
5. Ground guard plane is highly recommended

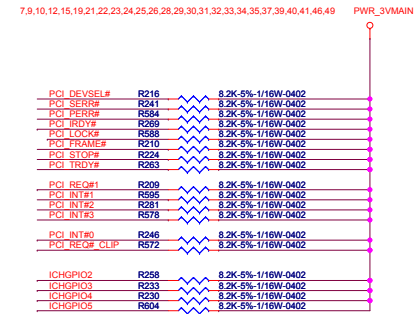


PCIE AC coupling caps need to be
within 250mils of the driver

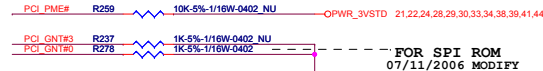
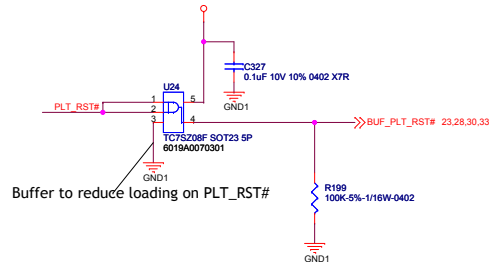


Place within 500mils of ICH
5/5 mils spacing on microstrip

PCI Pull up



7,9,10,12,15,19,21,22,23,24,25,26,28,29,30,31,32,33,34,35,37,39,40,41,46,49



PCI_GNT#3 No stuff : by default
Stuff : For A16 swap override

PCI_GNT#0	SPI_CS1#	
1	1	LPC
1	0	PCI
0	1	SPI

Check BIOS type

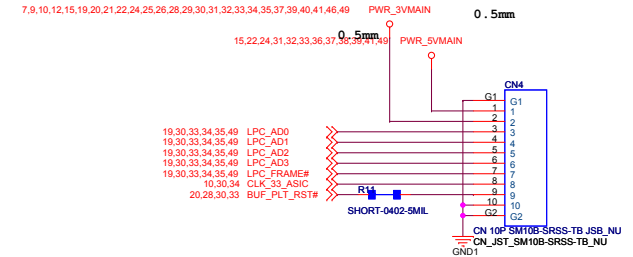
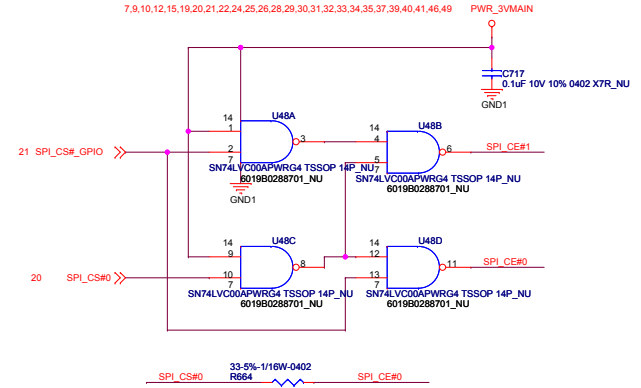
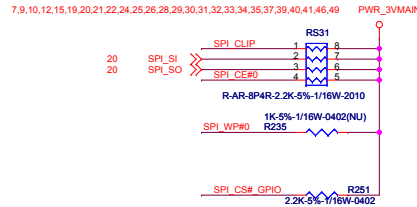
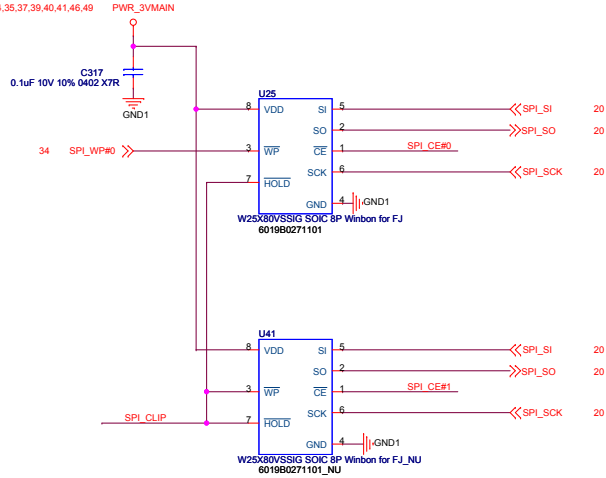
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Beitou District, Taipei 11270, Taiwan
TEL:+886-2-2881-0721

File J11Eagle(Merom+Crestline+ICH8M)
Size C Document Number ICH8M PCI/PCIE/DMI/USB(2/4)
Rev 04

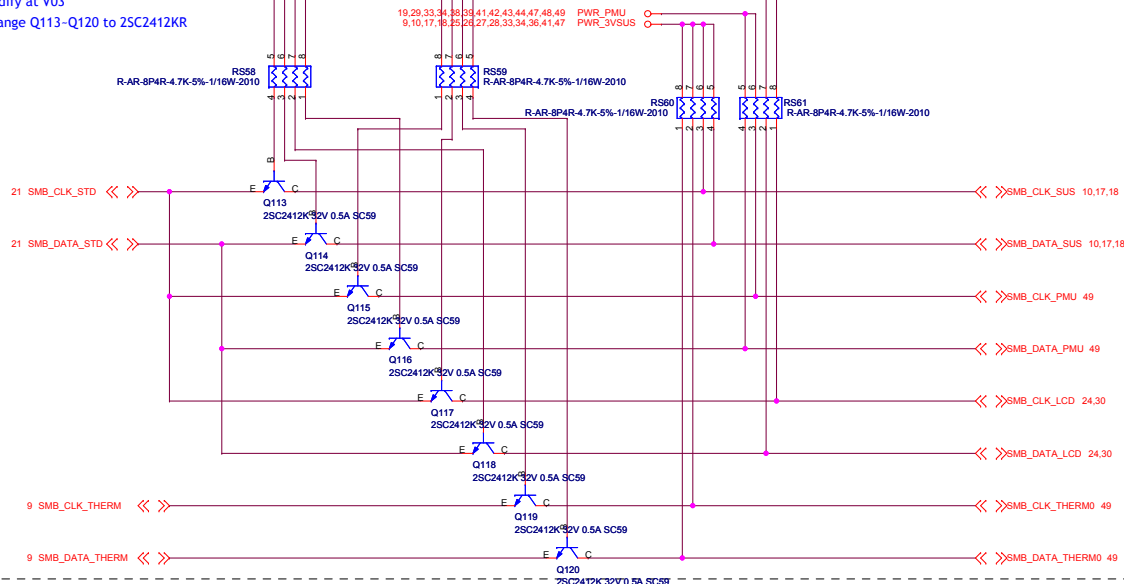
Date: Monday, April 09, 2007 Sheet 20 of 55

Delete at 2006/12/20



PORT80

Modify at V03
Change Q113-Q120 to 2SC2412KR



Device	Hex	Address
ADT7473	5Ch	0101 110x b
MEM slot0	A2h	1010 000x b
MEM slot1	A4h	1010 010x b
PMU	32h	0011 001x b
LCD (SPWG)	A0h	1010 000x b
JEPICO	90h	1001 000x b

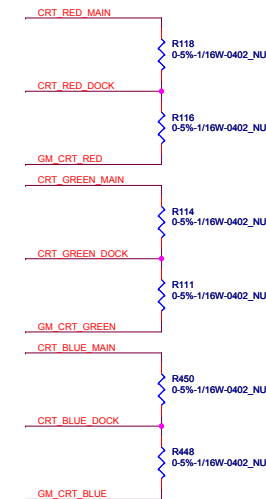
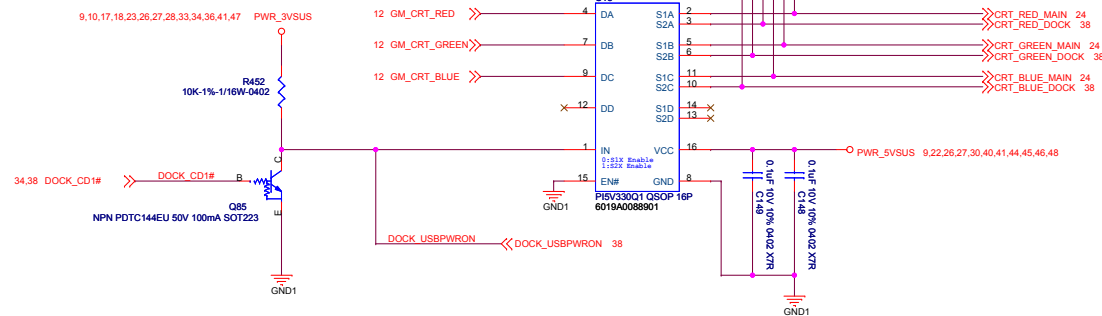
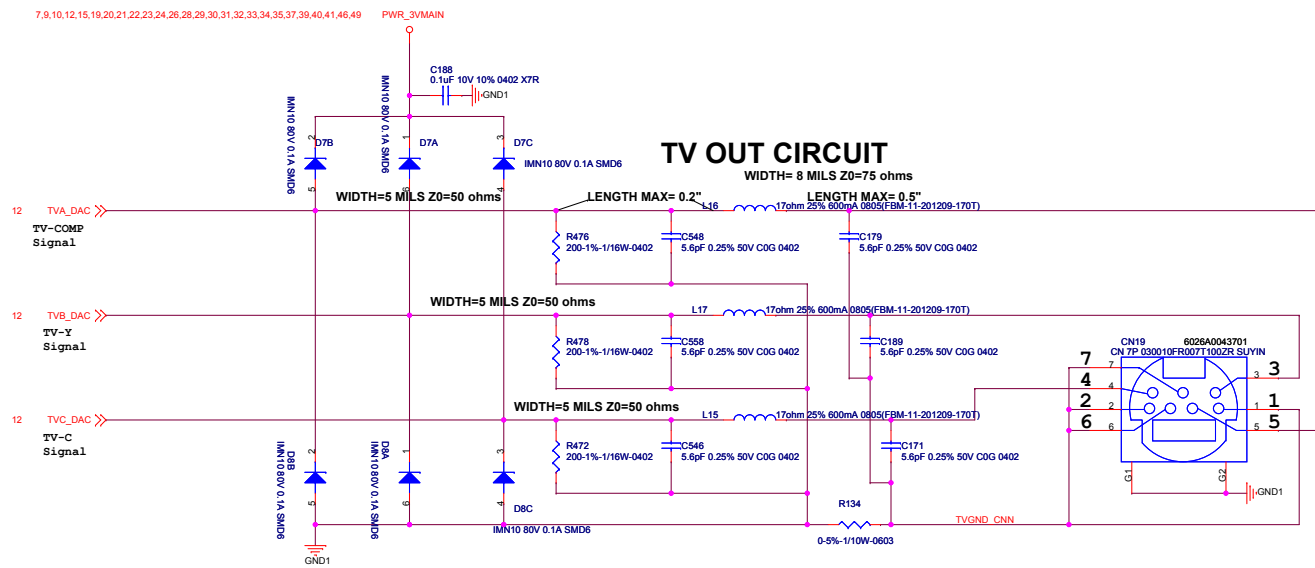
CBT3253 NPUS FUNCTION
OE S1 S0 FUNCTION
L L L A port = B1 port
L L H A port = B2 port
L H L A port = B3 port
L H H A port = B4 port
H X X Disconnect

SMBCNT[2:0]	Device
0,0,0	DIMM SLOT 0/1,CLK GEN.
0,0,1	EC control
0,1,0	EC control,ADT7473
0,1,1	LCD (SPWG),MiniCard

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5F, No. 35, Section 2, Zhongyang South Road
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TEL: +886-2-2861-0721

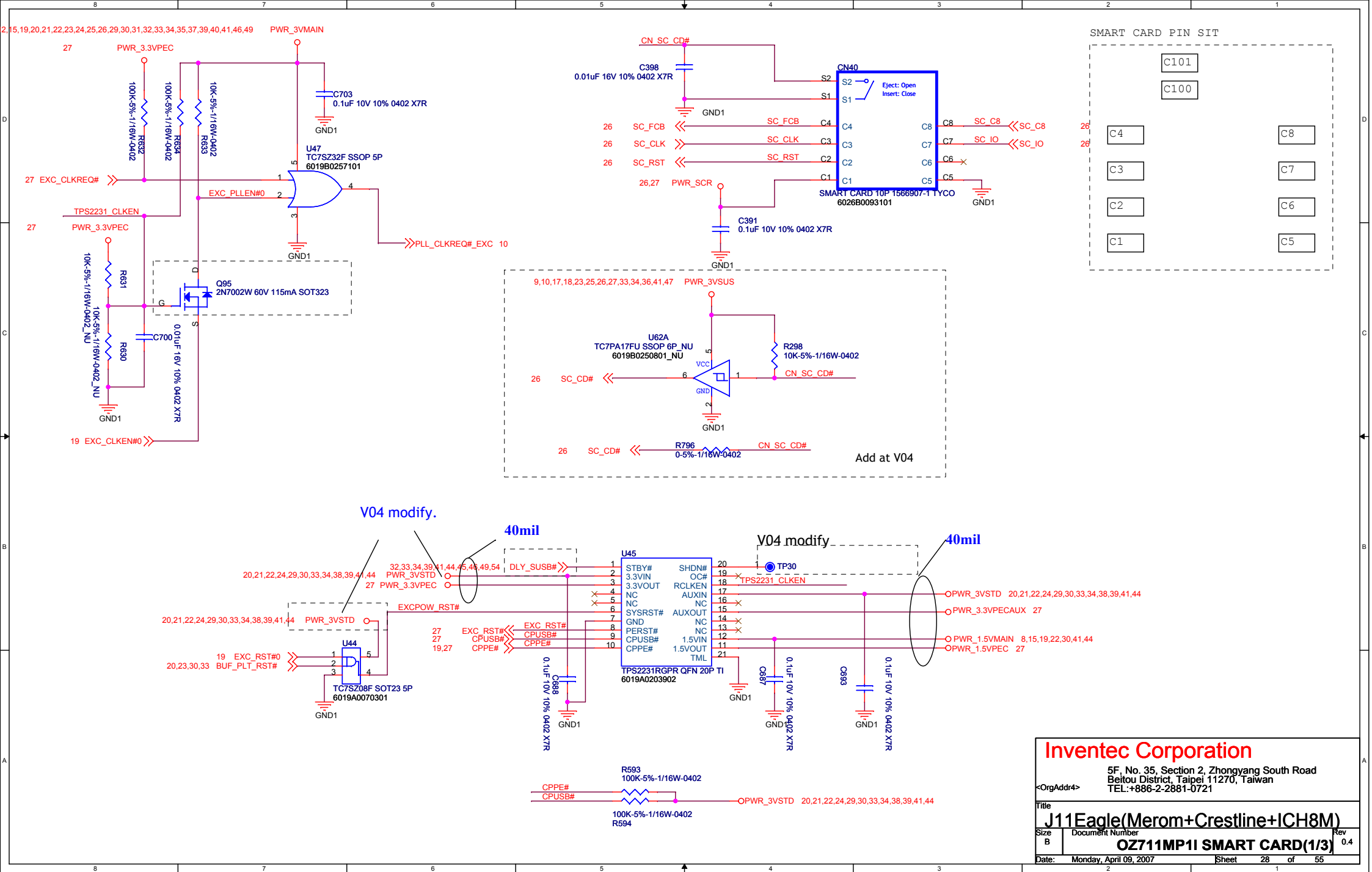
File	J11Eagle(Merom+Crestline+ICH8M)
Size	Document Number
C	BIOS/SMBUS SW/80 PORT
Date	Monday, April 09, 2007
Sheet	23 of 55
Rev	0.4



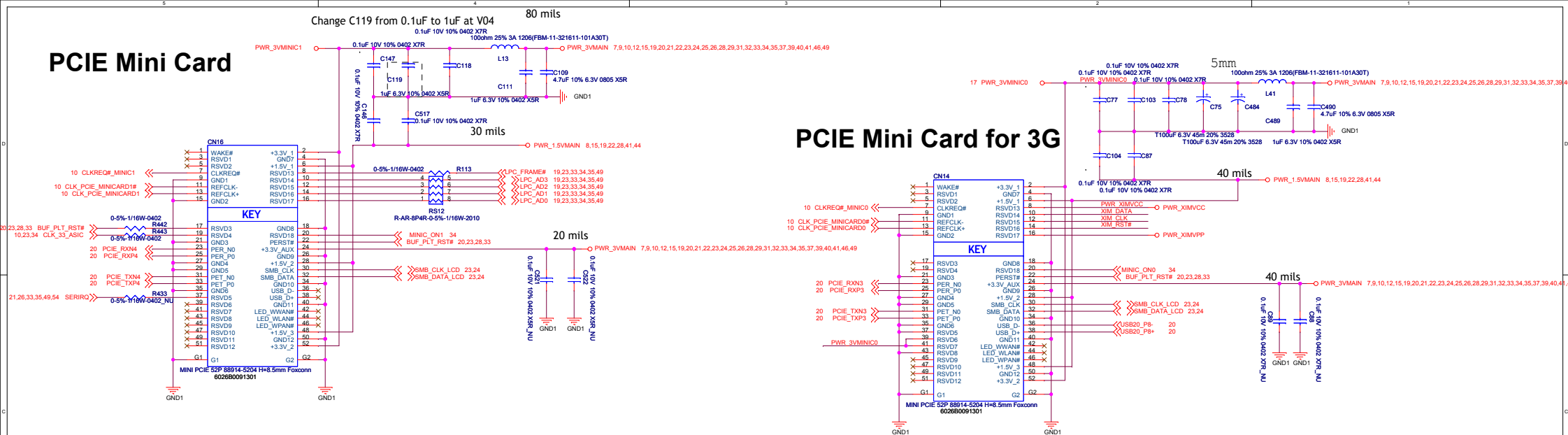
Inventec Corporation

5F, No. 35, Section 2, Zhongyang South Road
Beitou District, Taipei 11270, Taiwan
TEL: +886-2-2861-0721

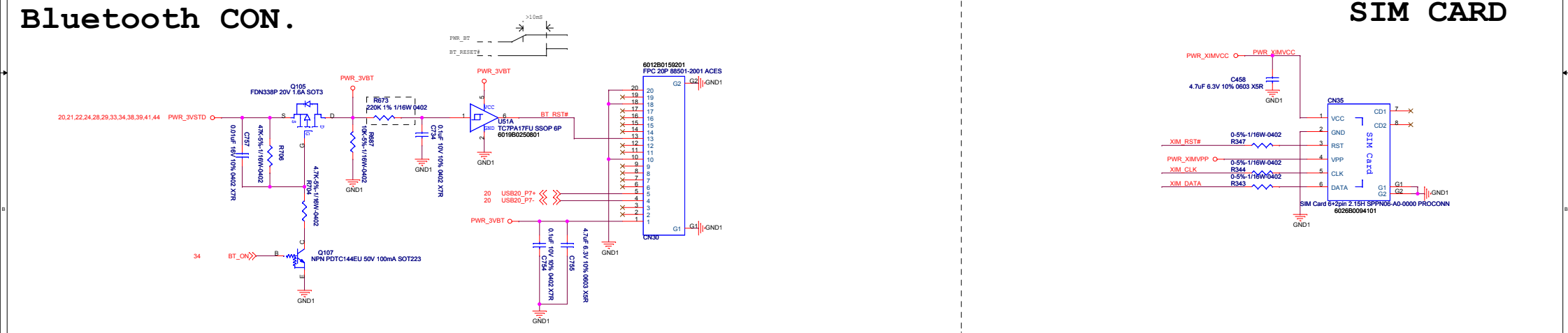
Title		Rev
J11Eagle(Merom+Crestline+ICH8M)		0.4
Size	Document Number	
C	TV OUT & CRT SW	
Date:	Monday, April 09, 2007	Sheet 25 of 55



PCIE Mini Card

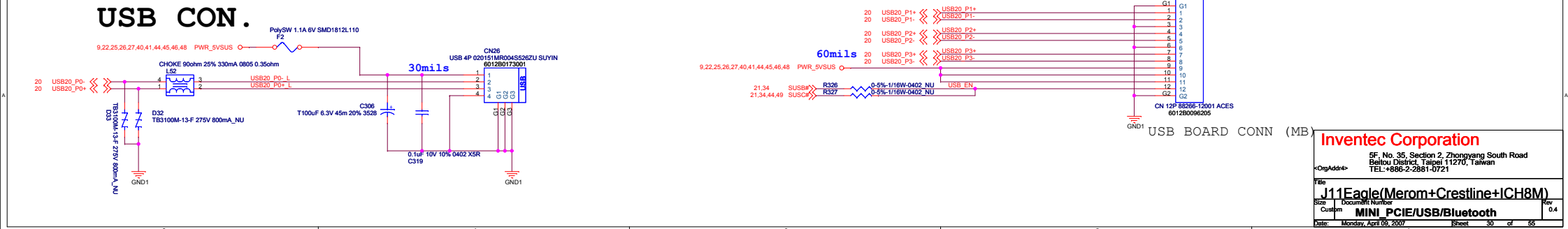


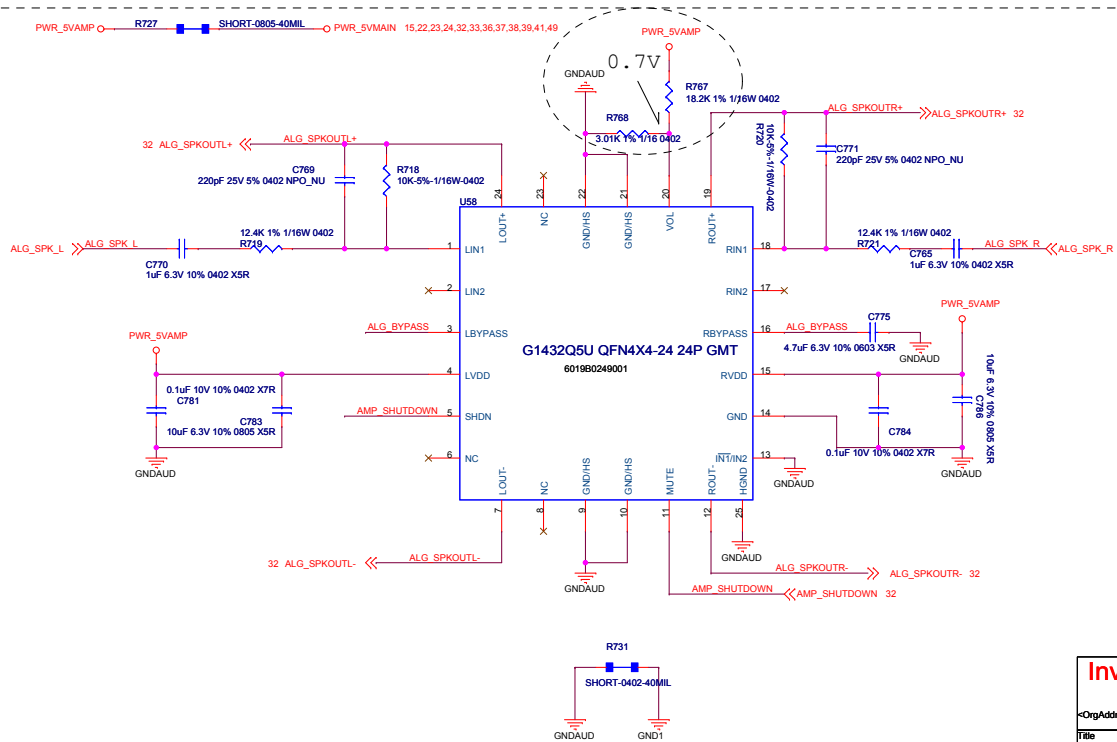
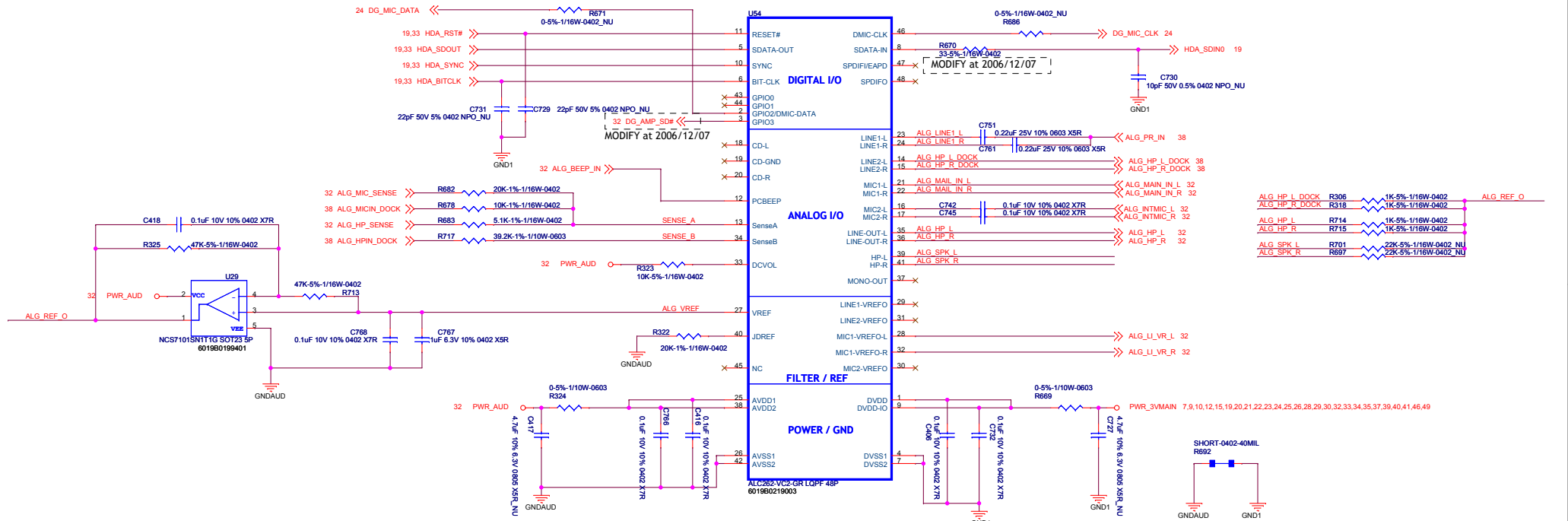
Bluetooth CON.



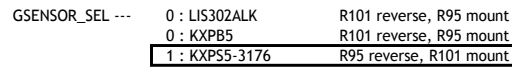
SIM CARD

USB CON.

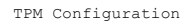




SATA CON.

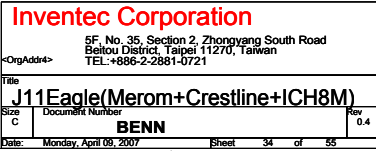


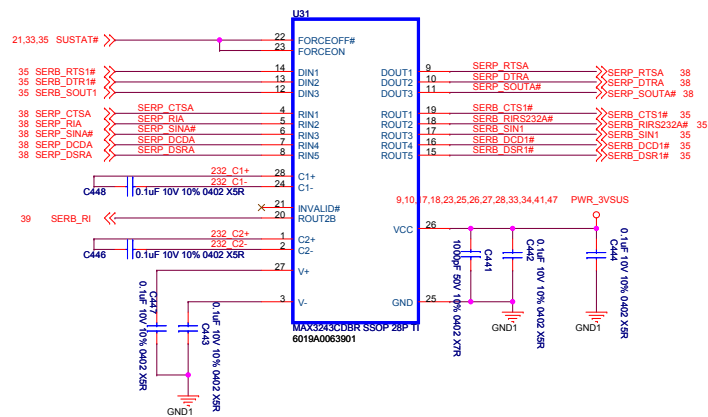
TPM CON.



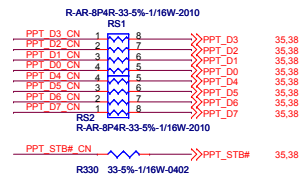
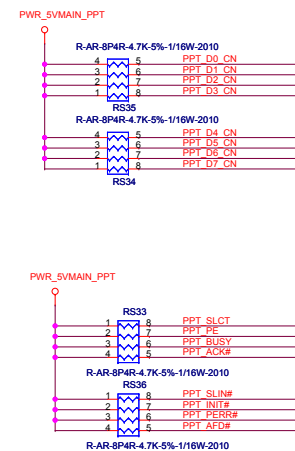
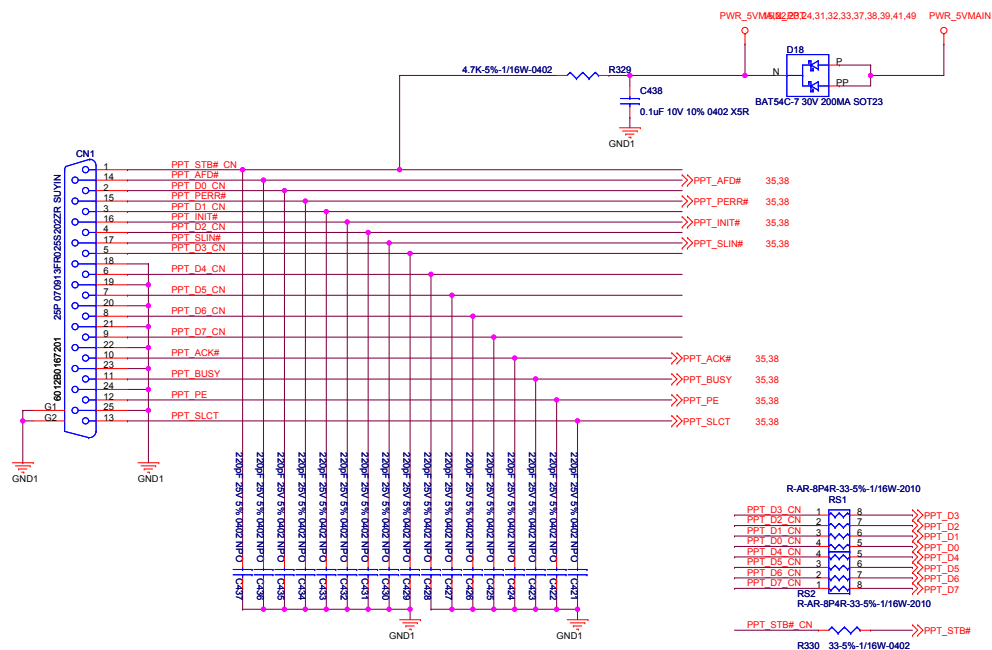
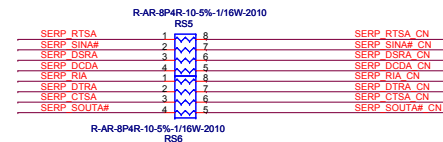
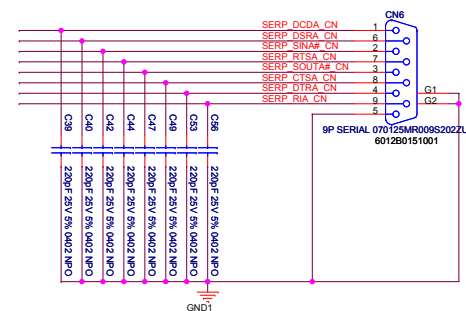
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TPM_PACCESS	Physical Presence ON	Physical Presence OFF







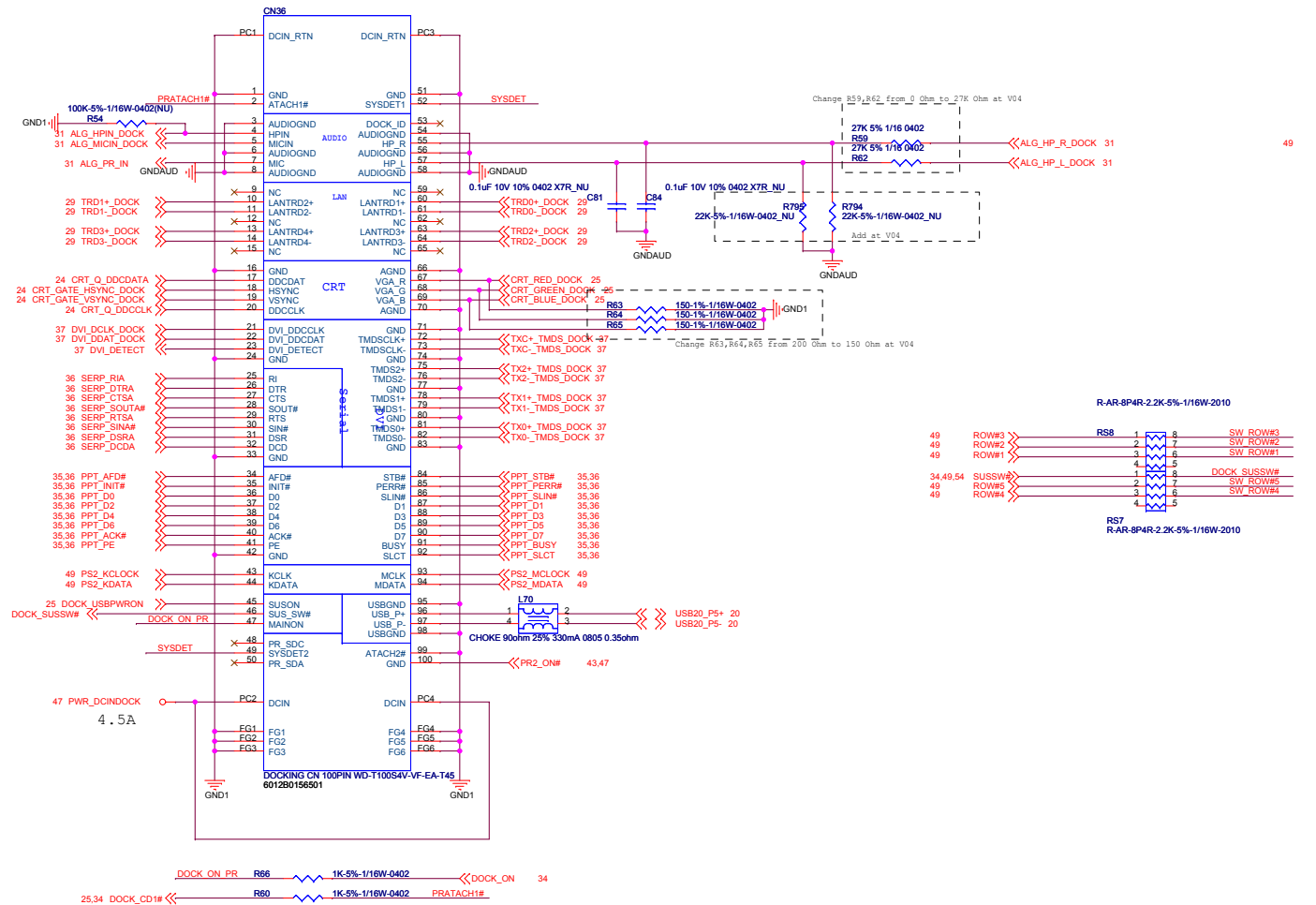
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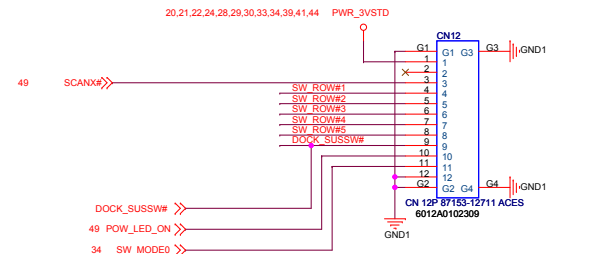
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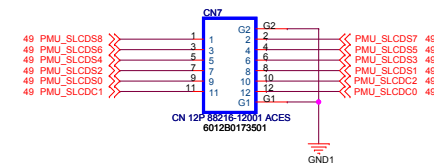
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SW BOARD

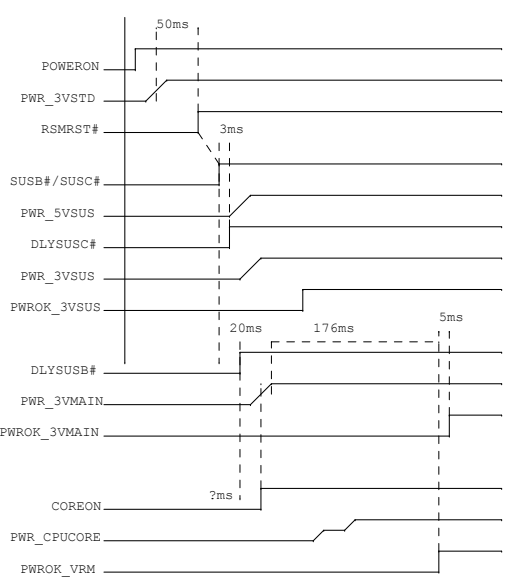


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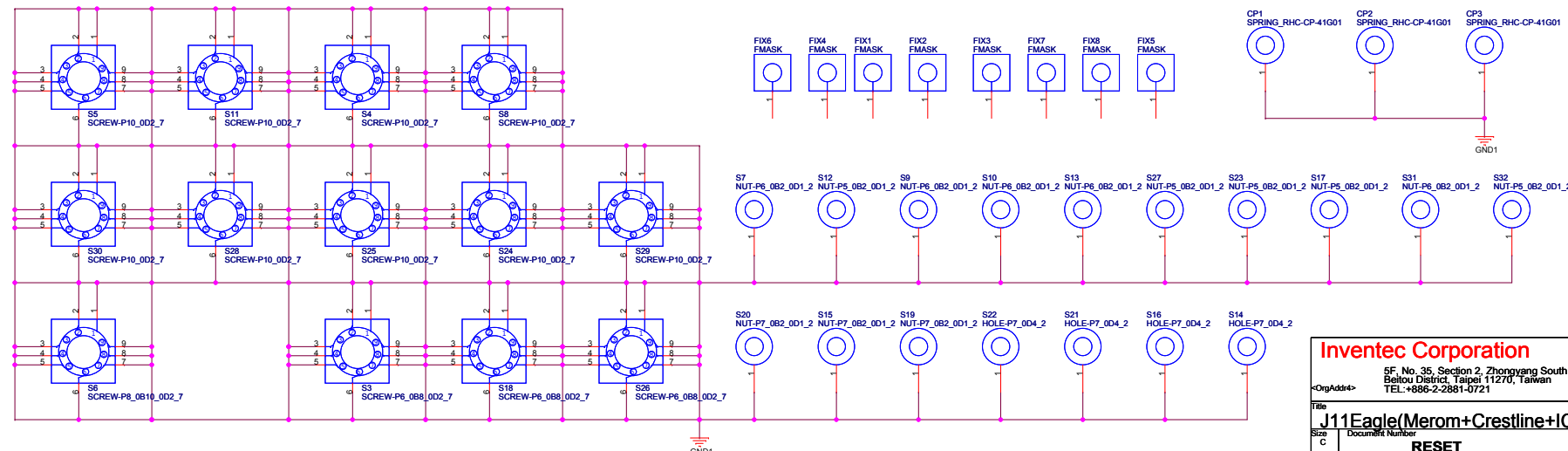
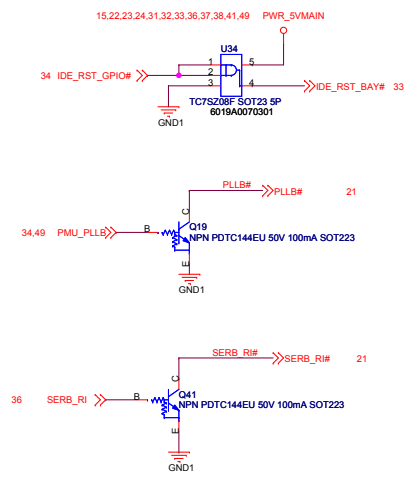
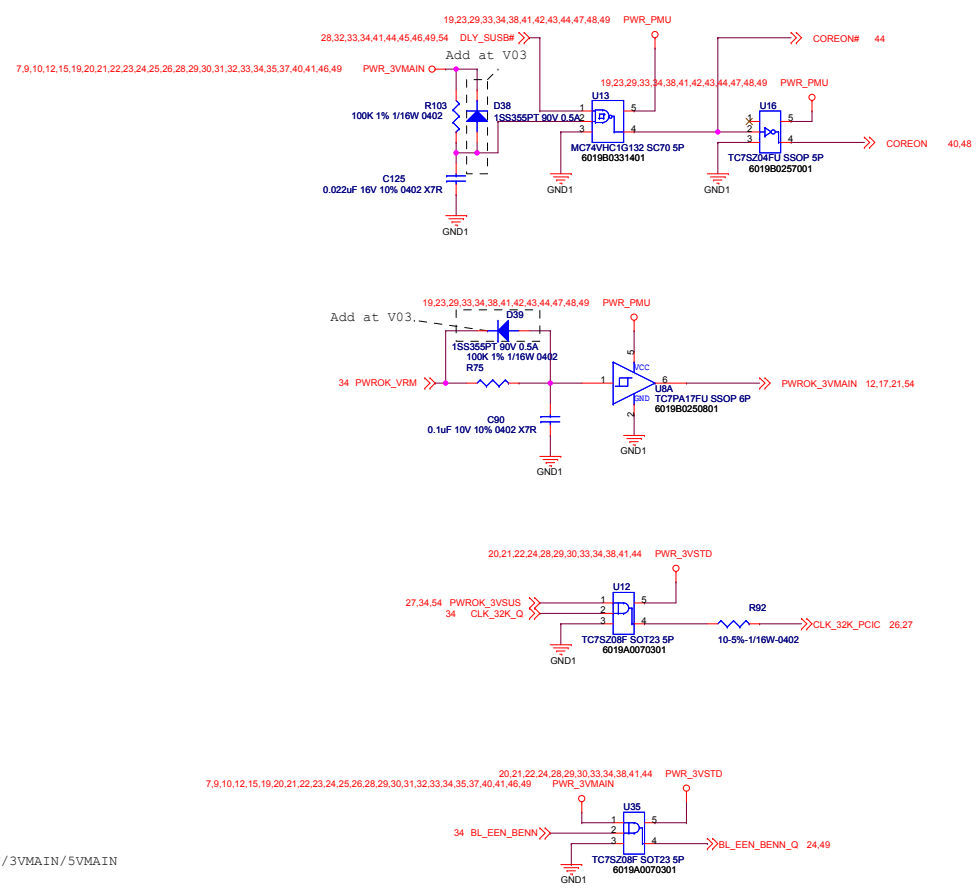
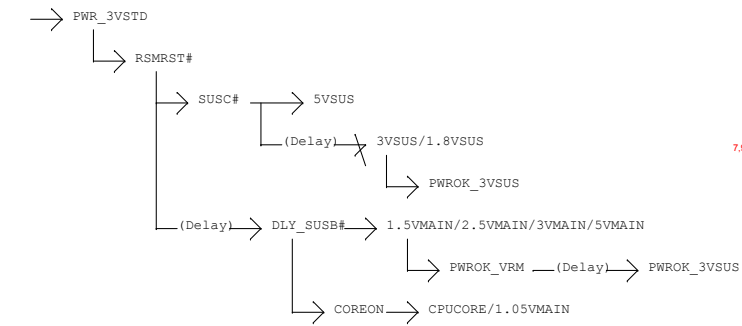


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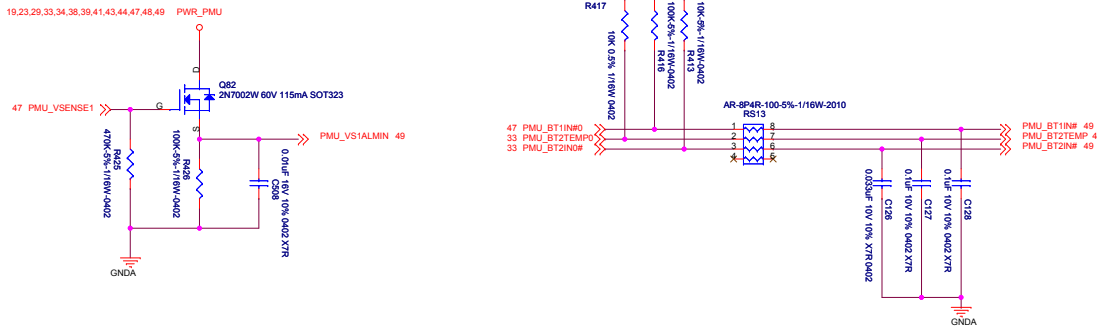
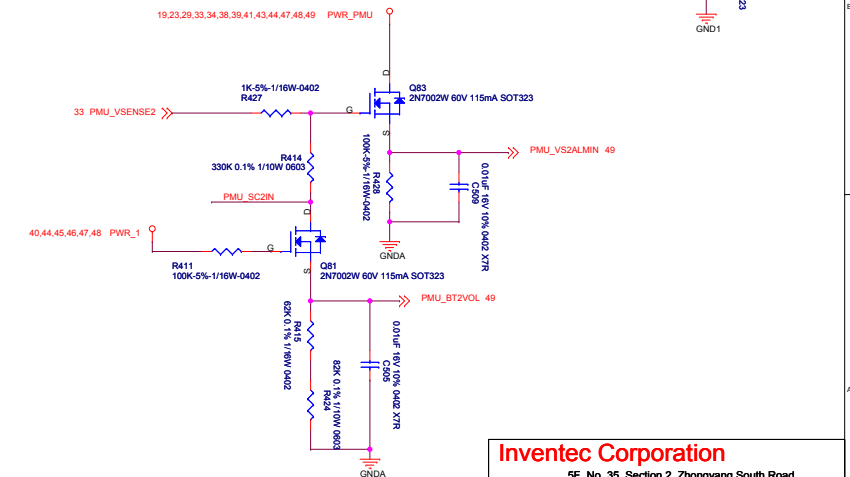
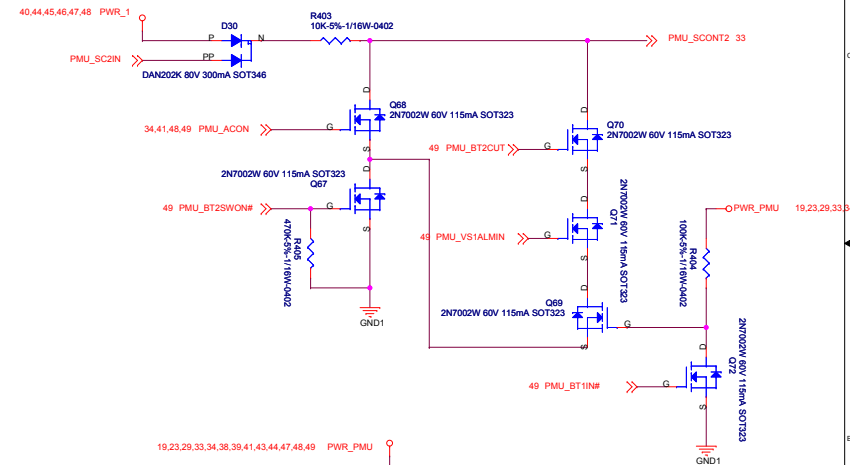
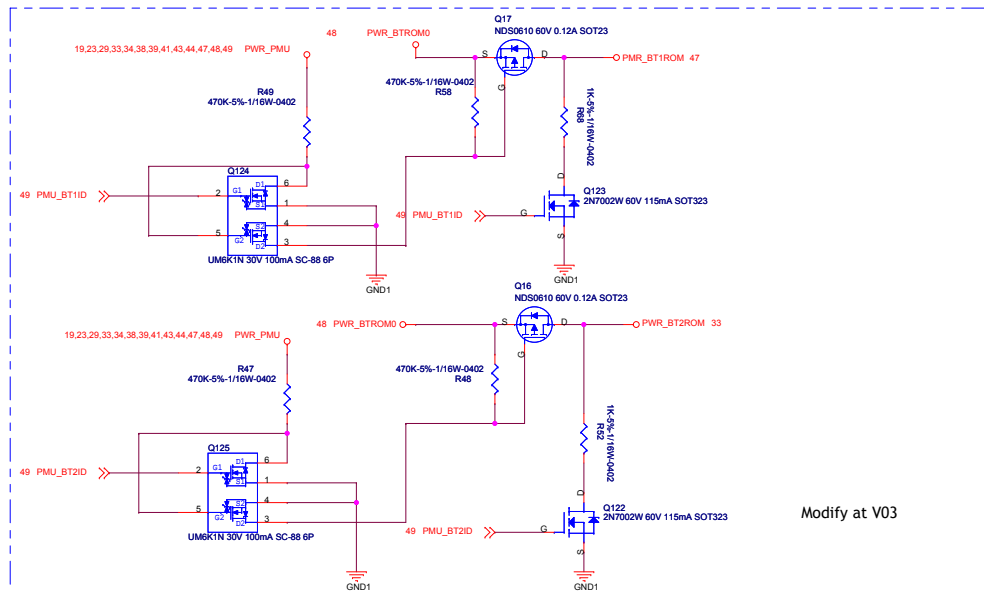
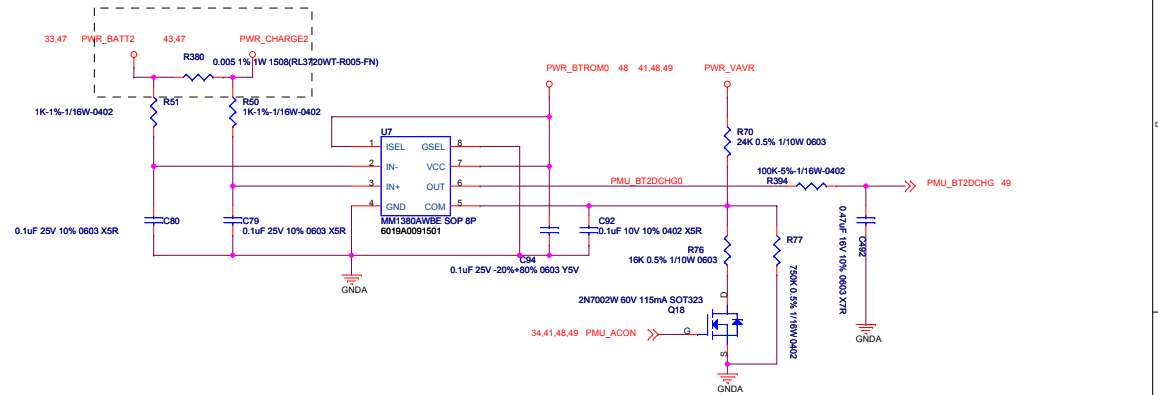
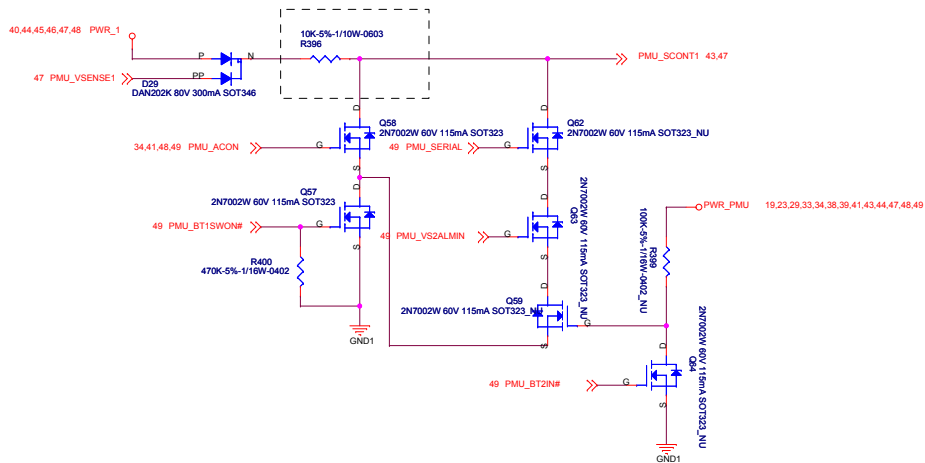


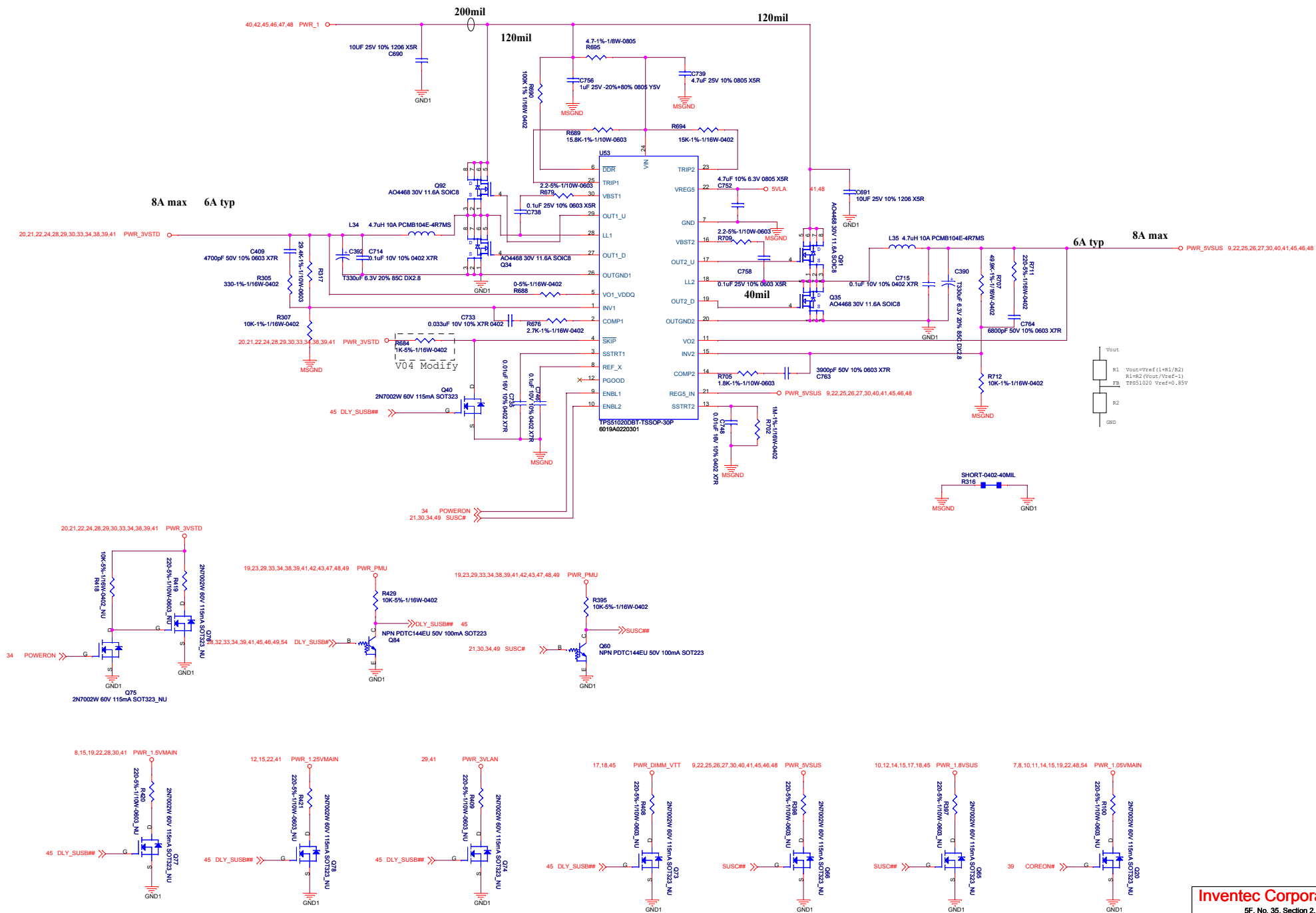
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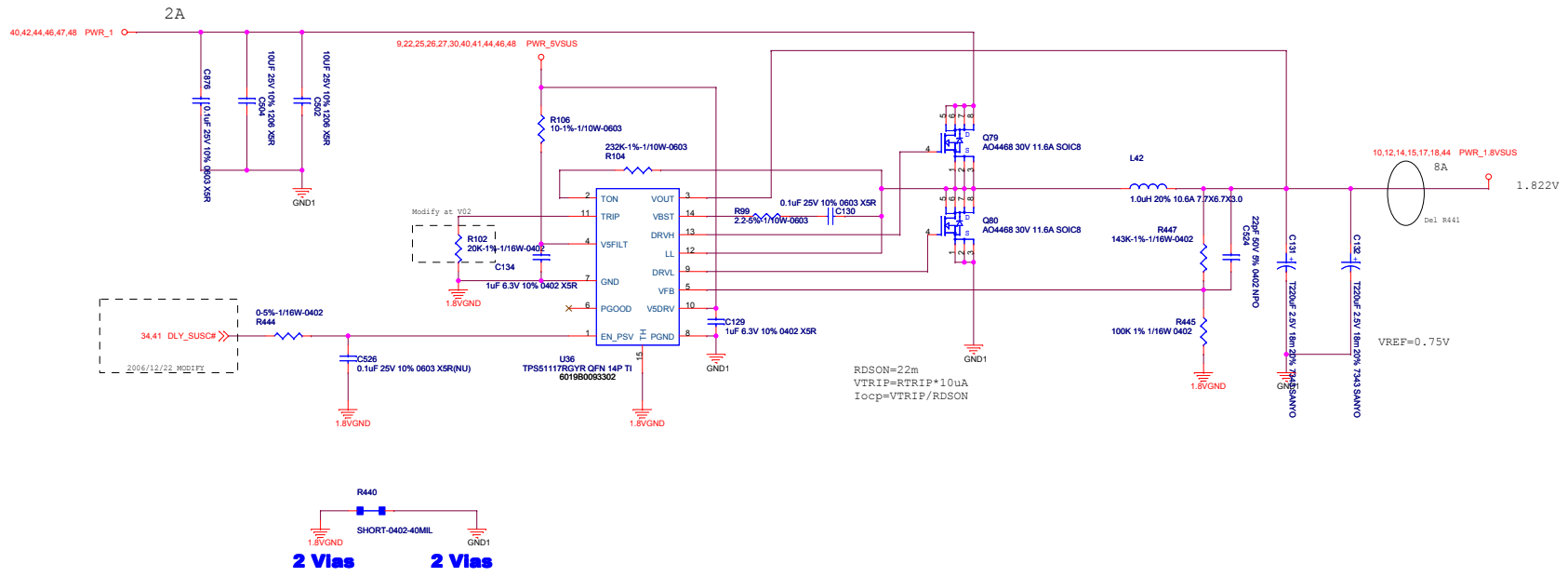


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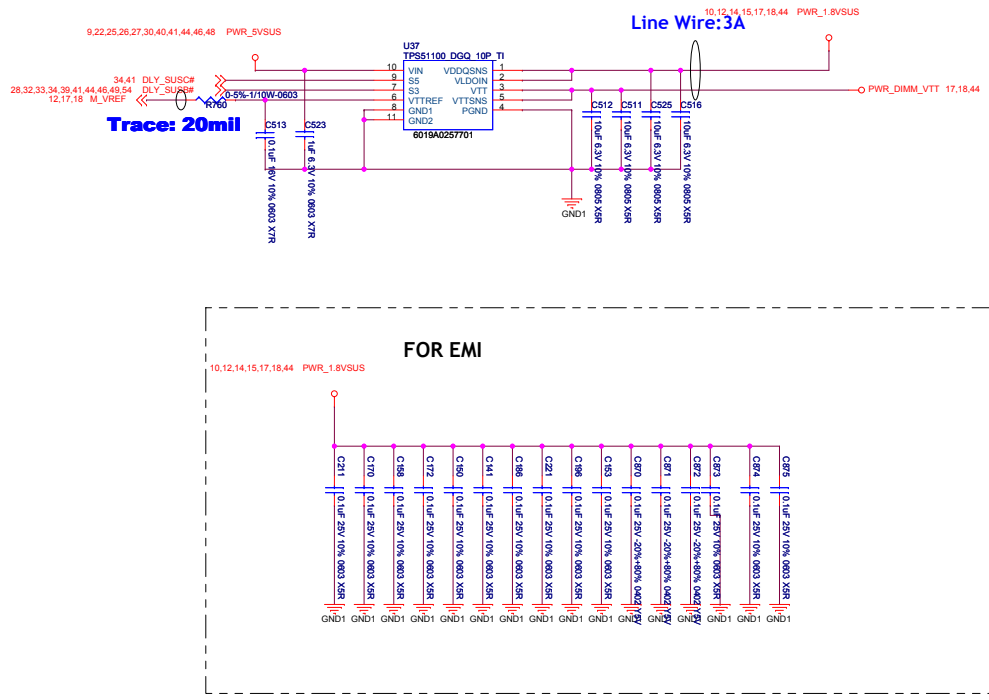
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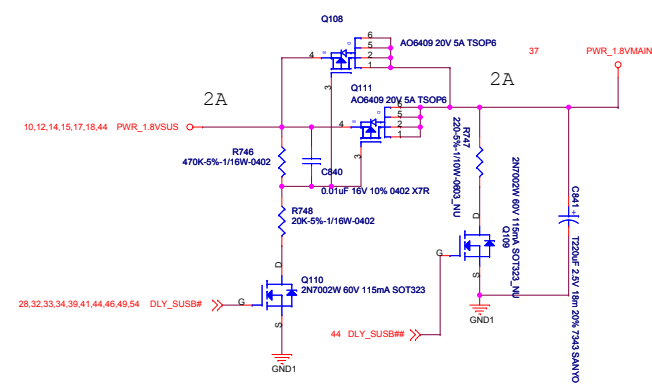


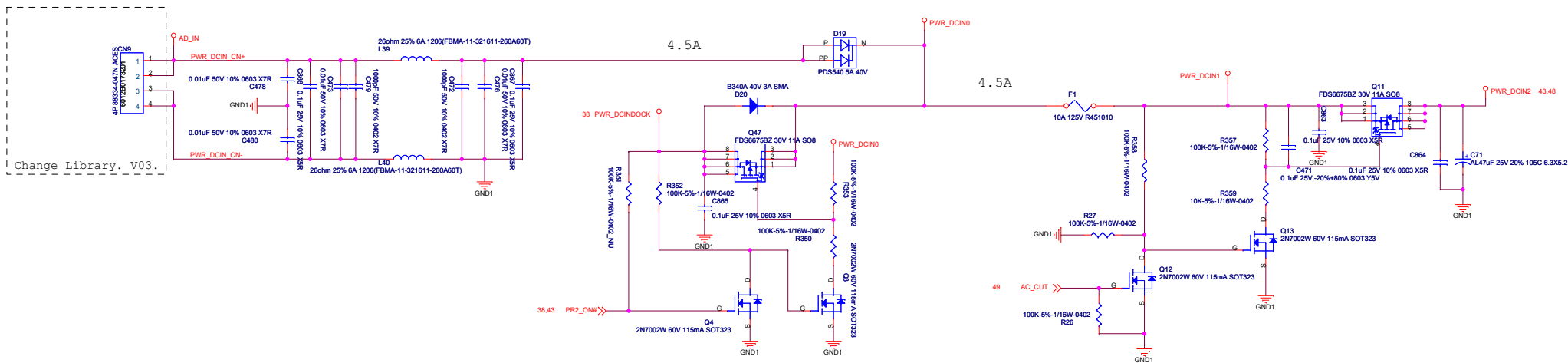


DDRII Terminator Power

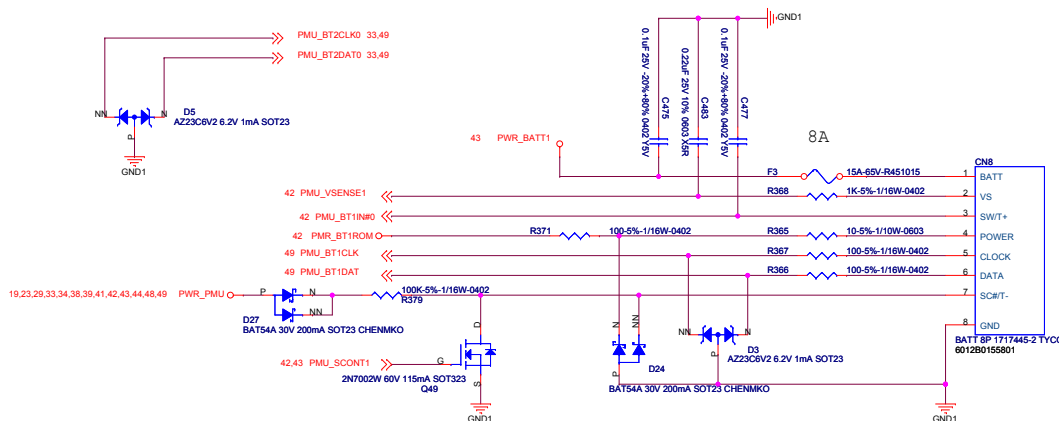
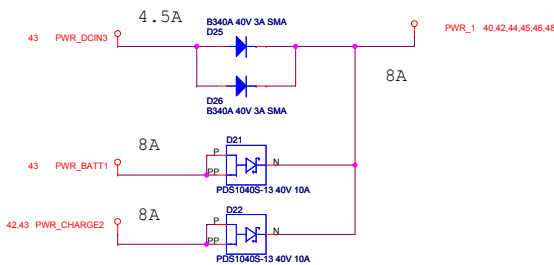
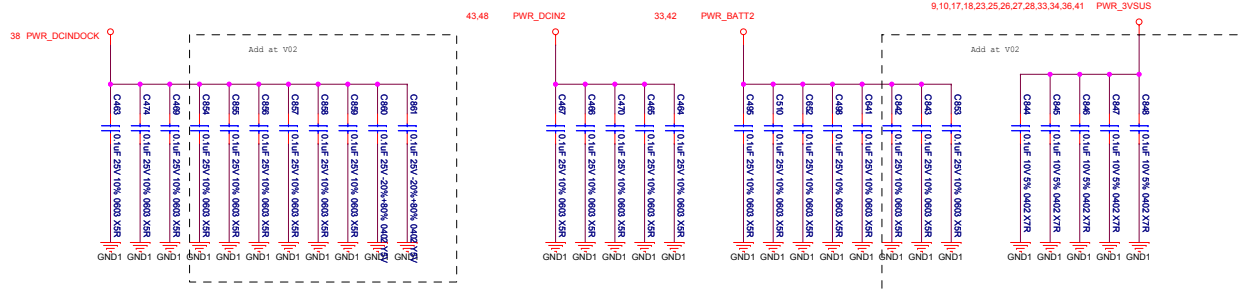


1.8V FOR DVI





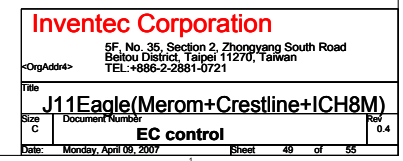
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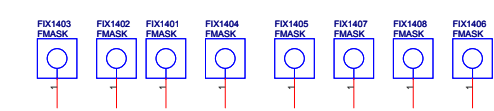
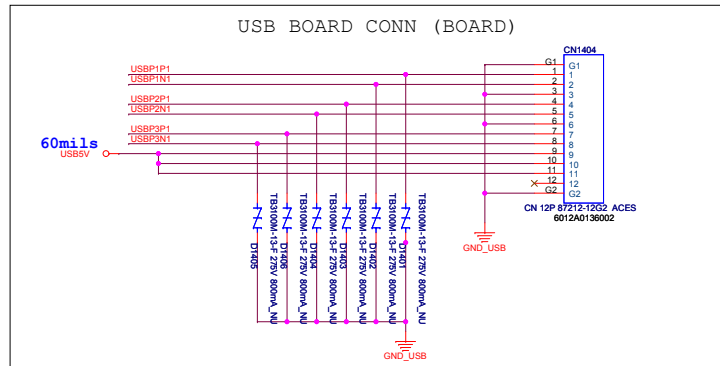
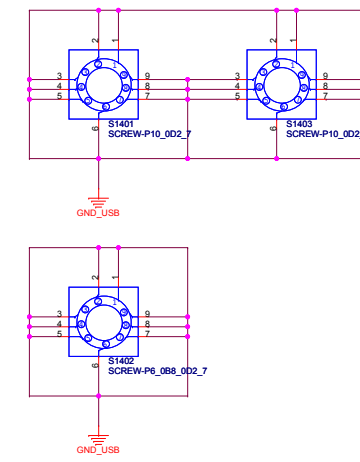
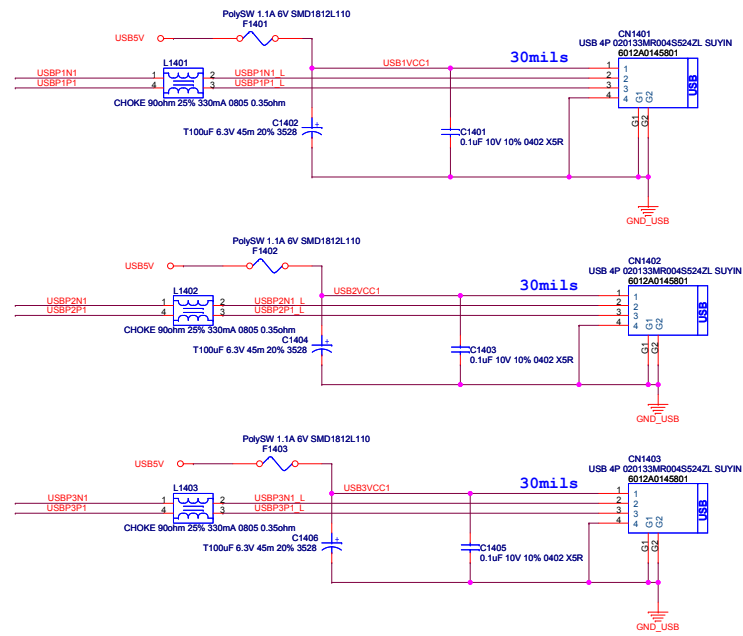


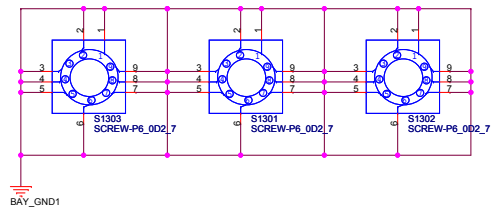
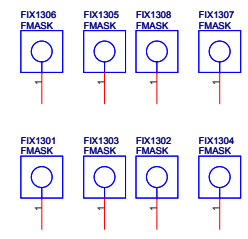
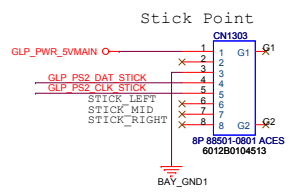
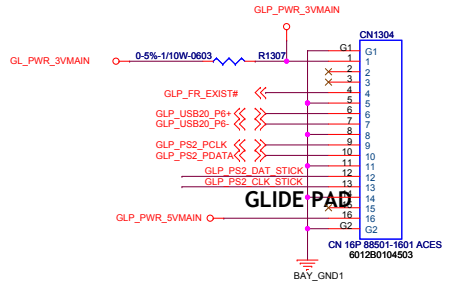
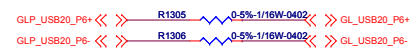
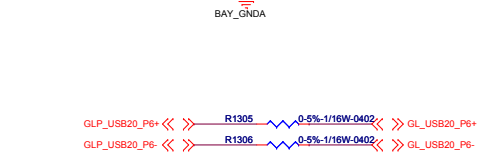
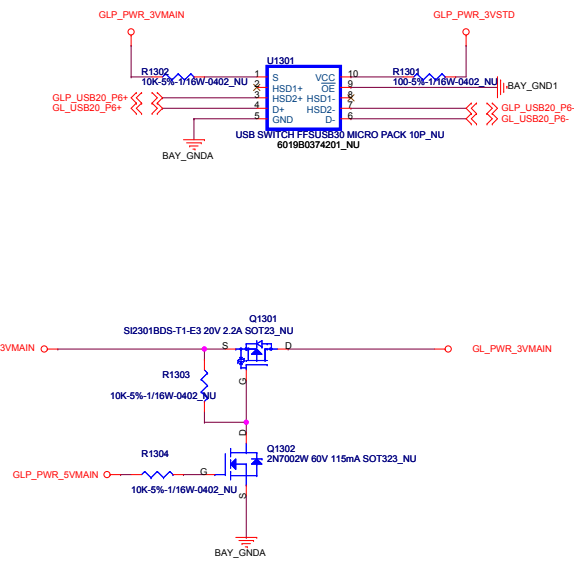
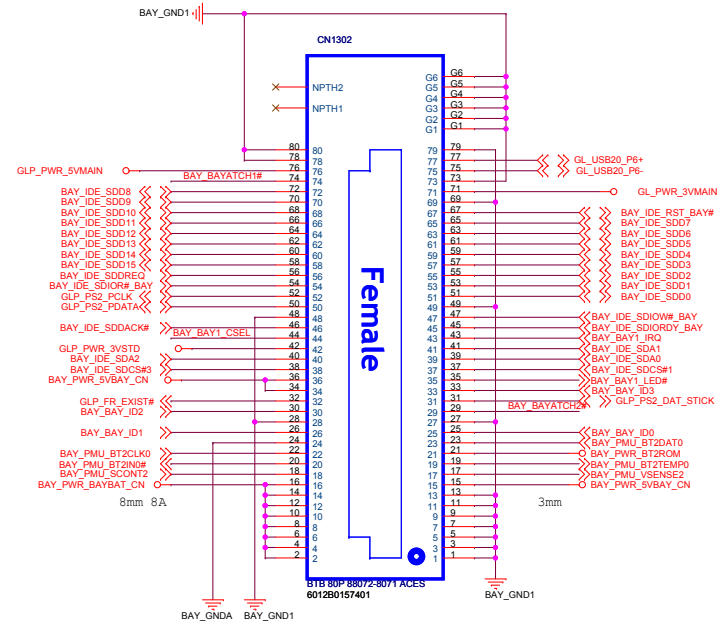
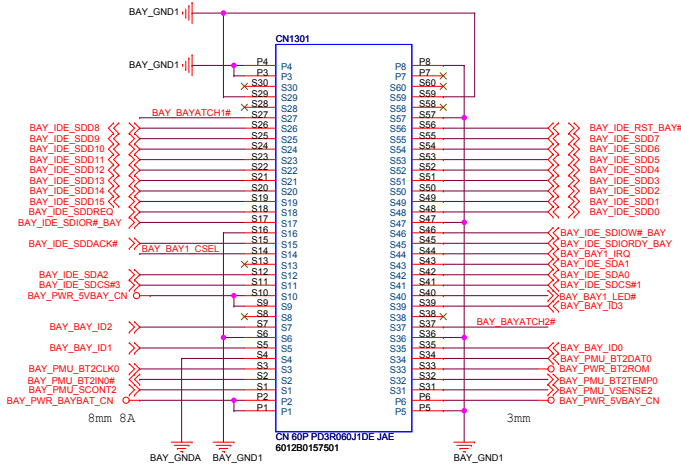
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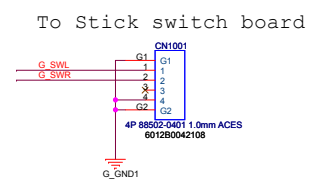
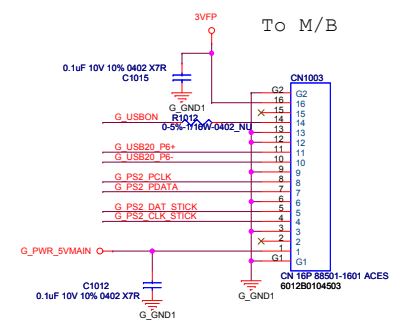
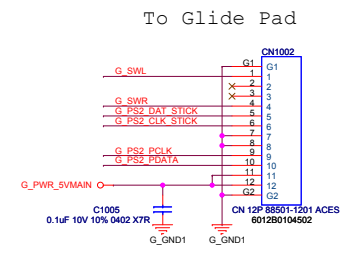
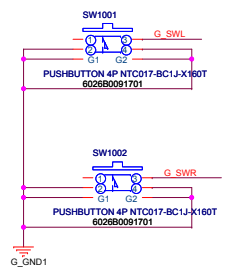
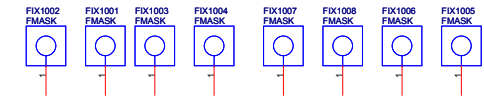
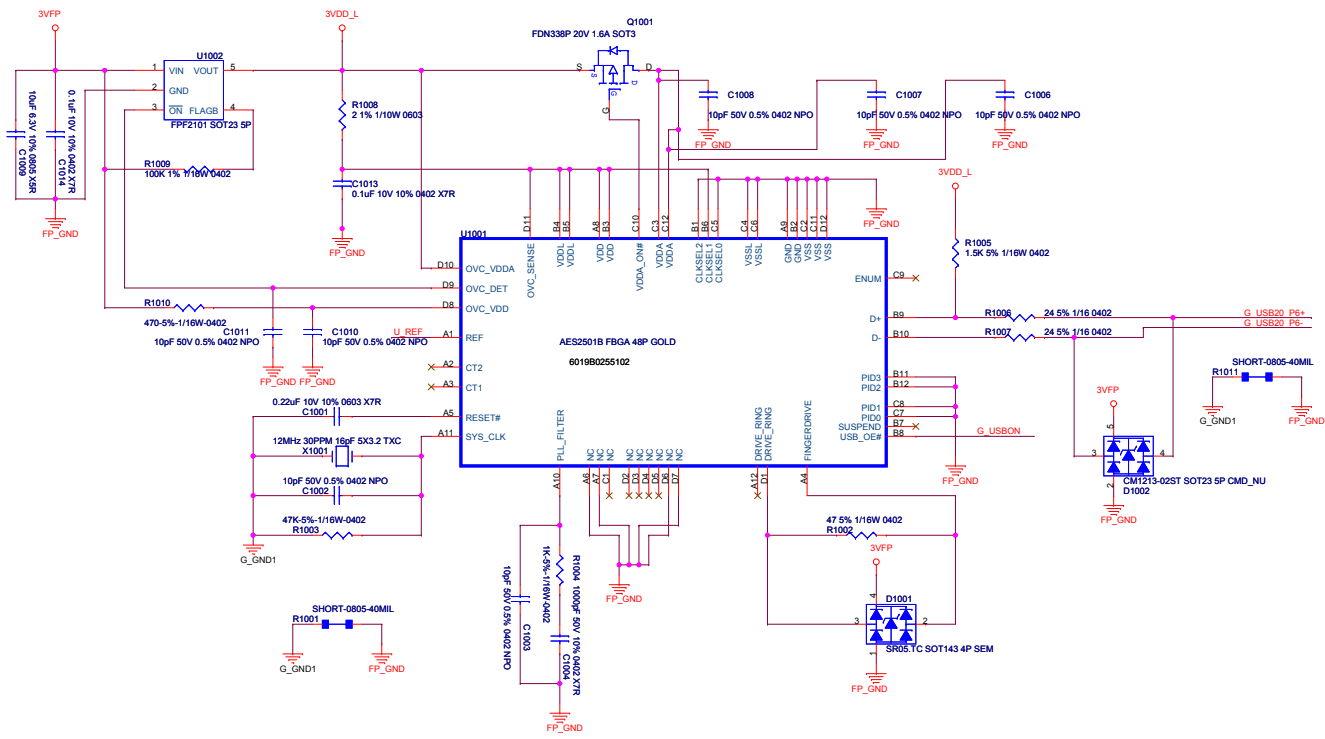
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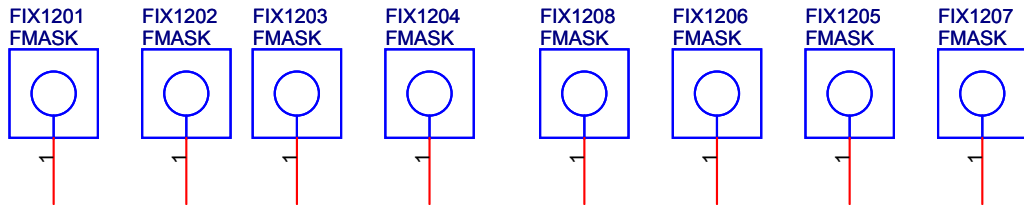
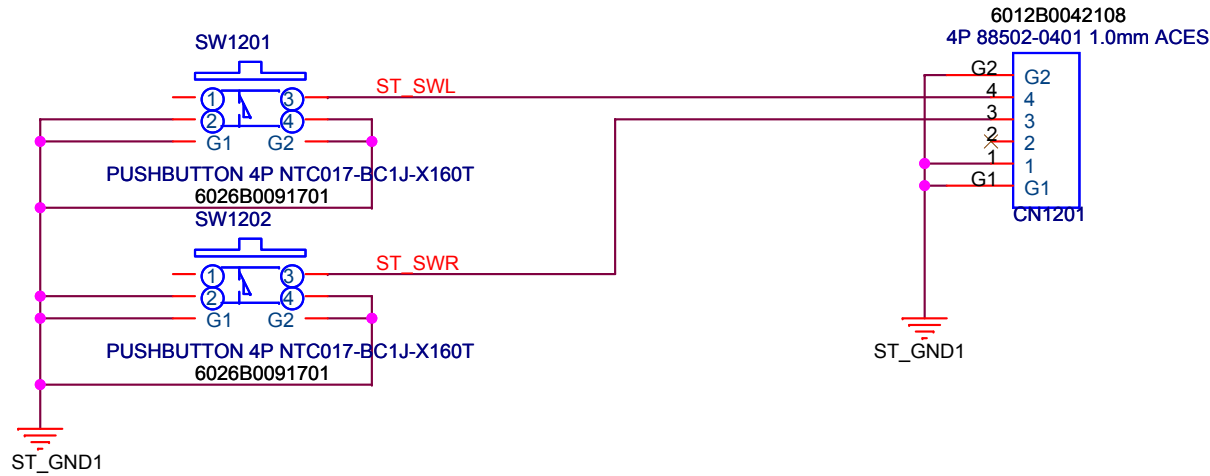








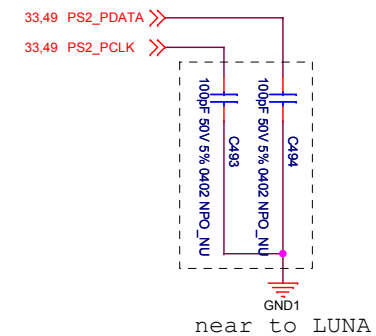
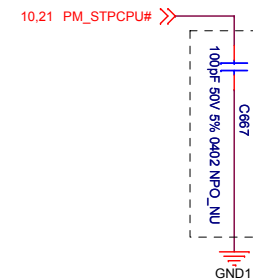
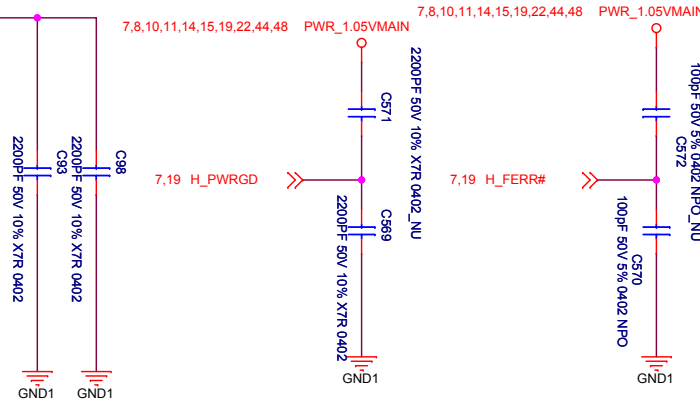
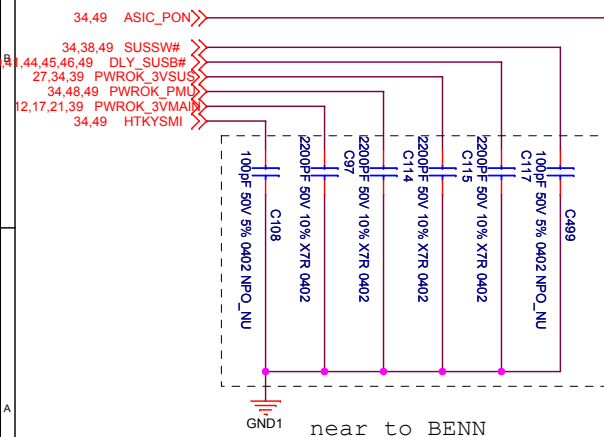
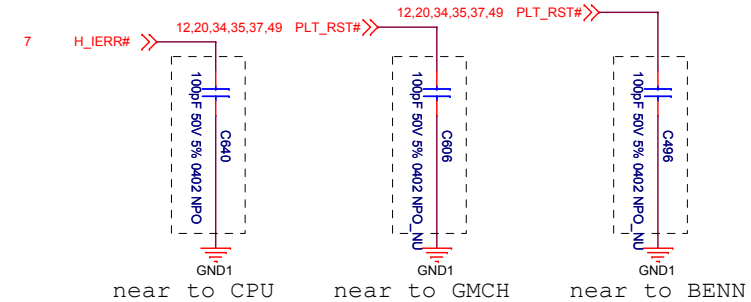
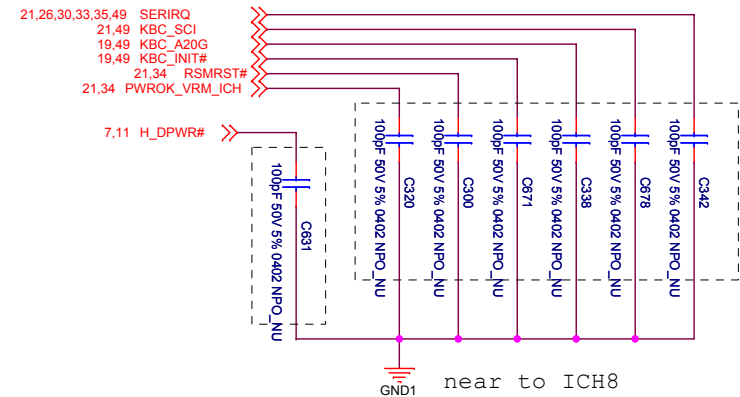
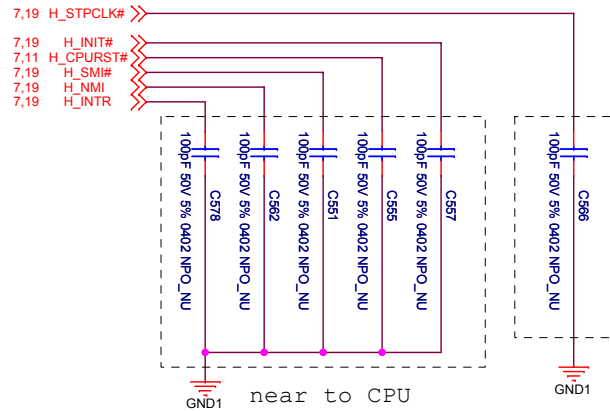
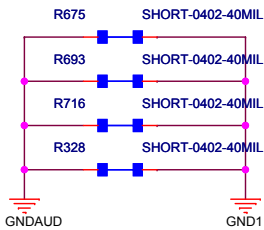
To Glide Pad switch board



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Title J11Eagle(Merom+Crestline+ICH8M)		
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For EMI

These resistors should be located the corner or Audio-GND.



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Title

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Size

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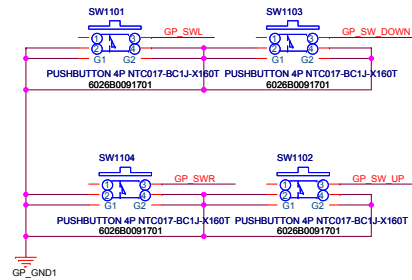
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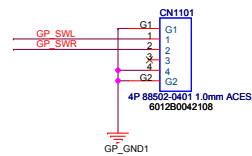
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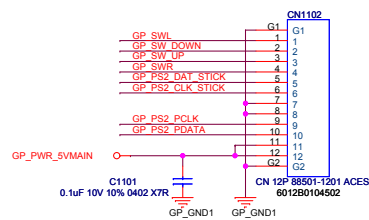
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To Stick switch board



To Glide Pad



To M/B

