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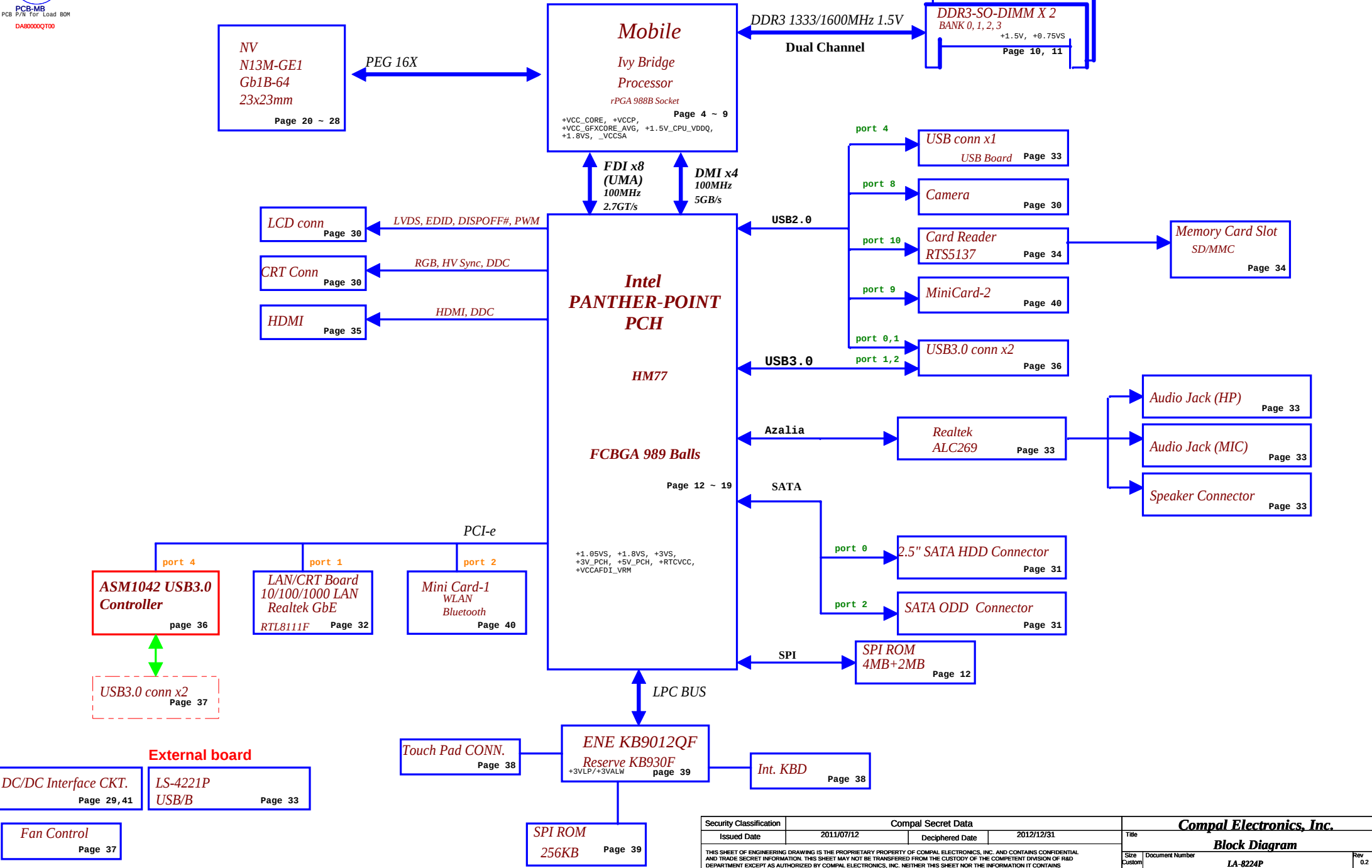
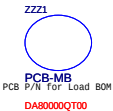
QCL40 MB Schematic Document

LA-8224P

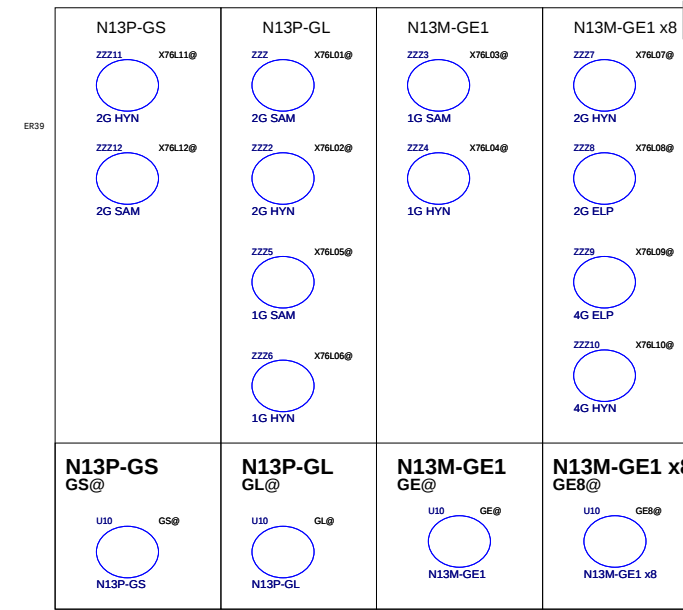
Rev: 0.2

2011.09.28

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X76@: VRAMX16X8 VRAMX16X4 VRAMX8X8



DIS@: VGA componet
GE8@: N13M-GE1_GB1b

9012@: EC(ENE 9012 chip)
930@: EC(ENE 930 chip)
XDP@: Intel debug port

IU3@: USB3.0 by PCH
USB30@:USB3.0 controller IC

AI@: AI Charger
NAI@: Non AI Charger

SMBUS Control Table							
	SOURCE	MINI1	BATT	PCH	EC	SODIMM	DGPU
EC_SMB_CK1 EC_SMB_DA1	KB930	X	V	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	KB930	X	X	V	X	X	V
PCH_SMBCLK PCH_SMBDATA	PCH	V	X	X	X	V	X
PCH_SMLCLK PCH_SMLDATA	PCH	X	X	X	V	X	V

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	10/100/1G LAN	CLKOUTFLEX0	CLK_SD_48M
	CLKOUT_PCIE1	MINI CARD WLAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	None	CLKOUTFLEX2	None
	CLKOUT_PCIE3	USB3.0 controller	CLKOUTFLEX3	None
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

Symbol Note :



: means Digital Ground



: means Analog Ground

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CLK OUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC
PCI2	None
PCI3	LPC Debug Port
PCI4	None

USB3 PORT	DESTINATION
1	USB2.0+3.0
2	USB2.0+3.0
3	None
4	None

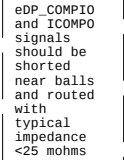
Voltage Rails

Power Plane	Description	S1	S3	Deep S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A	N/A
B+	AC or battery power rail for power circuit	N/A	N/A	N/A	N/A
+3VLP	3.3V power rail for 510N power management	ON	ON	ON	ON
+3VALW	3.3V always on power rail	ON	ON	ON	AC/ON; DC/OFF
+LAN_IO	3.3V power rail for ethernet	ON	ON	OFF	OFF
+3VS_WLAN	3.3V power rail for WLAN/BT Combo	ON	OFF	OFF	OFF
+3V_PCH	3.3V power rail for PCH suspend well plane	ON	ON	OFF	OFF
+3VS	3.3V power rail for DDR SPI,PCH,HDD,Audio,Card Reader	ON	OFF	OFF	OFF
+3VSG	3.3V power rail for VGA	ON	OFF	OFF	OFF
+LCDVDD	3.3V power rail for LCD	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON	AC/ON; DC/OFF
+5V_PCH	5V power rail for PCH suspend well plane	ON	ON	OFF	OFF
+5VS	5V power rail for HDD,AUDIO,FAN,Touch PAD	ON	OFF	OFF	OFF
+5VS_ODD	5V power rail for SATA ODD	ON	OFF	OFF	OFF
+1.8VS	1.8V power rail for CPU,PCH	ON	OFF	OFF	OFF
+1.05VS	1.05V power rail for PCH	ON	OFF	OFF	OFF
+VCCP	1.05V power rail for CPU VCCIO,PCH	ON	OFF	OFF	OFF
+1.05VSG	1.05V power rail for N13P	ON	OFF	OFF	OFF
+1.5V	1.5V power rail for DDR3 system memory	ON	ON	ON	OFF
+1.5V_CPU_VDDQ	1.5V power rail CPU VDDQ	ON	OFF	OFF	OFF
+1.5VSG	1.5V power rail for N13P,VRAM	ON	OFF	OFF	OFF
+1.5VS	1.5V power rail for PCH,WLAN/BT combo	ON	OFF	OFF	OFF
+0.75VS	0.75V power rail for DDR VREF	ON	OFF	OFF	OFF
+VCCSA	VCCSA for CPU system agent	ON	OFF	OFF	OFF
+VCC_CORE	CORE Voltage for CPU	ON	OFF	OFF	OFF
+VCC_GFXCORE_AXG	1.5V power rail for N13P,VRAM	ON	OFF	OFF	OFF
+VGA_CORE	CORE Voltage for N13P Graphics ON OFF OFF	ON	OFF	OFF	OFF

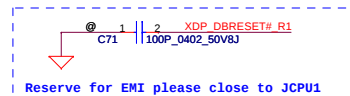
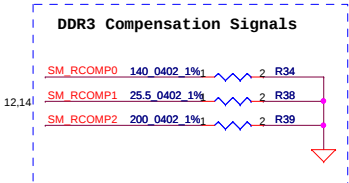
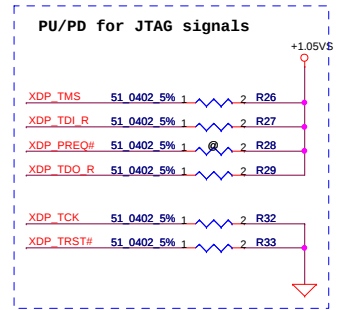
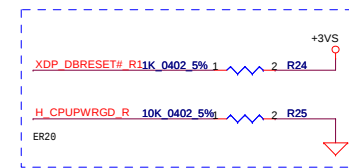
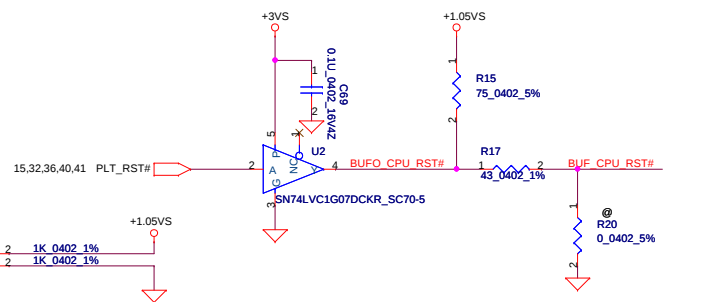
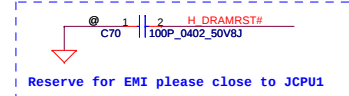
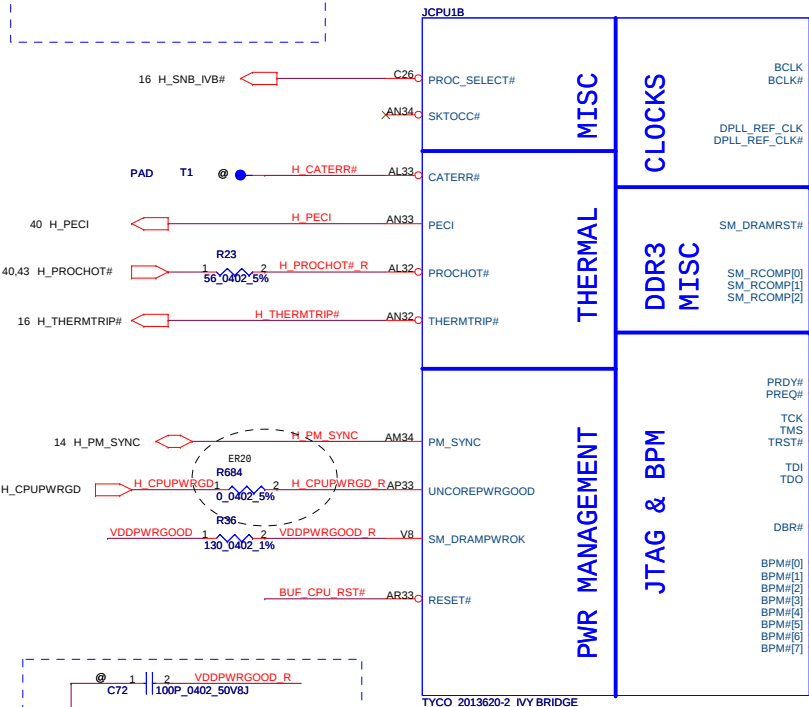
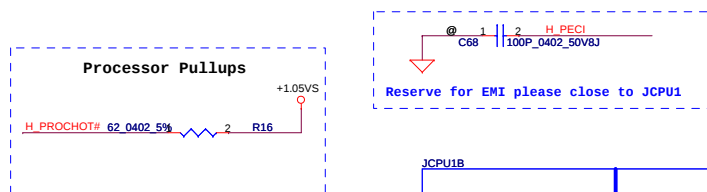
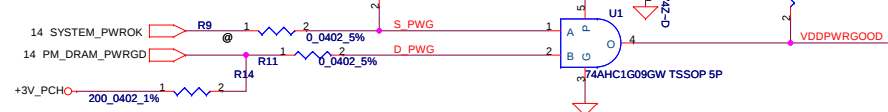
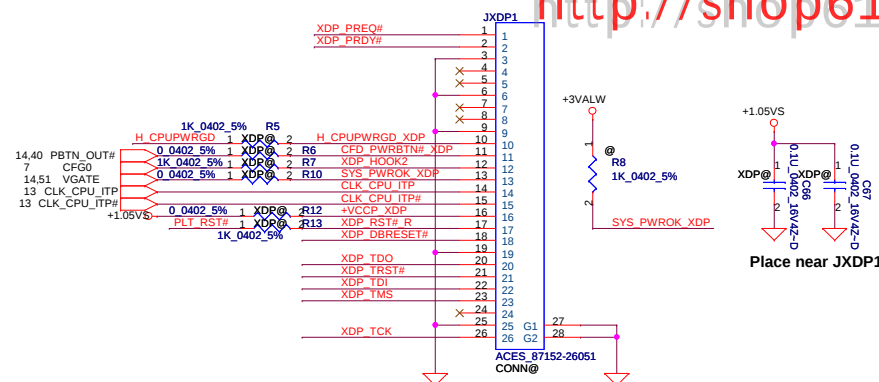
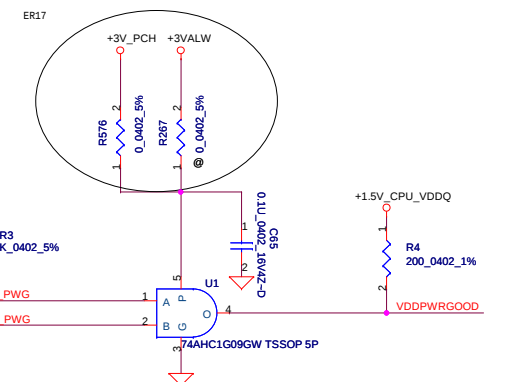
SATA	DESTINATION
SATA0	HDD
SATA1	None
SATA2	ODD
SATA3	None
SATA4	None
SATA5	None

USB2 PORT	DESTINATION
0	USB2.0+3.0
1	USB2.0+3.0
2	None
3	None
4	JMINI1 (WLAN) Bluetooth
5	None
6	None
7	None
8	CAMERA
9	USB2
10	Card Reader
11	None
12	None
13	None

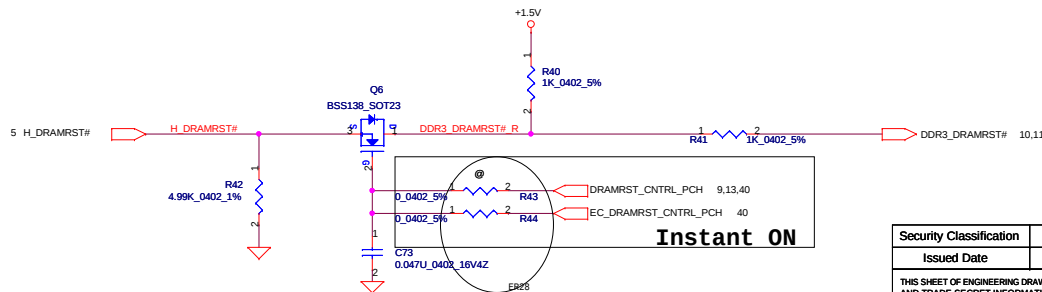
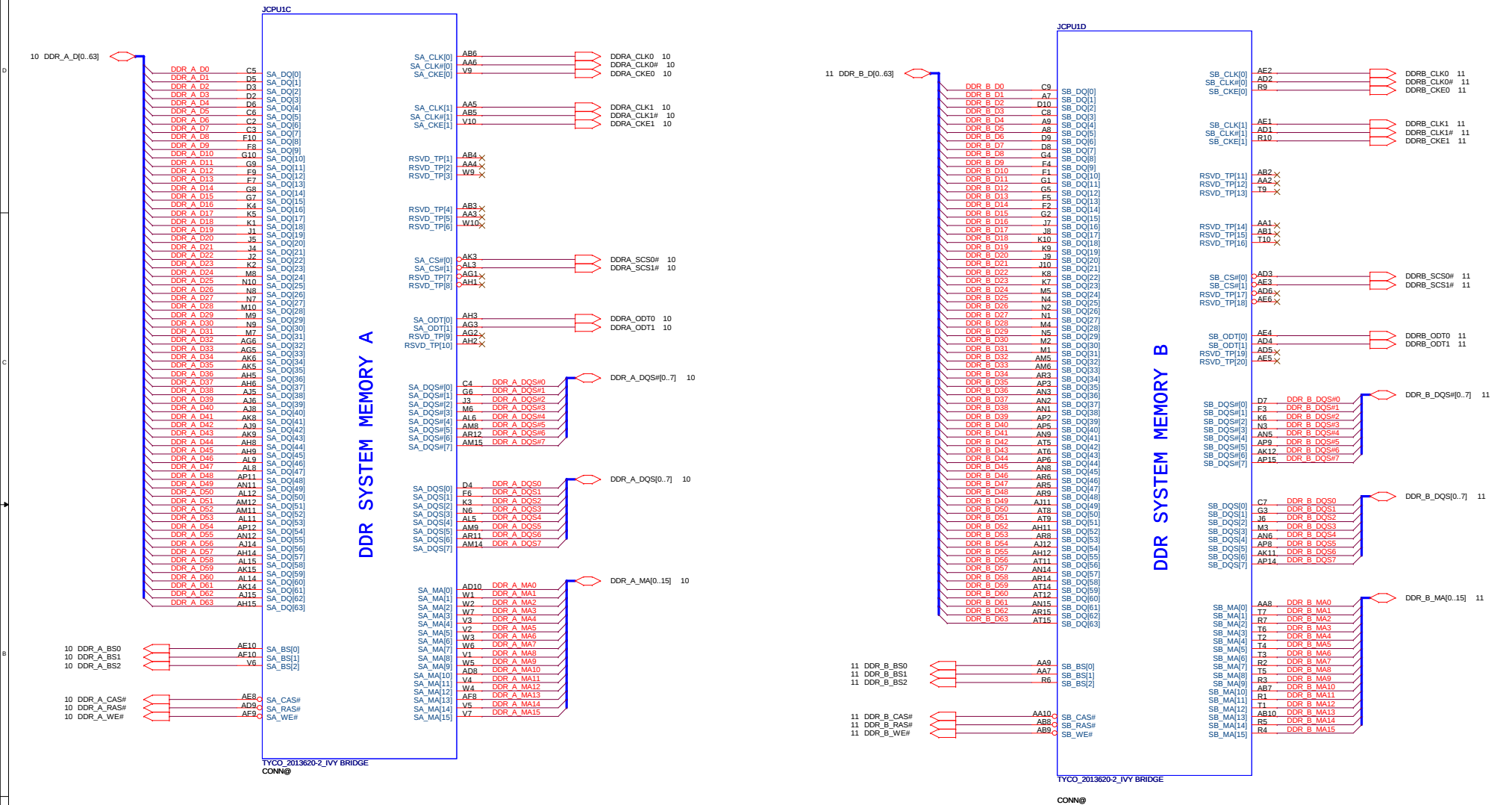
PCI EXPRESS	DESTINATION
Lane 1	10/100/1G LAN
Lane 2	MINI CARD WLAN
Lane 3	None
Lane 4	USB3.0 controller
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None



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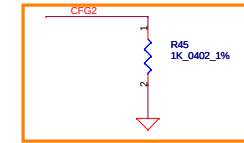
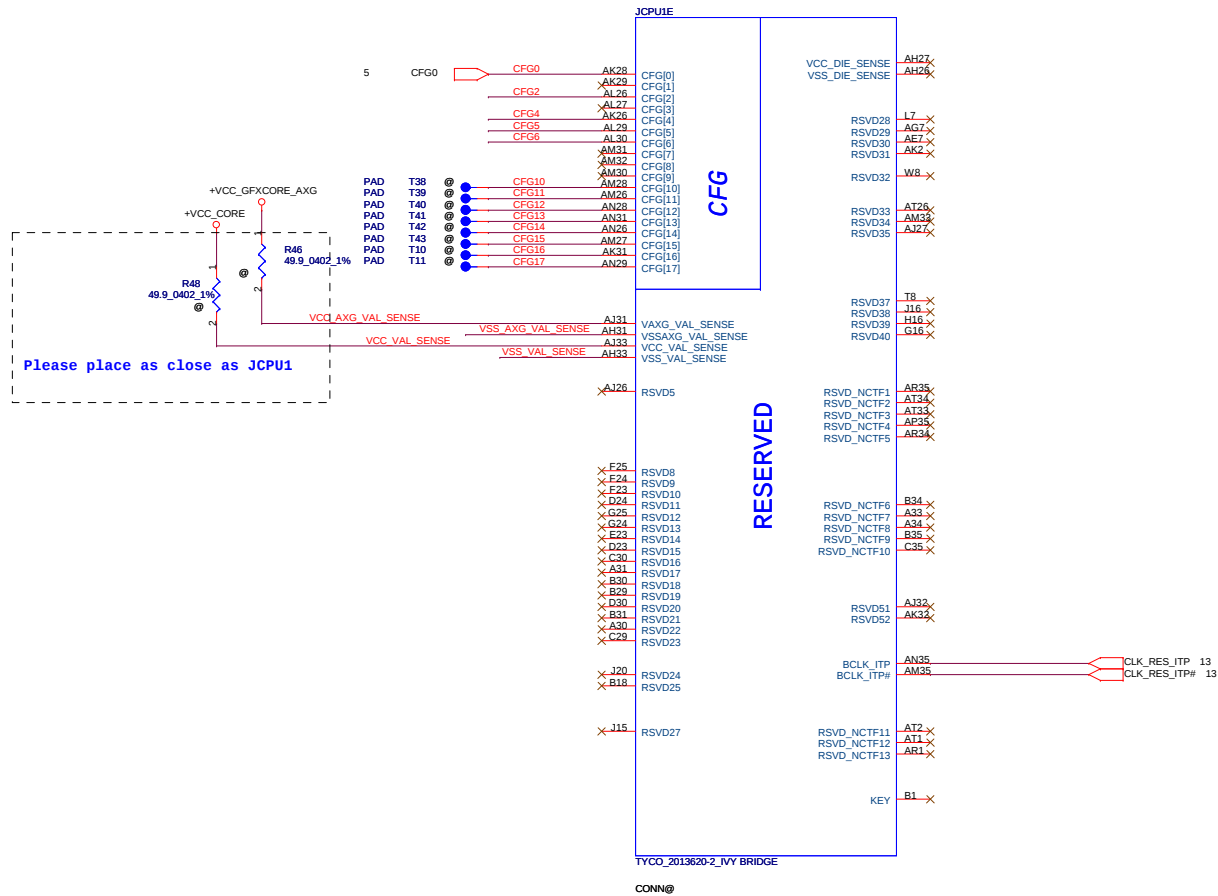


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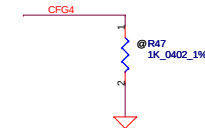
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CFG Straps for Processor



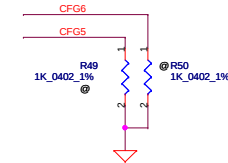
PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed
------	--



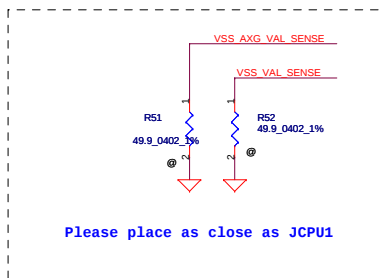
Display Port Presence Strap

CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port
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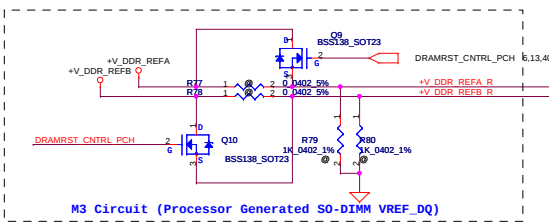
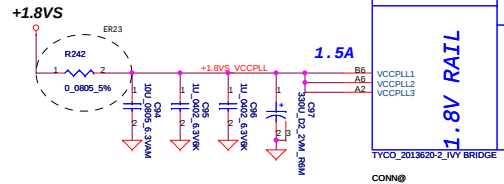
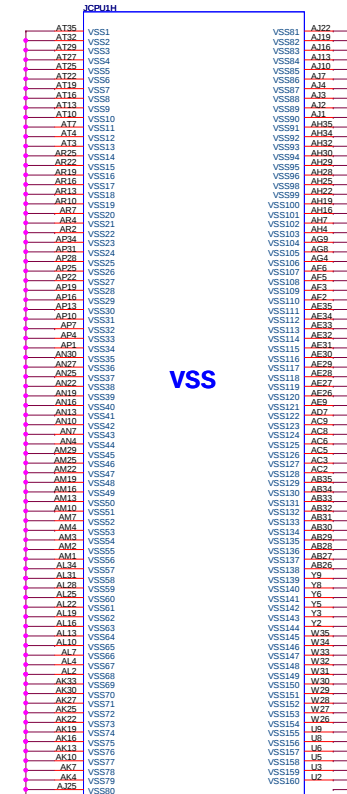
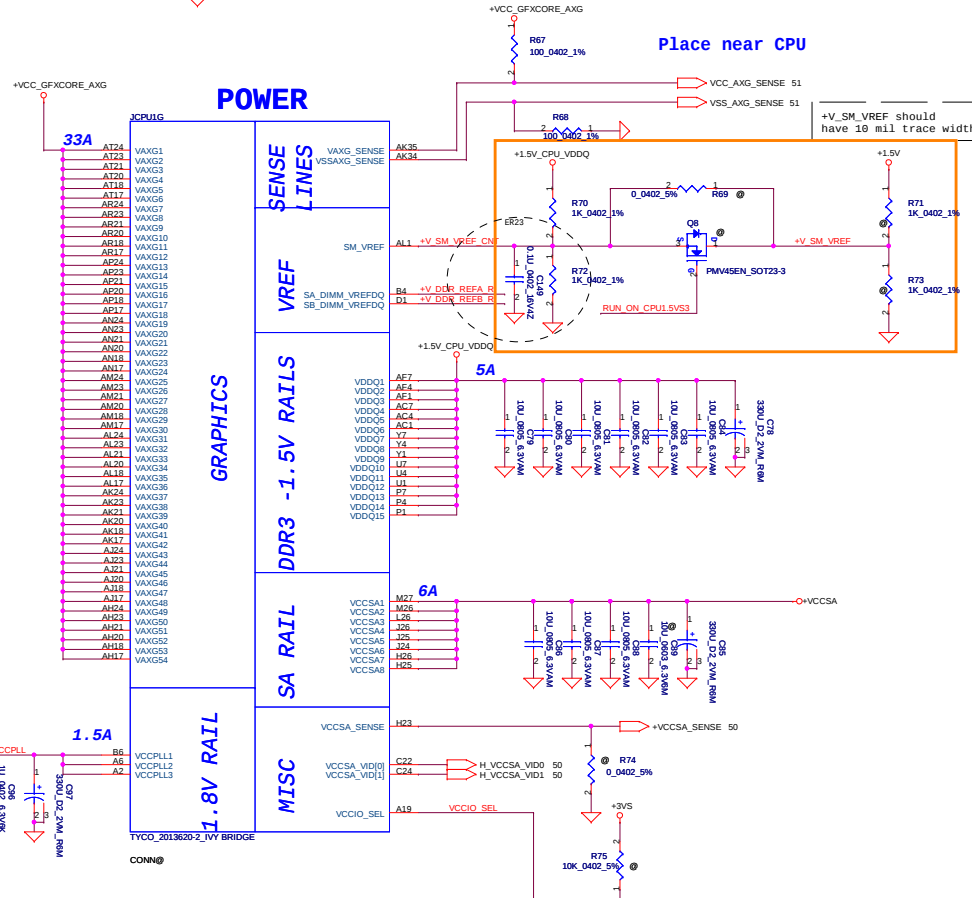
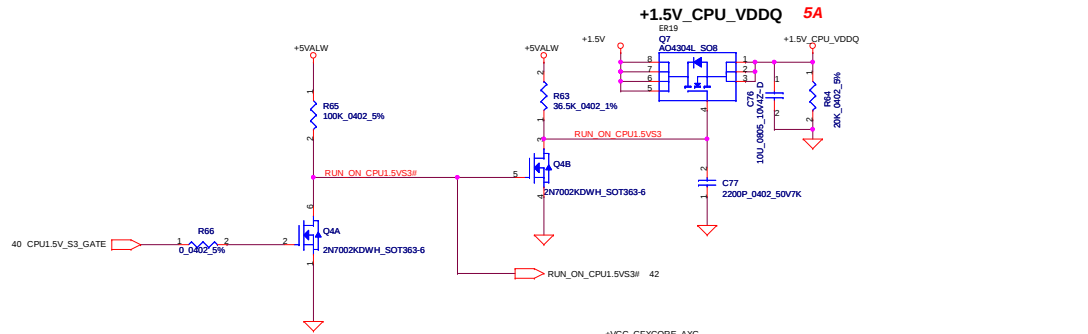
PCIE Port Bifurcation Straps

CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
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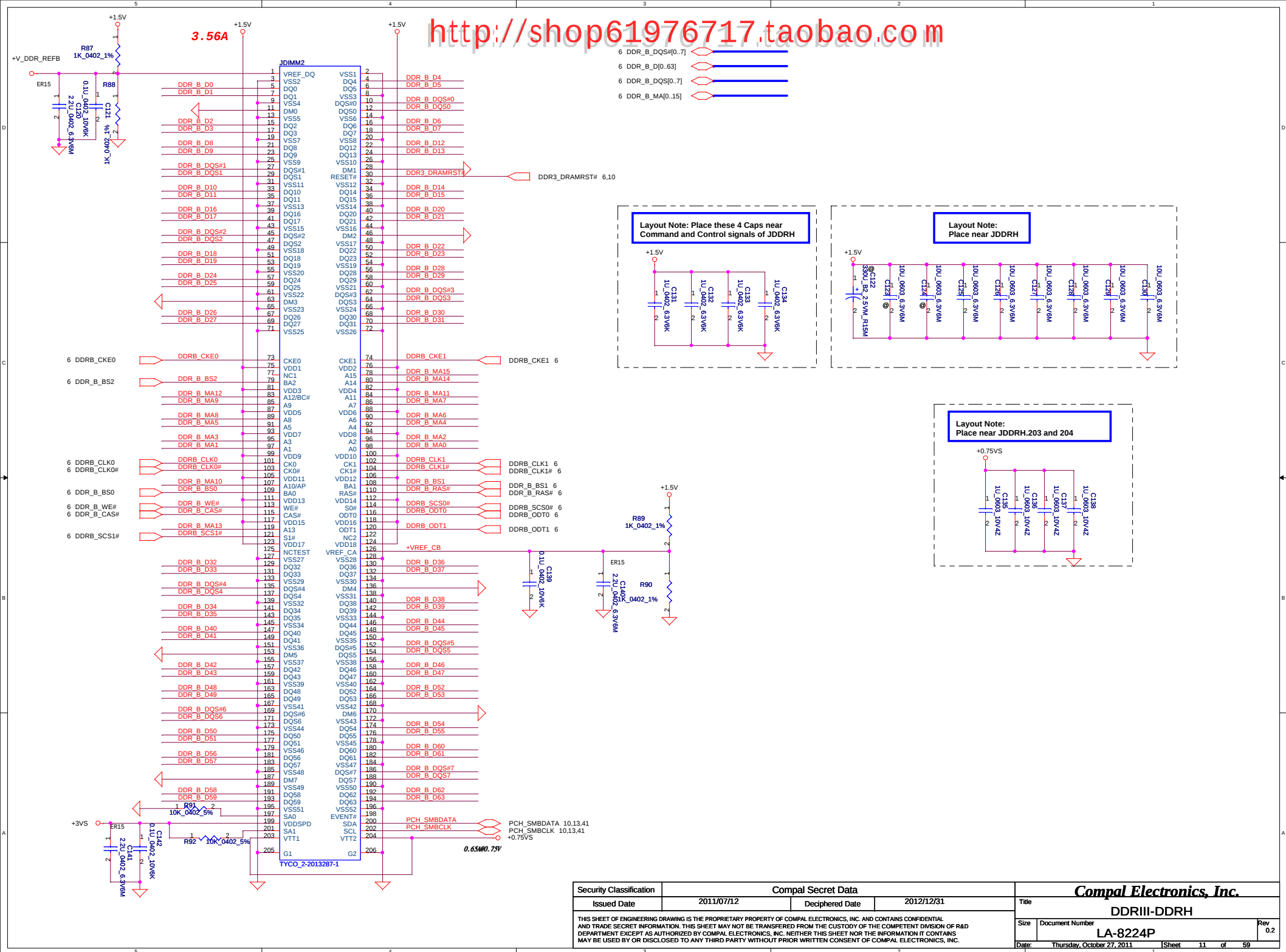


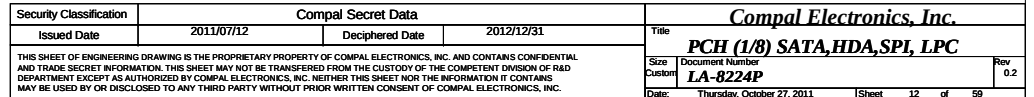


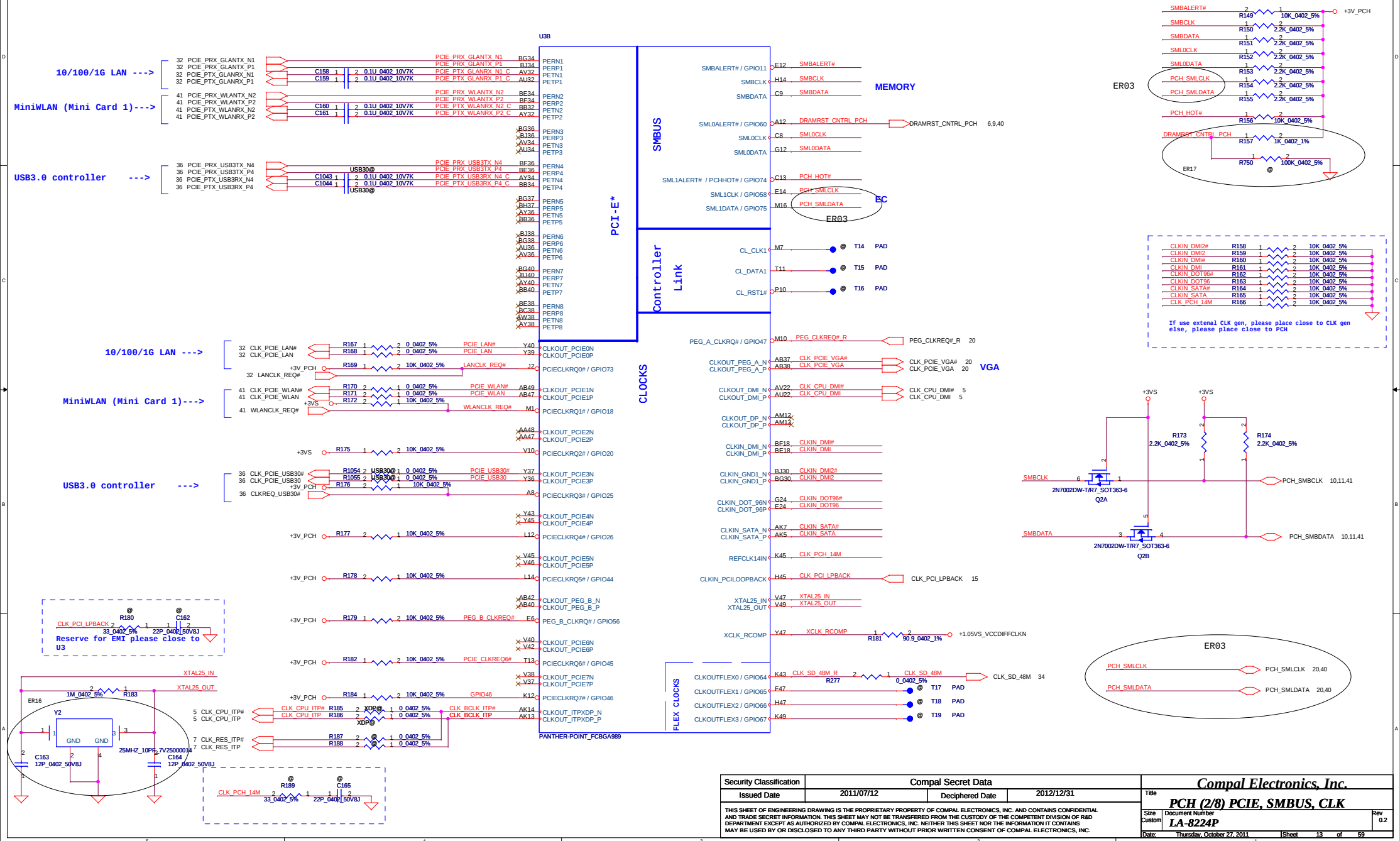
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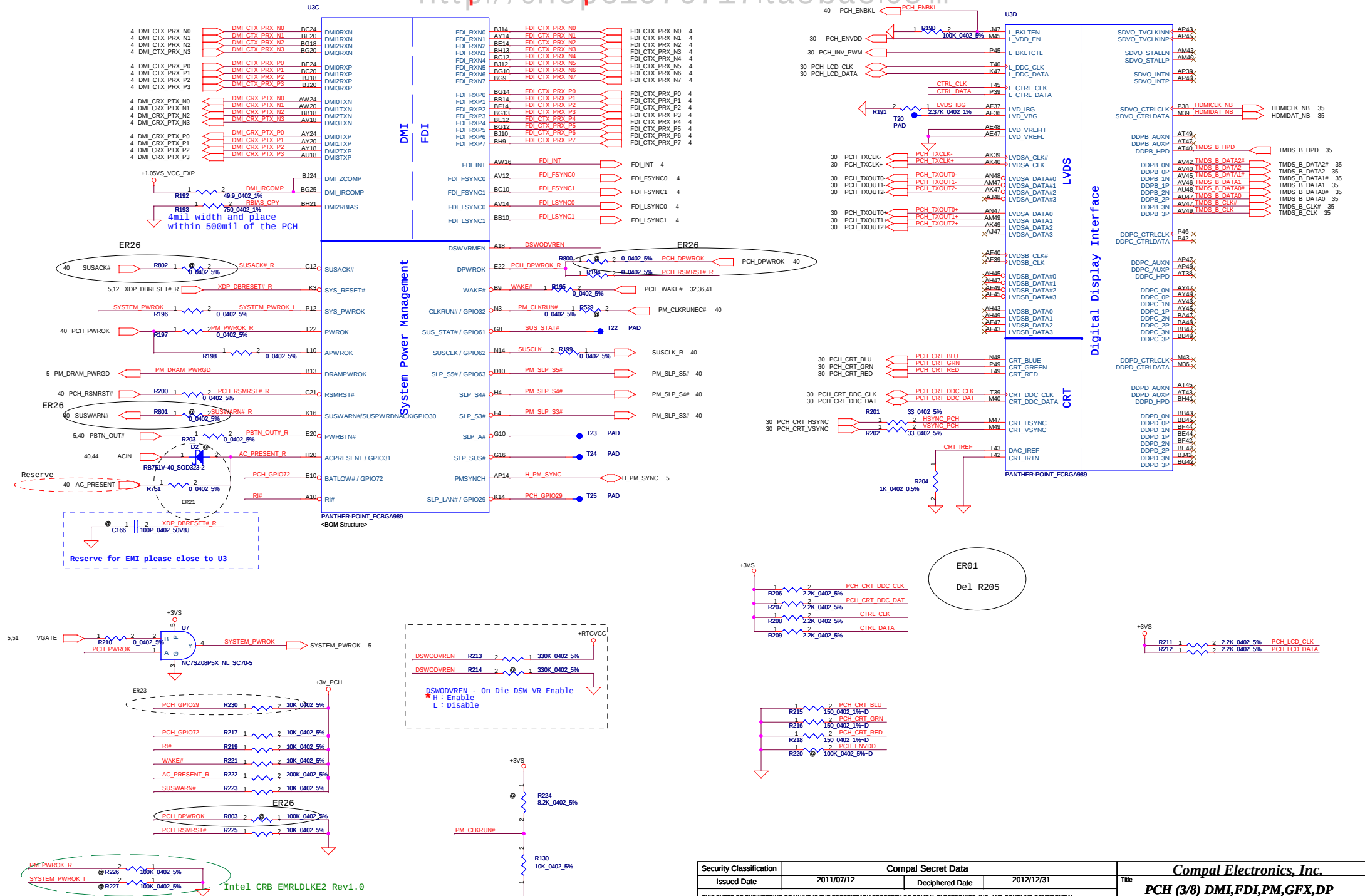


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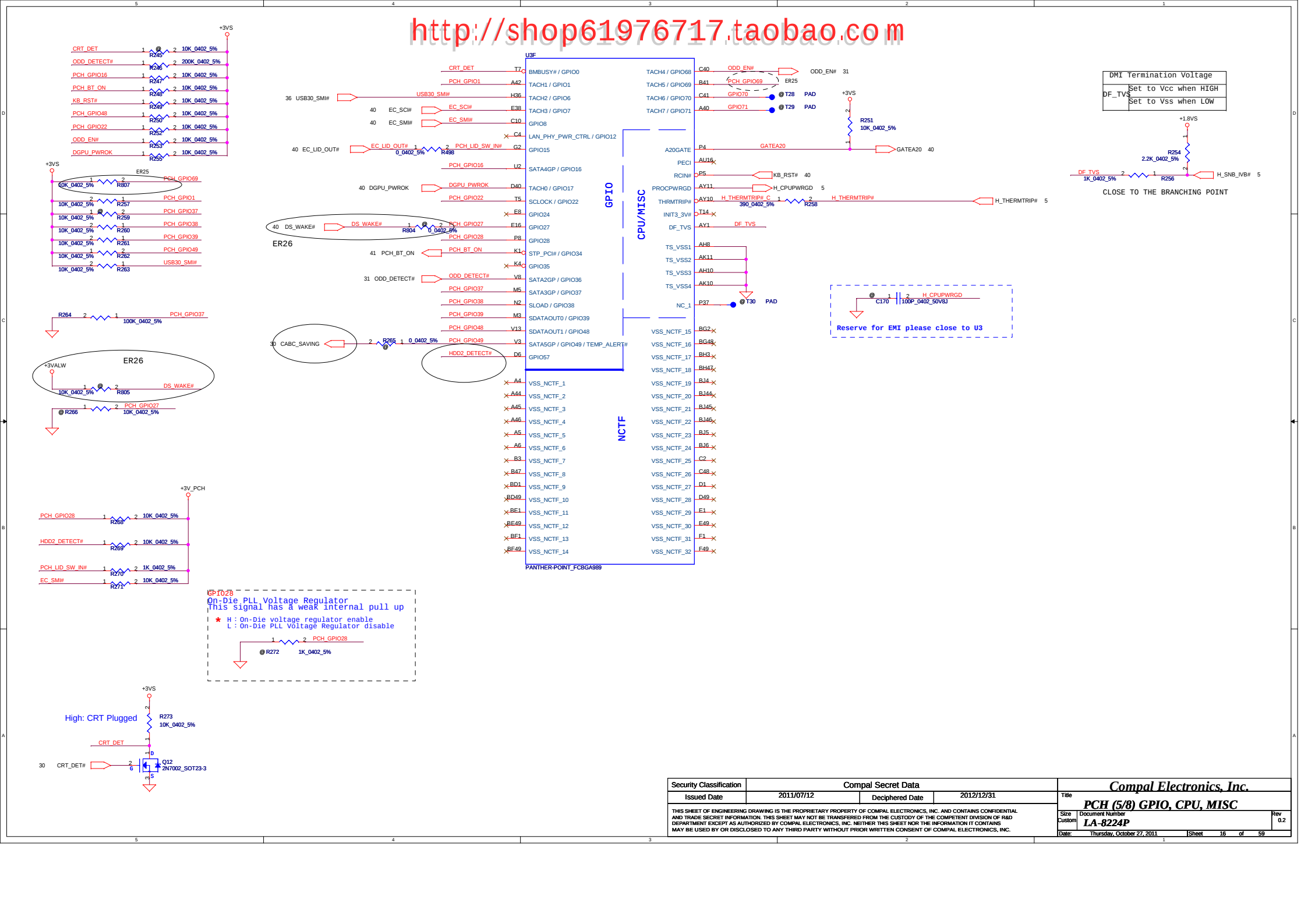








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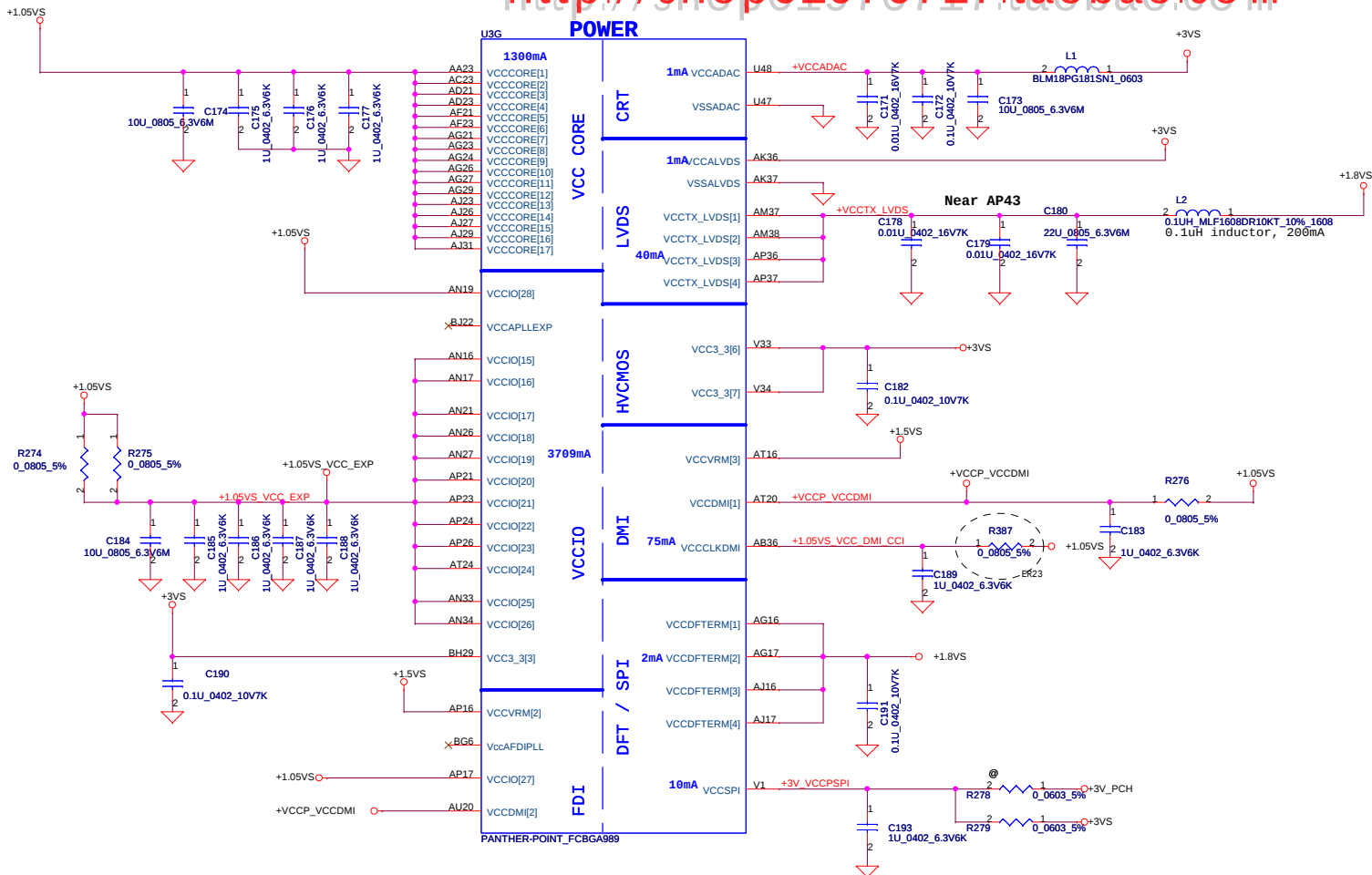
PCH (5/8) GPIO, CPU, MISC

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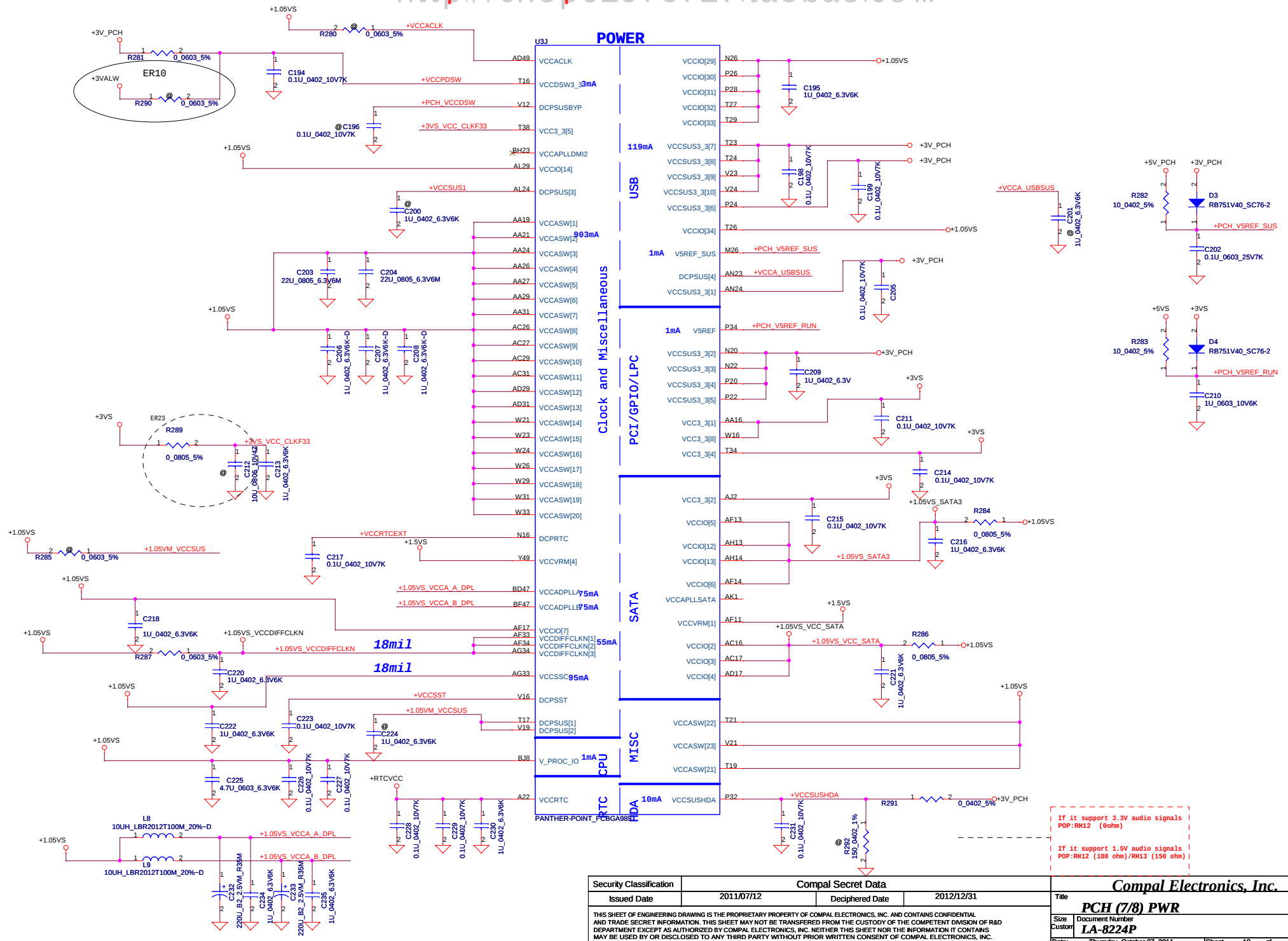
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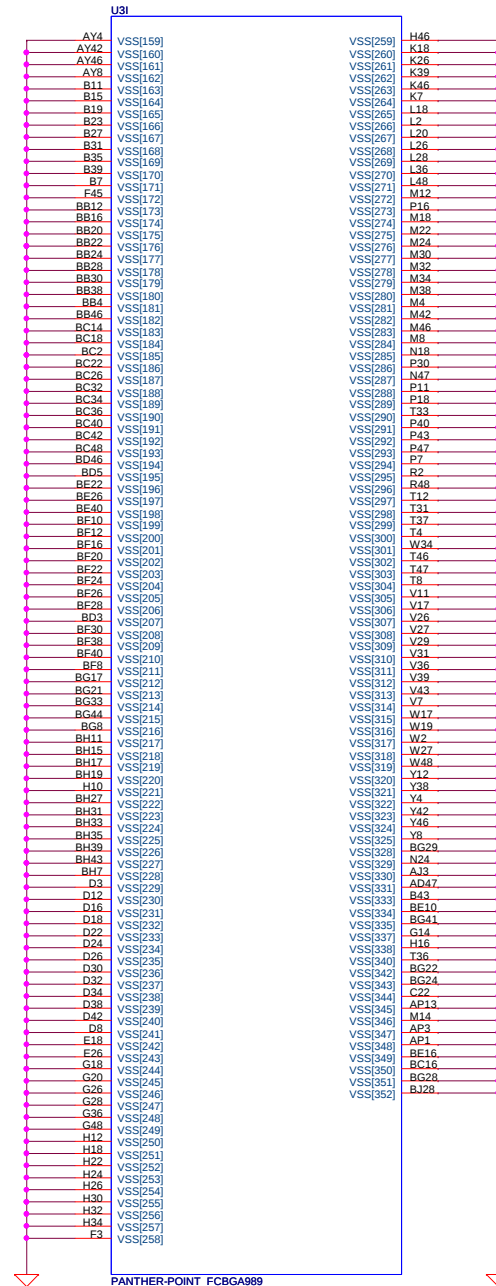
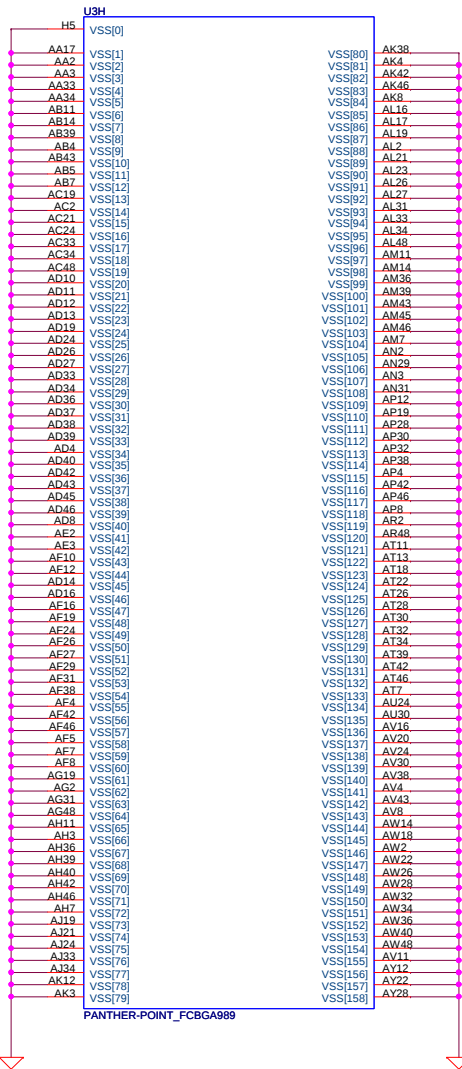


PCH Power Rail Table
Refer to CPU EDS R1.5

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.001
VccADPLLA	1.05	0.075
VccADPLLb	1.05	0.075
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	3.709
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTerm	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04



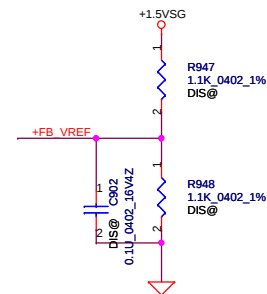
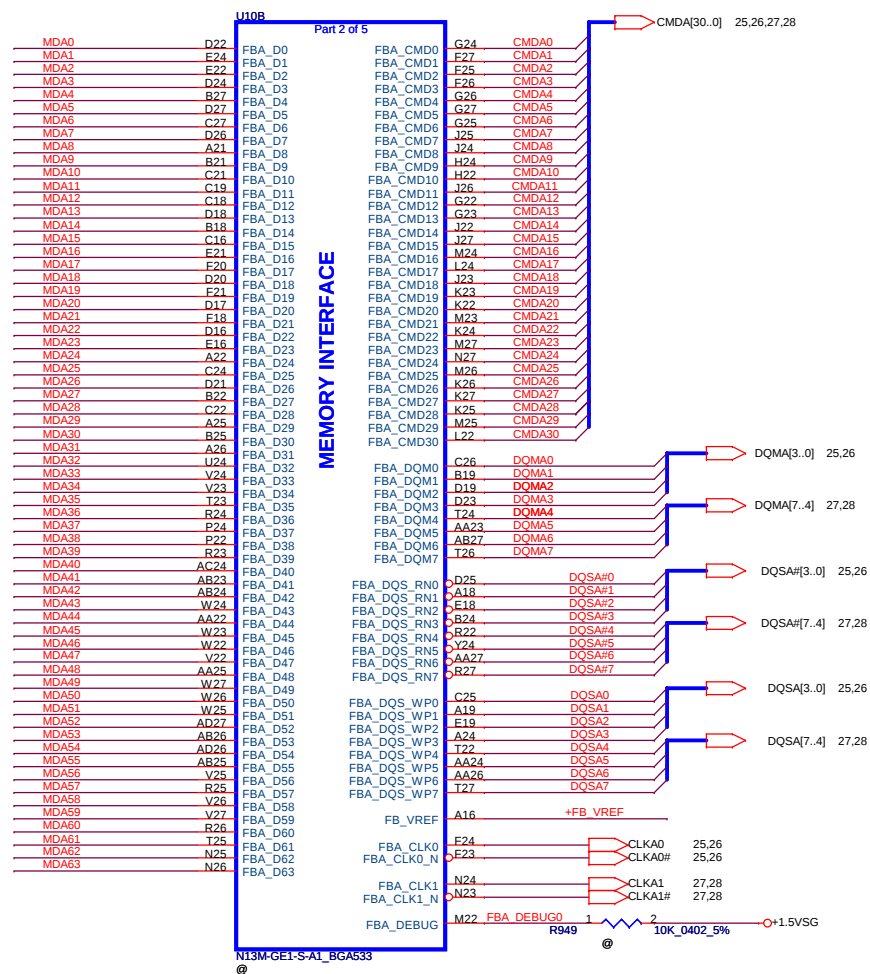
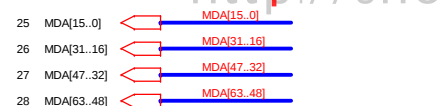
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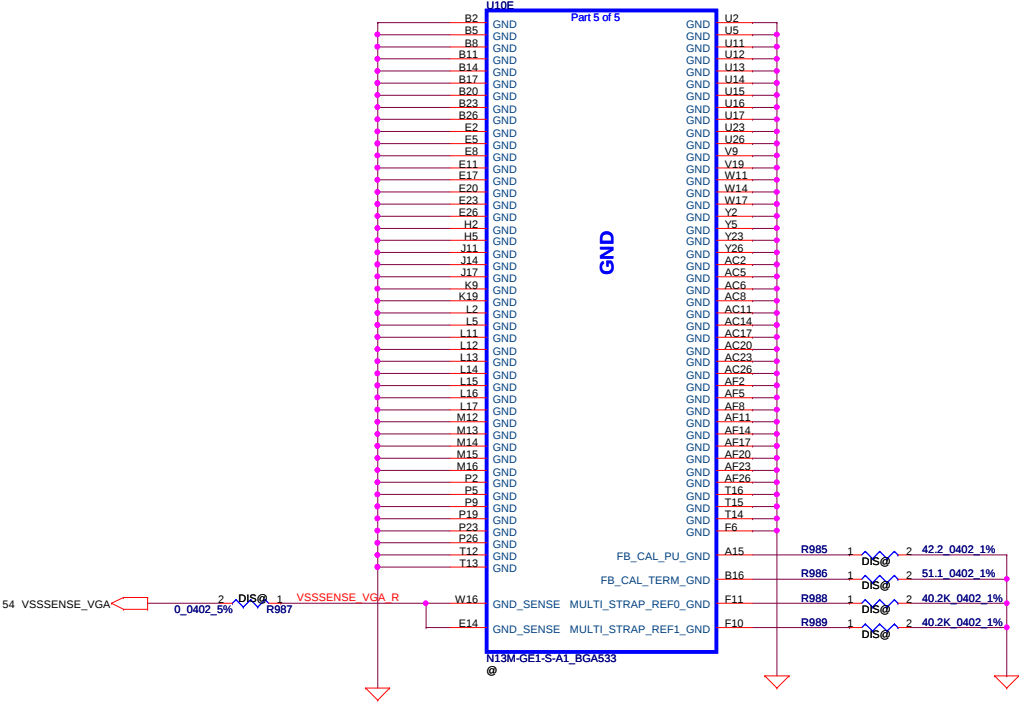
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VRAM Interface

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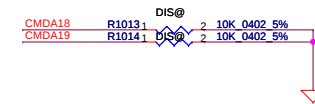
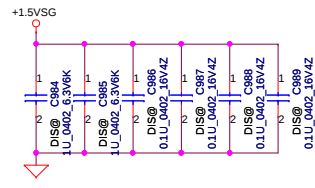
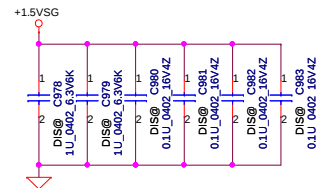
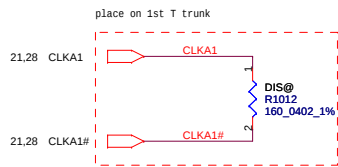
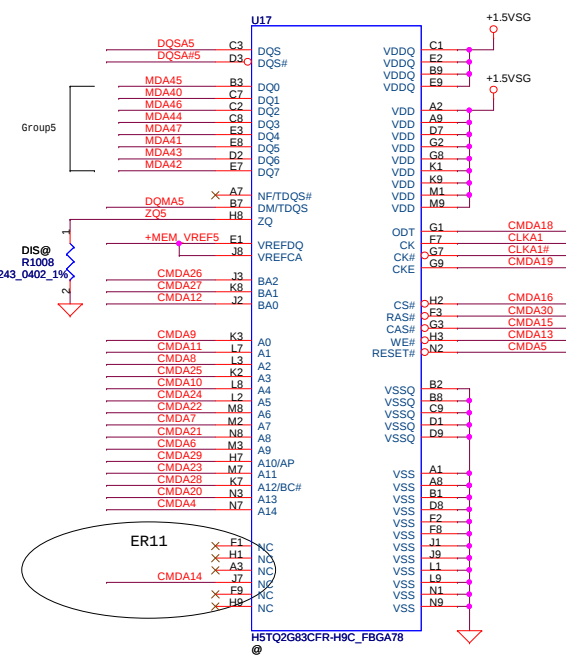
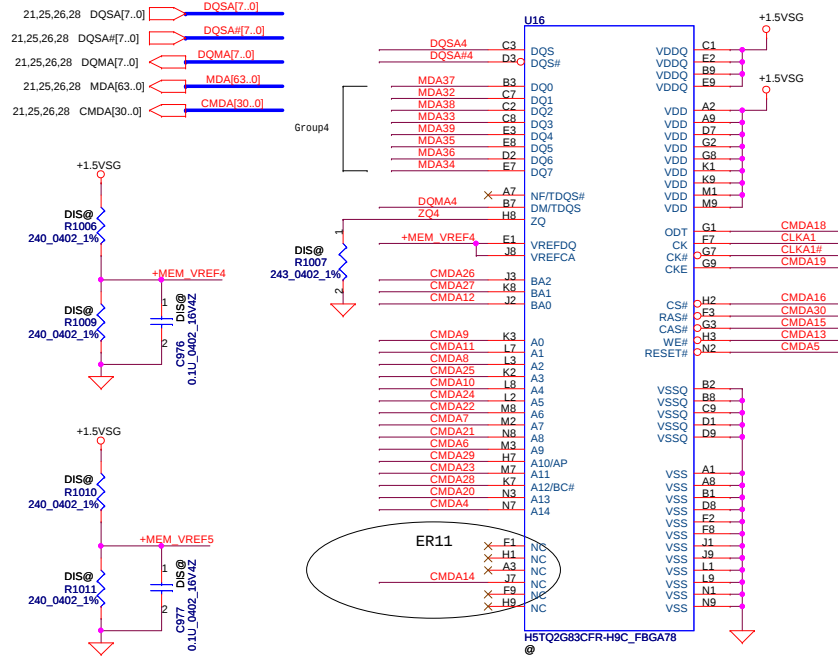


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Size	Document Number	Rev		0.2		
Custom	LA-8224P	Date		Thursday, October 27, 2011 Sheet 21 of 59		



VRAM DDR3 chips

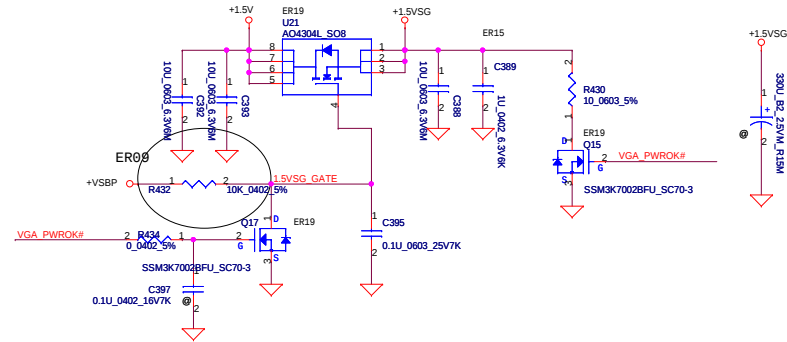
256Mx8 DDR3 *8==>2GB



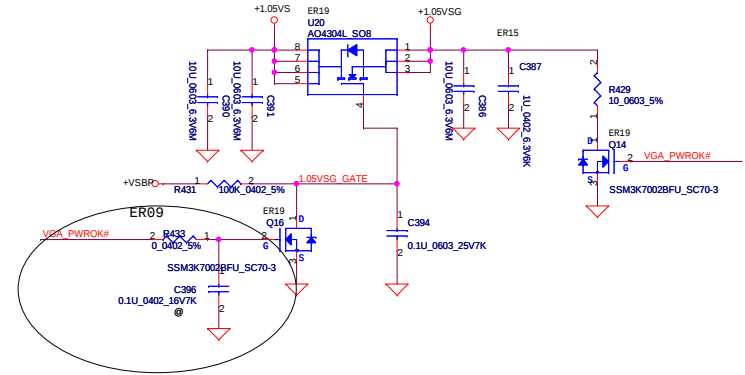
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CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

Hynix : SA000054600 (S IC D3 256MX8/1333 H5TQ2G83CFR-H9C FBGA)
 Elpida : SAxxxxxxx (S IC D3 256MX8/1333 xxxxxxxxxxxxxxxx)

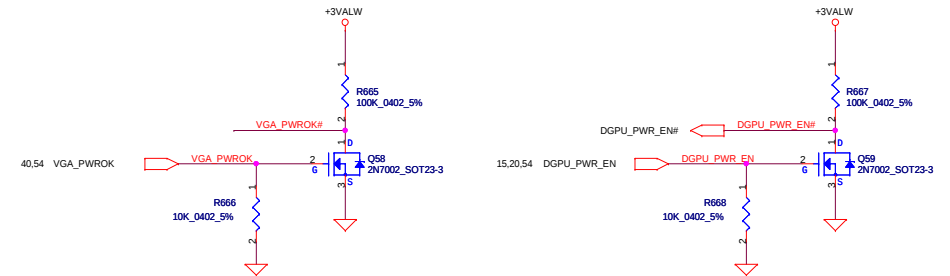
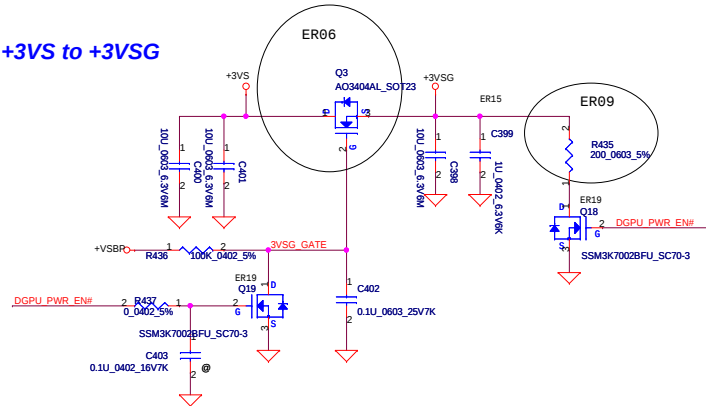
+1.5V to +1.5VSG



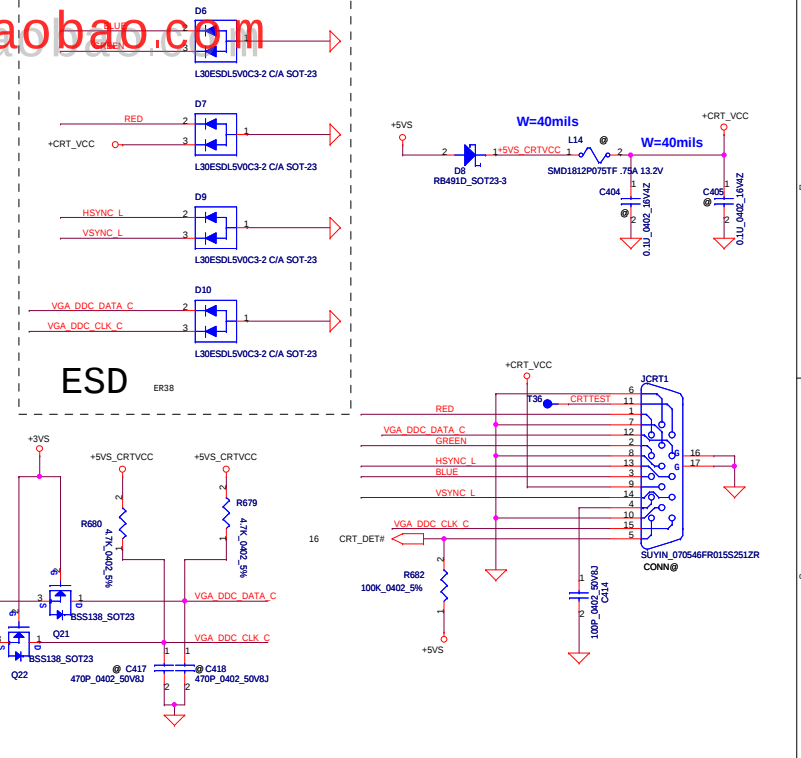
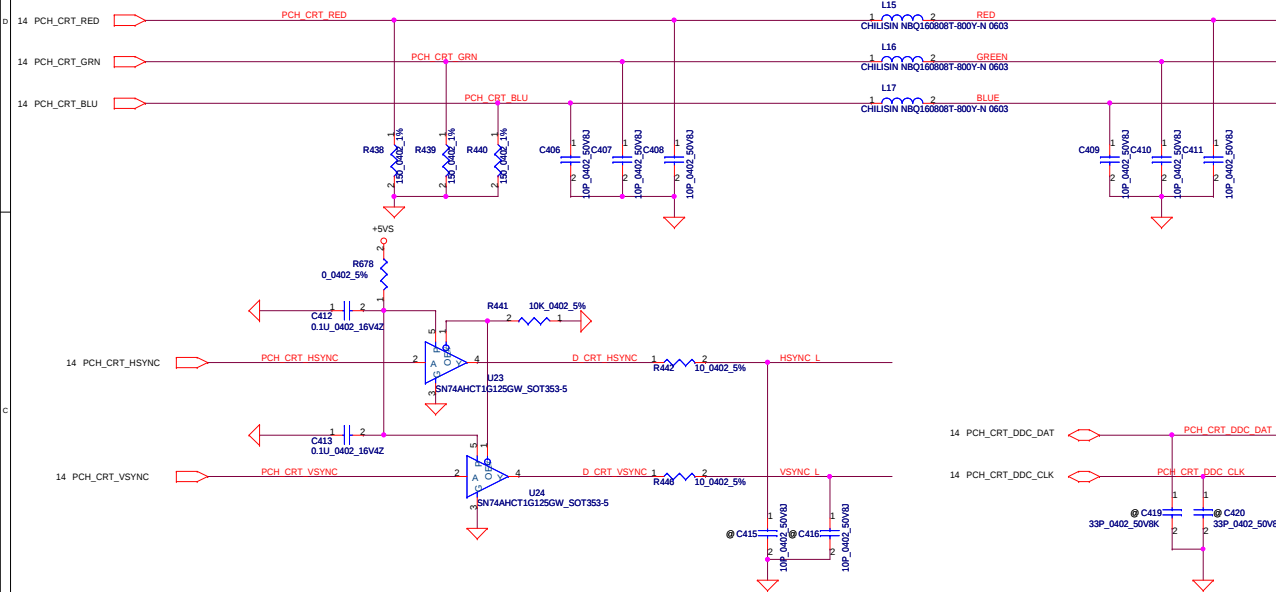
+VCCP to +1.05VSG



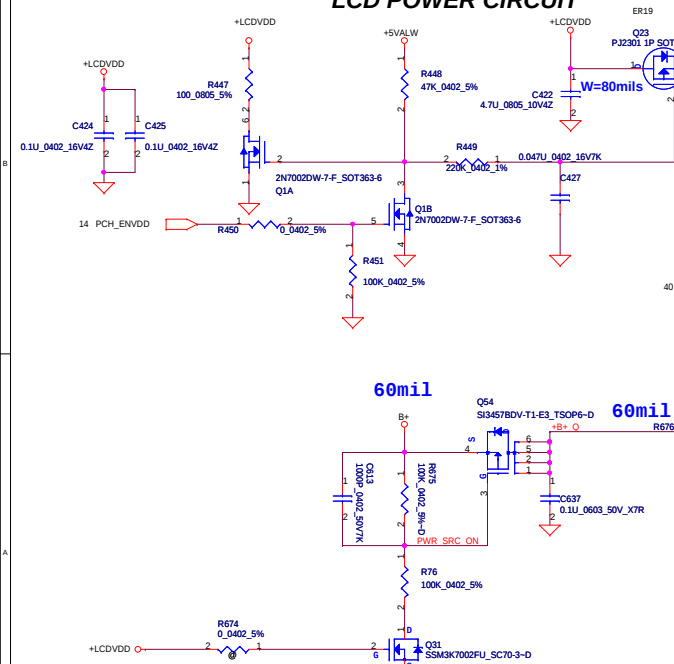
+3VS to +3VSG



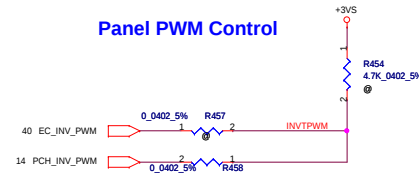
CRT



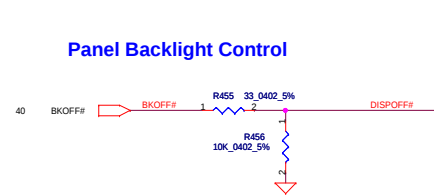
LCD POWER CIRCUIT



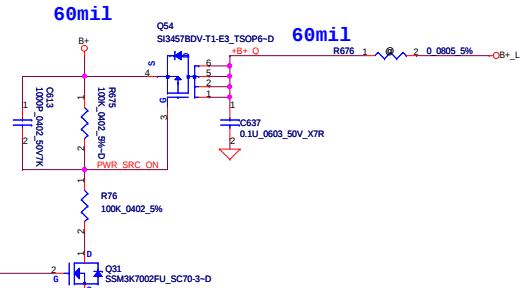
Panel PWM Control



Panel Backlight Control

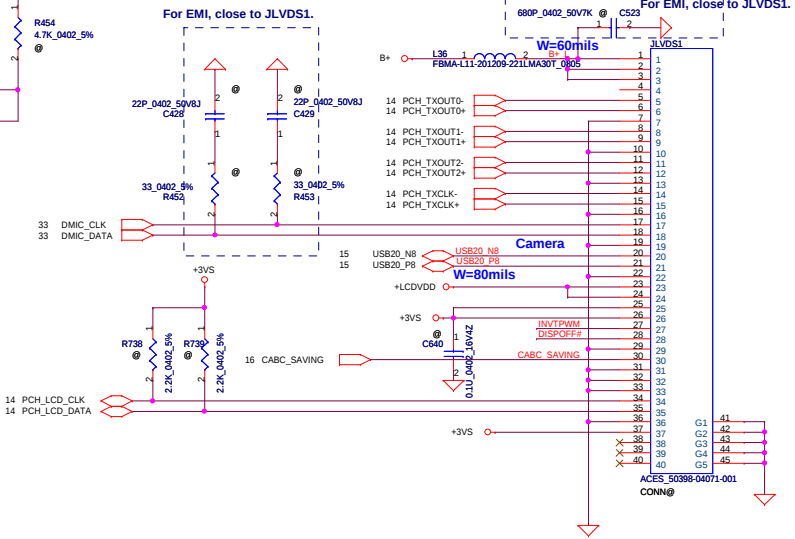


60mil



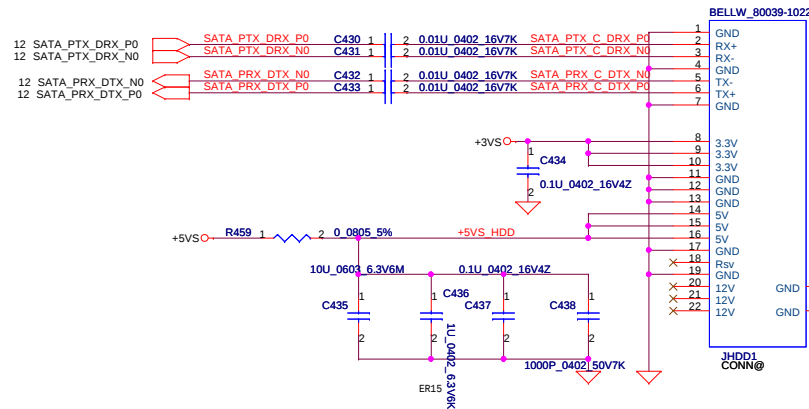
60mil

For EMI, close to JLVDS1.

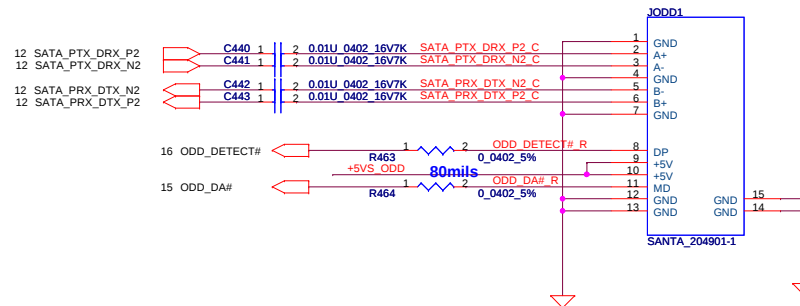


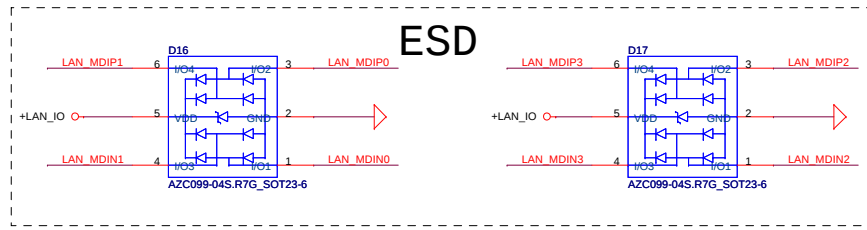
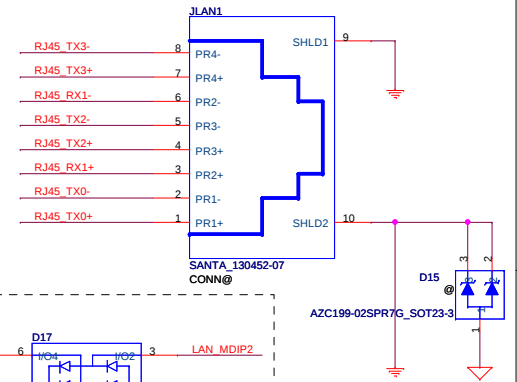
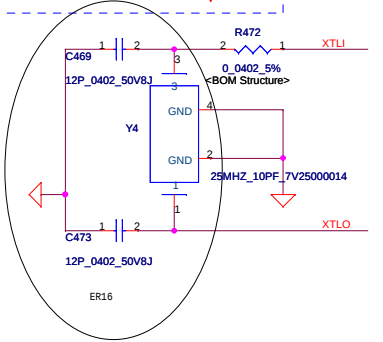
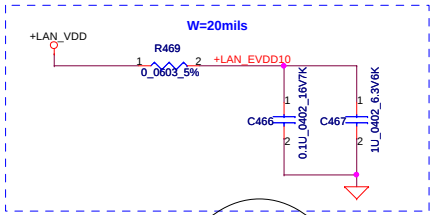
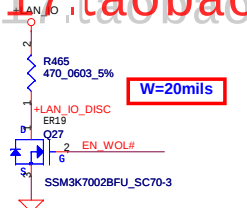
For EMI, close to JLVDS1.

SATA HDD Conn.

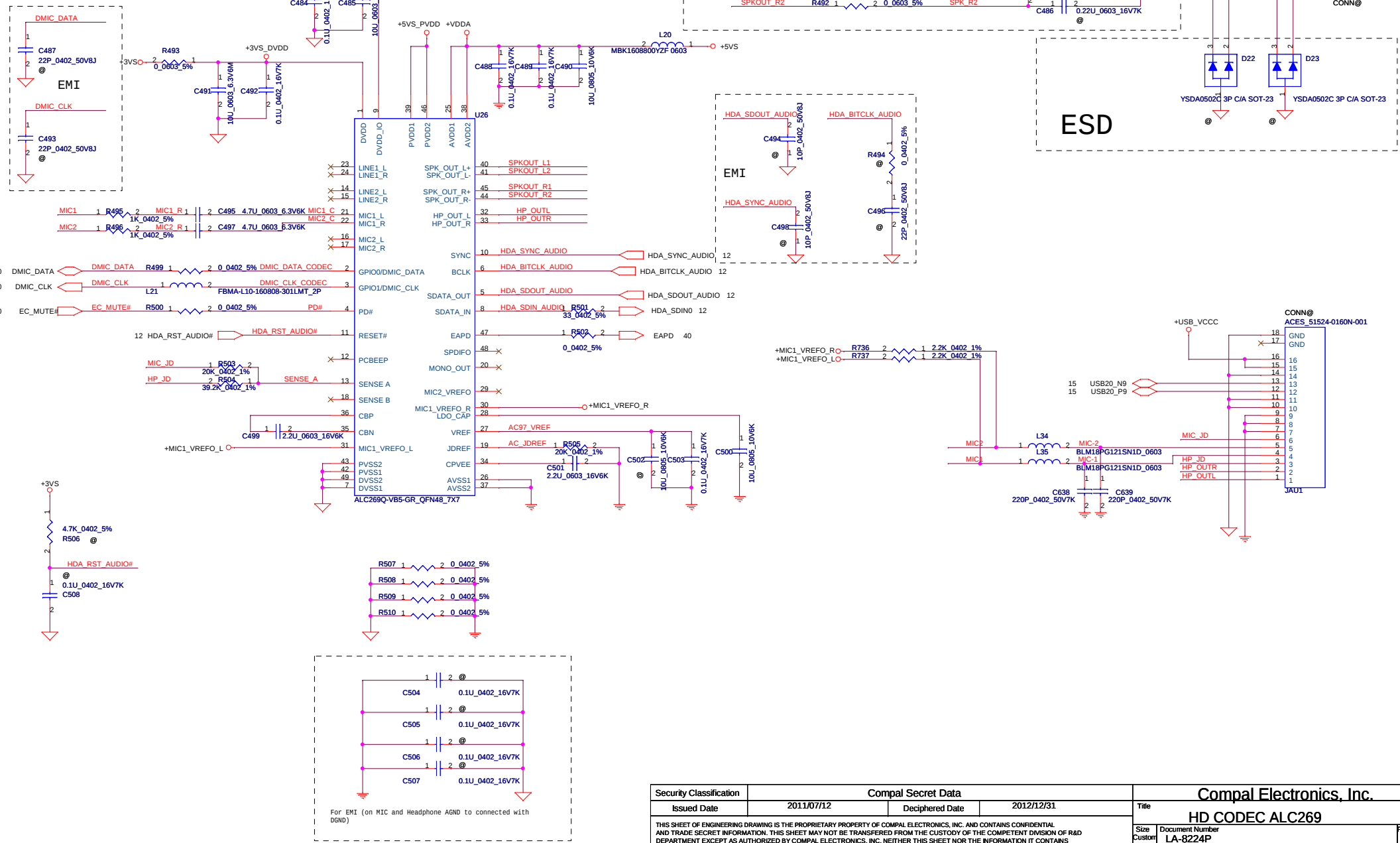


SATA ODD Conn.





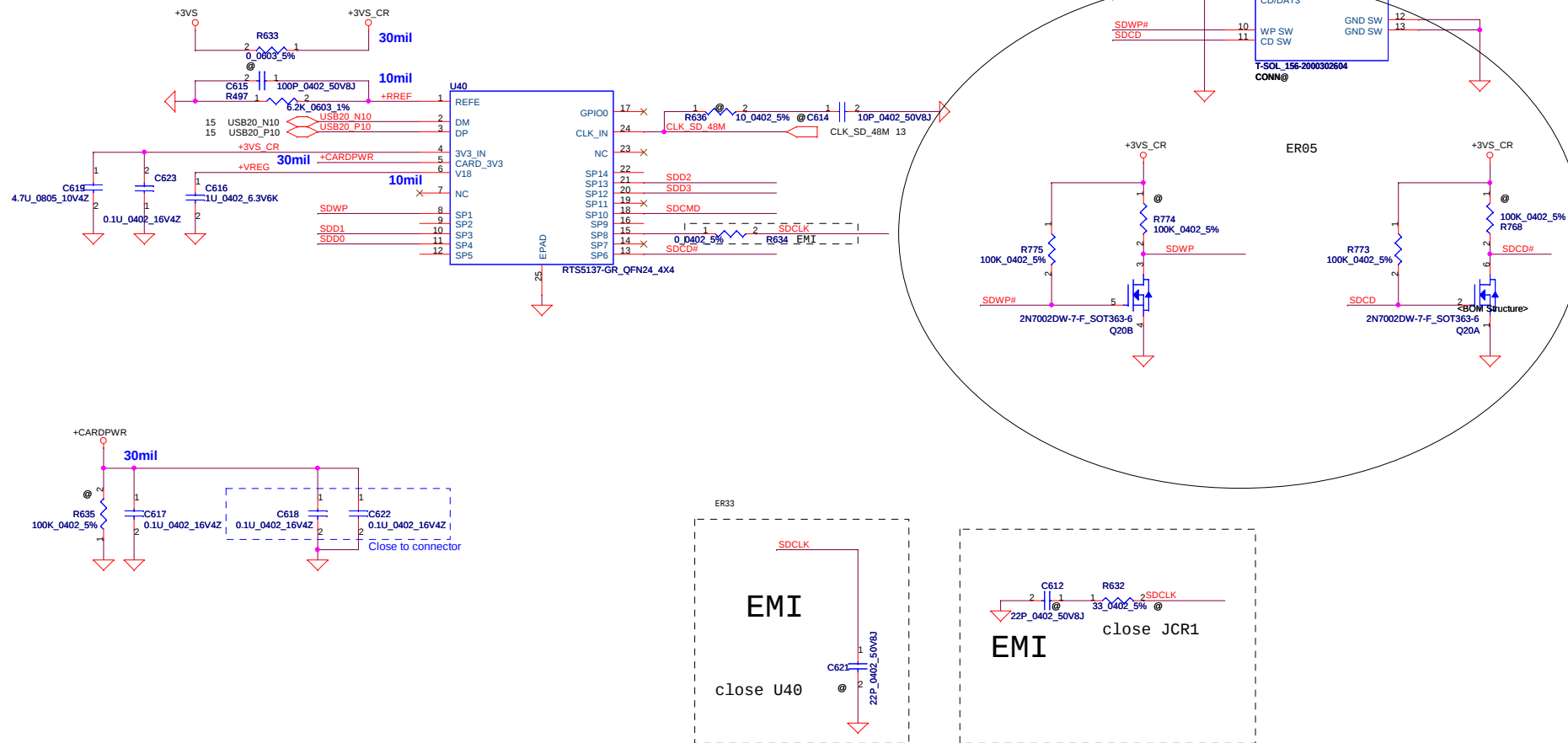
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				LA-8224P		0.2	
				Date:	Thursday, October 27, 2011	Sheet	32 of 59

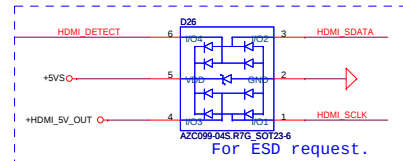
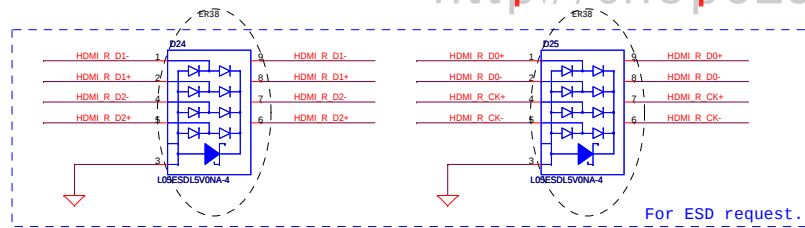


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Size		Document Number		LA-8224P		Rev		HD CODEC ALC269			
Date		Thursday, October 27, 2011		Sheet		33		of 59			

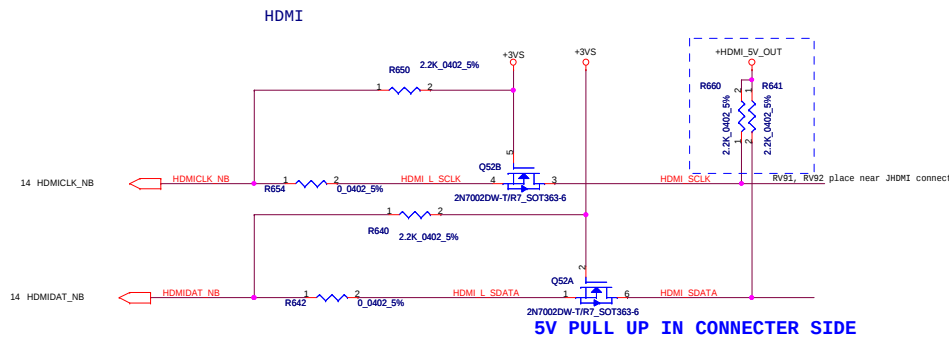
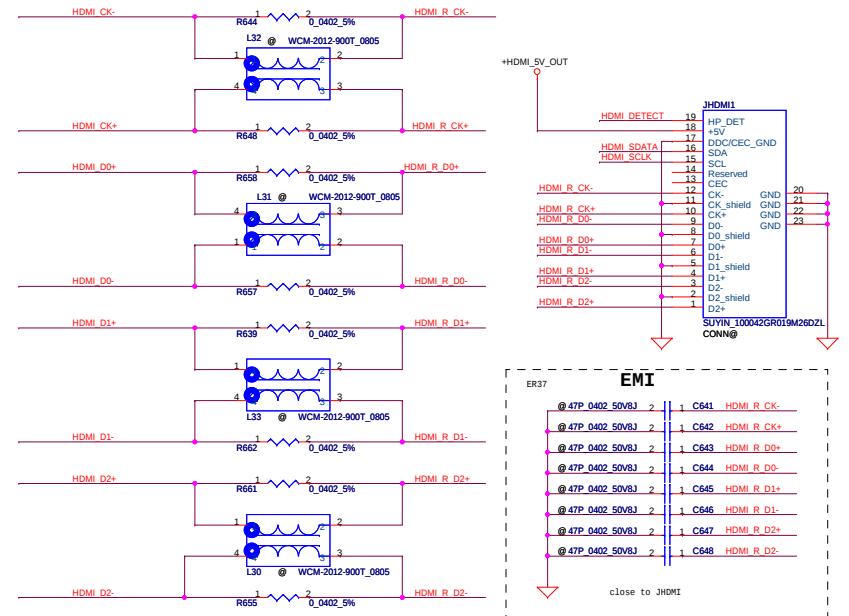
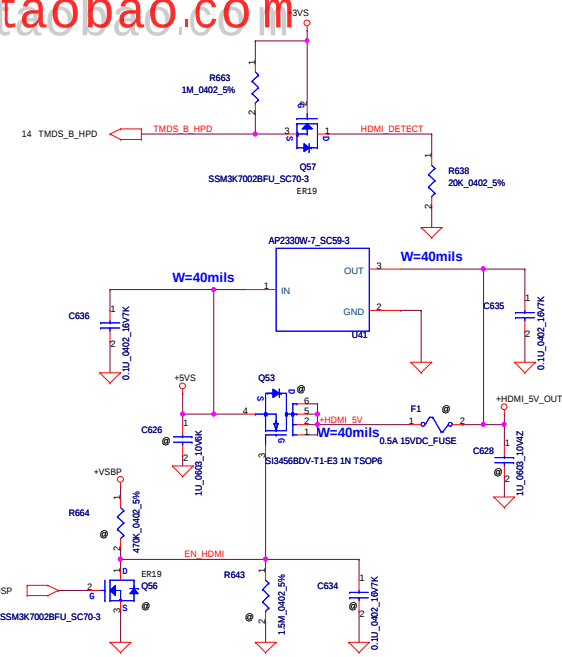
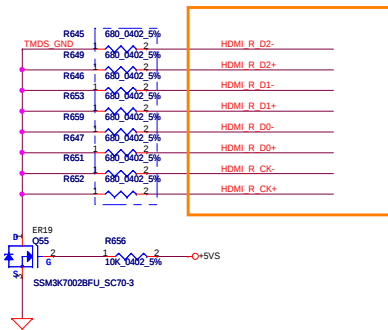
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Card Reader Connector

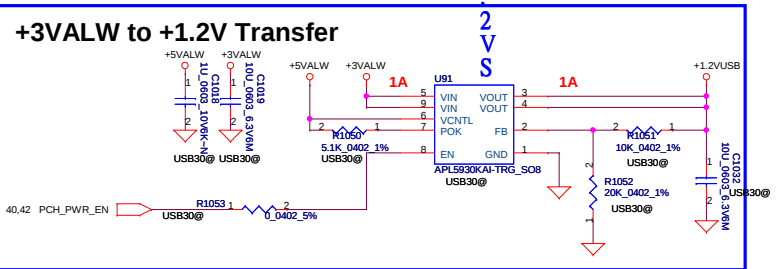
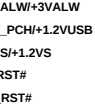
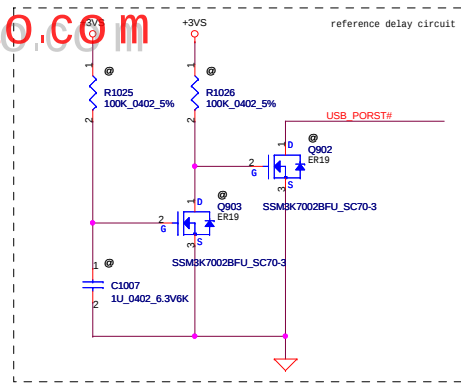
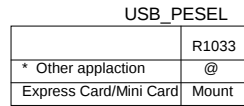




14	TMDS_B_CLK	TMDS_B_CLK#	0.1U 0402 18V7K	2	1	C625	HDMI CK+
14	TMDS_B_CLK#	TMDS_B_CLK#	0.1U 0402 18V7K	2	1	C624	HDMI CK-
14	TMDS_B_DATA0	TMDS_B_DATA0#	0.1U 0402 18V7K	2	1	C630	HDMI D0+
14	TMDS_B_DATA0#	TMDS_B_DATA0#	0.1U 0402 18V7K	2	1	C631	HDMI D0-
14	TMDS_B_DATA1	TMDS_B_DATA1#	0.1U 0402 18V7K	2	1	C633	HDMI D1+
14	TMDS_B_DATA1#	TMDS_B_DATA1#	0.1U 0402 18V7K	2	1	C627	HDMI D1-
14	TMDS_B_DATA2	TMDS_B_DATA2#	0.1U 0402 18V7K	2	1	C629	HDMI D2+
14	TMDS_B_DATA2#	TMDS_B_DATA2#	0.1U 0402 18V7K	2	1	C632	HDMI D2-

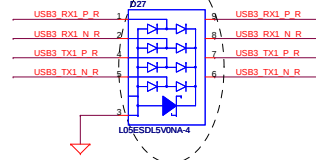
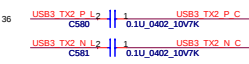
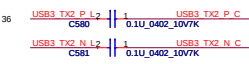
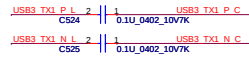
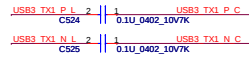


Power Sequence

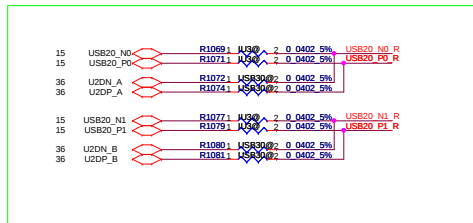
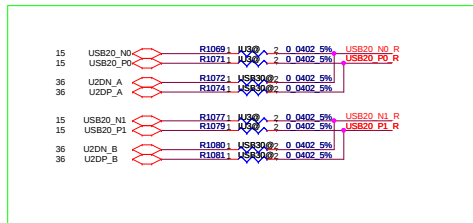
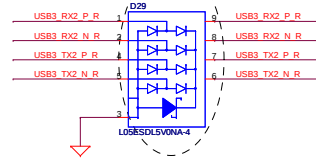


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				Size	Document Number	Rev
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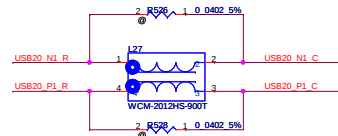
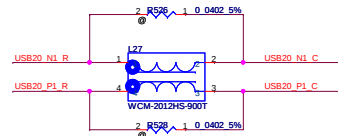
AI CHARGER



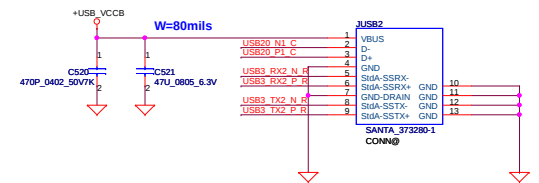
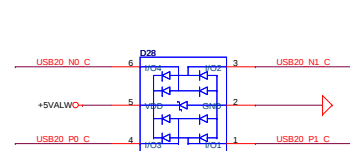
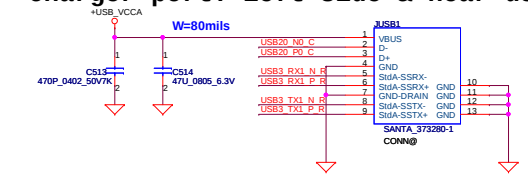
Logic diagram of the USB to RS-485 converter. The diagram shows a 74VHC04 hex inverters IC (D29) with pins 1, 2, 4, 5, 6, 7, 8, and 9 connected to USB signals: RX2_P, RX2_N, TX2_P, TX2_N, and TX2_N. Pin 3 is connected to a ground symbol. The output of pin 9 is labeled 'LOSBESOLVINGA-4'.



CB	SELCDP	Function
0	X	DCP autodetect charger mode
1	0	S0 charging with SDP only
1	1	S0 charging with SDP or CDP



charger port: left side & near user



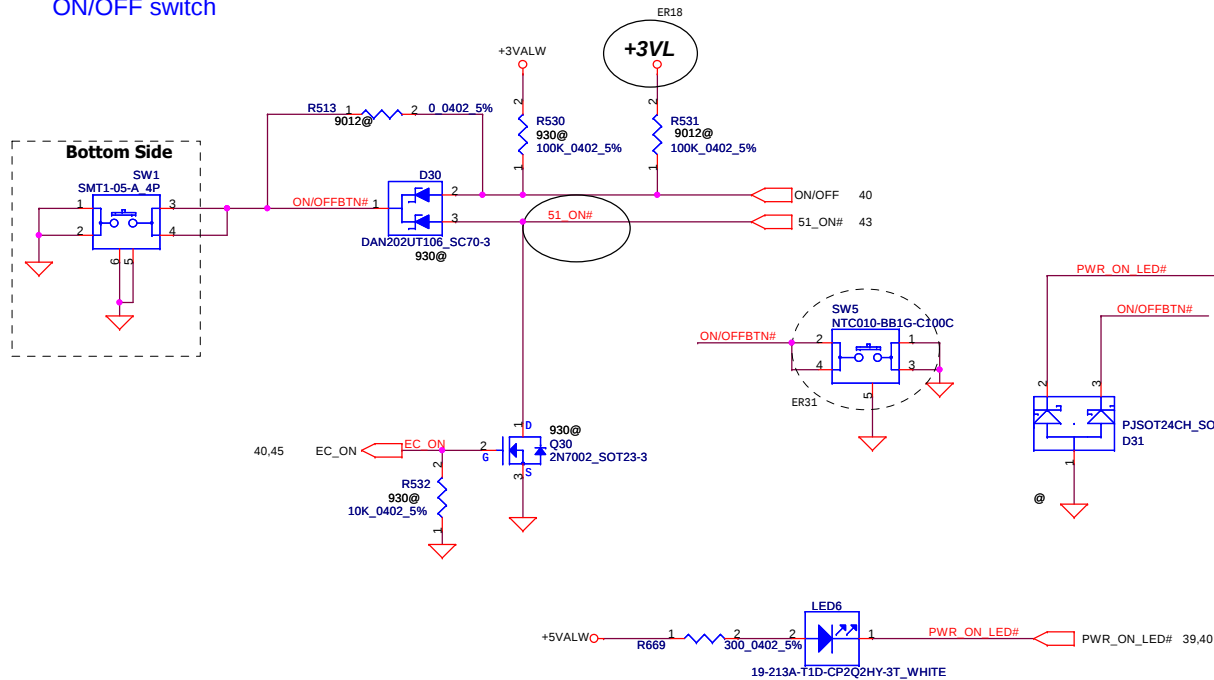
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Power Button

<http://shop61976717.taobao.com>

Screw Hole

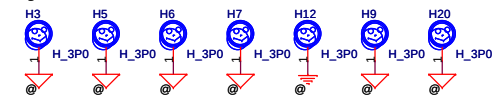
ON/OFF switch



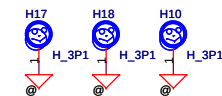
2.7



3.0



3.1



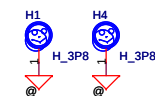
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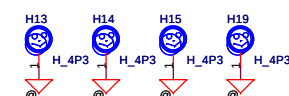
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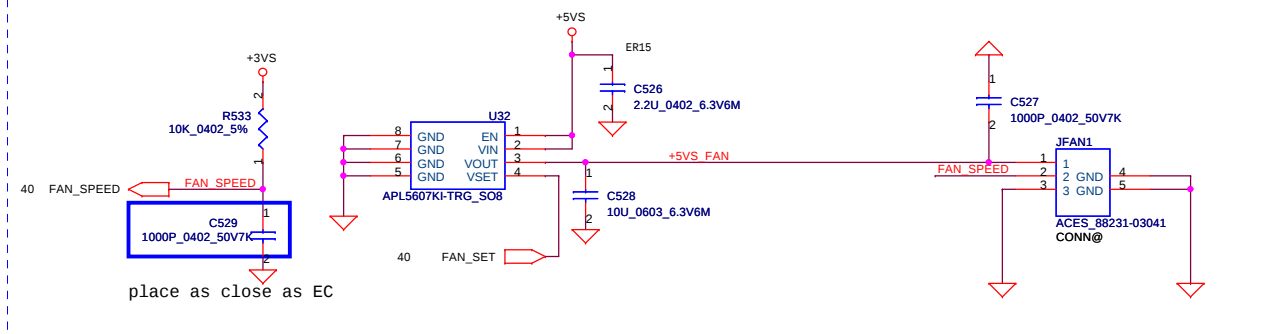
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4.3

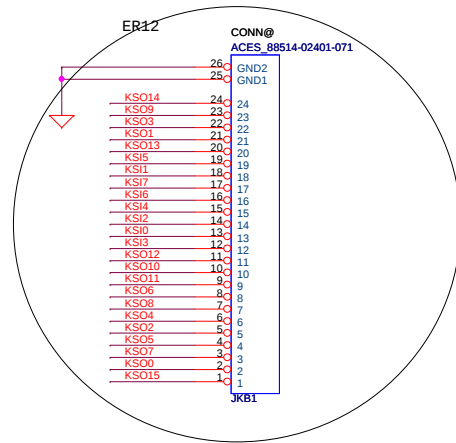
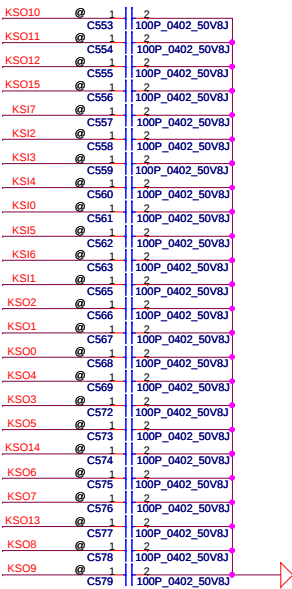
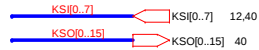


Fan Control Circuit

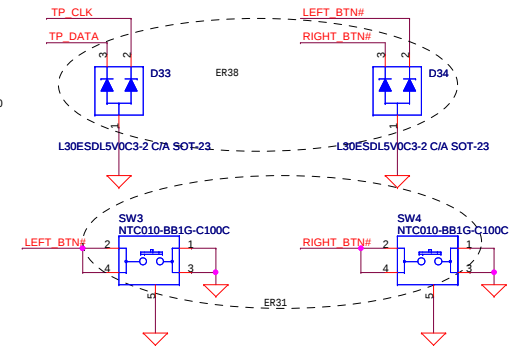
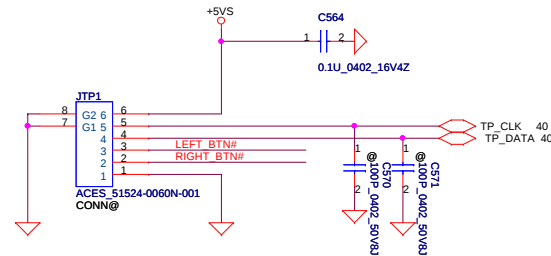


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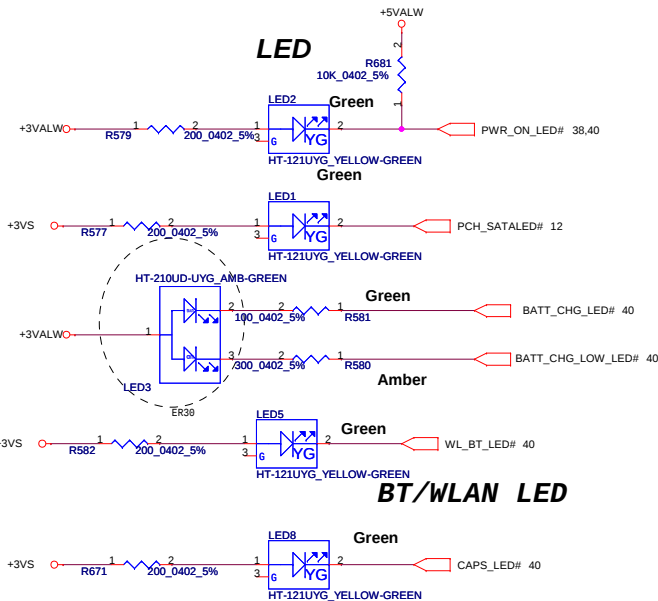
INT_KBD Conn.



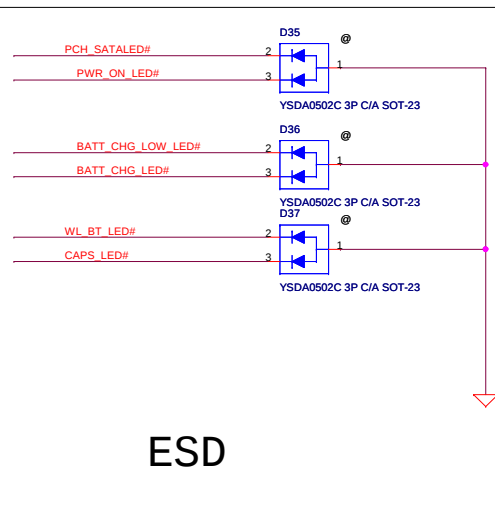
Touch/B Connector



LED

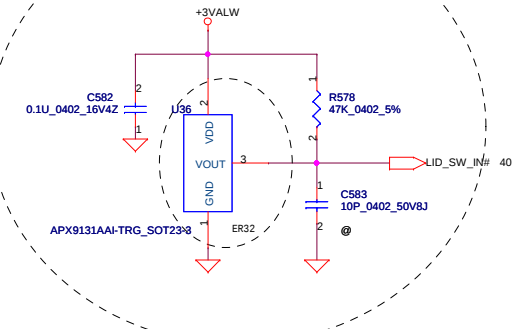


BT/WLAN LED

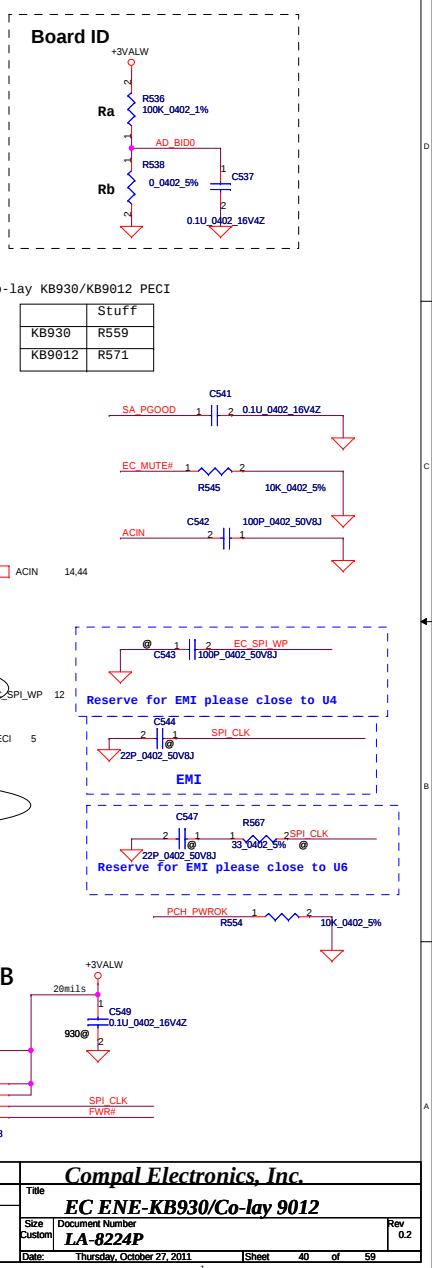


ESD

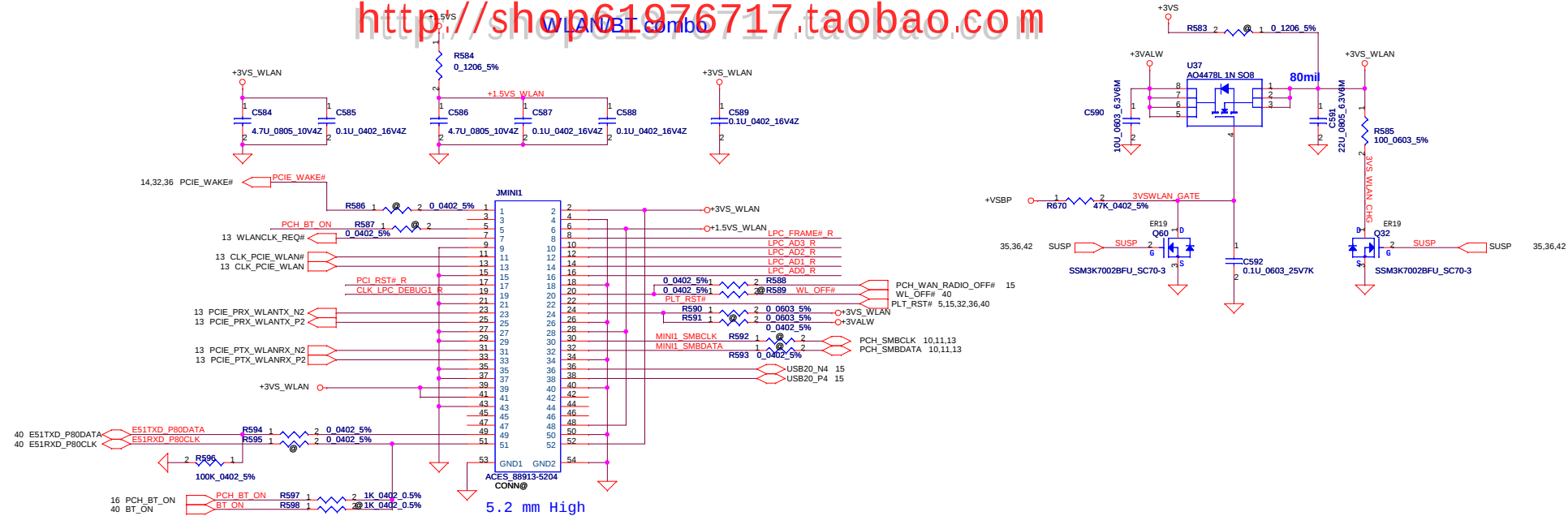
Lid Switch (Hall Effect Switch)



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				Document Number	0.2
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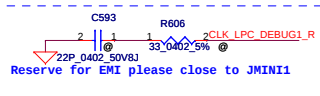


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				Custom	0.2
				LA-8224P	
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Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

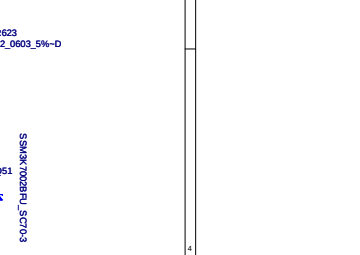
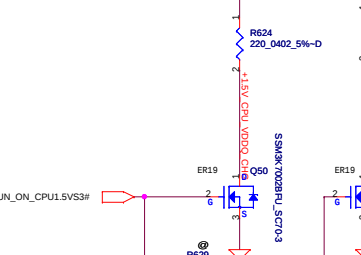
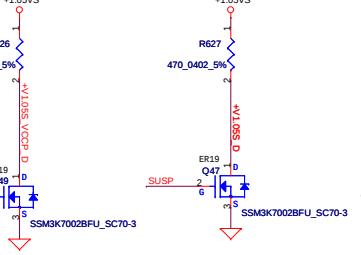
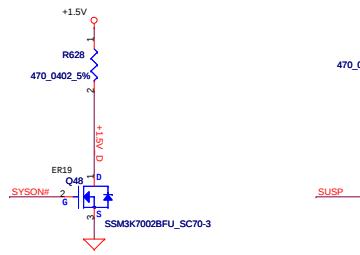
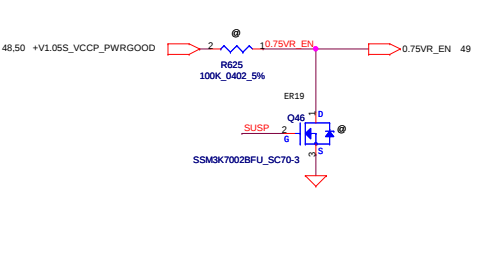
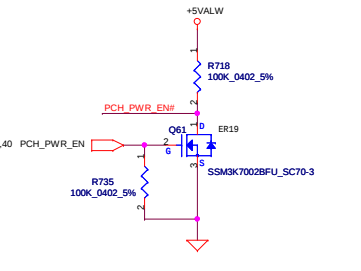
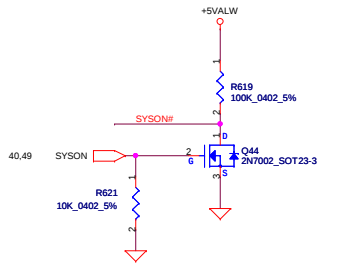
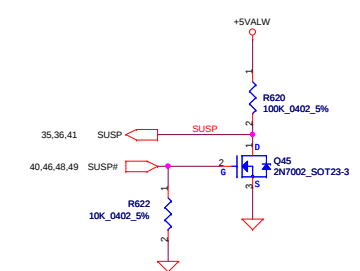
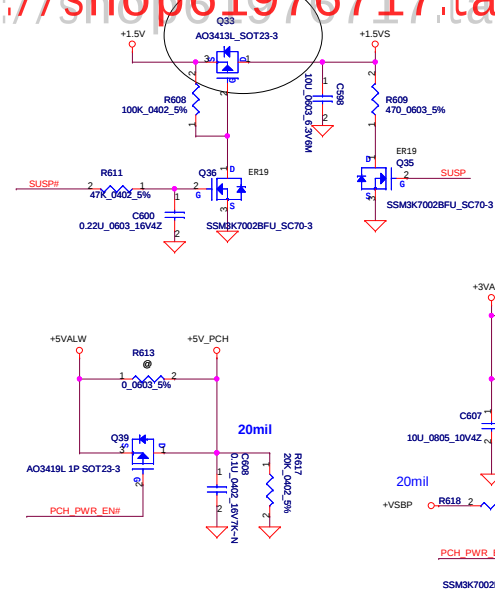
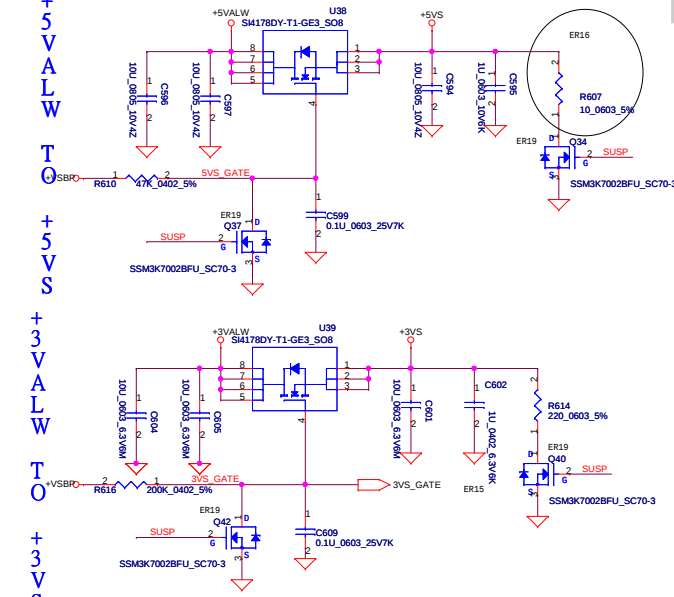
LPC_FRAME# R	R599	1	2	0.0402 5%	LPC_FRAME#	12,40
LPC_AD3 R	R600	1	2	0.0402 5%	LPC_AD3	12,40
LPC_AD2 R	R601	1	2	0.0402 5%	LPC_AD2	12,40
LPC_AD1 R	R602	1	2	0.0402 5%	LPC_AD1	12,40
LPC_AD0 R	R603	1	2	0.0402 5%	LPC_AD0	12,40
PCI_RST# R	R604	1	2	0.0402 5%	PLT_RST#	12,40
CLK_LPC_DEBUG1 R	R605	1	2	0.0402 5%	CLK_LPC_DEBUG1	15



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Date: Thursday, October 27, 2011				Sheet 41 of 59	

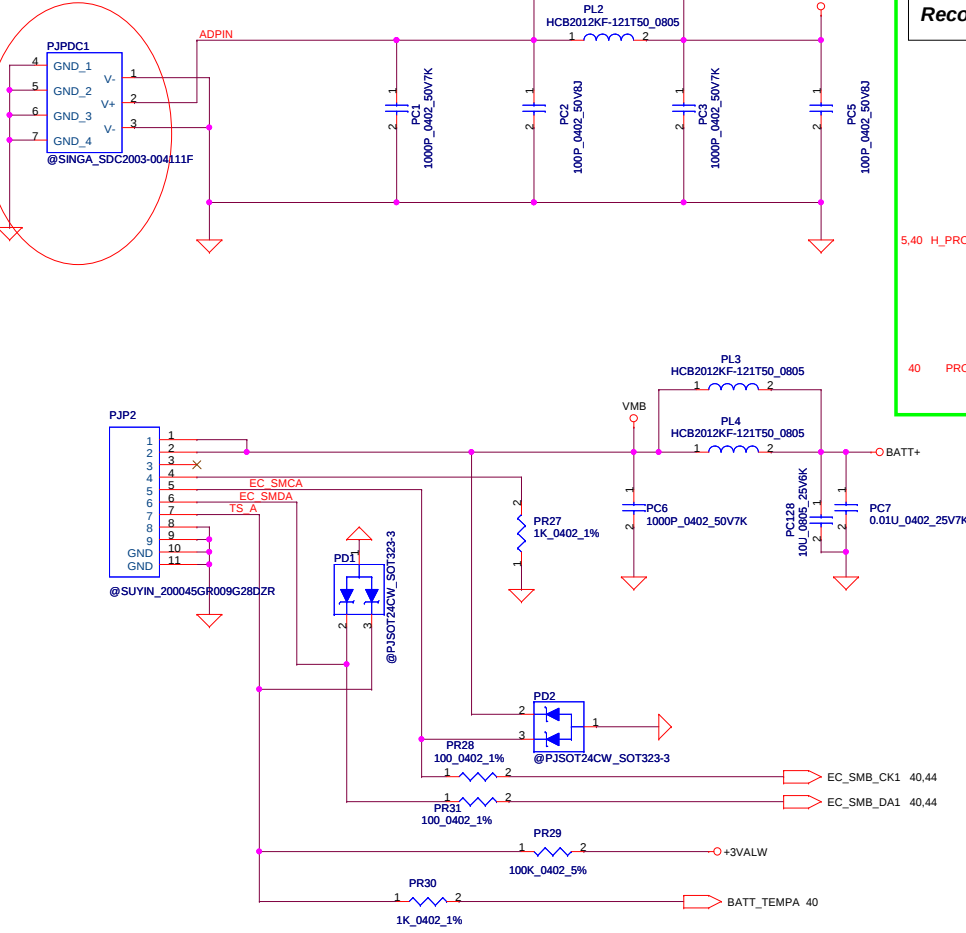
+5VALW
TO
+5VS
+3VALW
TO
+3VS

+5VS
TO
+5VS



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Size Custom				Document Number LA-8224P
Date Thursday, October 27, 2011				Rev 0.2
Sheet 42 of 59				

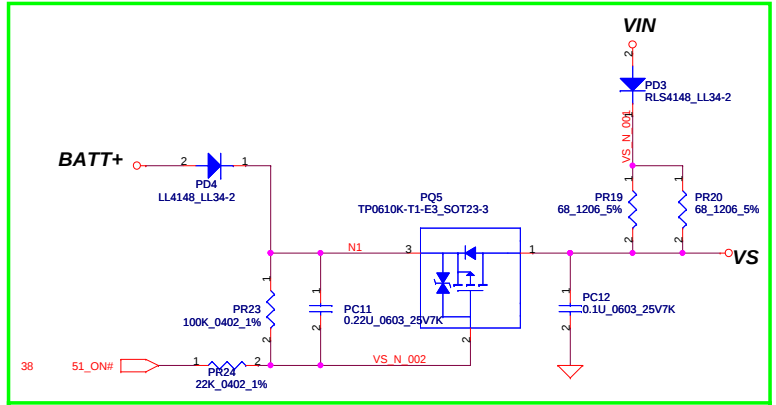
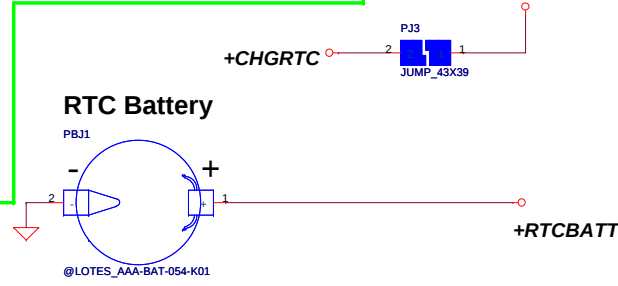
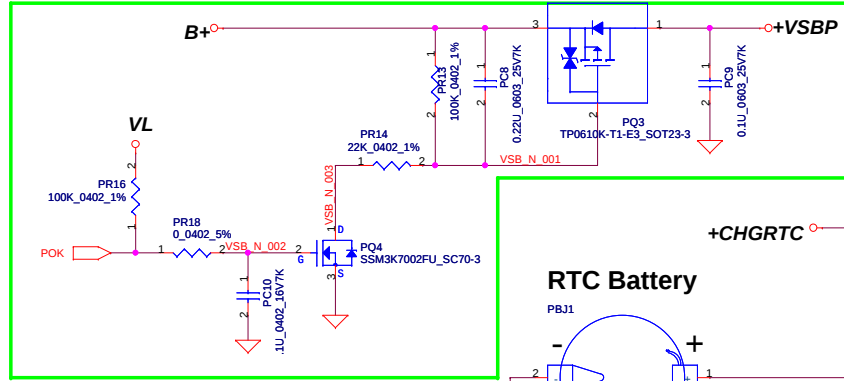
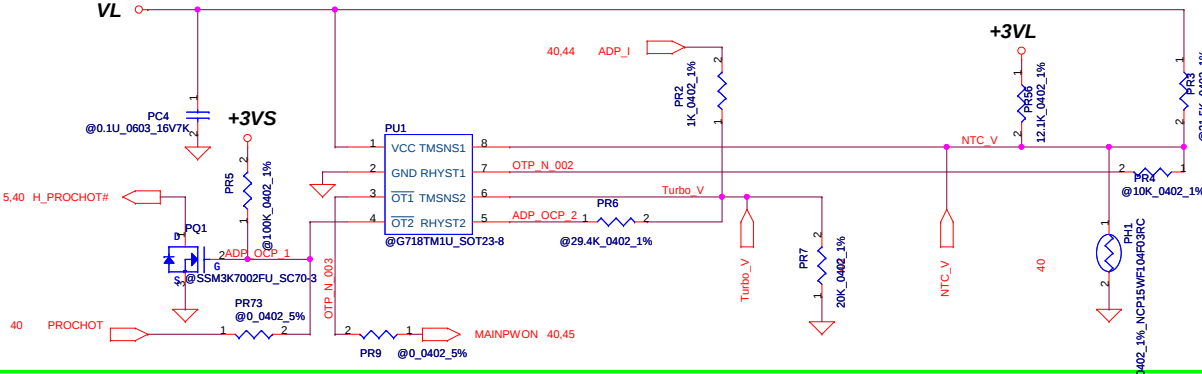
DCIN jack P/N:DC301008L00,
need doble confirm P/N with ME



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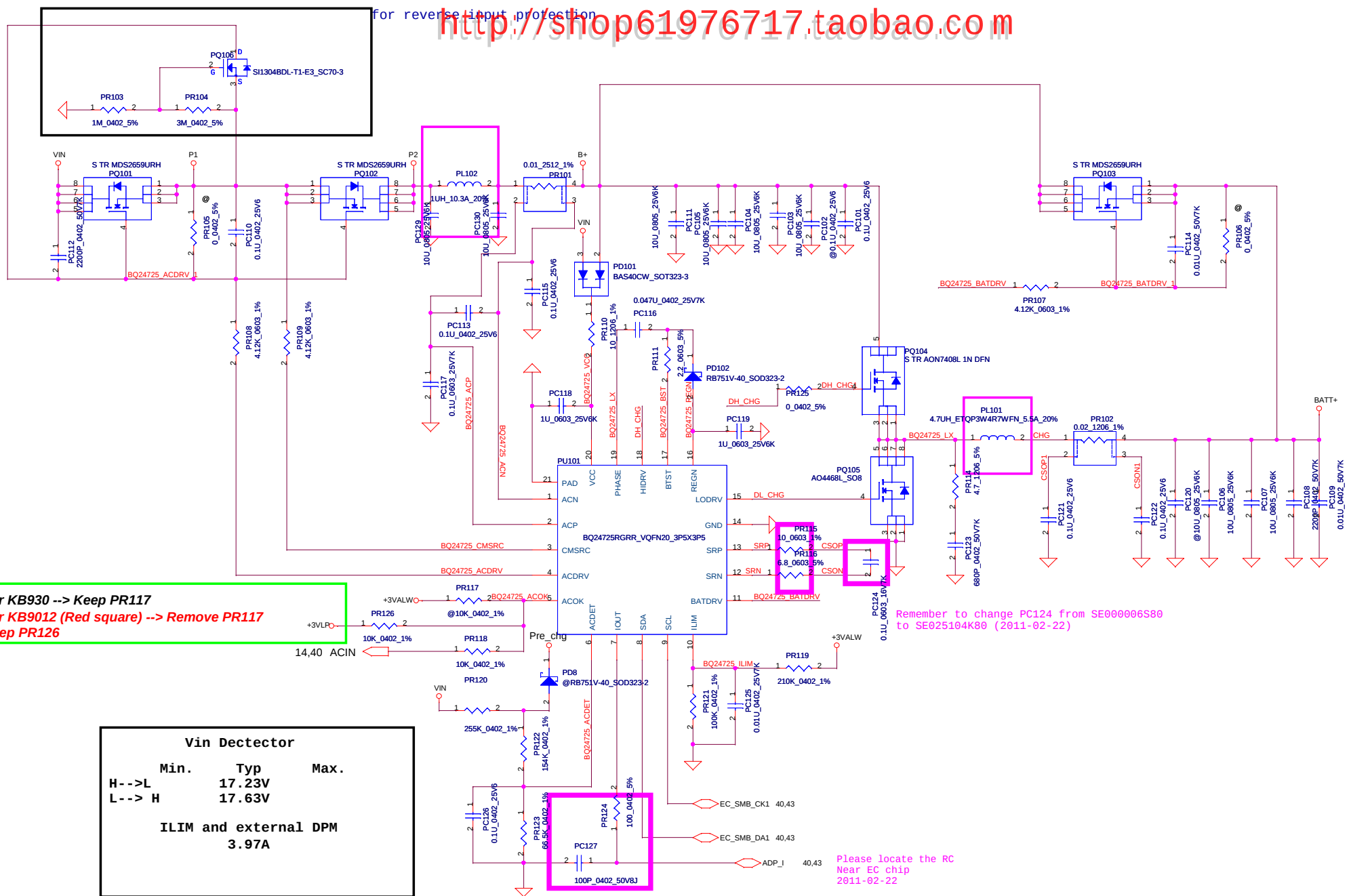
PH1 under CPU bottom side:
CPU thermal protection at 93 +3 degree C
Recovery at 56 +3 degree C

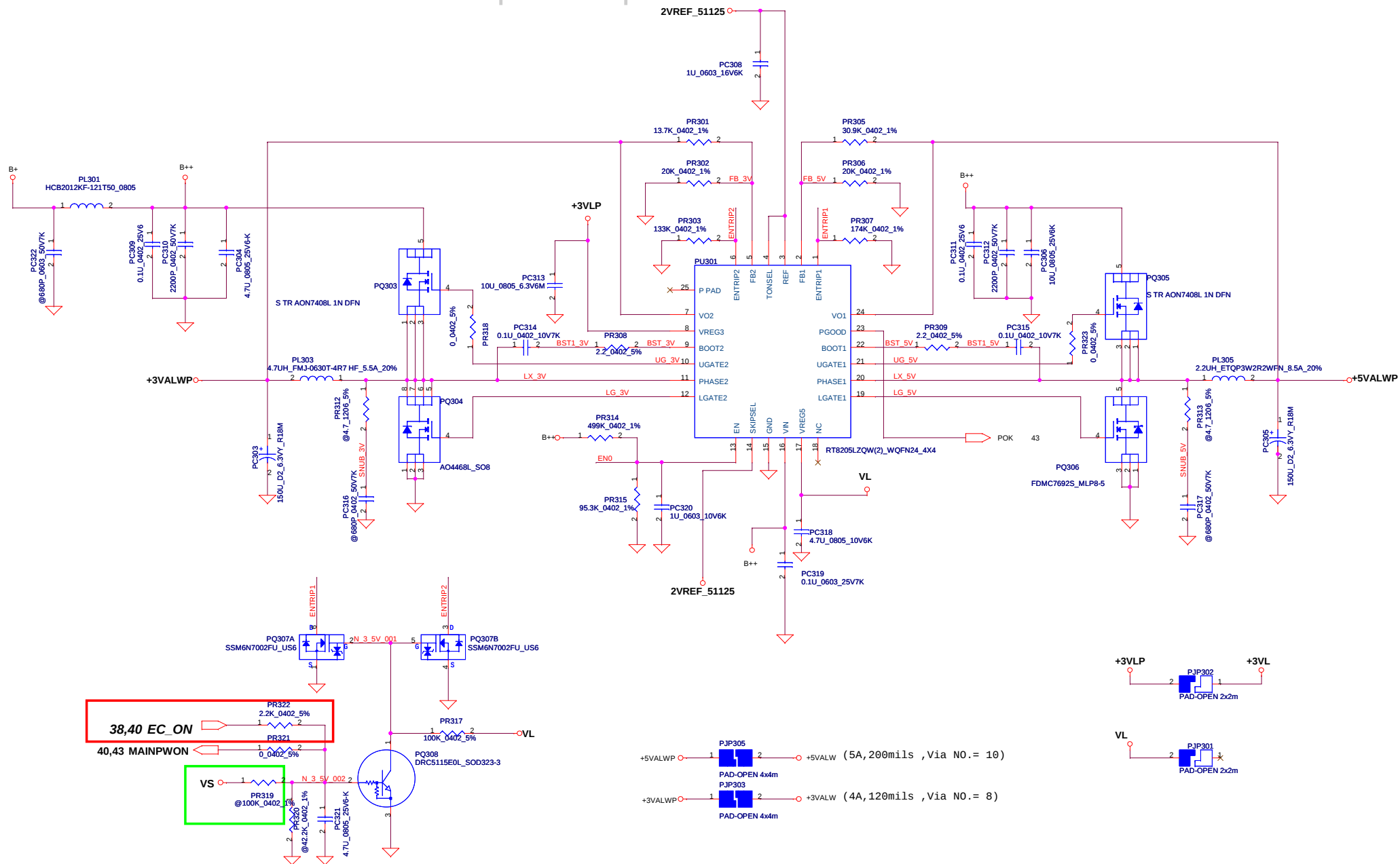
For KB930 --> Keep PU1 circuit
(Vth = 0.825V)
For KB9012 (Red square) --> Remove PU1 circuit, but keep PR56
PH1, PR2, PQ1, PR7, PQ15, PR73, PR56



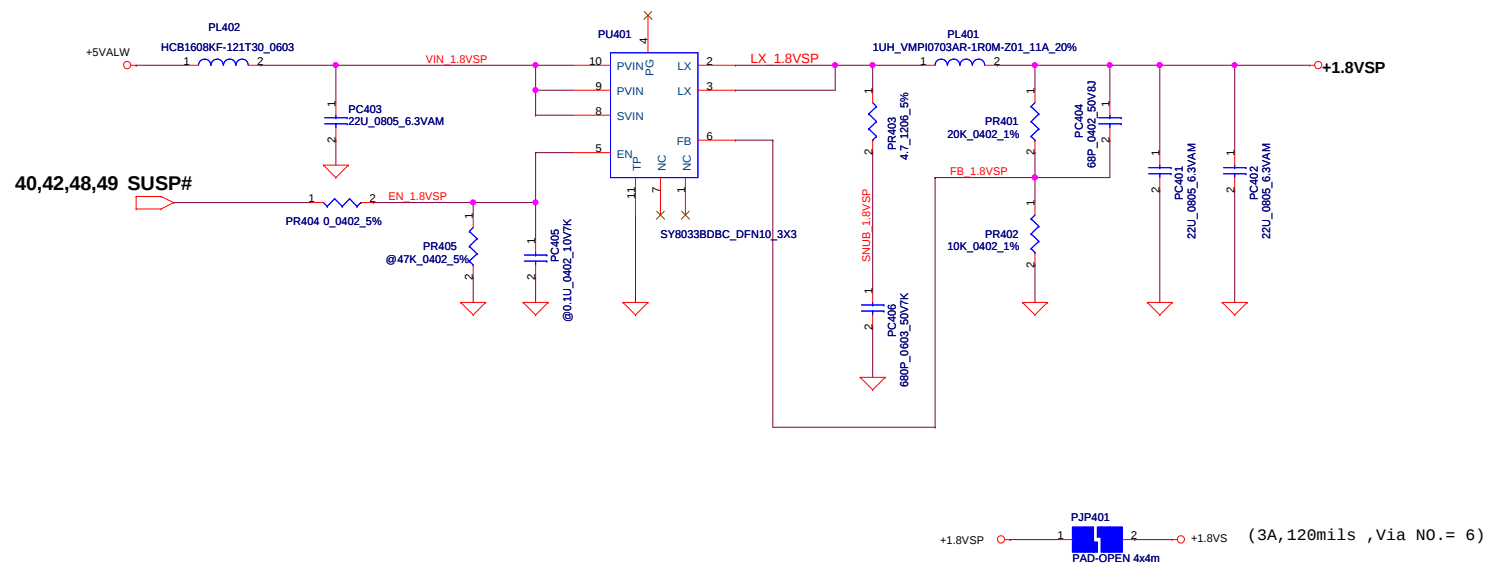
For KB9012 --> Remove all 51_ON# circuit

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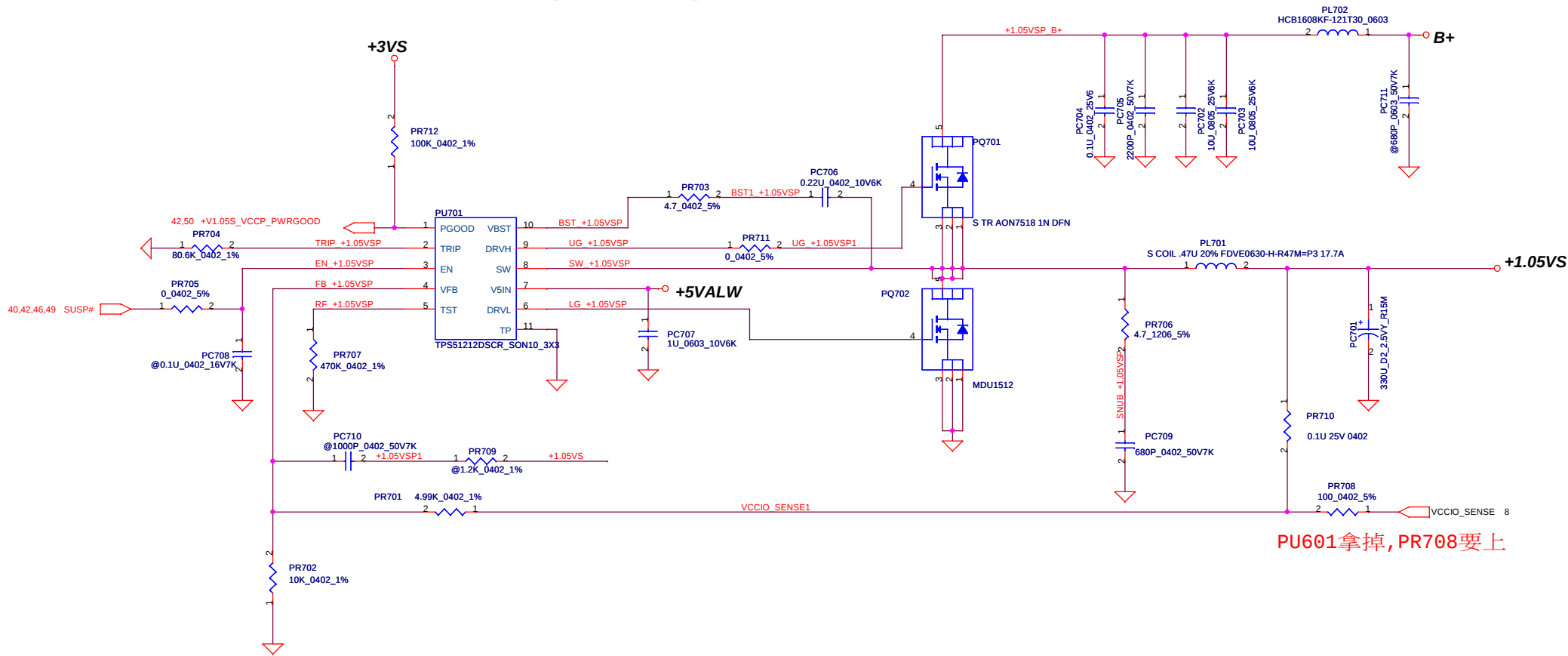
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Issued Date	2009/01/23	Deciphered Date	2012/12/31	Title	
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				Rev	0.2

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(8.5A,360mils ,Via NO.= 17)

PJP606,PJP607先斷開,確定拿掉PU605再接上

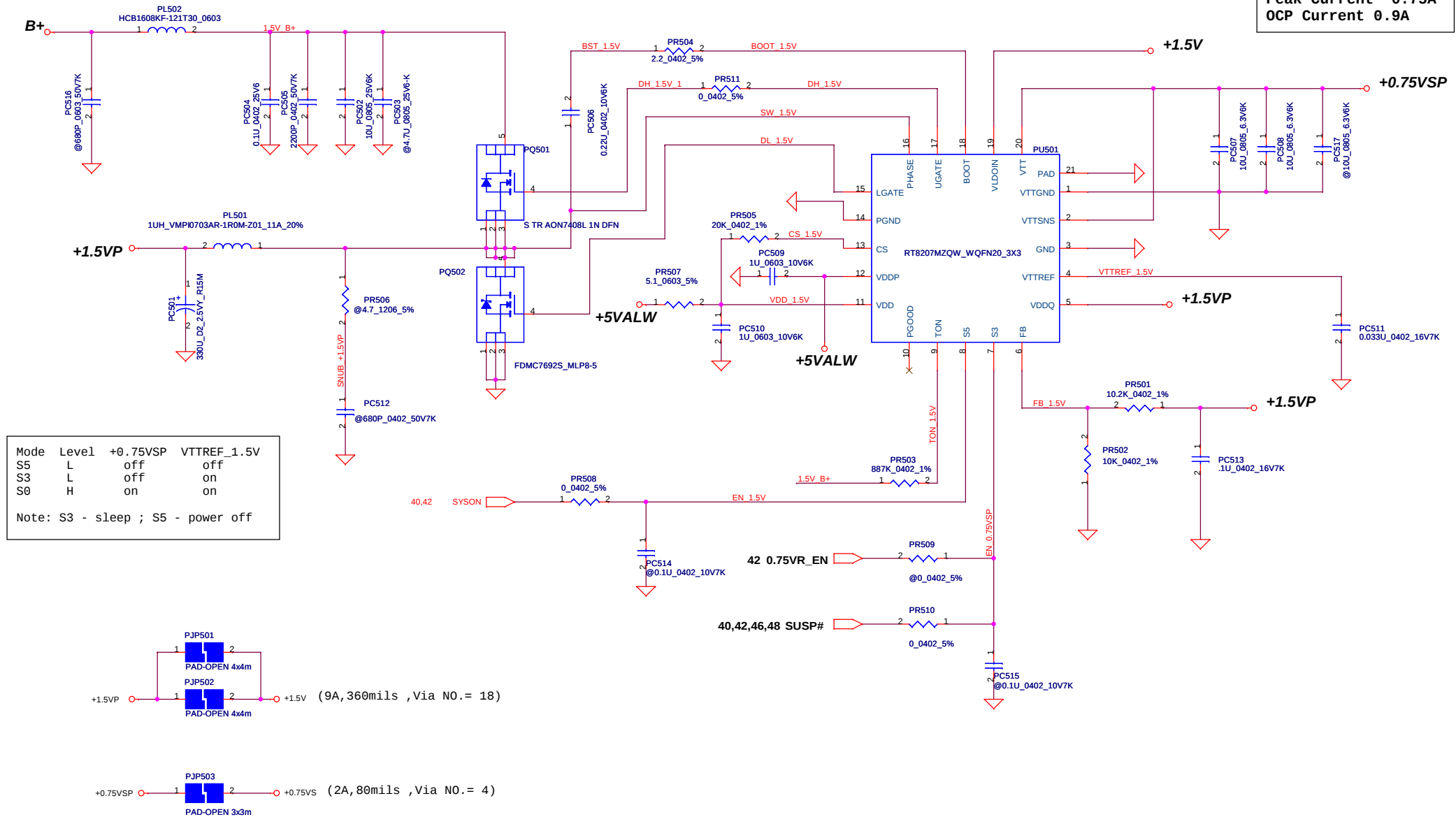
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Issued Date	2010/07/20	Deciphered Date	2012/12/31	Title	PWR-V1.05S_VCCP
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(12A,480mils ,Via N0.= 24)

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0.75Volt +/- 5%
TDC 0.525A
Peak Current 0.75A
OCP Current 0.9A

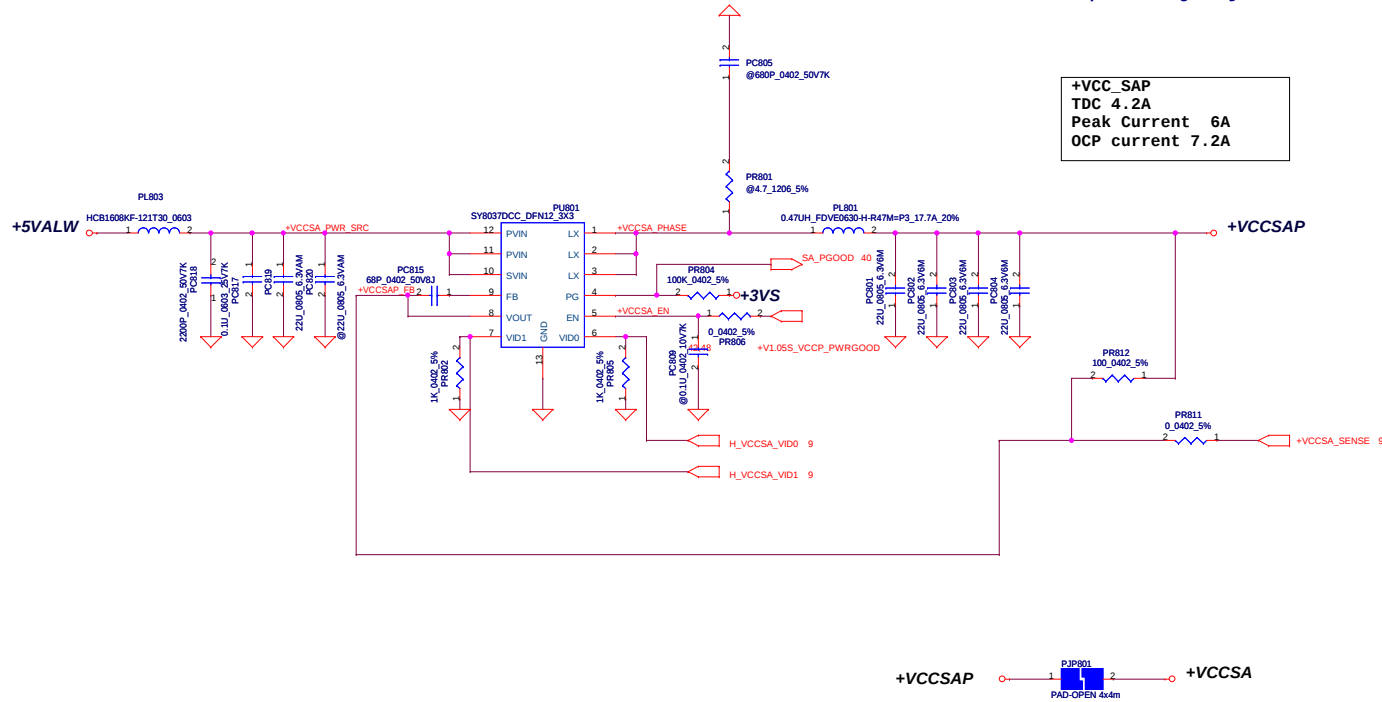


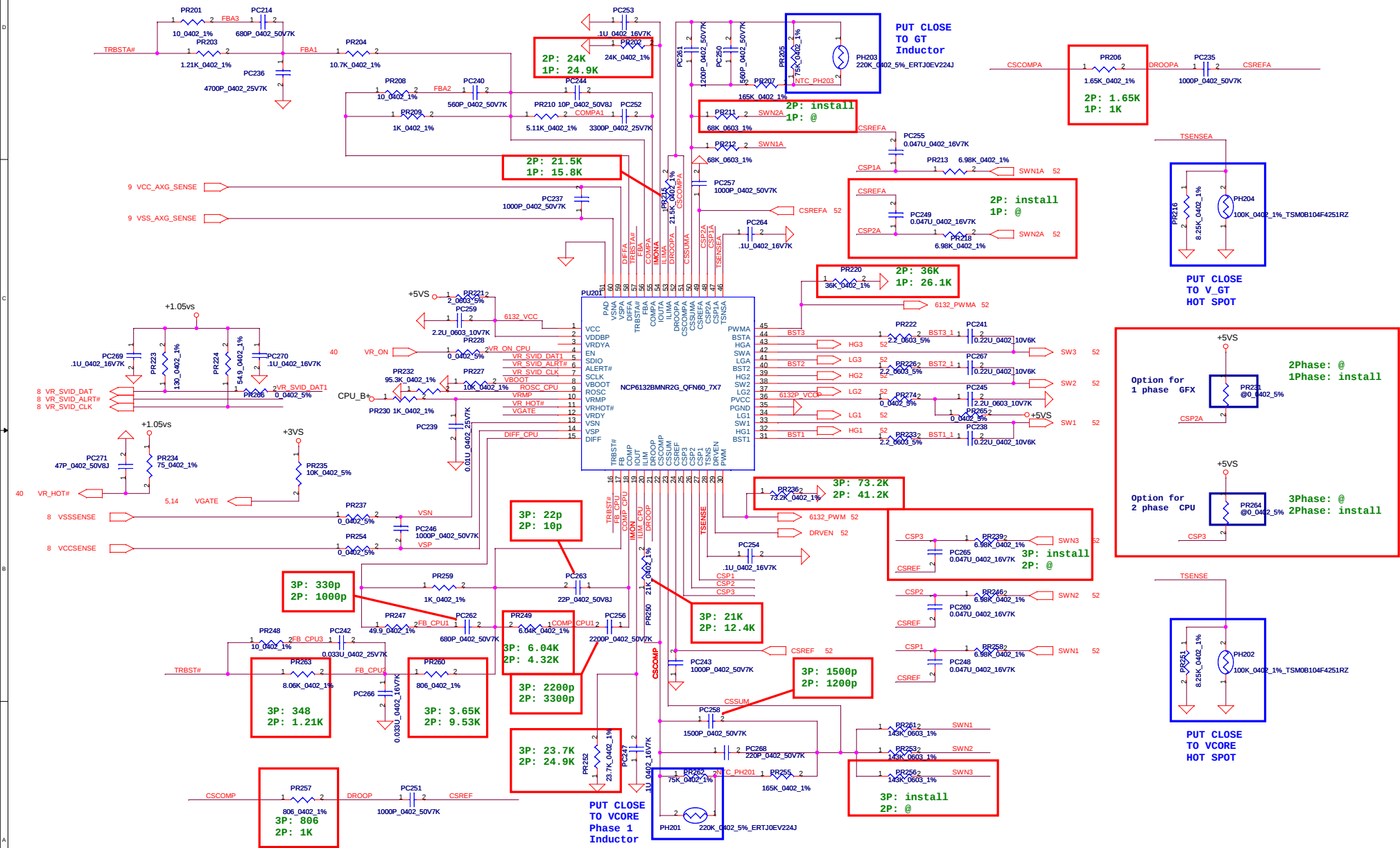
The 1k PD on the VCCSA VIDs are empty.
These should be stuffed to ensure that
VCCSA VID is 00 prior to VCCIO stability.

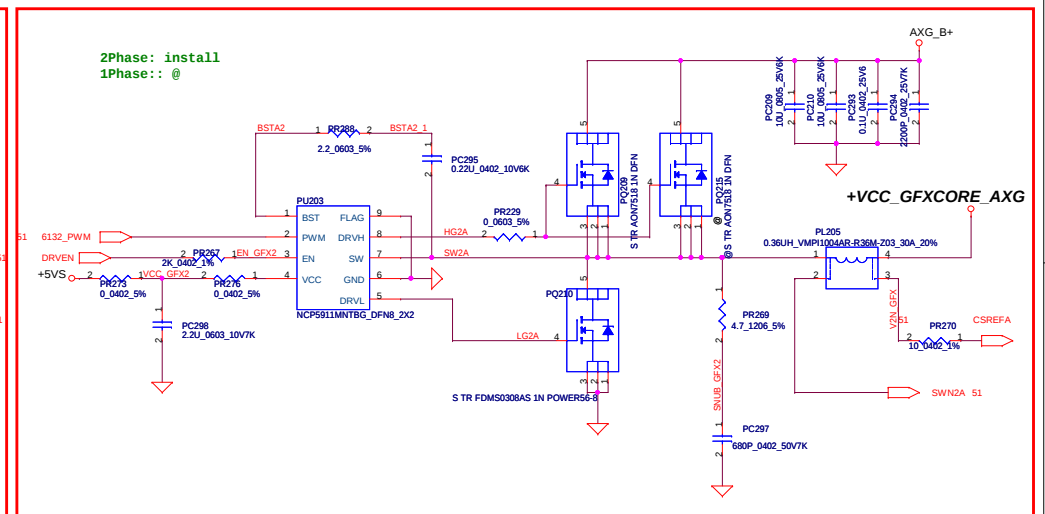
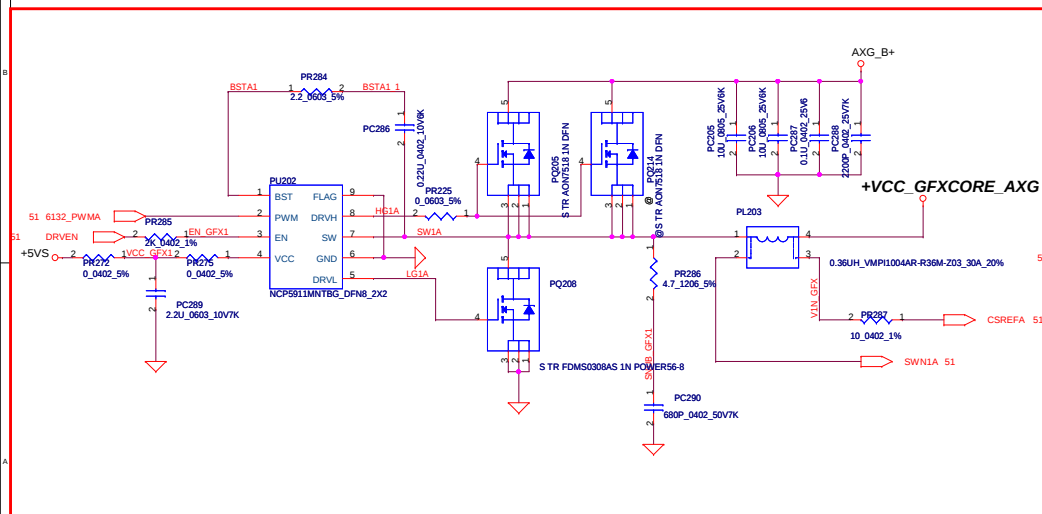
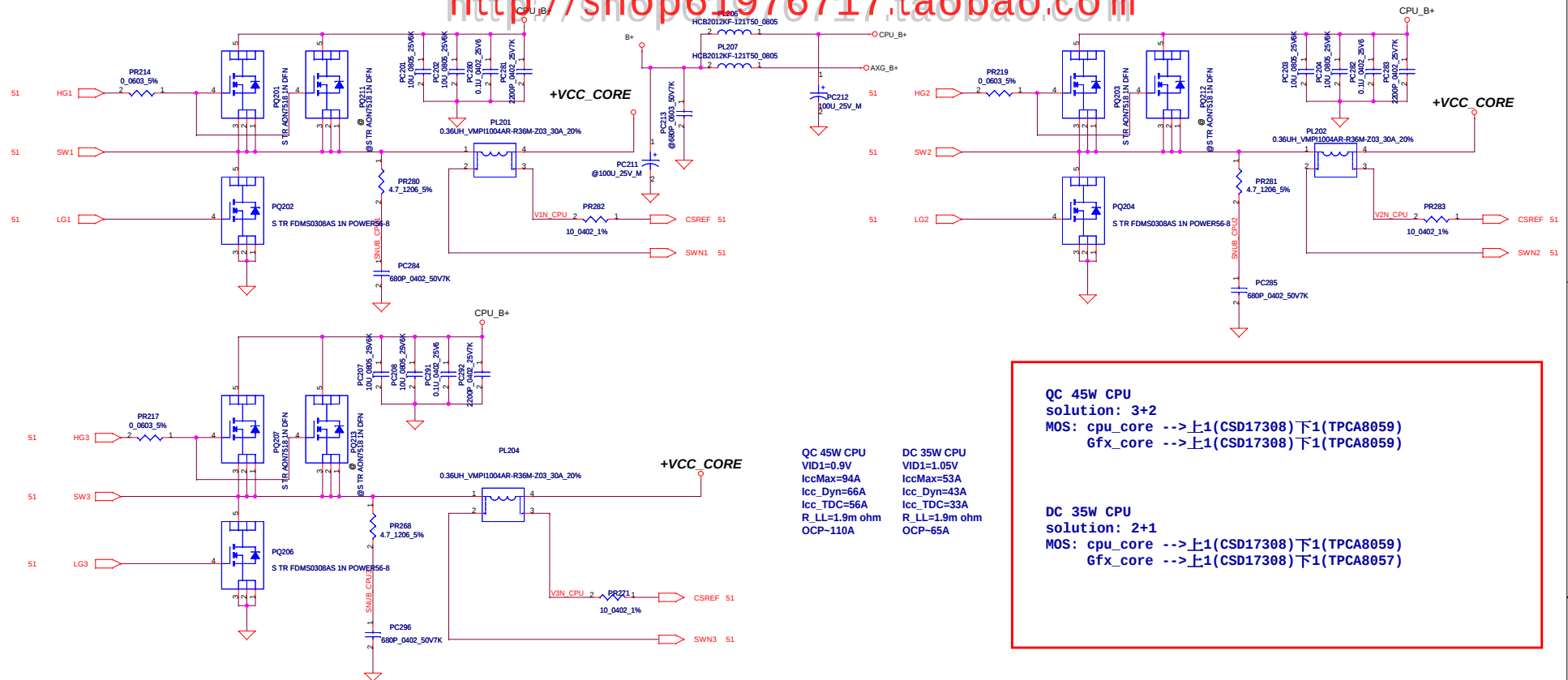
VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A





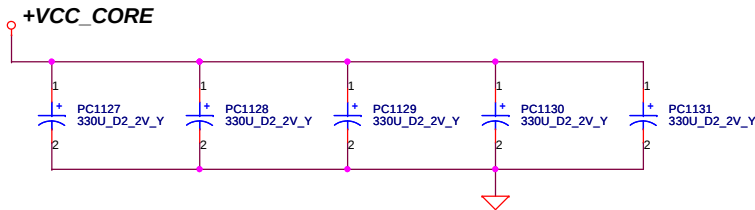
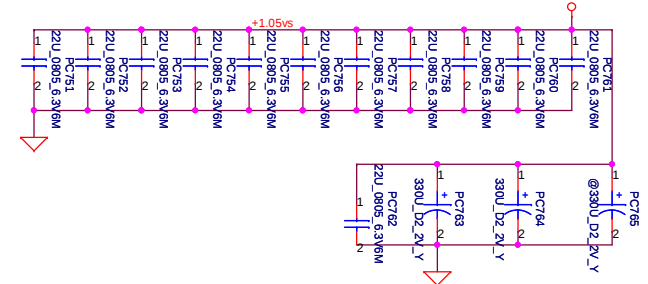
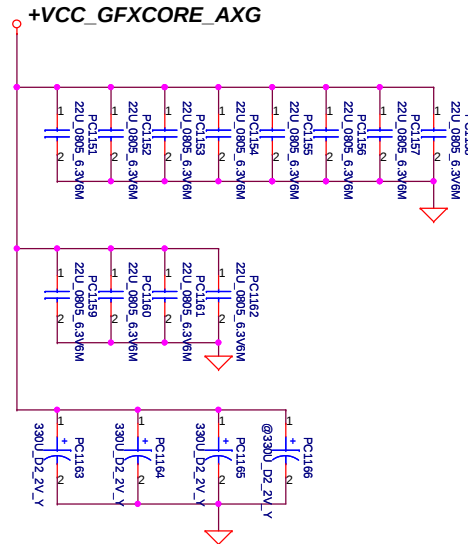
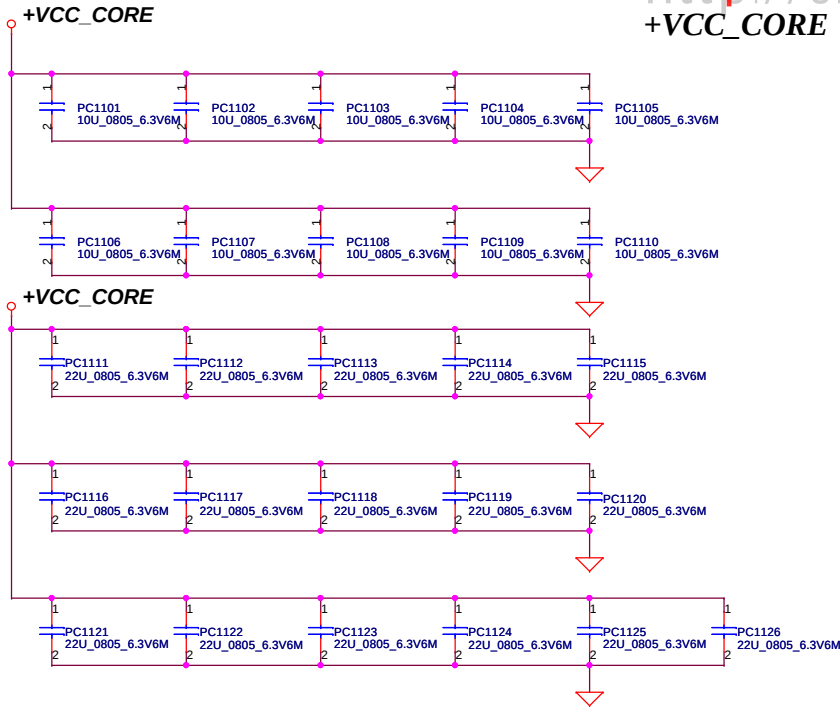


+VCC_CORE

+VCC_GFXCORE_AXG

Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 μ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 μ F (0805) 2 x (0805) no-stuff sites



Chief River	330uF*9m	470uF*4.5m	22uF	10uF
8layer for DC CPU	4		16	10
8layer for QC CPU	5		16	10
6layer for DC CPU	5		16	10
6layer for QC CPU	4	1	16	10
GFX_CORE DC	2		12	
GFX_CORE QC	3		12	
1.05V_VCCP	2		12	

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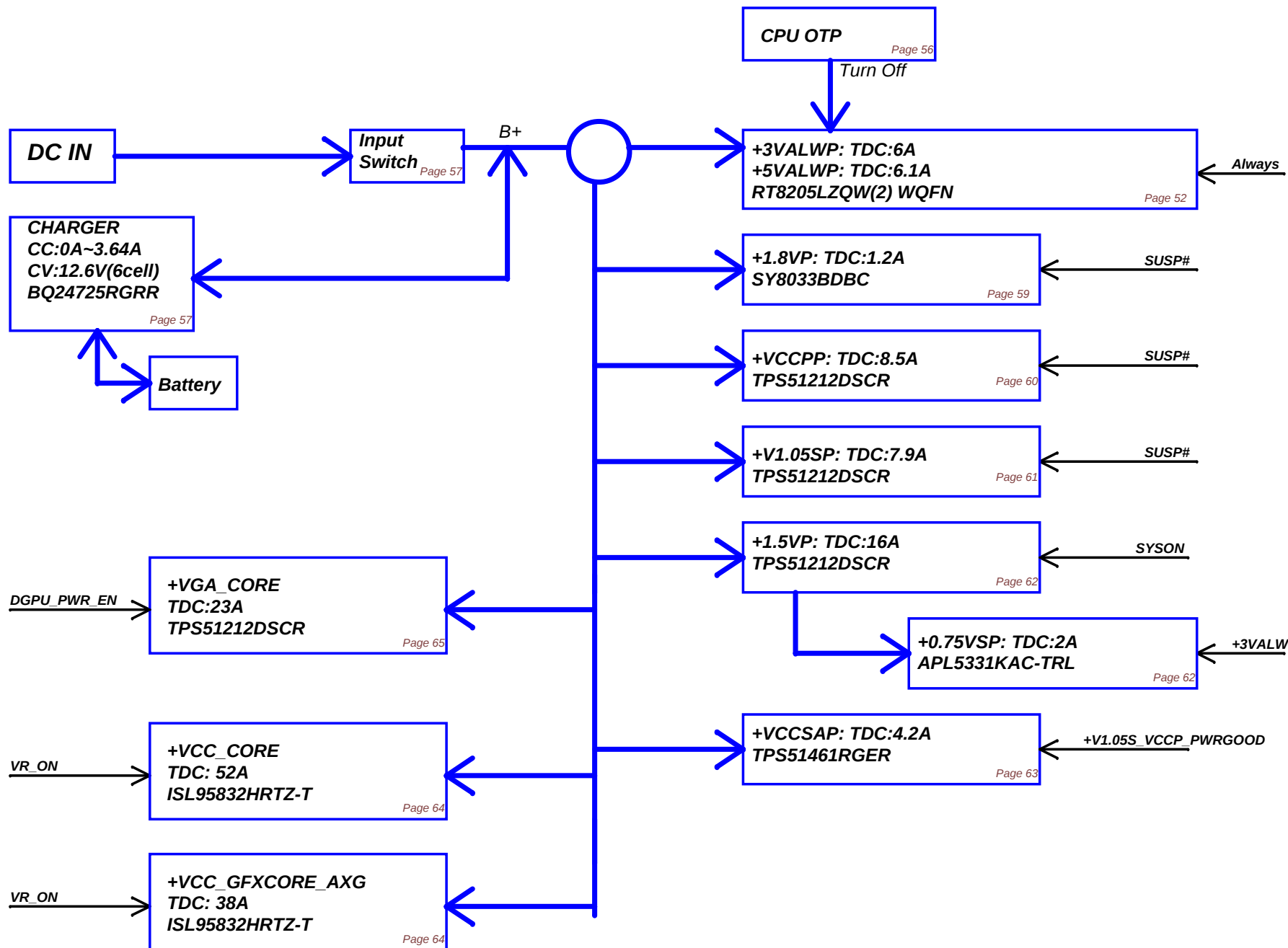
VGA的電容用料 (20W ~ 35W的bulk cap都用330uF_9m * 4)
35W--> 5 * 0.1uF +15 * 4.7u + 22u * 3 + 330_9m * 4

+VGA_CORE Near VGA Core

```
1P : @
2P: install
```

20W	25W ~30W
solution:1P	solution:2P
OCP:38A	OCP:75A

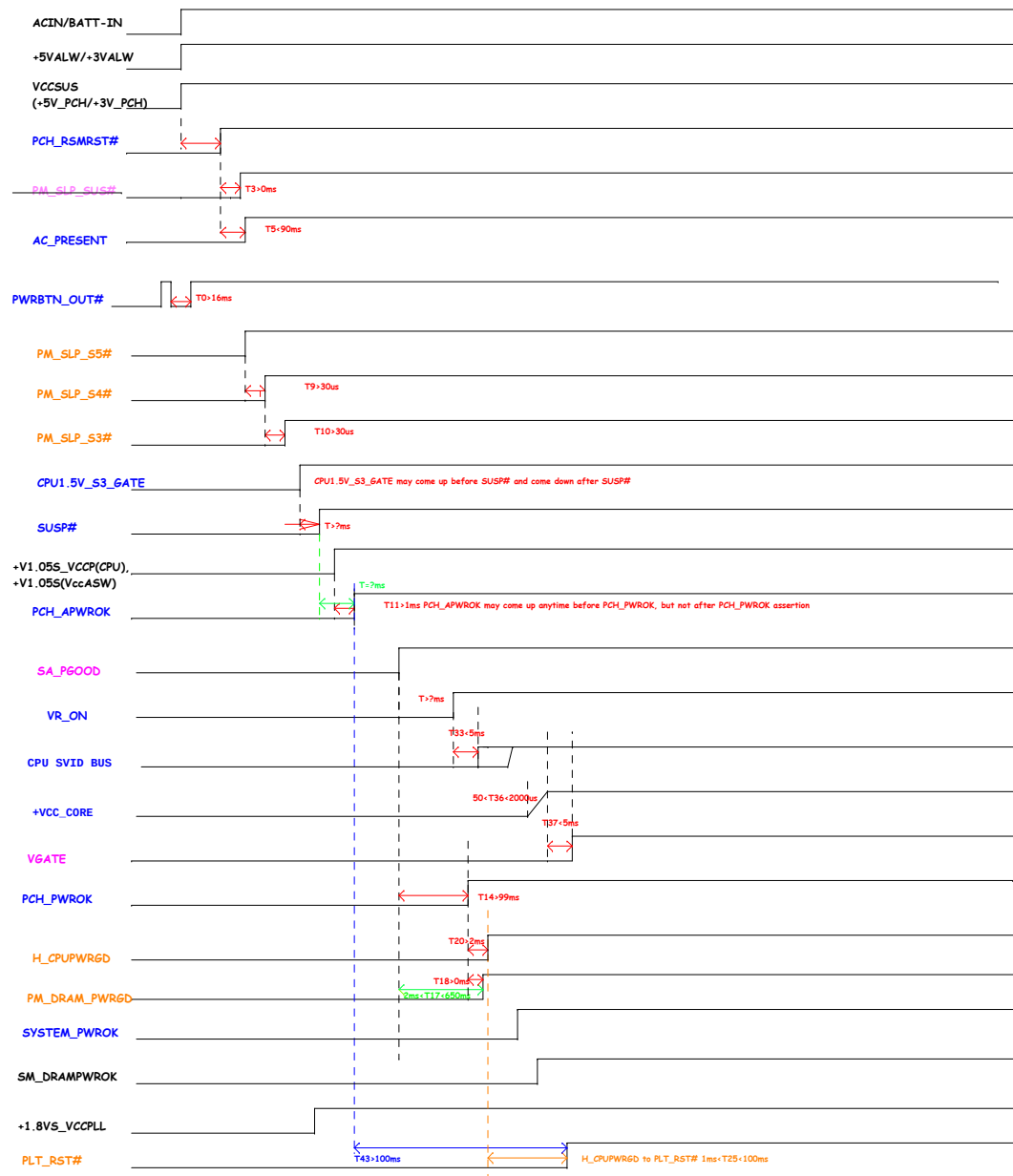
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Issued Date		Deciphered Date		Title PWR - VGA_COREP	
2008/09/15		2012/12/31		Size Document Number LA-8224P	
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DD

Timing Diagram for G3 or S4-5/M-off (Suspend Well Off) to S0/M0 (non Deep S4/S5 Platform)

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Color	Command
Signal Names	Timing of these signals is set by PCH or processor
Signal Names	Timing of these signals should be met by the platform (EC)
Signal Names	Timing of these signals is set by IntelR MVP
Signal Names	Voltage rails or chip-to-chip buses

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
ER01		HW Design (TMDS_B_HPD)	0.2	14	Delete R205	09/21	
ER02		For non AI co-lay	0.2	37	Add R745,R746 for non AI AI parts change to AI@	09/21	
ER03	+3VS Leakage	HW Design (SMBus leakage)	0.2	13 40	Delete Q3. (connect pin S & D) Remove R135, R137 Del R552, R556	09/21	
ER04	Can't detect USB30 (JUSB2)	HW Design (PCB2)	0.2	36	Swap U90_39/40 to U90_36/37 net Change R1040 to 47K from 4.7K ohm Reserve R1029	09/21	
ER05		Design change for card reader	0.2	34	Add Q20, R773, R775 Reserve R768, R774 Change Net name at Card reader Conn	09/22	
ER06		HW Design (PURC demand)	0.2	29	Change to Q3(A03404L) from U22(A04430L)	09/21	
ER07		HW Design(PCB2)	0.2	36	Change R1049 to 330k Change Q904 to A03404L from AP2301GN Change R1046 to 1.5M	09/21	
ER08		HW Design (PURC demand)	0.2	42	Change Q33 to A03413L from AP2301GN	09/21	
ER09		Fine-tune GPU timing	0.2	29	Change R433 to 0 ohm un-stuff C396 Change R432 to 10K Change R435 to 200 ohm	09/21	
ER10		HW Design (reserve)	0.2	18	Reserve R290	09/21	
ER11		HW Design(PCB2) for add VRAM DDR3 512MX8	0.2	25,26, 27,28	Add CMDA14 signal (U12-U19 pin J7)	09/28	
ER12		HW Design (change)	0.2	39	Reverse JKB1 connector	09/30	
ER13		HW Design	0.2	40	Del Y5 , C545 , C546	09/30	
ER14		HW Design (PURC demand)	0.2	15	Del R229,R230 (10K) Add R776-R783 (10K) Del R237,R239,R242 (8.2K) Add R784-R793 (8.2K)	09/30	
ER15		HW Design (PURC demand)	0.2	29,31 37,38 10,11	Change P/N C387, C389, C399, C436, C447, C602 Change P/N C389, C515, C518, C526, (0402) Change P/N C99, C109, C110, C120, C140, C141. (0402)	10/03	
ER16		HW Design(XTAL fine-tune)	0.2	42,12 13,32 20,36	Change R607 to 10 ohm Change Y3, C900, C901. Change Y1, C144, C145 Change Y4, C469, C473. Change Y2, C163, C164 Change Y9	10/07	
ER17		HW Design for instant on function	0.2	13 5	Reserve R750 R576 pin2 change to +3V_PCH from +3VS Change R576 to 0	10/07	
ER18		HW Design (power jumper change to +3VL)	0.2	38 40	jumper PJP302 (change +3VLP to +3VL @P38,P40)	10/07	
ER19		HW Design (PURC demand)	0.2		Change P/N Q7, U20, U21. Change P/N Q14-Q19, Q25, Q27-Q29, Q32, Q34-Q37, Q40-Q43, Q46-Q51, Q55-Q57, Q60, Q61, Q902, Q903, Q905. Change P/N Q23	10/14	
ER20		EMI solution	0.2	5	Add R684 to 0 (H_CPUPWRGD)	10/14	
ER21		Refer to ORB design	0.2	14 40	un-stuff D2, Add R751 un-stuff D32, R547, Add R752 Assign U33.18 to AC_PRESENT signal.	10/14	
ER22		change for GPU H/W strapping STRAP1 to PL 45K ohm to enhanced the PCIe PEG driving.	0.2	22	Change R349 from 34.8K to 45.3K	10/14	

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
ER23		modify parts for Intel review feedback message.	0.2	09 18 17 14 15	Add R289 , Add C149 0.1uf Del L6, Add R289 , un-stuff C212 Del L4, Add R387 Add R230 Stuff R244	10/14	
ER24		Modify H2 size	0.2	38	Modify H2 size	10/17	
ER25		Refer to Intel review feedback item 45.	0.2	16	Add R807	10/19	
ER26		Reserve for Deep Sx	0.2	14,16 40	Add unstuff R800, R801, R802, R803, R804, R805 Add PCH_DPWR0K, DS_WAKE#, SUSACK#, SUSWARN#	10/19	
ER27		Reserve for ROM protect	0.2	40	Add unstuff R806	10/19	
ER28		For Instant On function control by EC	0.2	06	Stuff R44, Unstuff R43	10/19	
ER29		RF request	0.2	36	Reserve R1082 , C1045	10/19	
ER30		For LED issue	0.2	39	change LED3 footprint to LED_HT-210UD-UYG_3P	10/20	
ER31		PRUC request	0.2	38 39	Change SW3, SW4, SW5 P/N	10/20	
ER32		PRUC request	0.2	39	Change U36 P/N	10/20	
ER33		For EMI request (without MS_CLK)	0.2	34	Remove R637, C611, R631, C620.	10/20	
ER34		dGPU thermal throttling.	0.2	20 40	Add R428, Revise U11 I/O signal. Un-stuff R730.	10/20	
ER35		SPI flash data crisis prevention.	0.2	12 40	Add Q63, R135, R137. Change U33.41 net to EC_SPI_WP. remove R806.	10/20	
ER36		Power switch EOS issue prevention.	0.2	37	Change C510, C516, C519 to 0.22uF/16V.	10/20	
ER37		For EMI request	0.2	32 35	Change R485 , R486 to 0.1uF Reserve C641-C648	10/20	
ER38		For ESD request	0.2	37,35 30,39	Change D27, D29, D24, D25. Change D6, D7, D9, D10, D33, D34.	10/20	
ER39		Modify X76 table (N13P-GS & N13M-GE1 x8)	0.2	3	update X76 table (add ZZZ9 -ZZZ12 for N13P-GS & N13M-GE1 x8) & P/N	10/25	
ER40		update Power circuit	0.2	43-56	update Power circuit. (PC211)	10/26	
ER41		Modify PCH_SPI_WP# singal control by EC	0.2	12	Stuff R135	10/26	
ER42		Add test point for DFT	0.2	20	Add GPU_JTAG_TCK, GPU_JTAG_TDI, GPU_JTAG_TDO, GPU_JTAG_TMS	10/27	
ER43		For ASM1042 OC# pull-up	0.2	37	Reserve R1023, R1024 un-stuff	10/27 b	

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