COMPAL CONFIDENTIAL

MODEL NAME : ZAM81

PCB NO : LA-A914P

BOM P/N :

GPIO MAP: 3.1

Huston 15" DSC Entry

Broadwell U

2013-08-20

REV : 0.1 (X00)

@ : Nopop Component

EMC@ : EMI, ESD and RF Component

@EMC@ : EMI, ESD and RF Nopop Component

XDP@ : XDP Component

CONN@ : Connector Component

MB PCB

Part Number	Description
DA8000Z8000	PCB 13N LA-A914P REV0 MB DSC NONDOCK 3

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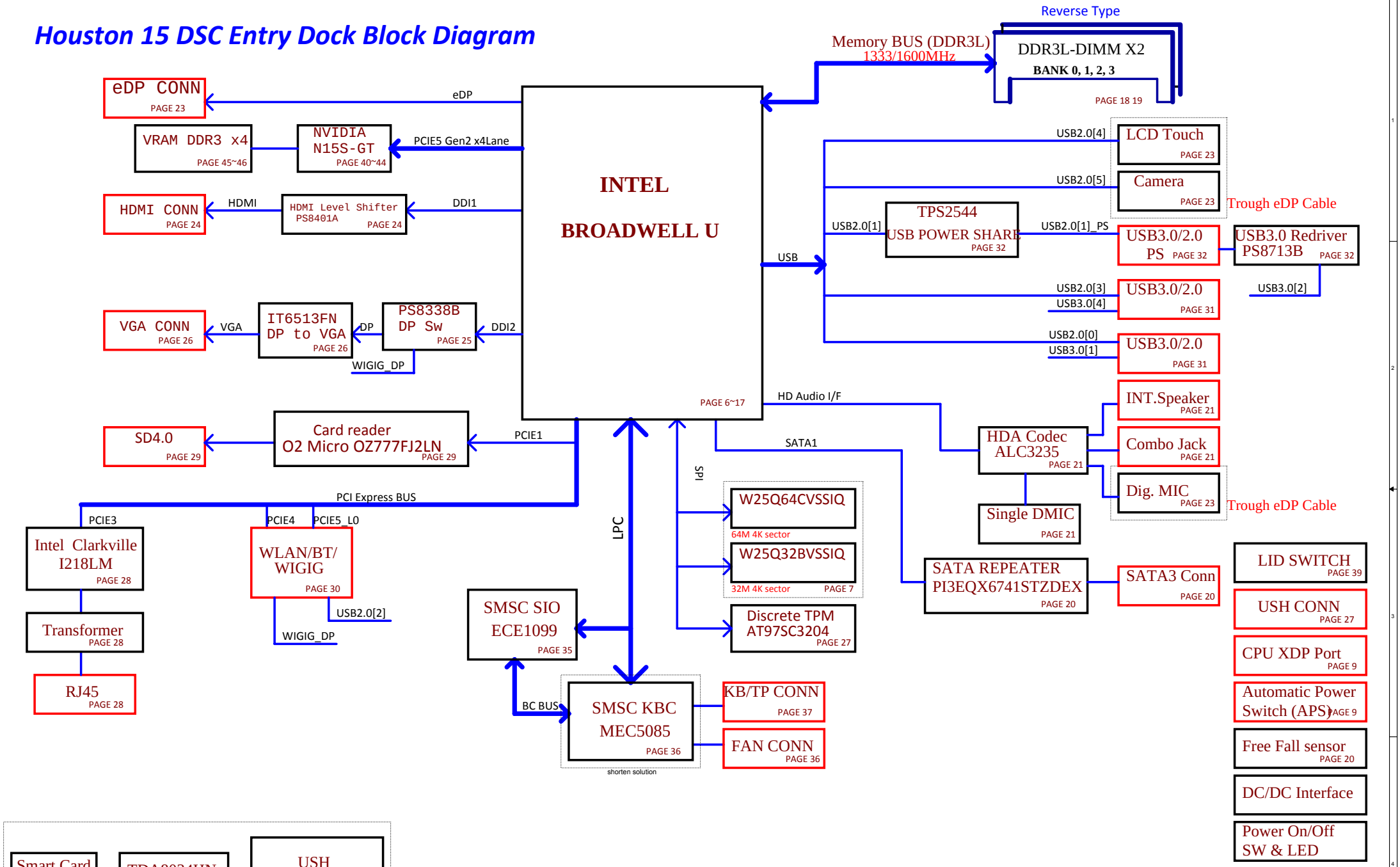
Houston 15 DSC Entry Dock Block Diagram



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POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

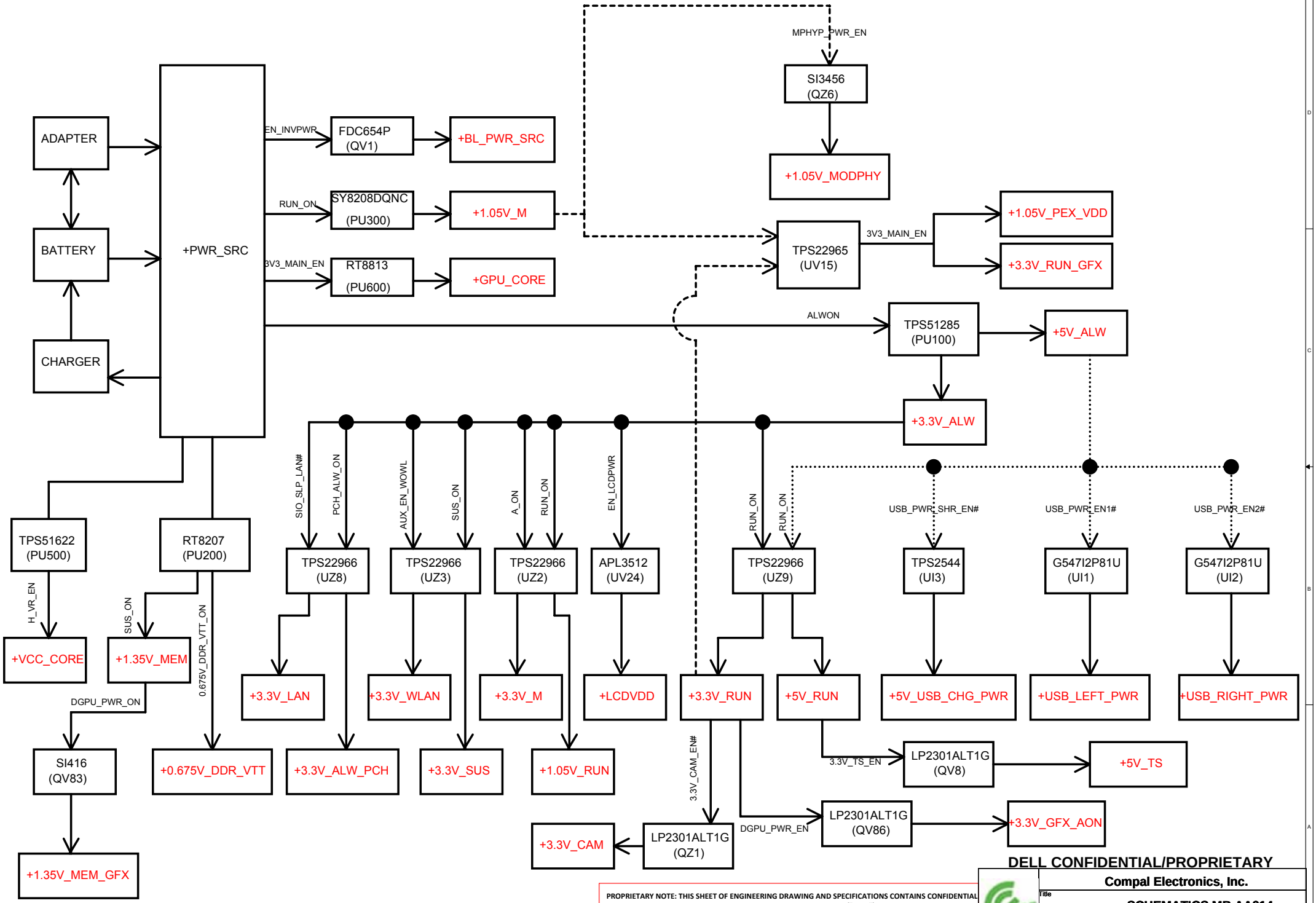
State \ power plane	+5V_ALW +3.3V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.35V_MEM	+5V_RUN +3.3V_RUN +0.675V_DDR_VTT +1.05V_RUN +VCC_CORE	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF	OFF	OFF

need to update Power Status and PM Table

PCIE	USB3.0	SATA	DESTINATION
	USB3.0 1		JUSB1-->Rear left
	USB3.0 2		JUSB3-->Right
PCIE 1	USB3.0 3		MMI (CARD READER)
PCIE 2	USB3.0 4		JUSB2-->Rear Right
PCIE 3			LOM
PCIE 4			WLAN
PCIE 5			GPU/WIGIG
PCIE 6		SATA 3	WIGI/Express
		SATA 2	mSATA/PCIE
		SATA 1	HDD
		SATA 0	DOCK

	USB PORT#	DESTINATION
BDW ULT	0	JUSB1
	1	JUSB3
	2	WLAN + BT
	3	JUSB2
	4	Touch Screen
	5	CAMERA
	6	USH
	7	WWAN

USH	0	BIO
	1	NA



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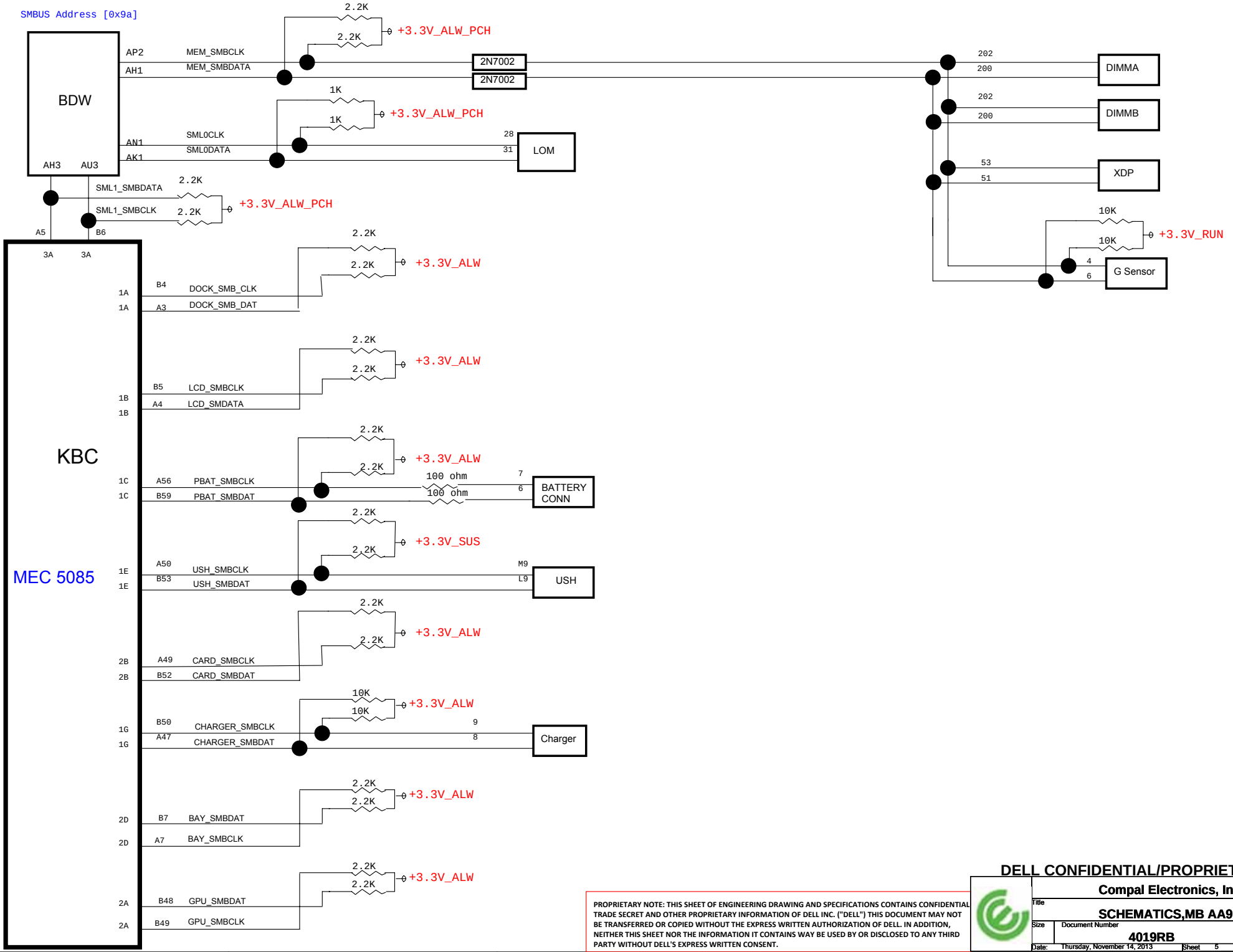

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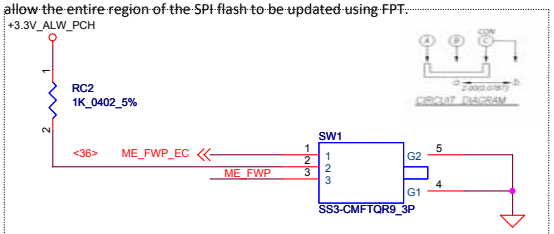
DSC SATA port

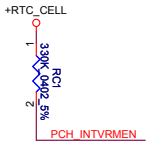
SATA0	SATA1	PCB	SATA2/PCIE6 L1	SATA3/PCIE6 L0	
E-Dock	HDD	H12 UMA	M2 3042 2nd PCIe Lane for PCIe Cache	M2 3042 (HCA & SATA-Cache)	contact to WWAN
NA	HDD	H12 Entry	NA	NA	
E-Dock	HDD	H14 DSC	M2 3042 SATA-Cache(no HCA)	M2 3030 WIGIG	SATA2/PCIE6_L1 contact to WWAN SATA3/PCIE6 L0 contact to WLAN
E-Dock	HDD	H14 UMA	M2 3042 2nd PCIe Lane for PCIe Cache	M2 3042 (HCA & SATA-Cache)	contact to WWAN
NA	HDD	H14D_En	NA	M2 3030 WIGIG	contact to WLAN
NA	HDD	H14U_En	NA	NA	
E-Dock	HDD	H15 DSC	M2 3042 SATA-Cache(no HCA)	M2 3030 WIGIG	SATA2/PCIE6_L1 contact to WWAN SATA3/PCIE6 L0 contact to WLAN
E-Dock	HDD	H15 UMA	M2 3042 2nd PCIe Lane for PCIe Cache	M2 3042 (HCA & SATA-Cache)	contact to WWAN
NA	HDD	H15D_En	NA	M2 3030 WIGIG	contact to WLAN
NA	HDD	H15U_En	NA	Express card	contact to Express card

Service Mode Switch:
Add a switch to ME_FWP signal to unlock the ME region and allow the entire region of the SPI flash to be updated using FPT.

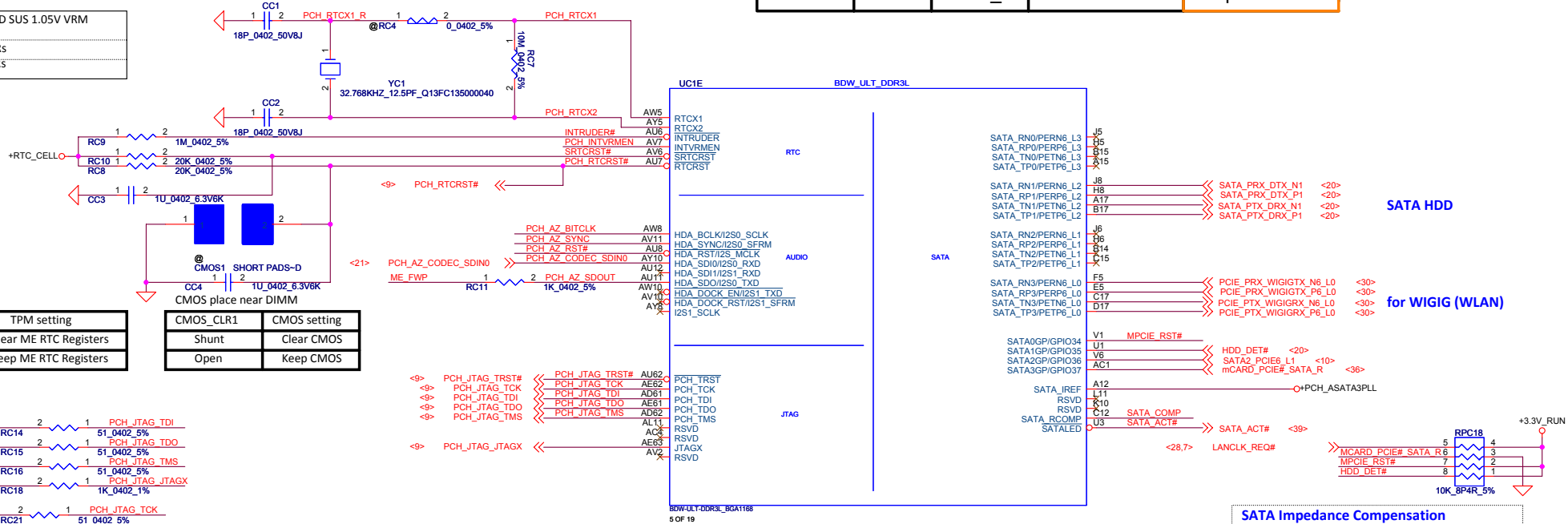


ME_FWP PCH has internal 20K PD.

FLASH DESCRIPTOR SECURITY OVERRIDE	
ME_FWP=LOW → ENABLE ME (DEFAULT)	--> Pin1 & Pin3 short
=HIGH → DISABLE ME (ME can update)	--> Pin2 & Pin3 short



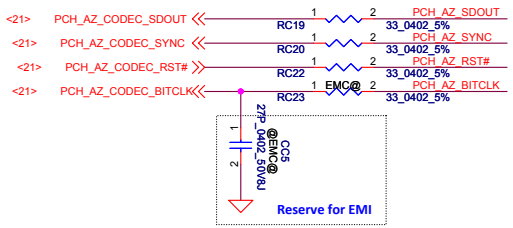
INTVRMEN - INTEGRATED SUS 1.05V VRM ENABLE
High - Enable Internal VRs
Low - Enable External VRs



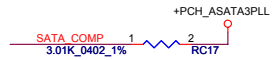
ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

HDA for Codec



SATA Impedance Compensation



CAD note:
Place the resistor within 500 mils of the PCH. Avoid routing next to clock pins.

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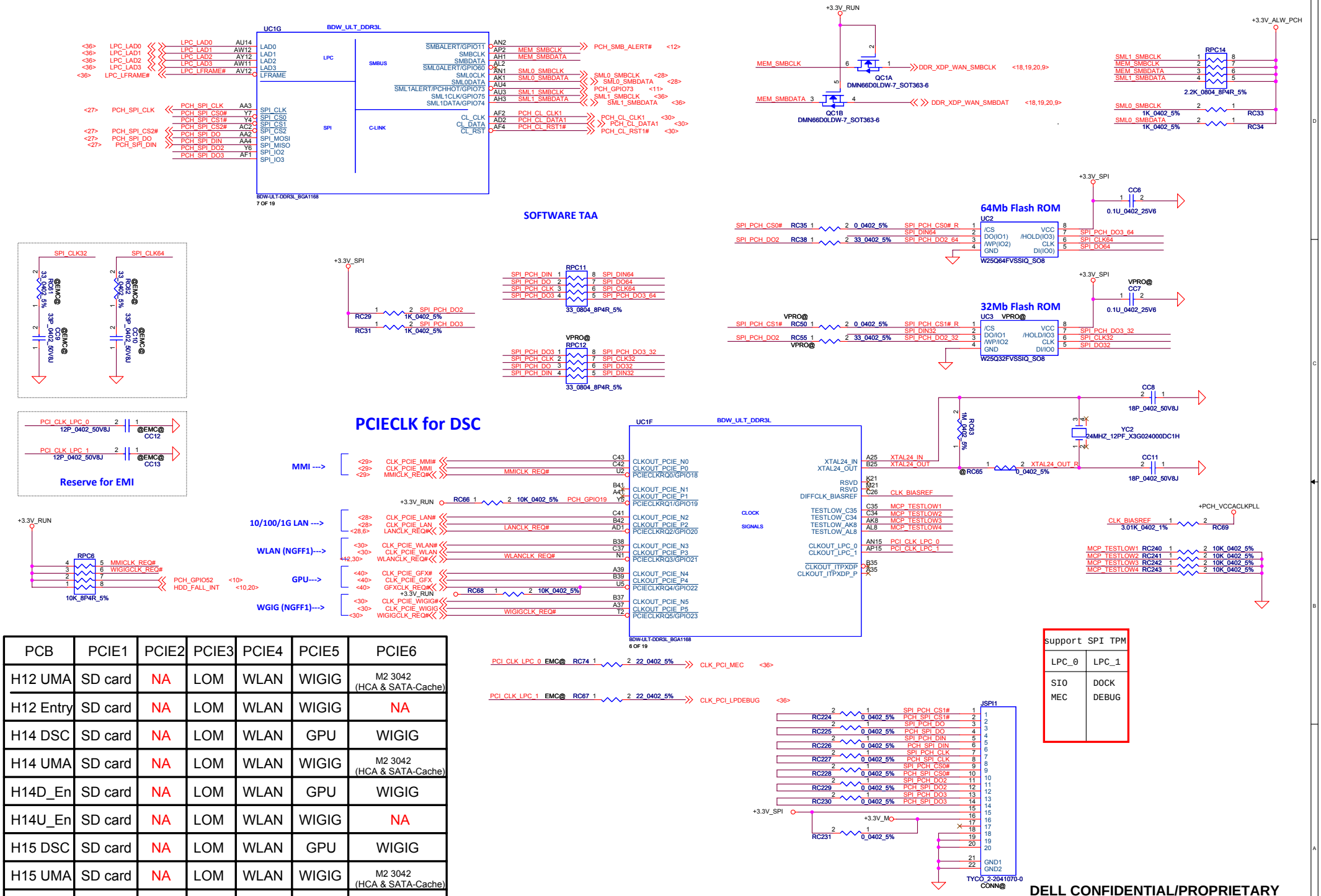

PCB	PCIE1	PCIE2	PCIE3	PCIE4	PCIE5	PCIE6
H12 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
H12 Entry	SD card	NA	LOM	WLAN	WIGIG	NA
H14 DSC	SD card	NA	LOM	WLAN	GPU	WIGIG
H14 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
H14D_En	SD card	NA	LOM	WLAN	GPU	WIGIG
H14U_En	SD card	NA	LOM	WLAN	WIGIG	NA
H15 DSC	SD card	NA	LOM	WLAN	GPU	WIGIG
H15 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
H15D_En	SD card	NA	LOM	WLAN	GPU	WIGIG
H15U_En	SD card	NA	LOM	WLAN	WIGIG	Express card

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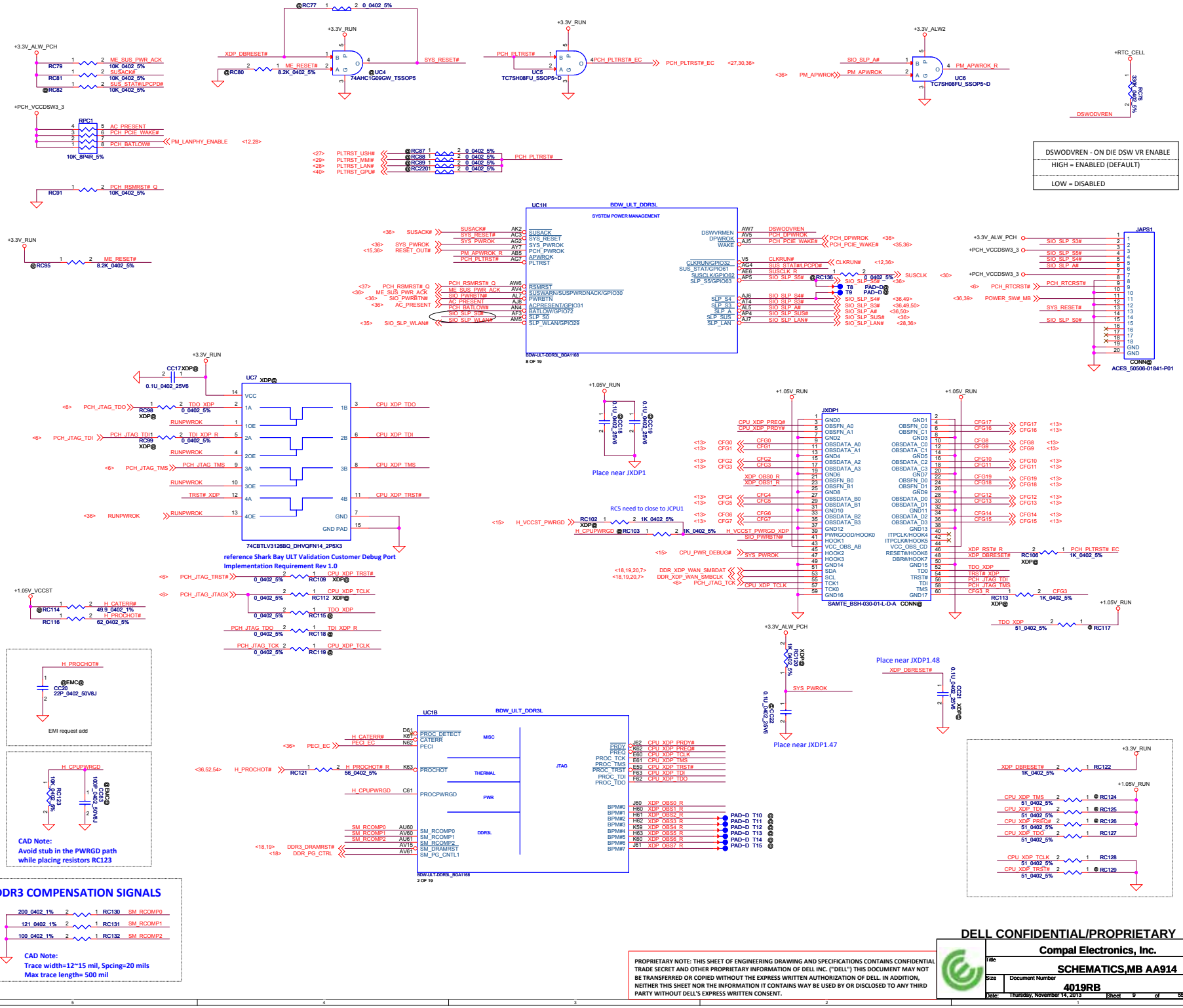
DSWODVREN - ON DIE DSW VR ENABLE
HIGH = ENABLED (DEFAULT)
LOW = DISABLED
reference Shark Bay ULT Validation Customer Debug Port Implementation Requirement Rev 1.0
Place near JXDP1
Place near JXDP1.48
Place near JXDP1.47
RC5 need to close to JCPU1
EMI request add
CAD Note: Avoid stub in the PWRGD path while placing resistors RC123
DDR3 COMPENSATION SIGNALS
CAD Note: Trace width=12~15 mil, Spcing=20 mils Max trace length= 500 mil
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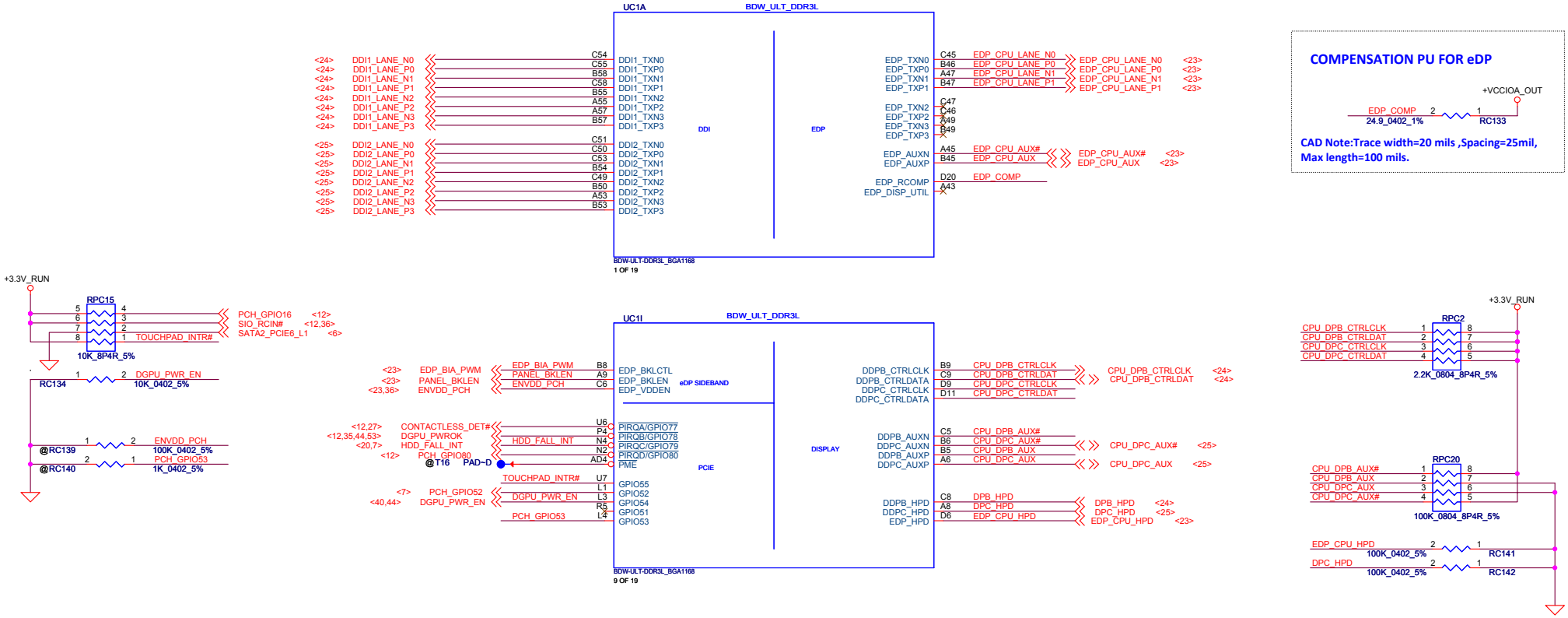

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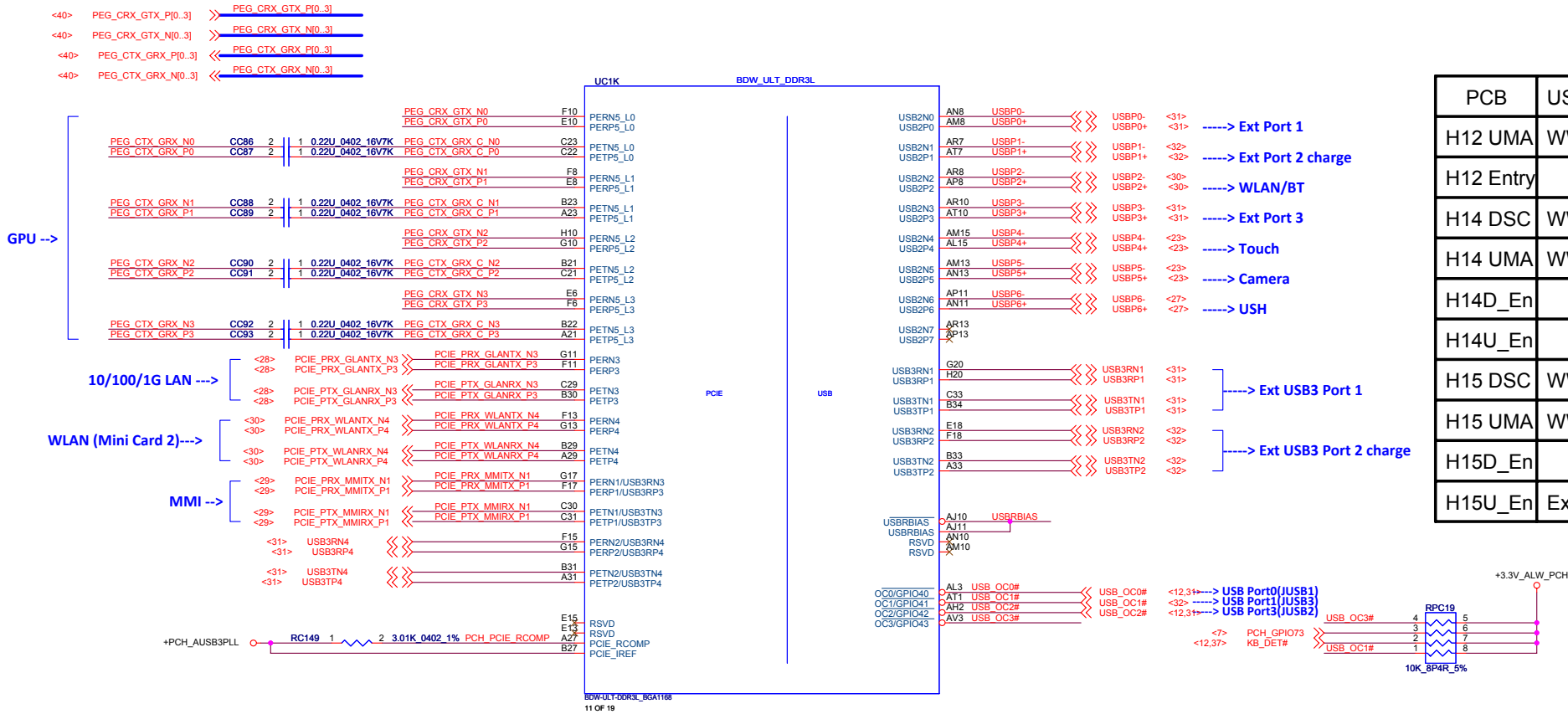

PCB	USB2 7
H12 UMA	WWAN
H12 Entry	NA
H14 DSC	WWAN
H14 UMA	WWAN
H14D_En	NA
H14U_En	NA
H15 DSC	WWAN
H15 UMA	WWAN
H15D_En	NA
H15U_En	Express

PCB	PCIE1	PCIE2	PCIE3	PCIE4	PCIE5	PCIE6
H12 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
H12 Entry	SD card	NA	LOM	WLAN	WIGIG	NA
H14 DSC	SD card	NA	LOM	WLAN	GPU	WIGIG
H14 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
H14D_En	SD card	NA	LOM	WLAN	GPU	WIGIG
H14U_En	SD card	NA	LOM	WLAN	WIGIG	NA
H15 DSC	SD card	NA	LOM	WLAN	GPU	WIGIG
H15 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
H15D_En	SD card	NA	LOM	WLAN	GPU	WIGIG
H15U_En	SD card	NA	LOM	WLAN	WIGIG	Express card

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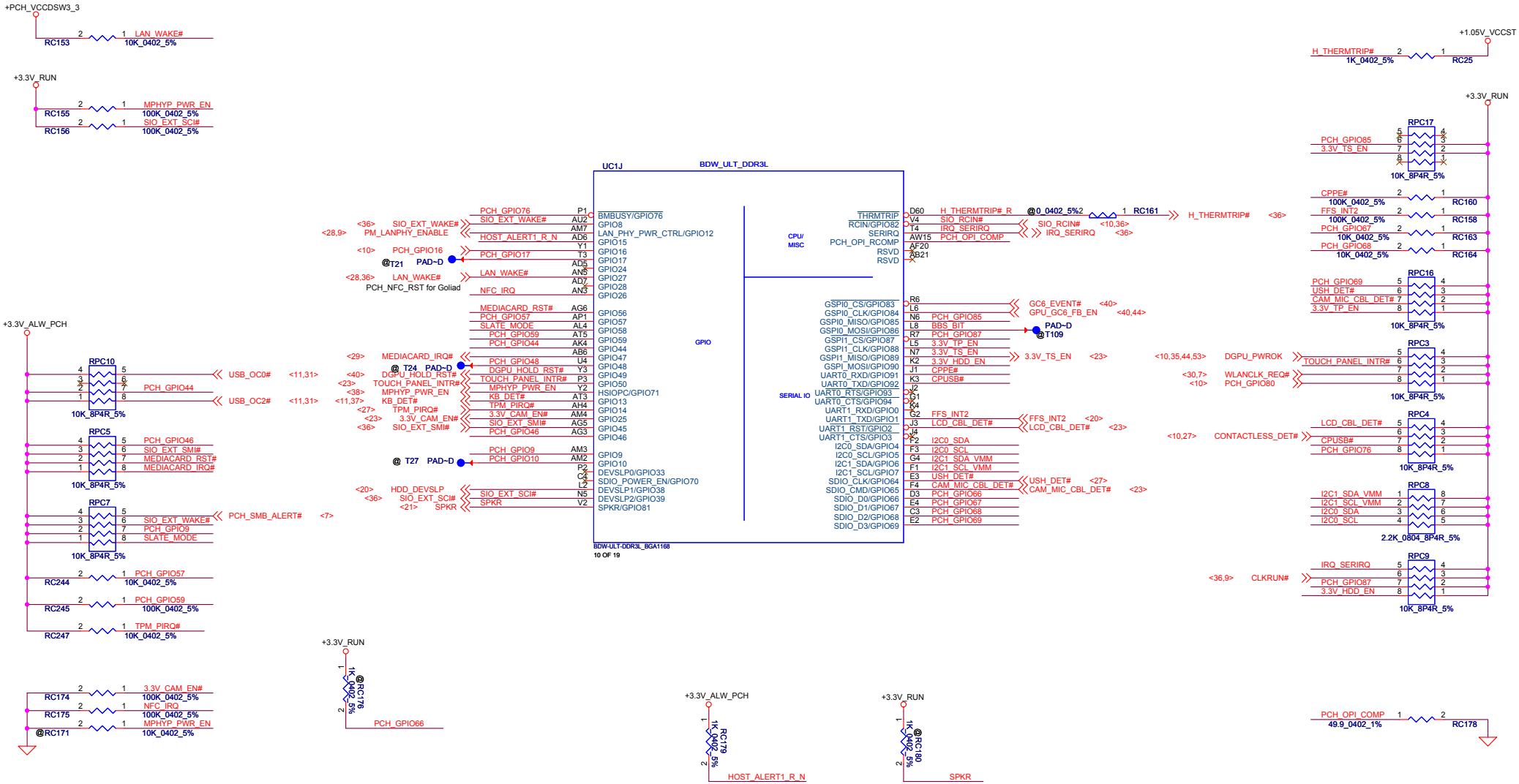

TOP-BLOCK SWAP OVERRIDE	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE

BOOT BIOS STRAP BIT BBS	
HIGH	LPC
LOW(DEFAULT)	SPI

TLS CONFIDENTIALITY	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE

No Reboot on TCO Timer expiration	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE

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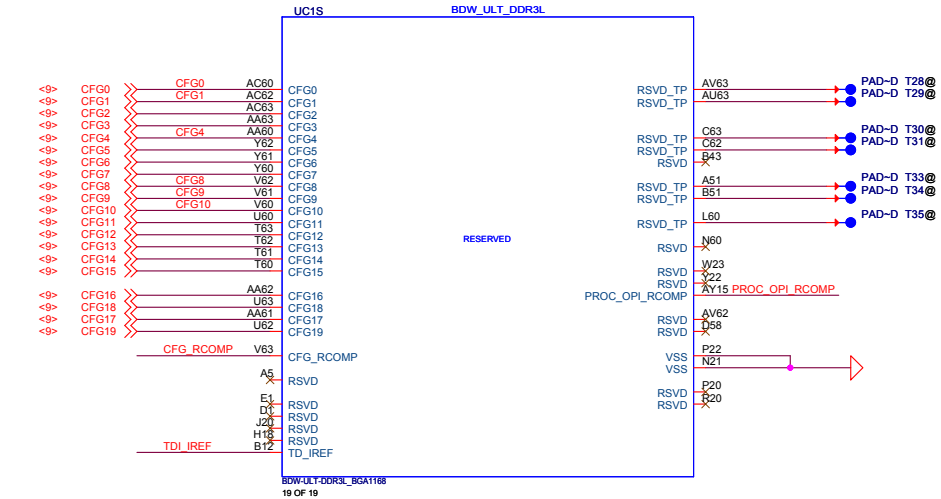
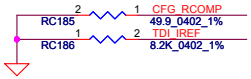
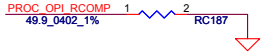
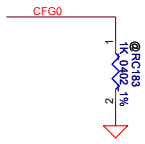
CFG STRAPS for CPU

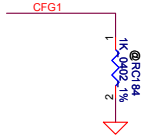




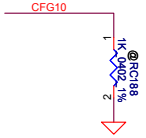


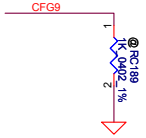


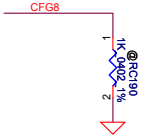
EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKE	
CFG0	1:(Default) Normal Operation; No stall 0:Lane Reversed

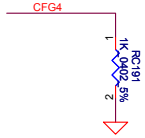


PCH/PCH LESS MODE SELECTION	
CFG1	1:(Default) Normal Operation 0:Lane Reversed









SAFE MODE BOOT	
CFG10	1: POWER FEATURES ACTIVATED DURING RESET 0: POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED

NO SVID PROTOCOL CAPABLE VR CONNECTED	
CFG9	1: VRS support SVID protocol are present 0:No VR support SVID is present The chip will not generate(OR Respond to) SVID activity

ALLOW THE USE OF NOA ON LOCKED UNITS	
CFG8	1: Enable(Default): Noa will be disable in locked units and enable in un-locked units 0: Enable Noa will be available pegardless of the locking of the unit

	Display Port Presence Strap
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port
	0 : Enabled; An external Display Port device is connected to the Embedded Display Port

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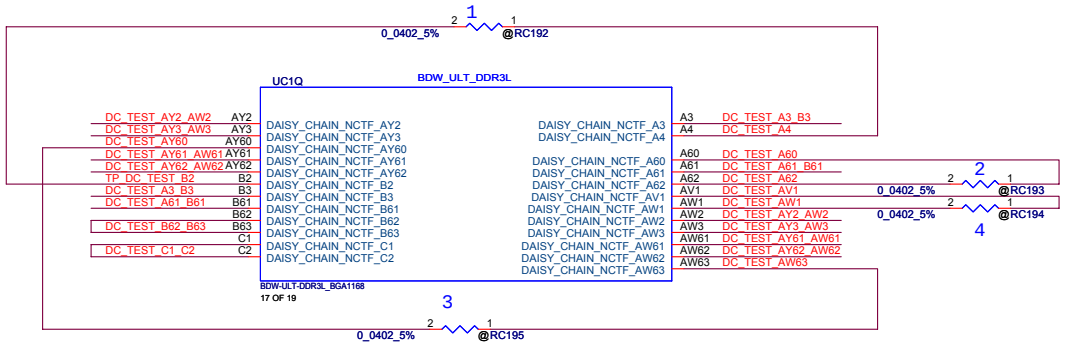


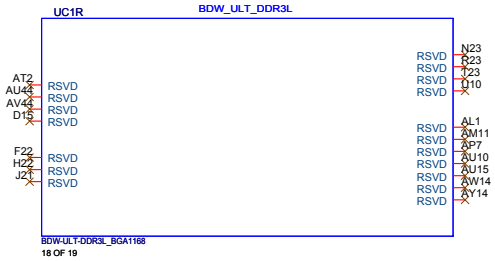
Package Daisy Chain:

1.B2-PKG-C1-PCB-C2-PKG-B3-PCB-A3-PKG-A4

2.A62-PKG-A61-PCB-B61-PKG-B62-PCB-B63-PKG-A60

3.AY60-PKG-AW61-PCB-AY61-PKG-AW62-PCB-AY62-PKG-AW63

4.AW1-PKG-AW3-PCB-AY3-PKG-AW2-PCB-AY2-PKG-AV1



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ESD Request

+1.05V_RUN
+VCCIO_OUT
@RC196
0_0603_5%

RESISTOR STUFFING OPTIONS ARE PROVIDED FOR TESTING PURPOSES

+1.05V_RUN
RC197 150_0402_1%
CPU_PWR_DEBUG#
@RC198 10K_0402_5%

+1.05V_VCCST
@RC199 10K_0402_5%
H_VR_EN
1.5K_0402_5%
RC201
H_VR_READY

+VCC_CORE
+1.35V_MEM
@EMC@ CC23 22U_0603_6.3V6M

+1.05V_RUN
+VCC_CORE
@EMC@ CC79 22U_0603_6.3V6M
@EMC@ CC84 22U_0603_6.3V6M

+1.05V_RUN
+3.3V_RUN
@EMC@ CC85 22U_0603_6.3V6M

H_VCCST_PWRGD
@EMC@
CC24
100P_0402_50V8J

+1.35V_MEM
VDDQ DECOUPLING
2.2U_0402_6.3V6M CC25
2.2U_0402_6.3V6M @CC26
2.2U_0402_6.3V6M CC27
2.2U_0402_6.3V6M CC28
10U_0603_6.3V6M CC29
10U_0603_6.3V6M @CC30
10U_0603_6.3V6M CC31
10U_0603_6.3V6M CC32
10U_0603_6.3V6M @CC33
10U_0603_6.3V6M CC34

+1.05V_VCCST
+3.3V_ALW
UC8
NC
VCC
A
Y
GND
74AUP1G07GW_TSSOP5
@CC35 0.1U_0402_25V6
1K_0402_5% RC202
<36,9> RESET_OUT#
H_VCCST_PWRGD

SVID ALERT
+1.05V_VCCST
RC204 75_0402_1%
CAD Note: Place the PU resistors close to CPU RC204 close to CPU 300 - 1500mils
<52> VIDALERT_N
43_0402_5%
RC207
H_CPU_SVIDALRT#

SVID DATA
+1.05V_VCCST
RC208 110_0402_1%
CAD Note: Place the PU resistors close to CPU RC208close to CPU 300 - 1500mils
<52> VIDSOUT
VIDSOUT

VCC_SENSE
+VCC_CORE
RC209 100_0402_1%
<52> VCCSENSE
VCCSENSE
CAD Note: RC209 SHOULD BE PLACED CLOSE TO CPU

UC1L
BDW_ULT_DDR3L
HSW ULT POWER
BDW-ULT-DDR3L_BGA1168
12 OF 19

+1.35V_MEM
+VCC_CORE
+VCCIO_OUT
+VCCIOA_OUT
+1.05V_VCCST
<52> VIDSCLK
<9> H_VCCST_PWRGD
<52> H_VR_EN
<52> H_VR_READY
<9> CPU_PWR_DEBUG#
@T74 PAD~D
@T75 PAD~D
@T76 PAD~D
@T77 PAD~D

+1.05V_RUN
@PJP23
PAD-OPEN1x1m
+1.05V_VCCST
CC36 22U_0603_6.3V6M
@CC37 1U_0402_6.3V6K

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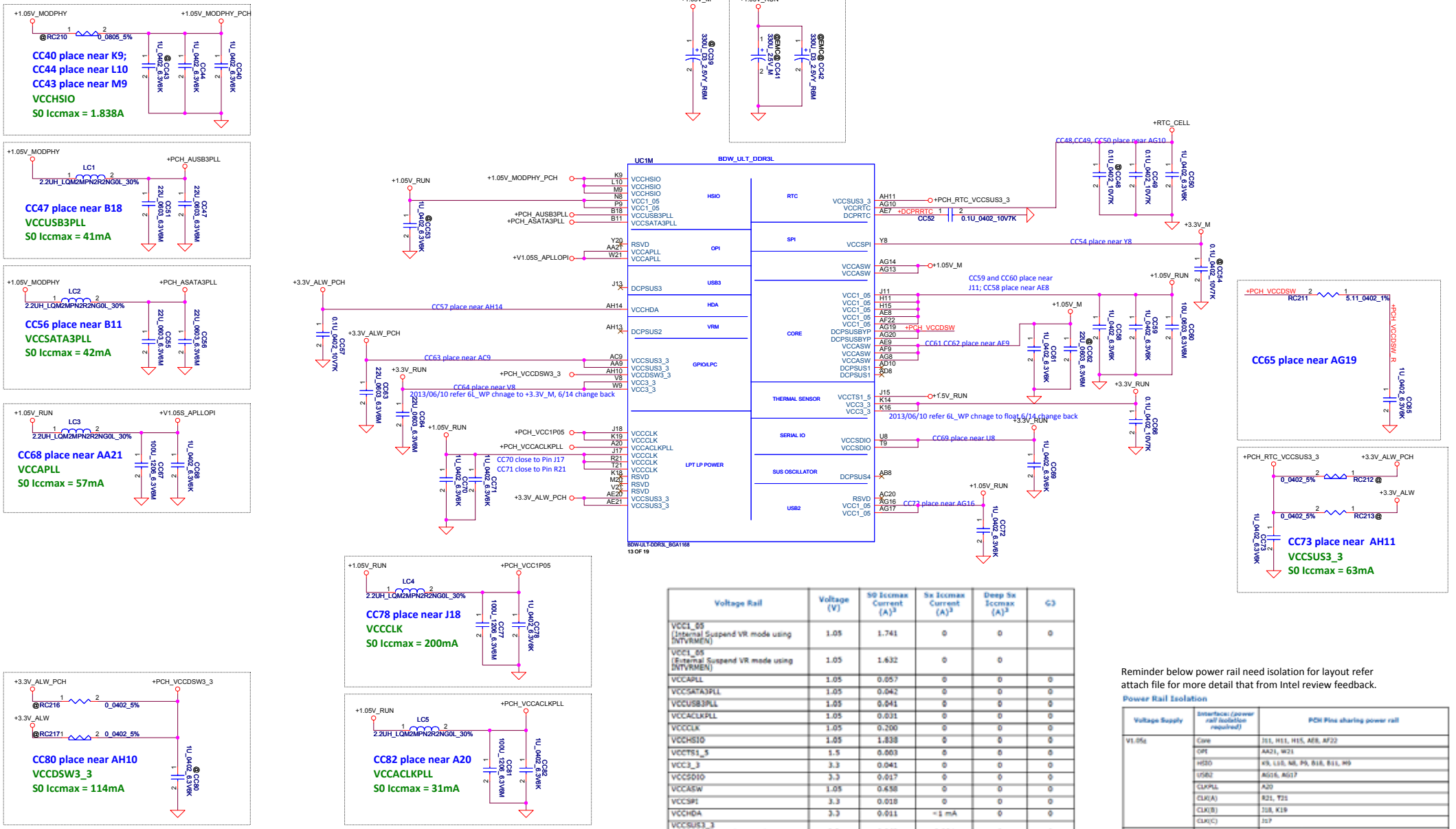

Voltage Rail	Voltage (V)	S0 Iccmax Current (A)[3]	Sx Iccmax Current (A)[3]	Deep Sx Iccmax (A)[3]	G3
VCC1_05 (Internal Suspend VR mode using INTVRMEN)	1.05	1.741	0	0	0
VCC1_05 (External Suspend VR mode using INTVRMEN)	1.05	1.632	0	0	
VCCAPLL	1.05	0.057	0	0	0
VCCSATA3PLL	1.05	0.042	0	0	0
VCCUSB3PLL	1.05	0.041	0	0	0
VCCACLKPLL	1.05	0.031	0	0	0
VCCCLK	1.05	0.200	0	0	0
VCCHSIO	1.05	1.838	0	0	0
VCCTS1_5	1.5	0.003	0	0	0
VCC3_3	3.3	0.041	0	0	0
VCCSDIO	3.3	0.017	0	0	0
VCCASW	1.05	0.458	0	0	0
VCCSPI	3.3	0.018	0	0	0
VCCHDA	3.3	0.011	<1 mA	0	0
VCCSUS3_3 (Internal Suspend VR mode using INTVRMEN)	3.3	0.063	0.024	0	0
VCCSUS3_3 (External Suspend VR mode using INTVRMEN)	3.3	0.062	0.005	0	0
DcpSus1[4]	1.05	0.109	0.014	0	0
DcpSus2[4]	1.05	0.025	0.001	0	0
DcpSus3[4]	1.05	0.010	0.003	0	0
DcpSus4[4]	1.05	0.001	0.001	0	0
VCCDSW3_3	3.3	0.114	0.004	0.002	0
VCCRTC	3.3	<1 mA	<1 mA	<1 mA	6 µA See notes 1, 2

Reminder below power rail need isolation for layout refer attach file for more detail that from Intel review feedback.

Power Rail Isolation

Voltage Supply	Interfaces (power rail isolation required)	PCH Pins sharing power rail
V1.05[4]	Core	J11, H11, H15, AE8, AF22
	OPI	AA21, W21
	HSIO	K9, L10, M8, P9, B18, B11, M9
	USB2	AG16, AG17
	CLK(A)	AJ20
	CLK(A)	R21, T21
	CLK(B)	J18, K19
	CLK(C)	J17
V3.3[4]	GPIO	AC9, AA9, AE10, AE21
	RTC	AH11
	HDA	AH14
V3.3[4]	GPIO	V8, W9
	SDIO	U8, T9
	Thermal Sensor	K14, K16

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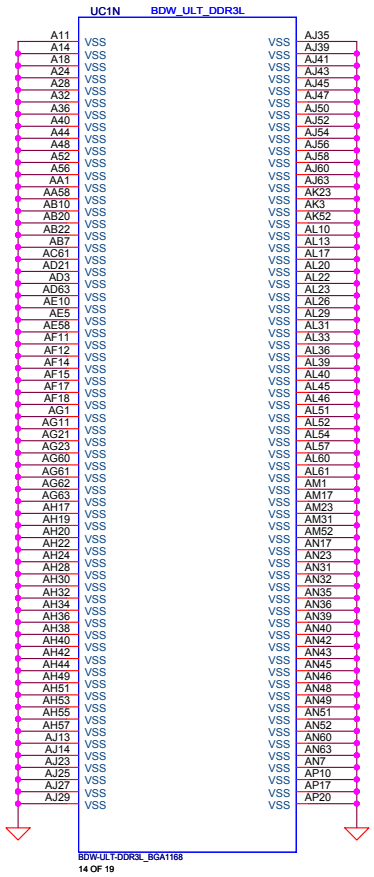

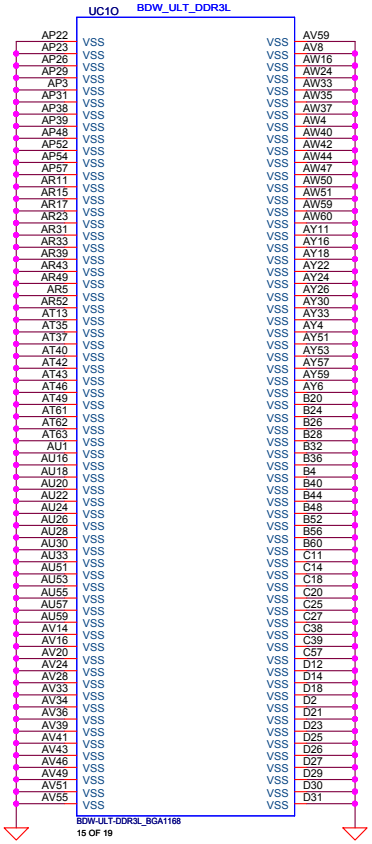

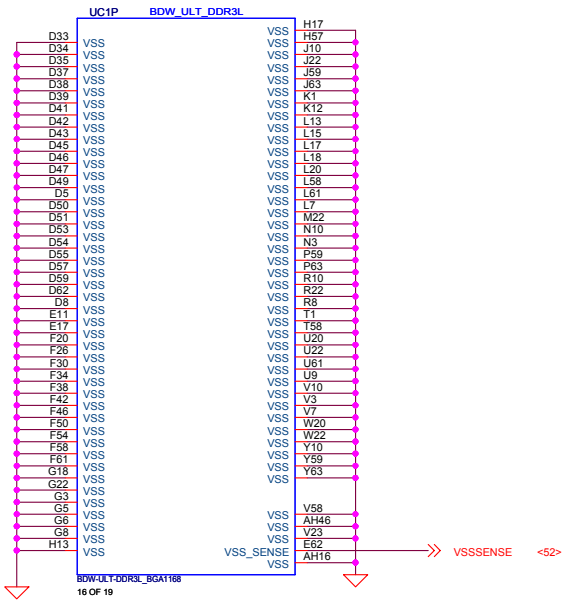

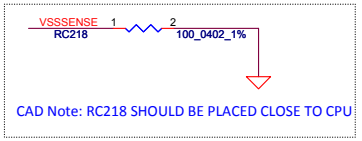

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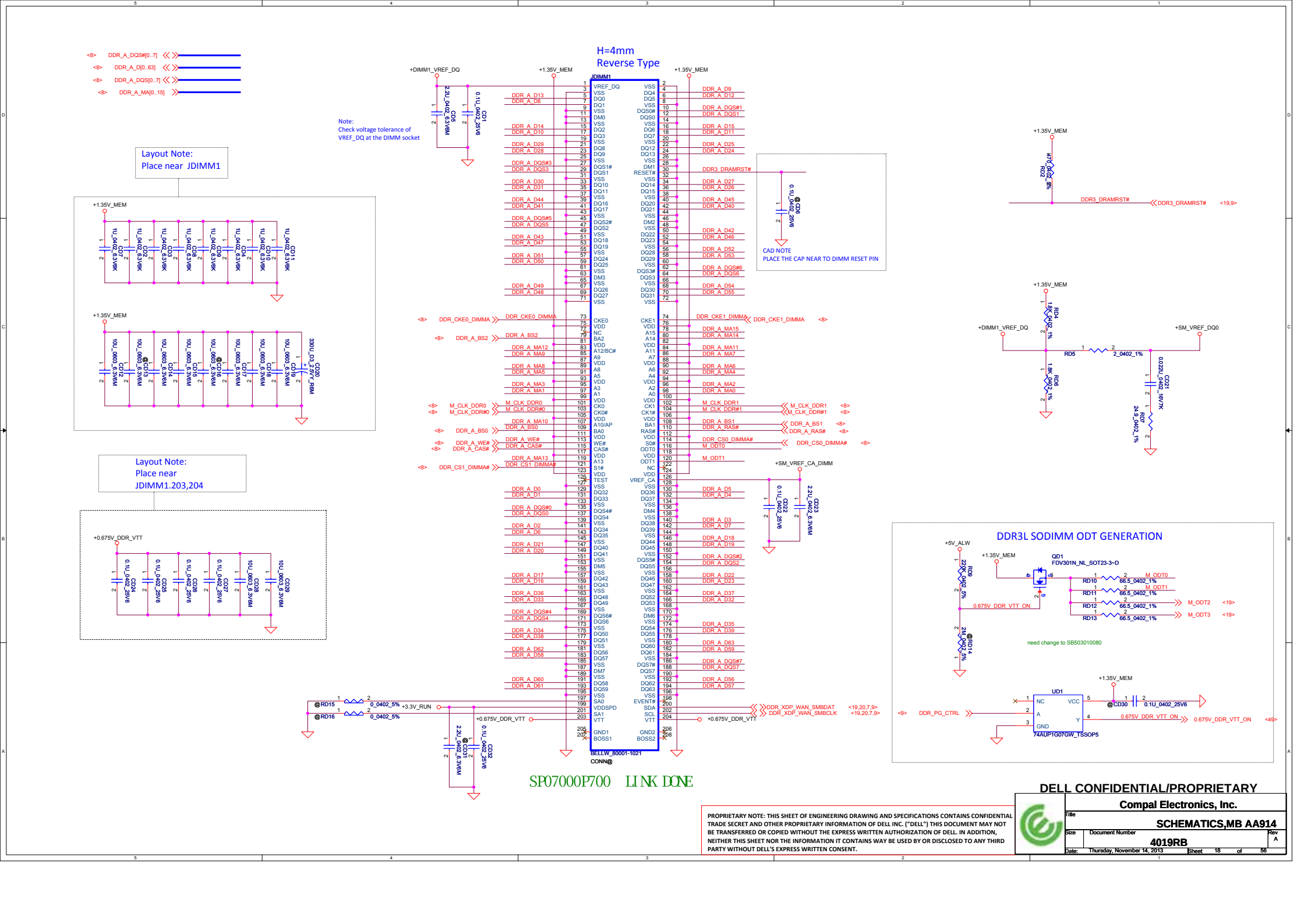
H=4mm
Reverse Type
JDIMM1
Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket
Layout Note:
Place near JDIMM1
Layout Note:
Place near
JDIMM1.203,204
CAD NOTE
PLACE THE CAP NEAR TO DIMM RESET PIN
DDR3L SODIMM ODT GENERATION
need change to SB503010080
SP07000P700 LINK DONE
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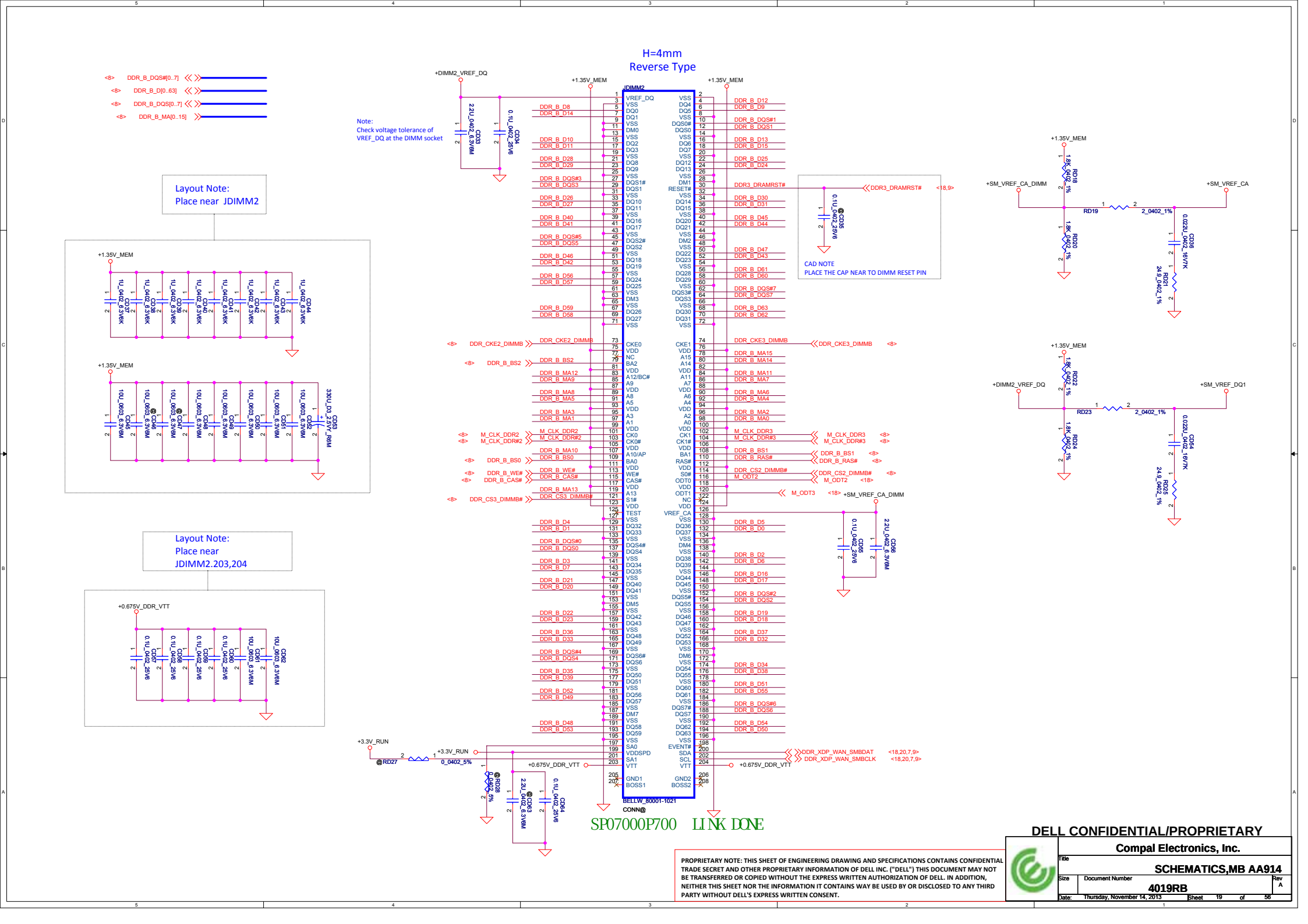
H=4mm
Reverse Type
JDIMM2
Note:
Check voltage tolerance of VREF_DQ at the DIMM socket
Layout Note:
Place near JDIMM2
Layout Note:
Place near
JDIMM2.203,204
CAD NOTE
PLACE THE CAP NEAR TO DIMM RESET PIN
BELLW_80001-1021
CONN@
SP07000P700 LINK DONE
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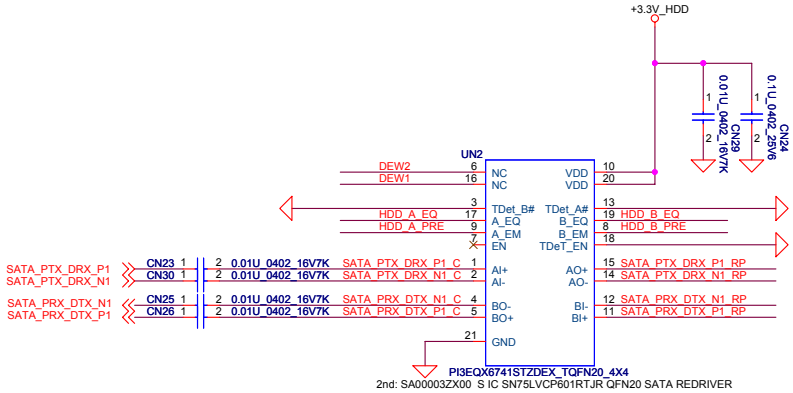
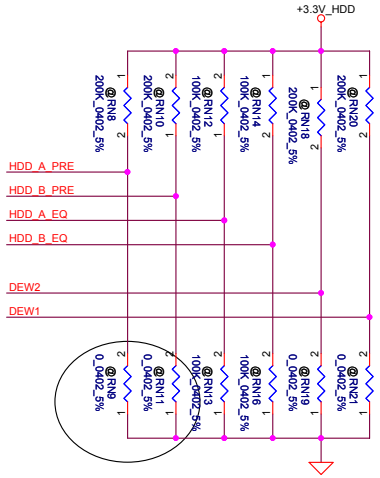
SATA Repeater

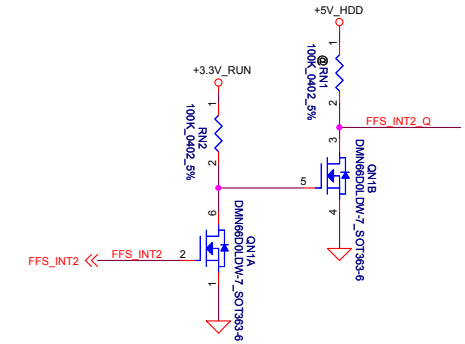


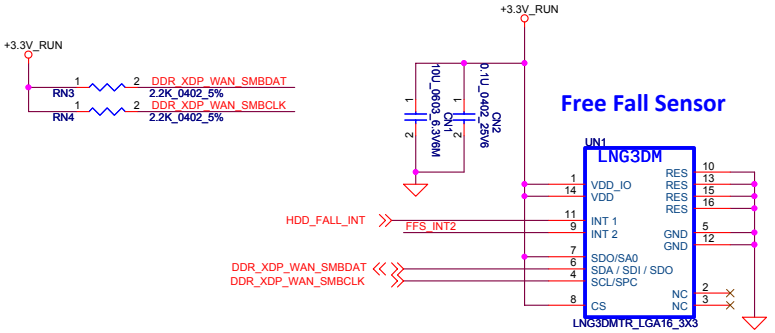
2nd: SA00003ZX00 S IC SN75LVCP601RTJR QFN20 SATA REDRIVER

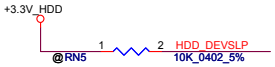
PERICOM PI3EQX6741ST:
Pin6/16, NC
Pin8/9, Pre-emphasis

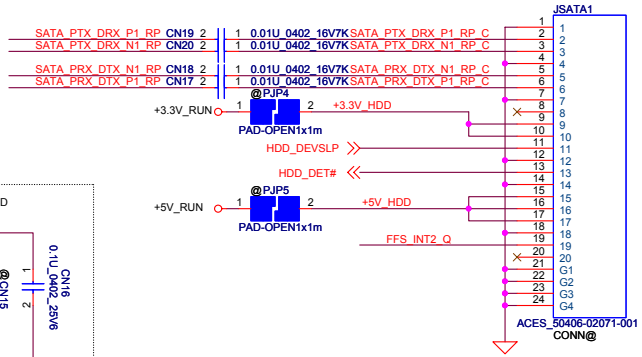
TI SN75LVCP601RTJR
Pin6/16, de-emphasis width setup
Pin8/9, de-emphasis

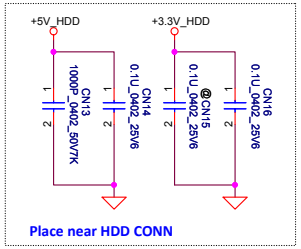












SP010016L00 LINK DONE

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SP02000W00 LINK DONE

1W x 1ch, 4ohm (Transducer spec is 8Ohm/0.5Watt per unit, there are two transducer units in one speaker box.)

Internal Speakers Header

40 mils trace keep 20 mil spacing

CONN@ JSPK1
ACES_50279-0040N-001

Close to U17

Close to U17 pin6

Verb table configures as 1 JD mode with internal 47K pull high to save external rBOM.

Place closely to Pin 13.

Add for solve pop noise and detect issue

place at AGND and DGND plane

Digital Mic

MIC1
SPM1437HM4H-6_6P

Realtek feedback
Prevent the Noise from Combo Jack while system entry into S3 / S4 /S5

UA1
ALC3235-CG_MQFN48_6X6

BCLK: Audio serial data bus bit clock input/output
LRCK: Audio serial data bus word clock input/output

Place CA29 close to Codec

Global Headset
Combo Jack

HP-Out-Right
HP-Out-Left
Nokia-MIC
iPhone-MIC

CONN@ JAUD1
E-T_6705K-Y12N-40L

6705K-Y12N-40L LINK DONE

EMI De-pop

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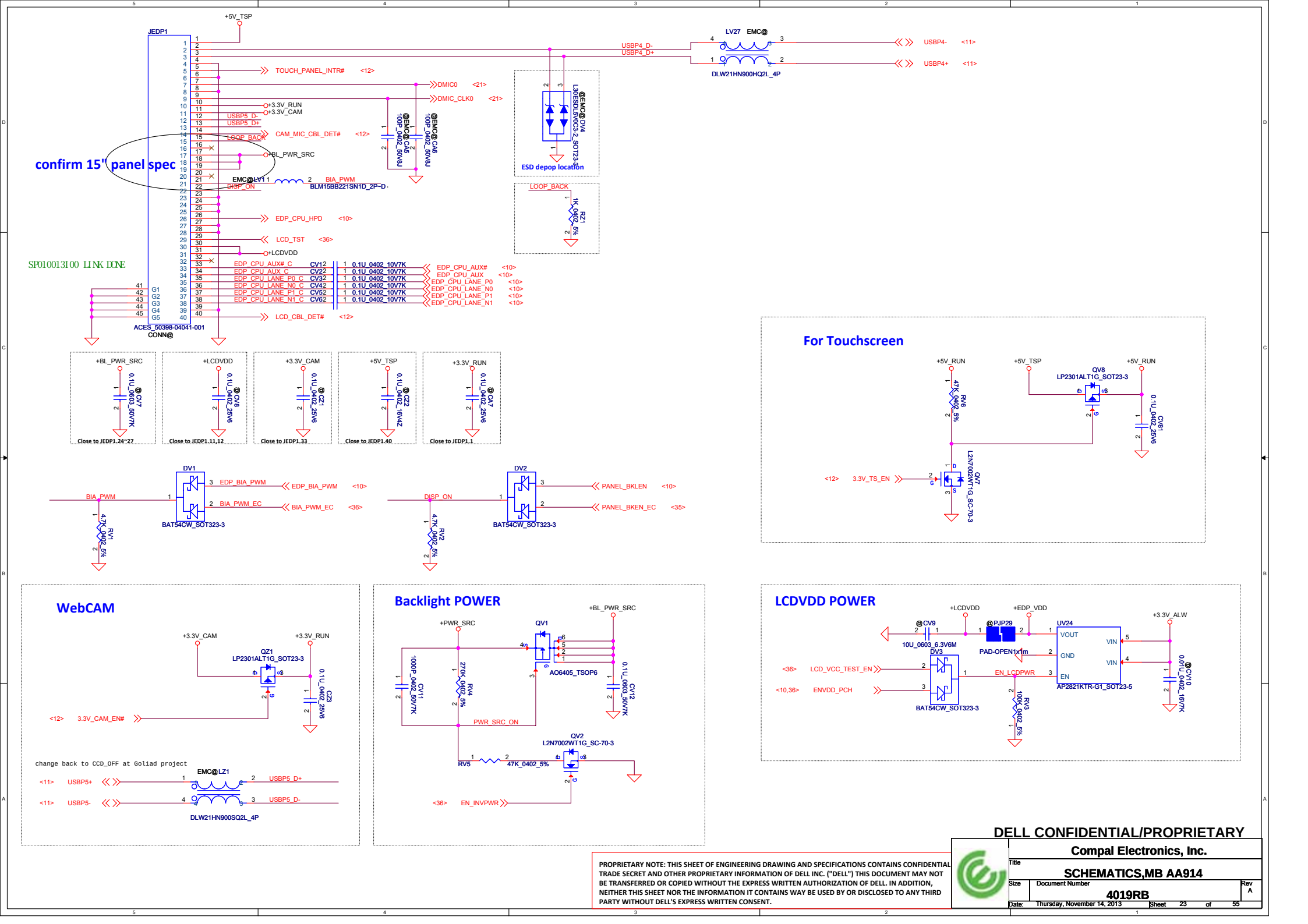

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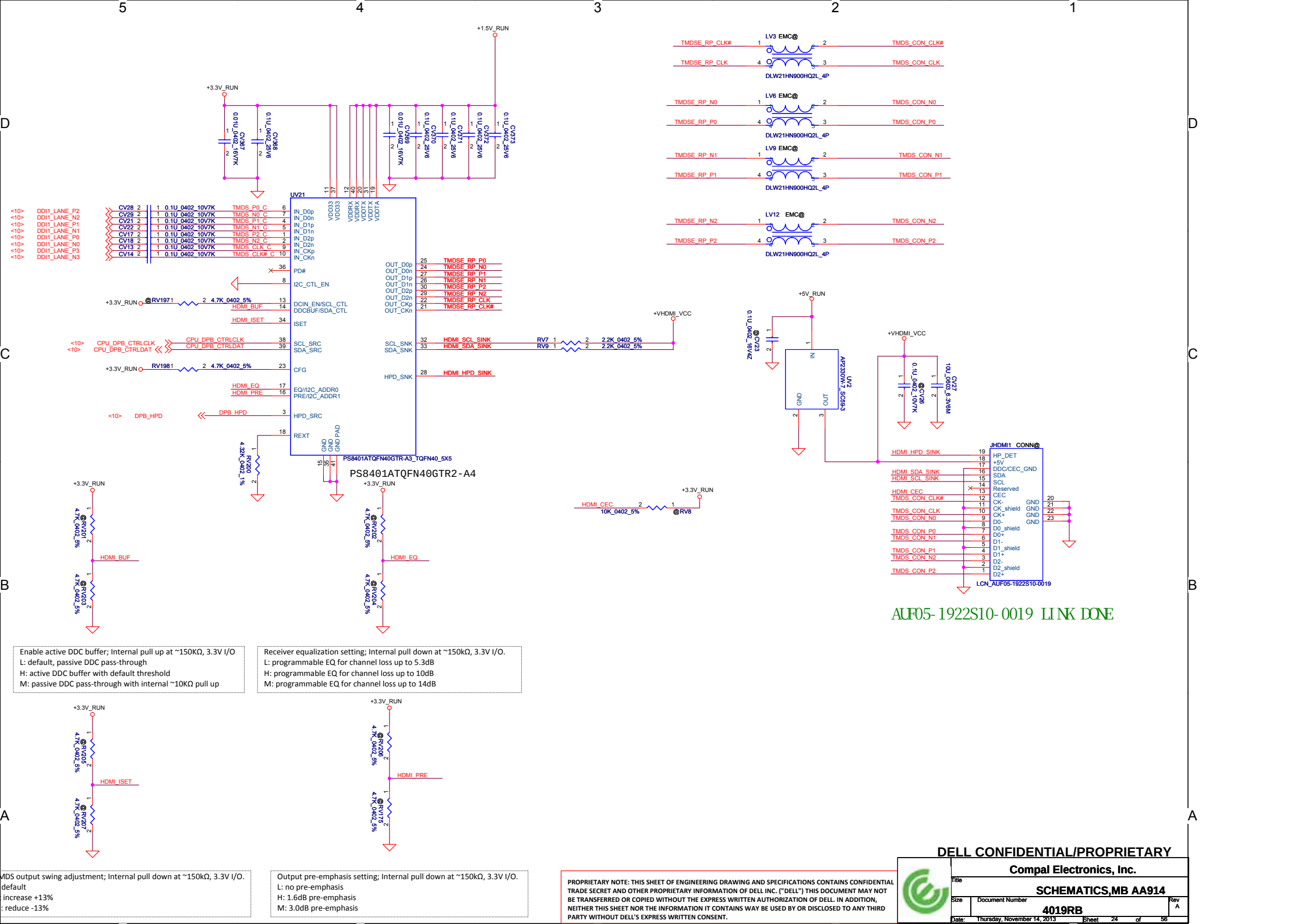
+1.5V_RUN
+3.3V_RUN
UV21
PS8401ATQFN40GTR-A4
PS8401ATQFN40GTR-A3_TQFN40_5X5
LV3 EMC@
LV6 EMC@
LV9 EMC@
LV12 EMC@
DLW21HN900HQ2L_4P
TMDSE_RP_CLK#
TMDSE_RP_CLK
TMDSE_RP_N0
TMDSE_RP_P0
TMDSE_RP_N1
TMDSE_RP_P1
TMDSE_RP_N2
TMDSE_RP_P2
TMDS_CON_CLK#
TMDS_CON_CLK
TMDS_CON_N0
TMDS_CON_P0
TMDS_CON_N1
TMDS_CON_P1
TMDS_CON_N2
TMDS_CON_P2
+5V_RUN
+VHDMI_VCC
LV2
AP2330W7_SC593
JHDMI1_CONN@
LCN_AUF05-1922S10-0019
HDMI_HPD_SINK
HDMI_SDA_SINK
HDMI_SCL_SINK
HDMI_CEC
HDMI_BUF
HDMI_EQ
HDMI_ISET
HDMI_PRE
DPB_HPD
CPU_DPB_CTRLCLK
CPU_DPB_CTRLDAT
AUF05-1922S10-0019 LINK DONE
Enable active DDC buffer; Internal pull up at ~150KΩ, 3.3V I/O
L: default, passive DDC pass-through
H: active DDC buffer with default threshold
M: passive DDC pass-through with internal ~10KΩ pull up
Receiver equalization setting; Internal pull down at ~150kΩ, 3.3V I/O.
L: programmable EQ for channel loss up to 5.3dB
H: programmable EQ for channel loss up to 10dB
M: programmable EQ for channel loss up to 14dB
MDS output swing adjustment; Internal pull down at ~150kΩ, 3.3V I/O.
default
increase +13%
reduce -13%
Output pre-emphasis setting; Internal pull down at ~150kΩ, 3.3V I/O.
L: no pre-emphasis
H: 1.6dB pre-emphasis
M: 3.0dB pre-emphasis
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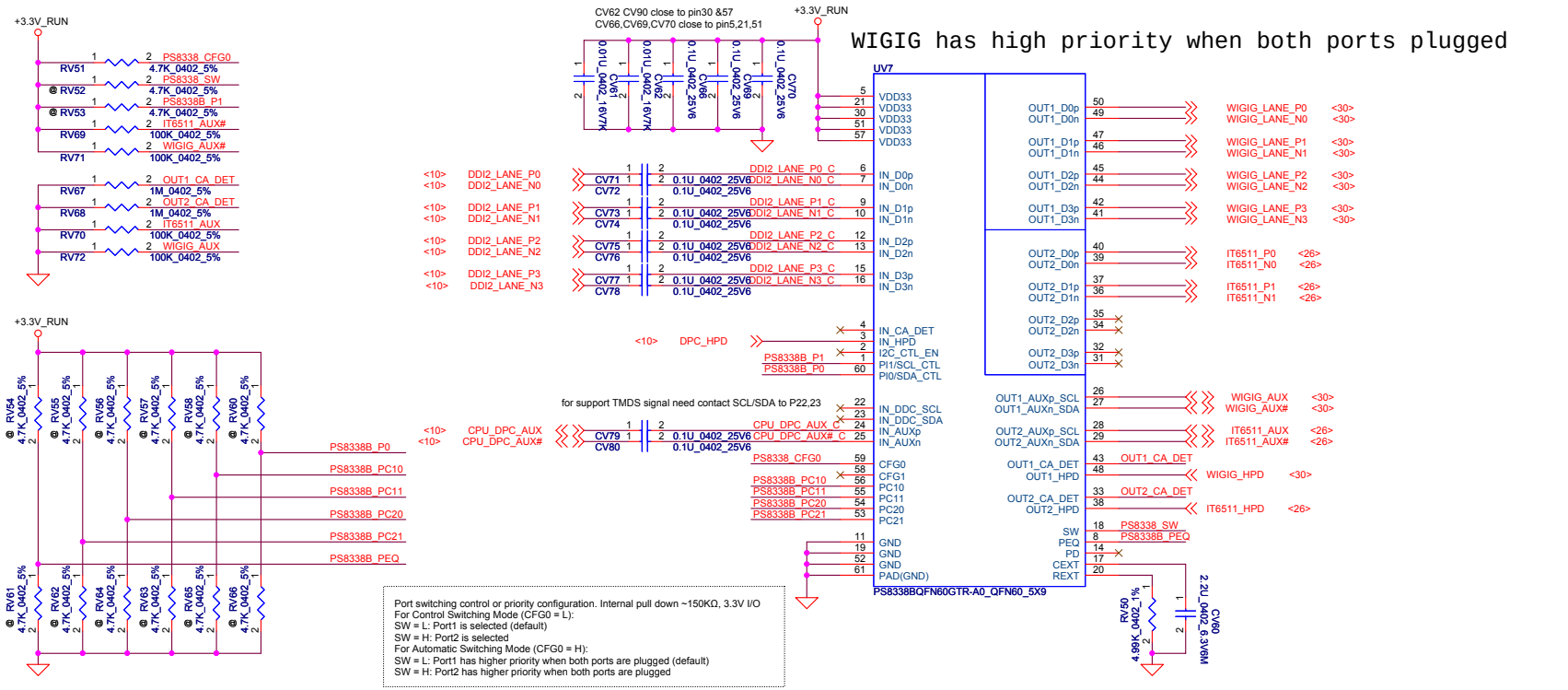
12" use 8339
14"/15" use 8338 at DOCK config
14"/15" use 12412 at Entry config

PCB	DP SWITCH
H12 UMA	PS8339+DP12412
H12 Entry	PS8339
H14 DSC	PS8338
H14 UMA	PS8338
H14D_En	DP12412
H14U_En	DP12412
H15 DSC	PS8338
H15 UMA	PS8338
H15D_En	DP12412
H15U_En	DP12412



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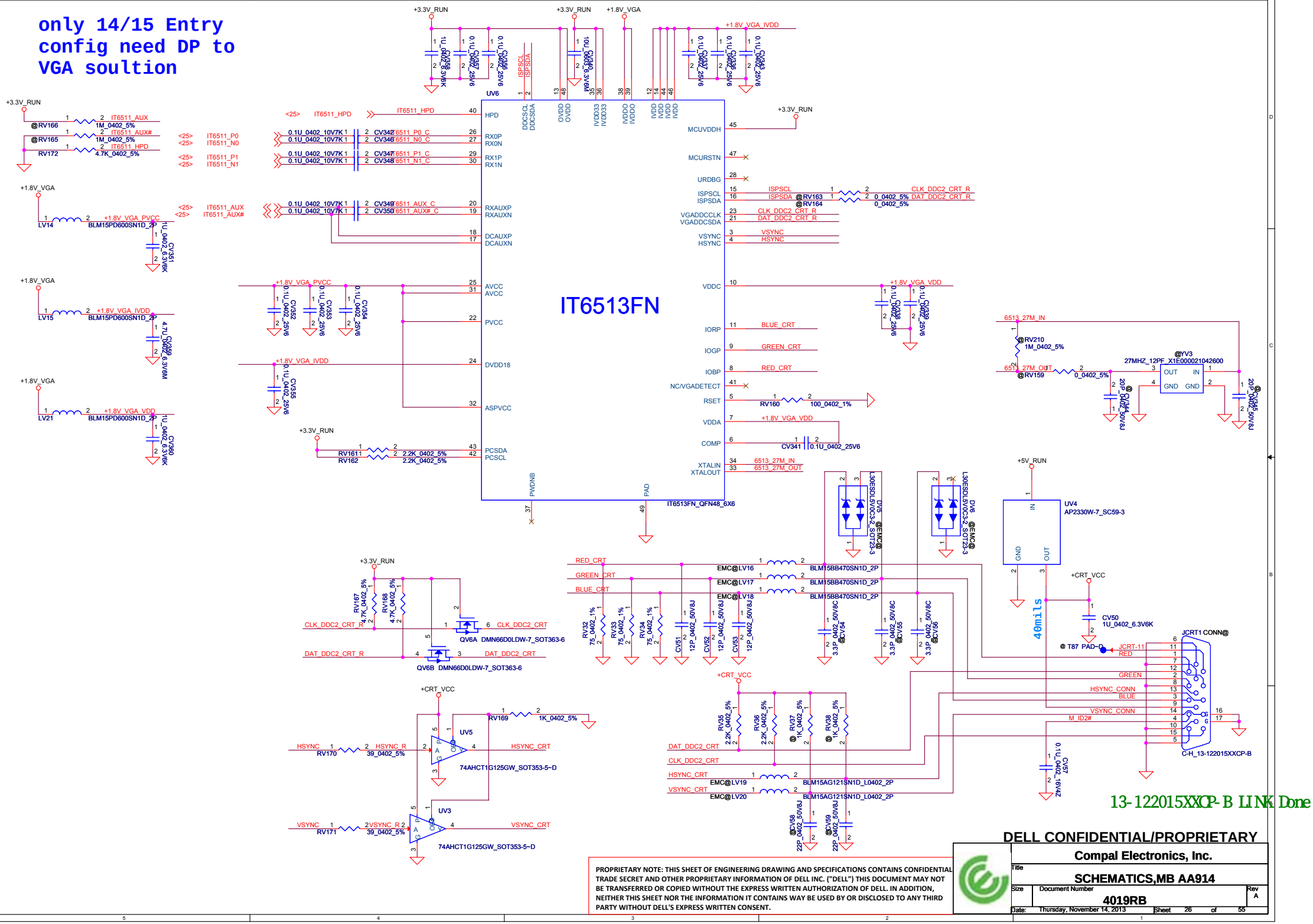
only 14/15 Entry config need DP to VGA soultion



13-122015XXCP-B LINK Done

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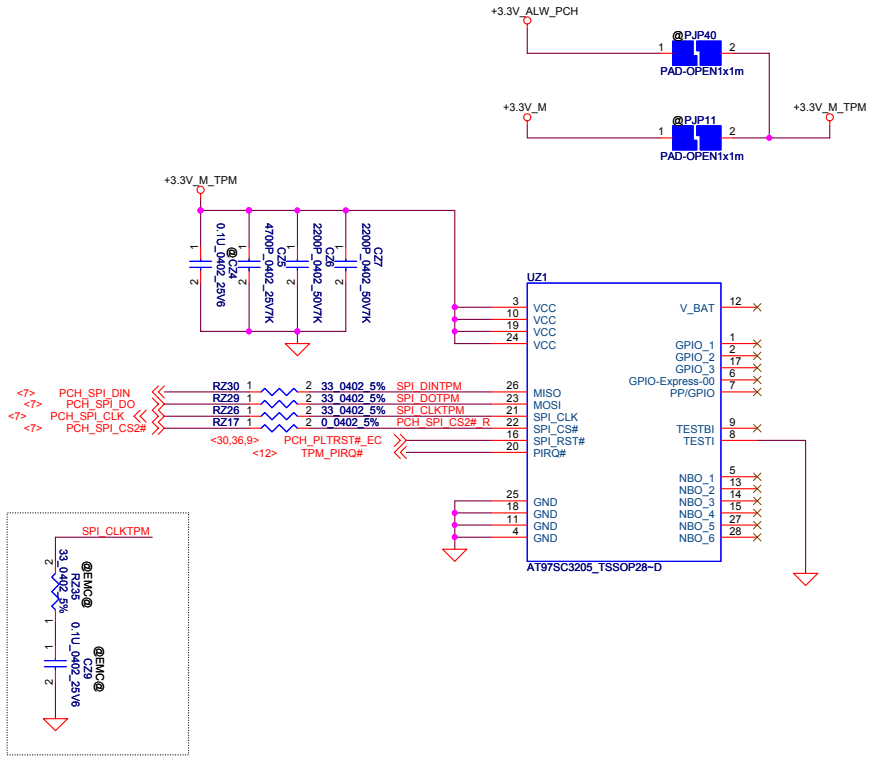
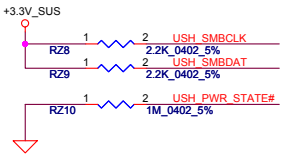
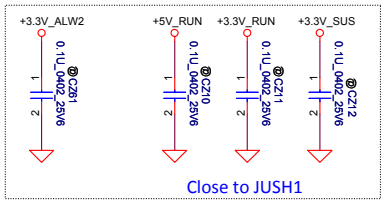
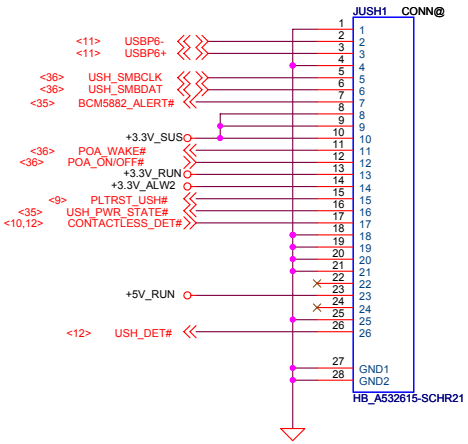






USH CONN



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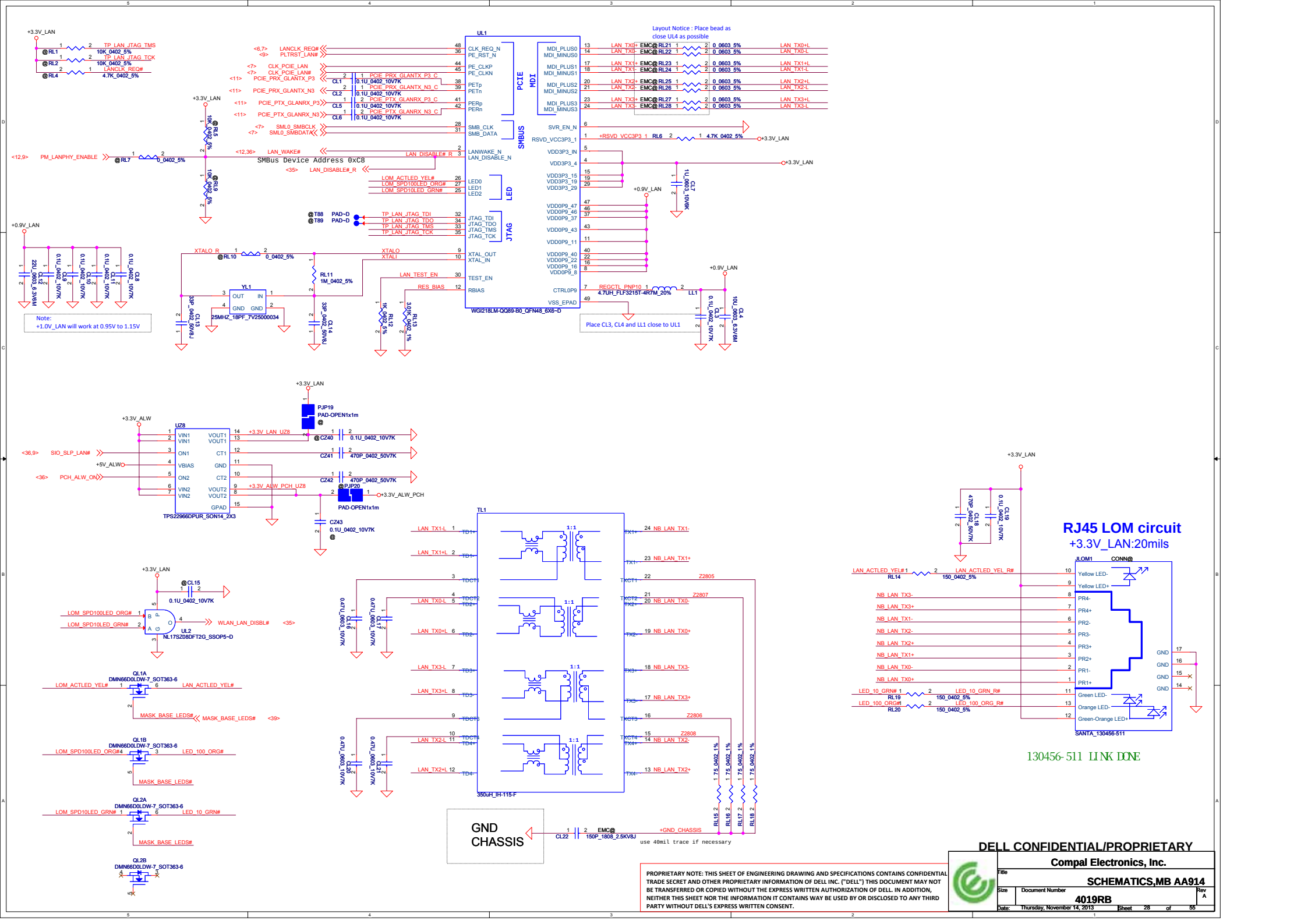

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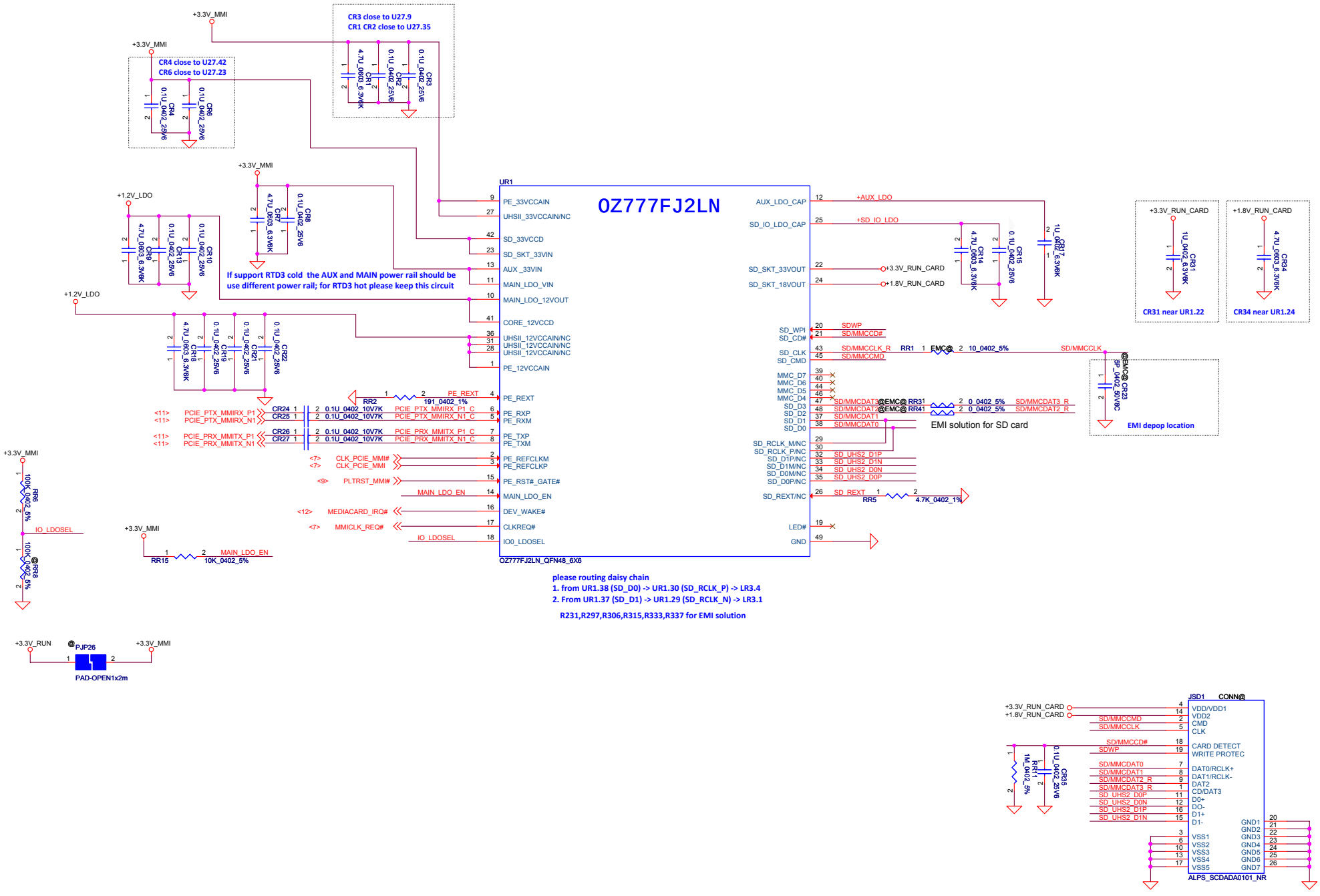

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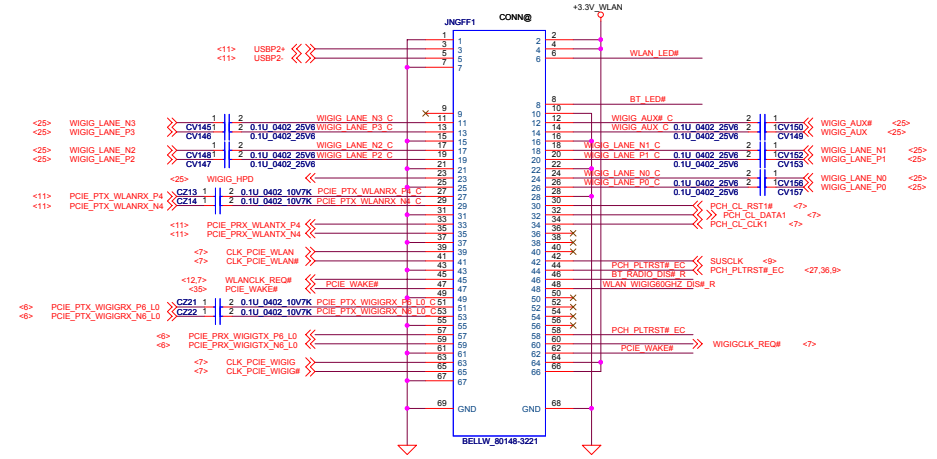
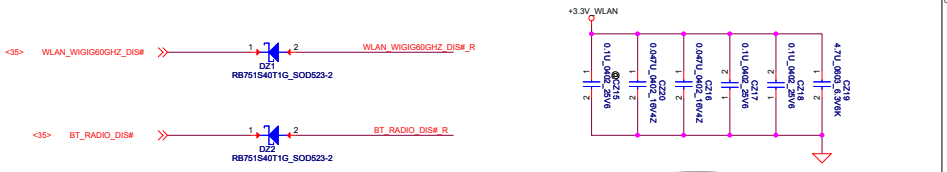
NGFF for DSC

NGFF slot A Key A



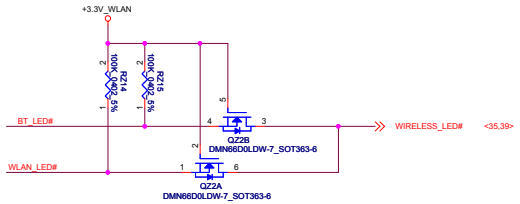
80148-3221 LINK DONE



Power Rating TBD

PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V				

LED control circuit



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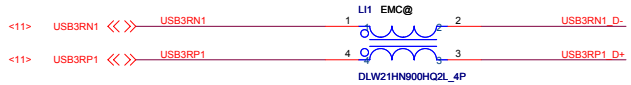
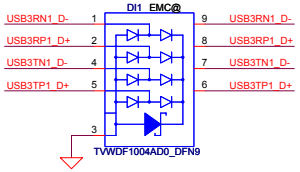
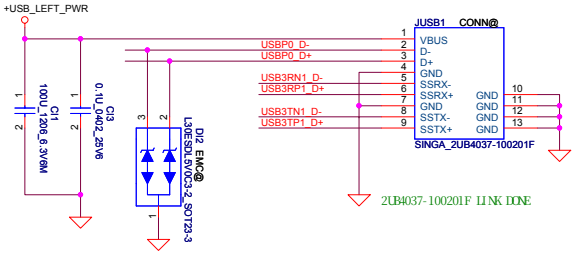
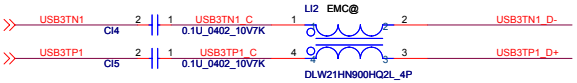
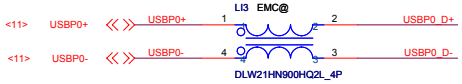
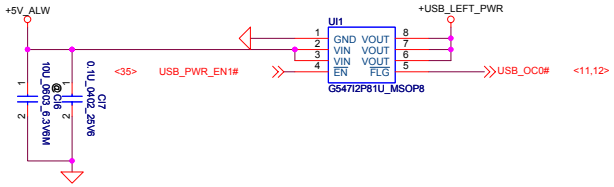




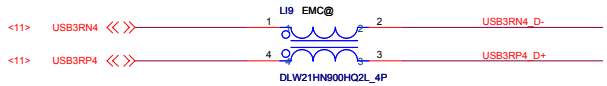


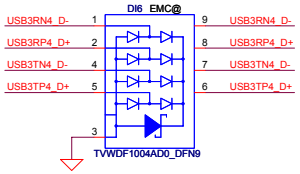


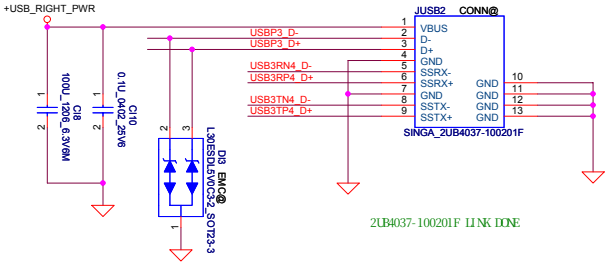


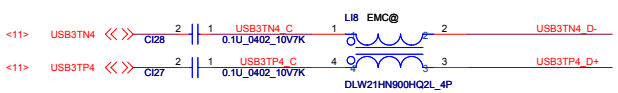


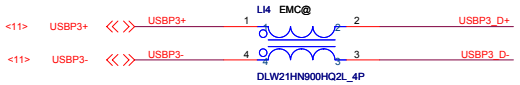
PCB	USB2 0	USB2 3
H12 UMA	USB3102	NX3DV221
H12 Entry	NA	NA
H14 DSC	USB3102	NX3DV221
H14 UMA	USB3102	NX3DV221
H14D_En	NA	NA
H14U_En	NA	NA
H15 DSC	USB3102	NX3DV221
H15 UMA	USB3102	NX3DV221
H15D_En	NA	NA
H15U_En	NA	NA

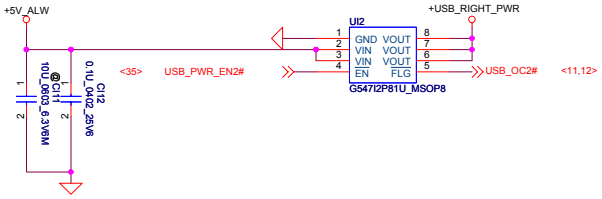












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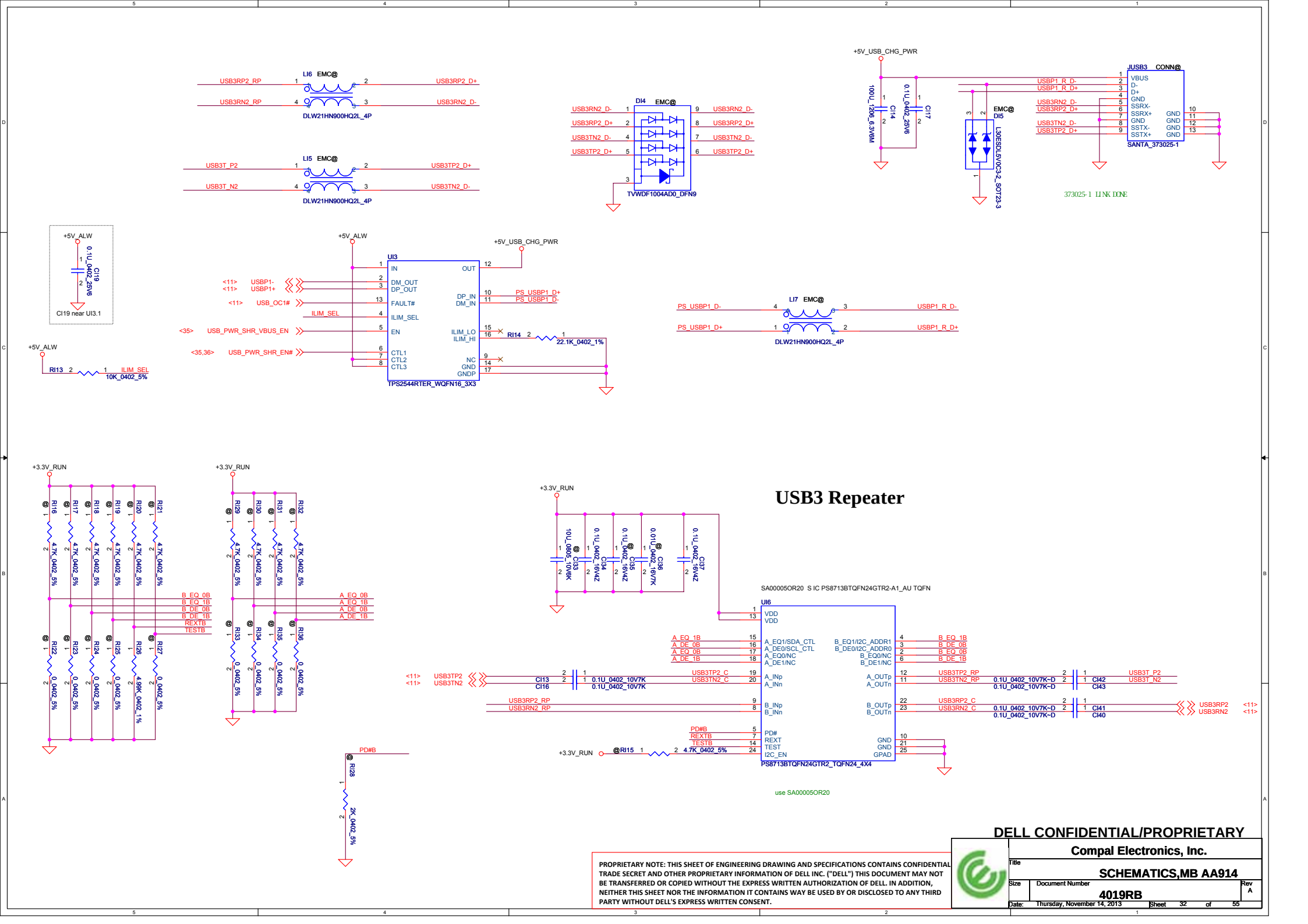

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Doesn't support.

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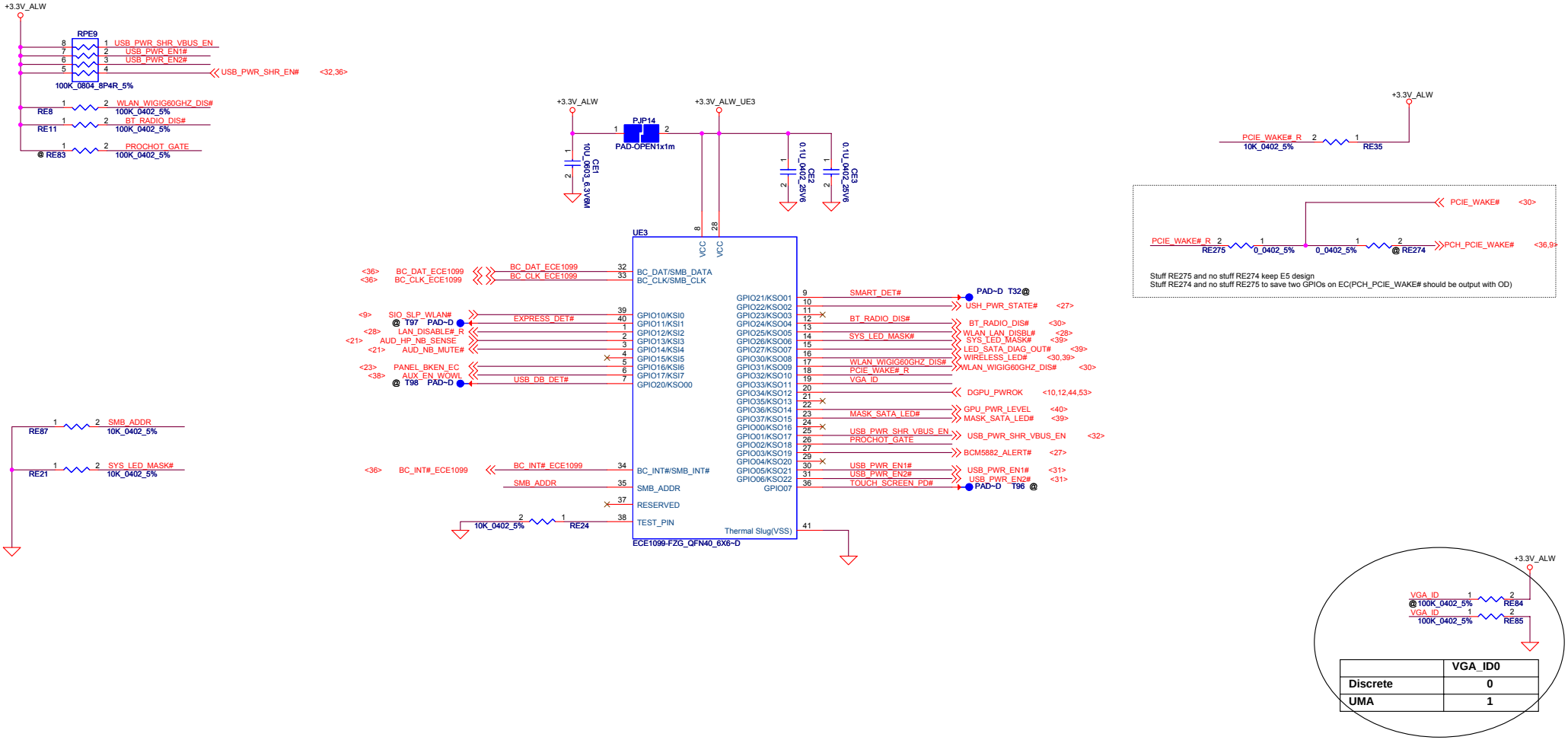

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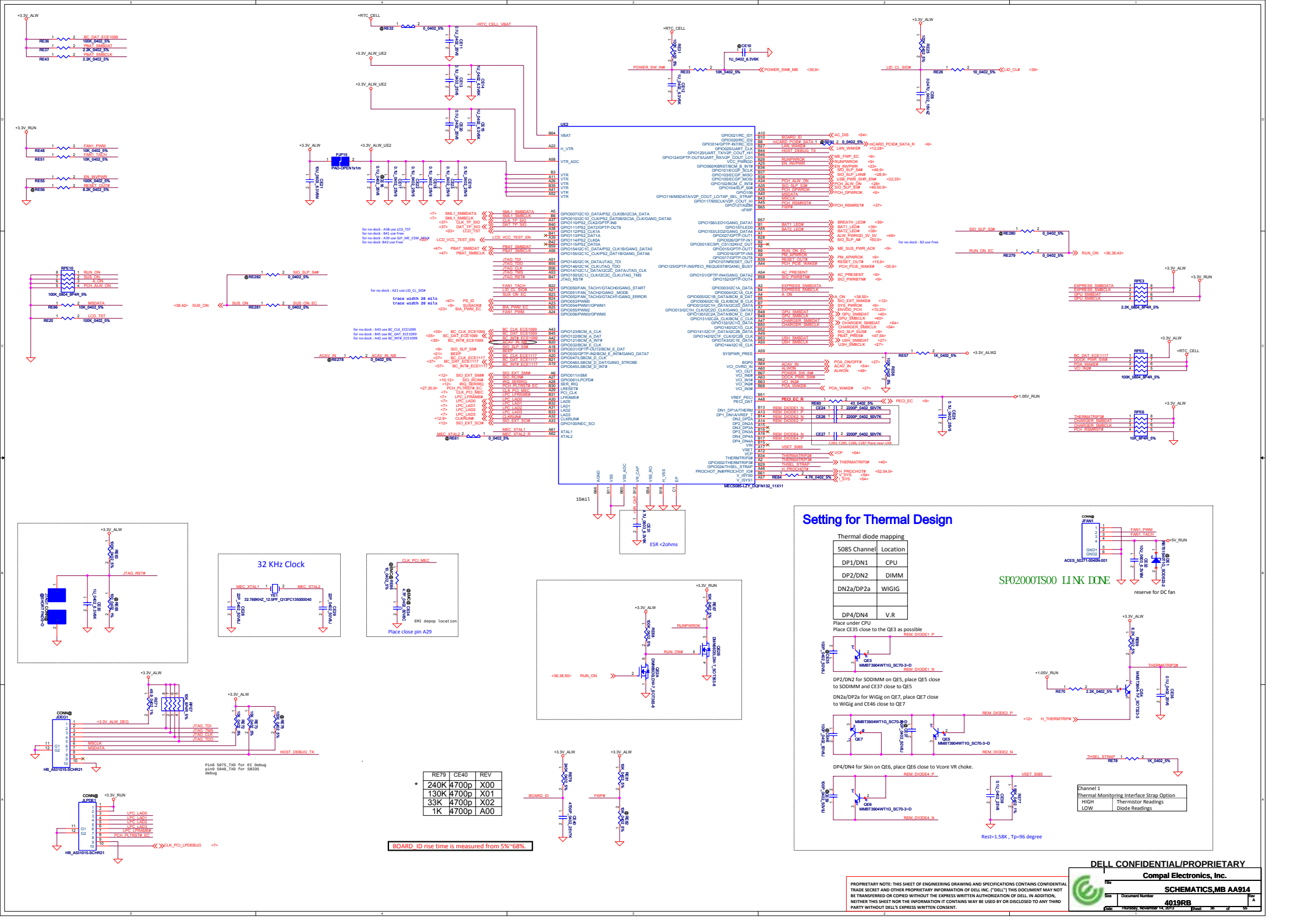
Setting for Thermal Design
Thermal diode mapping
5085 Channel | Location
DP1/DN1 | CPU
DP2/DN2 | DIMM
DN2a/DP2a | WIGIG
DP4/DN4 | V.R
Place under CPU
Place CE35 close to the QE3 as possible
DP2/DN2 for SODIMM on QE5, place QE5 close to SODIMM and CE37 close to QE5
DN2a/DP2a for WiGig on QE7, place QE7 close to WiGig and CE46 close to QE7
DP4/DN4 for Skin on QE6, place QE6 close to Vcore VR choke.
Rest=1.58K , Tp=96 degree
SP02000TS00 LINK DONE
reserve for DC fan
32 KHz Clock
32.768KHZ_12.5PF_Q13FC13500040
EMI depop location
Place close pin A29
Pin8 5075_TXD for EC Debug
pin9 5048_TXD for SBIOS debug
BOARD_ID rise time is measured from 5%~68%.
ESR <2ohms
Channel 1
Thermal Monitoring Interface Strap Option
HIGH | Thermistor Readings
LOW | Diode Readings
RE79 | CE40 | REV
240K | 4700p | X00
130K | 4700p | X01
33K | 4700p | X02
1K | 4700p | A00
UE2
MEC5085-LZY_DQFN132_11X11
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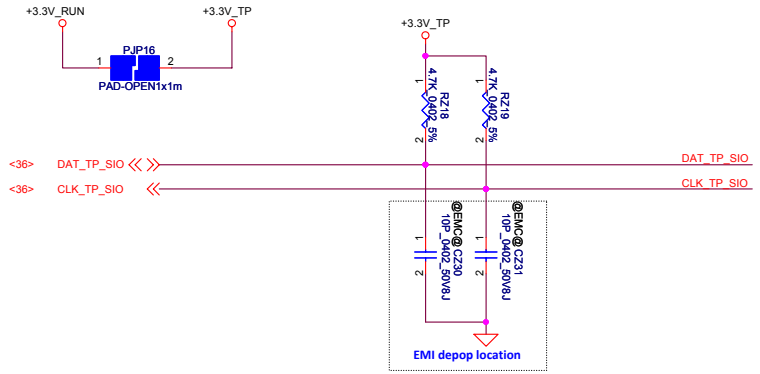
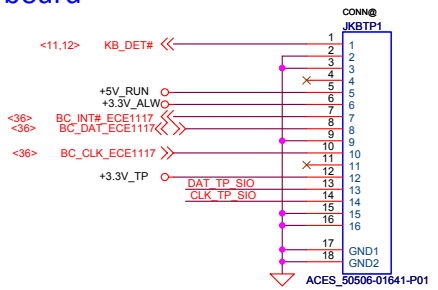
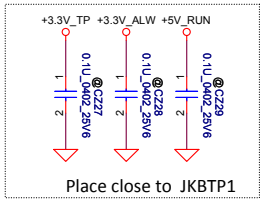
Touch Pad



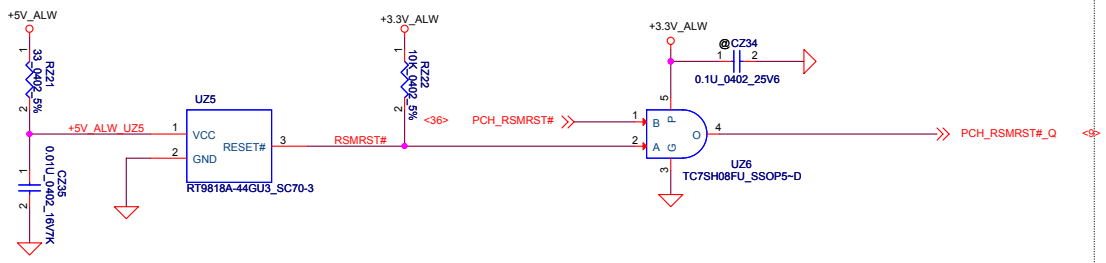
Keyboard



SP01001L400 LINK DONE



RSMRST circuit



@eDP Cable

Part Number	Description
DC02C007A00	H-CONN SET 13M MB-EDP

@eDP Cable w camera

Part Number	Description
DC02C007900	H-CONN SET 13M MB-EDP-CAMERA

@eDP TS Cable w camera

Part Number	Description
DC02C007B00	H-CONN SET 13M MB-EDP-CAMERA-TS

@SATA Cable-Spindle HDD

Part Number	Description
DC02C007800	H-CONN SET 13M MB-SPINDLE HDD

@SATA Cable-mSATA

Part Number	Description
DC02C007700	H-CONN SET 13M MB-MSATA HDD

@DC-IN Cable

Part Number	Description
DC30100MF00	CONN SET 0VN DCJACK-MB 2DW1003-038110F

@RTC BATT

Part Number	Description
DC30100MF00	CONN SET 0VN DCJACK-MB 2DW1003-038110F

@FAN

Part Number	Description
DC28A000800	FAN SET DAQ20 DC5V AB7405HB-HB3 ADDA

@KBTP FFC

Part Number	Description
NBX0001JH00	FFC 16P G P0.5 PAD=0.3 66.5MM MB-TP 13M

@Audio Board FFC

Part Number	Description
NBX0001JP00	FFC 12P F P.5 PAD=.35 26.85MM MB-AUDIO/B

@USH Board FFC

Part Number	Description
NBX0001JF00	FFC 26P G P0.5 PAD=0.3 58MM MB-USH/B 13M

@LED Board FFC

Part Number	Description
NBX0001JM00	FFC 10P G P.5 PAD.3 192.5MM MB-LED/B 13M

@PWR Board FFC

Part Number	Description
NBX0001JL00	FFC 6P G P0.5 PAD=0.3 31MM MB-PWR/B 13M

@FP FFC-Validity

Part Number	Description
NBX0001JN00	FFC 8P F P0.5 PAD=0.3 170MM USH/B-FP VALIDITY

@FP FFC-TCS

Part Number	Description
NBX0001JO00	FFC 8P F P0.5 PAD=0.3 164.8MM USH/B-FP_TCS

@Speak

Part Number	Description
PK230003Q0L	SPK PACK ZJX 2.0W 4 OHM FG

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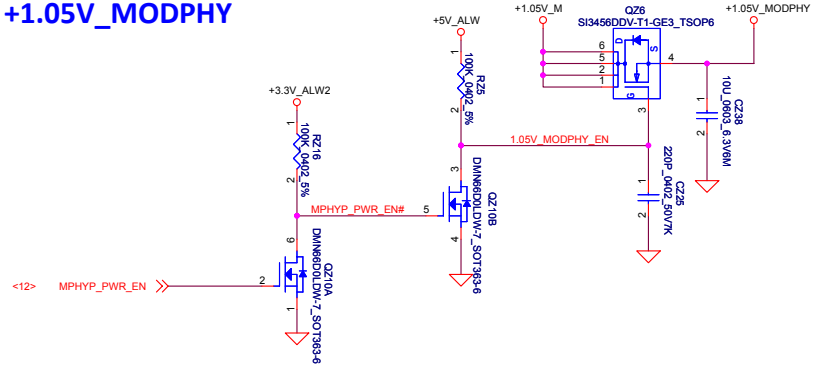
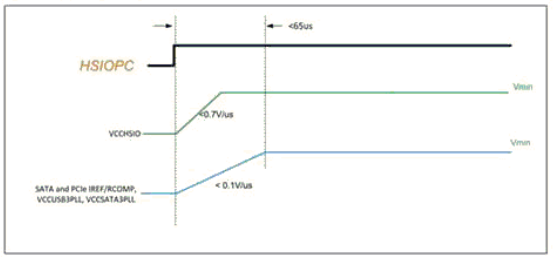
+1.05V_MODPHY

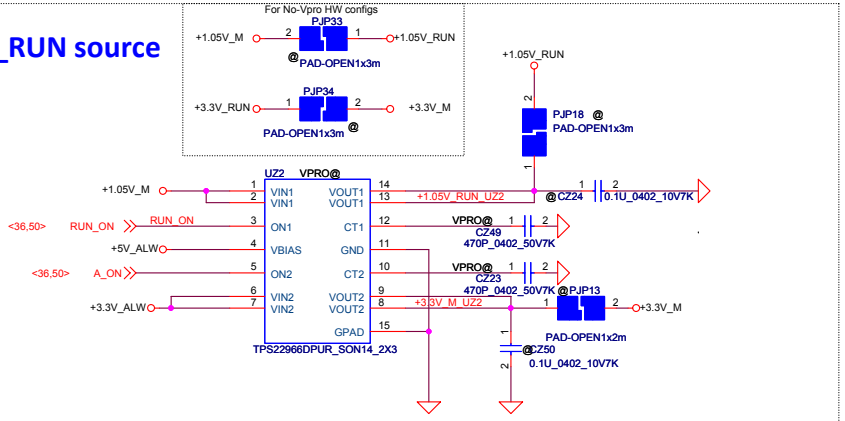


if support MODPHY off keep DSC solution
MODPHY timing spec 0.7V/us and <65us

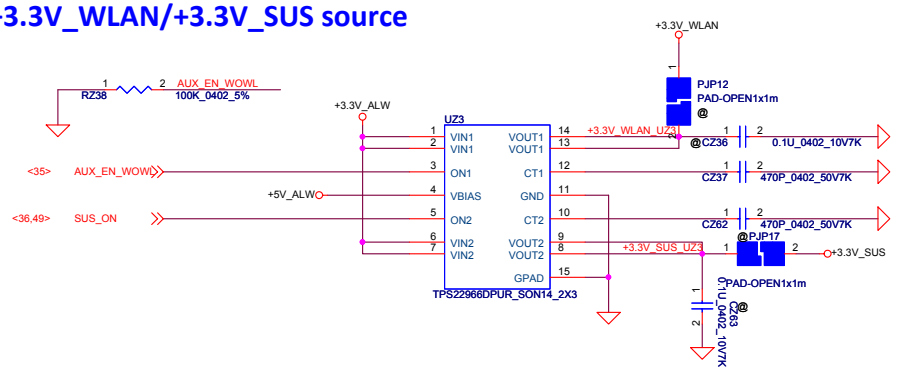
Figure 5-6. Sequencing Requirements between HSIOPC and LPT-LP 1.05V rails and COMP/IREF signals



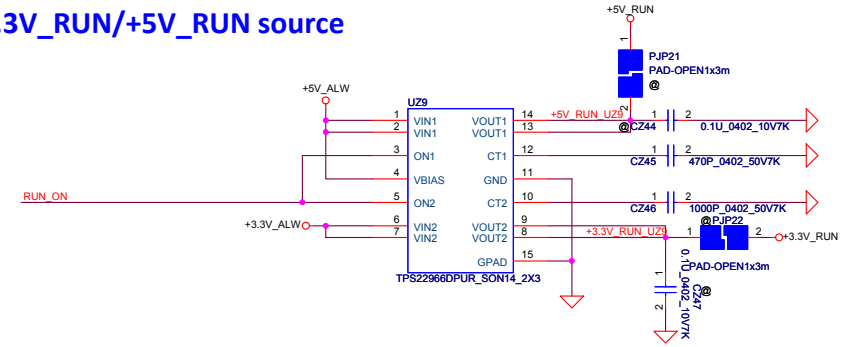
+1.05V_RUN source



+3.3V_WLAN/+3.3V_SUS source



+3.3V_RUN/+5V_RUN source



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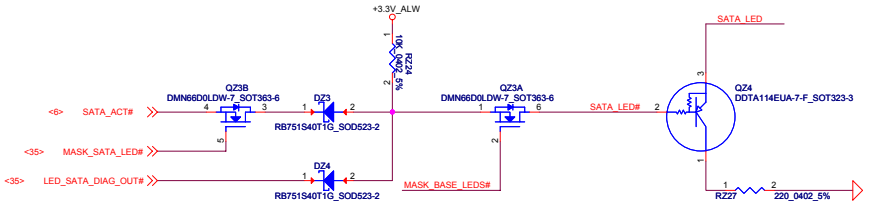
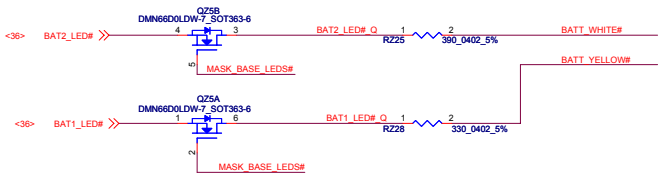
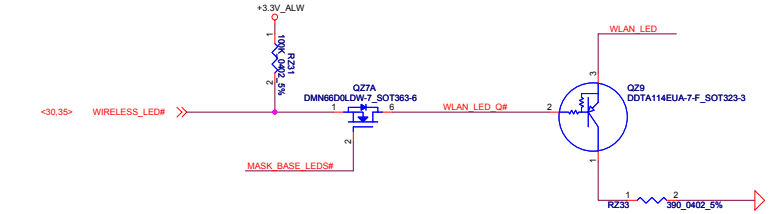
HDD LED solution for White LED



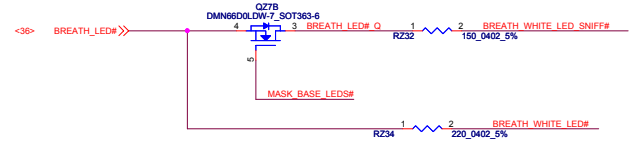
Battery LED

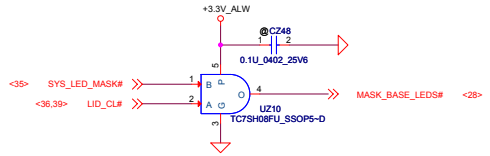


WLAN LED solution for White LED

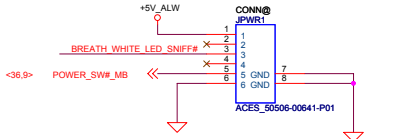


Breath LED



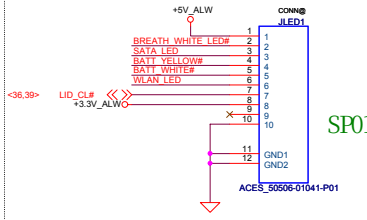


POWER board CONN



SP01001C000 LINK DONE

LED board CONN

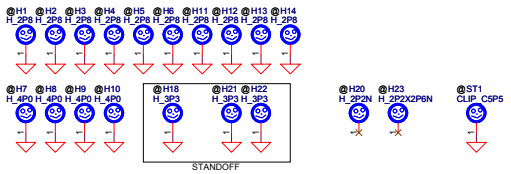


SP01001FR00 LINK DONE

Fiducial Mark

@FD1 FIDUCIAL MARK~D
@FD2 FIDUCIAL MARK~D
@FD3 FIDUCIAL MARK~D
@FD4 FIDUCIAL MARK~D

LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



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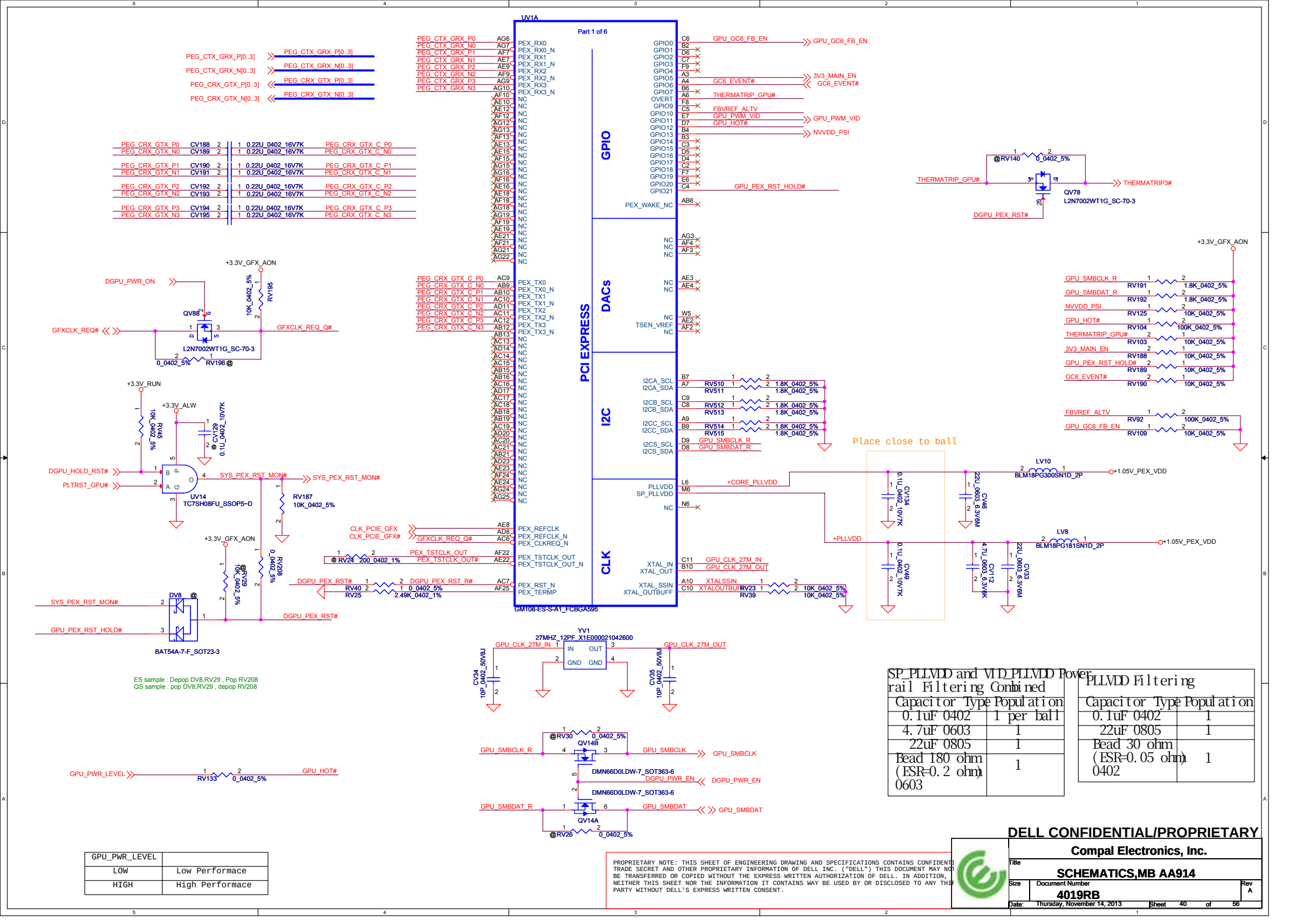

GPU_PWR_LEVEL	
LOW	Low Performace
HIGH	High Performace

SP_PLLVDD and VID_PLLVDD Power rail Filtering Combined

Capacitor Type	Population
0.1uF 0402	1 per ball
4.7uF 0603	1
22uF 0805	1
Bead 180 ohm (ESR=0.2 ohm) 0603	1

PLLVDD Filtering

Capacitor Type	Population
0.1uF 0402	1
22uF 0805	1
Bead 30 ohm (ESR=0.05 ohm) 0402	1

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I2CS Slave Address

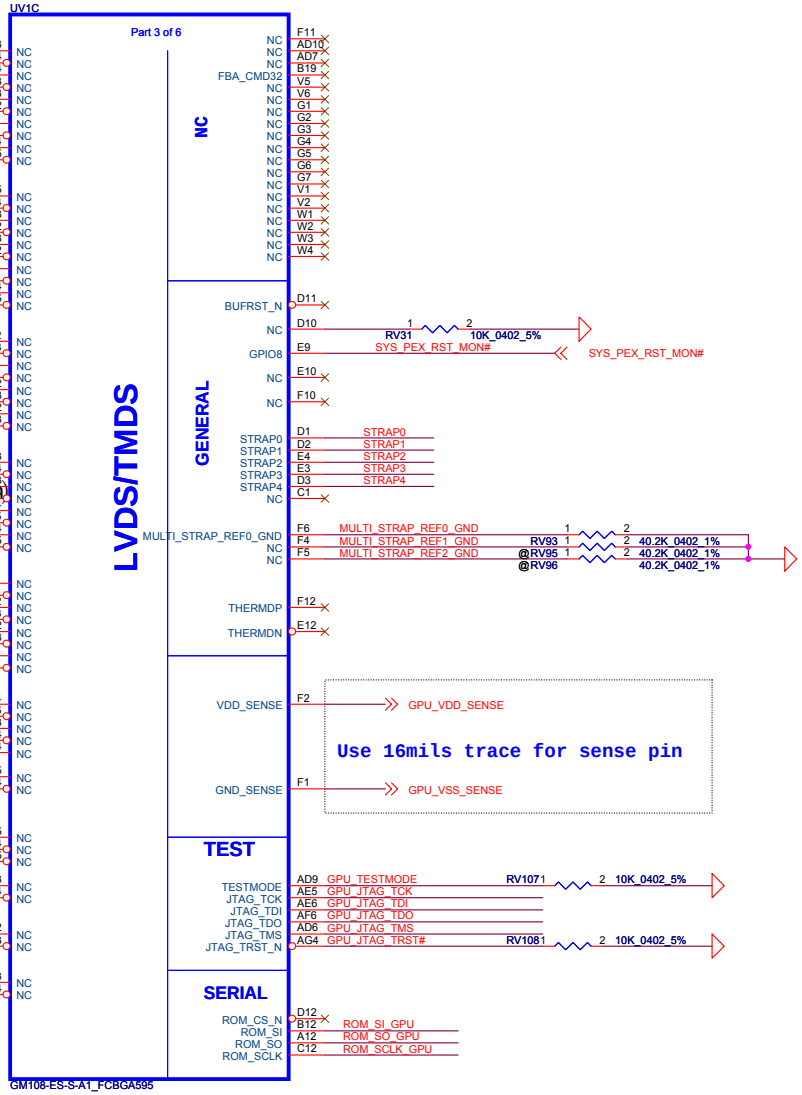
SMBUS_ALT_ADDR	Description
0	0x9E(Default)
1	0x9C(Multi-GPU usage)

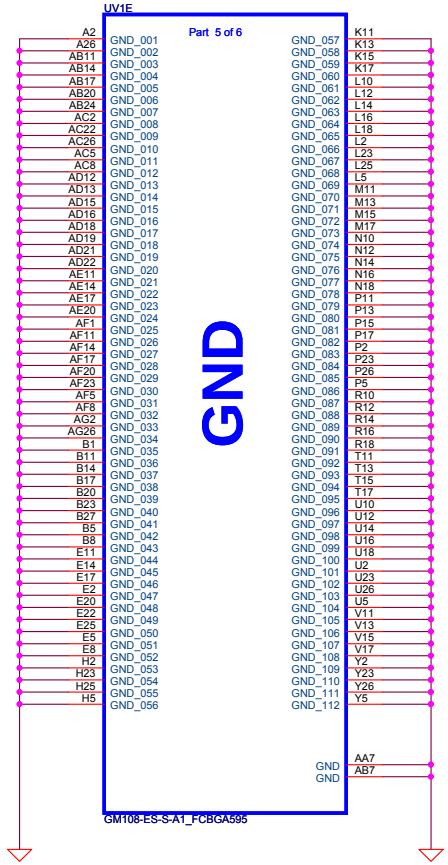
VGA_DEVICE Setting

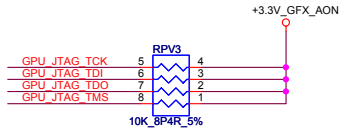
VGA_DEVICE	Description
0	Non-Primary 3D Acceleration Device(Class Code 030200h)
1	Primary Display or VGA Device(Class Code 300h)

Resistance Mapping to Hex Values

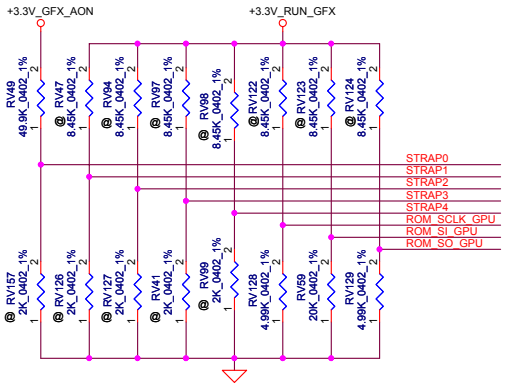
Resistor Value	Pull-up to VDDR3	Pull-down to GND
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111







Decive ID change to 0x1056



Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0	Note
ROM_SCLK	SOR3_EXPOSED->0	SOR2_EXPOSED->0	SOR1_EXPOSED->0	SOR0_EXPOSED->0	ROM_SCLK pull-down 4.99k to GND
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]	ROM_SI pull-down 20k to GND
ROM_SO	DEVID_SEL->0(default)	PCIE_CFG->0(defual)	SMB_ALT_ADDR->0(default)	VGA_DEVICE->0	ROM_SO pull-down 4.99k to GND
STRAP0	Keep pull up to 3V3_AON and pull-down to GND footprint and stuff 50k ohm pull up				STRAP0 pull up 50k to +3.3V_GFX_AON
STRAP1 STRAP2 STRAP3 STRAP4	Reserve				

DEVID_SEL/PCIE_CFG defaul set 0, need refer Platform Update Notification for the latest configuration

VENDER	STRAP	Part Number	Note(ROM_SI)
Hynix	0x3	H5TC4G63AFR-11C	20k PD
Micron	0x4	MT41J256M16HA-093G:E	24.9k PD need change to MT41K256M16HA-107G:E
Samsung	0x5	K4W4G1646D-HC1A	30.1k PD

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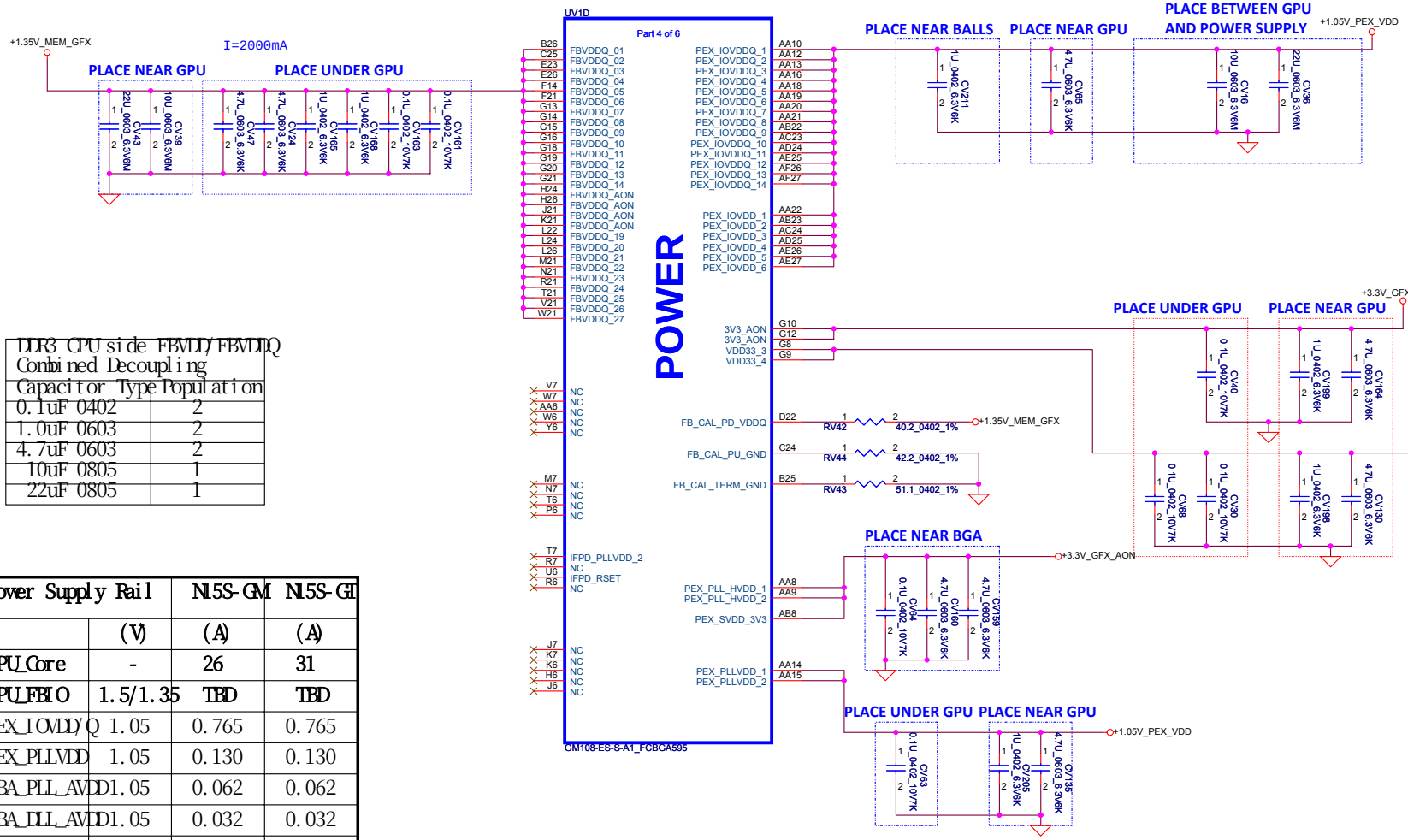

GC6_2.0_GI0/GI2 pin connect to +3.3V_GFX_AON

PEX_IOVDD/Q Power Rail Combined	
Capacitor Type	Population
1uF 0402	1
4.7uF 0603	1
10uF 0805	1
22uF 0805	1

DDR3 CPU side FBVDD/FBVDDQ Combined Decoupling	
Capacitor Type	Population
0.1uF 0402	2
1.0uF 0603	2
4.7uF 0603	2
10uF 0805	1
22uF 0805	1

Power Supply Rail		N15S-GM	N15S-GI
	(V)	(A)	(A)
GPU_Core	-	26	31
GPU_FBIO	1.5/1.35	TBD	TBD
PEX_IOVDD/Q	1.05	0.765	0.765
PEX_PLLVDD	1.05	0.130	0.130
FBA_PLL_AVDD	1.05	0.062	0.062
FBA_DLL_AVDD	1.05	0.032	0.032
PLL_VDD	1.05	0.058	0.058
SP_PLLVDD	1.05	0.030	0.030
1.05V Total	1.05	1.060	1.060
VDD33+3V3AON	3.3	0.036	0.036
PEX_SVDD_3V3	3.3	0.167	0.167
PEX_PLL_HVDD	3.3	0.022	0.022
3.3V Total	3.3	0.225	0.025

PEX_PLLVDD Decoupling	
Capacitor Type	Population
0.1uF 0402	1
1uF 0603	1
4.7uF 0805	1

PEX_SVDD/PEX_PLL_HVDD Decoupling	
Capacitor Type	Population
0.1uF 0402	1
4.7uF 0603	2

3V3_MAIN Decoupling	
Capacitor Type	Population
0.1uF 0402	2
1uF 0603	1
4.7uF 0603	1

3V3_AON Decoupling	
Capacitor Type	Population
0.1uF 0402	1
1uF 0603	1
4.7uF 0603	1

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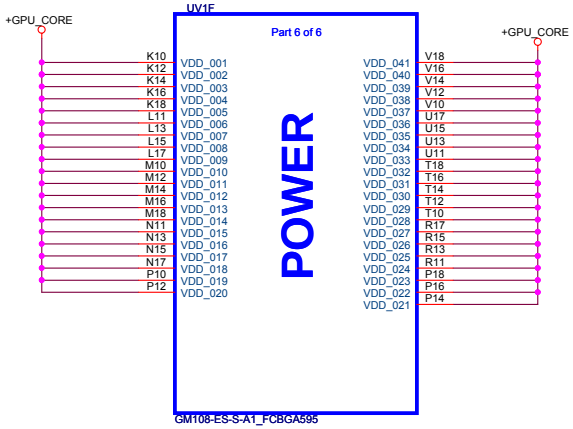
Caps on Power Side
1UX4 4.7UX10 under GPU
4.7UX5 22UX1 47UX2 330UX2 near GPU



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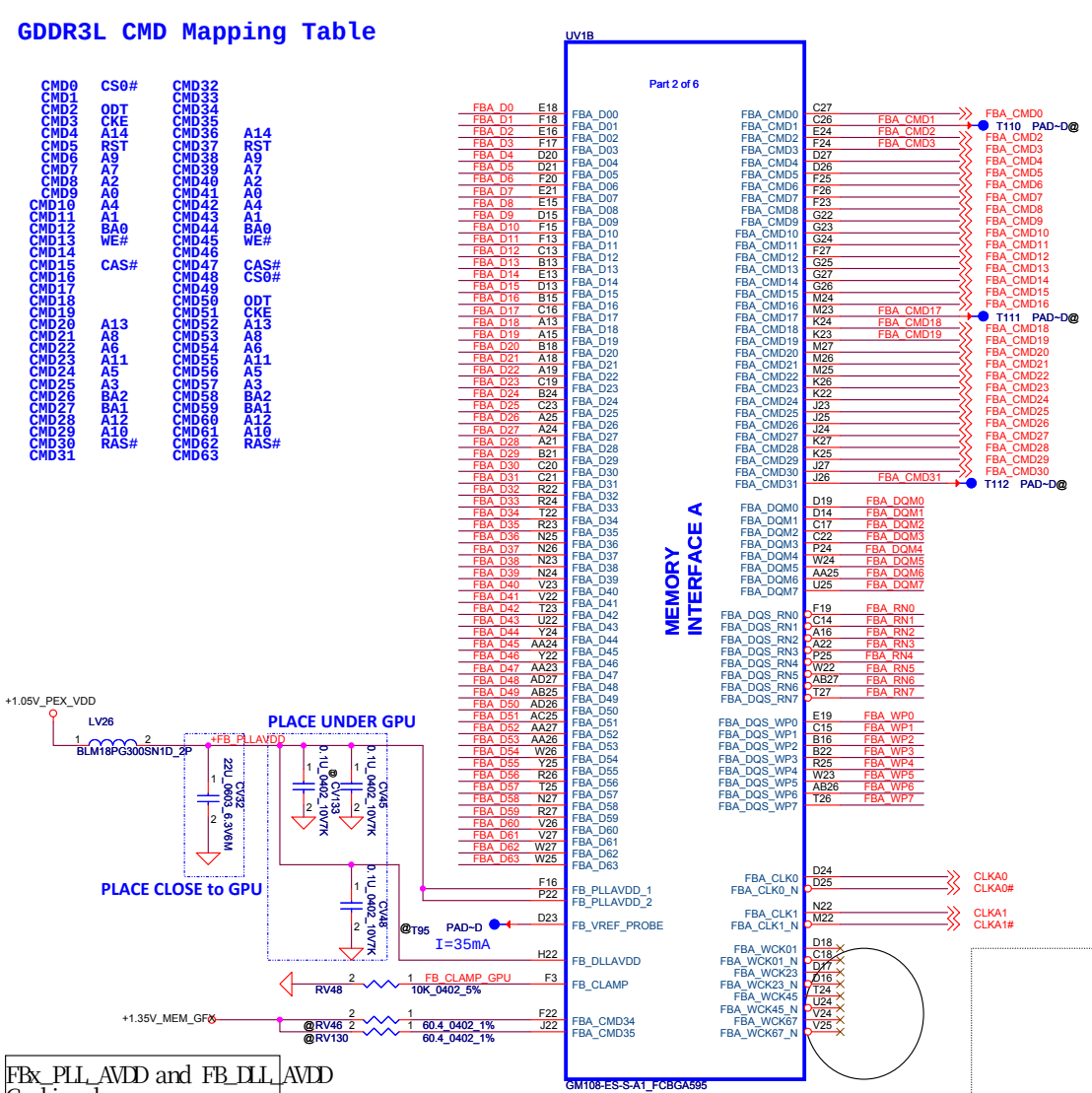
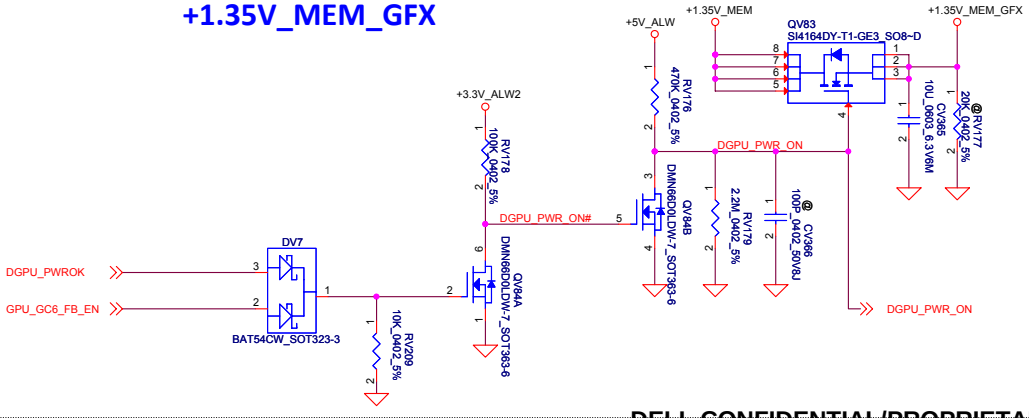
GDDR3L CMD Mapping Table

CMD0	CS0#	CMD32	
CMD1		CMD33	
CMD2	ODT	CMD34	
CMD3	CKE	CMD35	
CMD4	A14	CMD36	A14
CMD5	RST	CMD37	RST
CMD6	A9	CMD38	A9
CMD7	A7	CMD39	A7
CMD8	A2	CMD40	A2
CMD9	A0	CMD41	A0
CMD10	A4	CMD42	A4
CMD11	A1	CMD43	A1
CMD12	BA0	CMD44	BA0
CMD13	WE#	CMD45	WE#
CMD14		CMD46	
CMD15	CAS#	CMD47	CAS#
CMD16		CMD48	CS0#
CMD17		CMD49	
CMD18		CMD50	ODT
CMD19		CMD51	CKE
CMD20	A13	CMD52	A13
CMD21	A8	CMD53	A8
CMD22	A6	CMD54	A6
CMD23	A11	CMD55	A11
CMD24	A5	CMD56	A5
CMD25	A3	CMD57	A3
CMD26	BA2	CMD58	BA2
CMD27	BA1	CMD59	BA1
CMD28	A12	CMD60	A12
CMD29	A10	CMD61	A10
CMD30	RAS#	CMD62	RAS#
CMD31		CMD63	



+1.35V_MEM_GFX



FBx_PLL_AVDD and FB_DLL_AVDD Combined Capacitor Type	Population
0.1uF 0402	2
22uF 0805	1
Bead 30 ohm (ESR=0.01 ohm) 0603	1

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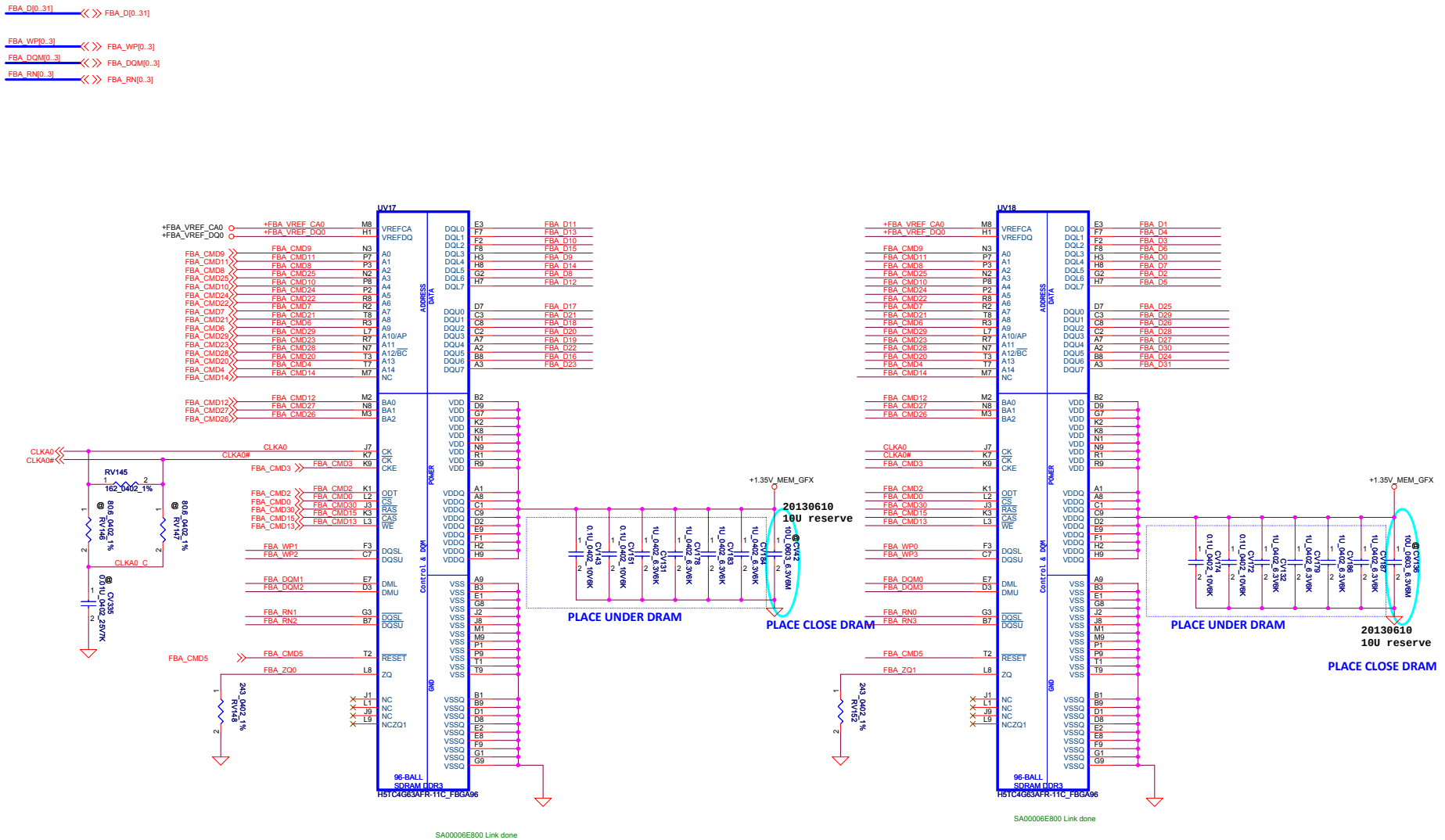
Memory Partition A - Upper 16 bits

256x16 DDR3L



DDR3 per Memory FBVDDQ Decoupling	
FBVDDQ Combined	
Capacitor Type	Population
0.1uF 0402	2
1.0uF 0603	4
10uF 0805	0

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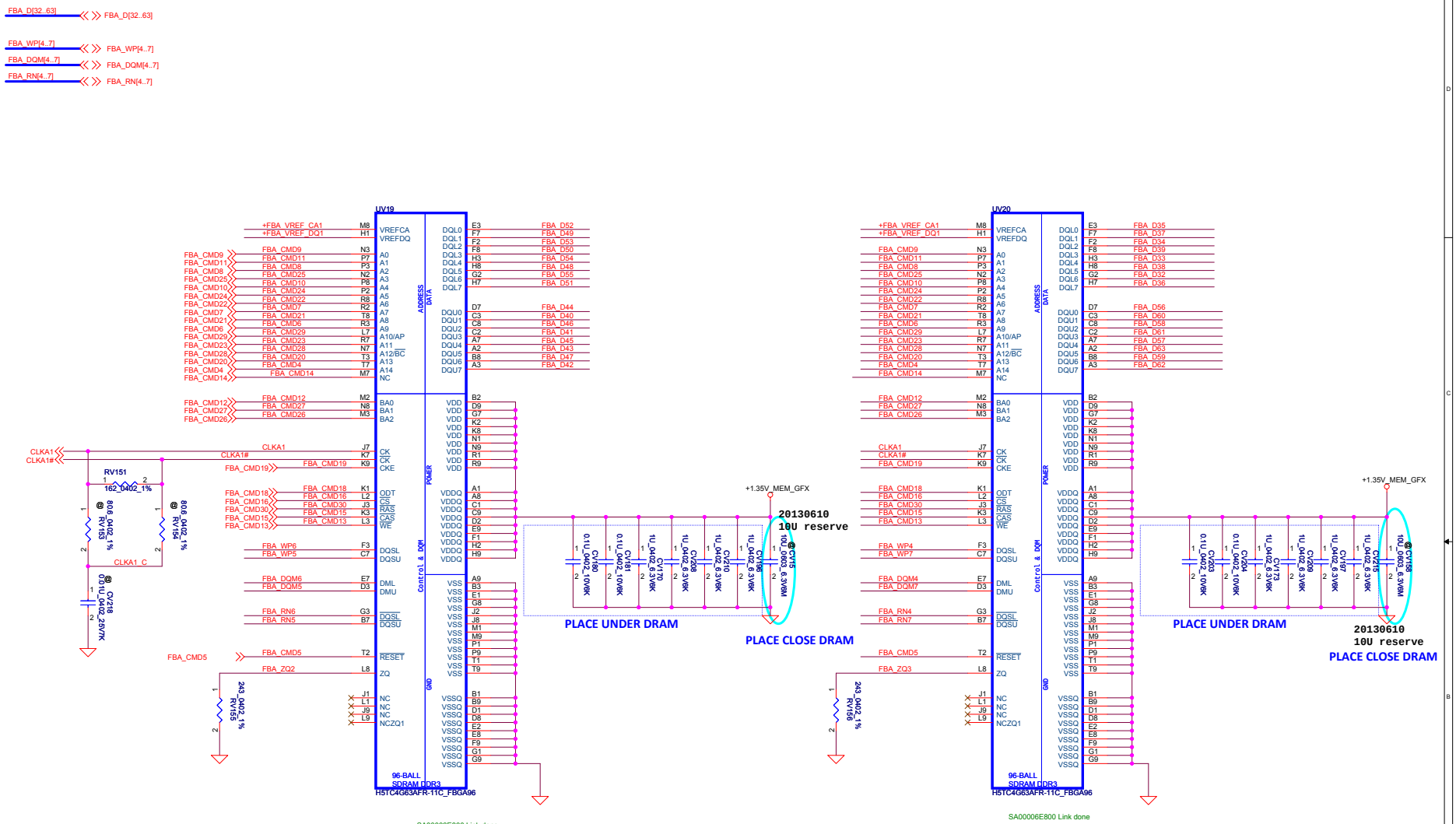
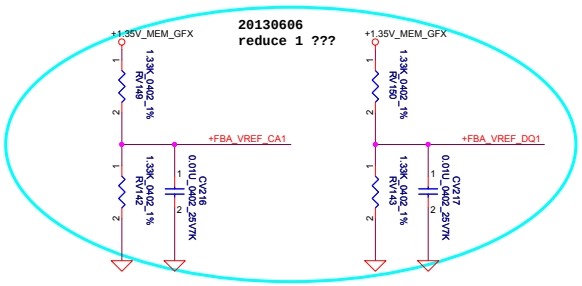
Memory Partition A - Lower 16 bits

256x16 DDR3L





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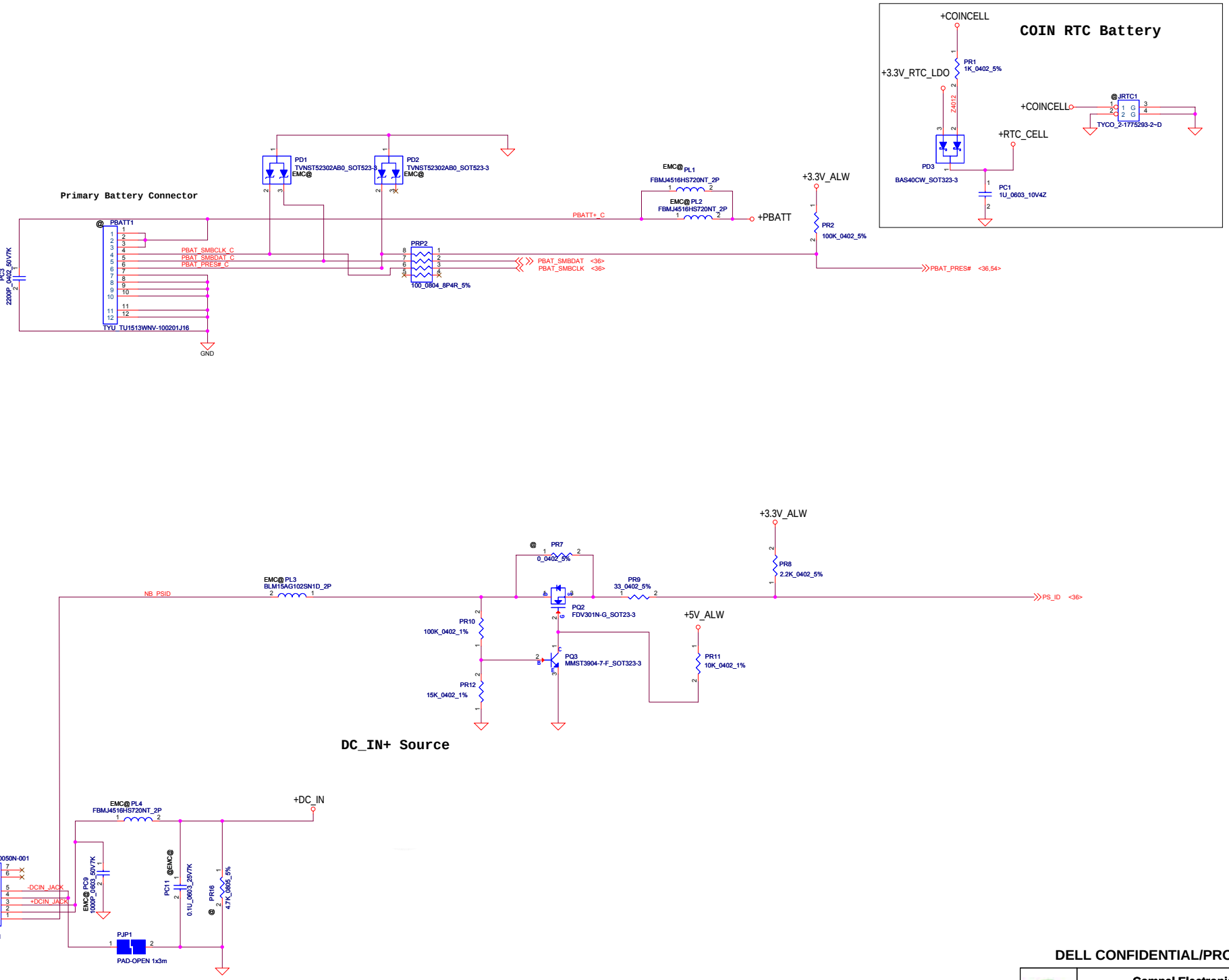

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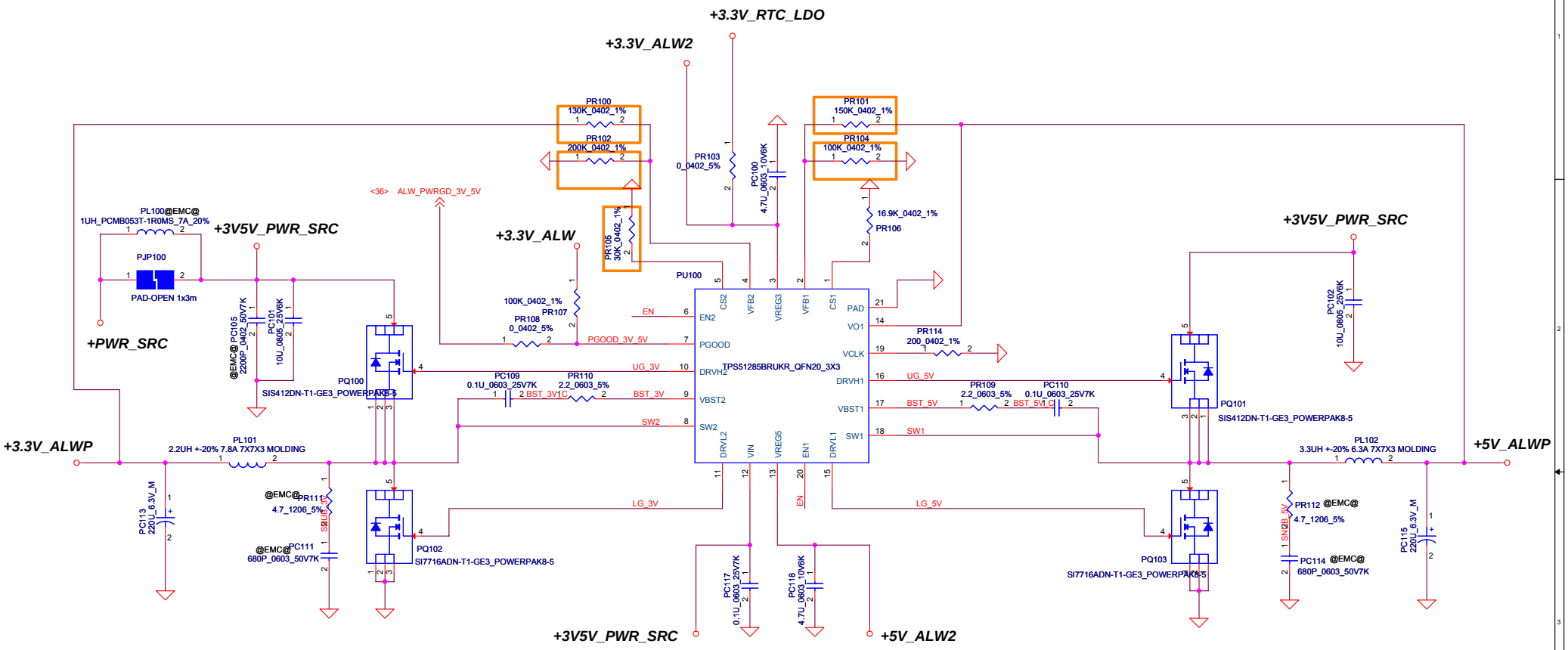
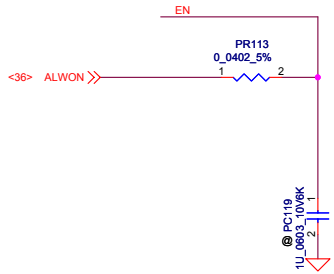
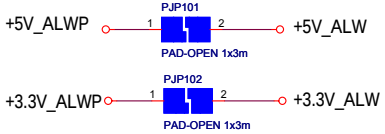


3.3 VALWP
TDC: 6.0 A
Peak Current: 8.6 A
OCP Current: 10.32 A
Cap ESR(@20℃): 18 mohm
Choke DCR(@20℃): 15.5 mohm

	TYP	MAX
H/S Rds(on)	:24.0 mohm ,	30.0 mohm
L/S Rds(on)	:13.5 mohm ,	16.5 mohm





5 VALWP
TDC: 3.5 A
Peak Current: 5.0 A
OCP Current: 6.0 A
Cap ESR(@20℃): 18 mohm
Choke DCR(@20℃): 25 mohm

	TYP	MAX
H/S Rds(on)	:24.0 mohm ,	30.0 mohm
L/S Rds(on)	:13.5 mohm ,	16.5 mohm

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0.675 Volt
TDC 0.7 A
Peak Current 1.0 A
OCP Current 1.2 A

+PWR_SRC
PJP200
PAD-OPEN 1x2m~D
1.35V_B+
PC200 10U_0805_25V6K
@ PC201 10U_0805_25V6K
PC203 @EMC@ 2200P_0402_50V7K
BOOT_1.35V_C
PC204 0.22U_0603_16V7K
PR200 2.2_0603_5%
BOOT_1.35V
DH_1.35V
SW_1.35V
DL_1.35V
+VLDOIN_1.35V
PJP201
PAD-OPEN1x1m
+1.35V_MEN_P
+0.675V_P
PC205 22U_0805_6.3V6M
PU200
RT8207MZQW_WQFN20_3X3
LGATE PHASE UGATE BOOT VLDOIN VTT PAD VTTGND VTTSNS GND VTTREF VDDQ PGOOD TON S5 S3 FB PGND CS VDDP VDD
+1.35V_MEN_P
+V_DDR_REF
PL200 1.0UH_PCMC104T-1R0MN_20A_20%
PC207 220U_D2_2V_R17M
PR203@EMC@ 4.7_1206_5%
SNUB_1.25V
PC208@EMC@ 680P_0603_50V7K
PQ201 AON6932A_DFN5X6-8-7
footprint use AON6932A
PR201 6.04K_0402_1%
CS_1.35V
PC209 1U_0603_10V6K
PR202 5.1_0603_5%
VDD_1.35V
PC211 1U_0603_10V6K
+5V_ALW
+5V_ALW
+V_DDR_REF
PC212 0.033U_0402_16V7K
FB sense trace
when FB pull down to GND
PR205 8.06K_0402_1%
1.35V_FB
PC213 100P_0402_50V8J
PR206 1M_0402_1%
1.35V_B+
<36,38> SUS_ON
10K_0402_1% PR209
@ PC214 .1U_0402_16V7K
@ PC215 .1U_0402_16V7K
PR210 0_0402_5%
<18> 0.675V_DDR_VTT_ON
@PR211 0_0402_5%
<9,36,50> SIO_SLP_S3#
+1.35V_MEN_P
FB sense trace

1.35 _MEN
TDC: 9.45 A
Peak Current: 13.5 A
OCP Current: 16.2 A
Cap ESR(@20℃): 17 mohm
Choke DCR(@20℃): 3.5 mohm

	TYP	MAX
H/S Rds(on) :	6.7 mohm ,	8.5 mohm
L/S Rds(on) :	2.4 mohm ,	3.2 mohm

PJP203
JUMP_1x3m
+1.35V_MEN_P
PJP204
JUMP_1x3m
+1.35V_MEM

+0.675V_P
PJP202
PAD-OPEN1x1m
+0.675V_DDR_VTT

Mode	S3	S5	+1.35V_MEN	+V_DDR_REF	+0.675V_P
S5	L	L	off	off	off
S3	L	H	on	on	off(Hi-Z)
S0	H	H	on	on	on

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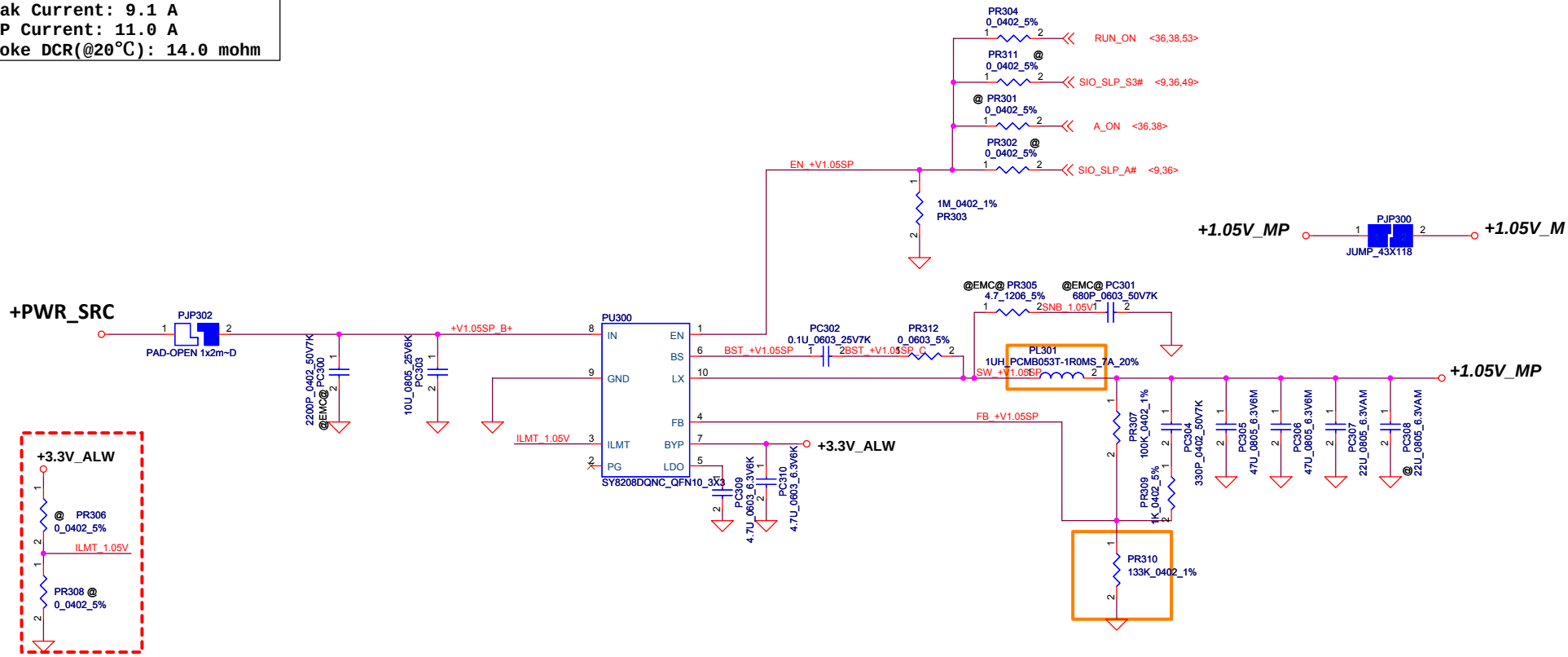
+1.05V_MEN
TDC: 6.5 A
Peak Current: 9.1 A
OCP Current: 11.0 A
Choke DCR(@20°C): 14.0 mohm



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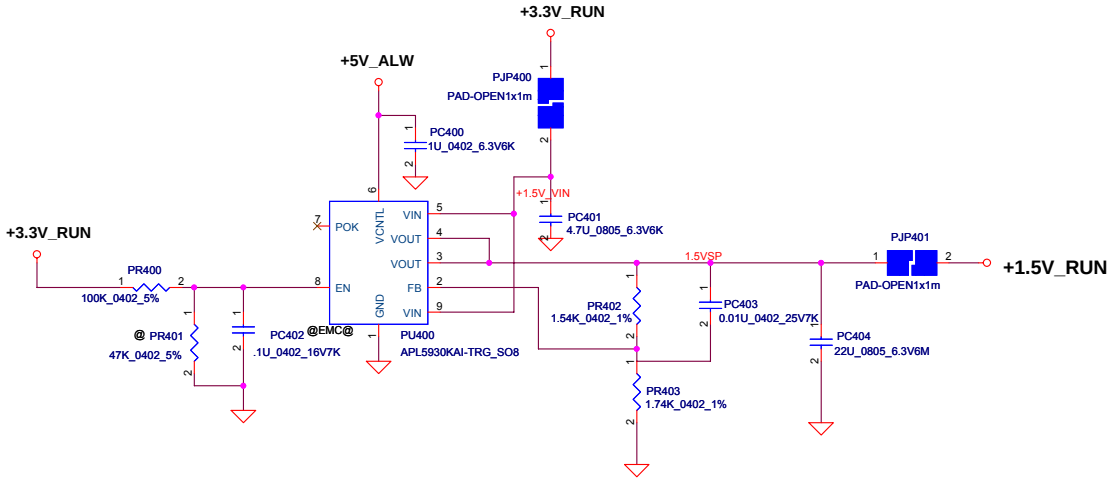
+1.5V_RUN
TDC: 0.47 A
Peak Current: 0.67 A



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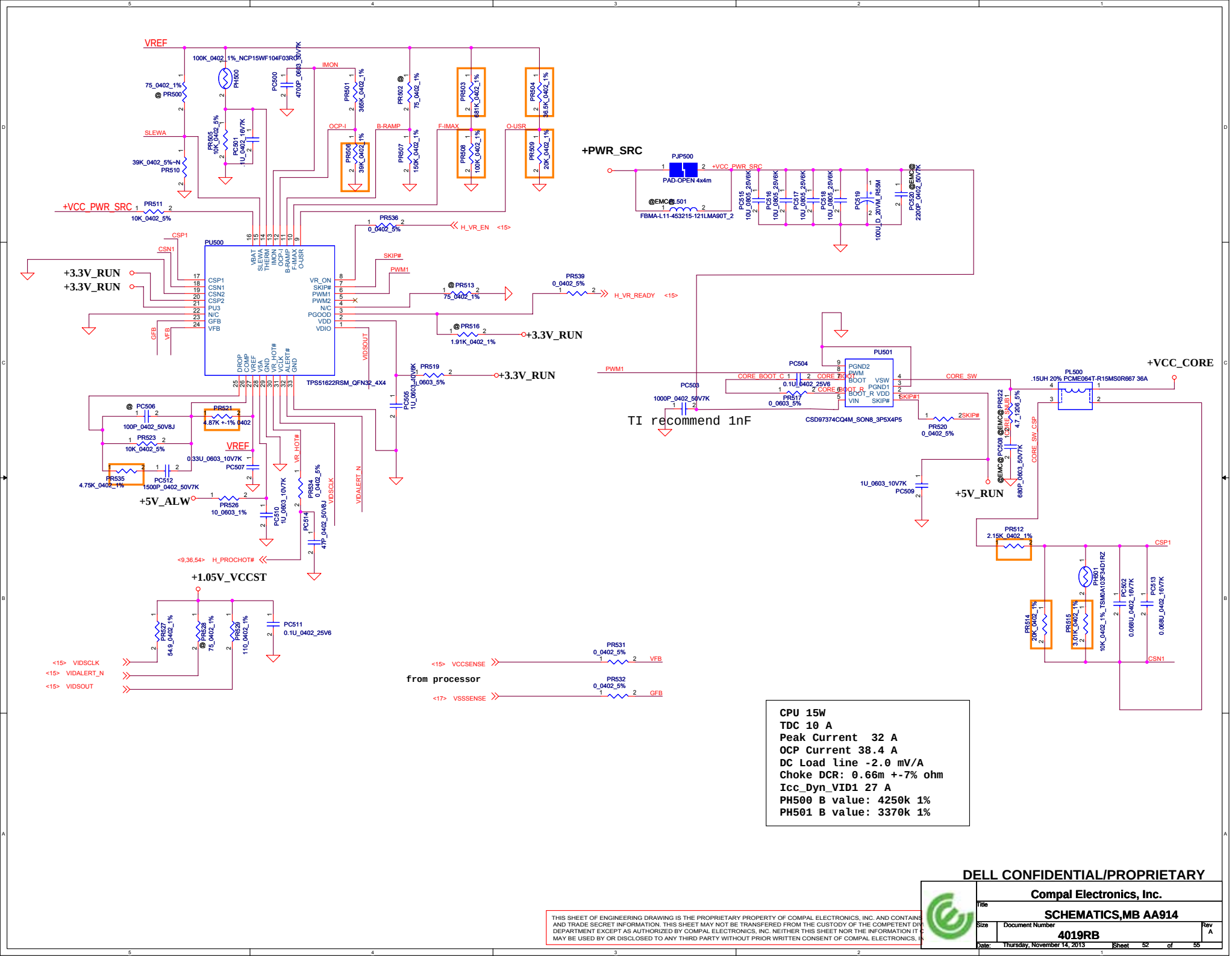

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Vboot=Vvref*Rref2/(Rref1+Rref2+Rboot)
Rt=Rrefadj // (Rboot+Rref2)
Vmin= Vvref*[Rref2/(Rref2+Rboot)]*[Rt/(Rref1+Rt)]
Vmax=Vvref*Rref2/[(Rref1//Rrefadj)+Rboot+Rref2]
Vout=Vmin+N*Vstep
Vstep=(Vmax-Vmin)/Nmax

Current Limit threshold setting
Rocset= (Ivalley * Rds(on) + 40 mV) / 10uA

I_ripple=(19-0.9)*0.9/
(304.89Khz*0.36u*19)=7.811A

OCP=54A/2=27A per phase
Ivalley=27A-7.811A/2=23.1A

H-side MOS:TPCA8065
Rds(on):
11.7mohm@Vgs=10V
9.4mohm@Vgs=4.5V
Id :16A@Ta=25 degC

L-side MOS:TPCA8057
Rds(on):
2.0mohm@Vgs=10V
2.6~3.2mohm@Vgs=4.5V
Id :42A@Ta=25 degC

Choke: 0.36uH (Size:10*10*4)
Rdc=1.1mohm +-5%
Heat Rating Current=30A
Saturation Current=50A

C=3*330uF (9mohm)=990uF
Vripple=Iripple*ESR(min)=7.811A*3mohm=23.4mV

Different VGA Chip (different EDP-Peak Current) need select different solution

VGA Chip	N14P-GV	N14P-GV2	N14M-GS	N14M-LP	N14P-LP	N14P-GE	N14P-GS	N14P-GT
OpenVReg Configurations	Config B	Config B	Config B	Config B	Config B	Config B	Config B	Config B
Rated TDP Power at Tj=102C	18W	25W	18W	13W	18.9W	25W	25.6W	35.5W
Boosted GPU Total at Tj=102C	25W	32W	25W	20W	23W	N/A	30W	40W
EDP-Continuous at Tj=102C	24A	32A	26A	22A	25A	27A	38A	45A
EDP-Peak at Tj=102C	35A	55A	45A	35A	35A	40A	60A	75A
Istep max (Evaluation)	15A	27A	25A	20A	14A	12A	31.5A	35A
OCP Setting Current	42A	66A	54A	42A	42A	48A	72A	90A
Rocset	8.96K	12.45K	10.7K	8.96K	8.96K	9.83K	8.3K	9.39K
Recommendation	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H2L	2phase 1H2L
Polymer Cap (330uF)	6mohm * 2	9mohm * 3	9mohm * 3	6mohm * 2	6mohm * 2	6mohm * 2	6mohm * 3 (L=0.22uH)	4.5mohm * 3 (L=0.15uH)
Or OSCON (390uF)	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	NULL	NULL

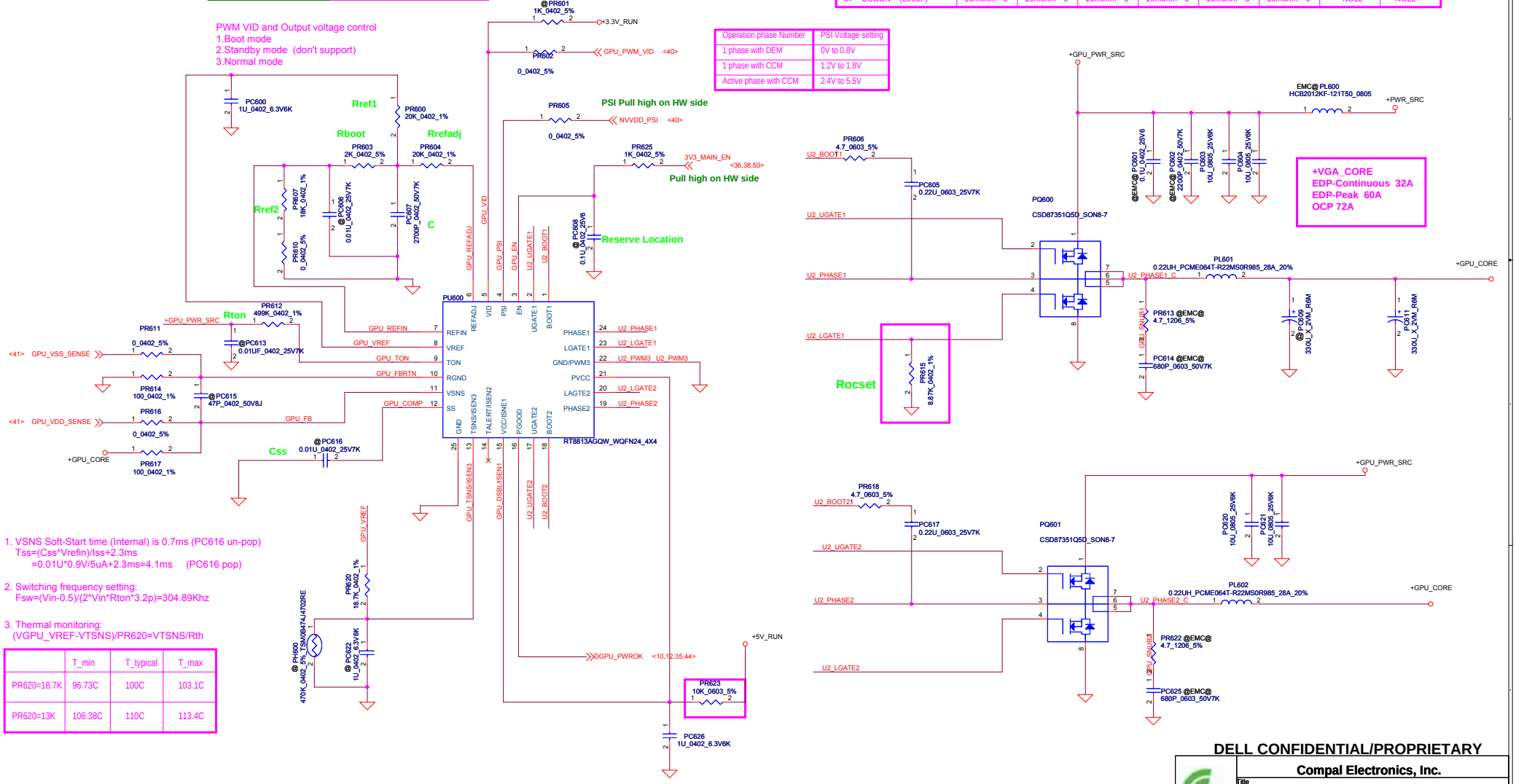
Module model information:
RT8813A_V1A for IC module
RT8813A_V1B for SW module

PWM-VID Spec and component Values

PWM-VID Spec		Config A	Config B	Config C
Vmin		0.6V	0.6V	0.65V
Vmax		1.2V	1.2V	1.15V
Vboot		0.875V	0.9V	0.9V
Voltage step		6.25mV	6.25mV	25mV
N of Voltage level		96	96	20
Rrefadj	PR9	39K	20K	39K
Rref1	PR5	39K	20K	30K
Rboot	PR8	1.5K	2K	3K
Rref2=PR10+PR12	PR10	30K	18K	24K
	PR12	1.5K	0	3K
C	PC8	1.5nf	2.7nf	1.8nf

PWM VID and Output voltage control
1.Boot mode
2.Standby mode (don't support)
3.Normal mode

Operation phase Number	PSI Voltage setting
1 phase with DEM	0V to 0.8V
1 phase with CCM	1.2V to 1.8V
Active phase with CCM	2.4V to 5.5V



1. VSNS Soft-Start time (Internal) is 0.7ms (PC616 un-pop)
Tss=(Css*Vrefin)/Iss+2.3ms
=0.01U*0.9V/5uA+2.3ms=4.1ms (PC616 pop)

2. Switching frequency setting:
Fsw=(Vin-0.5)/(2*Vin*Rton*3.2p)=304.89Khz

3. Thermal monitoring:
(VGPU_VREF-VTSNS)/PR620=VTSNS/Rth

	T_min	T_typical	T_max
PR620=18.7K	96.73C	100C	103.1C
PR620=13K	106.38C	110C	113.4C

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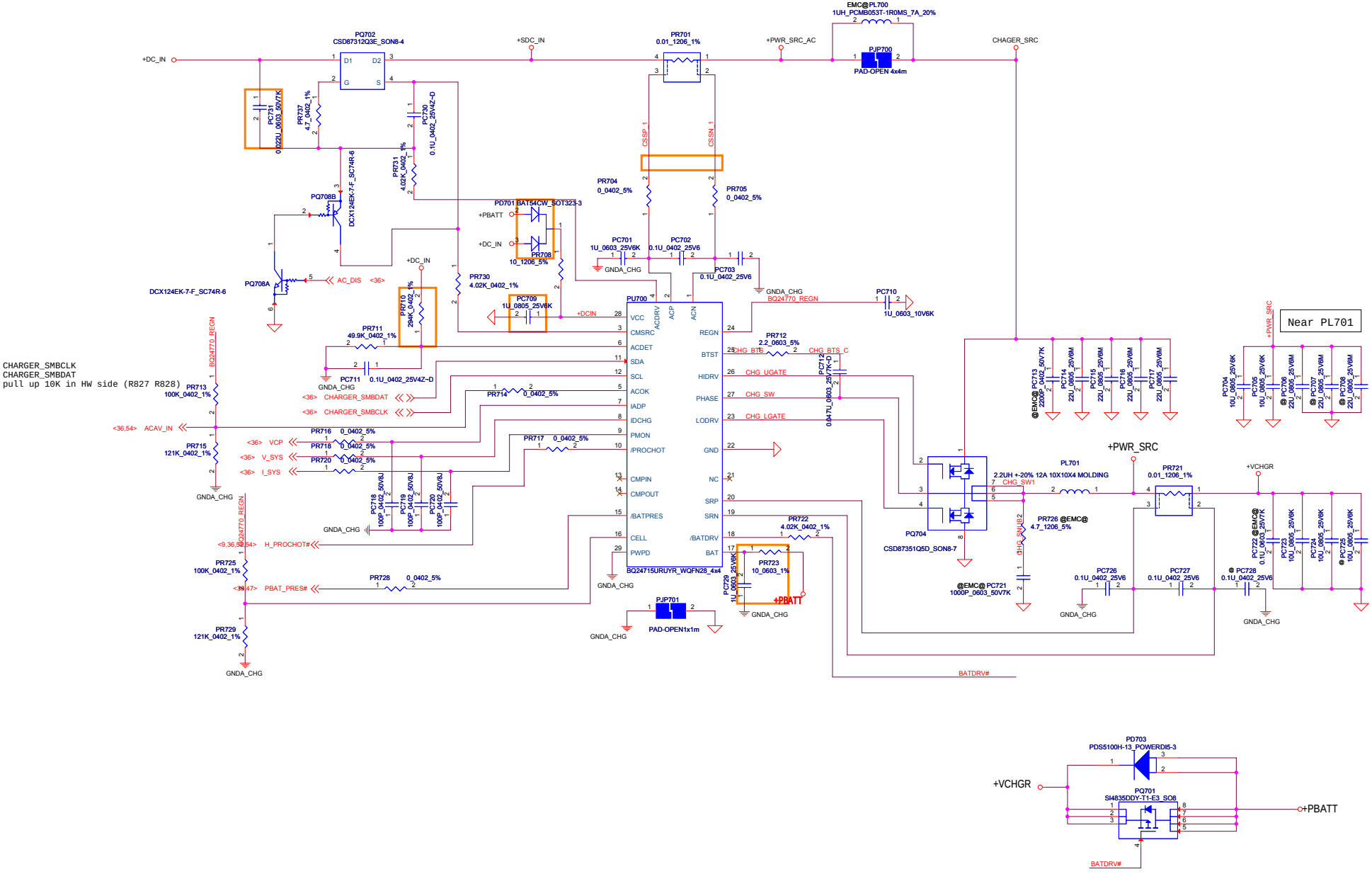

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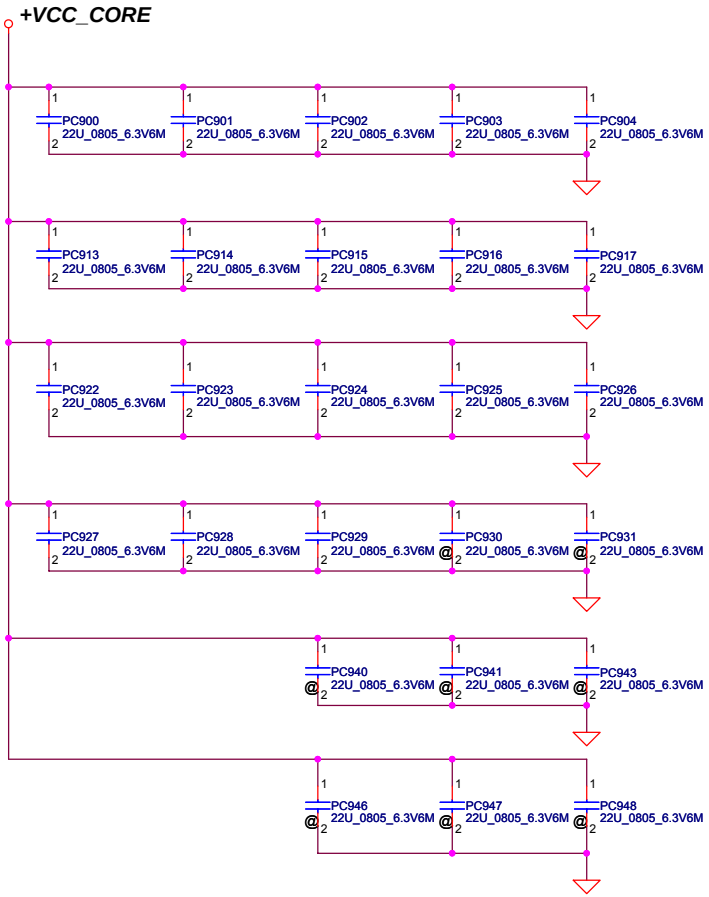
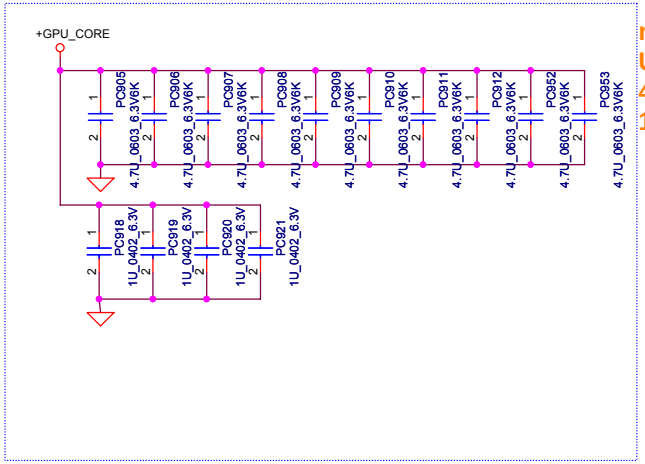
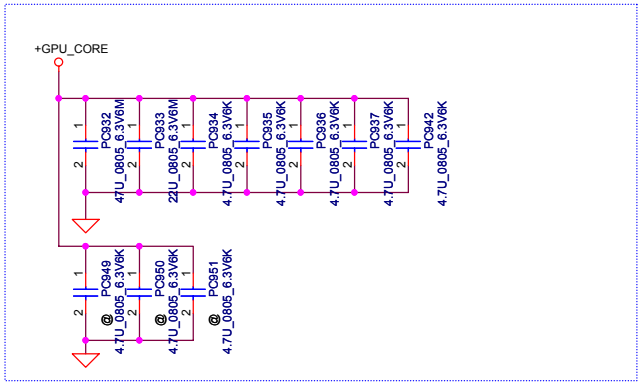




nVidia GB2B-64 package
Under GPU
4.7uF 0603 * 10
1uF 0402 * 4



nVidia GB2B-64 package
Near GPU
47uF 0805 *1
22uF 0805 *1
4.7uF 0805 *5

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