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PICASSO M Schematics Document

Nvdia(T30S) + LPDDRII

QAJA0-LA-8511P

2012-01-18 REV: 1.0

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Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/06/20	Deciphered Date	2012/06/20	Title: Cover Page
				Size: C; Document Number: Picasso 2 R04; Rev: 1.0
				Date: Wednesday, January 18, 2012; Sheet 1 of 38

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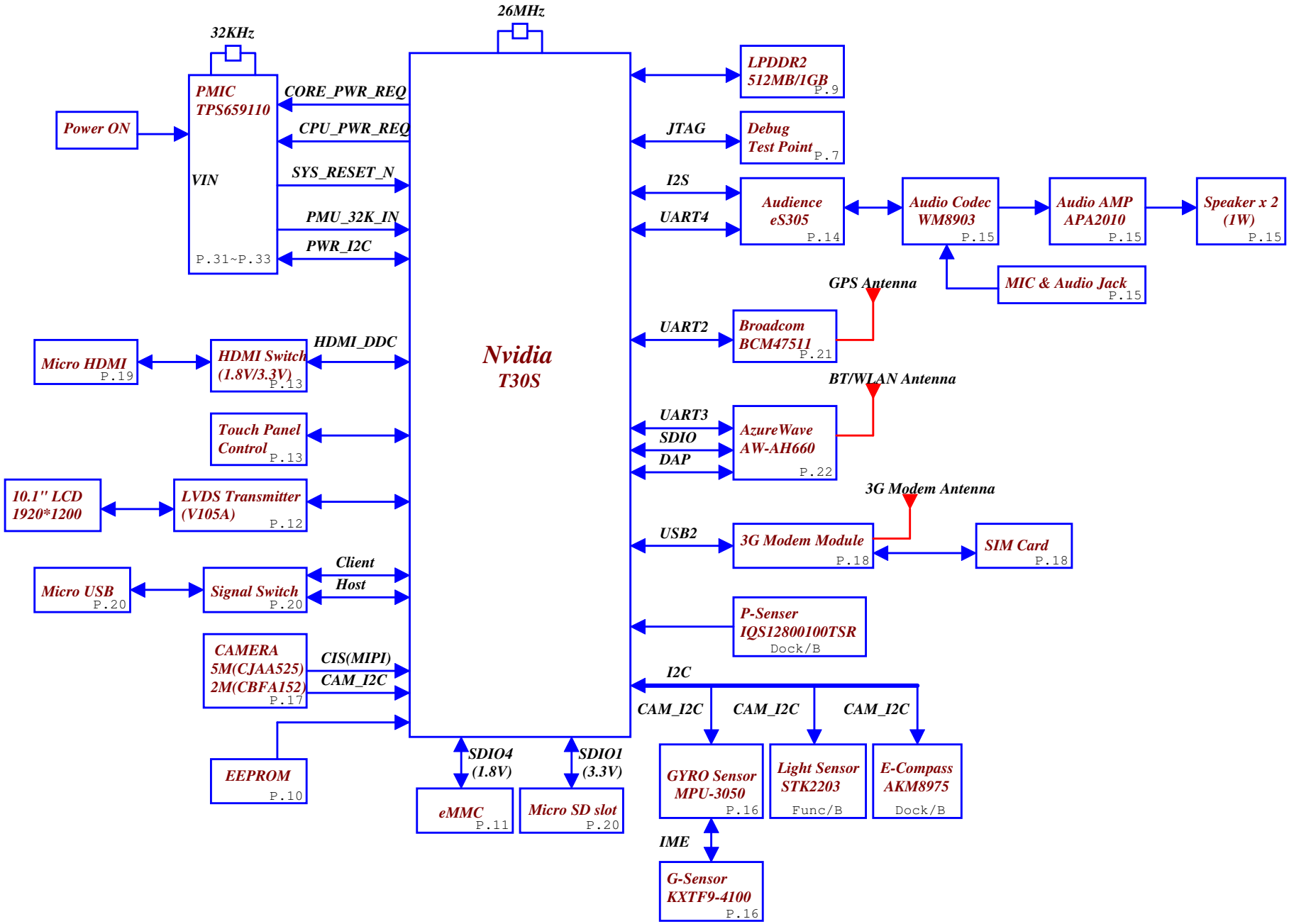
Model Name : NVIDIA T30S System Block Diagram



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				Size: C; Document Number: Picasso 2 R04; Rev: 1.0
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Voltage Rails

Power Plane	Description
VIN	Adapter power supply (19V)
B+	AC or battery power rail for power circuit.
+VDD_1V2_RTC_TEGRA	Power for RTC and always-on core logic.
VDD_1V2_SOC	Power for remainder of core logic
+AVDD_1V1_PLL_TEGRA	AVDD_PLL power rail
+VDD_1V8_PMU_VRTC	RTC power rail
+VDD_1V8_SYS_TEGRA	System power rail
+AVDD_3V3_USB_TEGRA	USB power rail
+VDD_2V85_EMMC	Core voltage for EMMC
+VDD_1V8_CAM_TEGRA	Core voltage for CAMERA
+AVDD_3V3_HDMI_S	HDMI power rail
VDD_1V8_GEN	1.8V switched power rail for standby mode
+VDD_3V3_DDR_RX_TEGRA	DDR RX power rail
+3VS	3.3V switched power rail for standby mode
+5VS	5V switched power rail for standby mode
+VDD_LED_BL	LED power rail
+VDD_3V3_SDMMC1_TEGRA	Micro SD power rail
+VDD_VCM_3V3	CAMERA power rail
+VDD_1V2_DDR_MEM	DDR power rail

GEN1_I2C <+VDD_1V8_SENSOR >

Device	Address<Write,Read>
Gyro	0xD0 , 0xD1
E Compass	0x18 , 0x19
Light Senser	0x38 , 0x39

GEN2_I2C / TS_I2C < +VDD_3V3_GMI_TEGRA >

Device	Address<Write,Read>
Touch Screen	0x98 , 0x99

CAM_I2C < +VDD_1V8_CAM_TEGRA >

Device	Address<Write,Read>
Camera 5M	0x78 , 0x79
Camera 2M	0x20 , 0x21
Flash LED	0x66 , 0x67

PWR_I2C < +VDD_1V8_SYS_TEGRA>

Device	Address<Write,Read>
Thermal Senser	0x98 , 0x99
ES305	0x3E
Codec	0x34 , 0x35
PMU	0x2D
TPS62361	0x60
BATT Conn	0xAA , 0xAB
EEPROM (Low level)	0xA0 , 0xA1
EEPROM (High level)	0xA2 , 0xA3

Board ID

PICASSO 2

EVT	QAJ50(2-6-2)		QAJ70(3-4-3)			
SKU	SKU1(3G only)	SKU1-1(WIFI&3G)	SKU2(3G only)	SKU2-1(WIFI&3G)		
WIFI/BT	NH660	AH662	NH660	AH662		
PCB_ID0	L	L	H	H	L : 262	H : 343
PCB_ID1	L	H	L	H	L : AH663	H : NH660
PCB_ID2	L	L	L	L	L: NON LTE	H: LTE
BOARD_ID0	L	L	L	L		
BOARD_ID1	L	L	L	L	00:EVT	

DVT1	QAJ50(2-6-2)		QAJ70(3-4-3)				
SKU	SKU1(WIFI only)	SKU2(WIFI only)	SKU3((WIFI&3G))	SKU4(WIFI&3G)	SKU5(WIFI& LTE)		
WIFI/BT	AW-AH663	AW-NH660	AW-NH660	AW-AH663	AW-AH663		
PCB_ID0	L	L	H	H	H	L : 262	H : 343
PCB_ID1	L	H	H	L	L	L : AH663	H : NH660
PCB_ID2	L	L	L	L	H	L: NON LTE	H: LTE
BOARD_ID0	H	H	H	H	H		
BOARD_ID1	L	L	L	L	L	01:DVT1	

DVT2	QAJ50(2-6-2)									
SKU	SKU1(WIFI only)	SKU2(WIFI only)	SKU3(WIFI only)	SKU4(WIFI only)	SKU5(WIFI only)	SKU6(WIFI only)	SKU7(WIFI only)	SKU8(WIFI only)		
WIFI/BT	AW-AH663	AW-AH663	AW-AH663	AW-AH663	AW-AH663	AW-AH663	AW-AH663	AW-AH663		
PCB_ID0	L	L	L	L	L	L	L	L	L : 262	H : 343
PCB_ID1	L	L	L	L	L	L	L	L	L : AH663	H : NH660
PCB_ID2	L	L	L	L	L	L	L	L	L: NON LTE	H: LTE
U1.J37	L	L	L	L	L	L	L	L	L: Picasso 2	H:Picasso M
BOARD_ID0	L	L	L	L	L	L	L	L		
BOARD_ID1	H	H	H	H	H	H	H	H	10:DVT2	
DVT2	QAJ70(3-4-3)									
SKU	SKU9(WIFI&3G)	SKU10(WIFI&3G)	SKU11(WIFI&3G)	SKU12(WIFI&3G)	SKU13(WIFI& LTE)	SKU14(WIFI& LTE)				
WIFI/BT	AW-AH663	AW-AH663	AW-AH663	AW-AH663	AW-AH663	AW-AH663				
PCB_ID0	H	H	H	H	H	H	L : 262	H : 343		
PCB_ID1	L	L	L	L	L	L	L : AH663	H : NH660		
PCB_ID2	L	L	L	L	H	H	L: NON LTE	H: LTE		
U1.R37	L	L	L	L	L	L	L: Picasso 2	H:Picasso M		
BOARD_ID0	L	L	L	L	L	L				
BOARD_ID1	H	H	H	H	H	H	10:DVT2			

PICASSO M

EVT	QAJA0(2-6-2)		
SKU	SKU1(Wifi only)		
PCB_ID0	L	L : 262	H : 343
PCB_ID1	H	L : AH663	H : NH660
PCB_ID2	L	L: NON LTE	H: LTE
U1.J37	H	L: Picasso 2	H:Picasso M
BOARD_ID0	L		
BOARD_ID1	L	00:EVT	

DVT	QAJA0(2-6-2)		
SKU	SKU1(Wifi only)		
PCB_ID0	L	L : 262	H : 343
PCB_ID1	H	L : AH663	H : NH660
PCB_ID2	L	L: NON LTE	H: LTE
U1.J37	H	L: Picasso 2	H:Picasso M
BOARD_ID0	L		
BOARD_ID1	L	00:EVT(R01)	

DVT2	QAJA0(2-6-2)		
SKU	SKU1(Wifi only)		
PCB_ID0	L	L : 262	H : 343
PCB_ID1	H	L : AH663	H : NH660
PCB_ID2	L	L: NON LTE	H: LTE
U1.J37	H	L: Picasso 2	H:Picasso M
BOARD_ID0	1		
BOARD_ID1	L	01:DVT(R02)	

LPDDR2

	Vendor PN	Acer PN	Compal PN	Assign Bit	NAND_D4	NAND_D5	
LPDDR2	EDB8132B2MA-1D-F	IC.0080E.002	SA000050Z10	00	0	0	ELP_1GB@
	K4P8G304EB-FGC2	IC.00809.002	SA00004YY20	01	1	0	SAM_1GB@

LVDS strap pin

	LVDS_CTRL2	LVDS_CTRL1	LVDS_CTRL0	LVDS_MAP	LCD_PCLK	LVDS_ACLK
PicassoM	L	H	H	H	70.34Mhz	71.56MHz
Picasso2	L	H	L	L	152.28Mhz	76.14Mhz

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Title: Notes List

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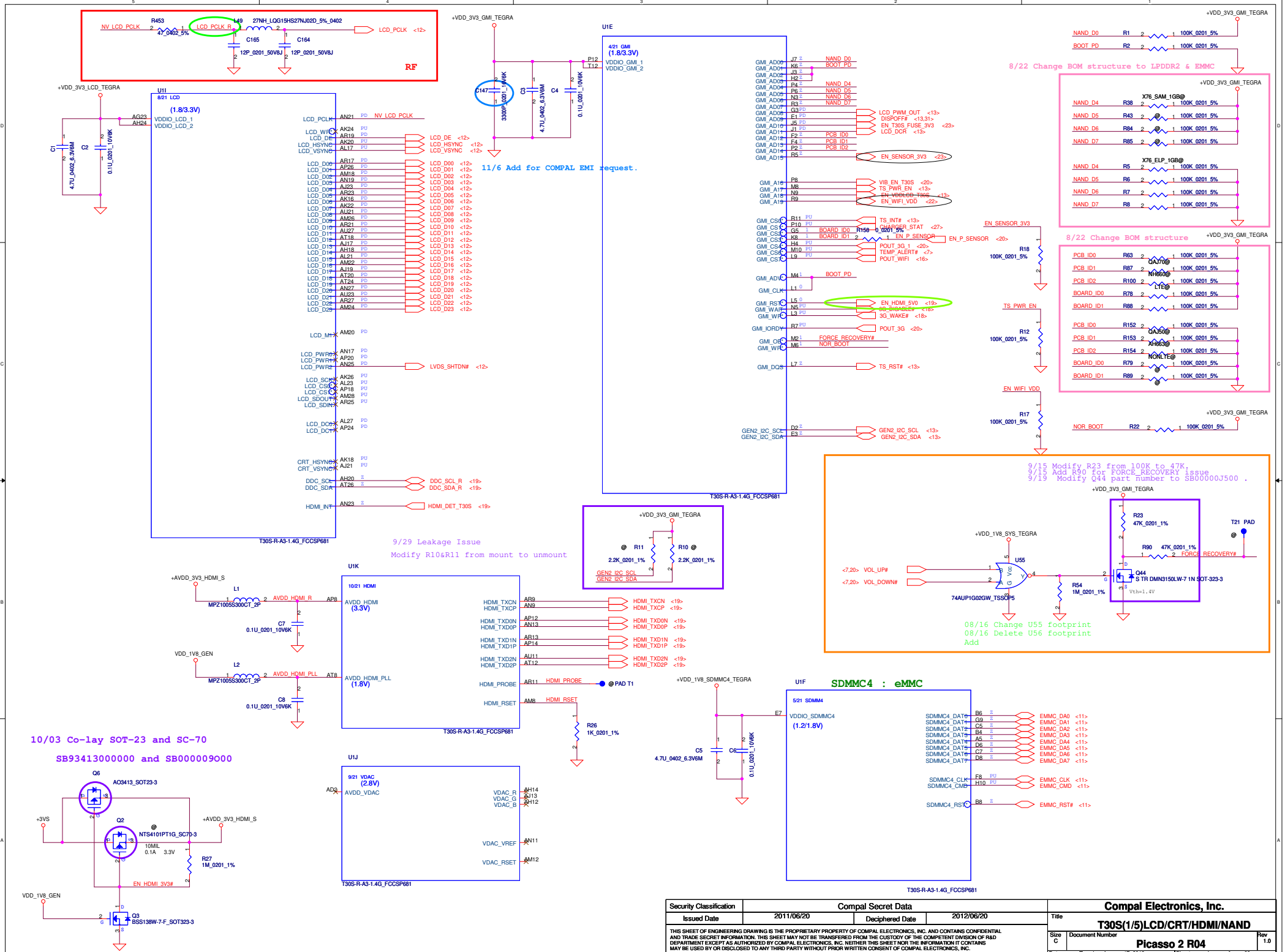

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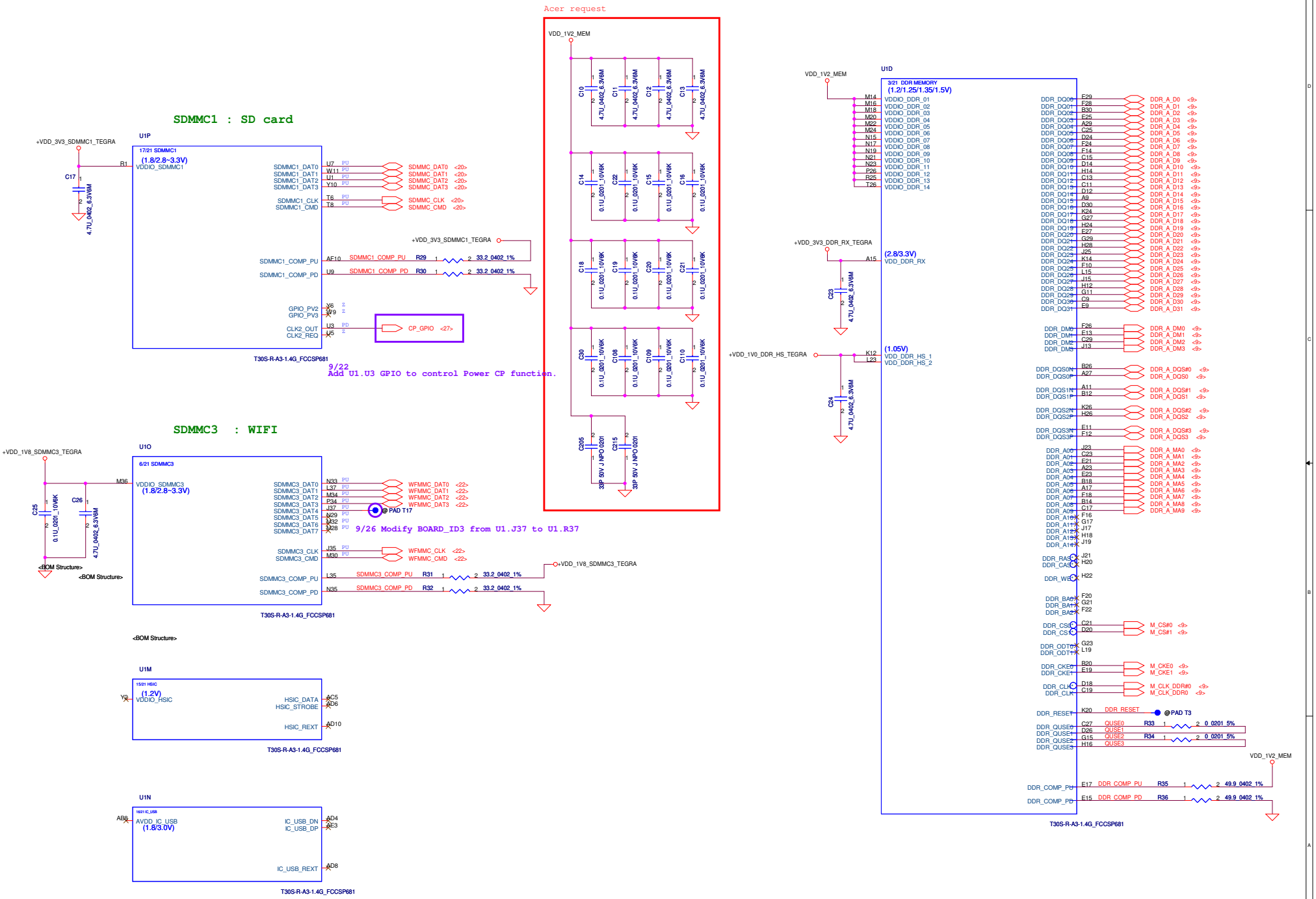

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Title: **T30S(2/5)OSC/PLL/SYS/DDR**

Size	Document Number	Rev
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U1Q is not place on grid , need check connection

RF note

8/24 Modify Off-Page type.

10/24 Add BATT_LEARN GPIO to Power request.

10/03 Add D18 on +T30S_USB1 to protect CPU.

10/19 Modify D18 from +T30S_USB1 to VBUS_USB

12/2 Modify D18 from moun to @,Add Zener on samll board.

SC400003Z00

USB VBUS overvoltage protection

9/26 Swap U1.AM16 to U1.AM10 for WAKE UP issue

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Compal Electronics, Inc.

Title: **T30S(3/5)USB/SDIO/UART/AUDIO**

Size: C | Document Number: **Picasso 2 R04** | Rev: 1.0

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8/25 Modify C36&C37 from 12P to 8P.
10/11 Modify C36&C37 from 8P to 10P.

+VDD_1V8_SENSOR

+VDD_1V8_UART_TEGRA

U1R

14/21 UART

(1.8/3.3V) VDDIO_UART

Open Drain

GEN1_I2C_SCL AH30 — GEN1_I2C_SCL <16,20>
GEN1_I2C_SDA AF29 — GEN1_I2C_SDA <16,20>

UART2_TXD AN35 — GPS_UART_TXD <21>
UART2_RXD AG29 — GPS_UART_RXD <21>
UART2_RTS AG31 — GPS_UART_RTS# <21>
UART2_CTS AJ31 — GPS_UART_CTS# <21>

UART3_TXD AE33 — BT_UART_TXD <22>
UART3_RXD AJ35 — BT_UART_RXD <22>
UART3_RTS AK36 — BT_UART_RTS# <22>
UART3_CTS AJ37 — BT_UART_CTS# <22>

GPIO_PU0 AK34 — BT_RST# <22>
GPIO_PU1 AF36 — EN_3V3_MODEM <18,30>
GPIO_PU2 AN37 — GPS_PWRON <21>
GPIO_PU3 AG33 — GPS_RESET# <18,21>
GPIO_PU4 AM36
GPIO_PU5 AG37 — DEBUG_UART1_RX_R — R149 0_0201_5% — DEBUG_UART1_RX <20>
GPIO_PU6 AJ33 — BT_PD# <22>

DAP4_DIN AF34 — BT_PCM_IN <22>
DAP4_DOUT AG35 — BT_PCM_OUT <22>
DAP4_FS AF28 — BT_PCM_SYNC <22>
DAP4_SCLK AL35 — BT_PCM_CLK <22>

CLK3_OUT AH32 — CLK_12M_ES305 <14>
CLK3_REQ AF32

T30S-R-A3-1.4G_FCCSP681

R46 2.2K_0201_1% — R47 2.2K_0201_1%

C38 0.1U_0201_10V6K

BT_RST# — R56 100K_0201_5%
GPS_RESET# — R75 100K_0201_5%

32> PMU_OSC32KIN — Y1 — PMU_OSC32KOUT <32>
32.768KHZ_12.5P_1TJF125DP1A000D

For PMU RTCCLK , Load BOM 屬於HW料.

+VDD_1V8_SYS_TEGRA
R48 100K_0201_5% — R49 100K_0201_5%
CORE_PWR_REQ
CPU_PWR_REQ

T30S_XTAL_IN — R50 2M_0201_5% — T30S_XTAL_OUT
Y10 26MHZ_10PF_7M26000039
C36 10P_0201_50V8J
C37 10P_0201_50V8J

9/22
Change EN_3V3_MODEM from AE35 to AF36.
9/26
Change BT_PD# from Y36 to AJ33

VDD_1V8_GEN — L3 MPZ1005S300CT_2P — AVDD_OSC P36 — C39 4.7U_0402_6.3V6M

U1T

19/21 PEX

(1.05V) AVDD_PEXB — AN29
(1.05V) VDD_PEXB — AM30
(1.05V) AVDD_PEX_PLL — AN31
(3.3V) HVDD_PEX — AL29
(3.3V) VDDIO_PEX_CTL — AK28

PEX_L5_TXN1 AT30
PEX_L5_TXP1 AU29
PEX_L5_RXN1 AP30
PEX_L5_RXP1 AR29
PEX_CLK3N AT34
PEX_CLK3P AR33
PEX_L2_CLKREQ AR31
PEX_L2_PRSNT AT32
PEX_L2_RST AU33
PEX_WAKE AP32
PEX_TERMP AP36

U1U

T30S-R-A3-1.4G_FCCSP681

U1C

2/21 OSC, PLL & SYS

AVDD_OSC (1.8V) — Deep Sleep : OFF
XTAL_IN R33 — T30S_XTAL_IN
XTAL_OUT R35 — T30S_XTAL_OUT

09/15 Add for Acer request.

+VDD_1V8_SYS_TEGRA — R91 100K_0201_5% — LINE_OUT_DET#

+AVDD_1V1_PLL_TEGRA
AVDD_PLLA_P_C_S B24 (1.1V)
AVDD_PLLX K18 (1.1V)
AVDD_PLLM A21 (1.1V)
AVDD_PLLU_D AG5 (1.1V)
AVDD_PLLE AF30 (1.05V)
PLL_S_PLL_LF R27 — PLL_S_PLL_LF — C40 0.1U_0201_10V6K

C41 0.1U_0201_10V6K — C42 0.1U_0201_10V6K

R53 0_0201_5%

+VDD_1V8_SYS_TEGRA — Y32 — C44 0.1U_0201_10V6K

VDDIO_SYS (1.8V) — Deep Sleep : ON

10/19 Modify R51 and R52 to 1K ohm

+VDD_1V8_SYS_TEGRA — R51 1K_0201_1% — R52 1K_0201_1%

PWR_I2C_SCL V36 — PWR_I2C_SCL <10,14,15,26,32,34>
PWR_I2C_SDA V30 — PWR_I2C_SDA <10,14,15,26,32,34>
SYS_RESET U31 — PMU_RESET_OUT_1V8# <32>
PWR_INT P28 — PMU_INT# <32>
CORE_PWR_REQ T32 — CORE_PWR_REQ <27,32>
CPU_PWR_REQ Y34 — CPU_PWR_REQ <32>
SYS_CLK_REQ W27 — SYS_CLK_REQ — @PAD T2
CLK_32K_IN T30 — PMU_CLK_32K <32>
CLK_32K_OUT AB32 — CLK_32K_OUT <22>

KB_COL00 U37 — SC_LOCK# <20>
KB_COL01 U29 — VOL_UP# <4,20>
KB_COL02 AD32 — VOL_DOWN# <4,20>
KB_COL03 AD35 — EN_CAM_2V8 <17>
KB_COL04 AC31 — BOARD_ID_WP <10>
KB_COL05 Y30
KB_COL06 AD30
KB_COL07 W35

9/22 Swap AD36 & W29 GPIO function.
Default pull up& pull down swap

KB_ROW00 AC33 — WAKEUP_LED <27>
KB_ROW01 R37 — PCB_ID3
KB_ROW02 W29 — EN_CAM_1V8# <23>
KB_ROW03 R31
KB_ROW04 U35 — not use Audio LDO
KB_ROW05 V34 — UART_SW <20>
KB_ROW06 U33
KB_ROW07 AE35 — @PAD T10
KB_ROW08 AA35 — SHORT_DET <15>
KB_ROW09 AA37
KB_ROW10 AA29 — WF_WAKE# <22>
KB_ROW11 Y36 — @PAD T14
KB_ROW12 P30 — SD_DET# <20>
KB_ROW13 AC29 — G_ACC_INT <16>
KB_ROW14 P32 — LINE_OUT_DET# <20>
KB_ROW15 AB30 — BT_IRQ# <22>

9/22 Change EN_3V3_MODEM to AF36
08/12 Delete EN_ACCK_USB_CHARGE
9/26 Change BT_PD# to AJ33

PICASSO_M@ R195 10K_0201_5%
PICASSO_2@ R193 10K_0201_5%

JTAG_TCK AA31 — JTAG_TCK — @PAD T4
JTAG_TDI AC35 — JTAG_TDI — @PAD T5
JTAG_TDO Y28 — JTAG_TDO — @PAD T6
JTAG_TMS AA33 — JTAG_TMS — @PAD T7
JTAG_TRST W33 — JTAG_TRST# — @PAD T8
JTAG_RTCK AD34 — JTAG_RTCK — @PAD T9

THERM_DN E31 — NV_THERM_DN
THERM_DP C31 — NV_THERM_DP
OWR R29
HDMI_CEC V32 — HDMI_CEC <19>
TEST_MODE_EN V28 — TEST_MODE_EN

T30S-R-A3-1.4G_FCCSP681

9/26 Change from J37 to R37.

	PICASSO_M	PICASSO_2
PCB_ID3	H	L

9/28 Change Net name from Board_ID3 to PCB_ID3

+VDD_1V8_BB_TEGRA

U1S

12/21 BB

VDDIO_BB (1.8/3.3V) — V6

ULPI_DATA0 AA7 — DEBUG_UART1_TX <20>
ULPI_DATA1 AC7 — DEBUG_UART1_RX <20>
ULPI_DATA2 W8
ULPI_DATA3 AC3 — WAKE_UP_ACIN <27>
ULPI_DATA4 V4 — SIM_DET <18>
ULPI_DATA5 AC11
ULPI_DATA6 AF6
ULPI_DATA7 AA9

ULPI_CLK AC1 — AUDIO_UART1_TX <14>
ULPI_DIR W3 — AUDIO_UART4_RX <14>
ULPI_NXT AC9 — EN_VDD_GPS <21>
ULPI_STP V10 — EN_SENSOR_1V8# <23>

DAP3_DIN AA1 — CAM_LED_EN_NV <35>
DAP3_DOUT W5 — WF_RST# <22>
DAP3_FS Y4 — BT_WAKEUP <22>
DAP3_SCLK AA3 — EN_SENSOR_3V3_2 <23>

9/27
ADD EN_SENSOR_3V3_2 to U1.AA3

GPIO_PV0 Y8 — ON_KEY#
GPIO_PV1 AA5 — WAKE_UP_VBUS <27>

T30S-R-A3-1.4G_FCCSP681

C43 0.1U_0201_10V6K

+VDD_1V8_BB_TEGRA — R164 100K_0201_5%

D20 RB751V-40_SOD323-2 — ON_KEY# — ONKEY# <20,32>

2021 SPARE

SPARE_1 AC27
SPARE_2 AD28
SPARE_3 AG19
SPARE_4 AL33
SPARE_5 AM34

T30S-R-A3-1.4G_FCCSP681

+VDD_1V8_SYS_TEGRA

JDBUG1 ACES_87036-1001-CP CONN@

JTAG_TRST# 2
JTAG_TDI 3
JTAG_TMS 4
JTAG_TCK 5
JTAG_RTCK 6
JTAG_TDO 7
8
9
ONKEY# 10
11 GND
12 GND

<20> HOT_RST#

+VDD_1V8_SYS_TEGRA

JTAG_TDI R155 — 10K_0201_5%
JTAG_TMS R159 — 10K_0201_5%
JTAG_RTCK R160 — 10K_0201_5%
JTAG_TCK R161 — 100K_0201_5%
JTAG_TRST# R162 — 100K_0201_5%

+3VS — R57 49.9_0402_1% — C45 0.1U_0201_10V6K — +3VS_TH

VDD_1V8_PMU_VRTC — R58 100K_0201_5% — R60 100K_0201_5%

max current is 350uA
VR1 =17mV

NV_THERM_DP — R59 100_0201_1% — THERMD_F_P
C46 1000P_0201_16V7K
NV_THERM_DN — R61 100_0201_1% — THERMD_F_N

<10,14,15,26,32,34> PWR_I2C_SCL
<10,14,15,26,32,34> PWR_I2C_SDA

U4 NCT1008CMT3R2G_WDFN8_2X2
D+ VDD
D- THERM# / ALERT#
SCL GND
SDA

AP_OVERHEAT# <32>
TEMP_ALERT# <4>

Thermal

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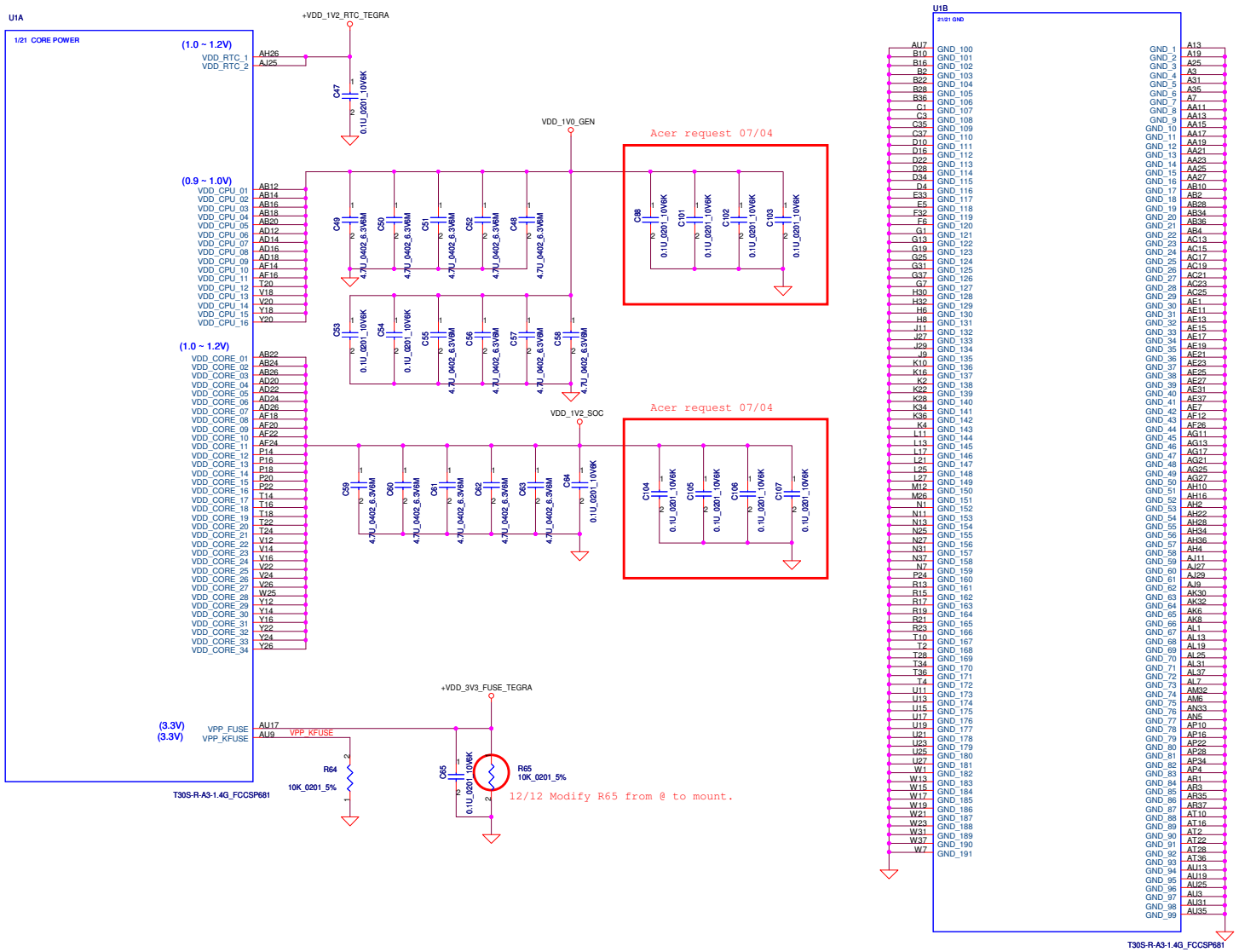
Security Classification	Compal Secret Data		
Issued Date	2011/06/20	Deciphered Date	2012/06/20

Compal Electronics, Inc.

Title: T30S(4/5) UART/OSC/PLL

Size: C | Document Number: Picasso 2 R04 | Rev: 1.0

Date: Tuesday, January 17, 2012 | Sheet 7 of 38



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/06/20	Deciphered Date	2012/06/20	Title: T30S(5/5)PWR_GND_NC
				Size: C; Document Number: Picasso 2 R04; Rev: 1.0
				Date: Tuesday, January 17, 2012; Sheet 8 of 38

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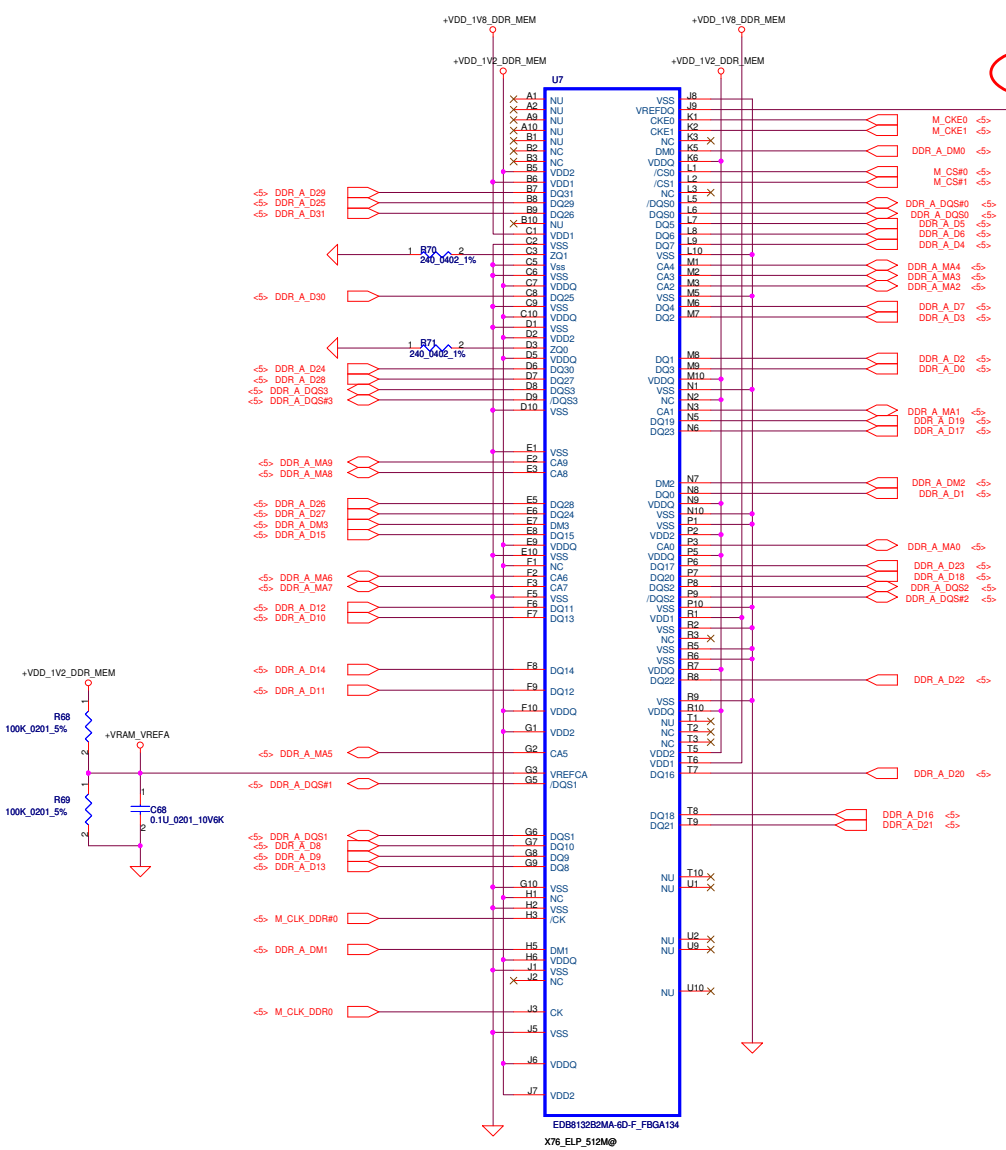
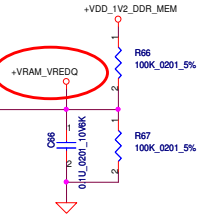
Follow NV design

NET NAME	BALL NAME
A0	P3
A1	N3
A2	M3
A3	M2
A4	M1
A5	G2
A6	F2
A7	F3
A8	E3
A9	E2
CKE0	K1
CKE1	K2
CLK	J3
CLK#	H3
CS0	L1
CS1	L2
DM0	K5
DM1	H5
DQ0	M9
DQ1	N8
DQ10	F7
DQ11	F9
DQ12	F6
DQ13	G9
DQ14	F8
DQ15	E8
DQ2	M8
DQ3	M7
DQ4	L9
DQ5	L7
DQ6	L8
DQ7	M6
DQ8	G7
DQ9	G8
DQS0	L6
DQS0#	L5
DQS1	G6
DQS1#	G5

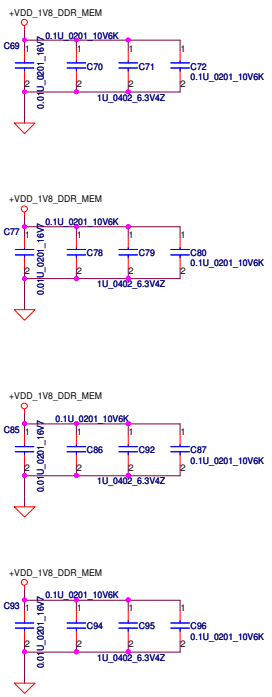
Layer 2

DM2	N7
DM3	E7
DQ16	T8
DQ17	N6
DQ18	P7
DQ19	N5
DQ20	T7
DQ21	T9
DQ22	R8
DQ23	P6
DQ24	D6
DQ25	B8
DQ26	E5
DQ27	E6
DQ28	D7
DQ29	B7
DQ30	C8
DQ31	B9
DQS2	P8
DQS2#	P9
DQS3	D8
DQS3#	D9

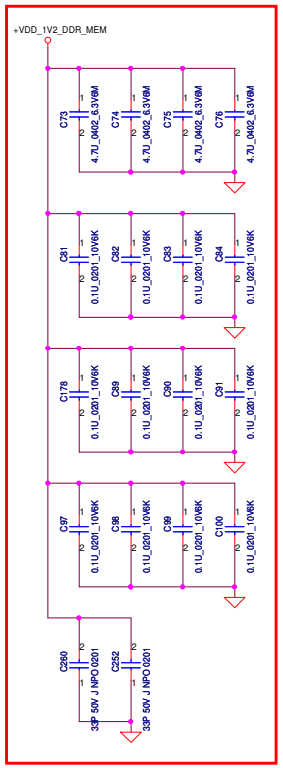




F1,H1,N2 are the NC pins which assembled/embedded the interconnection into ELP Vdd sources already. due to co-layout the LPDDR2, it is need to apply 1.2 volt on F1, H1 and N2 pins.



Acer request



U7 X76_SAM_1GB@ SA00004YY20 (1GB Samsung)

U7 X76_ELP_1GB@ SA000050Z10 (1GB Elpida)

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/06/20	Deciphered Date	2012/06/20	Title: LPDDRII-DEVICE DOWN
				Size: C; Document Number: Picasso 2 R04; Rev: 1.0
				Date: Wednesday, January 18, 2012; Sheet 9 of 38

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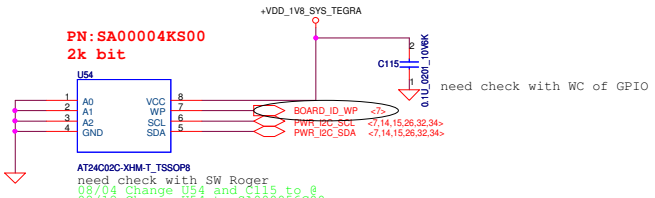
Remove EC



need check with SW Roger
08/04 Change U54 and C115 to 0
08/12 Change U54 to SA000056G00
08/12 Change U54 footprint to AT24C64A-10TQ-2P7_TSSOP8
08/12 Change U54 footprint to AT24C64A-10TQ-2P7_TSSOP9
08/20 Change U54 to SA00004KS00
11/30 Change U54 to SA00005GV00
12/16 Change U54 to SA00004KS00(2K).

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/06/20	Deciphered Date	2012/06/20	Title: EC(Reserved)
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				Date: Tuesday, January 17, 2012; Sheet 10 of 38

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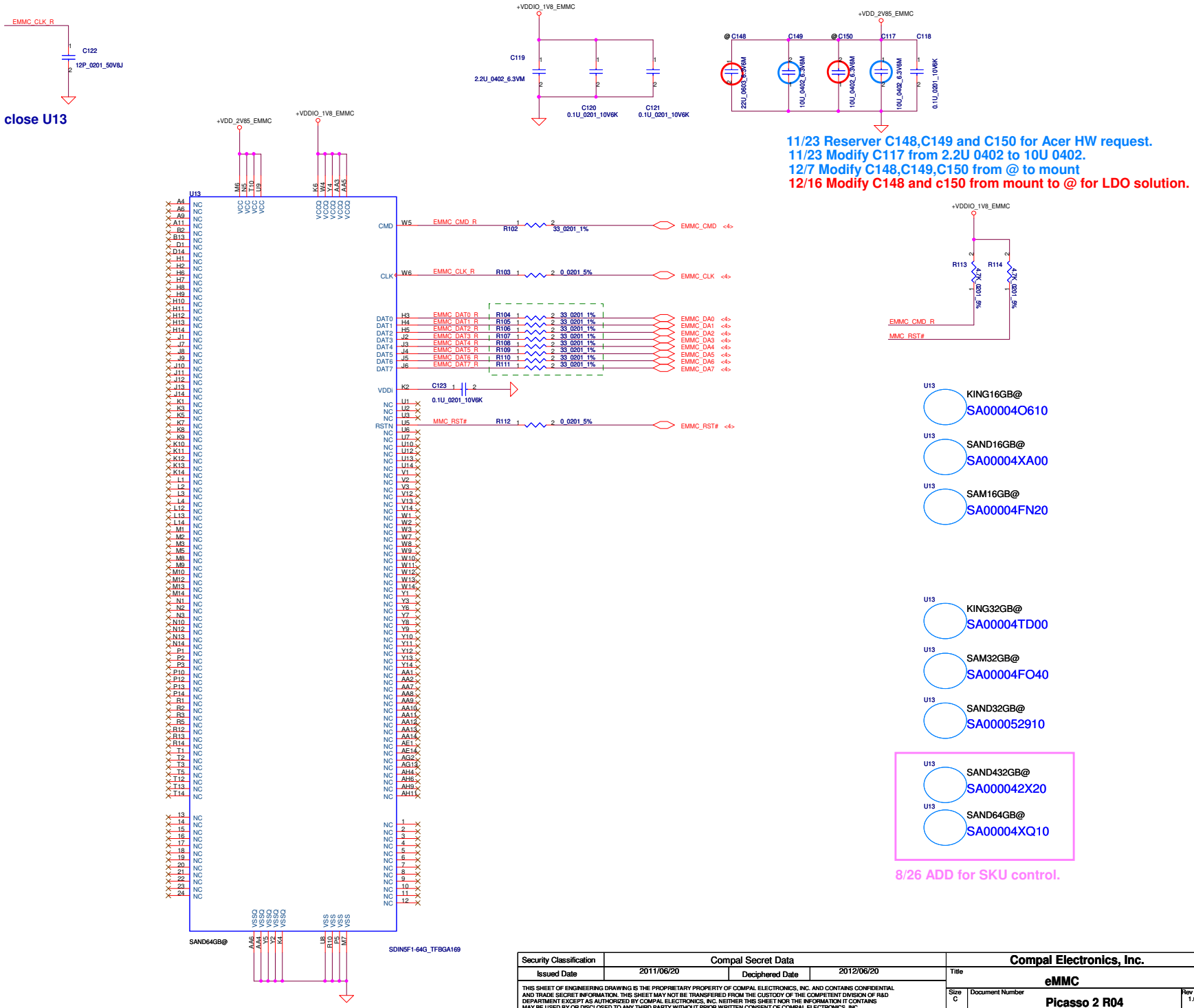

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/06/20	Deciphered Date	2012/06/20	Title: eMMC
				Size: C; Document Number: Picasso 2 R04; Rev: 1.0
				Date: Wednesday, January 18, 2012; Sheet 11 of 38

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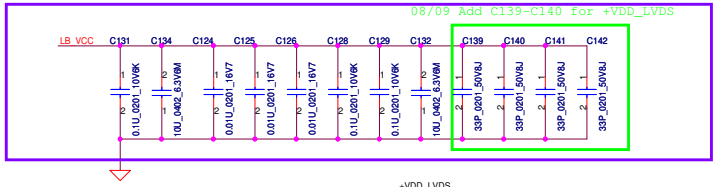
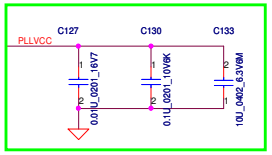
10/03 Modify C125,C126,C128,C129,C132,C139,C140,C141 and C142 from +VDD_LVDS to LB_VCC power domain.

08/09 Add C139-C140 for +VDD_LVDS





10/19 Modify U20 PN from SA000050500 to SA000059A00

09/21 swap LCD_D00~LCD_D23 for colay.

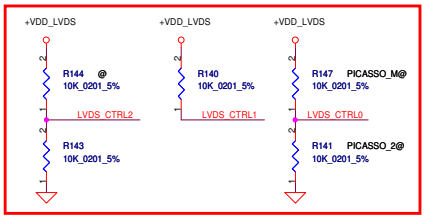
09/21 Add R165 select pin for Picasso M.

LVDS_MAP configuration:
High: Picasso M
Low: Picasso 2

11/11 Add C328,C338,C360 and C364 for Acer RF request.

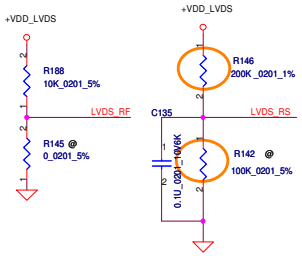
08/12 Add R148 PD LVDS_SHTDN# to GND

need check for single in single out



CTRL[2:0] = LHL	Single-In, Dual-Out (DDR Off)
CTRL[2:0] = HHL	Single-In, Dual-Out (DDR On)

CTRL[2:0] = LHH	Single-In, Single-Out (Distribution Off)
CTRL[2:0] = HHH	Single-In, Single-Out (Distribution On)



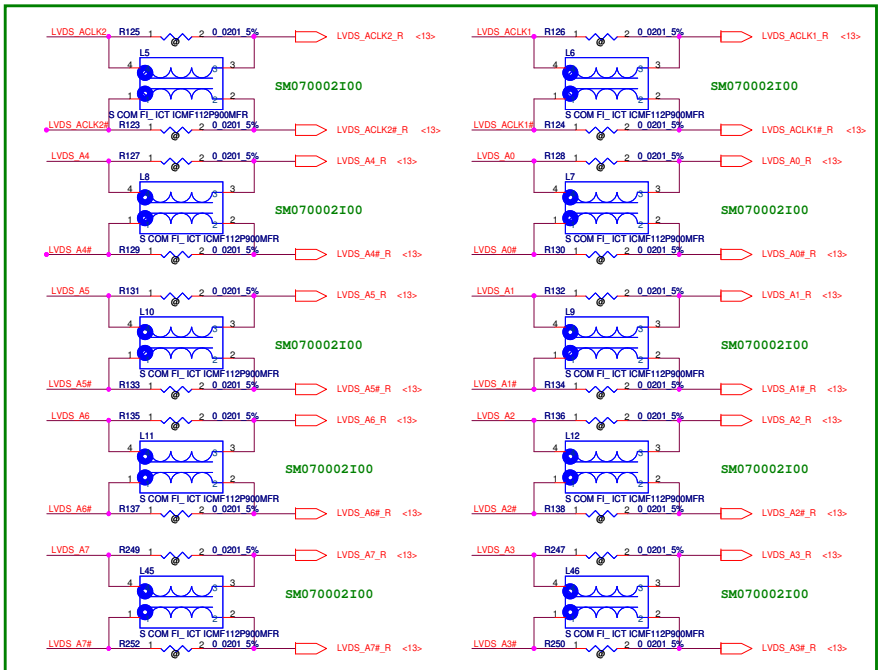
RS Input Voltage	LVDS Output Swing	CMOS/TTL Input Configuration (Input Voltage Swing
VCC	350 mV	Standard Input and Output Configuration
0.6 ~ 1.4 V	350 mV	Small Input Swing, Standard Output Swing Configuration
GND	200 mV	Standard Input Swing, Reduced Output Swing Configuration

10/14 Modify LVDS_RS from pull up to pull down to reduce power consumption.

11/1 Modify LVDS_RS from pull down to pull up to meet SPEC

09/21 Isolated LB_VCC and PLLVCC.

09/26
Change R122 & R156 package from 0201 to 0402



08/05 Change L5-L12,L45,L46 to mount

08/12 Change L5-L12,L45,L46 to SM070002N00

10/17 Chanfe Bead P/N from SM070002N00 to SM070002I00

Close LVDS Transmitter (U20)

Security Classification	Compal Secret Data		
Issued Date	2011/06/20	Deciphered Date	2012/06/20

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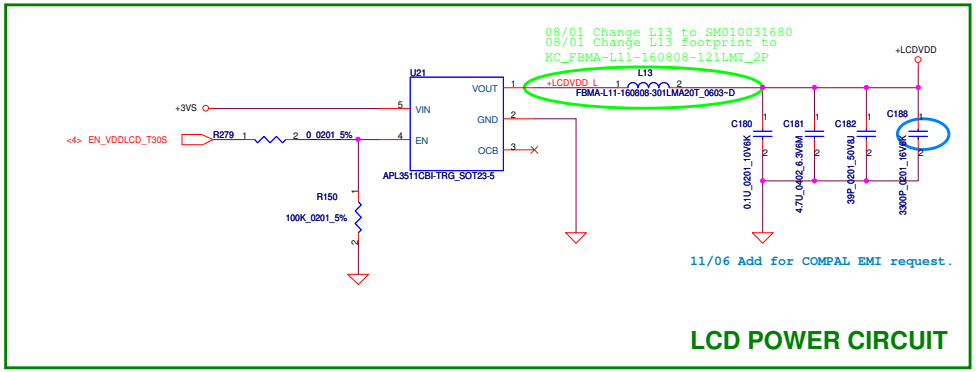
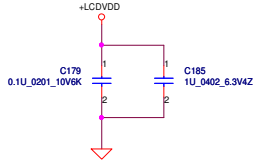
Compal Electronics, Inc.

Title: **LVDS Transmitter**

Size: C | Document Number: **Picasso 2 R04** | Rev: 1.0

Date: Tuesday, January 17, 2012 | Sheet 12 of 38





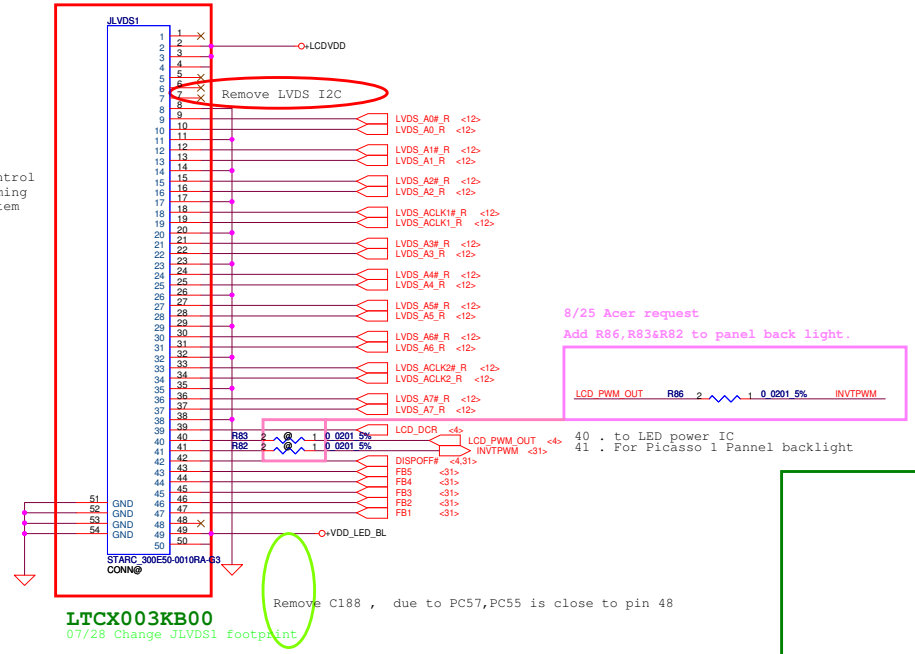
Panel SPEC

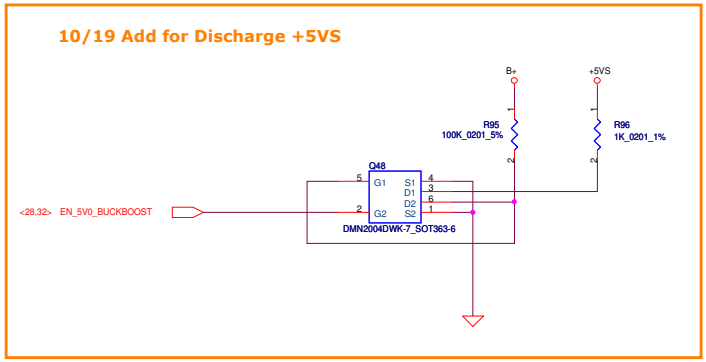
2 VDD Power Supply +3.3V
3 VDD Power Supply +3.3V
4 VDDEDID EDID +3.3V

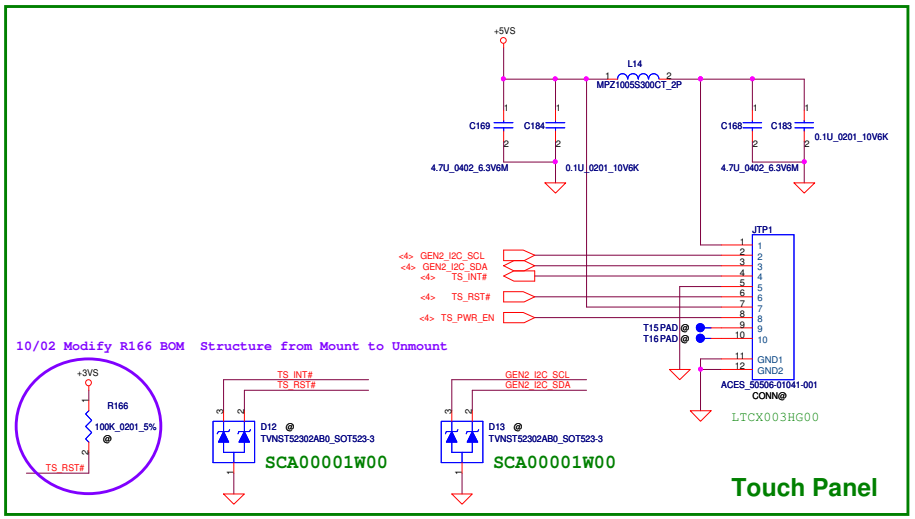
38 DCR_EN (CABC_EN) Dynamic backlight control
39 PWM_IN System PWM signal input for dimming
40 PWM_OUT Panel PWM signal output to system

43 LED_CA5 LED Cathode 5
44 LED_CA4 LED Cathode 4
45 LED_CA3 LED Cathode 3
46 LED_CA2 LED Cathode 2
47 LED_CA1 LED Cathode 1

49 VLED Output LED Backlight power
50 VLED Output LED Backlight power







Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/06/20	Deciphered Date	2012/06/20	Title: LCD Panel/Touch Panel
				Size: C; Document Number: Picasso 2 R04; Rev: 1.0
				Date: Tuesday, January 17, 2012; Sheet 13 of 38

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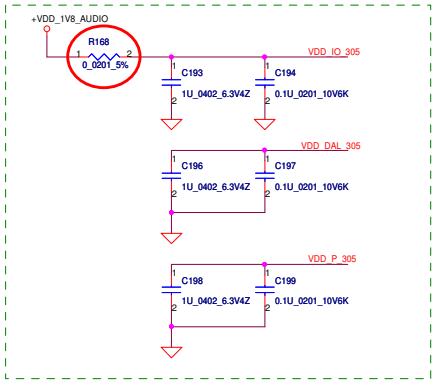
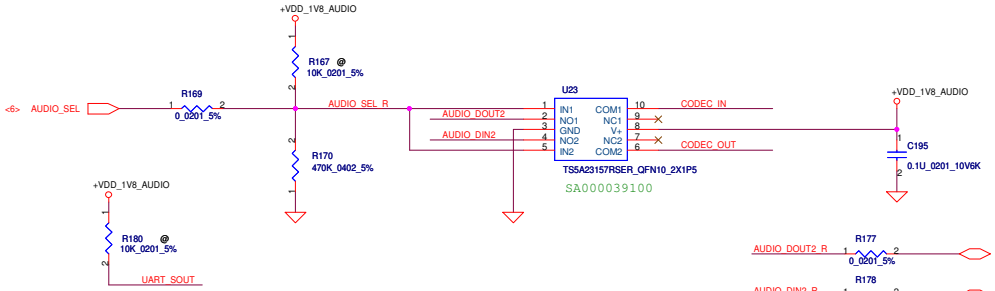
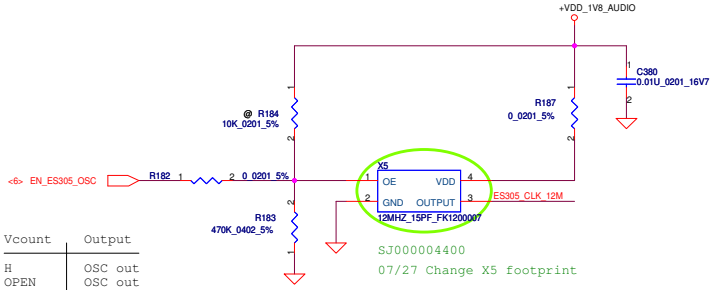
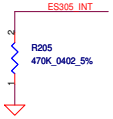


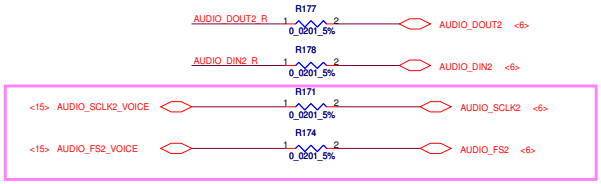


Support for input clock frequencies of 24 MHz and 26 MHz requires a 10kΩ pull-up resistor on the UART_SOUT pin.



Vcount	Output
H	OSC out
OPEN	OSC out
L	High Z

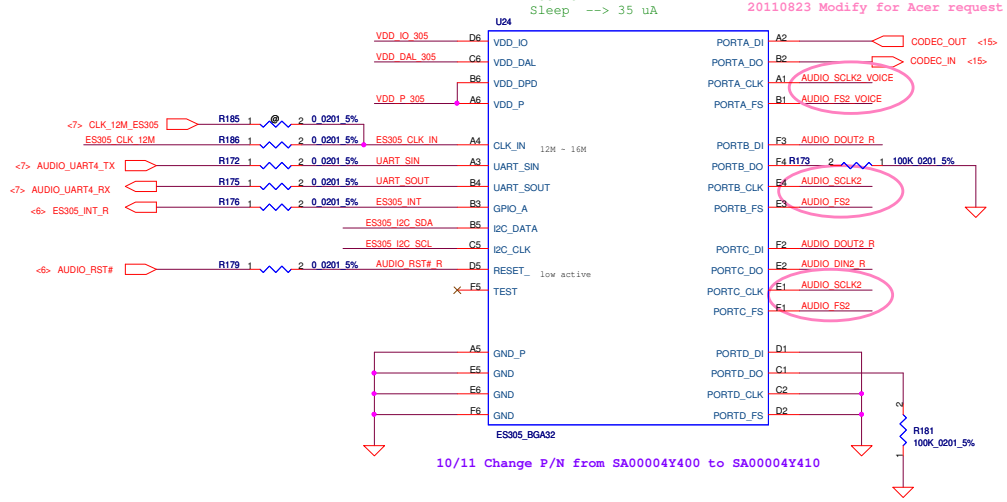




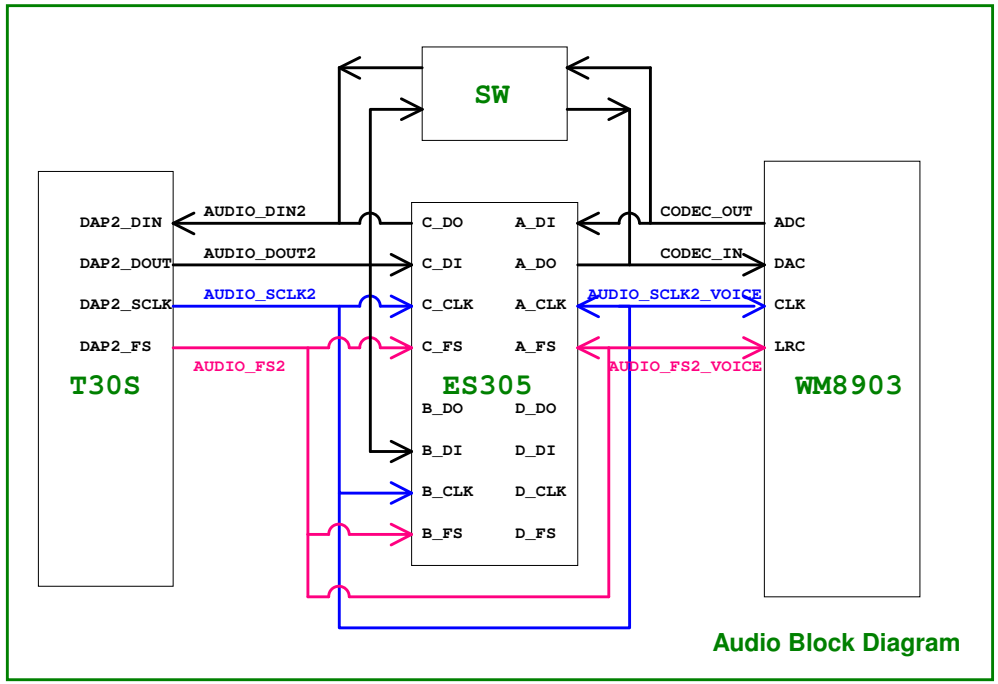
20110823 Modify for Acer request
AUDIO_FS2_VOICE connect to portA and CODEC,
AUDIO_FS2 connect to portB, portC and CPU.
AUDIO_SCLK2_VOICE connect to portA and CODEC
AUDIO_SCLK2 connect to portB, portC and CPU.

Active --> 17 mA
Sleep --> 35 uA

20110823 Modify for Acer request



10/11 Change P/N from SA00004Y400 to SA00004Y410



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/06/20	Deciphered Date	2012/06/20	Title: ES305
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				Date: Tuesday, January 17, 2012; Sheet 14 of 38

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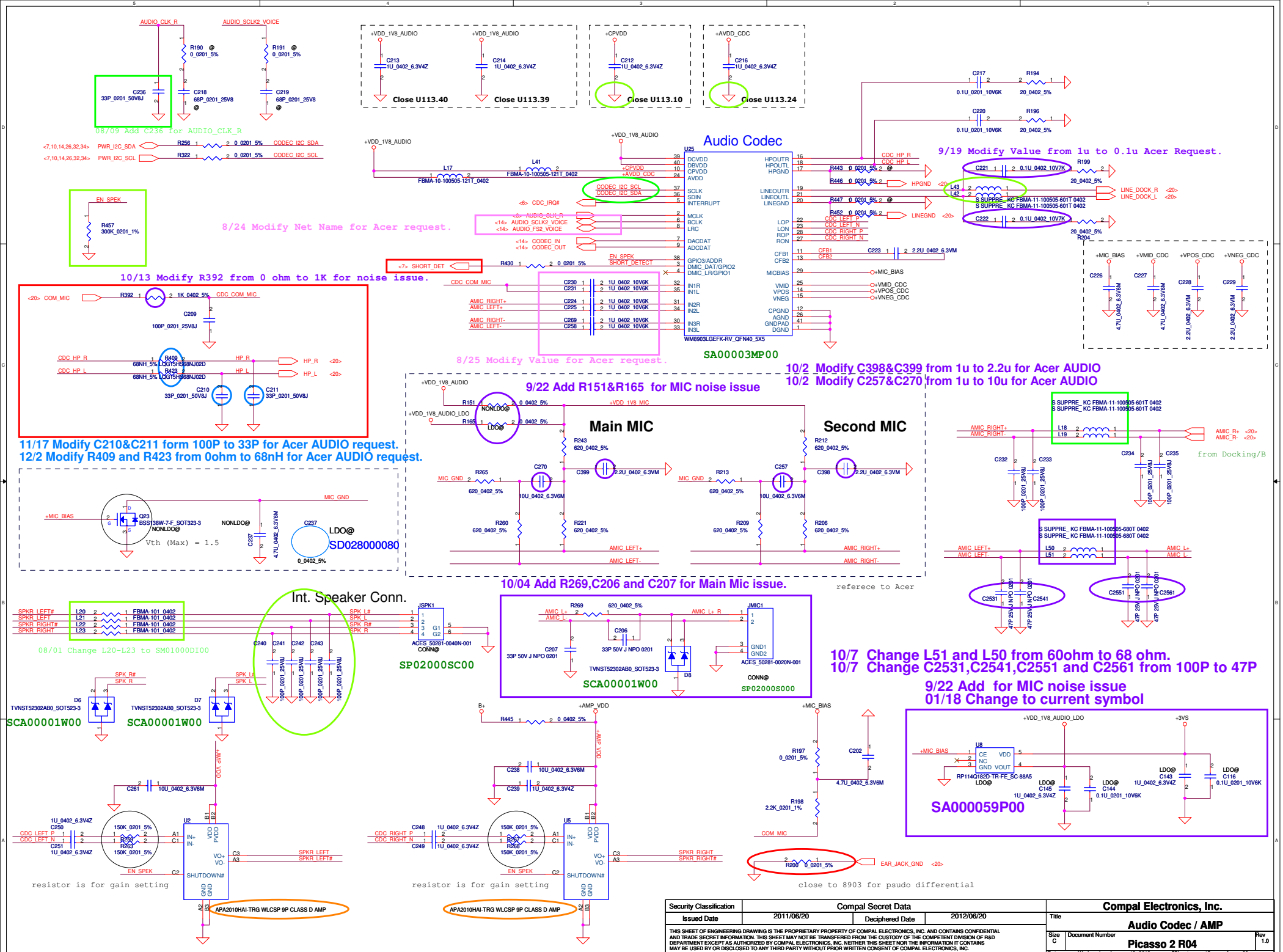

Security Classification	Compal Secret Data		
Issued Date	2011/06/20	Deciphered Date	2012/06/20

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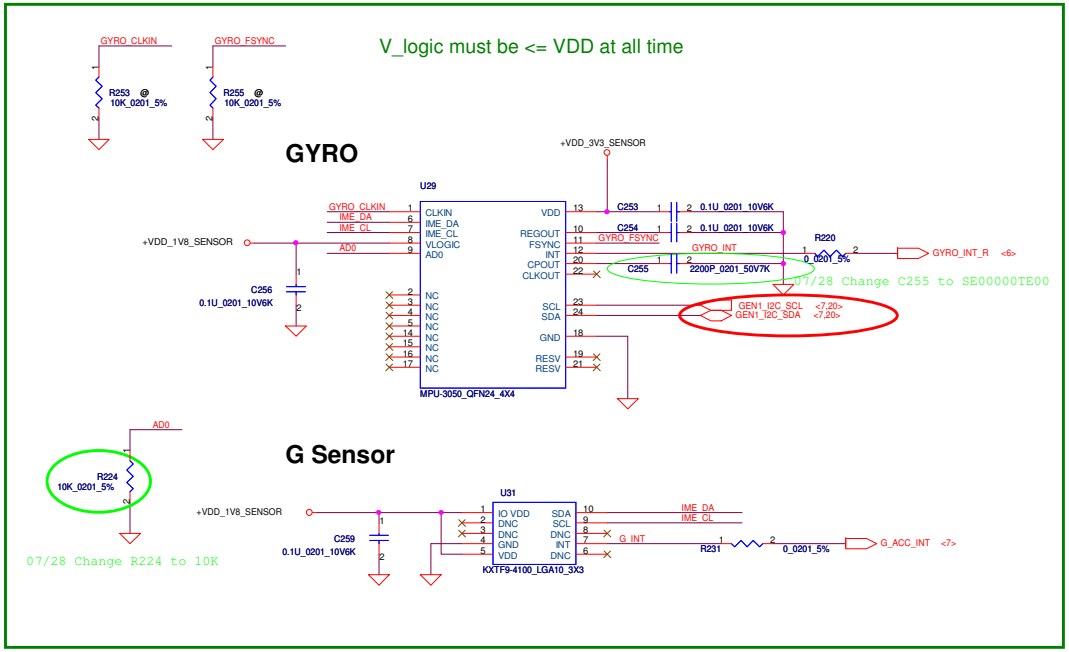
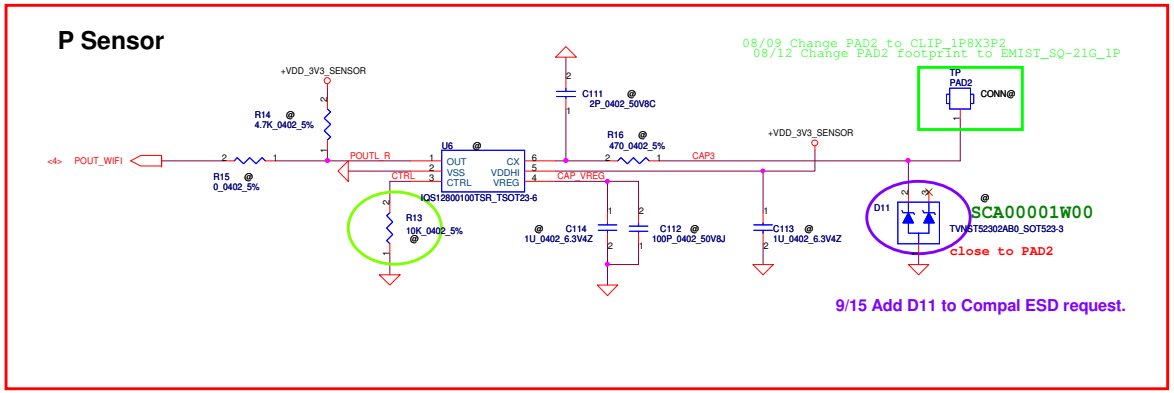
Compal Electronics, Inc.

Title: **Audio Codec / AMP**

Size: C | Document Number: **Picasso 2 R04** | Rev: 1.0

Date: Wednesday, January 18, 2012 | Sheet 15 of 38





10/13 Modify R14,U6,C111,R16,D11,C113,C112 and C114 from WIFI @ to @ .

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/06/20	Deciphered Date	2012/06/20	Title: GYRO/P-Sen/G-Sen
				Size: C; Document Number: Picasso 2 R04; Rev: 1.0
				Date: Tuesday, January 17, 2012; Sheet 16 of 38

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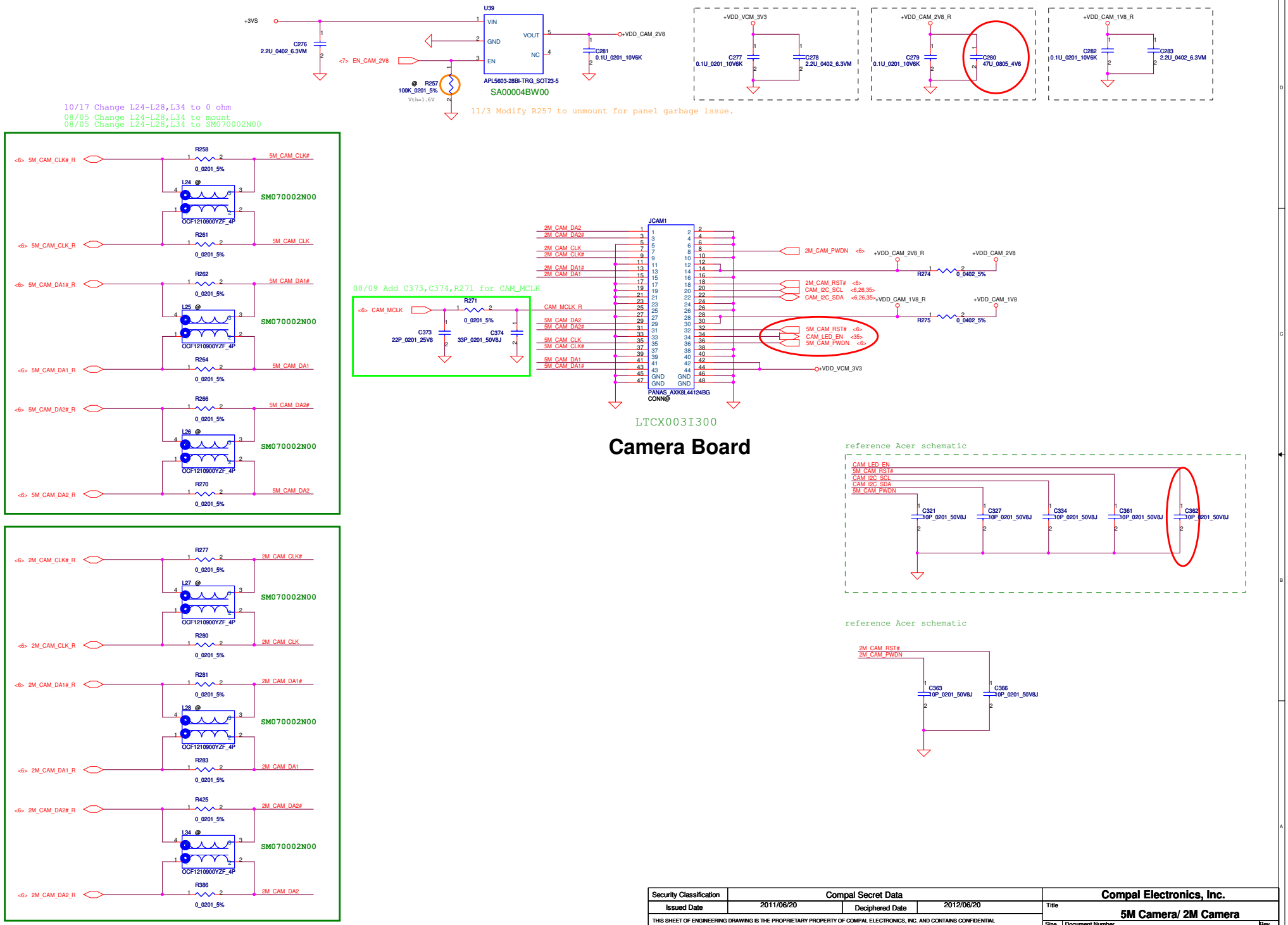

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/06/20	Deciphered Date	2012/06/20	Title: 5M Camera/ 2M Camera
				Size: C; Document Number: Picasso 2 R04; Rev: 1.0
				Date: Tuesday, January 17, 2012; Sheet 17 of 38

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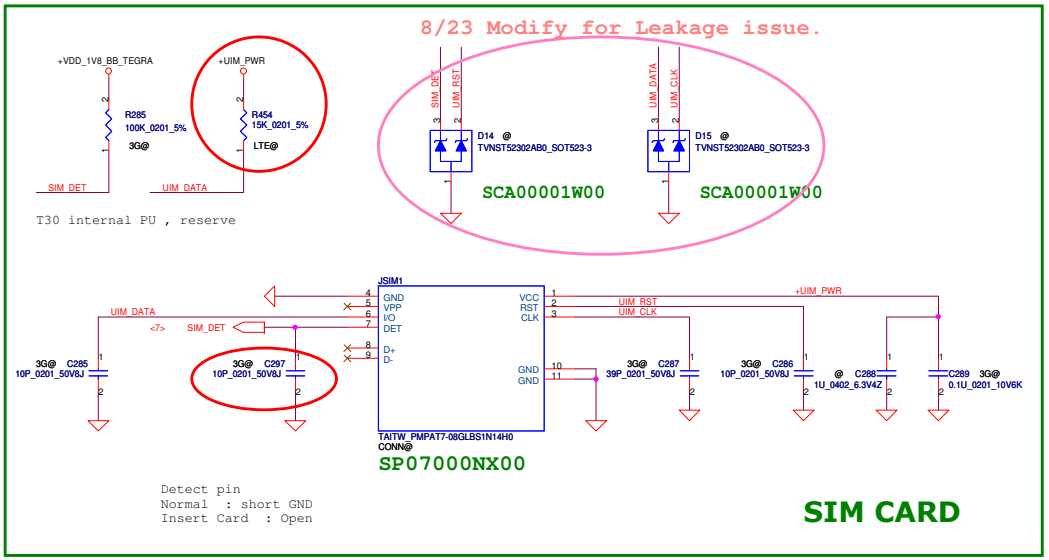
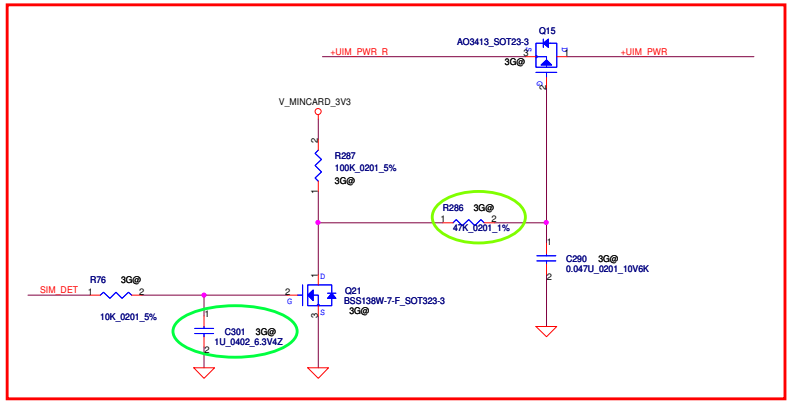
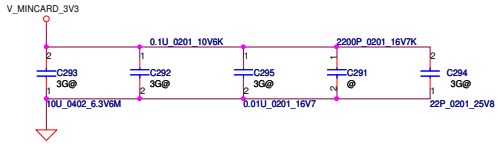
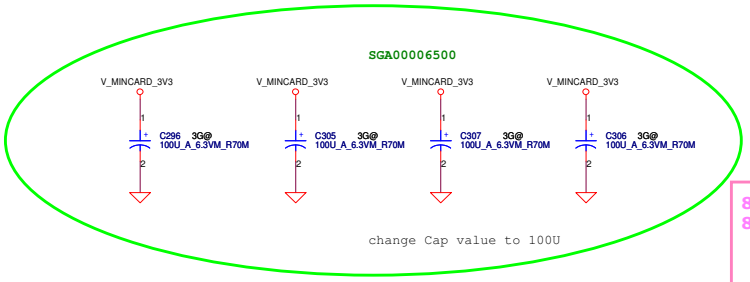
12/16 Modify R454 from 3G@ to LTE@ to meet SPEC.

8/23 Modify for Leakage issue.



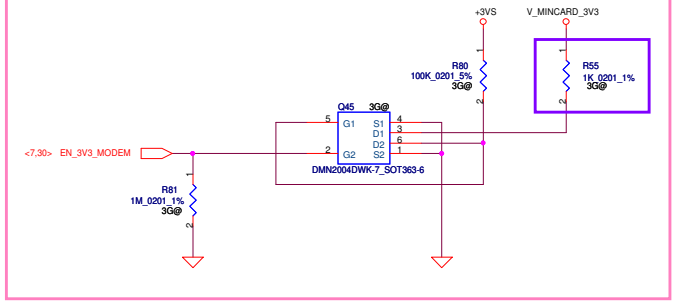


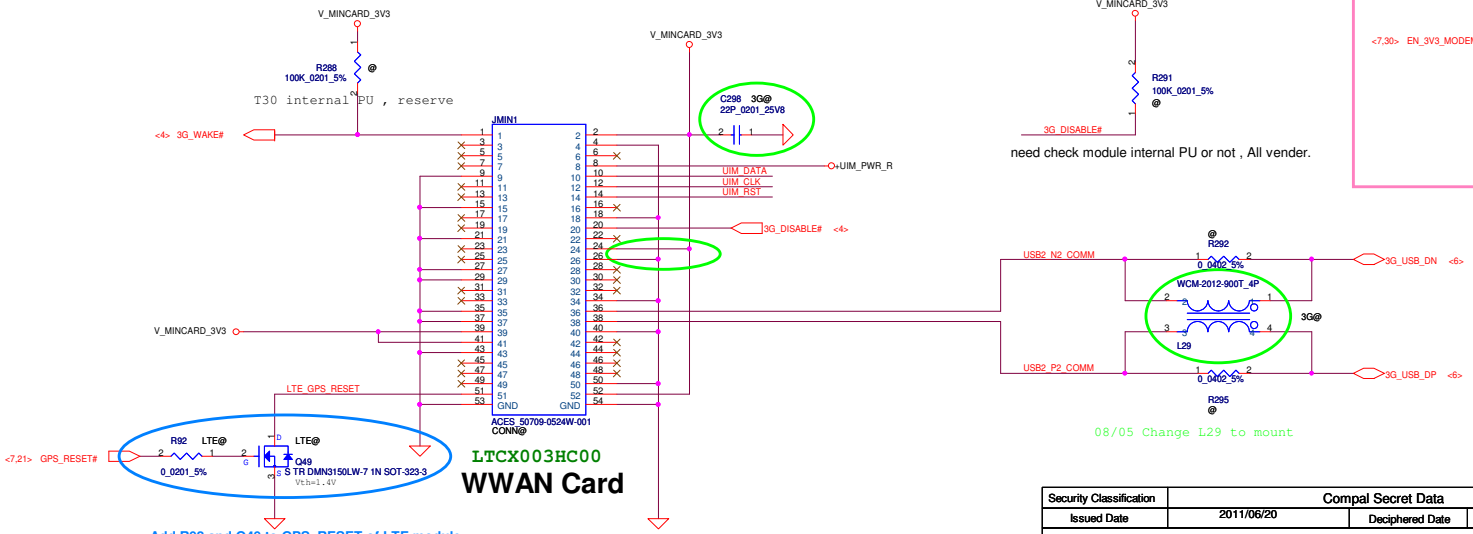




10/04 Modify R55 from 2.2K to 1K.

8/23 Add for Discharge V_MINCARD_3V3
8/25 Modify part form SB00000EO10 to SB00000IV00





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Issued Date	2011/06/20	Deciphered Date	2012/06/20	Title: 3G card
				Size: C; Document Number: Picasso 2 R04; Rev: 1.0
				Date: Tuesday, January 17, 2012; Sheet 18 of 38

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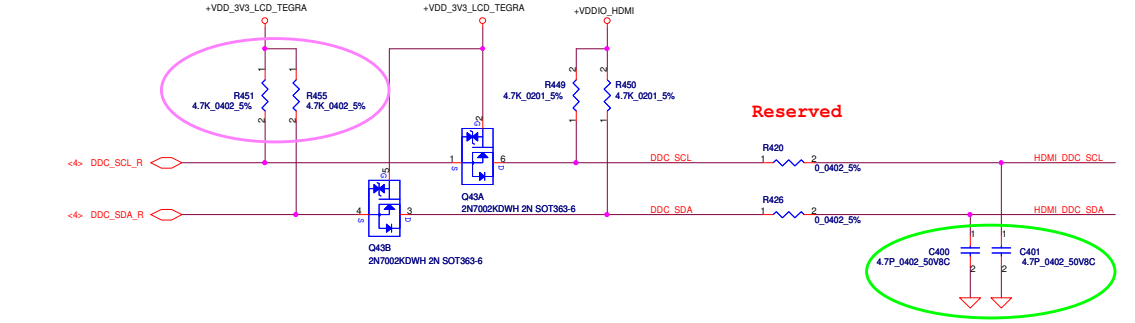
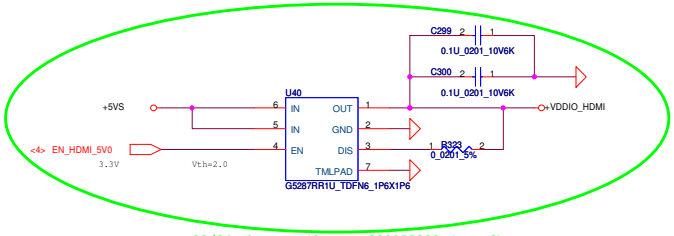
8/25 Modify R451&R455 from 47K 1% to 4.7K 5%

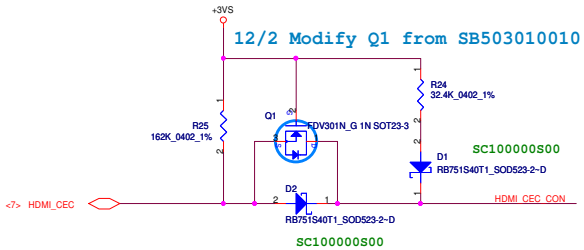


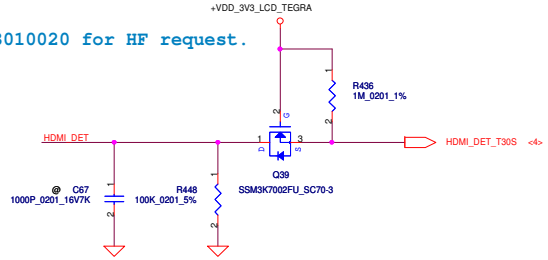
07/28 Change C400,C401 to SE07147AC80

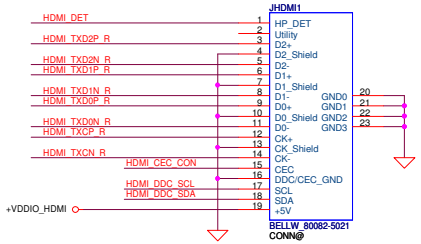


08/04 Change U40 to SA000055200 (TDFN6)

12/2 Modify Q1 from SB503010010 to SB503010020 for HF request.



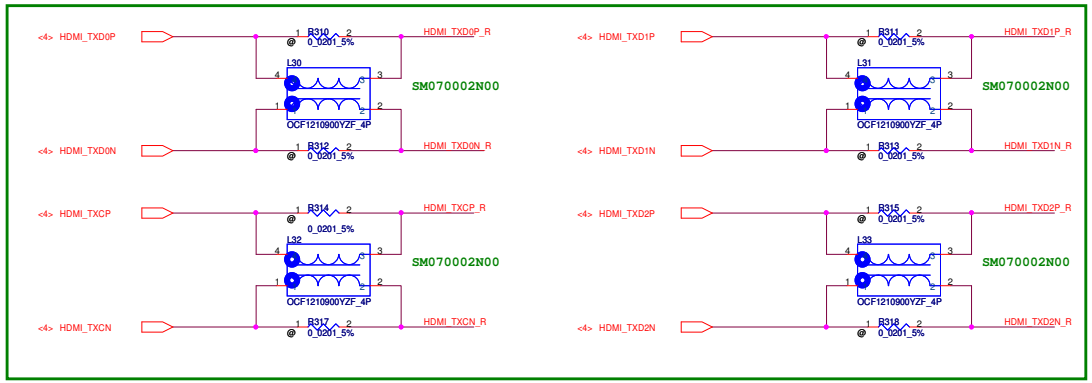




DC232001M10

HDMI Type D Connector

08/05 Change L30~L33 to SM070002N00



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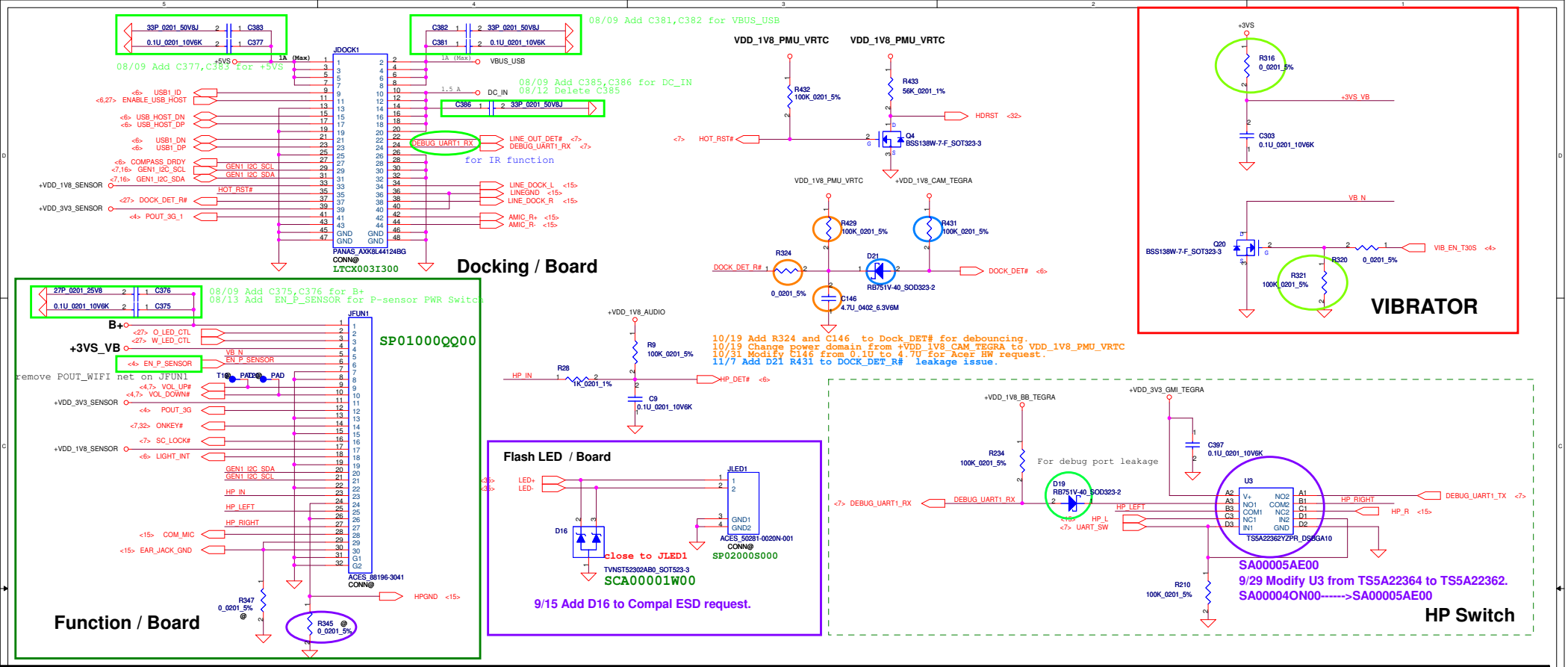
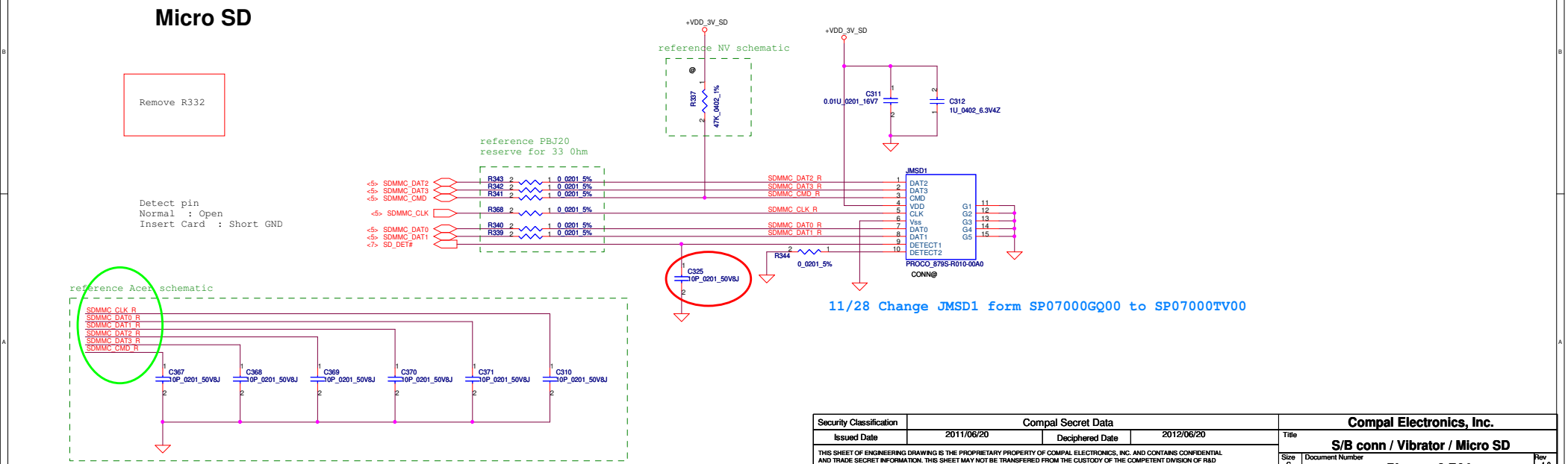
				Date: Tuesday, January 17, 2012 / Sheet 19 of 38



10/13 Modify R345 from mount to @ for Acer AUDIO request.

Micro SD



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Issued Date	2011/06/20	Deciphered Date	2012/06/20

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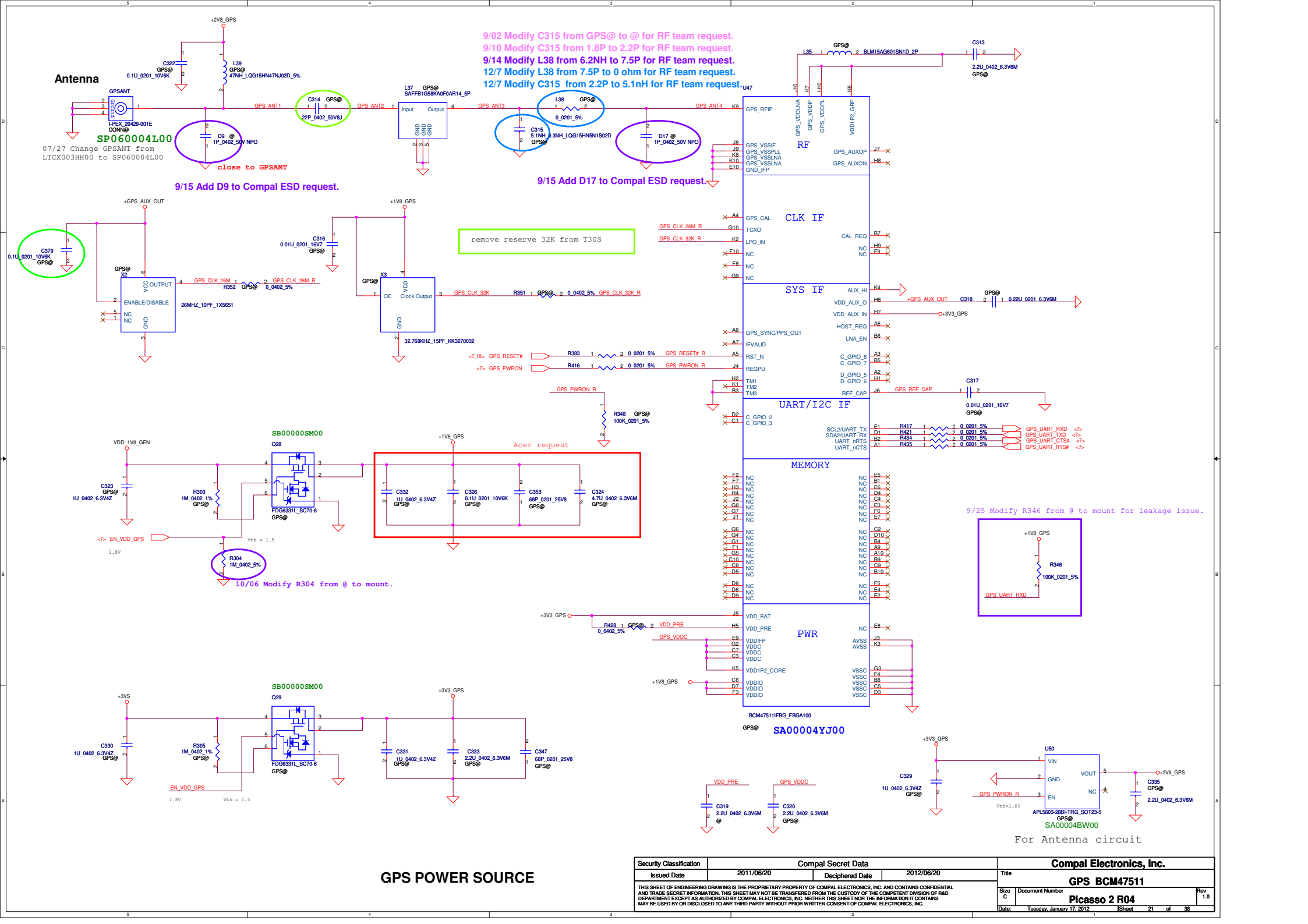
Compal Electronics, Inc.

Title: **S/B conn / Vibrator / Micro SD**

Size: C | Document Number: **Picasso 2 R04** | Rev: 1.0

Date: Tuesday, January 17, 2012 | Sheet 20 of 38



GPS POWER SOURCE

Security Classification	Compal Secret Data		
Issued Date	2011/06/20	Deciphered Date	2012/06/20

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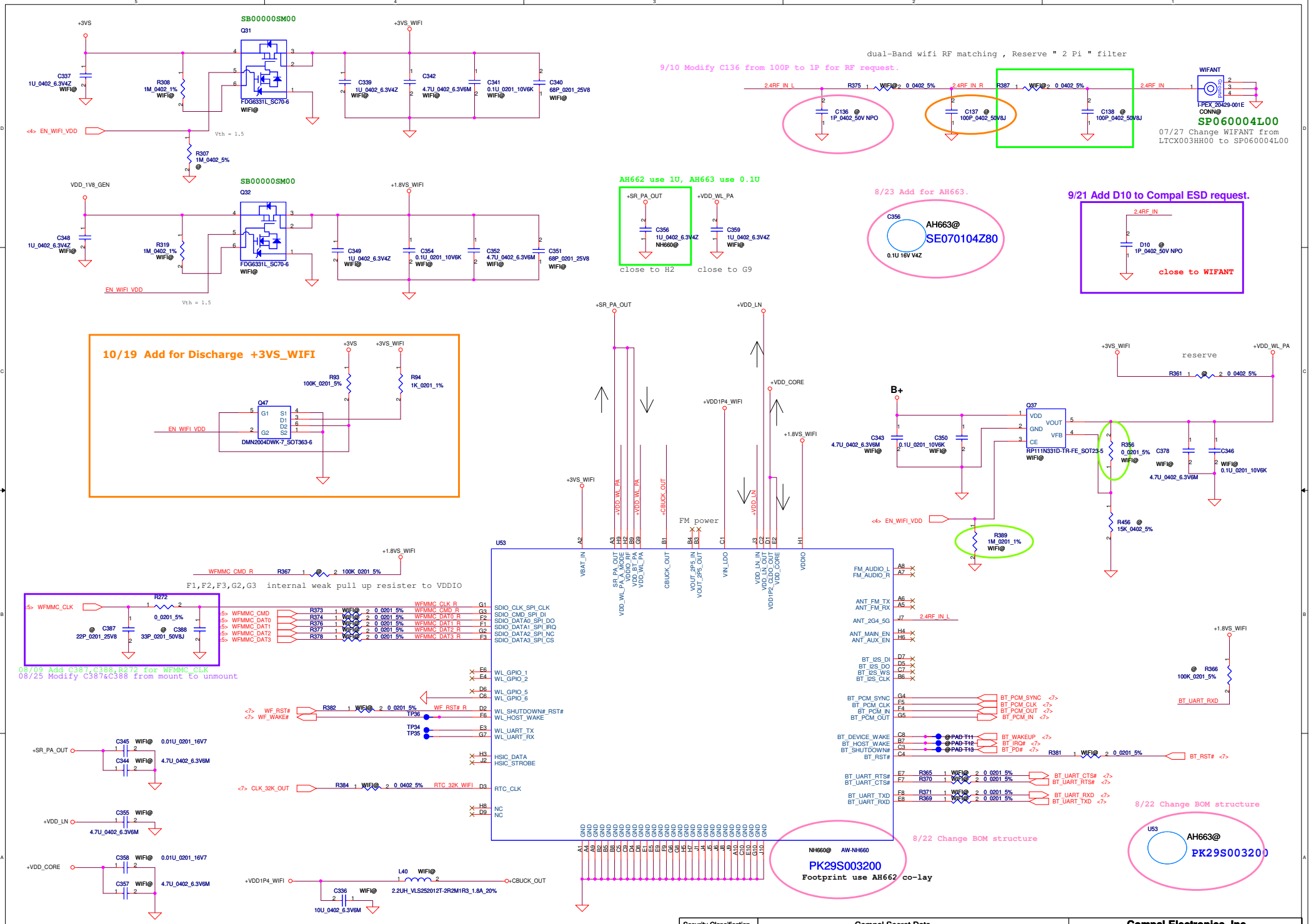
Compal Electronics, Inc.

Title: GPS BCM47511

Size: C | Document Number: Picasso 2 R04 | Rev: 1.0

Date: Tuesday, January 17, 2012 | Sheet 21 of 38



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/06/20	Deciphered Date	2012/06/20	Title: WIFI/BT AH662
				Size: C; Document Number: Picasso 2 R04; Rev: 1.0
				Date: Wednesday, January 18, 2012; Sheet 22 of 38

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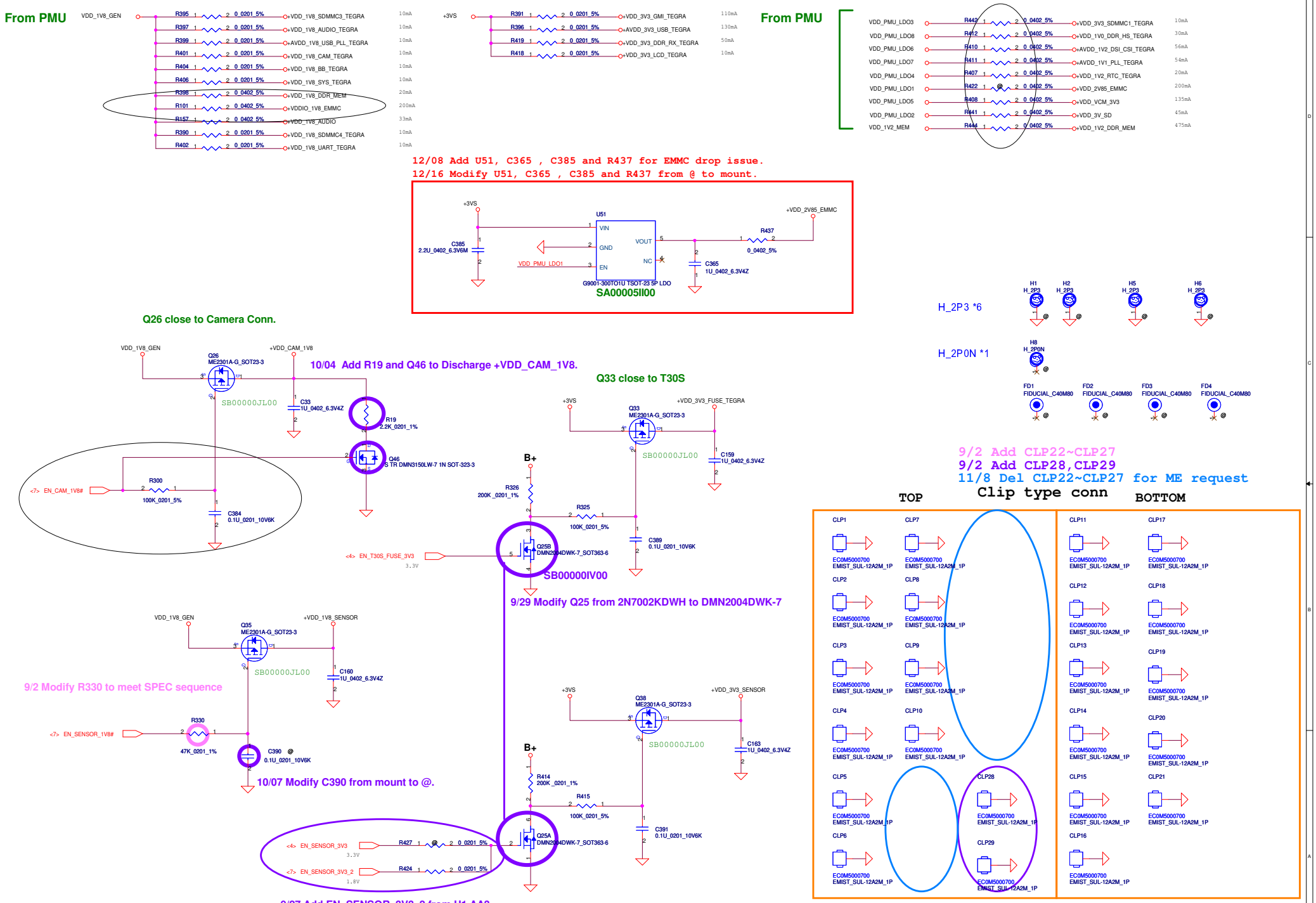

Security Classification	Compal Secret Data		
Issued Date	2011/06/20	Deciphered Date	2012/06/20

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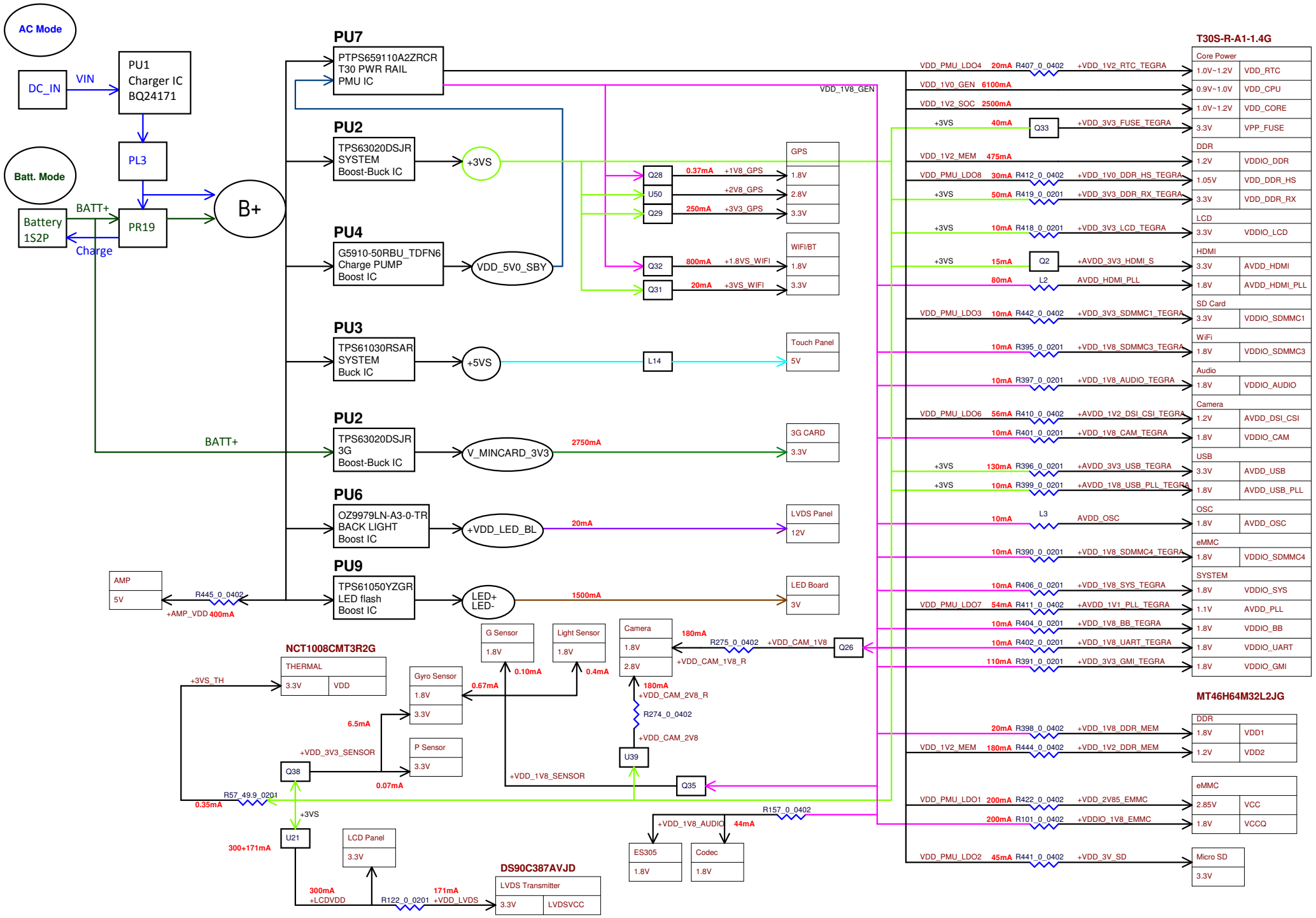
Compal Electronics, Inc.

Title: **DC interface/Power Button**

Size: C | Document Number: **Picasso 2 R04** | Rev: 1.0

Date: Wednesday, January 18, 2012 | Sheet 23 of 38



Security Classification	Compal Secret Data		
Issued Date	2011/05/20	Deciphered Date	2012/05/20

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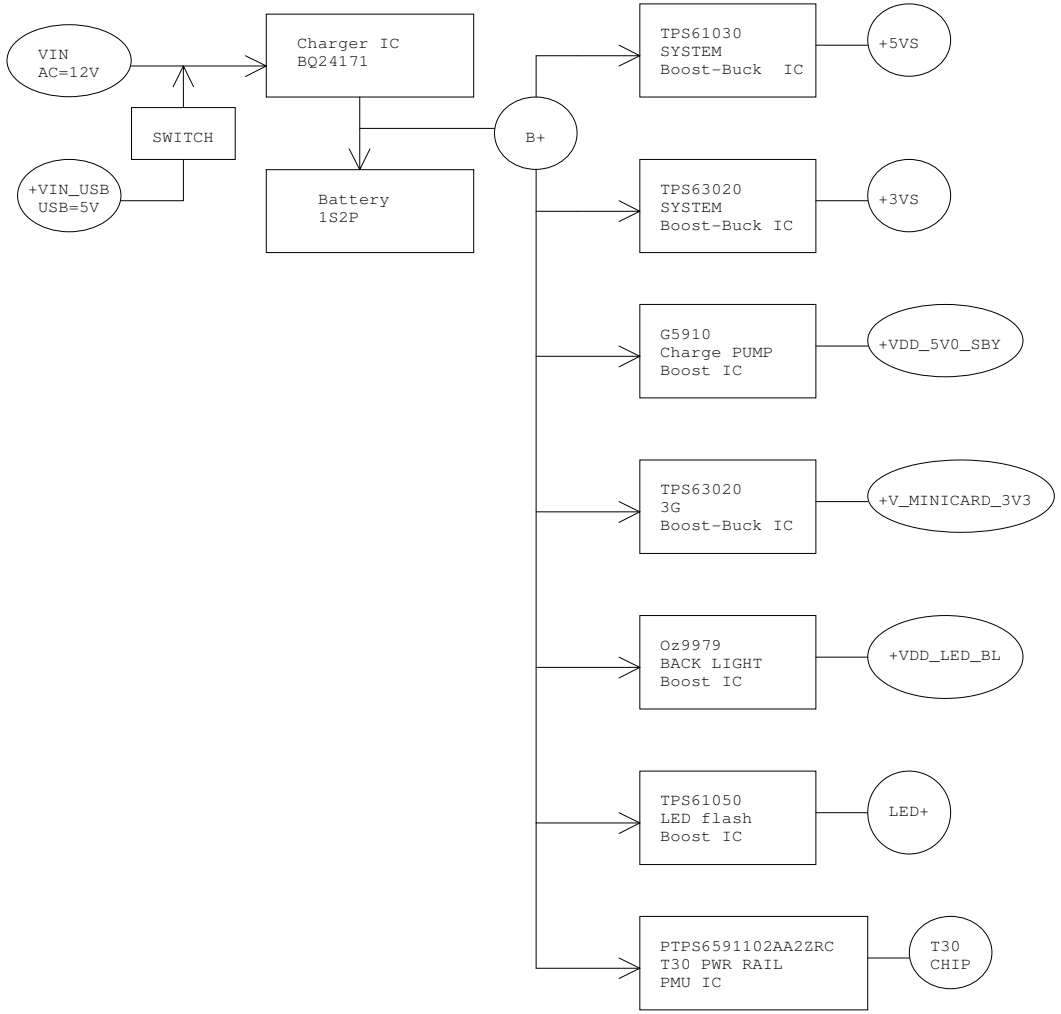
Compal Electronics, Inc.

Title: Power Tree

Size: Custom | Document Number: Picasso 2 R04 | Rev: 1.0

Date: Tuesday, January 17, 2012 | Sheet 34 of 38



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/06/20	Deciphered Date	2012/06/20	Title: Block Diagram
				Size: C; Document Number: Picasso II/M; Rev: 1.0
				Date: Tuesday, January 17, 2012; Sheet 25 of 38

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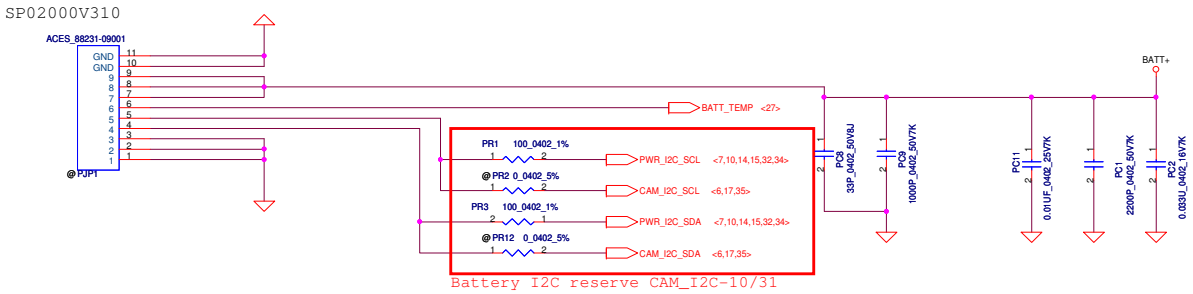

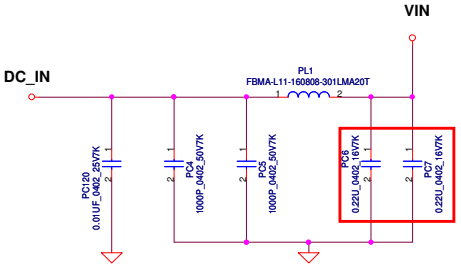

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/06/20	Deciphered Date	2012/06/20	Title: DC IN/BATT IN
				Size: C; Document Number: Picasso II/M; Rev: 1.0
				Date: Tuesday, January 17, 2012; Sheet 26 of 38

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CHARGER BQ24171

OVP UVP Range setting:
##OVPSET voltage is between 0.497~1.6V ##
1.6V*(768+100)/100=13.888V
0.497V*(768+100)/100=4.314V
Setting "OVP 13.888V" & "UVP 4.314V"

AC Insert or remove --> Wake up T30S
USB Insert or remove --> Wake up T30S
SW to check if Acer USB --> Change charge current to 1A

Max Rds(on) 36mohm
Max Rds(on) 16.5mohm
Change 0.22U*2 for VBUS_USB issue 10/19

Charge Current setting:
ICHG=VISET/(20*PR352)
<<AC adaptor charge>>
VISET=VREF*[PR26/(PR26+(PR22//PR46))]
=3.3*[11/(11+267//47.5)]= 0.707V
ICHG=0.707/(20*0.01)=3.536A
<<USB charge>>
VISET=VREF*[PR26/(PR26+PR22)]
=3.3*[11/(11 +267)]= 0.131V
ICHG=VISET/(20*0.01)=0.653A

VISET voltage is between 0.12~0.8V

Batt OVP :
Batt+ over 4.4V
Back to back will turn off

LED status: (AC/Dock station)
No charge : LED off
Fully charged : Static White LED
Charging : Static Orange LED
Charging error : Blink

LED status: (USB)
All LED off

Boot : Static White LED 5sec
Wake up : Static White LED 5sec

TTC setting:
High:Disable charge timer,allow termination.
Low:Disable charge termination & timer.
Connect capacitor:Set fast charge timer.

Pre-Charge reserved circuit

BATT+ over 3.3V,
Pre-charge will start

SB00000SP00 use BSS8402DW footprint

L: charge in progress
H : charge is complete or in sleep mode
Blink (0.5Hz): fault occur (charge suspend, input over-voltage, timer fault and battery absent)

CP setting:
Idpm=Vacset/(20*PR9)
<<AC adaptor>>
Vacset=3.3*PR25/(PR21+PR25)=1.395V
Iin=Vacset/(20*PR9)=1.395A
<<USB>>
Vacset=3.3*(PR25//PR20)/(PR21+PR25//PR20)=0.463V
Iin=Vacset/(20*PR9)=0.463A
<<Dock-in>>
Vacset=3.3*(PR25//PR23)/(PR21+PR25//PR123)=0.804V
Iin=Vacset/(20*PR9)=0.804A

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/20	Deciphered Date 2012/06/20	Title: Charger
			Size A2 / Document Number: Picasso II/M / Rev 1.0
			Date: Tuesday, January 17, 2012 / Sheet 27 of 38

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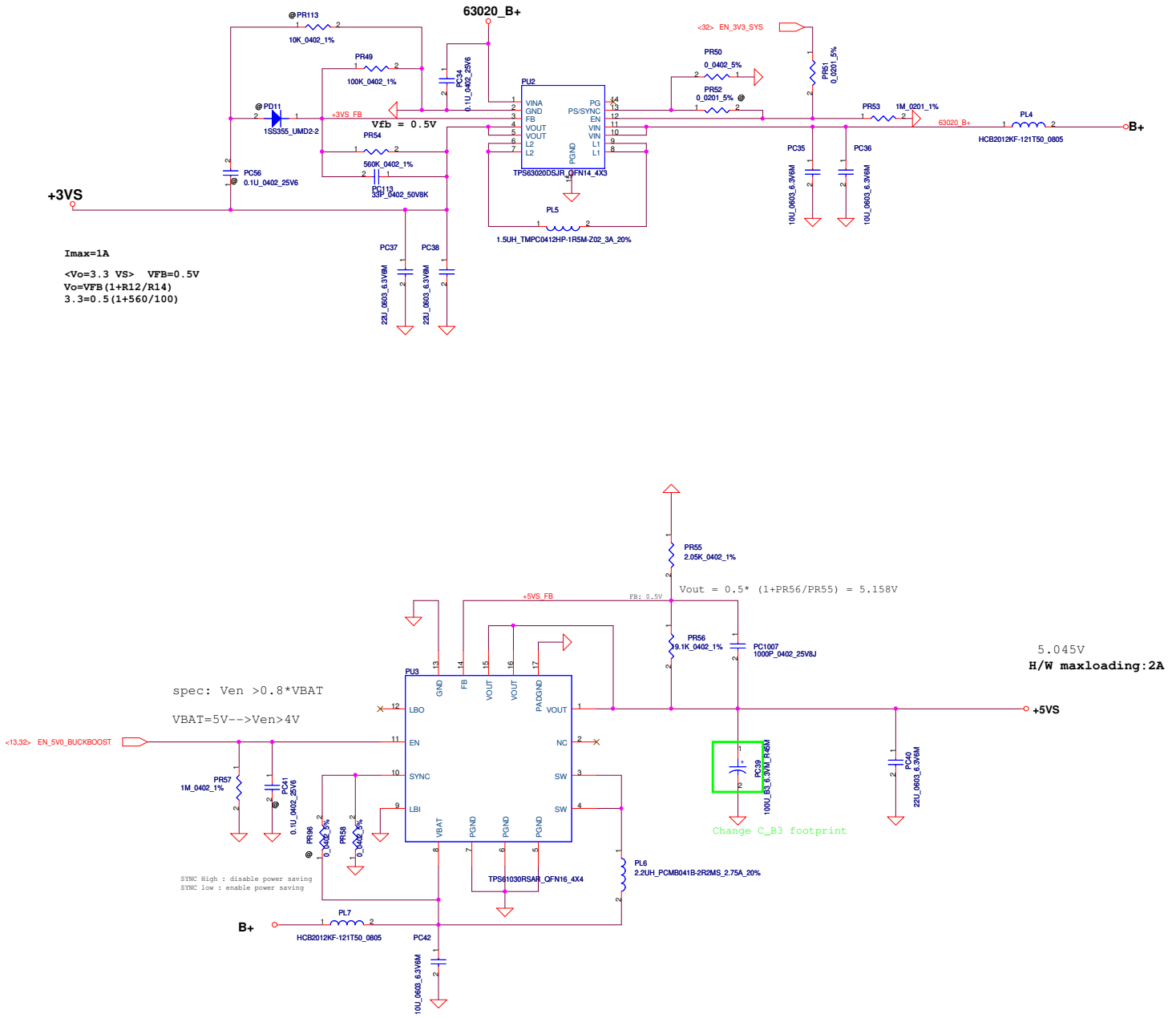

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/06/20	Deciphered Date	2012/06/20	Title: +3.3VALWP/+5VALWP
				Size: C; Document Number: Picasso II/M; Rev: 1.0
				Date: Tuesday, January 17, 2012; Sheet 28 of 38

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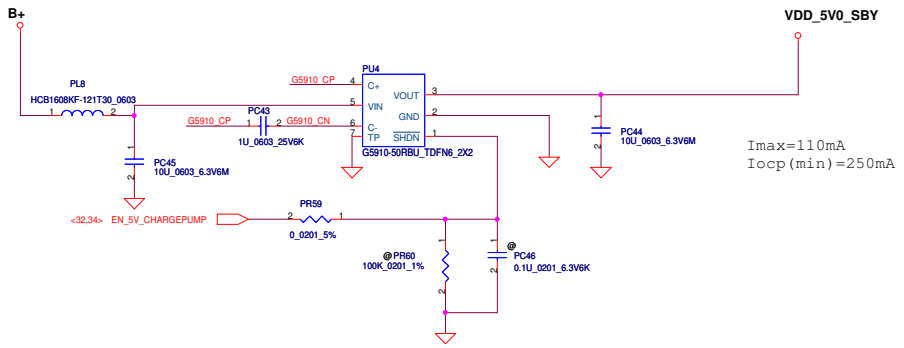

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Issued Date	2011/06/20	Deciphered Date	2012/06/20	Title: +5V_charge_pump
				Size: C; Document Number: Picasso II/M; Rev: 1.0
				Date: Tuesday, January 17, 2012; Sheet 29 of 38

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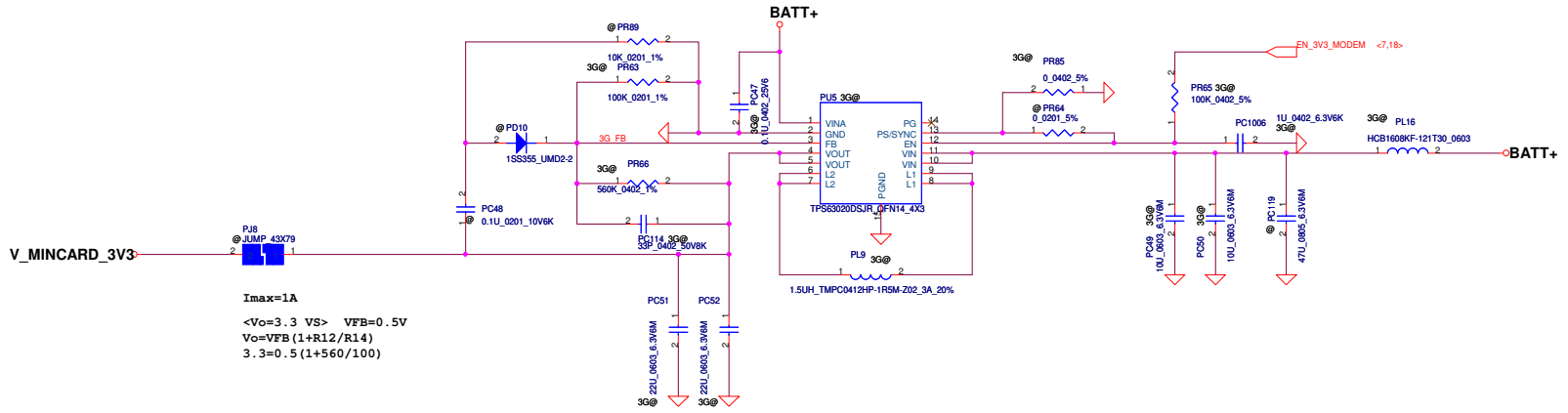

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/06/20	Deciphered Date	2012/06/20	Title: 3G PA(SY8033B/APL5916)
				Size: C; Document Number: Picasso II/M; Rev: 1.0
				Date: Tuesday, January 17, 2012; Sheet 30 of 38

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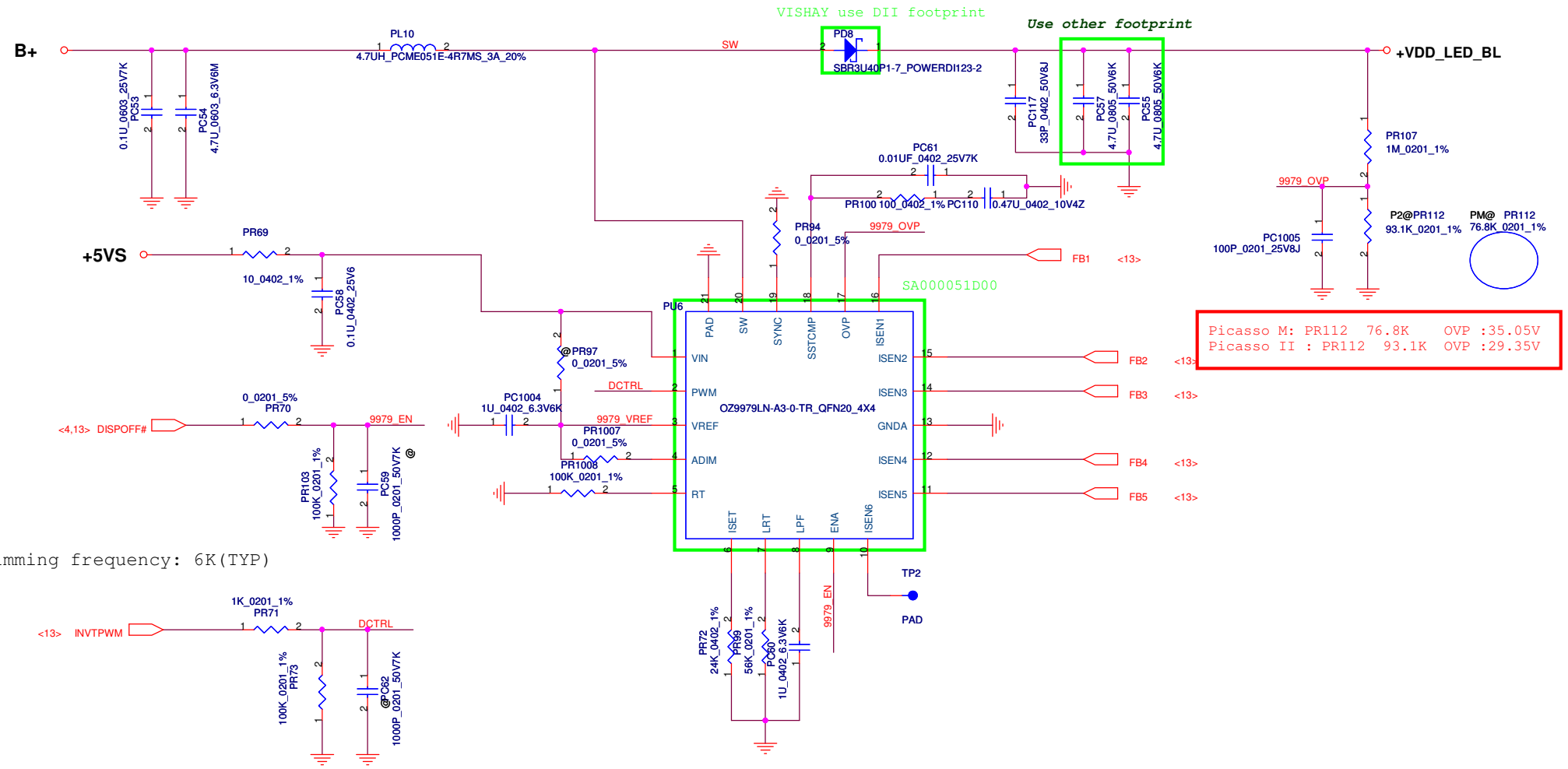

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Issued Date	2011/06/20	Deciphered Date	2012/06/20

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Compal Electronics, Inc.

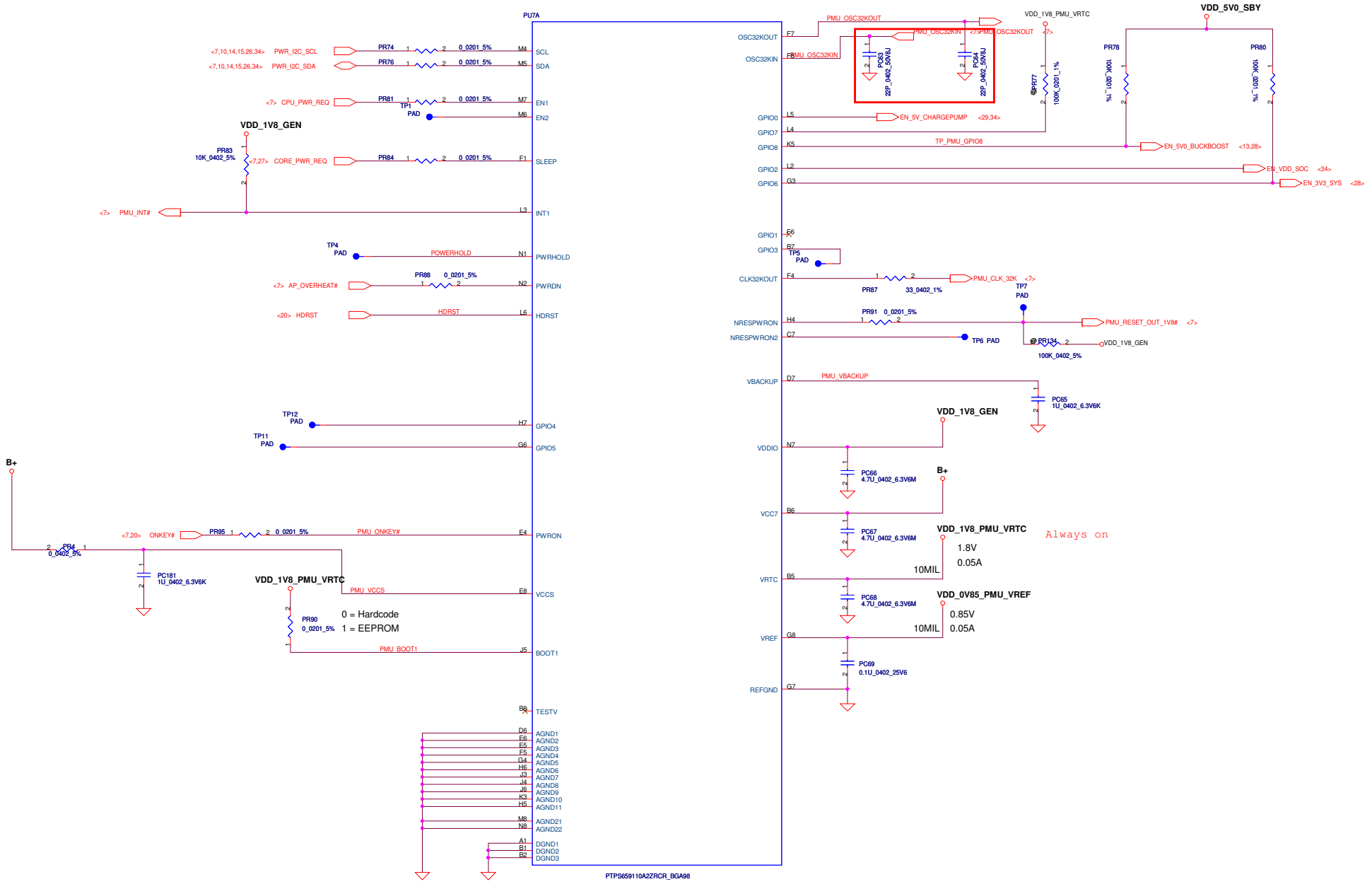
Title: **LED driver**

Size: B | Document Number: **Picasso II/M** | Rev: 1.0

Date: Wednesday, January 18, 2012 | Sheet 31 of 38

PMU-TPS65911 1/3

a. GP0: EN_5V_CP Follow ACER circuit 6/22
b. GP2: EN_SOC
c. GP6: EN_3V3_SYS
d. GP7: EN_DDR (Optional on Cardhu S since we are using VDD2 for memory)
e. GP8: EN_5V0



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Issued Date	2011/06/20	Deciphered Date	2012/06/20	Title: PMU part1
				Size: C; Document Number: Picasso II/M; Rev: 1.0
				Date: Tuesday, January 17, 2012; Sheet 32 of 38

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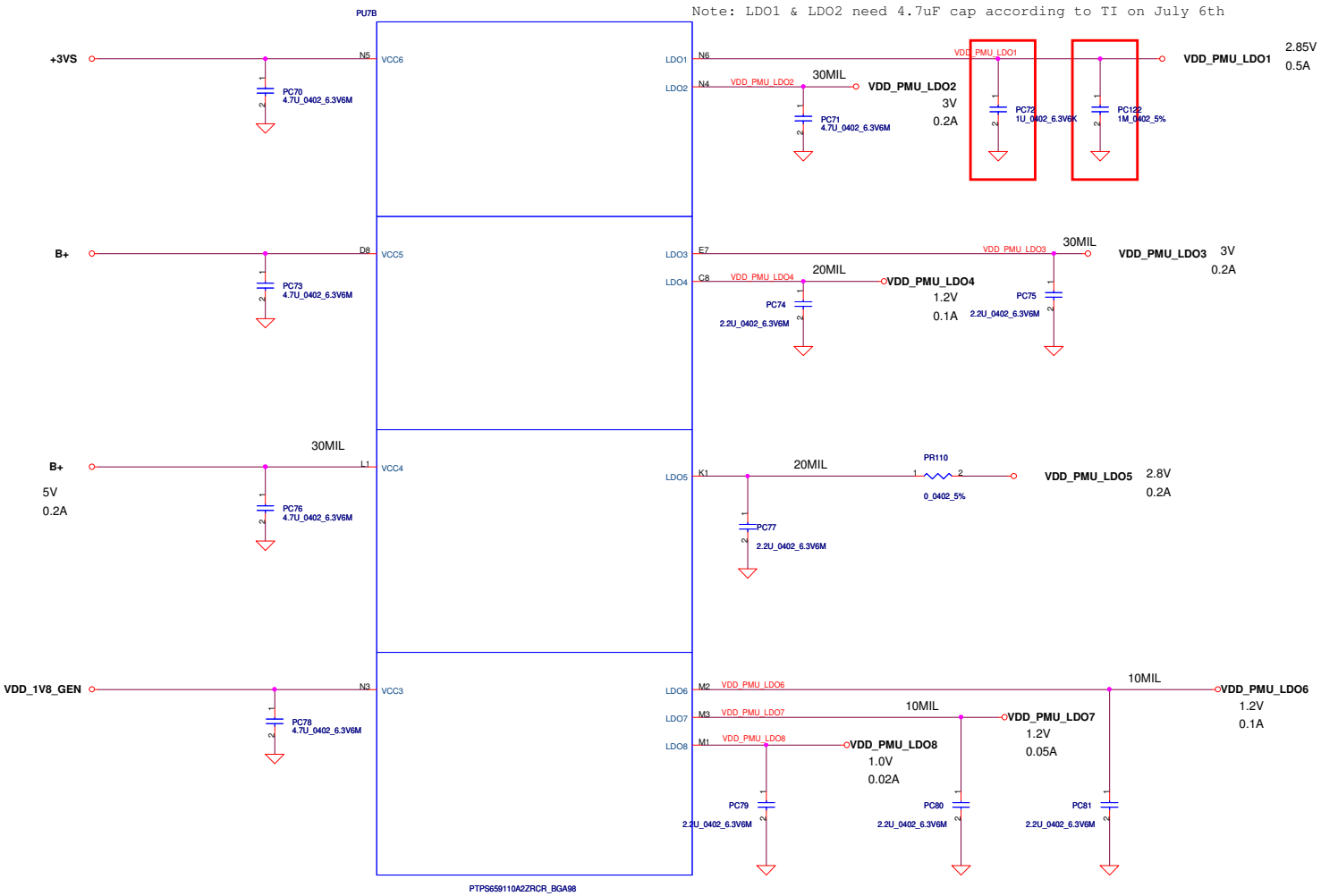
PMU-TPS65911 2/3



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Issued Date	2011/06/20	Deciphered Date	2012/06/20	Title: PMU part2
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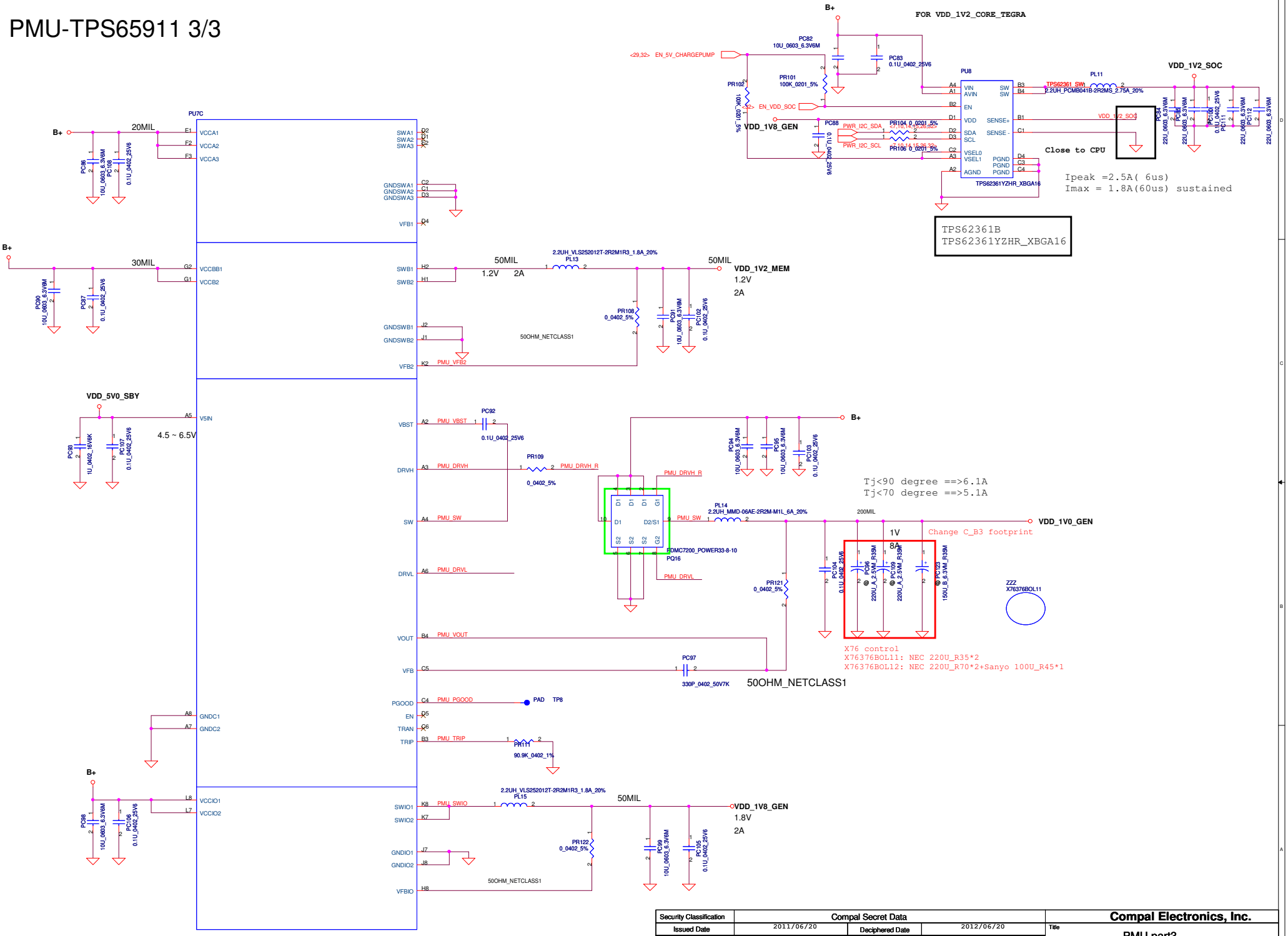
PMU-TPS65911 3/3



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Issued Date	2011/06/20	Deciphered Date	2012/06/20	Title: PMU part3
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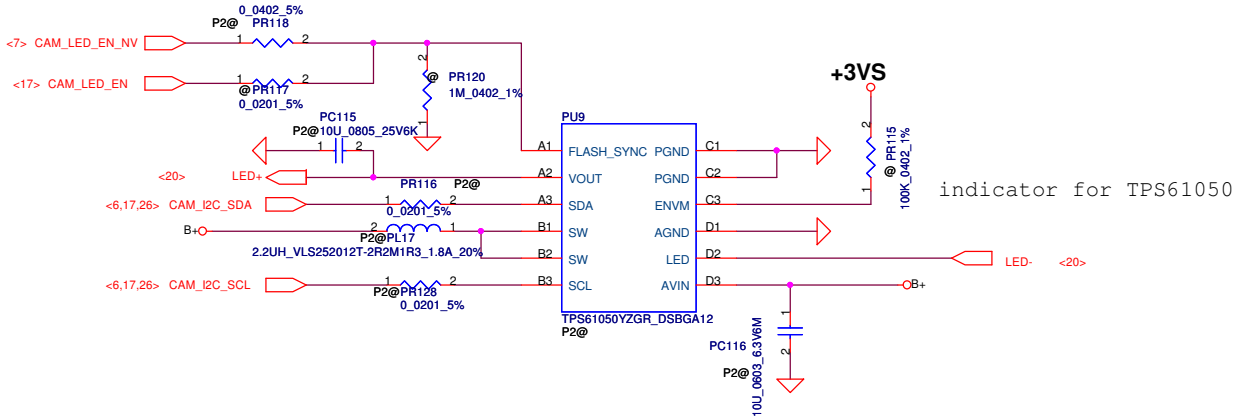

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Compal Electronics, Inc.

Title: **LED FLASH**

Size: A3 | Document Number: **Picasso II/M** | Rev: 1.0

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Ripple un-stable	Loop stable for TPS63020	01	28 30	change PL5, PL9 from PCMB041B-2R2MS 2.75A to PCMB041B-1R5MS 3A,	20110806	EVT (QAJ70)
2		charger CP setting for adaptor protect	02	26	change PR9 form 0.01_1206_1% to 0.05_1206_1% change PR25 form 10K to 73.2K change PR20 form 3.83K to 21K Remove ACER USB setting circuit	20110809	DVT (QAJ50)
3		Net name error	02	35	change net name from VDD_1V8_SYS to VDD_1V8_GEN	20110809	DVT (QAJ50)
4		Material version change	02	35	change PQ16 from FDMC7200 2N POWER33-8 to FDMC7200S 2N POWER33-8	20110809	DVT (QAJ50)
5	GPIO only support 1.8V	Use low Vth dual N TR	02	26	change PQ4,PQ6,PQ7,PQ21,PQ21 from DMN66D0LDW-7_SOT363 to SI1034CX	20110809	DVT (QAJ50)
6		material change for common use	02	26	change PQ18 from BSS8402DW 1P/1N SOT363-6 to SI1553CDL-T1-GE3 1P/1N SC70-6	20110809	DVT (QAJ50)
7		No support Acer USB, delete related control circuit	02	26	Delete PQ19, PR40, PR44, PR47, PR41.	20110809	DVT (QAJ50)
8	Back-to-back MOS can't fully turn on	The BATDRV# pull low 1K will cause ACDRV abnormal	02	26	Change PR16, PR12, PD4 to reserve	20110809	DVT (QAJ50)
9	Charger will terminate	The TTC pull high 100K will cause wrong voltage level	02	26	Change PR34 from 100K to 10K	20110809	DVT (QAJ50)
10	Orange LED can't turn off	STAT pull high 100K can't drive TR	02	26	Change PR36 from 100K to 10Kohm	20110809	DVT (QAJ50)
11		Modify Battery OVP circuit to avoid AC turn off when Battery over discharge	02	26	Add PC118, PR144,PQ23. Delete PD7	20110809	DVT (QAJ50)
12	Pre-charge circuit can't work normally	Modify Pre-charge circuit	02	26	Change PR86,PR92,PR93 to PNP 2SA1037K	20110816	DVT (QAJ50)
13	Sub/B +5VS will drop to under 4.75V	Modify +5VS voltage setting to 5.15V	02	28	Change PU3 to TPS61030, PR56 to 19.1K, PR55 to 2.05K	20110824	DVT (QAJ50)
14		TPS63020 add 33P on feedback resistor for loop stable	02	28 30	Add PC113, PC114 33P	20110824	DVT (QAJ50)
15		V_MINCARD_3V3 sequence	02	30	Change PR65 from 1M_0402_1% to 100K_0402_1% Add PC1006 1U_0402_6.3V6K	20110824	DVT (QAJ70)
16		modify crystal cap	02	32	Change PC63, PC64 from 12P_0402_50V8J to 22P_0402_50V8J	20110825	DVT (QAJ70)
17		Add LED control circuit for wake up/boot define	02	26	Add PQ22 to turn off O_LED	20110825	DVT (QAJ70)

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		Add for pre-charge and fast charge timeout	02	27	Add PQ19 ,PR44,PR47	20110826	DVT (QAJ70)
2		BOM control	02	27,31	Modify PD1, PD5, PD8 from SS3P4-M3-84A_SMP2 to SBR3U40P1	20110826	DVT (QAJ70)
3		footprint control	02	34,35	Modify PL13, PL15, PL17 footprint to TOKO_1239AS-H-2R2N-P2_2P	20110826	DVT (QAJ70)
4		Change CP setting for adaptor protect	02	27	Add PQ23	20110826	DVT (QAJ70)
5		Add VDD_1V0_GEN and VDD_1V8_GEN Fb resistor for test request	02	34	Add PR121, PR122	20110826	DVT (QAJ70)
6		EMI request	03	27	Change PL1 to 300ohm bead, add PC120, PR11, PC15, PC20, PR98, PC1,PC2 for EMI request	20110920	DVT2 (QAJ50)
7		Cancel the function	03	27	Delete PR12, PR16, PD4	20110920	DVT2 (QAJ50)
8		Reserve the CP control for thermal improve	03	27	Add PR48, PQ24 for reserve	20110920	DVT2 (QAJ50)
9		Dock in CP setting	03	27	Add PQ26 PR93 PR96 PR124 PR123 PR40	20110920	DVT2 (QAJ50)
10		Solve White LED flash issue when AC plug in	03	27	Add PD4,PC121,PR126,PR127,PQ27	20110920	DVT2 (QAJ50)
11		Battery OTP change to 55C	03	27	Change PR29 to 2.74K, PR30 to 8.87K	20110920	DVT2 (QAJ50)
12		remove pre-charge function	03		Reserved PU18, PQ9, PR7, PR61, PR79, PR86, PR41	20111006	DVT2 (QAJ50)
13		solve leakage current	03	27,31	Change PD1,PD5,PD8 from SBR3U40 to SS3P4; PR62, PR114 to 806K	20111006	DVT2 (QAJ50)
14		Thermal over temperature	04	28	Change PC39 to 100U_B3_6.3VM_R45	20111027	DVT2 (QAJ70)
15	VBUS leakage	PQ1 will turn on when AC plug out	04	26,27	Change PC6, PC7 to 0.22U. Add PC89 2.2U	20111027	PVT (QAJ50)
16		OTP change to 58C	04	27	Change PR29 to 2.43K, PR30 to 7.68K	20111027	PVT (QAJ50)
17		Modify battery OVP to 4.4V	04	27	Change PR67 to 38.3K	20111105	PVT (QAJ50)

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Compal Electronics, Inc.

Title: **PIR**

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		Turn off charge LED when USB in	04	27	Add PQ29, PC126, PC127	20111210	PVT (QAJ50)
2	White LED can't light when power on	Don't need the component	04	27	Change PR45 to reserve	20111210	PVT (QAJ50)
3		Adjust CP setting when power on for thermal issue	04	27	Add PQ22, PR132, PR135	20111210	PVT (QAJ50)
4	Battery can't be charged when dock in	Modify the battery capacity control for EN_USB_HOST to BATT_LEARN	04	27	Add PR1012, change P135 to 4.99K	20111210	PVT (QAJ50)
5	T30S WAKE_UP_ACIN damage	Avoid WAKE_UP_ACIN in-rush voltage	04	27	Add PR136, PR131	20111210	PVT (QAJ50)
6		Modify charge output voltage to improve battery capacity	04	27	Change PR35 to 82K and PR31 to 82.5K	20111210	PVT (QAJ50)
7		Avoid white LED will flash 1s when AC/USB plug in/out	04	27	Change PD4 to reserve, Add PR1013, PR126, PC124	20111210	PVT (QAJ50)
8		Modify crystal cap value	04	32	Change PC63, PC64 to 22P	20111210	PVT (QAJ50)
9	EMMC voltage drop	PMIC LDO1 compensation	04	33	Change PC72 to 1U	20111210	PVT (QAJ50)
10		Avoid EMMC external LDO floating	04	33	Add PC122 1M	20111219	PVT (QAJ50)
11							
12							
13							
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15							
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17							

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