

MODEL NAME : VBW00
PROJECT CODE : ANRVBW0100
PCB NO : DA8000WK000 LA-9981P M/B
DA40001FO00 LS-9101P POWER BUTTON/B
DA40001FP00 LS-9102P USB/B
DA40001FQ00 LS-9103P TP BUTTON/B

Dell / Compal Confidential

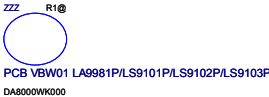
Schematic Document

Intel Shark Bay ULT
OAK Value2
UMA/DIS AMD Sun XT

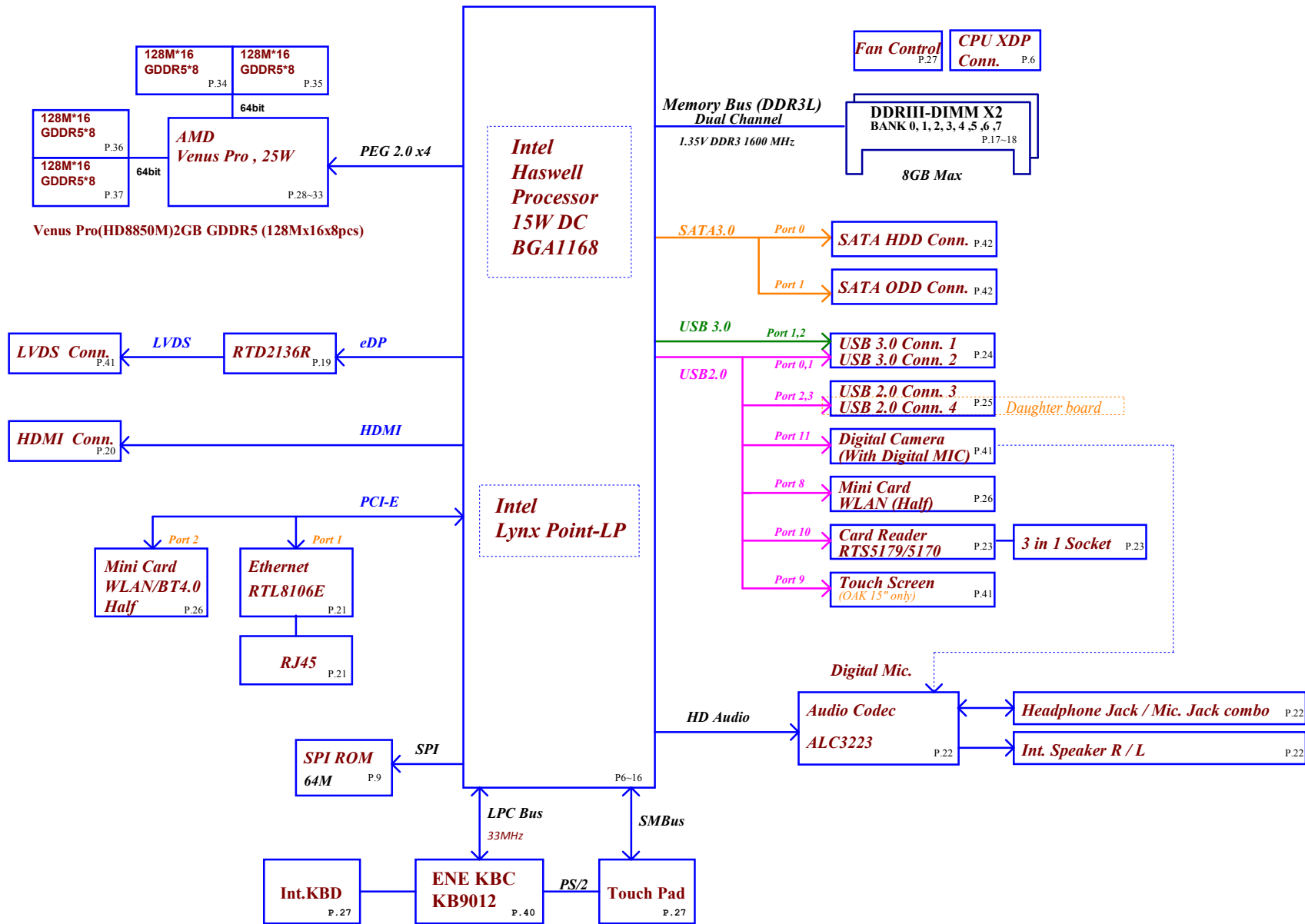
2013-03-09 Rev: 0.2

X76@ : 76 level
46@ : 46 level
@ : Nopop component
CONN@ : Connector component
XDP@ : XDP function
UMA@ : Only for UMA
DIS@ : Only for Discrete
SUN@ : SUN XT
EMI@ : EMI parts
@EMI@ : Reserve EMI parts
ESD@ : ESD parts
RF@ : RF parts

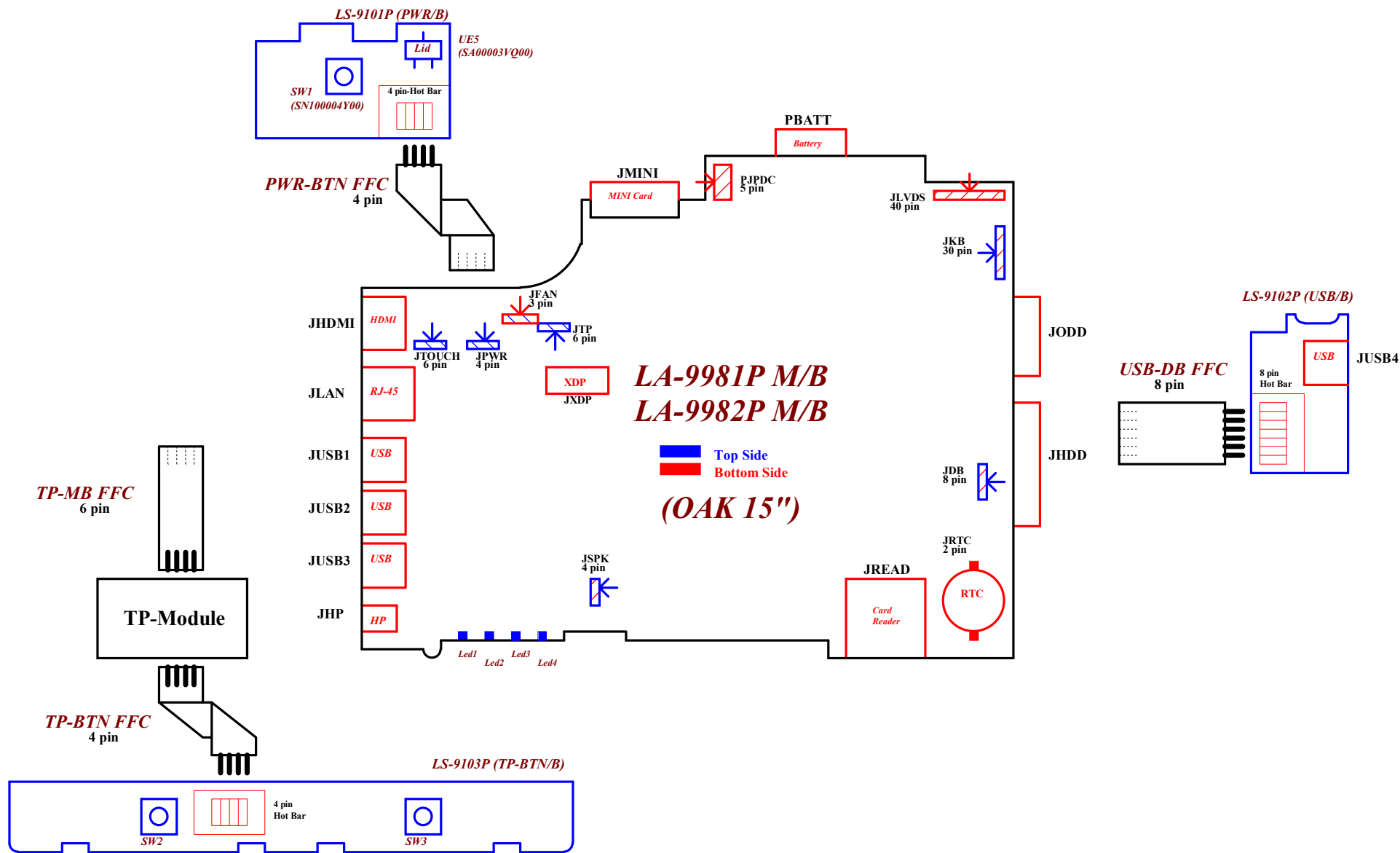
BOM config
UMA : UMA@,EMI@,ESD@,RF@,XDP@
DIS SUN : SUN@,DIS@,EMI@,ESD@,RF@,XDP@



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Project Code : VAW00 / VAW01
File Name : LA-9981P / LA-9982P



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								Size	Document Number						Rev
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Board ID Table for AD channel

Vcc	3.3V +/- 1%				
Ra	100K +/- 1%				
Board ID	Rb	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6
19	NC	3.000V	3.300V	3.300V	0xE7 - 0xFF

SMBUS Control Table

	SOURCE	BATT	Charger	RTD2136S	VGA	DDR3L	XDP	WLAN mini card	Touch pad
EC_SMB_CK1 EC_SMB_DA1	KB9012	V	V						
EC_SMB_CK2 EC_SMB_DA2	KB9012			V	V				
SMBCLK SMBDATA	ULT					V	V	V	V
SMLCLK SMLDATA	ULT								
SML1CLK SML1DATA	ULT								

Link

BOARD ID Table

ID	PCB Revision			
	UMA	Sun XT	Venus Pro	Venus XT
0	0.1			
1		0.1		
2			0.1	
3				0.1
4	0.2			
5		0.2		
6			0.2	
7				0.2
8	0.3			
9		0.3		
10			0.3	
11				0.3
12	1.0			
13		1.0		
14			1.0	
15				1.0

Symbol Note :



: means Digital Ground



: means Analog Ground

CLOCK SIGNAL

CLKOUT_PCIE0	
CLKOUT_PCIE1	
CLKOUT_PCIE2	10/100 LAN
CLKOUT_PCIE3	MINI Card (WLAN)
CLKOUT_PCIE4	dGPU (N14P)
CLKOUT_PCIE5	

ULT

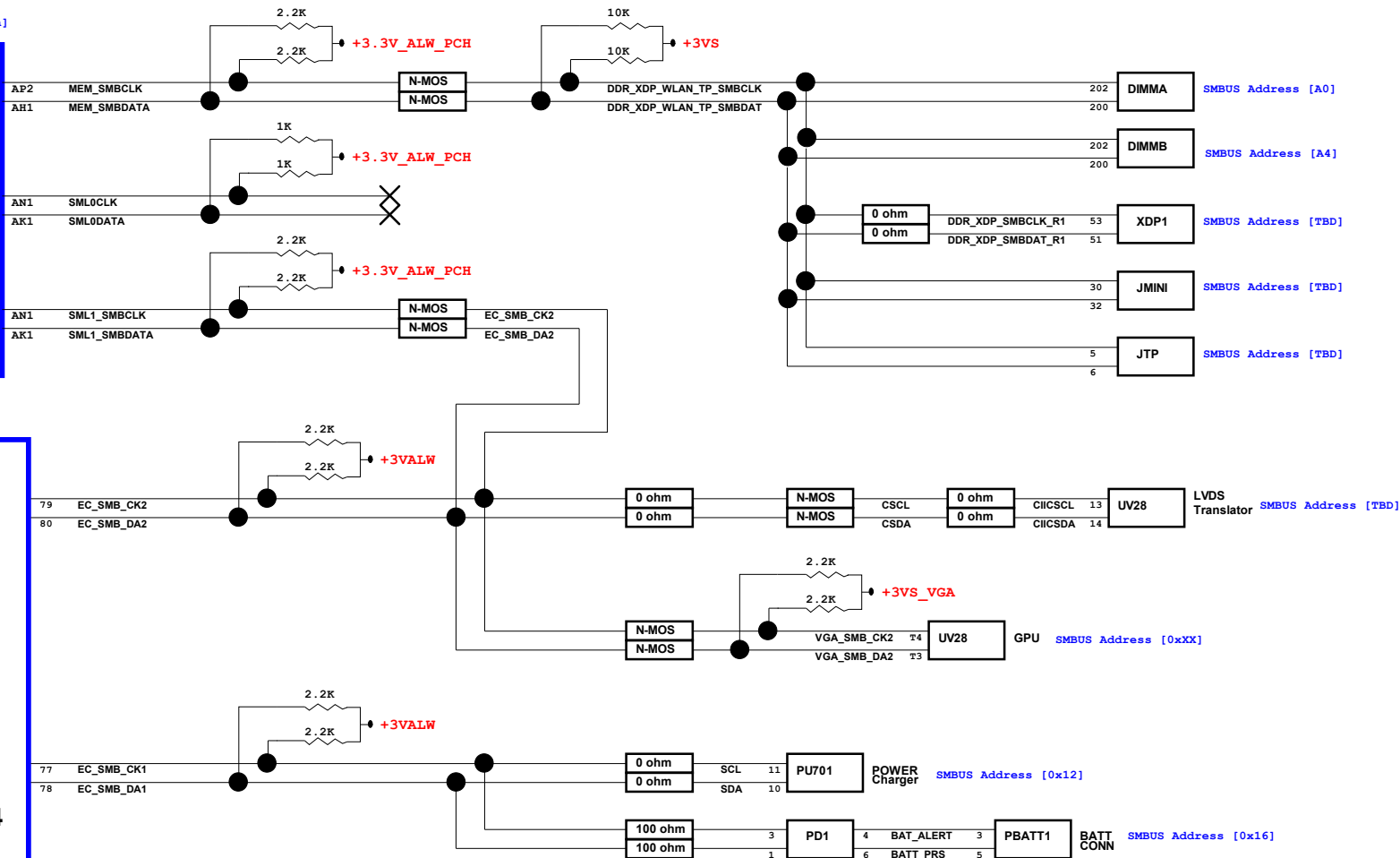
USB3.0	
Port1	USB connector 2
Port2	USB connector 1
Port3	
Port4	
USB2.0	
Port0	USB connector 2
Port1	USB connector 1
Port2	USB connector 3
Port3	USB connector 4 (DB)
Port4	MINI Card (WLAN)
Port5	Touch Screen Panel
Port6	Card Reader
Port7	Camera
PCI EXPRESS	
Lane 1	
Lane 2	
Lane 3	10/100 LAN
Lane 4	MINI Card (WLAN)
Lane 5	PEG (N14P)
Lane 6	PEG (N14P)
SATA	
SATA0	HDD
SATA1	ODD
SATA2	
SATA3	

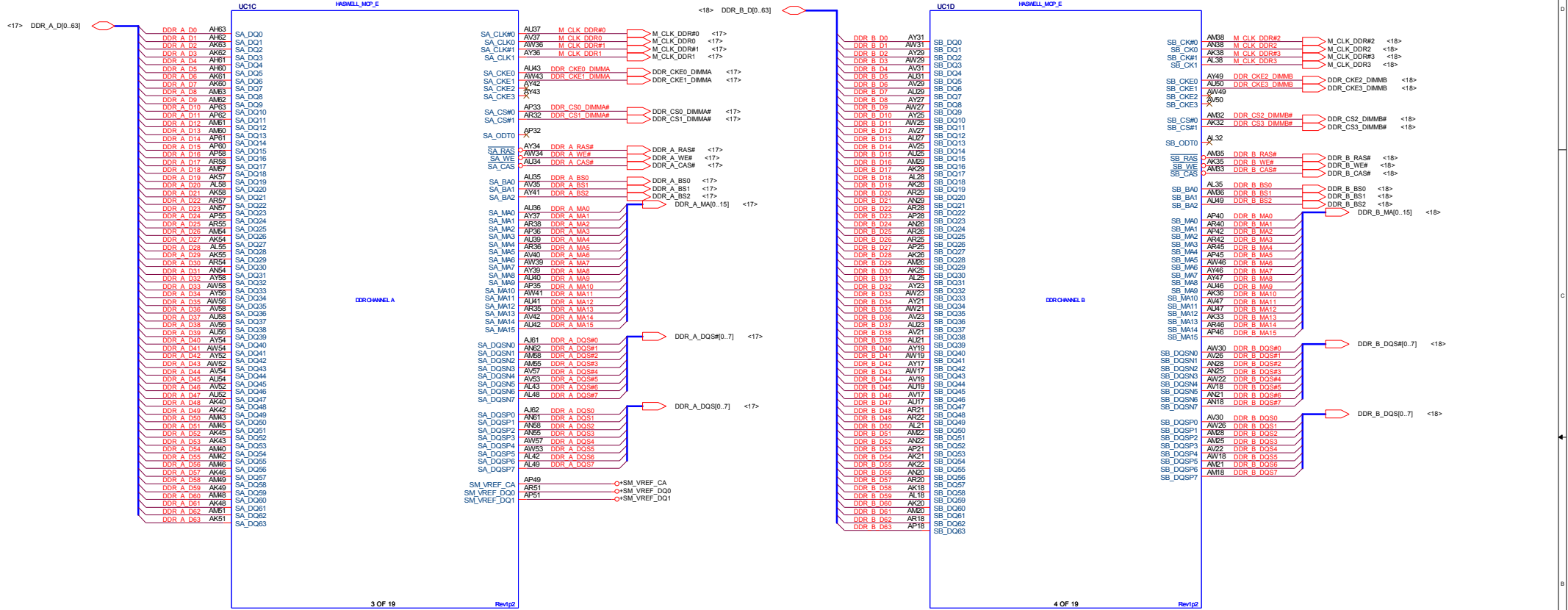
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SMBUS Address [0x9a]

MCH
Shark bay

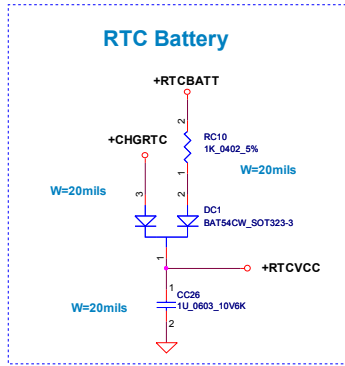
KBC
KB9012A4



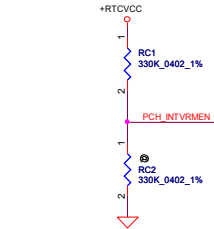


confirm by intel request PDG P141

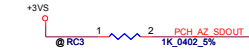
Security Classification		Compal Secret Data		Title	
Issued Date	2013/03/09	Deciphered Date	2014/04/01	MCP(3,4/19) DDR3	
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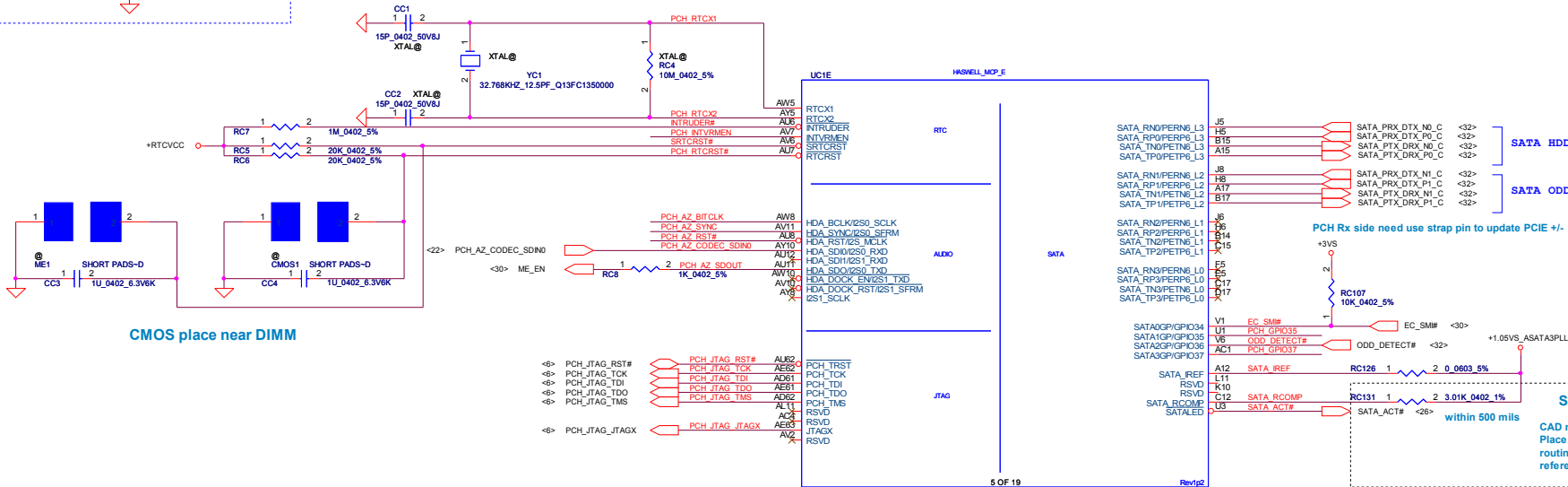
For GCLK



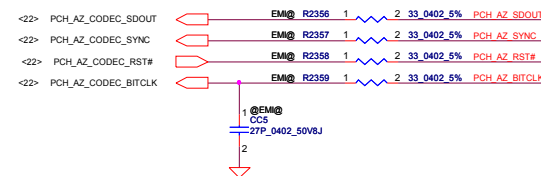
INTVRMEN - INTEGRATED SUS 1.05V VRM
ENABLE
High - Enable Internal VRs
Low - Enable External VRs



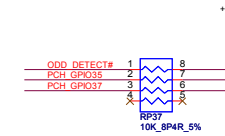
FLASH DESCRIPTOR SECURITY OVERRIDE
LOW = DISABLED (DEFAULT)
HIGH = ENABLED



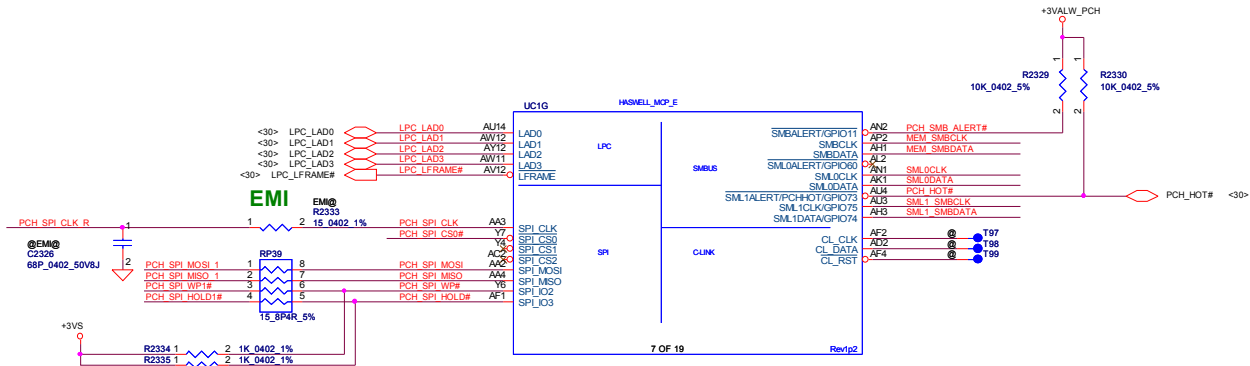
HDA for Codec



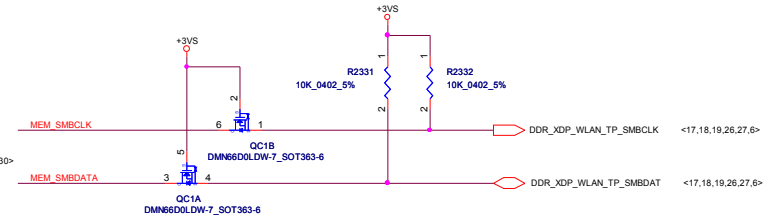
EMI depop location



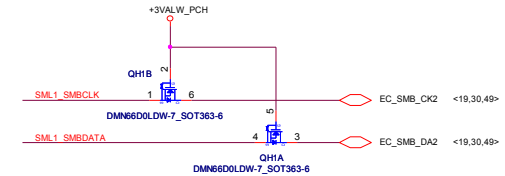
SATA Impedance Compensation
CAD note:
Place the resistor within 500 mils of the PCH. Avoid routing next to clock pins. reference FFRD sch 0.5



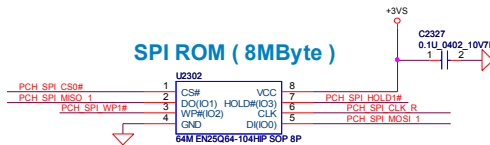
MEM Bus : DDR/XDP/WLAN/TP



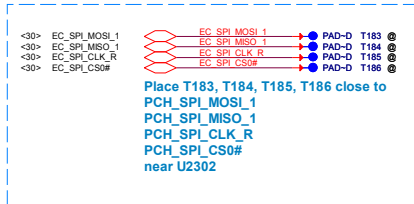
SML1 Bus : EC/Sensors



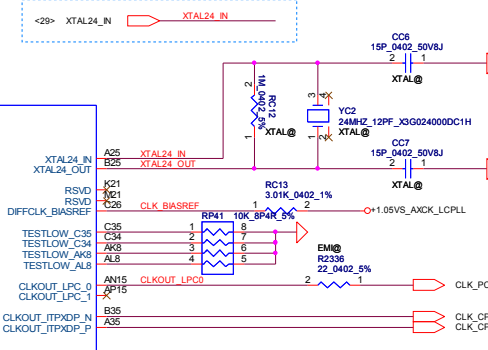
SPI ROM (8MByte)



PN : SA000046400 ,64M,EN25Q64-104HIP



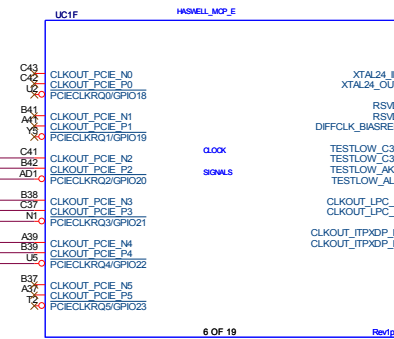
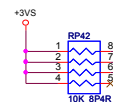
For GCLK



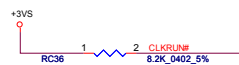
10/100 LAN ----->
WLAN (Mini Card) ---->
dGPU ---->

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<21> CLK_PCIE_LAN#
<21> LAN_CLKREQ#
<26> CLK_PCIE_WLAN#
<26> CLK_PCIE_WLAN#
<26> WLAN_CLKREQ#
<48> CLK_PEG_VGA#
<48> CLK_PEG_VGA#
<49> PEG_CLKREQ#

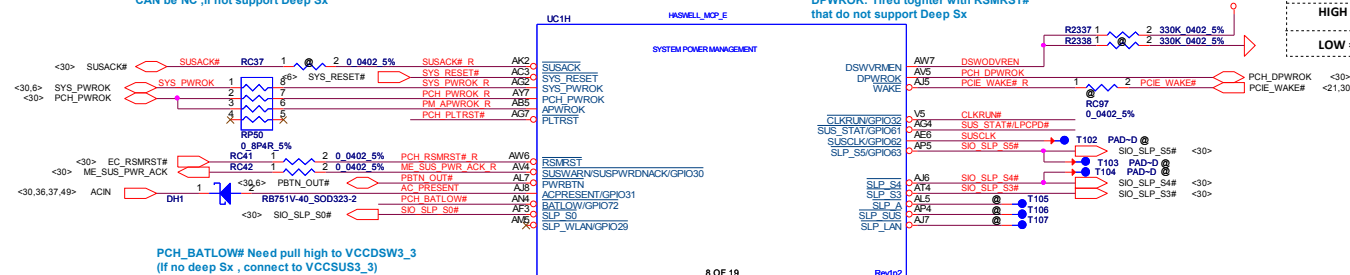
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CLK_PCIE_LAN#
LAN_CLKREQ#
CLK_PCIE_WLAN#
CLK_PCIE_WLAN#
WLAN_CLKREQ#
CLK_PEG_VGA#
CLK_PEG_VGA#
PEG_CLKREQ#



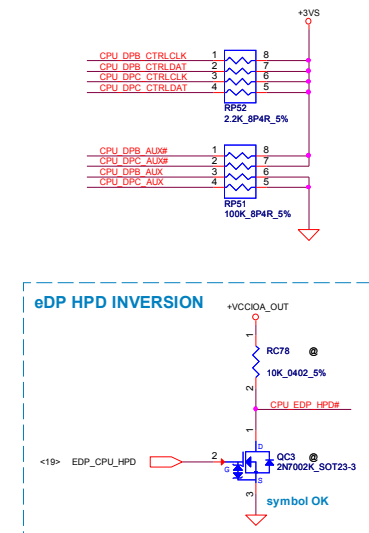
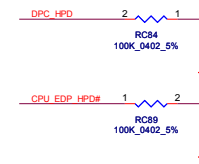
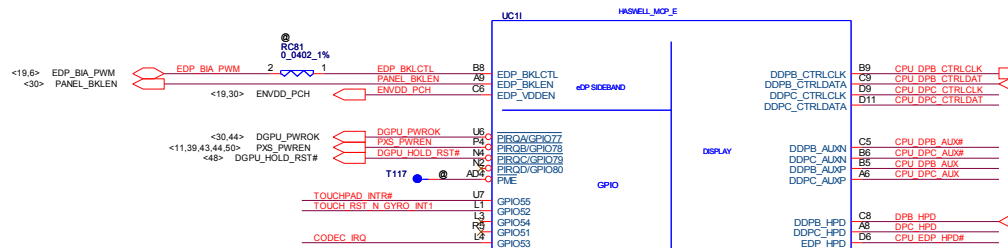
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Note: SUSACK# and SUSWARN# can be tied together if EC does not want to involve in the handshake mechanism for the Deep Sleep state entry and exit
CAN be NC ,if not support Deep Sx



PCH_BATLOW# Need pull high to VCCDSW3_3
(If no deep Sx , connect to VCCSUS3_3)



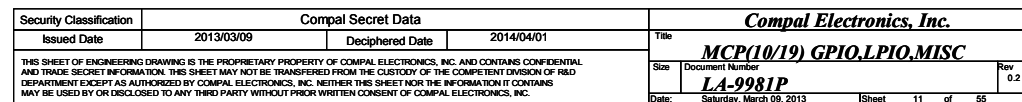
RC105

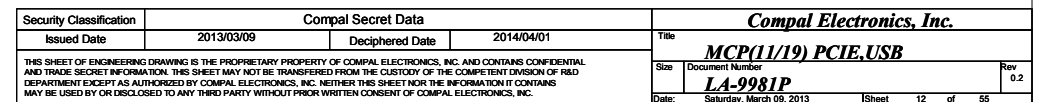
EDP CPU HPD 1 2 CPU EDP HPD#

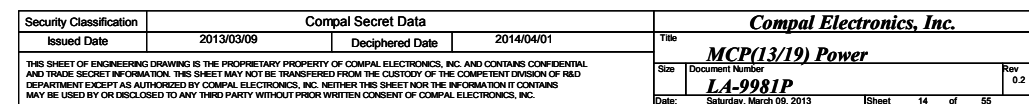
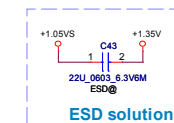
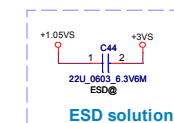
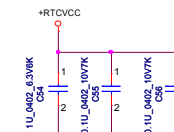
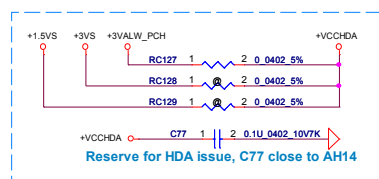
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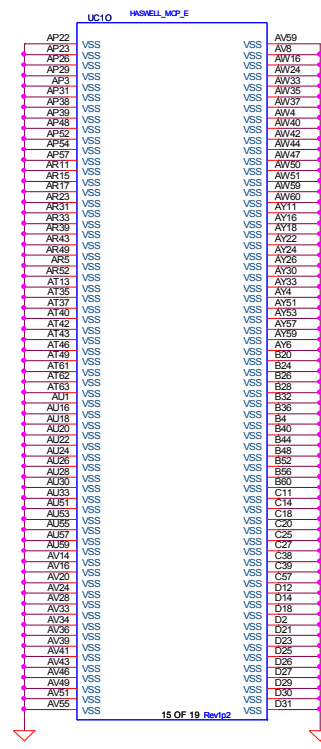
Reserve for debug

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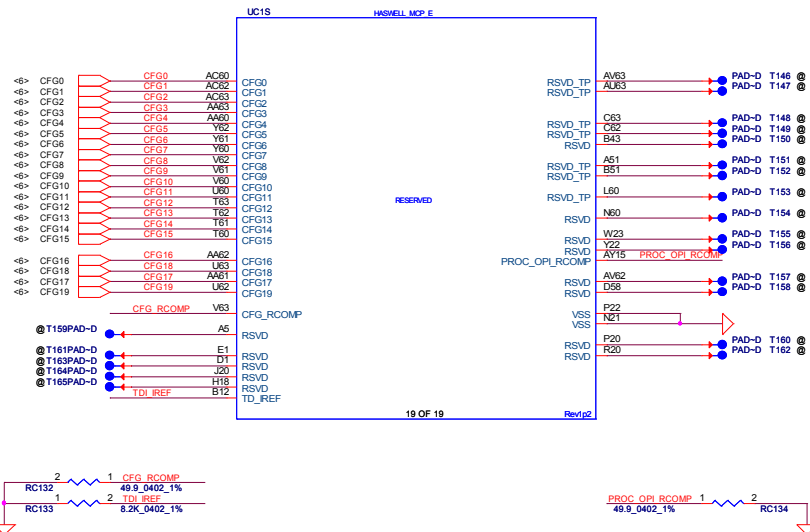
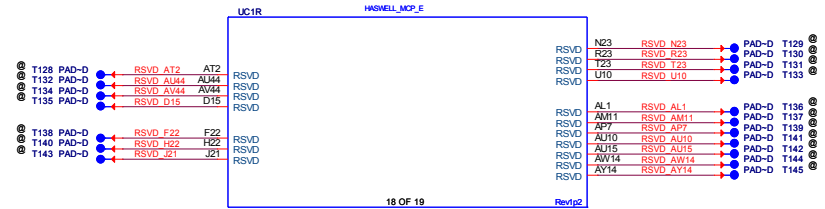
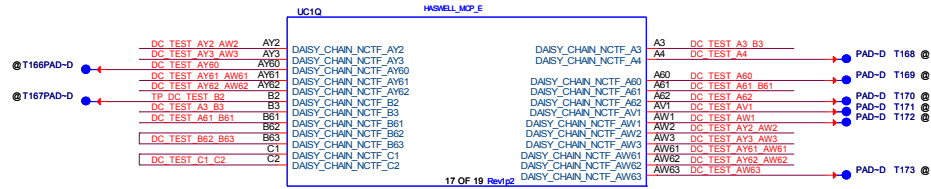




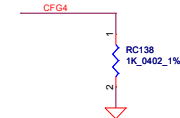




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CFG STRAPS for CPU



Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port
	0: Enabled; An external Display Port device is connected to the Embedded Display Port

H=4mm

2-3A to 1 DIMMs/channel

Populate RD1, De-Populate RD7 for Intel DDR3 VREFDQ multiple methods M1
Populate RD7, De-Populate RD1 for Intel DDR3 VREFDQ multiple methods M3

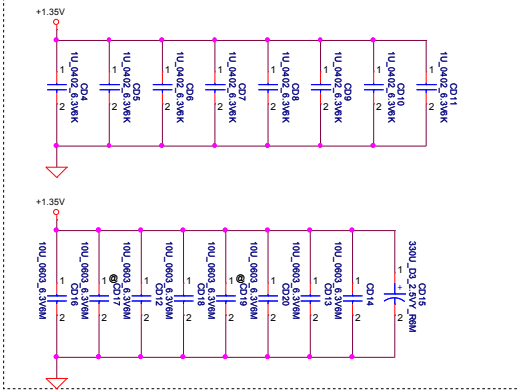
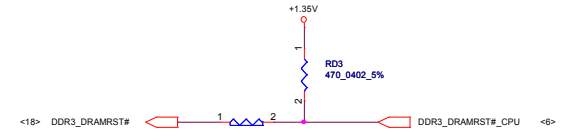
<7> DDR_A_DQS[0..7]
<7> DDR_A_DQ[0..63]
<7> DDR_A_DQS[0..7]
<7> DDR_A_MA[0..15]

All VREF traces should have 10 mil trace width

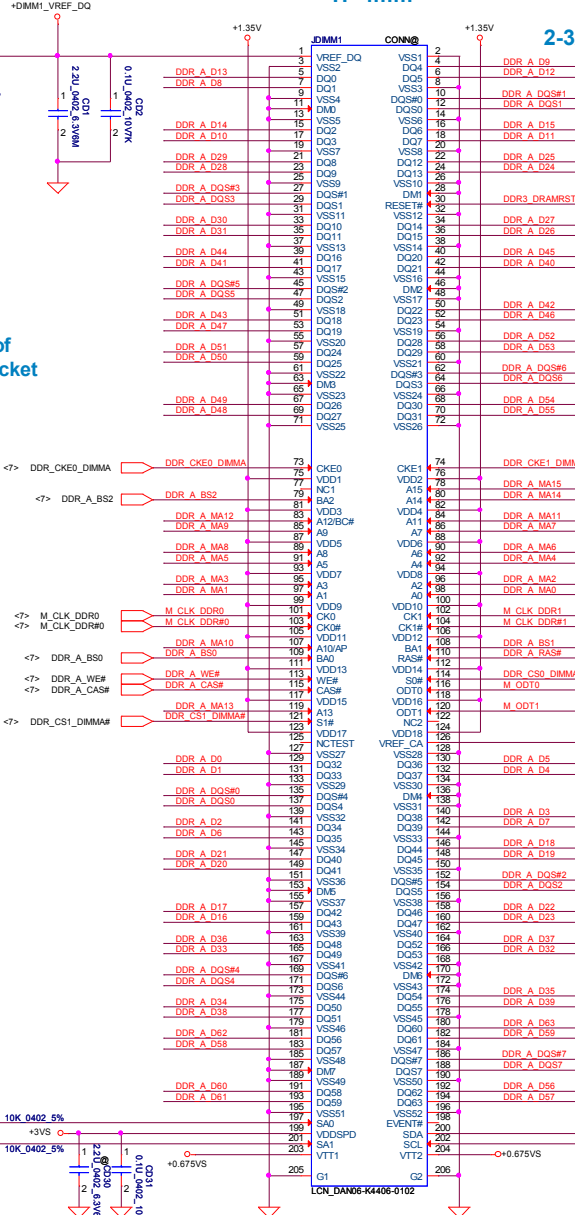
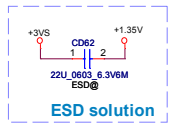
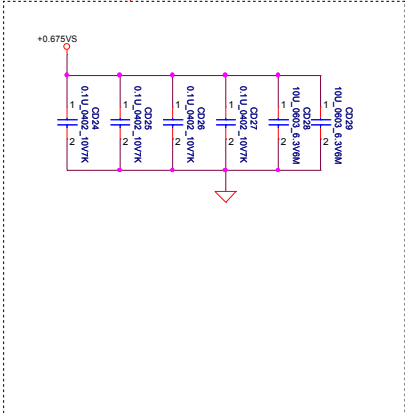
Layout Note:
Place near JDIMM1

Note:
Check voltage tolerance of VREF_DQ at the DIMM socket

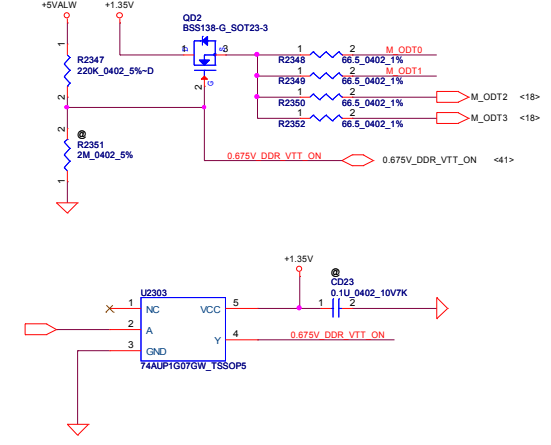
CAD NOTE
PLACE THE CAP NEAR TO DIMM RESET PIN



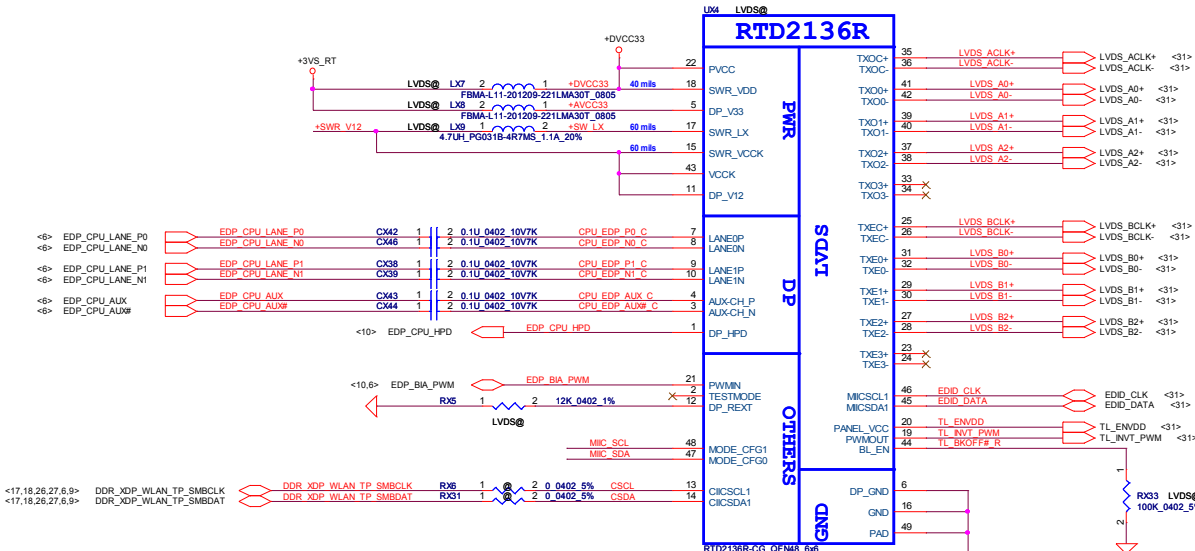
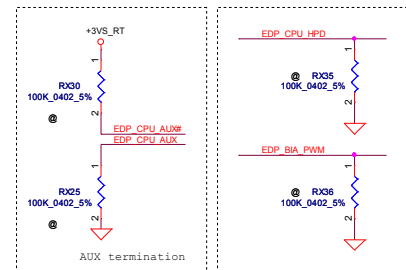
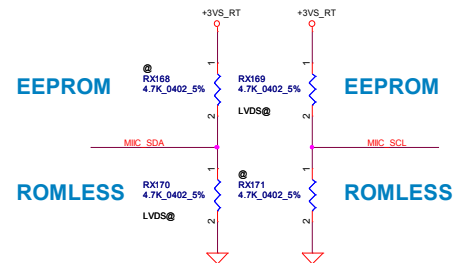
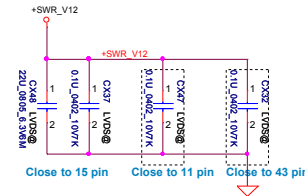
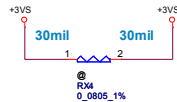
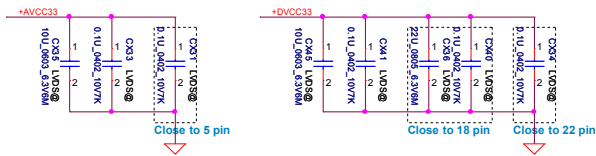
Layout Note:
Place near JDIMM1.203,204



DDR3L SODIMM ODT GENERATION

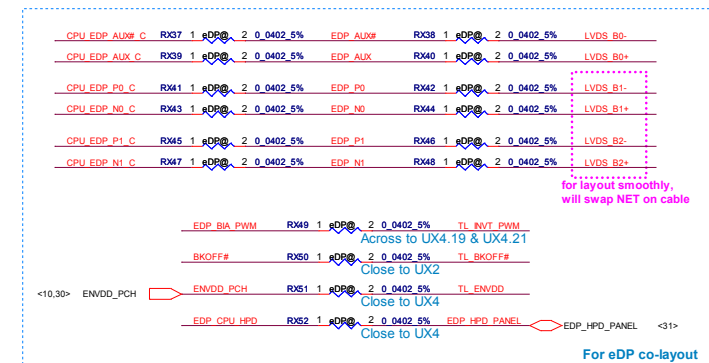
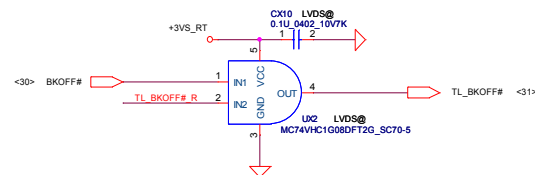


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Issued Date	2013/03/09	Deciphered Date	2014/04/01	DDR3L DIMMA	
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				Date	Sheet
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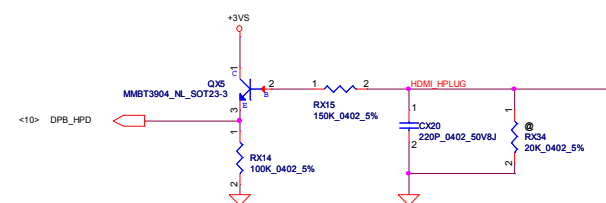
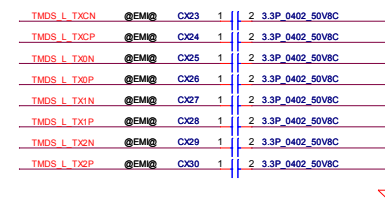
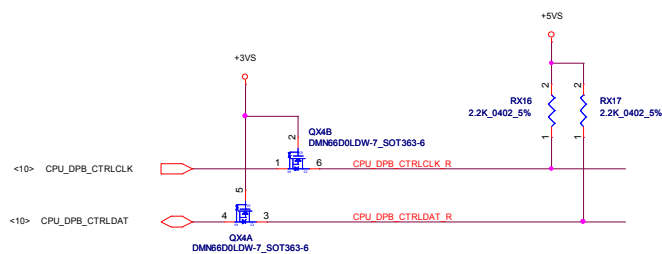
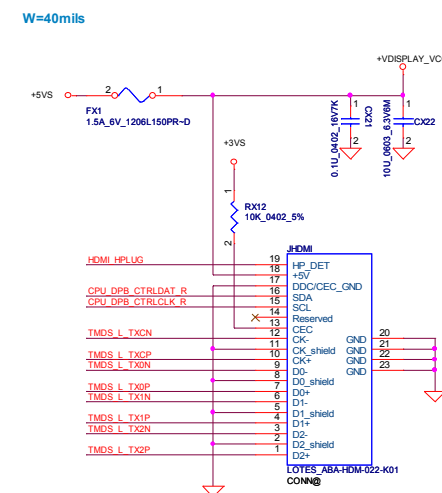
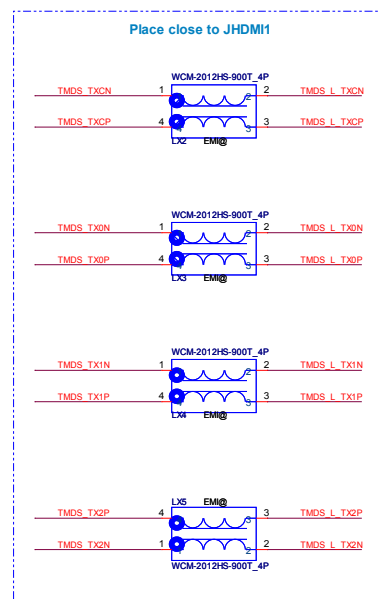
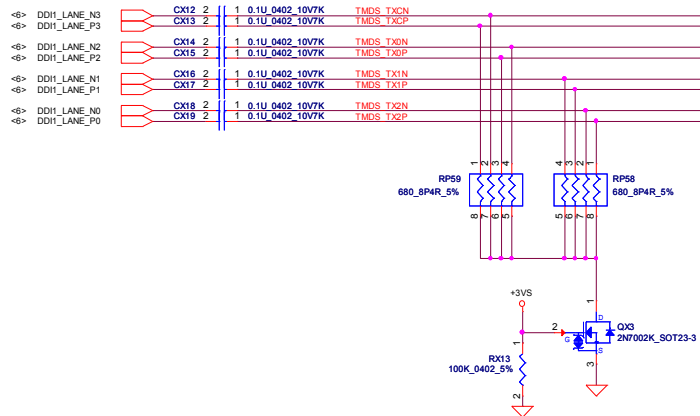


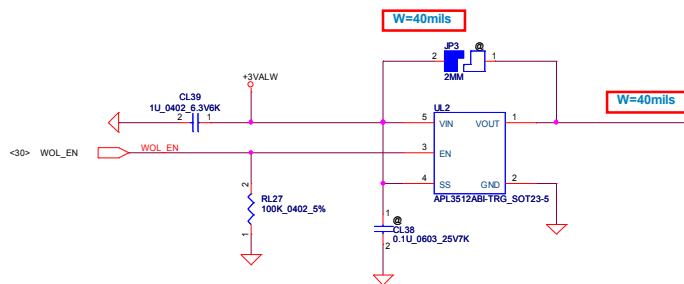
RTD2136S : SA00004NW10
RTD2136R : SA000067100

Vendor advise reserve it



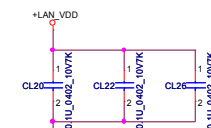
Security Classification		Compal Secret Data		Title	
Issued Date	2013/03/09	Deciphered Date	2014/04/01	Compal Electronics, Inc.	
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				Size	Document Number
				LA-9981P	
				Date	Rev
				Saltwater, March 08, 2013	0.2
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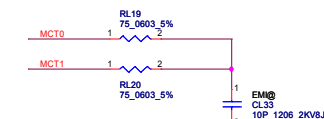


W=40mils +LAN_IO rising time : >1ms and <100ms

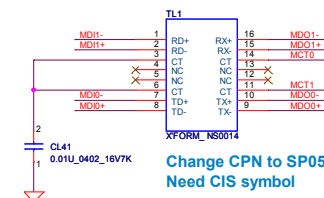
These caps close to Pin 23,32
For 8106E pop the capacitor close pin 23,32



These caps close to Pin 8,30
For 8106E pop capacitor close to pin 8,30

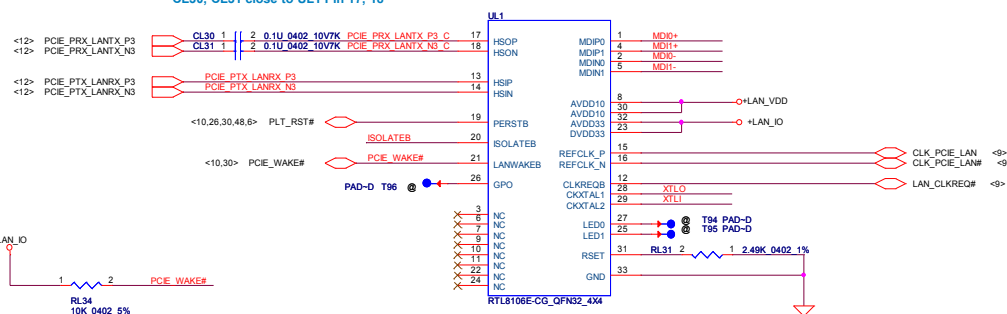


Place close to TCT pin

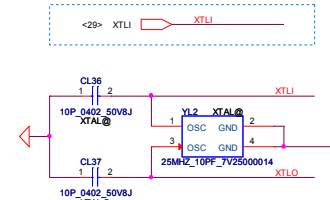


Change CPN to SP050007J00 only
Need CIS symbol

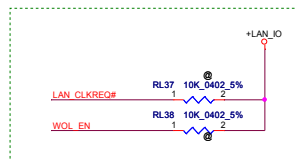
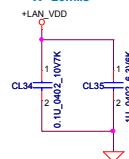
CL30, CL31 close to UL1 Pin 17, 18



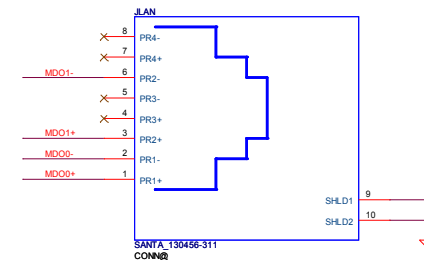
For GCLK



W=20mils



Reserve 10K pull LAN_IO

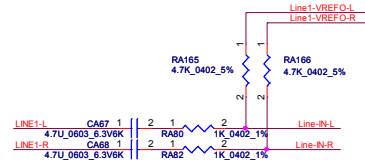


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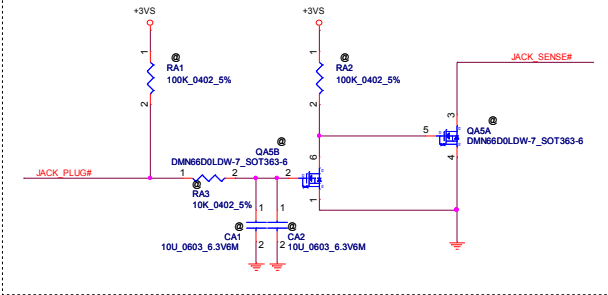
CA71, CA51 place close to Pin 26

CA53, CA55 change Value
from 10U_0603_6.3V6M~D to
4.7U_0603_6.3V6K

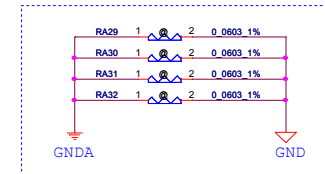
Reserve for HDA issue



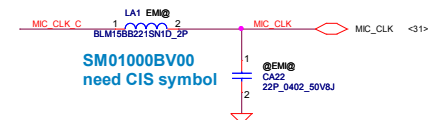
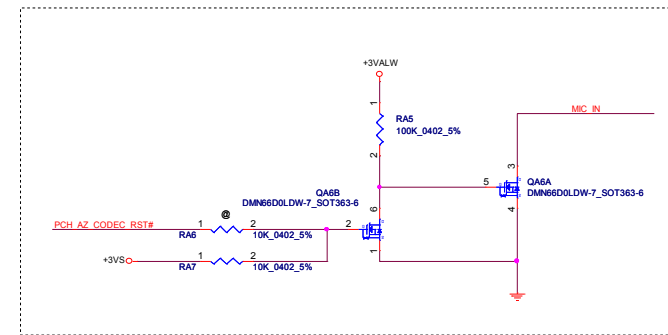
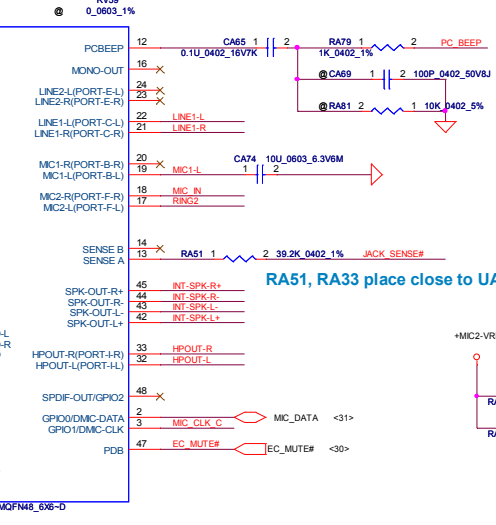
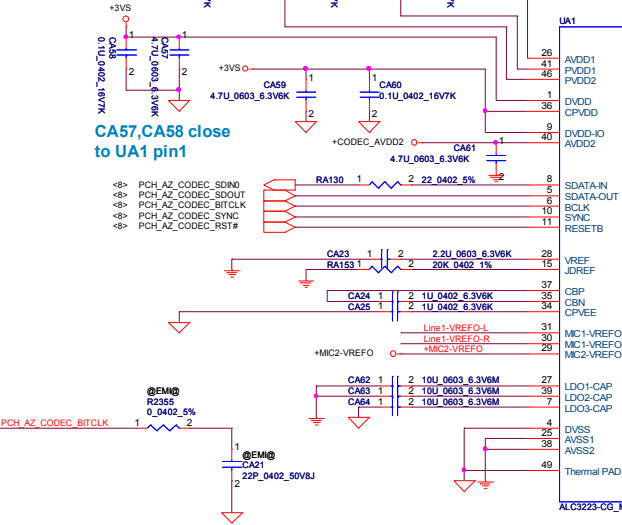
JACK_PLUG Delay circuitis



Reserve for cancel Delay circuitis



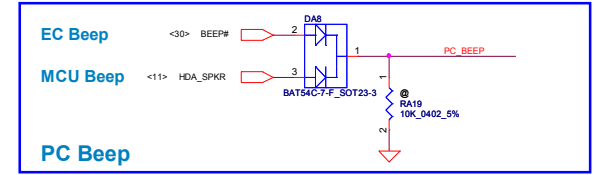
Place on the moat between GND & GNDA.



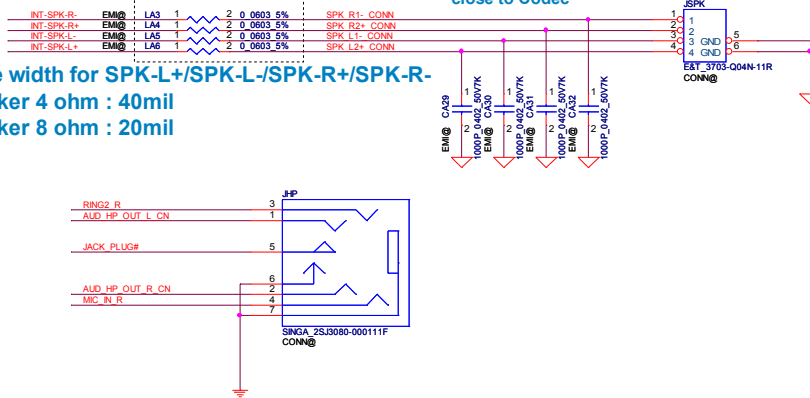
SM01000BV00
need CIS symbol

Close to UA1
Pin11,13,14,16

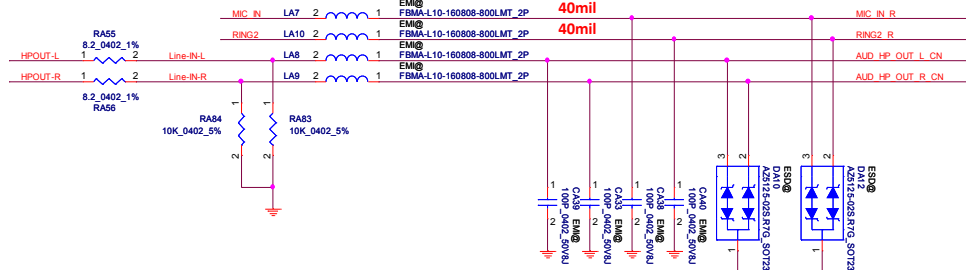
Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-R-
Speaker 4 ohm : 40mil
Speaker 8 ohm : 20mil



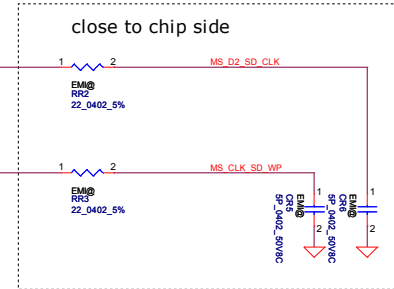
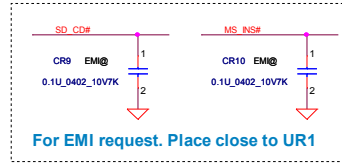
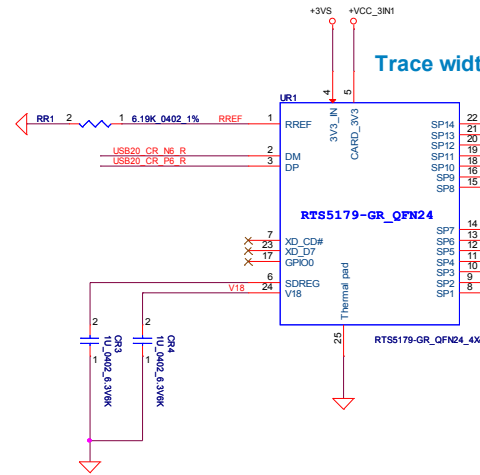
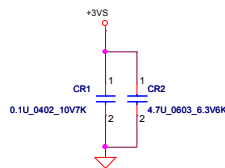
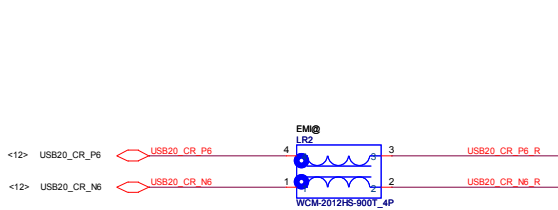
close to Codec



iPhone and Nokia type Combo Jack

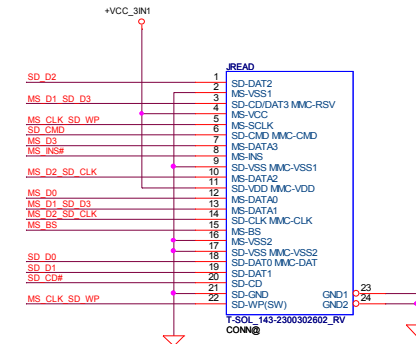
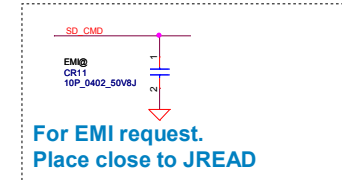
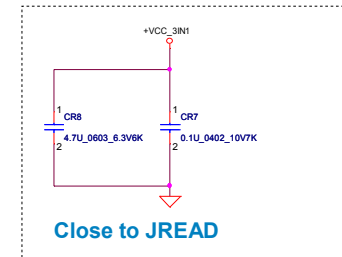


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2013/03/09		2014/04/01		Audio Codec ALC3223	
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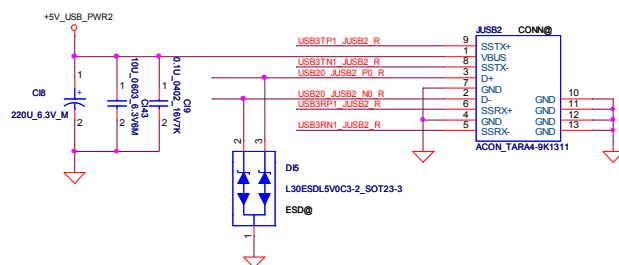
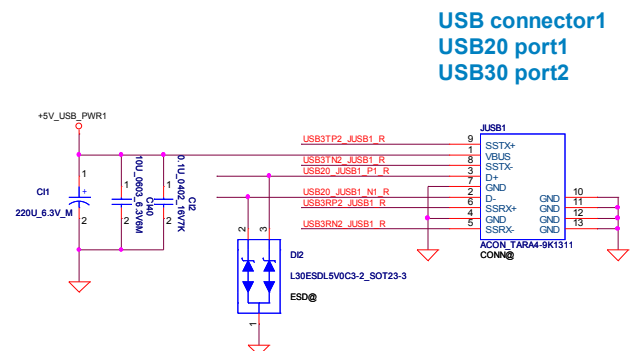


拉MS_D2_SD_CLK到Conn pin 13 SD_CLK
再打Via拉到pin 10 MS_D2

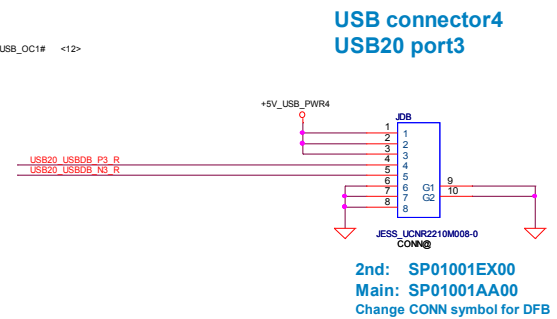
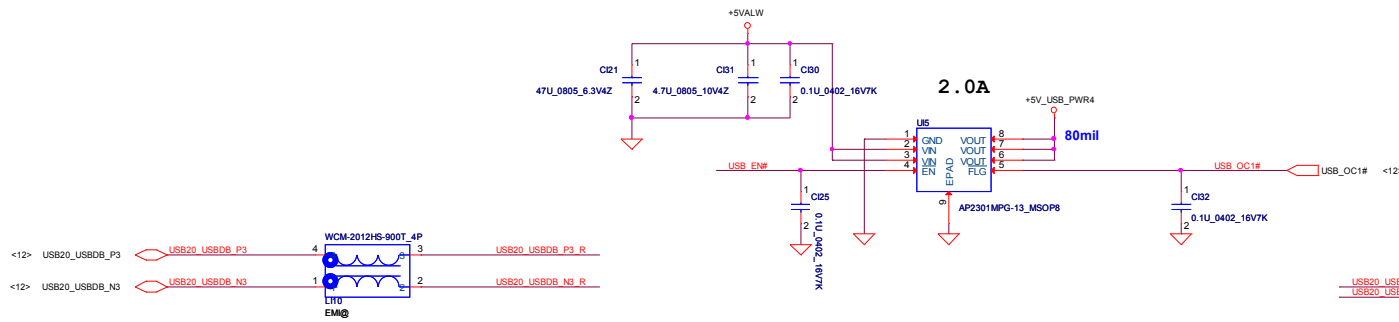
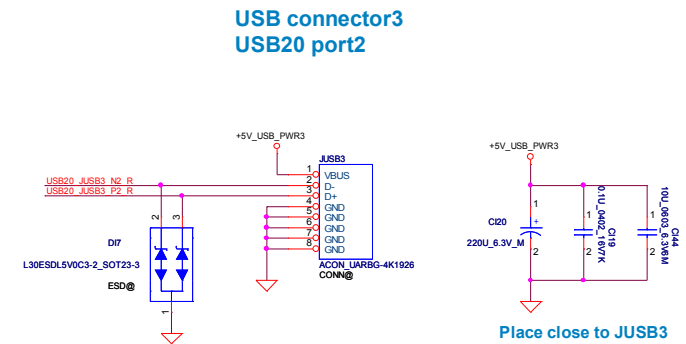
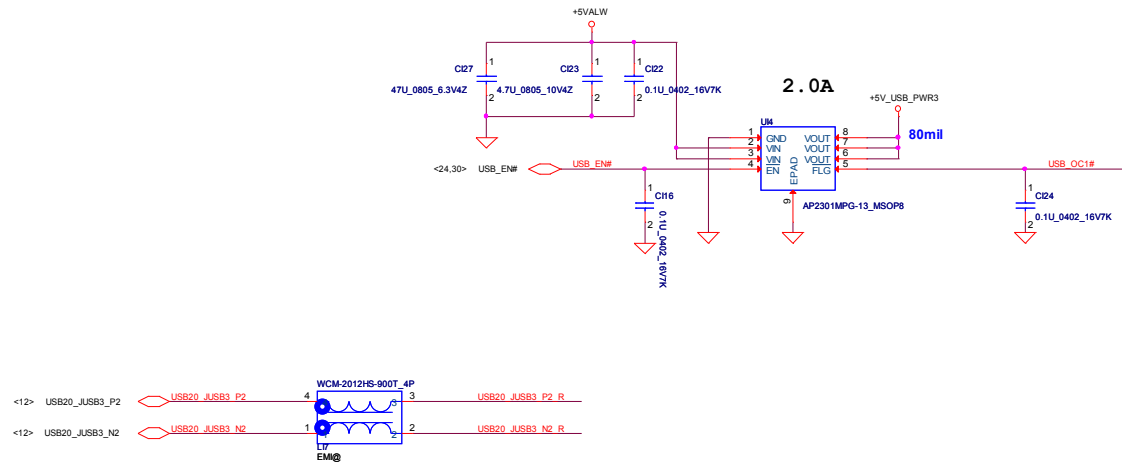
拉MS_CLK_SD_WP到Conn pin 5 MS_CLK
再打Via拉到pin 20 SD_W



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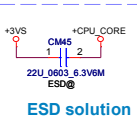
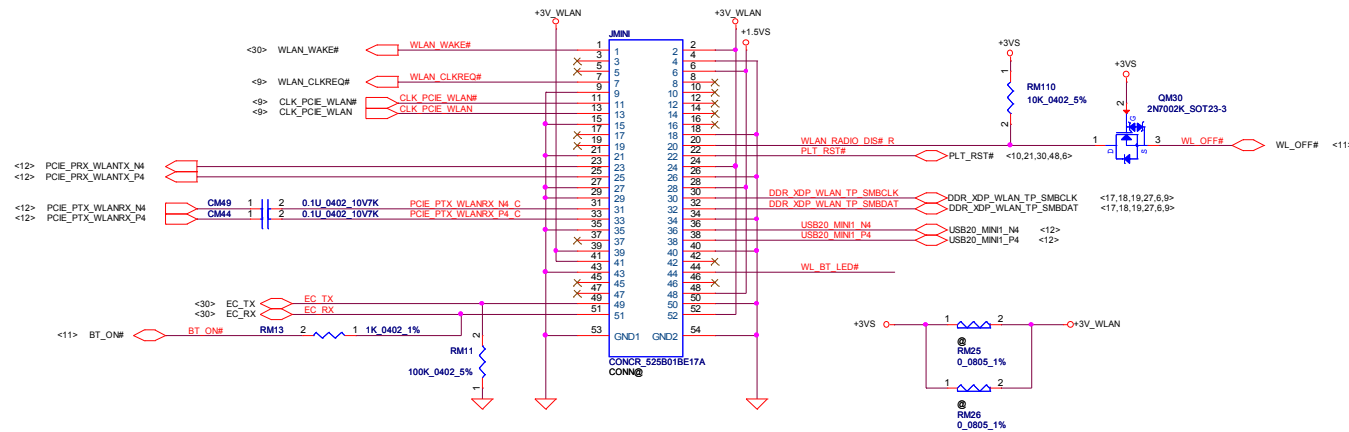


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						Size	Document Number		Rev
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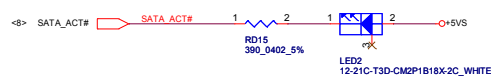


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Mini WLAN/WIMAX H=6.7



HDD LED

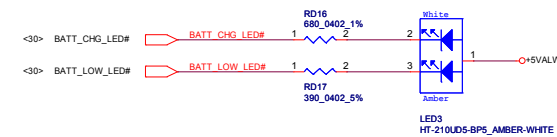


Power LED

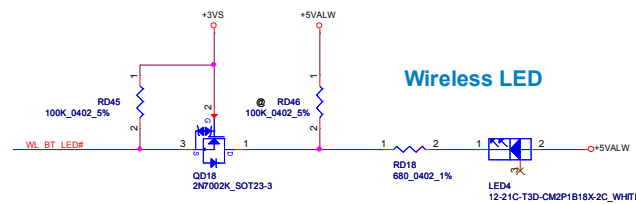


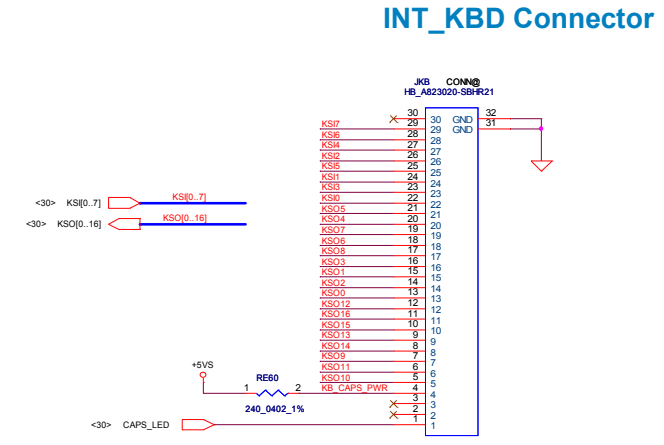
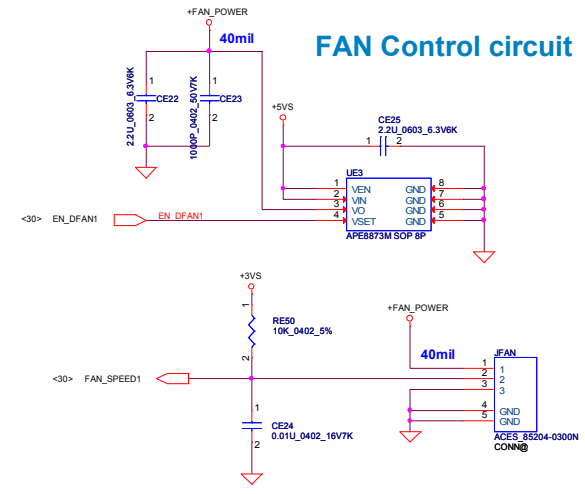
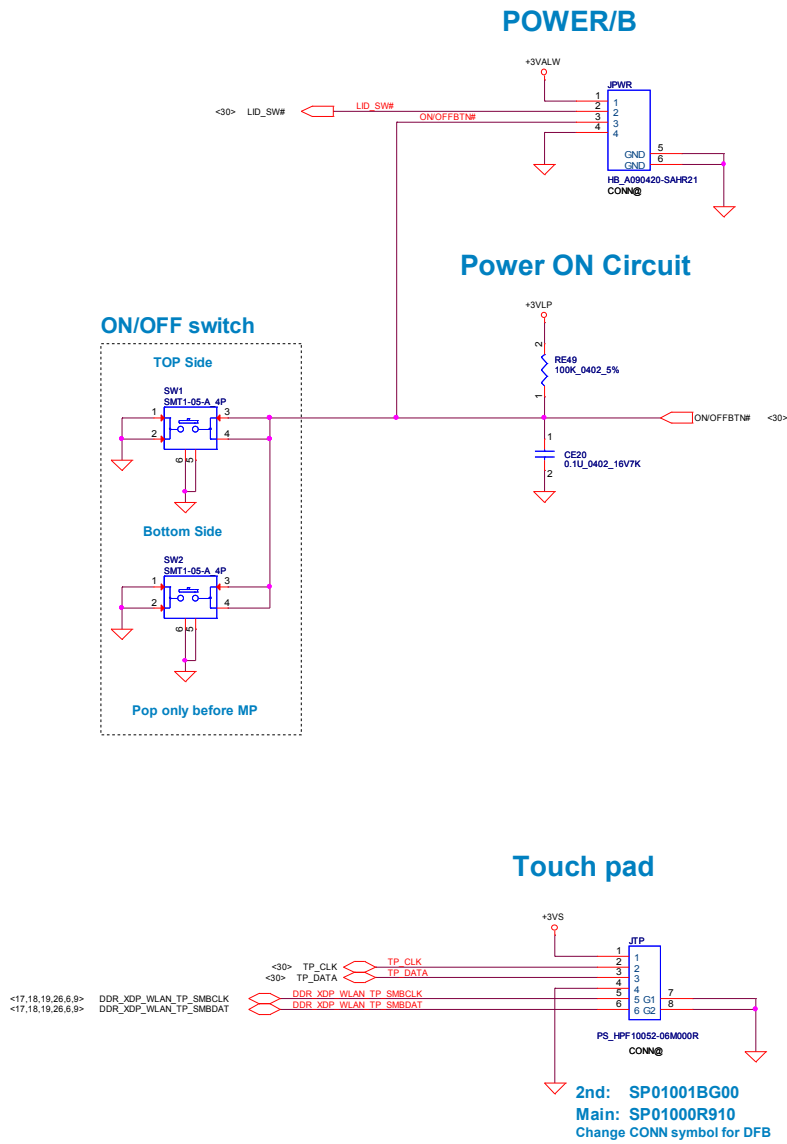
10mils, All pins

Battery LED

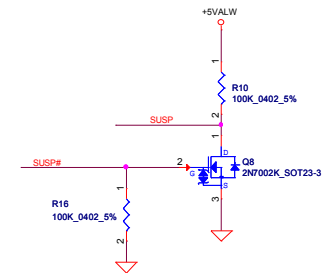
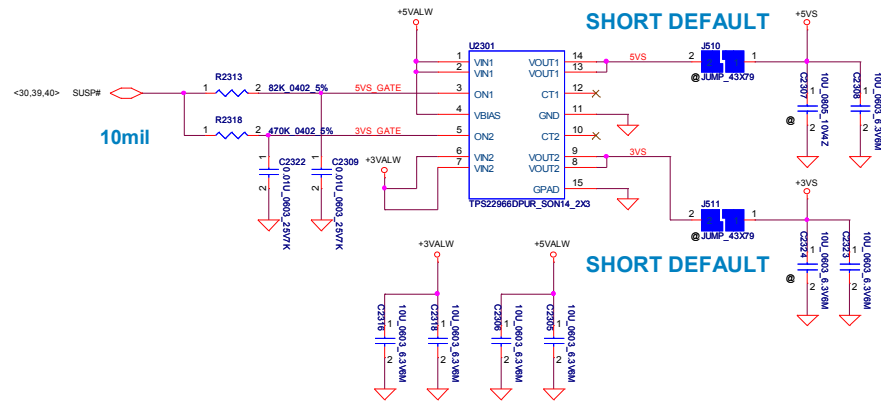


Wireless LED

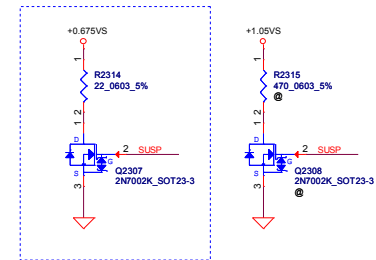
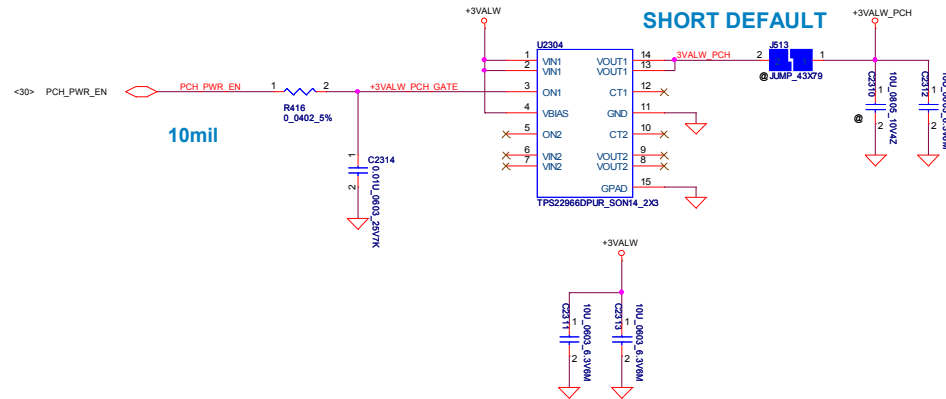




+5VS and +3VS switch

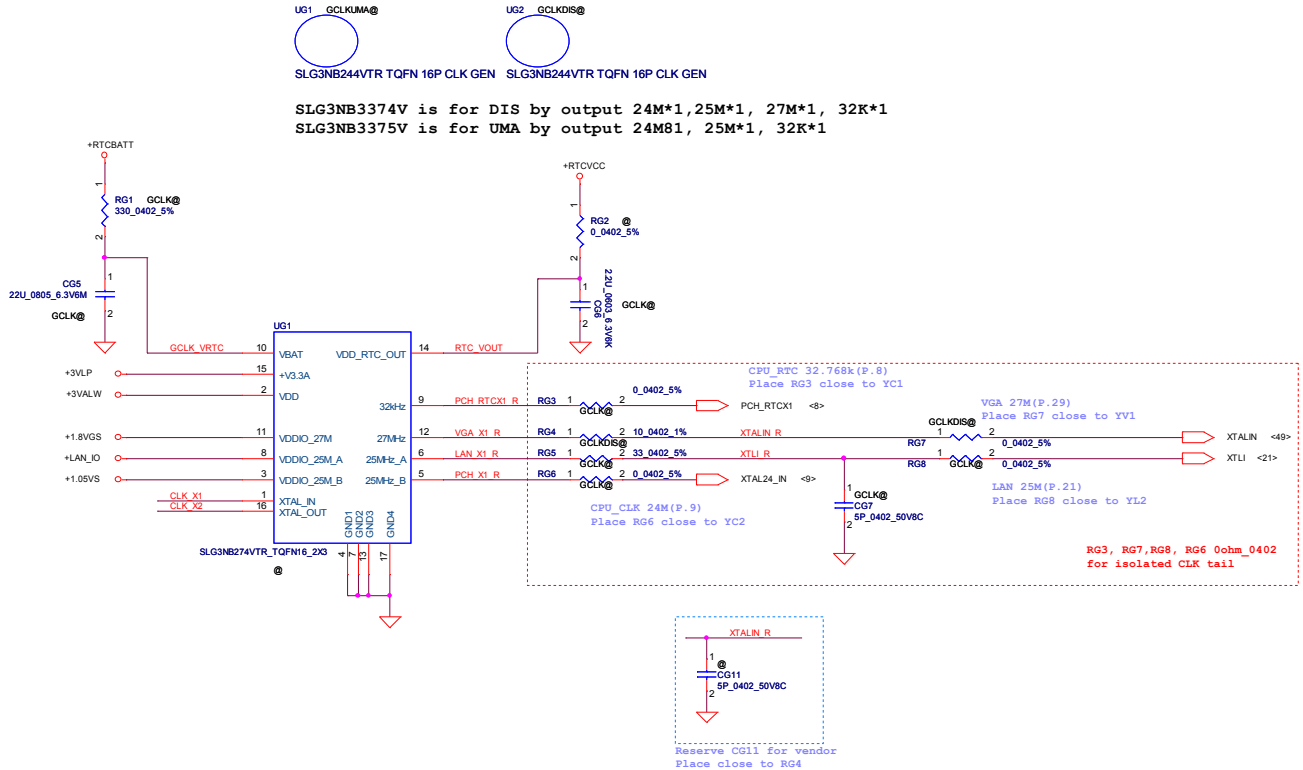
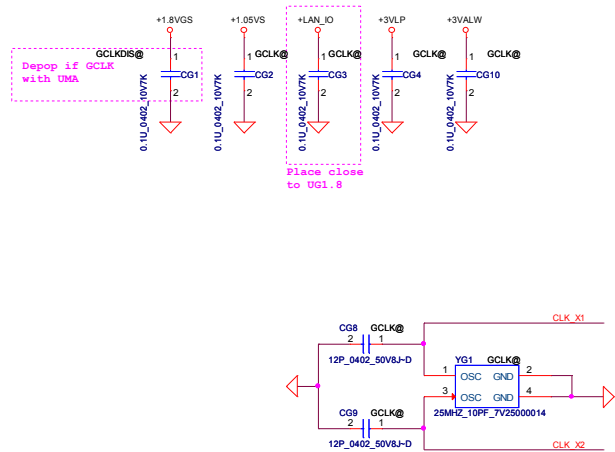


+3VALW_PCH switch

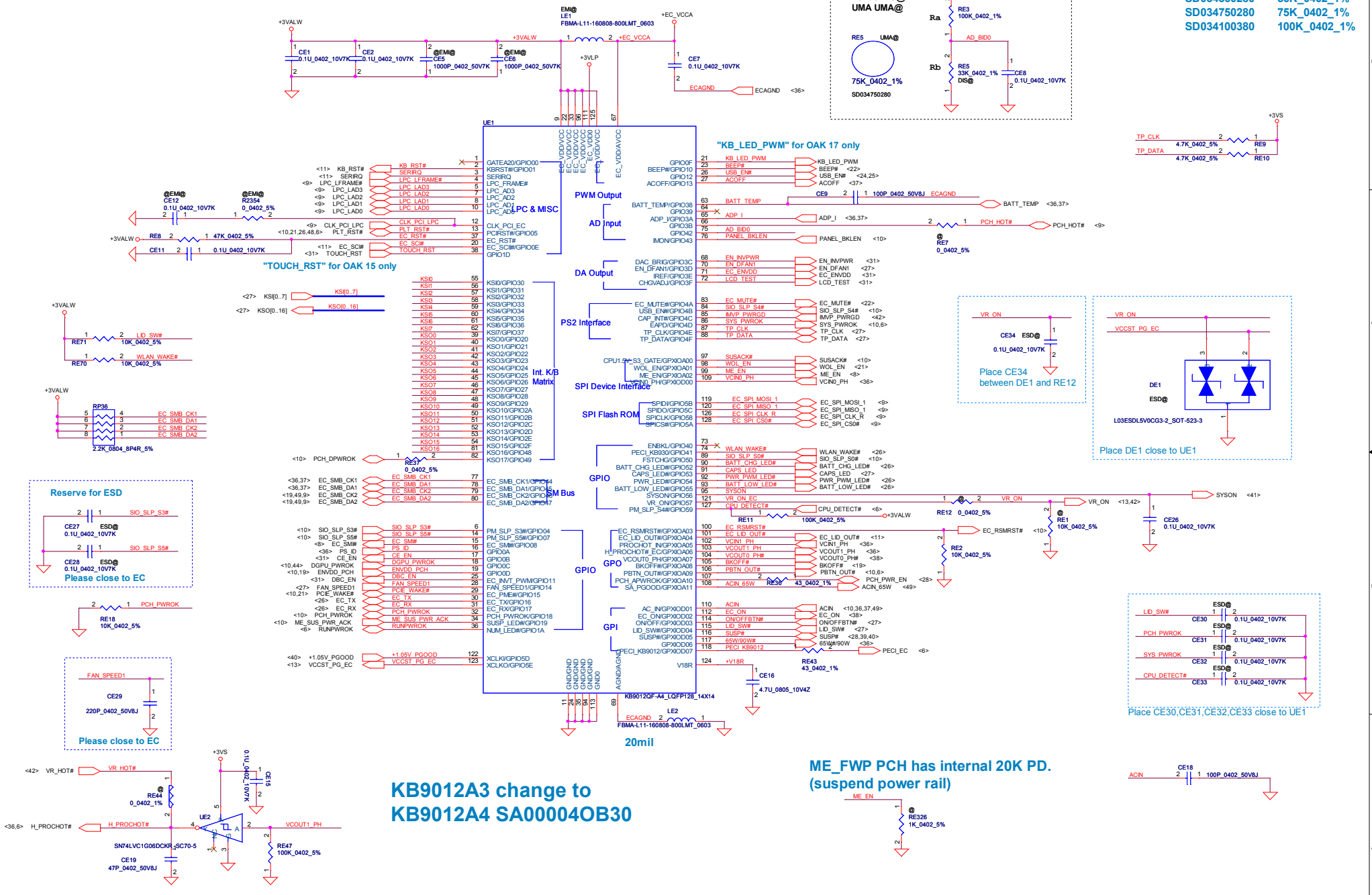
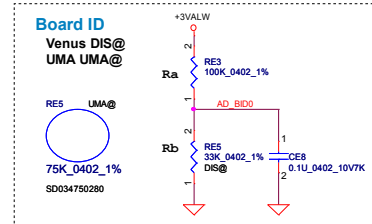


For Intel S3 Power Reduction

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SD034120280 12K_0402_1%
SD034100300 27K_0402_1%
SD034430280 33K_0402_1%
SD034430280 43K_0402_1%
SD034560280 56K_0402_1%
SD034750280 75K_0402_1%
SD034100380 100K_0402_1%

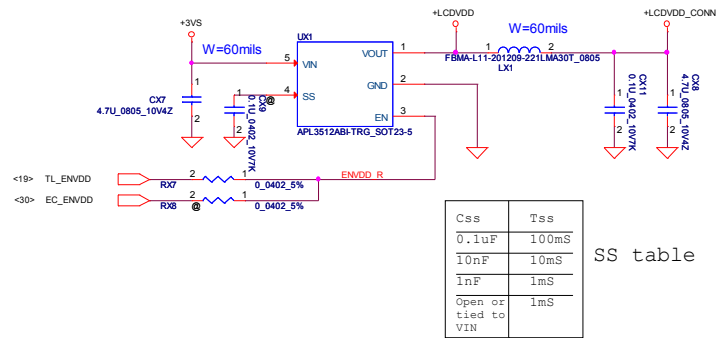


KB9012A3 change to
KB9012A4 SA00004OB30

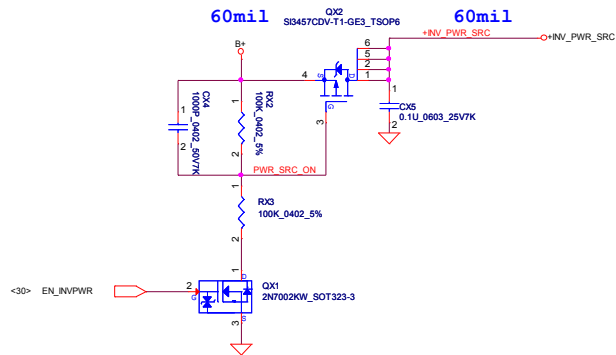
ME_FWP PCH has internal 20K PD.
(suspend power rail)

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				Rev	0.2
				Date	Saturday, March 09, 2013
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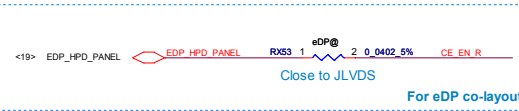
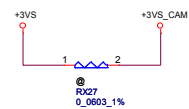
LCD PWR CTRL



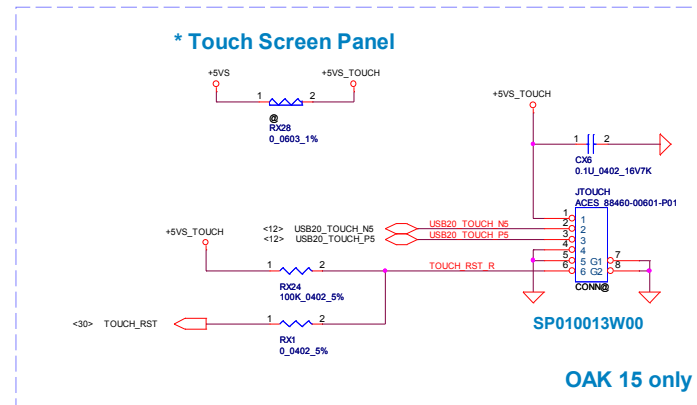
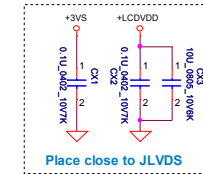
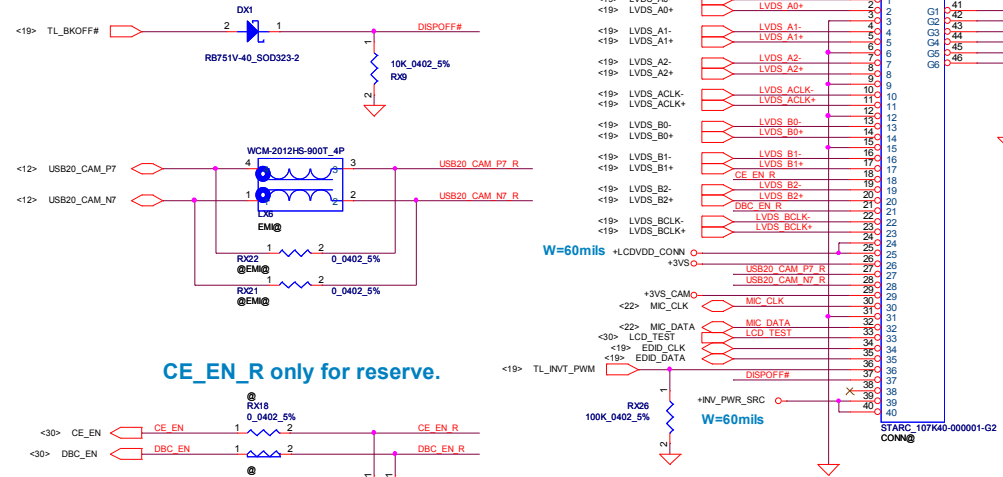
LCD backlight PWR CTRL



Webcam PWR CTRL

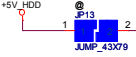


LVDS Connector

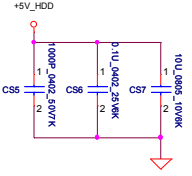
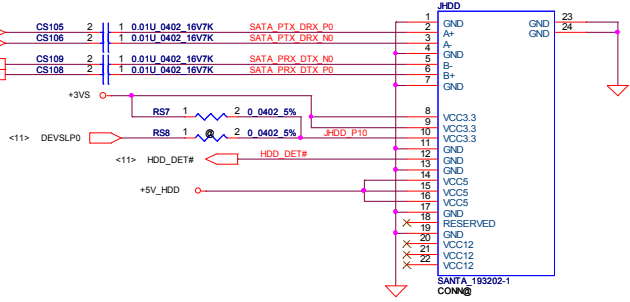


SATA HDD Connector

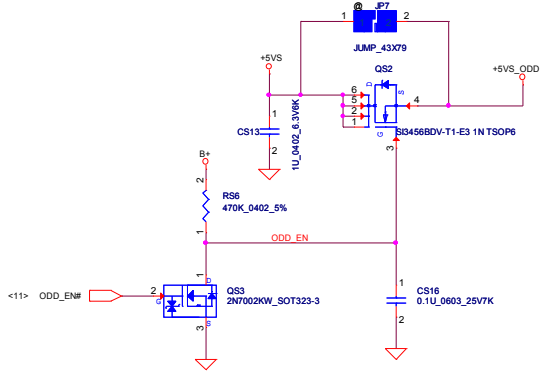
+5V_HDD Source



SHORT DEFAULT

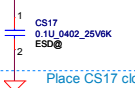
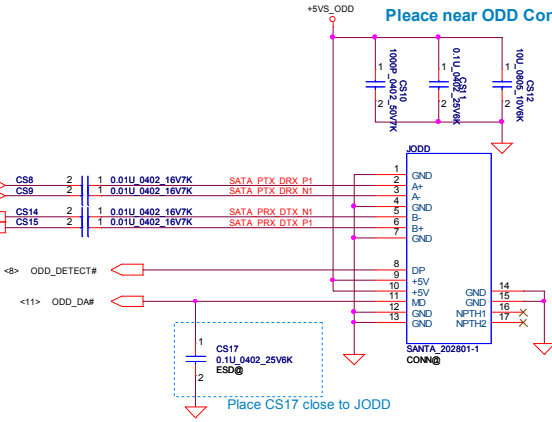


ODD Power Control

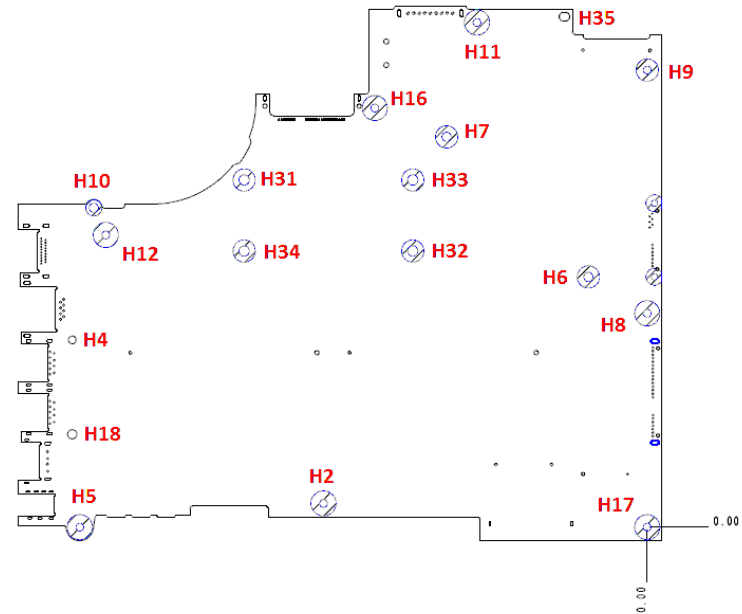
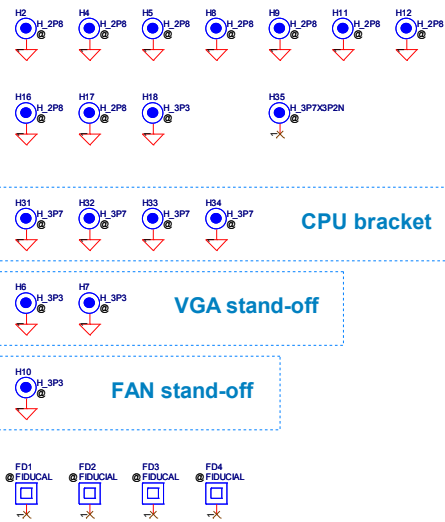


SATA ODD Connector

Please near ODD Connector



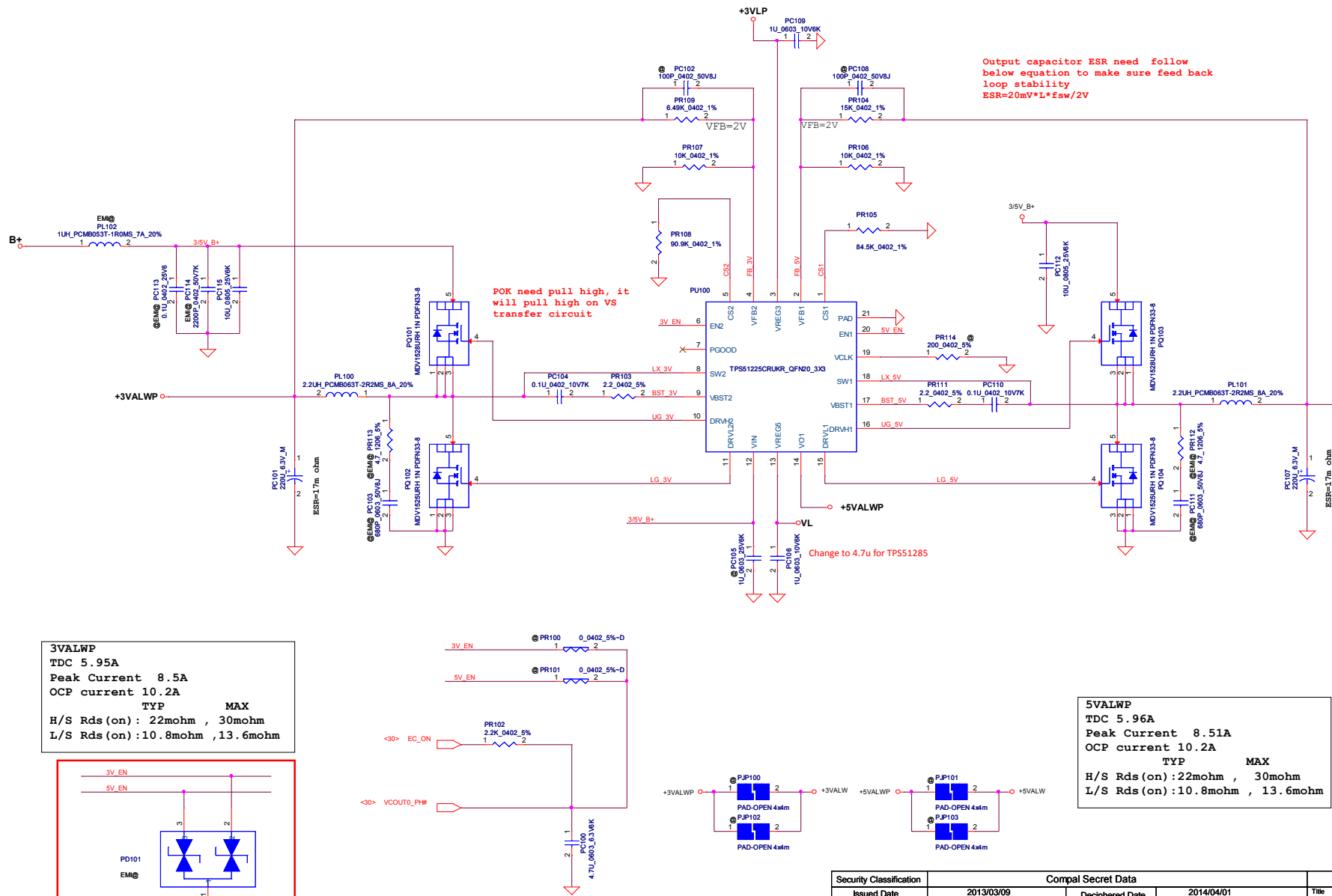
Screw Hole



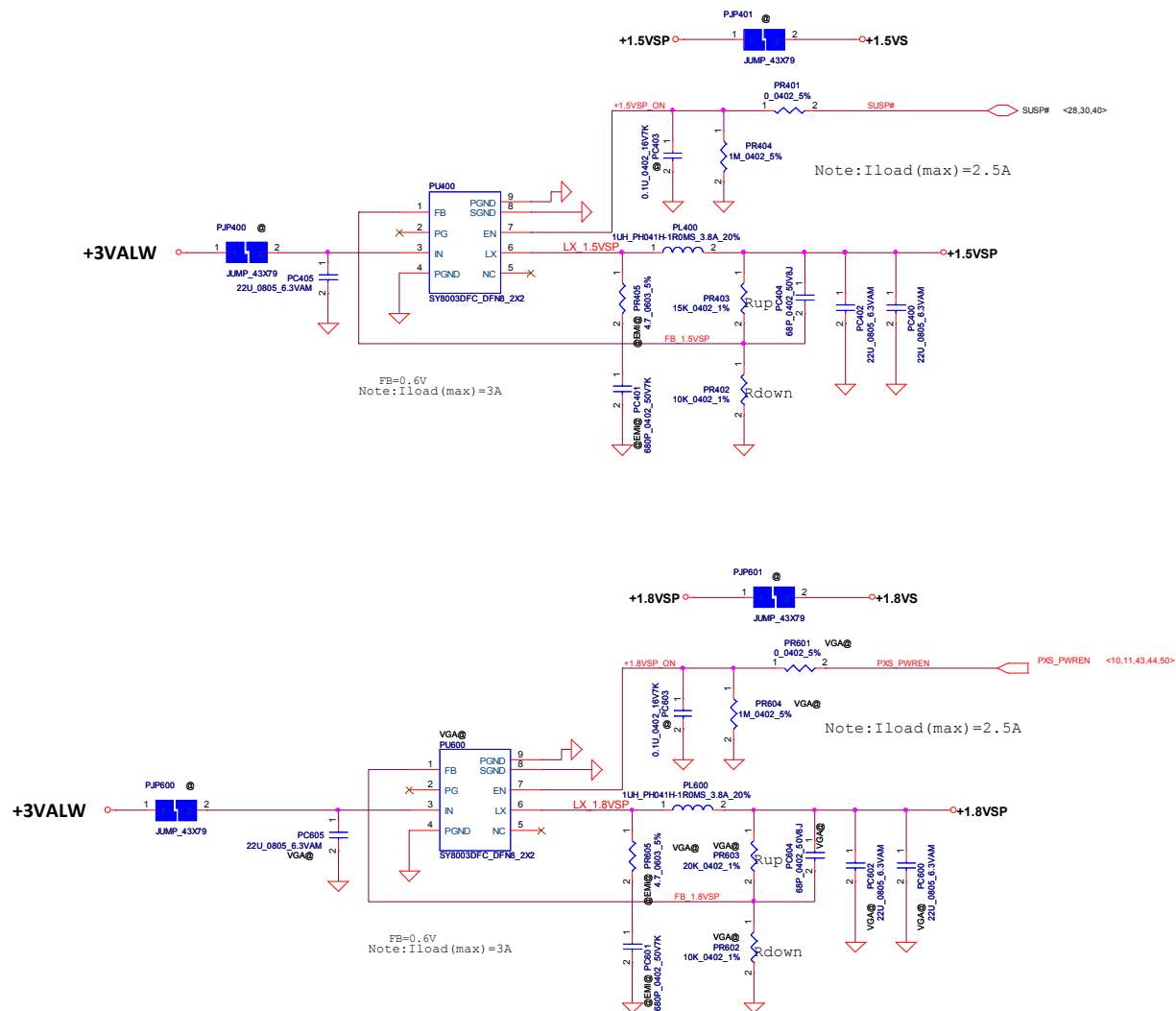
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Issued Date	2013/03/09	Deciphered Date	2014/04/01	Title		
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Date:				Saturday, March 09, 2013	Sheet 33 of 55	

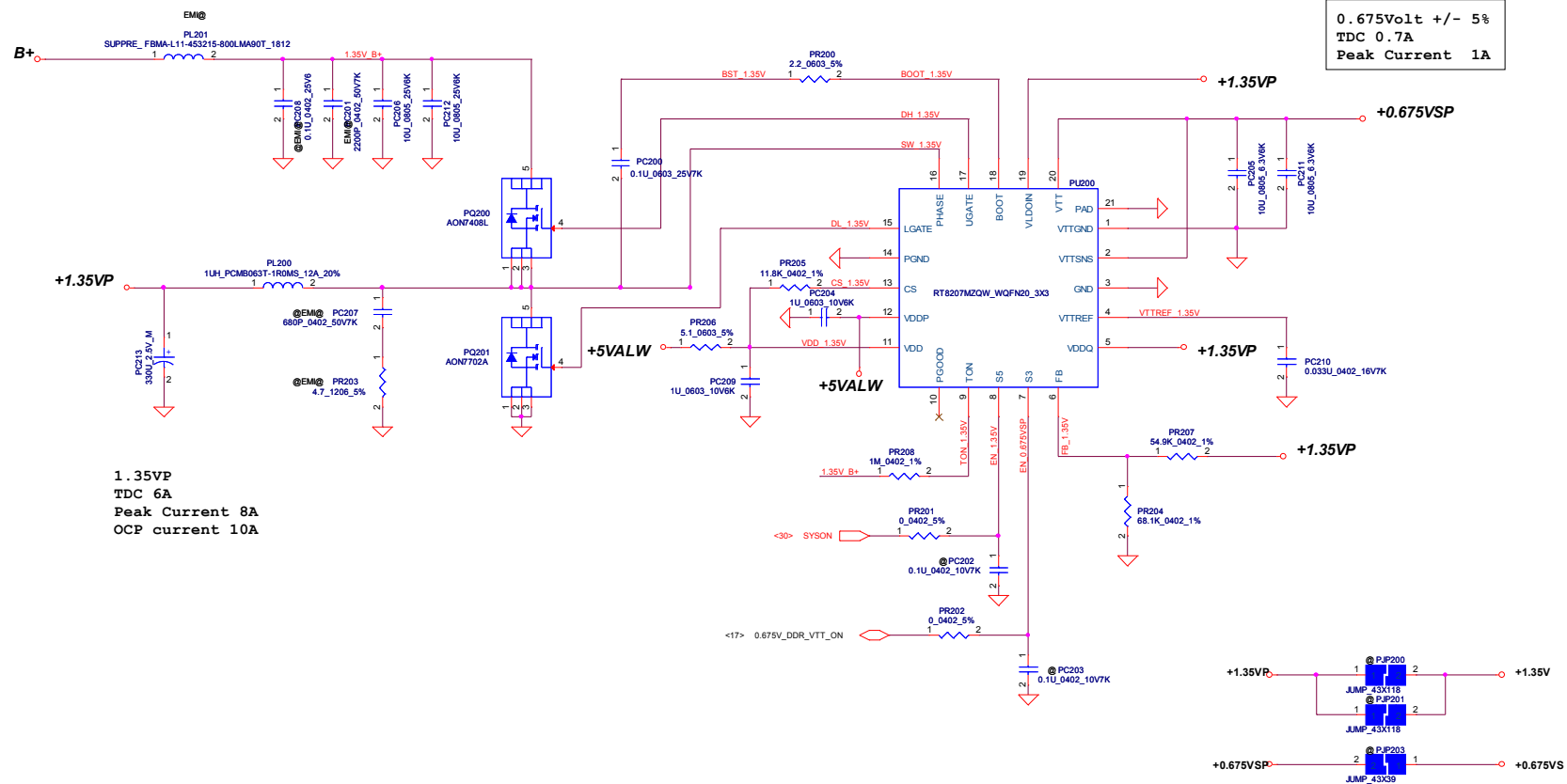
Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	34	Card Reader	2012/04/27	HW	The Card reader USB signal is incorrect.	SWAP URL USB signal P/N	0.2
2							
3							
4							
5							
6							
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Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
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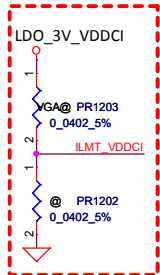
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/03/09	Deciphered Date	2014/04/01	Title	PWR 3.3VALWP/SVALWP
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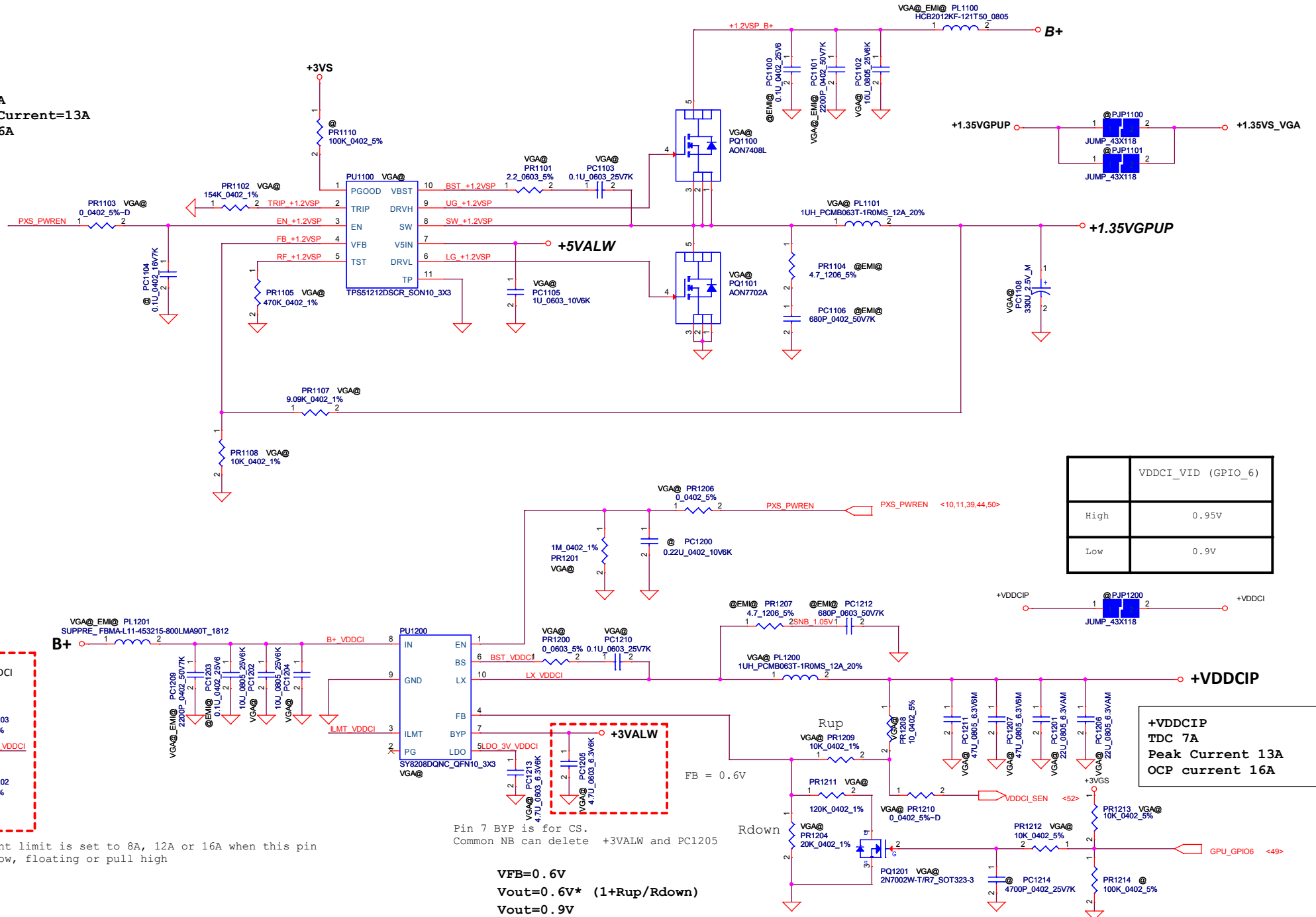


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TDC=9A
Peak Current=13A
OCP=16A



The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high



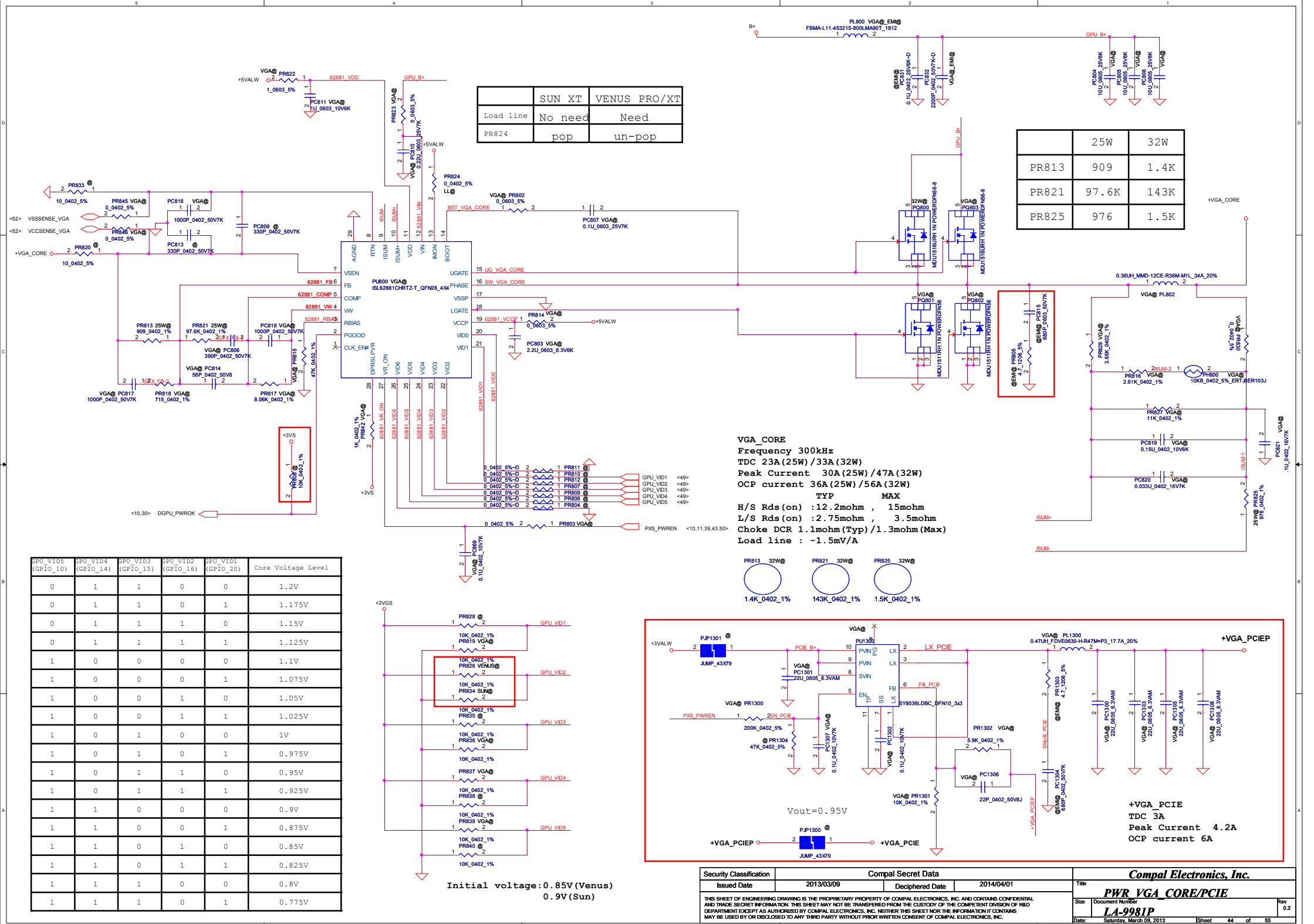
	VDDCI_VID (GPIO_6)
High	0.95V
Low	0.9V

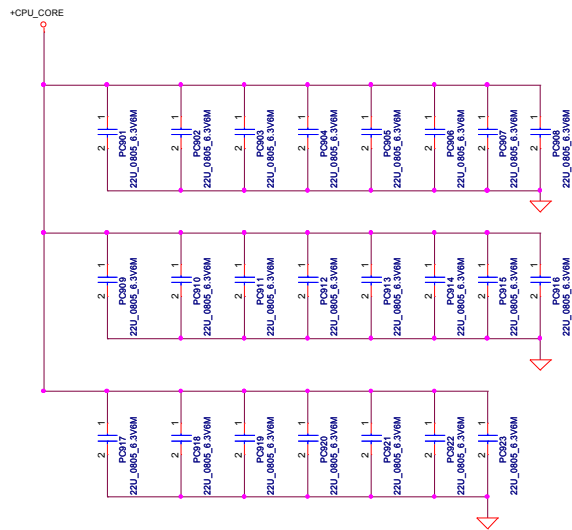
+VDDCIP
TDC 7A
Peak Current 13A
OCP current 16A

VFB=0.6V
Vout=0.6V* (1+Rup/Rdown)
Vout=0.9V

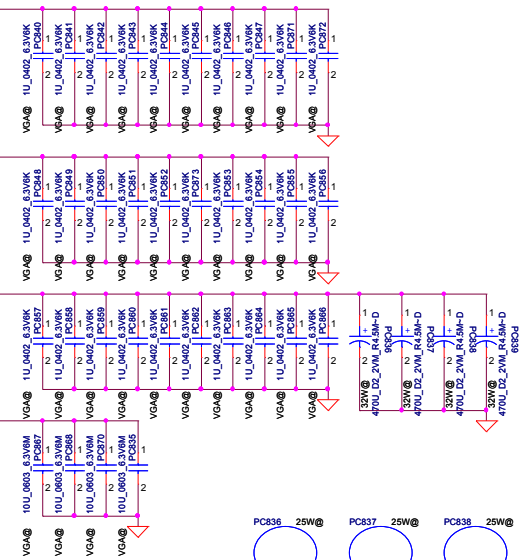
Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC1205

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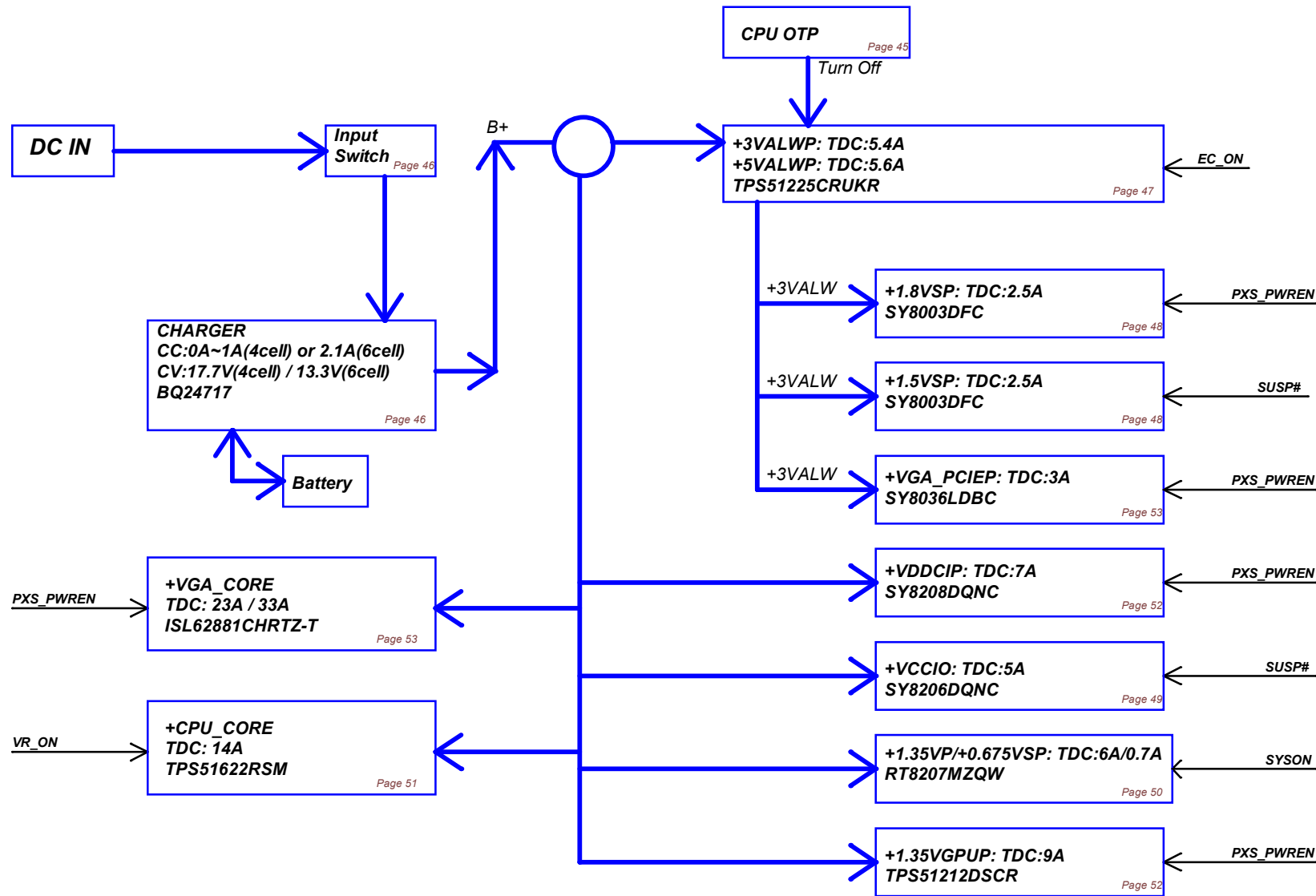




+VGA_CORE



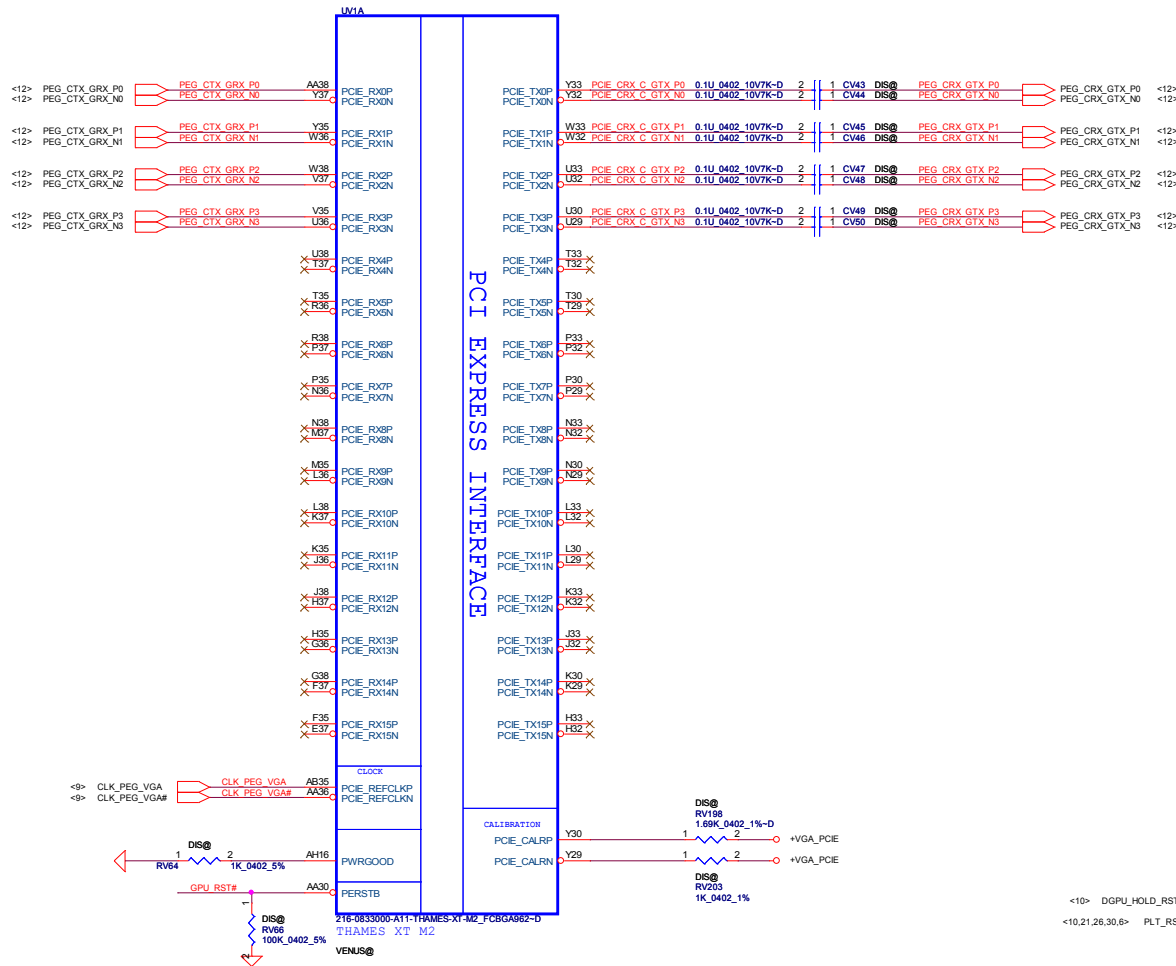
Power block



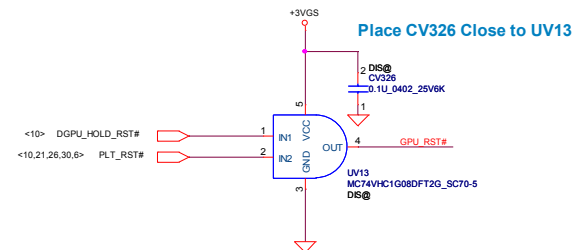
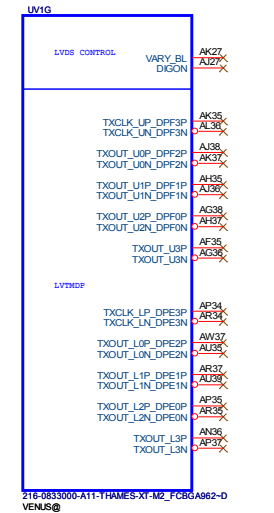
Page 1

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GFX PCIE LANE REVERSAL

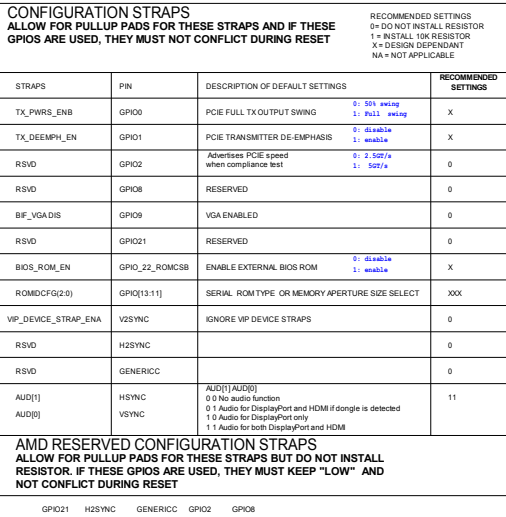


LVDS Interface



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GPIO1	GPU_GPIO1
GPIO2	GPU_GPIO2
GPIO7	N.C
GPIO11	GPU_GPIO11
GPIO12	GPU_GPIO12
GPIO13	GPU_GPIO13
GPIO14	N.C
GPIO18	N.C

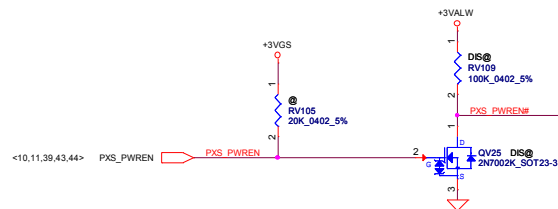


Vendor	RV241	RV242	Bits [3:1]
HYXINX 2Gb SA00006H40L(R1) SA00006H41L(R3)	NC	4.75K	000
SAMSUNG 2Gb SA00005SH0L(R3) SA00005SH1L(R1)	8.45K	2K	001
MICRON 2Gb SA00005XB0L(R3) SA00005XB1L(R1)	4.75K	NC	111

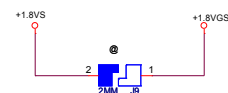
Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date	2013/03/09	Deciphered Date	2014/04/01	Title	ATI Sun XT M2 Main MSIC		
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Note:

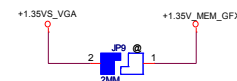
PX4.0 +VGA_CORE,VDDCI,+1.5VGS ON
PX4.0 +3VGS, +1.0VGS,+1.8VGS OFF
PX5.0 +3VGS,+VGA_CORE,VDDCI,+1.5VGV,+1.0VGS,+1.8VGS OFF



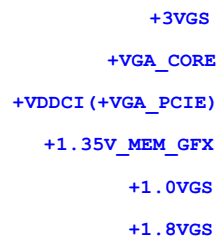
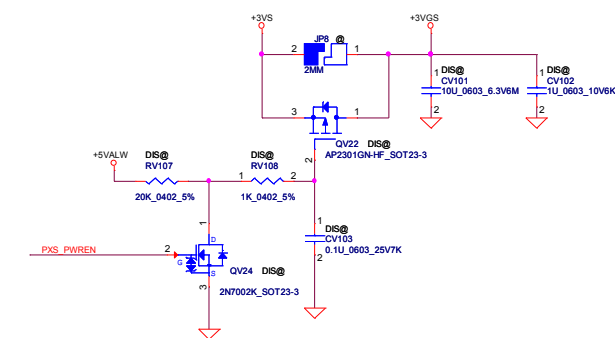
+1.8VS TO +1.8VGS



+1.35VS_VGA TO +1.35V_MEM_GFX

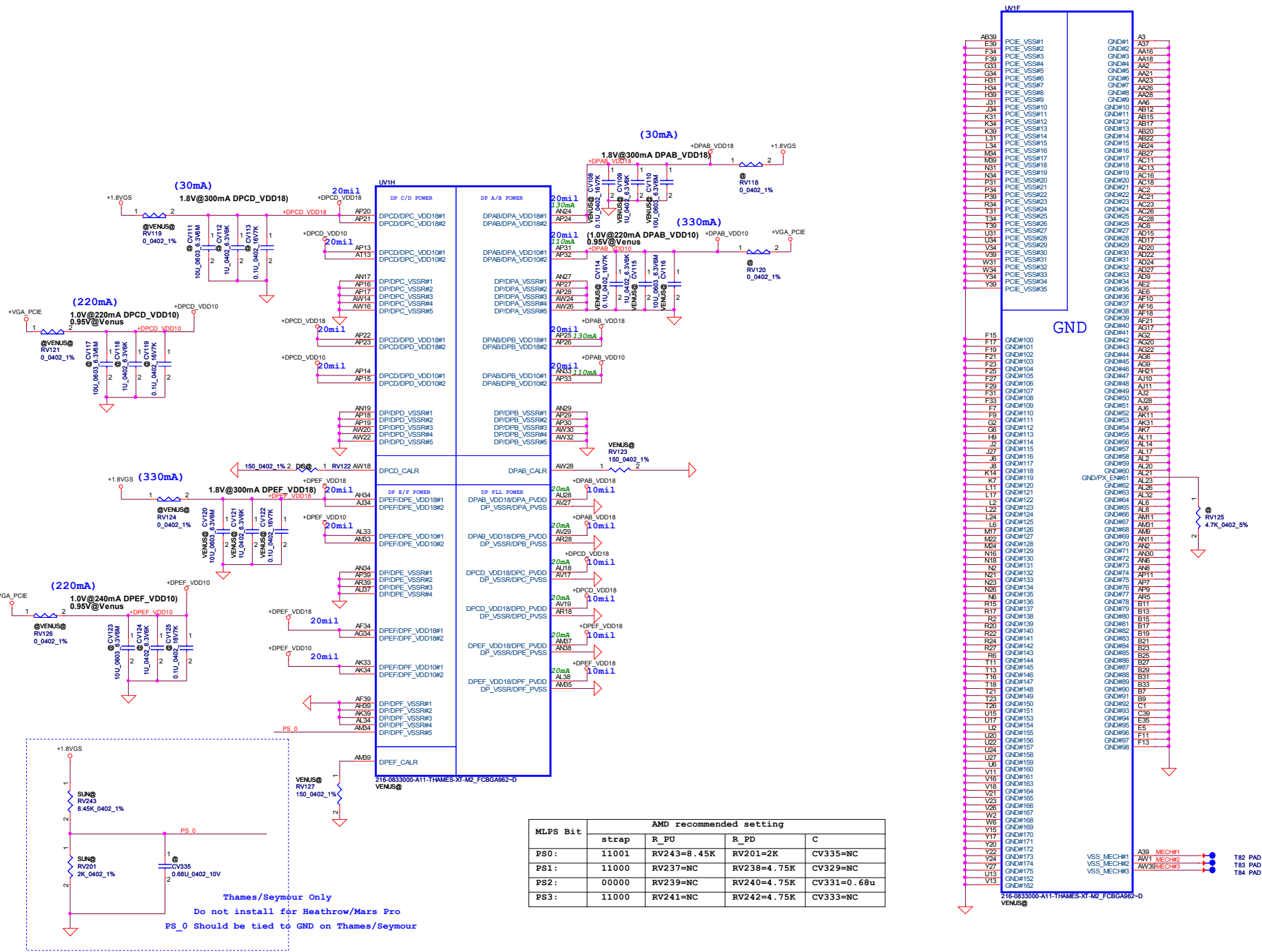


+3VS TO +3VGS



<20ms

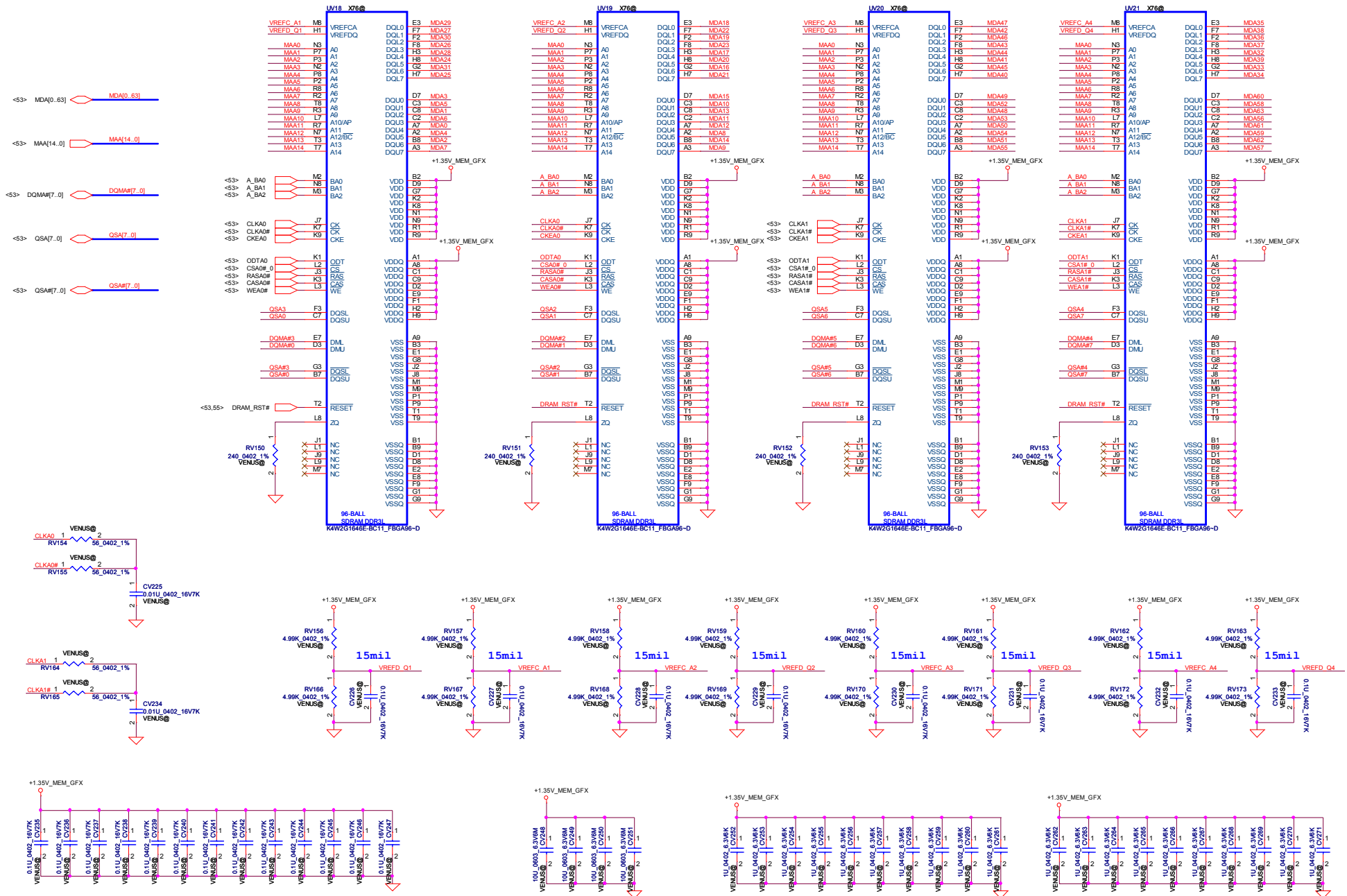
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MLPS Bit	AMD recommended setting			
	strap	R_PU	R_PD	C
PS0:	11001	RV243=8.45K	RV201=2K	CV335=NC
PS1:	11000	RV237=NC	RV238=4.75K	CV329=NC
PS2:	00000	RV239=NC	RV240=4.75K	CV331=0.68u
PS3:	11000	RV241=NC	RV242=4.75K	CV333=NC

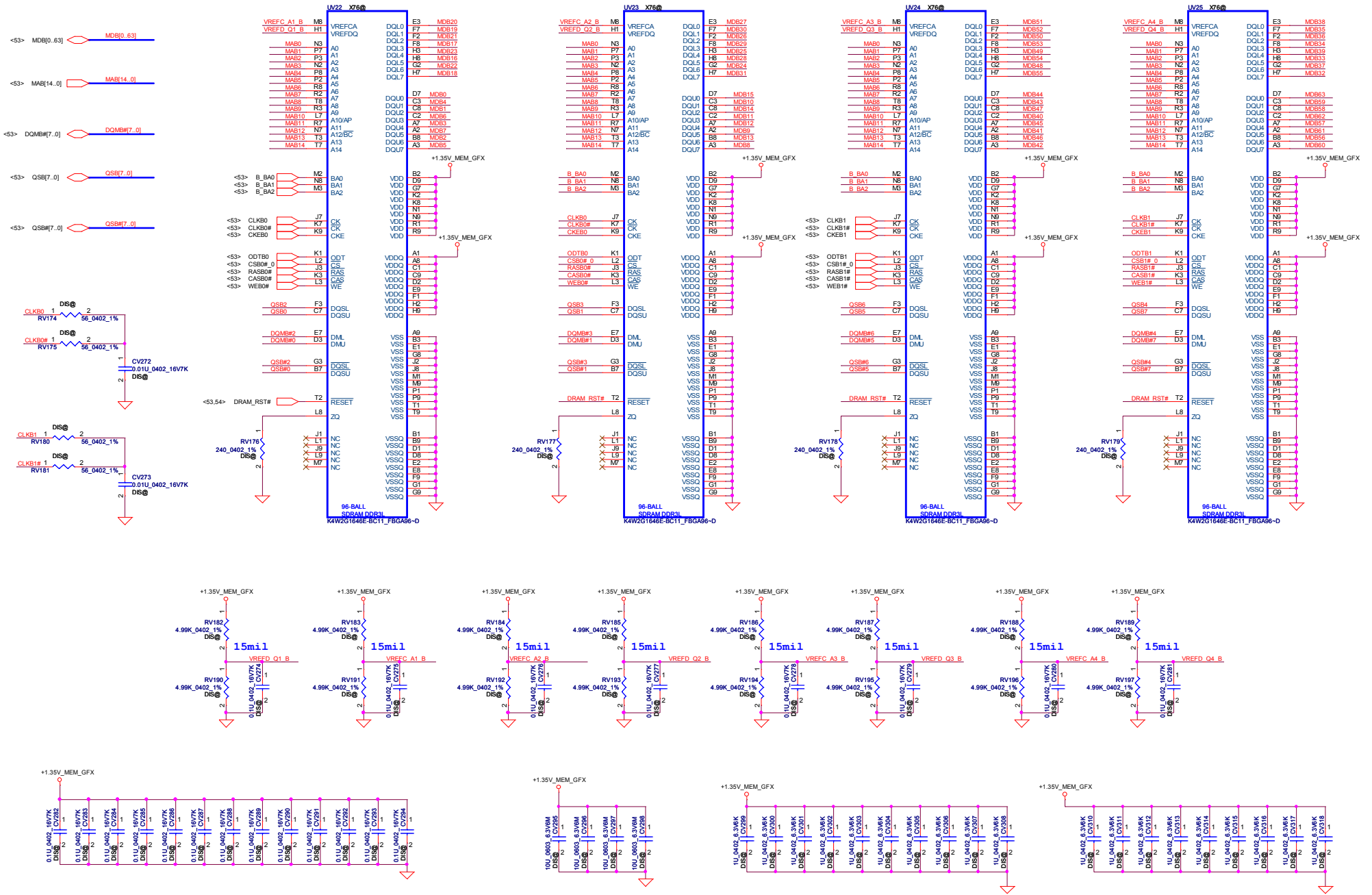
Thames/Seymour Only
Do not install for Heathrow/Mars Pro
PS_0 Should be tied to GND on Thames/Seymour

CHANNEL A: 256MB DDR3



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CHANNEL B: 256MB DDR3



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