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PCB

Compal Confidential

NDWG0 Schematics Document

AMD S1g3/ RS880M/ SB710

2009 / 09 / 22

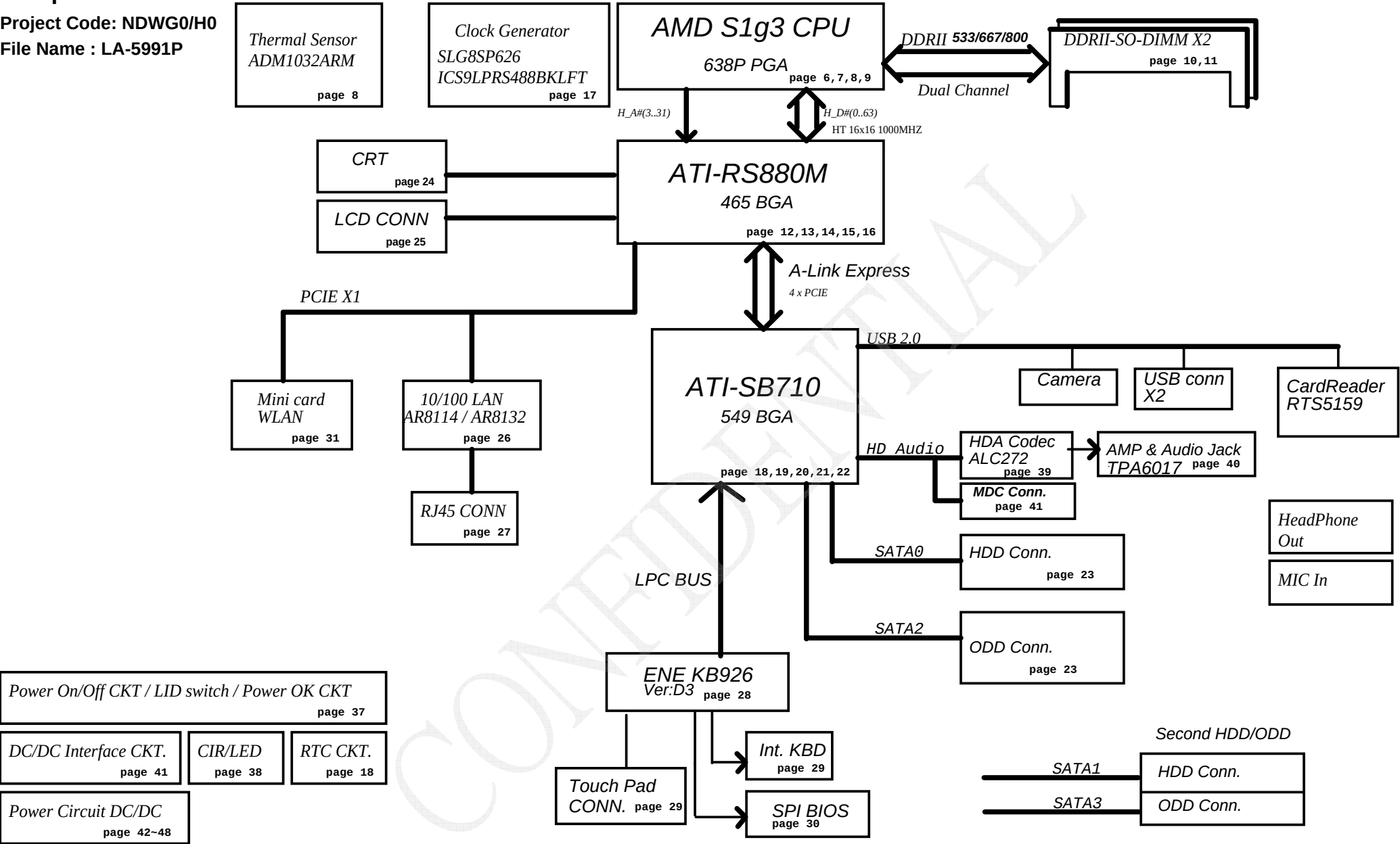
LA-5991P

Rev: 0.1

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Project Code: NDWG0/H0
File Name : LA-5991P



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VIN	Adapter power supply (19V)			
B+	AC or battery power rail for power circuit.			
+CPU_CORE	Core voltage for CPU			
+0.9V	0.9V switched power rail for DDR terminator			
+1.2V_HT	1.2V switched power rail	ON	OFF	
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON		ON*
+1.8VS	1.8V switched power rail		OFF	
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Device	IDSEL#	REQ#/GNT#	Interrupts
--------	--------	-----------	------------

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 100X b

Device	Address
ADM1032	1001 100X b

Device	Address	Device	Address
Clock Generator	1101 001Xb	New Card	
DDR DIMM0	1001 000Xb		
DDR DIMM2	1001 010Xb		
Wireless Lan			

Device	Address
New Card	

SIGNAL STATE	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

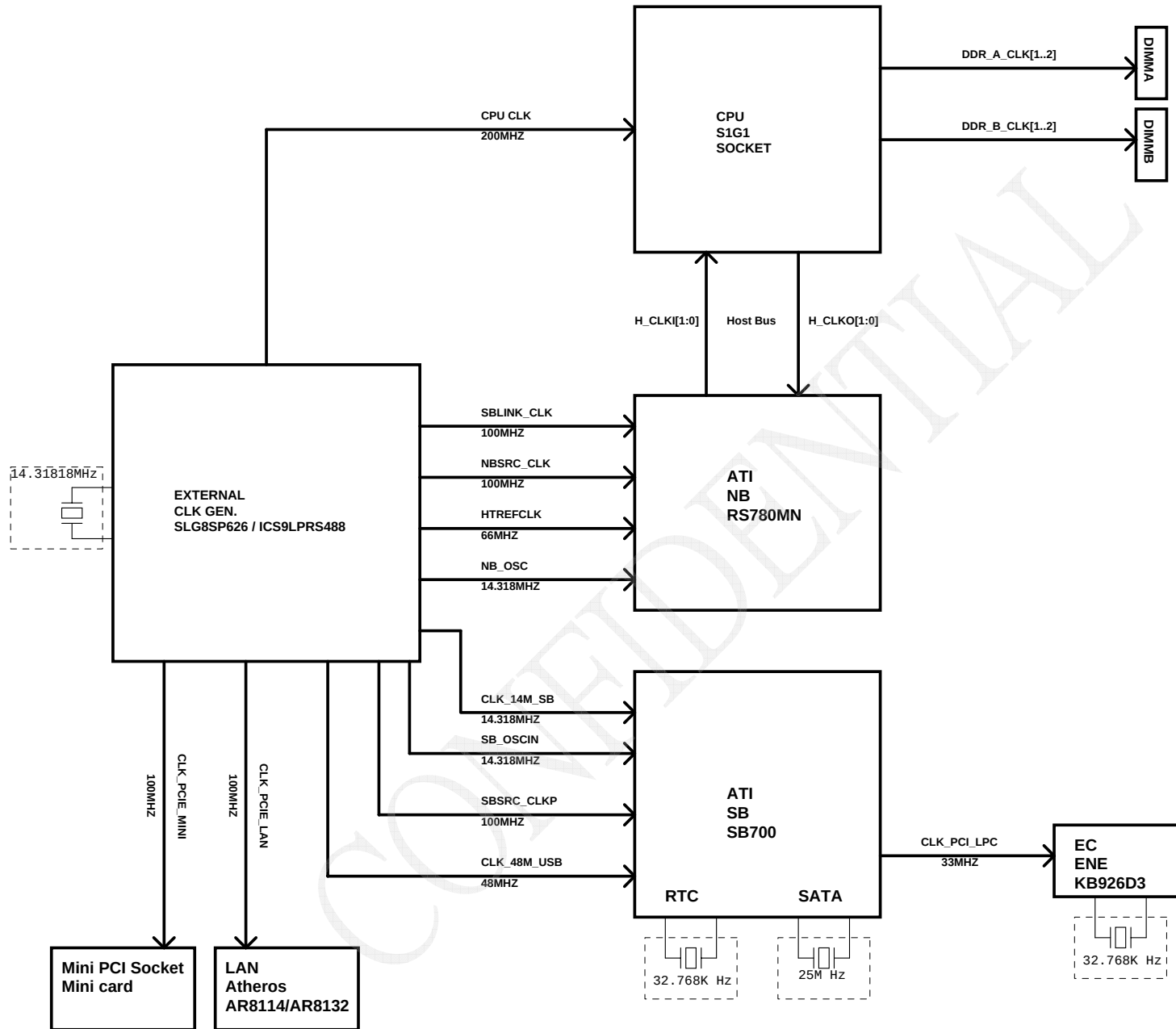
Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

Board ID	PCB Revision
0	No Support VaryBright
1	
2	
3	Support VaryBright
4	
5	
6	
7	

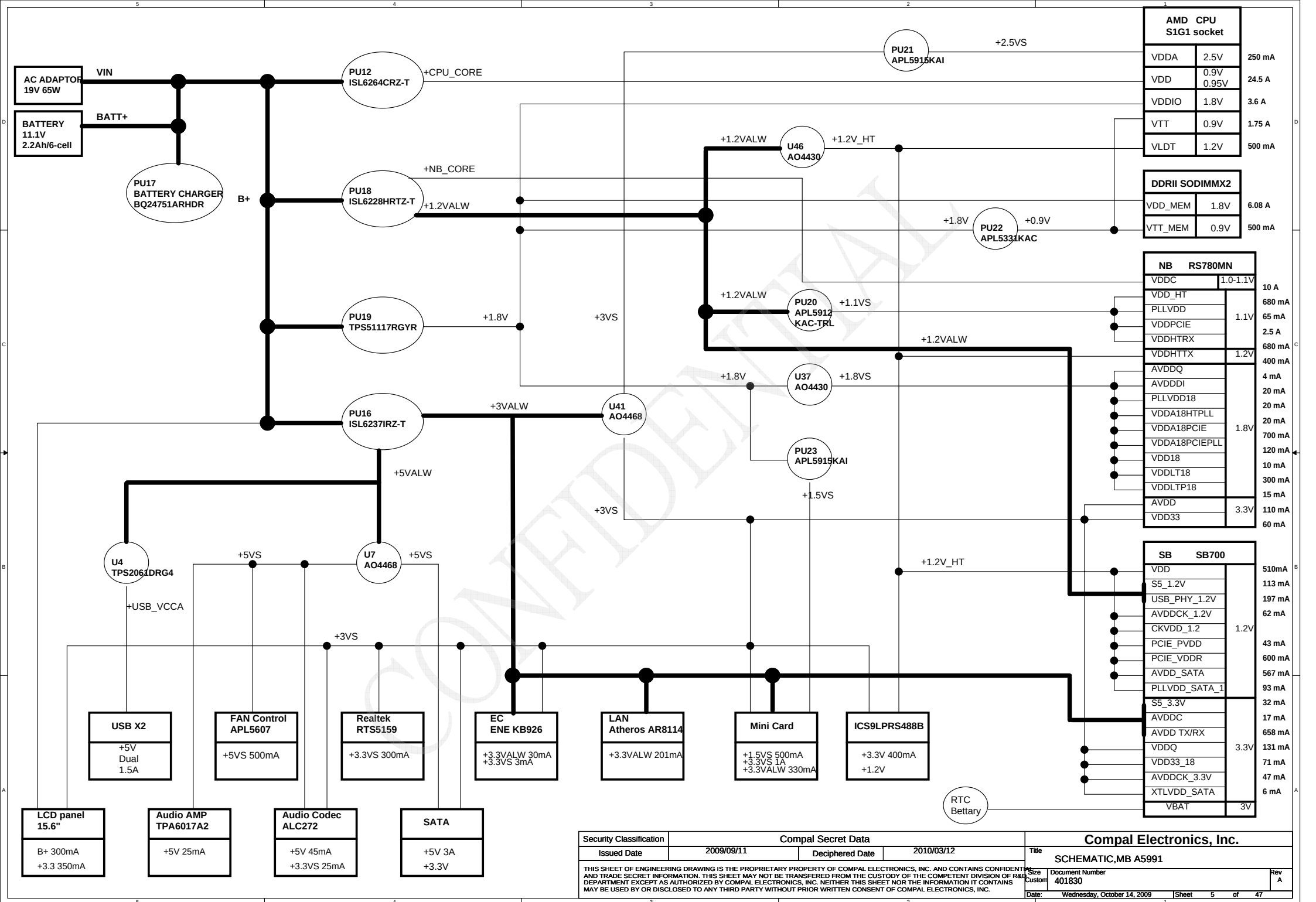
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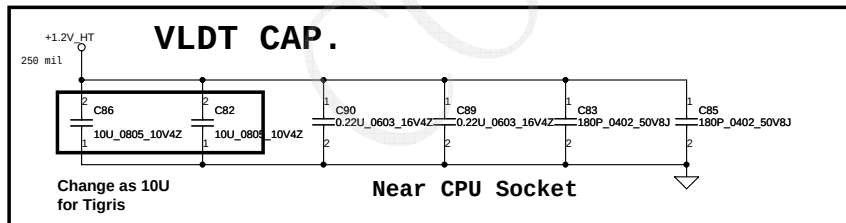
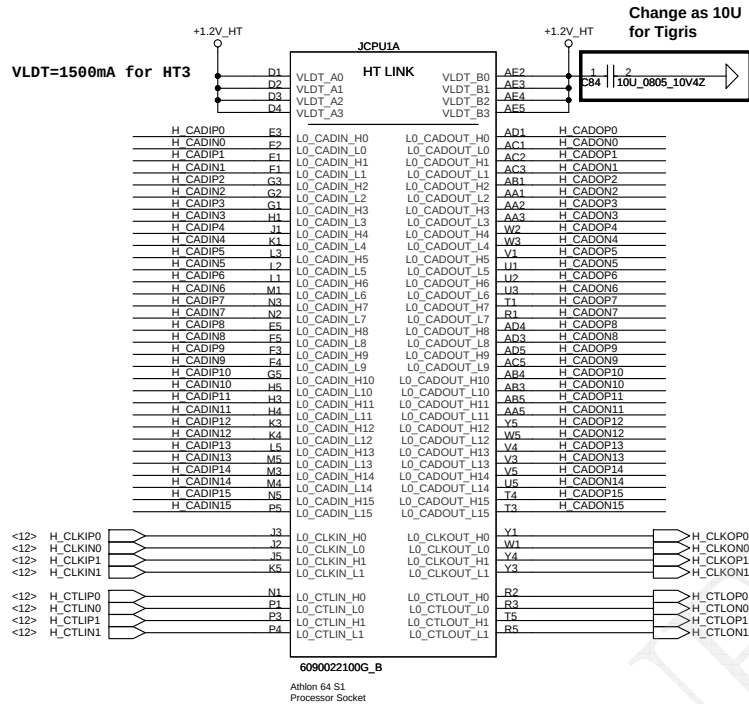
SKU ID	SKU
0	NCWG0
1	
2	
3	NAL00
4	
5	
6	
7	NCWH0

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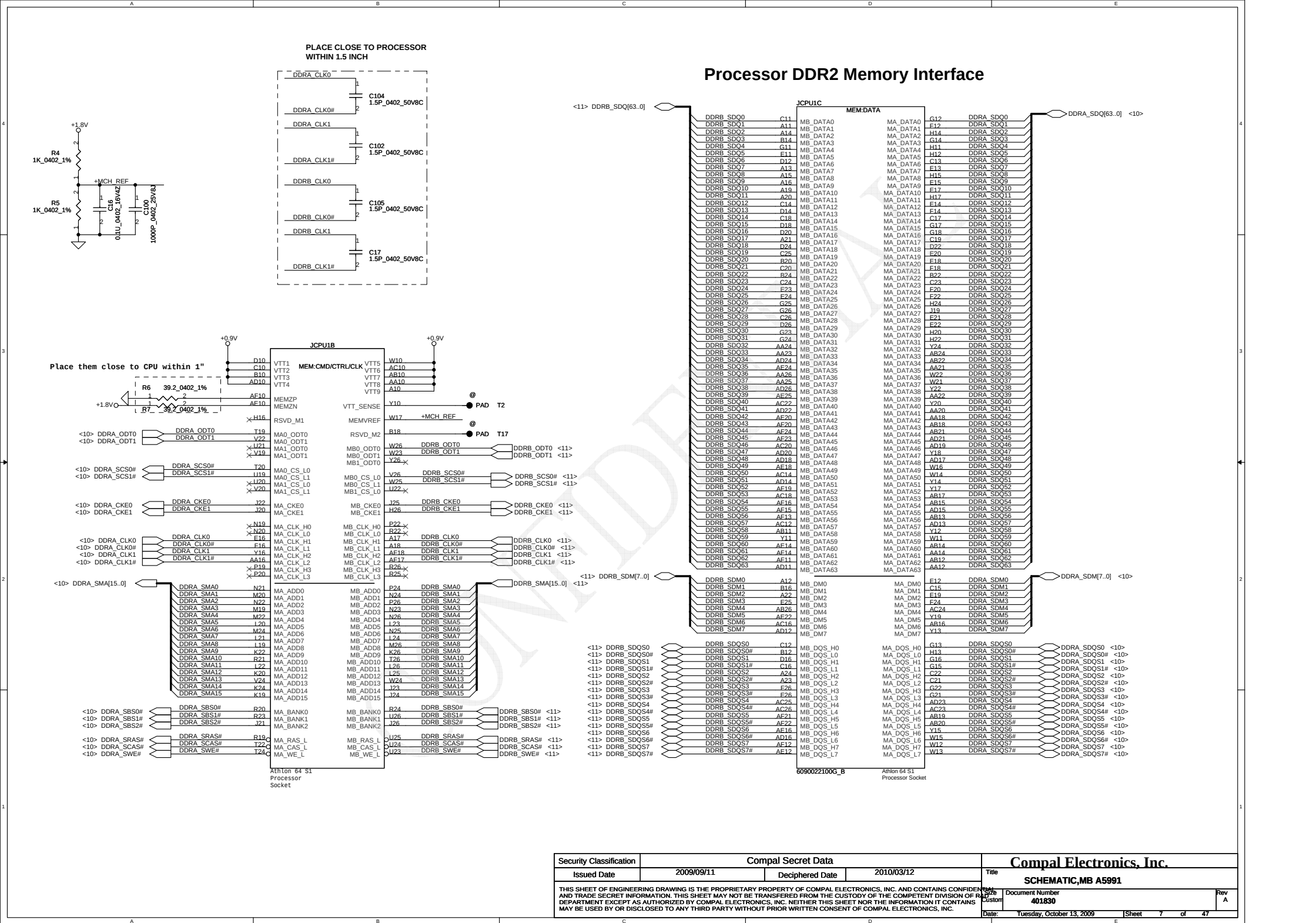


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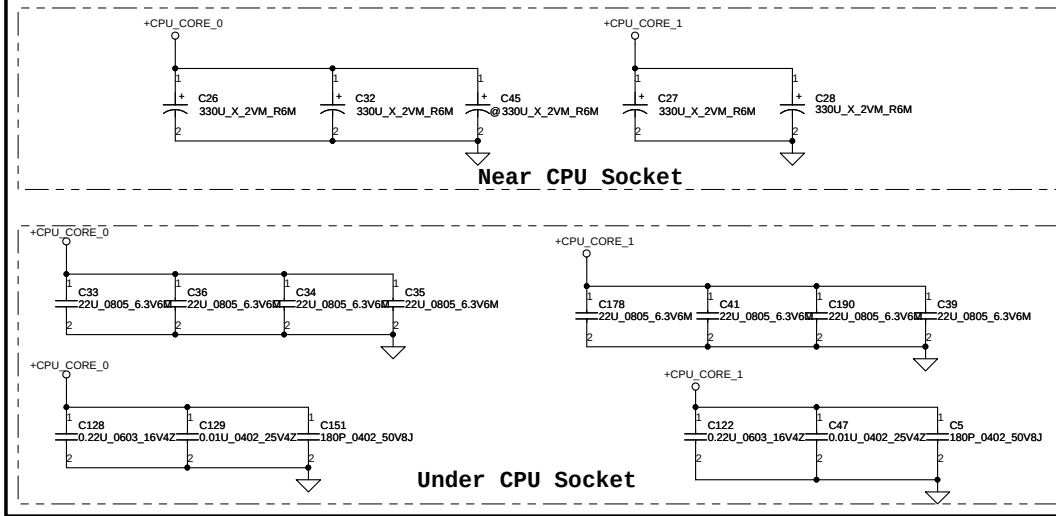
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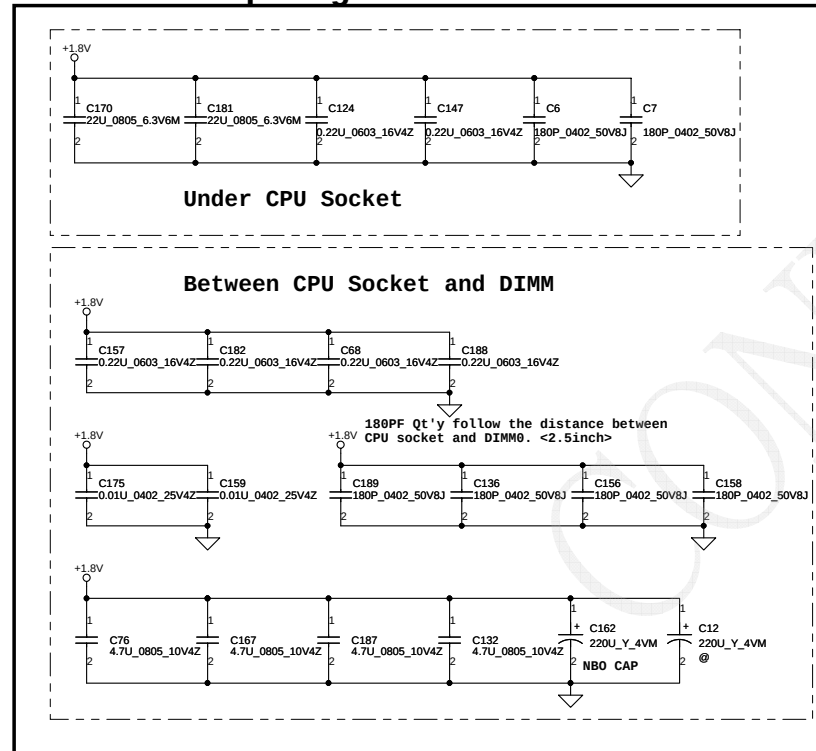
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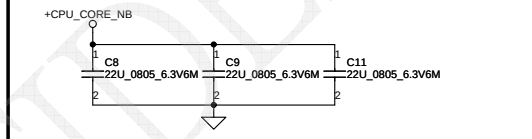
VDD(+CPU_CORE) decoupling.



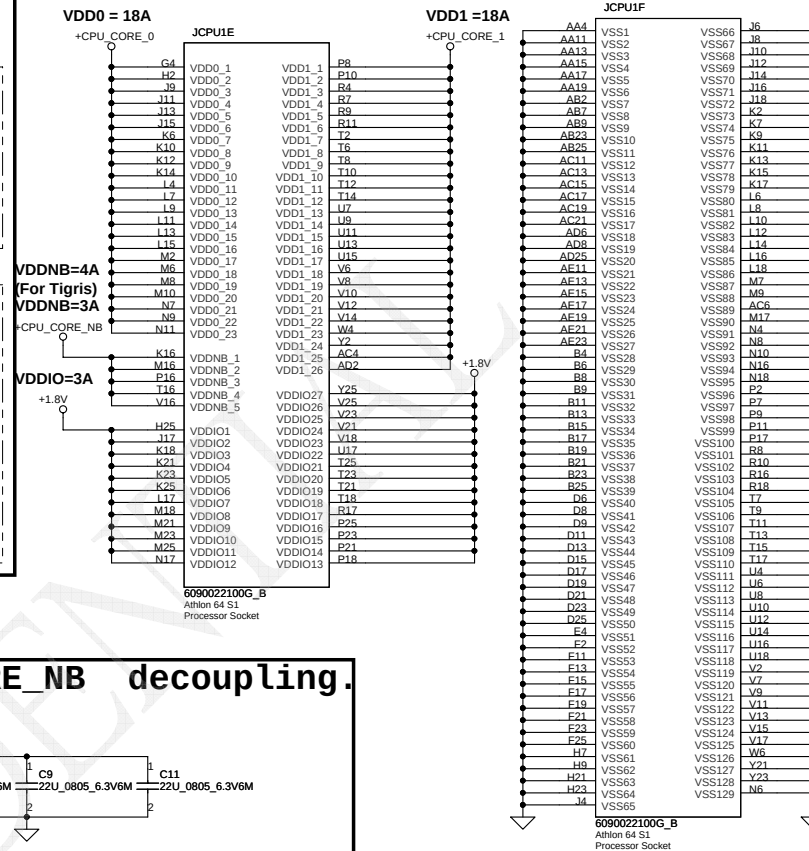
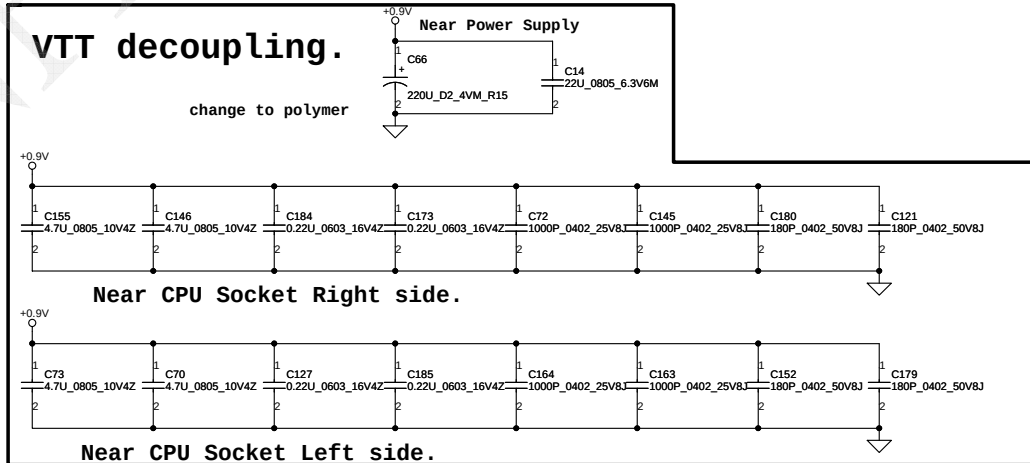
VDDIO decoupling.



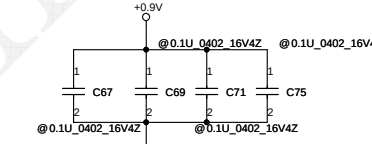
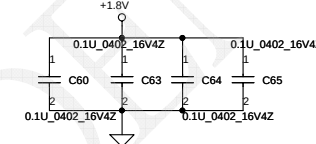
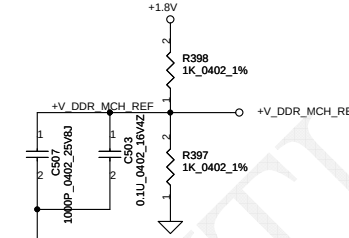
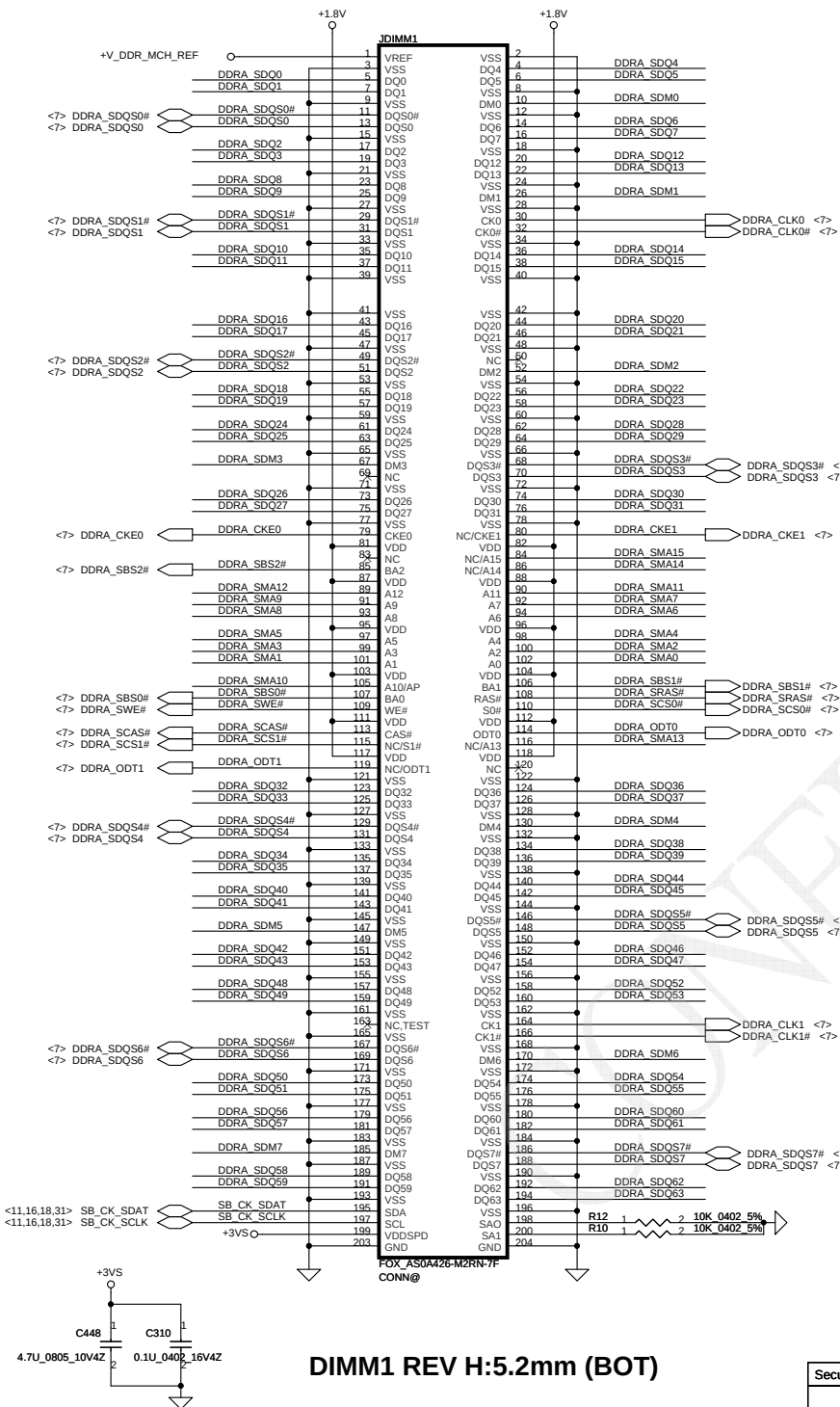
+CPU_CORE_NB decoupling.



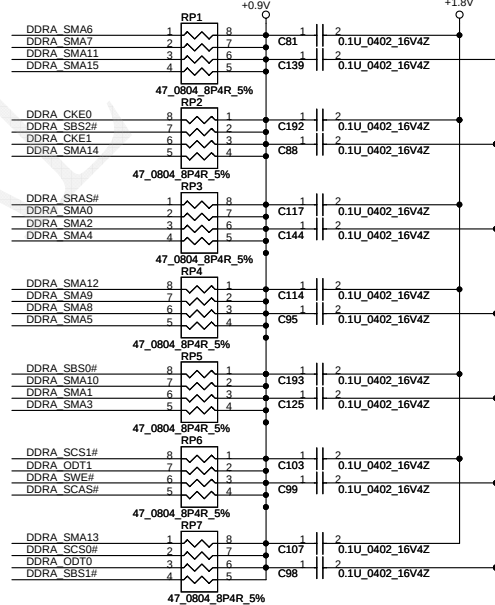
VTT decoupling.



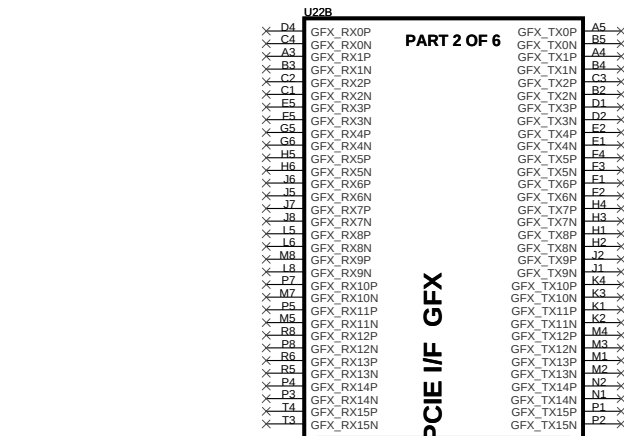
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RESERVE +V_DDR_MCH_REF BUFFER CIRCUIT

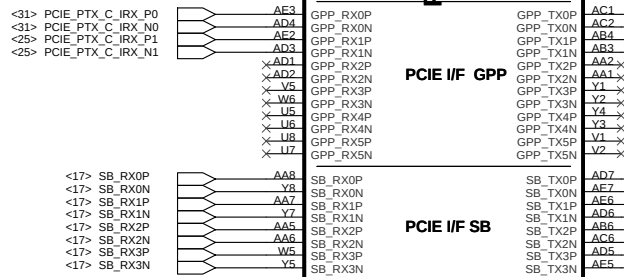


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Check SW Routing

AN_RS780MN1. Only suggest pair0-3 can
usage for power save.



RS780M_FCBGA528

RS780MN-SA00002DR30 Ver:A13

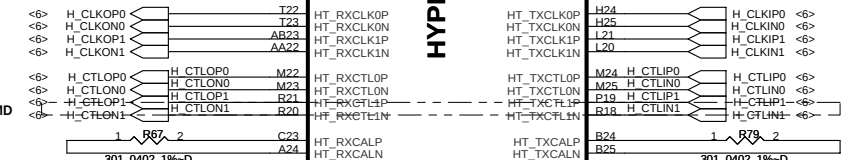
RS780M Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

HT Link

When tune trace length, must
keep 1:4 on self-trace

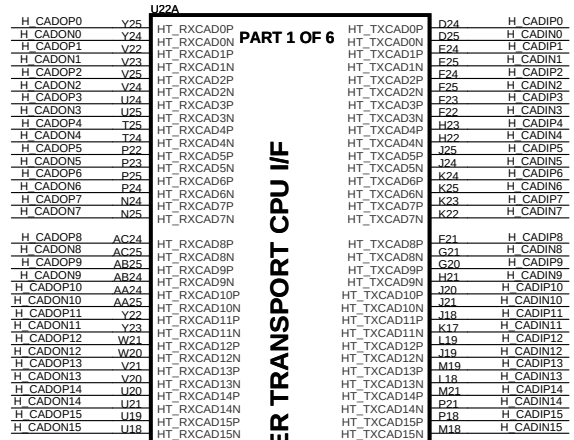
Check AMD



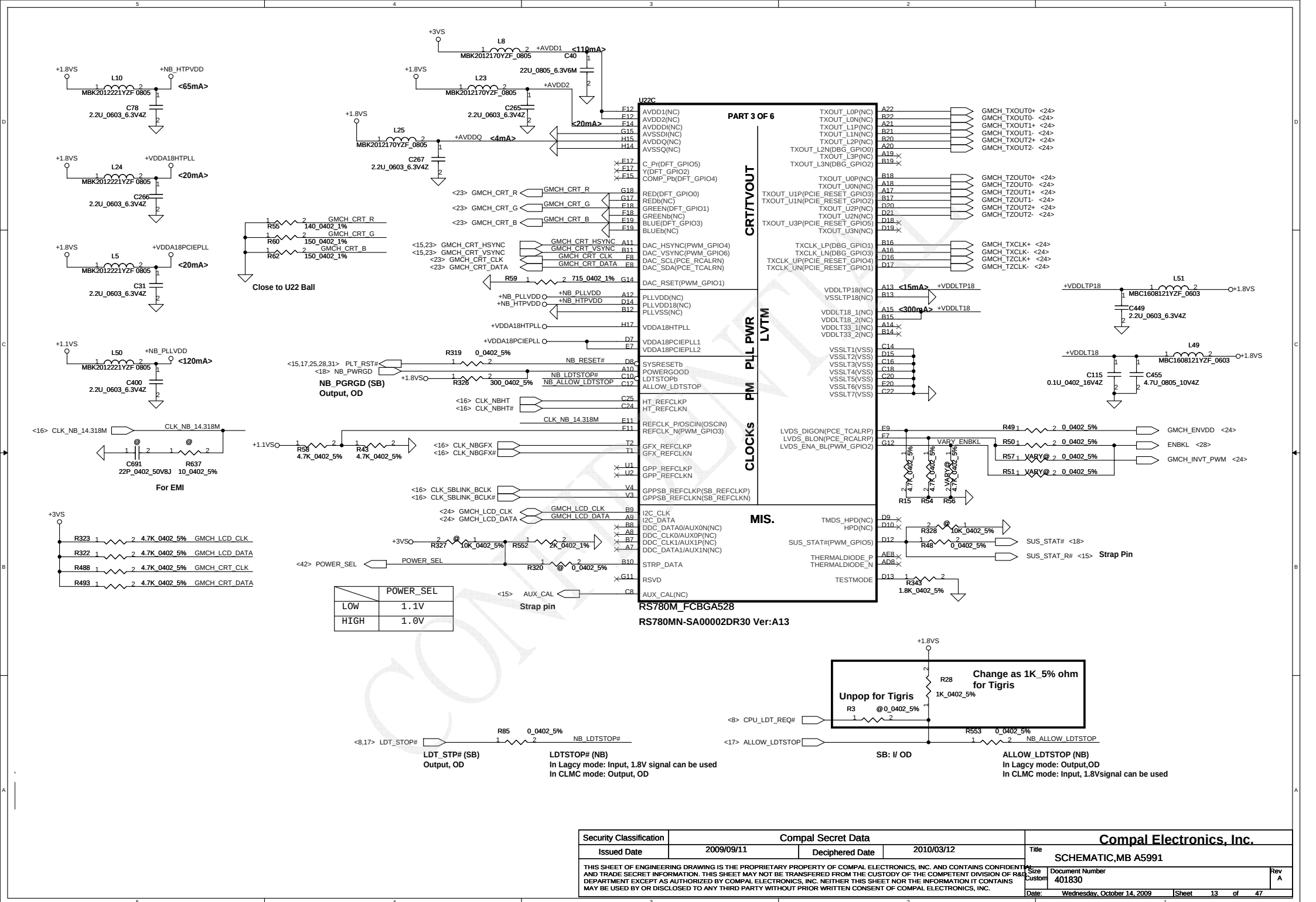
Place within 1"
layout 4/8

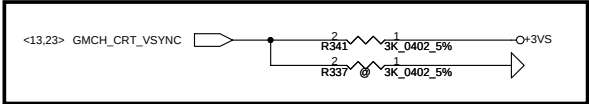
RS780M_FCBGA528
RS780MN-SA00002DR30 Ver:A13

Place within 1"
layout 4/8



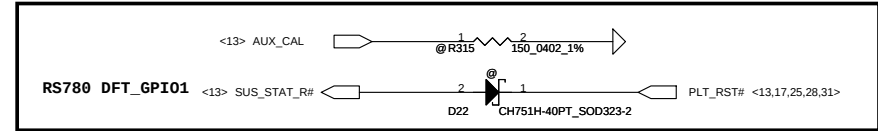
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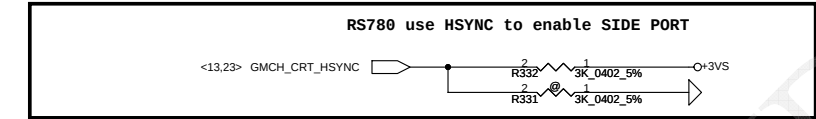
DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLED

Enables the Test Debug Bus using GPIO. (VSYNC)
1 : Disable (RS780)
0 : Enable (Rs780)



DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
RS740/RX780: DFT_GPIO1 RS780:SUS_STAT



RS780 use HSYNC to enable SIDE PORT

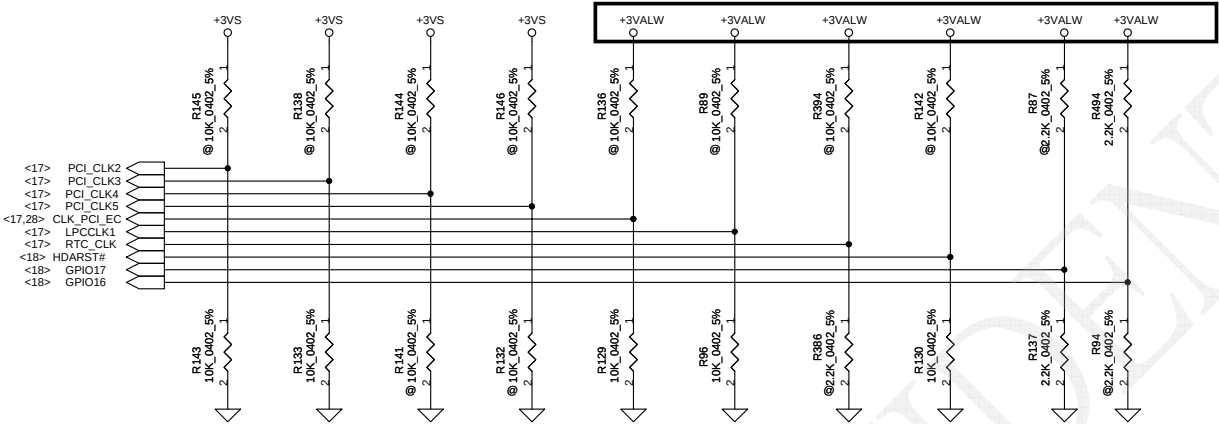
RS740/RS780: Enables Side port memory (RS780 use HSYNC#)
0. Enable (RS780)
1 : Disable(RS780)

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REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0 CLK_PCI_EC	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM	
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT		L,H = LPC ROM (Default L,NC) L,L = FWH ROM

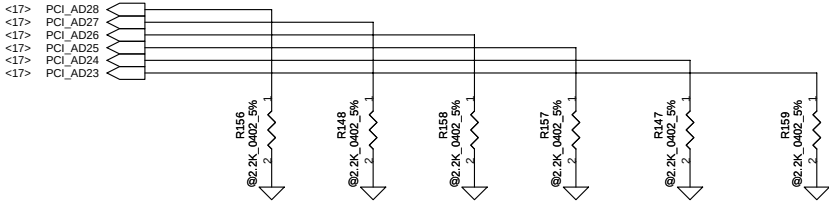


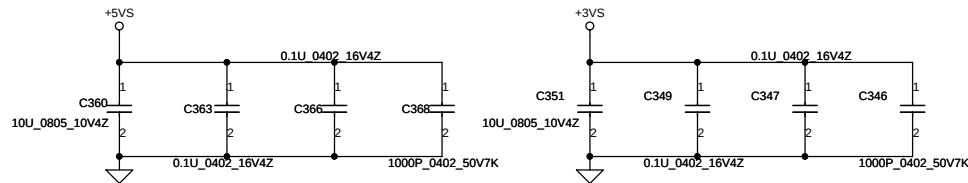
DEBUG STRAPS

DEBUG STRAPS

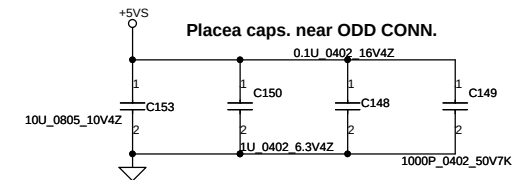
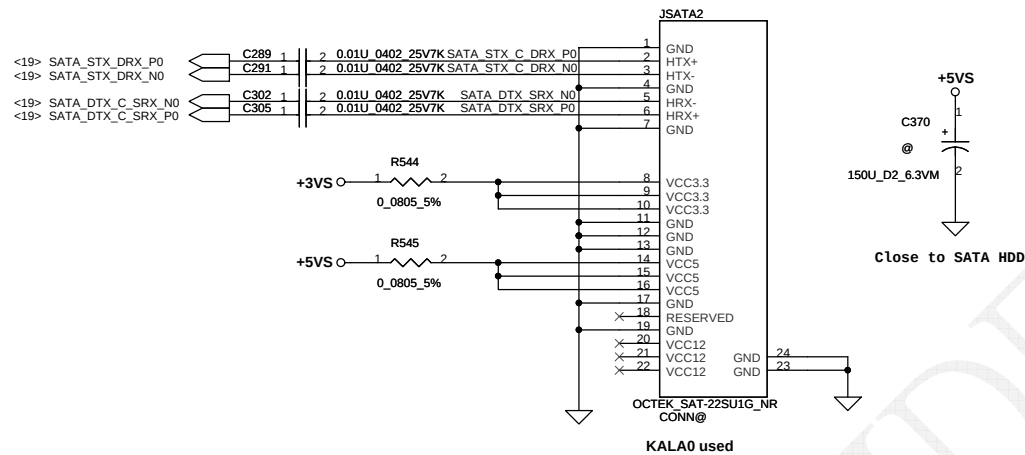
SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

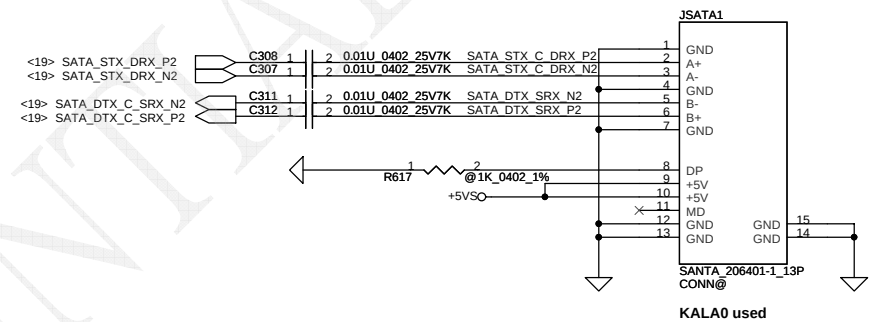




SATA HDD CONN

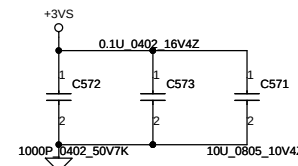
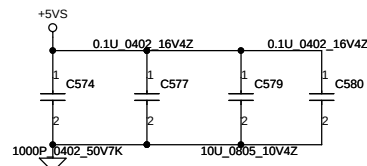
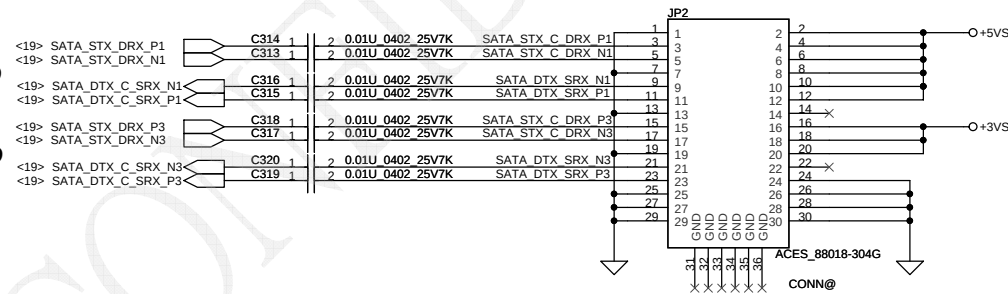


SATA ODD CONN



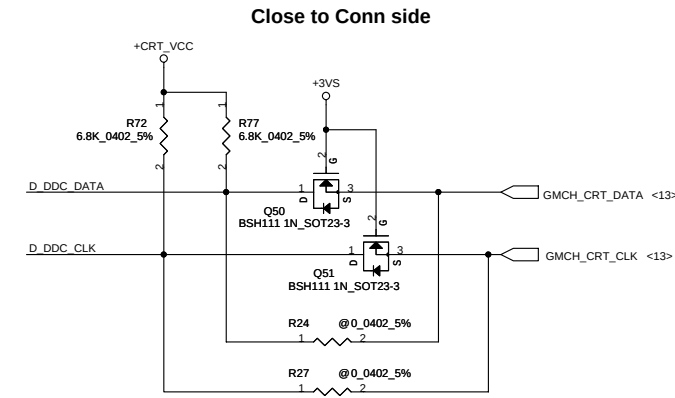
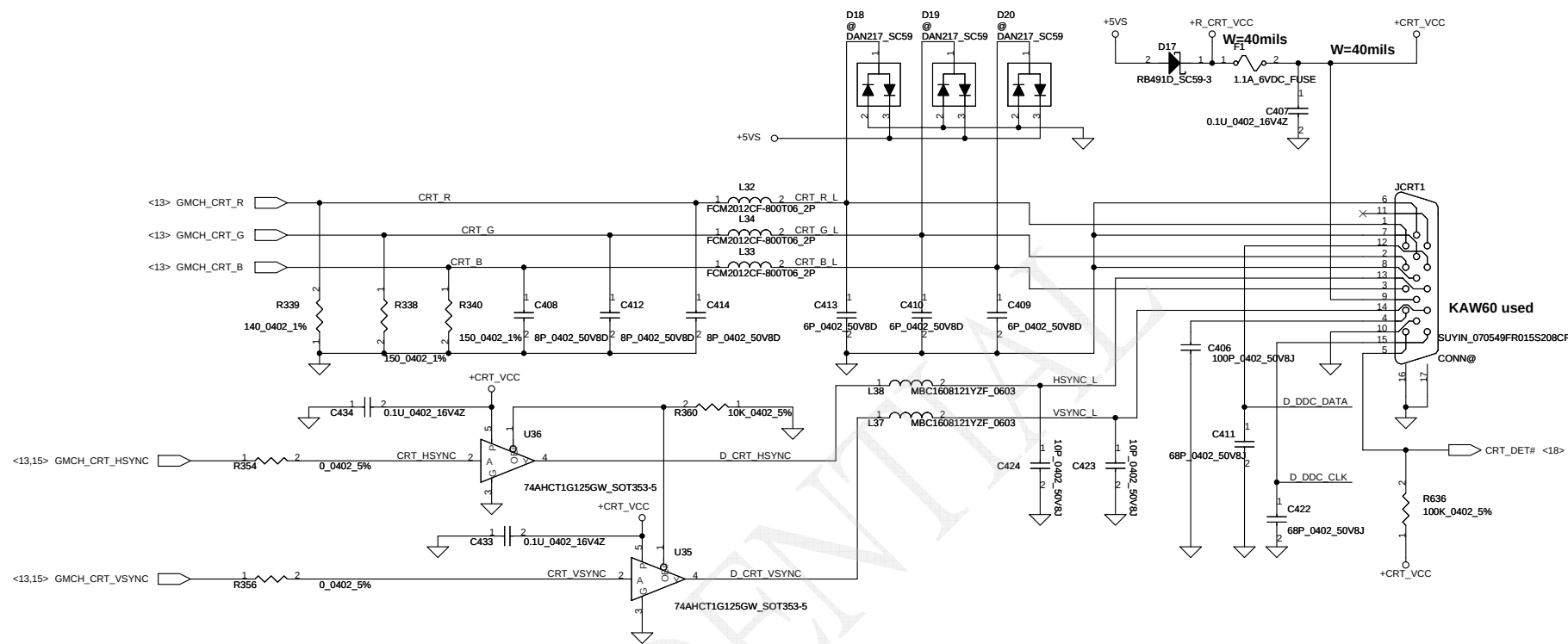
Second HDD

Second ODD

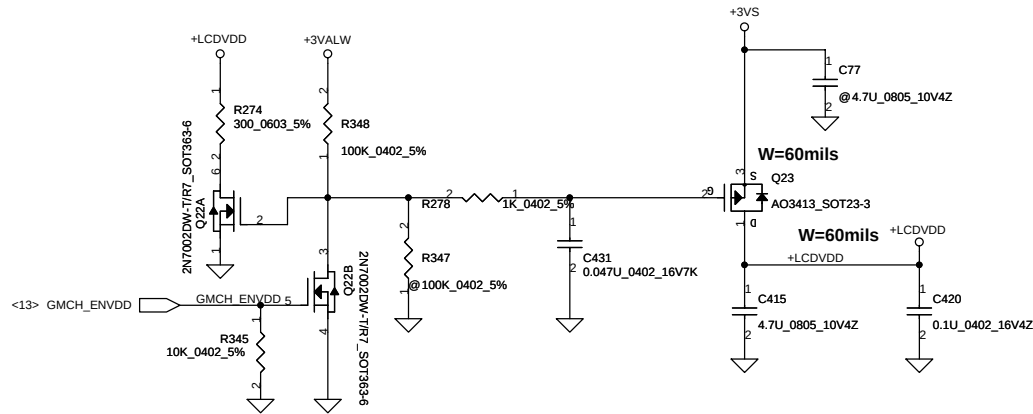


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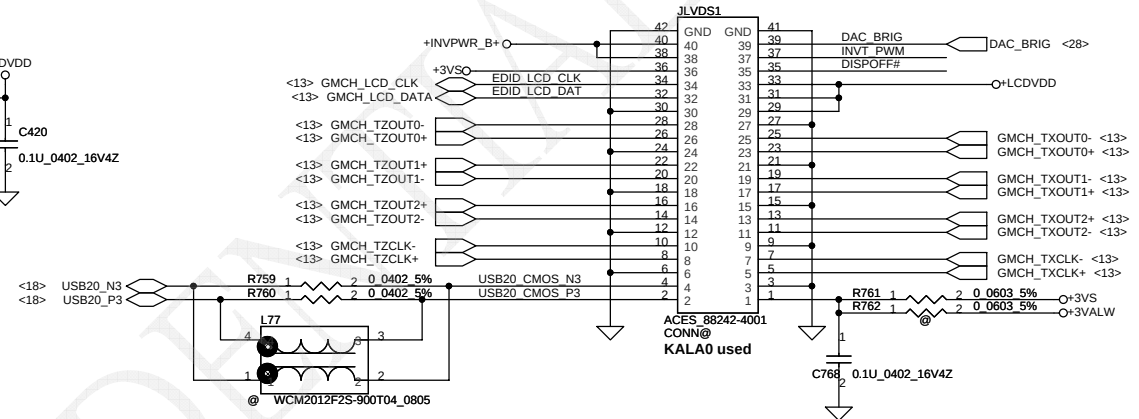
CRT Connector



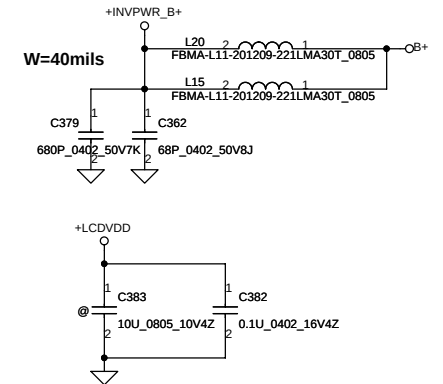
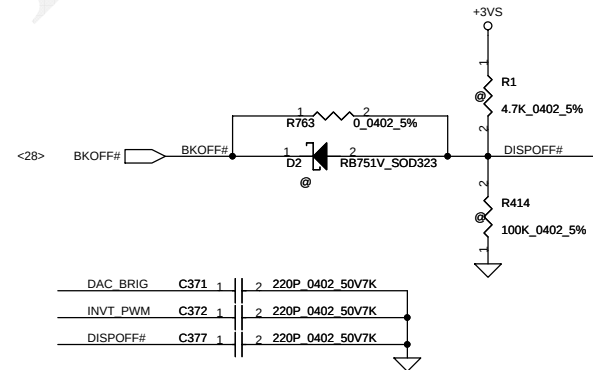
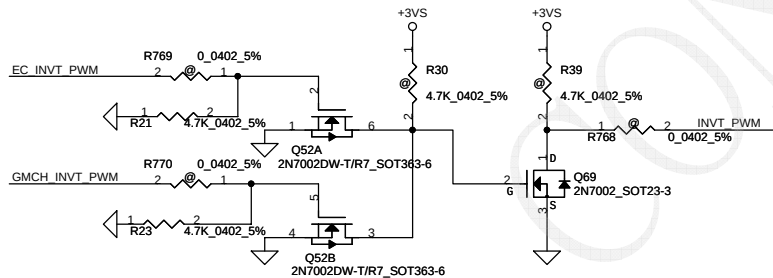
LCD POWER CIRCUIT



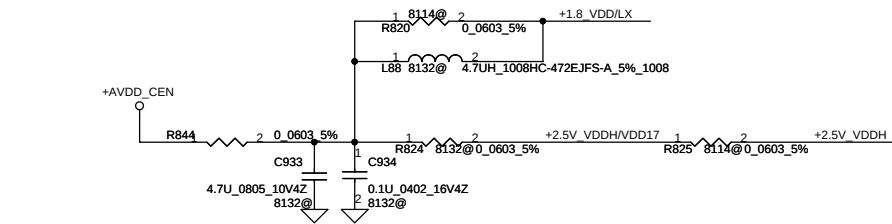
LCD/PANEL CONN.



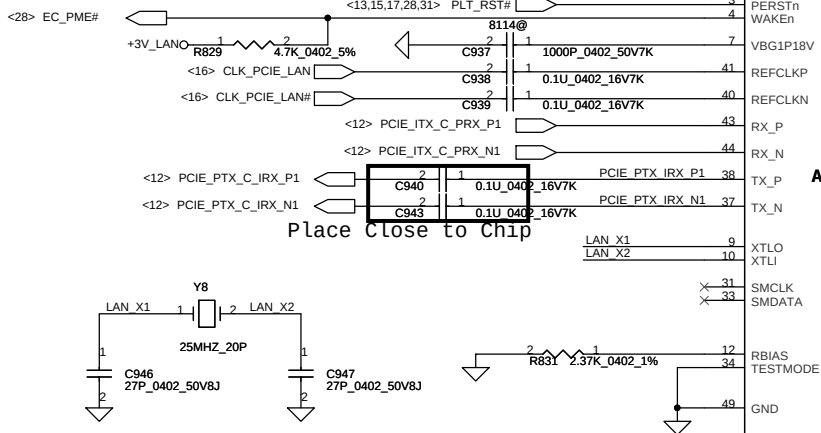
VARYBRIGHT FUNCTION



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WAKEn
8114: Internal PU
8132: OD



Place Close to Chip

U85

VDD180

VDD33

VDDHO

CTR12

PERSTn

WAKEn

VBG1P18V

REFCLKP

REFCLKN

RX_P

RX_N

TX_P

TX_N

LAN_X1

LAN_X2

SMCLK

SMDATA

RBIAS

TESTMODE

GND

AVDDL0

AVDDL1

AVDDL2

AVDDL3

AVDDL4

AVDDH0

AVDDH1

AVDDH2

NC_0

NC_1

NC_2

NC_3

NC_4

NC_5

AVDDVCO1

AVDDVCO2

AVDDVCO3

AVDDVCO4

AVDDVCO5

AVDDVCO6

AVDDVCO7

AVDDVCO8

AVDDVCO9

AVDDVCO10

AVDDVCO11

AVDDVCO12

AVDDVCO13

AVDDVCO14

AVDDVCO15

AVDDVCO16

AVDDVCO17

AVDDVCO18

AVDDVCO19

AVDDVCO20

AVDDVCO21

AVDDVCO22

AVDDVCO23

AVDDVCO24

AVDDVCO25

AVDDVCO26

AVDDVCO27

AVDDVCO28

AVDDVCO29

AVDDVCO30

AVDDVCO31

AVDDVCO32

AVDDVCO33

AVDDVCO34

AVDDVCO35

AVDDVCO36

AVDDVCO37

AVDDVCO38

AVDDVCO39

AVDDVCO40

AVDDVCO41

AVDDVCO42

AVDDVCO43

AVDDVCO44

AVDDVCO45

AVDDVCO46

AVDDVCO47

AVDDVCO48

AVDDVCO49

AVDDVCO50

AVDDVCO51

AVDDVCO52

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AVDDVCO61

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AVDDVCO67

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AVDDVCO69

AVDDVCO70

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AVDDVCO72

AVDDVCO73

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AVDDVCO93

AVDDVCO94

AVDDVCO95

AVDDVCO96

AVDDVCO97

AVDDVCO98

AVDDVCO99

AVDDVCO100

AVDDVCO101

AVDDVCO102

AVDDVCO103

AVDDVCO104

AVDDVCO105

AVDDVCO106

AVDDVCO107

AVDDVCO108

AVDDVCO109

AVDDVCO110

AVDDVCO111

AVDDVCO112

AVDDVCO113

AVDDVCO114

AVDDVCO115

AVDDVCO116

AVDDVCO117

AVDDVCO118

AVDDVCO119

AVDDVCO120

AVDDVCO121

AVDDVCO122

AVDDVCO123

AVDDVCO124

AVDDVCO125

AVDDVCO126

AVDDVCO127

AVDDVCO128

AVDDVCO129

AVDDVCO130

AVDDVCO131

AVDDVCO132

AVDDVCO133

AVDDVCO134

AVDDVCO135

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AVDDVCO137

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AVDDVCO146

AVDDVCO147

AVDDVCO148

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AVDDVCO150

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AVDDVCO152

AVDDVCO153

AVDDVCO154

AVDDVCO155

AVDDVCO156

AVDDVCO157

AVDDVCO158

AVDDVCO159

AVDDVCO160

AVDDVCO161

AVDDVCO162

AVDDVCO163

AVDDVCO164

AVDDVCO165

AVDDVCO166

AVDDVCO167

AVDDVCO168

AVDDVCO169

AVDDVCO170

AVDDVCO171

AVDDVCO172

AVDDVCO173

AVDDVCO174

AVDDVCO175

AVDDVCO176

AVDDVCO177

AVDDVCO178

AVDDVCO179

AVDDVCO180

AVDDVCO181

AVDDVCO182

AVDDVCO183

AVDDVCO184

AVDDVCO185

AVDDVCO186

AVDDVCO187

AVDDVCO188

AVDDVCO189

AVDDVCO190

AVDDVCO191

AVDDVCO192

AVDDVCO193

AVDDVCO194

AVDDVCO195

AVDDVCO196

AVDDVCO197

AVDDVCO198

AVDDVCO199

AVDDVCO200

AVDDVCO201

AVDDVCO202

AVDDVCO203

AVDDVCO204

AVDDVCO205

AVDDVCO206

AVDDVCO207

AVDDVCO208

AVDDVCO209

AVDDVCO210

AVDDVCO211

AVDDVCO212

AVDDVCO213

AVDDVCO214

AVDDVCO215

AVDDVCO216

AVDDVCO217

AVDDVCO218

AVDDVCO219

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AVDDVCO224

AVDDVCO225

AVDDVCO226

AVDDVCO227

AVDDVCO228

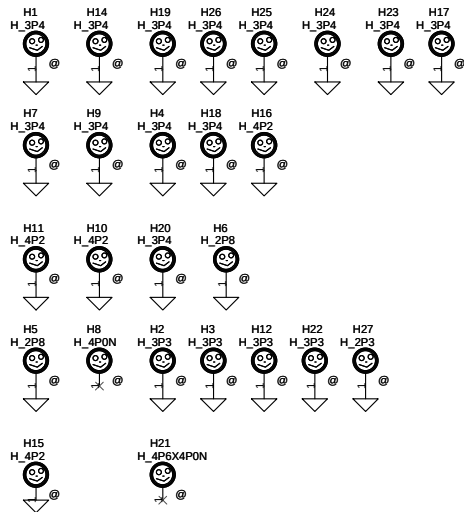
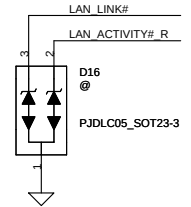
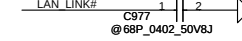
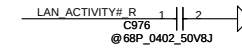
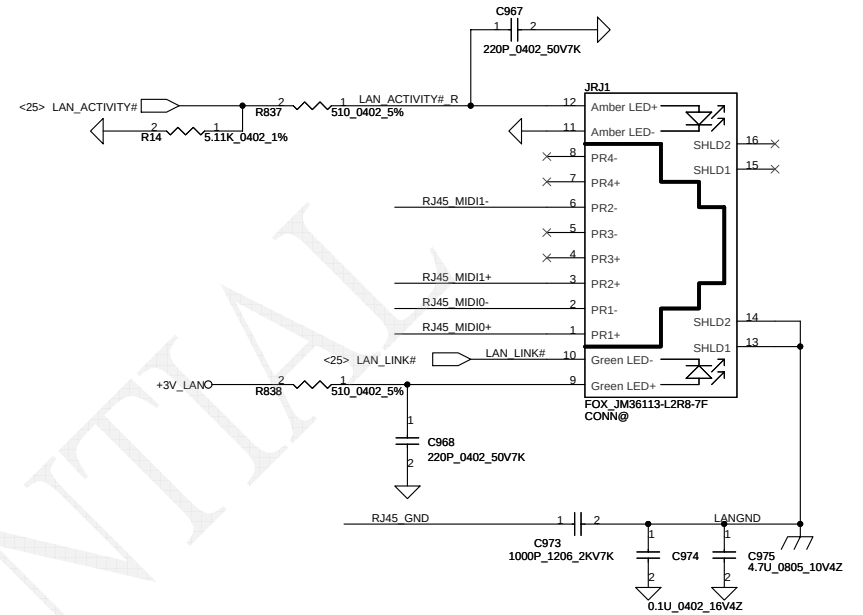
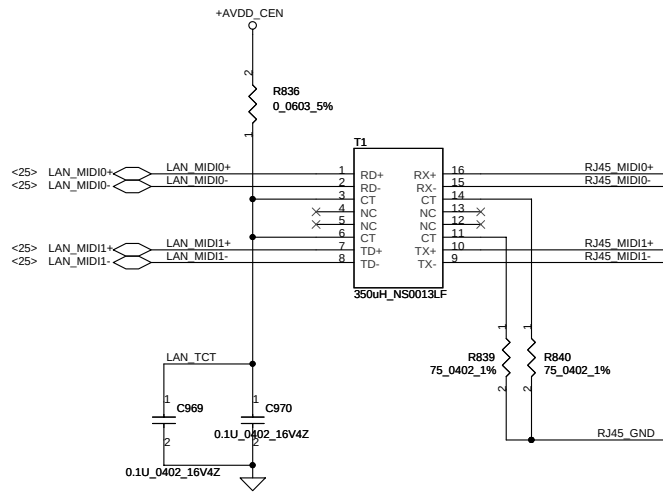
AVDDVCO229

AVDDVCO230

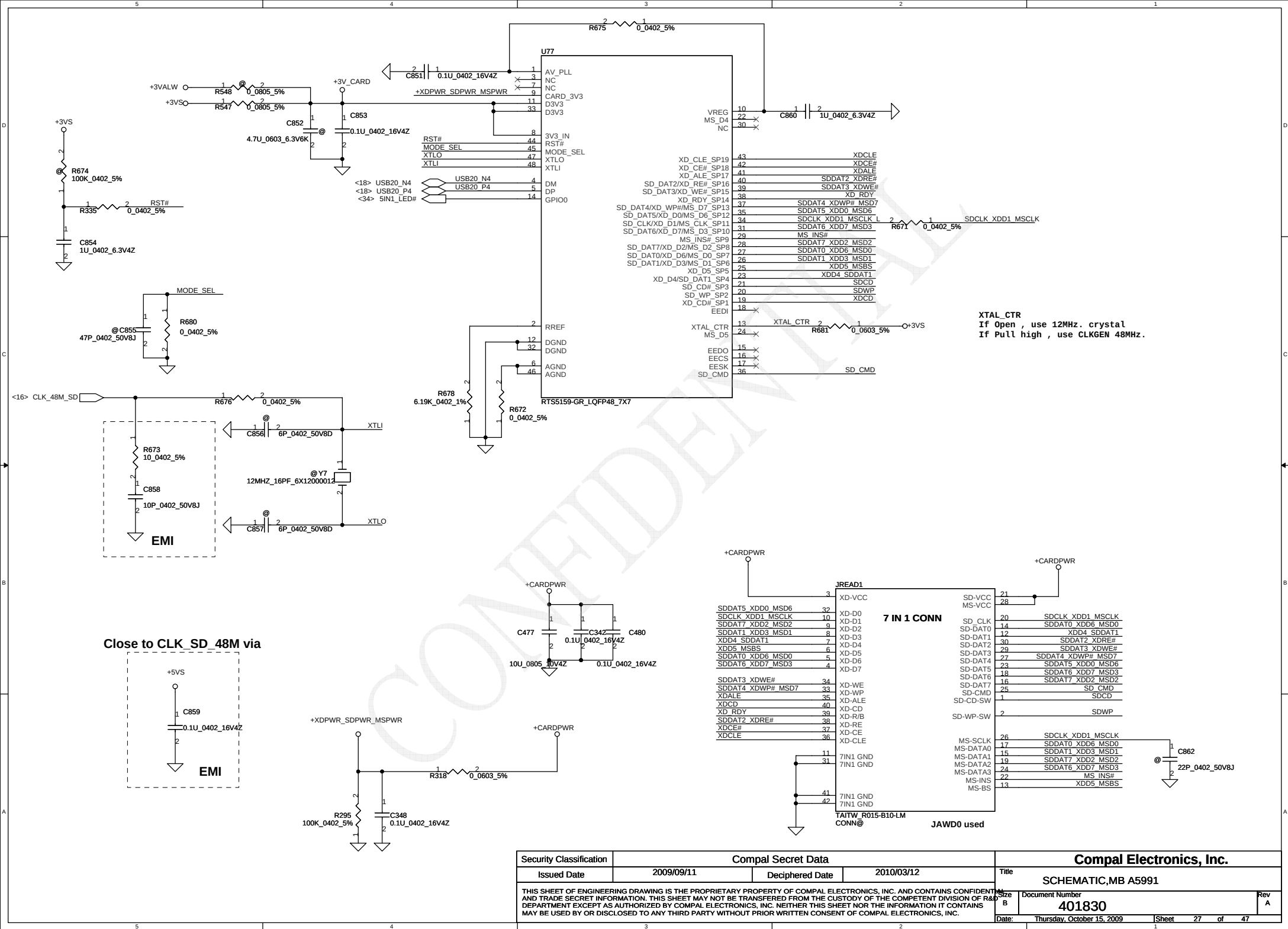
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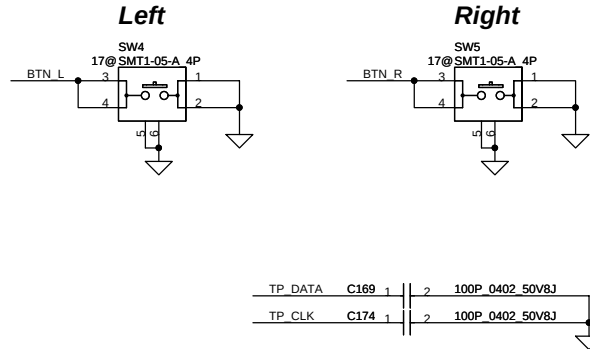
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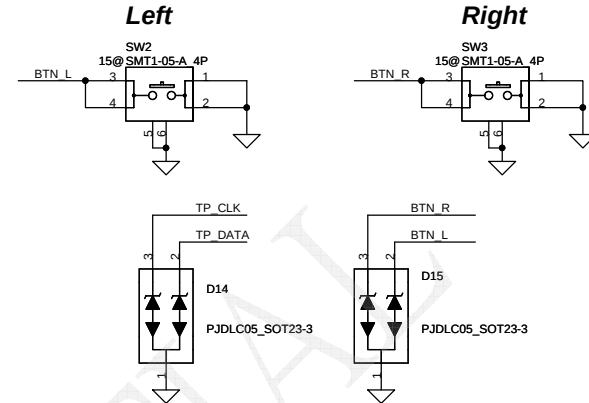
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For 17"

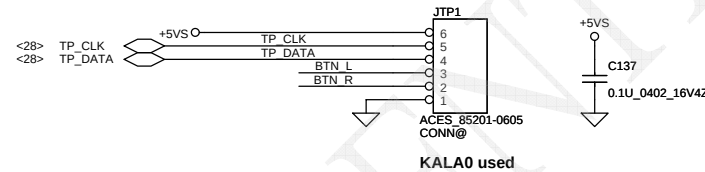


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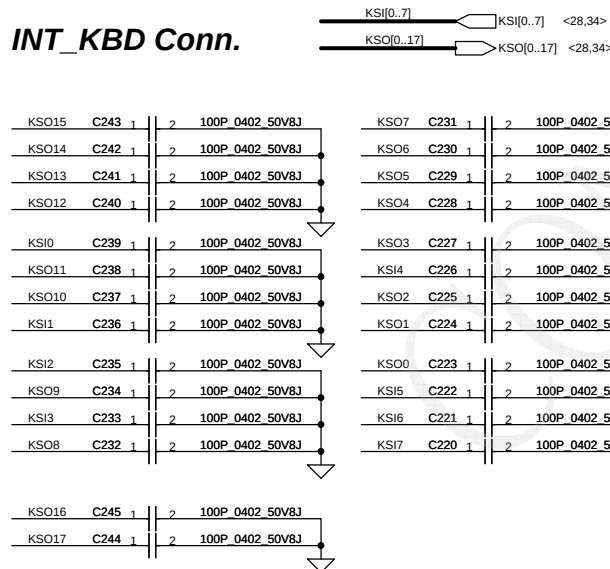


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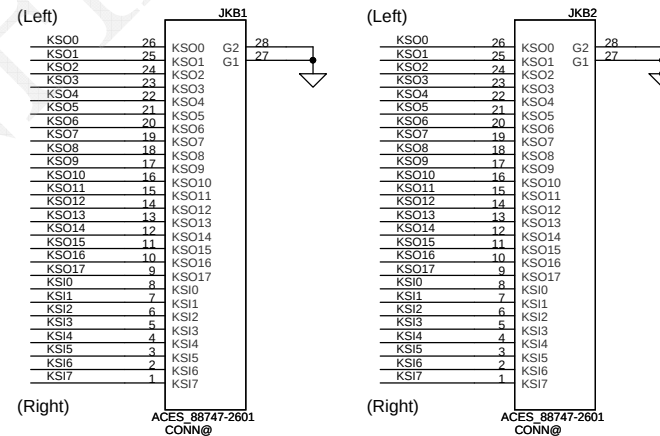
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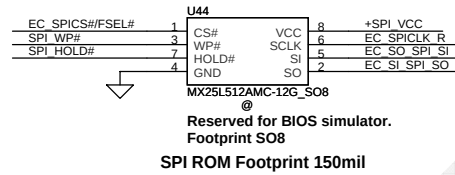
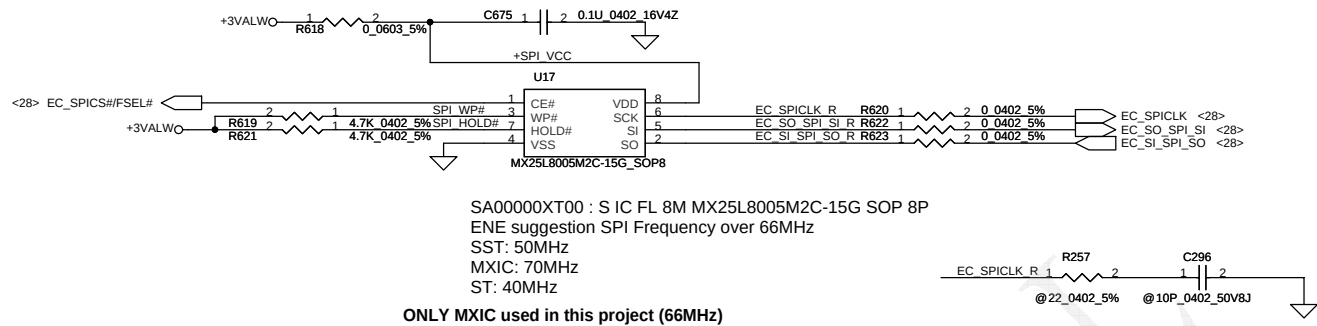
INT_KBD Conn.



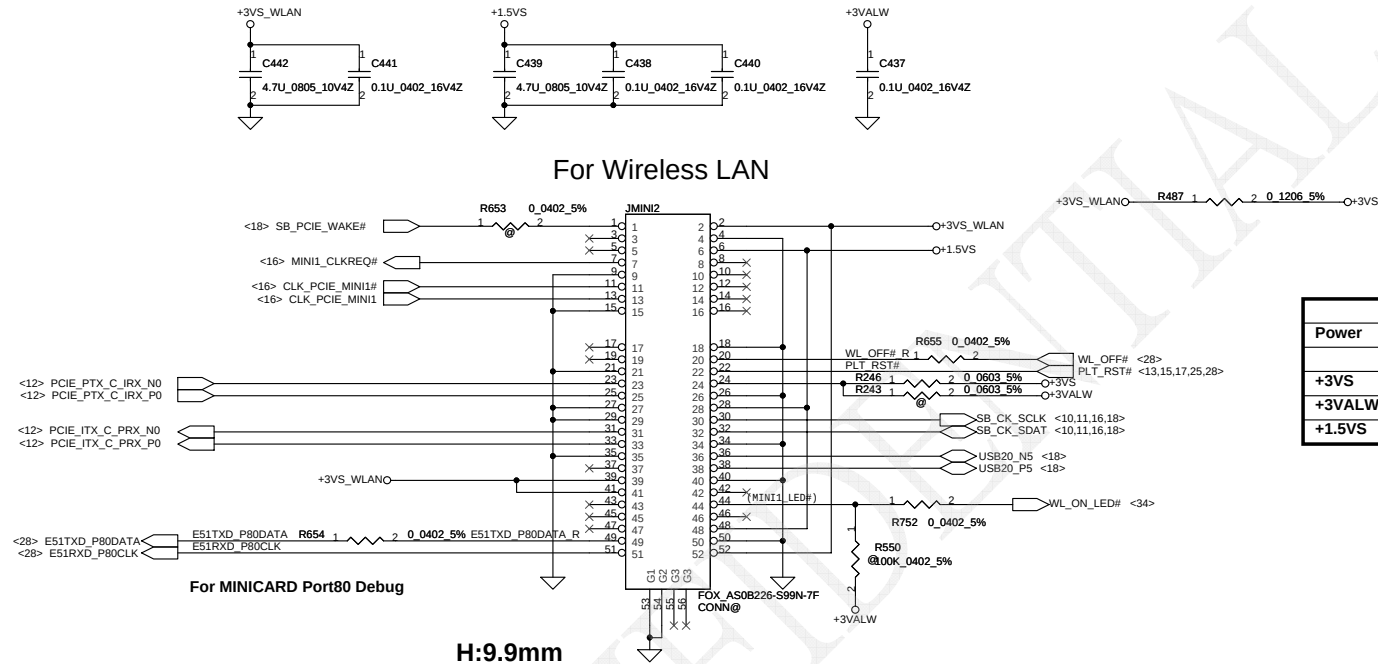
KB1 for 15"
KB2 for 17"



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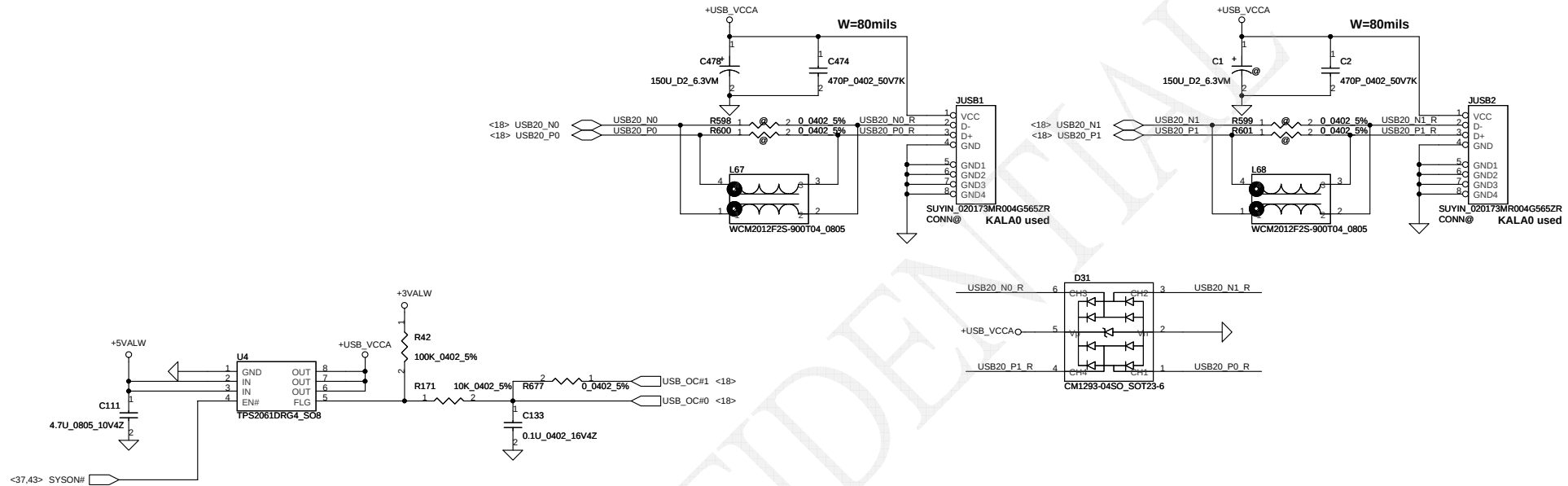
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Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3VALW	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

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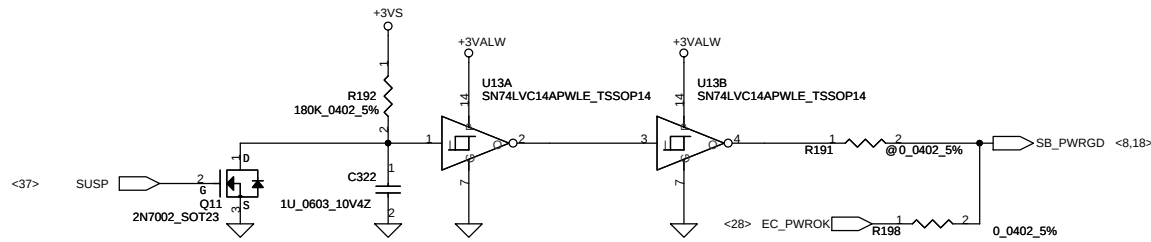
USB CONN. 1 & 2



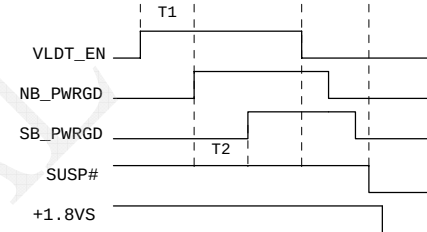
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Power ON Circuit

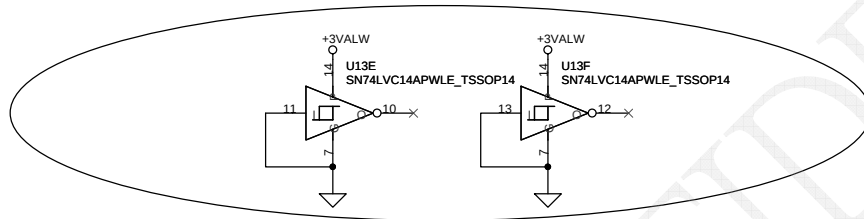
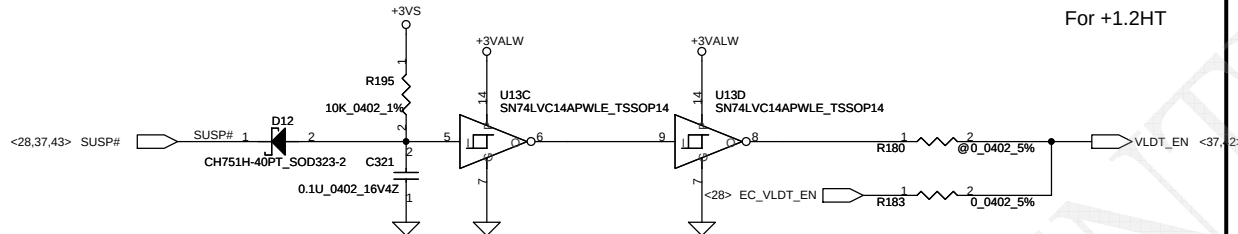
For South Bridge



note: T1 minimum 15ms, T2 minimum 33ms/maximum 500ms, SUSP# goes to low after SB_PWRGD goes to low for power down.



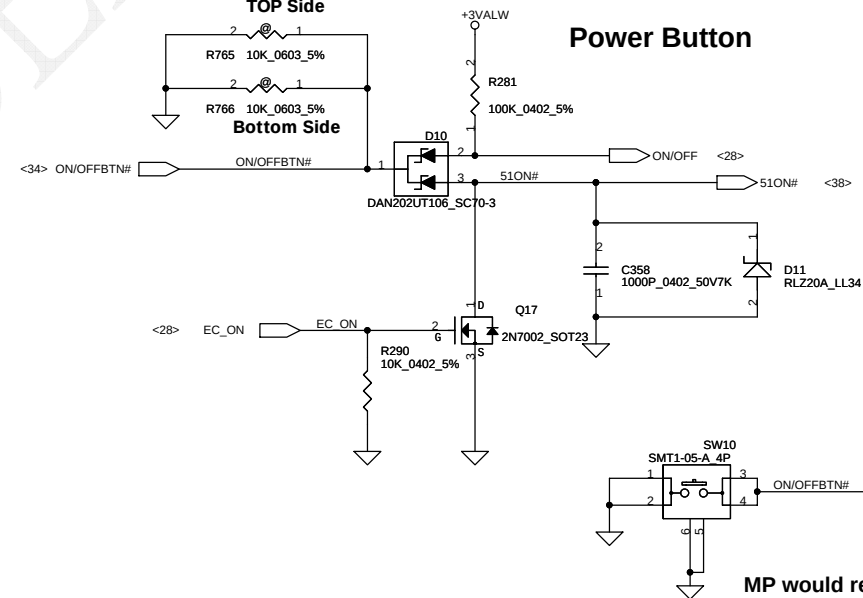
For +1.2HT



TOP Side

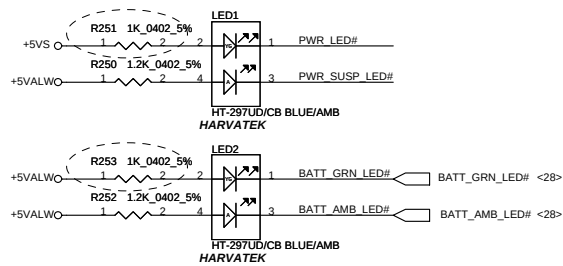
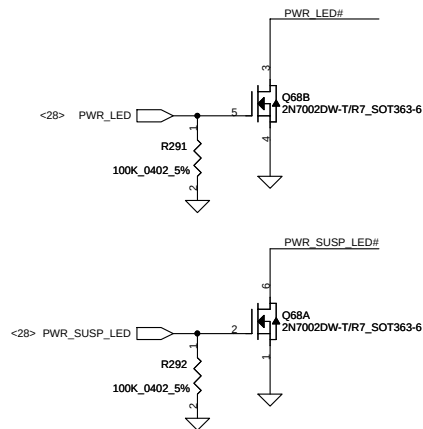
Bottom Side

Power Button

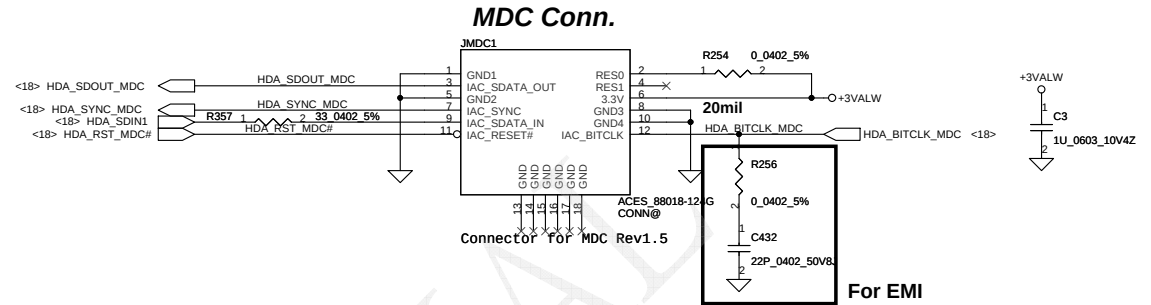


MP would remove

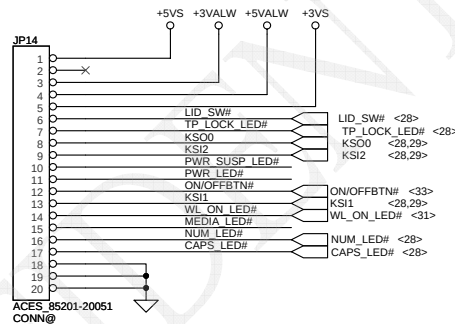
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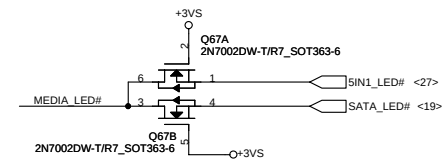
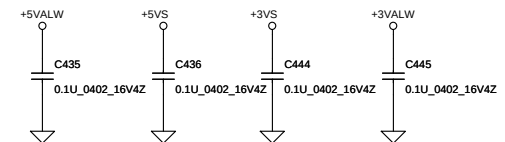
BLUE/AMB LED

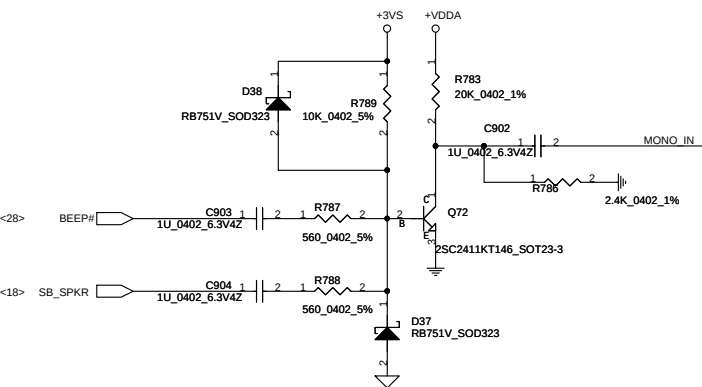


To PWR LED/B

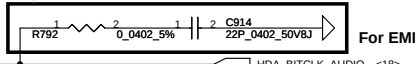
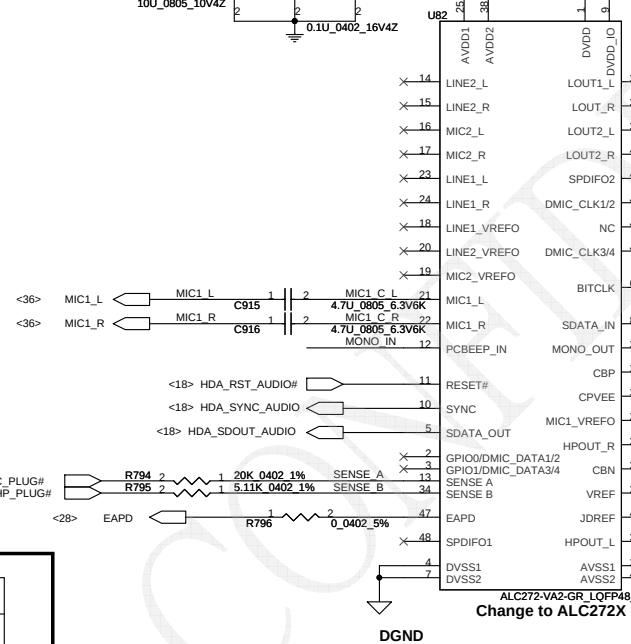
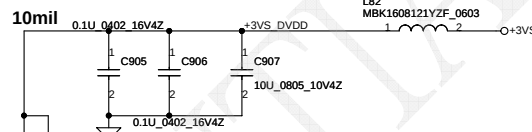
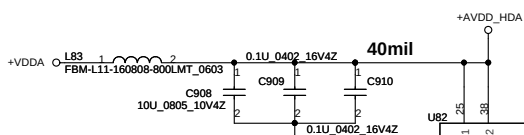
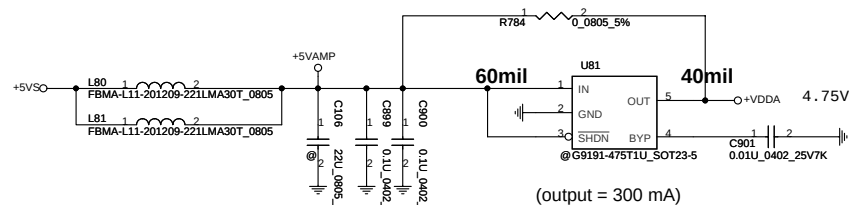


	KSO0
KSI1	WL_BTN#
KSI2	TP_LOCK_BTN#
KSI3	
KSI4	
KSI5	
KSI6	





HD Audio Codec



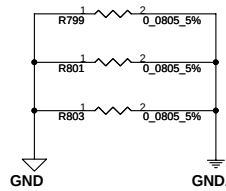
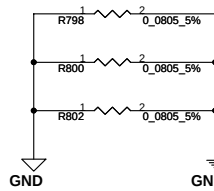
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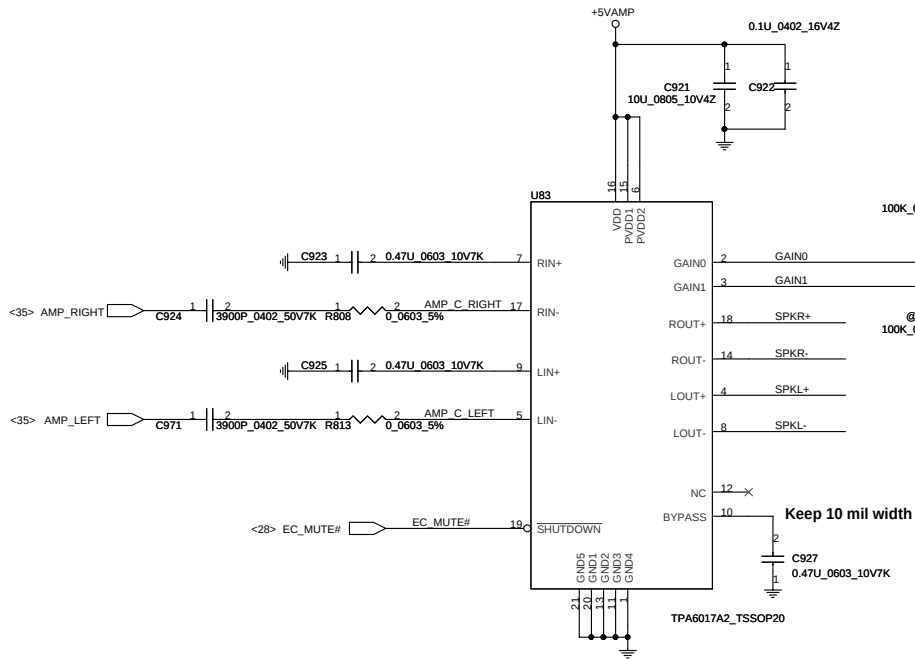
update this table

Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

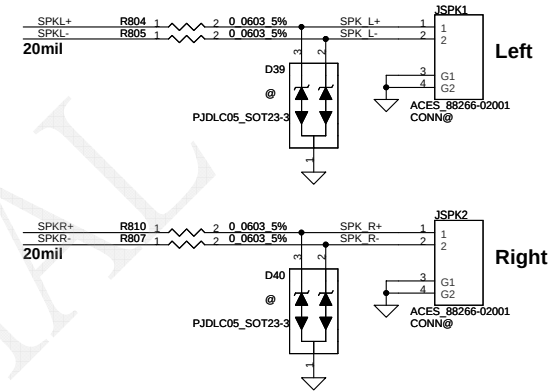
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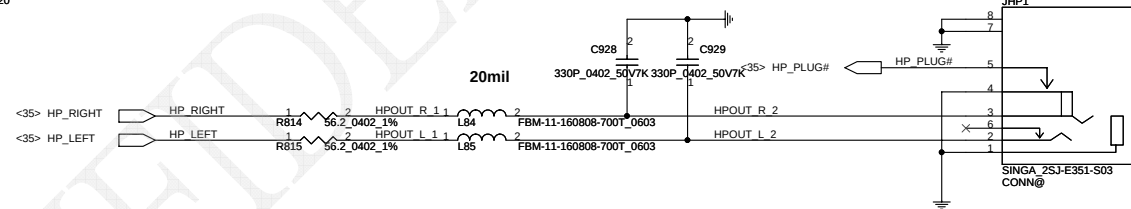
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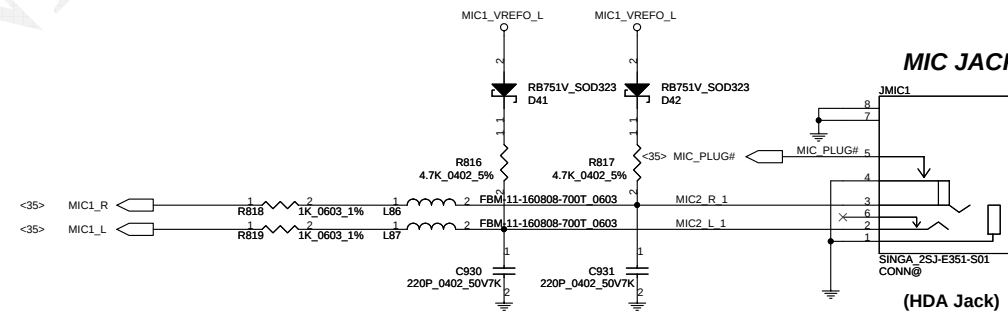
Int. Speaker Conn.



LINE Out/Headphone Out

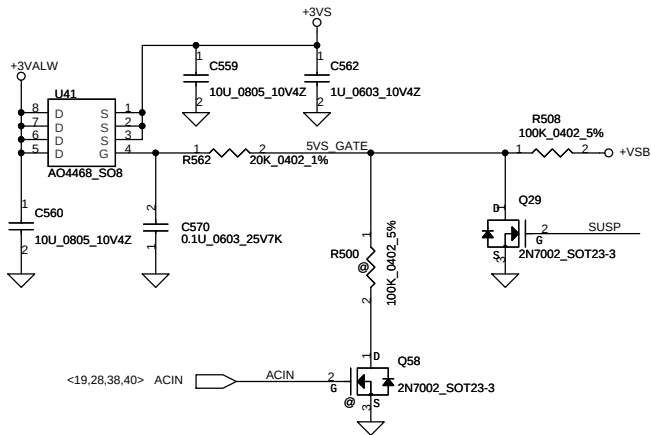


MIC JACK

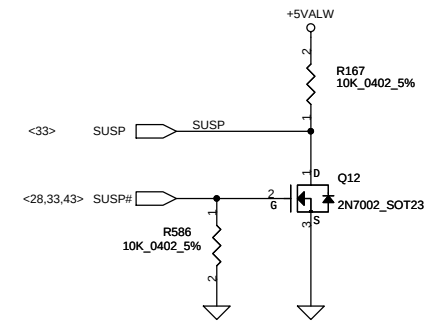
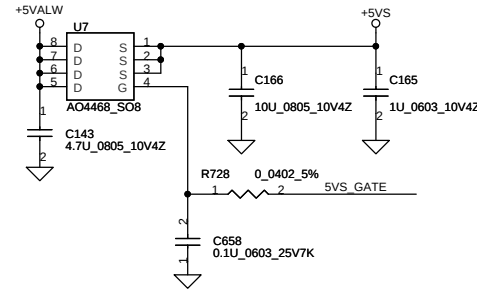


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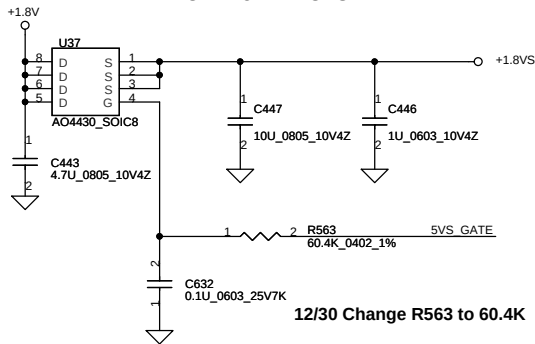
+3VALW TO +3VS



+5VALW TO +5VS

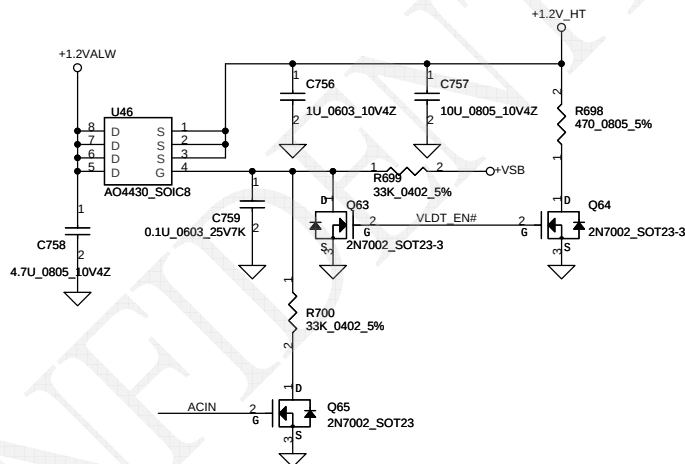


+1.8V TO +1.8VS

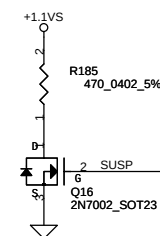
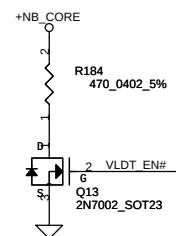
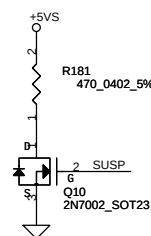
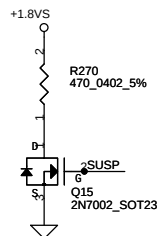
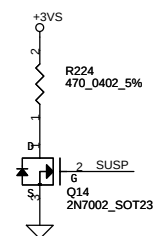
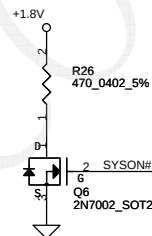
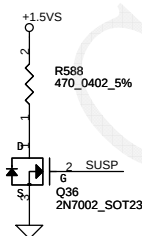
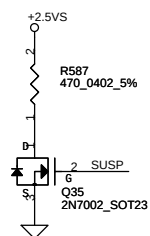
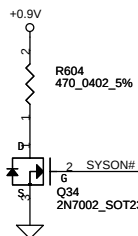
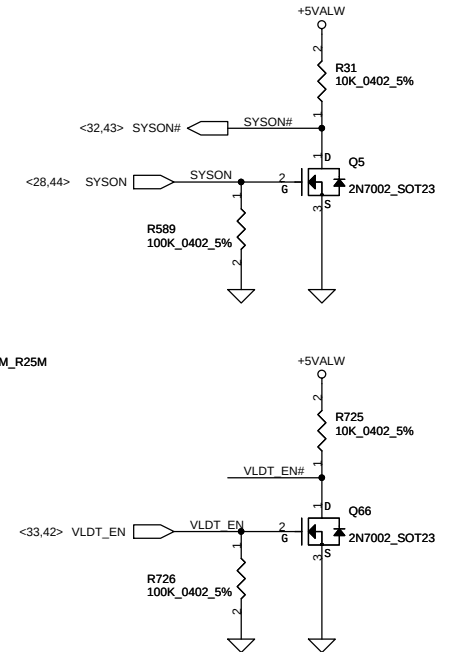


12/30 Change R563 to 60.4K

+1.2VALW TO +1.2V_HT

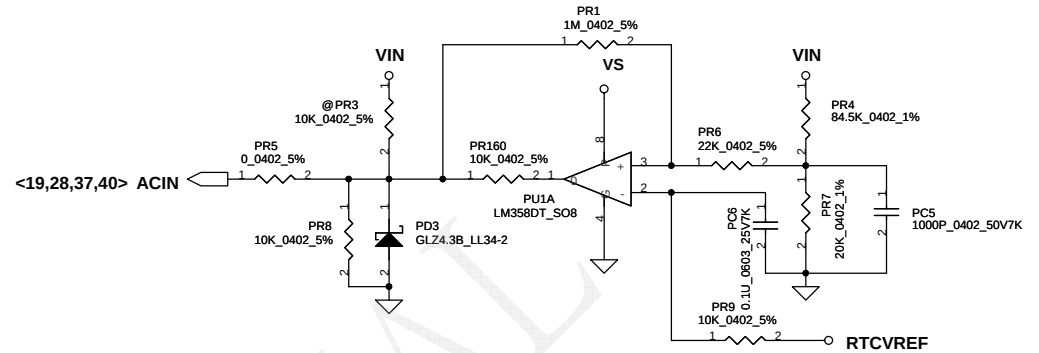
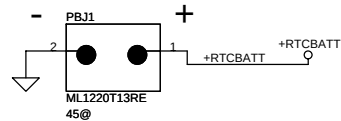
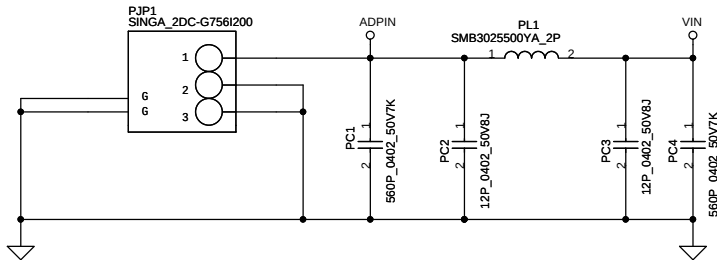


For PWR request

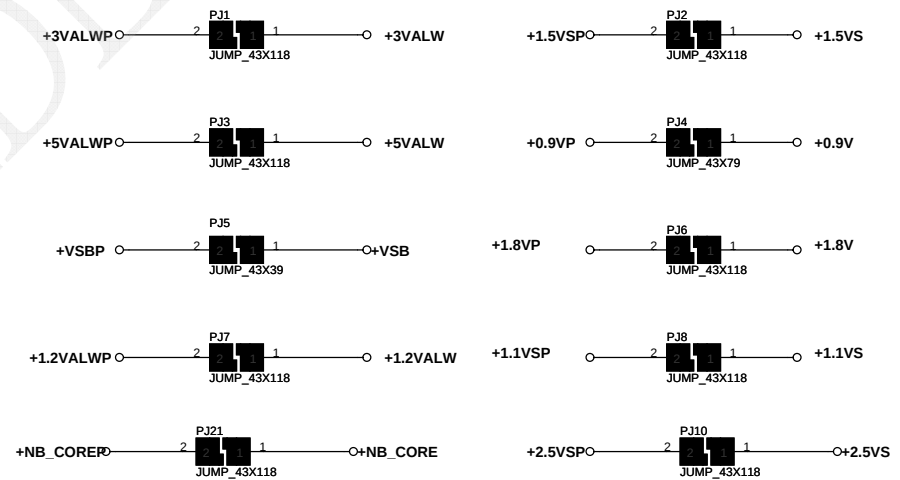
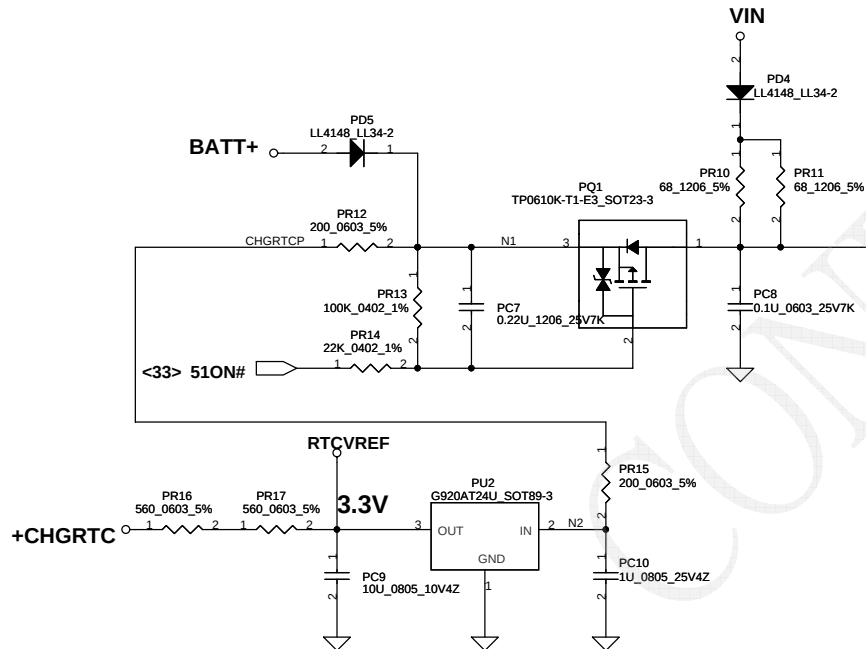


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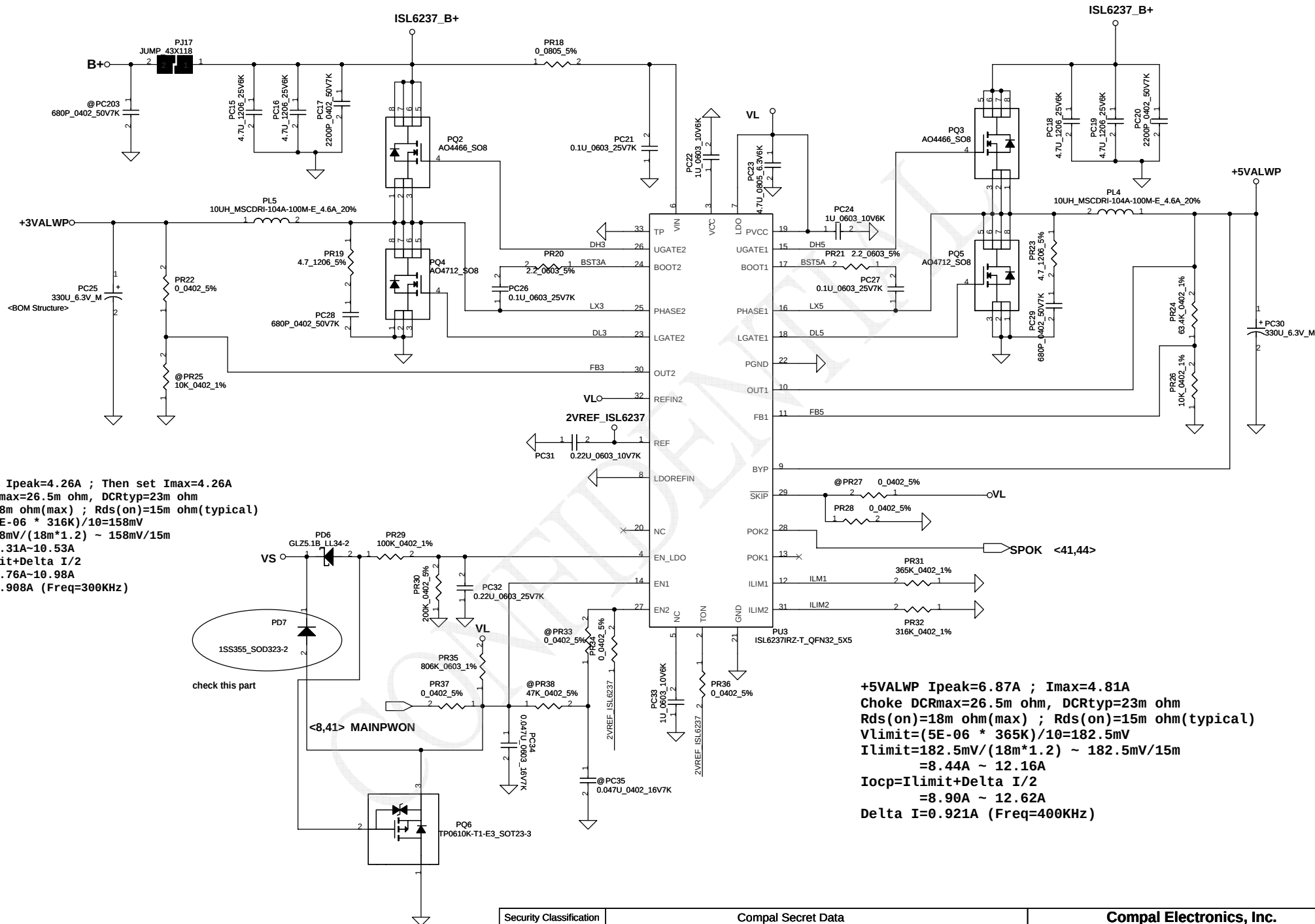
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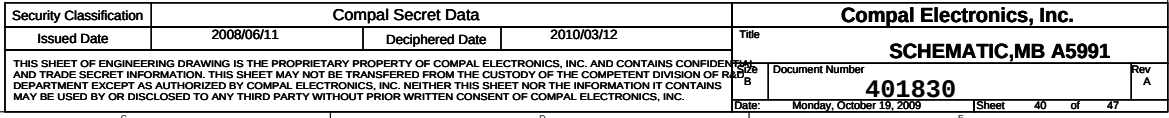
Vin Dectector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V



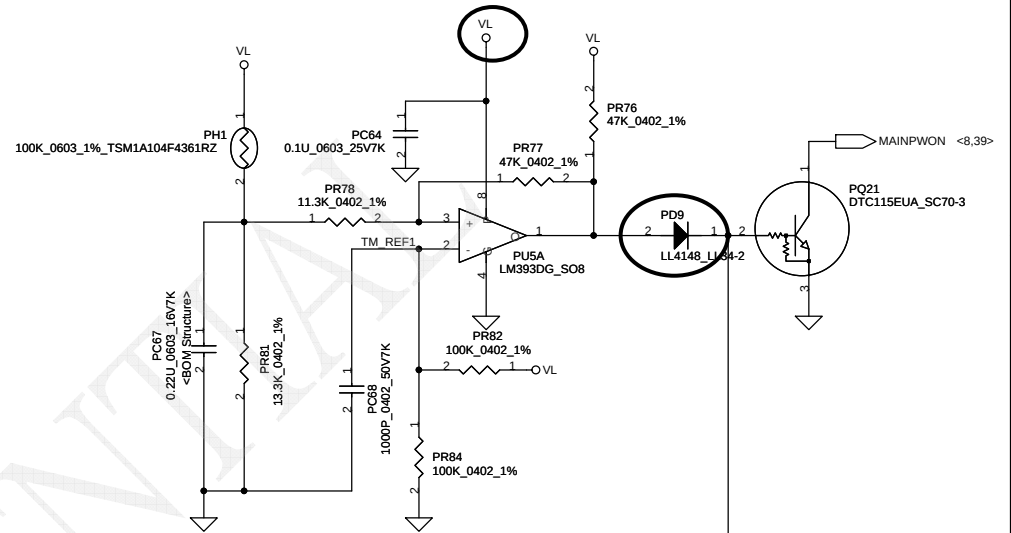
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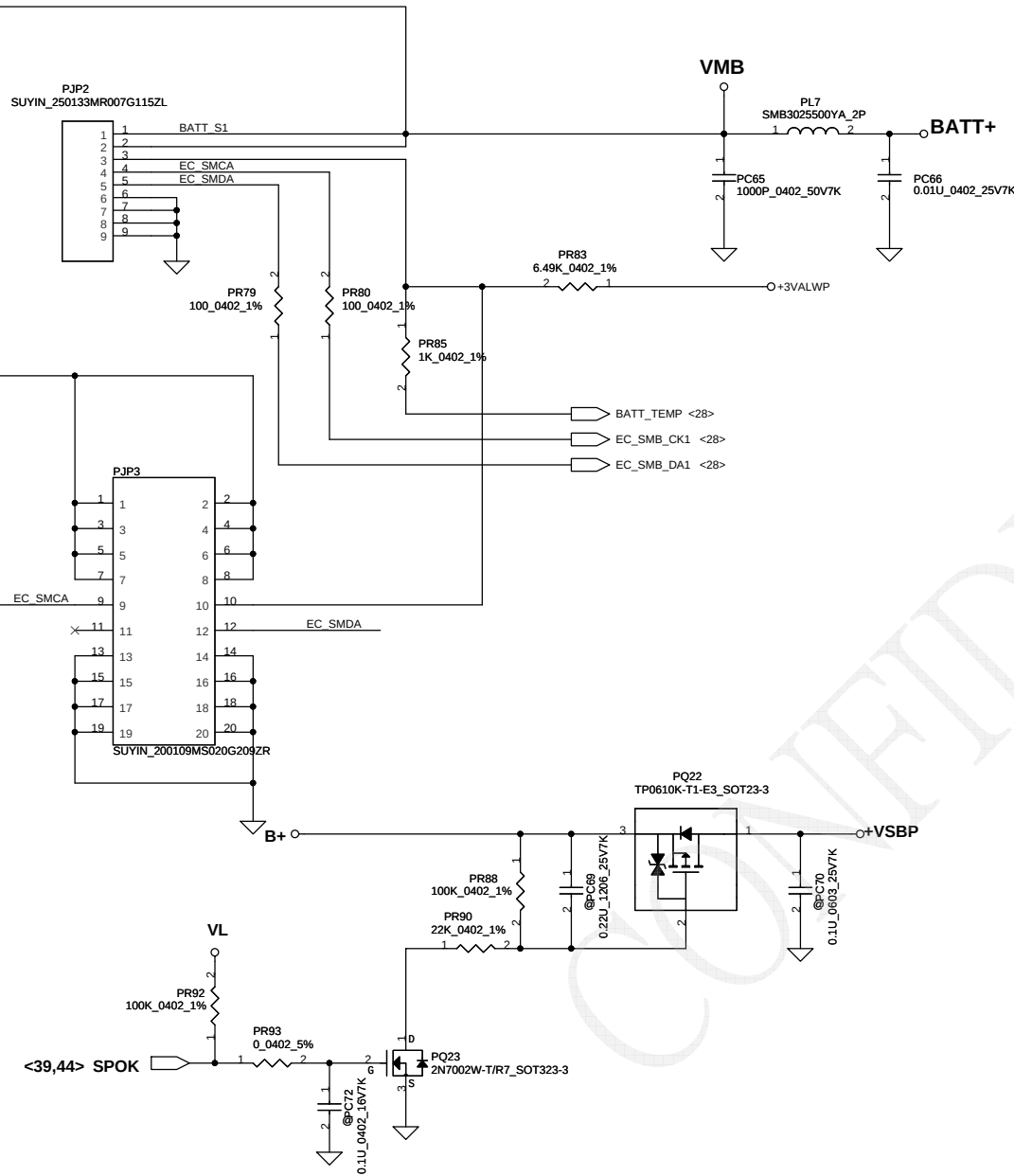
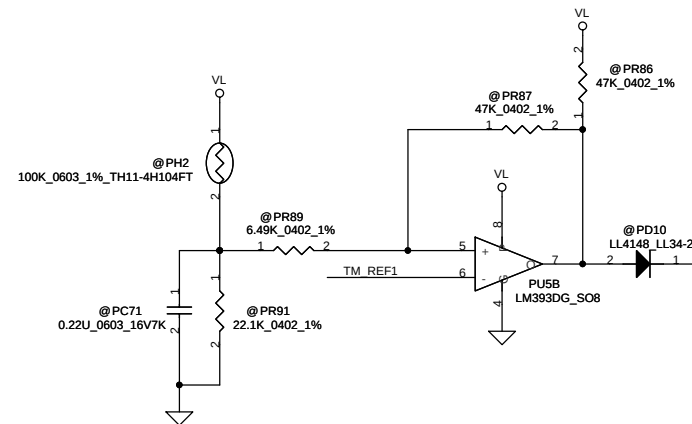
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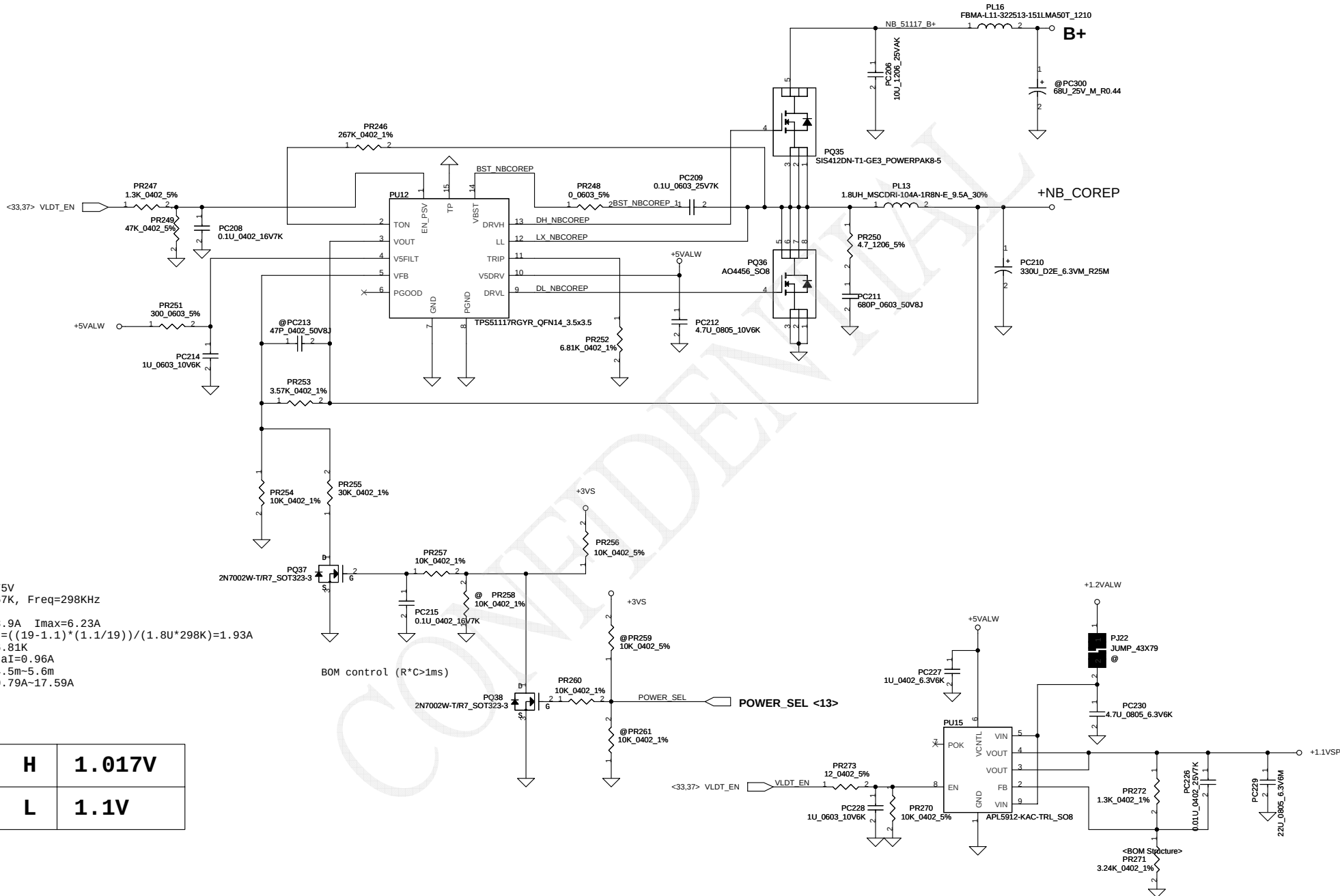
PH1 under CPU botten side :
CPU thermal protection at 92 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 75 degree C

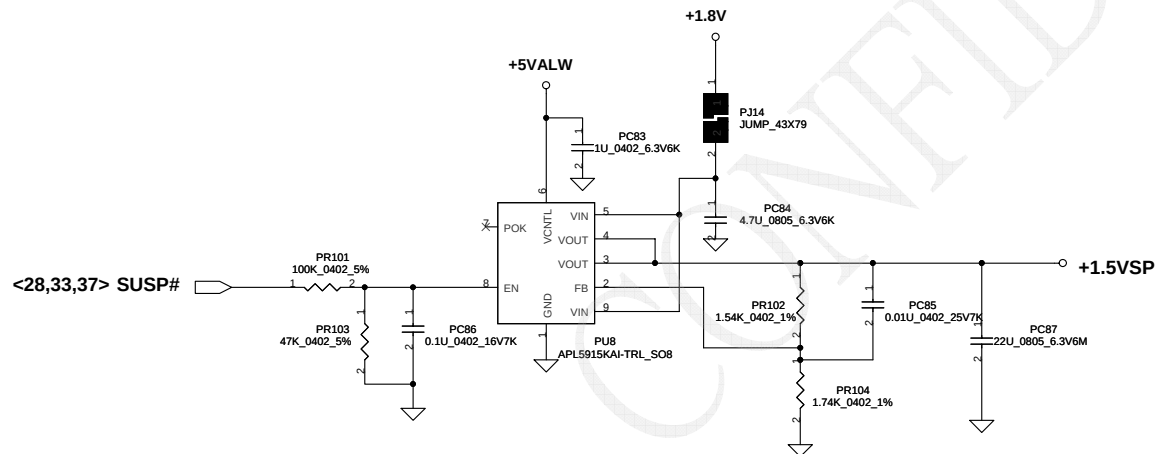
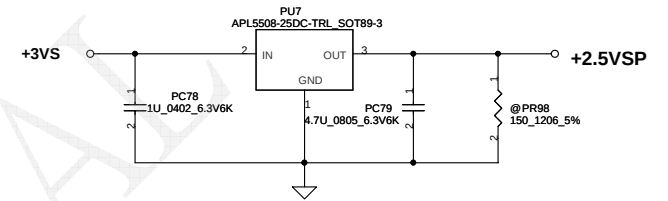
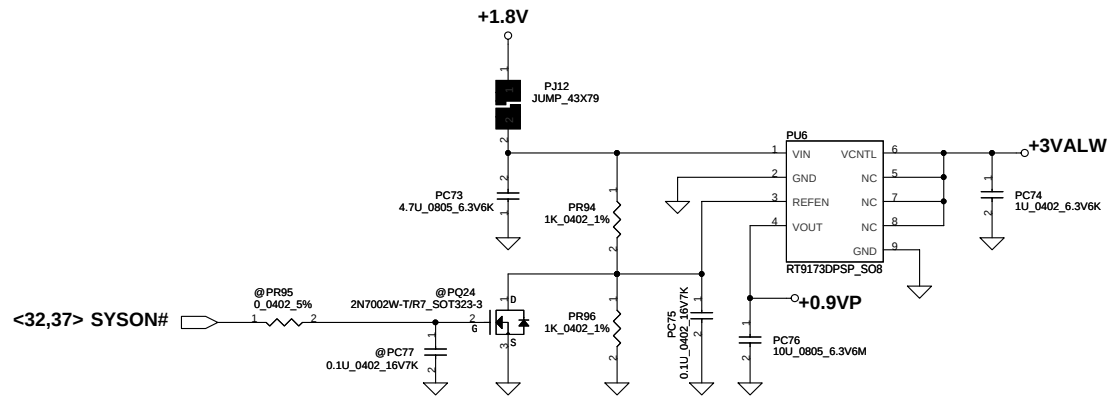


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H	1.017V
L	1.1V

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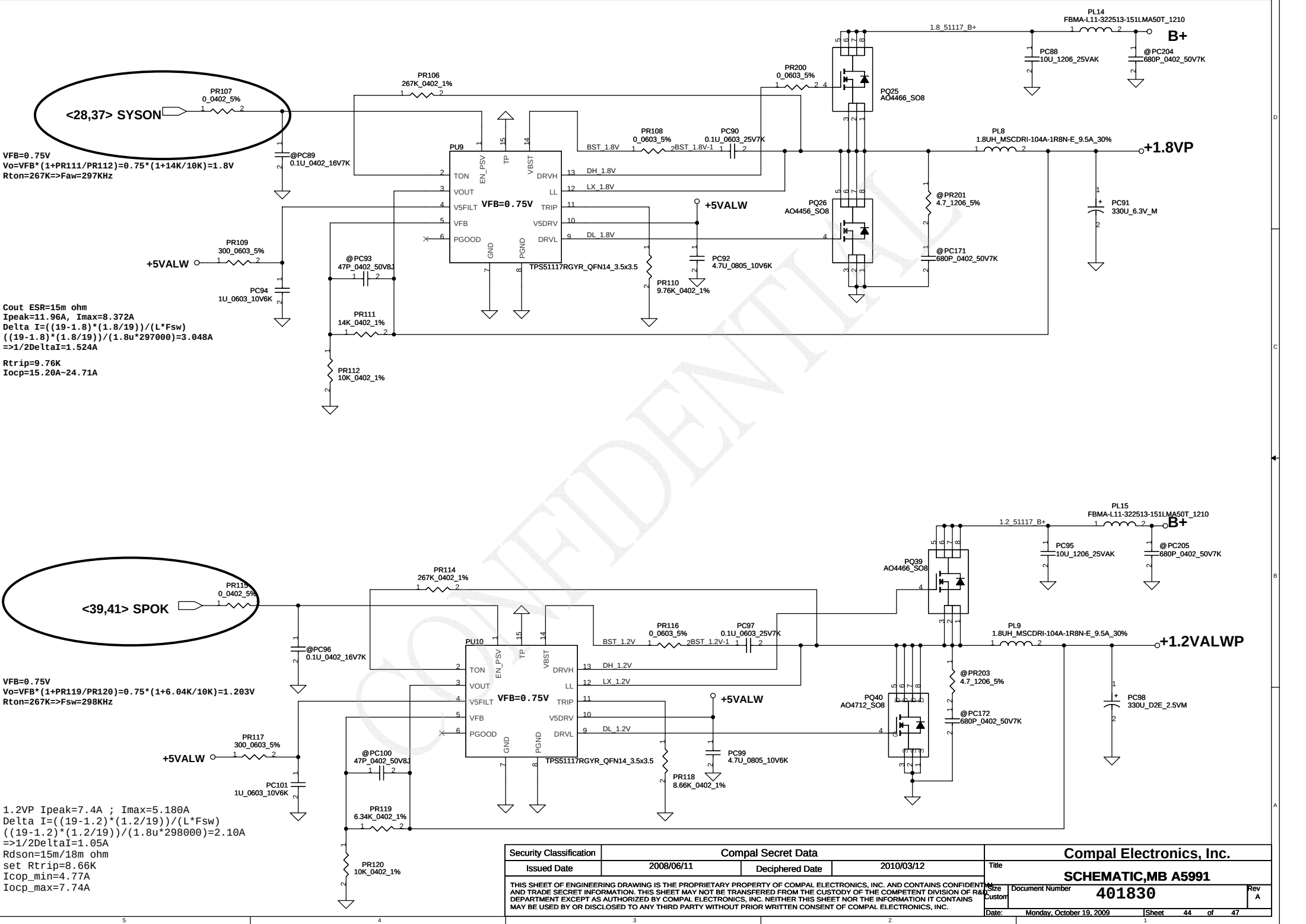
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VFB=0.75V
 $V_o = VFB * (1 + PR111 / PR112) = 0.75 * (1 + 14K / 10K) = 1.8V$
 $R_{ton} = 267K \Rightarrow F_{sw} = 297KHz$

Cout ESR=15m ohm
 $I_{peak} = 11.96A$, $I_{max} = 8.372A$
 $\Delta I = ((19 - 1.8) * (1.8 / 19)) / (L * F_{sw})$
 $((19 - 1.8) * (1.8 / 19)) / (1.8u * 297000) = 3.048A$
 $\Rightarrow 1/2 \Delta I = 1.524A$
 $R_{trip} = 9.76K$
 $I_{ocp} = 15.20A - 24.71A$

VFB=0.75V
 $V_o = VFB * (1 + PR119 / PR120) = 0.75 * (1 + 6.04K / 10K) = 1.203V$
 $R_{ton} = 267K \Rightarrow F_{sw} = 298KHz$

1.2VP $I_{peak} = 7.4A$; $I_{max} = 5.180A$
 $\Delta I = ((19 - 1.2) * (1.2 / 19)) / (L * F_{sw})$
 $((19 - 1.2) * (1.2 / 19)) / (1.8u * 298000) = 2.10A$
 $\Rightarrow 1/2 \Delta I = 1.05A$
 $R_{dson} = 15m / 18m \text{ ohm}$
 $R_{trip} = 8.66K$
 $I_{ocp_min} = 4.77A$
 $I_{ocp_max} = 7.74A$



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