MODEL NAME : *Viking 18*
PCB NO : *LA-9332P*
BOM P/N : *4619KU31L01*

Compal Confidential

Viking 18

Schematic Document

Rev: X02

2012-11-19

@ : Nopop Component

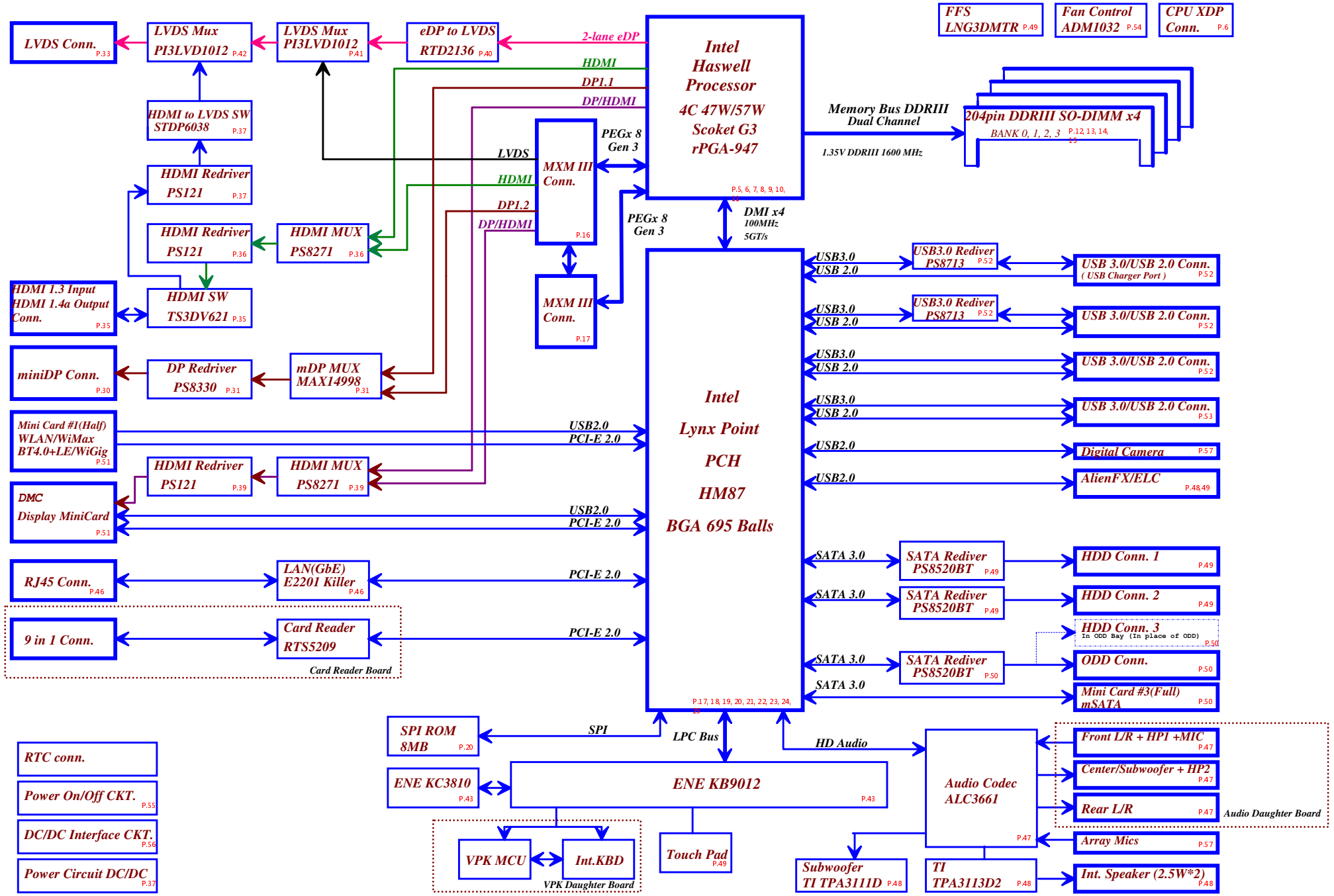
Security Classification	Compal Secret Data		
Issued Date	2012/05/14	Deciphered Date	2013/05/13

Compal Electronics, Inc.

Title: *Cover Sheet*

Size: Custom | Document Number: *\\tperdfs1\CIS\SPEC\BAS40-04_SOT23-3.pdf* | Rev: *pdf*

Date: Friday, December 14, 2012 | Sheet 1 of 56



Security Classification	Compal Secret Data		
Issued Date	2012/02/28	Deciphered Date	2013/02/27

Title	Block Diagram		
Size	Document Number		Rev
Custom	LA-9332P		0.1
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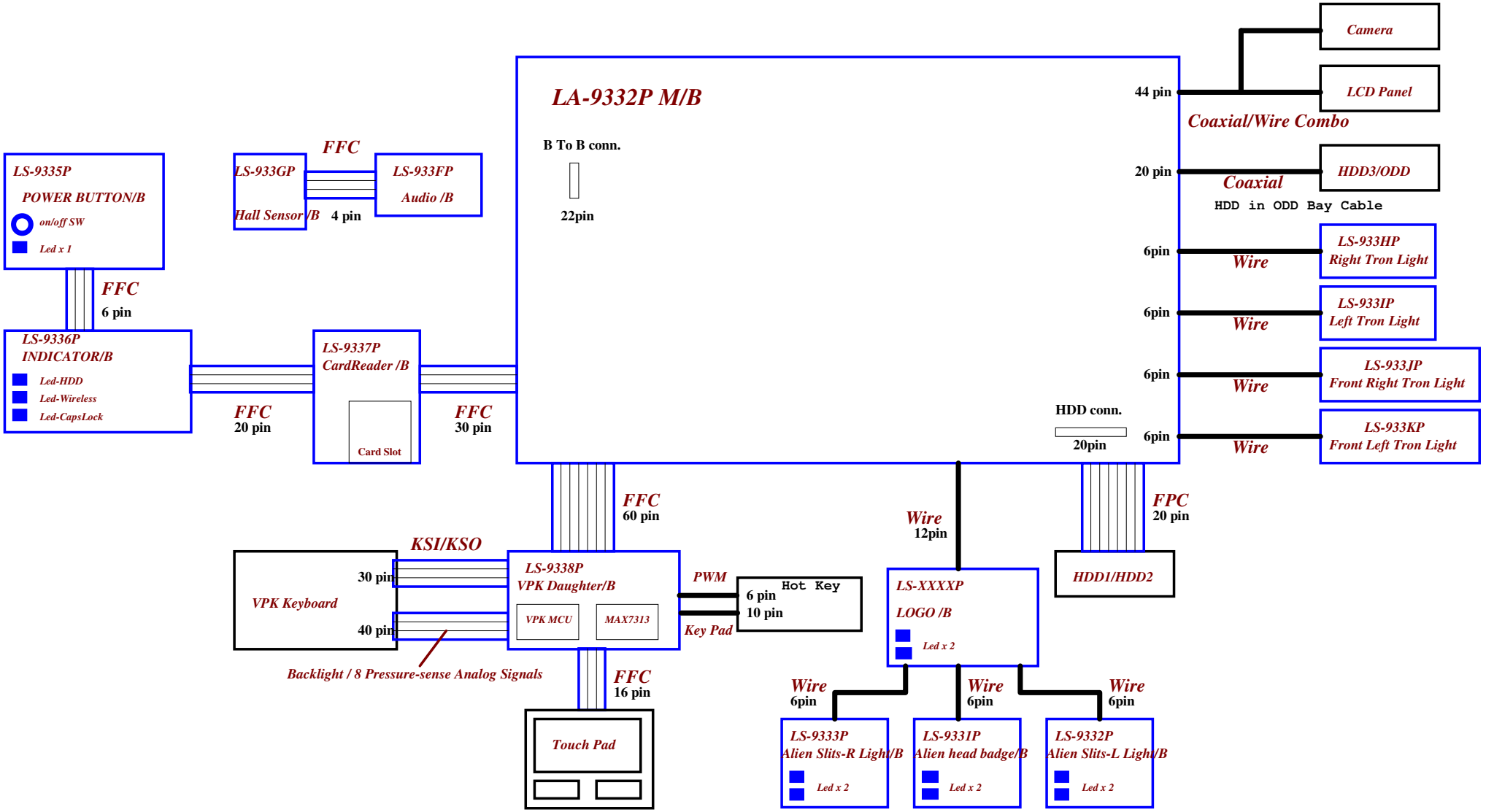
Project Code : VAS10

File Name : LA-9332P



Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

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Title: **Block Diagram**

Size | Document Number | Rev 0.1

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Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

BOARD ID Table

Board ID	PCB Revision
0	0.1 (SSI)
1	0.2 (PT)
2	0.3 (ST)
3	0.4 (QT)
4	1.0 (MP)
5	
6	
7	

USB 3.0 PORT	Connetion
1	JUSB1 (Right side)
2	JUSB2 (Right side)
3	NA
4	NA
5	JUSB3 (Left side)
6	JUSB4 (Left side)

	USB PORT#	DESTINATION
USB2.0	0	JUSB1(USB3.0 P1)
	1	JUSB2(USB3.0 P2)
	2	JUSB3(USB3.0 P5)
	3	JUSB4(USB3.0 P6)
	4	JMINI1 (WLAN)
	5	JMINI2 (DMC)
	6	AlienFX/ELC
	7	None
	8	None
	9	None
	10	None
	11	None
	12	LVDS CAMERA
	13	VPK K/B

POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM) / M-OFF	LOW	HIGH		HIGH	LOW	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Symbol Note :

: means Digital Ground

: means Analog Ground

PM TABLE

State \ power plane	+5VALW +3VALW +3VLP +3V_PCH	+1.35V +1.05V	+5VS +3VS +1.5VS +1.05VS +0.675VS +3VMXM +5VMXM +VCC_CORE +1.35V_CPU_VDDQ
S0	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
CLK	CLKOUT_PCIE0	MINI CARD-1 WLAN	CLKOUTFLEX0	None
	CLKOUT_PCIE1	MINI CARD-2 DMC	CLKOUTFLEX1	None
	CLKOUT_PCIE2	10/100/1G LAN	CLKOUTFLEX2	None
	CLKOUT_PCIE3	CARD READER	CLKOUTFLEX3	None
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_A	MXM		

CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC
PCI2	80port debug card
PCI3	None
PCI4	None

SATAIII	DESTINATION
SATA0	HDD1
SATA1	HDD2
SATA2	ODD
SATA3	mSATA
SATA4/PCIE LANE1	MINI CARD-1 WLAN
SATA5/PCIE LANE2	MINI CARD-2 DMC

PCI EXPRESS	DESTINATION
Lane 1/USB3.0 Port 3	None
Lane 2/USB3.0 Port 4	None
Lane 3	10/100/1G LAN
Lane 4	CARD READER
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None

SMBUS Control Table

	SOURCE	WLAN	DMC	BATT	DIMM	6038	4028	Thermal Sensor	FFS	2136	VPK MCU	MXM	XDP	Charger	TP	mSATA
EC_SMB_CK1 EC_SMB_DA1	KB9012			V								V		V		
EC_SMB_CK2 EC_SMB_DA2	KB9012					V	V	V		V	V					
PCH_SML0CLK PCH_SML0DATA	PCH															
PCH_SML1CLK PCH_SML1DATA	PCH															
MEM_SMBCLK MEM_SMBDATA	PCH		V		V				V				V		V	V

Link

+VCOMP_OUT

PEG_COMP 2 1 RC2
24.9_0402_1%~D

CAD Note:
Trace width=12 mils ,Spacing=15mil
Max length= 400 mils.

PEG_GTX_HRX_P[0..15] 29,30
PEG_GTX_HRX_N[0..15] 29,30
PEG_HTX_C_GRX_P[0..15] 29,30
PEG_HTX_C_GRX_N[0..15] 29,30

Haswell rPGA EDS
JCPU1A

17	DMI_CRX_PTX_N0	DMI_CRX_PTX_N0	D21	DMI_RXN_0	PEG_RCOMP	E23	PEG_COMP								
17	DMI_CRX_PTX_N1	DMI_CRX_PTX_N1	C21	DMI_RXN_1	PEG_RXN_0	M29	PEG_GTX_C_HRX_N0	CC1	1	2	0.22U_0402_16V7K~D	PEG_GTX_HRX_N0			
17	DMI_CRX_PTX_N2	DMI_CRX_PTX_N2	B21	DMI_RXN_2	PEG_RXN_1	K28	PEG_GTX_C_HRX_N1	CC2	1	2	0.22U_0402_16V7K~D	PEG_GTX_HRX_N1			
17	DMI_CRX_PTX_N3	DMI_CRX_PTX_N3	A21	DMI_RXN_3	PEG_RXN_2	M31	PEG_GTX_C_HRX_N2	CC3	1	2	0.22U_0402_16V7K~D	PEG_GTX_HRX_N2			
					PEG_RXN_3	L30	PEG_GTX_C_HRX_N3	CC4	1	2	0.22U_0402_16V7K~D	PEG_GTX_HRX_N3			
17	DMI_CRX_PTX_P0	DMI_CRX_PTX_P0	D20	DMI_RXP_0	PEG_RXN_4	M33	PEG_GTX_C_HRX_N4	CC5	1	2	0.22U_0402_16V7K~D	PEG_GTX_HRX_N4			
17	DMI_CRX_PTX_P1	DMI_CRX_PTX_P1	C20	DMI_RXP_1	PEG_RXN_5	L32	PEG_GTX_C_HRX_N5	CC13	1	2	0.22U_0402_16V7K~D	PEG_GTX_HRX_N5			
17	DMI_CRX_PTX_P2	DMI_CRX_PTX_P2	B20	DMI_RXP_2	PEG_RXN_6	M35	PEG_GTX_C_HRX_N6	CC6	1	2	0.22U_0402_16V7K~D	PEG_GTX_HRX_N6			
17	DMI_CRX_PTX_P3	DMI_CRX_PTX_P3	A20	DMI_RXP_3	PEG_RXN_7	L34	PEG_GTX_C_HRX_N7	CC7	1	2	0.22U_0402_16V7K~D	PEG_GTX_HRX_N7			
					PEG_RXN_8	E29	PEG_GTX_C_HRX_N8	CC8	1	2	0.22U_0402_16V7K~D	PEG_GTX_HRX_N8			
17	DMI_CTX_PRX_N0	DMI_CTX_PRX_N0	D18	DMI_TXN_0	PEG_RXN_9	D28	PEG_GTX_C_HRX_N9	CC9	1	2	0.22U_0402_16V7K~D	PEG_GTX_HRX_N9			
17	DMI_CTX_PRX_N1	DMI_CTX_PRX_N1	C17	DMI_TXN_1	PEG_RXN_10	E31	PEG_GTX_C_HRX_N10	CC10	1	2	0.22U_0402_16V7K~D	PEG_GTX_HRX_N10			
17	DMI_CTX_PRX_N2	DMI_CTX_PRX_N2	B17	DMI_TXN_2	PEG_RXN_11	D30	PEG_GTX_C_HRX_N11	CC11	1	2	0.22U_0402_16V7K~D	PEG_GTX_HRX_N11			
17	DMI_CTX_PRX_N3	DMI_CTX_PRX_N3	A17	DMI_TXN_3	PEG_RXN_12	E35	PEG_GTX_C_HRX_N12	CC12	1	2	0.22U_0402_16V7K~D	PEG_GTX_HRX_N12			
					PEG_RXN_13	D34	PEG_GTX_C_HRX_N13	CC14	1	2	0.22U_0402_16V7K~D	PEG_GTX_HRX_N13			
17	DMI_CTX_PRX_P0	DMI_CTX_PRX_P0	D17	DMI_TXP_0	PEG_RXN_14	E33	PEG_GTX_C_HRX_N14	CC15	1	2	0.22U_0402_16V7K~D	PEG_GTX_HRX_N14			
17	DMI_CTX_PRX_P1	DMI_CTX_PRX_P1	C18	DMI_TXP_1	PEG_RXN_15	E32	PEG_GTX_C_HRX_N15	CC16	1	2	0.22U_0402_16V7K~D	PEG_GTX_HRX_N15			
17	DMI_CTX_PRX_P2	DMI_CTX_PRX_P2	B18	DMI_TXP_2	PEG_RXP_0	L29	PEG_GTX_C_HRX_P0	CC17	1	2	0.22U_0402_16V7K~D	PEG_GTX_HRX_P0			
17	DMI_CTX_PRX_P3	DMI_CTX_PRX_P3	A18	DMI_TXP_3	PEG_RXP_1	L28	PEG_GTX_C_HRX_P1	CC18	1	2	0.22U_0402_16V7K~D	PEG_GTX_HRX_P1			
					PEG_RXP_2	L31	PEG_GTX_C_HRX_P2	CC19	1	2	0.22U_0402_16V7K~D	PEG_GTX_HRX_P2			
					PEG_RXP_3	K30	PEG_GTX_C_HRX_P3	CC20	1	2	0.22U_0402_16V7K~D	PEG_GTX_HRX_P3			
					PEG_RXP_4	L33	PEG_GTX_C_HRX_P4	CC21	1	2	0.22U_0402_16V7K~D	PEG_GTX_HRX_P4			
					PEG_RXP_5	K32	PEG_GTX_C_HRX_P5	CC22	1	2	0.22U_0402_16V7K~D	PEG_GTX_HRX_P5			
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					PEG_RXP_7	K34	PEG_GTX_C_HRX_P7	CC24	1	2	0.22U_0402_16V7K~D	PEG_GTX_HRX_P7			
					PEG_RXP_8	F29	PEG_GTX_C_HRX_P8	CC25	1	2	0.22U_0402_16V7K~D	PEG_GTX_HRX_P8			
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					PEG_RXP_11	E30	PEG_GTX_C_HRX_P11	CC28	1	2	0.22U_0402_16V7K~D	PEG_GTX_HRX_P11			
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					PEG_TXP_5	H30	PEG_HTX_GRX_P5	CC54	1	2	0.22U_0402_16V7K~D	PEG_HTX_C_GRX_P5			
					PEG_TXP_6	B33	PEG_HTX_GRX_P6	CC55	1	2	0.22U_0402_16V7K~D	PEG_HTX_C_GRX_P6			
					PEG_TXP_7	A32	PEG_HTX_GRX_P7	CC56	1	2	0.22U_0402_16V7K~D	PEG_HTX_C_GRX_P7			
					PEG_TXP_8	C31	PEG_HTX_GRX_P8	CC57	1	2	0.22U_0402_16V7K~D	PEG_HTX_C_GRX_P8			
					PEG_TXP_9	B30	PEG_HTX_GRX_P9	CC58	1	2	0.22U_0402_16V7K~D	PEG_HTX_C_GRX_P9			
					PEG_TXP_10	C29	PEG_HTX_GRX_P10	CC59	1	2	0.22U_0402_16V7K~D	PEG_HTX_C_GRX_P10			
					PEG_TXP_11	B28	PEG_HTX_GRX_P11	CC60	1	2	0.22U_0402_16V7K~D	PEG_HTX_C_GRX_P11			
					PEG_TXP_12	C27	PEG_HTX_GRX_P12	CC61	1	2	0.22U_0402_16V7K~D	PEG_HTX_C_GRX_P12			
					PEG_TXP_13	B26	PEG_HTX_GRX_P13	CC62	1	2	0.22U_0402_16V7K~D	PEG_HTX_C_GRX_P13			
					PEG_TXP_14	C25	PEG_HTX_GRX_P14	CC63	1	2	0.22U_0402_16V7K~D	PEG_HTX_C_GRX_P14			
					PEG_TXP_15	B24	PEG_HTX_GRX_P15	CC64	1	2	0.22U_0402_16V7K~D	PEG_HTX_C_GRX_P15			

Near MXM Connector

@
17 FDI_CSYNC — RC3 2 — 1 0_0402_1% — FDI_CSYNC_R H29 — FDI_CSYNC
17 FDI_INT — RC87 2 — 1 0_0402_1% — FDI_INT_R J29 — FDI_INT
@

DMI
PEG
FDI

1 OF 9
INTEL_HASWELL_HASWELL

CONN@

Security Classification	Compal Secret Data		
Issued Date	2012/05/28	Deciphered Date	2013/05/27

Compal Electronics, Inc.

Title: CPU (1/7) DMI,PEG

Size: Custom | Document Number: LA-9332P | Rev: 0.1

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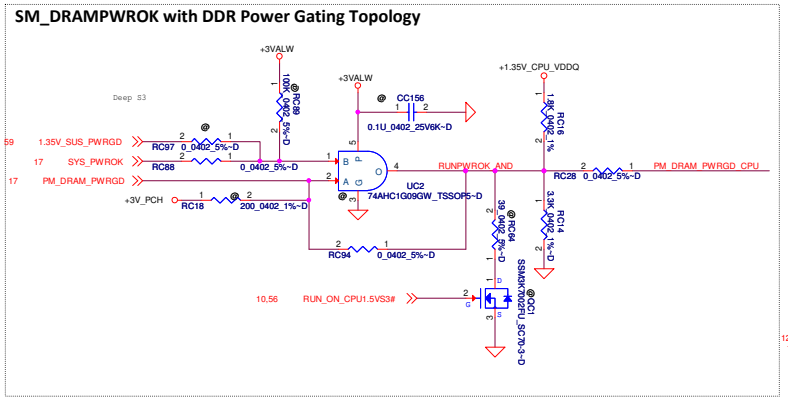
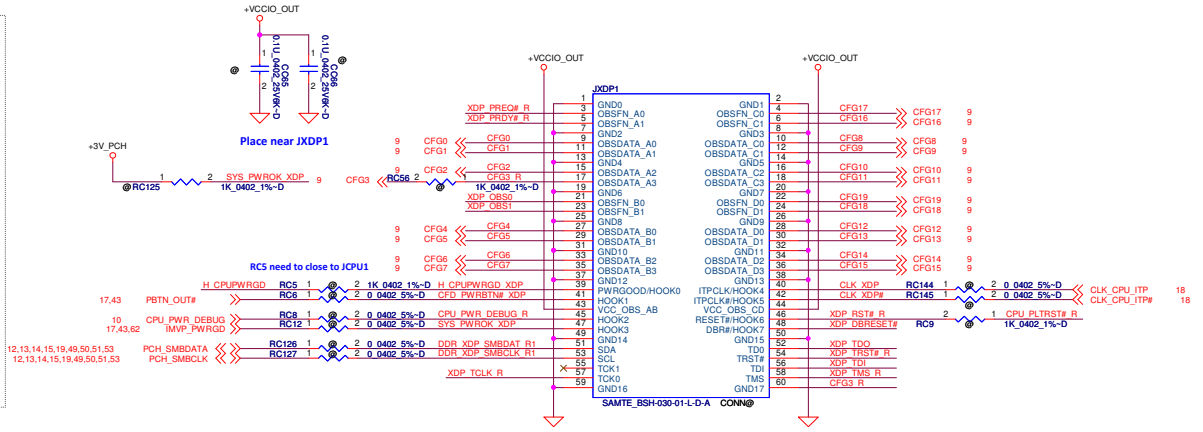
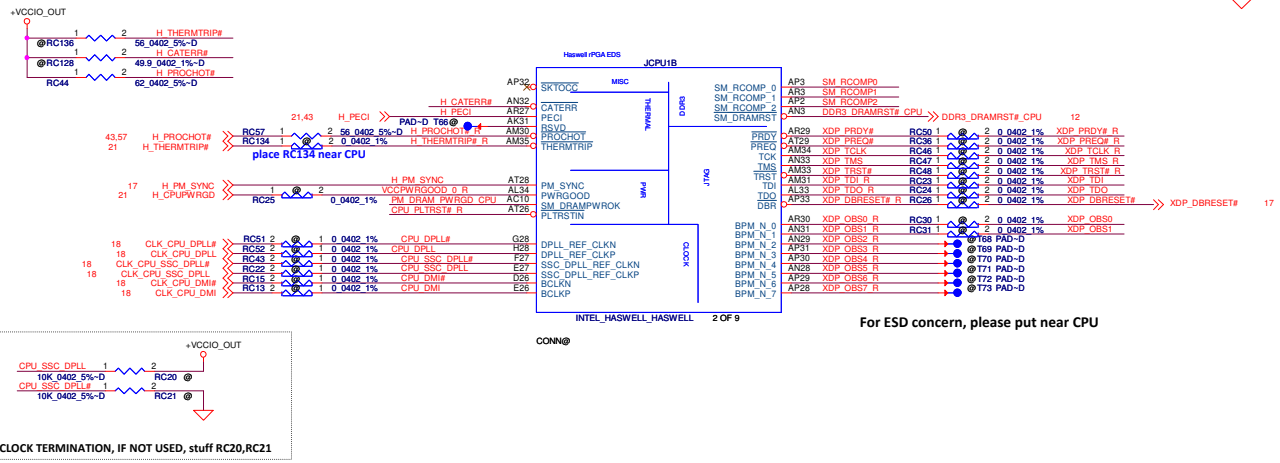
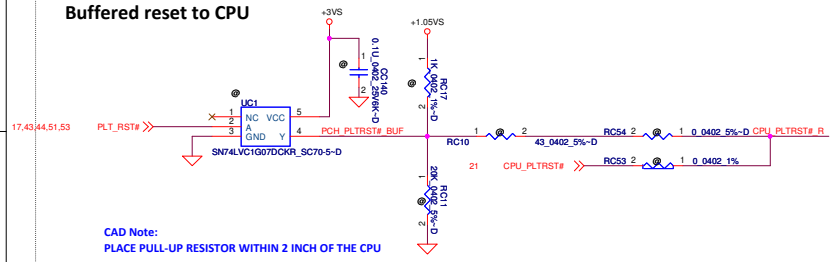
SM_DRAMPWROK with DDR Power Gating Topology

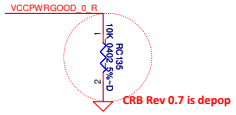




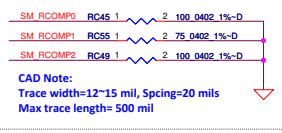


Buffered reset to CPU



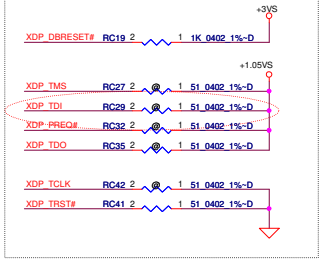


DDR3 COMPENSATION SIGNALS



CRB Rev 0.7 no pull up

PU/PD for JTAG signals



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Compal Electronics, Inc.

Title: CPU (2/7) PM,XDP,CLK

Size: Custom | Document Number: LA-9332P | Rev: 0.1

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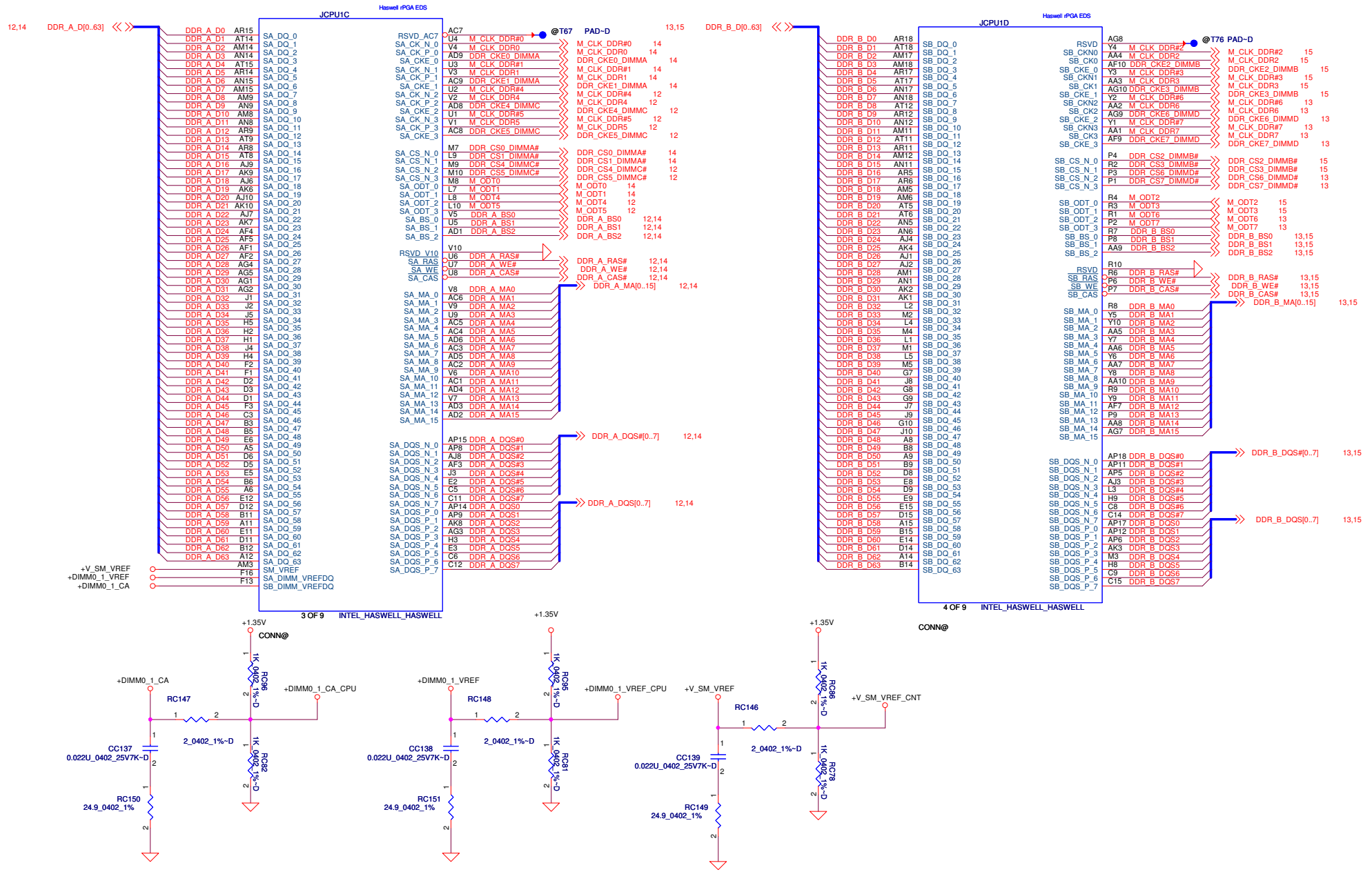

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Issued Date	2012/05/28	Deciphered Date	2013/05/27

Compal Electronics, Inc.

Title: CPU (3/7) DDRIII

Size	Document Number	Rev
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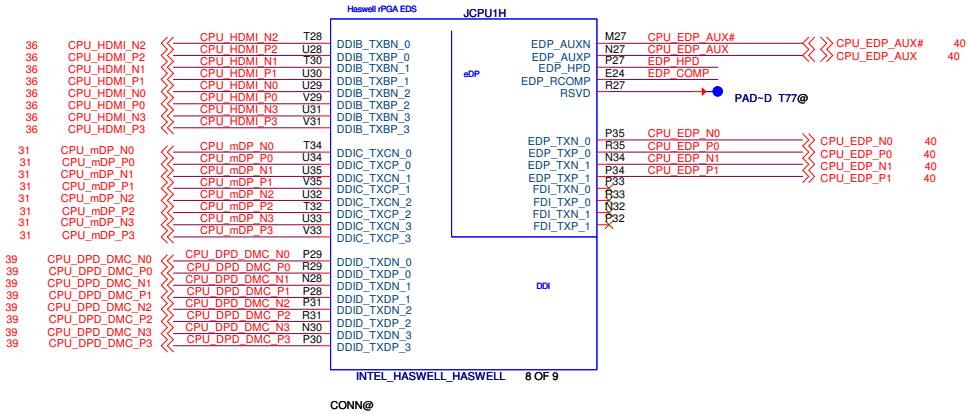
COMPENSATION PU FOR eDP

CAD Note:Trace width=20 mils ,Spacing=25mil, Max length=100 mils.

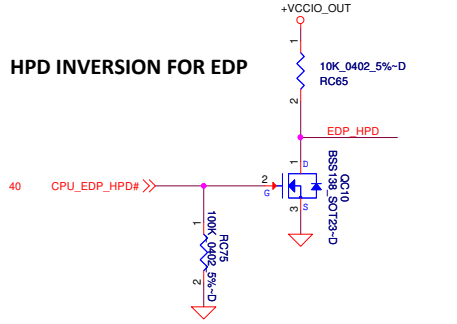
HDMI

mDP

DMC



HPD INVERSION FOR EDP



Security Classification	Compal Secret Data		
Issued Date	2012/05/28	Deciphered Date	2013/05/27

Compal Electronics, Inc.

Title: CPU (4/7) FDI,eDP,DDI

Size: Custom | Document Number: LA-9332P | Rev: 0.1

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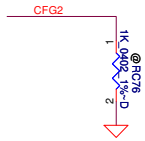
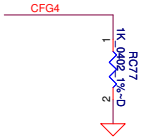
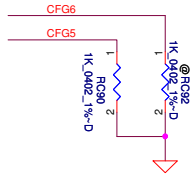
CFG STRAPS for CPU



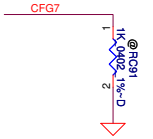
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



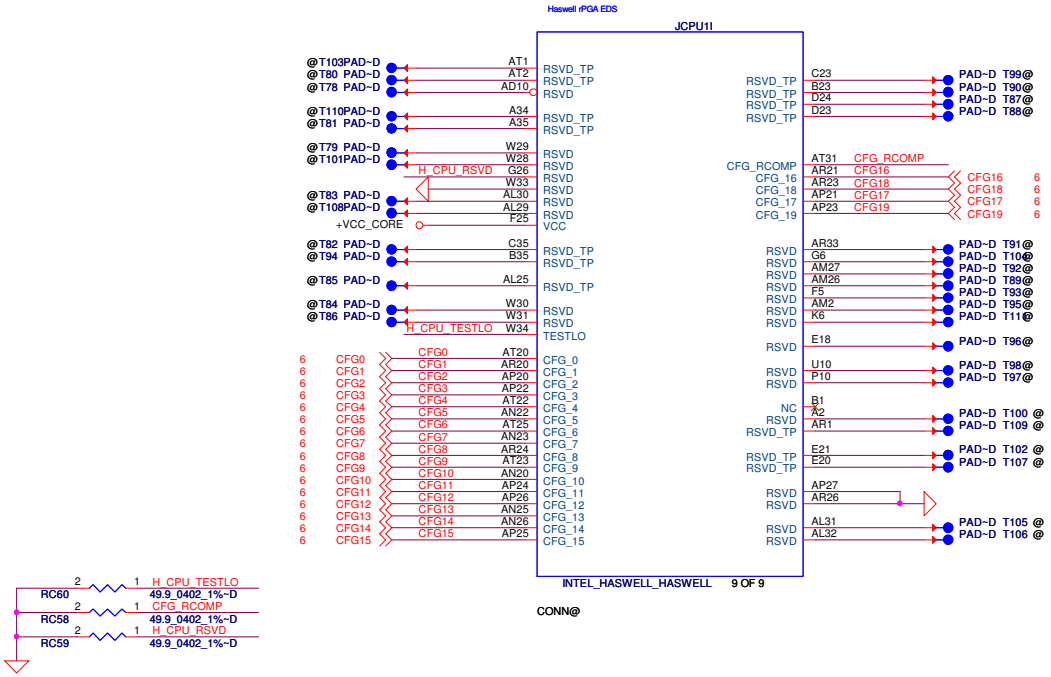
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



Security Classification	Compal Secret Data		
Issued Date	2012/05/28	Deciphered Date	2013/05/27

Compal Electronics, Inc.

Title: CPU (5/7) RSVD,CFG

Size: Custom | Document Number: LA-9332P | Rev: 0.1

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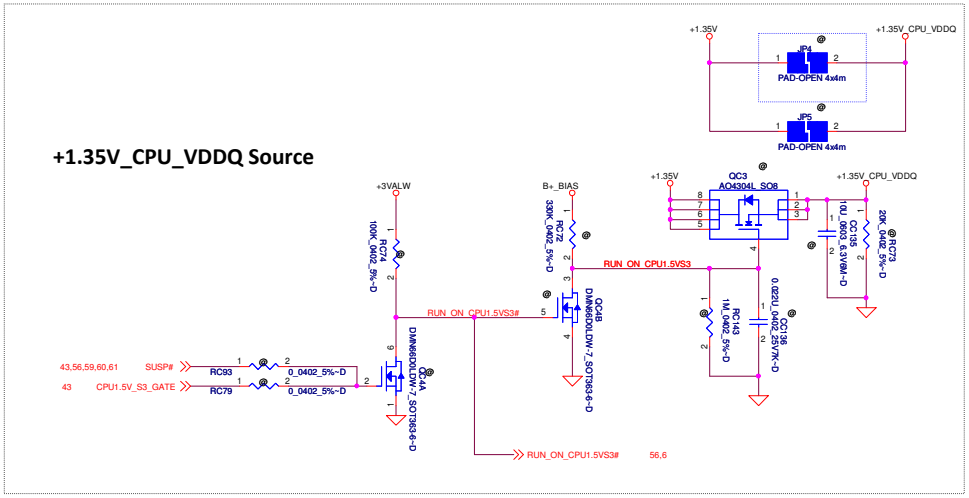
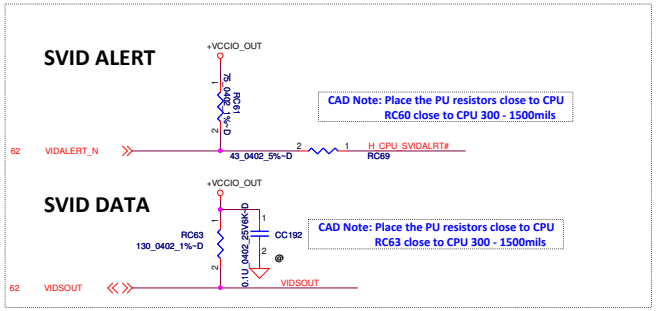
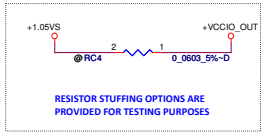
+1.35V_CPU_VDDQ Source



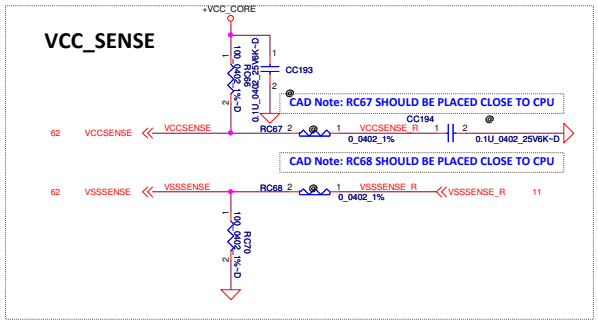
SVID ALERT

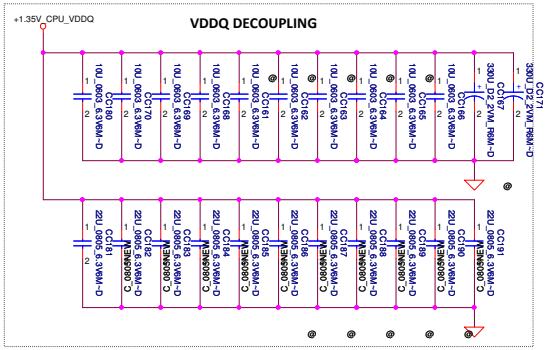


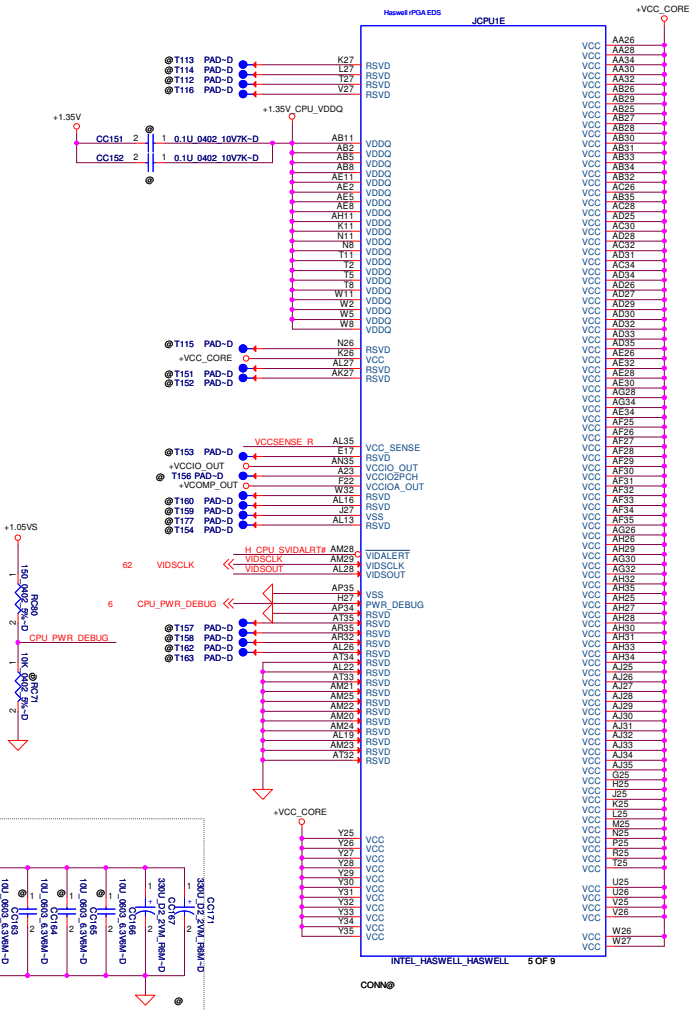
SVID DATA



VCC_SENSE







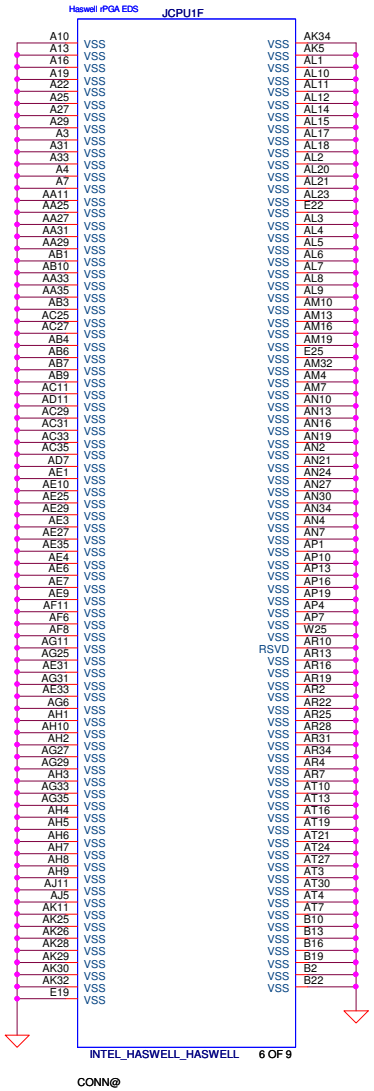
Security Classification	Compal Secret Data		
Issued Date	2012/05/28	Deciphered Date	2013/05/27

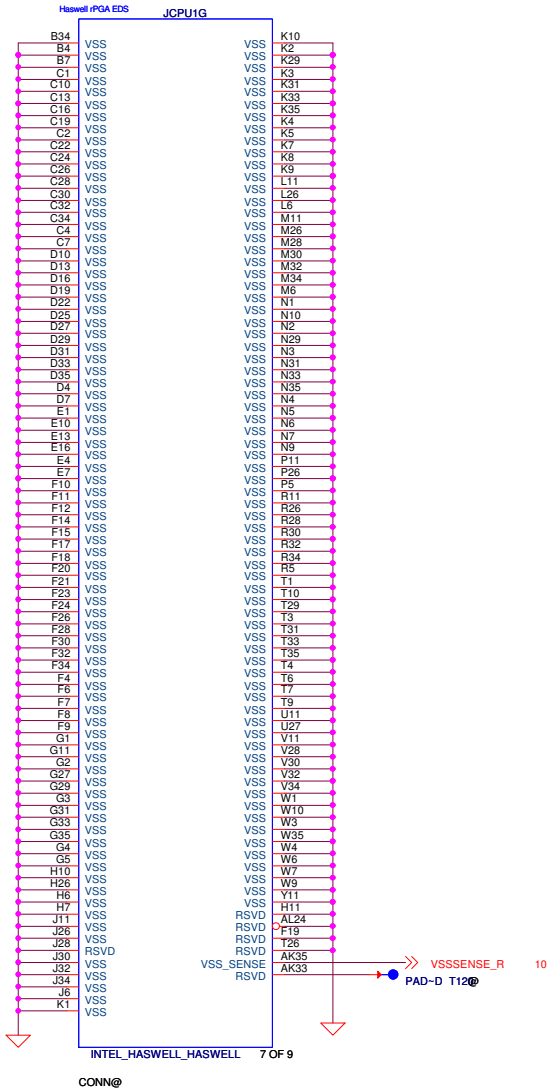
Compal Electronics, Inc.

Title: CPU (6/7) PWR

Size: Custom | Document Number: LA-9332P | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 10 of 56





Security Classification	Compal Secret Data		
Issued Date	2012/05/28	Deciphered Date	2013/05/27

Compal Electronics, Inc.

Title: CPU (7/7) VSS

Size	Document Number	Rev
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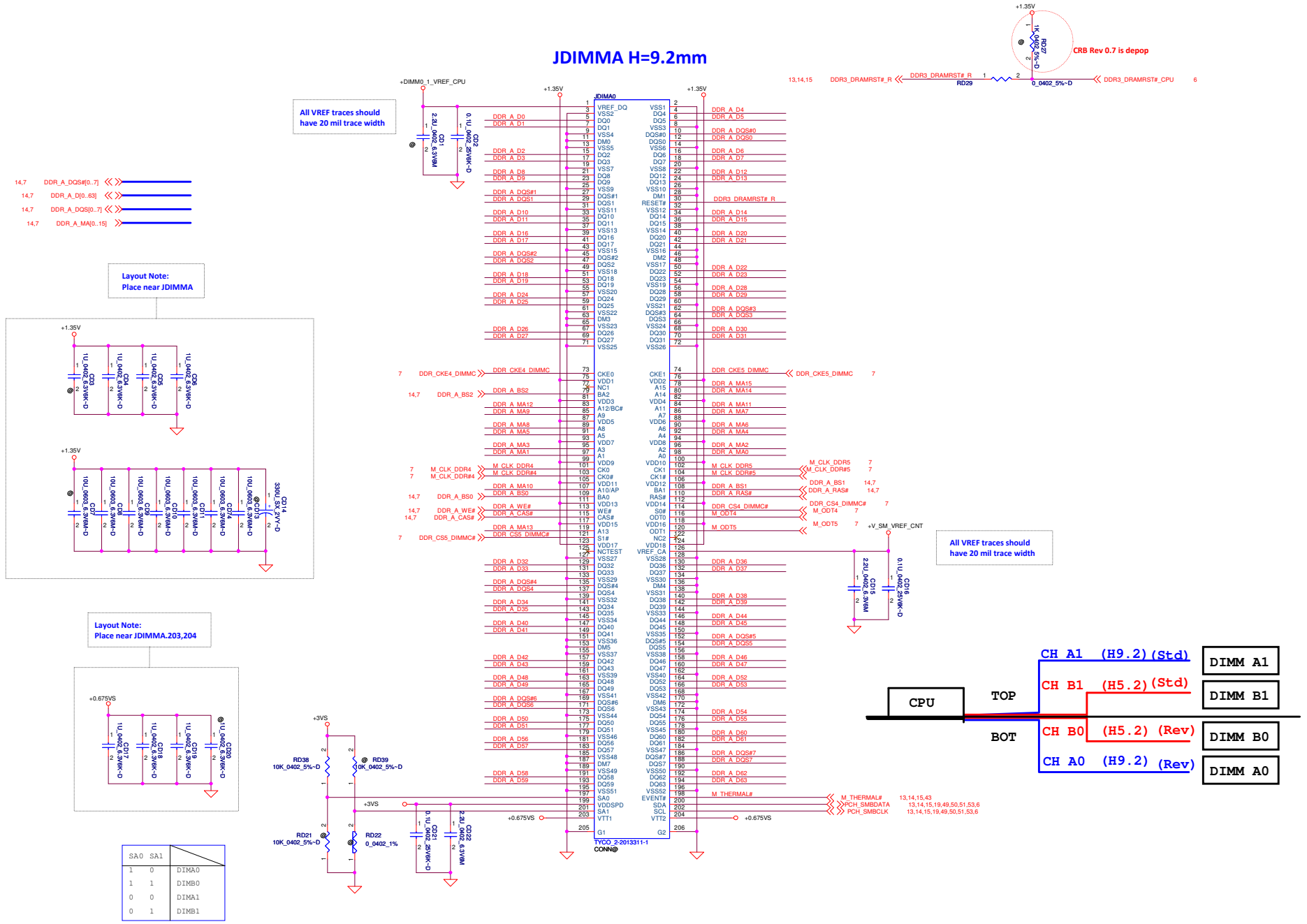
JDIMMA H=9.2mm



SA0	SA1	
1	0	DIMA0
1	1	DIMB0
0	0	DIMA1
0	1	DIMB1

Security Classification	Compal Secret Data		
Issued Date	2012/05/28	Deciphered Date	2013/05/27

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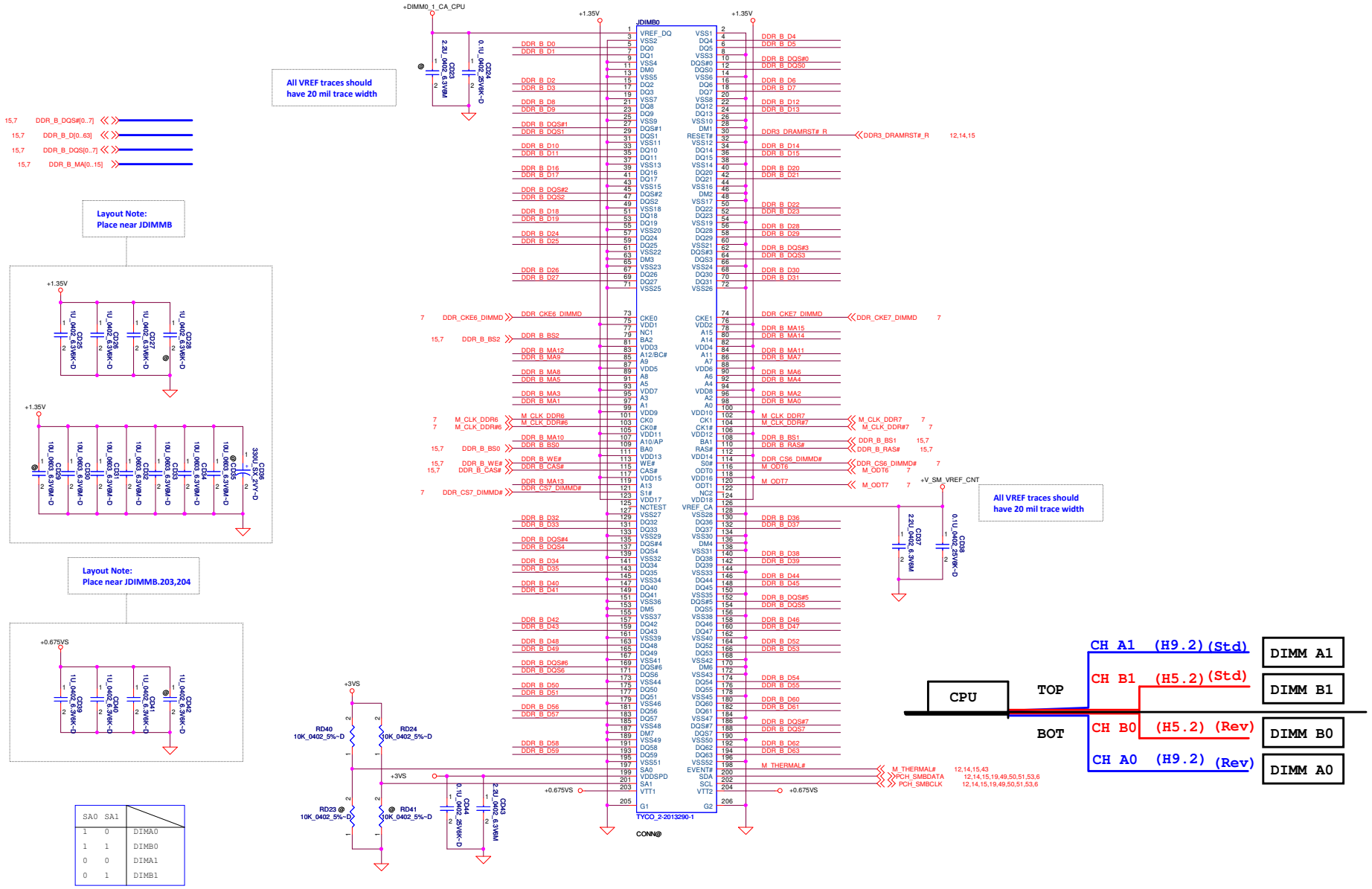
Title: DDRIII DIMMA

Size: Custom | Document Number: LA-9332P | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 12 of 56

JDIMMB H=5.2mm



SA0	SA1	
1	0	DIMA0
1	1	DIMB0
0	0	DIMA1
0	1	DIMB1

Security Classification	Compal Secret Data		
Issued Date	2012/05/28	Deciphered Date	2013/05/27

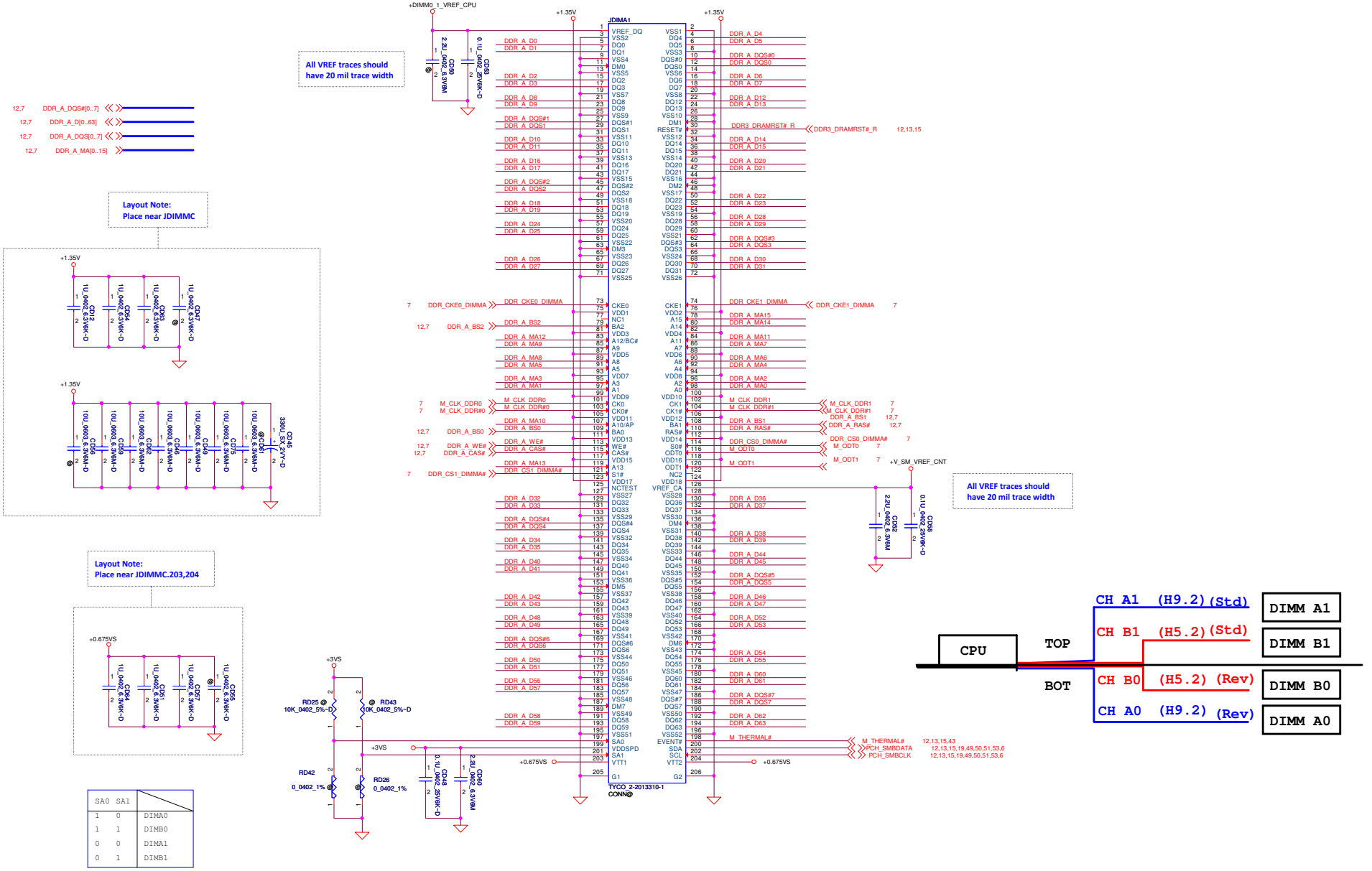
Compal Electronics, Inc.

Title: DDRIII DIMMB

Size: Custom | Document Number: LA-9332P | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 13 of 56

JDIMMC H=9.2mm



SA0	SA1	
1	0	DIMA0
1	1	DIMB0
0	0	DIMA1
0	1	DIMB1

Security Classification	Compal Secret Data		
Issued Date	2012/05/28	Deciphered Date	2013/05/27

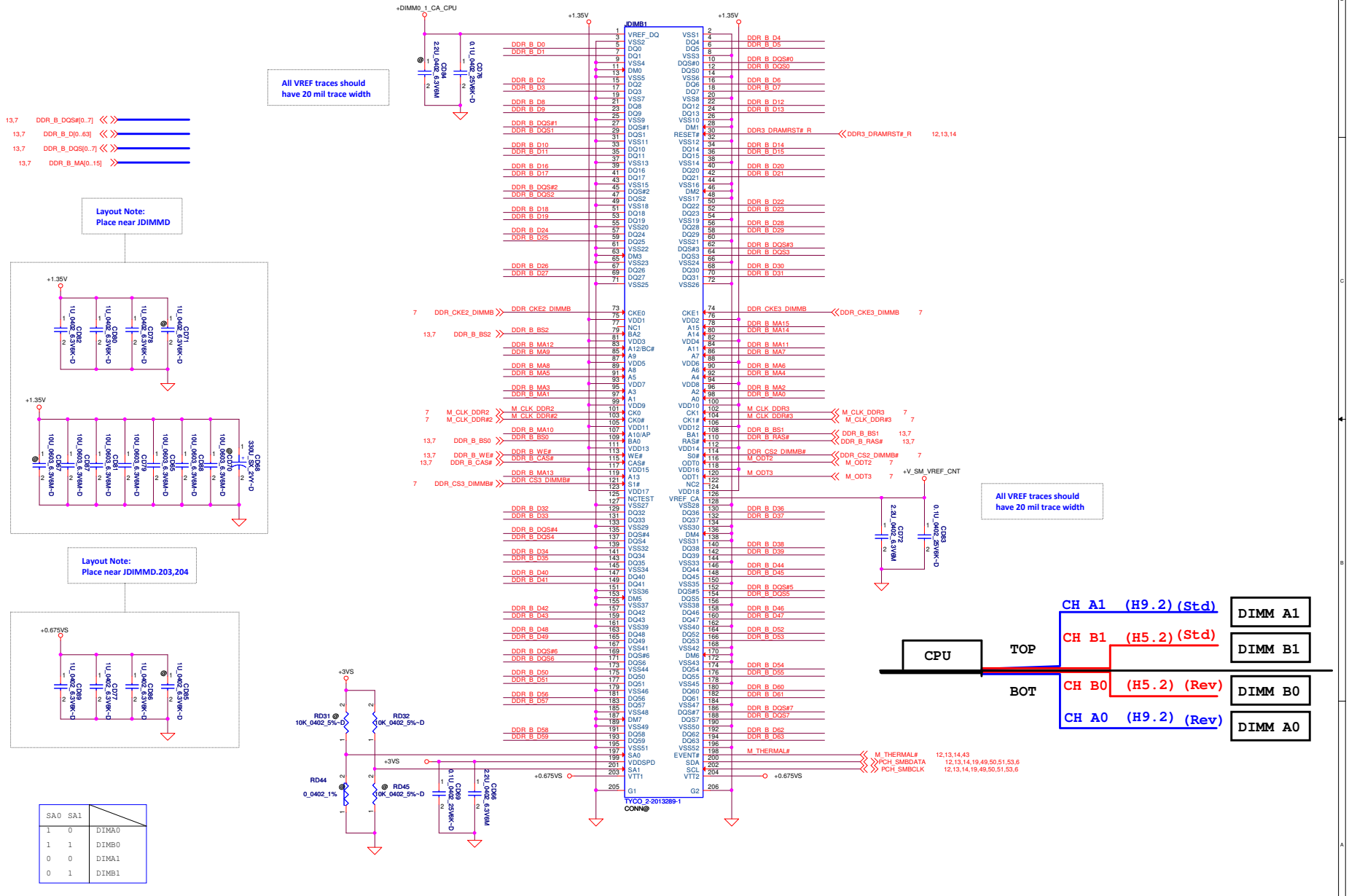
Compal Electronics, Inc.

Title: DDRIII DIMMC

Size: Custom | Document Number: LA-9332P | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 14 of 56

JDIMMD H=5.2mm



SA0	SA1	
1	0	DIMA0
1	1	DIMB0
0	0	DIMA1
0	1	DIMB1

Security Classification	Compal Secret Data		
Issued Date	2012/05/28	Deciphered Date	2013/05/27

Compal Electronics, Inc.

Title: DDRIII DIMMD

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+RTC_CELL

RH38 330K_0402_1%~D — PCH_INTVRMEN — RH39 330K_0402_1%~D

INTVRMEN - INTEGRATED SUS 1.05V VRM ENABLE
High - Enable Internal VRs
Low - Enable External VRs

+3VS — RH35 @ HDA_SPKR 10K_0402_5%~D

+3V_PCH — RH287 @ PCH_AZ_SDOUT 1K_0402_1%~D

NO REBOOT STRAP
DISABLED WHEN LOW (DEFAULT)
ENABLED WHEN HIGH

FLASH DESCRIPTOR SECURITY OVERRIDE
LOW = DESABLED (DEFAULT)
HIGH = ENABLED

+3VS — RH355 @ PCH_GPIO33 100K_0402_5%~D

CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

ME1 @ — SHORT PADS~D — CH5 1U_0402_6.3V6K~D

CMOS1 @ — SHORT PADS~D — CH4 1U_0402_6.3V6K~D — CMOS place near DIMM

CH2 18P_0402_50V8J~D — PCH_RTCX1_R — RH286 0_0402_1% — PCH_RTCX1

YH1 32.768KHZ_12.5PF_Q13FC1350000~D — RH2 10M_0402_5%~D

CH3 18P_0402_50V8J~D — PCH_RTCX2

+RTC_CELL — RH22 20K_0402_5%~D — SRTCRST#

RH11 1M_0402_5%~D — INTRUDER#

PCH_INTVRMEN

RH23 20K_0402_5%~D — PCH_RTCRST#

PCH_AZ_BITCLK

PCH_AZ_SYNC

45 HDA_SPKR — HDA_SPKR

PCH_AZ_RST#

45 PCH_AZ_CODEC_SDIN0 — PCH_AZ_CODEC_SDIN0

43 HDA_SDO — RH50 1K_0402_1%~D — PCH_AZ_SDOUT

PCH_GPIO33

17,31 PCH_mDP_HPD — PCH_mDP_HPD

+3V_PCH — RH288 0_0402_5%~D

+3.3V_ALW_PCH_JTAG

RH59 51_0402_1%~D — PCH_JTAG_TCK

RH44 210_0402_1%~D — PCH_JTAG_TMS

RH45 210_0402_1%~D — PCH_JTAG_TDI

RH46 210_0402_1%~D — PCH_JTAG_TDO

RH289 @ 0_0402_1% — PCH_TP25

T122 PAD~D — PCH_JTAG_RST

T175 PAD~D

RH285 100_0402_1%~D — RH48 100_0402_1%~D — RH47 100_0402_1%~D

HDA_SYNC Isolation Circuit

+5VS — Q8 SSM3K7002FU_SC70-3~D — PCH_AZ_SYNC_Q — PCH_AZ_SYNC — RH31 1M_0402_5%~D

HDA for Codec

45 PCH_AZ_CODEC_SDOUT — RH29 33_0402_5%~D — PCH_AZ_SDOUT

45 PCH_AZ_CODEC_SYNC — RH56 33_0402_5%~D — PCH_AZ_SYNC_Q

45 PCH_AZ_CODEC_RST# — RH27 33_0402_5%~D — PCH_AZ_RST#

45 PCH_AZ_CODEC_BITCLK — RH26 33_0402_5%~D — PCH_AZ_BITCLK

CH101 @ 27P_0402_50V8J~D

+RTC_CELL — W=20mils — CH12 1U_0603_10V6K

U41A LPT_PCH_M_EDS

RTCX1	B5	RTC	
RTCX2	B4		
SRTCRST#	B9		
INTRUDER#	A8		
INTVRMEN	G10		
RTCRST#	D9		
HDA_BCLK	B25	AZALIA	
HDA_SYNC	A22		
SPKR	AL10		
HDA_RST#	C24		
HDA_SDI0	L22		
HDA_SDI1	K22		
HDA_SDI2	G22		
HDA_SDI3	F22		
HDA_SDO	A24		
DOCKEN#/GPIO33	B17		
HDA_DOCK_RST#/GPIO13	C22		
JTAG_TCK	AB3	JTAG	
JTAG_TMS	AD1		
JTAG_TDI	AE2		
JTAG_TDO	AD3		
TP25	F8		
TP22	C26		
TP20	AB6		

LYNXPOINT_BGA695 1 OF 11

SATA_RXN_0 / SATA_RXP_0	BC8 / BE8	SATA_PRX_DTX_N0 / SATA_PRX_DTX_P0	SATA_PRX_DTX_N0 / SATA_PRX_DTX_P0	49 / 49
SATA_TXN_0 / SATA_TXP_0	AW8 / AY8	SATA_PTX_DRX_N0 / SATA_PTX_DRX_P0	SATA_PTX_DRX_N0 / SATA_PTX_DRX_P0	49 / 49
SATA_RXN_1 / SATA_RXP_1	BC10 / BE10	SATA_PRX_DTX_N1 / SATA_PRX_DTX_P1	SATA_PRX_DTX_N1 / SATA_PRX_DTX_P1	49 / 49
SATA_TXN_1 / SATA_TXP_1	AV10 / AW10	SATA_PTX_DRX_N1 / SATA_PTX_DRX_P1	SATA_PTX_DRX_N1 / SATA_PTX_DRX_P1	49 / 49
SATA_RXN_2 / SATA_RXP_2	BB9 / BD9			
SATA_TXN_2 / SATA_TXP_2	AY13 / AW13			
SATA_RXN_3 / SATA_RXP_3	BC12 / BE12			
SATA_TXN_3 / SATA_TXP_3	AR13 / AT13			
SATA_RXN4/PERN1 / SATA_RXP4/PERP1	BD13 / BB13	SATA_ODD_PRX_DTX_N4 / SATA_ODD_PRX_DTX_P4	SATA_ODD_PRX_DTX_N4 / SATA_ODD_PRX_DTX_P4	50 / 50
SATA_TXN4/PETN1 / SATA_TXP4/PETP1	AV15 / AW15	SATA_ODD_PTX_DRX_N4 / SATA_ODD_PTX_DRX_P4	SATA_ODD_PTX_DRX_N4 / SATA_ODD_PTX_DRX_P4	50 / 50
SATA_RXN5/PERN2 / SATA_RXP5/PERP2	BC14 / BE14	MSATA_PRX_DTX_N5 / MSATA_PRX_DTX_P5	MSATA_PRX_DTX_N5 / MSATA_PRX_DTX_P5	50 / 50
SATA_TXN5/PETN2 / SATA_TXP5/PETP2	AP15 / AR15	MSATA_PTX_DRX_N5 / MSATA_PTX_DRX_P5	MSATA_PTX_DRX_N5 / MSATA_PTX_DRX_P5	50 / 50
SATA_RCOMP	AY5	SATA_COMP		
SATALED#	AP3	PCH_SATALED#	PCH_SATALED#	48
SATA0GP/GPIO21	AT1	PCH_GPIO21		
SATA1GP/GPIO19	AU2	BBS_BIT0_R		
SATA_IREF	BD4	SATA_IREF — RH41 0_0402_1% — +1.5VS		
TP9	BA2	PAD~D T161@		
TP8	BB2	PAD~D T155@		

HDD1 (Master)

HDD2 (Slave)

ODD/HDD3 Bay

mSATA

+3VS — PCH_GPIO21 10K_0402_5%~D — RH30

BBS_BIT0_R 4.7K_0402_5%~D — RH52

PCH_SATALED# 10K_0402_5%~D — RH55

SATA Impedance Compensation

+1.5VS — SATA_COMP 7.5K_0402_1%~D — RH40

CAD note:
Place the resistor within 500 mils of the PCH. Avoid routing next to clock pins.

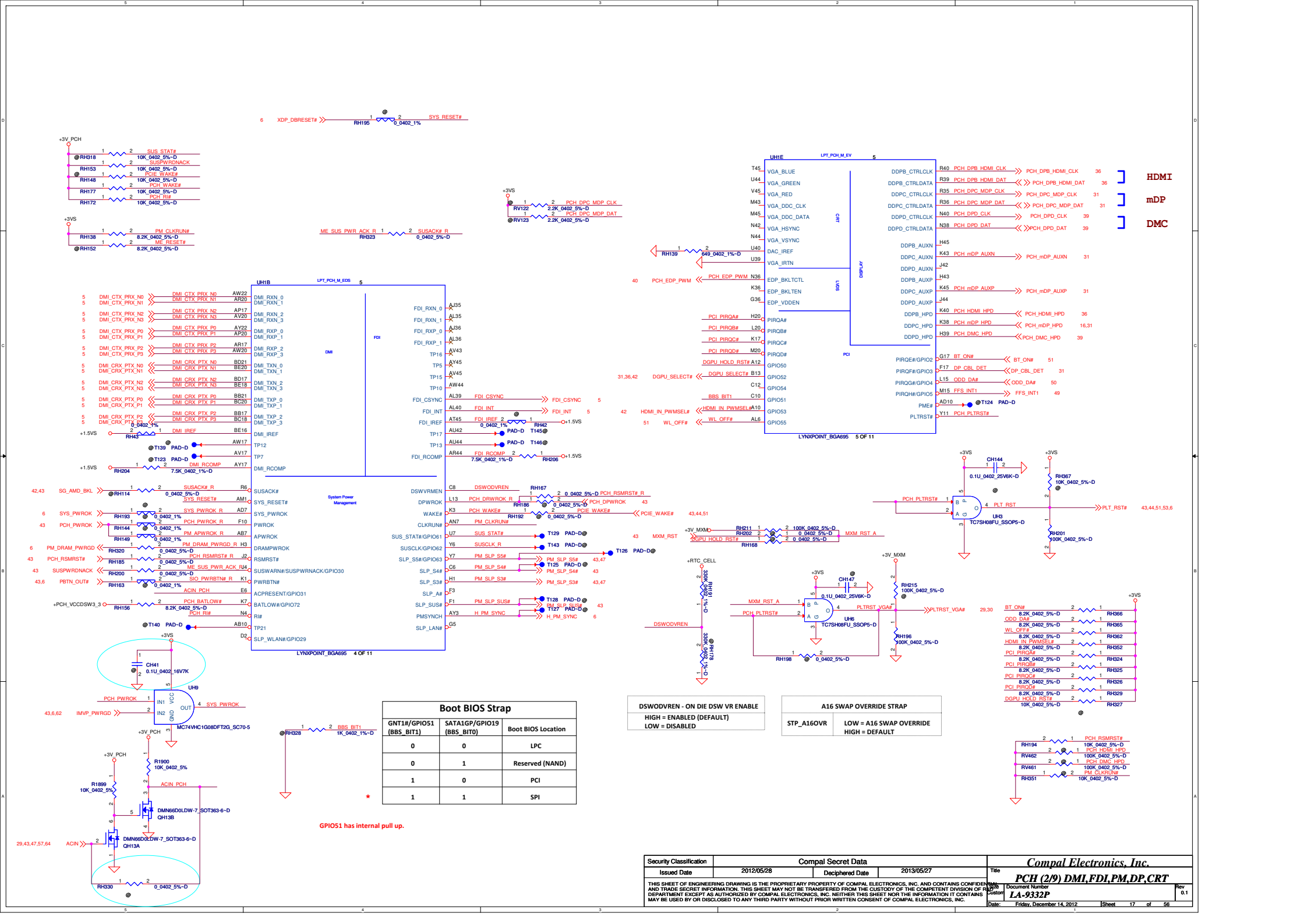
Security Classification	Compal Secret Data		
Issued Date	2012/05/28	Deciphered Date	2013/05/27

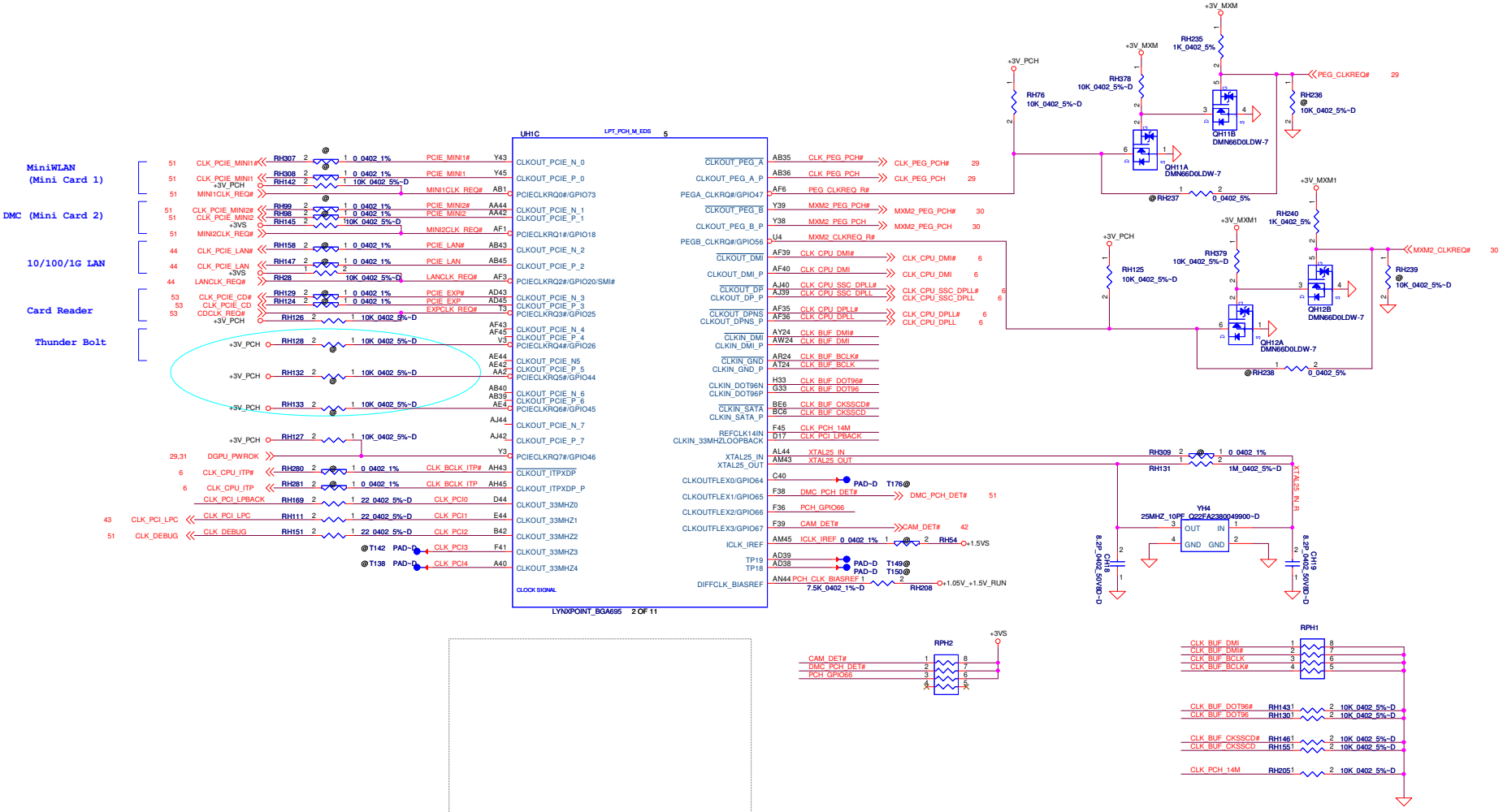
Compal Electronics, Inc.

Title: PCH (1/9) RTC,HDA,SATA,XDP

Size: Custom | Document Number: LA-9332P | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 16 of 56


UH1B
LPT_PCH_M_EDS
LYNXPOINT_BGA695 4 OF 11
UH1E
LPT_PCH_M_EV
LYNXPOINT_BGA695 5 OF 11
HDMI
mDP
DMC
Boot BIOS Strap
GNT1#/GPIO51 (BBS_BIT1)
SATA1GP/GPIO19 (BBS_BIT0)
Boot BIOS Location
0 0 LPC
0 1 Reserved (NAND)
1 0 PCI
1 1 SPI
GPIO51 has internal pull up.
DSWODVREN - ON DIE DSW VR ENABLE
HIGH = ENABLED (DEFAULT)
LOW = DISABLED
A16 SWAP OVERRIDE STRAP
STP_A16OVR
LOW = A16 SWAP OVERRIDE
HIGH = DEFAULT
Security Classification
Compal Secret Data
Issued Date
2012/05/28
Deciphered Date
2013/05/27
Compal Electronics, Inc.
PCH (2/9) DMI,FDI,PM,DP,CRT
Document Number
LA-9332P
Rev
0.1
Date: Friday, December 14, 2012
Sheet 17 of 56



CLOCK TERMINATION for FCIM and need close to PCH

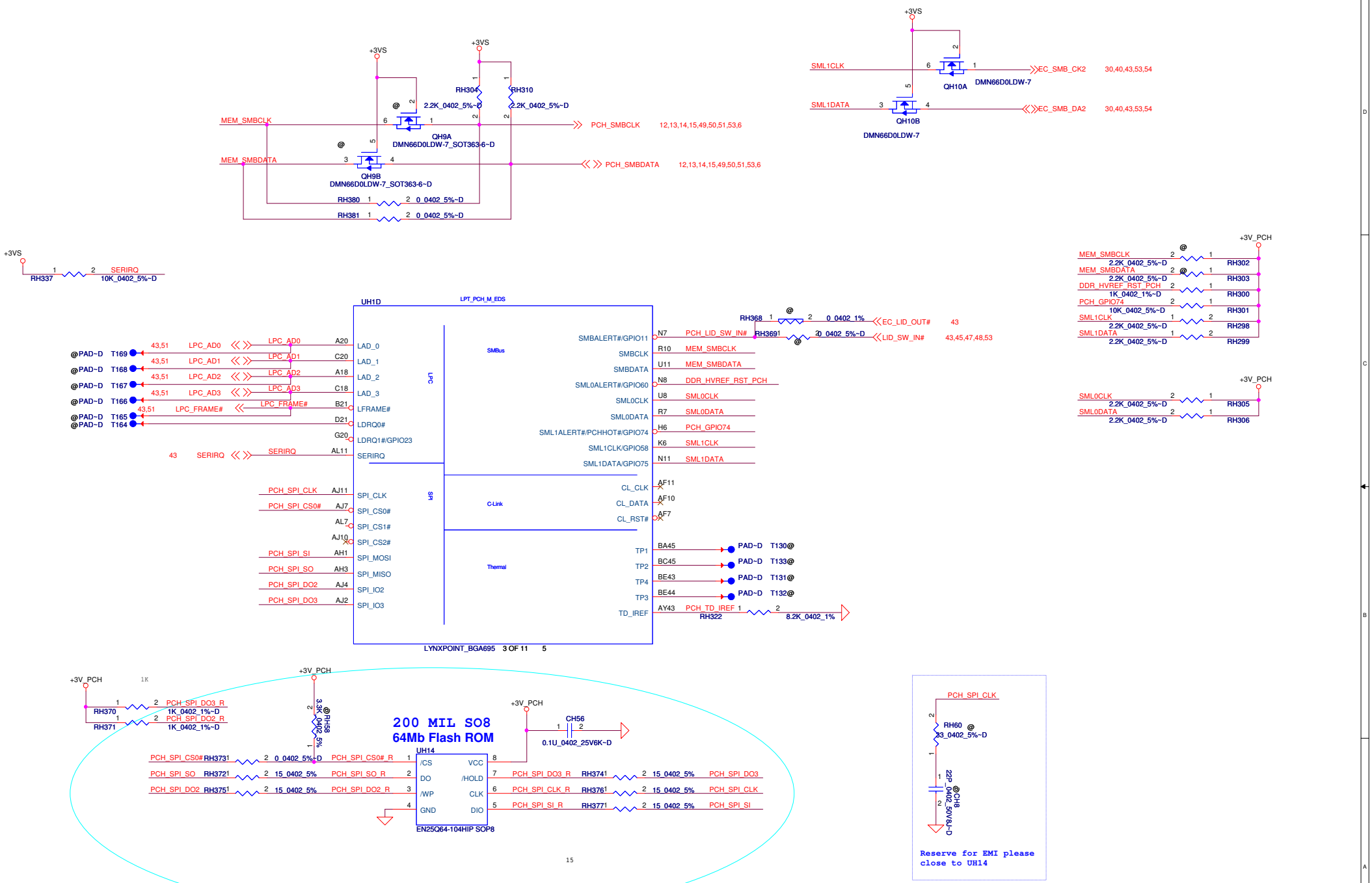
Security Classification	Compal Secret Data		
Issued Date	2012/05/28	Deciphered Date	2013/05/27

Compal Electronics, Inc.

Title: PCH (3/9) CLK

Size: Custom | Document Number: LA-9332P | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 18 of 56

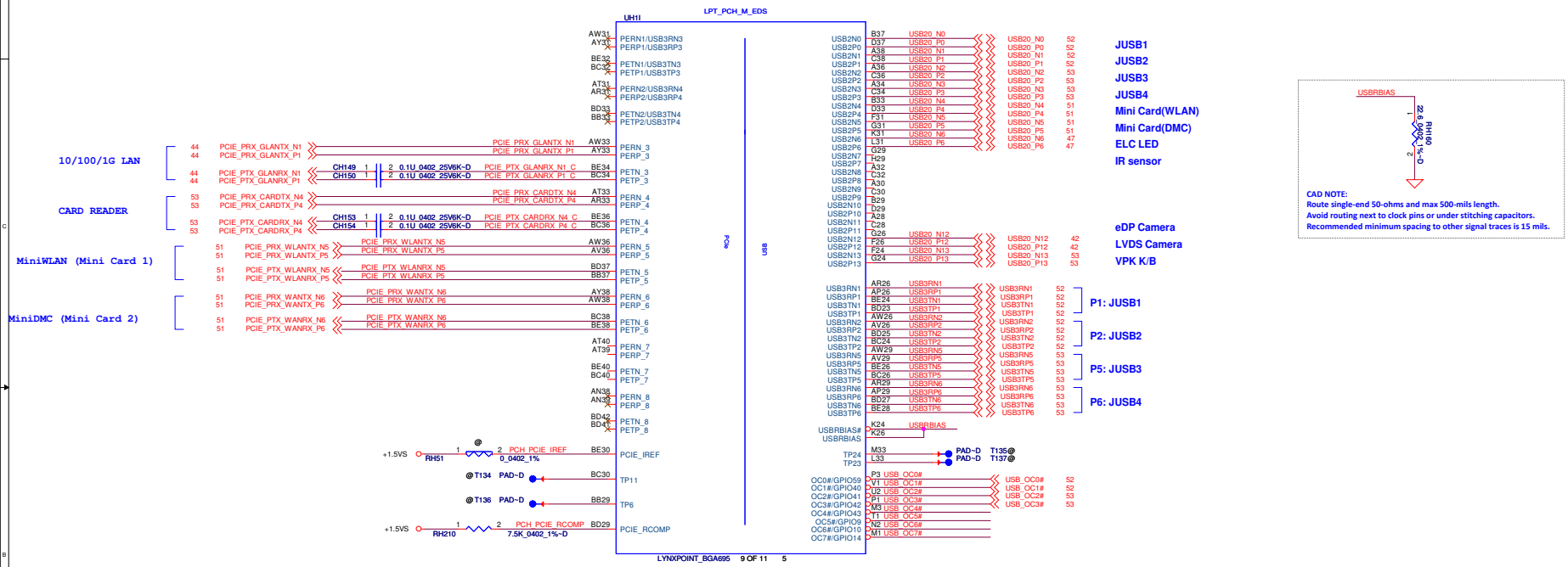


Security Classification	Compal Secret Data		
Issued Date	2012/05/28	Deciphered Date	2013/05/27

Title: **PCH (4/9) SPI, SMBUS,LPC**

Size	Document Number	Rev
Custom	LA-9332P	0.1

Date: Friday, December 14, 2012 Sheet 19 of 56



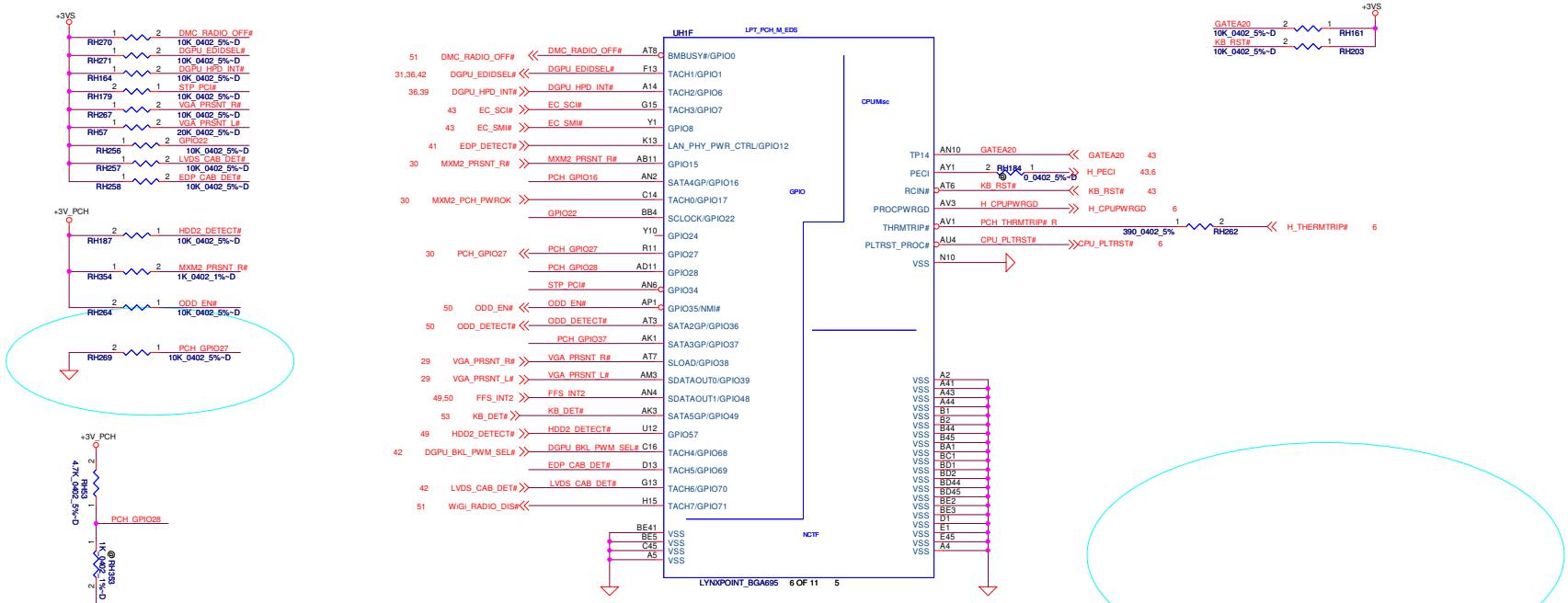
Security Classification	Compal Secret Data		
Issued Date	2012/05/28	Deciphered Date	2013/05/27

Compal Electronics, Inc.

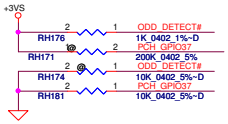
Title: PCH (5/9) PCIE,USB

Size: Custom | Document Number: LA-9332P | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 20 of 56



Config	GPIO16,49
USB X4,PCIEX8,SATAX6	11
* USB X6,PCIEX8,SATAX4	01



SATA2GP/GPIO36 , SATA3GP/GPIO37 SAMPLED AT RISING EDGE OF PWROK.
WEAK INTERNAL PULL-DOWN.(WEAK INTERNAL PULL-DOWN IS DISABLED AFTER PLRST_N DE-ASSERTS).
NOTE: THIS SIGNAL SHOLD NOT BE PULLED HIGH WHEN STRAP IS SAMPLED.

Fixed Signals				Muxed Signals		Fixed Signals						Muxed Signals		Fixed Signals			
USB3 1	USB3 2	USB3 5	USB3 6	PCIE 1 (00)	PCIE 2 (00)	PCIE 3	PCIE 4	PCIE 5	PCIE 6	PCIE 7	PCIE 8	SATA 4 (00)	SATA 5 (00)	SATA 0	SATA 1	SATA 2	SATA 3
				USB3 3 (01)	USB3 4 (01)							PCIE 1 (01)	PCIE 2 (01)				

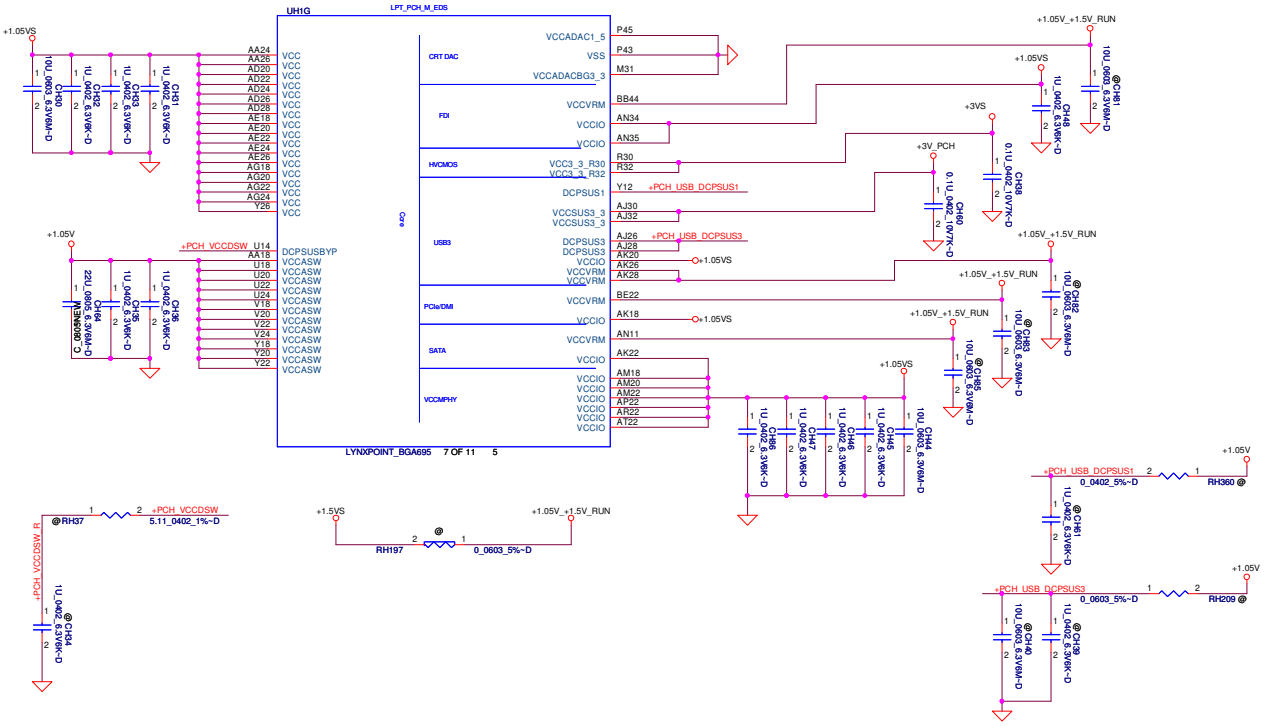
Security Classification	Compal Secret Data		
Issued Date	2012/05/28	Deciphered Date	2013/05/27

Compal Electronics, Inc.

Title: PCH (6/9) GPIO,MISC,NTFC

Size: Custom | Document Number: LA-9332P | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 21 of 56



PCH Power Rail Table

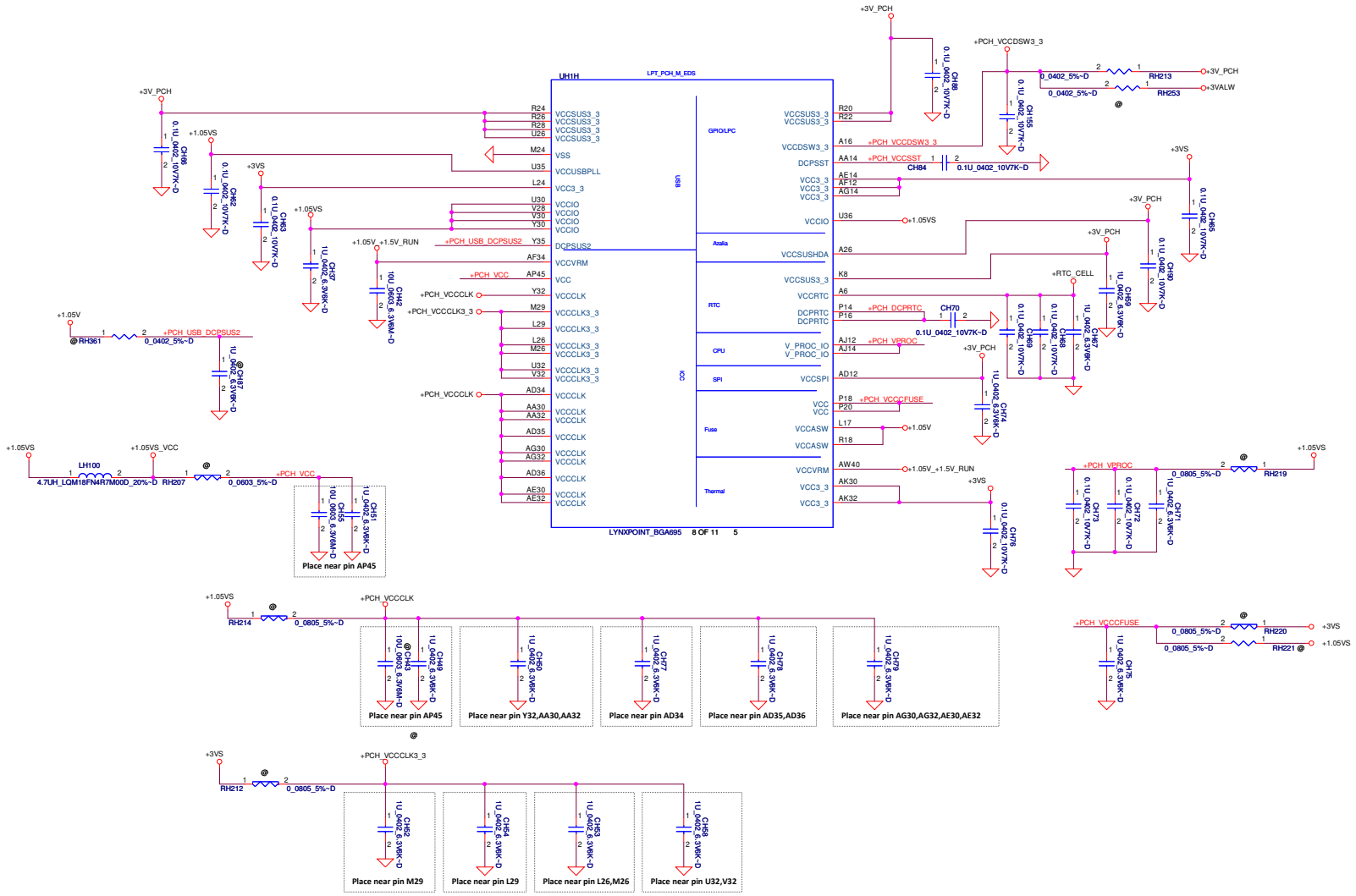
Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCADAC1_5	1.5V	0.070 A
VCCADAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK3_3	3.3V	0.055 A
VCCVRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A

Compal Electronics, Inc.

Title: PCH (7/9) Power

Size: Custom | Document Number: LA-9332P | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 22 of 56



Security Classification	Compal Secret Data		
Issued Date	2012/05/28	Deciphered Date	2013/05/27

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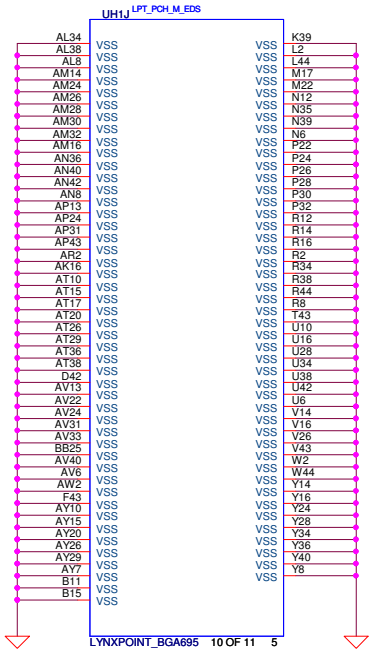
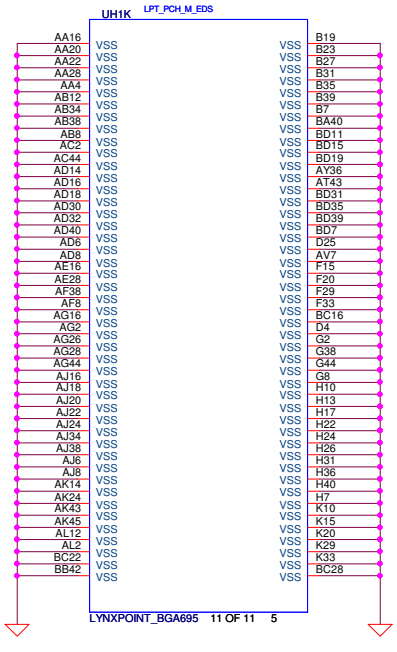
Compal Electronics, Inc.

Title: PCH (8/9) Power

Size: Custom | Document Number: LA-9332P | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 23 of 56





Security Classification	Compal Secret Data		
Issued Date	2012/05/28	Deciphered Date	2013/05/27

Compal Electronics, Inc.

Title: PCH (9/9) Power

Size	Document Number	Rev
Custom	LA-9332P	0.1

Date: Friday, December 14, 2012 Sheet 24 of 56

Security Classification	Compal Secret Data		
Issued Date	2010/08/25	Deciphered Date	2012/08/25

Compal Electronics, Inc.

Title: Cactus (1/4) DP/PCIE

Size	Document Number	Rev
Custom	LA-9332P	0.1

Date: Friday, December 14, 2012 | Sheet 25 of 56

Security Classification	Compal Secret Data		
Issued Date	2010/08/25	Deciphered Date	2012/08/25

Compal Electronics, Inc.

Title: Cactus (2/4) CIO

Size	Document Number	Rev
C	LA-9332P	0,1

Date: Friday, December 14, 2012 | Sheet 26 of 56

Security Classification	Compal Secret Data		
Issued Date	2010/08/25	Deciphered Date	2012/08/25

Compal Electronics, Inc.

Title: Cactus (3/4) PWR/VSS/DC-DC

Size	Document Number	Rev
Custom	LA-9332P	0.1

Date: Friday, December 14, 2012 | Sheet 27 of 56

Security Classification	Compal Secret Data		
Issued Date	2010/08/25	Deciphered Date	2012/08/25

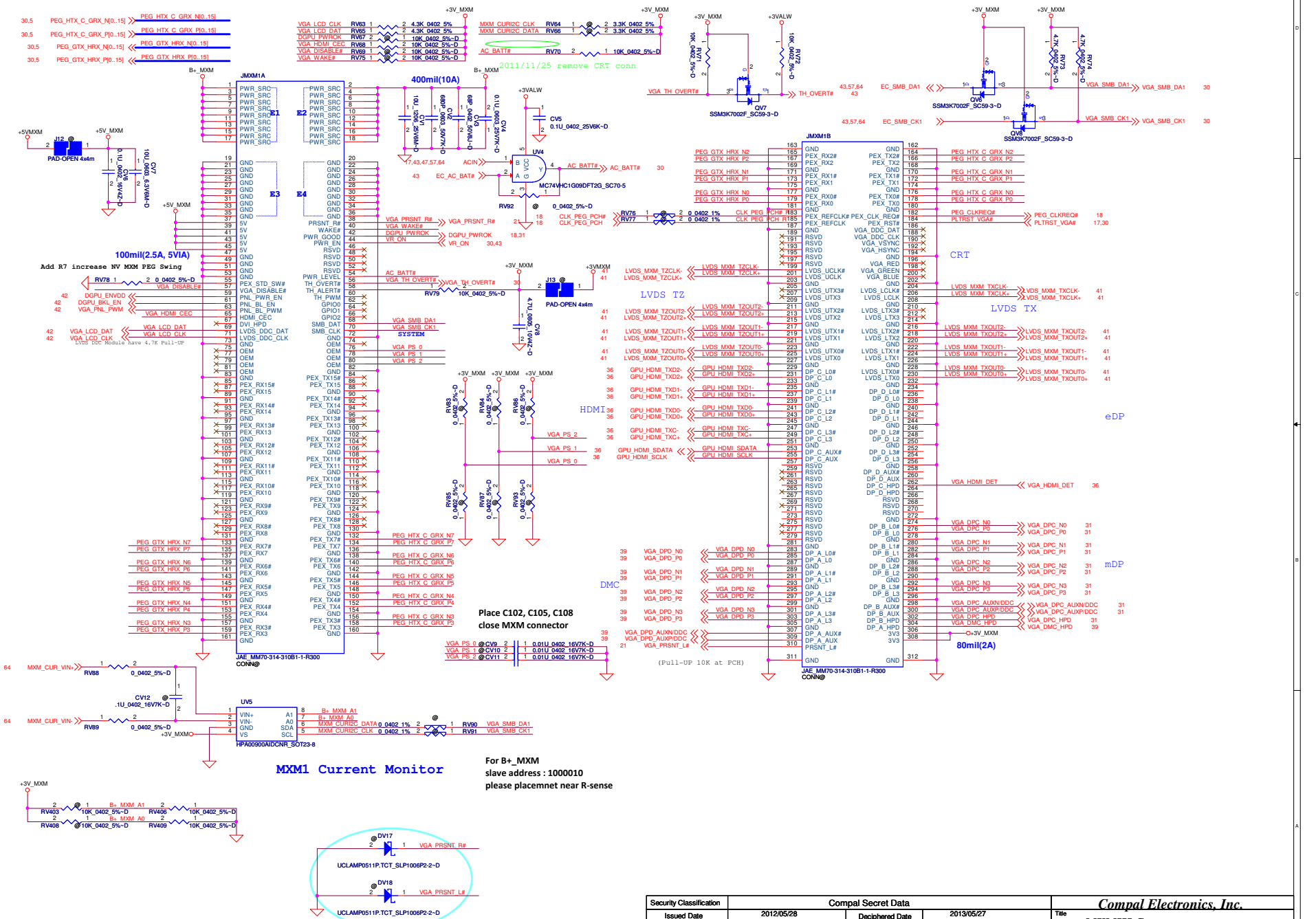
Compal Electronics, Inc.

Title

A

Size	Document Number	Rev
Custom	LA-9332P	0.1

Date: Friday, December 14, 2012 Sheet 28 of 56



Security Classification	Compal Secret Data		
Issued Date	2012/05/28	Deciphered Date	2013/05/27

Compal Electronics, Inc.

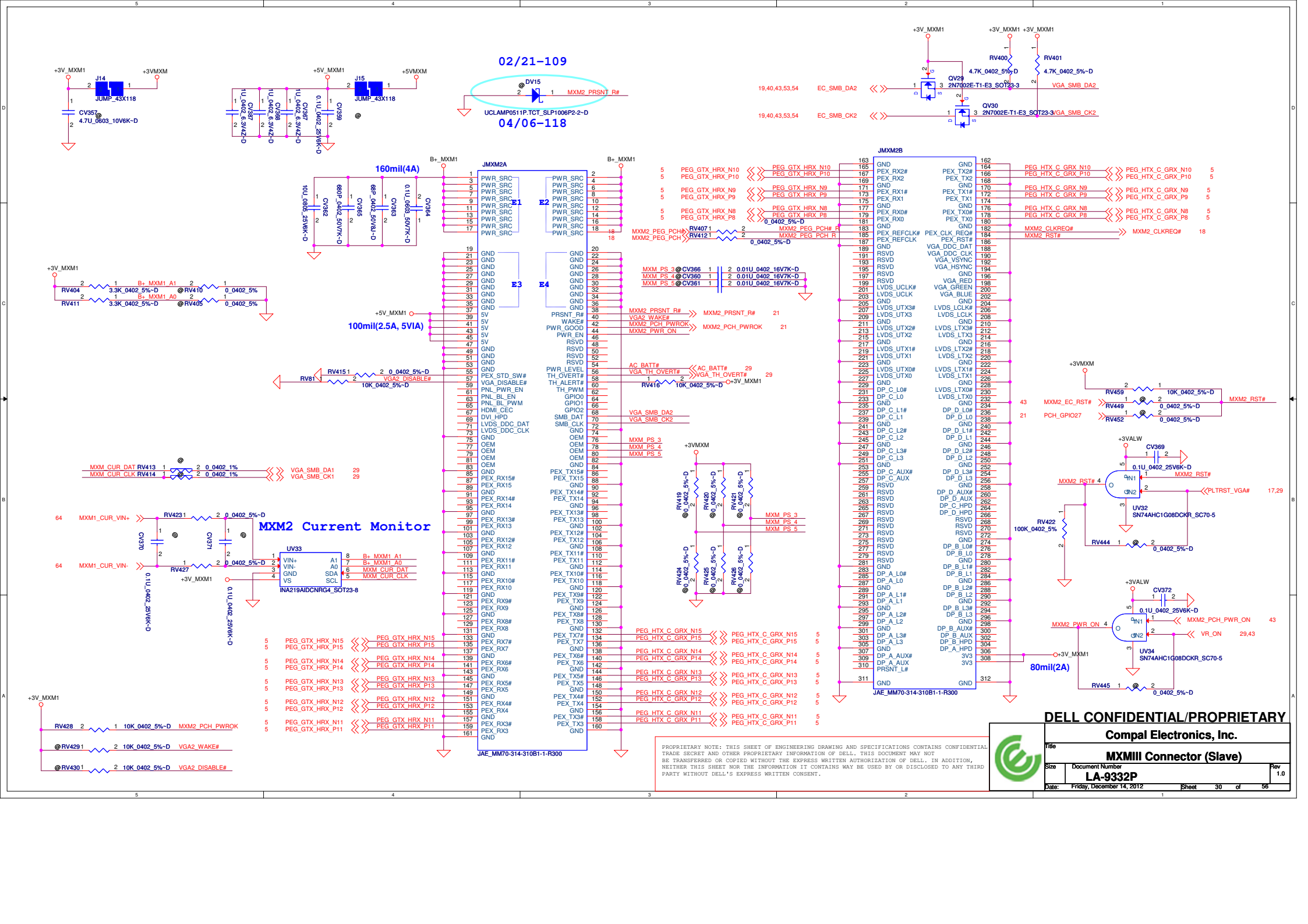
Title: MXMIII Connector

Size: Custom | Document Number: LA-9332P | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 29 of 56

02/21-109

04/06-118



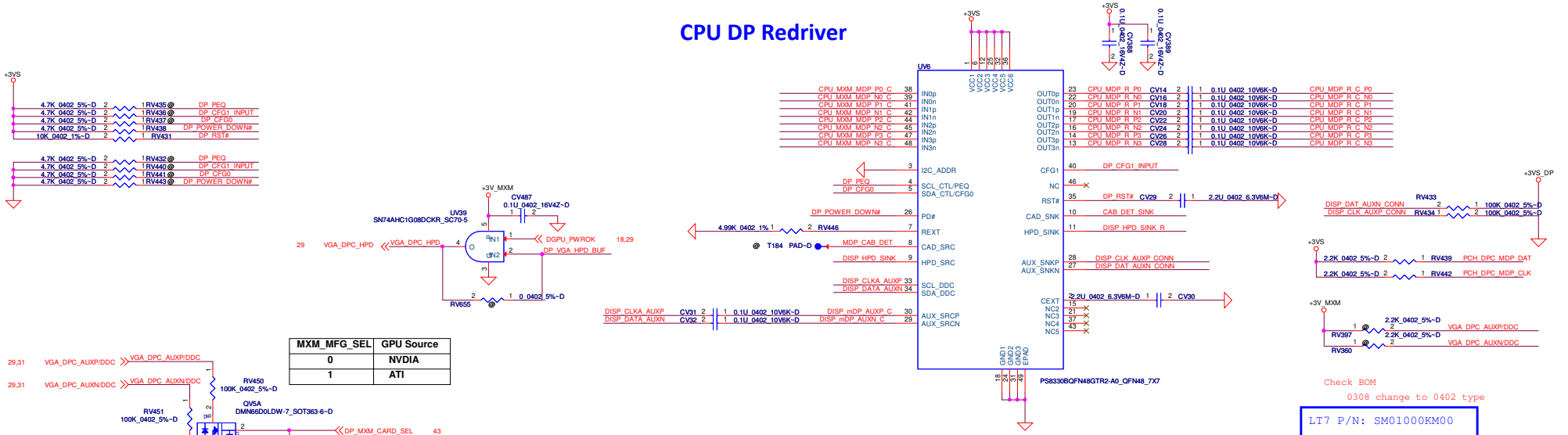
Compal Electronics, Inc.

Title: MXMIII Connector (Slave)

Size: | Document Number: LA-9332P | Rev: 1.0

Date: Friday, December 14, 2012 | Sheet 30 of 56

CPU DP Redriver



MXM_MFG_SEL	GPU Source
0	NVDIA
1	ATI

Check BOM

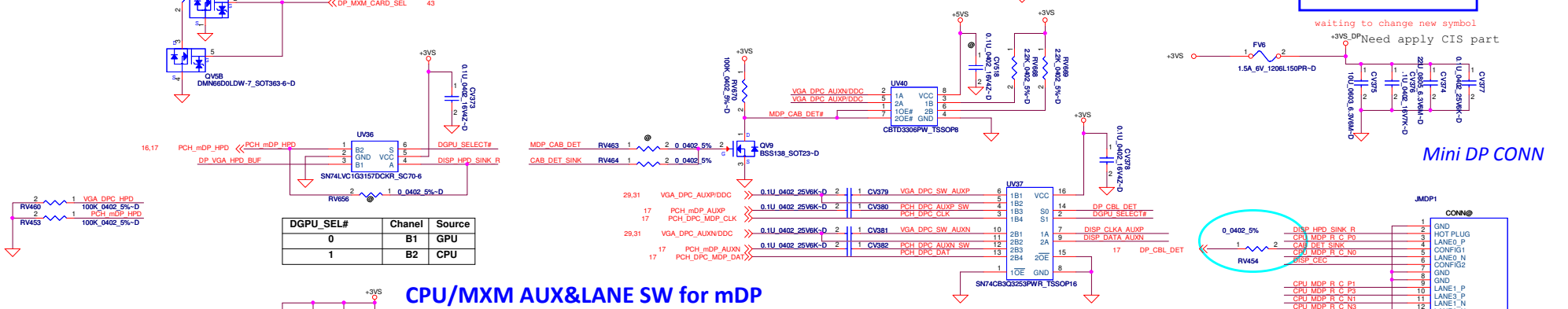
0308 change to 0402 type

LT7 P/N: SM01000KM00

waiting to change new symbol

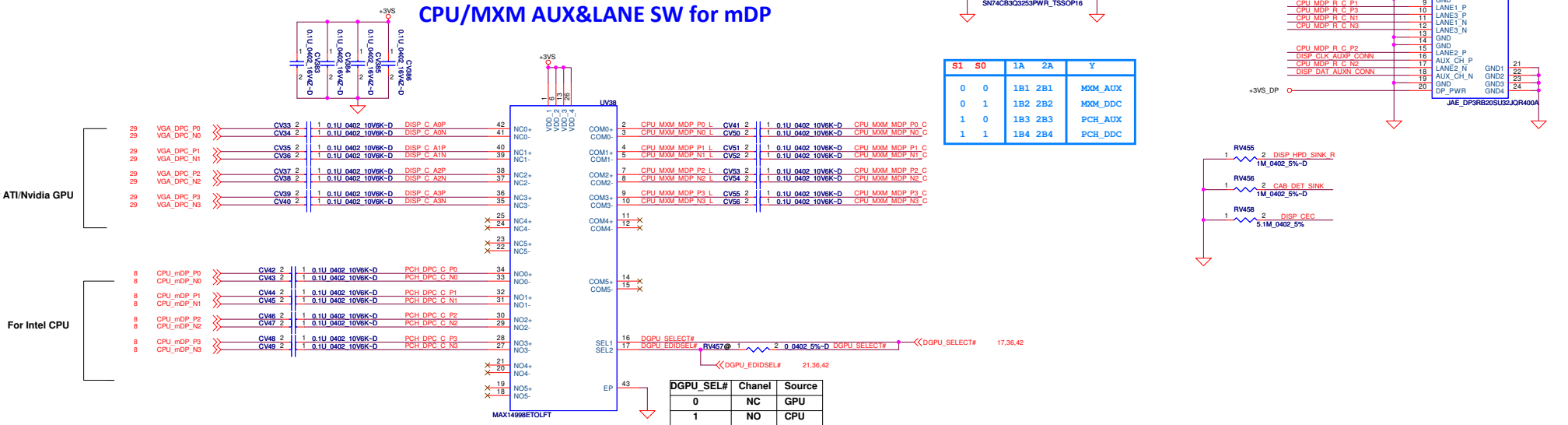
Need apply CIS part

Mini DP CONN



DGPU_SEL#	Chanel	Source
0	B1	GPU
1	B2	CPU

CPU/MXM AUX&LANE SW for mDP



S1	S0	1A 2A	Y
0	0	1B1 2B1	MXM_AUX
0	1	1B2 2B2	MXM_DDC
1	0	1B3 2B3	PCH_AUX
1	1	1B4 2B4	PCH_DDC

DGPU_SEL#	Chanel	Source
0	NC	GPU
1	NO	CPU

Security Classification	Compal Secret Data		
Issued Date	2012/05/14	Deciphered Date	2013/05/13

Compal Electronics, Inc.

Title: Mini DP/Thunder Bolt power

Size: Custom | Document Number: LA-9332P | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 31 of 56

Security Classification	Compal Secret Data		
Issued Date	2012/05/14	Deciphered Date	2013/05/13

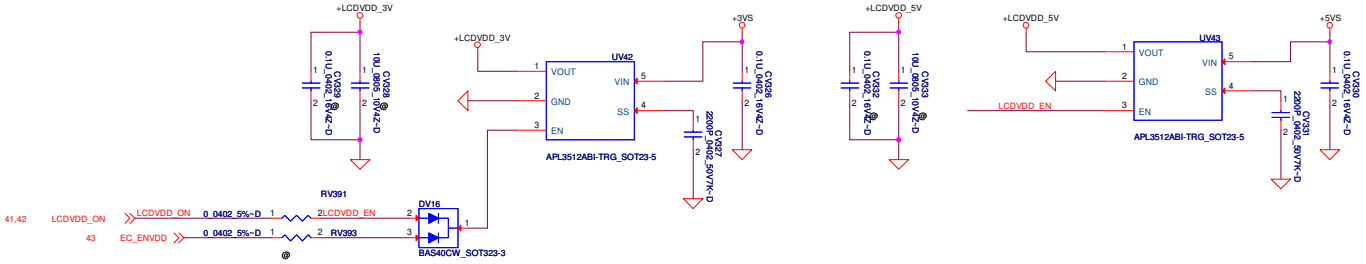
Compal Electronics, Inc.

Title: ***eDP SW-CPU & MXM***

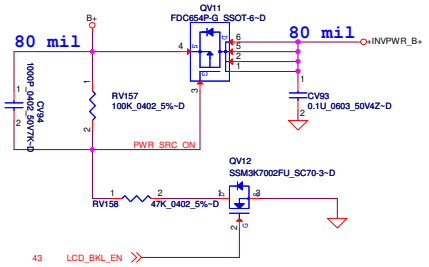
Size: Custom | Document Number: ***LA-9332P*** | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 32 of 56

LCD POWER



Back light power



FDC654P: P CHANNAL

Panel backlight power control by EC

Security Classification	Compal Secret Data		
Issued Date	2012/05/14	Deciphered Date	2013/05/13

Compal Electronics, Inc.

Title: eDP SW-eDP CONN

Size: Custom | Document Number: LA-9332P | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 33 of 56

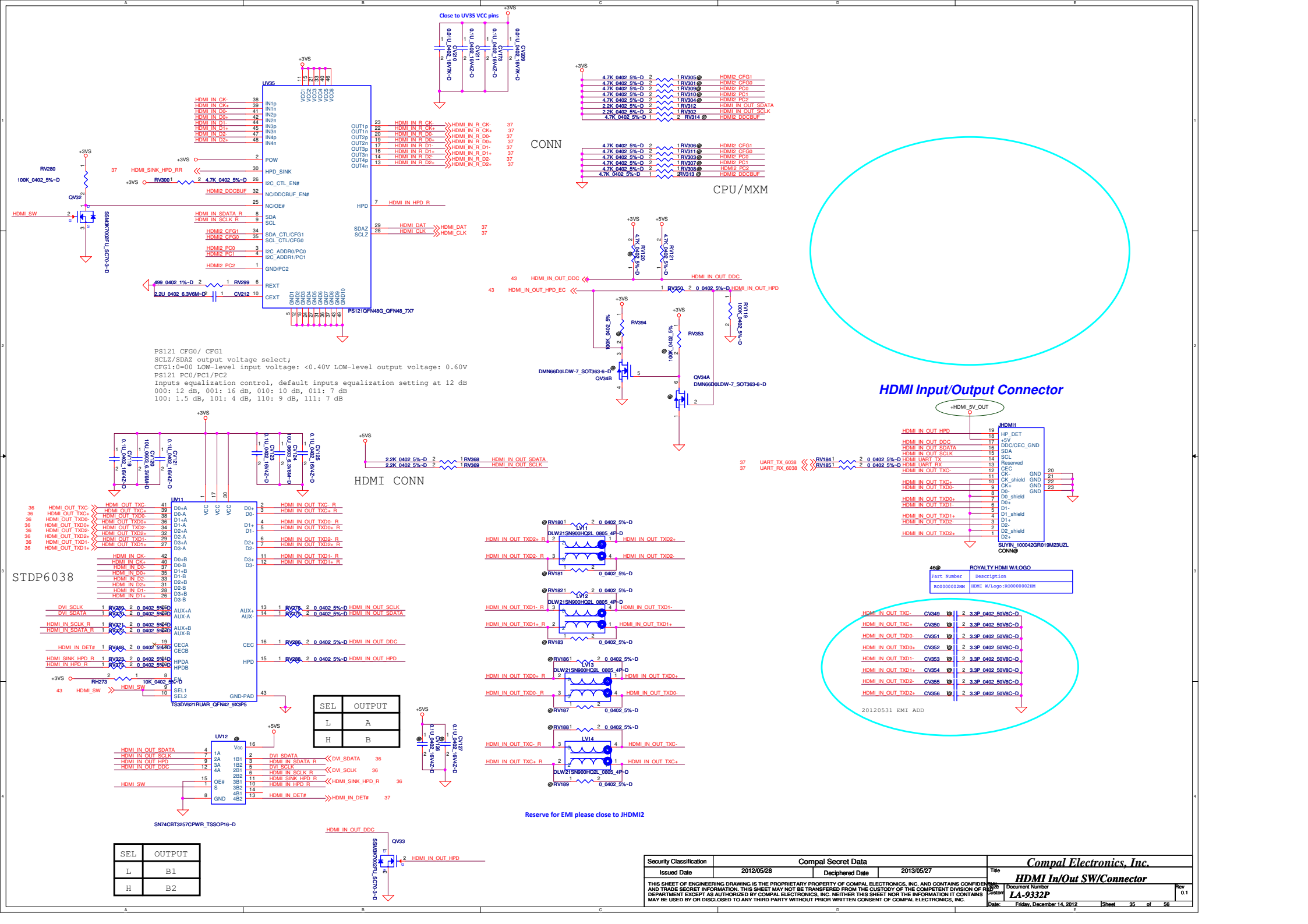
Security Classification	Compal Secret Data		
Issued Date	2012/05/14	Deciphered Date	2013/05/13

Title

reserved

Size	Document Number	Rev
Custom	*LA-9332P*	0.1

Date: Friday, December 14, 2012 Sheet 34 of 56



SEL	OUTPUT
L	A
H	B

SEL	OUTPUT
L	B1
H	B2

Part Number	Description
RO0000002HM	HDMI W/LOGO:RO0000002HM

Security Classification	Compal Secret Data		
Issued Date	2012/05/28	Deciphered Date	2013/05/27

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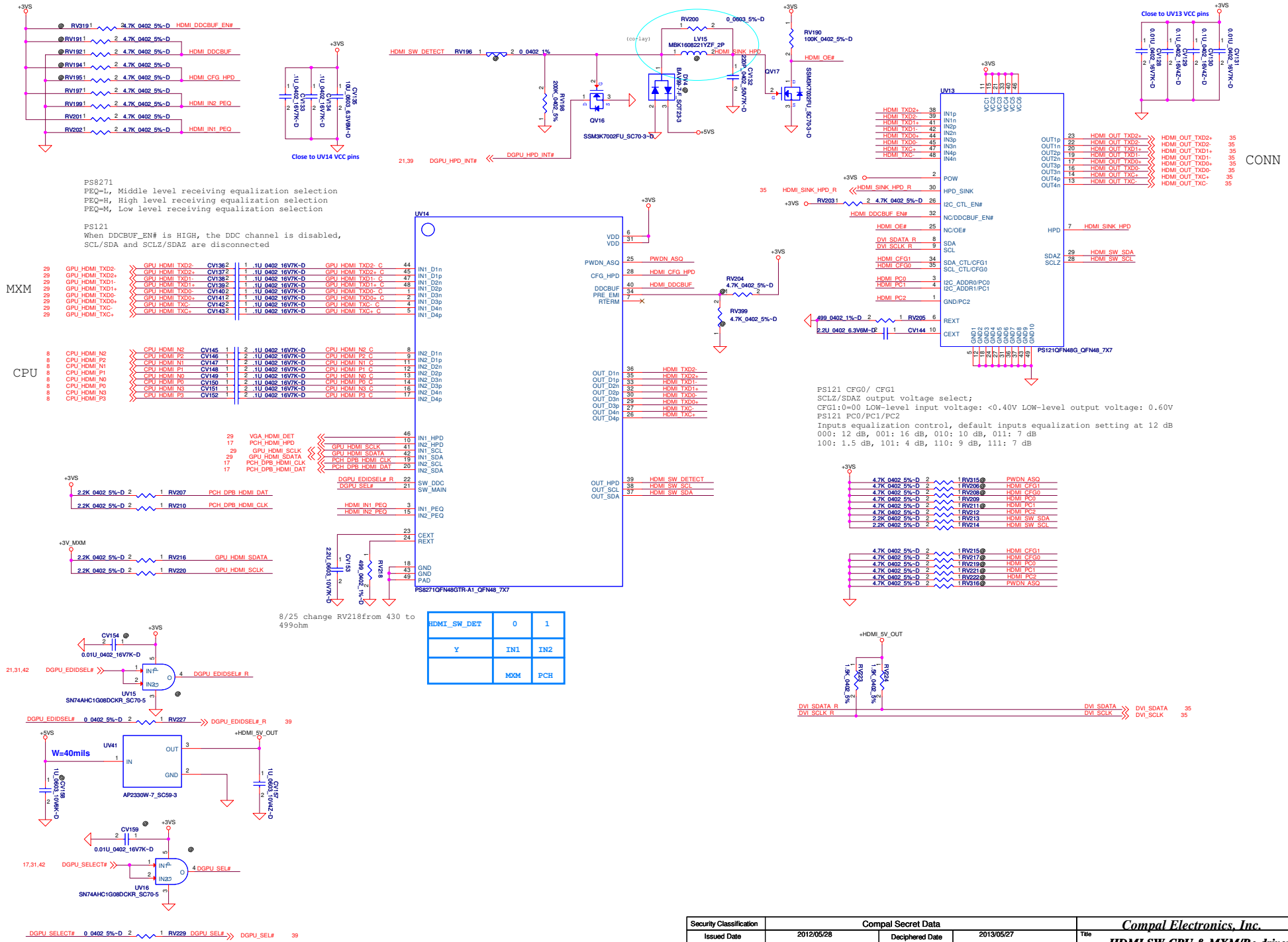
Compal Electronics, Inc.

Title: HDMI In/Out SW/Connector

Size: Custom | Document Number: LA-9332P | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 35 of 56



HDMI_SW_DET	0	1
Y	IN1	IN2
	MXM	PCH

Security Classification	Compal Secret Data		
Issued Date	2012/05/28	Deciphered Date	2013/05/27

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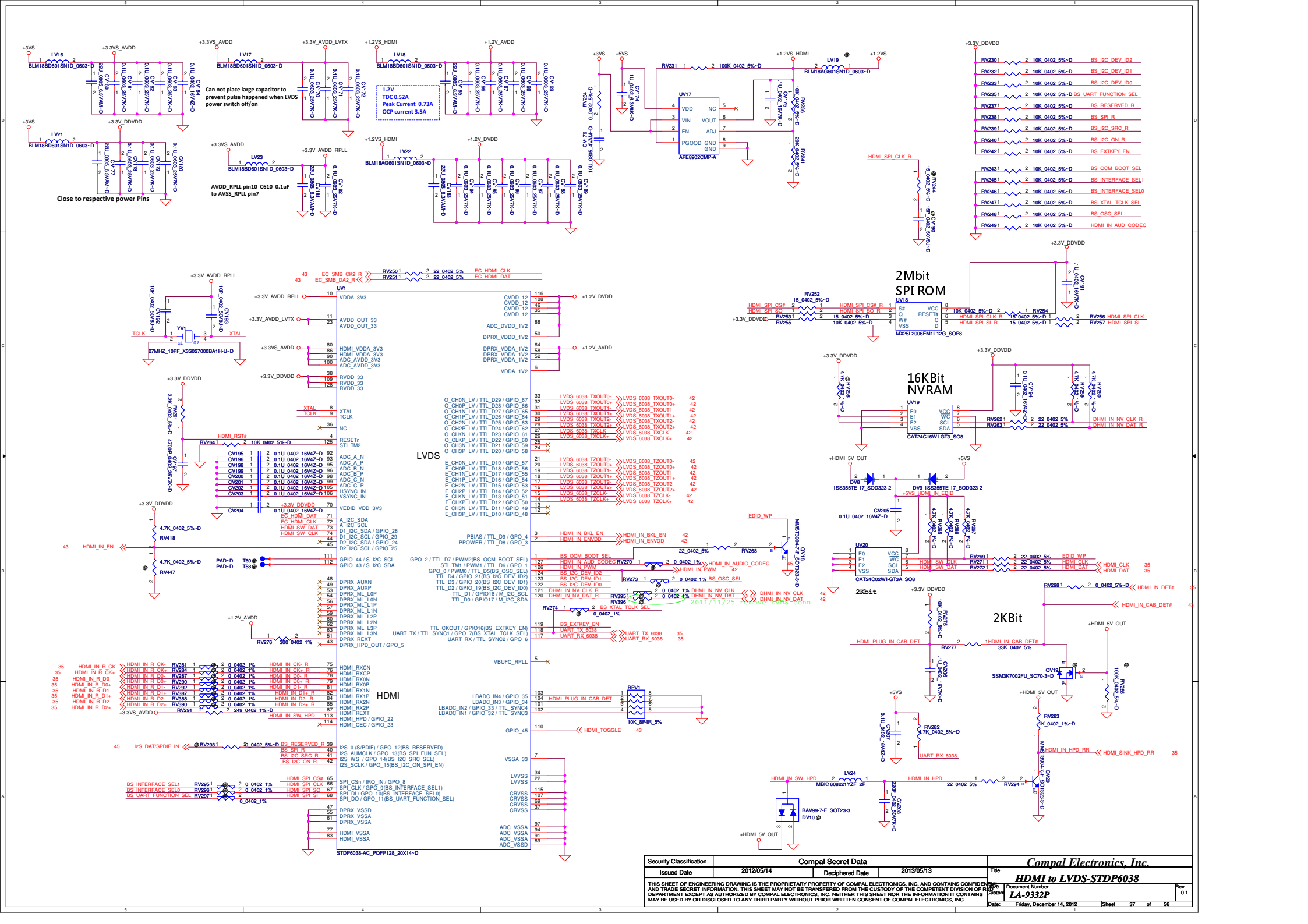
Compal Electronics, Inc.

Title: HDMI SW-CPU & MXM/Re-driver

Size: Custom | Document Number: LA-9332P | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 36 of 56



Security Classification	Compal Secret Data		
Issued Date	2012/05/14	Deciphered Date	2013/05/13

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Compal Electronics, Inc.

Title: HDMI to LVDS-STDP6038

Size: Custom | Document Number: LA-9332P | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 37 of 56

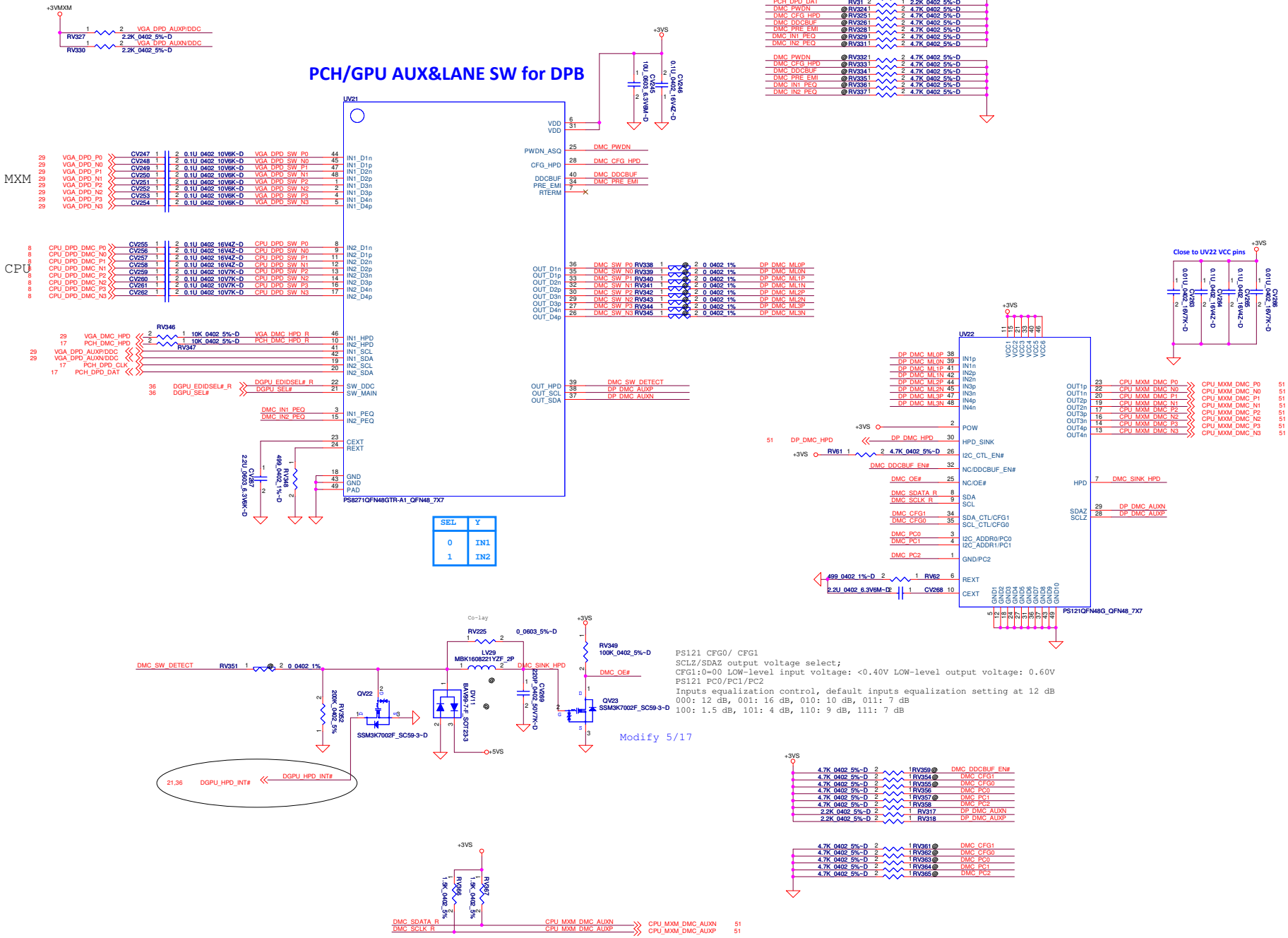
Security Classification	Compal Secret Data		
Issued Date	2012/05/14	Deciphered Date	2013/05/13

Compal Electronics, Inc.

Title: ***LVDS to eDP-STDP4028***

Size: Custom	Document Number: ***LA-9332P***	Rev: 0.1
Date: Friday, December 14, 2012	Sheet 38 of 56	

PCH/GPU AUX&LANE SW for DPB



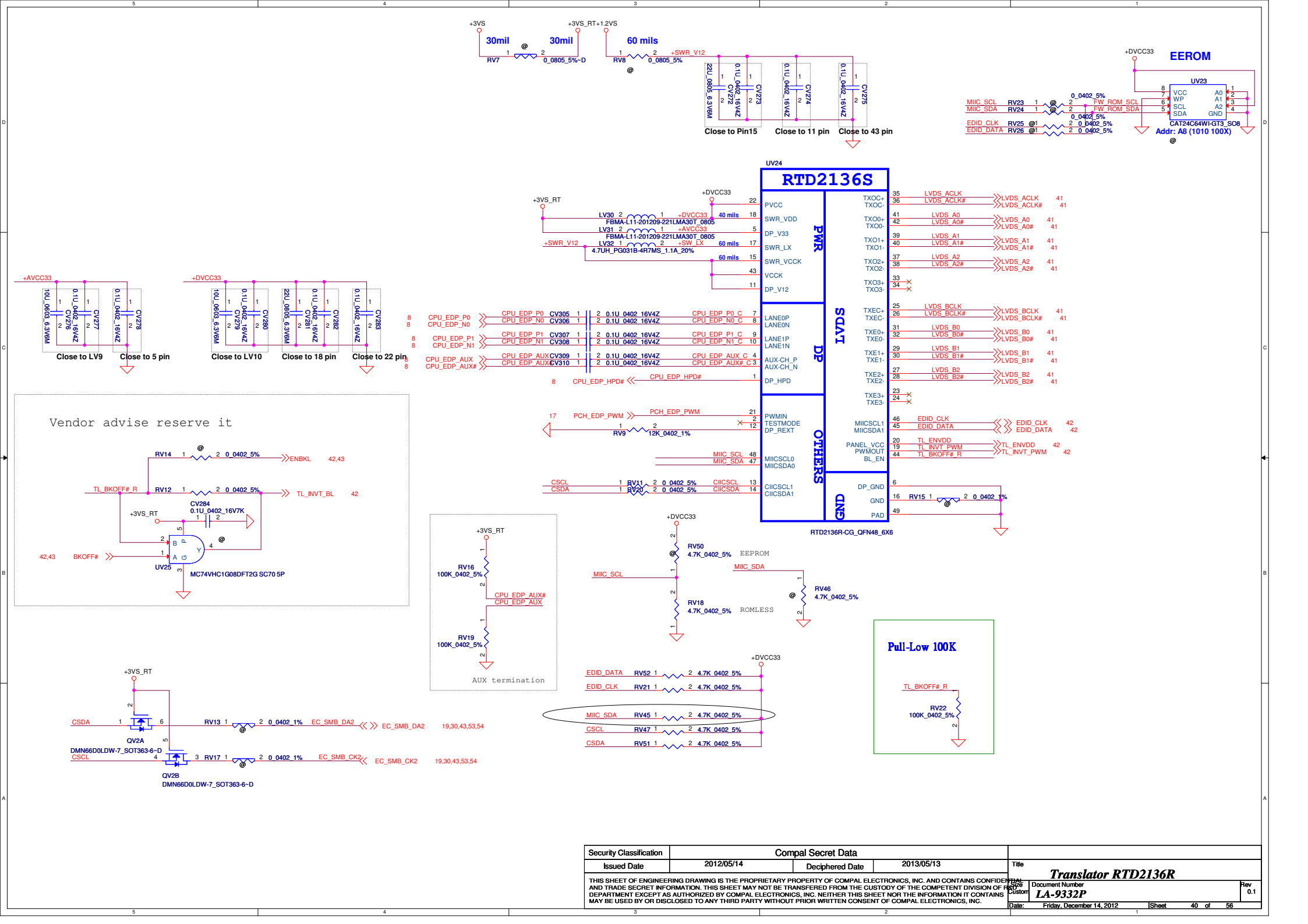
Security Classification	Compal Secret Data		
Issued Date	2012/05/14	Deciphered Date	2013/05/13

Compal Electronics, Inc.

Title: DP SW for DMC

Size: Custom | Document Number: LA-9332P | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 39 of 56



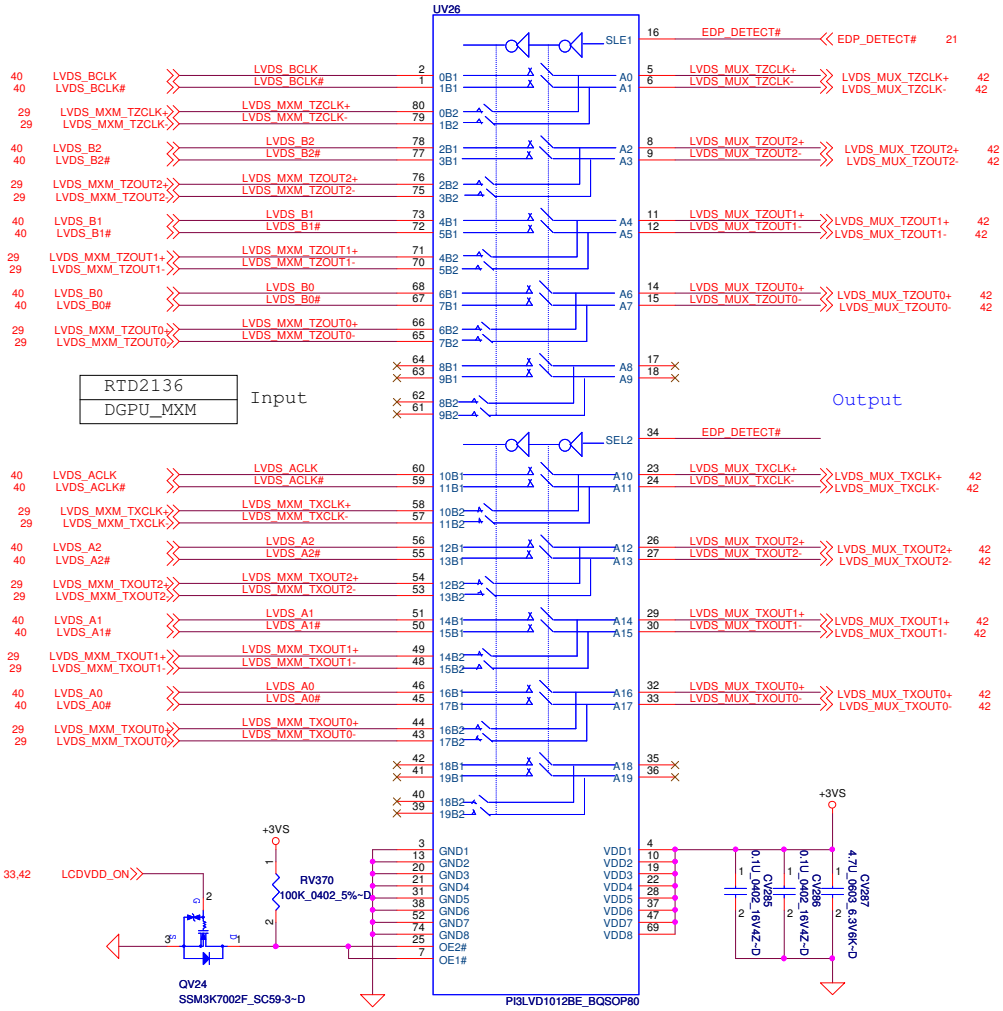
Security Classification	Compal Secret Data		
Issued Date	2012/05/14	Deciphered Date	2013/05/13

Title: *Translator RTD2136R*

Size	Document Number	Rev
Custom	*LA-9332P*	0.1

Date: Friday, December 14, 2012 Sheet 40 of 56

STDP6038 SW STDP4028 PCH/GPU AUX for LVDS



SEL	Y
L	RTD2136
H	DGPU_MXM

Security Classification	Compal Secret Data		
Issued Date	2012/05/14	Deciphered Date	2013/05/13

Compal Electronics, Inc.

Title: LVDS SW- 1 to 2 & GPU/PCH

Size: Custom | Document Number: LA-9332P | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 41 of 56

LCD Backlight Selector

S1	S0	1A 2A	Y
0	0	1B1 2B1	HDMI IN (D)
0	1	1B2 2B2	DSC
1	0	1B3 2B3	HDMI IN (I)
1	1	1B4 2B4	UMA

LCD DDC Selector

S1	S0	1A 2A	Y
0	0	1B1 2B1	HDMI IN (D)
0	1	1B2 2B2	DSC
1	0	1B3 2B3	HDMI IN (I)
1	1	1B4 2B4	UMA

PCH/GPU MUX & 6038 MUX SW for LVDS

CPU/MXM(MUX) Input
HDMI IN(6038)

SEL	Y
L	B1
H	B2

Output

S1	S0	1A 2A	Y
0	0	1B1 2B1	HDMI IN
0	1	1B2 2B2	DSC
1	0	1B3 2B3	HDMI IN
1	1	1B4 2B4	UMA

EN_CAM control circuit

Close to JLVDS1

LVDS Conn.

Link Done

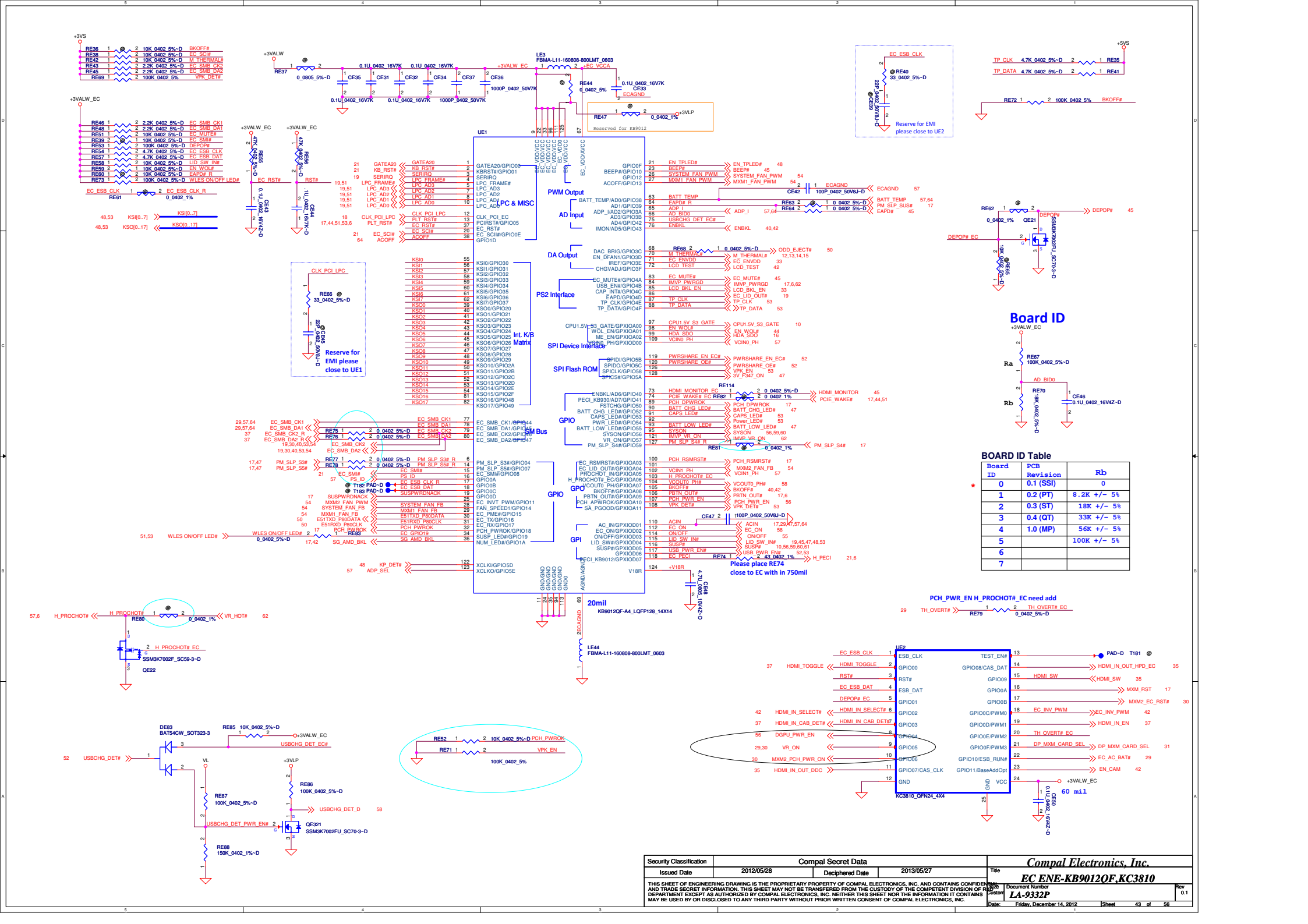
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: LVDS SW- 6038/SYSTEM & CONN

Size | Document Number: LA-9332P | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 42 of 56



Security Classification	Compal Secret Data		
Issued Date	2012/05/28	Deciphered Date	2013/05/27

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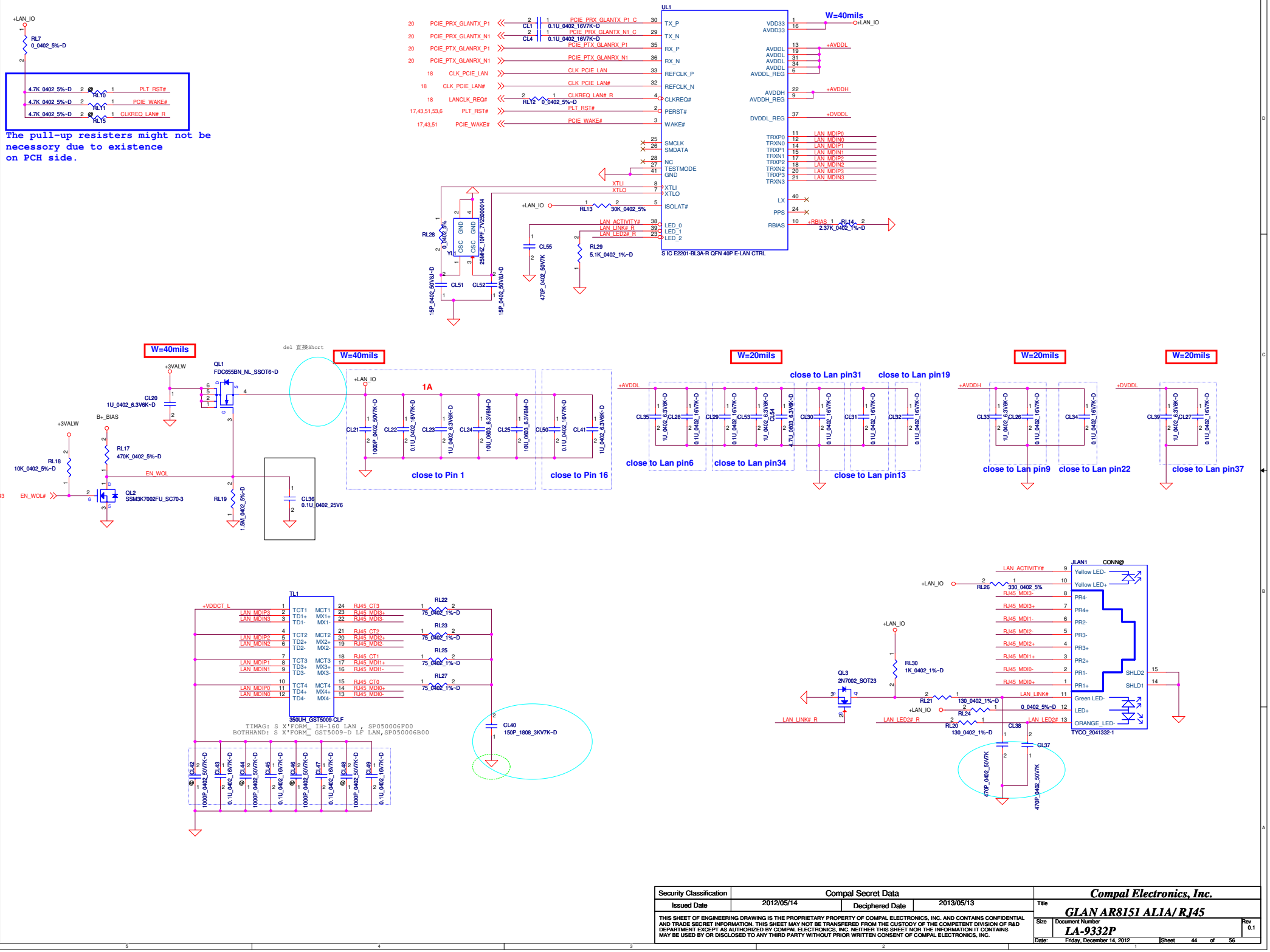
Compal Electronics, Inc.

Title: EC ENE-KB9012QF,KC3810

Size: Custom | Document Number: LA-9332P | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 43 of 56



Security Classification	Compal Secret Data		
Issued Date	2012/05/14	Deciphered Date	2013/05/13

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Compal Electronics, Inc.

Title: **GLAN AR8151 AL1A/ RJ45**

Size	Document Number	Rev
	LA-9332P	0.1

Date: Friday, December 14, 2012 | Sheet 44 of 56

Close to Pin39

Place under codec

Place closely to Pin 33.

Add for solve pop noise and detect issue

JACK_PLUG Delay cricutis

Reserve for cancel Delay cricutis

Need double check this pin

ESD

GND AGND

ALC3661-CG_MQFN48_6X6-D

Security Classification	Compal Secret Data		
Issued Date	2012/05/14	Deciphered Date	2013/05/13

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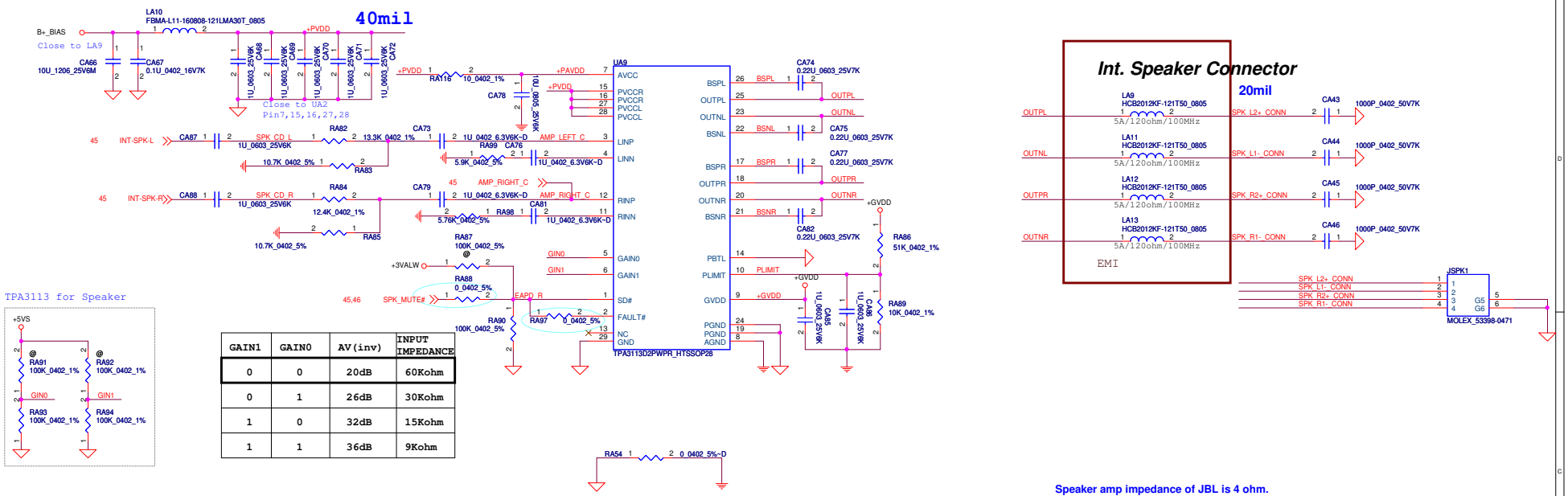
Compal Electronics, Inc.

Title: HD Audio ALC3661

Size: Custom | Document Number: LA-9332P | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 45 of 56



GAIN1	GAIN0	AV(inv)	INPUT IMPEDANCE
0	0	20dB	60Kohm
0	1	26dB	30Kohm
1	0	32dB	15Kohm
1	1	36dB	9Kohm

Woofer Amp Table

G1	G0	GAIN(dB)	Input Impedance (Rl) (Kohm)
0	0	20	60
0	1	26	30
1	**0**	**32**	**15**
1	1	36	9

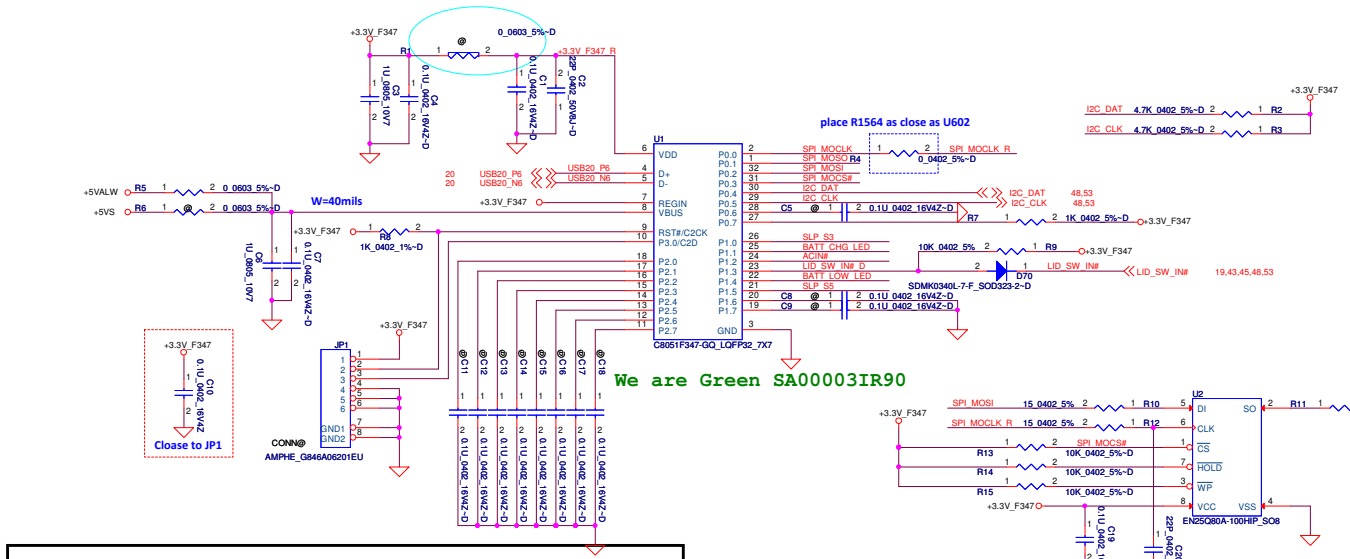
Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

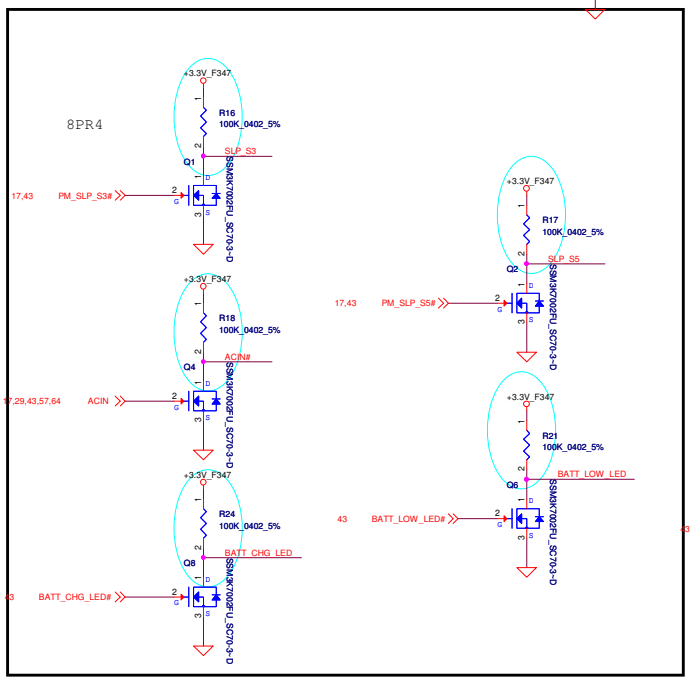
Compal Electronics, Inc.

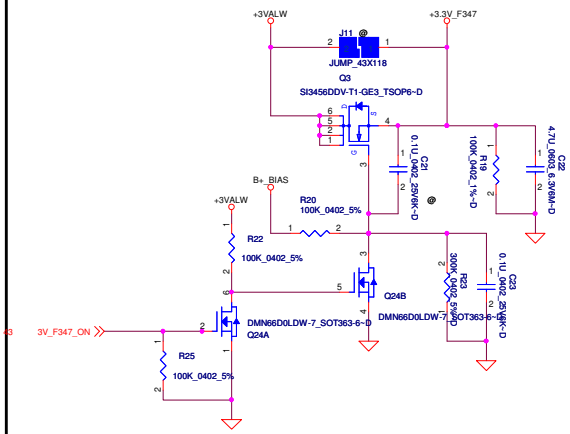
Title: Amp TPA6017/subwoofer/ Audio Jack

Size: | Document Number: LA-9332P | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 46 of 56







DEVICE	SMBUS ADDRESS
MAXIM - LED	0100 000b
MAXIM - GPIO	0100 001b
I2C EEPROM	1010 000b

+3.3V_F347 behavior

	STATE			
	S0	S3	S4	S5
AC IN	ON	ON	ON	ON
BAT only	ON	ON	OFF	OFF

AC mode battery full in S5:turn off ELC controller

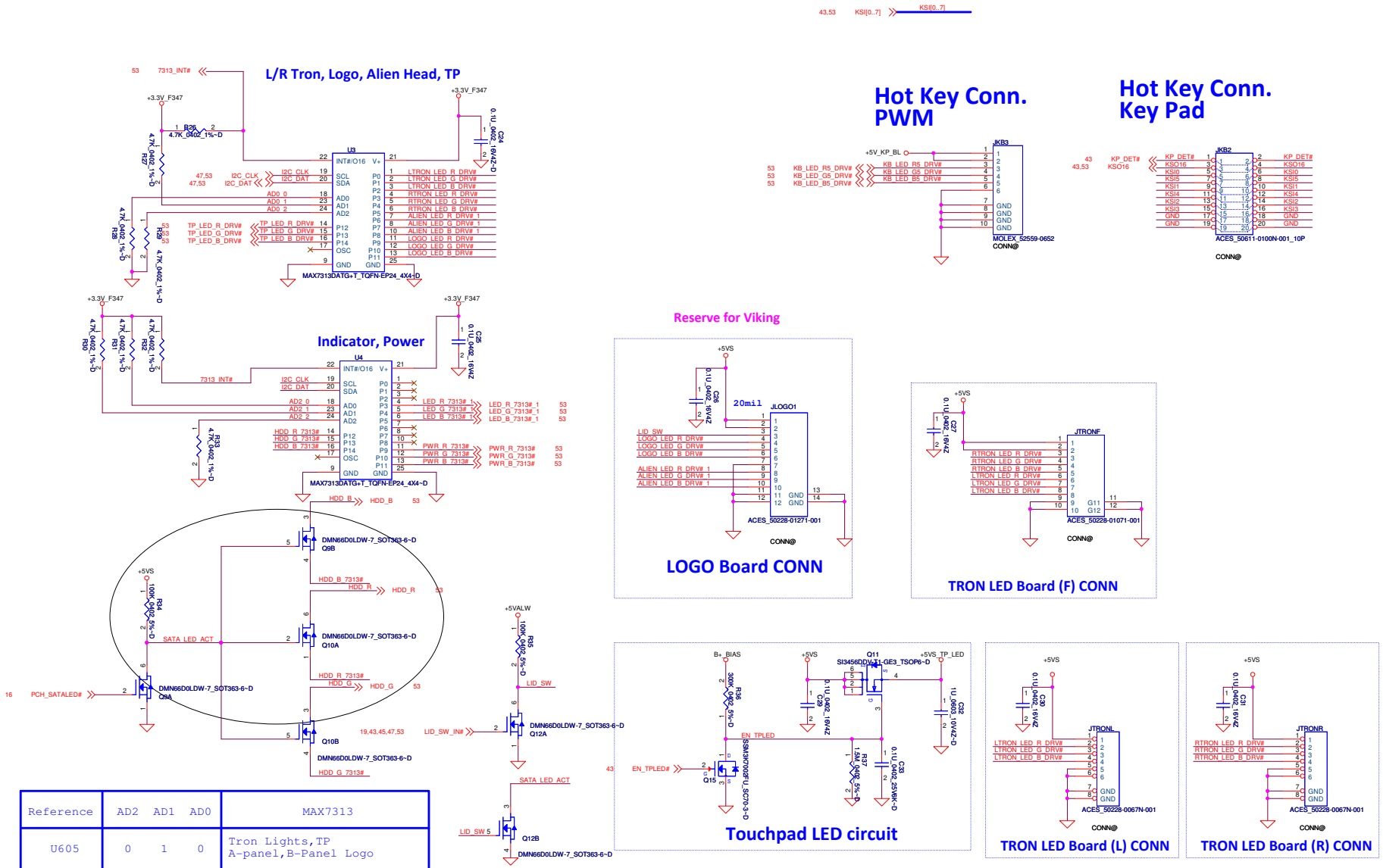
Security Classification	Compal Secret Data		
Issued Date	2012/05/28	Deciphered Date	2013/05/27

Compal Electronics, Inc.

Title: ELC (1)

Size: Custom | Document Number: LA-9332P | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 47 of 56



Reference	AD2	AD1	AD0	MAX7313
U605	0	1	0	Tron Lights,TP A-panel,B-Panel Logo
U608	0	1	1	Power Button, Media and Status LED Color
U?	1	0	0	Button, Indicator Brightness

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Issued Date	2012/05/28	Deciphered Date	2013/05/27

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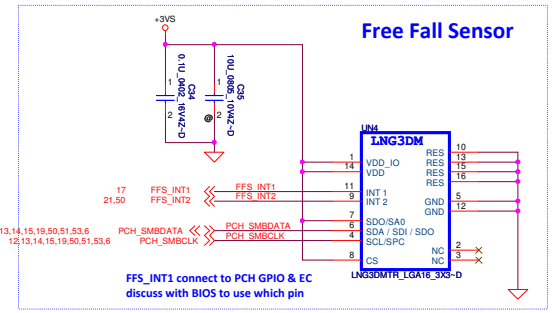
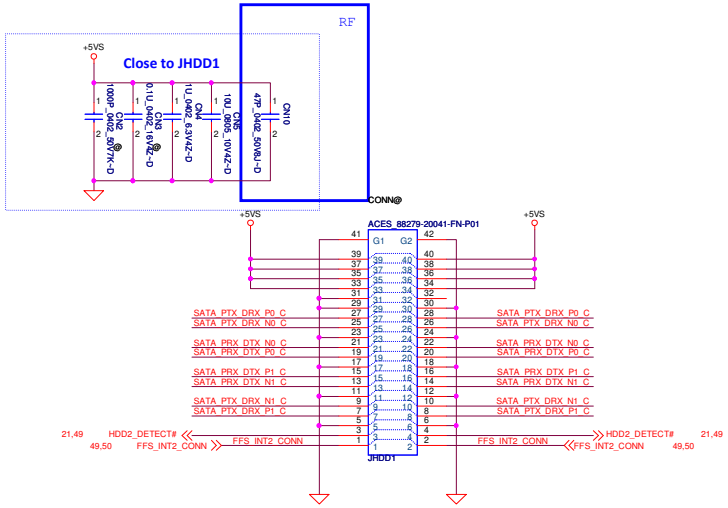
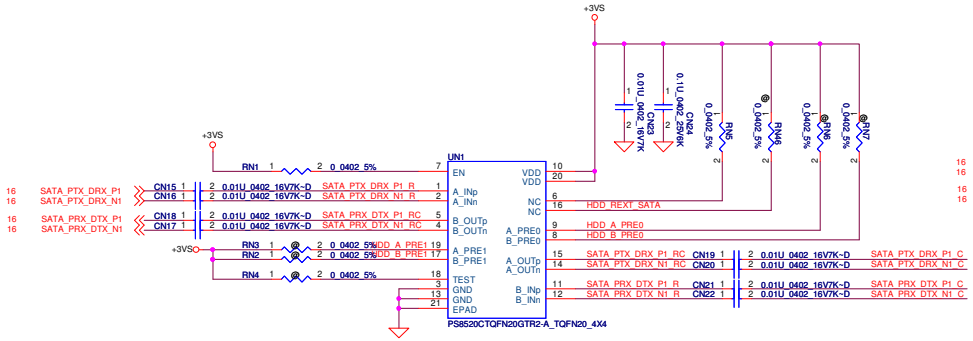
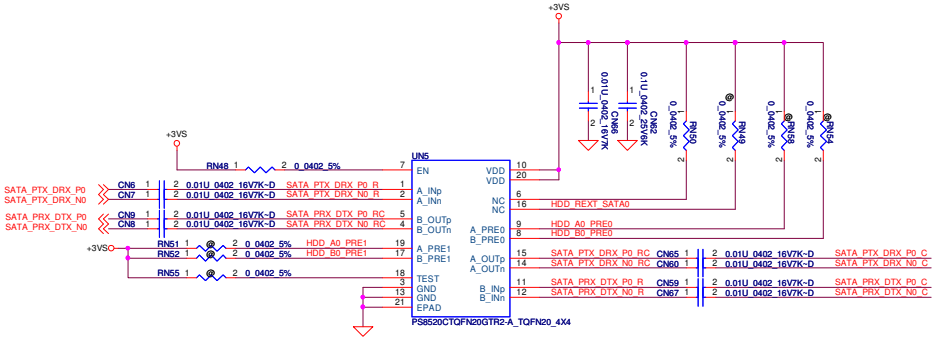
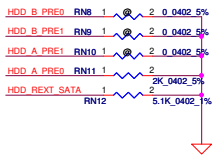
Title	ELC (2)		
Size: Custom	Document Number: LA-9332P		Rev: 0.1
Date: Friday, December 14, 2012	Sheet 48 of 56		

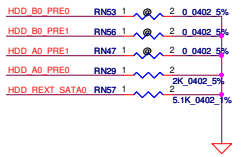












Pin 20:
PARADE PS8250B:
Reserve RN46, Mount RN12

PERICOM PI3EQX6741ST:
Mount RN46, Reserve RN12

ASMEDIA ASM1466:
Mount RN46, Reserve RN12

Pin 9:
PARADE PS8250B:
Reserve RN11.

PERICOM PI3EQX6741ST:
Reserve RN11

ASMEDIA ASM1466:
Mount RN11 to pull down

Pin 20:
PARADE PS8250B:
Reserve R49, Mount R57

PERICOM PI3EQX6741ST:
Mount R49, Reserve R57

ASMEDIA ASM1466:
Mount R49, Reserve R57

Pin 9:
PARADE PS8250B:
Reserve R29.

PERICOM PI3EQX6741ST:
Reserve R29

ASMEDIA ASM1466:
Mount R29 to pull down

Security Classification	Compal Secret Data		
Issued Date	2012/05/28	Deciphered Date	2013/05/27

Compal Electronics, Inc.

Title: SATA HDD1 & HDD2/FFS

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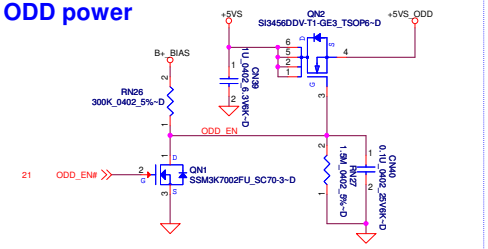
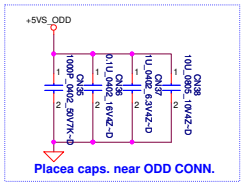
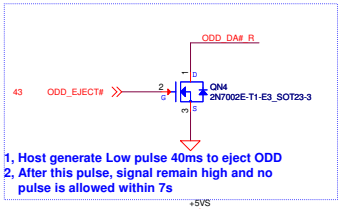
ODD power

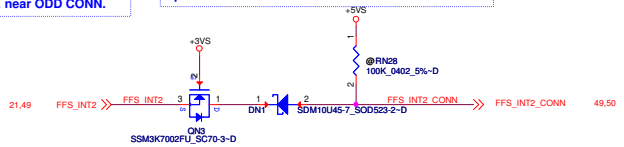




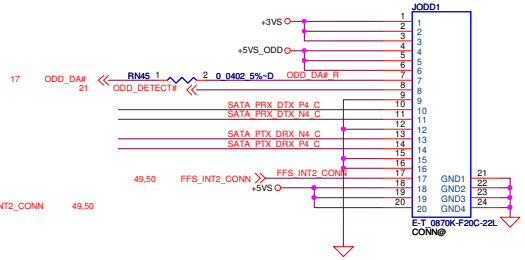
Placea caps. near ODD CONN.



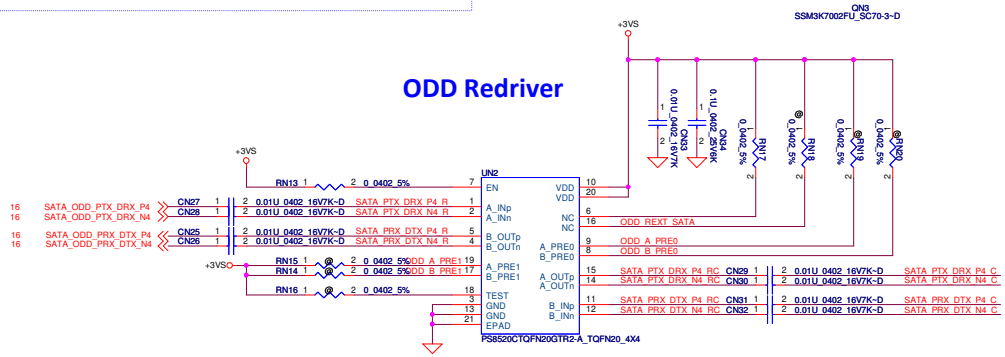
1, Host generate Low pulse 40ms to eject ODD
2, After this pulse, signal remain high and no pulse is allowed within 7s

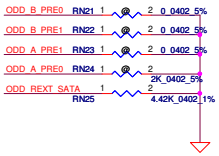


SATA ODD Conn.



ODD Redriver





Pin 20:
PARADE PS8250B:
Reserve RN18, Mount RN25

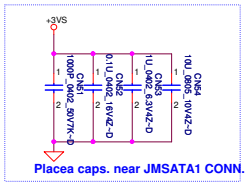
PERICOM PI3EQX6741ST:
Mount RN18, Reserve RN25

ASMEDIA ASM1466:
Mount RN18, Reserve RN25

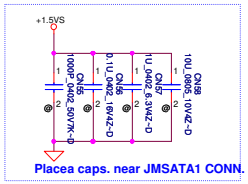
Pin 9:
PARADE PS8250B:
Reserve RN24.

PERICOM PI3EQX6741ST:
Reserve RN24

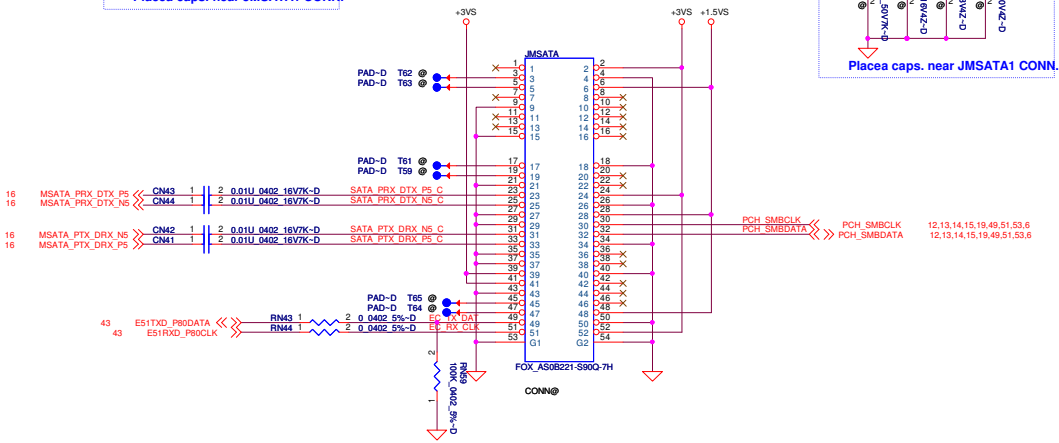
ASMEDIA ASM1466:
Mount RN24 to pull down



Placea caps. near JMSATA1 CONN.



Placea caps. near JMSATA1 CONN.



Security Classification	Compal Secret Data		
Issued Date	2012/05/28	Deciphered Date	2013/05/27

Compal Electronics, Inc.

Title: SATA ODD/mSATA

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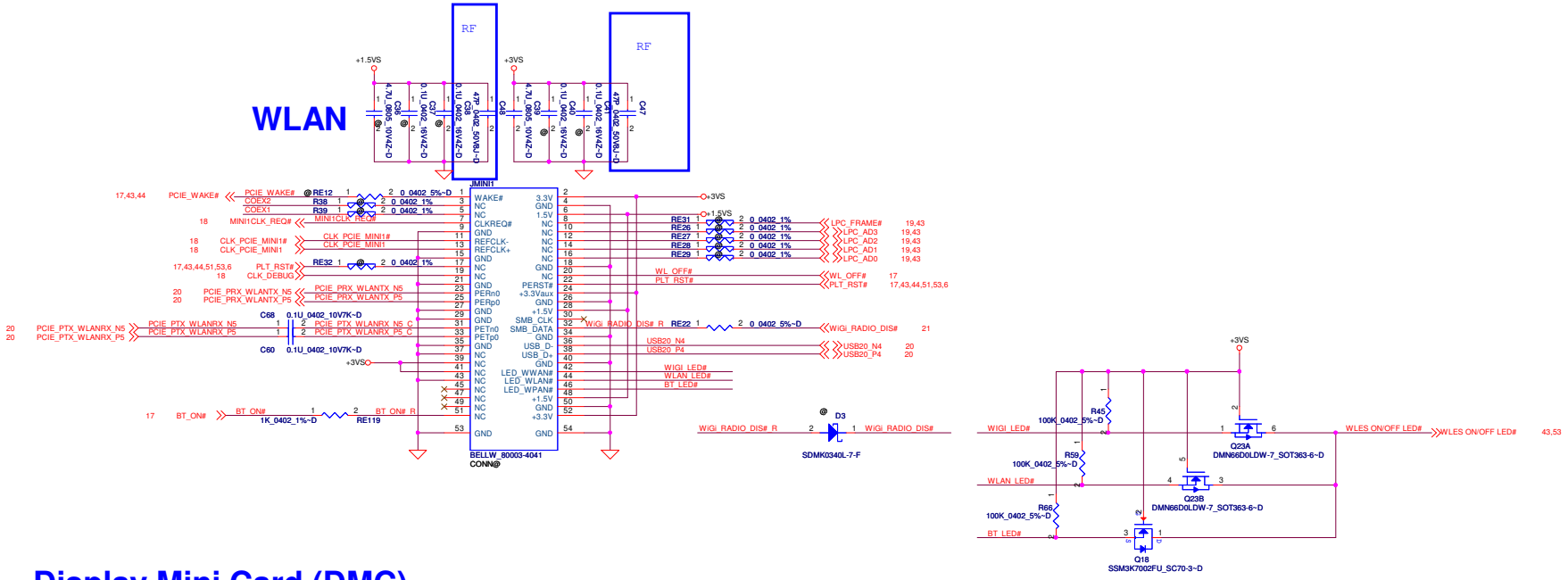
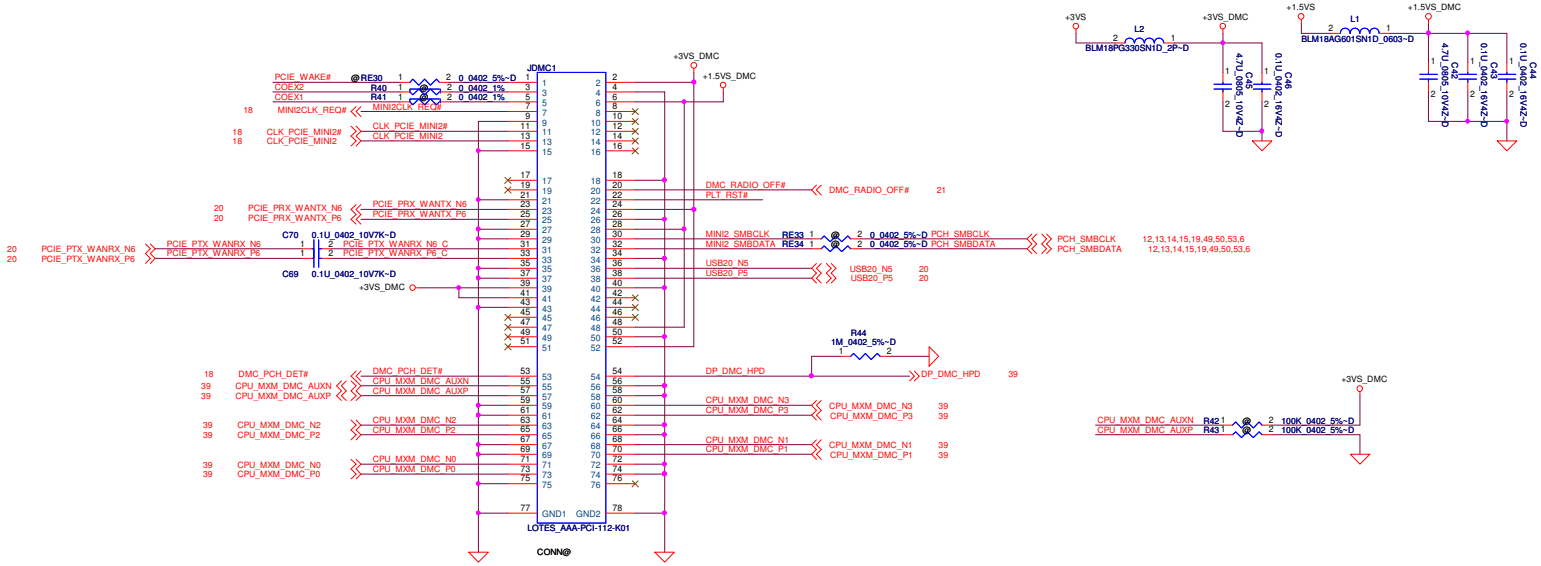
Date: Friday, December 14, 2012 | Sheet 50 of 56

WLAN



Display Mini Card (DMC)



Security Classification	Compal Secret Data		
Issued Date	2012/05/28	Deciphered Date	2013/05/27

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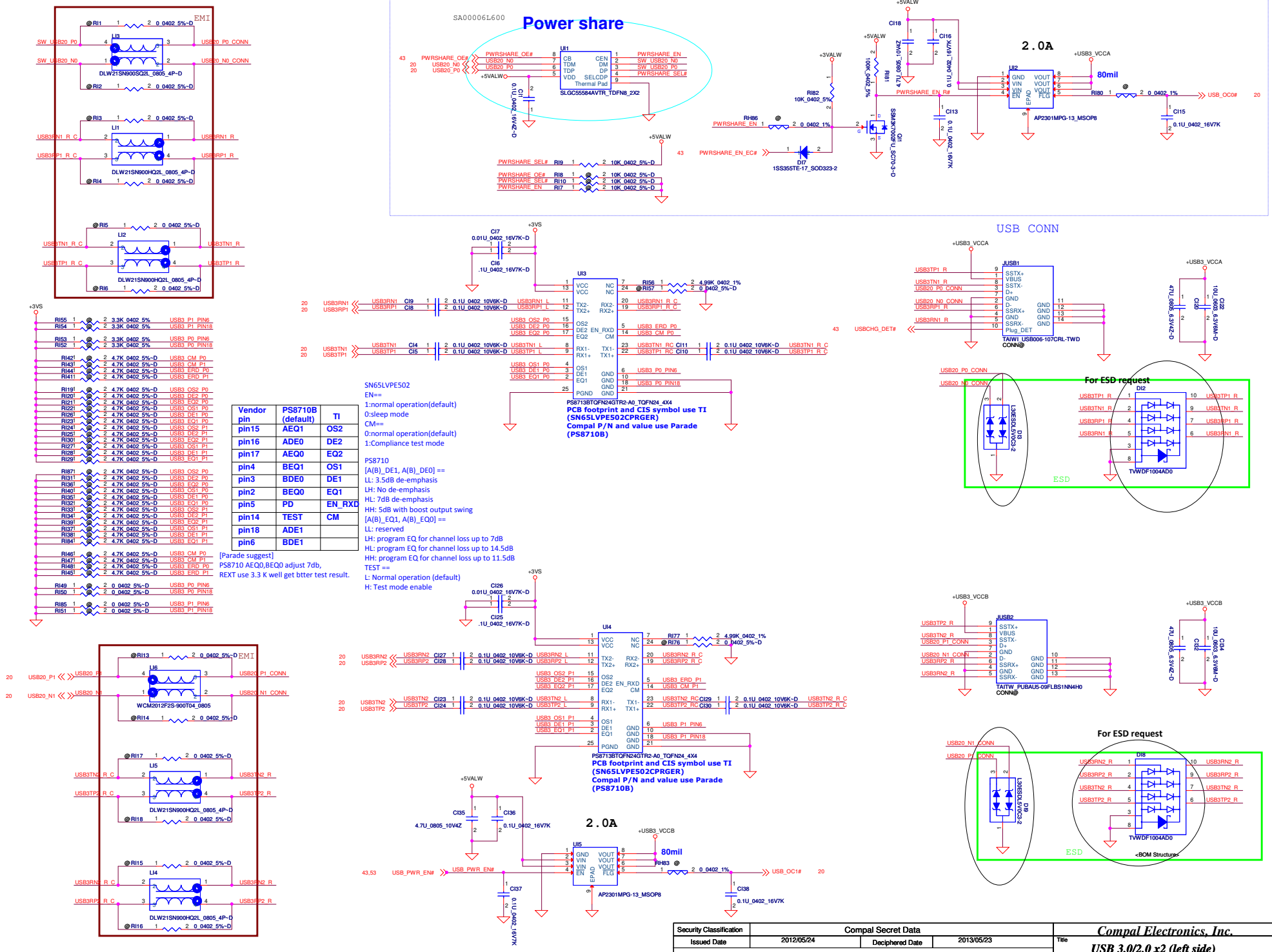
Compal Electronics, Inc.

Title: Mini Card -WLAN/DMC/BT

Size: Custom | Document Number: LA-9332P | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 51 of 56



Vendor pin	PS8710B (default)	TI
pin15	AEQ1	OS2
pin16	ADE0	DE2
pin17	AEQ0	EQ2
pin4	BEQ1	OS1
pin3	BDE0	DE1
pin2	BEQ0	EQ1
pin5	PD	EN_RXD
pin14	TEST	CM
pin18	ADE1	
pin6	BDE1	

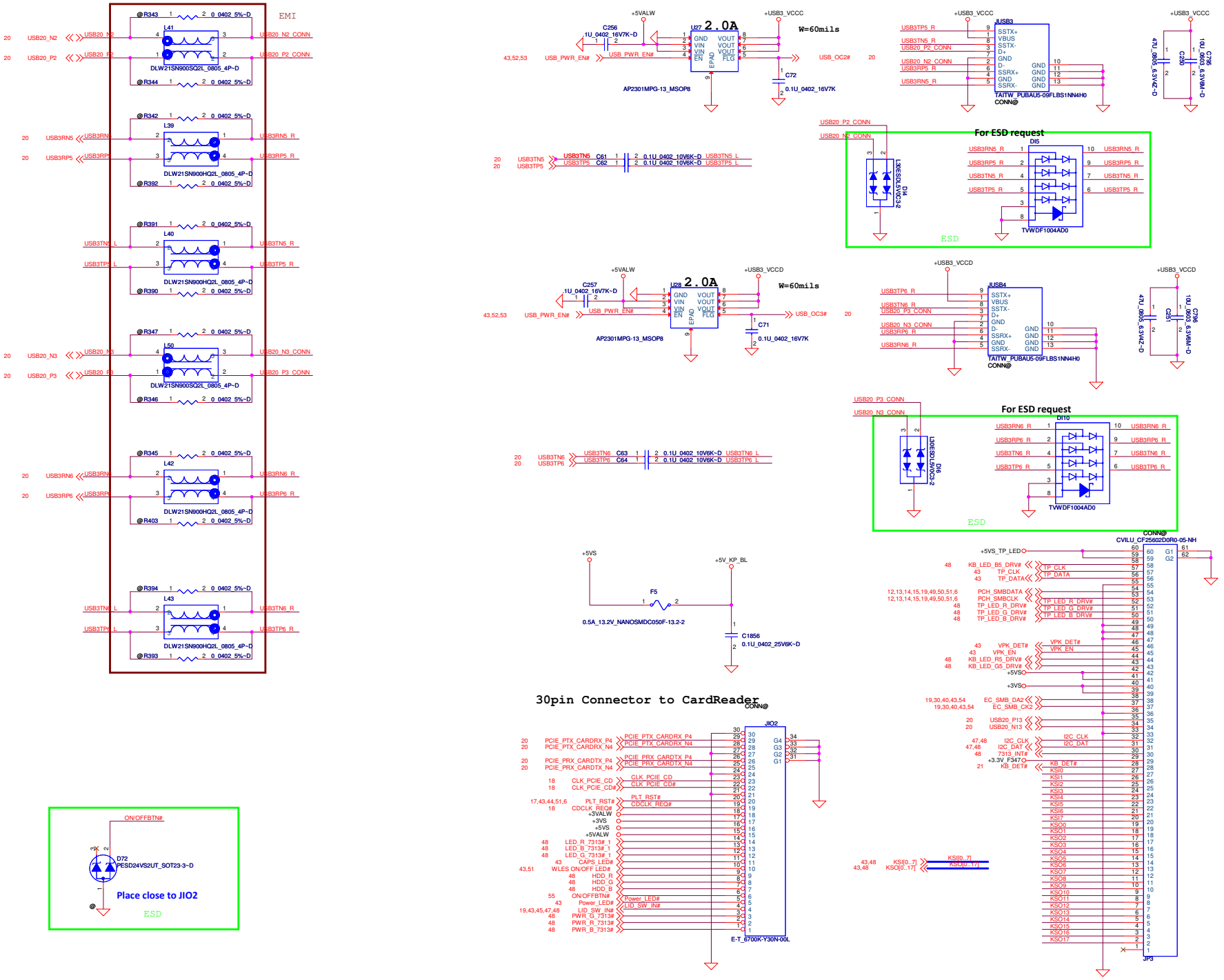
Security Classification	Compal Secret Data		
Issued Date	2012/05/24	Deciphered Date	2013/05/23

Compal Electronics, Inc.

Title: USB 3.0/2.0 x2 (left side)

Size: Custom | Document Number: LA-9332P | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 52 of 56



Security Classification	Compal Secret Data		
Issued Date	2012/02/28	Deciphered Date	2013/02/27

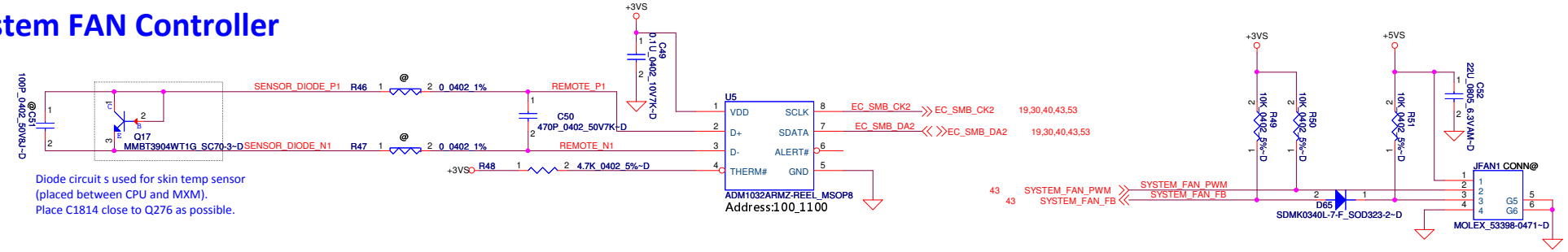
Compal Electronics, Inc.

Title: IO BTB CONN

Size: Custom | Document Number: LA-9332P | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 53 of 56

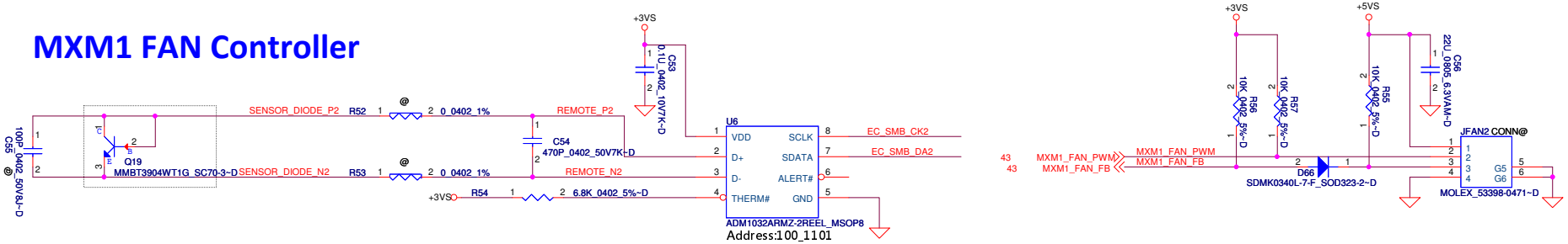
System FAN Controller



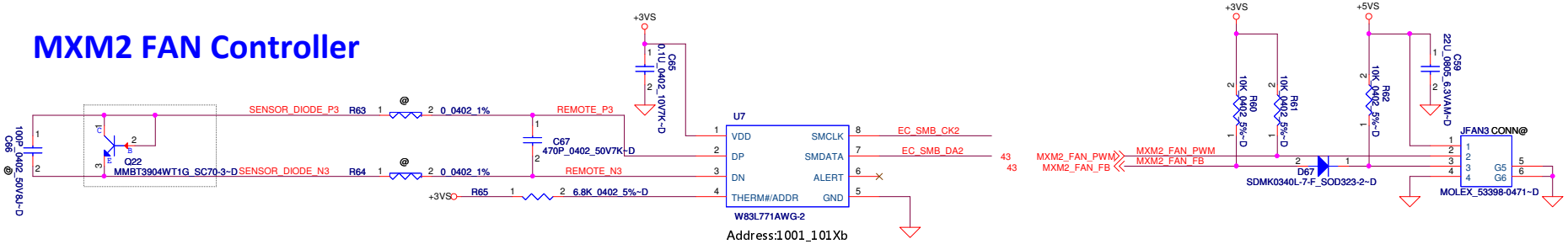
Diode circuit s used for skin temp sensor
(placed between CPU and MXM).
Place C1814 close to Q276 as possible.

Pull up resistor on thermtrip pin	SMBUS address
4.7k	1111
6.8k	1011
10k	1001
15k	1101
22k	0011
33k	0111

MXM1 FAN Controller



MXM2 FAN Controller



Security Classification	Compal Secret Data		
Issued Date	2012/05/14	Deciphered Date	2013/05/13

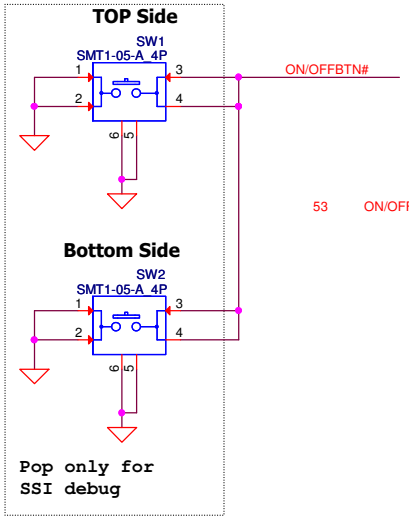
Compal Electronics, Inc.

Title: Thermal Sensor & FAN

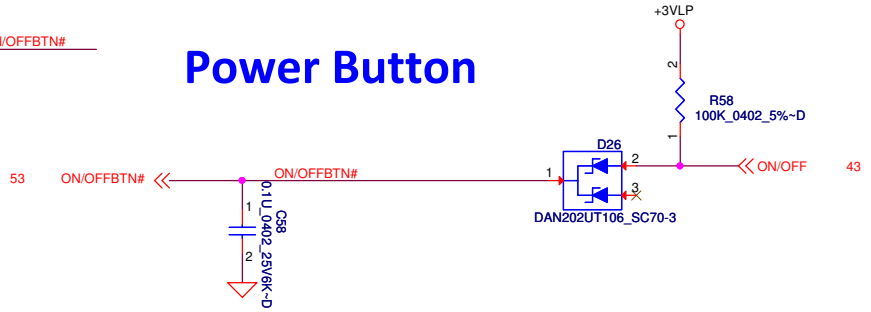
Size: Custom | Document Number: LA-9332P | Rev: 0.1

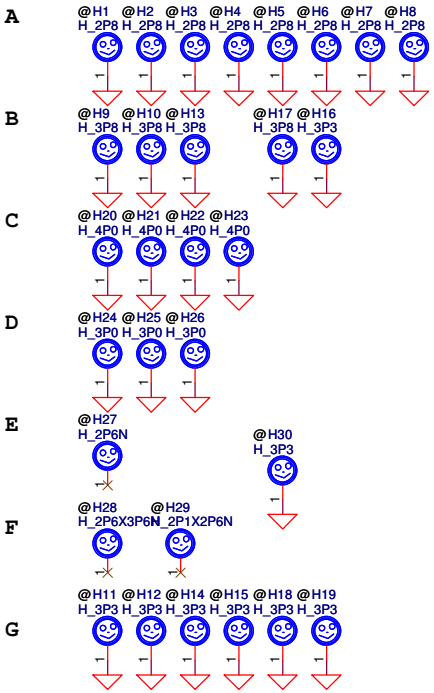
Date: Friday, December 14, 2012 | Sheet 54 of 56

ON/OFF switch

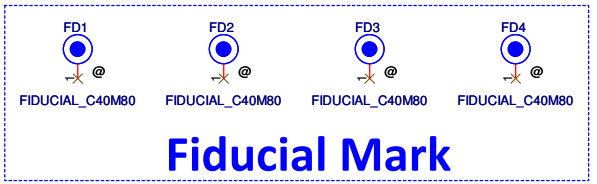


Power Button





ZZZ1
PCB-MB



Security Classification	Compal Secret Data		
Issued Date	2012/05/28	Deciphered Date	2013/05/27

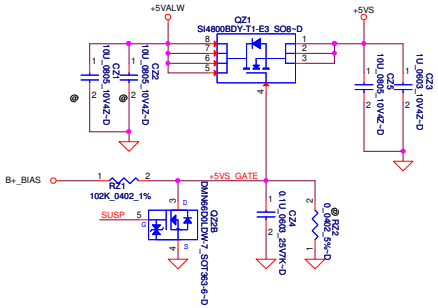
Title: KB & Power Button & IR

Size: B | Document Number: LA-9332P | Rev: 0.1

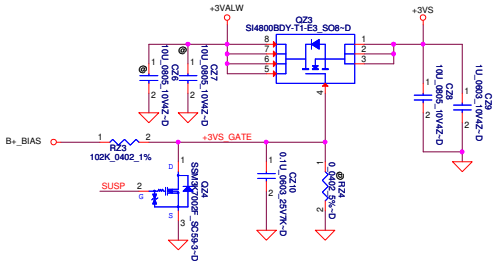
Date: Friday, December 14, 2012 | Sheet 55 of 56

DC to DC

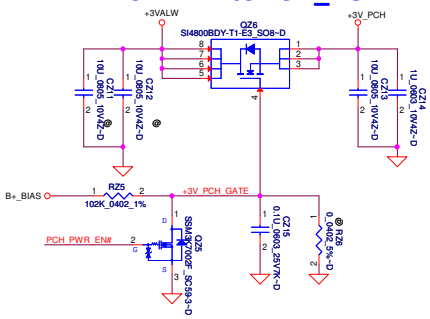
+5VALW to +5VS



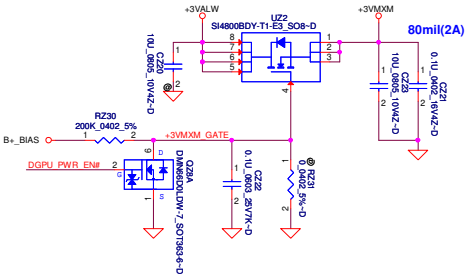
+3VALW to +3VS



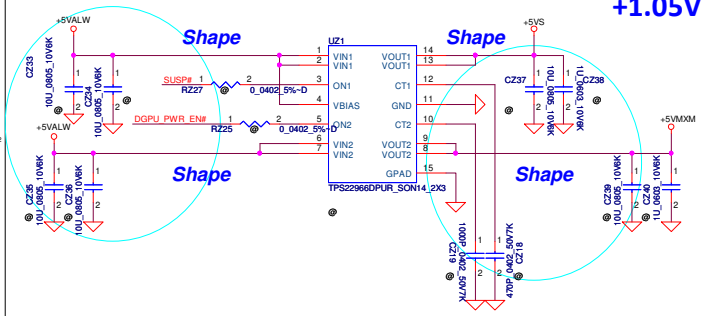
+3VALW to +3V_PCH



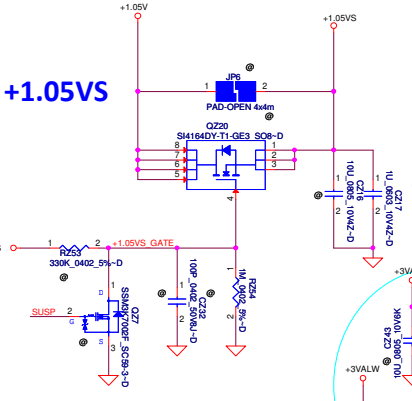
+3VALW to +3VMXM Transfer



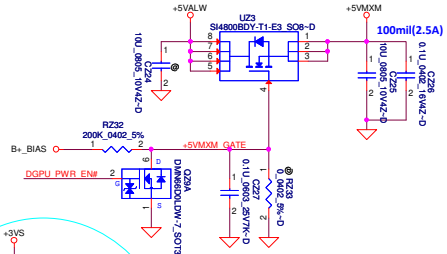
+5VALW to +5VS
+3VALW to +3VS



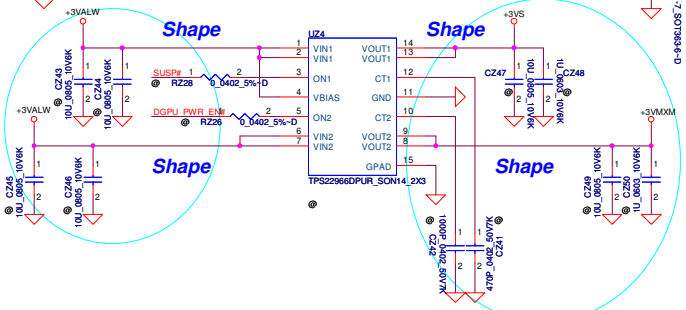
+1.05V to +1.05VS



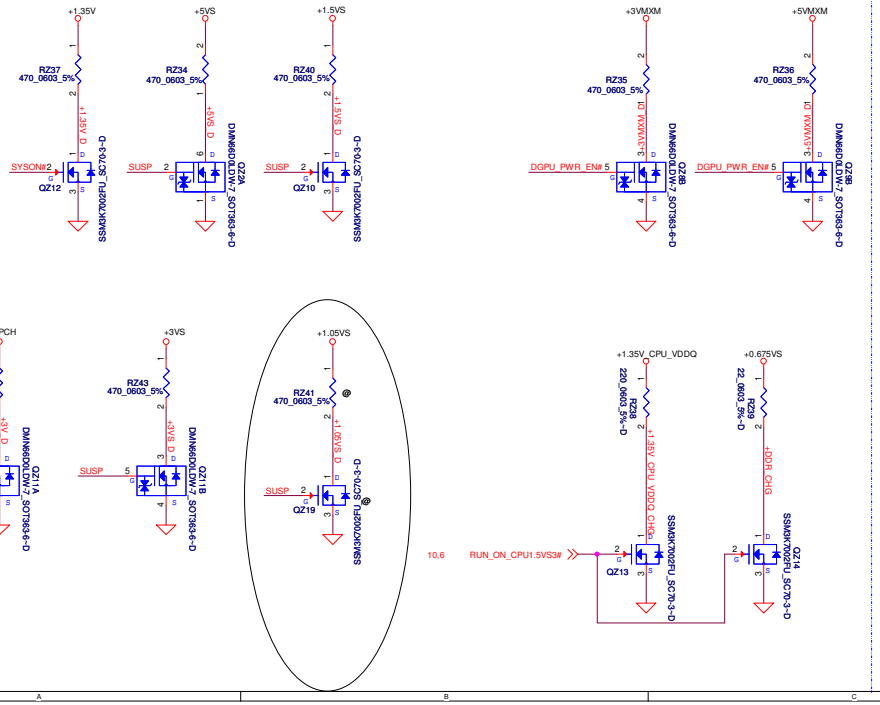
+5VALW to +5VMXM

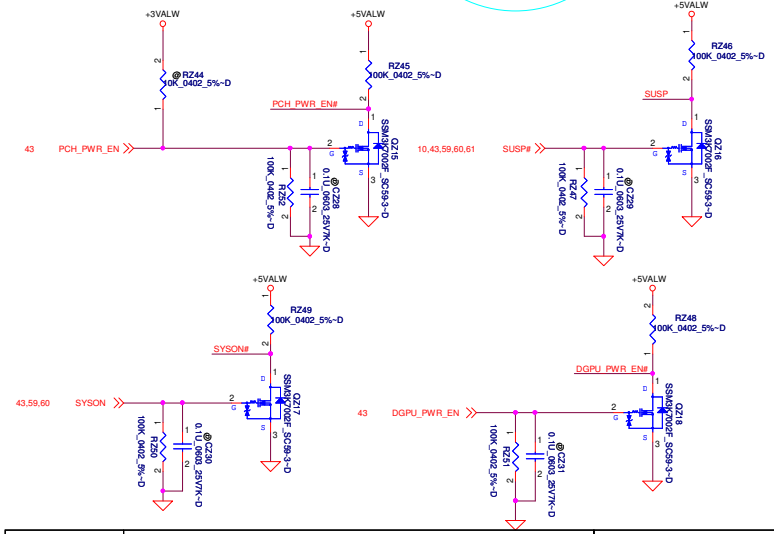


+5VALW to +5VMXM
+3VALW to +3VMXM



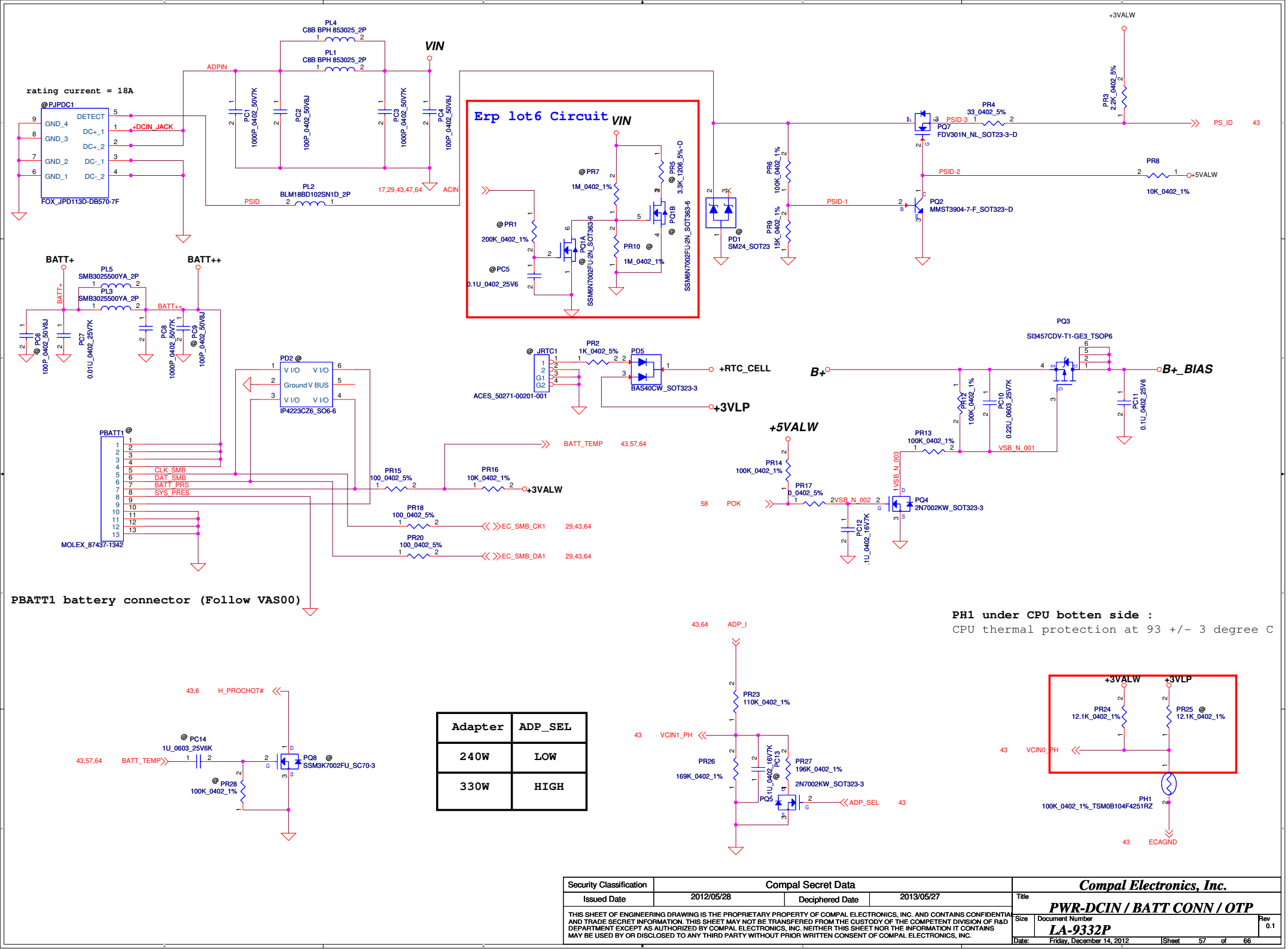
Discharge Circuit





Security Classification	Compal Secret Data		
Issued Date	2012/05/28	Deciphered Date	2013/05/27

Compal Electronics, Inc.	
Title	DC/DC Interface
Size	Document Number: LA-9332P
Custom	Rev: 0.1
Date: Friday, December 14, 2012	Sheet 56 of 56



Adapter	ADP_SEL
240W	LOW
330W	HIGH

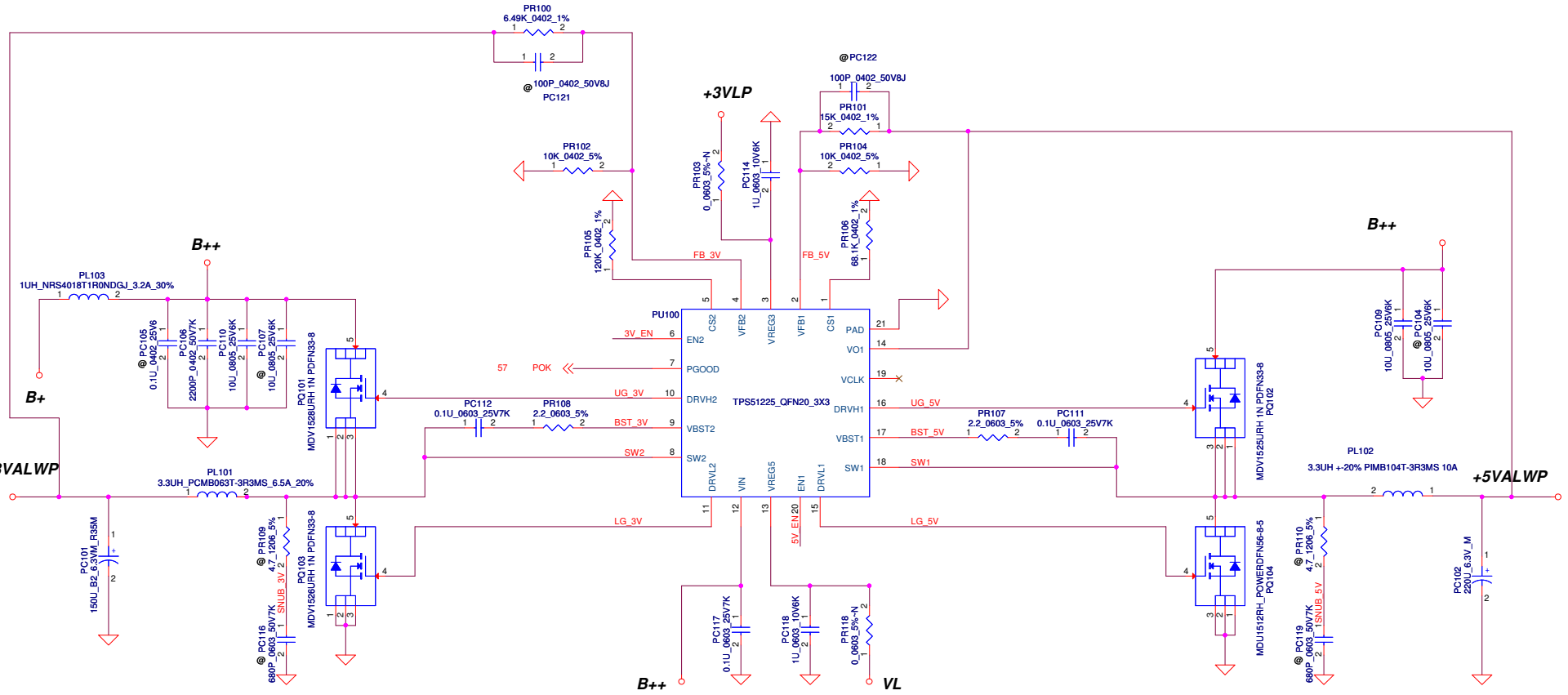
Security Classification	Compal Secret Data		
Issued Date	2012/05/28	Deciphered Date	2013/05/27

Compal Electronics, Inc.

Title: PWR-DCIN / BATT CONN / OTP

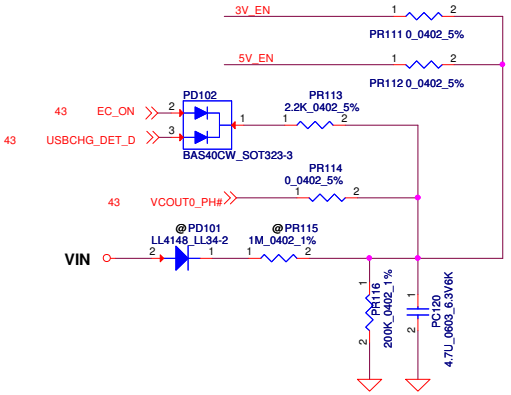
Size: | Document Number: LA-9332P | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 57 of 66



3VALWP
TDC 6.08A
Peak Current 8.11A
OCP current 9.73A

	TYP	MAX
H/S Rds(on)	11.2mohm ,	14mohm
L/S Rds(on)	3.7mohm ,	5mohm



5VALWP
TDC 11A
Peak Current 16A
OCP current 20A

	TYP	MAX
H/S Rds(on)	11.2mohm ,	14mohm
L/S Rds(on)	3.7mohm ,	5mohm

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/05/28	Deciphered Date 2013/05/27	Title PWR-3VALWP/5VALWP
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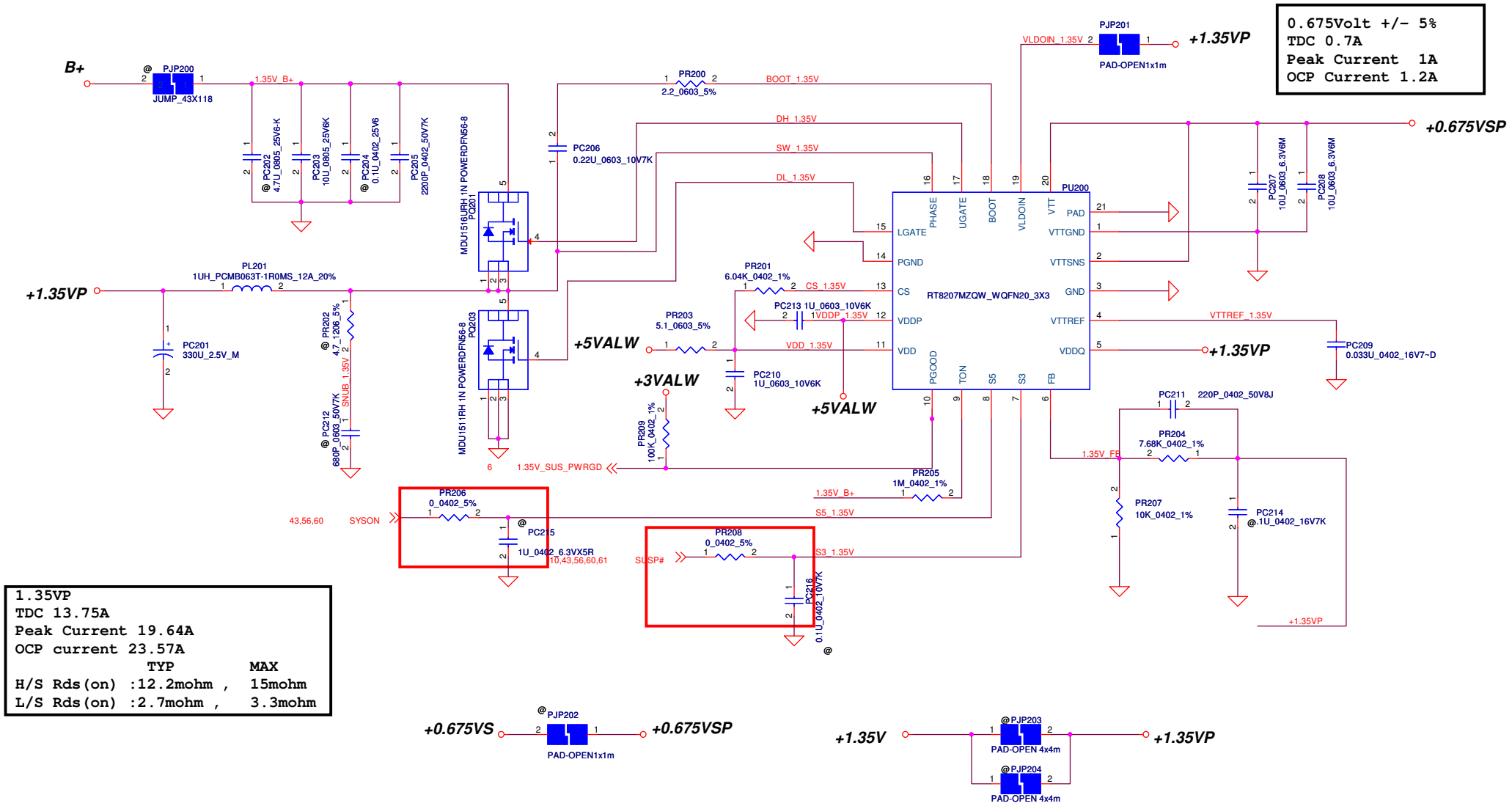
			Date: Friday, December 14, 2012 Sheet 58 of 66



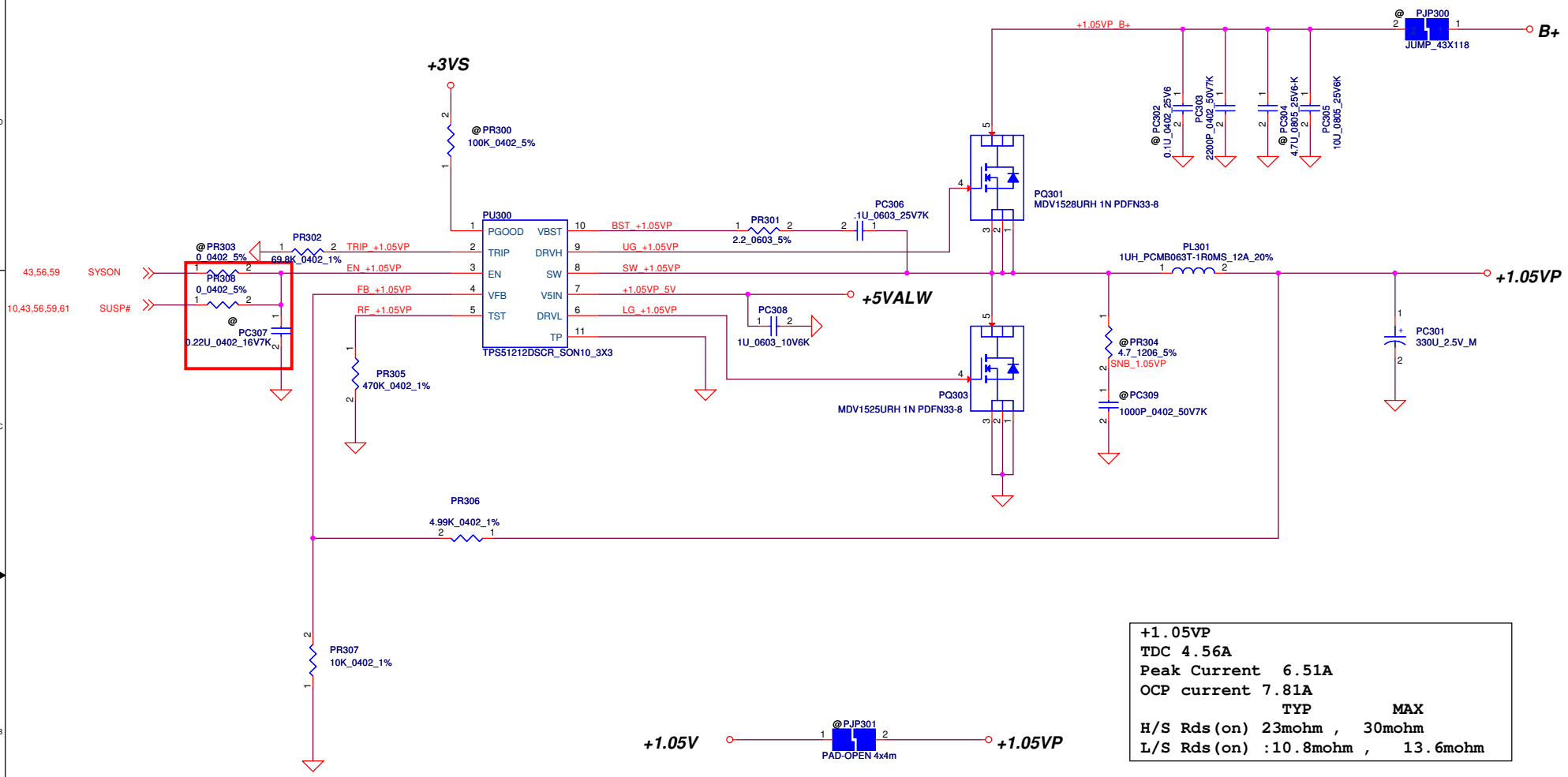
Security Classification	Compal Secret Data		
Issued Date	2012/05/28	Deciphered Date	2013/05/27

Compal Electronics, Inc.

Title: PWR-1.35VP/0.675VSP

Size | Document Number: LA-9332P | Rev: 0.1

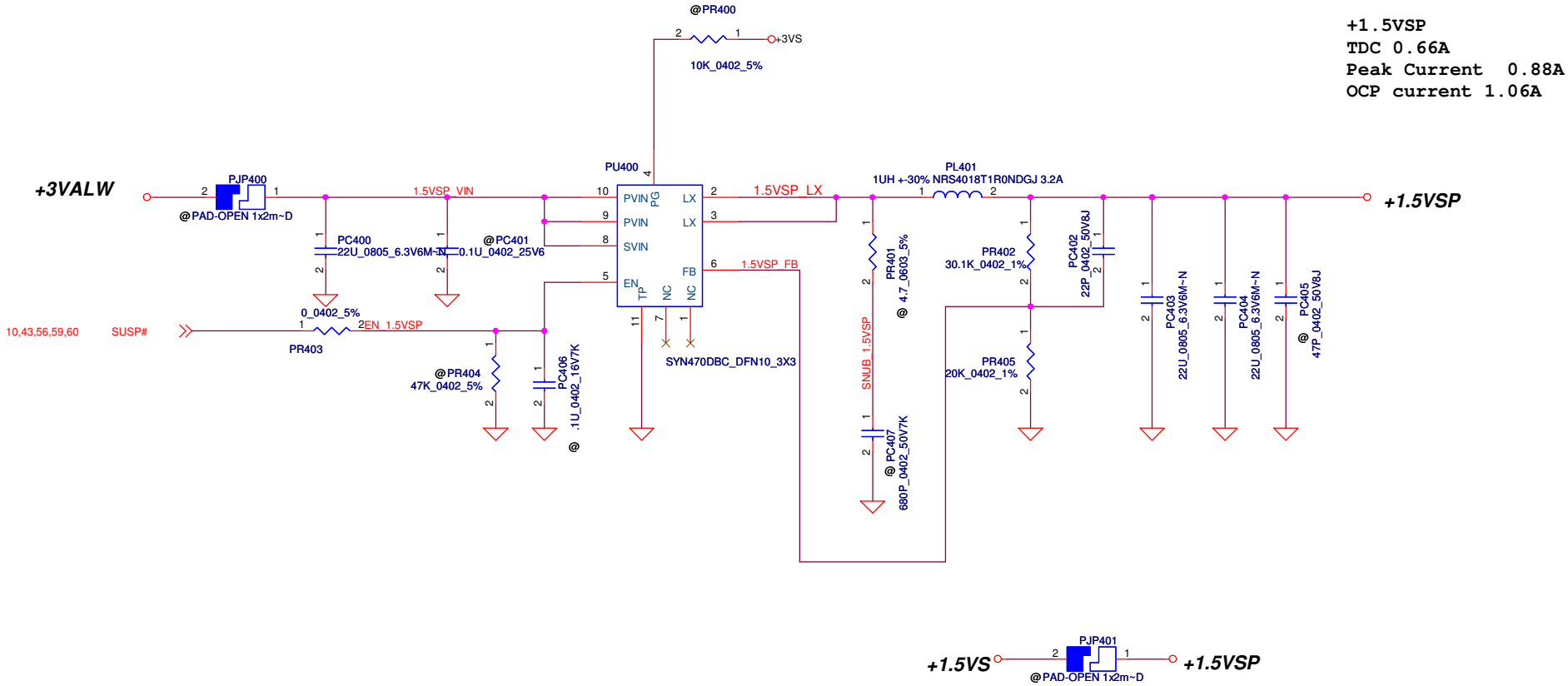
Date: Friday, December 14, 2012 | Sheet 59 of 66




```
+1.05VP
TDC 4.56A
Peak Current  6.51A
OCP current 7.81A
                TYP          MAX
H/S Rds(on) 23mohm ,   30mohm
L/S Rds(on) :10.8mohm ,    13.6mohm
```

Security Classification	Compal Secret Data		
Issued Date	2012/05/28	Deciphered Date	2013/05/27

Compal Electronics, Inc.		
Title: PWR-+1.05VP		
Size	Document Number: LA-9332P	Rev: 0.1
Date: Friday, December 14, 2012	Sheet 60 of 66	



Security Classification	Compal Secret Data		
Issued Date	2012/05/28	Deciphered Date	2013/05/27

Compal Electronics, Inc.

Title: **PWR-1.5VSP**

Size | Document Number: **LA-9332P** | Rev: 0.1

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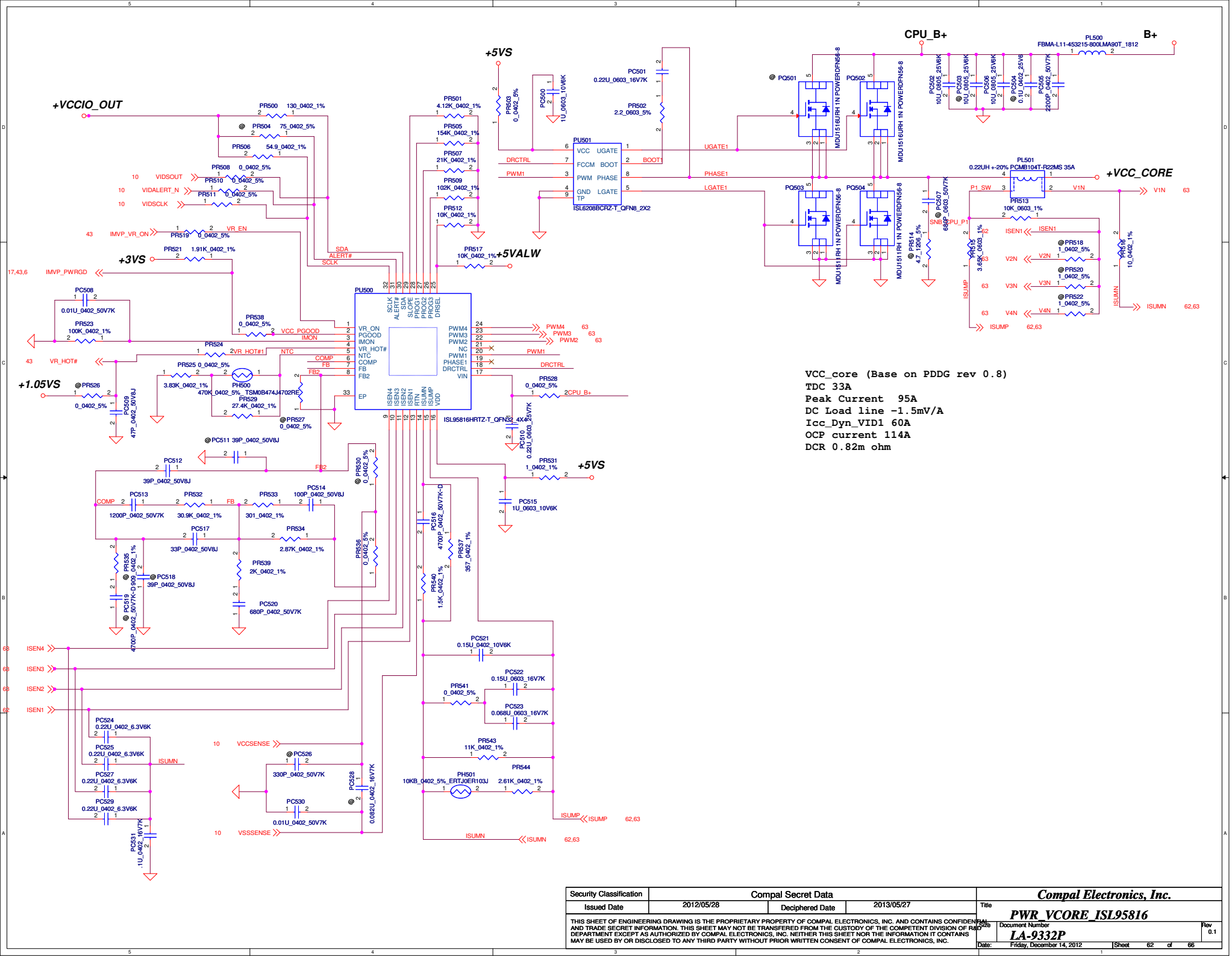

Security Classification	Compal Secret Data		
Issued Date	2012/05/28	Deciphered Date	2013/05/27

Compal Electronics, Inc.			
Title: PWR_VCORE_ISL95816			
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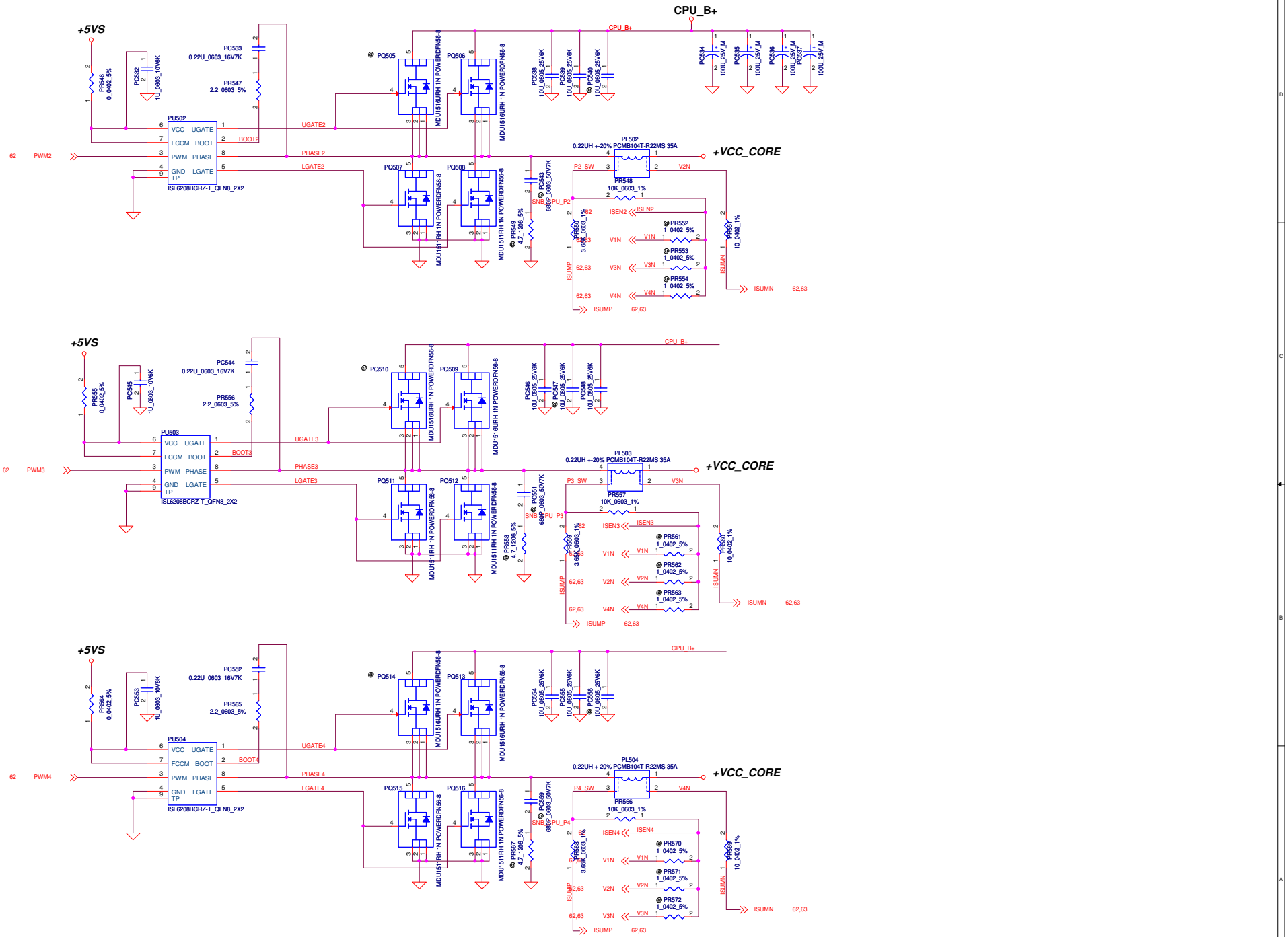

Security Classification	Compal Secret Data		
Issued Date	2012/05/28	Deciphered Date	2013/05/27

Compal Electronics, Inc.

Title: **PWR_VCORE_ISL6208**

Size	Document Number	Rev
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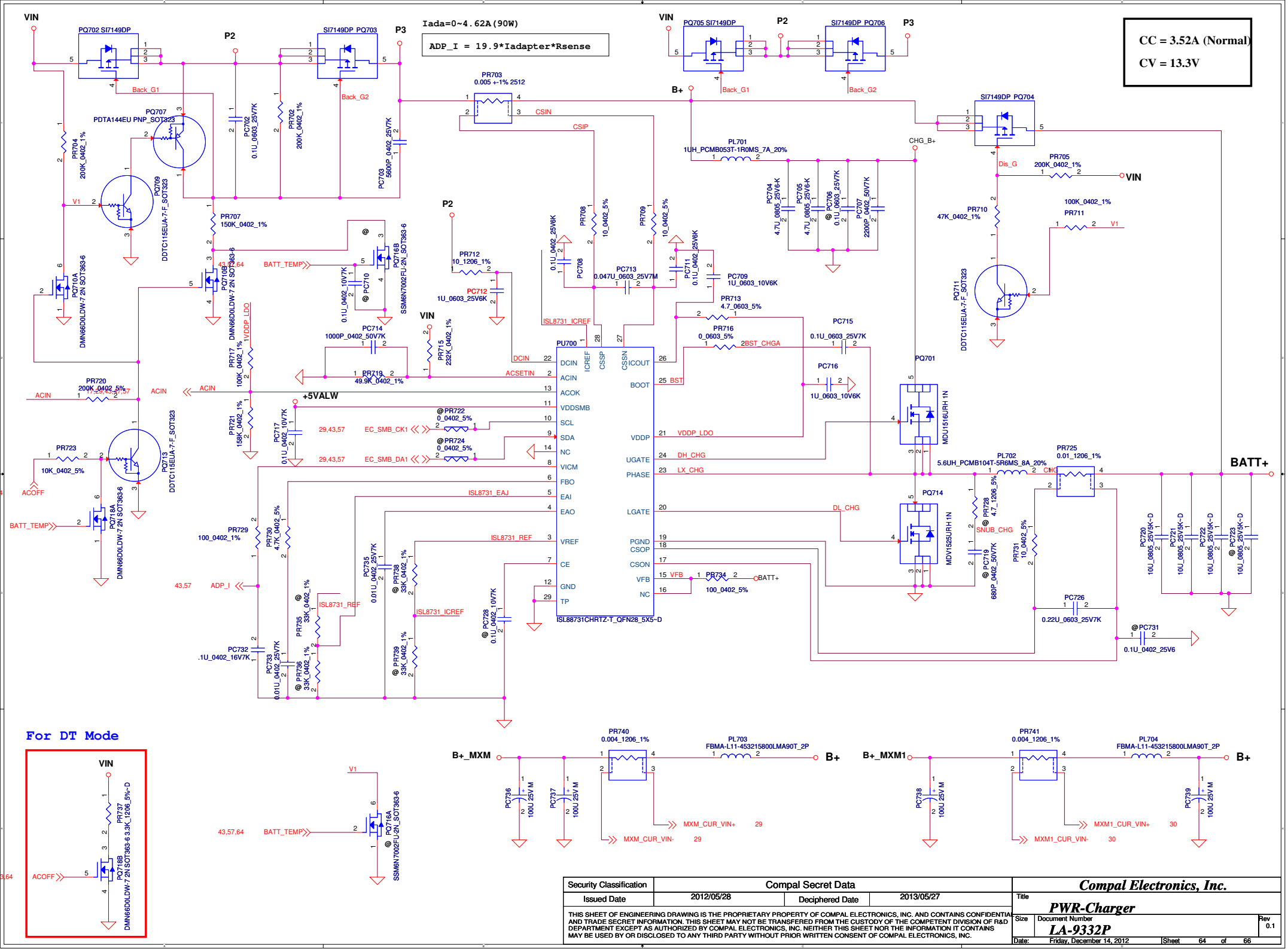

Security Classification	Compal Secret Data		
Issued Date	2012/05/28	Deciphered Date	2013/05/27

Compal Electronics, Inc.

Title: **PWR-Charger**

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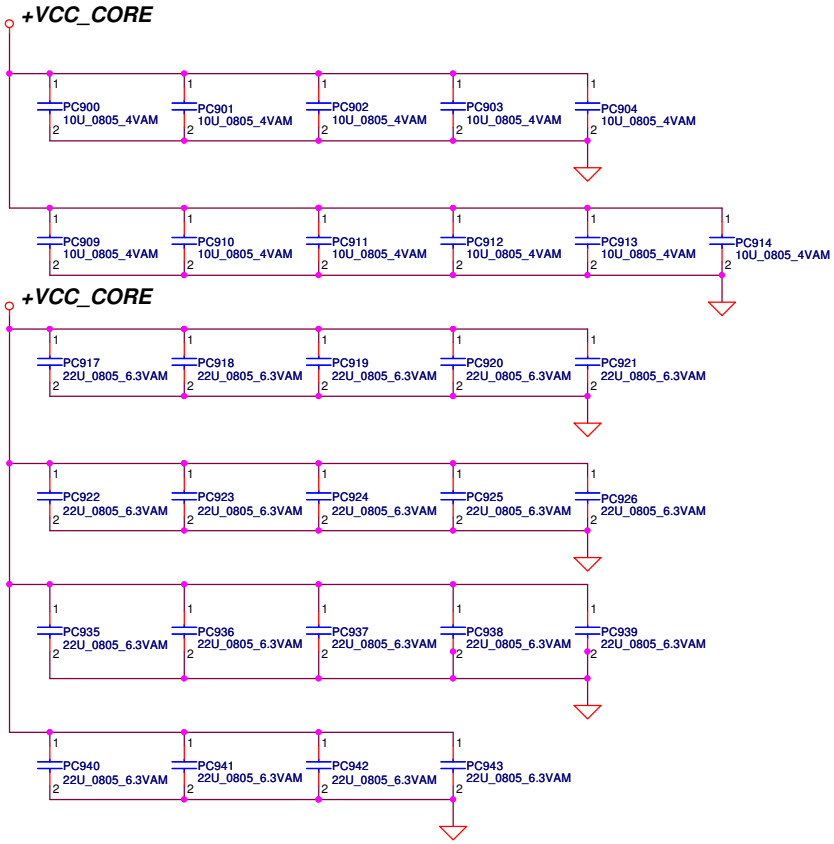
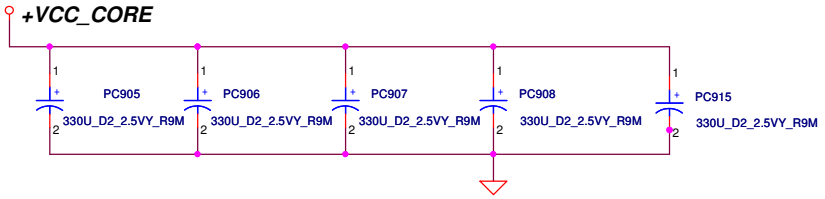
Based on PDDG rev 0.8 Table 5-1.





Compal Electronics, Inc.

Title: PWR_PROCESSOR DECOUPLING

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Version change list (P.I.R. List)

Item	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Adjust 1.5V output volatge		P61	change PR402 to 30.1K_0402_1% PR405 to 20K_0402_1%	2012.7.30	SSI
2	Adjust 3.3V OCP seeting		P58	change PR105 to 120K_0402_1%.	2012.7.30	SSI
3	Adjust 3V/5V always OTP seeting		P58	modify PD100 to PR114 0_0402_1%.	2012.7.30	SSI
4	Adjust Vcore OTP seeting		P62	PR531 connect to +5VS	2012.7.30	SSI
5	Add PD3 PD4 for EMD requirement		P57	add PD3 PD4 to PESD24VS2UT_SOT23-3	2012.8.16	SSI
6	hiccup mode issue is not happen so we haven't need solution.		P57	remove Erp Iot6 Circuit	2012.8.16	SSI
7	change diode for EMI requirement		P57	use PD2 (6 PIN) to combine combine PD3(2PIN) PD4(2PIN).	2012.8.31	SSI
8	adjust the component for the 88731 schematic		P64	change PR722 and PR724 to short footprint remove PR701 PR706 PC701 PC734 PR732	2012.9.10	SSI
9	adjust RTC circuit for safety concern		P57	add PR2 1K_0402_5%	2012.9.10	SSI
10	change ACIN bead for current limit rating		P57	change PL1 PL4 to C8B BPH 853025_2P	2012.9.10	SSI
11	add PR116 for 3v 5v_EN delay time solution		P58	add PR116 402K_0402_1%	2012.9.18	SSI
12	change output choke to improve efficiency		P59	change PL201 to 1UH_PCMC063T-1R0MN	2012.9.18	SSI
13	change PR500 value to meet INTEL SPEC.		P62	change PR500 to 130_0402_1%~D	2012.10.4	SSI
			P67			
14						
15						
16						
17						