Model Name : QILE1 & QILE2
File Name : LA-8131P, LA-8133P
BOM P/N:

QILE1:
4319GG39L01 : SMT MB A8131 QILE1 DIS-N13P
4319GG39L02 : SMT MB A8131 QILE1 DIS GPU-N13M
4319GG39L03 : SMT MB A8131 QILE1 UMA

QILE2:
4319GJ39L01 : SMT MB A8133 QILE2 DIS-N13P
4319GJ39L02 : SMT MB A8133 QILE2 DIS GPU-N13M
4319GJ39L03 : SMT MB A8133 QILE2 UMA

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M/B Schematics Document

Intel Ivy Bridge Processor with DDRIII + Panther Point PCH

GPU nVIDIA N13M-GE1 / N13P-GL

2012-01-11

REV:1.0

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Title: Cover Sheet

Size: Custom | Document Number: LA-8133P | Rev: 1.0

Date: Friday, January 13, 2012 | Sheet 1 of 58

zzz
LA8131P
DA_PCB
DA80000QL00

nVIDIA N13M-GE1
DDR3*4
VRAM 256M*16/
128M*16/64M*16
nVIDIA N13P-GL
DDR3*8
VRAM 256M*16/
128M*16/64M*16
Page 24~32

PCI-E X16

Intel
Ivy Bridge
rPGA 989 Socket
37.5mm * 37.5mm
Page 4~10

Memory Bus
Dual Channel
1.5V DDR3 1600MHz

DDR3-SO-DIMM X2
Page 11~12

HDMI Connector
Page 34

HDMI

CRT Connector
Page 33

RGB

LVDS Connector
Page 32

LVDS

FDI x8
(UMA)
100MHz
2.7GT/s

DMI x4
100MHz
5GB/s

Intel
Panther Point
FCBGA 989
25mm*25mm
HM76
Page 13~21

HD Audio

Audio Codec
CX20671-21Z CODEC
Page 35

2Channel Speaker
Page 35

Digital MIC
Page 35

Audio combo Jack
Page 35

Sub-Board

PCI-E

Card Reader
Realtek RTS5229
Page 36

cable

Realtek
RTL8111F(Giga)
Page 40

cable

RJ45 CONN
Page 40

Sub-Board

SPI ROM
BIOS 8M+4M
Page 13

SPI

USB 2.0

USB 3.0

SATA

CMOS Camera
Page 32

USB PORT 2.0 x 1(charger)
Page 39

Finger Printer
UPEK TCS5DA6C0
Page 40

Sub-Board

USB PORT 3.0 x 3
Page 37

LPC BUS

EC
ENE KBC9012
Page 41

TPM
Page 40

Track Point
Page 39

G-Sensor
Page 36

Click Pad
Page 39

Int.KBD
Page 39

Thermal Sensor
Fintek F75303M Page 39

SATA3.0 HDD CONN
Page 36

SATA ODD CONN
Page 36

m-SATA CONN
Page 38

PCI Express
Mini card
Slot 1
WLAN/WiMAX/BT
Page 38

USB(BT)

PCI-E(WLAN)

PCI Express
Mini card
Slot 2
WWAN/mSATA
Page 38

USB

SATA

SIM Card
Page 38

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Compal Electronics, Inc.

Title: **Block Diagram**

Size: Custom | Document Number: **LA-8133P** | Rev: 1.0

Date: Friday, January 13, 2012 | Sheet 2 of 58

Voltage Rails

State \ power plane	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.75VS +1.05VS	+3VM +1.05VM
S0	0	0	0	0	0 M3 Supported
S3	0	0	0	X	0 M3 Supported
S5 S4/AC	0	0	X	X	0 M3 Supported
S5 S4/ Battery only	X	X	X	X	
S5 S4/AC & Battery don't exist	X	X	X	X	

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	0.5
5	0.6
6	
7	

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor Fintek F75303M	1001_101xb

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

USB Port Table

	USB 2.0	Port	3 External USB Port
EHCI1 USB3.0	UHCI0	0	
		1	USB 3.0 Port (Left Side)
	UHCI1	2	USB 3.0 Port (Left Side)
		3	USB 3.0 Port (Left Side)
	UHCI2	4	
		5	Camera
	UHCI3	6	
		7	
EHCI2	UHCI4	8	
		9	~~USB Port (Right Side)~~
	UHCI5	10	Mini Card(WLAN/BT)
		11	~~EPR~~
	UHCI6	12	Mini Card(WWAN)
		13	~~Blue Tooth~~

BOM Structure Table

BTO Item	BOM Structure
Connector	CONN@
45 LEVEL	45@
Unpop	@
nVidia	DIS@
INTEL DD3 M3	M3@
SIM Card Slot	3G@
Intel UMA	UMA@
VRAM Option	X76@
Intel SBA	SBA@
Intel AOAC	AOAC@
TPM	TPM@
GPU N13M	N13M@
GPU N13P	N13MP

SMBUS Control Table

	SOURCE	VGA	BATT	KE9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	KB9012 +3VALW	X	V +3VALW	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB9012 +3VALW	X	X	X	X	X	X	V +3VS
SMBCLK SMBDATA	PCH +3VALW	X	X	X	V +3VS	V +3VS	X	X
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VS	X	V +3VS	X	X	V +3VS	X

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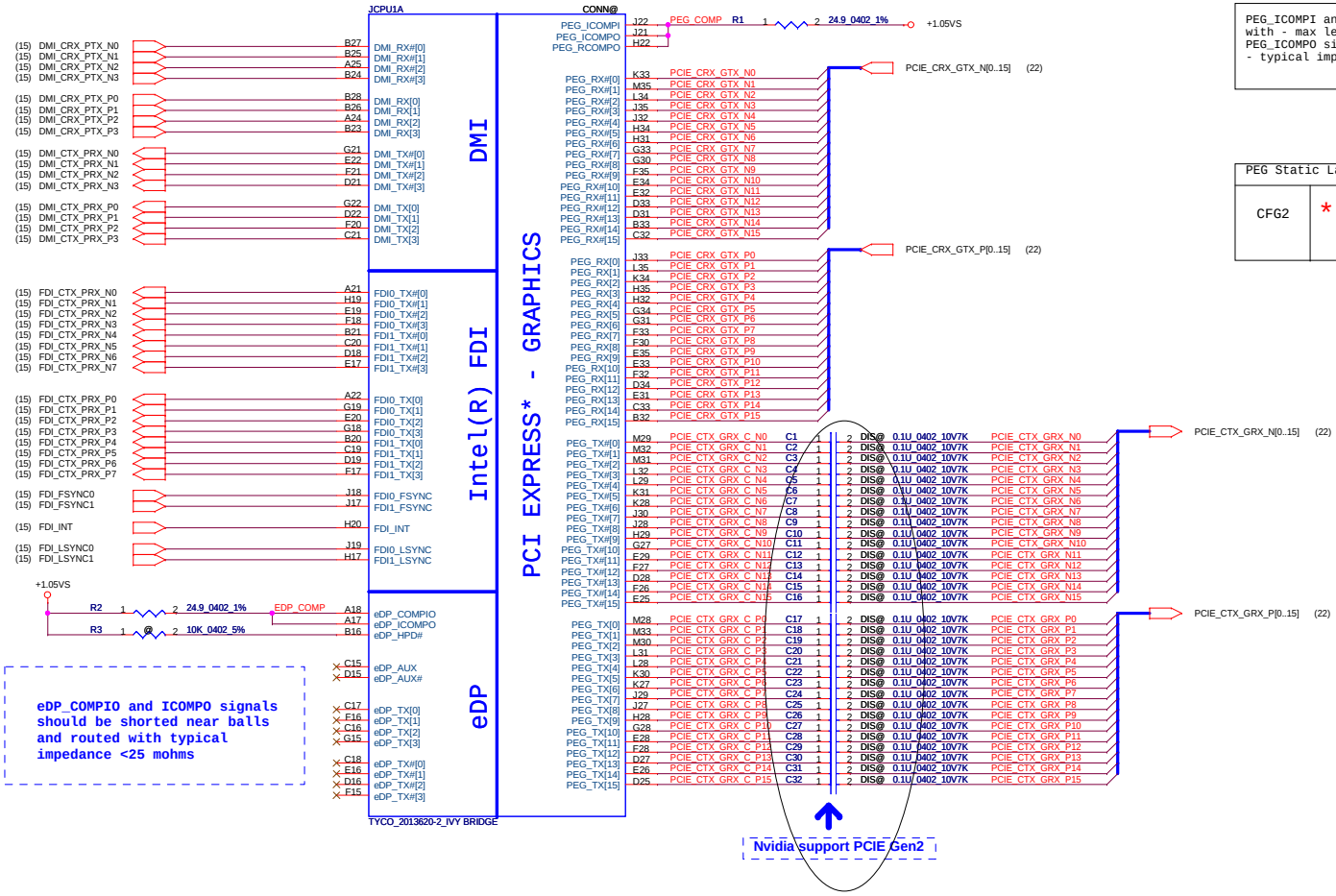
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: Notes List

Size: Custom | Document Number: LA-8133P | Rev: 1.0

Date: Friday, January 13, 2012 | Sheet 3 of 58



PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	* 1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

Nvidia support PCIE Gen2

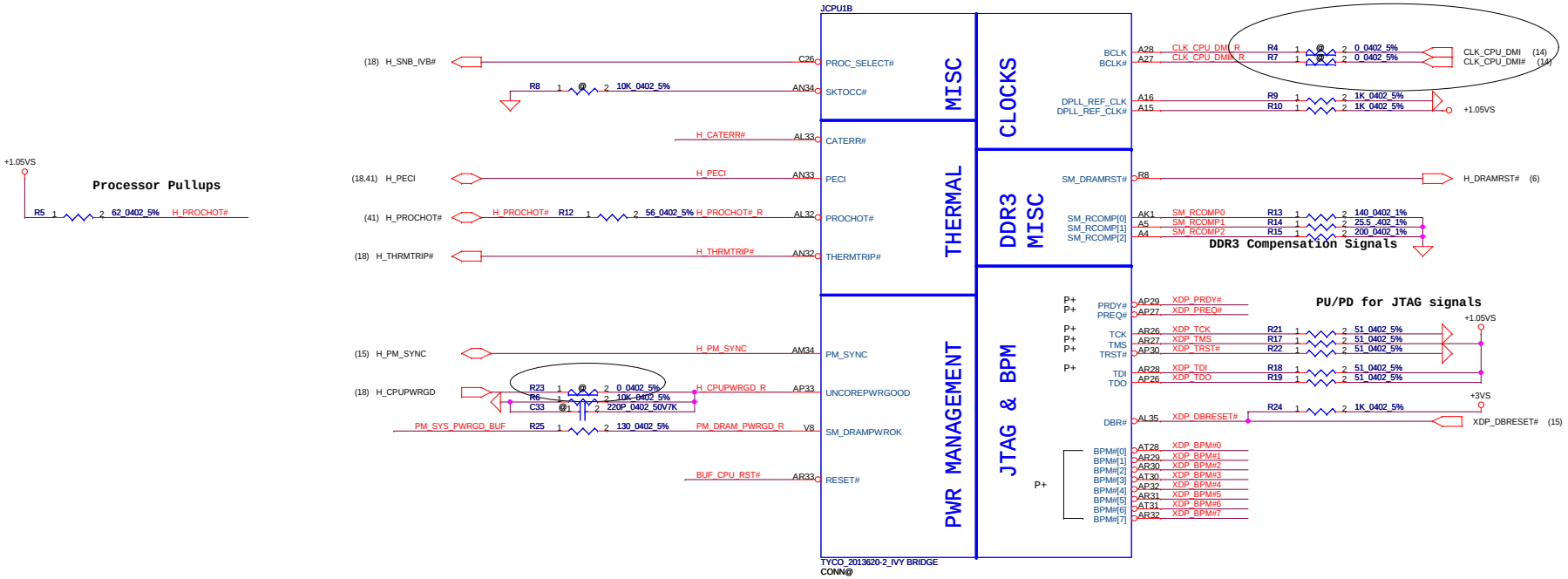
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

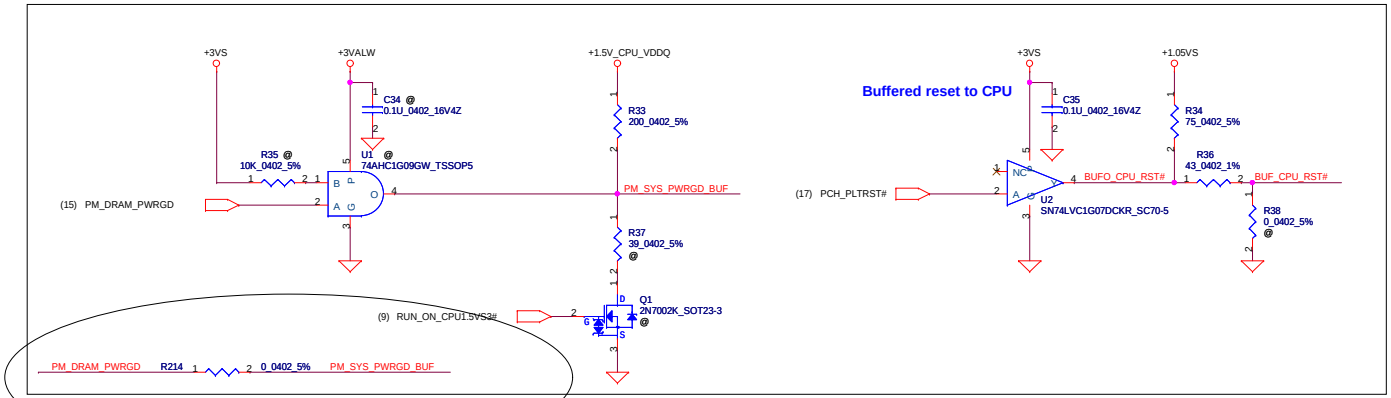
Compal Electronics, Inc.

Title: PROCESSOR(1/7) DMI,FDI,PEG

Size: Custom | Document Number: LA-8133P | Rev: 1.0

Date: Friday, January 13, 2012 | Sheet 4 of 58





For 26 Pin XDP Conn.

(18) H_CPUPWRGD	R26 @	1K_0402_1%	
(15,41) PBTN_OUT#	R27 @	0_0402_5%	
(7) XDP_CFG0	R28 @	1K_0402_1%	
(15) SYS_PWROK	R29 @	0_0402_5%	
(14) CLK_XDP_CLK	R30 @	0_0402_5%	
(14) CLK_XDP_CLK#	R31 @	0_0402_5%	
(14,17,22,36,38,40,41) PLT_RST#	PLT_RST# R32 @	1K_0402_1%	

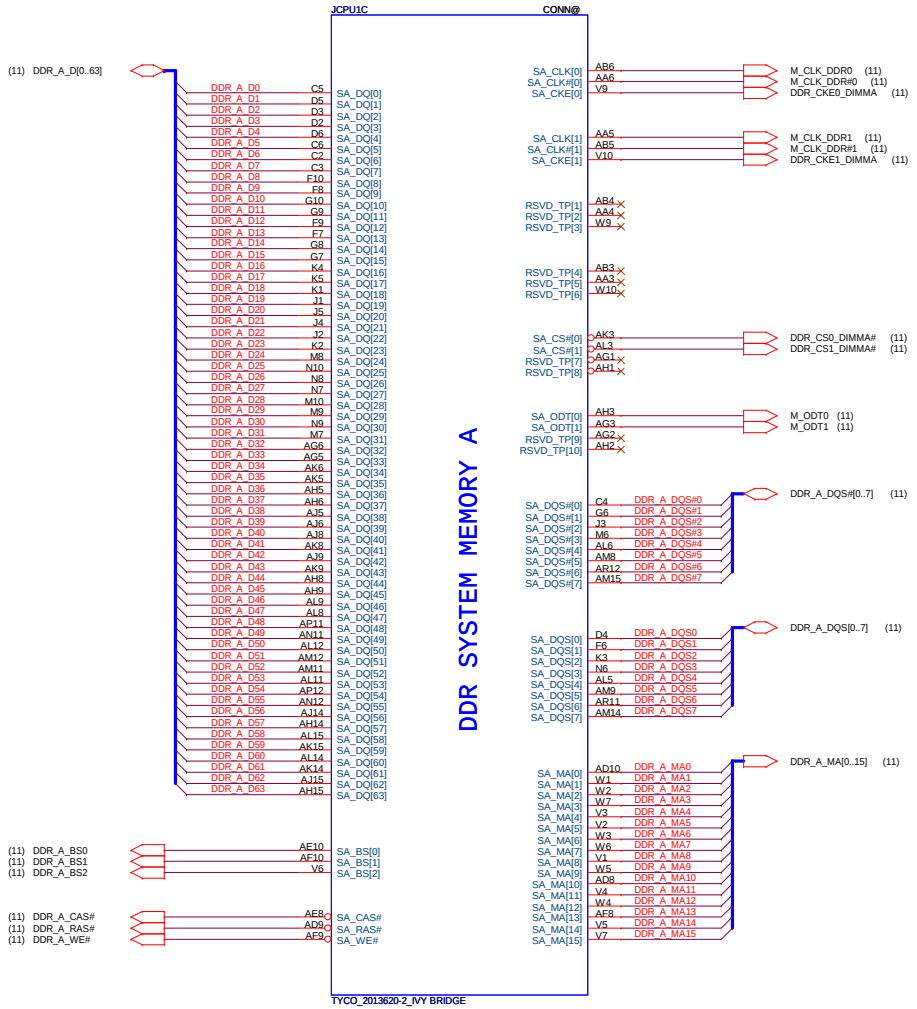
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

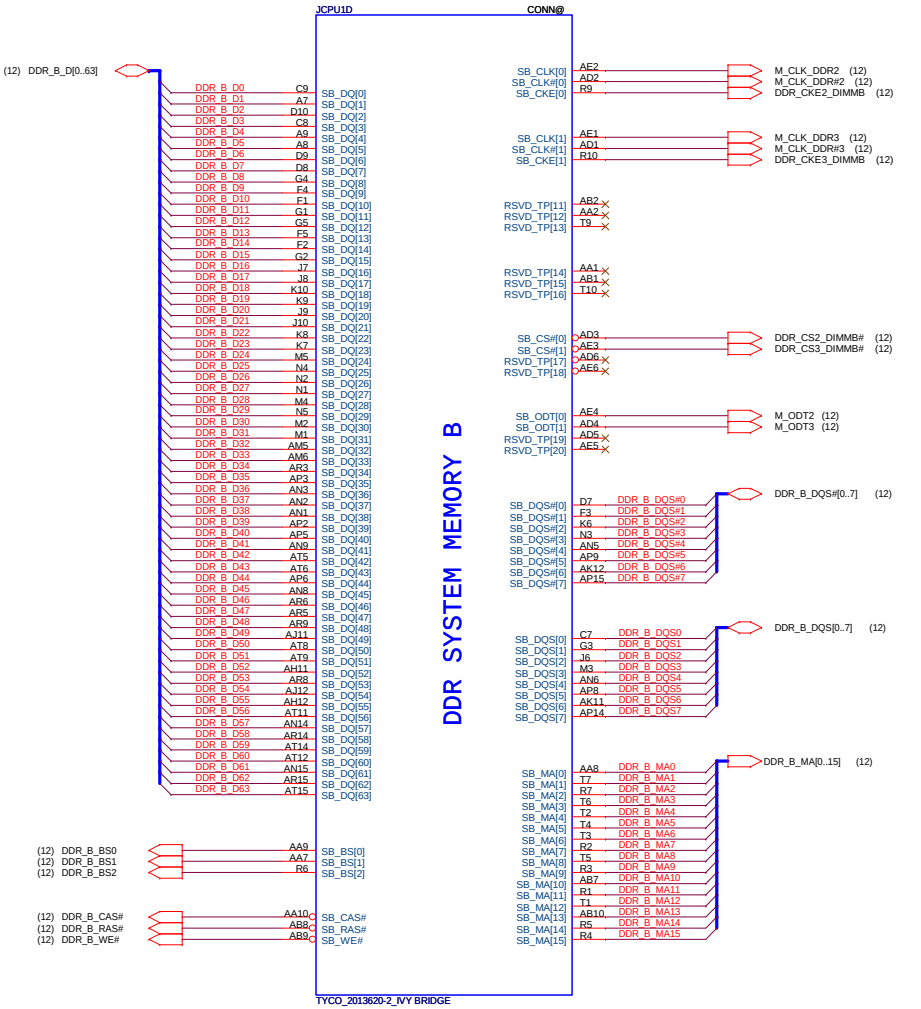
Compal Electronics, Inc.

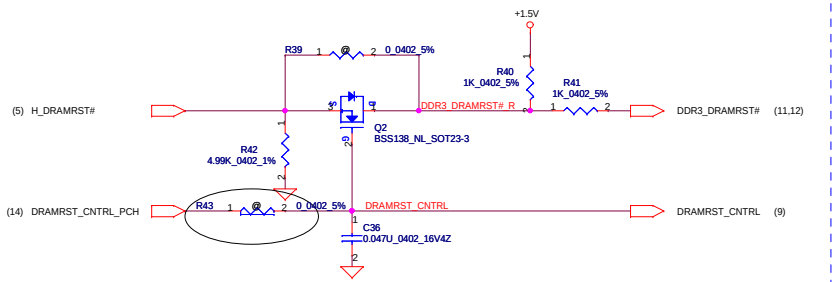
Title: PROCESSOR(2/7) PM,XDP,CLK

Size	Document Number	Rev
Custom	LA-8133P	1.0

Date: Friday, January 13, 2012 Sheet 5 of 58







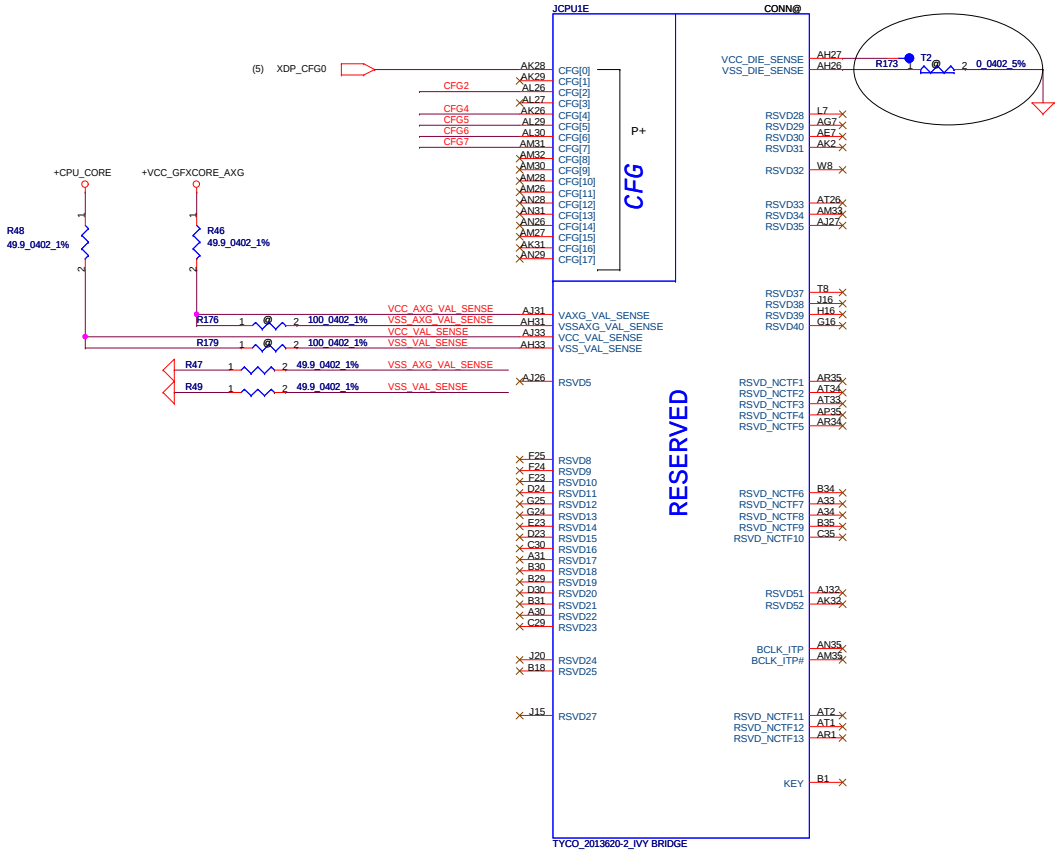
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: **PROCESSOR(3/7) DDRIII**

Size	Document Number	Rev
Custom	LA-8133P	1.0

Date: Friday, January 13, 2012 | Sheet 6 of 58



CFG Straps for Processor

CFG2

R45
1K_0402_1%
@

PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	* 1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed

CFG4

@R50
1K_0402_1%

Display Port Presence Strap

CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

CFG6
CFG5

@R51
1K_0402_1%

@R52
1K_0402_1%

PCIE Port Bifurcation Straps

CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

CFG7

@R53
1K_0402_1%

PEG DEFER TRAINING

CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

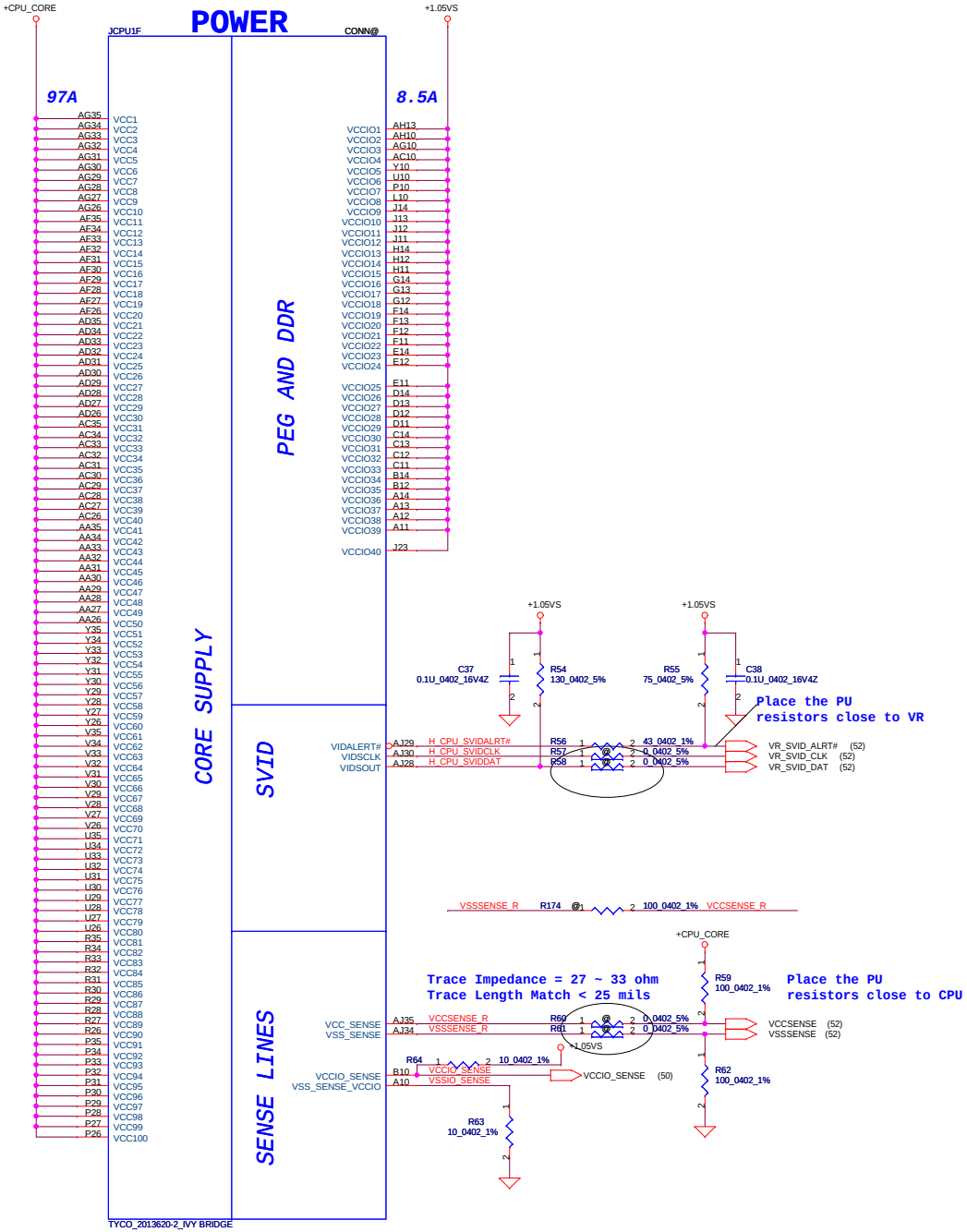
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: PROCESSOR(4/7) RSVD,CFG

Size: Custom | Document Number: LA-8133P | Rev: 1.0

Date: Friday, January 13, 2012 | Sheet 7 of 58



Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

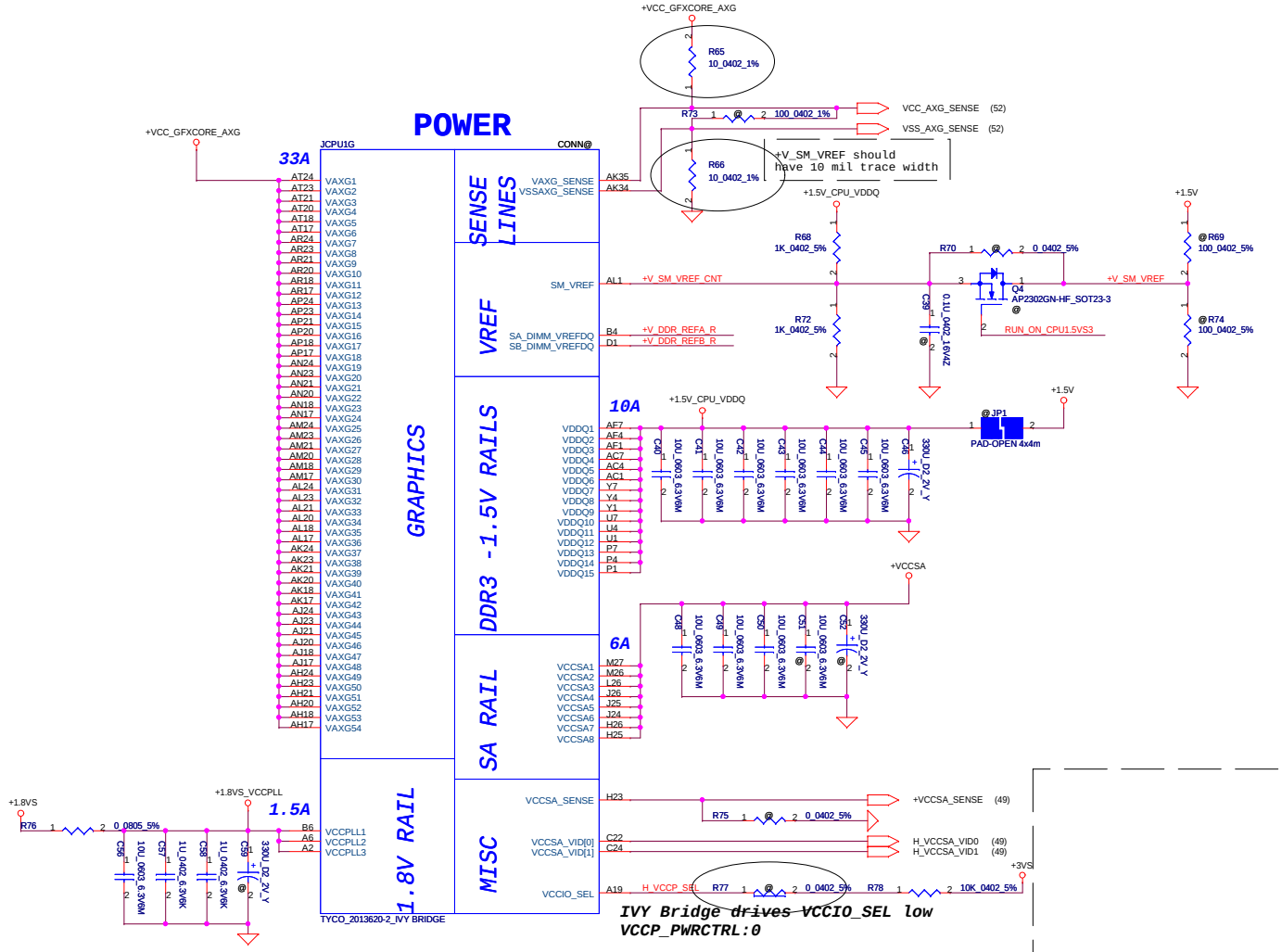
Compal Electronics, Inc.

Title: PROCESSOR(5/7) PWR,BYPASS

Size	Document Number	Rev
Custom	LA-8133P	1.0

Date: Friday, January 13, 2012 Sheet 8 of 58

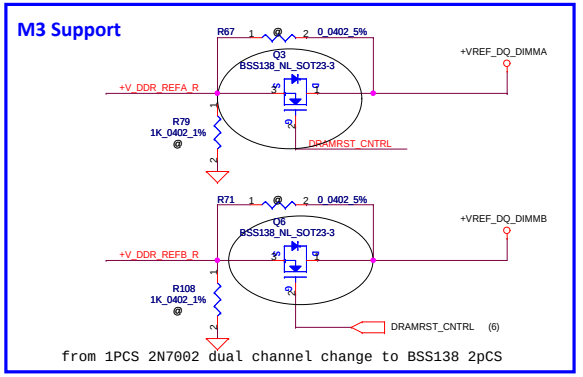
POWER



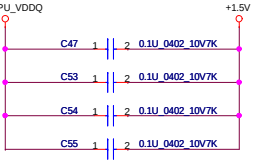
IVY Bridge drives VCCIO_SEL low
VCCP_PWRCTRL:0

Sandy Bridge is NC for A19
VCCP_PWRCTRL:1

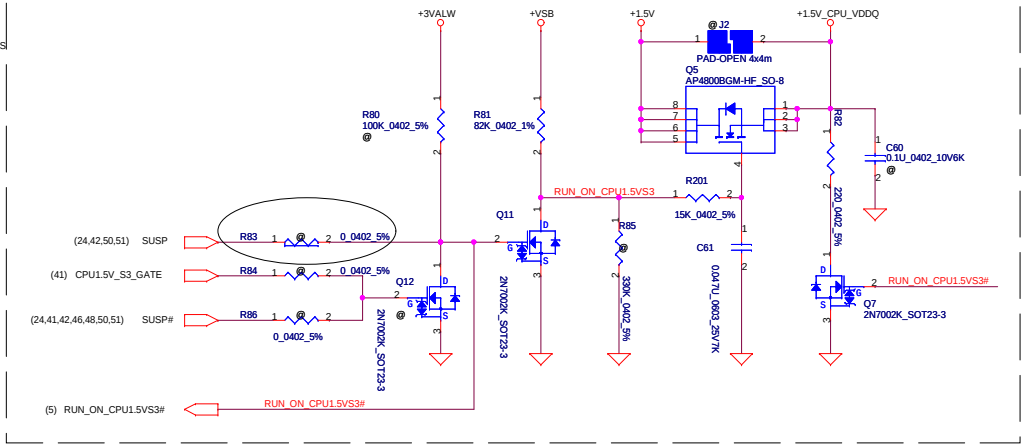
M3 Support



from 1PCS 2N7002 dual channel change to BSS138 2pCS



+1.5V_CPU_VDDQ Source



Vaxg

- Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,
- VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed

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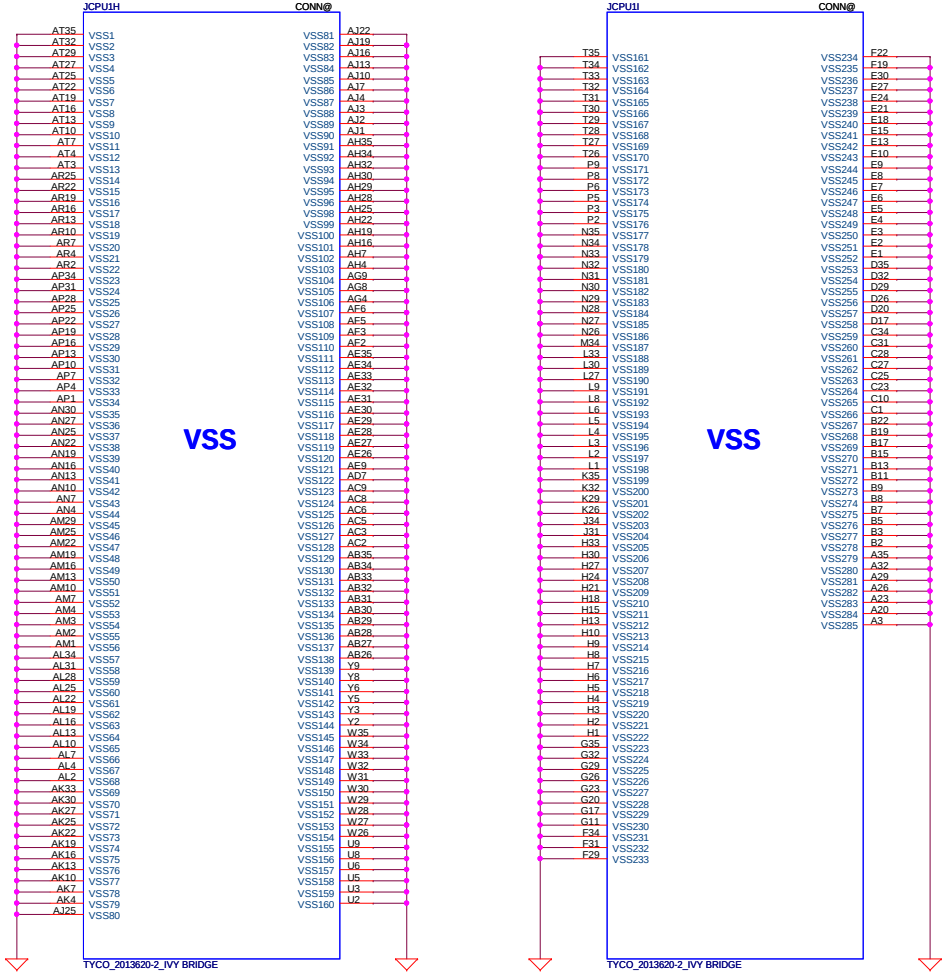
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: **PROCESSOR(6/7) PWR**

Size: Custom | Document Number: **LA-8133P** | Rev: 1.0

Date: Friday, January 13, 2012 | Sheet 9 of 58



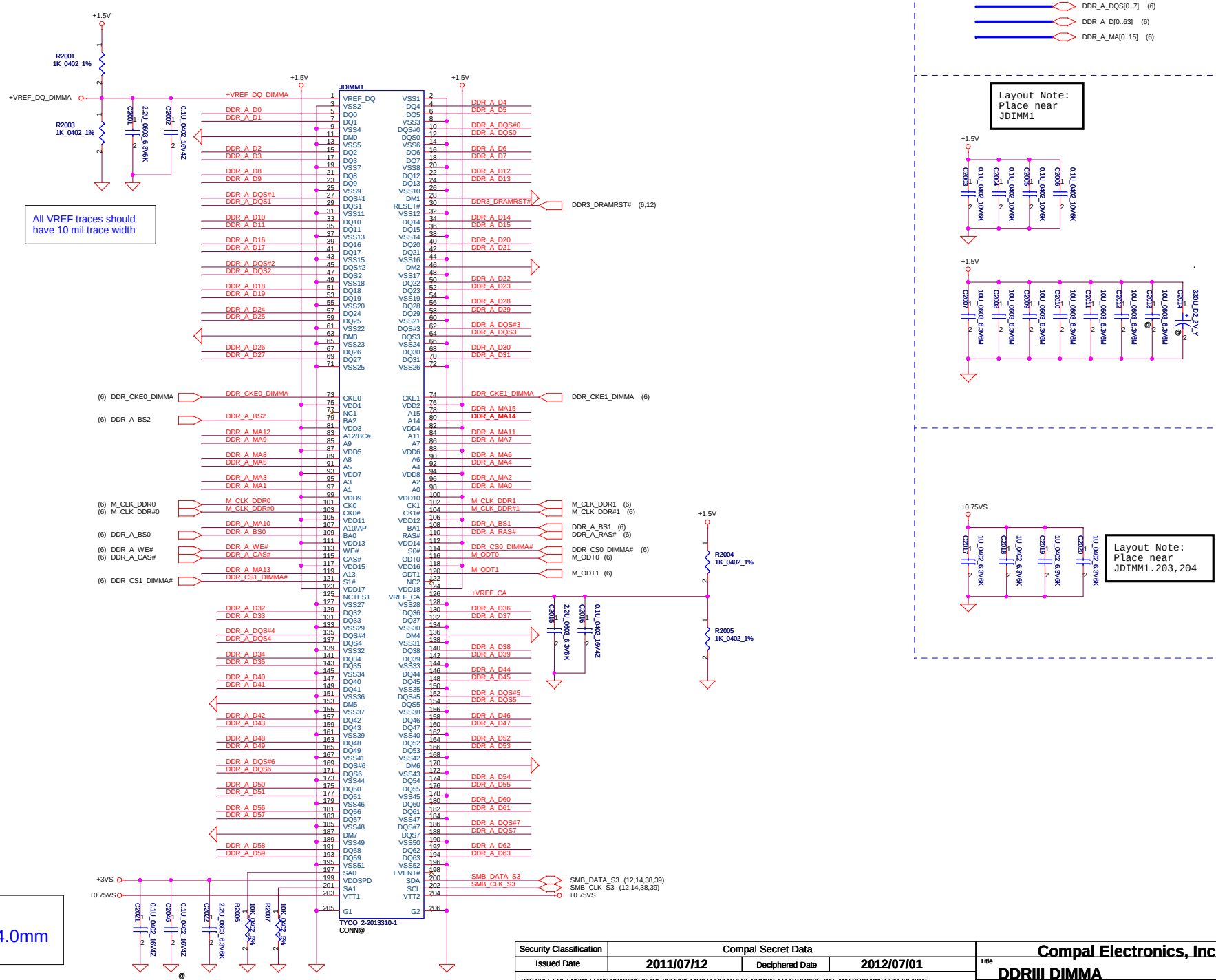
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: **PROCESSOR(7/7) VSS**

Size: Custom | Document Number: **LA-8133P** | Rev: 1.0

Date: Friday, January 13, 2012 | Sheet 10 of 58



<Address: 00>
DIMM_A Reserve H:4.0mm

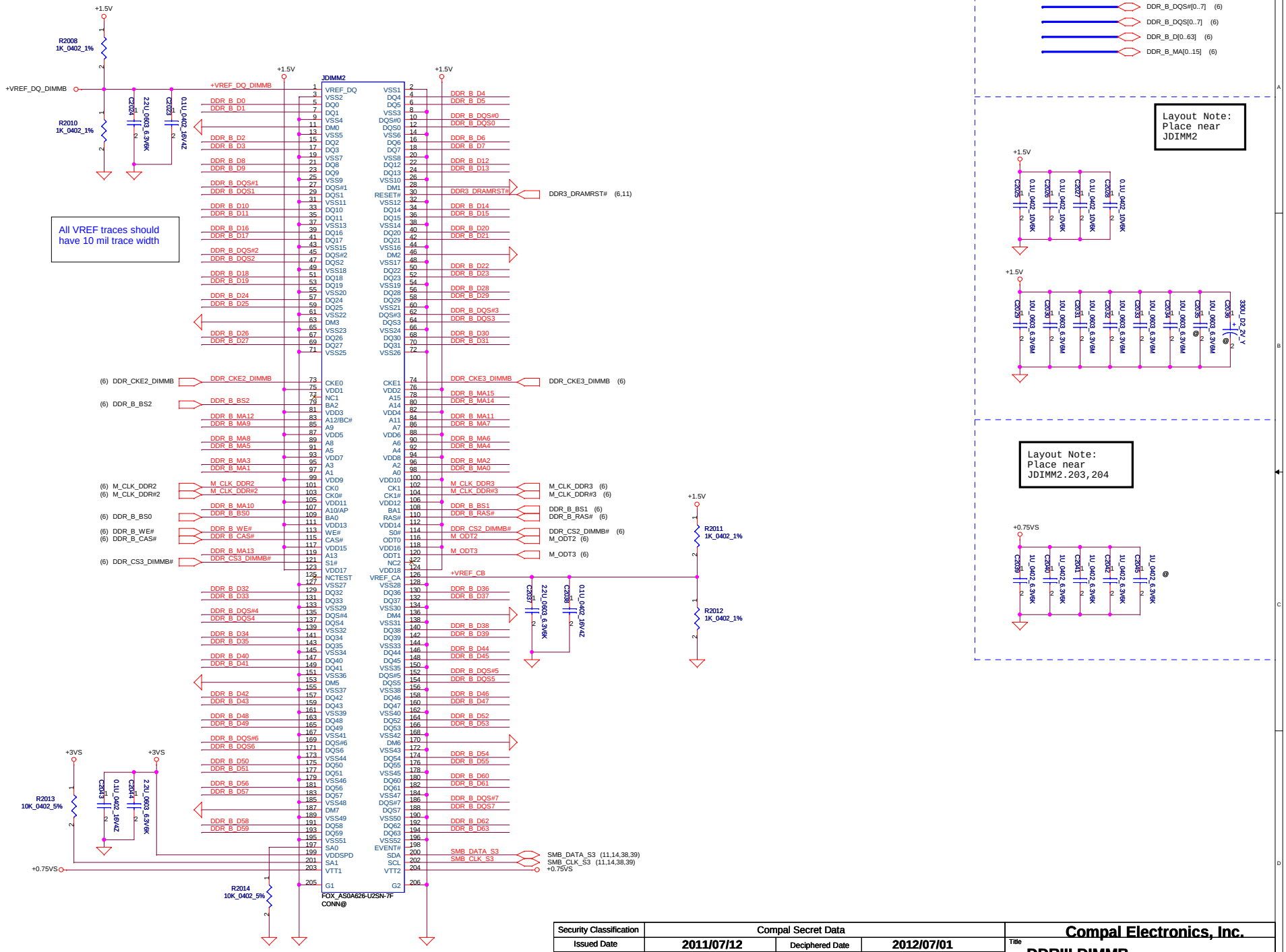
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: DDRIII DIMMA

Size	Document Number	Rev
Custom	LA-8133P	1.0

Date: Friday, January 13, 2012 Sheet 11 of 58



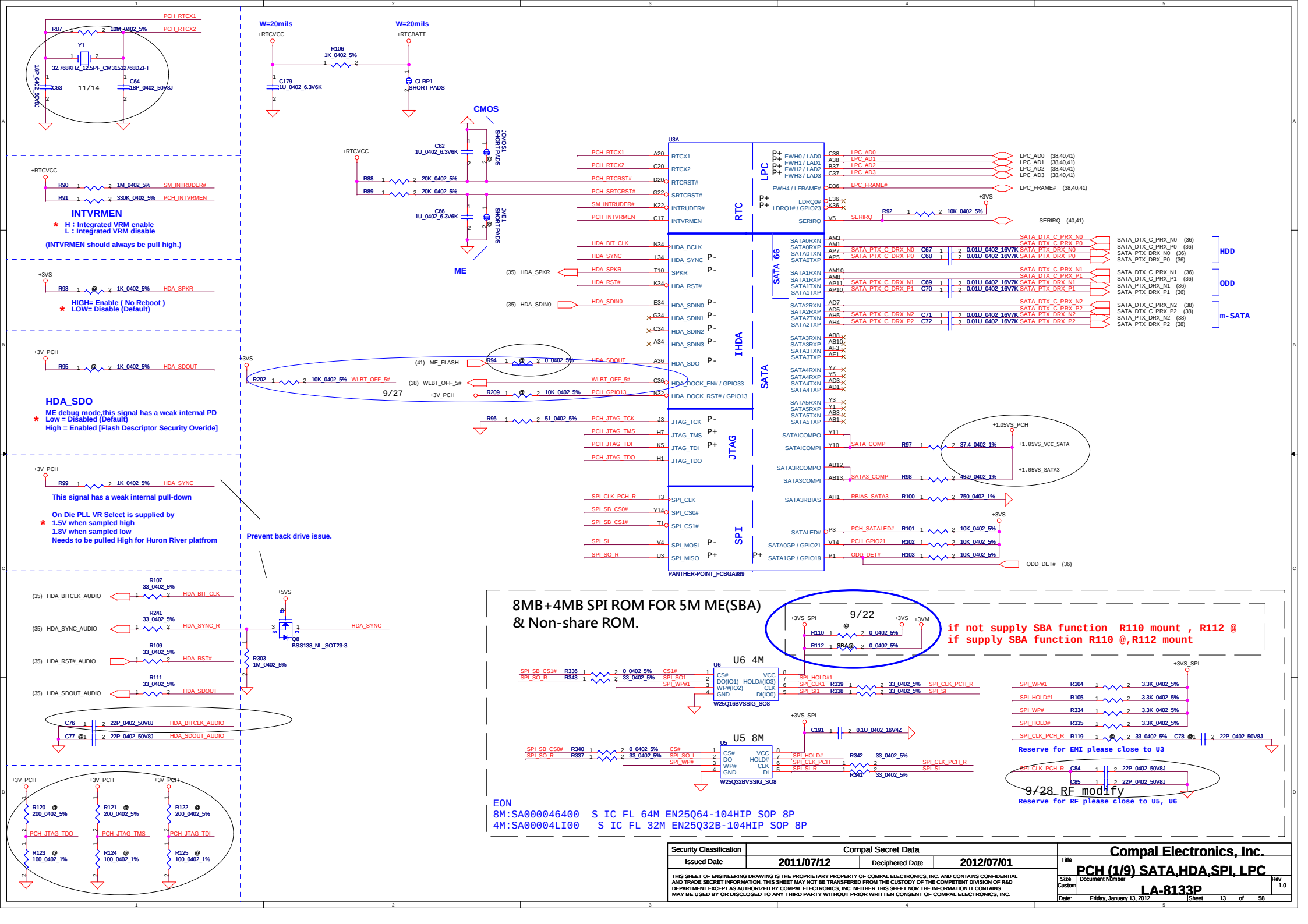
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: **DDRIII DIMMB**

Size	Document Number	Rev
Custom	LA-8133P	1.0

Date: Friday, January 13, 2012 Sheet 12 of 58



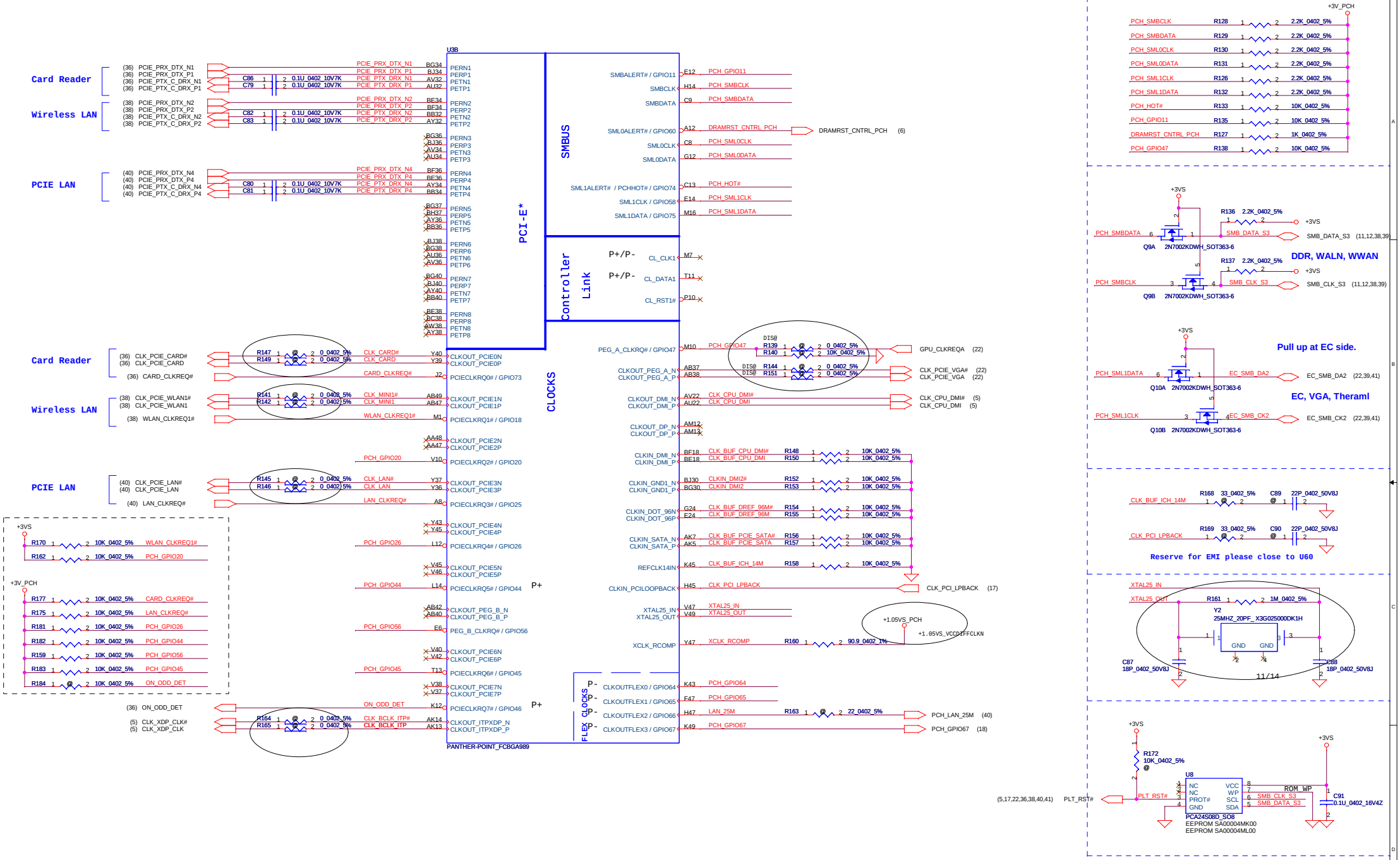
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: PCH (1/9) SATA,HDA,SPI, LPC

Size	Document Number	Rev
Custom	LA-8133P	1.0

Date: Friday, January 13, 2012 Sheet 13 of 58



Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

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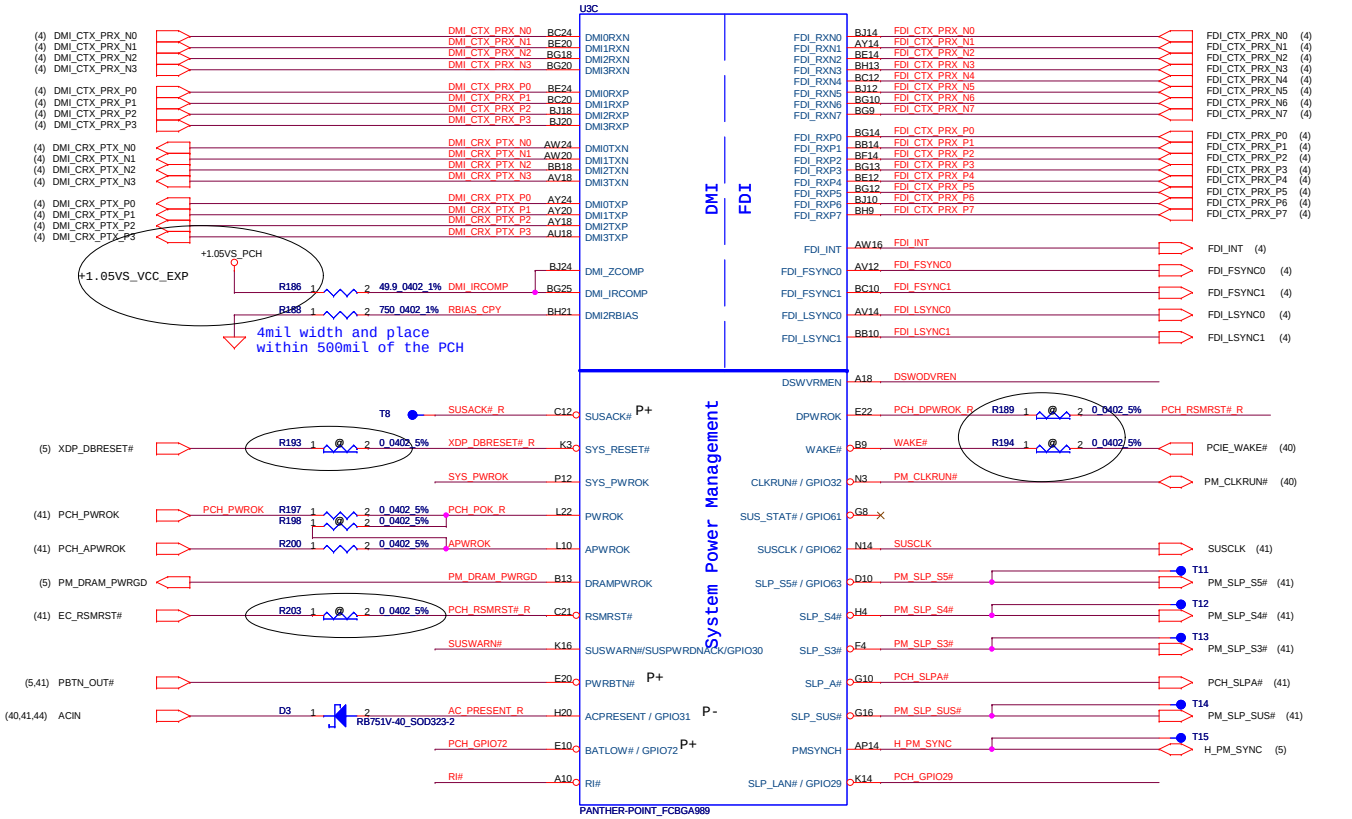
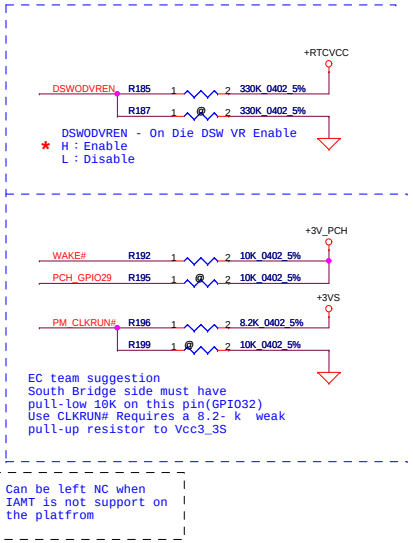
Title: PCH (2/8) PCIE, SMBUS, CLK

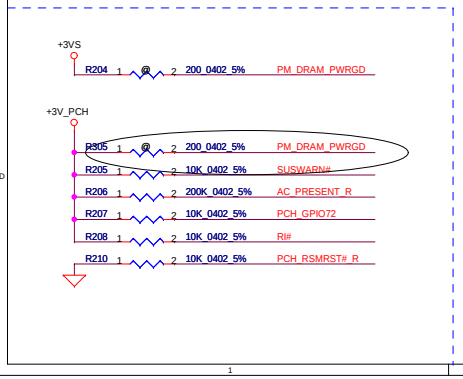
Size: Custom | Document Number: LA-8133P | Rev: 1.0

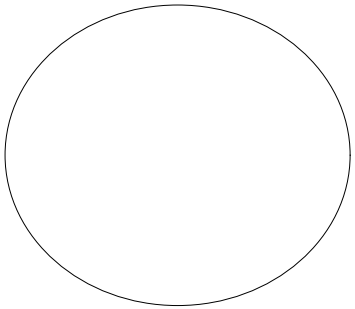
Date: Friday, January 13, 2012 | Sheet 14 of 58

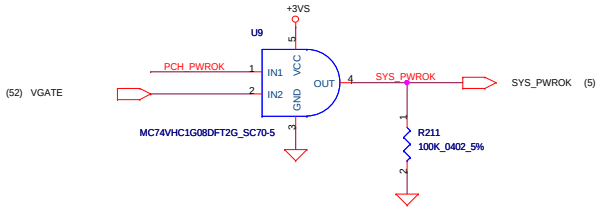




Can be left NC when IAMT is not support on the platfrom







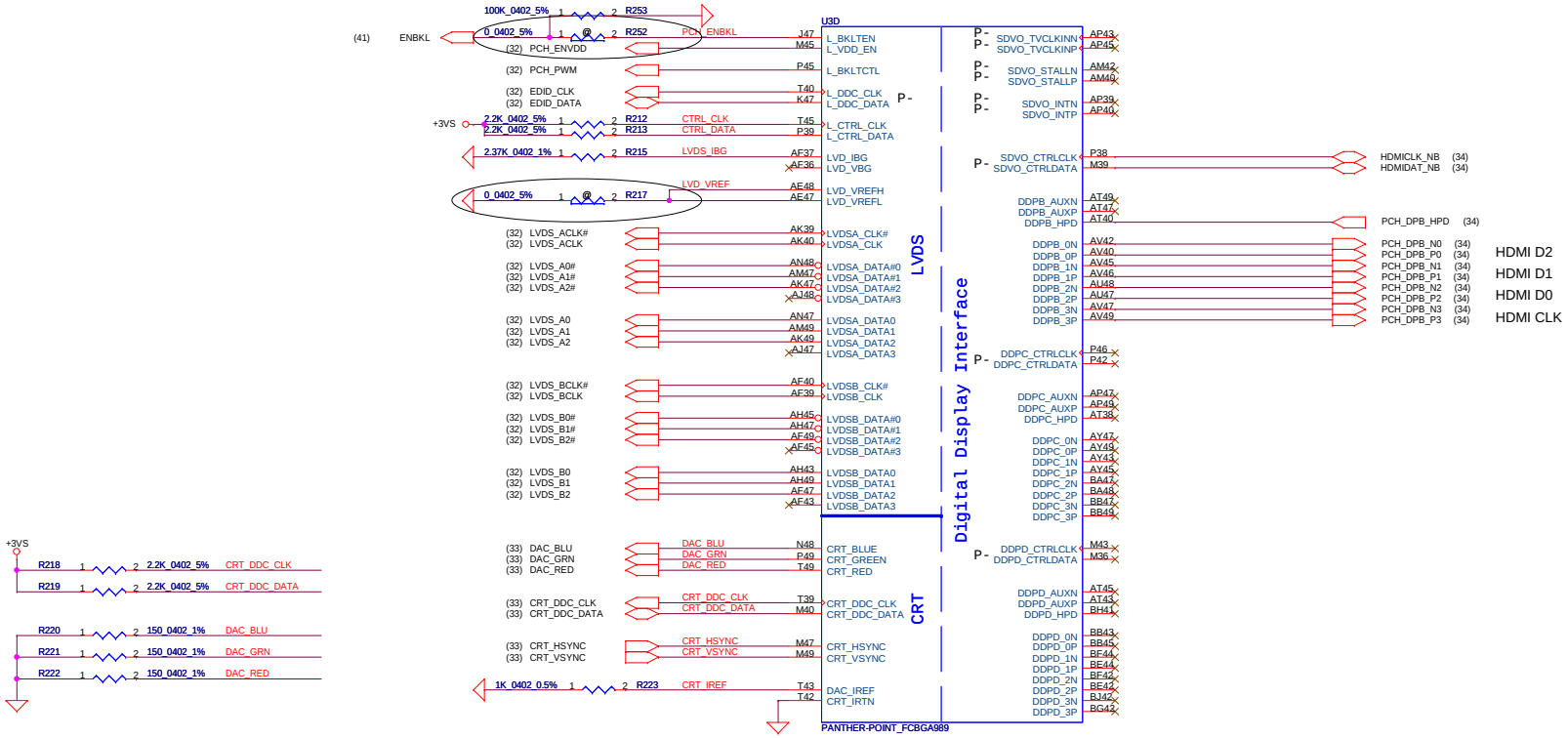
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: PCH (3/8) DMI,FDI,PM,

Size: Custom | Document Number: LA-8133P | Rev: 1.0

Date: Friday, January 13, 2012 | Sheet 15 of 58



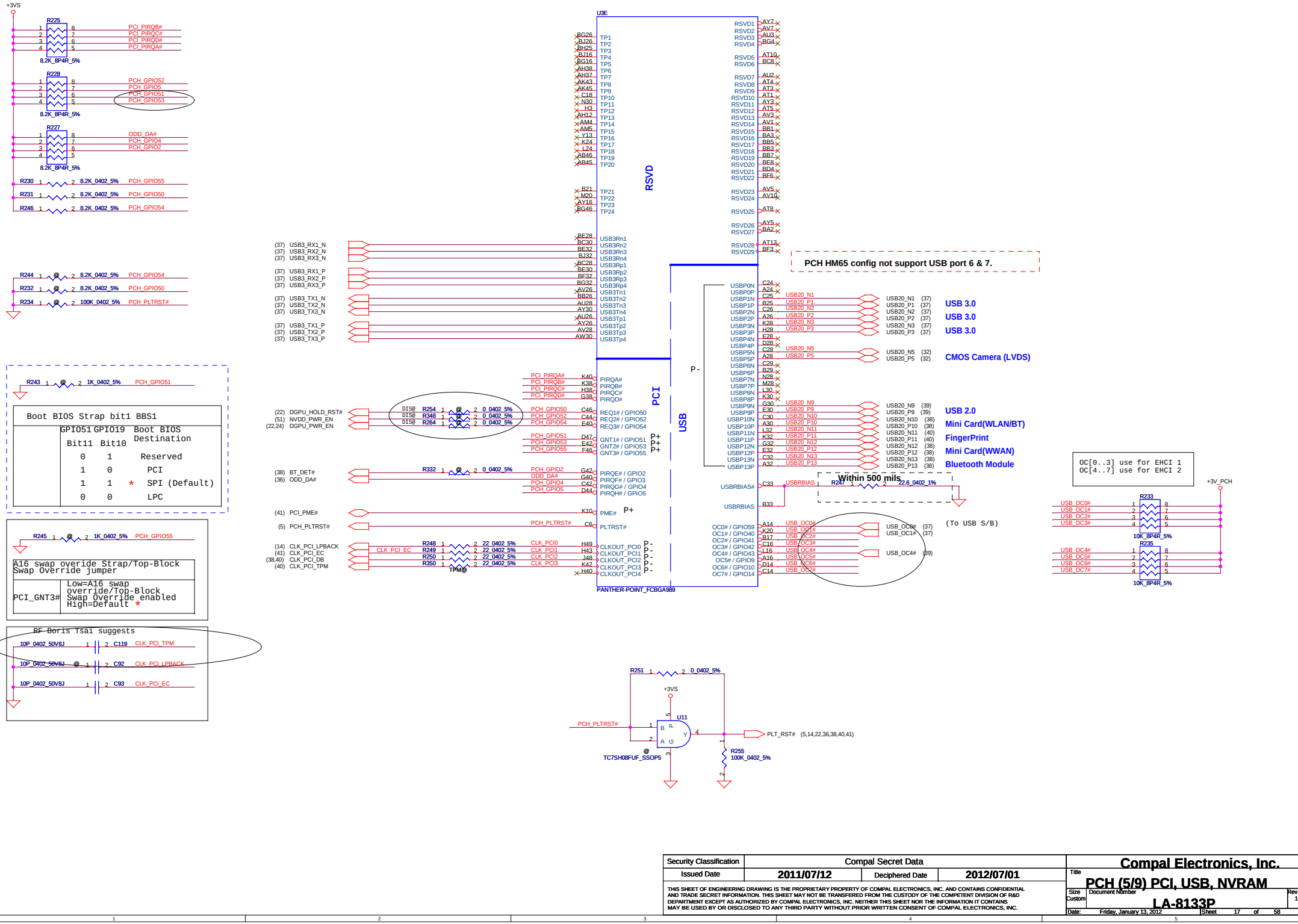
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: **PCH (4/9) LVDS,CRT,DP,HDMI**

Size	Document Number	Rev
Custom	LA-8133P	1.0

Date: Friday, January 13, 2012 Sheet 16 of 58



Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: PCH (5/9) PCI, USB, NVRAM

Size: Custom | Document Number: LA-8133P | Rev: 1.0

Date: Friday, January 13, 2012 | Sheet 17 of 58

GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

* H : On-Die voltage regulator enable
  L : On-Die PLL Voltage Regulator disable

R265 1 @ 2 1K_0402_5% PCH_GPIO28

GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

* H : On-Die voltage regulator enable
  L : On-Die PLL Voltage Regulator disable

R274 1 @ 2 1K_0402_5% EC_SMI#

+3VS
R280 1 @ 2 10K_0402_5%
R282 1 2 10K_0402_5% WLBT_OFF_51#

+3V_PCH
R288 1 2 10K_0402_5%
R290 1 @ 2 10K_0402_5% PCH_GPIO24

+3VS
R285 1 @ 2 10K_0402_5%
R284 1 2 10K_0402_5% PCH_GPIO37

+3VS
R269 1 2 10K_0402_5% PCH_GPIO0
R270 1 2 10K_0402_5% PCH_GPIO1
R266 1 2 10K_0402_5% PCH_GPIO6
R344 1 @ 2 10K_0402_5% EC_SCI#
R275 1 2 10K_0402_5% PCH_GPIO16
R268 1 2 10K_0402_5% DGPU_PWROK
R277 1 2 10K_0402_5% PCH_GPIO22
R346 1 2 10K_0402_5% BT_ON#
R283 1 2 10K_0402_5% 3G_DET#
R287 1 2 10K_0402_5% 3G_OFF#
R289 1 2 10K_0402_5% PCH_GPIO48
R291 1 2 10K_0402_5% PCH_GPIO49

+3V_PCH
R345 1 2 10K_0402_5% EC_SMI#
R271 1 2 10K_0402_5% PCH_GPIO12
R273 1 2 1K_0402_5% PCH_GPIO15
R347 1 2 10K_0402_5% PCH_GPIO28
R292 1 @ 2 10K_0402_5% PCH_GPIO57

U3F

PCH_GPIO0 T7 BMBUSY# / GPIO0
PCH_GPIO1 A42 TACH1 / GPIO1
PCH_GPIO6 H36 TACH2 / GPIO6
EC_SCI# E38 TACH3 / GPIO7
EC_SMI# C10 GPIO8
PCH_GPIO12 C4 LAN_PHY_PWR_CTRL / GPIO12
PCH_GPIO15 G2 GPIO15
PCH_GPIO16 U2 SATA4GP / GPIO16
DGPU_PWROK D40 TACH0 / GPIO17
PCH_GPIO22 T5 SCLOCK / GPIO22
PCH_GPIO24 E8 GPIO24
PCH_GPIO27 E16 GPIO27
PCH_GPIO28 P8 GPIO28
BT_ON# K1 STP_PCI# / GPIO34
3G_DET# K4 GPIO35
WLBT_OFF_51# V8 SATA2GP / GPIO36
PCH_GPIO37 M5 SATA3GP / GPIO37
PCH_GPIO38 N2 SLOAD / GPIO38
3G_OFF# M3 SDATAOUT0 / GPIO39
PCH_GPIO48 V13 SDATAOUT1 / GPIO48
PCH_GPIO49 V3 SATA5GP / GPIO49 / TEMP_ALERT#
PCH_GPIO57 D6 GPIO57

TACH4 / GPIO68 C40 ODD_EN#
TACH5 / GPIO69 B41 PCH_GPIO69
TACH6 / GPIO70 C41 PCH_GPIO70
TACH7 / GPIO71 A40 PCH_GPIO71

A20GATE P4 GATEA20 (41)
PECI AU16 PCH_PECI_R R267 1 @ 2 0_0402_5% H_PECI (5,41)
RCIN# P5 KB_RST# KB_RST# (41)
PROCPWRGD AY11 H_CPUPWRGD H_CPUPWRGD (5)
THRMTRIP# AY10 R278 1 2 390_0402_5% H_THRMTRIP# H_THRMTRIP# (5)
INIT3_3V# T14 VGA_THRMTRIP# (22)
DF_TVS AY1 DF_TVS

GPIO
CPU/MISC
NCTF

TS_VSS1 AH8
TS_VSS2 AK11
TS_VSS3 AH10
TS_VSS4 AK10
NC_1 P37

VSS_NCTF_1 A4
VSS_NCTF_2 A44
VSS_NCTF_3 A45
VSS_NCTF_4 A46
VSS_NCTF_5 A5
VSS_NCTF_6 A6
VSS_NCTF_7 B3
VSS_NCTF_8 B47
VSS_NCTF_9 BD1
VSS_NCTF_10 BD49
VSS_NCTF_11 BE1
VSS_NCTF_12 BE49
VSS_NCTF_13 BF1
VSS_NCTF_14 BF49

VSS_NCTF_15 BG2 T18
VSS_NCTF_16 BG48 T19
VSS_NCTF_17 BH3 T20
VSS_NCTF_18 BH47 T21
VSS_NCTF_19 BJ4 T23
VSS_NCTF_20 BJ44 T25
VSS_NCTF_21 BJ45 T27
VSS_NCTF_22 BJ46 T29
VSS_NCTF_23 BJ5 T31
VSS_NCTF_24 BJ6 T33
VSS_NCTF_25 C2 T35
VSS_NCTF_26 C48 T37
VSS_NCTF_27 D1 T39
VSS_NCTF_28 D49 T41
VSS_NCTF_29 E1 T43
VSS_NCTF_30 F49 T45
VSS_NCTF_31 F1 T47
VSS_NCTF_32 F49 T49

PANTHER-POINT_FCBGA989

(41) EC_SCI#
(41) EC_SMI#
EC_WAKE# R178 1 @ 2 0_0402_5%
(41) EC_WAKE# R167 1 2 0_0402_5%
(24,51) DGPU_PWROK
(38) BT_ON#
(38) 3G_DET#
(38) WLBT_OFF_51#
(38) 3G_OFF#
(38) mSATA_PCH R293 1 @ 2 0_0402_5%
(41) mSATA_DETEC# R294 1 2 10K_0402_5%

ODD_EN# (36)

INIT3_3V
This signal has weak internal PU, can't pull low

Intel schematic reviwe recommand.

ODD_EN# R256 1 2 8.2K_0402_5%
R260 1 @ 2 8.2K_0402_5%
PCH_GPIO70 R258 2 1 10K_0402_5%
R262 1 @ 2 10K_0402_5%
PCH_GPIO71 R257 2 1 10K_0402_5%
R263 1 @ 2 10K_0402_5%
GATEA20 R272 1 2 10K_0402_5%
KB_RST# R276 1 2 10K_0402_5%

+1.8VS
R226 2.2K_0402_5%
DF_TVS R229 1 2 1K_0402_5% H_SNB_IVB# (5)

DMI Termination Voltage	
NV_CLE	Set to Vcc when HIGH
	Set to Vss when LOW

CLOSE TO THE BRANCHING POINT

For Edge code setting

PCH_GPIO69	PCH_GPIO38	PCH_GPIO67	Function
0	0	0	Optimus
0	0	1	Reserved
0	1	0	DIS
0	1	1	UMA

+3VS
R259 10K_0402_5% @
R330 10K_0402_5% UMA@
R311 10K_0402_5% UMA@
R261 10K_0402_5%
R329 10K_0402_5% DIS@
R286 10K_0402_5% DIS@
PCH_GPIO69
PCH_GPIO38
PCH_GPIO67
PCH_GPIO67 (14)
{MB_ID_2}
{MB_ID_1}
{MB_ID_0}

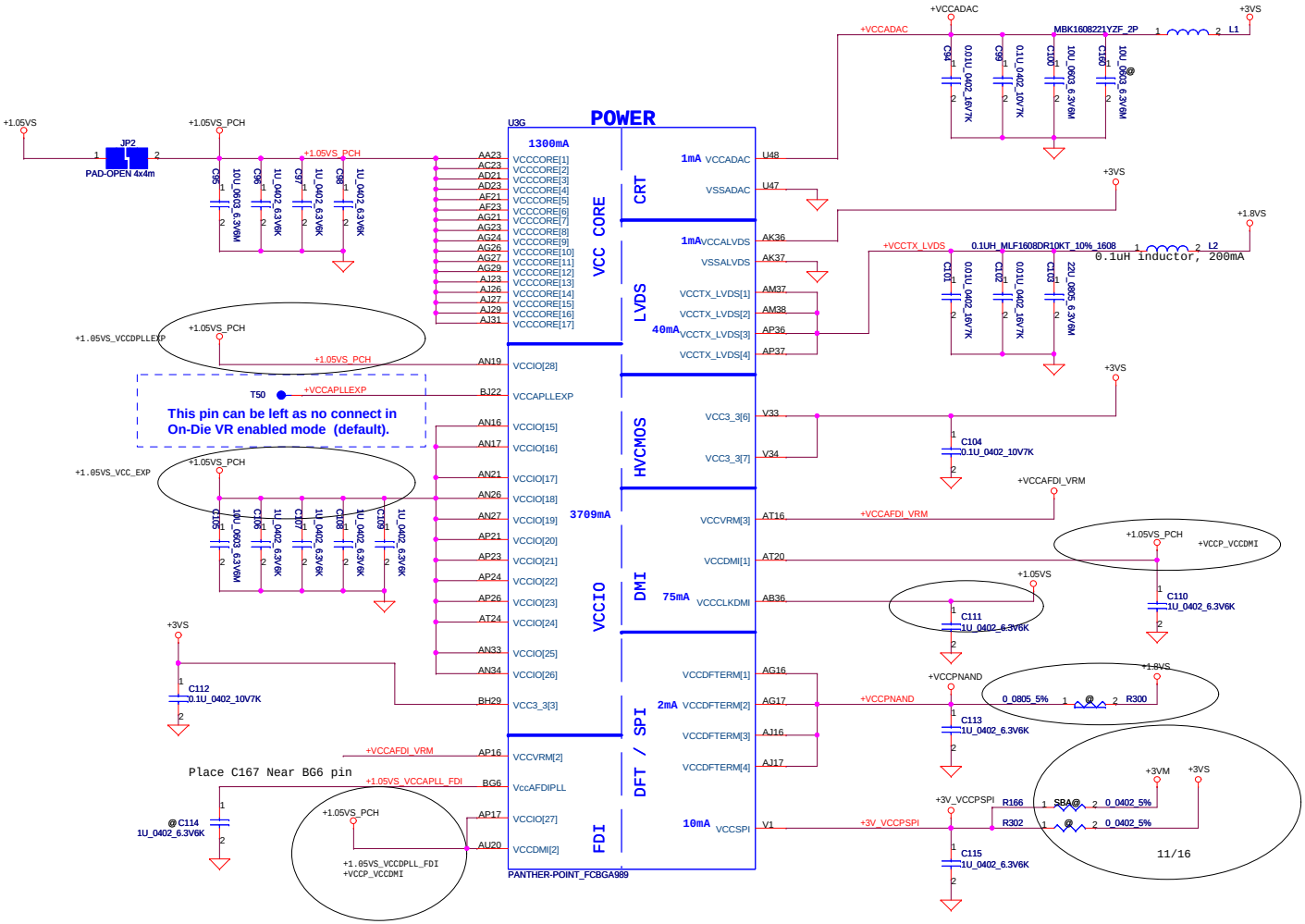
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: PCH (6/9) GPIO, CPU, MISC

Size: Custom | Document Number: LA-8133P | Rev: 1.0

Date: Friday, January 13, 2012 | Sheet 18 of 58



Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: PCH (7/9) PWR

Size: Custom | Document Number: LA-8133P | Rev: 1.0

Date: Friday, January 13, 2012 | Sheet 19 of 58

VCC3_3 = 266mA detal waiting for newest spec
VCCDMI = 42mA detal waiting for newest spec

Have internal VRM

If platform does not support Deep S4/S5 then tie to VccSus3_3.

if not supply SBA R316 mount , R349 @
if supply SBA R316 @,R349 mount

Ensure independent power routing for SSC and DIFFCLKN

Place C199 Near AK1 pin

POWER

U3J

PANTHER-POINT_FCBGA989

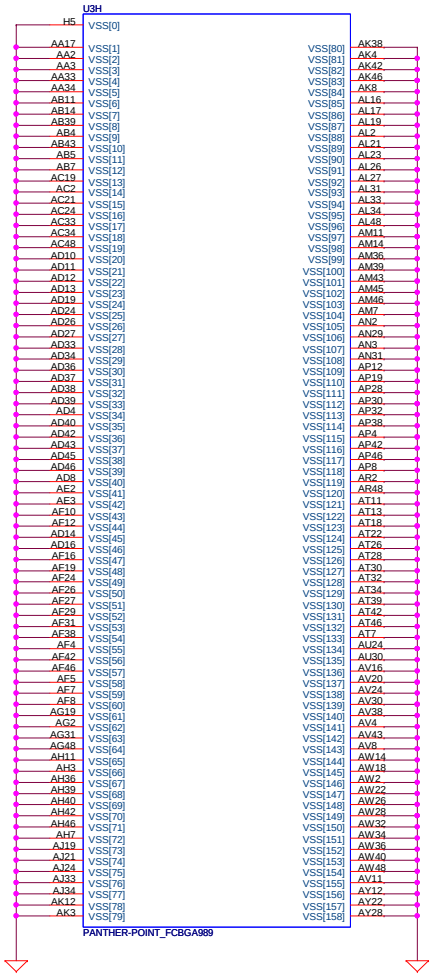
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

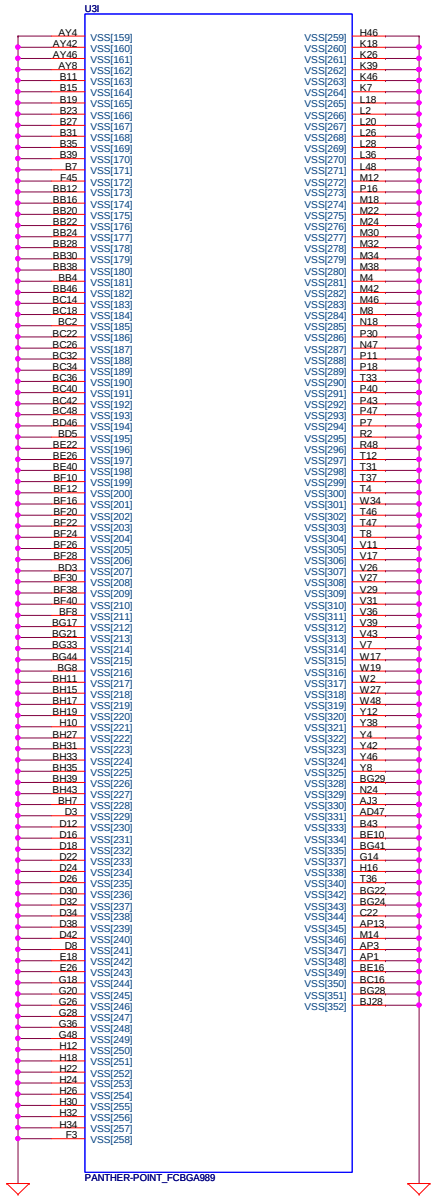
Compal Electronics, Inc.

Title: PCH (8/9) PWR

Size: Custom | Document Number: LA-8133P | Rev: 1.0

Date: Friday, January 13, 2012 | Sheet 20 of 58





Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: **PCH (9/9) VSS**

Size	Document Number	Rev
Custom	LA-8133P	1.0

Date: Friday, January 13, 2012 Sheet 21 of 58

(4) PCIE_CTX_GRX_N[0..15]
(4) PCIE_CTX_GRX_P[0..15]
(4) PCIE_CRX_GTX_N[0..15]
(4) PCIE_CRX_GTX_P[0..15]

PCIE_CTX_GRX_N[0..15]
PCIE_CTX_GRX_P[0..15]
PCIE_CRX_GTX_N[0..15]
PCIE_CRX_GTX_P[0..15]

U1401A

Part 1 of 7

PCIE_CTX_GRX_P0 AN12
PCIE_CTX_GRX_N0 AM12
PCIE_CTX_GRX_P1 AN14
PCIE_CTX_GRX_N1 AM14
PCIE_CTX_GRX_P2 AP14
PCIE_CTX_GRX_N2 AP15
PCIE_CTX_GRX_P3 AN15
PCIE_CTX_GRX_N3 AM15
PCIE_CTX_GRX_P4 AN17
PCIE_CTX_GRX_N4 AM17
PCIE_CTX_GRX_P5 AP17
PCIE_CTX_GRX_N5 AP18
PCIE_CTX_GRX_P6 AN18
PCIE_CTX_GRX_N6 AM18
PCIE_CTX_GRX_P7 AN20
PCIE_CTX_GRX_N7 AM20
PCIE_CTX_GRX_P8 AP20
PCIE_CTX_GRX_N8 AP21
PCIE_CTX_GRX_P9 AN21
PCIE_CTX_GRX_N9 AM21
PCIE_CTX_GRX_P10 AN23
PCIE_CTX_GRX_N10 AM23
PCIE_CTX_GRX_P11 AP23
PCIE_CTX_GRX_N11 AP24
PCIE_CTX_GRX_P12 AN24
PCIE_CTX_GRX_N12 AM24
PCIE_CTX_GRX_P13 AN26
PCIE_CTX_GRX_N13 AM26
PCIE_CTX_GRX_P14 AP26
PCIE_CTX_GRX_N14 AP27
PCIE_CTX_GRX_P15 AN27
PCIE_CTX_GRX_N15 AM27

PEX_RX0 PEX_RX0_N PEX_RX1 PEX_RX1_N PEX_RX2 PEX_RX2_N PEX_RX3 PEX_RX3_N PEX_RX4 PEX_RX4_N PEX_RX5 PEX_RX5_N PEX_RX6 PEX_RX6_N PEX_RX7 PEX_RX7_N PEX_RX8 PEX_RX8_N PEX_RX9 PEX_RX9_N PEX_RX10 PEX_RX10_N PEX_RX11 PEX_RX11_N PEX_RX12 PEX_RX12_N PEX_RX13 PEX_RX13_N PEX_RX14 PEX_RX14_N PEX_RX15 PEX_RX15_N

PEX_TX0 PEX_TX0_N PEX_TX1 PEX_TX1_N PEX_TX2 PEX_TX2_N PEX_TX3 PEX_TX3_N PEX_TX4 PEX_TX4_N PEX_TX5 PEX_TX5_N PEX_TX6 PEX_TX6_N PEX_TX7 PEX_TX7_N PEX_TX8 PEX_TX8_N PEX_TX9 PEX_TX9_N PEX_TX10 PEX_TX10_N PEX_TX11 PEX_TX11_N PEX_TX12 PEX_TX12_N PEX_TX13 PEX_TX13_N PEX_TX14 PEX_TX14_N PEX_TX15 PEX_TX15_N

PEX_WAKE_N AJ11

PEX_REFCLK PEX_REFCLK_N PEX_CLKREQ_N

PEX_TSTCLK_OUT AJ26
PEX_TSTCLK_OUT_N AK26

PEX_RST_N AJ12
PEX_TERMP AP29

PCI EXPRESS

GPIO

GPIO0 P6 GPU_VID4
GPIO1 M3 GPU_VID3
GPIO2 L6 VGA_BL_PWM
GPIO3 P5 VGA_ENVDD
GPIO4 P7 VGA_ENBKL
GPIO5 L7 GPU_VID1
GPIO6 M7 GPU_VID2
GPIO7 N8
GPIO8 M1 OVERT#
GPIO9 M2 THERM#_VGA
GPIO10 L1
GPIO11 M5 GPU_VID0
GPIO12 N3 VGA_GPIO12
GPIO13 M4 GPU_VID5
GPIO14 N4
GPIO15 P2 VGA_GPIO15
GPIO16 R8 VGA_GPIO16
GPIO17 M6
GPIO18 R1
GPIO19 P3
GPIO20 P4
GPIO21 P1

GPU_VID4 (51)
GPU_VID3 (51)
DPRSLPVR_VGA (51)
GPU_VID1 (51)
GPU_VID2 (51)
GPU_VID0 (51)
VGA_AC_DET (41,51)
GPU_VID5 (51)
DPRSLPVR_VGA (51)

R1429 @ 0_0402_5%
D2414 RB751V-40_SOD323-2 DIS@
R1430 @ 0_0402_5%

DACs

DACA_RED AK9
DACA_GREEN AL10
DACA_BLUE AL9
DACA_HSYNC AM9
DACA_VSYNC AN9
DACA_VDD AG10
DACA_VREF AP9
DACA_RSET AP8

R1448 DIS@ 10K_0402_5%

I2C

I2CA_SCL R4 I2CA_SCL R1452 DIS@ 2.2K_0402_5%
I2CA_SDA R5 I2CA_SDA R1460 DIS@ 2.2K_0402_5%
I2CB_SCL R7 I2CB_SCL R1406 DIS@ 2.2K_0402_5%
I2CB_SDA R6 I2CB_SDA R1407 DIS@ 2.2K_0402_5%
I2CC_SCL R2 I2CC_SCL R1402 DIS@ 2.2K_0402_5%
I2CC_SDA R3 I2CC_SDA R1403 DIS@ 2.2K_0402_5%
I2CS_SCL T4 I2CS_SCL R1404 DIS@ 2.2K_0402_5%
I2CS_SDA T3 I2CS_SDA R1405 DIS@ 2.2K_0402_5%

+3VS_VGA

CLK

PLLVDD AD8 +PLLVDD R1428 @ 0_0402_5%
SP_PLLVDD AE8 45mA
VID_PLLVDD AD7 45mA
+SP_PLLVDD

60mA

XTAL_IN H3 XTALIN
XTAL_OUT H2 XTAL_OUT
XTAL_OUTBUFF J4 XTALOUT R1433 DIS@ 10K_0402_5%
XTAL_SSIN H1 XTALSSIN R1435 DIS@ 10K_0402_5%

Internal Thermal Sensor

N13P-PES-A1_FCBGA908
DIS@

DIS@

C1401 DIS@ 0.1U_0402_10V7K
C1402 DIS@ 0.1U_0402_10V7K
C1403 DIS@ 0.1U_0402_10V7K
C1404 DIS@ 0.1U_0402_10V7K
C1405 DIS@ 0.1U_0402_10V7K
C1406 DIS@ 0.1U_0402_10V7K
C1407 DIS@ 0.1U_0402_10V7K
C1409 DIS@ 0.1U_0402_10V7K
C1410 DIS@ 0.1U_0402_10V7K
C1411 DIS@ 0.1U_0402_10V7K
C1412 DIS@ 0.1U_0402_10V7K
C1413 DIS@ 0.1U_0402_10V7K
C1414 DIS@ 0.1U_0402_10V7K
C1415 DIS@ 0.1U_0402_10V7K
C1416 DIS@ 0.1U_0402_10V7K
C1417 DIS@ 0.1U_0402_10V7K
C1418 DIS@ 0.1U_0402_10V7K
C1419 DIS@ 0.1U_0402_10V7K
C1420 DIS@ 0.1U_0402_10V7K
C1421 DIS@ 0.1U_0402_10V7K
C1422 DIS@ 0.1U_0402_10V7K
C1423 DIS@ 0.1U_0402_10V7K
C1424 DIS@ 0.1U_0402_10V7K
C1425 DIS@ 0.1U_0402_10V7K
C1426 DIS@ 0.1U_0402_10V7K
C1427 DIS@ 0.1U_0402_10V7K
C1428 DIS@ 0.1U_0402_10V7K
C1429 DIS@ 0.1U_0402_10V7K
C1430 DIS@ 0.1U_0402_10V7K
C1431 DIS@ 0.1U_0402_10V7K
C1432 DIS@ 0.1U_0402_10V7K
C1433 DIS@ 0.1U_0402_10V7K

PCIE_CRX_GTX_P0 PCIE_CRX_GTX_N0 PCIE_CRX_GTX_P1 PCIE_CRX_GTX_N1 PCIE_CRX_GTX_P2 PCIE_CRX_GTX_N2 PCIE_CRX_GTX_P3 PCIE_CRX_GTX_N3 PCIE_CRX_GTX_P4 PCIE_CRX_GTX_N4 PCIE_CRX_GTX_P5 PCIE_CRX_GTX_N5 PCIE_CRX_GTX_P6 PCIE_CRX_GTX_N6 PCIE_CRX_GTX_P7 PCIE_CRX_GTX_N7 PCIE_CRX_GTX_P8 PCIE_CRX_GTX_N8 PCIE_CRX_GTX_P9 PCIE_CRX_GTX_N9 PCIE_CRX_GTX_P10 PCIE_CRX_GTX_N10 PCIE_CRX_GTX_P11 PCIE_CRX_GTX_N11 PCIE_CRX_GTX_P12 PCIE_CRX_GTX_N12 PCIE_CRX_GTX_P13 PCIE_CRX_GTX_N13 PCIE_CRX_GTX_P14 PCIE_CRX_GTX_N14 PCIE_CRX_GTX_P15 PCIE_CRX_GTX_N15

PCIE_CRX_C_GTX_P0 AK14
PCIE_CRX_C_GTX_N0 AJ14
PCIE_CRX_C_GTX_P1 AH14
PCIE_CRX_C_GTX_N1 AG14
PCIE_CRX_C_GTX_P2 AK15
PCIE_CRX_C_GTX_N2 AJ15
PCIE_CRX_C_GTX_P3 AJ16
PCIE_CRX_C_GTX_N3 AK16
PCIE_CRX_C_GTX_P4 AK17
PCIE_CRX_C_GTX_N4 AJ17
PCIE_CRX_C_GTX_P5 AH17
PCIE_CRX_C_GTX_N5 AG17
PCIE_CRX_C_GTX_P6 AK18
PCIE_CRX_C_GTX_N6 AJ18
PCIE_CRX_C_GTX_P7 AL19
PCIE_CRX_C_GTX_N7 AK19
PCIE_CRX_C_GTX_P8 AK20
PCIE_CRX_C_GTX_N8 AJ20
PCIE_CRX_C_GTX_P9 AH20
PCIE_CRX_C_GTX_N9 AG20
PCIE_CRX_C_GTX_P10 AK21
PCIE_CRX_C_GTX_N10 AJ21
PCIE_CRX_C_GTX_P11 AL22
PCIE_CRX_C_GTX_N11 AK22
PCIE_CRX_C_GTX_P12 AK23
PCIE_CRX_C_GTX_N12 AJ23
PCIE_CRX_C_GTX_P13 AH23
PCIE_CRX_C_GTX_N13 AG23
PCIE_CRX_C_GTX_P14 AK24
PCIE_CRX_C_GTX_N14 AJ24
PCIE_CRX_C_GTX_P15 AL25
PCIE_CRX_C_GTX_N15 AK25

(14) CLK_PCIE_VGA
(14) CLK_PCIE_VGA#
CLK_PCIE_VGA AL13
CLK_PCIE_VGA# AK13
CLK_REQ_GPU# AK12

Differential signal

R1432 @ 200_0402_1%

R1434 DIS@ 2.49K_0402_1%

SA000056B30
S IC N13M-GE1-B-A1 FCBGA 908P GPU A39

SA000051A40
S IC N13P-GL-A1 FCBGA 908P GPU A39

+3VS_VGA

OVERT# R1408 DIS@ 10K_0402_5%
THERM#_VGA R1410 DIS@ 10K_0402_5%
VGA_GPIO12 R1409 DIS@ 10K_0402_5%
VGA_BL_PWM R1413 DIS@ 10K_0402_5%
VGA_ENVDD R1411 DIS@ 10K_0402_5%
VGA_ENBKL R1412 @ 10K_0402_5%
VGA_GPIO15 R1414 DIS@ 100K_0402_5%

+3VS_VGA

VGA_THRMTRIP# (18)

R1423 10K_0402_5% DIS@
Q1401B 2N7002KDWH_SOT363-6 DIS@
OVERT# DIS@ Q1401A 2N7002KDWH_SOT363-6

+3VS_VGA

I2CS_SCL
Q1402B DIS@ 2N7002KDWH_SOT363-6
EC_SMB_CK2 (14,39,41)
R1442 @ 0_0402_5%
I2CS_SDA
Q1402A DIS@ 2N7002KDWH_SOT363-6
EC_SMB_DA2 (14,39,41)
R1443 @ 0_0402_5%

PU AT EC SIDE, +3VS AND 4.7K

R1436 DIS@ 10M_0402_5%
DIS@ Y1401
XTALIN XTAL_OUT GND GND
C1441 18P_0402_50V8J DIS@
C1442 18P_0402_50V8J DIS@
27MHZ 16PF X3G027000FG1H-HX

Under GPU(below 150mils)

+SP_PLLVDD
150mA
L1402 DIS@ BLM18PG330SN1_2P
+1.05VS_VGA
180ohms (ESR=0.2) Bead
C1443 DIS@ 22U_0805_6.3V6M
C1444 DIS@ 4.7U_0402_6.3V6M
C1445 DIS@ 0.1U_0402_10V7K
C1446 DIS@ 0.1U_0402_10V7K

+PLLVDD
L1403 DIS@ BLM18PG181SN1D_2P
+1.05VS_VGA
30 ohms @100MHz (ESR=0.05)
Under GPU
C1447 DIS@ 0.1U_0402_10V7K
C1448 DIS@ 22U_0805_6.3V6M
Near GPU

+3VS_VGA +3VS_VGA

R1437 @ 0_0402_5%
R1438 10K_0402_5% @
R1441 10K_0402_5% DIS@
U1402 TC7SH08FUF_SSOP5 DIS@

(5,14,17,36,38,40,41) PLT_RST#
PLT_RST#
(17) DGPU_HOLD_RST#
DGPU_HOLD_RST#
PLT_RST_VGA#

(17,24) DGPU_PWR_EN

R1444 10K_0402_5% DIS@
C2154 0.1U_0402_16V4Z DIS@
11/17
C2108 0.1U_0402_16V4Z
Q2414 DIS@ 2N7002K_SOT23-3
R1447 @ 0_0402_5%

+3VS_VGA

R1445 10K_0402_5% DIS@
R1446 10K_0402_5% @

(14) GPU_CLKREQA
CLK_REQ_GPU#

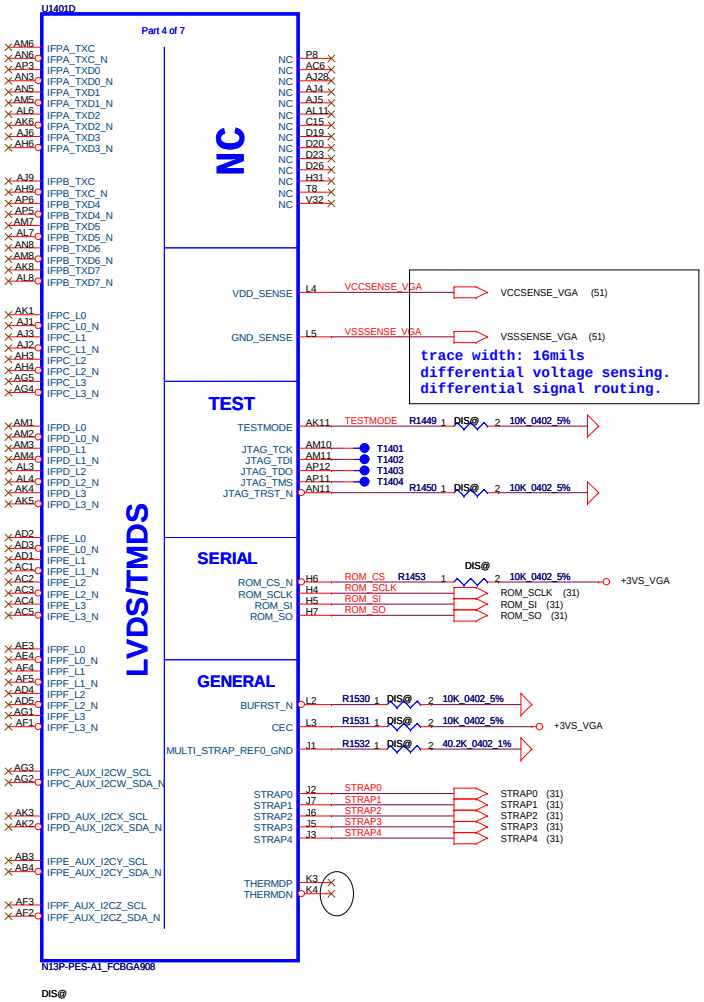
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: N13X-PCIE/DAC/GPIO

Size: Custom | Document Number: LA-8133P | Rev: 1.0

Date: Friday, January 13, 2012 | Sheet 22 of 58



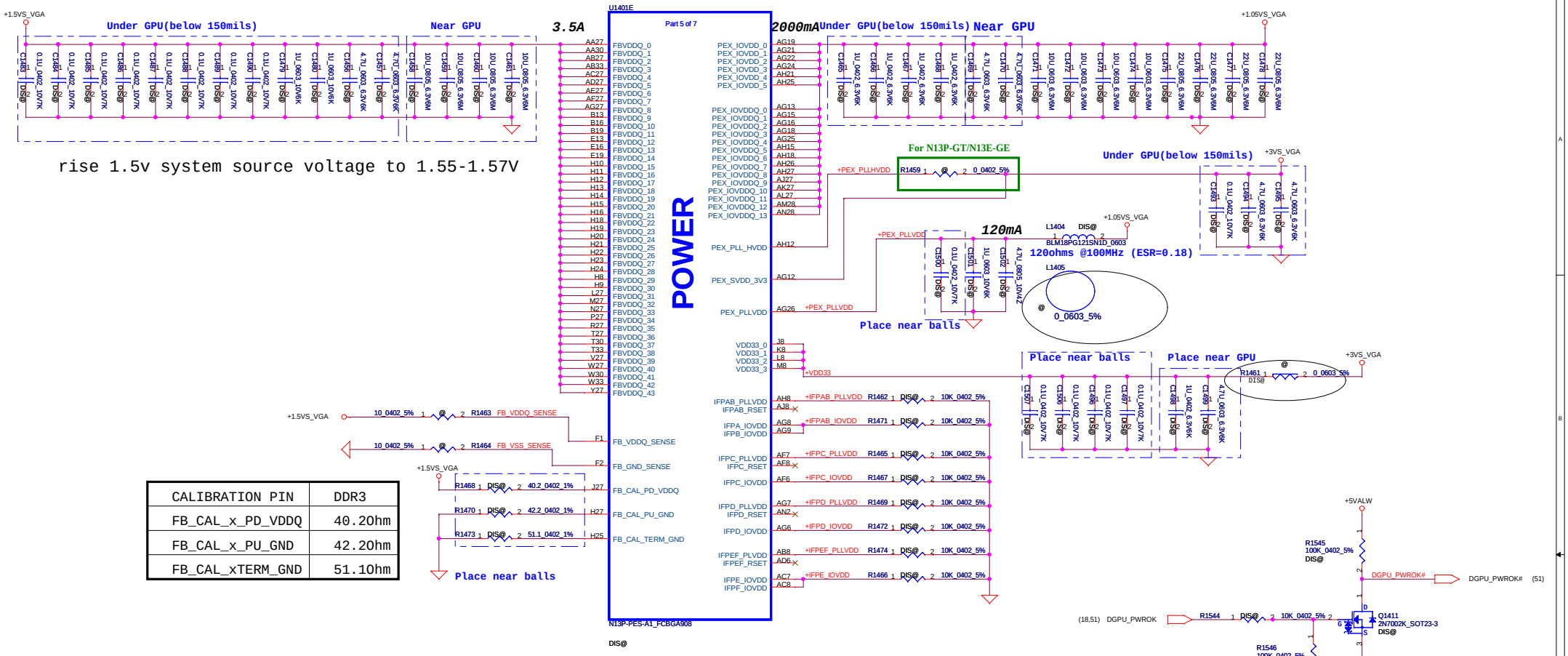
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: N13X-LVDS/HDMI/DP/THM

Size: Custom | Document Number: LA-8133P | Rev: 1.0

Date: Friday, January 13, 2012 | Sheet 23 of 58



CALIBRATION PIN	DDR3
FB_CAL_x_PD_VDDQ	40.2ohm
FB_CAL_x_PU_GND	42.2ohm
FB_CAL_xTERM_GND	51.1ohm

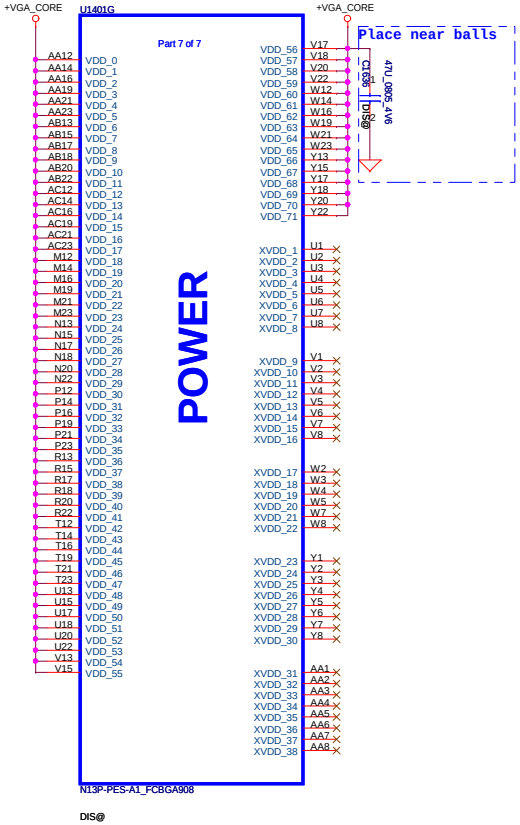
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

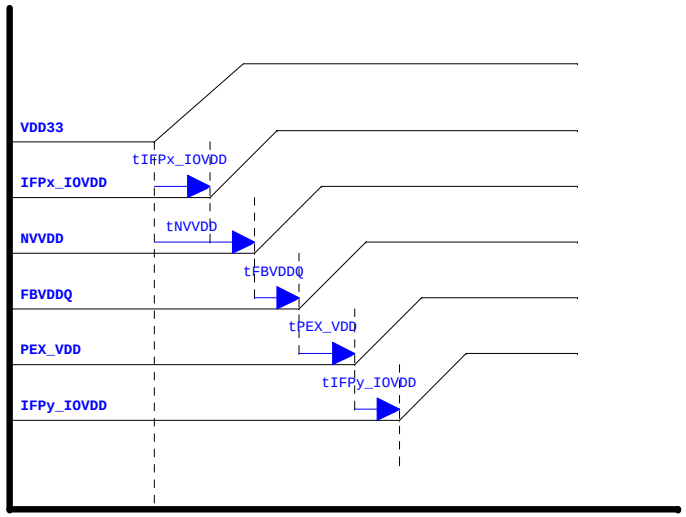
Compal Electronics, Inc.

Title: N13X-POWER

Size: Custom | Document Number: LA-8133P | Rev: 1.0

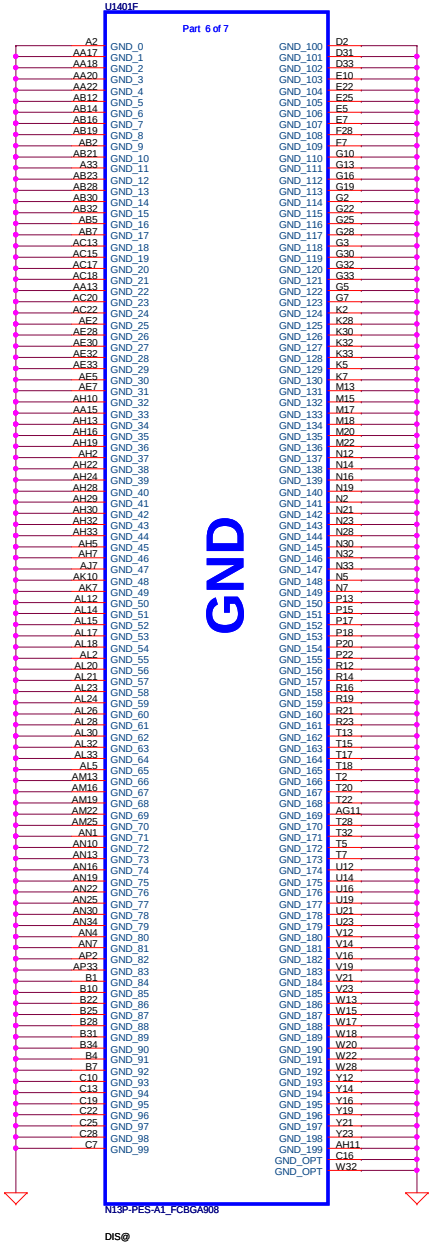
Date: Friday, January 13, 2012 | Sheet 24 of 58





NV Recommended Power On Sequencing Order

X=A and B
Y=C,D,E and F



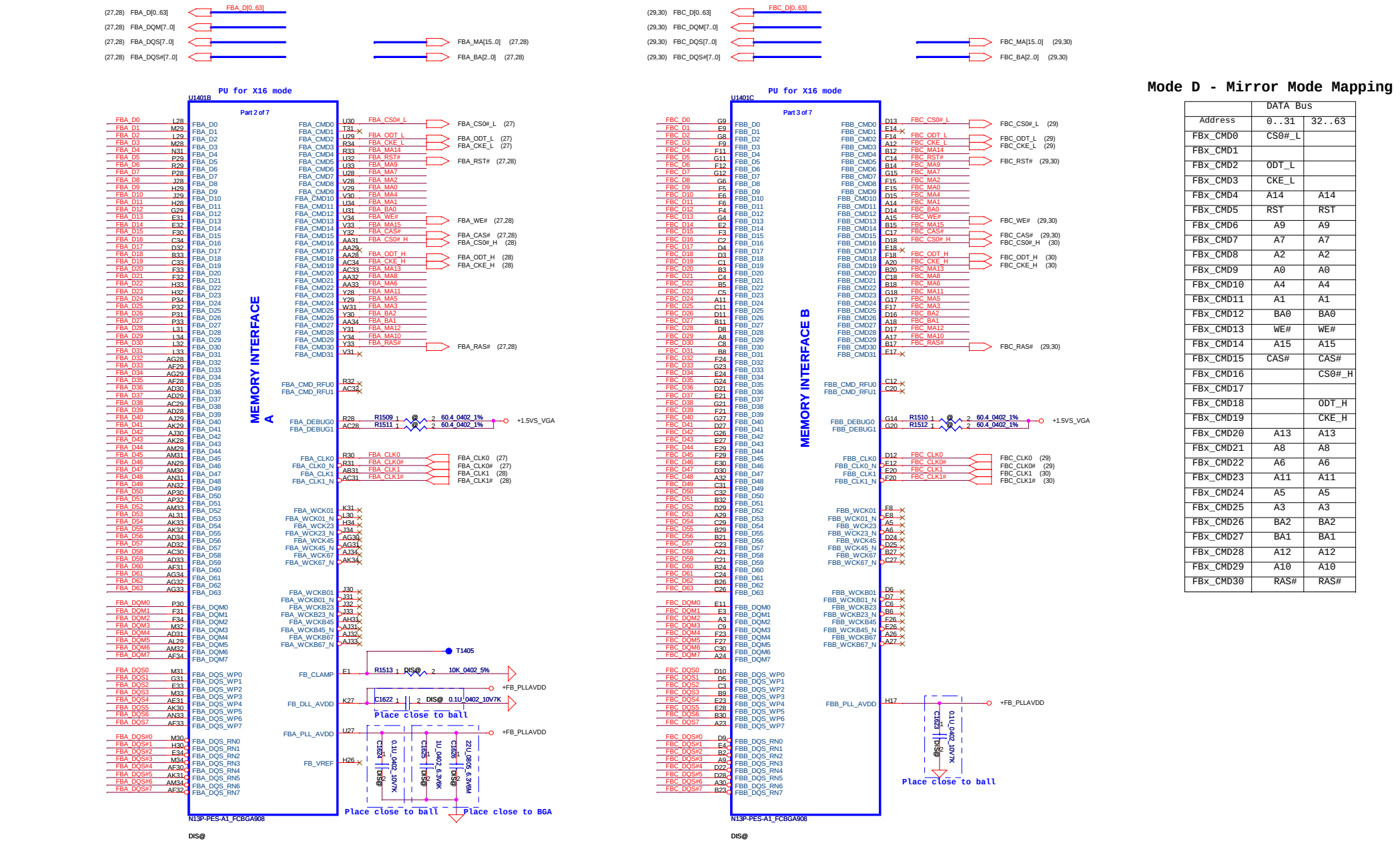
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: N13X-VGA CORE, GND

Size: Custom | Document Number: LA-8133P | Rev: 1.0

Date: Friday, January 13, 2012 | Sheet 25 of 58



Mode D - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

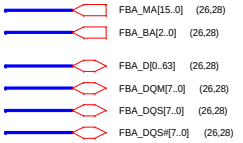
Compal Electronics, Inc.

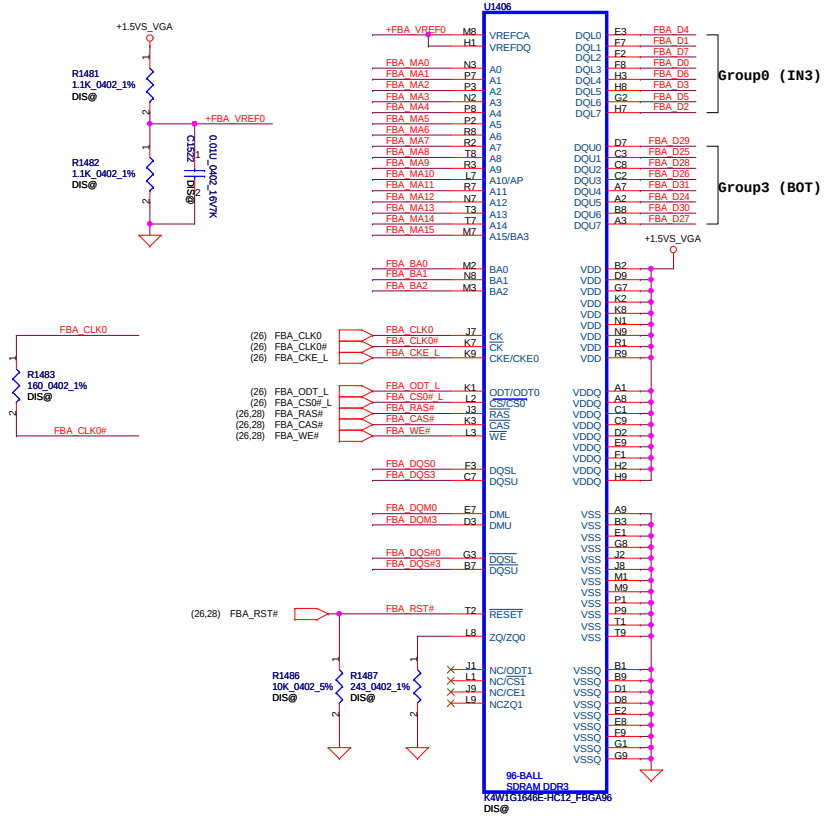
Title: **N13X-MEM Interface**

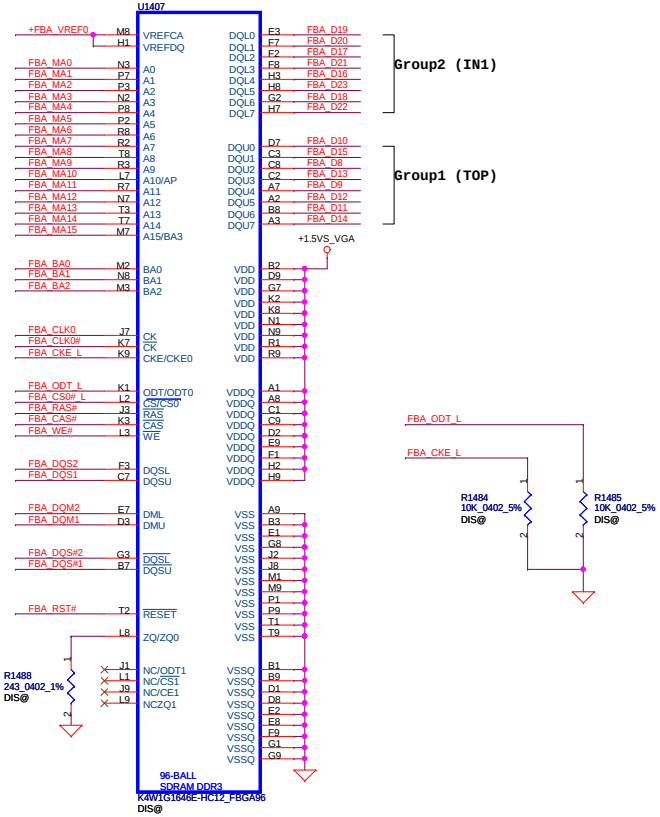
Size: Custom | Document Number: **LA-8133P** | Rev: 1.0

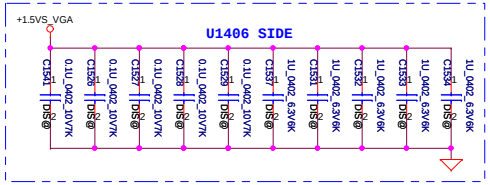
Date: Friday, January 13, 2012 | Sheet 26 of 58

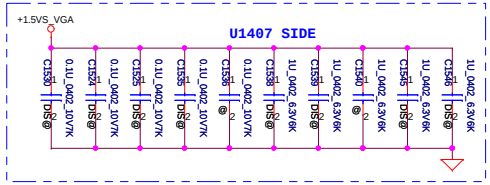
Memory Partition A - Lower 32 bits











Mode D - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

Compal Electronics, Inc.

Title: N13X-VRAM A Lower

Size: Custom | Document Number: LA-8133P | Rev: 1.0

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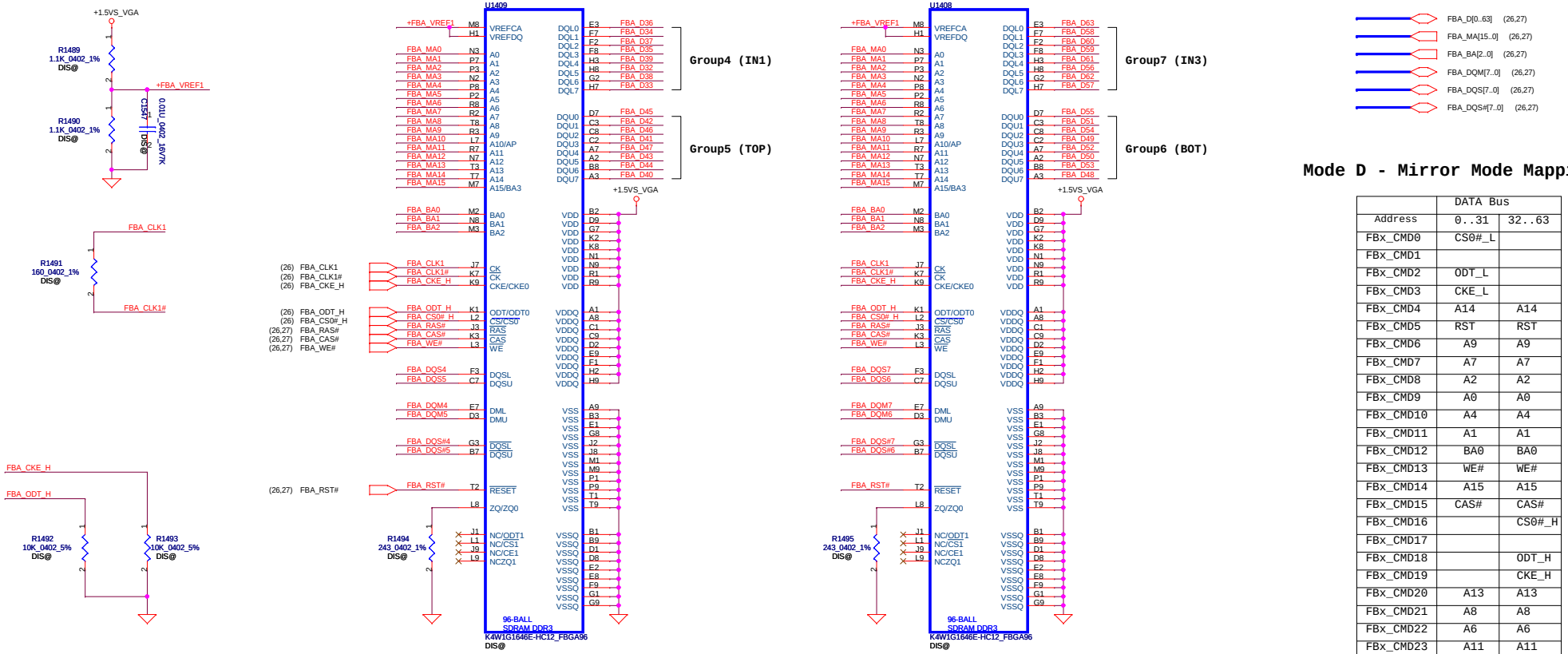
Memory Partition A - Upper 32 bits



Mode D - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

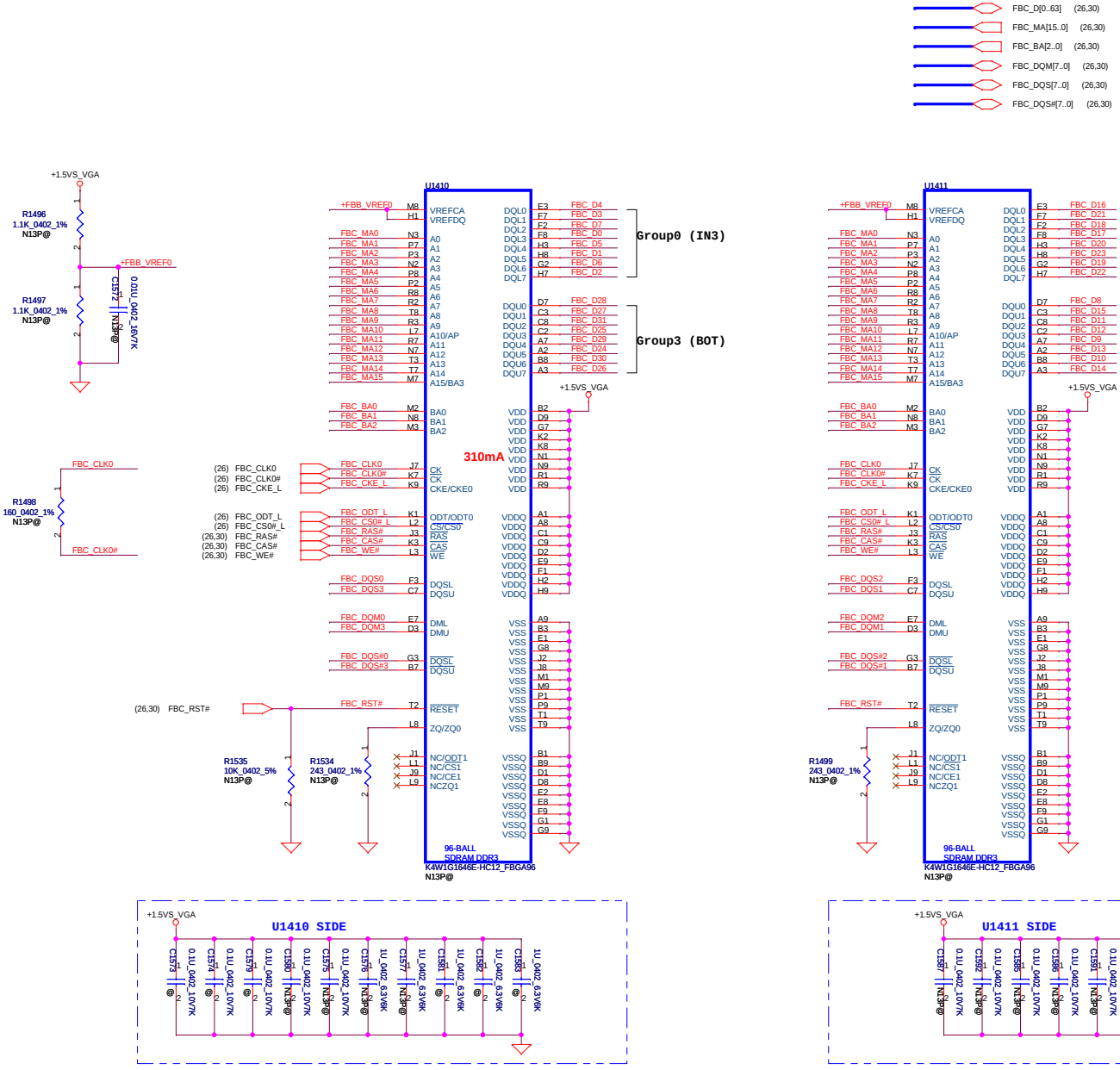
Compal Electronics, Inc.

Title: N13X-VRAM A Upper

Size: Custom | Document Number: LA-8133P | Rev: 1.0

Date: Friday, January 13, 2012 | Sheet 28 of 58

Memory Partition C - Lower 32 bits



Mode D - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

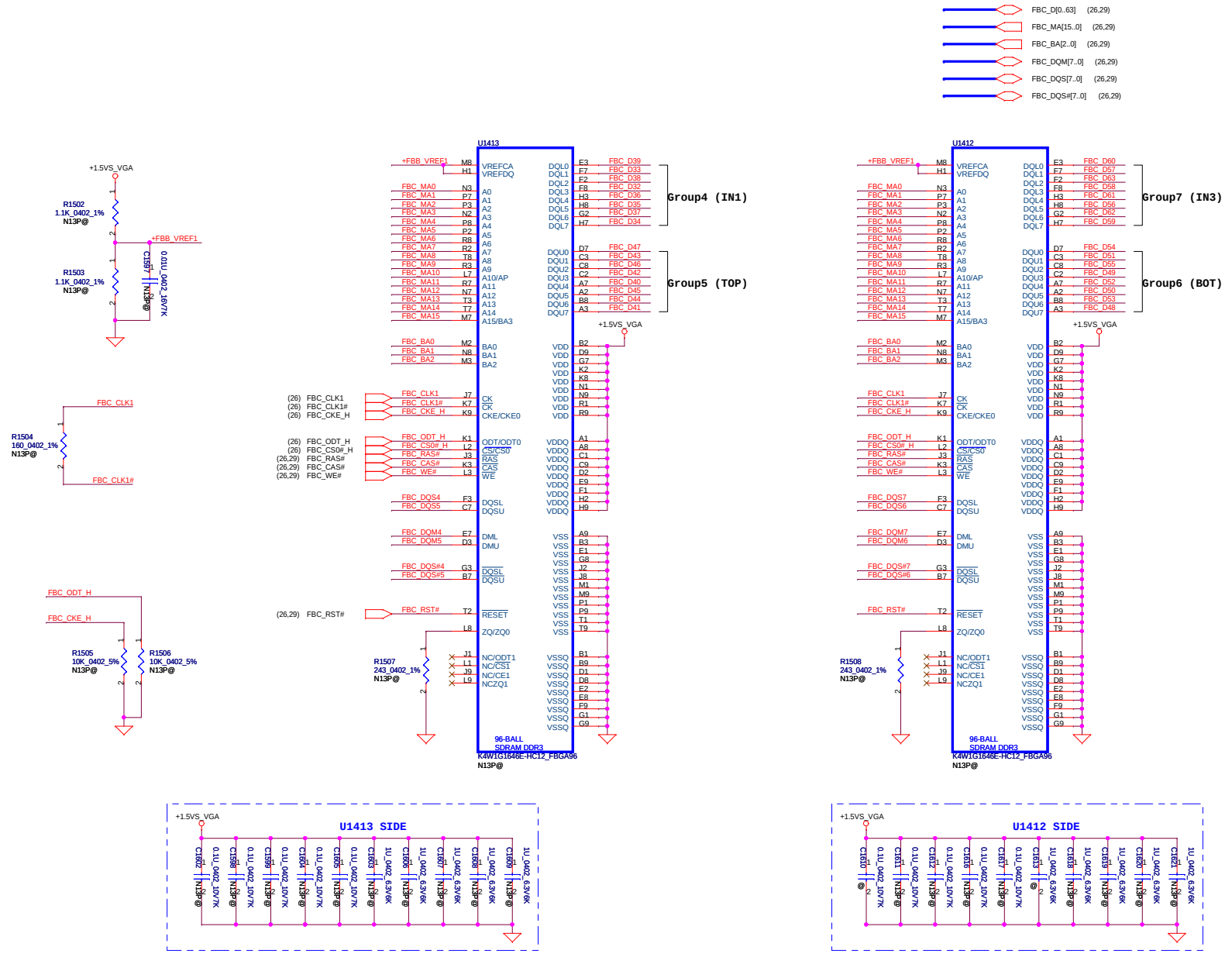
Compal Electronics, Inc.

Title: N13X-VRAM C Lower

Size: Custom | Document Number: LA-8133P | Rev: 1.0

Date: Friday, January 13, 2012 | Sheet 29 of 58

Memory Partition C - Upper 32 bits



Mode D - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

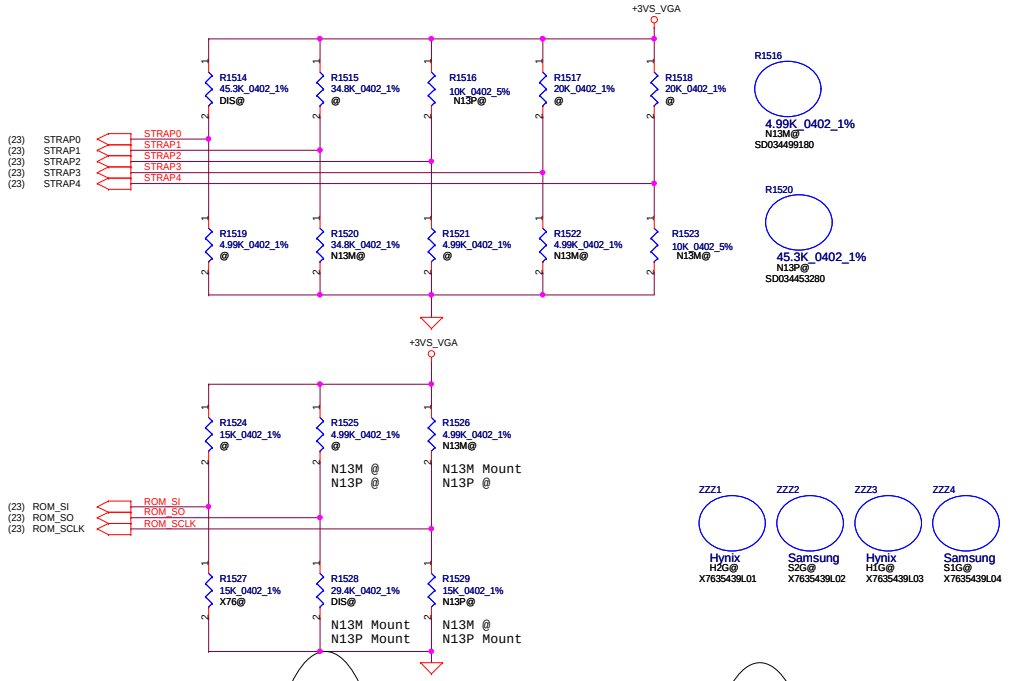
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: N13X-VRAM C Upper

Size: Custom | Document Number: LA-8133P | Rev: 1.0

Date: Friday, January 13, 2012 | Sheet 30 of 58



GPU	FB Memory gDDR3		ROM_SO	ROM_SCLK	ROM_SI	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N13P-GL	Samsung 900MHz	K4W1G1646G-BC11 64Mx16	PD 10K	PD 15K	PD 20K	PU 45K	PD 45K	PU 10K PU 45K(ES)	NC	NC
	Hynix 900MHz	H5TQ1G63DFR-11C 64Mx16	PD 10K	PD 15K	PD 15K	PU 45K	PD 45K	PU 10K PU 45K(ES)	NC	NC
	Samsung 900MHz	K4W2G1646C-HC11 128Mx16	PD 10K	PD 15K	PD 45K	PU 45K	PD 45K	PU 10K PU 45K(ES)	NC	NC
	Hynix 900MHz	H5TQ2G63BFR-11C 128Mx16	PD 10K	PD 15K	PD 35K	PU 45K	PD 45K	PU 10K PU 45K(ES)	NC	NC

X76

GPU	FB Memory gDDR3		ROM_SO	ROM_SCLK	ROM_SI	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N13M-GE1	Samsung 900MHz	K4W1G1646G-BC11 64Mx16	PD 30K	PU 5K	PD 20K	PU 45K	PD 35K	PU 5K	PD 5K	PD 10K
	Hynix 900MHz	H5TQ1G63DFR-11C 64Mx16	PD 30K	PU 5K	PD 15K	PU 45K	PD 35K	PU 5K	PD 5K	PD 10K
	Samsung 900MHz	K4W2G1646C-HC11 128Mx16	PD 30K	PU 5K	PD 45K	PU 45K	PD 35K	PU 5K	PD 5K	PD 10K
	Hynix 900MHz	H5TQ2G63BFR-11C 128Mx16	PD 30K	PU 5K	PD 35K	PU 45K	PD 35K	PU 5K	PD 5K	PD 10K

9/27 from 15K to 5K

X76

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110	Notebook Default

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

USER Straps	
User[3:0]	
1000-1100	Customer defined

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

PCIE_MAX_SPEED	
0	Limit to PCIE Gen1
1	PCIE Gen 2/3 Capable

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: N13X-MISC

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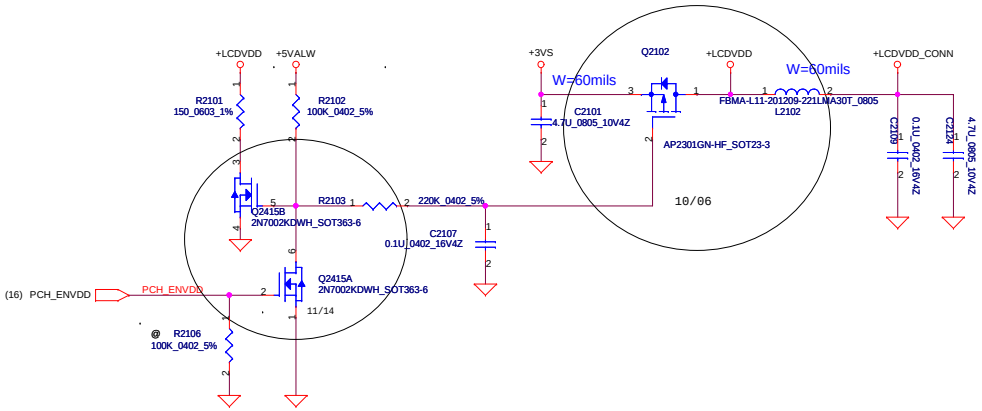
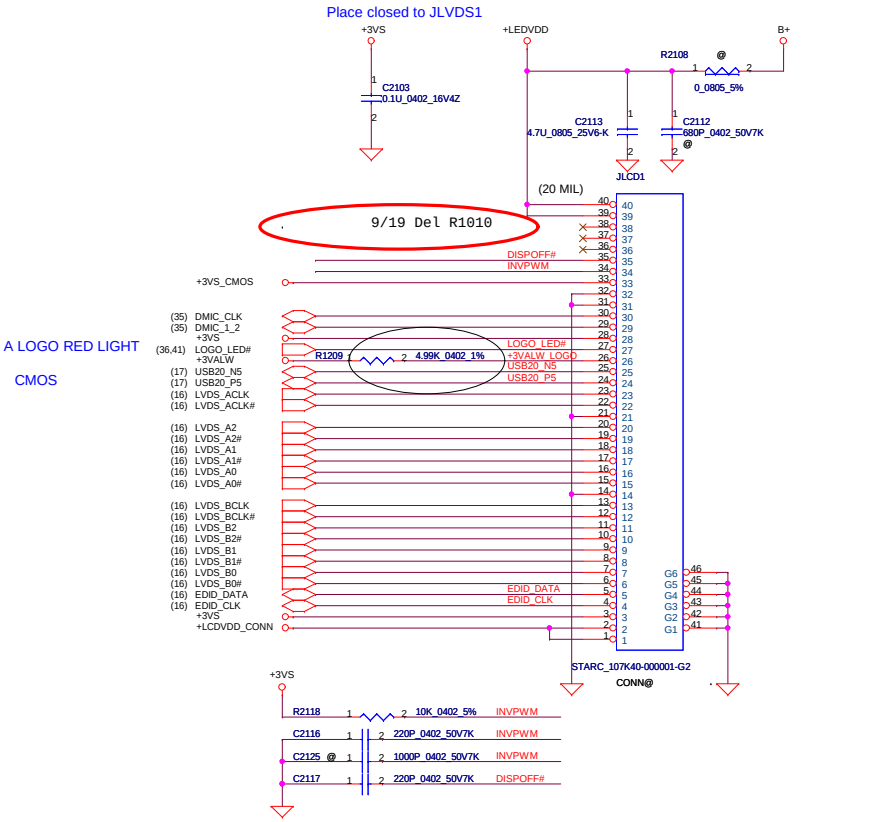
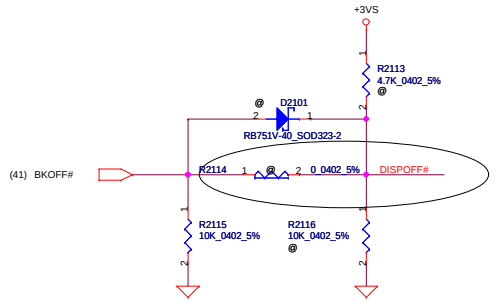
LCD POWER CIRCUIT

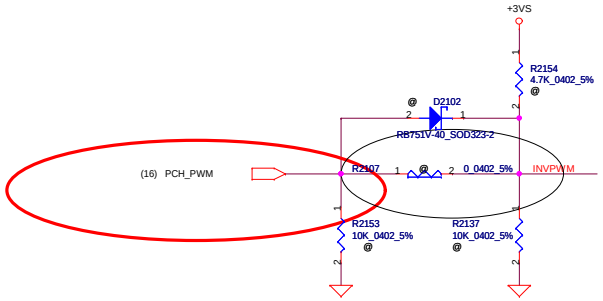


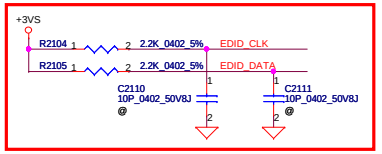
LCD/LED PANEL Conn.

PN:SP01000XE00

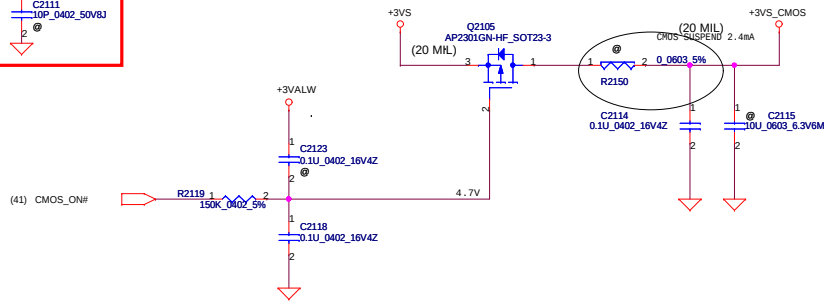








CMOS Camera Conn



Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: **LVDS Connector**

Size	Document Number	Rev
Custom	LA-8133P	1.0

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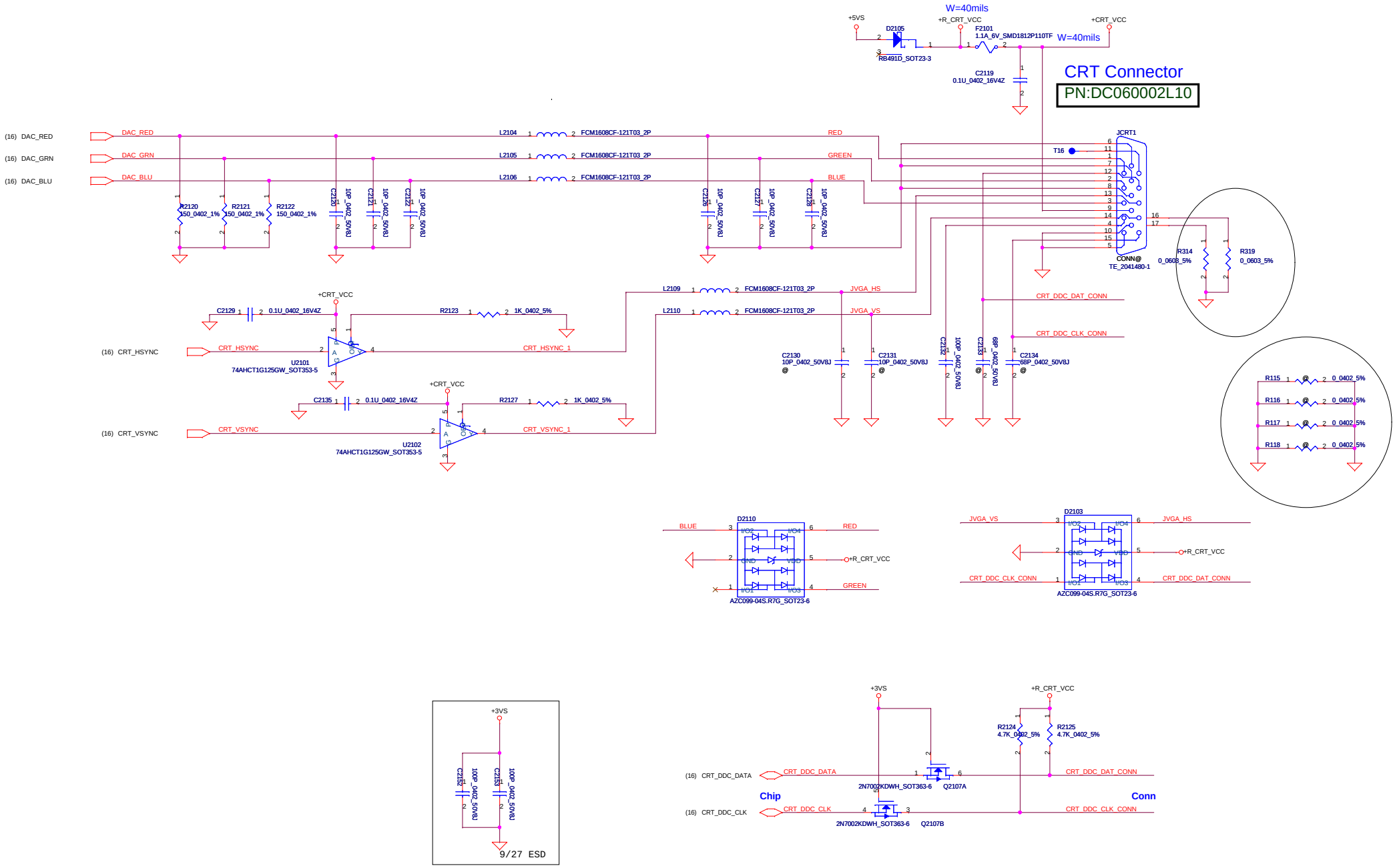


Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: **CRT Connector**

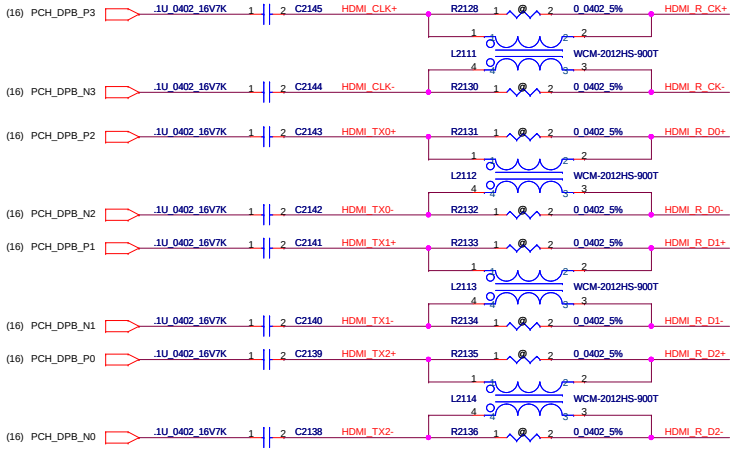
Size: Custom | Document Number: **LA-8133P** | Rev: 1.0

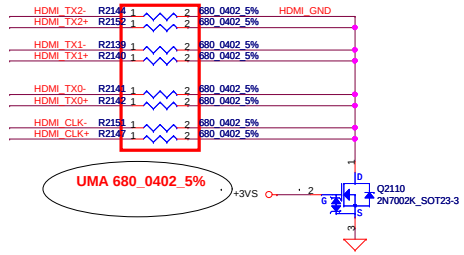
Date: Friday, January 13, 2012 | Sheet 33 of 58

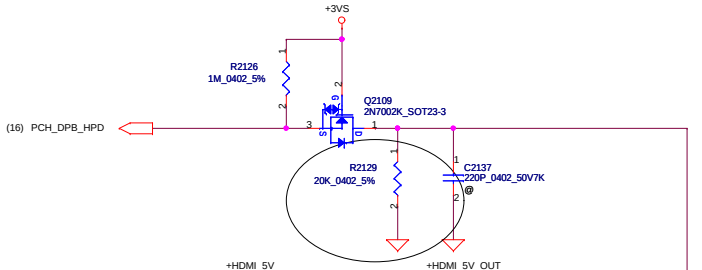
HDMI Connector

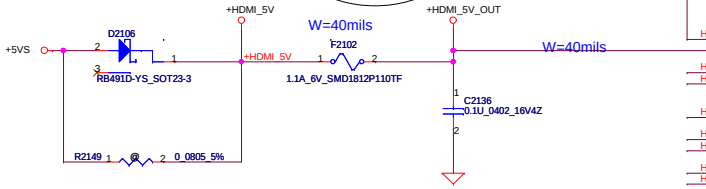
PN:DC232001K10

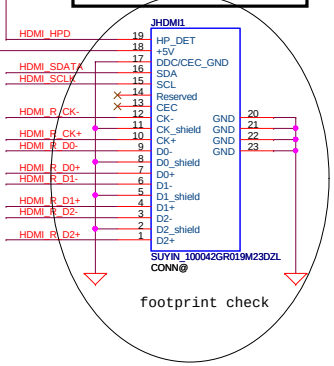
ESD request
Common mode choke 90ohm on these singals
Compal PN: SM070000K00
Vendor PN: WCM-2012-900T

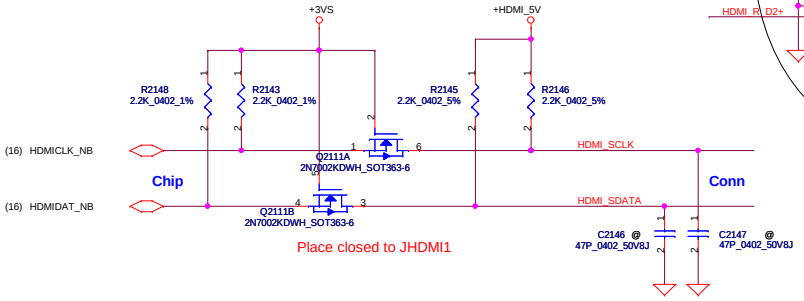


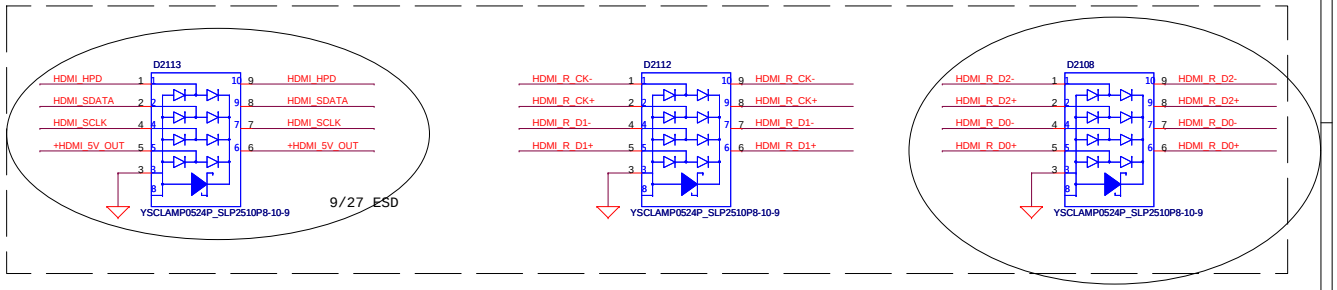












Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: **HDMI Connector**

Size: Custom | Document Number: **LA-8133P** | Rev: 1.0

Date: Friday, January 13, 2012 | Sheet 34 of 58

CX20671
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).

EC Beep

ICH Beep

PC Beep

Combo Jack detect (normal open)

Layout Note:Path from +5VS to Pin12, Pin15 must be very low resistance (<0.01 ohms)

To support Wake-on-Jack or Wake-on-Ring, the CODEC VAUX_3.3 & VDD_IO pins must be powerd by a rail that is not removed unless AC power is removed. *DSH page42 has more detail.

10K only needed if supply to VAUX_3.3 is removed during system re-start.

EAPD active low
0=power down ex AMP
1=power up ex AMP

Internal DMIC

Internal SPEAKER

Decoupling CAP

Near Pin 2
Near Pin 7
Near Pin 3
Near Pin 29
Near Pin 27
Near Pin 28
Near Pin 26
Near Pin 17
Near Pin 12
Near Pin 15
Near Pin 21

AVDD_3.3 pinis output of internal LDO. NOT connect to external supply.

Sense resistors must be connected same power that is used for VAUX_3.3

Port B
Port A
External MIC

Headphone

Changed from 5.1ohm to 15ohm for "zi zi"noise.

EMC request
Bead 120ohm on these singals
Compal PN: SM010016720
Vendor PN: FBMA-L11-160808-121LMT

Rdc < 0.05 ohms
Rated Current > 2A

Width 20 mil

EMI

9/28 RF modify

GND

GNDA

Internal Speaker

SP02000N010
SP02000SM10

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

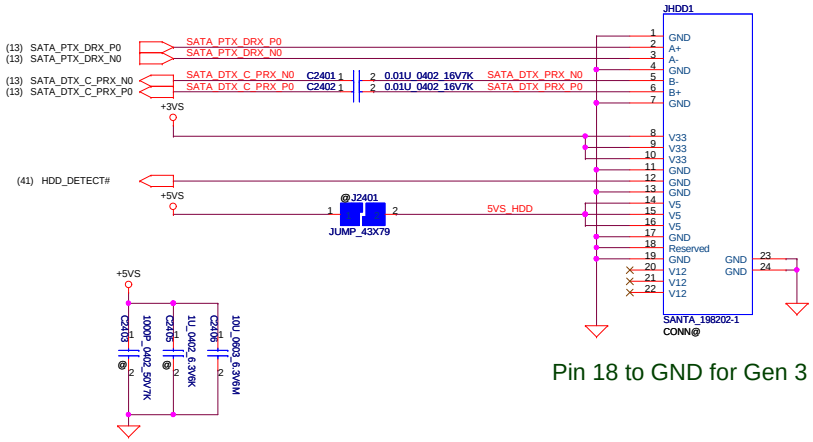
Title: HD Audio Codec CX20671

Size: Custom | Document Number: LA-8133P | Rev: 1.0

Date: Friday, January 13, 2012 | Sheet 35 of 58

SATA HDD CONN.

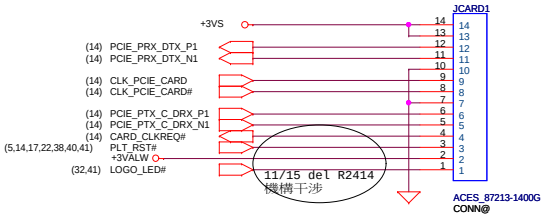
PN:DC010004C00



Pin 18 to GND for Gen 3

Card Reader CONN.

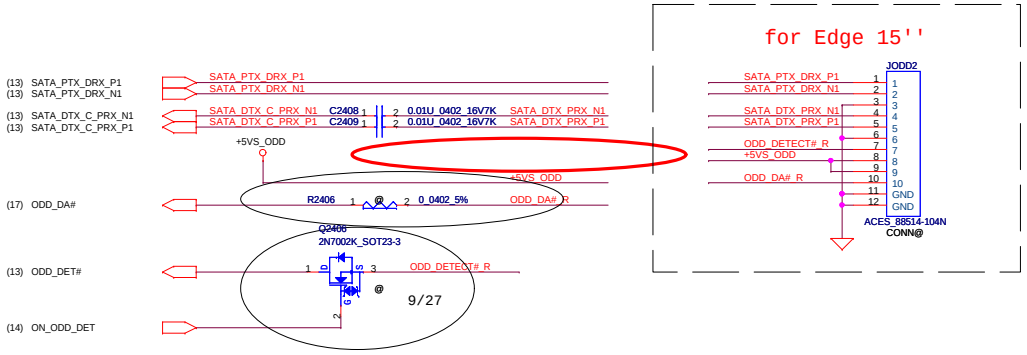
PN:SP01001BF00

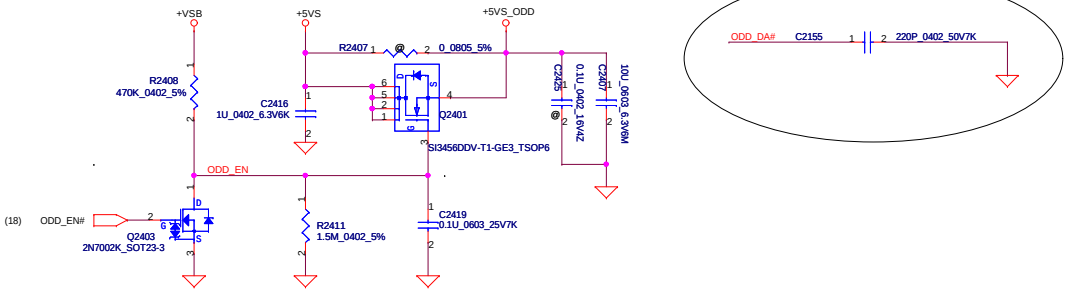


10/06
change PN to SP02000H810
footprint: ACES_87213-1400G_14P

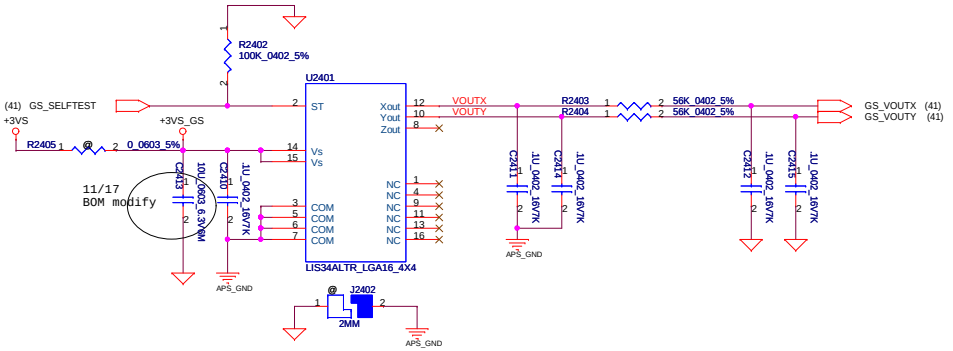
SATA ODD CONN.

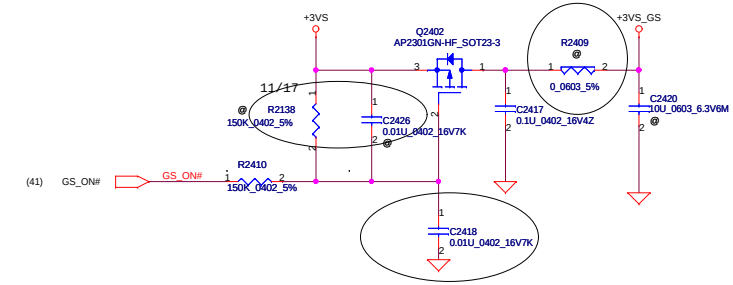
PN:SP01000TU10





APS G-Sensor





Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

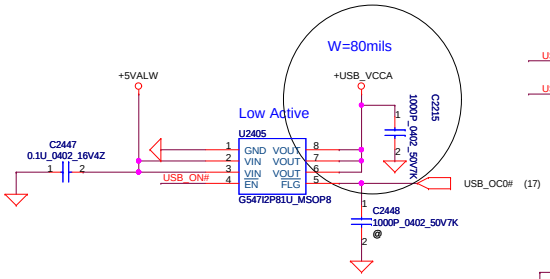
Compal Electronics, Inc.

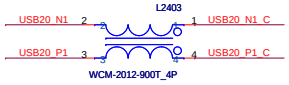
Title: HDD/ODD/Card reader/G-Sensor

Size: Custom | Document Number: LA-8133P | Rev: 1.0

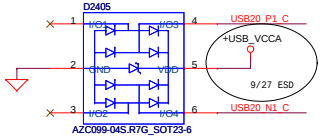
Date: Friday, January 13, 2012 | Sheet 36 of 58

USB 3.0 Conn.

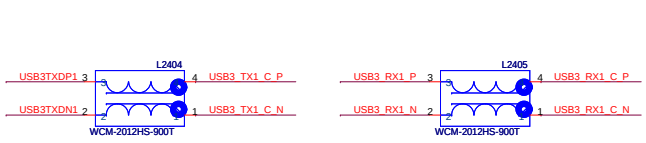




PN: SM070000K00 x 1

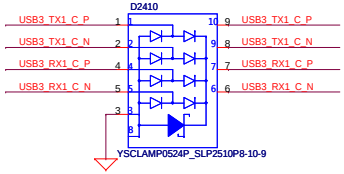


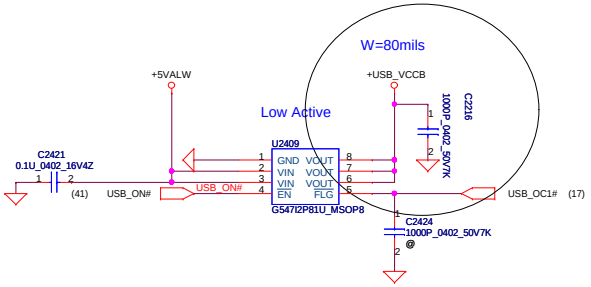
PN: SC300001G00



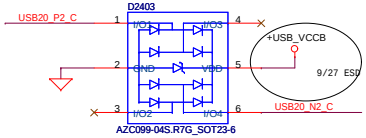
PN: SM070001S00 x 2

PN:DC23300AS20

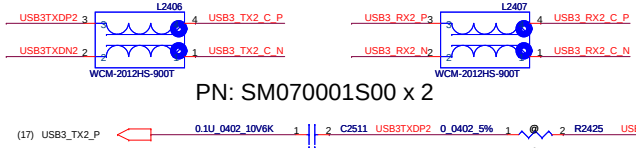




PN: SM070000K00 x 1

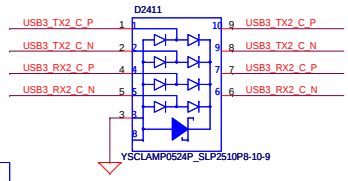


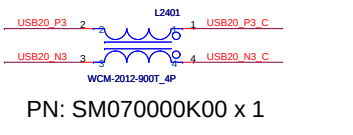
PN: SC300001G00



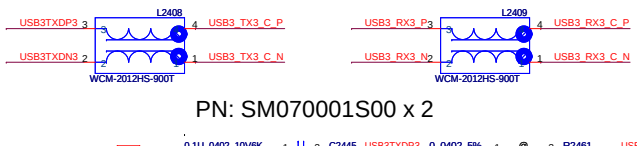
PN: SM070001S00 x 2

PN:DC23300AS20



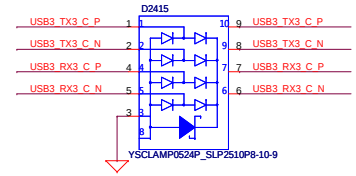


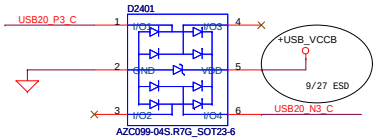
PN: SM070000K00 x 1



PN: SM070001S00 x 2

PN:DC23300AS20





PN: SC300001G00

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: **USB 3.0 Connector**

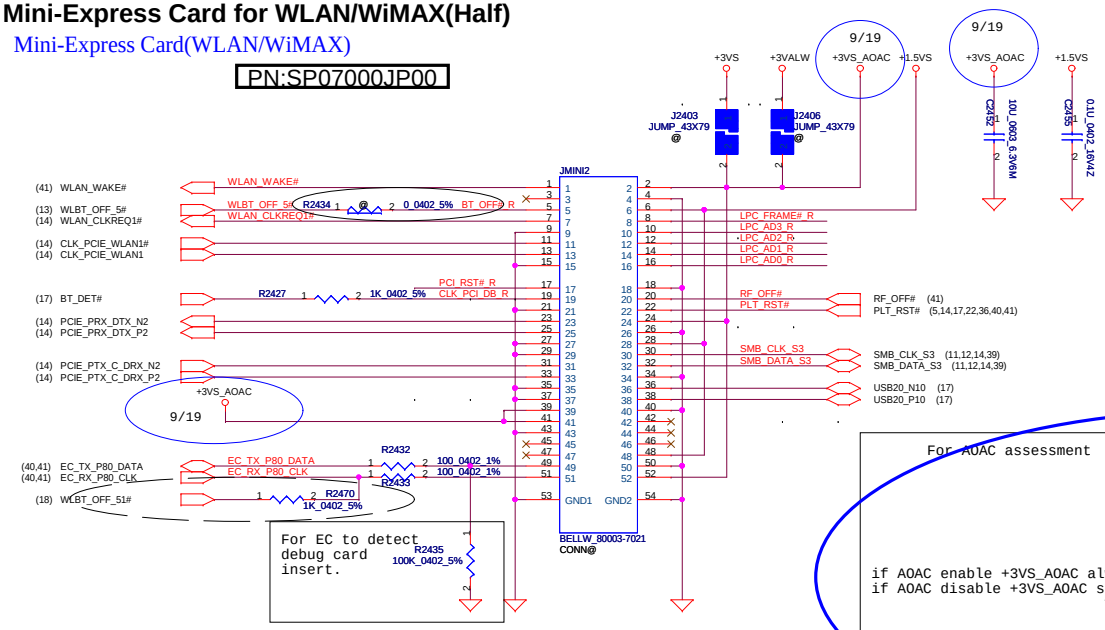
Size	Document Number	Rev
Custom	LA-8133P	1.0

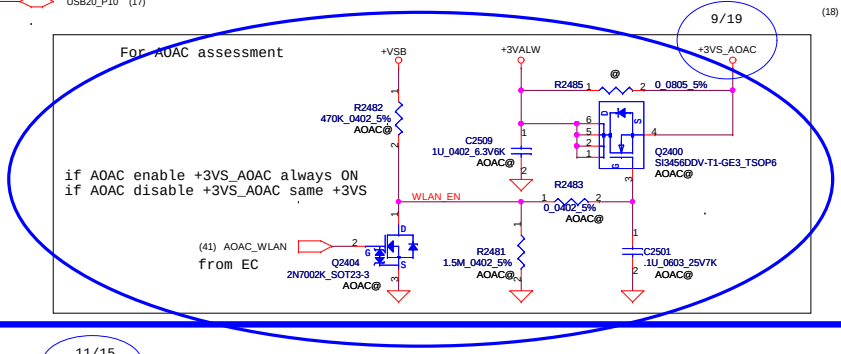
Date: Friday, January 13, 2012 Sheet 37 of 58

Mini-Express Card for WLAN/WiMAX(Half)

Mini-Express Card(WLAN/WiMAX)

PN:SP07000JP00

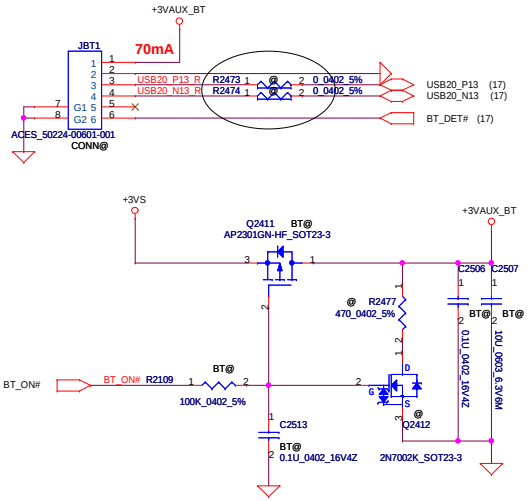




Mini Card Power Rating

Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

BT Connector

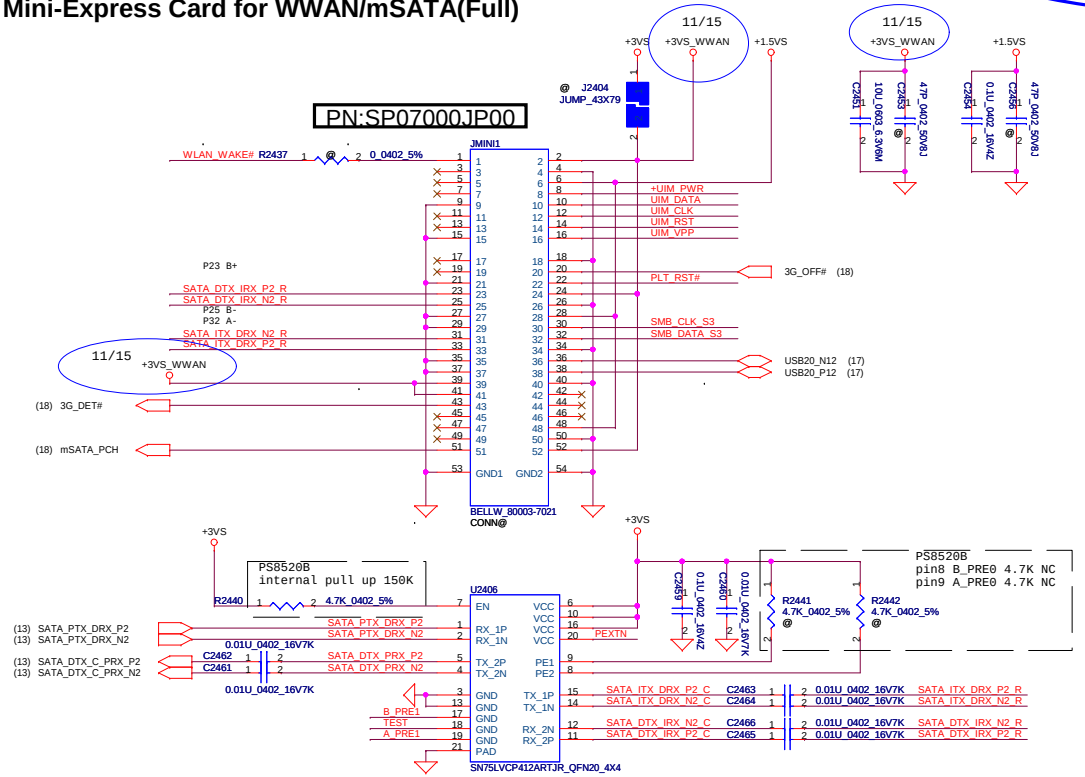


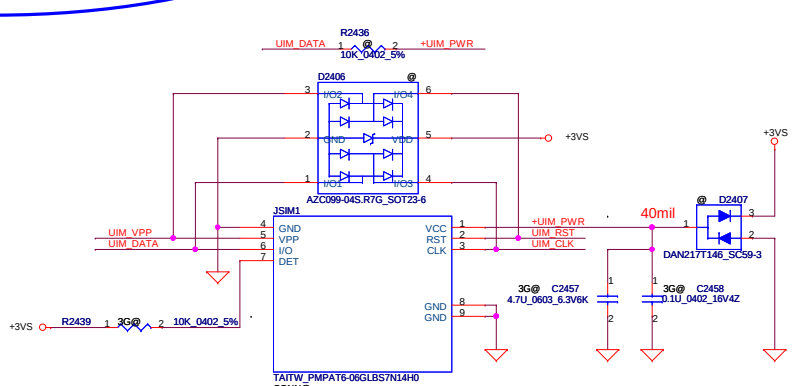
Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

LPC_FRAME# R	R2449	0_0402_5%	LPC_FRAME#	LPC_FRAME# (13,40,41)
LPC_AD3_R	R2455	0_0402_5%	LPC_AD3	LPC_AD3 (13,40,41)
LPC_AD2_R	R2456	0_0402_5%	LPC_AD2	LPC_AD2 (13,40,41)
LPC_AD1_R	R2457	0_0402_5%	LPC_AD1	LPC_AD1 (13,40,41)
LPC_AD0_R	R2458	0_0402_5%	LPC_AD0	LPC_AD0 (13,40,41)
PCI_RST# R	R2459	0_0402_5%	PLT_RST#	
CLK_PCI_DB_R	R2428	0_0402_5%	CLK_PCI_DB	CLK_PCI_DB (17,40)

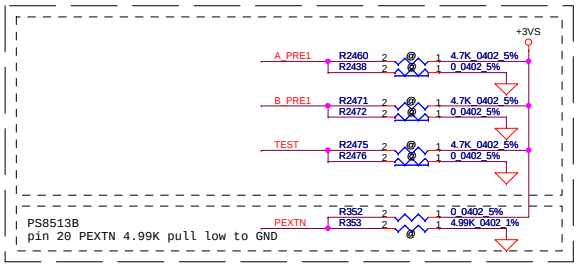
Mini-Express Card for WWAN/mSATA(Full)

PN:SP07000JP00





PN:SP07000LM00



Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

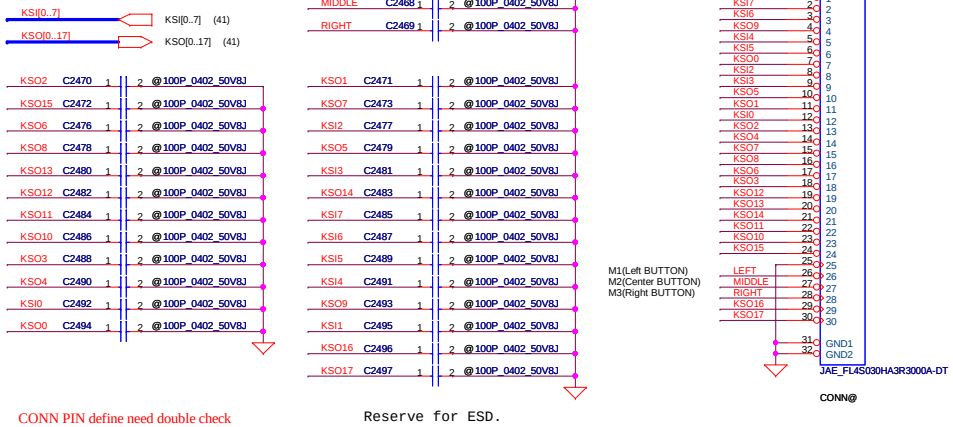
Compal Electronics, Inc.

Title: WLAN and WWAN/mSATA

Size: Custom | Document Number: LA-8133P | Rev: 1.0

Date: Friday, January 13, 2012 | Sheet 38 of 58

INT_KBD Conn.



CONN PIN define need double check

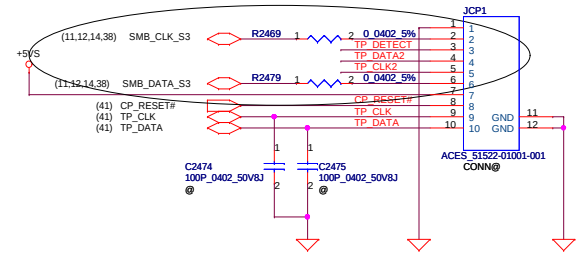
Reserve for ESD.

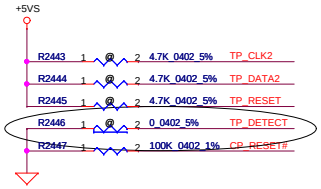
PN:SP01000YH00

M1(Left BUTTON)
M2(Center BUTTON)
M3(Right BUTTON)

Click pad

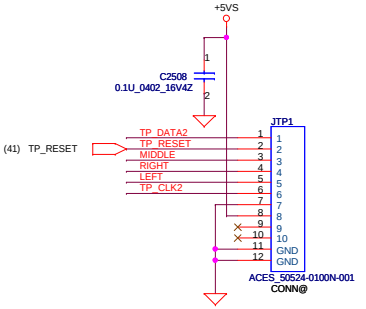
PN:SP01001AL00

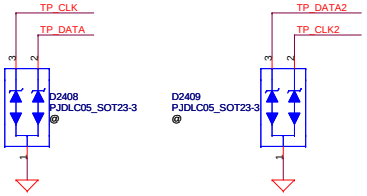




Track point

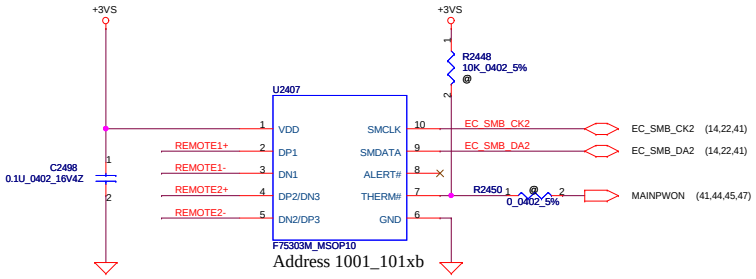
PN:SP01001CH00





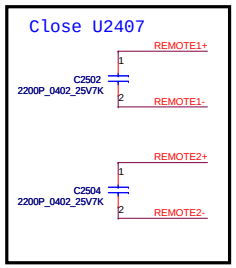
PN: SCA00000U10 X 2

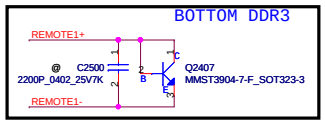
Fintek thermal sensor placed near by TOP DDR3

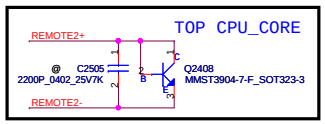


Address 1001_101xb

2nd source
SA000029210-->EMC1403-2-AIZL-TR

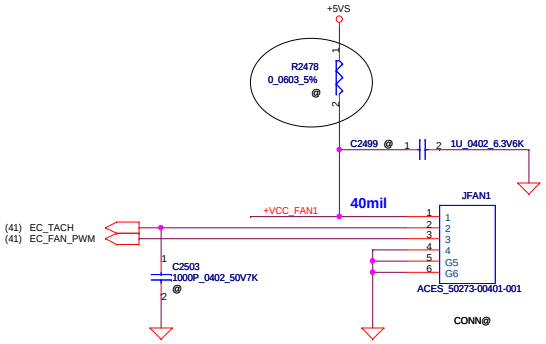






REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

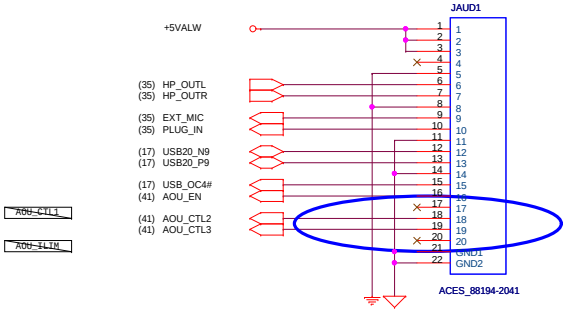
FAN CONN.



PN:SP02000U900

Audio Board

PN:SP011108040



Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: KB/TP/Thermal Sensor/Audio

Size: Custom | Document Number: LA-8133P | Rev: 1.0

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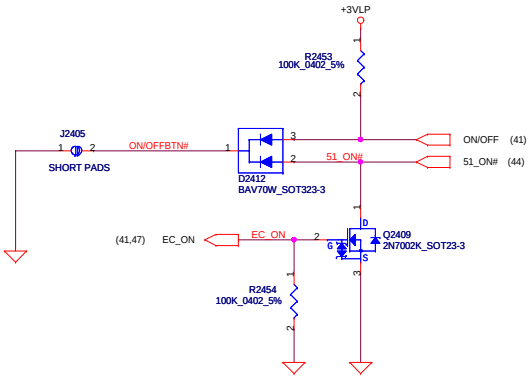
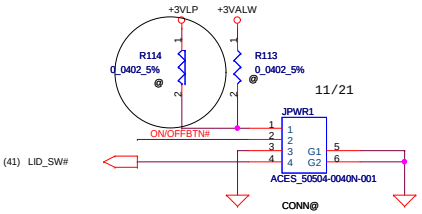
Power Button



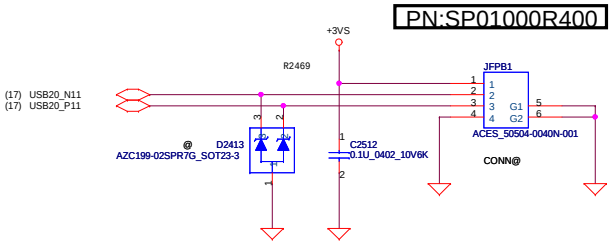
Power Button CONN.

PN:SP01000R400

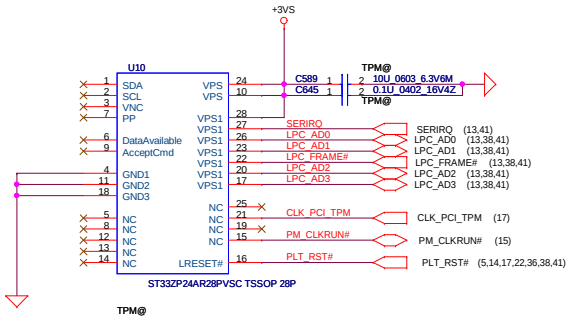


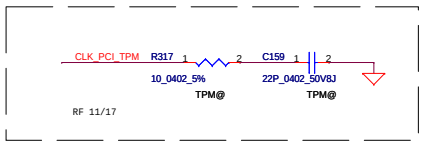
Finger Print Board

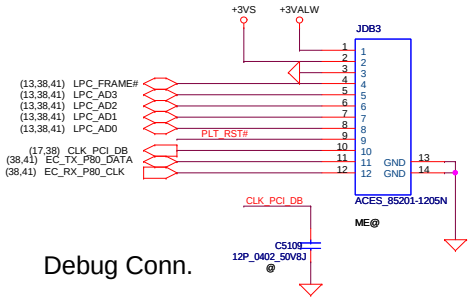
PN:SP01000R400



TPM



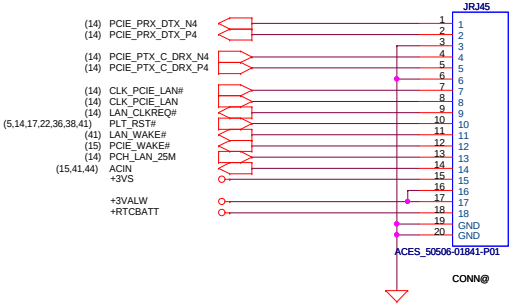




Debug Conn.

RJ45 Board

PN:SP01001CB00



Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: **PWR Button/Power OK/RJ45**

Size	Document Number	Rev
Custom	LA-8133P	1.0

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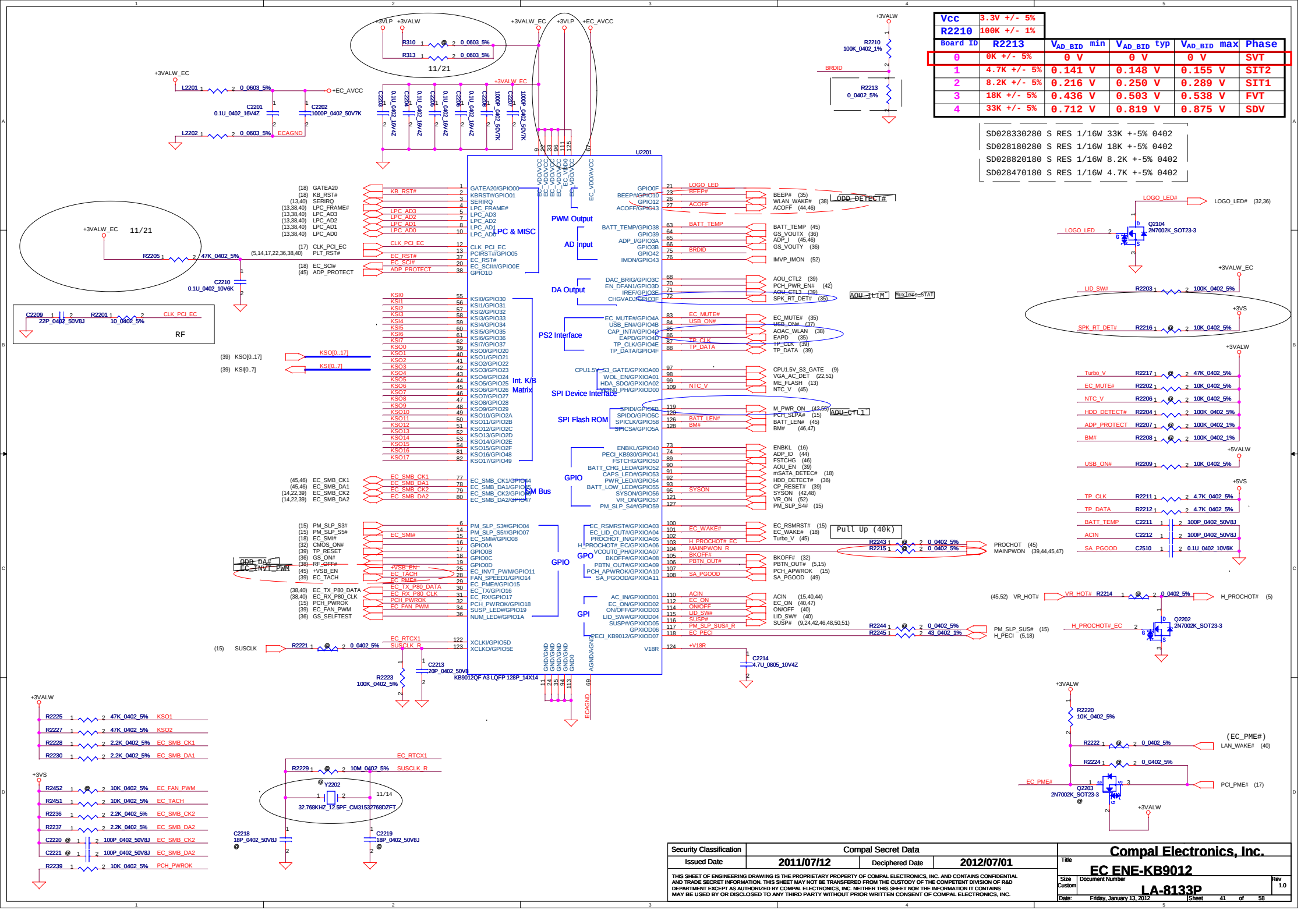
Vcc 3.3V +/- 5%
R2210 100K +/- 1%
Board ID | R2213 | VAD_BID min | VAD_BID typ | VAD_BID max | Phase
0 | 0K +/- 5% | 0 V | 0 V | 0 V | SVT
1 | 4.7K +/- 5% | 0.141 V | 0.148 V | 0.155 V | SIT2
2 | 8.2K +/- 5% | 0.216 V | 0.250 V | 0.289 V | SIT1
3 | 18K +/- 5% | 0.436 V | 0.503 V | 0.538 V | FVT
4 | 33K +/- 5% | 0.712 V | 0.819 V | 0.875 V | SDV
SD028330280 S RES 1/16W 33K +-5% 0402
SD028180280 S RES 1/16W 18K +-5% 0402
SD028820180 S RES 1/16W 8.2K +-5% 0402
SD028470180 S RES 1/16W 4.7K +-5% 0402
U2201
KB9012QF A3 LQFP 128P_14X14
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
GPIO
SM Bus
GPO
GPI
RF
Pull Up (40k)
Security Classification
Compal Secret Data
Issued Date
2011/07/12
Deciphered Date
2012/07/01
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Compal Electronics, Inc.
Title
EC ENE-KB9012
Size Custom
Document Number
LA-8133P
Rev 1.0
Date: Friday, January 13, 2012
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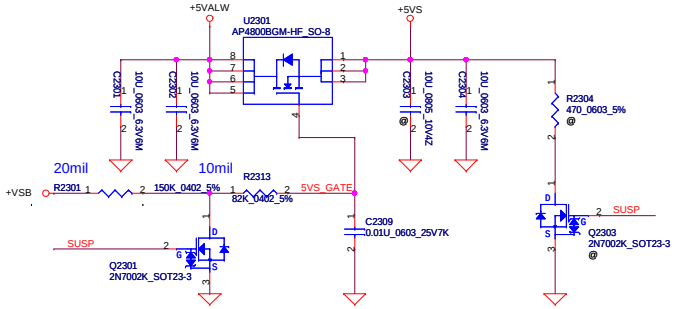
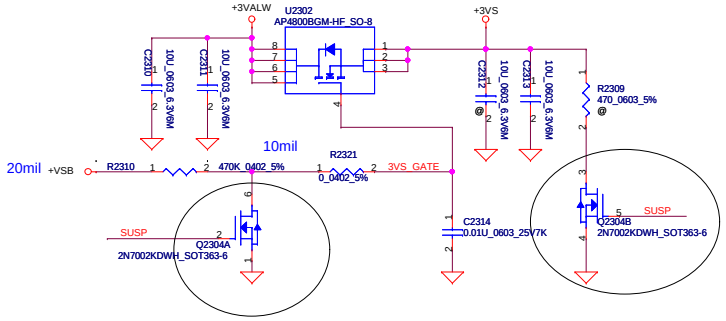
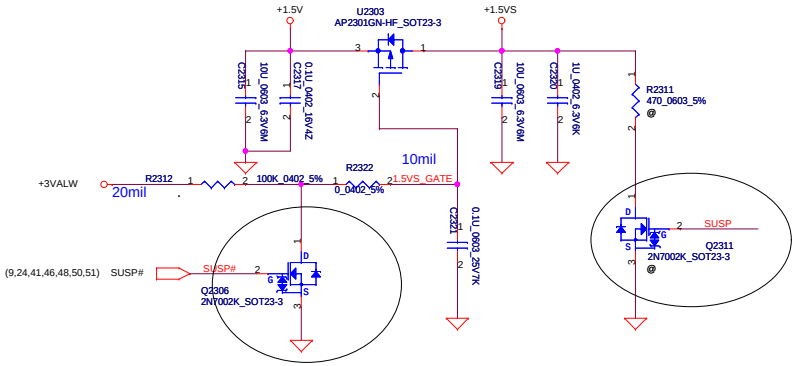
+5VALW TO +5VS

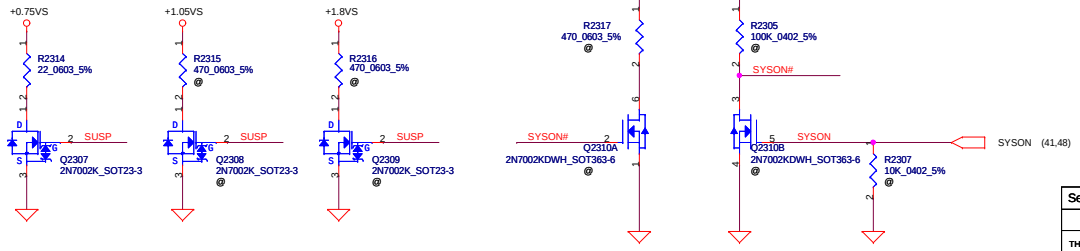


+3VALW TO +3VS



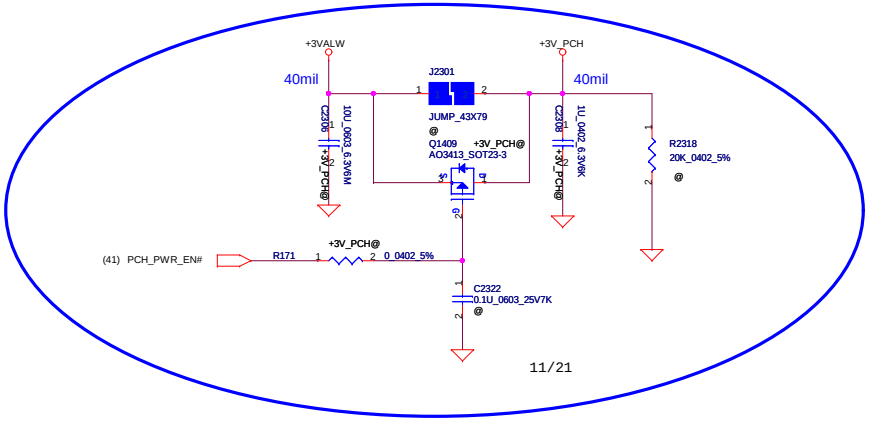
+1.5V to +1.5VS

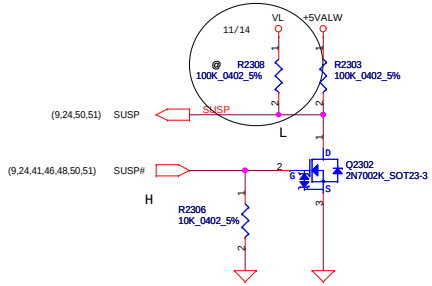


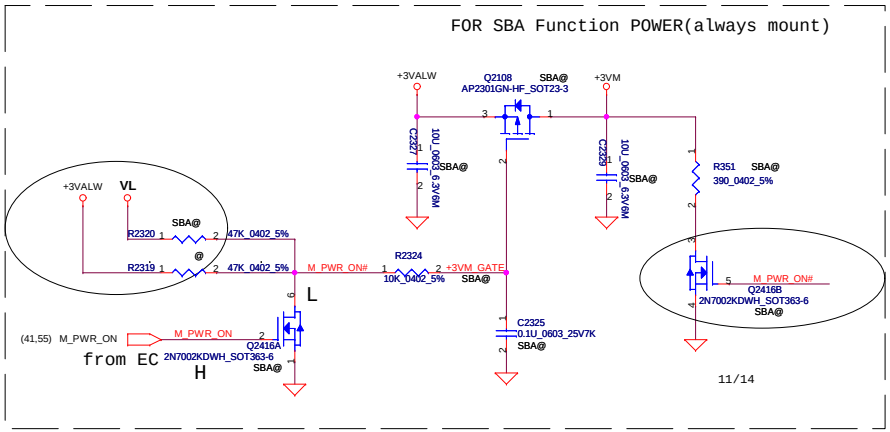


+3VALW TO +3VALW(PCH AUX Power)

Short J2301 for PCH VCCSUS3.3







Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: DC Interface

Size: Custom | Document Number: LA-8133P | Rev: 1.0

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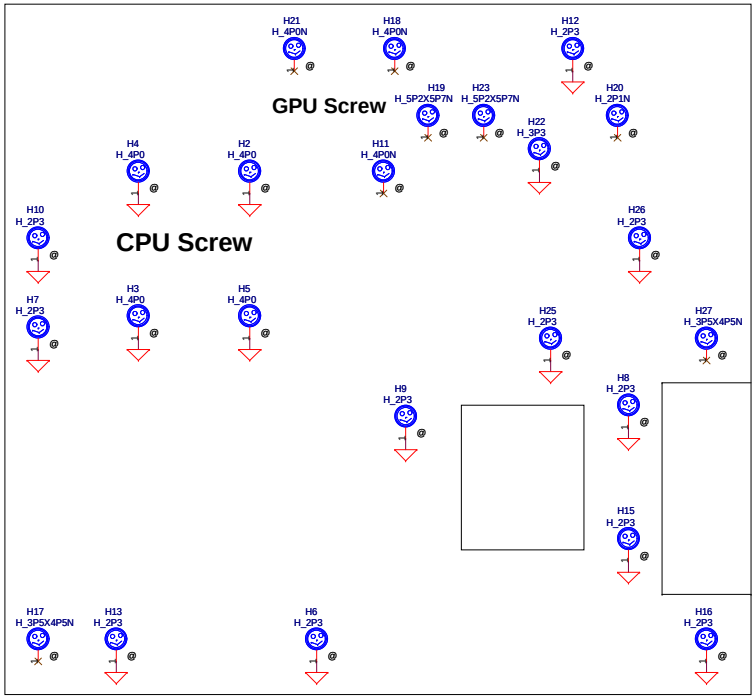
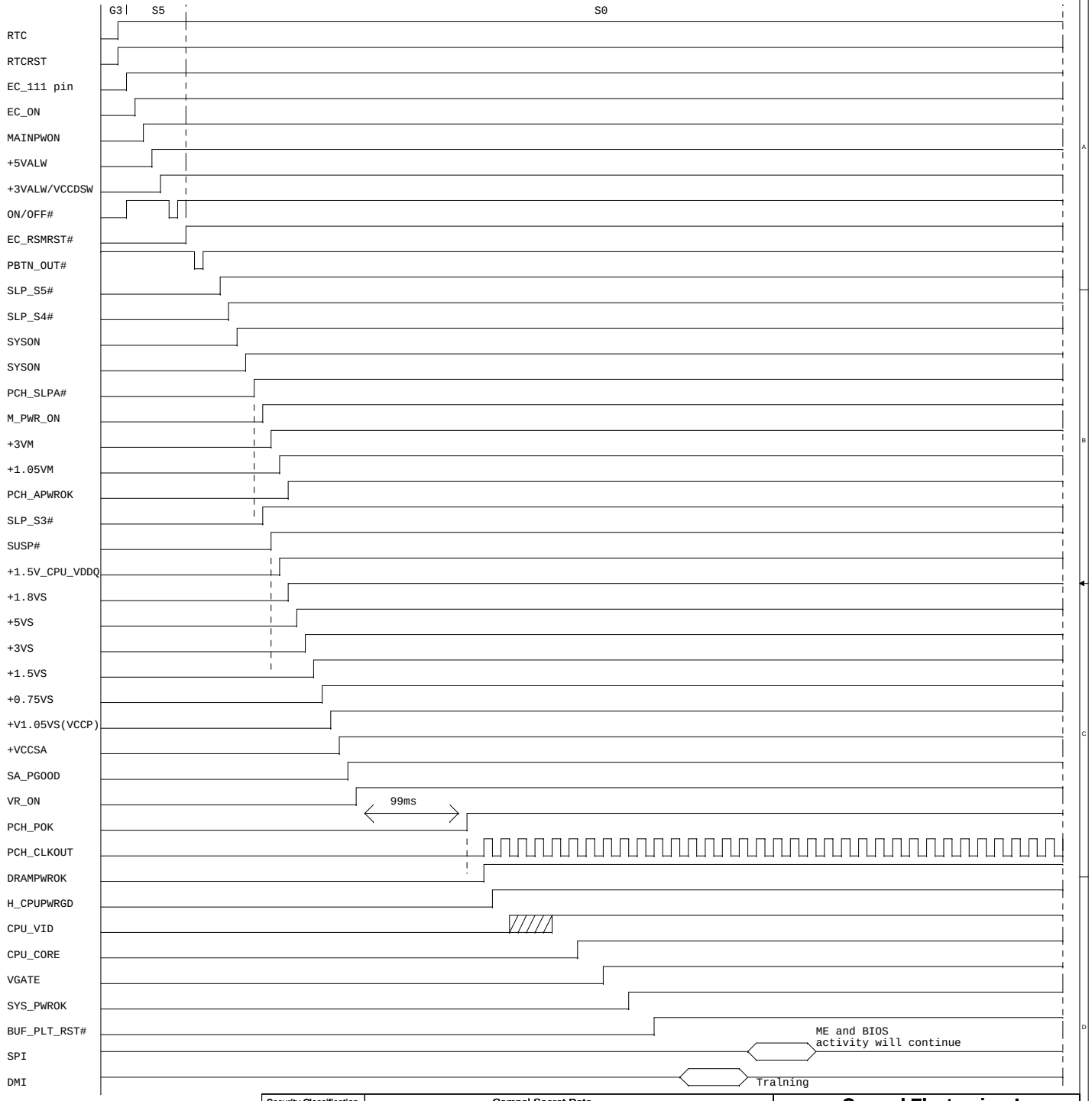
Screw Hole & FD

FD1 FIDUCIAL_C40M80
FD2 FIDUCIAL_C40M80
FD3 FIDUCIAL_C40M80
FD4 FIDUCIAL_C40M80





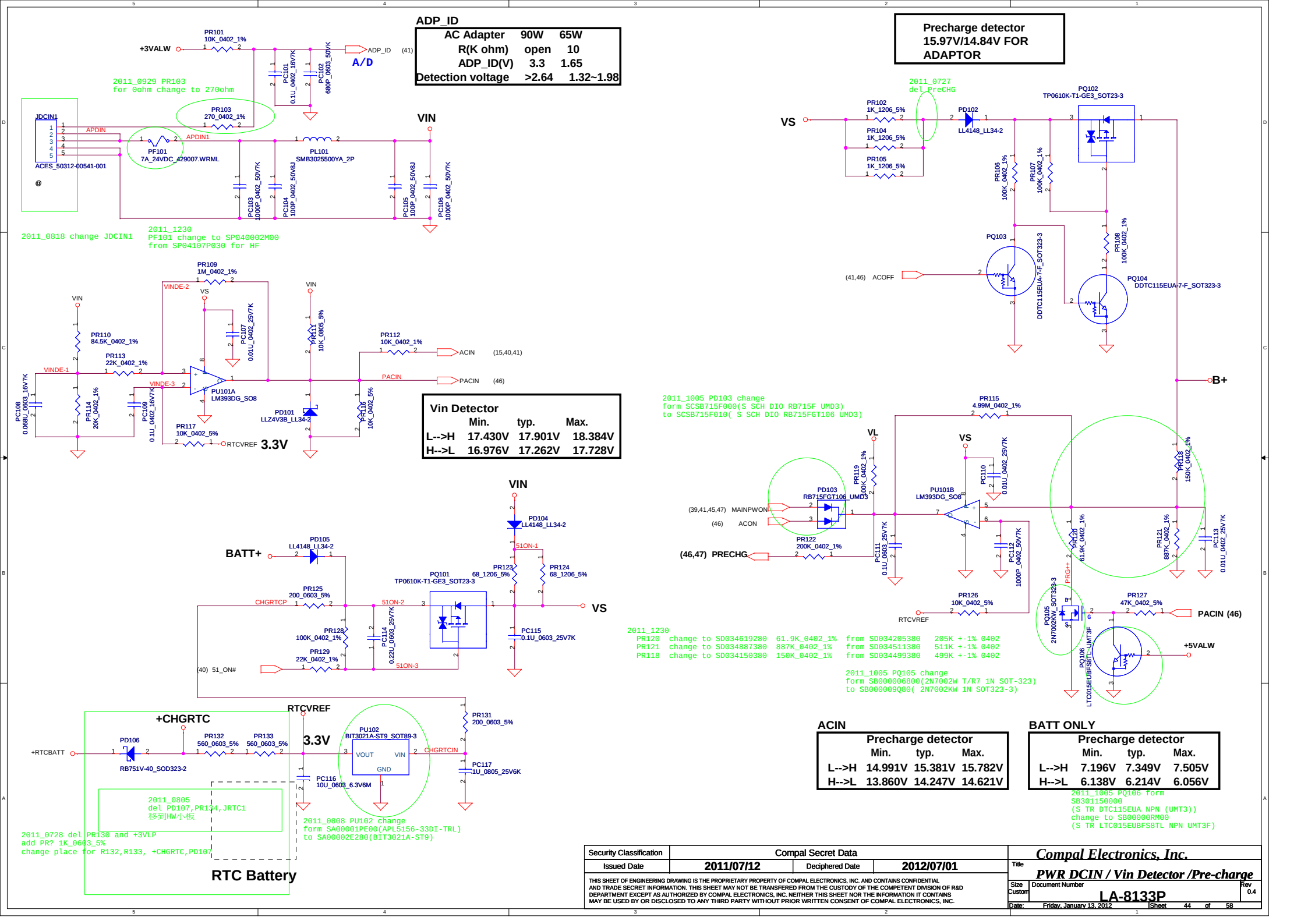
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: **Screw Hole**

Size	Document Number	Rev
Custom	LA-8133P	1.0

Date: Friday, January 13, 2012 Sheet 43 of 58


ADP_ID
AC Adapter 90W 65W
R(K ohm) open 10
ADP_ID(V) 3.3 1.65
Detection voltage >2.64 1.32~1.98
Precharge detector
15.97V/14.84V FOR
ADAPTOR
Vin Detector
Min. typ. Max.
L-->H 17.430V 17.901V 18.384V
H-->L 16.976V 17.262V 17.728V
ACIN
Precharge detector
Min. typ. Max.
L-->H 14.991V 15.381V 15.782V
H-->L 13.860V 14.247V 14.621V
BATT ONLY
Precharge detector
Min. typ. Max.
L-->H 7.196V 7.349V 7.505V
H-->L 6.138V 6.214V 6.056V
RTC Battery
2011_0929 PR103 for 0ohm change to 270ohm
2011_0818 change JDCIN1
2011_1230 PF101 change to SP040002M00 from SP04107P030 for HF
2011_0727 del_PreCHG
2011_1005 PD103 change form SCSB715F000(S SCH DIO RB715F UMD3) to SCSB715F010(S SCH DIO RB715FGT106 UMD3)
2011_1230
PR120 change to SD034619280 61.9K_0402_1% from SD034205380 205K +-1% 0402
PR121 change to SD034887380 887K_0402_1% from SD034511380 511K +-1% 0402
PR118 change to SD034150380 150K_0402_1% from SD034499380 499K +-1% 0402
2011_1005 PQ105 change form SB000006800(2N7002W T/R7 1N SOT-323) to SB000009Q80(2N7002KW 1N SOT323-3)
2011_1005 PQ106 form SB301150000 (S TR DTC115EUA NPN (UMT3)) change to SB00000RM00 (S TR LTC015EUBFS8TL NPN UMT3F)
2011_0805 del PD107,PR134,JRTC1 移到HW小板
2011_0728 del PR130 and +3VLP add PR? 1K_0603_5% change place for R132,R133, +CHGRTC,PD107
2011_0808 PU102 change form SA00001PE00(APL5156-33DI-TRL) to SA00002E280(BIT3021A-ST9)
Security Classification: Compal Secret Data
Issued Date: 2011/07/12 Deciphered Date: 2012/07/01
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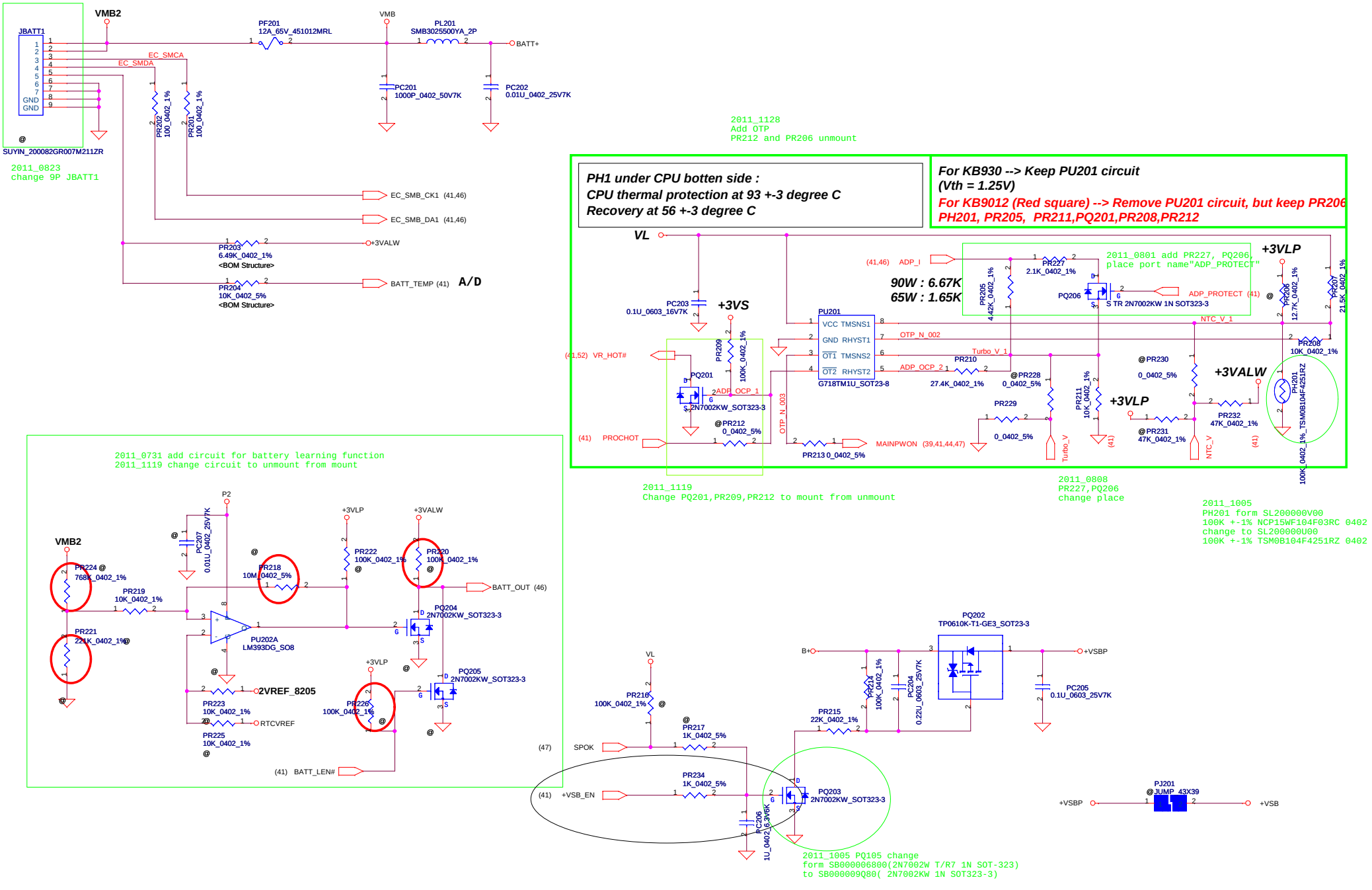
Compal Electronics, Inc.
Title: PWR DCIN / Vin Detector /Pre-charge
Size: Custom Document Number: LA-8133P Rev: 0.4
Date: Friday, January 13, 2012 Sheet 44 of 58



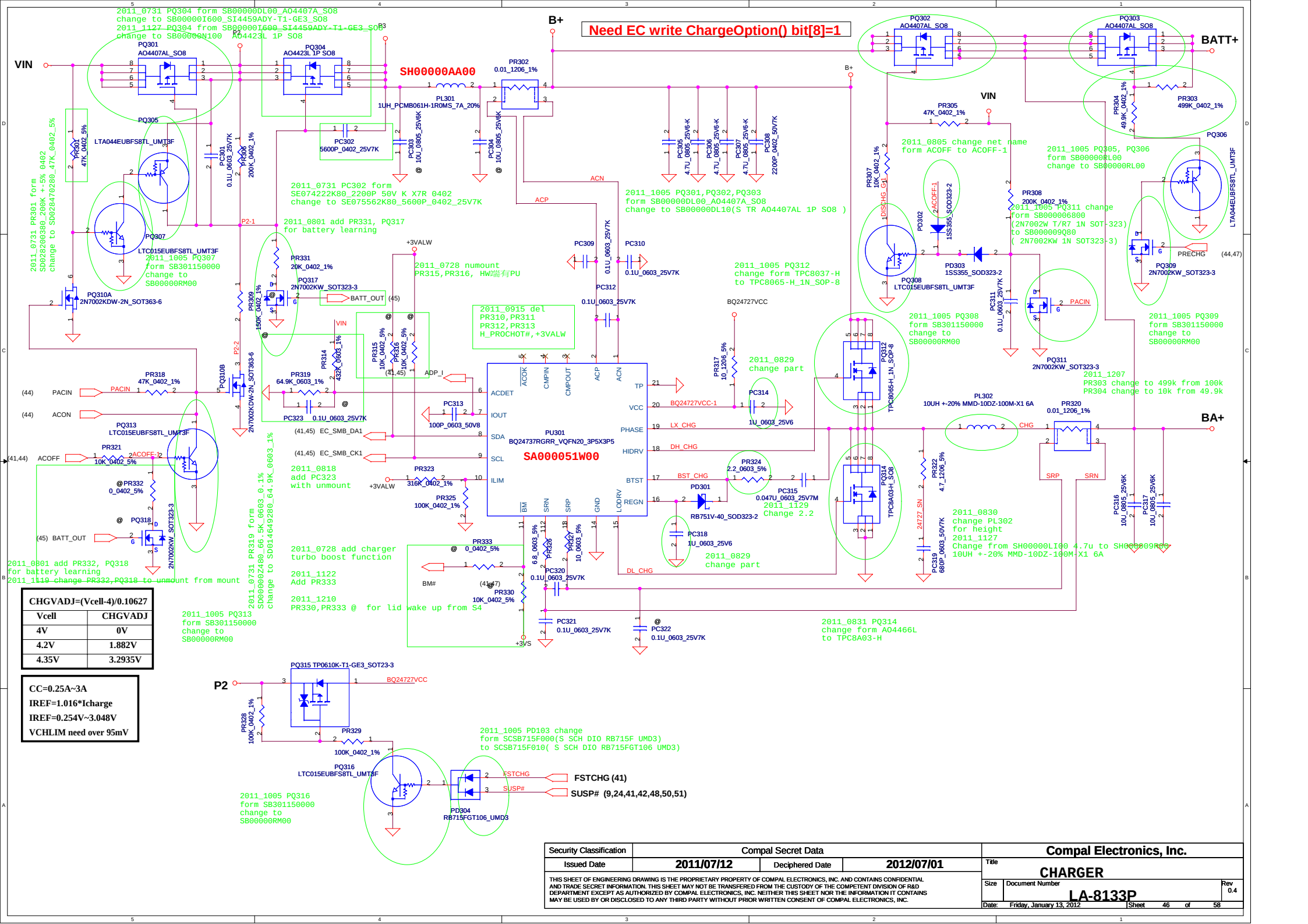
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: PWR-BATTERY CONN/OTP

Size: Custom | Document Number: LA-8133P | Rev: 0.4

Date: Friday, January 13, 2012 | Sheet 45 of 58


Need EC write ChargeOption() bit[8]=1
SH00000AA00
SA000051W00
VIN
BATT+
B+
BA+
P2
PU301
BQ24737RGRR_VQFN20_3P5X3P5
2011_0731 PQ304 form SB00000DL00_AO4407A_SO8
change to SB00000I600_SI4459ADY-T1-GE3_SO8
2011_1127 PQ304 from SB00000I600_SI4459ADY-T1-GE3_SO8
change to SB00000N100 AO4423L 1P SO8
2011_0731 PR301 form
SD028200380_200K +-5% 0402
change to SD028470280_47K_0402_5%
2011_0731 PC302 form
SE074222K80_2200P 50V K X7R 0402
change to SE075562K80_5600P_0402_25V7K
2011_0801 add PR331, PQ317
for battery learning
2011_1005 PQ307
form SB301150000
change to
SB00000RM00
2011_0728 numount
PR315,PR316, HW端有PU
2011_0915 del
PR310,PR311
PR312,PR313
H_PROCHOT#,+3VALW
2011_1005 PQ301,PQ302,PQ303
form SB00000DL00_AO4407A_SO8
change to SB00000DL10(S TR AO4407AL 1P SO8)
2011_1005 PQ312
change form TPC8037-H
to TPC8065-H_1N_SOP-8
2011_0829
change part
2011_0805 change net name
form ACOFF to ACOFF-1
2011_1005 PQ305, PQ306
form SB00000RL00
change to SB00000RL00
2011_1005 PQ311 change
form SB000006800
(2N7002W T/R7 1N SOT-323)
to SB000009Q80
(2N7002KW 1N SOT323-3)
2011_1005 PQ308
form SB301150000
change to
SB00000RM00
2011_1005 PQ309
form SB301150000
change to
SB00000RM00
2011_1207
PR303 change to 499k from 100k
PR304 change to 10k from 49.9k
2011_0818
add PC323
with unmount
2011_0728 add charger
turbo boost function
2011_1122
Add PR333
2011_1210
PR330,PR333 @ for lid wake up from S4
2011_0731 PR319 form
SD000002480_66.5K_0603_0.1%
change to SD014649280_64.9K_0603_1%
2011_1005 PQ313
form SB301150000
change to
SB00000RM00
2011_0830
change PL302
for height
2011_1127
Change from SH00000LI00 4.7u to SH000009RC0
10UH +-20% MMD-10DZ-100M-X1 6A
2011_0831 PQ314
change form AO4466L
to TPC8A03-H
2011_0829
change part
2011_1129
Change 2.2
2011_0801 add PR332, PQ318
for battery learning
2011_1119 change PR332,PQ318 to unmount from mount
2011_1005 PD103 change
form SCSB715F000(S SCH DIO RB715F UMD3)
to SCSB715F010(S SCH DIO RB715FGT106 UMD3)
2011_1005 PQ316
form SB301150000
change to
SB00000RM00
CHGVADJ=(Vcell-4)/0.10627
Vcell | CHGVADJ
4V | 0V
4.2V | 1.882V
4.35V | 3.2935V
CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV
FSTCHG (41)
SUSP# (9,24,41,42,48,50,51)
Security Classification | Compal Secret Data
Issued Date | 2011/07/12 | Deciphered Date | 2012/07/01
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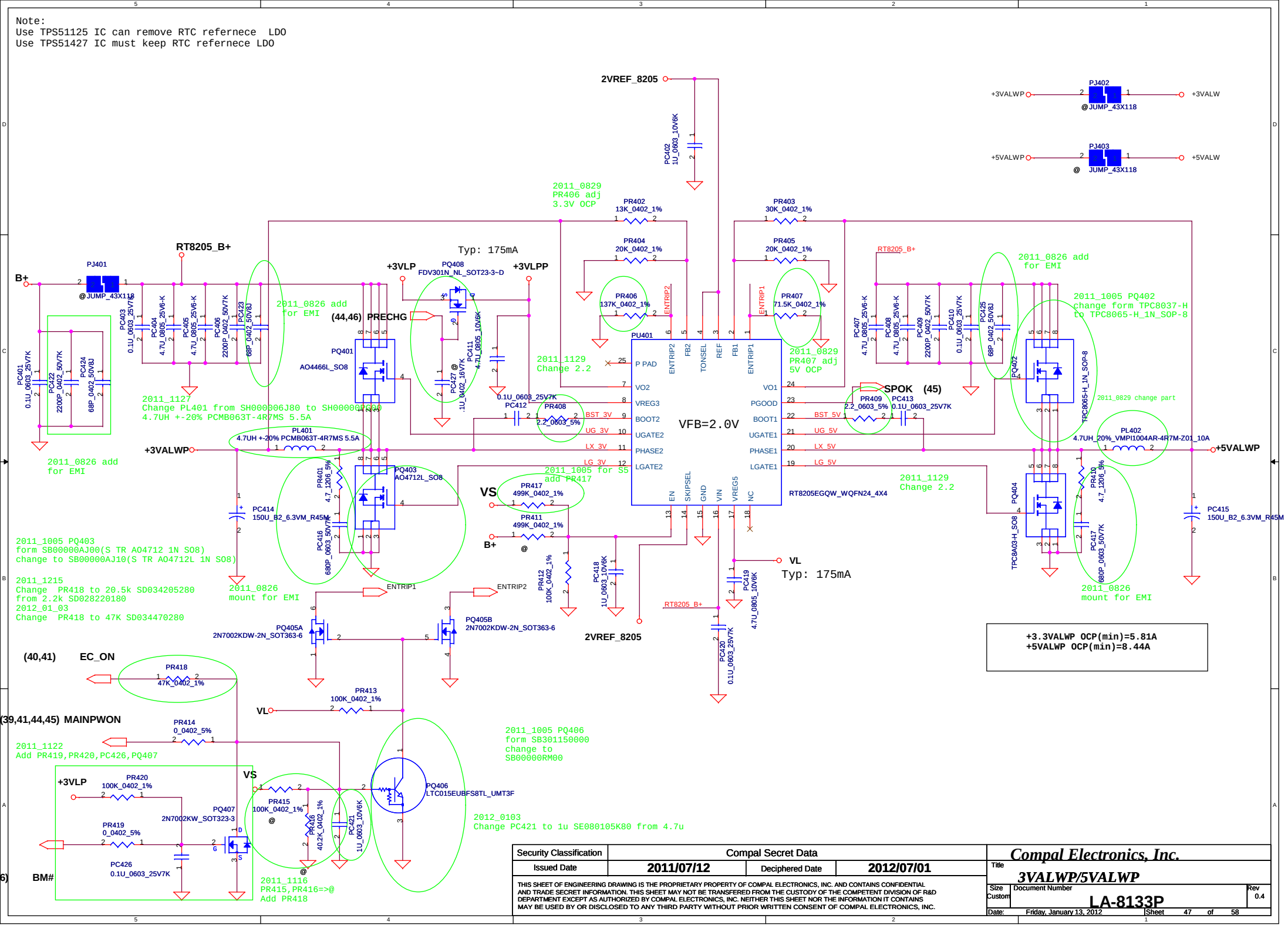
Compal Electronics, Inc.
Title
CHARGER
Size | Document Number | Rev
LA-8133P | 0.4
Date: Friday, January 13, 2012 | Sheet 46 of 58

Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



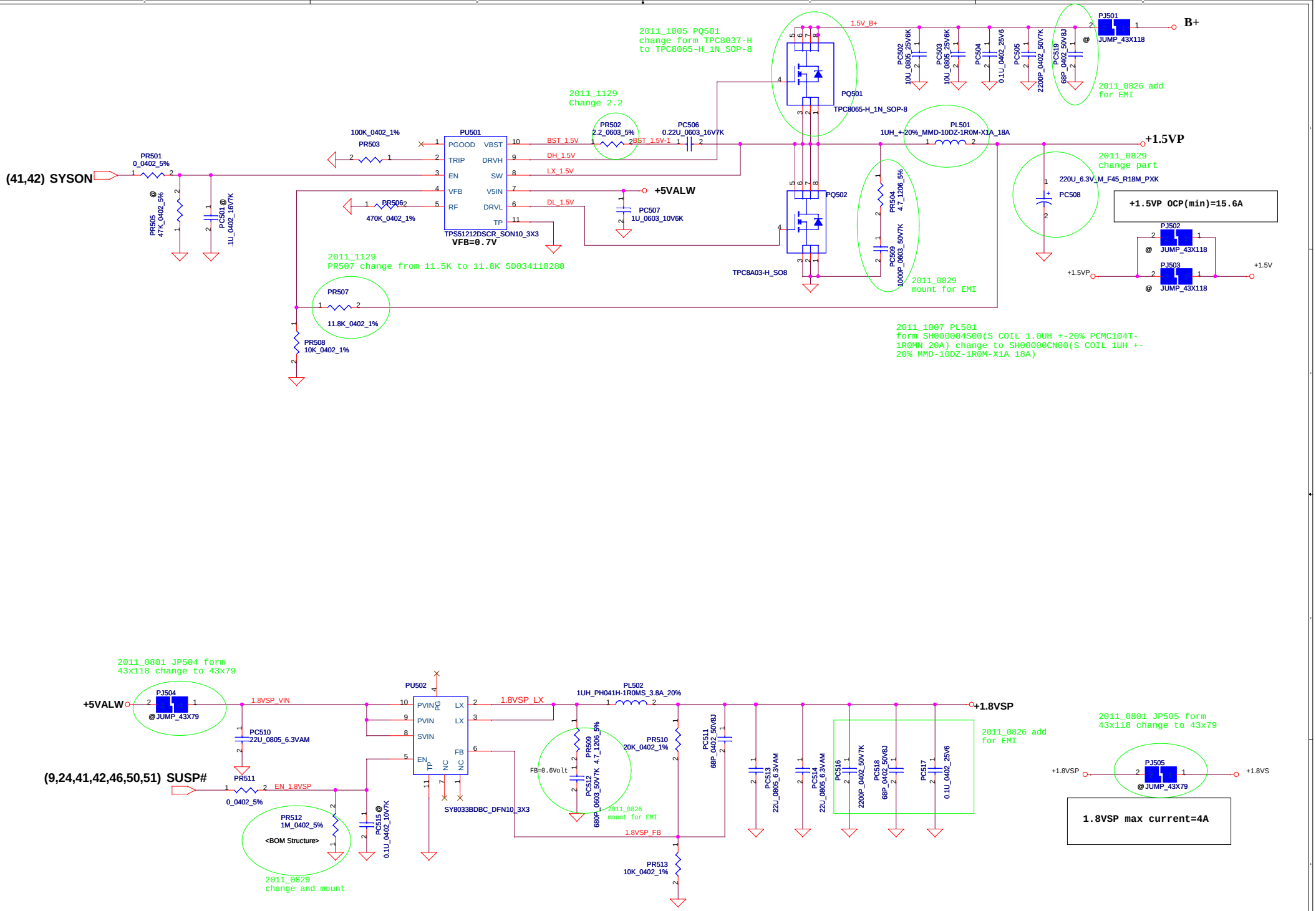
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: 3VALWP/5VALWP

Size: Custom | Document Number: LA-8133P | Rev: 0.4

Date: Friday, January 13, 2012 | Sheet 47 of 58



Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: PWR-+1.5VP/+1.8VSP

Size	Document Number	Rev
Custom	LA-8133P	0.4

Date: Friday, January 13, 2012 Sheet 48 of 58

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A

The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.

2011_0818 change VCCSA of enable name

2011_0826 add for EMI

2011_0826 mount for EMI

2011_0929 del PC606 (22U_0805_6.3V6M)

2011_1012 PC607 PC610 mount for RF

2011_0801 del +V1.05S_VCCPP circuit

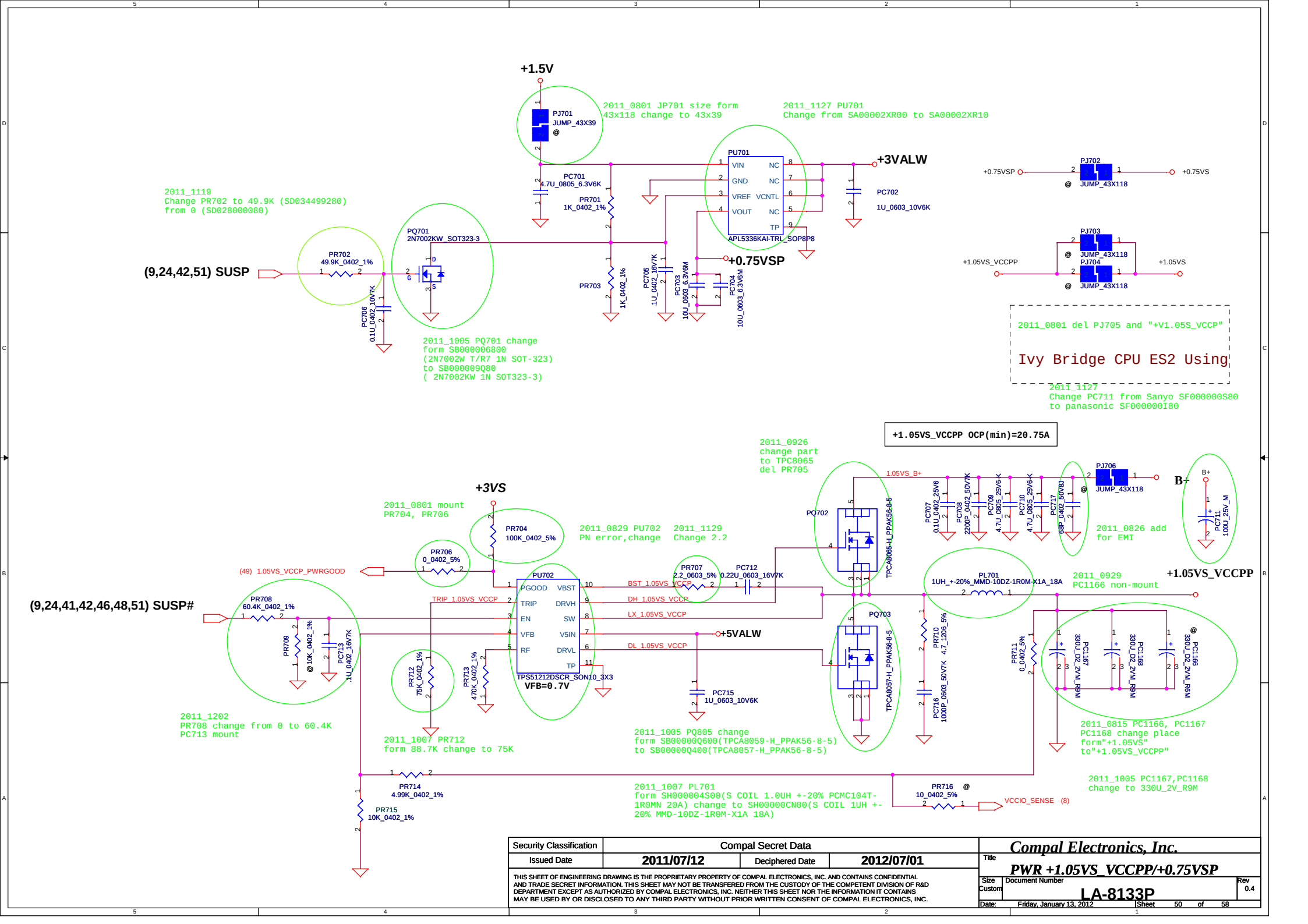
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: PWR +VCCSAP/1.0

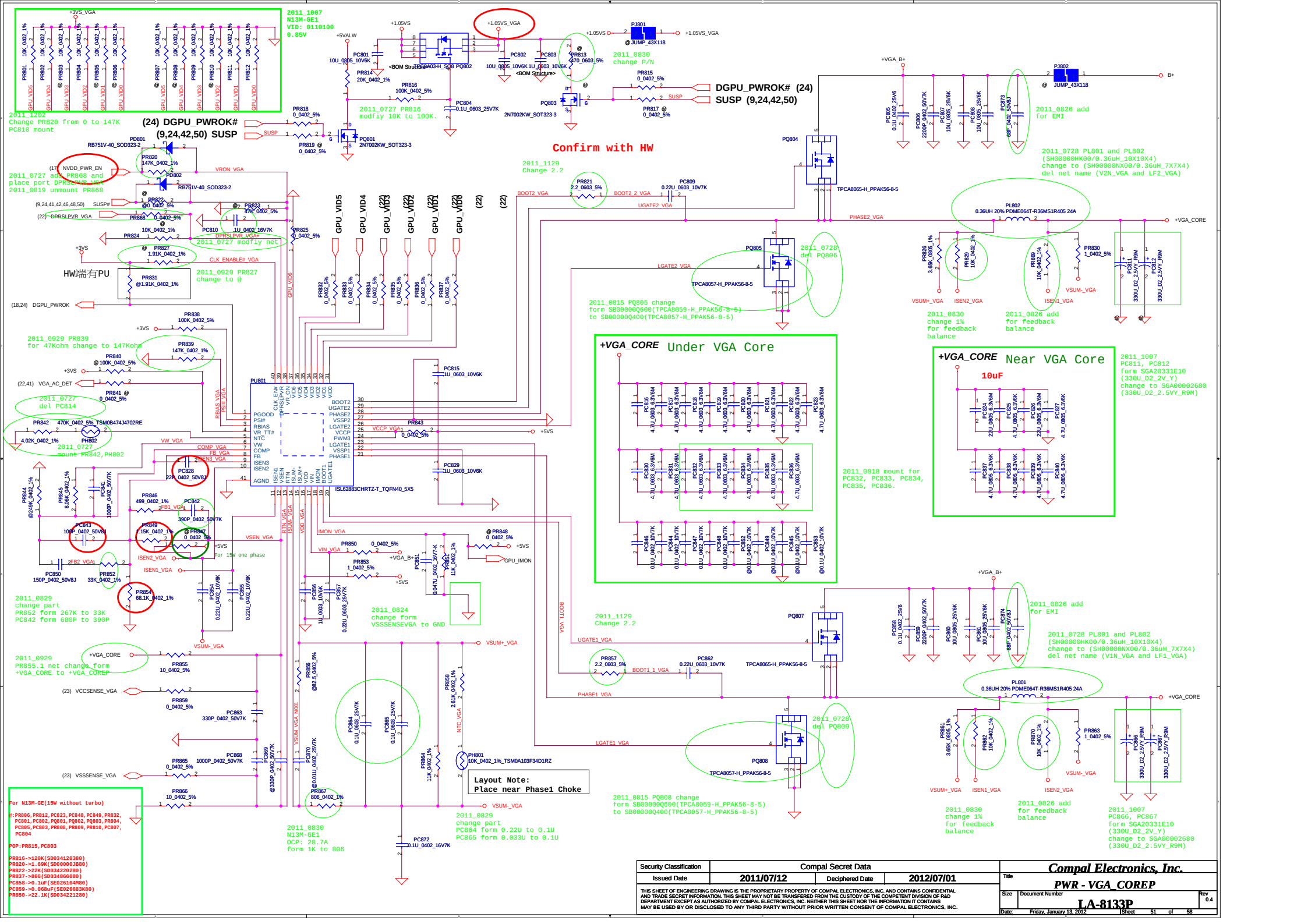
Size: C | Document Number: LA-8133P | Rev: 0.4

Date: Friday, January 13, 2012 | Sheet 49 of 58



Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.			
Title	PWR +1.05VS_VCCPP/+0.75VSP		
Size	Custom	Document Number	LA-8133P
Rev	0.4		
Date:	Friday, January 13, 2012	Sheet	50 of 58


2011_1007
N13M-GE1
VID: 0110100
0.85V
(24) DGPU_PWROK#
(9,24,42,50) SUSP
DGPU_PWROK# (24)
SUSP (9,24,42,50)
Confirm with HW
2011_1202
Change PR820 from 0 to 147K
PC810 mount
2011_0727 add PR868 and
place port DPRSLPVR_VGA
2011_0819 unmount PR868
HW端有PU
2011_0929 PR827
change to @
2011_0727
modfiy net
2011_0929 PR839
for 47Kohm change to 147Kohm
2011_0727
del PC814
2011_0727
mount PR842,PH802
2011_0829
change part
PR852 form 267K to 33K
PC842 form 680P to 390P
2011_0929
PR855.1 net change form
+VGA_CORE to +VGA_COREP
2011_0830
N13M-GE1
OCP: 28.7A
form 1K to 806
2011_0824
change form
VSSSENSEVGA to GND
2011_0829
change part
PC864 form 0.22U to 0.1U
PC865 form 0.033U to 0.1U
Layout Note:
Place near Phase1 Choke
2011_0727 PR816
modfiy 10K to 100K.
2011_0830
change P/N
2011_1129
Change 2.2
2011_0728
del PQ806
2011_0815 PQ805 change
form SB00000Q600(TPCA8059-H_PPAK56-8-5)
to SB00000Q400(TPCA8057-H_PPAK56-8-5)
2011_0826 add
for EMI
2011_0728 PL801 and PL802
(SH00000HK00/0.36uH_10X10X4)
change to (SH00000NX00/0.36uH_7X7X4)
del net name (V2N_VGA and LF2_VGA)
2011_0830
change 1%
for feedback
balance
2011_0826 add
for feedback
balance
+VGA_CORE Under VGA Core
2011_0818 mount for
PC832, PC833, PC834,
PC835, PC836.
+VGA_CORE Near VGA Core
10uF
2011_1007
PC811, PC812
form SGA20331E10
(330U_D2_2V_Y)
change to SGA00002680
(330U_D2_2.5VY_R9M)
2011_1129
Change 2.2
2011_0728
del PQ809
2011_0815 PQ808 change
form SB00000Q600(TPCA8059-H_PPAK56-8-5)
to SB00000Q400(TPCA8057-H_PPAK56-8-5)
2011_0826 add
for EMI
2011_0728 PL801 and PL802
(SH00000HK00/0.36uH_10X10X4)
change to (SH00000NX00/0.36uH_7X7X4)
del net name (V1N_VGA and LF1_VGA)
2011_0830
change 1%
for feedback
balance
2011_0826 add
for feedback
balance
2011_1007
PC866, PC867
form SGA20331E10
(330U_D2_2V_Y)
change to SGA00002680
(330U_D2_2.5VY_R9M)
For N13M-GE(15W without turbo)
R:PR806,PR812,PC823,PC848,PC849,PR832,
PC801,PC802,PQ801,PQ802,PQ803,PR804,
PC805,PC803,PR808,PR809,PR810,PC807,
PC804
POP:PR815,PC803
PR816->120K(SD034120380)
PR820->1.69K(SD00000JB80)
PR822->22K(SD034220280)
PR837->866(SD034866080)
PC858->0.1uF(SE026104M80)
PC859->0.068uF(SE026683K80)
PR859->22.1K(SD034221280)
Security Classification
Compal Secret Data
Issued Date
2011/07/12
Deciphered Date
2012/07/01
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Compal Electronics, Inc.
Title
PWR - VGA_COREP
Size
Document Number
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0.4
Date: Friday, January 13, 2012
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2011_0830
PC901,PC905,PR901,PR903,PR904 mount

2011_1119
Change PC901,PC905 to 0.033u (SE076333K80)
from 0.033u (SE076333KN0)

2011_1007 for function test
1. modify PR903 form 1.21K to 8.2K,
2. PC905 form 4700p to 33n,
3. PC901 form 680p to 33n,
4. PR904 form 10.7K to 806,
5. PC907 form 330p to 560p
6. PC909 form 3300p to 1500p
7. PC904 form 330p to 820p
8. PR911 form 63.4K to 66.5K
9. PR942 form 4.32K to 6.04K
10. PC927 form 3300p to 2200p
11. PC934 330p to 820p

2011_0829
PC909
change part

2P: 24K
1P: 24.9K

PUT COLSE
TO GT
Inductor

2P: 21.5K
1P: 15.8K

2P: 1.65K
1P: 1K

PUT COLSE
TO V_GT
HOT SPOT

2011_0819 +V1.05VS_VCCP
change to +1.05VS

2011_0829
PR920,PR924,PR931
form 4.7 to 2.2

2P: 36K
1P: 26.1K

Option for
1 phase GFX

2Phase: @
1Phase: install

Option for
2 phase CPU

3Phase: @
2Phase: install

2011_0809
PR928 change place

2011_0930
add PR954 20k_0402_1%

2011_0930
add PR955 20k_0402_1%

2011_1005
for Intel add PC836 SE00000D180 (43P_0402_50V8J)

2011_1119
Change PC936 to 47P (SE071470J80)
form 43P (SE00000D180)

3P: 330p
2P: 1000p

3P: 22p
2P: 10p

3P: 73.2K
2P: 41.2K

3P: 21K
2P: 12.4K

3P: 6.04K
2P: 4.32K

3P: 1500p
2P: 1200p

3P: 2200p
2P: 3300p

3P: 348
2P: 1.21K

3P: 3.65K
2P: 9.53K

3P: 23.7K
2P: 24.9K

3P: 1K
2P: 1K

PUT COLSE
TO VCORE
Phase 1
Inductor

PUT COLSE
TO VCORE
HOT SPOT

NCP6132AMNR2G_QFN60_7X7

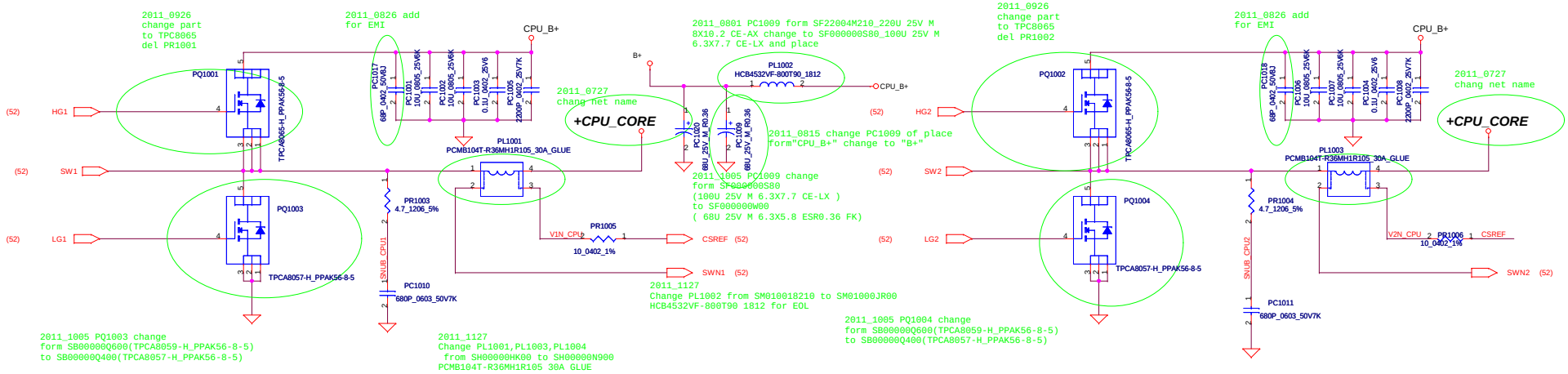
Security Classification	Compal Secret Data
Issued Date	2011/07/12
Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: PWR-CPU_CORE1

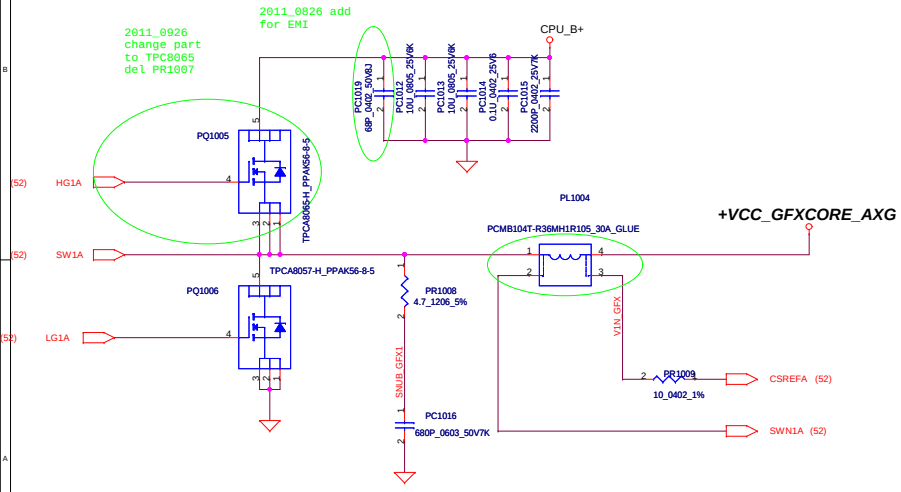
Size: Custom | Document Number: LA-8133P | Rev: 0.4

Date: Friday, January 13, 2012 | Sheet 52 of 58



QC 45W CPU
VID1=0.9V
IccMax=94A
Icc_Dyn=66A
Icc_TDC=52A
R_LL=1.9m ohm
OCP~110A

DC 35W CPU
VID1=1.05V
IccMax=53A
Icc_Dyn=43A
Icc_TDC=36A
R_LL=1.9m ohm
OCP~65A



QC 45W GT2
VID1=1.23V
IccMax=46A
Icc_Dyn=37A
Icc_TDC=38A
R_LL=3.9m ohm
OCP~55A

DC 35W GT2
VID1=1.23V
IccMax=33A
Icc_Dyn=20.2A
Icc_TDC=21.5A
R_LL=3.9m ohm
OCP~40A

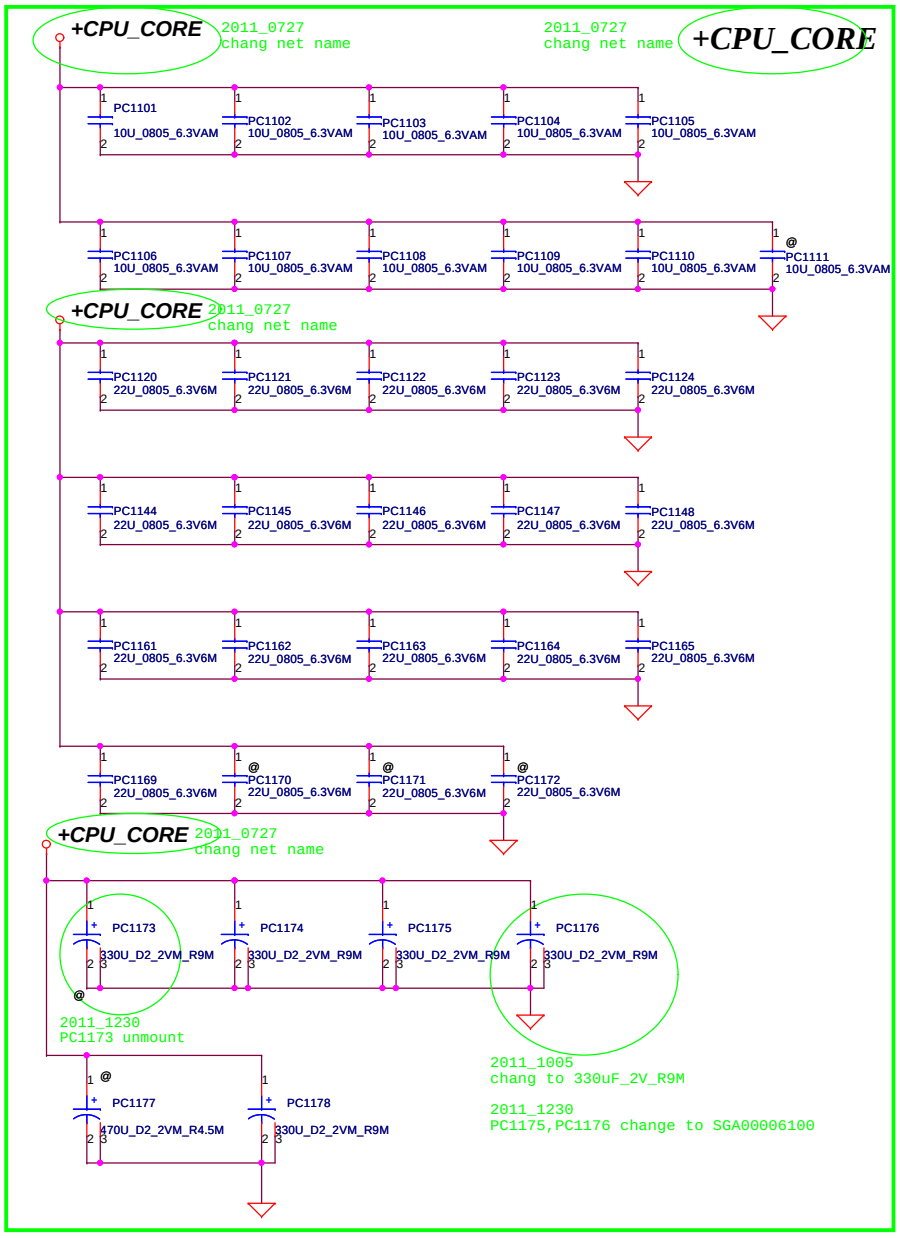
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

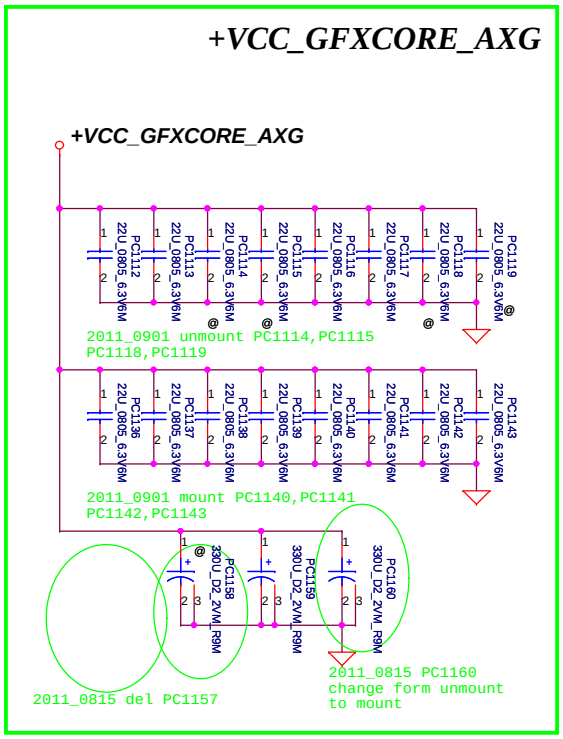
Compal Electronics, Inc.

Title: PWR-CPU_CORE2

Size	Document Number	Rev
C	LA-8133P	0.4

Date: Friday, January 13, 2012 Sheet 53 of 58

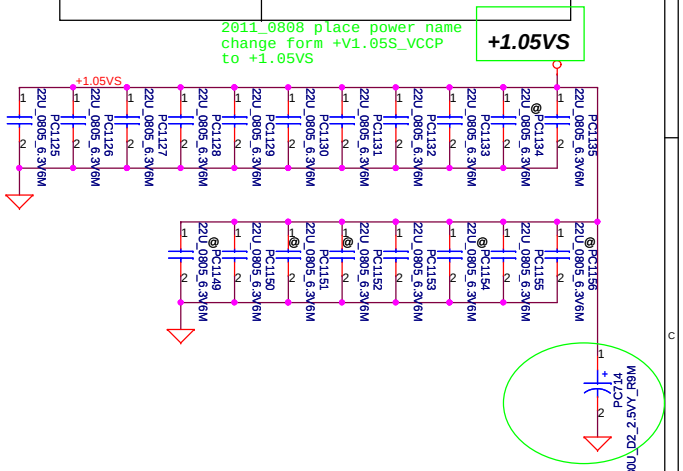




2011_07929
PC1158 non-mount

Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 µF (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 µF (0805) 2 x (0805) no-stuff sites



2011_0815 PC714 change place
form "+1.05VS_VCCPP" to "+1.05VS"

2011_1005 PC714 change to
330uF_2V_R9M

2011_1007
PC714
form SGA00001Q802
(S POLY C 330U 2V M X LESR6M SX H1.9)
change to SGA00002680
(330U_D2_2.5VY_R9M)

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

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Title: PWR - PROCESSOR DECOUPLING

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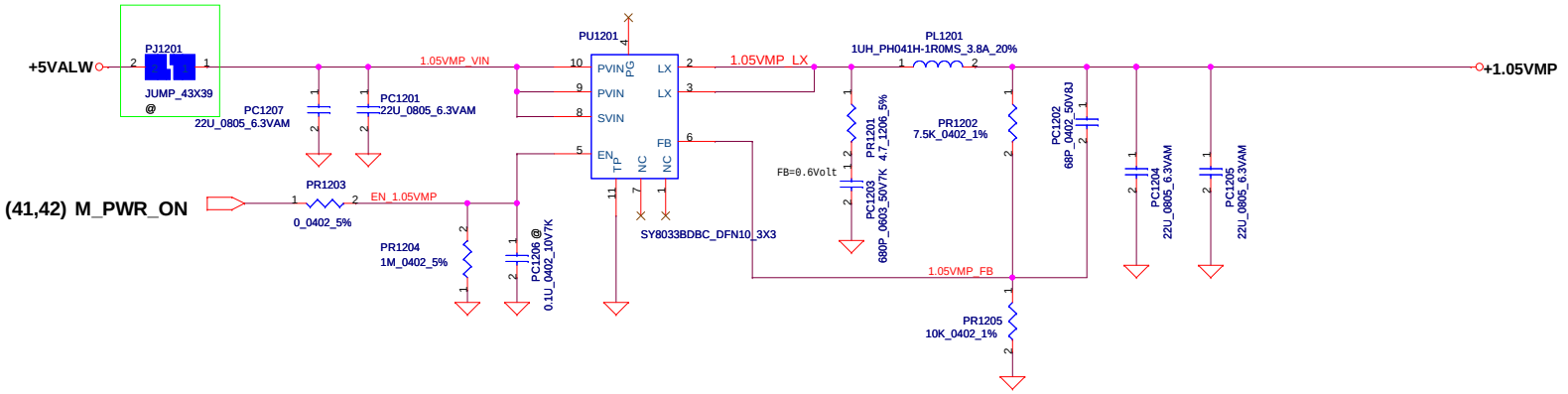
2011_0923 JUMP form 43X79 change to 43X79



1.05VMP max current=1A

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: PWR-+1.05VMP

Size: Custom | Document Number: LA-8133P | Rev: 0.4

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Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: **PWR-Thermal Protect**

Size	Document Number	Rev
	LA-8133P	1.0

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Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: **PIR (PWR)**

Size	Document Number	Rev
Custom	LA-8133P	1.0

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Version Change List (P.I.R. List)

Phase	Date	No.	BOM	Sch	Layout	Description	function
	2011/09/13	No1		V	V	Add C2325,C2326,C2327,C2328,C2329,R2319,R2324,Q2312	Add SBA function (+3VM) power
	2011/09/15	No2		V		Del Q2305	Del SYSYON#
	2011/09/15	No3		V		Add EC pin 119(M_PWR_ON) for SBA function	Add SBA function
	2011/09/15	No4		V		Add EC pin 120(PCH_SLPA#) from PCH to EC for SBA function	Add SBA function
	2011/09/15	No5		V		Add EC pin72 (Muxless_STAT) for GPU STAT	Add Muxless_STAT function
	2011/09/15	No6		V		Del PR310, PR311, PR312, PR313, net name:"H_PROCHOT#", +3VALW.	PWR-CHARGER-BQ24727
	2011/09/15	No7	V			mount PC832	
	2011/09/15	No8		V	V	Add R2482,Q2404,C2509,R2481,R2485,Q2400,R2483,C2501	AOAC Function
	2011/09/15	No9		V	V	change net name BT_OFF# to BT_ON# and change PCH EN GPIO from GPIO34 to GPIO36 R280 from @ to mount,R282 from mount to @	BT Function
	2011/09/15	No10		V	V	change net name(Mini-Express) from BT_OFF# to WLBT_OFF# PCH EN GPIO change to GPIO34	BT Function
	2011/09/19	No11		V	V	change +3VS_WLAN net name to +3VS_AOAC change +3VS_WWAN net name to +3VS_AOAC	AOAC Function
	2011/09/19	No12		V	V	Del R1010 for LVDS CONN plug high voltage	LVDS CONN
	2011/09/19	No13		V	V	R1102,R1104,R1105 from @ to mount fix MIC(ECR97236)issue	MIC function
	2011/09/19	No14		V	V	Add R2470 for 80 port function	80 port function
	2011/09/19	No15		V	V	Del R2476 Add Q2405	BT Function
	2011/09/20	No16		V	V	Add power schematic 9/15 again modify RF PC423, PC425, PC519, PC620, PC717, PC873, PC874, PC424, PC518 PC1017, PC1018, PC1019, PC422, PC516, PC517 modify POWER在VGA的PWM IC 加的零件PR869, PR870	
	2011/09/22	No17		V	V	Add U10,C589,C645 for TPM function	TPM function
	2011/09/22	No18		V	V	Add R110,R112 for SPI POWER choose(SBA function)	
	2011/09/23	No19		V	V	modify power page 44~57(PJ1201 JUMP form 43X79 change to 43X79)	
	2011/09/26	No20		V	V	change CPU footprint from TYCO_2013620-2_989P-T to TYCO_2013620-2_989P-T-A39 change PCH footprint from PANTHER-POINT_FCBGA_989P-T to PANTHER-POINT_FCBGA_989P-T-A39 change GPU footprint N13P-PES-A1_FCBGA_908P to N13P-PES-A1_FCBGA_908P-A39 change VRAM footprint K4W1G1646E-HC12_FBGA_96P to K4W1G1646E-HC12_FBGA_96P-A39	
	2011/09/26	No21		V	V	change PCH_GPIO24(R288) pull up to +3V_PCH	
	2011/09/26	No22		V		change P18 (R311,R330,R286,R329) for UMA and Optimus memon	
	2011/09/26	No23		V		change net name PCH_THRMTRIP#_R to VGA_THRMTRIP#	
	2011/09/26	No24		V	V	PQ702 change to TPC8065,Del PR705 PQ1001,PQ1002,PQ1005 change to TOC8065,Del PR1001,PR1002,PR1007	
	2011/09/26	No25		V	V	p43 change Q2304 dual channel 2n7002 to single channel Q2304,Q2305(Q2305 @) p43 change Q2306 dual channel 2n7002 to single channel Q2306,Q2311(Q2311 @)	
	2011/09/27	No27	V			modify EC Board ID R2213 to 18K	
	2011/09/27	No28		V	V	net name CX_GPIO0 connect to U1101 pin 38	
	2011/09/27	No29		V	V	Add C2152,C2153,D2113 for ESD	
	2011/09/27	No30		V	V	change NVIDIA N13M ROM_SCLK from 15K PU to 5K PU	
	2011/09/27	No31		V	V	change ESD part D2401,D2403,D2405 power from +5VALW to +USB VCCA	
	2011/09/27	No32		V	V	Add C2108 for GPU_CLKREQA	
	2011/09/27	No33				Add Q2406 , modify R2401,Change PCH_GPIO19 to ODD_DET#,for zero power ODD	
	2011/09/27	No34				change WLBT_OFF# to PCH_GPIO34	
	2011/09/27	No35				change PCH_GPIO34 to WLBT_OFF#(mini card pin5)	
	2011/09/27	No36				change BT_ON# connect to WLBT_OFF#(mini card pin51)	
	2011/09/28	No37				C76 , R1123 , c1131 , R2201,C2209 C84,C85 from @ to mount for RF team	
	2011/09/29	No38				R1529 change to 15K	
	2011/09/29	No39				Add CONN JDB3 fo debug	
	2011/09/29	No40				Add R2460,R2438,R2471,R2472,R2475,R2476 for PS8520B	
	2011/09/29	No41				change D2403 ,D2401 power to +USB_VCCB,and del D2403 ,D2401,D2405 Pin3 net	
	2011/09/29	No42				change power schematic del PC606 (22U_0805_6.3V6M) PR855.1 net change form +VGA_CORE to +VGA_COREP PR827 mount change to @(non-mount) PR839 for 47Kohm change to 147Kohm PR103 for 0ohm change to 270ohm PC1166 non-mount,PC1173 non-mount,PC1158 non-mount	
	2011/09/29	No43				Add Q2313,C2305,C2306,C2307,C2308,R2318,R2320,R2320,C2322 for +3V_PCH	

	2011/09/29	No44				change CRT CONN to DC061109231(footprint pin modify)
						Add PR954,PR955
						Add H16,H27
						change Q2304.Q2305 to Q2304
						modify PTH H11,H18 ,H21
						Del T10 for SUS_STAT(SLP_S3# 走不出來)	

	2011/10/04	No46				reserve R352,R353 for SATA re-drive PS-8131B change net name fron WLBT_OFF to WLBT_OFF_5# modify PCH_GPIO34 connect to BT_ON# for BT module modify PCH_GPIO36 from BT_ON# connect to WLBT_OFF_51# for mini card BT combo module changr Q2301 to 2N7002	
	2011/10/05	No47				Del R2469,T49,T45,T41,T37,T36,T28,T26 for ME 限高0 changer power net +3VS_FP to +3VS update power schematics P44~P57	
	2011/10/06	No48				change Q1202 part to SB000007H10. change JCARD1 PN to SP02000H810 footprint: ACES_87213-1400G_14P change some CONN part NO. for ME CONN list Add D2416	

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