Compal Confidential

Cougar

Schematics Document

Intel Cedar Trail Processor/ Tiger point

2010-11-05

REV:0.1

Security Classification	Compal Secret Data		
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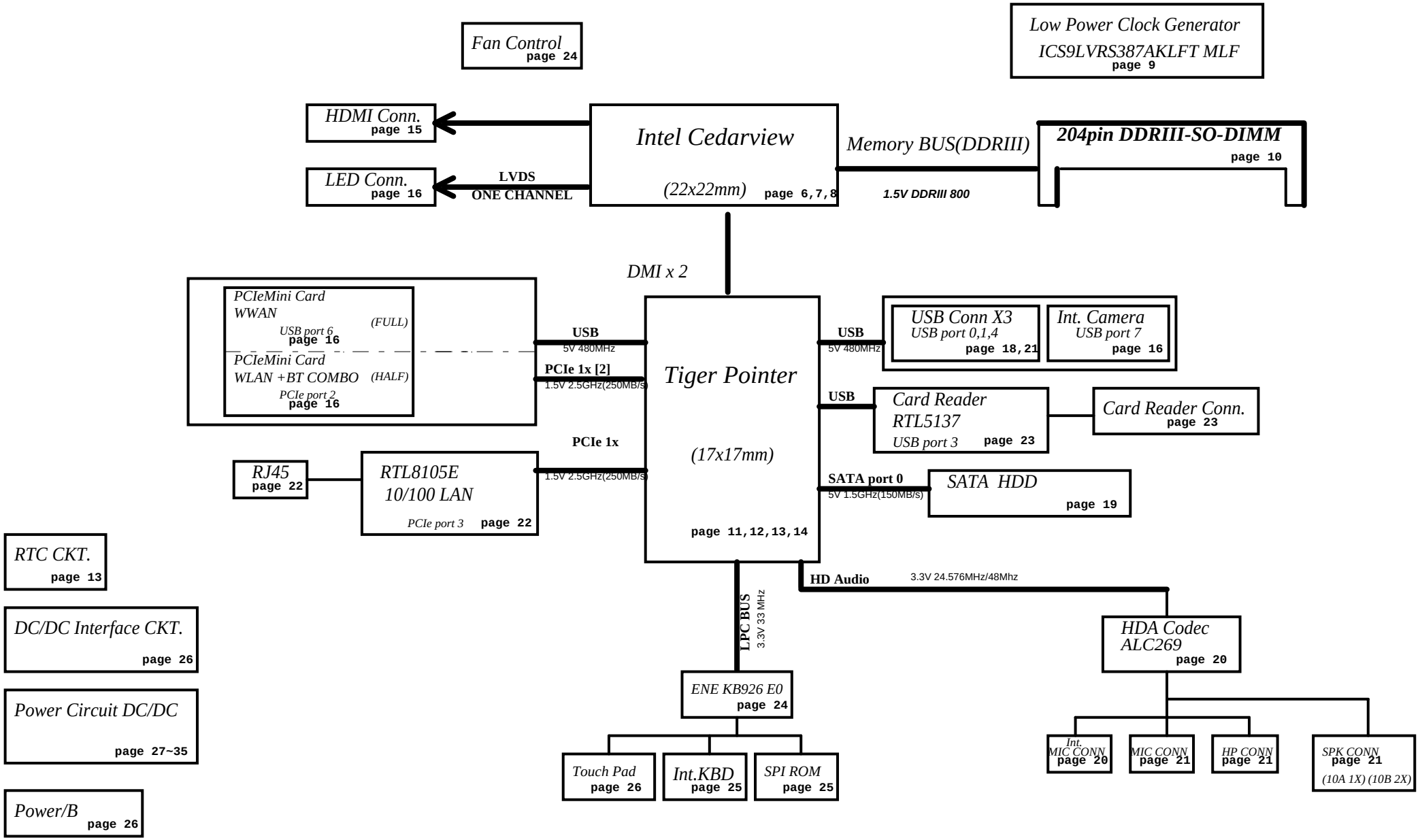
Model Name : PBU00
File Name : P



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Voltage Rails

Power Plane	Description	S1	S3	S5	G3
VIN	Adapter power supply (19V)	ON	ON	ON	OFF
B+	AC or battery power rail for power circuit.	ON	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+0.89VS	0.89VS GFX support voltage	ON	OFF	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF	OFF
+1.05VS	VCCP switched power rail	ON	OFF	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF	OFF
+1.5V	1.5V power rail for DDR	ON	ON	OFF	OFF
+1.8VS	1.8VS switched power rail	ON	OFF	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3V_WLAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	ON	OFF	OFF
+5VALW	5V always on power rail	ON	OFF	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON	OFF
+RTCVCC	RTC power	ON	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BTO Option Table

Function	Mini PCI-E SLOT				CAMERA & MIC		BLUE TOOTH		Clock gen	
description										
explain	Wi-Fi	WiMax	3GGPS	3G	CAMERA	MIC	BLUE TOOTH		Tpye	
BTO	WLAN@	WIMAX@	3GGPS@	3G@	CAM@	MIC@	BT@		low@	normal@

Function			
description			
explain			
BTO			

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
EMC1402	1001 010X b

ICH7M SM Bus address

Device	Address
Clock Generator (SLG8SP556VTR)	1101 001Xb
DDR DIMMA	1010 000Xb
WWAN/WLAN	

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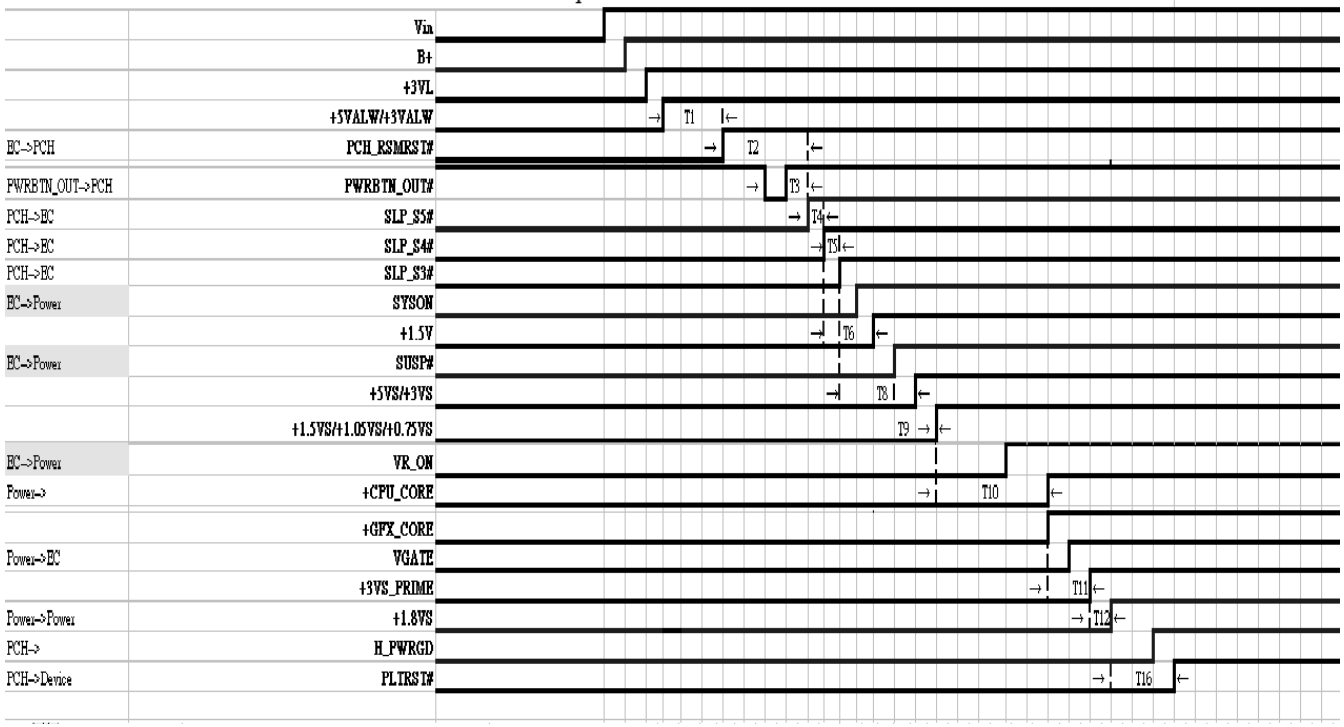
PBU00 Power ON sequence

2010/7/2



Power-on Sequence

Time	Description	Expected
T1	+5V/3VALW to PCH_RSMRST# inactive	>0ms
T2	PCH_RSMRST# inactive to SLP_S5# inactive	<110ms
T3	PWRBTN_OUT# inactive to SLP_S5# inactive	"
T4	SLP_S5# inactive to SLP_S4# inactive	28.992us ~ 64.088us
T5	SLP_S4# inactive to SLP_S3# inactive	28.992us ~ 64.088us
T6	SLP_S4# inactive to +1.5V active	"
T8	SLP_S3# inactive to +5VS inactive	"
T9	+1.5VS active to +1.05VS active	"
T10	+1.05VS active to +CPU_CORE	"
T11	+CPU_COREactive to +3.3V_PRIME	"
T12	+3.3V_PRIME active to +1.8VS	3.3-1.8<700mV
T16	H_PWRGD inactive to PLTRST# inactive	34<RTCCLK<41

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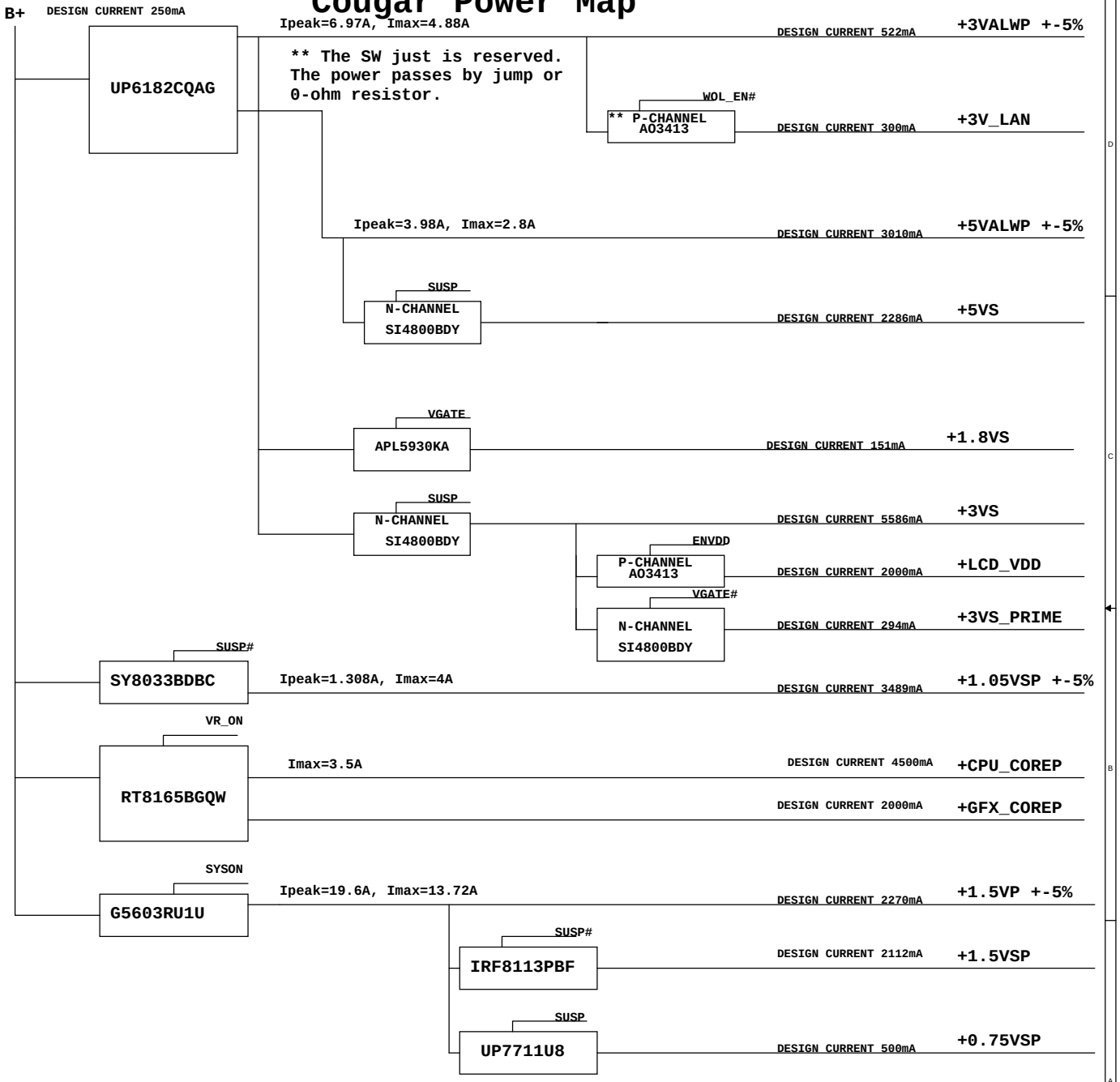
Cougar Power Map



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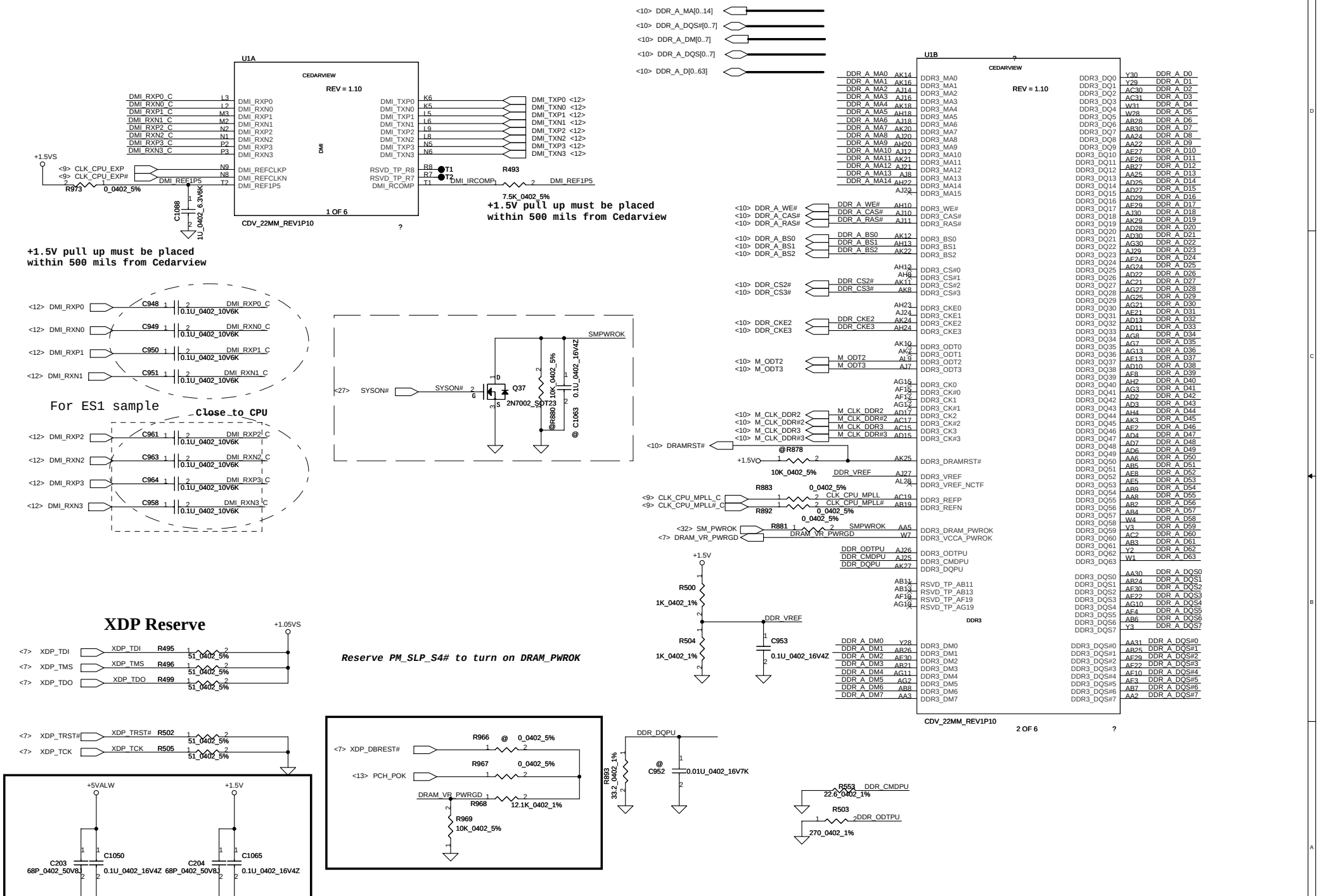

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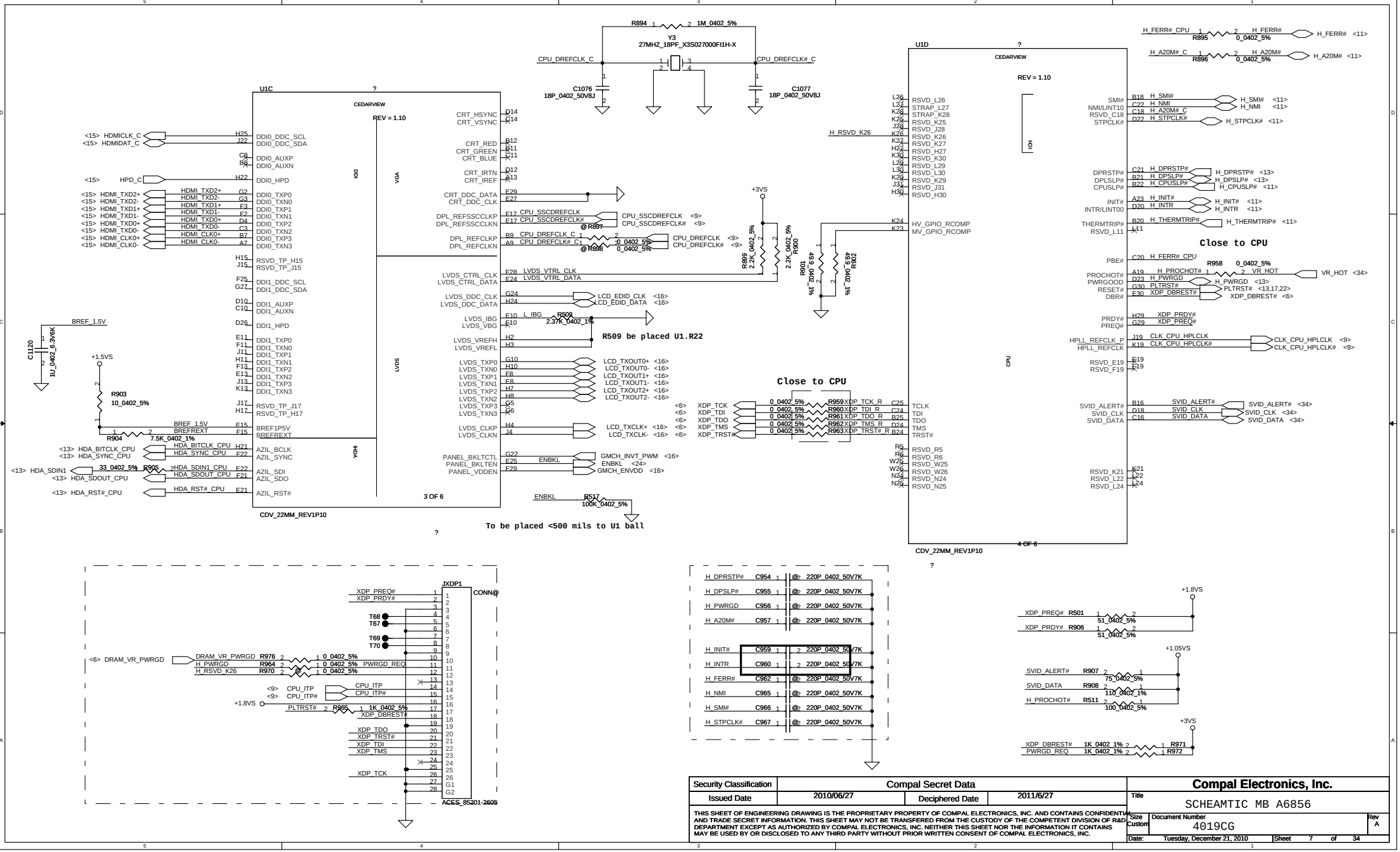

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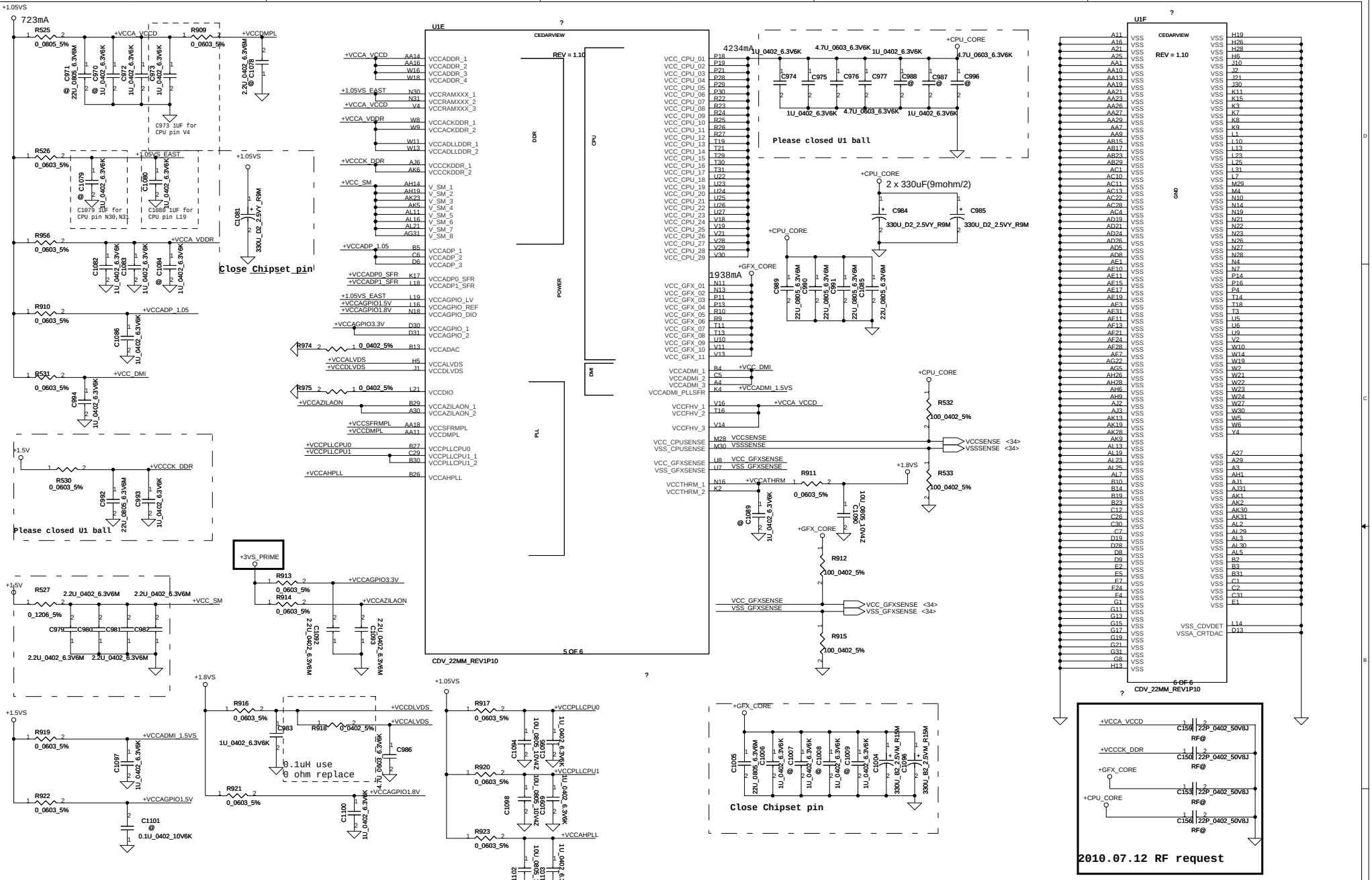

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FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					

	Normal Power	Low Power
R477	@	Stuff
R478	Stuff	@
R479	Stuff	@
R480	@	Stuff
R483	@	Stuff

2010.03.23 Change R81 from bead to 0 ohm

+3VS R81 0_0603_5% +3VM_CK505 250 mA C126 10U_0805_10V4Z C127 0.1U_0402_16V4Z C128 0.1U_0402_16V4Z C129 0.1U_0402_16V4Z C133 47P_0402_50V8J

+1.05VS R82 FBMH1608HM601-T_0603 +1.05VM_CK505 80 mA C134 10U_0805_10V4Z C135 0.1U_0402_16V4Z C136 0.1U_0402_16V4Z C137 0.1U_0402_16V4Z C138 0.1U_0402_16V4Z C139 0.1U_0402_16V4Z C141 47P_0402_50V8J

7/13 For RF request

2010.03.23 Change R477 from bead to 0 ohm

8/27 Delete C93, C94, C95, C102 for low power CLK GEN

+1.5VS R477 0_0603_5% LOW@ +1.5VM_CK505 C942 10U_0805_10V4Z

7/13 For RF request

7/13 For RF request

CPU_SSCDREFCLK C940 @ 33P_0402_50V8K CPU_SSCDREFCLK# C941 @ 33P_0402_50V8K

7/13 Add 33pFfor RF request

7/21 Reserve 33pFfor RF request

+3VS R83 2.2K_0402_5% R84 2.2K_0402_5%

Q1A 2N7002DW-T/R7_SOT363-6

<13> PCH_SMBDATA — CLK_SMBDATA

+3VS

<13> PCH_SMBCLK — CLK_SMBCLK

Q1B 2N7002DW-T/R7_SOT363-6

SA00003H610 (ICS :CS9LVRS387AKLFT MLF)

Low power CLK Gen.

7/21 Delete C296, C297 for RF request

7/13 Add 22pF to gnd and close to U3 for RF request

7/21 Reserve 22pF to gnd and close to U3 for RF request

NORMAL@ U4 RTM875N-397-GR

LOW@U4

+3VM_CK505 NORMAL@ R478 0_0603_5% +3VM_1.5VM_R LOW@R483 0_0603_5% C943 0.1U_0402_16V4Z C944 0.1U_0402_16V4Z C945 0.1U_0402_16V4Z

+1.05VM_CK505 NORMAL@ R479 0_0603_5%

+1.5VM_CK505 LOW@R480 0_0603_5% +1.05VM_1.5VM_R C946 0.1U_0402_16V4Z C947 @ 47P_0402_50V8J

7/13 For RF request

+1.05VS R481 470_0402_5% R482 2.2K_0402_5% FSA @R484 1K_0402_5%

8/24 Change net name to FSB for U3.2

7/13 Add 33pF to GND for RF request

7/21 Reserve 33pF to GND for RF request

8/27 C303, C324, C325, C326, C327 to GND for RF request

<23> CLK_48M_CR — 10_0402_5% R92

<12> CLK_PCH_48M — 10_0402_5% R91

<13> CLK_PCH_14M — 33_0402_5% R93

C143 22P_0402_50V8J C868 22P_0402_50V8J

+3VS R65 10K_0402_5% H_STP_CPU#_R

<13,24,27,33,34> VGATE

7/22 Add R241 pull up to +3VS for RF Intel request

+1.05VS R485@ 470_0402_5% R486 1K_0402_5% FSB R488 0_0402_5%

<13> H_STP_CPU# — R432 0_0402_5% H_STP_CPU#_R

<13> H_STP_PCI# — R427 0_0402_5% H_STP_PCI#_R

+3VS R608 10K_0402_5% H_STP_PCI#_R

<17> CLK_PCI_DDR — 33_0402_5% R103 CLK_PCI_DDR_R

C144 22P_0402_50V8J C145 22P_0402_50V8J

<24> CLK_PCI_LPC — 33_0402_5% R107 PCI4_SEL

<11> CLK_PCI_PCH — 33_0402_5% R108 ITP_EN

C146 22P_0402_50V8J

7/13 Add 33pF to GND for RF request

+1.05VS R489 470_0402_5% R490 10K_0402_5% FSC @R491 0_0402_5%

8/14 Add R250 pull up for Intel request

For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#

For PCI4_SEL, 0 = Pin24/25 : DOT96 / DOT96#
Pin28/29 : LCDCLK / LCDCLK#
1 = Pin24/25 : SRC_0 / SRC_0#
Pin28/29 : 27M/27M_SS

For PCI2_TME:0=Overclocking of CPU and SRC allowed
(ICS only) 1=Overclocking of CPU and SRC NOT allowed

+3VS R119 10K_0402_5% ITP_EN R113@ 10K_0402_5%
+3VS R118 10K_0402_5% PCI4_SEL R114@ 10K_0402_5%
+3VS R112 10K_0402_5% PCI2_TME @ R115 10K_0402_5%

7/22 Add R242 to R253 for Intel request

C147 22P_0402_50V8J CLK_XTAL_IN Y1 14.31818MHZ 20PF 7A14300003 C148 22P_0402_50V8J CLK_XTAL_OUT

Routing the trace at least 10mil

2010.03.09 Change Y1 to 5 x3.2 size

ICS9LVRS387AKLFT MLF

Pin	Signal	Net
55	VDD_SRC	
6	VDD_REF	
12	VDD_PCI	
72	VDD_CPU	
19	VDD_48	
27	VDD_PLL3	
66	VDD_CPU_IO	
31	VDD_PLL3_IO	
62	VDD_SRC_IO	
52	VDD_SRC_IO	
23	VDD_IO	
38	VDD_SRC_IO	
20	USB_0/FS_A	FSA
2	FS_B/TEST_MODE	FSB
7	REF_0/FS_C/TEST_	FSC
8	REF_1	
1	CKPWRGD/PD#	VGATE
11	NC	
53	CPU_STOP#	
54	PCI_STOP#	
5	XTAL_IN	CLK_XTAL_IN
4	XTAL_OUT	CLK_XTAL_OUT
13	PCI_1	CLK_PCI_DDR_R
14	PCI_2	PCI2_TME
15	PCI_3	
16	PCI_4/SEL_LCDCL	PCI4_SEL
17	PCIF_5/ITP_EN	ITP_EN
18	VSS_PCI	
3	VSS_REF	
22	VSS_48	
26	VSS_IO	
69	VSS_CPU	
30	VSS_PLL3	
34	VSS_SRC	
59	VSS_SRC	
42	VSS_SRC	
73	VSS	
9	SDA	CLK_SMBDATA — CLK_SMBDATA <10,17>
10	SCL	CLK_SMBCLK — CLK_SMBCLK <10,17>
71	CPU_0	CLK_CPU_HPLCLK — CLK_CPU_HPLCLK <7>
70	CPU_0#	CLK_CPU_HPLCLK# — CLK_CPU_HPLCLK# <7>
68	CPU_1	CLK_CPU_MPLL_C — CLK_CPU_MPLL_C <6>
67	CPU_1#	CLK_CPU_MPLL#_C — CLK_CPU_MPLL#_C <6>
24	SRC_0/DOT_96	CPU_SSCDREFCLK — CPU_SSCDREFCLK <7>
25	SRC_0#/DOT_96#	CPU_SSCDREFCLK# — CPU_SSCDREFCLK# <7>
28	LCDCLK/27M	CPU_DREFCLK — CPU_DREFCLK <7>
29	LCDCLK#/27M_SS	CPU_DREFCLK# — CPU_DREFCLK# <7>
32	SRC_2	CLK_CPU_EXP — CLK_CPU_EXP <6>
33	SRC_2#	CLK_CPU_EXP# — CLK_CPU_EXP# <6>
35	SRC_3	
36	SRC_3#	
39	SRC_4	CLK_PCIE_SATA — CLK_PCIE_SATA <11>
40	SRC_4#	CLK_PCIE_SATA# — CLK_PCIE_SATA# <11>
57	SRC_6	CLK_PCIE_WLAN — CLK_PCIE_WLAN <17>
56	SRC_6#	CLK_PCIE_WLAN# — CLK_PCIE_WLAN# <17>
61	SRC_7	
60	SRC_7#	
64	SRC_8/CPU_ITP	CPU_ITP — CPU_ITP <7>
63	SRC_8#/CPU_ITP#	CPU_ITP# — CPU_ITP# <7>
44	SRC_9	CLK_PCIE_LAN — CLK_PCIE_LAN <22>
45	SRC_9#	CLK_PCIE_LAN# — CLK_PCIE_LAN# <22>
50	SRC_10	CLK_PCIE_PCH — CLK_PCIE_PCH <12>
51	SRC_10#	CLK_PCIE_PCH# — CLK_PCIE_PCH# <12>
48	SRC_11	CLK_PCIE_WWAN — CLK_PCIE_WWAN <17>
47	SRC_11#	CLK_PCIE_WWAN# — CLK_PCIE_WWAN# <17>
37	CLKREQ_3#	
41	CLKREQ_4#	
58	CLKREQ_6#	WLAN_CLKREQ# — WLAN_CLKREQ# <17>
65	CLKREQ_7#	
43	CLKREQ_9#	LAN_CLKREQ# — LAN_CLKREQ# <22>
49	SLKREQ_10#	
46	CLKREQ_11#	WWAN_CLKREQ# — WWAN_CLKREQ# <17>
21	USB_1/CLKREQ_A#	

7/21 Change WWAN_CLKREQ# from REQ4 to REQ11

SRC PORT LIST

PORT	DEVICE
SRC0	CPU_DREFCLK
SRC2	CPU_EXP
SRC3	
SRC4	PCIE_SATA
SRC6	PCIE_WLAN
SRC7	
SRC8	
SRC9	PCIE_LAN
SRC10	PCIE_PCH
SRC11	PCIE_WWAN

+3VS

WLAN_CLKREQ# R99 10K_0402_5%
WWAN_CLKREQ# R100 10K_0402_5%
LAN_CLKREQ# R101 10K_0402_5%

CLK_PCIE_PCH @C1067 56P_0402_50V8
CLK_PCIE_PCH# @C1066 56P_0402_50V8

2010.07.12 RF request

REQ PORT LIST

PORT	DEVICE
REQ_3#	
REQ_4#	
REQ_6#	PEIC_WLAN
REQ_7#	
REQ_9#	PCIE_LAN
REQ_10#	
REQ_11#	PEIC_WWAN
REQ_A#	

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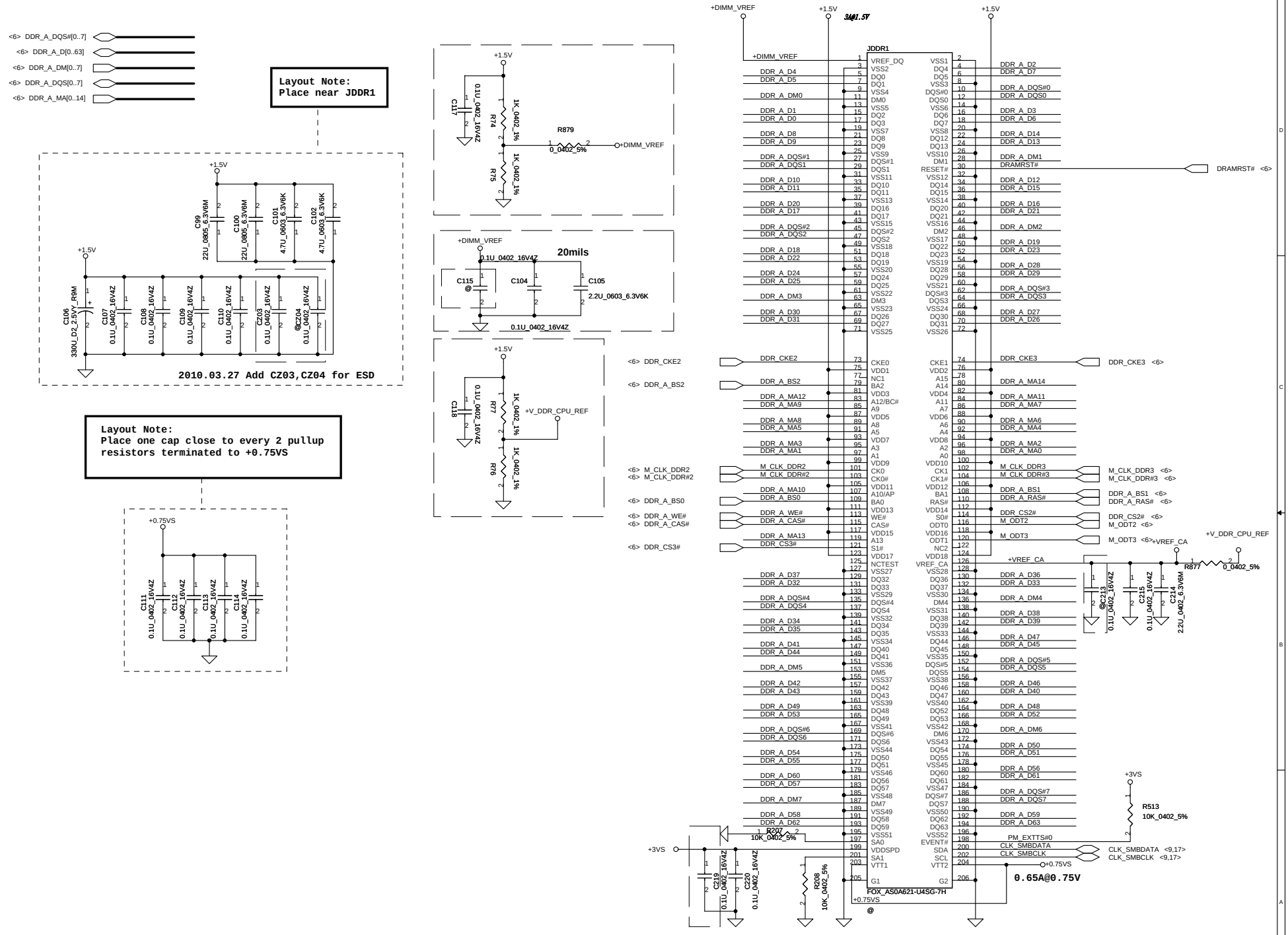

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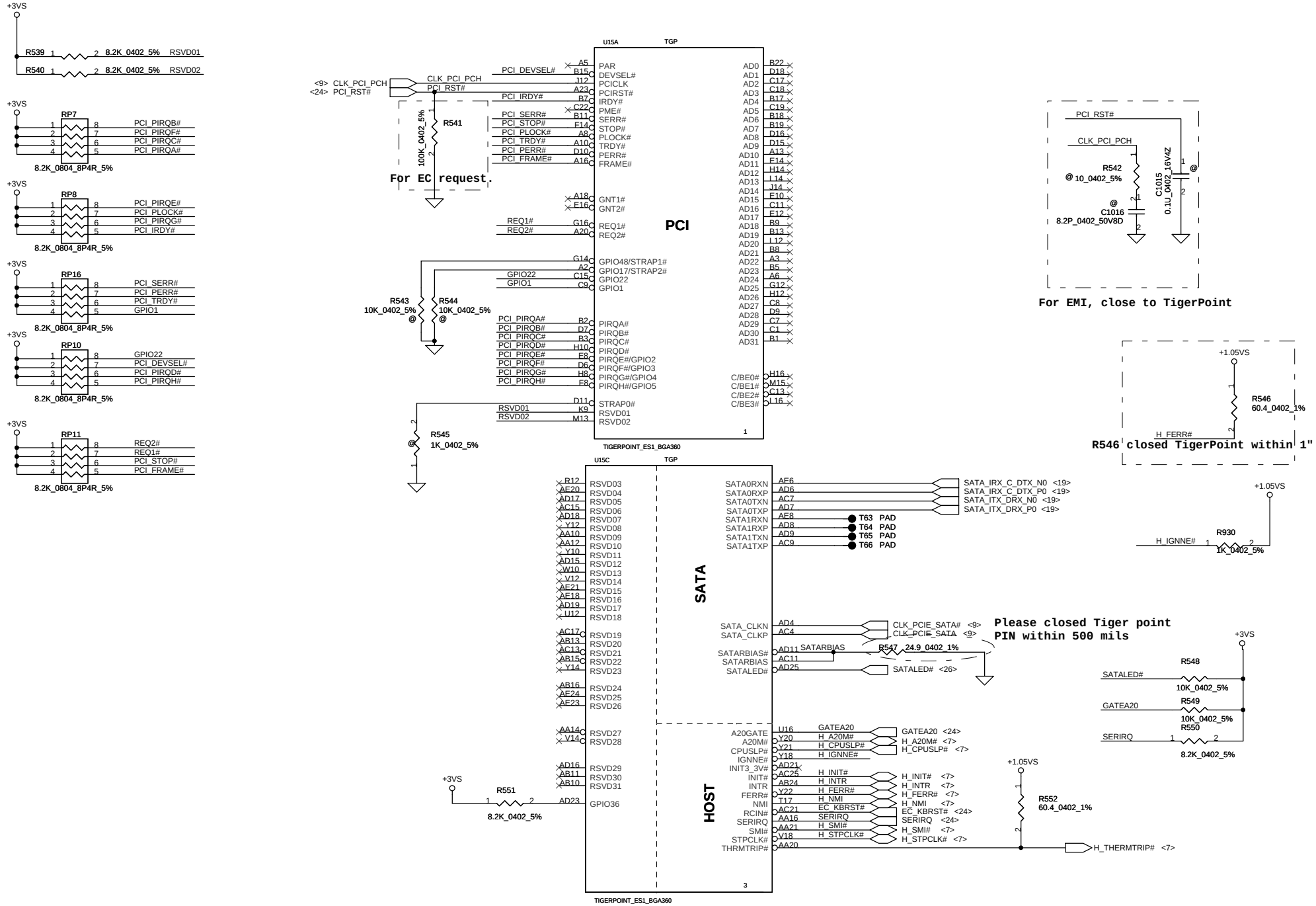

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Compal Electronics, Inc.

Title: SCHEAMTIC MB A6856

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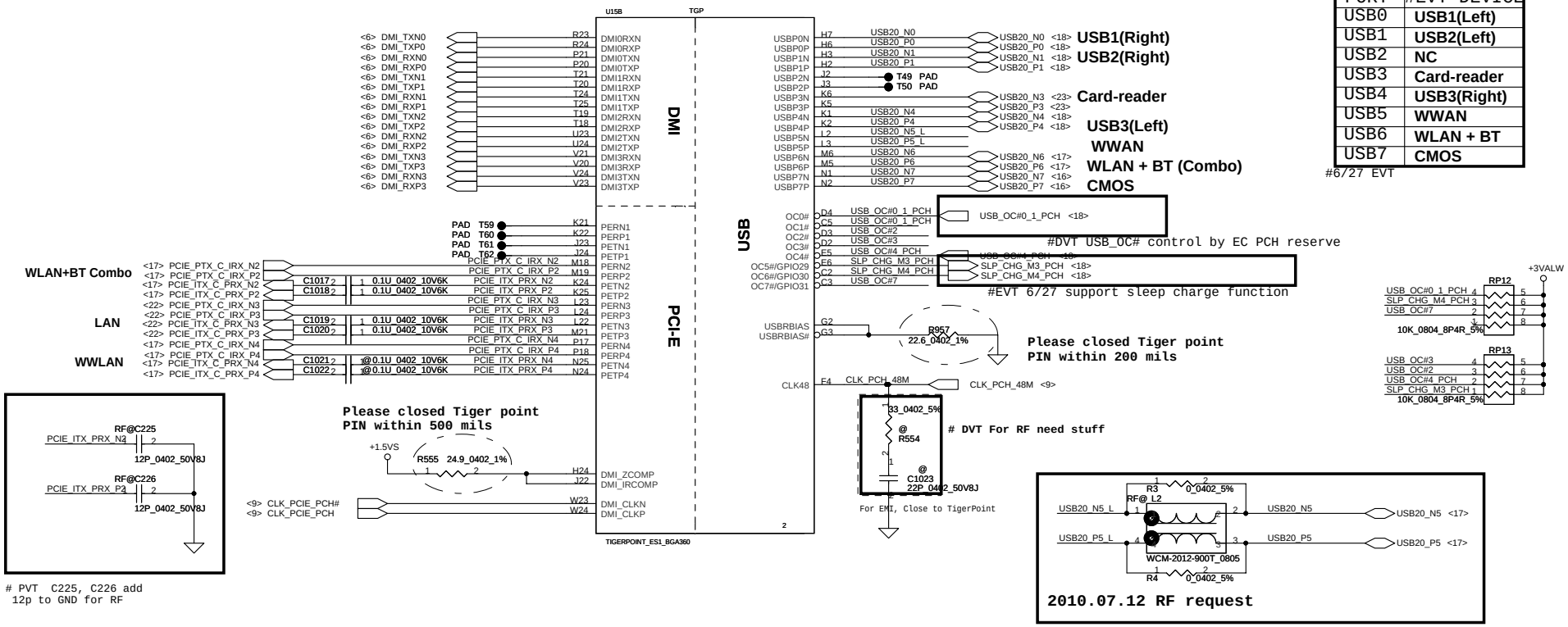
USB PORT LIST

PORT	#EVT DEVICE
USB0	USB1(Left)
USB1	USB2(Left)
USB2	NC
USB3	Card-reader
USB4	USB3(Right)
USB5	WWAN
USB6	WLAN + BT
USB7	CMOS

#6/27 EVT



PVT C225, C226 add 12p to GND for RF

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Compal Electronics, Inc.

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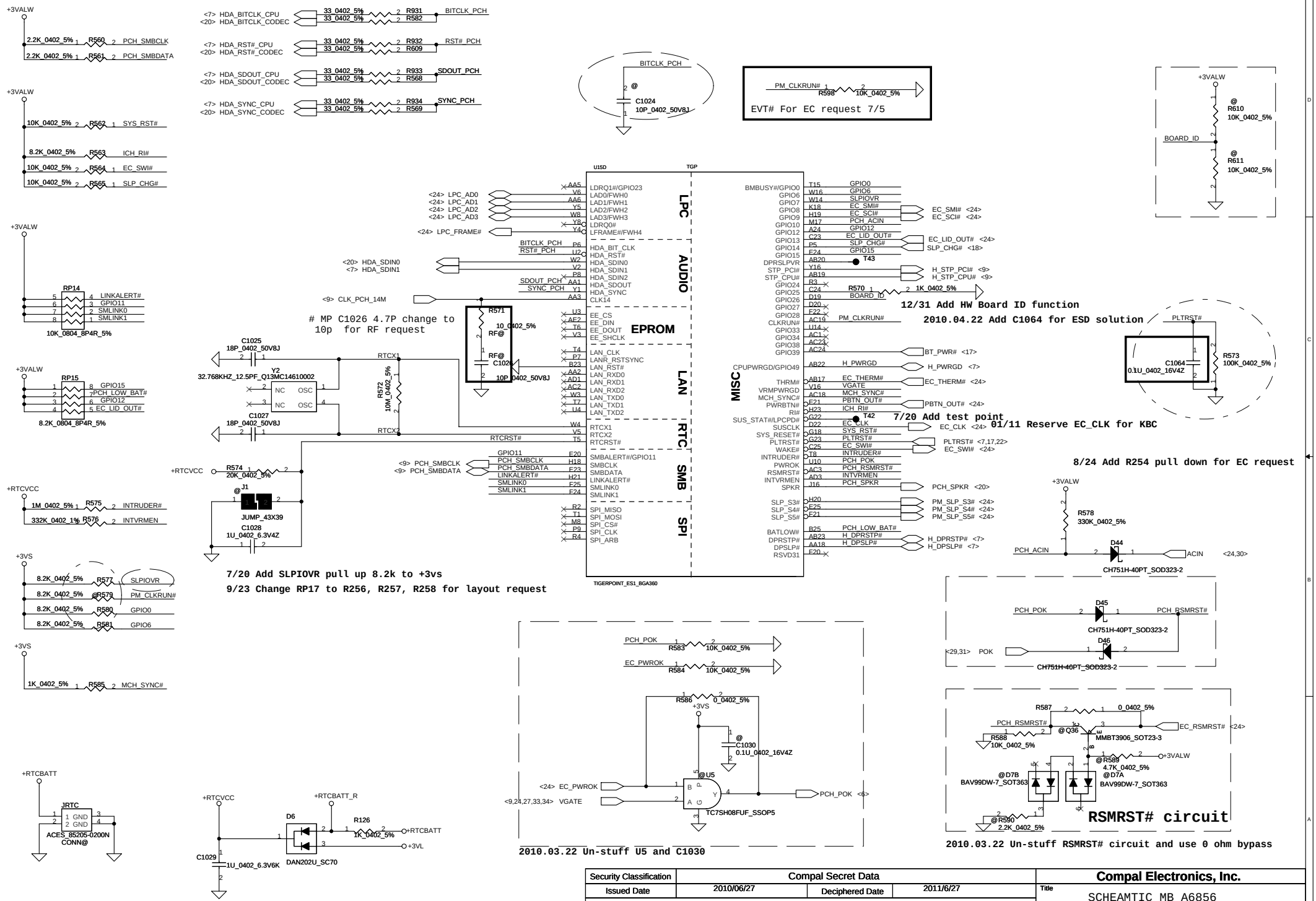

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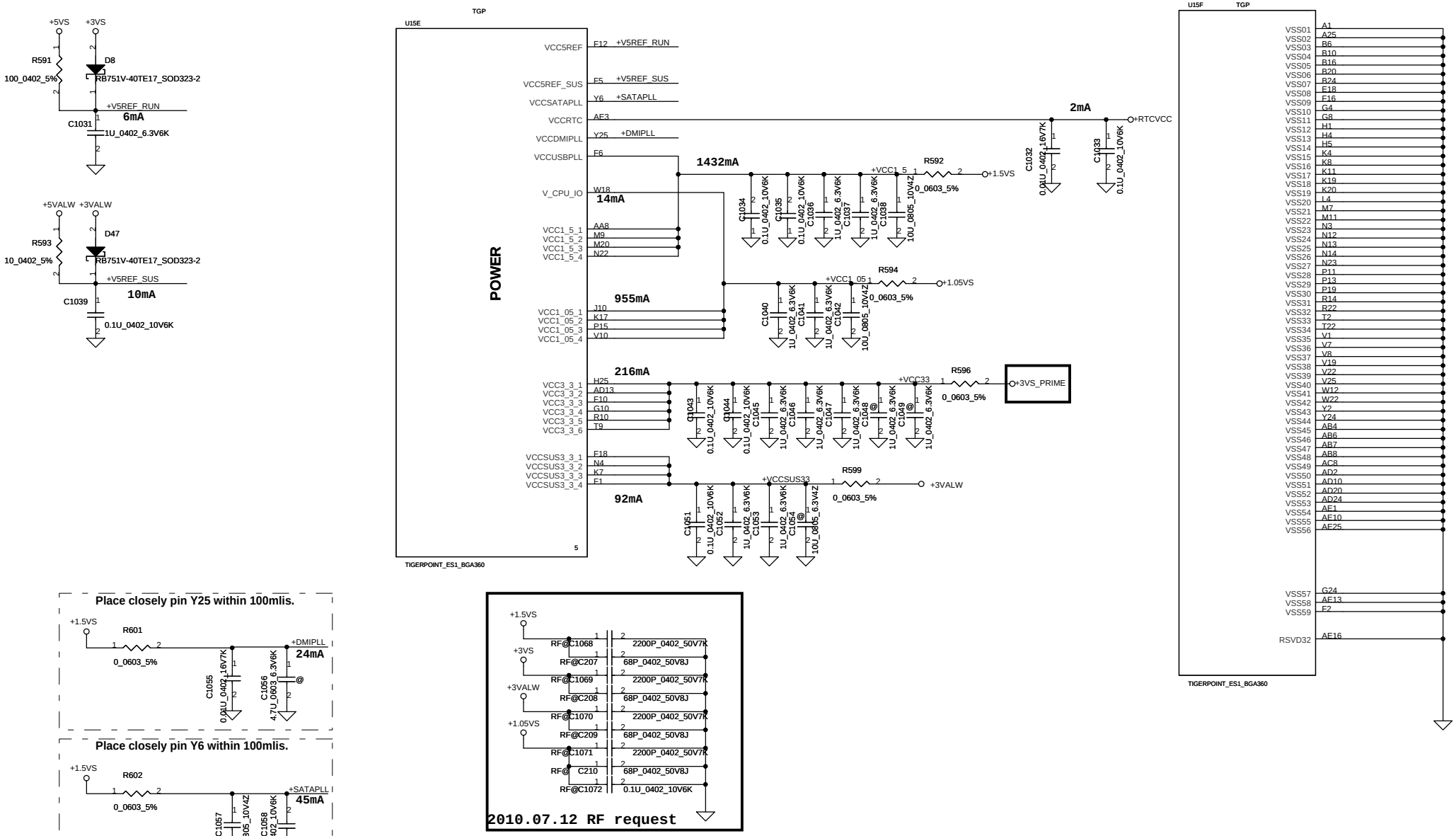

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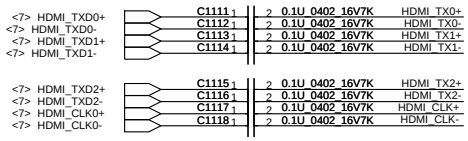
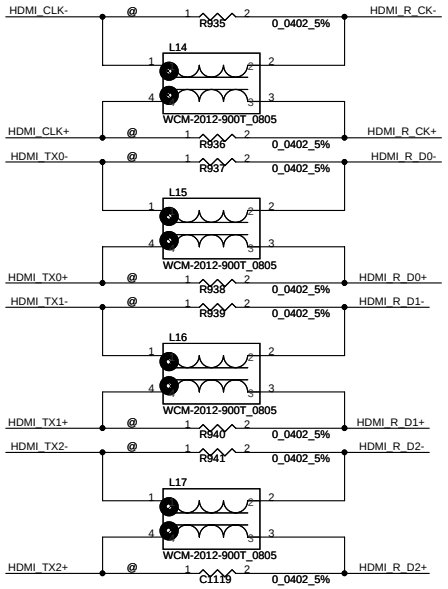
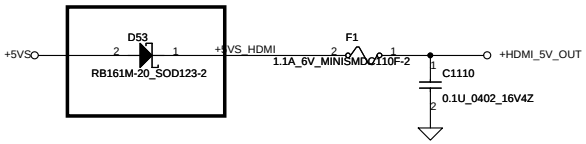
HDMI CONNECTOR

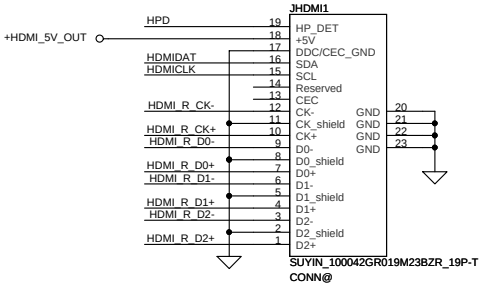


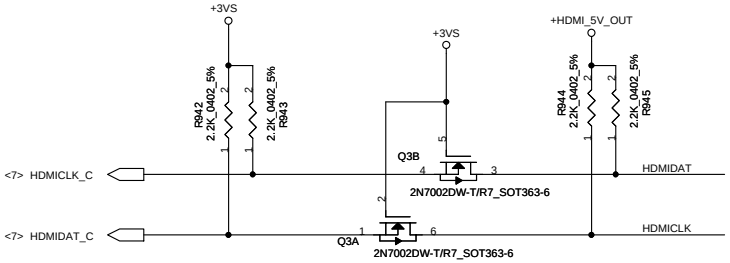


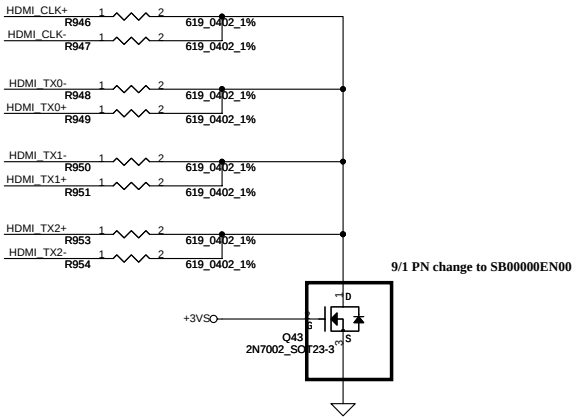
9/1 PN change to SCS00004000



< HDMI Connector >







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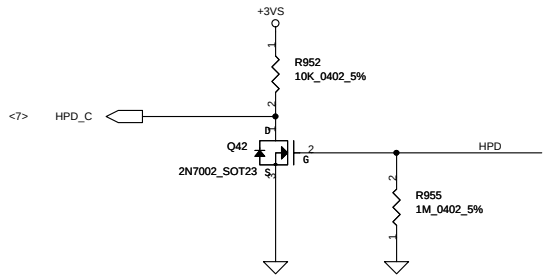

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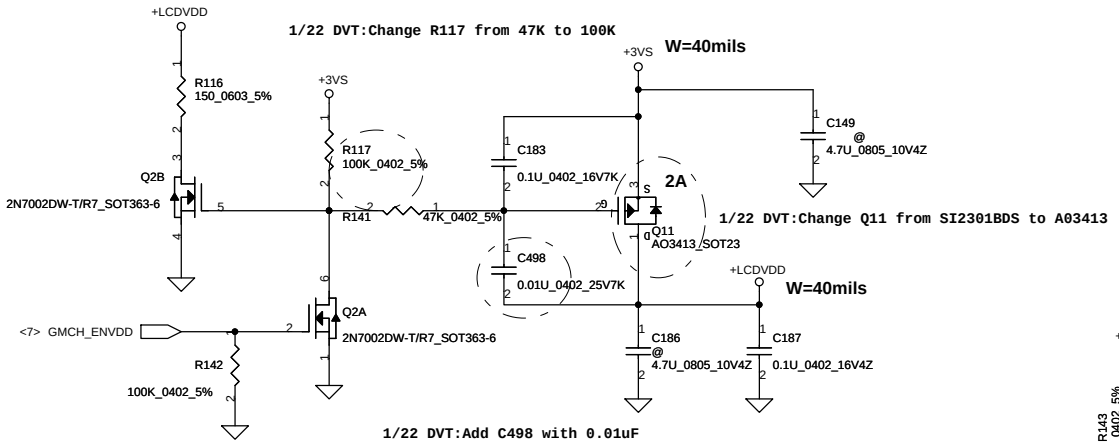
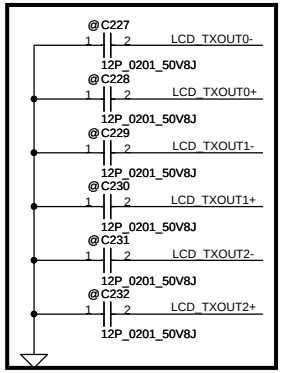
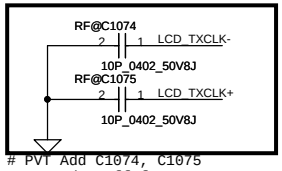
LCD POWER CIRCUIT

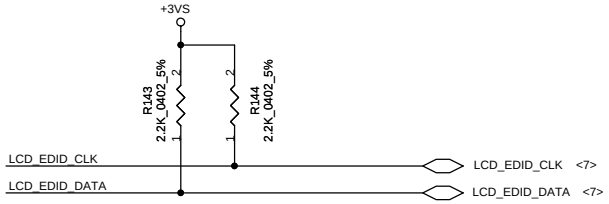


MP Add C227~C232 for RF request

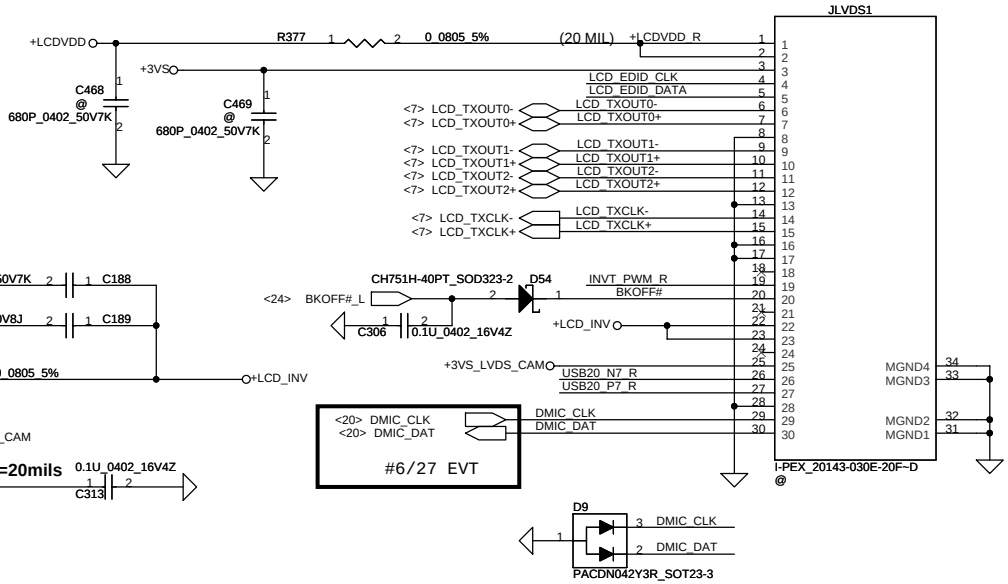


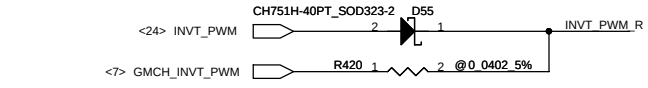


PVT Add C1074, C1075
10p and stuff for RF

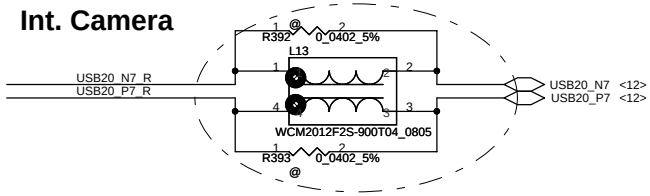


LED/PANEL BD. Conn.

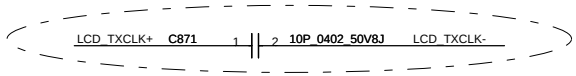




Int. Camera



For EMI request



2/25 PVT:Mount C871 with 10pF

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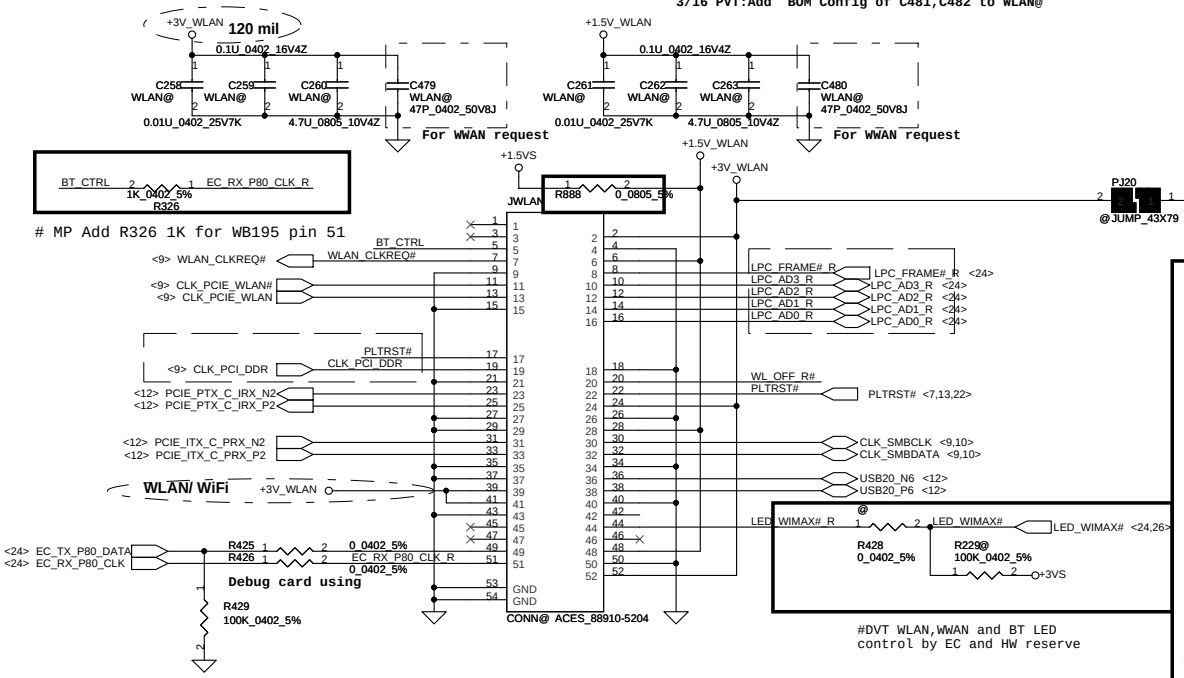
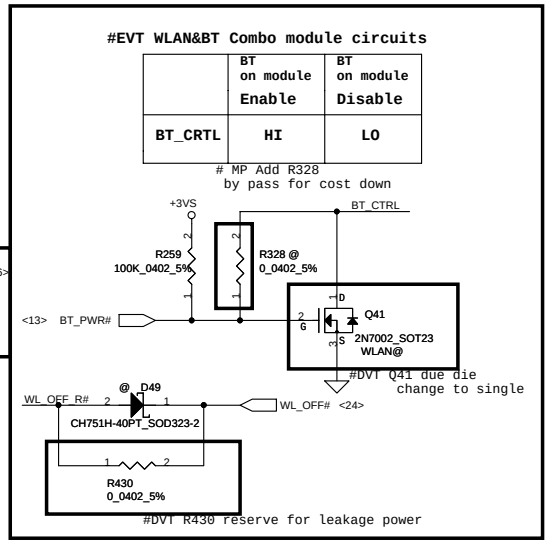
Mini-Express Card for WLAN/WiMax

2/25 PVT:Mount C479,C480 with 47pf
3/16 PVT:Add BOM Config of C481,C482 to WLAN@

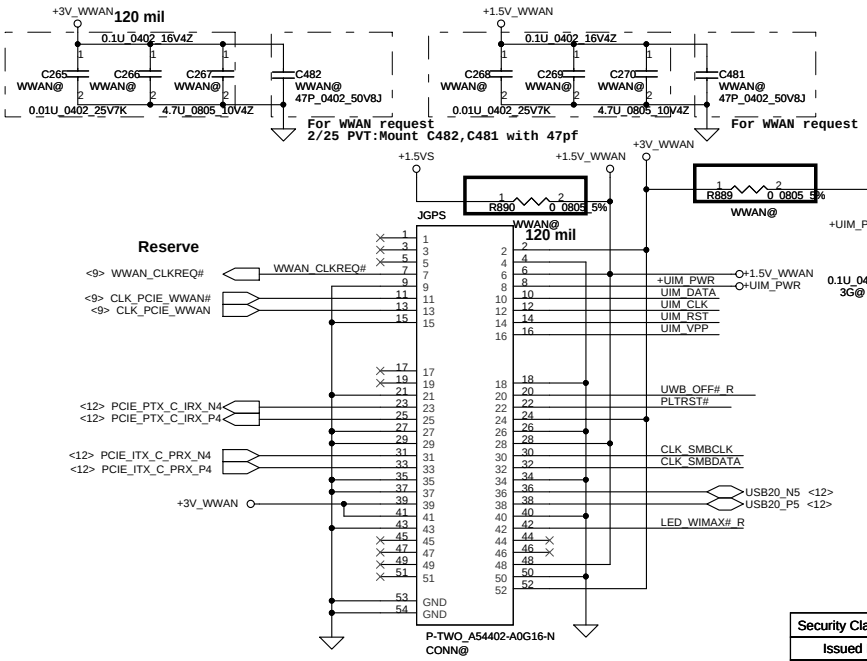


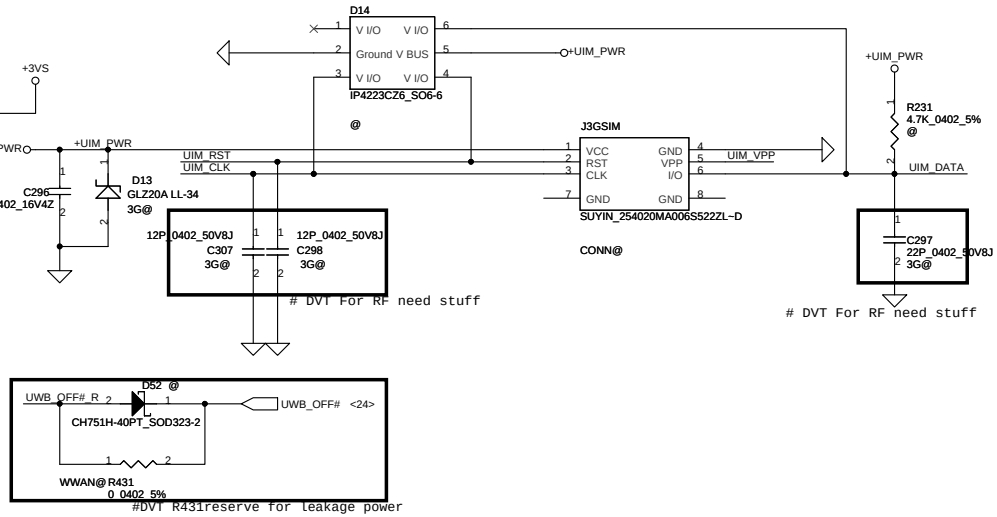


Mini-Express Card for 3G/GPS

3G current need to 2750mA

3/16 PVT:Add BOM Config of C481,C482 to 3GGPS@





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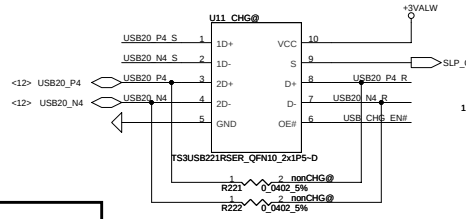
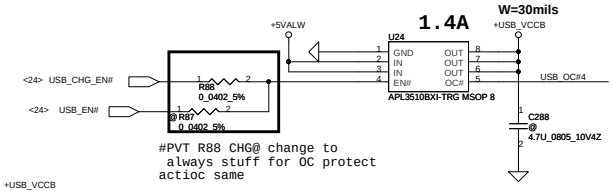
USB CONN- -Left

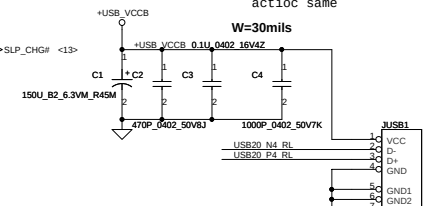
	SLP_CHG_M3	SLP_CHG_M4
Mode 3	HIGH	LOW
Mode 4	LOW	HIGH

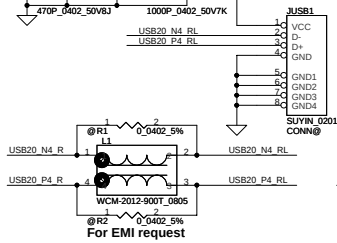
SLP_CHG	FUNCTION
LOW	D=1D
HIGH	D=2D

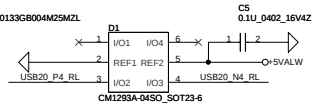


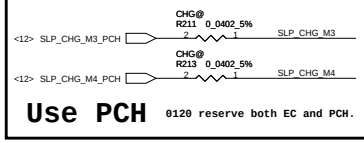


#PVT R88 CHG@ change to always stuff for OC protect actioc same

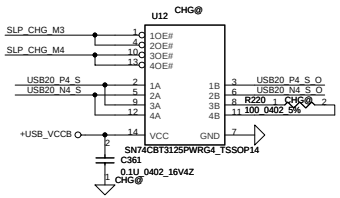


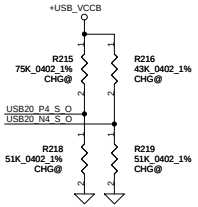


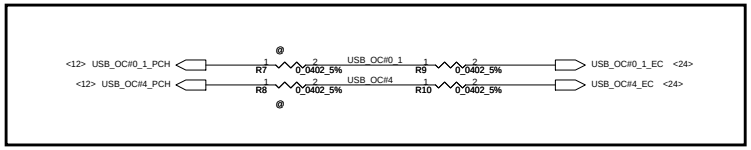




Use PCH 0120 reserve both EC and PCH.







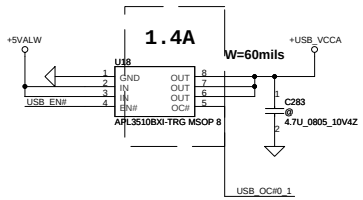
#DVT USB_OC# control by EC

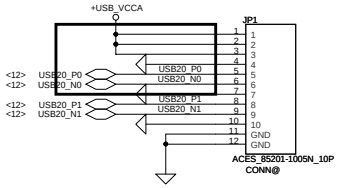
For EMI request

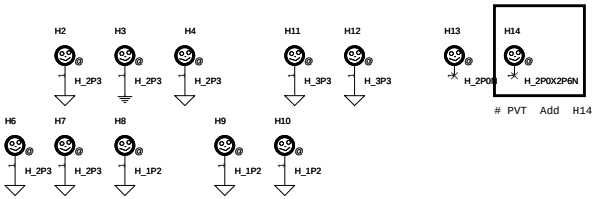
2/3 DVT: Change D38,D37 from PRTR5V0U2X_SOT143-4 to CM1293A-04SO_SOT23-6

For EMI request

USB CONN

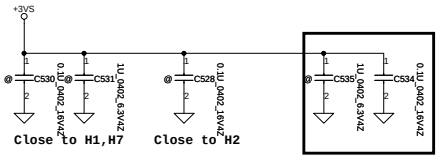






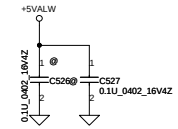
PVT Add H14 and remove H1

Add 0.1u Caps for each screw hole for ESD rule



Close to H1,H7 Close to H2

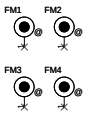
PVT Close to H4



Close to H9,H6

2010.07.20 Add for ESD solution

FIDUCIAL_C40M80



Close to H5

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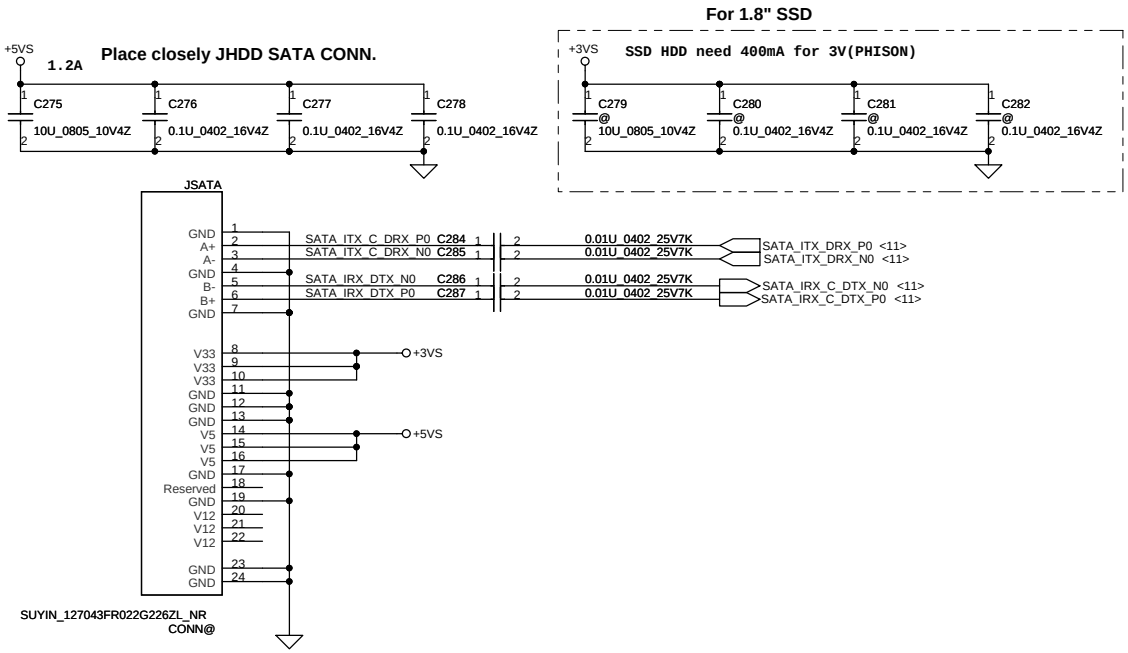
SATA Conn.



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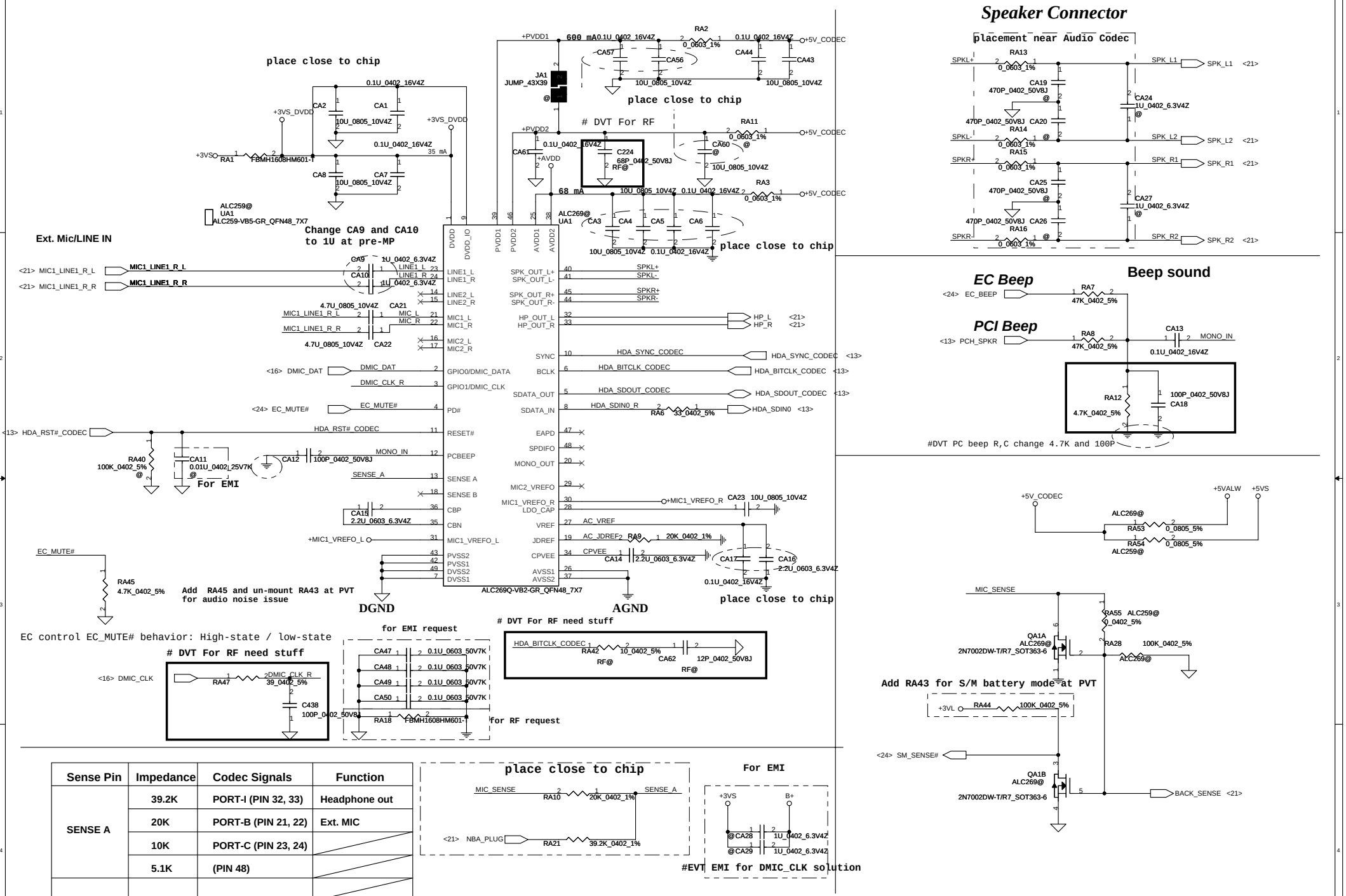

Speaker Connector

Beep sound

Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	

#EVT EMI for DMIC_CLK solution

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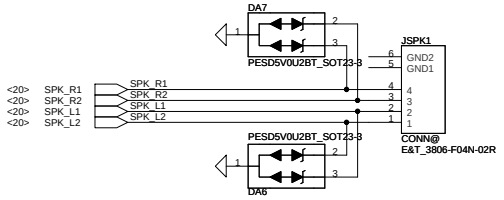
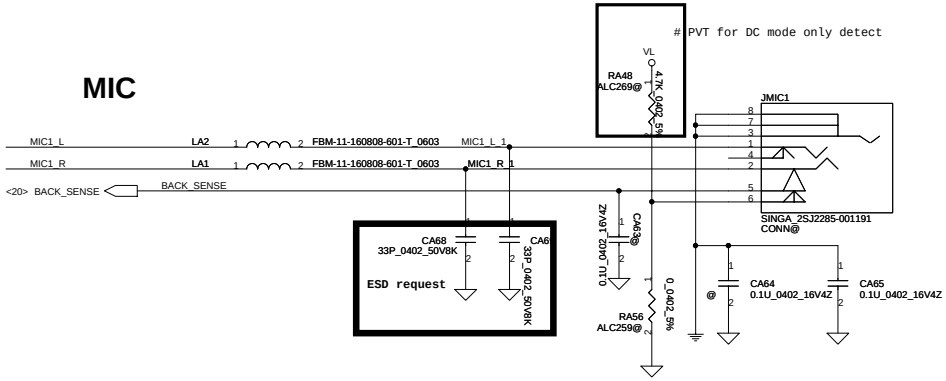
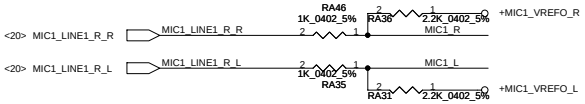
SPEAKER



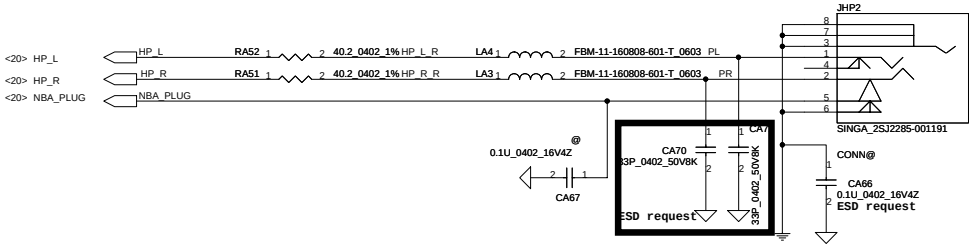
MIC



Ext.MIC/LINE IN JACK



Head phone



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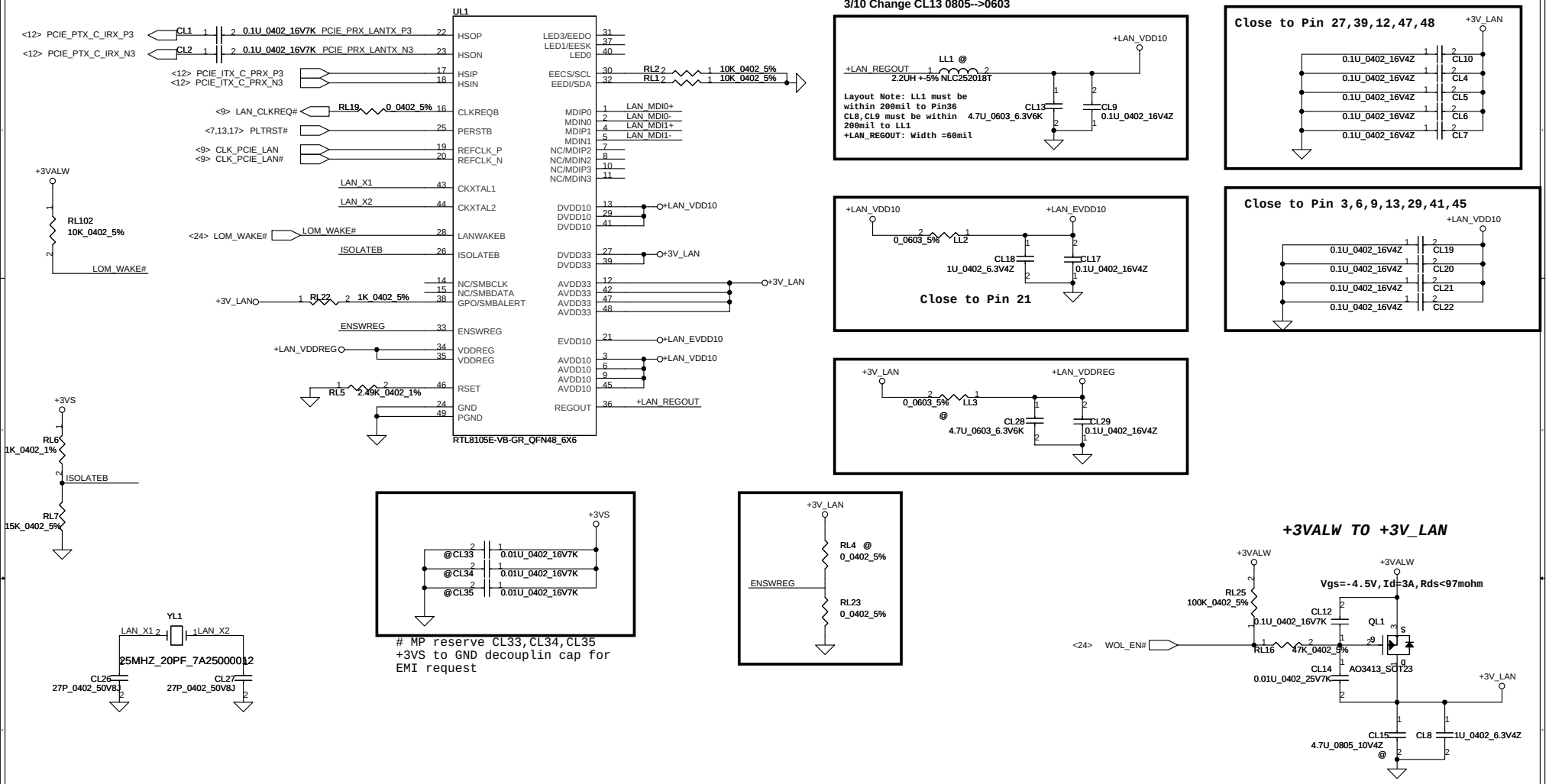

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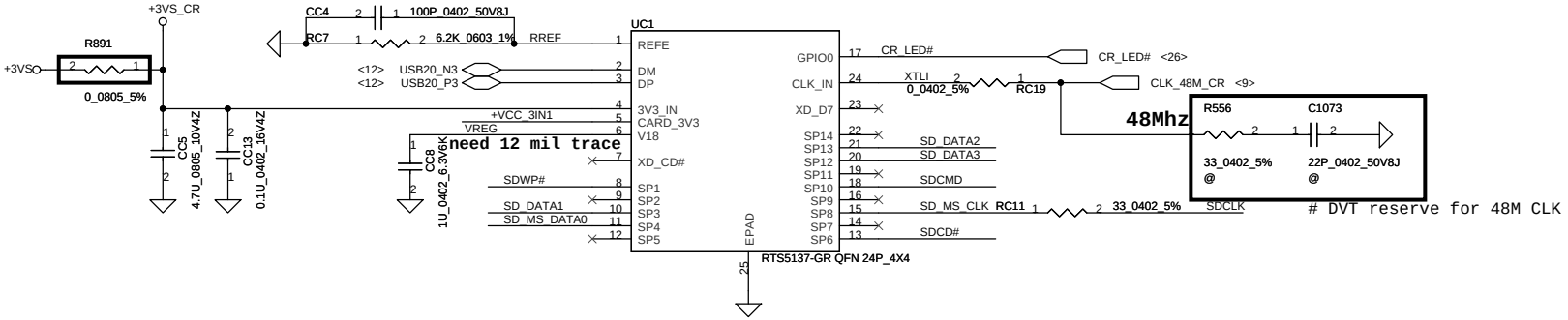
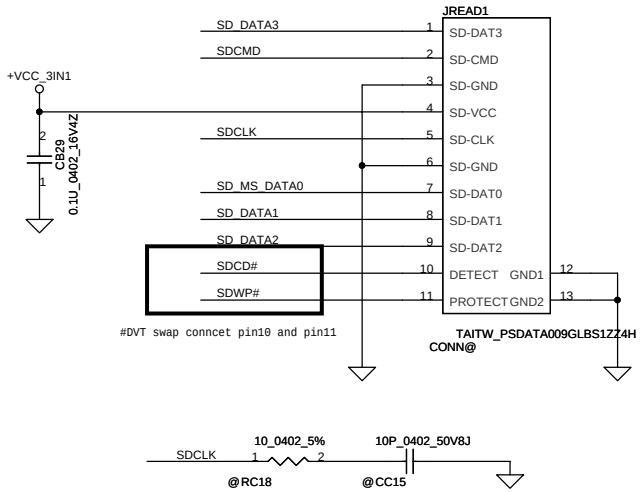
	XD_CD#		
SP1	XD_RDY	SD_WP	MS_CLK
SP2	XD_RE#		MS_INS#
SP3	XD_CE#	SD_D1	
SP4	XD_CLE	SD_D0	MS_D7
SP5	XD_ALE	SD_D7	MS_D3
SP6	XD_WE#	SD_CD#	
SP7	XD_WP	SD_D6	MS_D6
SP8	XD_D0	SD_CLK	MS_D2
SP9	XD_D1	SD_D5	MS_D0
SP10	XD_D2	SD_CMD	
SP11	XD_D3	SD_D4	MS_D4
SP12	XD_D4	SD_D3	MS_D1
SP13	XD_D5	SD_D2	MS_D5
SP14	XD_D6		MS_BS
	XD_D7		



2 in 1 Card Reader



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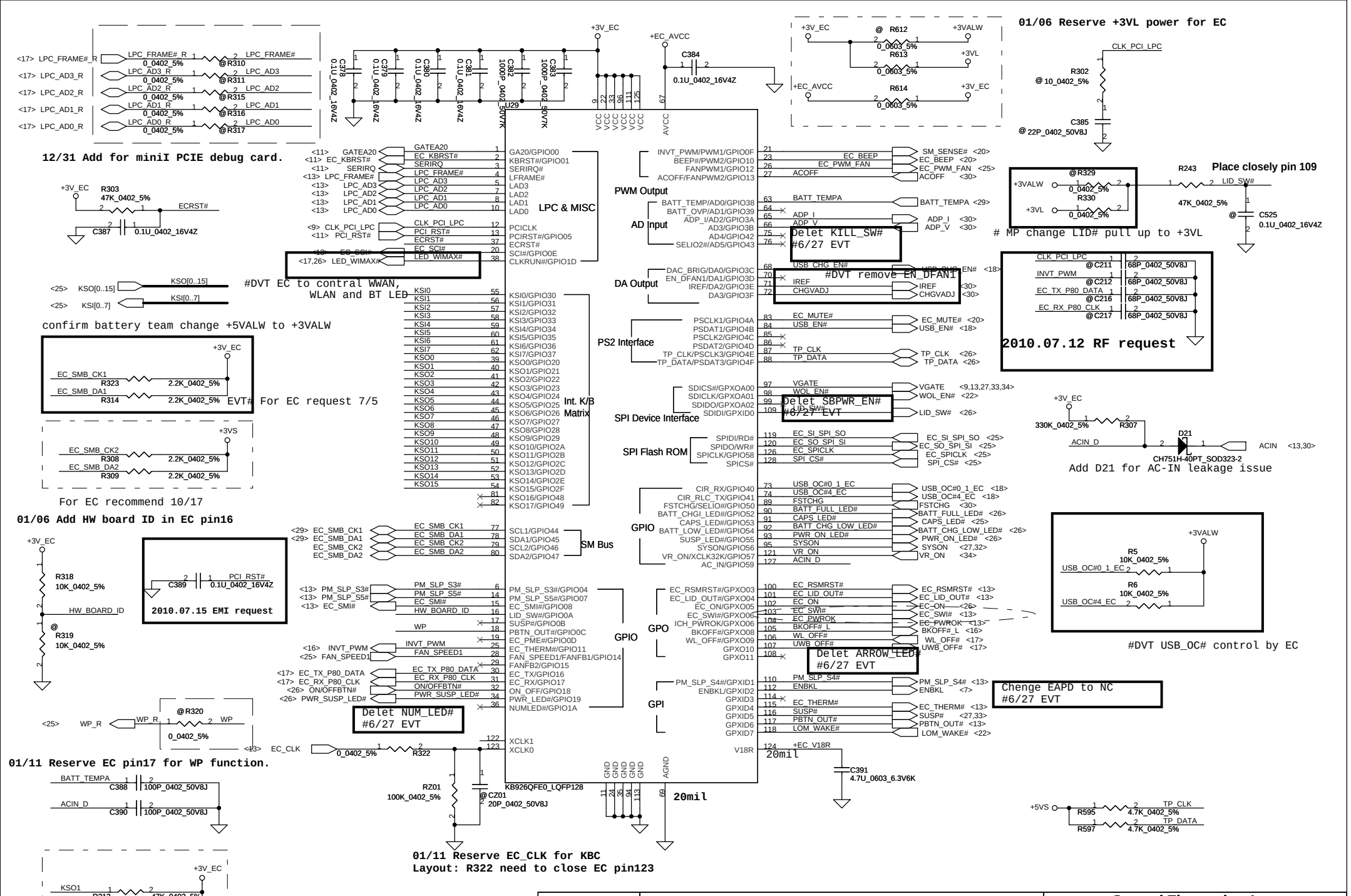

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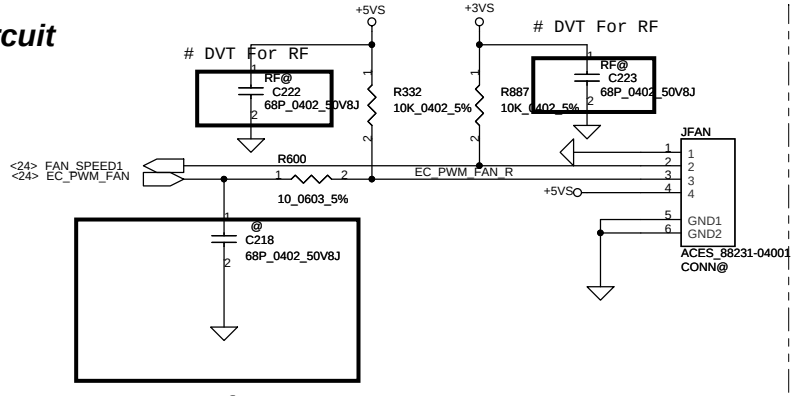
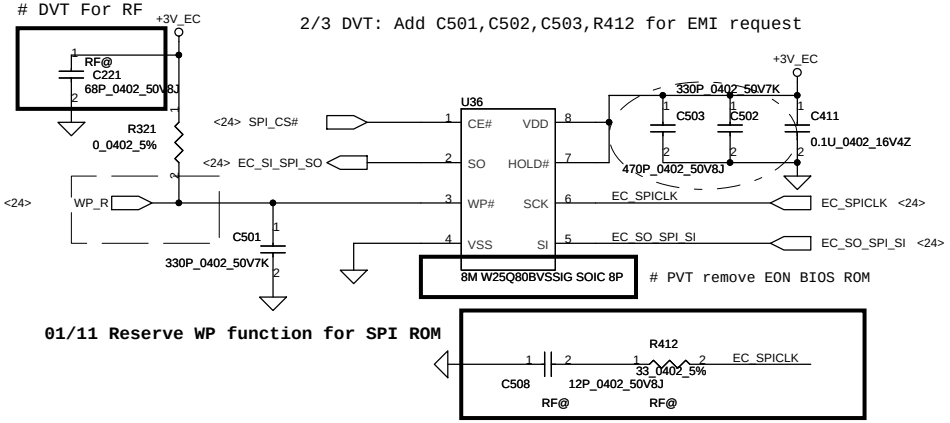
FAN Control Circuit



#DVT Reserve for EC protect

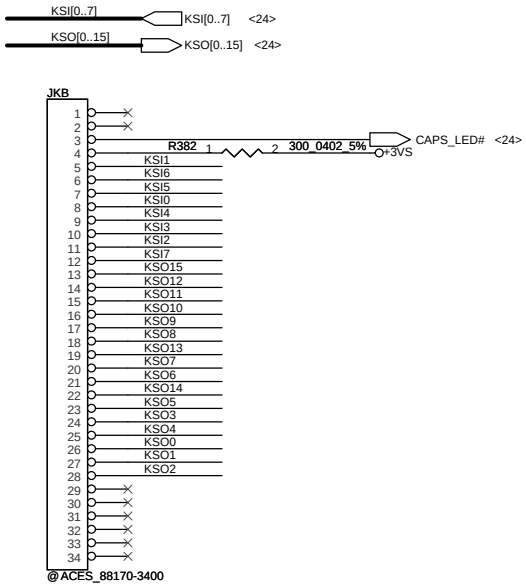
SPI Flash (8Mb*1)



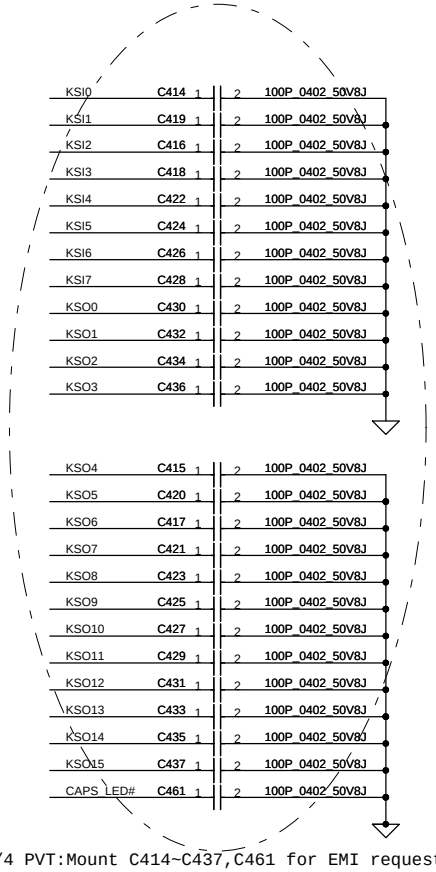
DVT For RF need stuff

LPC Debug Port

KEYBOARD CONN.



12/18 Follow KB Matrix the same to KSKAA



3/4 PVT:Mount C414~C437,C461 for EMI request

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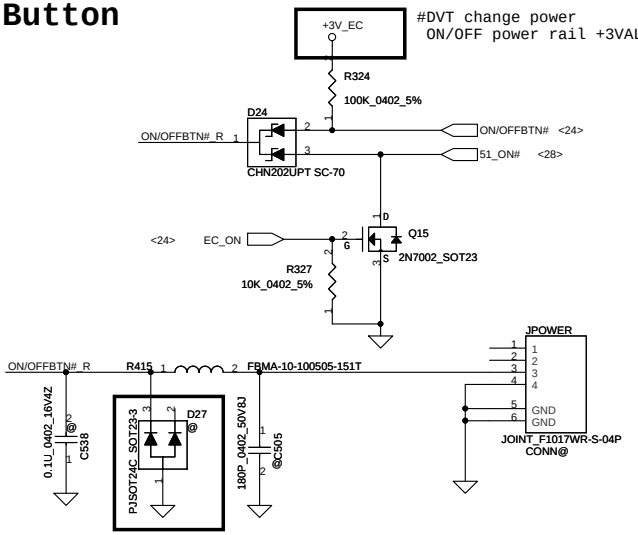
Power Button

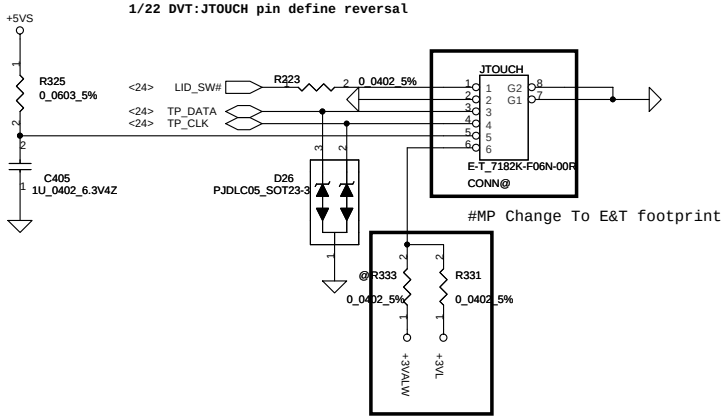


#DVT change power
ON/OFF power rail +3VALW-->+3V_EC

DVT change D27 reverse voltage
to 24V from 6V

Touch/B Connector

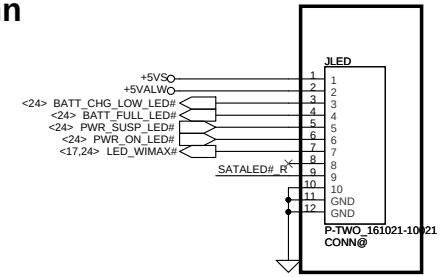
1/22 DVT:JTOUCH pin define reversal



#MP Change To E&T footprint

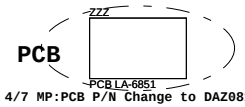
MP change LID power to +3VL

LED Conn



PVT change non ZIF for cost

ISPD



4/7 MP:PCB P/N Change to DAZ08100105

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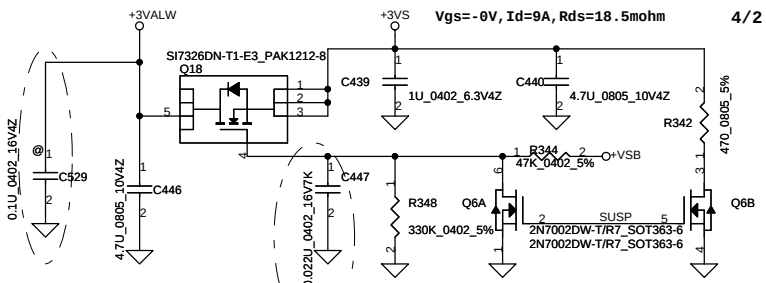
+3VALW TO +3VS



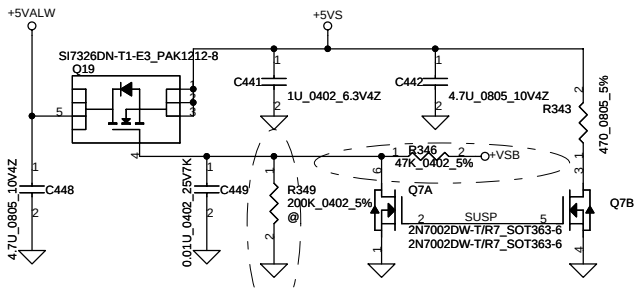
4/2 MP:For EMI ESD solution

4/2 MP:For EMI ESD solution

2/25 PVT:Change C447 with 0.022uF

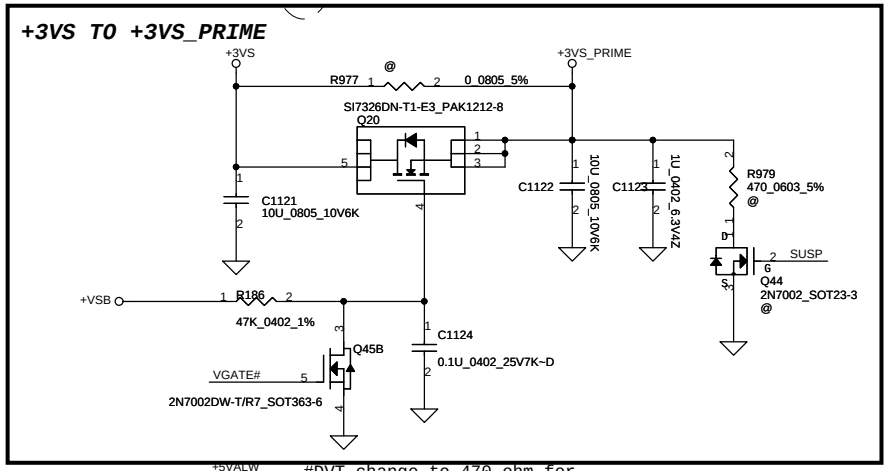
+5VALW TO +5VS

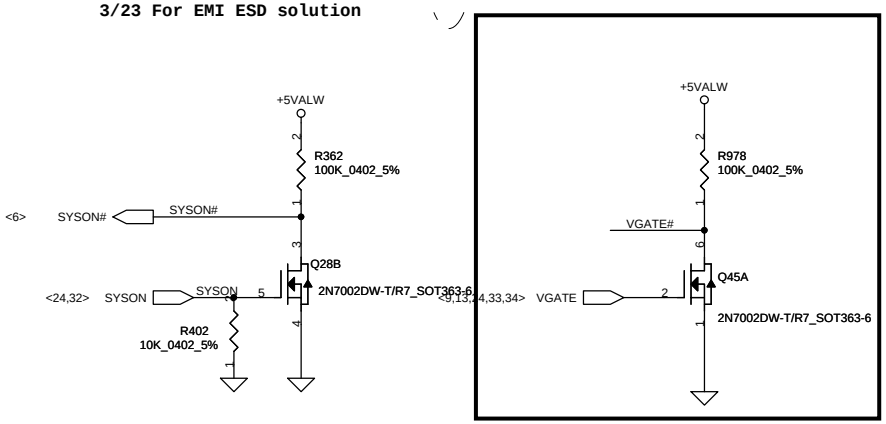
4/2 MP:For EMI ESD solution

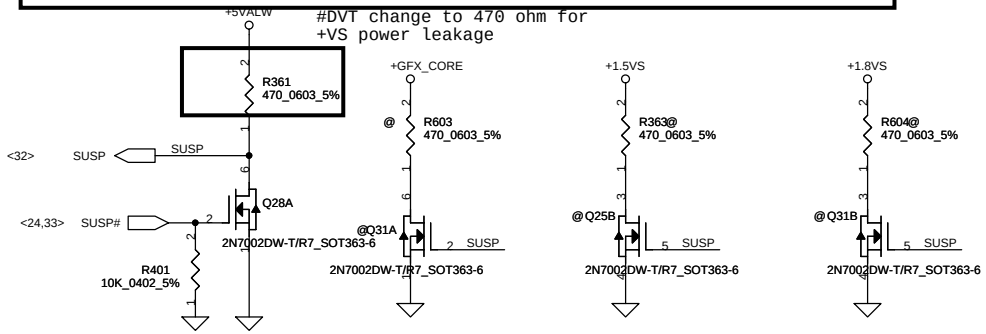


3/23 For EMI ESD solution

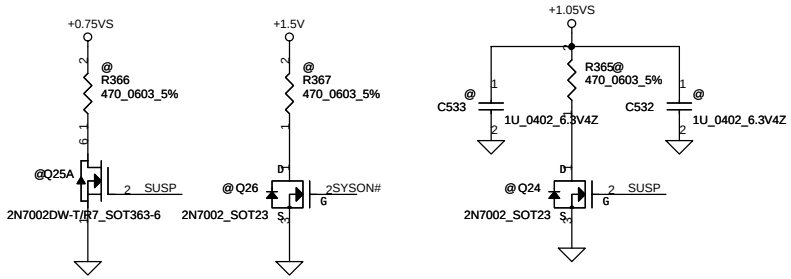
+3VS TO +3VS_PRIME



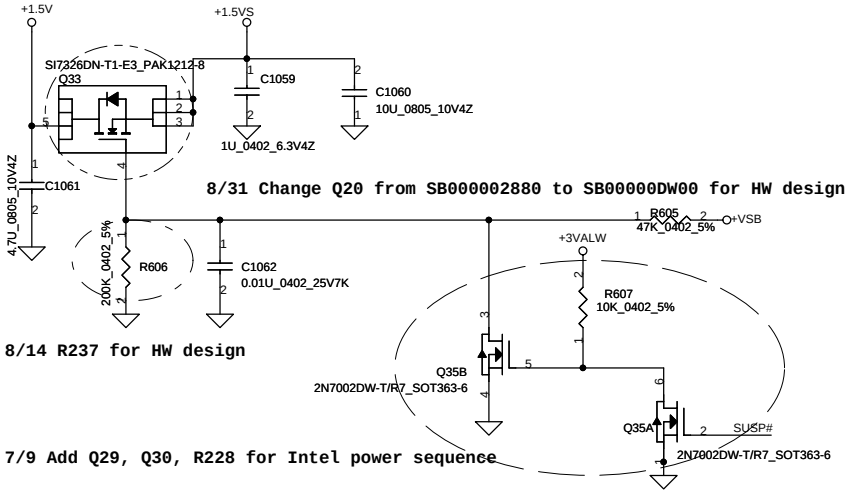




2/6 DVT: Reserve +1.5VS,+1.05VS,+0.75VS,+1.8VS discharge circuit



+1.5V TO +1.5VS



8/31 Change Q20 from SB000002880 to SB00000DW00 for HW design

8/14 R237 for HW design

7/9 Add Q29, Q30, R228 for Intel power sequence

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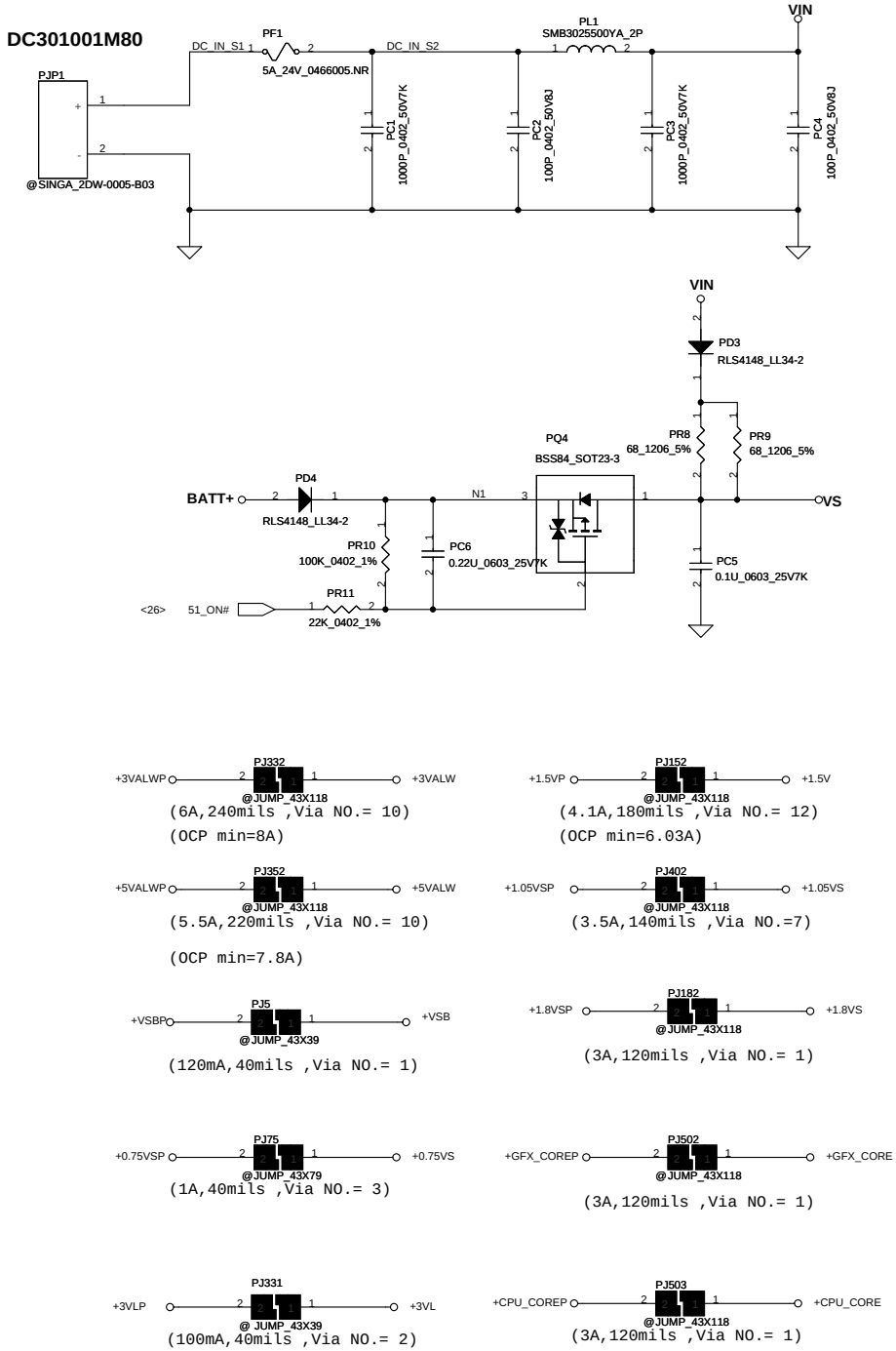

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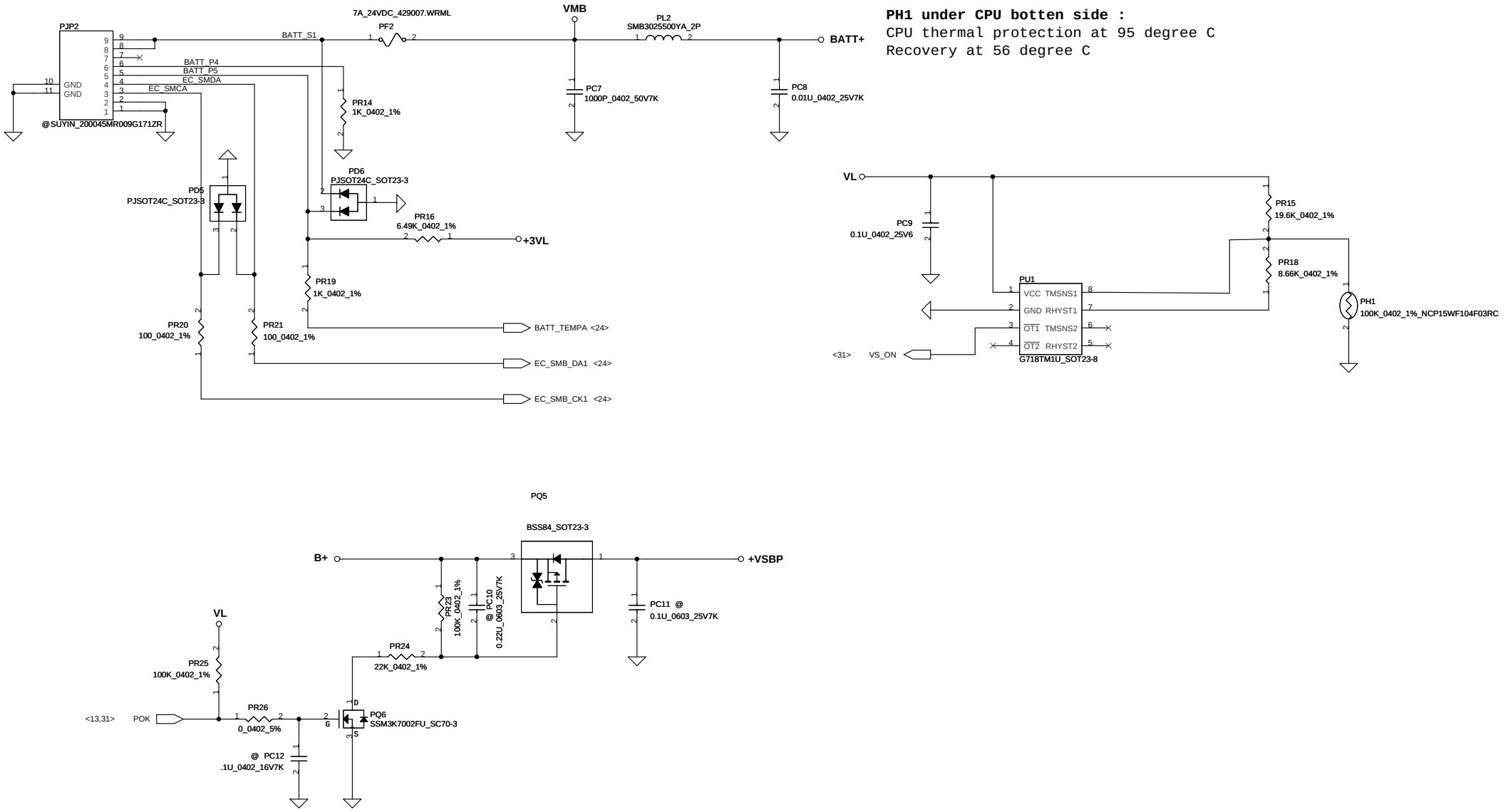
PH1 under CPU botten side :
CPU thermal protection at 95 degree C
Recovery at 56 degree C



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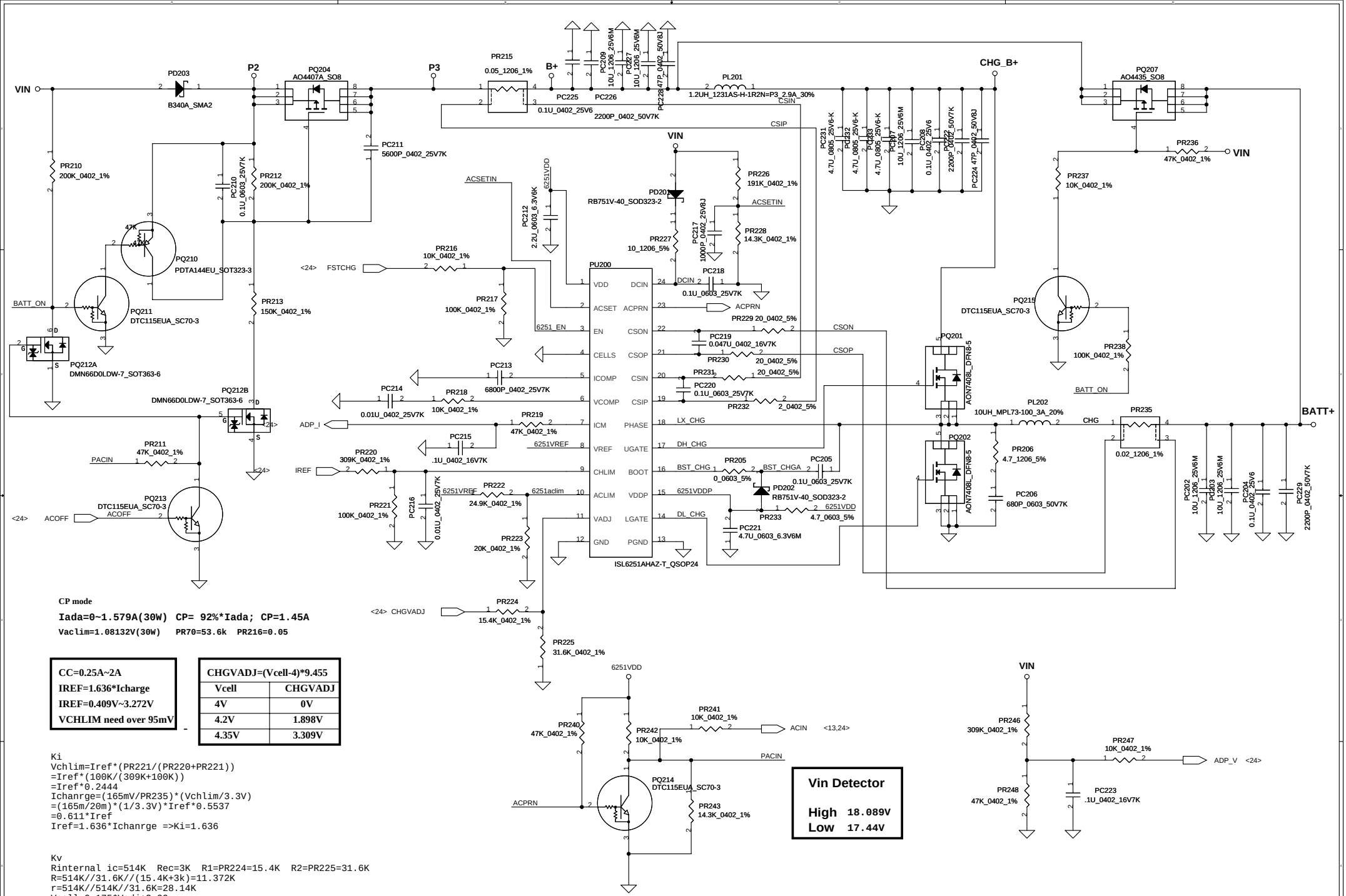

Ki
Vchlim=Iref*(PR221/(PR220+PR221))
=Iref*(100K/(309K+100K))
=Iref*0.2444
Ichanrge=(165mV/PR235)*(Vchlim/3.3V)
=(165m/20m)*(1/3.3V)*Iref*0.5537
=0.611*Iref
Iref=1.636*Ichanrge =>Ki=1.636

Kv
Rinternal ic=514K Rec=3K R1=PR224=15.4K R2=PR225=31.6K
R=514K//31.6K//(15.4K+3k)=11.372K
r=514K//514K//31.6K=28.14K
Vcell=0.175*Vadj+3.99v
4.2V=0.175*Vadj+3.99V =>Vadj=1.2V
Vadj=Vref*(R/(R+514K))+CALIBRATE*(r/(r=514K))
1.1483=CALIBRATE*0.6046 =>CALIBRATE=1.899
1.899=(4.2-(Vcell+A*0.175))*Kv=(4.2-(4.2+A*0.175))*Kv
A=Vref*(R/(R+514K))=0.052
Kv=9.455

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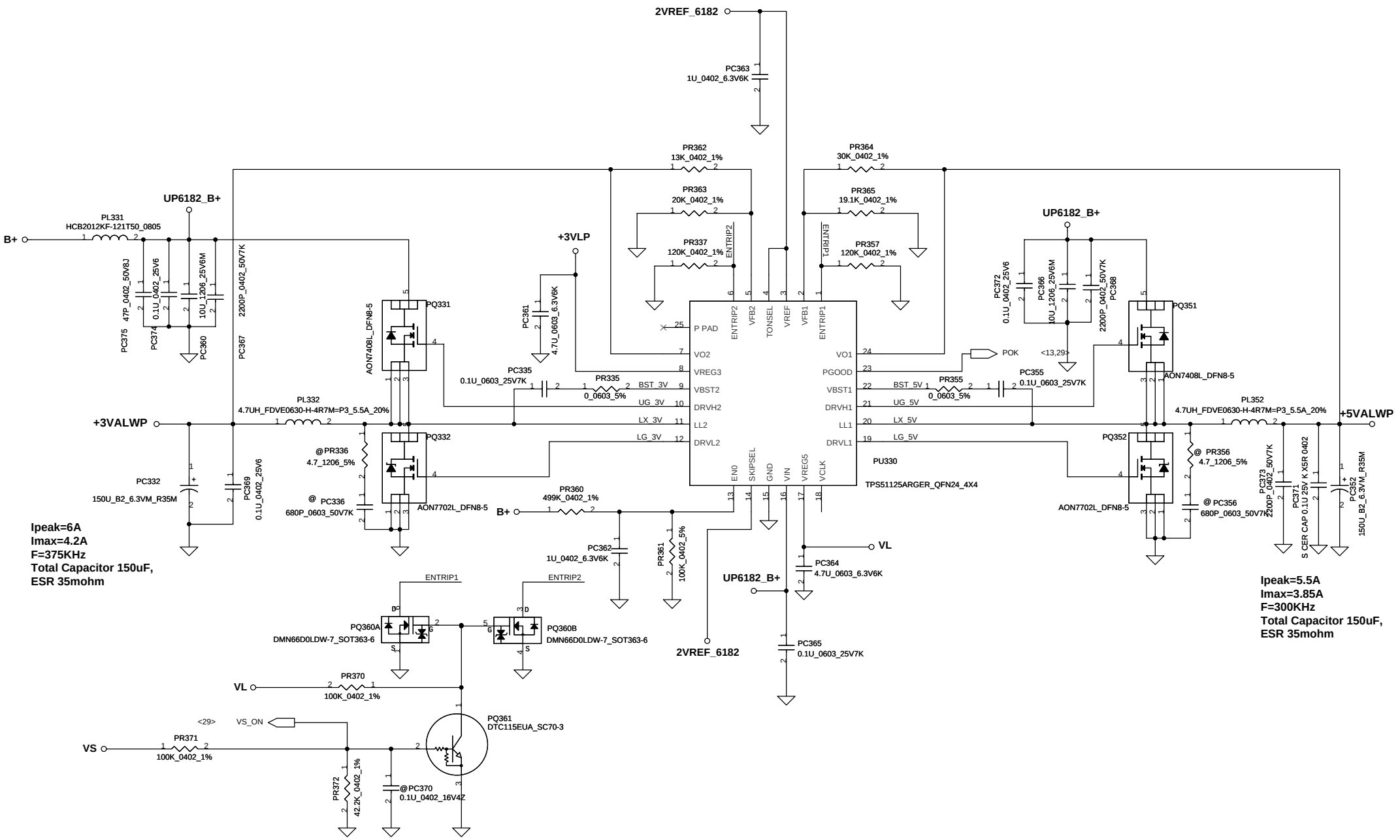

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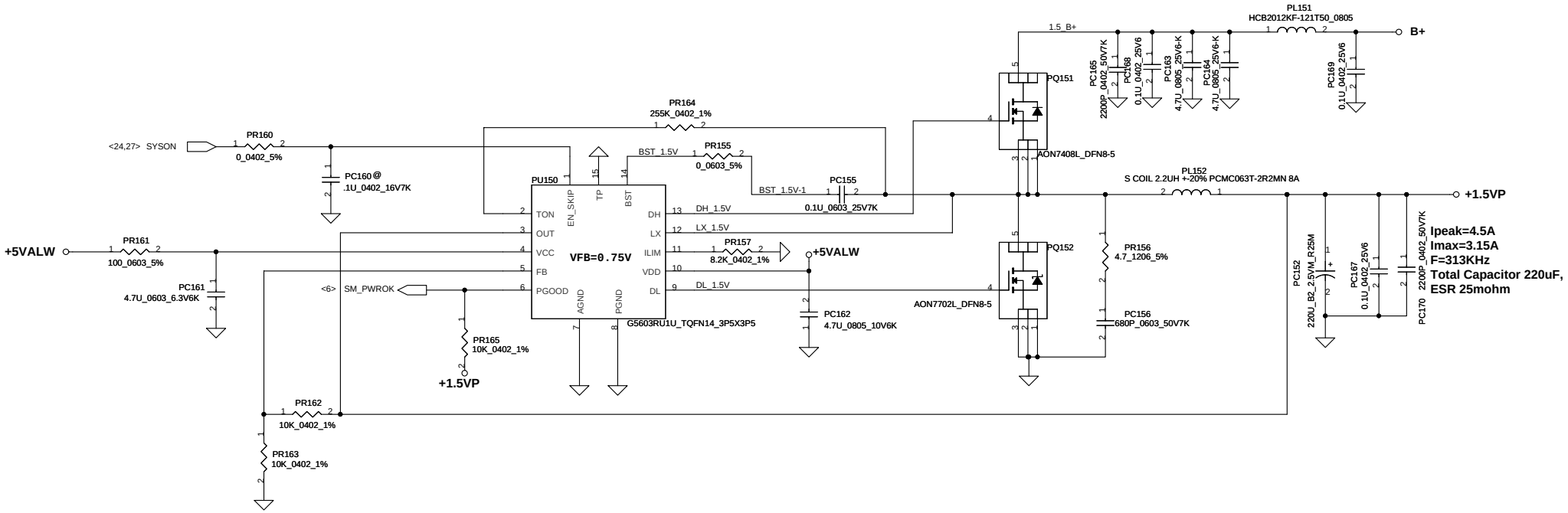

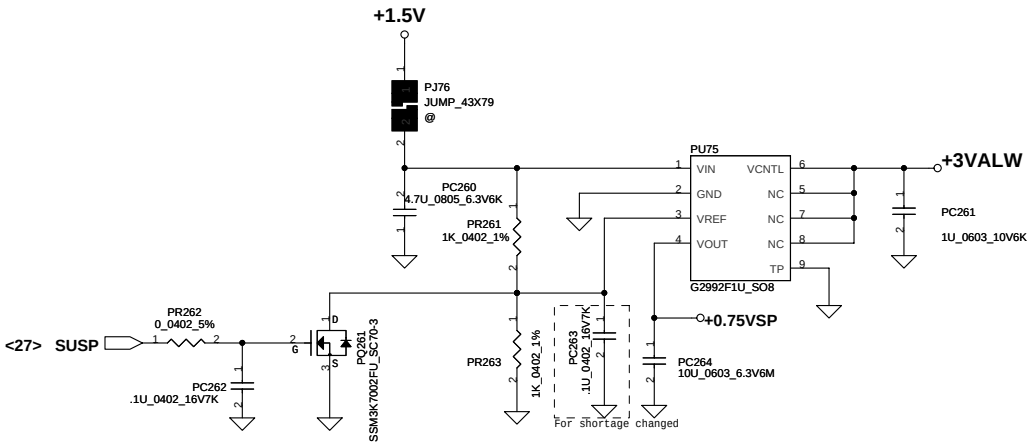

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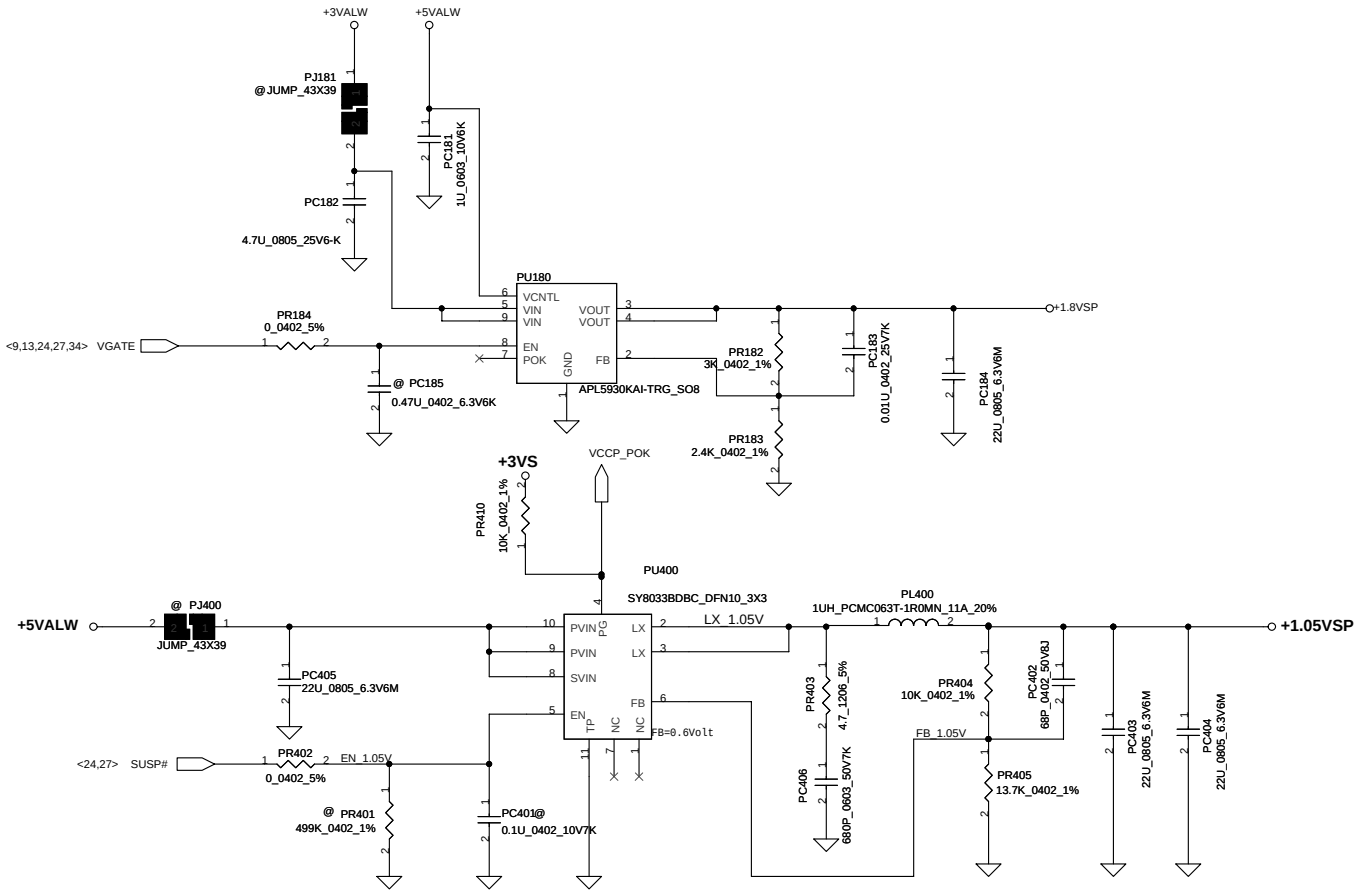

Ipeak=3.5A
ILIM = 2.45A
F=1MHz
Total Capacitor66uF,

Pin 1 define same with Pin 2 & Pin 3 that just for SY8035 ,
SY8035 is for 5A loading , let LX shape can bigger!!

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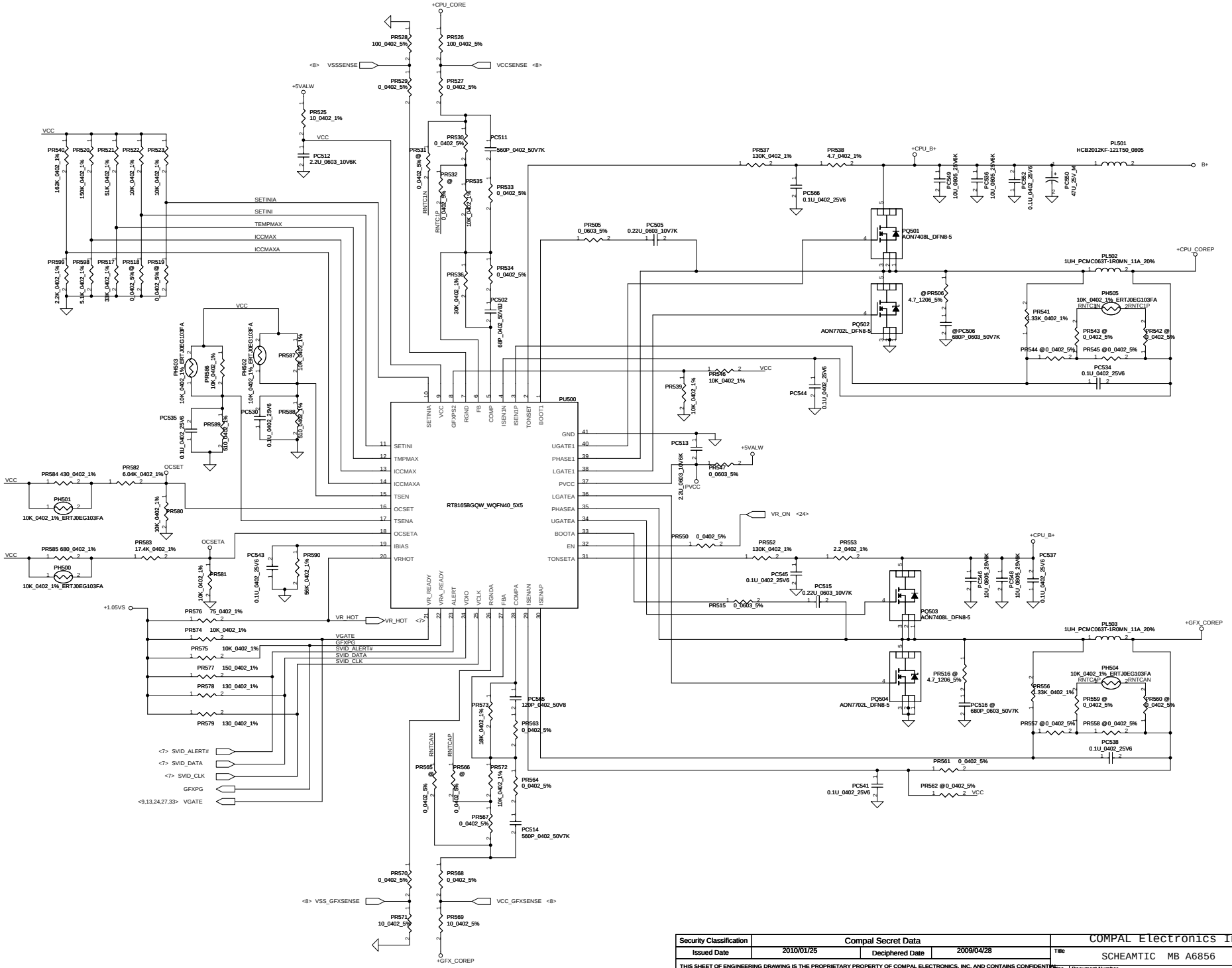

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