

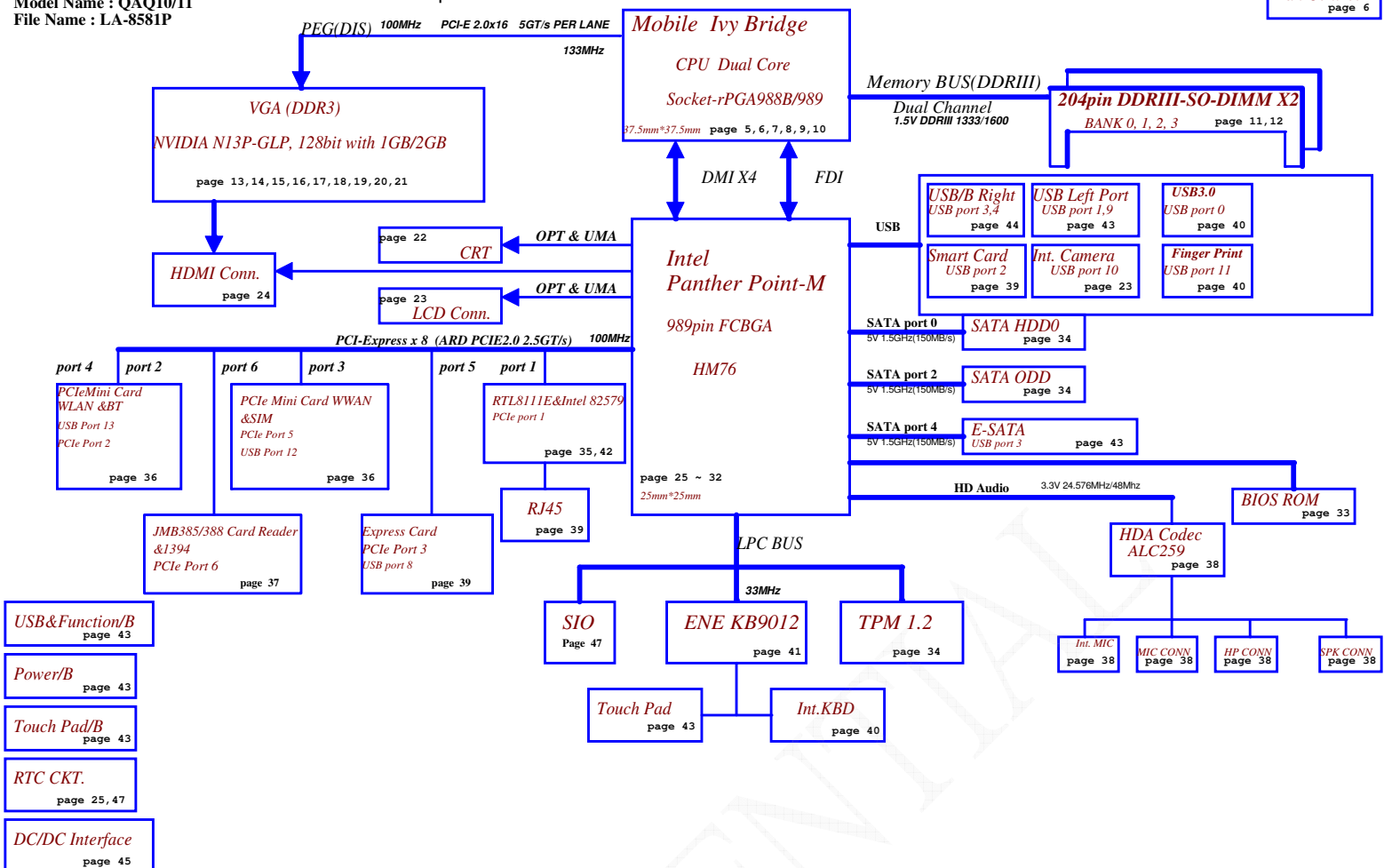
Compal Confidential

QAQ10/11

LA-8581P REV1.0 Schematic

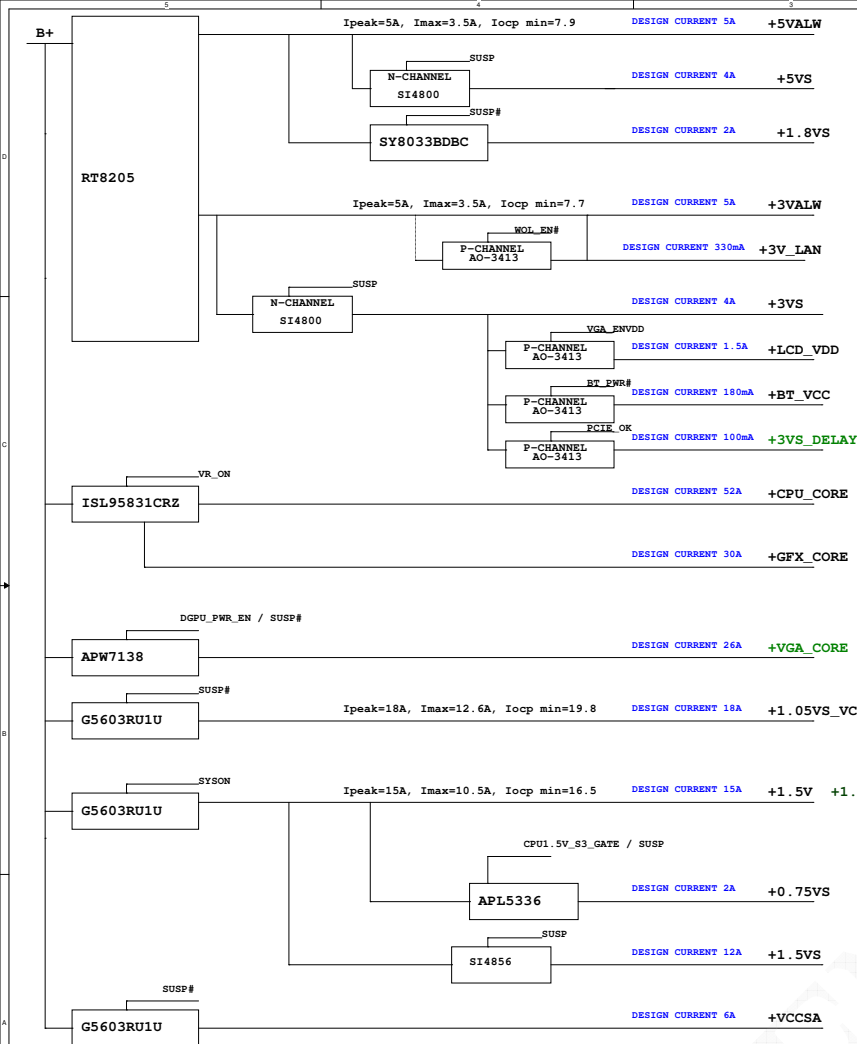
Intel Ivy Bridge/Pather Point
UMA&OPT
2012-04-23 Rev 1.0

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				Document Number
				4019IE
				Date: Friday, August 24, 2012
				Sheet 1 of 60



Power Circuit DC/DC
page 46,47,48,49,50,51,52,53,54,55,56,57,58

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				40191E
				Date: Friday, August 24, 2012
				Sheet 2 of 60



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					4019IE	6
				Date	Friday, August 24, 2012	Sheet 3 of 60

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGF_X_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VSDGPU	+1.0VSPDGPU to +1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VCCP	+1.05VS_VCCPP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VCCPP to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VALW_PCH	+5VALW to +5VALW_PCH power rail for PCH (Short resistor)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

EC SM Bus1 address			EC SM Bus2 address		
Power	Device	Address	Power	Device	Address
+3VL	charger	0x12	+3VS	VGA(N13P:GLP)	0X9E
+3VL	Smart Battery	0x16	+3VS	PCH	0x96

PCH SM Bus address		
Power	Device	Address
+3VALW	PCH	
+3VS	Clock Generator	1101 001x b
+3VS	DDR DIMMA	1001 000x b
+3VS	DDR DIMMB	1001 010x b
+3VS	Slot#1-WLAN	

BOM configu table

SKU	Description	Bom config
1	QAQ10 UMA GIGA W/HDMI	DA8@/8111E@/UMA@/TF@/10@/WIN8@/388@/COM@ 4619IE30L01
2	QAQ11 DIS N13PGLP1G W/HDMI	DA8@/8111E@/OPT@/TF@/11@/WIN8@/388@/COM@ 4619IE30L11
3	QAQ13 DIS GLP2G W/HDMI/TPM	DA8@/8111E@/OPT@/030@/13@/WIN8@/388@/COM@/TPM@/IN_TPM@ 4619IE30L21
4		
5		
6		
7		
8		

DA8@/8111E@/PCH@/UMA@/OPT@/385@/388@/389@/IN_TPM@/TPM@/WB_TPM@/SM@/COM@/030@/TF@/WIN8@/10@/11@/12@/13@/Rev02@/Rev03@/Rev04@/Rev10@/VPRO@

388@: with 1394;
389@: without 1394.

IN_TPM@: TPM chip from vendor "INFINEON";
WB_TPM@: TPM chip from vendor "Nuvoton"
With TPM SKUs: mount "TPM@ and IN_TPM@" or "TPM@ and WB_TPM@".

If has Vpro@, no 8111E@, Rev02@, Rev03@, Rev04@ and Rev10@.

X76 AND VGA configu table

SKU	Description	Config
1	4619IE30L11	222 SAM1G@ 222 HY1G@ HY1G 1G
2		
3	4619IE30L21	222 SAM2G@ 222 HY2G@ SAM 2G HY2G 2G
4		
5		

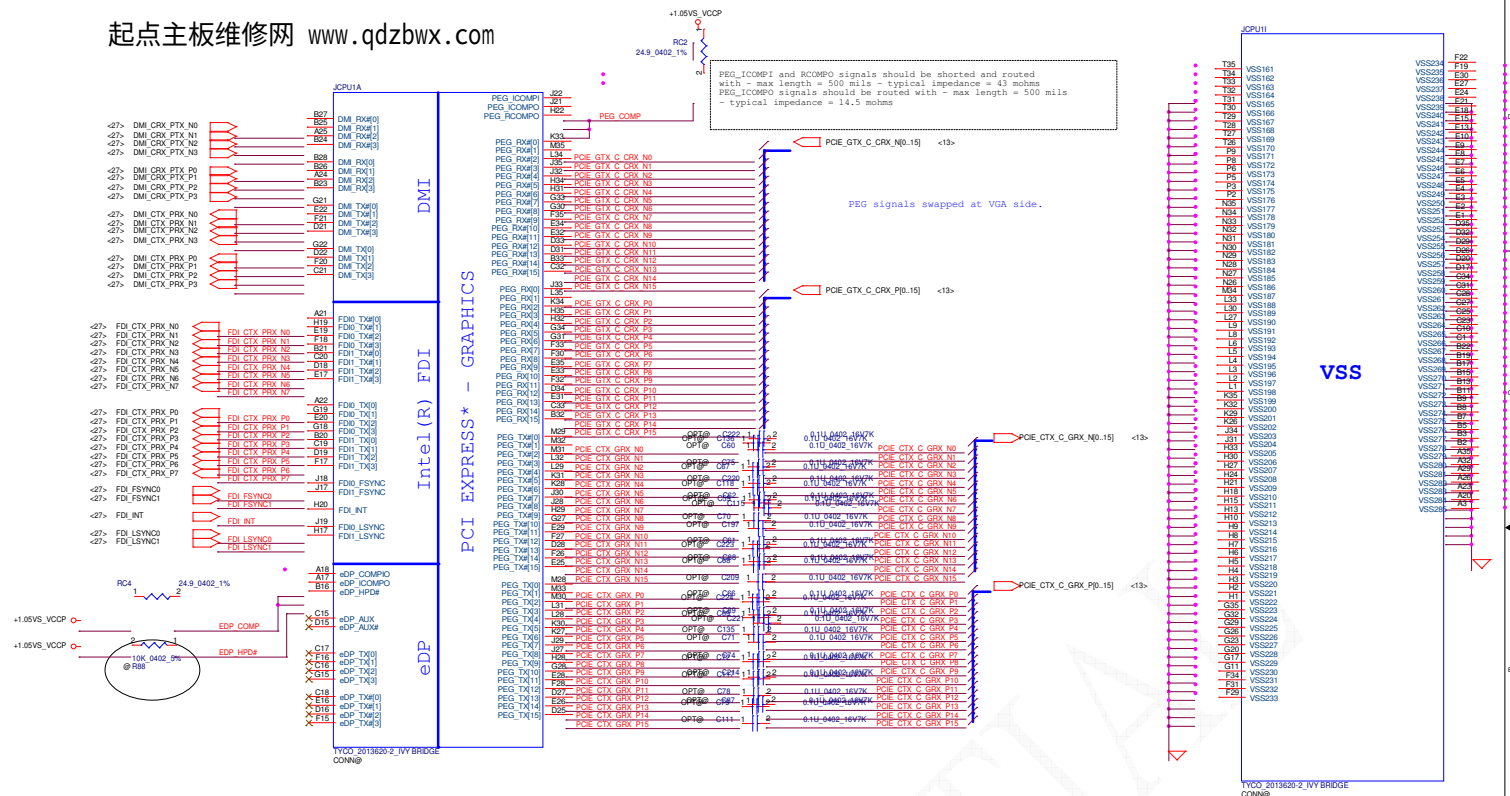
Board ID Table

Part No.	Rev	Ra	R/C	V_BLD	V_Typ	Max	PCB Revision
1	0	100K +/- 5%	3.3V +/- 5%	3V	3V	3.1	1
2	8.2K +/- 5%	100K +/- 5%	3.3V +/- 5%	3.216 V	3.250 V	3.289 V	2
3	18K +/- 5%	100K +/- 5%	3.3V +/- 5%	3.436 V	3.503 V	3.538 V	3
4	33K +/- 5%	100K +/- 5%	3.3V +/- 5%	3.712 V	3.819 V	3.875 V	4
5	56K +/- 5%	100K +/- 5%	3.3V +/- 5%	1.036 V	1.185 V	1.264 V	5
6	100K +/- 5%	100K +/- 5%	3.3V +/- 5%	1.453 V	1.450 V	1.759 V	6
7	200K +/- 5%	100K +/- 5%	3.3V +/- 5%	1.935 V	2.200 V	2.341 V	7
8	NC	100K +/- 5%	3.3V +/- 5%	2.500 V	3.300 V	3.300 V	8

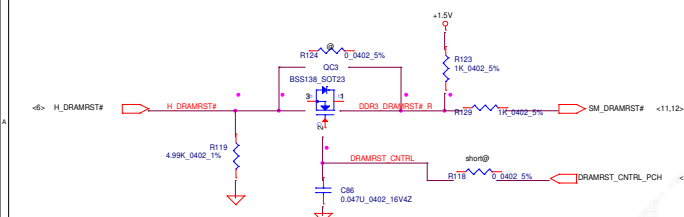
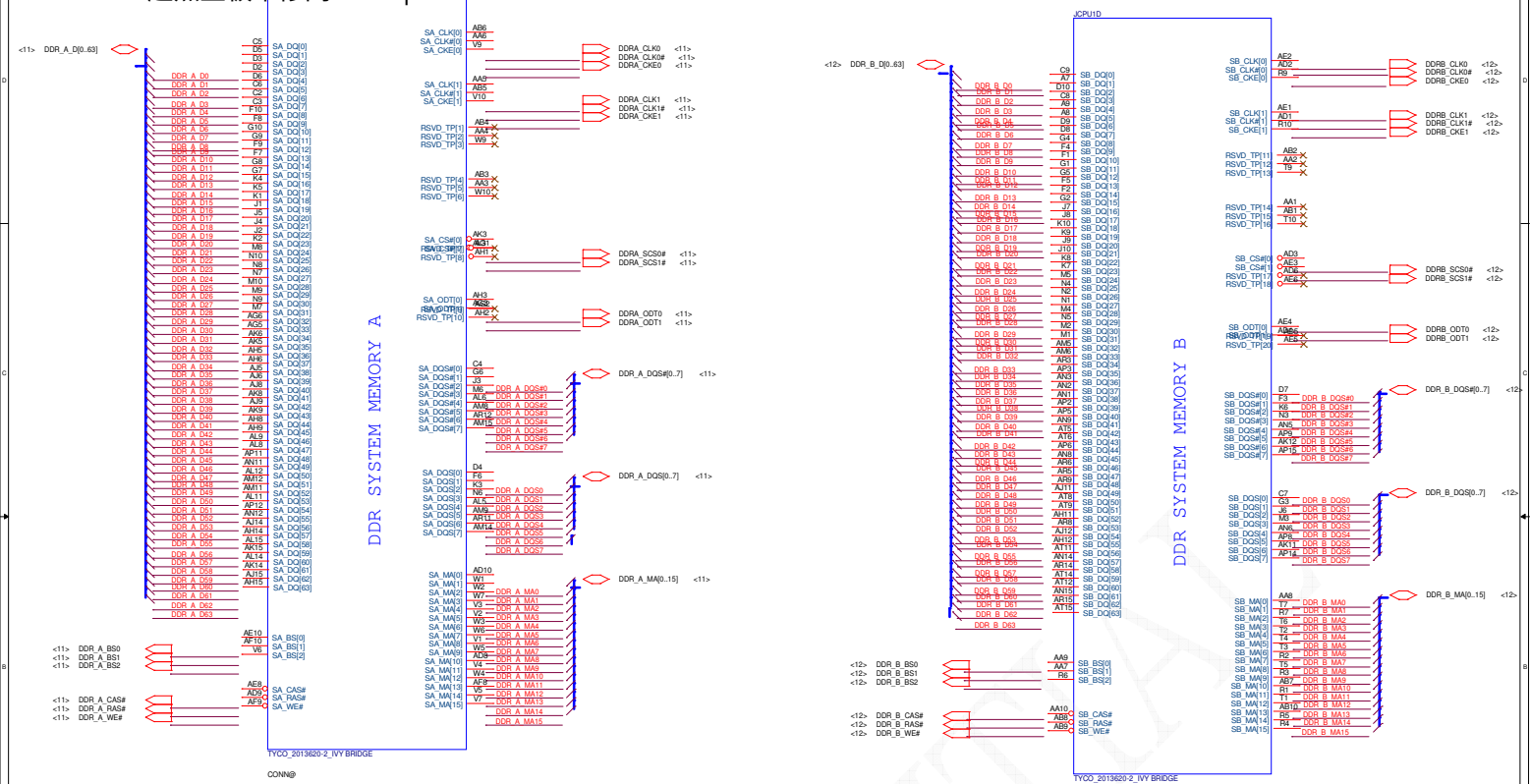
PCH And PCBA table

PCH	UPCH1 B08CMT7S SLJ8E C1 BGA 989P PCH 0301 8111E@	UPCH1 B08CMT77 QPRE C1 BGA 989P PCH VPRO@
PCB	222 DA8@ PCB LA-8881P REV1 MB	222 DA2@ PCB QAQ10

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Rev	0	Document Number	4019IE	Rev
Date	Friday, August 24, 2012	Sheet	4	of 50



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Sheet		3		of 60	

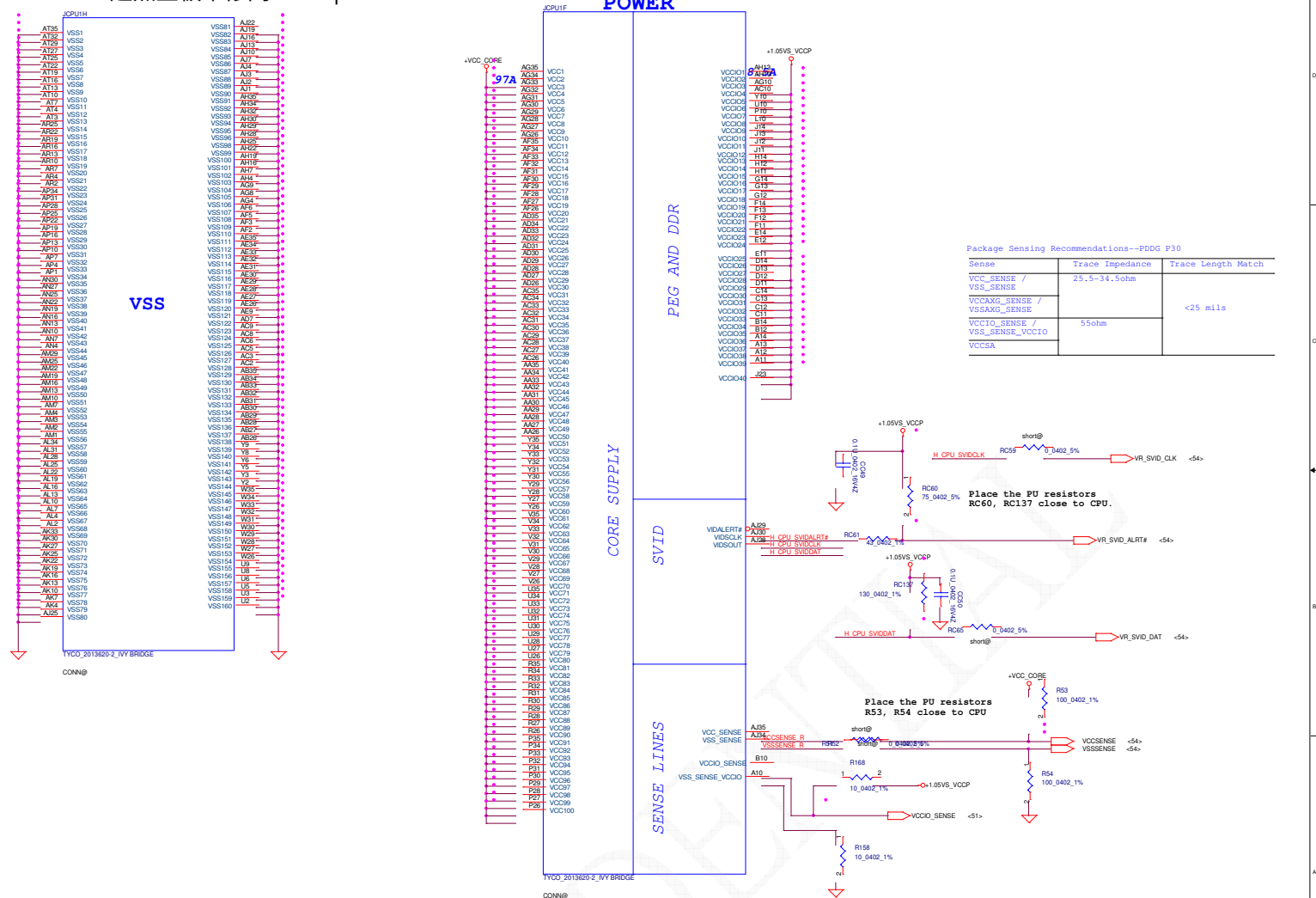


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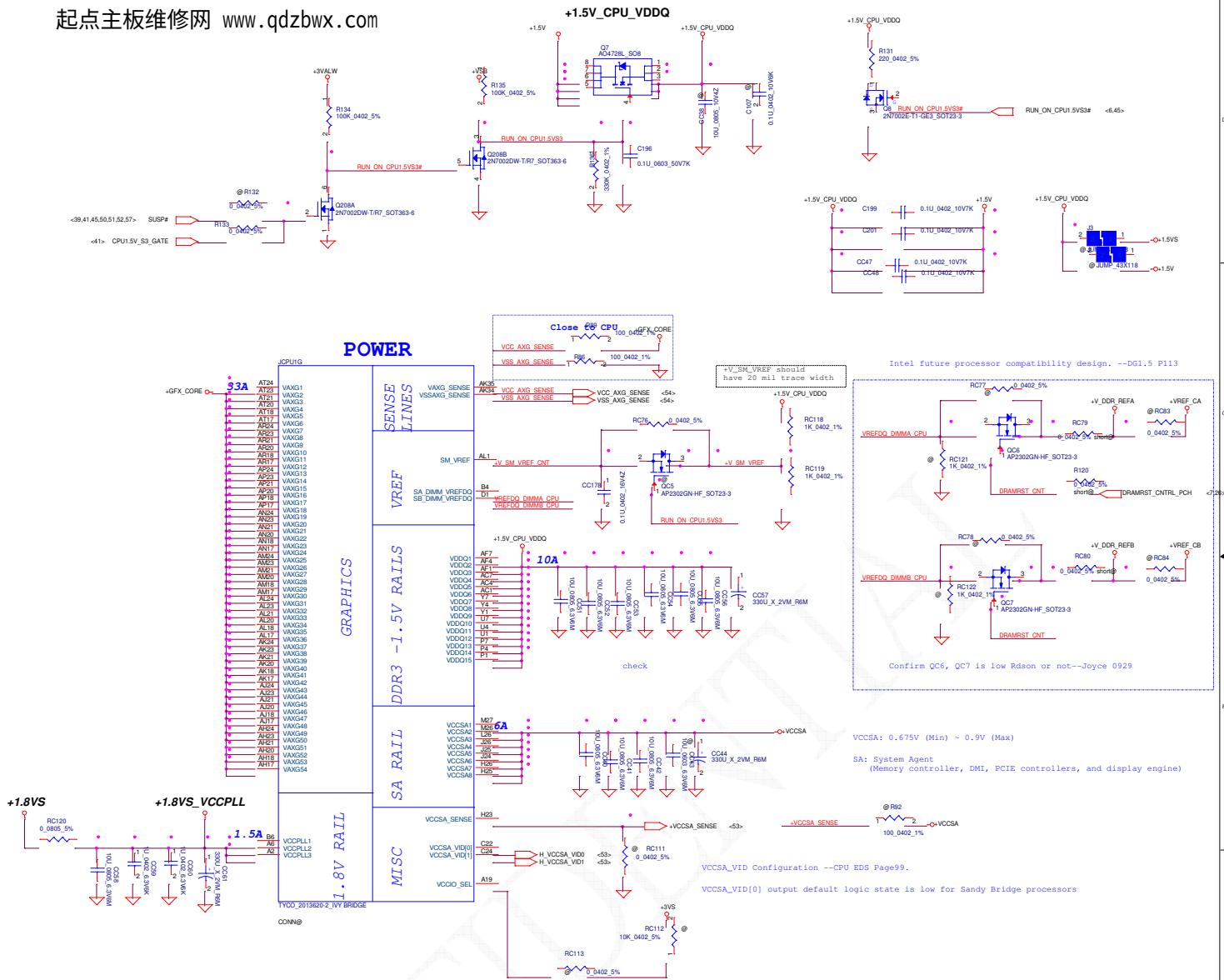
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CFG[17:0]:
Processor internal pull up 5~15Kohm to VCCIO
```

CFG Straps for Processor

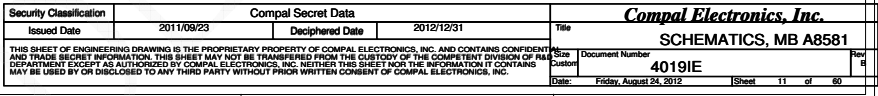
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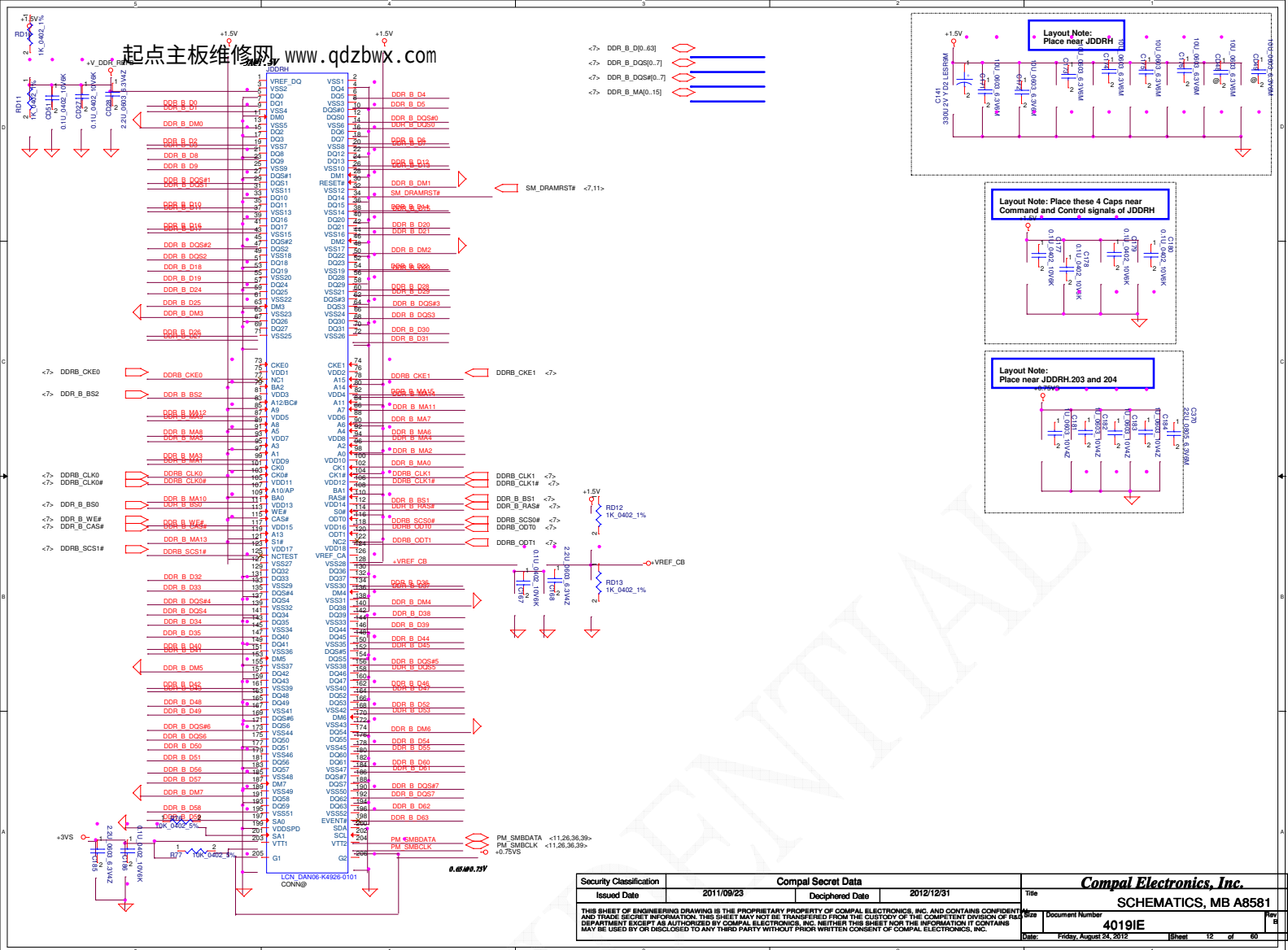


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				Size	
				Document Number	
				40191E	
				Date	
				Friday, August 24, 2012	
				Sheet	
				9 of 60	

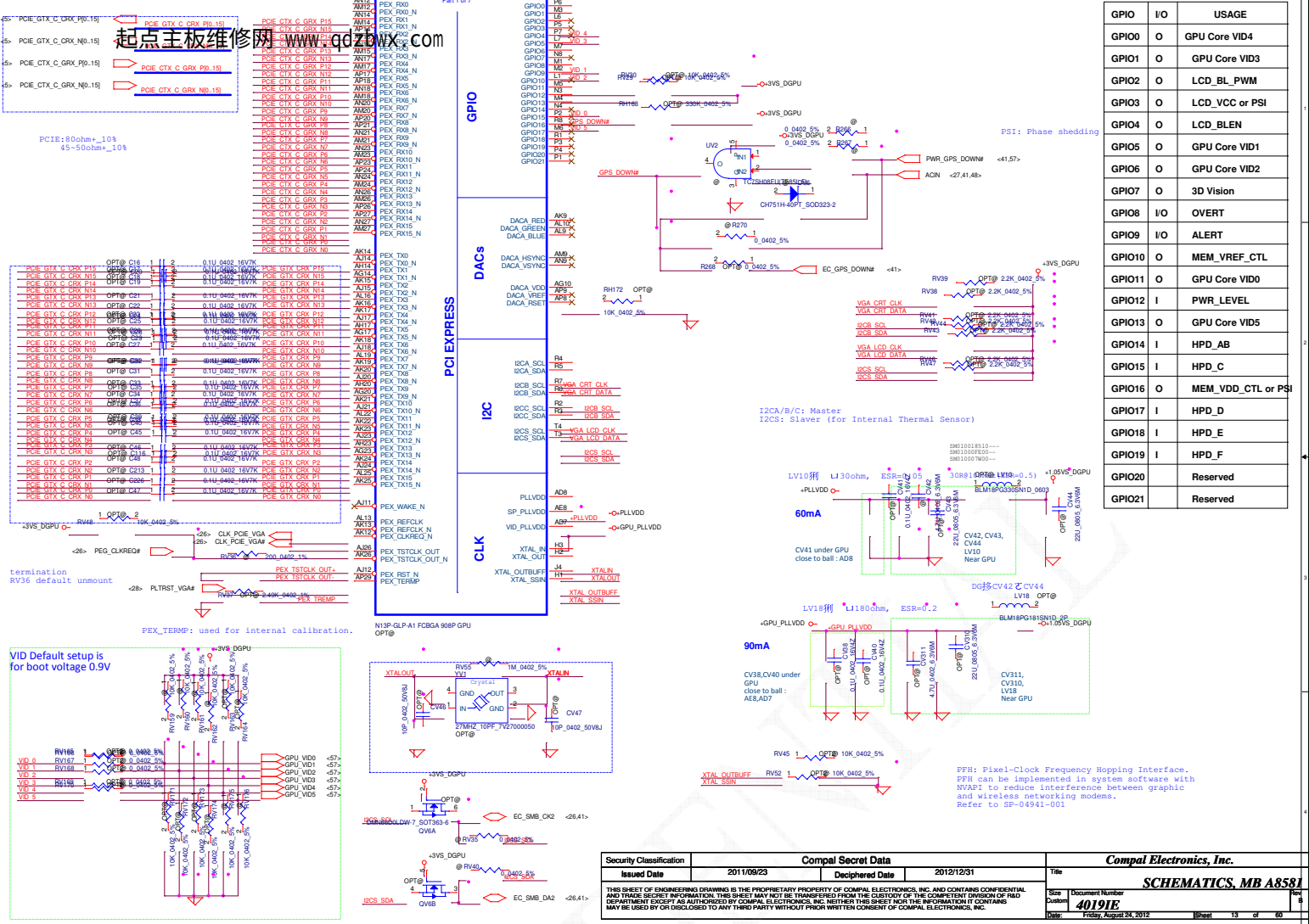


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				Date	Y0000, August 24, 2012
				Sheet	18 of 60

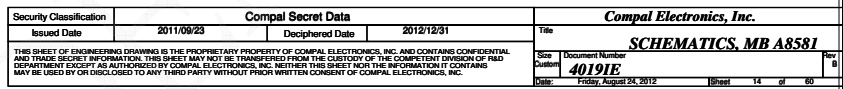


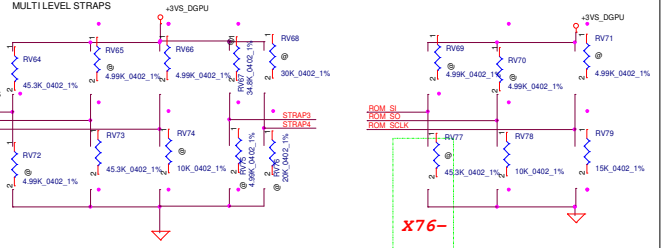
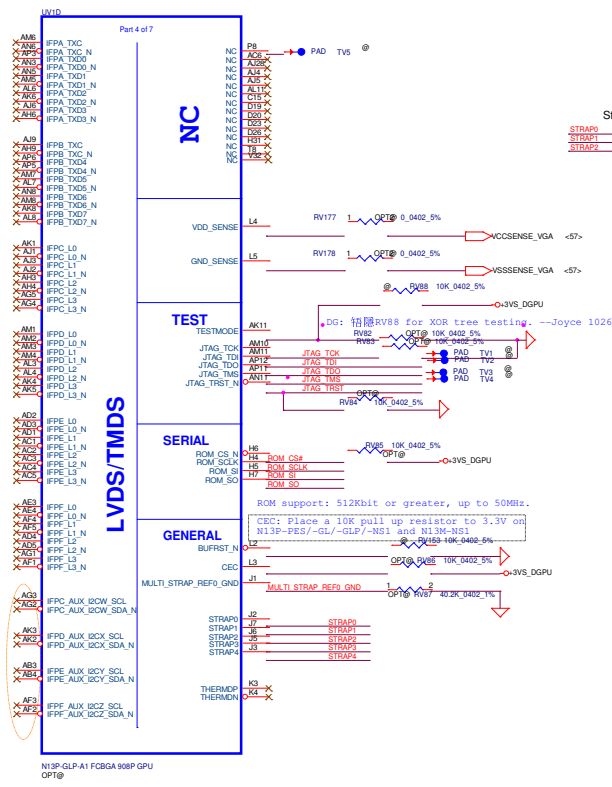


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				Sheet 12 of 60	



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Size	Document Number	Customer	4019IE
Date	Friday, August 24, 2012	Sheet	13 of 66





Physical strapping pin	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	Resistor Values	Pull up to 3V	Pull down to GND
ROM_SCLK	PCI_DEV0[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	5K	1000	0000
ROM_SI	RAM_CFG[3]	RAM_CFG[1]	RAM_CFG[0]	RAM_CFG[0]	10K	1001	0001
ROM_SO	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE	15K	1010	0010
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	20K	1011	0011
STRAP1	SGIO_PAD_CFG_ADR[3]	SGIO_PAD_CFG_ADR[2]	SGIO_PAD_CFG_ADR[1]	SGIO_PAD_CFG_ADR[0]	25K	1100	0100
STRAP2	PCI_DEV0[3]	PCI_DEV0[2]	PCI_DEV0[1]	PCI_DEV0[0]	30K	1101	0101
STRAP3	SORD_EXPOSED	SORD_EXPOSED	SORD_EXPOSED	SORD_EXPOSED	35K	1110	0110
STRAP4	RESERVED	PCI_SPEED_CHANGE_SEL[3]	PCI_MAX_SPEED	DP_PLL_V0003V	45K	1111	0111

SUB_VENDOR	PEX_PLL_EN_TERM	PCI_MAX_SPEED
0 No VBIOS ROM	PLL termination setting	0 Limited to PCIe GEN 1
1 BIOS ROM is present (Default)	0 Disable (Default)	1 PCIe GEN 2/3 capable
1 Enable		

FB[1:0] NT5x FB Aperture Size
0 RESERVED
1 RESERVED
2 256 MB (Default)
3 RESERVED

USER Straps
1111 EDIO is used
others: DG-05587 Page155

SGIO_PAD_CFG
0000-0101 RESERVED
0110 Notebook (default)
0111-1111 RESERVED

For N13P-GLP strap table

For N13P-PES :
Strap 0 : PU45
Strap 1 : PD35
Strap 2 : PU35
ROM_SCLK : PU15
ROM_SI : PD35
ROM_SO : PD10

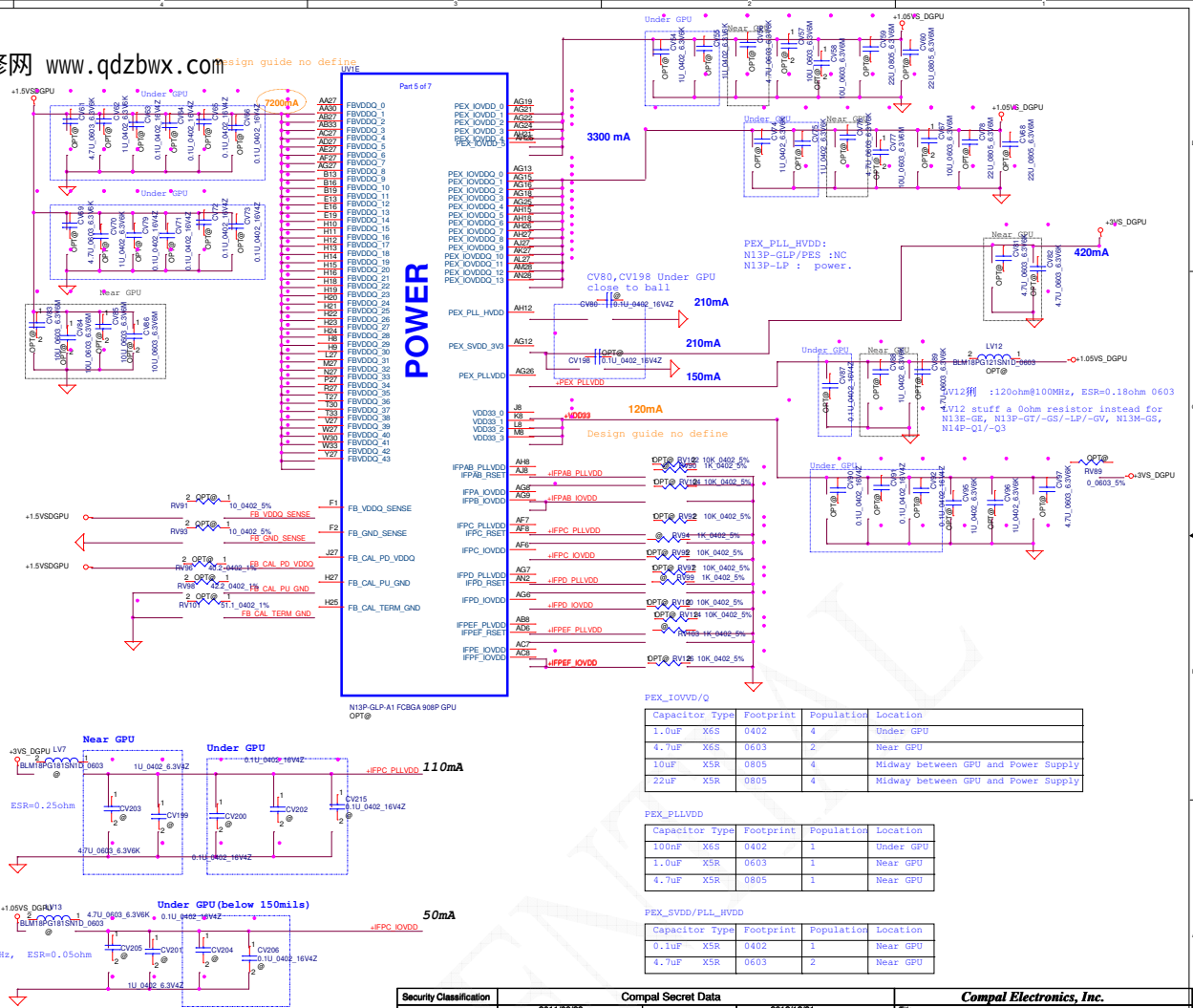
GPU	Freq	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13P-GLP	900 MHz	64M 16" 8	Hynix SA000041S20	RV64 PU 45K	RV73 PD 45K	RV74 PU 5K	NC	NC	RV77 PD 15K	RV70 PD 30K	RV71 PD 15K
	900 MHz	64M 16" 8	Samsung SA000043S00	RV64 PU 45K	RV73 PD 45K	RV74 PU 5K	NC	NC	RV77 PD 20K	RV70 PD 30K	RV71 PD 15K
	900 MHz	128M 16" 8	Hynix SA00003YC00	RV64 PU 45K	RV73 PD 45K	RV74 PU 5K	NC	NC	RV77 PD 35K	RV70 PD 30K	RV71 PD 15K
	900 MHz	128M 16" 8	Samsung SA00004YC00	RV64 PU 45K	RV73 PD 45K	RV74 PU 5K	NC	NC	RV77 PD 45K	RV70 PD 30K	RV71 PD 15K

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Title			Schematics, MB A8581	
Size			Document Number	
Case			40191E	
Date			Friday, August 24, 2012	
Sheet			19 of 80	

FBVDDQ Decoupling Design Guide:

0.1uF	X7R	0402	8pcs	under GPU
1uF	X7R	0603	2pcs	under GPU
4.7uF	X6S	0603	2pcs	under GPU
10uF	X5R	0805	4pcs	Near GPU

Calibration Pin	DDR3	GDDR5
FB_CAL_PD_VDDQ	40.2ohm	40.2ohm
FB_CAL_PU_GND	42.2ohm	40.2ohm
FB_CAL_TERM_GND	51.1ohm	60.4ohm

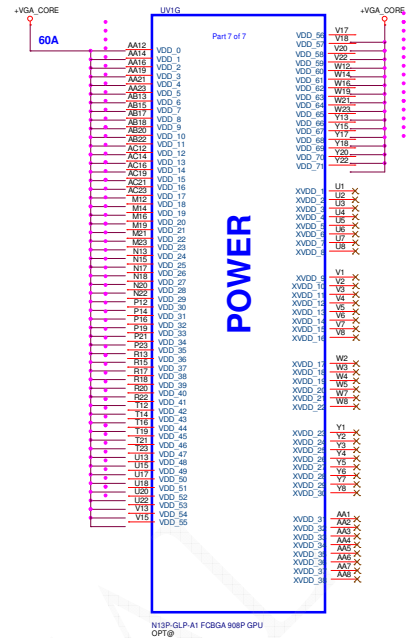
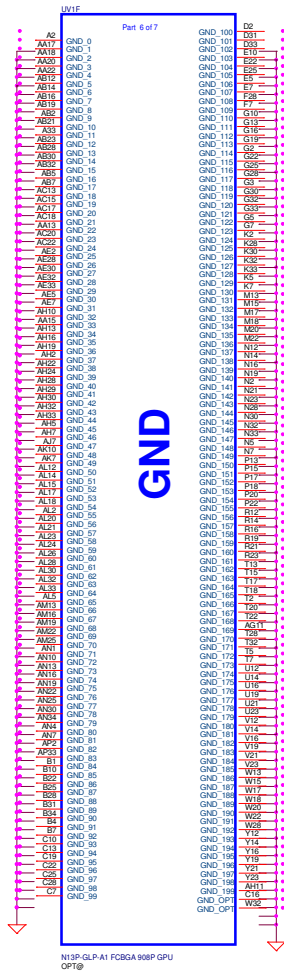


Capacitor Type	Footprint	Population	Location
1.0uF X6S	0402	4	Under GPU
4.7uF X6S	0603	2	Near GPU
10uF X5R	0805	4	Midway between GPU and Power Supply
22uF X5R	0805	4	Midway between GPU and Power Supply

PEX_PLLVDD				
Capacitor Type		Footprint	Population	Location
100nF	X6S	0402	1	Under GPU
1.0uF	X5R	0603	1	Near GPU
4.7uF	X5R	0805	1	Near GPU

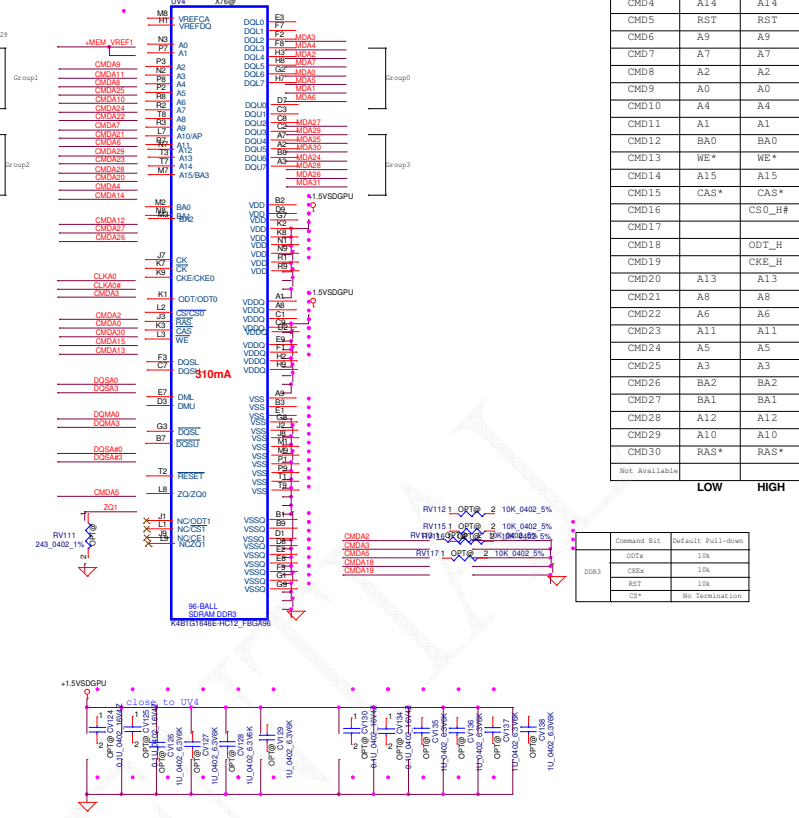
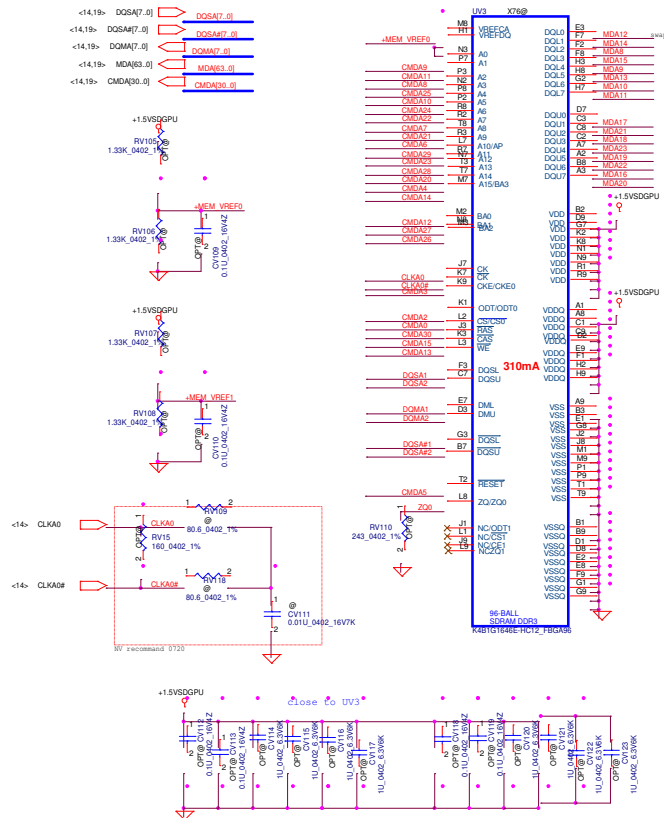
PEX_SVDD/PLL_HVDD				
Capacitor	Type	Footprint	Population	Location
0.1uF	X5R	0402	1	Near GPU
4.7uF	X5R	0603	2	Near GPU

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			Sheet	16 of 41



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				Contour	40191E
				Date	Friday, August 24, 2012
				Sheet	17 of 80

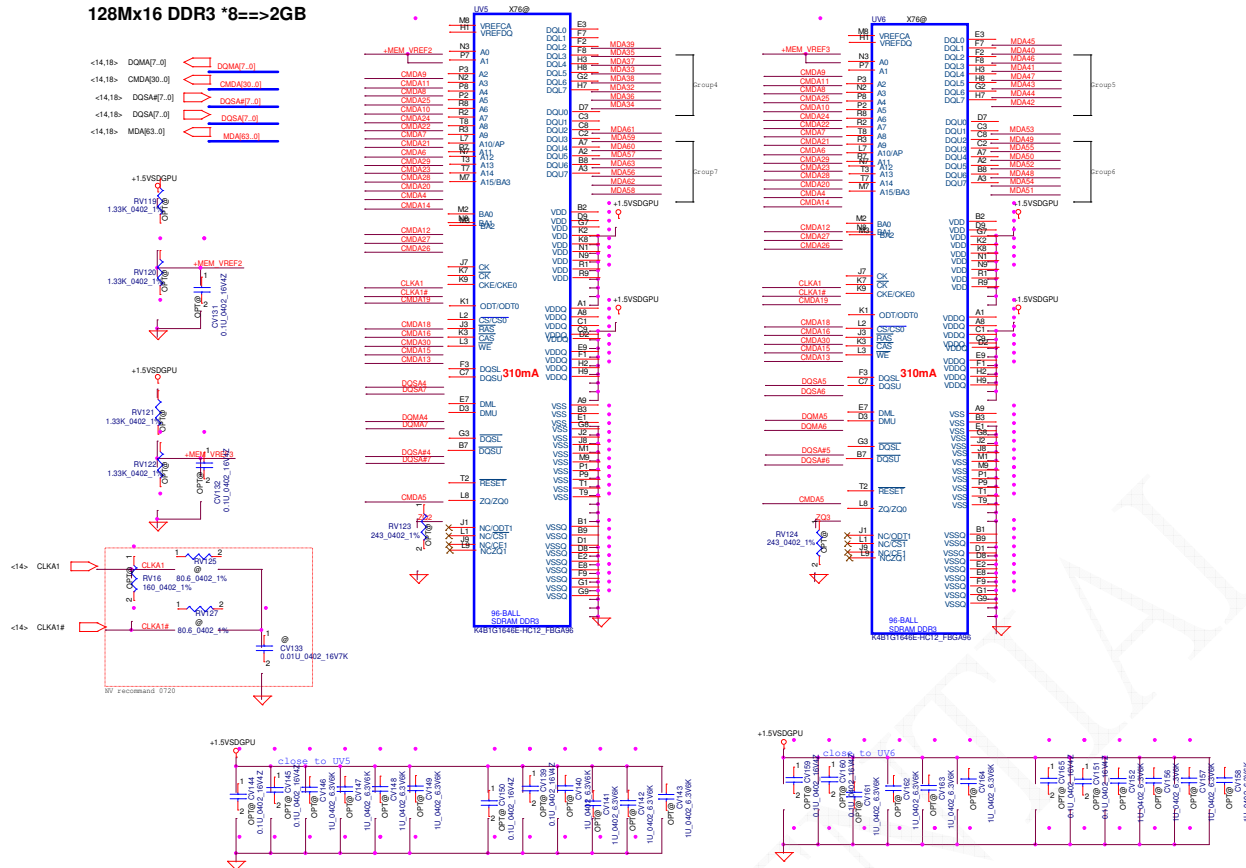
Input	Output
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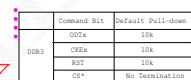
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CM01		
CM02	ODT_L	
CM03	CKE	
CM04	A14	A14
CM05	RST	RST
CM06	A9	A9
CM07	A7	A7
CM08	A2	A2
CM09	A0	A0
CM10	A4	A4
CM11	A1	A1
CM12	BA0	BA0
CM13	WE*	WE*
CM14	A15	A15
CM15	CAS*	CAS*
CM16		CS0_R#
CM17		
CM18		ODT_R
CM19		CKE_R
CM20	A13	A13
CM21	A8	A8
CM22	A6	A6
CM23	A11	A11
CM24	A5	A5
CM25	A3	A3
CM26	BA2	BA2
CM27	BA1	BA1
CM28	A12	A12
CM29	A10	A10
CM30	RAS*	RAS*
Wtr. Available		

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CREx	10k
	RST	10k
	CS*	No Termination

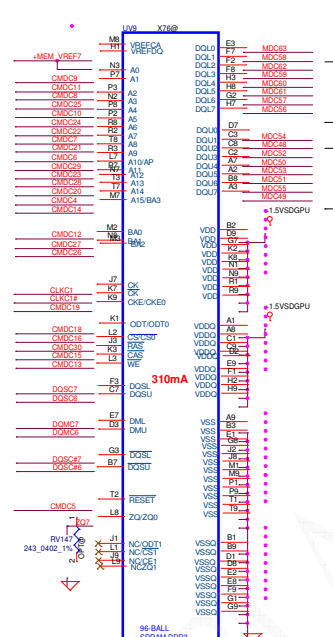
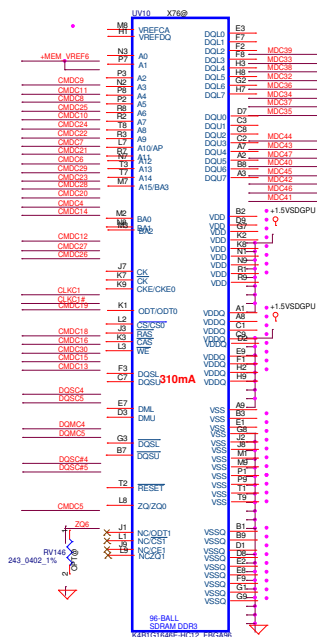
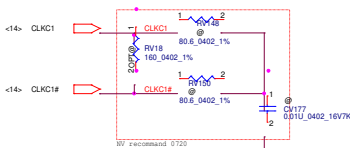
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				40191E	18	B
				Date	10/29/2012	18 of 60



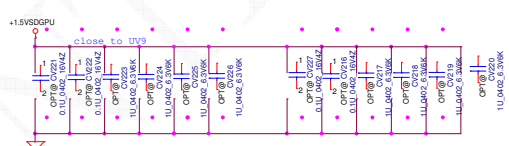
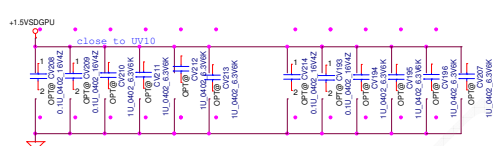
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Date				2011/09/23		2011/09/23		2011/09/23		2011/09/23	
Sheet				19		19		19		19	



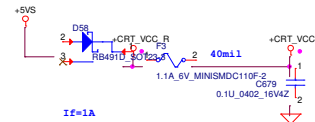
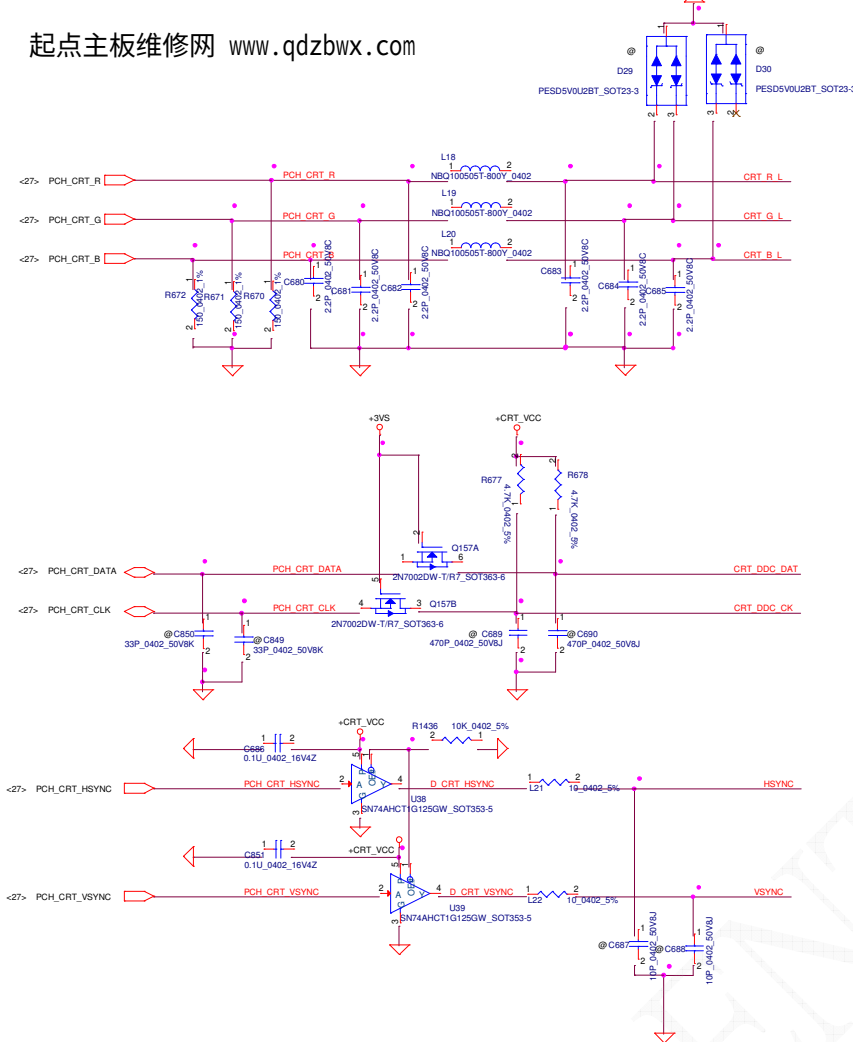
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Size	Date		Rev	
A B	Friday, August 26, 2012		20 of 60	



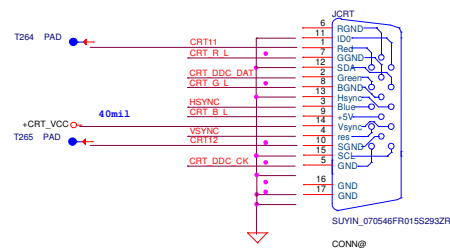
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CM02	ODT_L	
CM03	CKE	
CM04	A14	A14
CM05	RST	RST
CM06	A9	A9
CM07	A7	A7
CM08	A2	A2
CM09	A0	A0
CM10	A4	A4
CM11	A1	A1
CM12	BA0	BA0
CM13	WE*	WE*
CM14	A15	A15
CM15	CAS*	CAS*
CM16	CAS0_H#	
CM17		
CM18	ODT_H	
CM19	CKE_H	
CM20	A13	A13
CM21	A8	A8
CM22	A6	A6
CM23	A11	A11
CM24	A5	A5
CM25	A3	A3
CM26	BA2	BA2
CM27	BA1	BA1
CM28	A12	A12
CM29	A10	A10
CM30	RAS*	RAS*
Not Available		



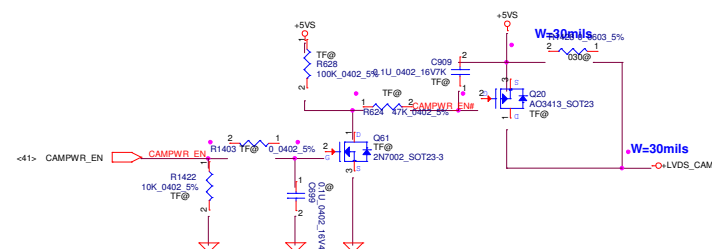
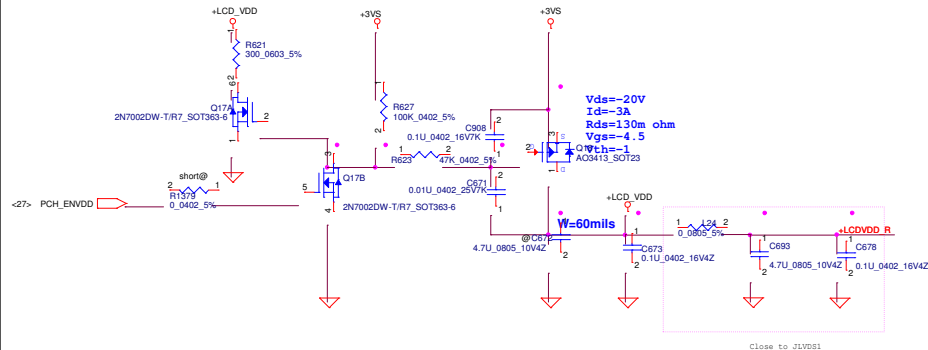
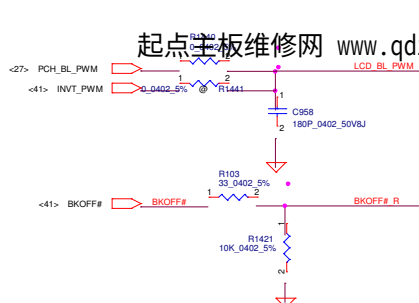
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			Sheet	21 of 60



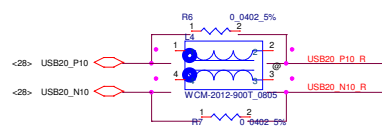
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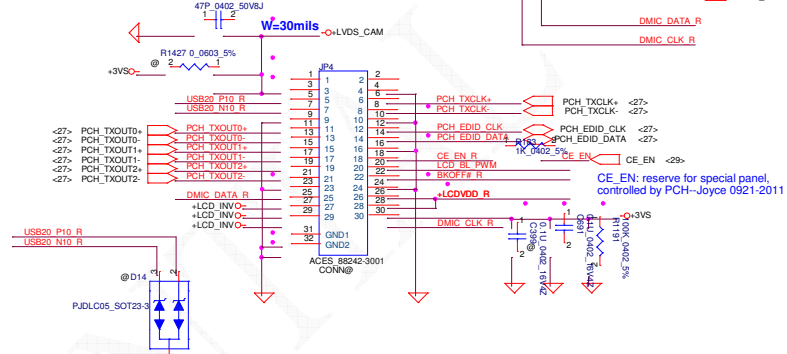
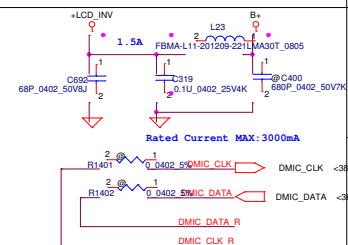
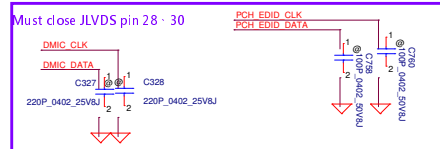
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				Document Number
				4019IE
				Date: Friday, August 24, 2012
				Sheet 22 of 90



Add on 7/27 for fn+f5 turn off camera.

**LCD/PANEL BD. Conn.**

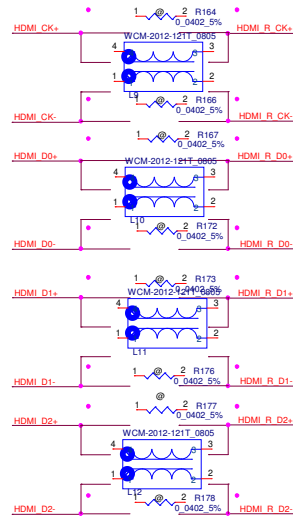
Must close JLVDS pin 28、30



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Internal Graphic Video Chanel
UMA0 Channel



HOT PLUG1



if use VGA_RDM1,
R690~R697 should be 499ohm+/-1%.

HDMI R CK+ R690 1 2 680 +5% 0402

HDMI R CK- R691 1 2 680 +5% 0402

HDMI R D1+ R692 1 2 680 +5% 0402

HDMI R D1- R693 1 2 680 +5% 0402

HDMI R D0+ R694 1 2 680 +5% 0402

HDMI R D0- R695 1 2 680 +5% 0402

HDMI R D2+ R696 1 2 680 +5% 0402

HDMI R D2- R697 1 2 680 +5% 0402

2 1 C2 2N7002 50T23

100K 0402 5% R698

0.1uF 0402 16V42 C366

EDID SELECT

3V5

HDMI_5V_OUT

R431 short@ 2 0.0402_5%

R1329 2.2K_0402_5%

R1328 2.2K_0402_5%

BSH111_SOT23-3 Q183

Q182 BSH111 SOT23-3

HDMI R_CLK

HDMI SCLK

HDMI R_DATA

HDMI SDATA

short@ 2 0.0402_5%

R436 short@ 2 0.0402_5%

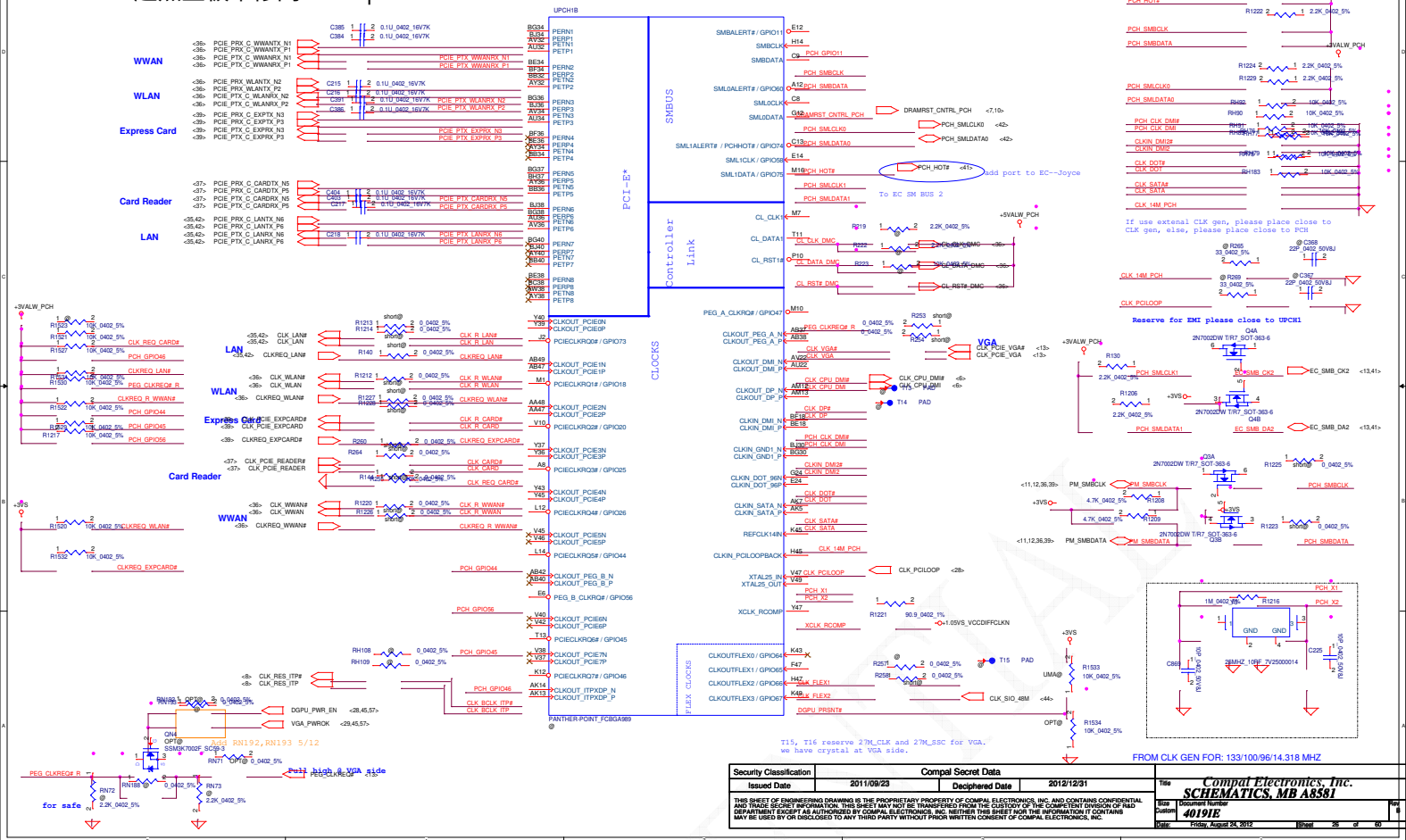
HDMI R_CLK

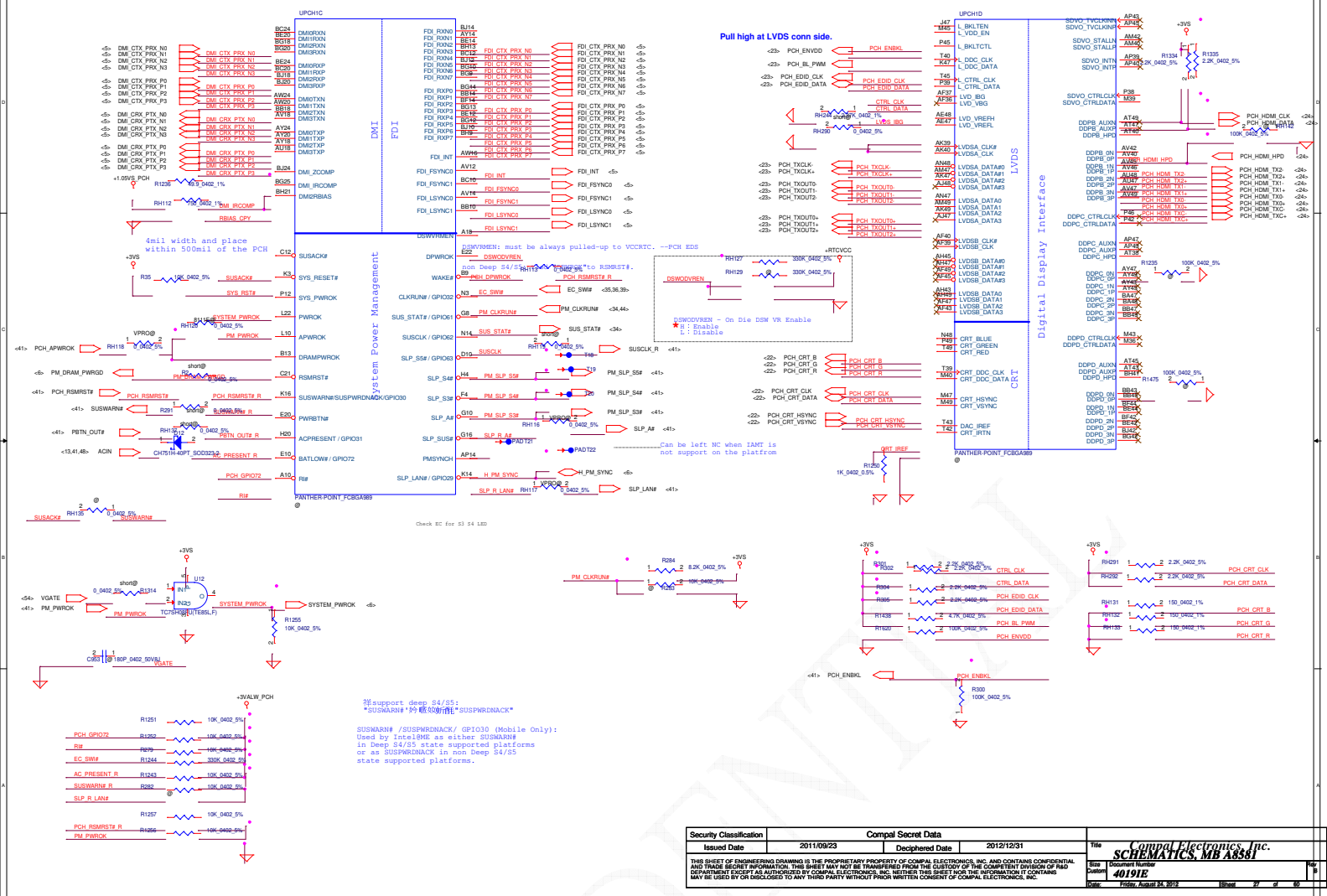
HDMI R_DATA

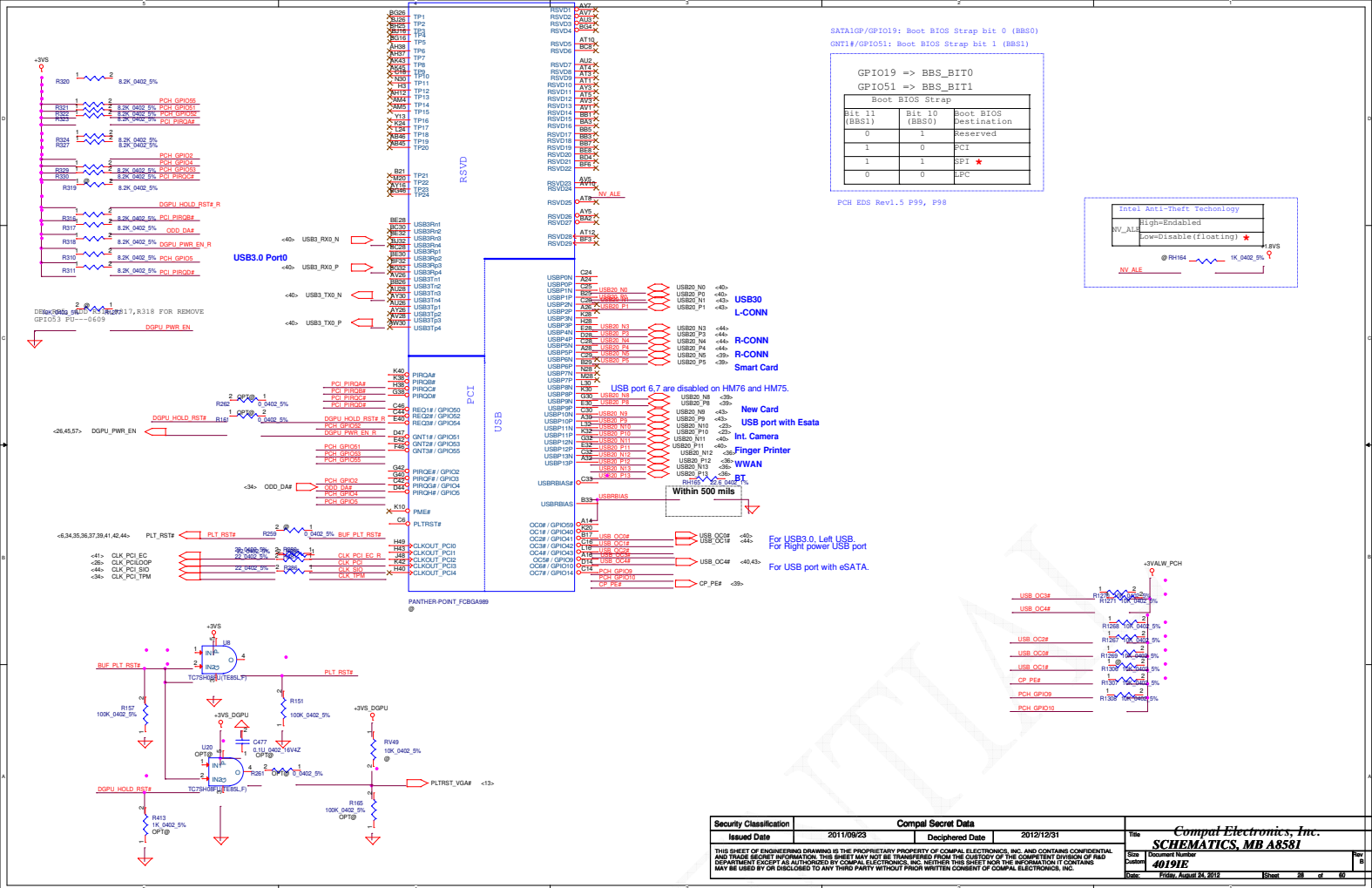
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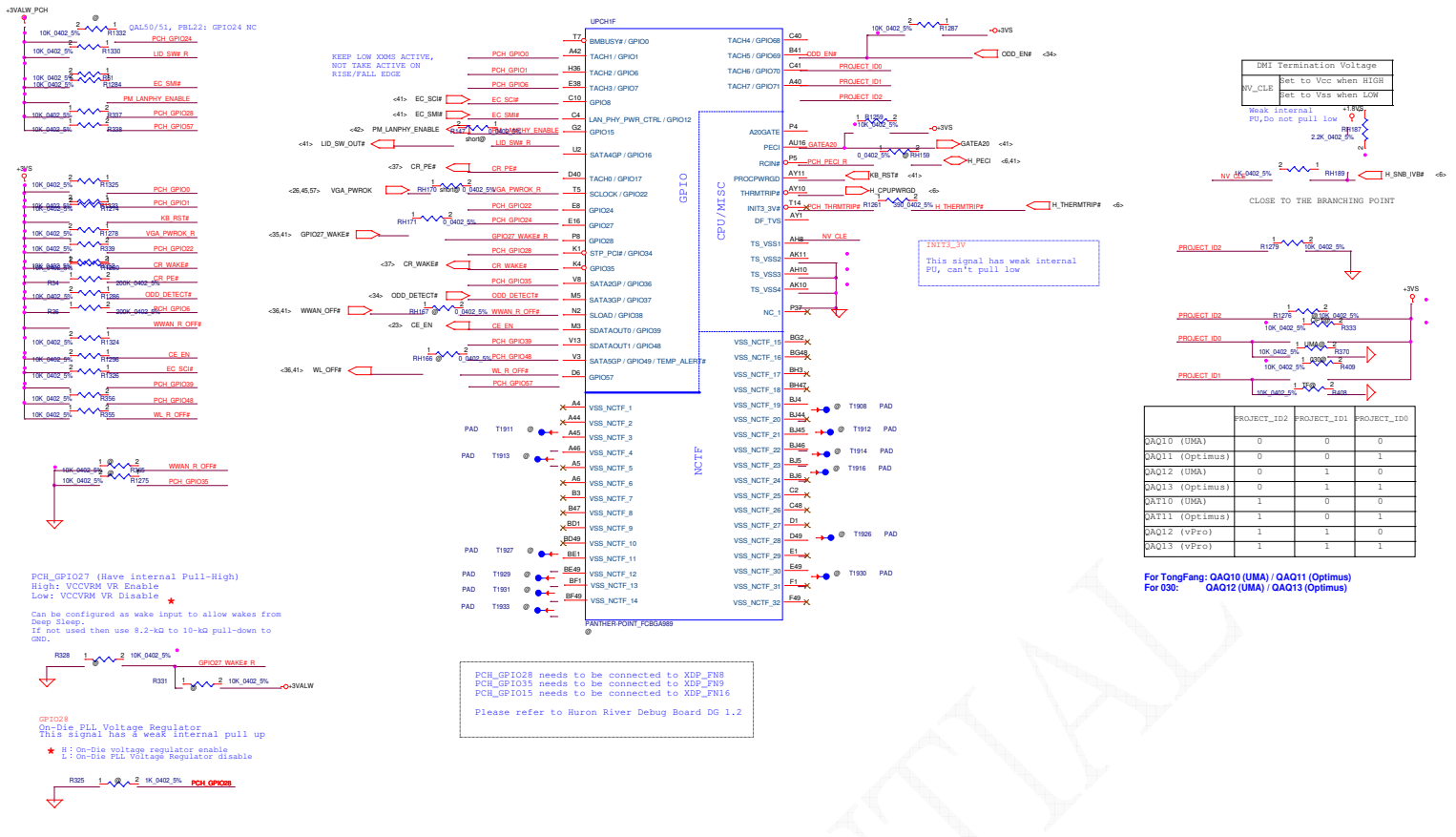
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Date	Friday, August 24, 2012		Sheet	24 of 60	









PCB_GPIO127 (Have internal Pull-High)
High: VCCVRM VR Enable
Low: VCCVRM VR Disable

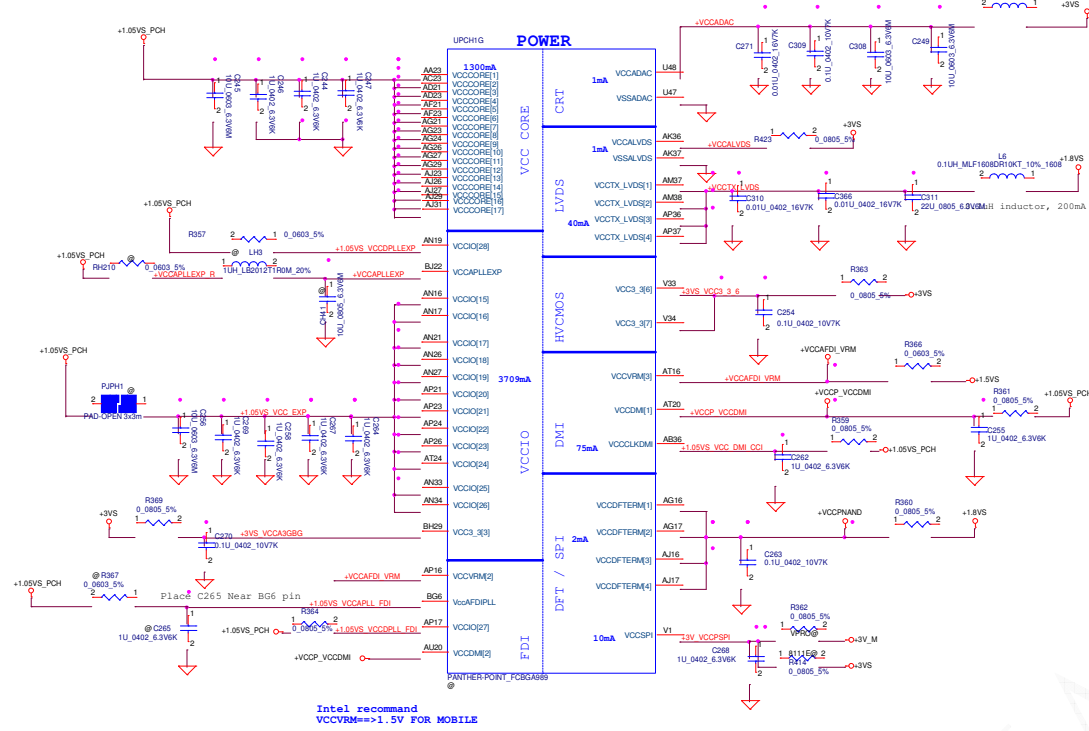
Can be configured as wake input to allow wakes from Deep Sleep.
If not used then use 8.2-kΩ to 10-kΩ pull-down to GND.

PCB_GPIO28 needs to be connected to XDP_FN8
PCB_GPIO35 needs to be connected to XDP_FN9
PCB_GPIO105 needs to be connected to XDP_FN16
Please refer to Huron River Debug Board DG 1.2

	PROJECT_ID0	PROJECT_ID1	PROJECT_ID2
QAQ10 (UMA)	0	0	0
QAQ11 (Optimus)	0	0	1
QAQ12 (UMA)	0	1	0
QAQ13 (Optimus)	0	1	1
DAT10 (UMA)	1	0	0
DAT11 (Optimus)	1	0	1
QAQ12 (vPro)	1	1	0
QAQ13 (vPro)	1	1	1

For TongFang: QAQ10 (UMA) QAQ11 (Optimus)
For O30: QAQ12 (UMA) QAQ13 (Optimus)

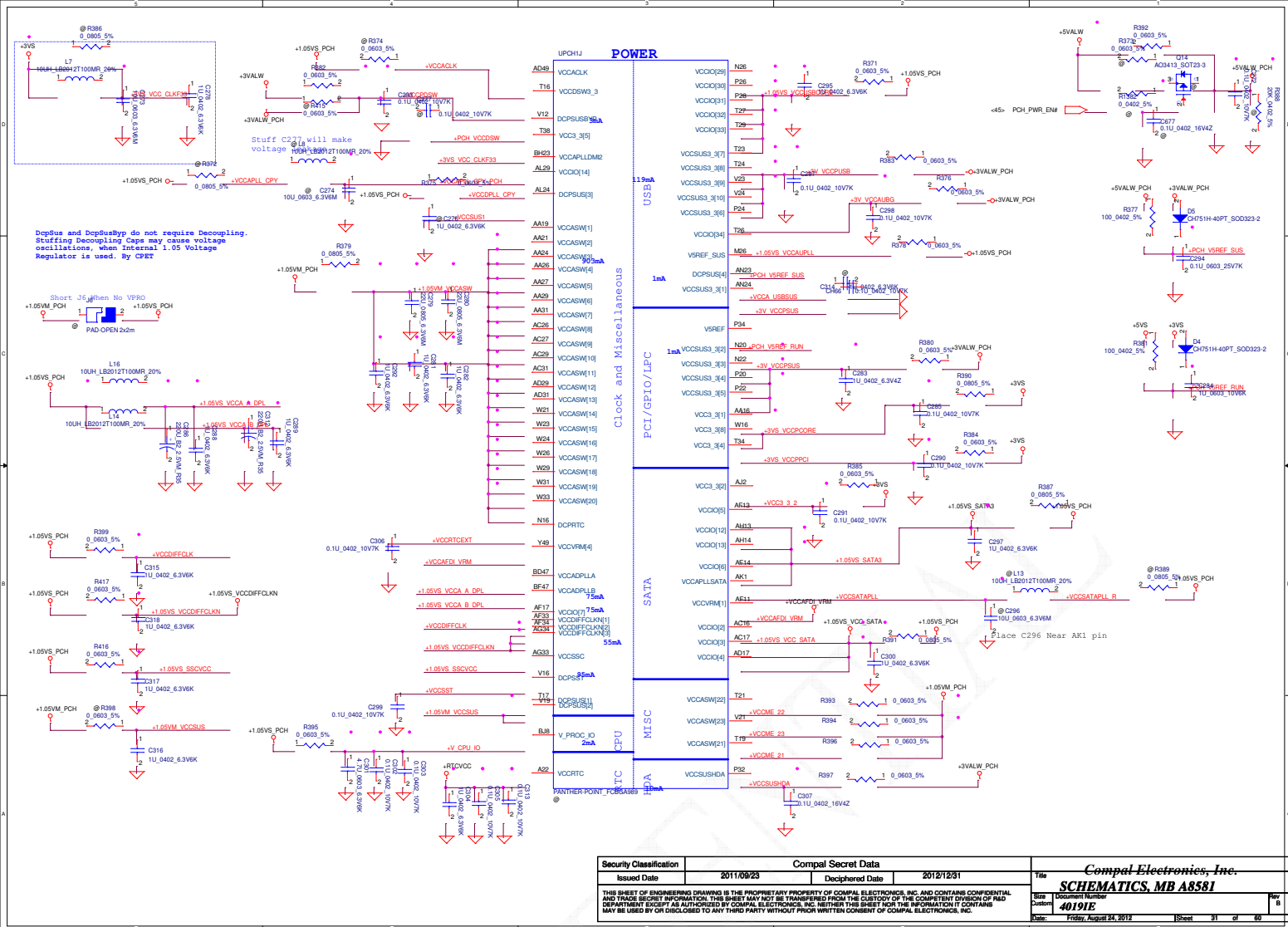
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File				Compal Electronics, Inc.	
Schematic				SCHEMATICS, MB A8581	
Doc No				40191E	
Date				2012/08/24/2013	
Sheet				28 of 66	



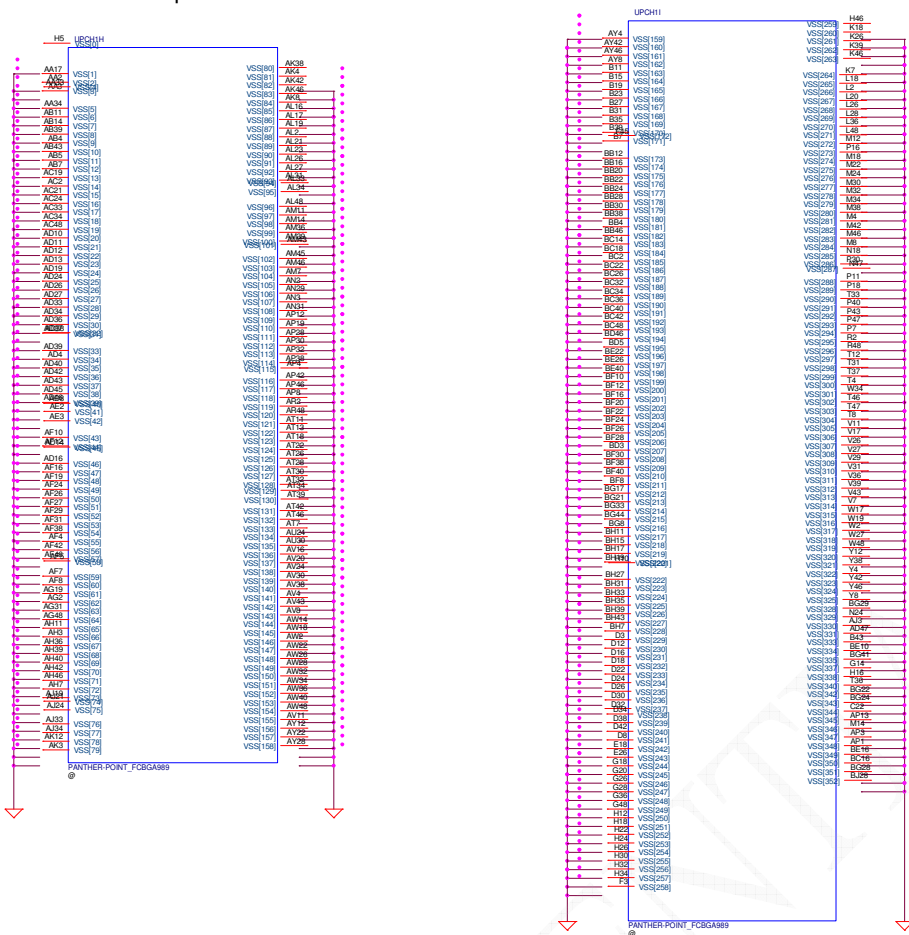
Intel recommend
VCCVRM>=1.5V FOR MOBILE

PCH Power Rail Table Refer to PCH EDS R1.5		
Voltage Rail	Voltage	SO Iccmax Current (A)
V_PROC_IO	1.05/1.0	0.002
V5REF	5	0.001
V5REF_Bus	5	0.001
Vcc3_3	3.3	0.178
VccADAC	3.3	0.063
VccADPLL	1.05	0.075
VccADPLL	1.05	0.075
VccCore	1.05	1.73
VccDMI	1.1	0.047
VccIO	1.05	3.799
VccASH	1.05	0.803
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	N/A
VccBus3_3	3.3	0.065
VccBusHDA	3.3	0.01
VccVRM	1.5	0.147
VccCLKDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.050
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

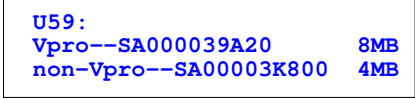
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				Date	Friday, August 24, 2012
				Sheet	30 of 35



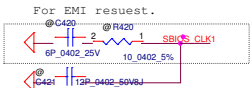
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				Issue Date	Friday, April 04, 2013	Sheet 91 of 60



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				40191E	Rev B
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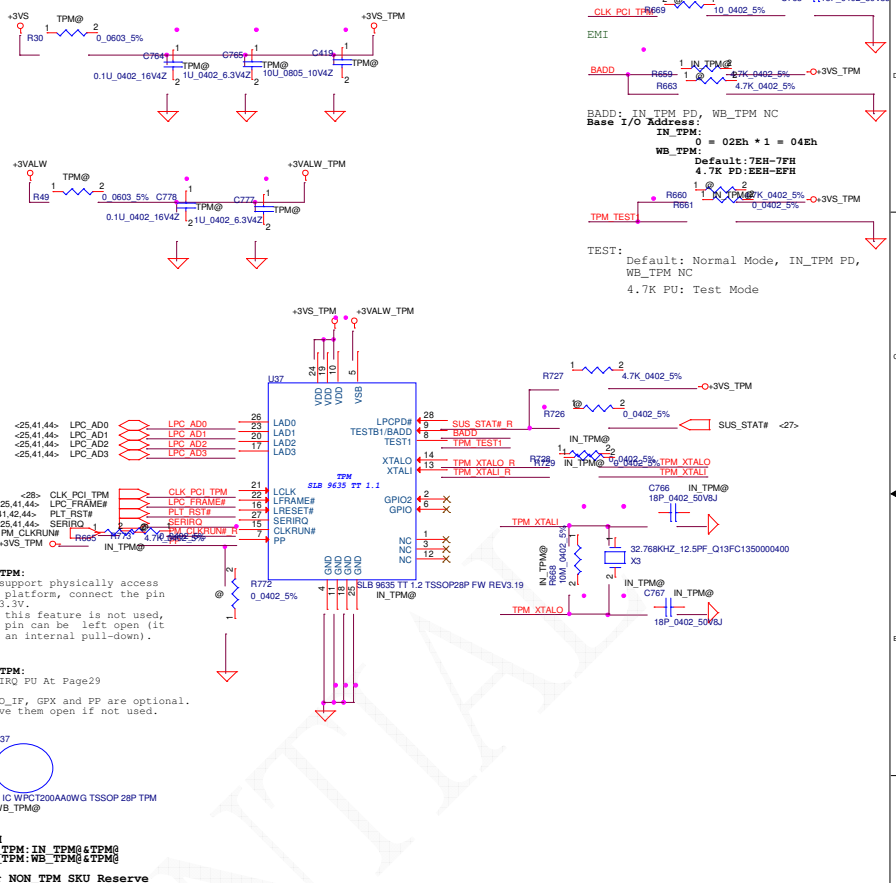


BIOS SPI Flash (2MByte*1) For Win8



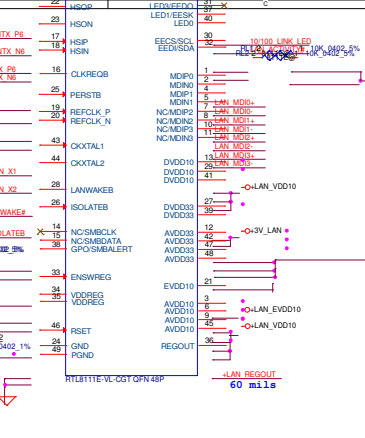
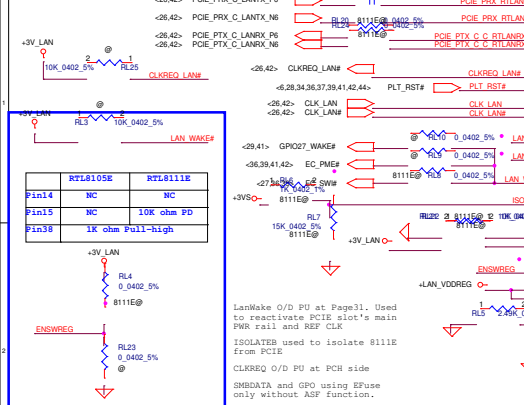
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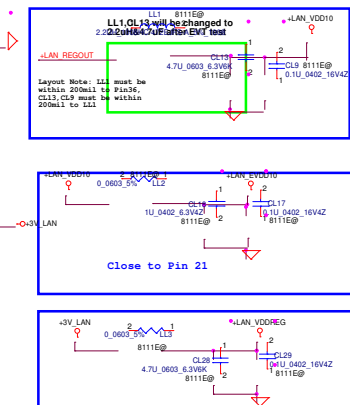


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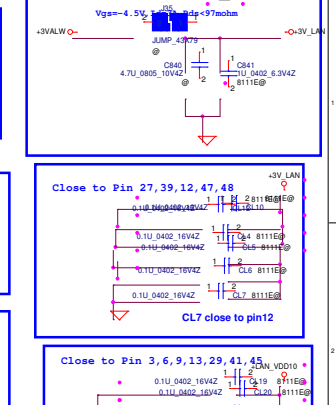
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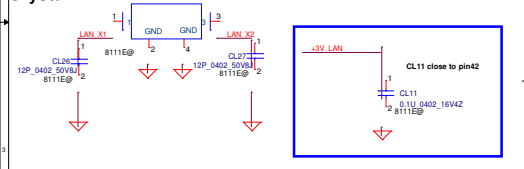
PWF



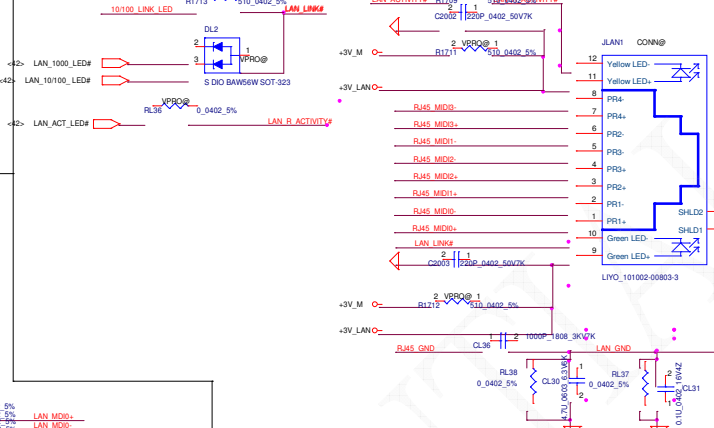
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	+3VALW TO +3V_LAN	



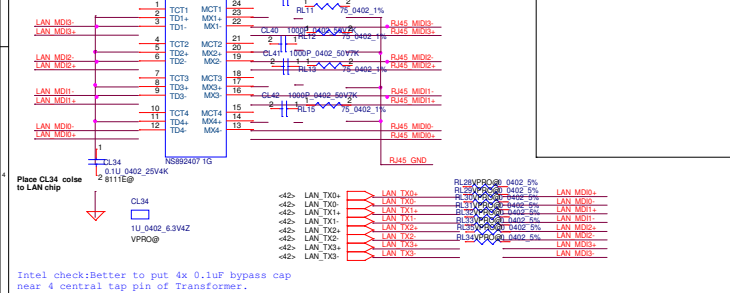
Crystal



LAN Conn.



Transformer

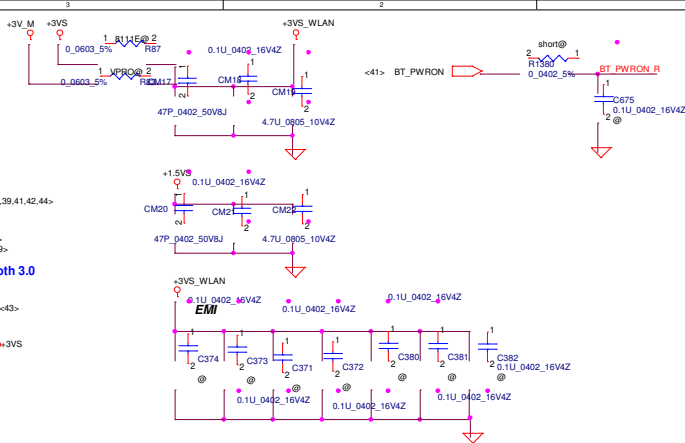


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Date:	Friday, August 24, 2012		Sheet	35 of 60	

Intel check: Better to put 4x 0.1uF bypass cap near 4 central tap pin of Transformer.

Vpro SKU: please delete E51_TXD_R /RXD connection on JMINI1.

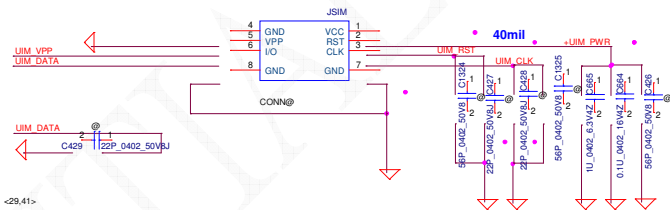


D19 @
CM1293-04S0 SOT23-6

UIM_DATA 1 CH1 CH4 4 UIM_VPP

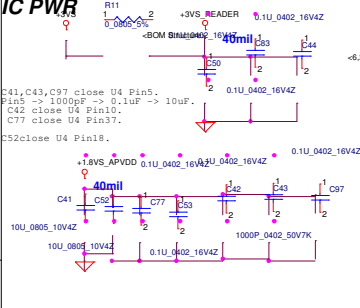
2 CH2 CH3 5 UIM_PWR

UIM_CLK 3 CH2 CH3 6 UIM_RST

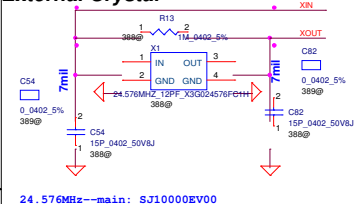


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Date:	Friday, August 24, 2012	Sheet	36	of	60

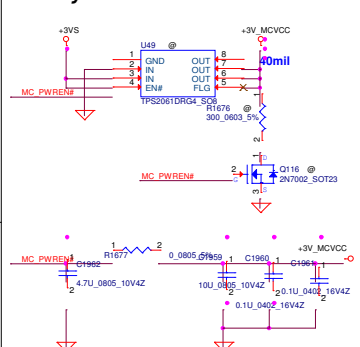
IC PWR R11



External Crystal



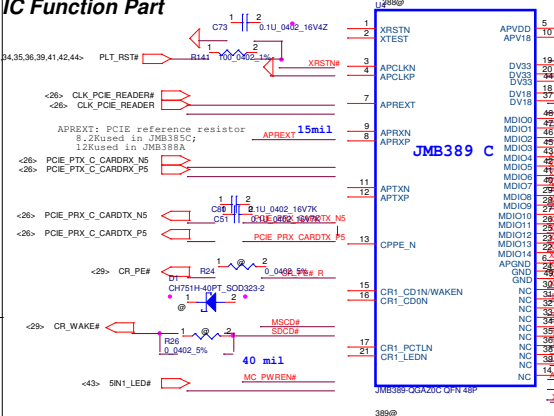
Memory Card Power



Note:

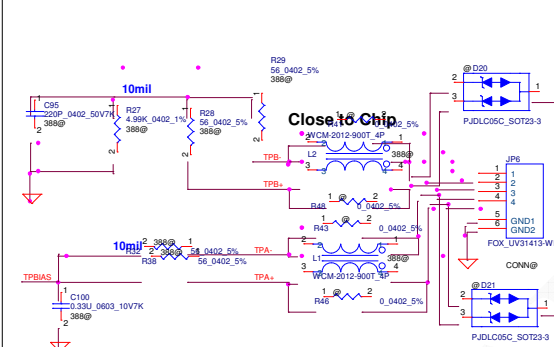
- if use external PWR and change +3V_MCPWR as control signal, Need BIOS to change the Setting.

IC Function Part

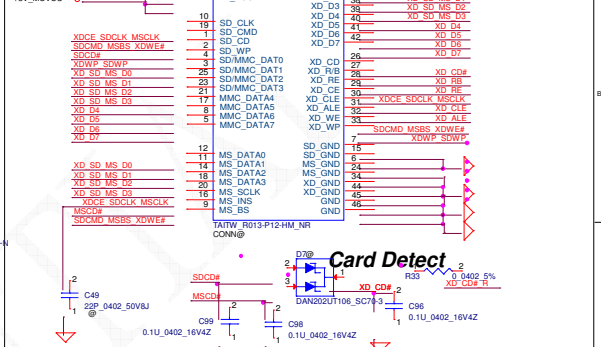


Note:
Colay With JMB385; W/1394, mount JMB388;WO/1394, mount JMB385.
CR PE# and CR WAKE reserve for D3 mode

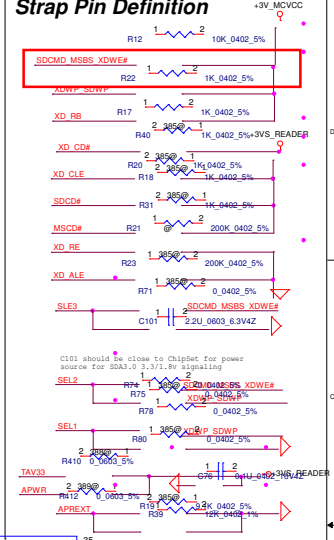
1394 Conn



7 IN 1 Conn

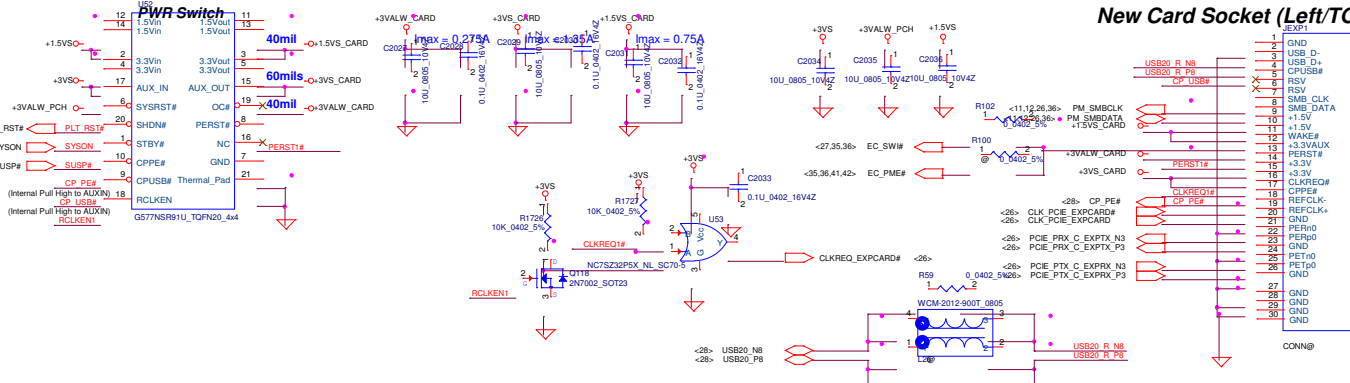


Strap Pin Definition



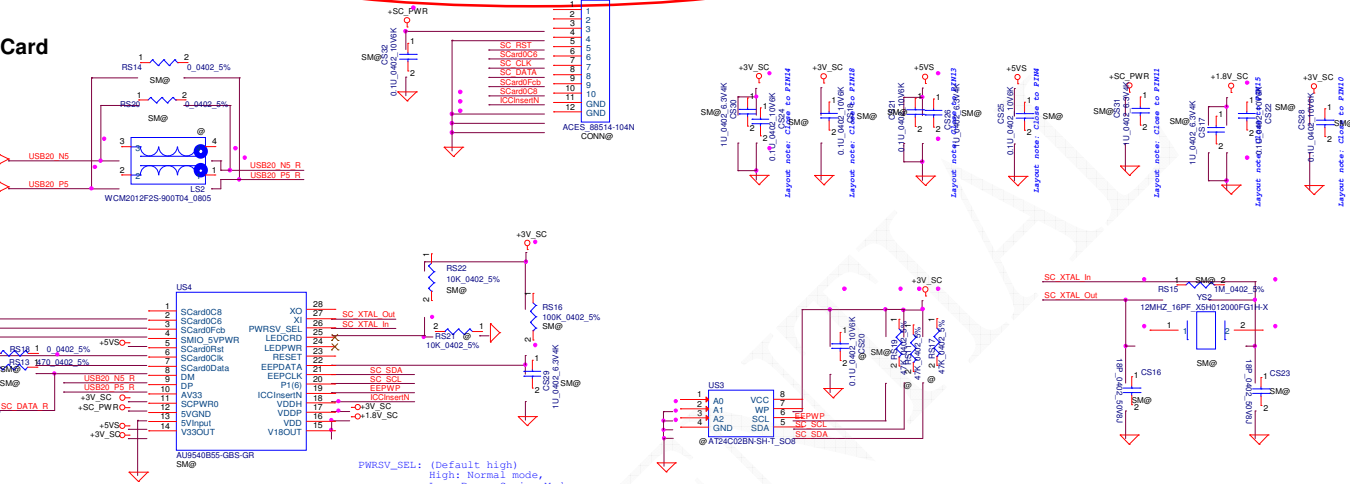
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			Date:	Friday, August 24, 2012
			Sheet:	37 of 60

(Left/TOP)



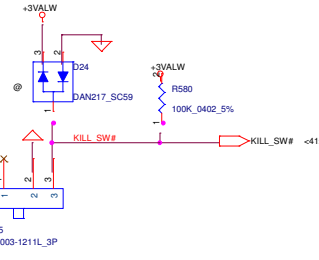
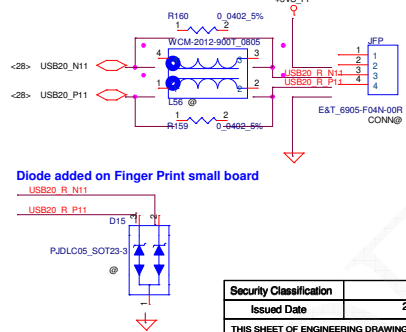
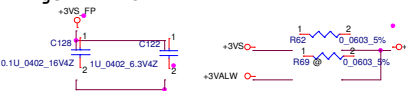
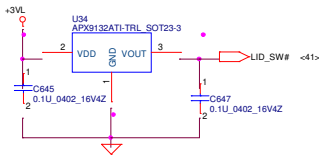
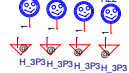
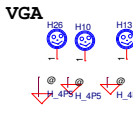
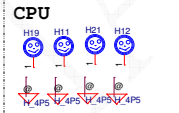
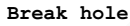
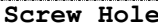
This pin1 define need check

Smart Card

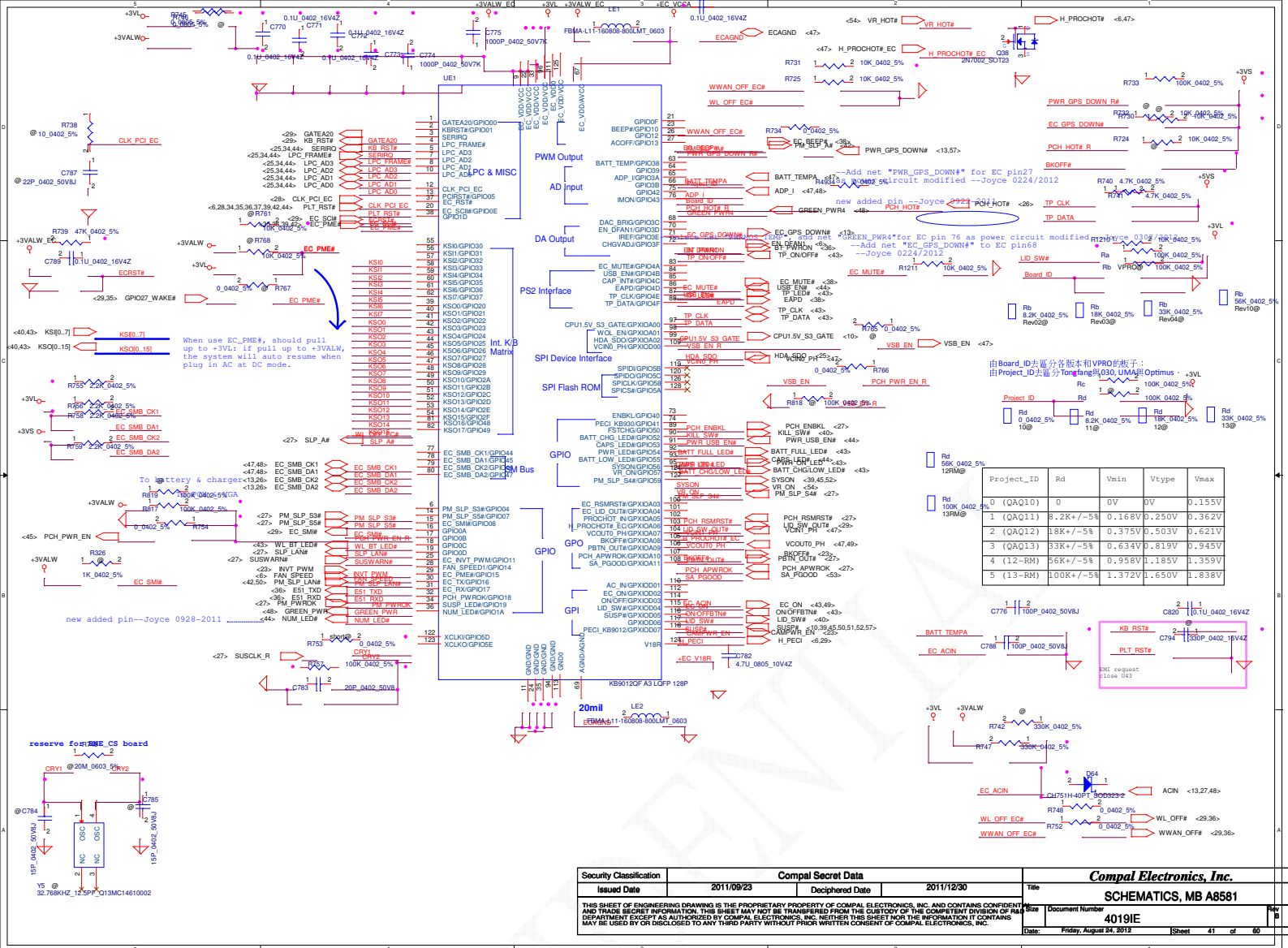


MP: to solve issue of "Smart Card also show in Device Manager after plug out it", change US4 from SA000042100 to SA000042110.

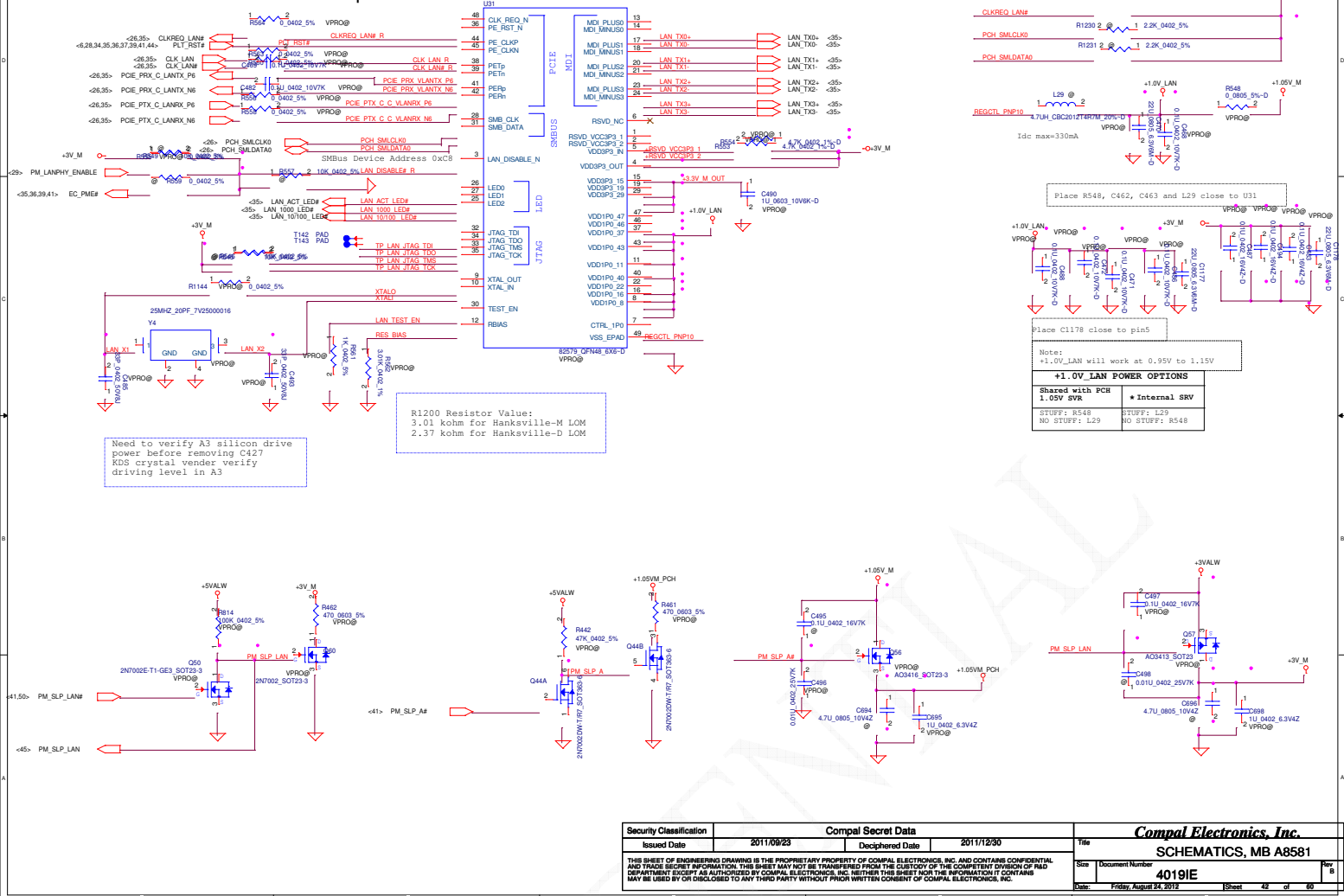
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Size Document Number 4019IE			Date Edition 4.0 Revision 50 of 20	



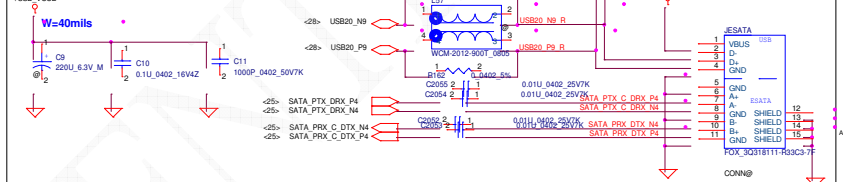
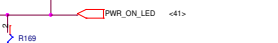
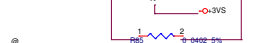
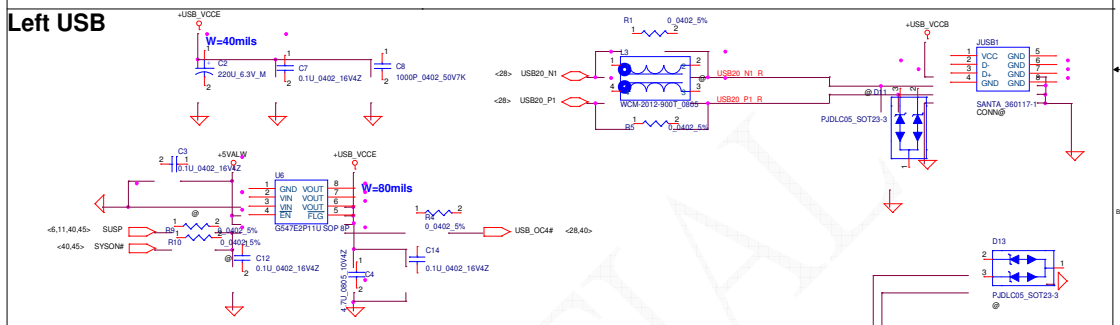
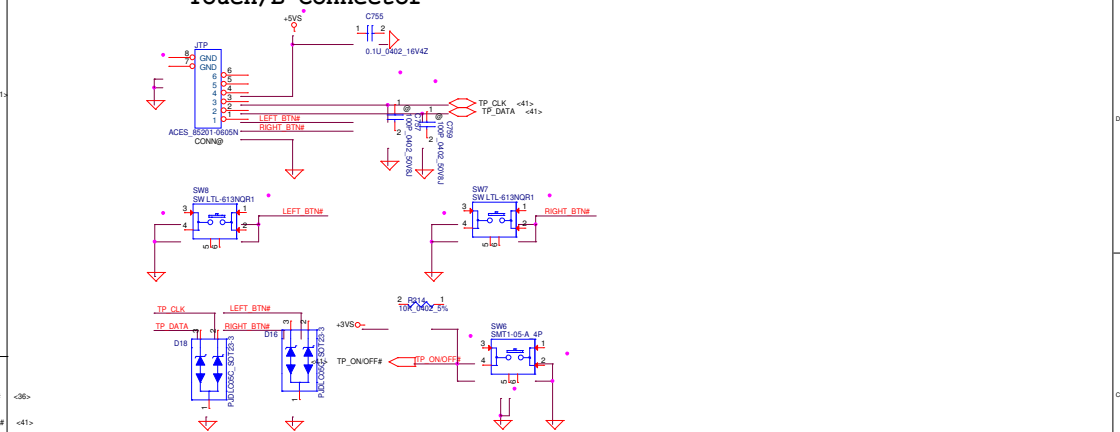
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				40191E	
Date:	Friday, August 31, 2012	Sheet	40 of 60		



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4019IE		Date		Friday, August 24, 2012	
Sheet		41		of 60	



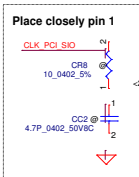
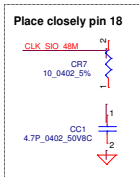
Touch/B Connector



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				Date:	Friday, August 14, 2012
				Sheet	43 of 60

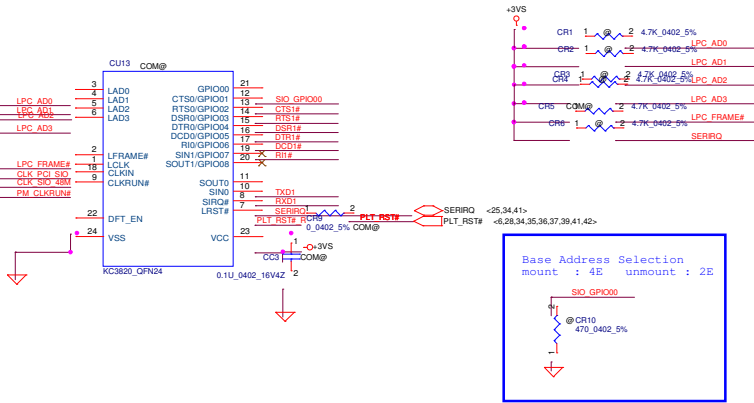
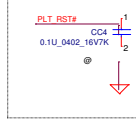
EMI And ESD

Reserve R199,C207,R226,C208 <EMI> 0601

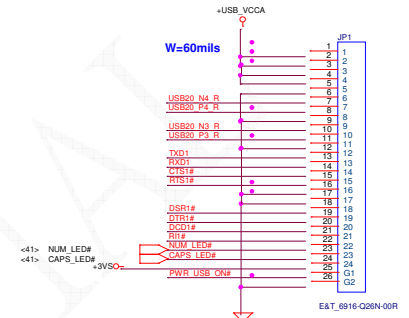
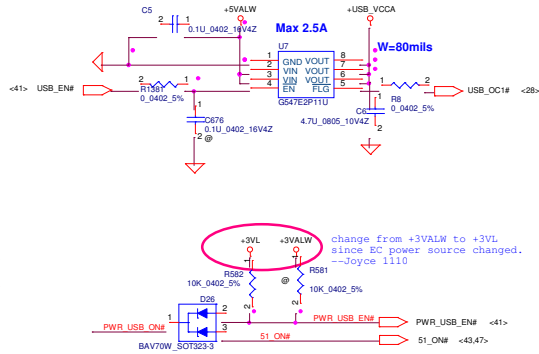
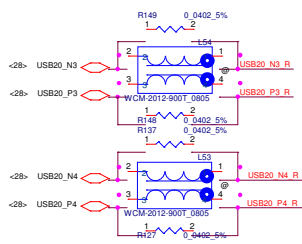


Add CR7,CC1 for EMI test fail issue--0929-2011

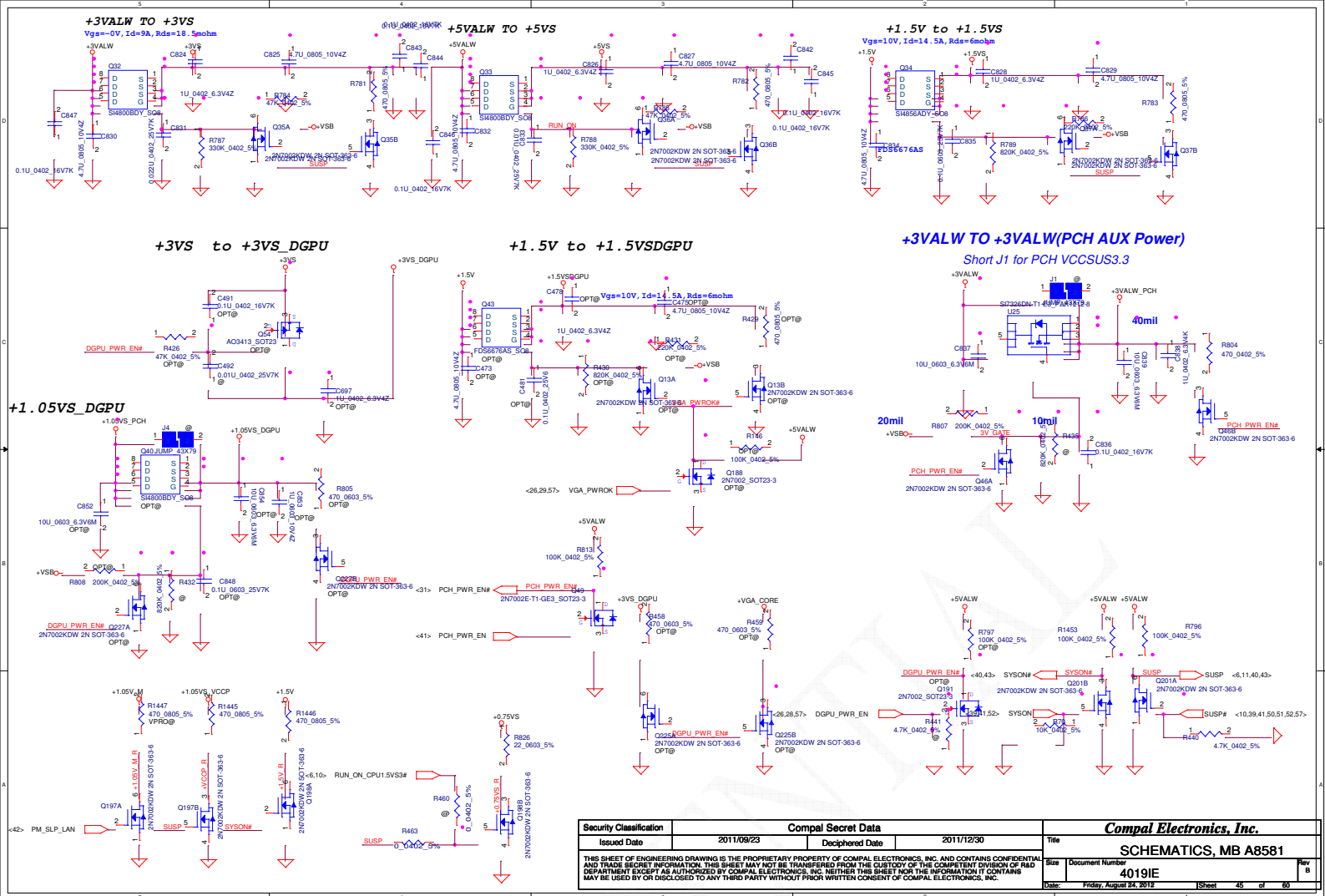
Reserve C292 for SIO_RST# <ESD> 0608

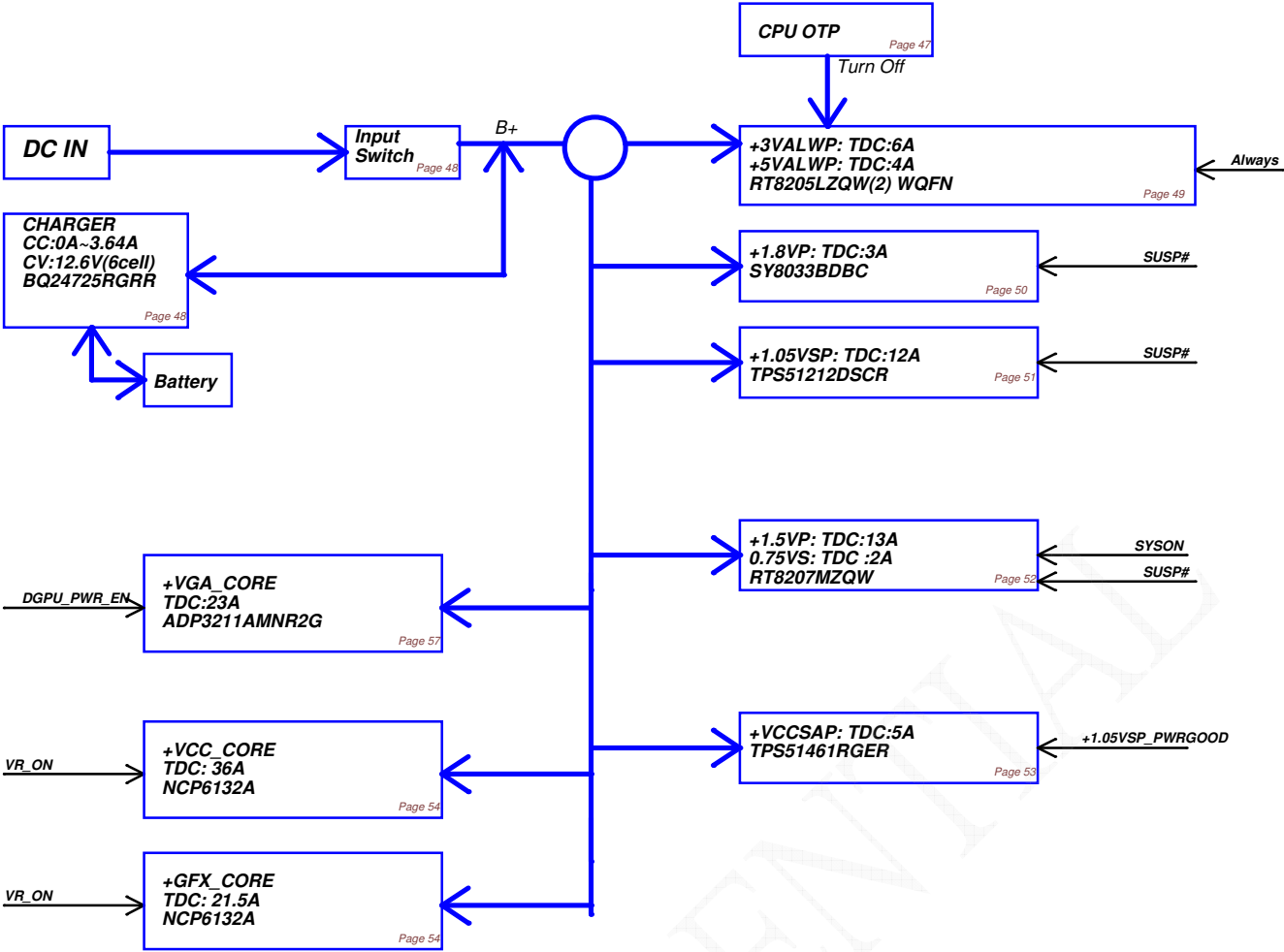


PWR USB



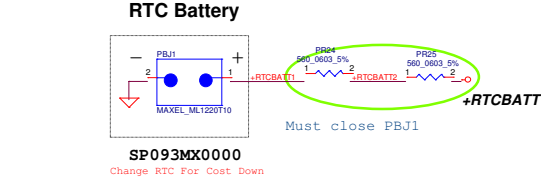
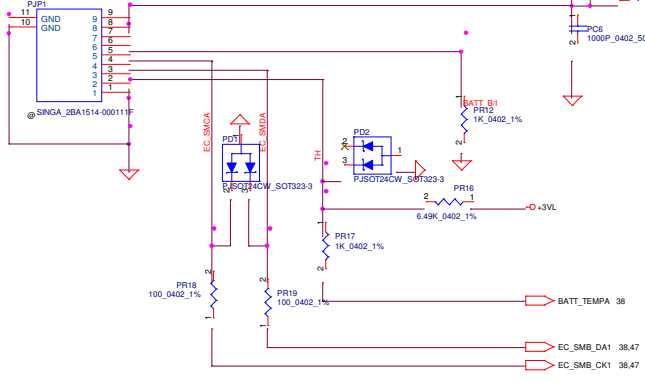
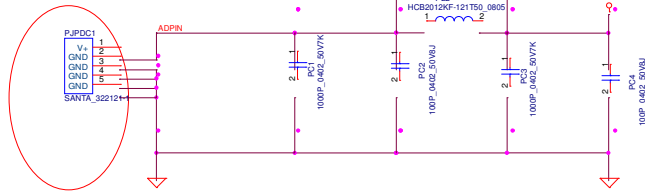
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Size	Document Number	4019IE	File	Friday, August 24, 2012
Sheet 44 of 60				



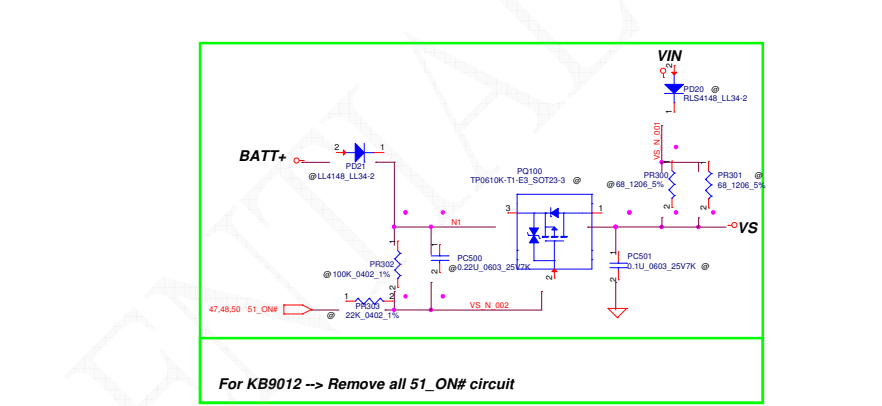
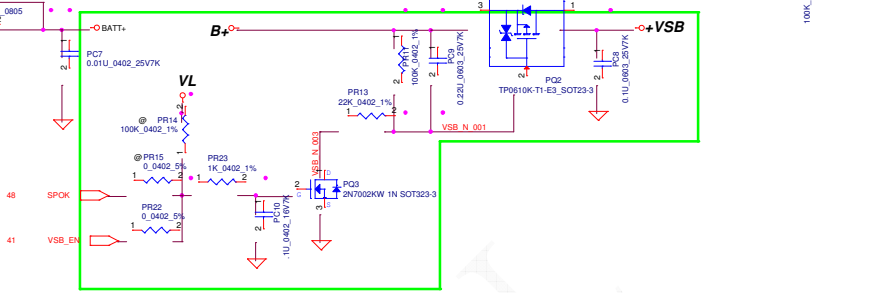
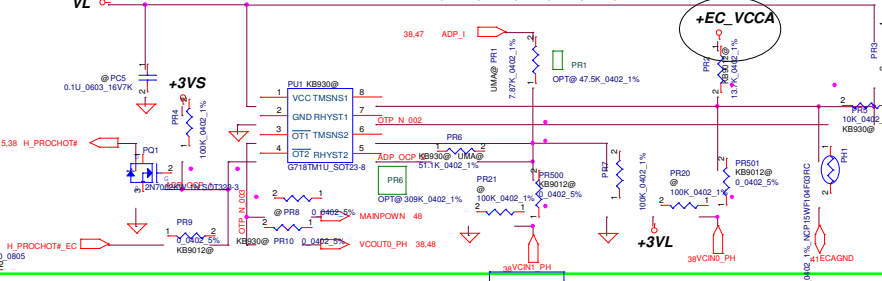


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				Revision	40191E
				Date	Friday, August 24, 2012
				Sheet	46 of 60

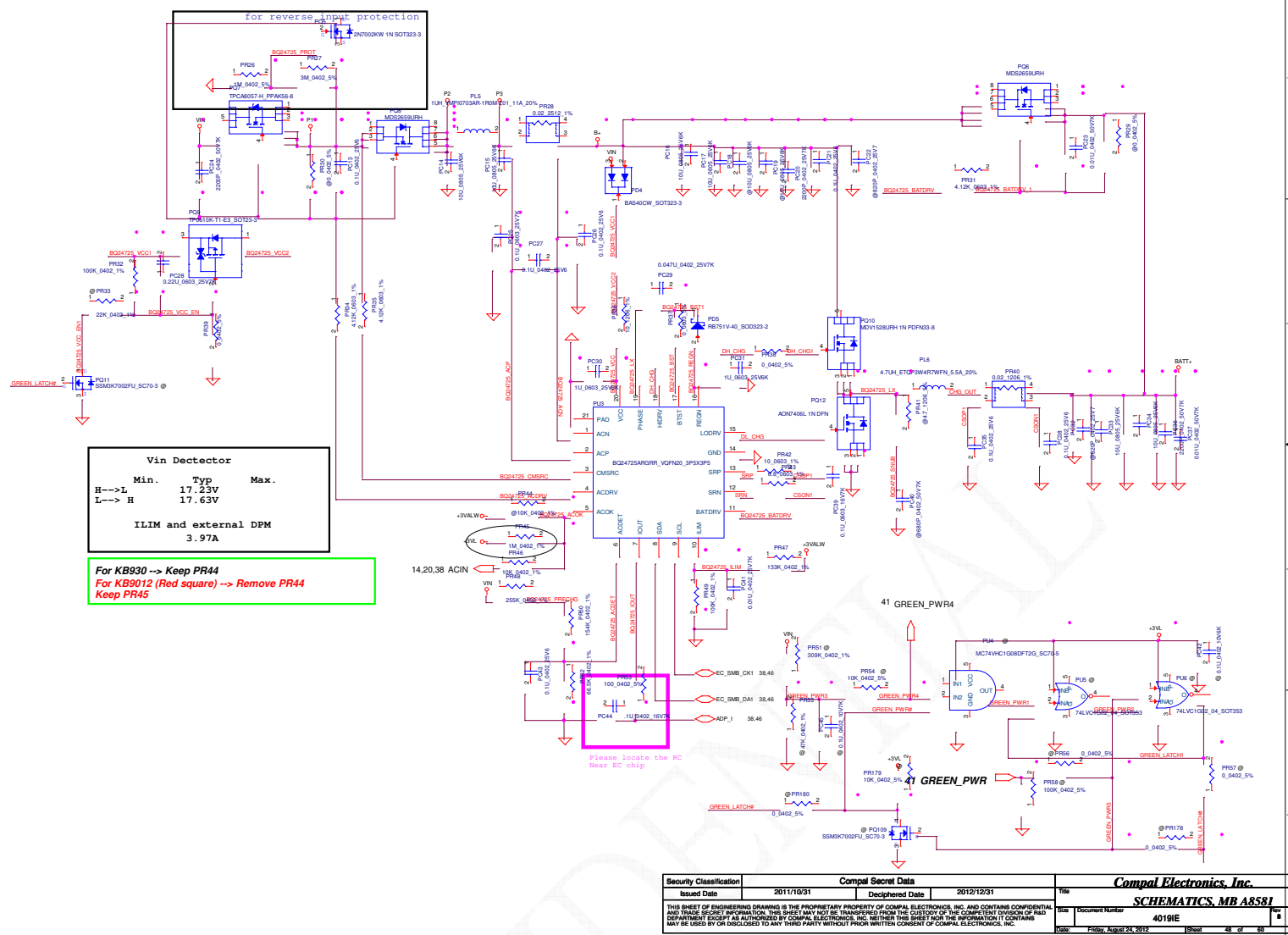
DCIN jack P/N:DC301008L00,
need doble confirm P/N with ME



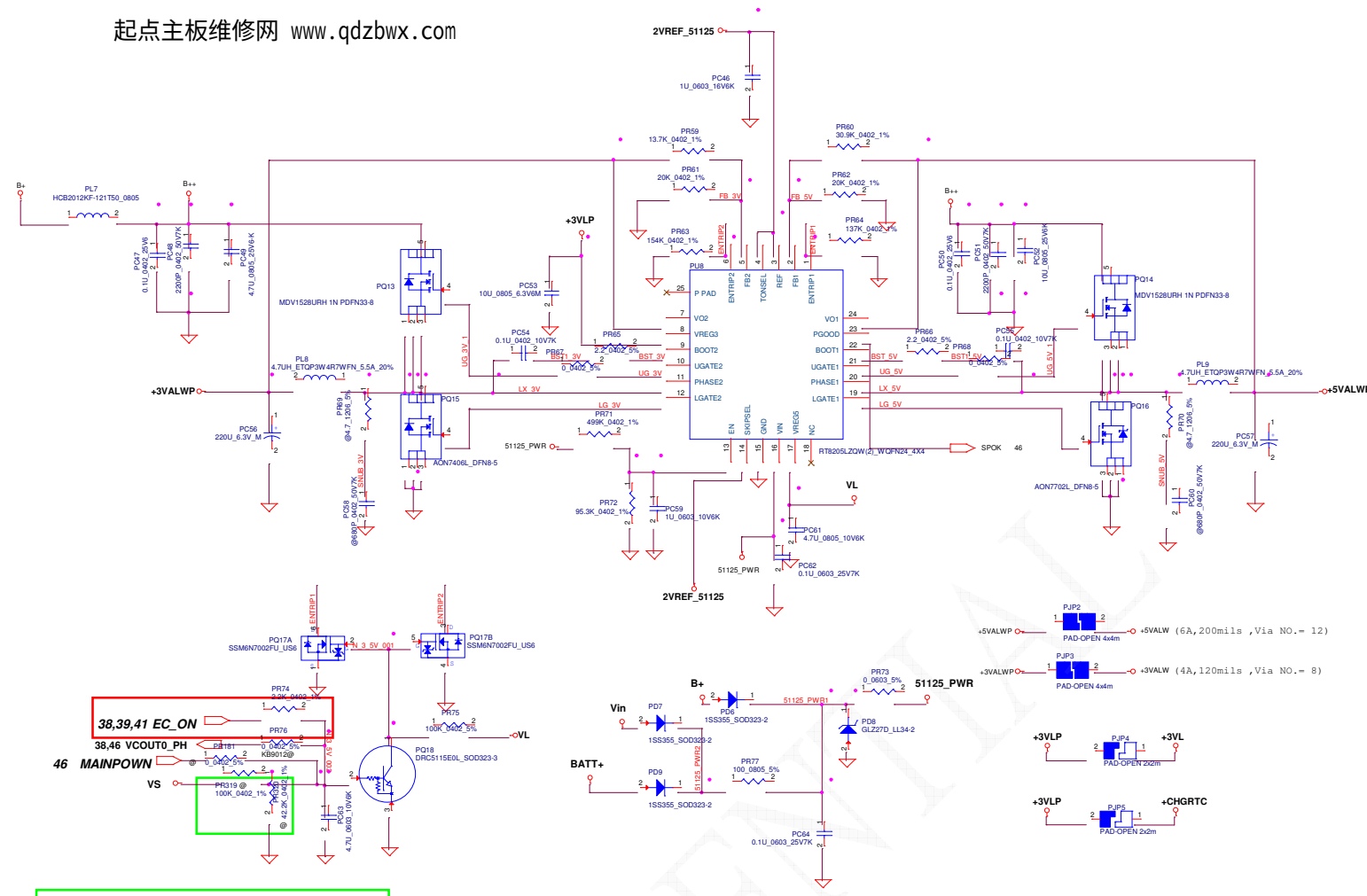
PH1 under CPU bottom side :
CPU thermal protection at 93 +3 degree C
Recovery at 56 +3 degree C



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				Date	Friday, August 24, 2012
				Sheet	47 of 60

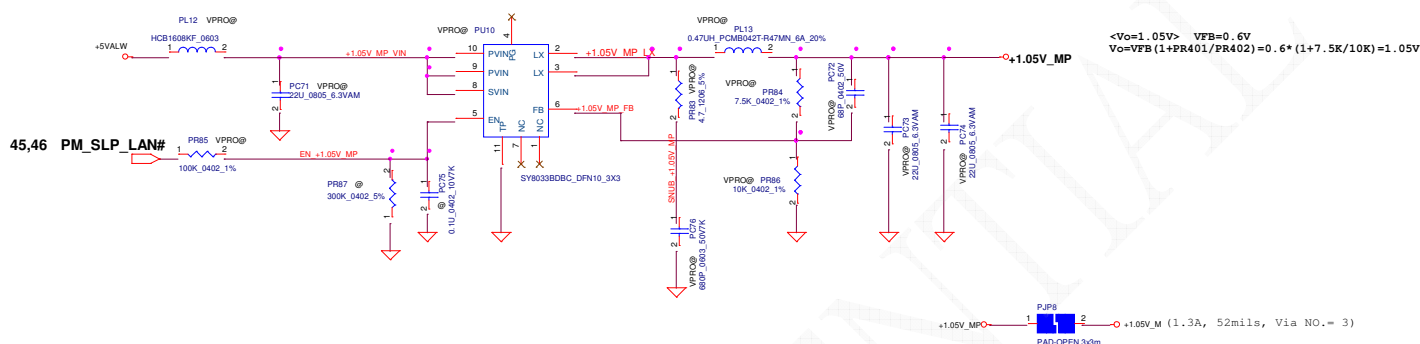
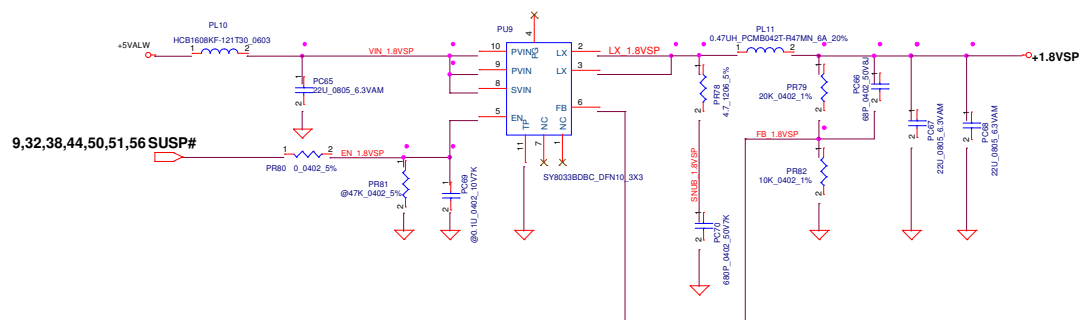


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Date:	Friday, August 24, 2012	Sheet	48	of 68

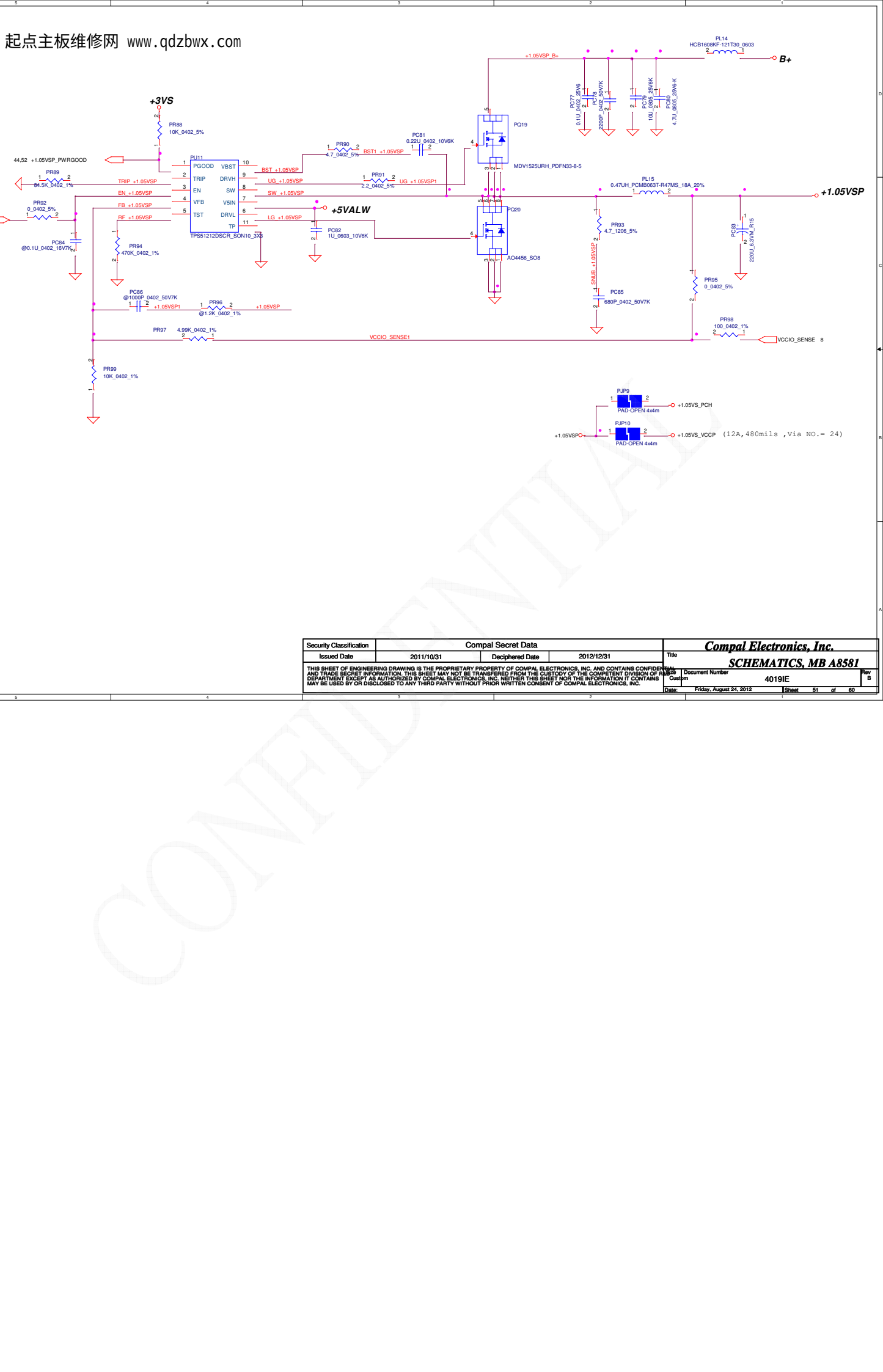


For KB930 --> Keep PR319, Remove PR74
 For KB9012 (Red square) --> Remove PR319
 Keep PR74

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				Justified	4019IE
				Date	Friday, August 24, 2012
				Sheet	49 of 60



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Date				Volume	1
File: 4019E_A8581_2012				Sheet	50 of 50



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The schematic diagram illustrates the power management section of a motherboard, specifically focusing on the +3VS, +5VALW, and +1.05VSP rails. Key components include:

- ICs:** U11 (TPS51212DSCR, SON10_3x8), PQ19 (MDV1525URH, PDFN33-8-5), PQ20 (A04456, SO8), and U10 (L6920, SON8).
- Resistors:** PR88 (10K, 0402_5%), PR89 (84.5K, 0402_1%), PR90 (4.7, 0402_5%), PR91 (2.2, 0402_5%), PR92 (0.0402_5%), PR93 (4.7, 1206_5%), PR94 (470K, 0402_1%), PR95 (0.0402_5%), PR96 (1, 0402_1%), PR97 (4.99K, 0402_1%), PR98 (100, 0402_1%), PR99 (10K, 0402_1%), and PR100 (100, 0402_1%).
- Capacitors:** PC81 (0.22U, 0402_10V6K), PC82 (1U, 0803_10V6K), PC84 (0.1U, 0402_16V7K), PC85 (680P, 0402_50V7K), PC86 (1000P, 0402_50V7K), PC87 (0.1U, 0402_25V6), PC88 (220P, 0402_50V7K), PC89 (100, 0402_25V6K), PC90 (4.7U, 0805_25V6-K), and PC91 (220U, 33VW, 1115).
- Inductors:** PL14 (HCB1608KF-121T30_0603) and PL15 (0.47UH, PCMB03T-R47MS_18A_20%).
- Other:** VCCIO_SENSE1, VCCIO_SENSE2, and VCCIO_SENSE3 are shown as sense lines for the +1.05VSP rail.

Table 1: Security Classification

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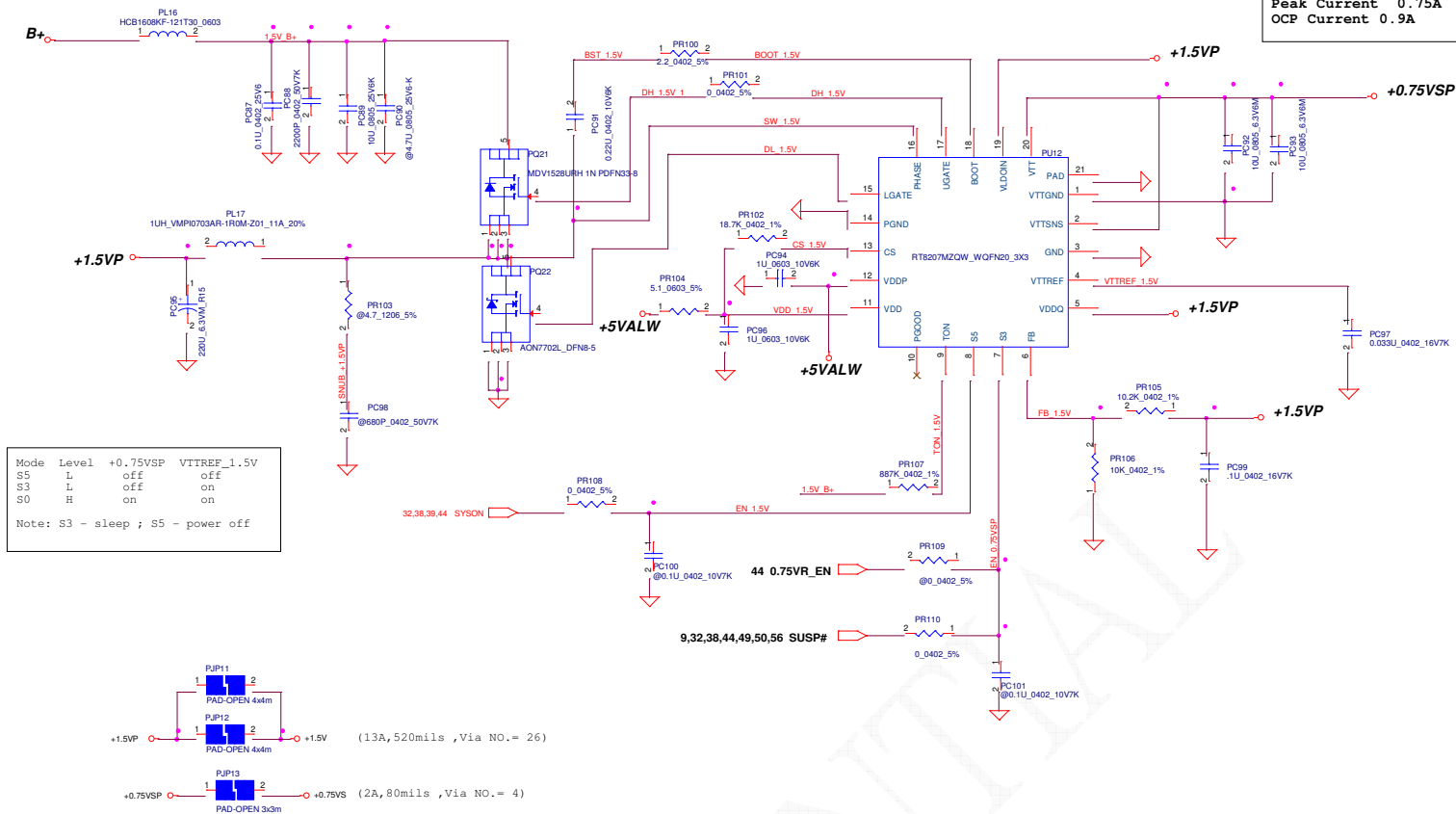
Table 2: Title and Document Information

Title		Document Number	Rev
Compal Electronics, Inc.		40191E	B
SCHEMATICS, MB A8581			

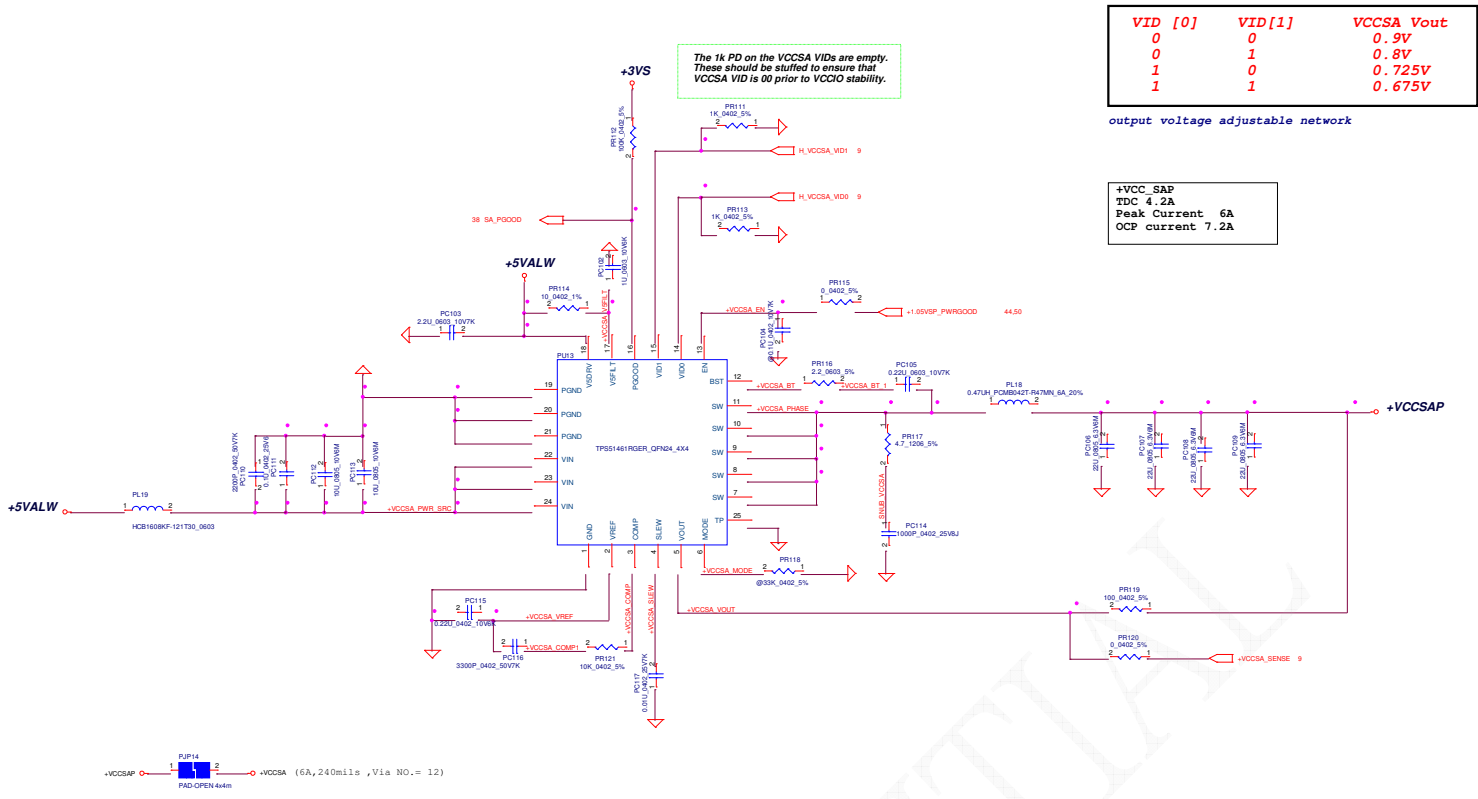
Table 3: Date and Sheet Information

Date	Sheet	of
Friday, August 24, 2012	51	60

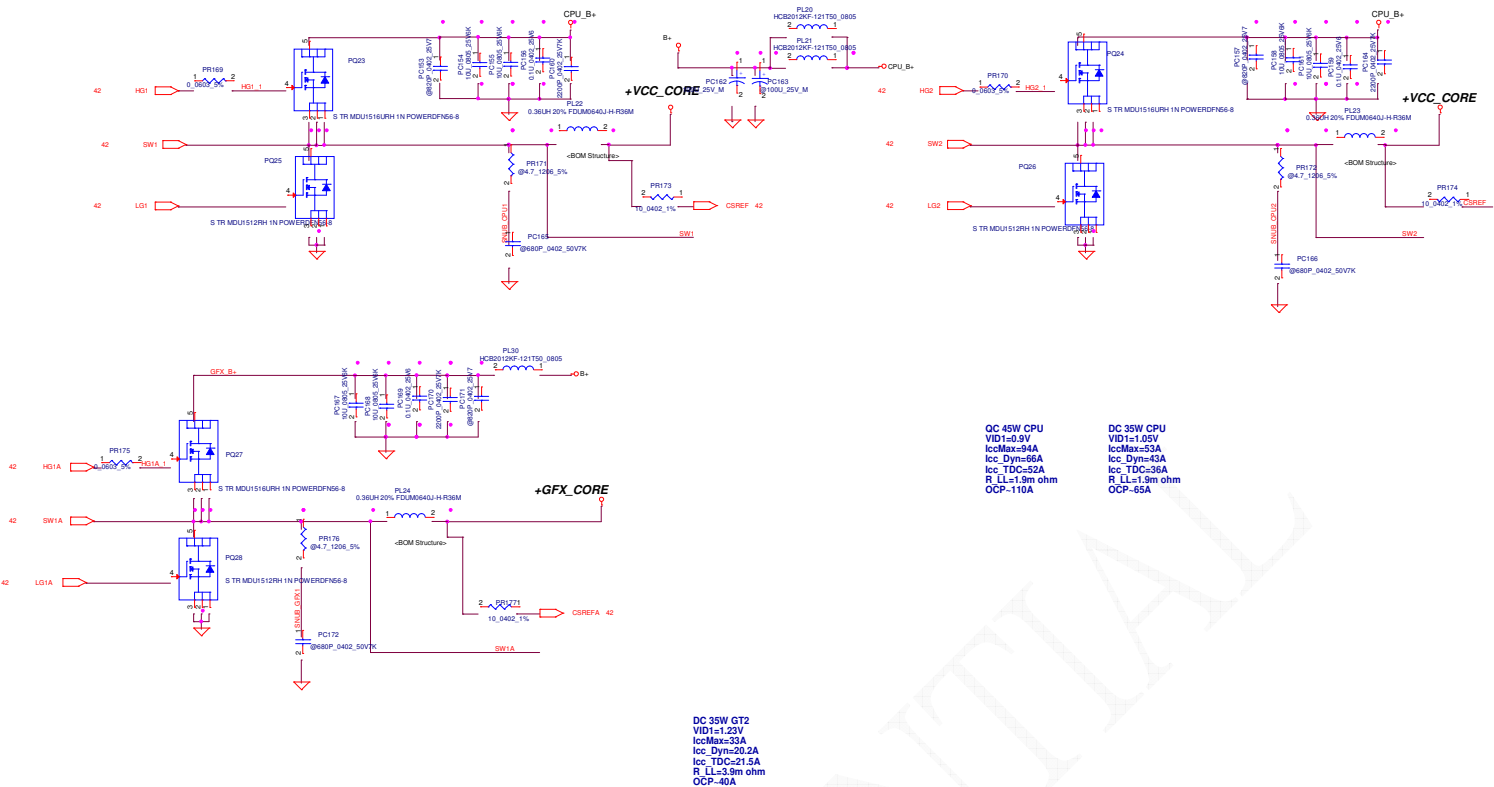
0.75Volt +/- 5%
TDC 0.525A
Peak Current 0.75A
OCP Current 0.9A



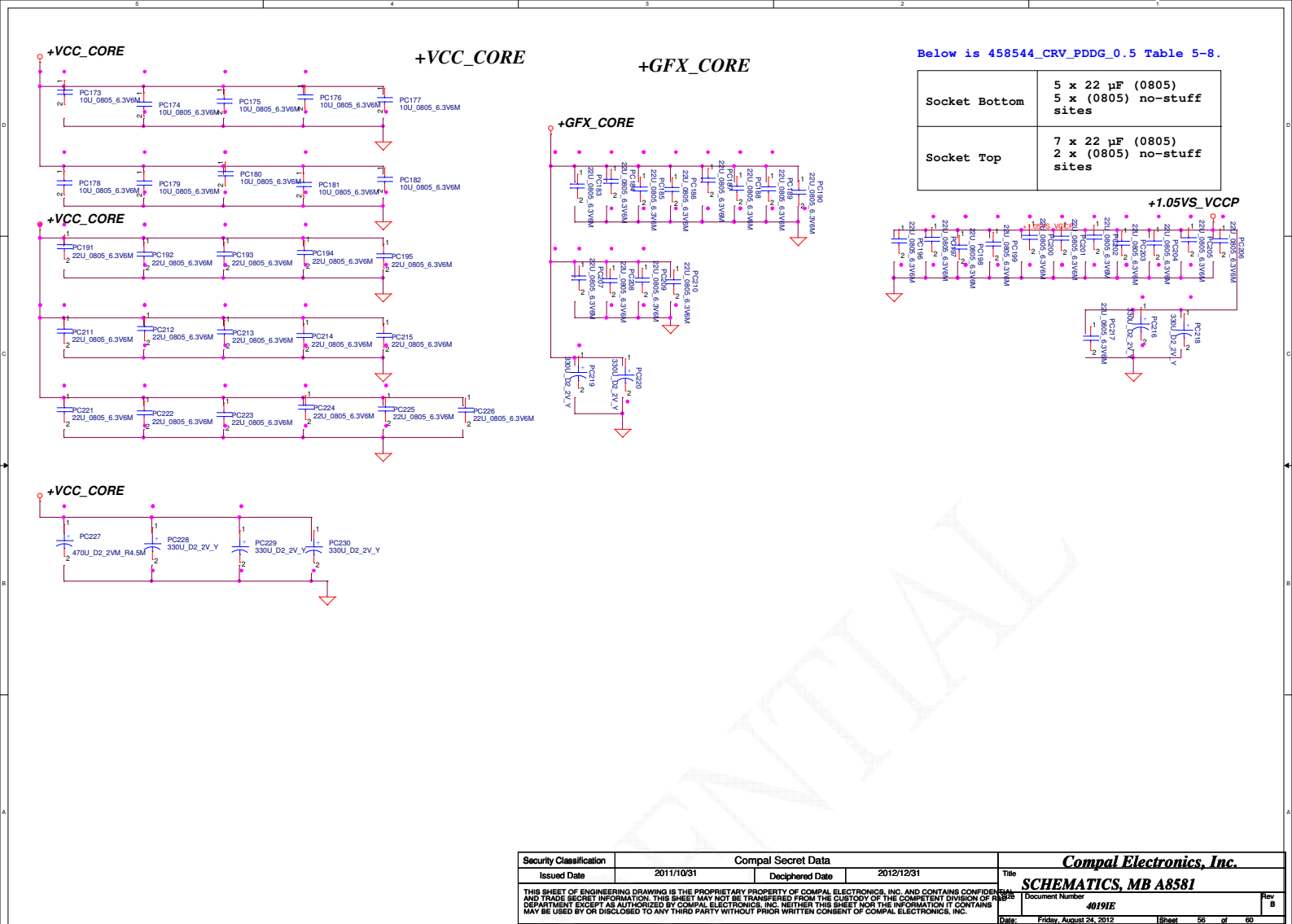
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				Customer	
				Date	Friday, August 24, 2012
				Sheet	52 of 60



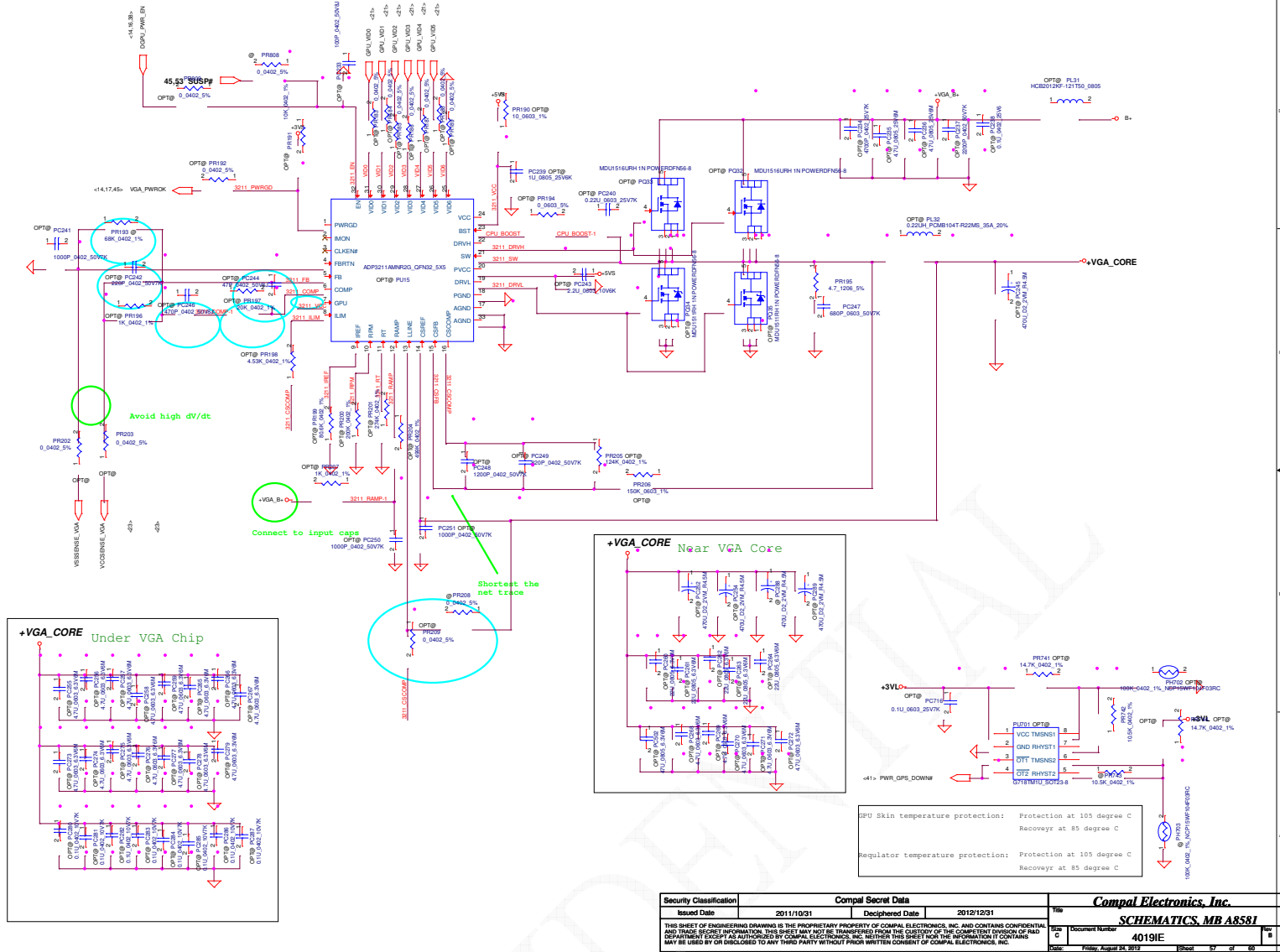
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				Rev	1
				File	Folder, August 24, 2012
				Sheet	53 of 50



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Issued Date	2011/10/31	Deciphered Date	2012/12/31	
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				40191E
				Date: Friday, August 24, 2012 Sheet 55 of 65



Security Classification	Compal Secret Data		Title	
Issued Date	2011/10/31	Deciphered Date	2012/12/31	SCHEMATICS, MB A8581
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Date: Friday, August 24, 2012				Sheet 56 of 60



Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	Page 47		2012/02/24		For DVT can't power on and need to disable EC VCIN0_PH VCINI_PH pin detect	Reserve PR20 PR21 for DVT can't power on issue	PVT
2	Page 57		2012/02/24		3D mark06&3D mark Vantage score don't meet SPEC need to support GPS function	Add PC288 PC289 470U_D2_2VM_R4.5M PC248 1200P_0402_50V7K PR209 0_0402_5% Change PC242 to 220P_0402_50V7K PC246 to 470P_0402_50V8J PC244 to 47P_0402_50V8J PR197 to 20K_0402_1% PR198 to 4.53K_0402_1% PC249 to 820P_0402_50V7K PR205 to 124K_0402_1% PR206 to 150K_D603_1% Delete PR208 0_0402_5%	PVT
3	Page 49		2012/02/24		For DVT SMT PC56, PC57 footprint did not match issue	Change PC56,PC57 footprint from D2 to C_6SVPE220MX	PVT
4	Page 57		2012/02/24		3D mark06&3D mark Vantage score don't meet SPEC need to support GPS function	Reserve GPU Skin and Regulator temperature protection circuit for if temperature over spec issue Add PC716 SD042104K80 0.1U_0603_25V7K PR741,PR744 SD034147280 14.7K_0402_1% PR742 SD034105280 10.5K_0402_1% PH702 SL200000U00 100K_0402_1%_NCP15WF104F03RC	PVT
5	Page 47		2012/02/24		Change PH1 protect action to EC	Change PH1 pull high vcc from +3VL to +EC_VACC Change PH1 GND from normal GND to EC_AGND	PVT
6	Page 48		2012/02/27		Update Green power Circuit	Delete PU7 741VC1G17GW TSSOP and change to PQ109 SSM3K7002FU_SC70-3 Add PR10 0_0402_5% to connect GREEN_LATCH# Reserve PR178 0_0402_5%	PVT
7	Page 48		2012/03/02		Update Green power Circuit	Connect the Green_PWR4 net to EC GPIO for AC decete for Green power circuit ACOR will drop once time issue	PVT
8	Page 47		2012/03/06		Add one control signal in order to disable B+ to VSB circuit in AC S5 for LOT6 system little than 0.5W issue	Reserve PR22 to add VSB_EN	PVT
9	Page 47 49		2012/03/06		For System can power on immediately after HW shutdown	Change PU1.3 output name from EN0 to MAINPOWN Dis-connect EN0 to PU8.13 Connect MAINPOWN to PQ18.2	
10	Page 47		2012/04/23		For EU Erp lot6 fail, need to cut off +VSB when system at S5	Add PR22, delete PR14,PR15	Pre_MP
11	Page 47 48,50,51 52,53,54 57		2012/04/23		Change to new footprint	ChangePR56,PR80,PR92,PR95,PR108,PR110,PR115,PR120,PR142,PR144,PR183,PR184,PR185,PR186,PR187,PR188,PR189,PR192,PR809 footprint from R_0402 to R0402_0ohm	Pre_MP

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Size		Document Number		40191E
Date		Friday, August 24, 2012		Sheet 58 of 60

QAA1x HW PIR from EVT to DVT LA-8581P REV:0.1 -> 0.2 <2011.12.05~2012.01.02. >

Rev	Item	Date	Impact	Page	Change Cause	Modify Description
0.2	1	12/05	Circuit, Layout, BOM	37	Sourcer require to change crystal to small size.	Change X1 from "SJ100009A00" to "SJ10000EV00"
	2	12/21	Circuit, Layout	41	EVT can't power on issue.	Change R739 pull up power source from "+3VALW" to "+3VALW_EC".
	3	12/21	Circuit, Layout	26,35,42,36	Vpro require PCIE port1 can't connect to LAN.	Swap PCH PCIE port1 and port5.
	4	12/21	Circuit, BOM	43	SW7, SW8 part number error.	change SW7,SW8 part number to "SN100005G00"
	5	12/21	BOM	27	just reserve pull up resistor for SLP_LAN#.	Add @ to R282.
	6	12/26	BOM	34	TPM IC FW update from FW3.16 to FW3.19.	Change U37 from "SA00000GG40" to "SA00000GG70".
	7	12/26	Circuit, BOM	33	Add Vpro & non-Vpro WIN8 BIOS ROM power source selection.	Add R421, R422.
	8	01/05	BOM	40, 43	issue: redetect USB HDD when resume from S3.	Add @ to RU27, delete @ to R90; add @ to R9, delete @ to R10.
	9	01/05	BOM	41	Board ID issue	Add "Rev02@", "Rev03@", "Rev04@", "Rev10@" serial Rb to distinguish the boards.
	10	01/09	Circuit, layout	40	LID_SW# will cause system can't power on at DC mode if use +3VALW, not +3VL.	Change U34 Pin2 VDD from +3VALW to +3VL if EC use +3VL.
	11	01/09	Circuit, layout,BOM	43	PWR ON LED will flash when doing Crisis.	Add a pull down resistor R169 100K to PWR_ON_LED; Reserve a 0ohm resistor R93.
	12	01/09	Circuit, layout,BOM	36	DVT will build Vpro SKU, delete EC port80 debug signals to WLAN connector.	Delete R684, R1336 and the EC port80 debug signals to WLAN connector.
	13	01/09	Circuit, layout,BOM	13,15,24	No need reserve VGA HDMI connection.	Change PCH net "DGPU_HPD_INT#" to PCH_GPIO6; Delete U13,CV197,RV140,RV149,C430,C378,C455,C377,C376,C434,C456,C432,R432,R435,R443,Q65,R439,R437RV132,L88.
	14	01/10	Circuit, layout	37,35,26,42	BIOS prefer LAN connect to PCIE port6 for Vpro.	Swap PCIE port5 and port6 connection.
	15	01/10	BOM	33,	Distinguish with Vpro SKU.	Change UPCH1 and U59 BOM Structure to "8111E@" for non-Vpro SKUs.
	16	01/11	Circuit, layout	43	+USB_VCCE no bulk capacitor.	Change C2,C7,C8 power source from +USB_VCCB to +USB_VCCE.
	17	01/11	Circuit, layout	41	power CPU OTP issue, and power modified schematic.	Delete net EC pin27 "PWR_GPS_DOWN#" and EC pin 76 "PWRMOS_TEMP", delete R732.

QAA1x HW PIR from DVT to PVT LA-8581P REV:0.2 -> 0.3 <2012.02.24~2012.03.07. >

Rev	Item	Date	Impact	Page	Change Cause	Modify Description
0.3	1	02/24	Circuit, BOM	35	LL1 and CL13 change after EVT, DVT schematic missed and used MEMO for change.	Change LL1 from 4.7uH "SH100004T00" to 2.2uH "SH10000AA00". CL13 from 22uF "SE000000I10" to 4.7uF "SE107475K80".
	2	02/24	BOM	37	DVT board card reader JMB389 can't detect 4IN1 card.	Delete R39 BOM structure "388@".
	3	02/24	BOM	27	HDMI HPD signal level is too low for HDMI detection.	Add "@" to RH142.
	4	02/24	Circuit, layout,BOM	41,13	PVT add GPU GPS feature.	Add R266 "@", R267 "@", R268 at Page13, add "@" to DV6. Change net ACIN_BUF to GPS_DOWN#, add net PWR_GPS_DOWN#, EC_GPS_DOWN#, PWRMOS_TEMP.
	5					
	6	02/24	Circuit, layout,BOM	28	requirement from Sourcer and buyer.	Change RP1, RP3 from row resistor "SD309820180" to single ones "SD028820180"-R320,R321,R322,R323,R324,R327,R329,R330.
	7	02/24	BOM	35	UL5 BOM structure error with vPro SKU.	Delete UL5 BOM structure "8111E@".
	8	03/01	Circuit, layout,BOM	35	LAN vendor Realtek suggest:Reserve CLKREQ_LAN# pull up 10Kohm to +3V_LAN.	Reserve CLKREQ_LAN# pull up 10Kohm to +3V_LAN; add RL25 and unmount it.
	9	03/01	BOM	35	LAN vendor Realtek suggest:Reserve UL1 pin28 "EC_SWI#"pull up 10Kohm to +3V_LAN.	Modify reserved resistor RL3 from 100Kohm to 10Kohm.
	10	03/01	Circuit, layout,BOM	35	LAN vendor Realtek suggest: 6pcs decoupling capacitor for UL1 Pin 12, 27, 39, 42, 47, 48.	Add one more piece capacitor CL12 close to UL1.
	11	03/01	Circuit, layout,BOM	41	Reserve and add pull up for added net of EC pin27,68.	Reserve R732 10Kohm and add R733 100Kohm pull up to +3VS for EC pin27,68, add R734 0ohm for PWR_GPS_DOWN# connect to EC.
	12	03/01	Circuit, layout,BOM	13	Reserve a 0ohm resistor for "GPS_DOWN#" to "PWR_GPS_DOWN#".	Reserve a 0ohm resistor R270 for "GPS_DOWN#" to "PWR_GPS_DOWN#".
	13	03/02	Circuit, layout	41	power circuit removed net "PWR_MOS_TEMP", added net "GREEN_PWR4".	Remove net "PWR_MOS_TEMP", add net "GREEN_PWR4" to EC pin 76.
	14	03/05	BOM	26 35 37,34 13	Adjust crystal loading capacitors' value according to matching test result.	Change Y3 from SJ10000DJ00 to SJ10000E800, C869 from SE071150J80 to SE071100J80, C225 from SE071120J80 to SE071100J80. Change YL1 from SJ10000DJ00 to SJ10000E800, CL26 and CL27 from SE071270J80 to SE071120J80. Change C54 and C82 from SE071120J80 to SE071150J80; C766,C767 from SE071150J80 to SE071180J80. Change YV1 from SJ10000DK00 to SJ100009700, CV46 and CV47 from SE071180J80 to SE071100J80.
	15	03/05	Circuit, layout,BOM	39	Refer to QAL50/S1 design for smart card to add pull high to US4 pin26.	Add RS22 10Kohm pull up to +3V_SC for US4 Pin26, and change reserved pull down resistor RS21 from 0ohm to 10Kohm.

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				Document Number 40191E
				Date Friday, August 24, 2012
				Sheet 59 of 60

Rev	Item	Date	Impact	Page	Change Cause	Modify Description
0.3	16	03/05	Circuit, BOM	28,39	smart card device lost at USB 3.0 port.	Change smart card reader from USB port 2 to port 5.
	17	03/06	BOM	31	PCH VCCDSW3_3 change power connection from +3VALW_PCH to +3VALW.	Add "@ " to R415, delete "@ " to R382.
	18	03/06	Circuit, layout, BOM	35,36, 39,29 41,45	ErP lot 6 fail, reserve a EC pin VSB_EN to control VSB; reserve LAN WAKE to EC and PCH GPIO27.	Delete reserved net AOAC_ON (EC pin 38) and DRAMRST_GATE (EC pin 98) and their test point T23,T24. Use these two pins for new added net VSB_EN and EC_PME# Reserve net GPIO27_WAKE#, EC_PME# for LAN WAKE, reserve net EC_PME# to WLAN, WWAN and PCIE Express card wake. thus, add R702@, RH122@, RH171, R331@, RL8(8111E@),RL9@, RL10@, R100@, R102, R761@, R767@,R768@. Reserve net VSB_EN, thus add R765@, R766, R817, R818@, R819@; delete R816@, add @ to R754.
	19	03/06	Circuit, layout, BOM	25	Reserve big size crystal Y6 for 32.768KHz.	Reserve big size crystal Y6 for 32.768KHz.
	20	03/08	BOM	40,43	UU1 SA000047500 was forbidden, change material requirement from buyer.	Change UU1 from SA000047500 to SA000033H00; Correct U6 description and value.
	21	03/08	BOM	43,44	Change C4,C6 from SE053475Z05 to normal part SE053475Z80.	Change C4,C6 from SE053475Z05 to normal part SE053475Z80.

Rev	Item	Date	Impact	Page	Change Cause	Modify Description
1.0	1	04/19	Circuit, BOM,layout	25	Reserve +5VS for MOS Q10 gate of audio sync signal to PCH HDA sync signal.	Add 0ohm 0402 resistor R189@ and R190.
	2	04/19	BOM	25,34	Change 32.768KHz crystal P/N, and RTC capacitor C204 from 15pF to 18pF.	Change Y2, X3 from SJ10000BM00 to SJ100001K00. change C204 from SE071150J80 to SE071180J80.
	3	04/19	BOM	39	to solve issue of "Smart Card also show in Device Manager after plug out it".	Change U54 from SA000042I00 to SA000042I10.
	4	04/19	Circuit,layout	45	Reserve 820Kohm resistor to GND for +3VALW_PCH and +1.05VS_DGPU DC/DC MOS	GATE. Add 820Kohm R432@ and R435@.
	5	04/19	BOM	45,41	For ErP lot6, add +3VALW to +3VALW_PCH DC/DC circuit.	Delete @ for U25, Q46, Q49, R813, C837, C839, C838, R804, C836, R807, R754.
	6	04/20	BOM,layout		cost down: change some 0ohm resistors to short pad.	cost down: change some 0ohm resistors to short pad.
	7	04/23	BOM	42	vPro: Intel suggest to change R1232 from 2.2K to 10K.	vPro: change R1232@ from 2.2K to 10K.
	8	04/23	BOM	42	vPro: Intel suggest to change C470 from 10uF to 22uF.	vPro: change C470 from 10uF to 22uF.
	9	04/23	BOM	35	vPro: Intel suggest to change CL34 from 0.1uF to 1uF.	vPro: change CL34 from 0.1uF to 1uF. keep CL34 0.1uF for 8111E LAN.
		04/23	Circuit, BOM,layout	42	vPro: Reserve LAN WAKE to EC.	vPro reserve R559@ 0ohm for LAN WAKE connect to EC.
		04/25	Circuit,layout	35	There is not enough space for LAN GND ESD diodes. EMI test OK without the two ESD diodes.	Remove DL3@, DL4@.

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				4019IE	Rev 6
				Date:	Friday, August 24, 2012
				Sheet	60 of 60