

Compal Confidential

Intel Haswell rPGA Processor with Lynx Point-H

Afterburn MXM

LA-9371P

2012-09-28

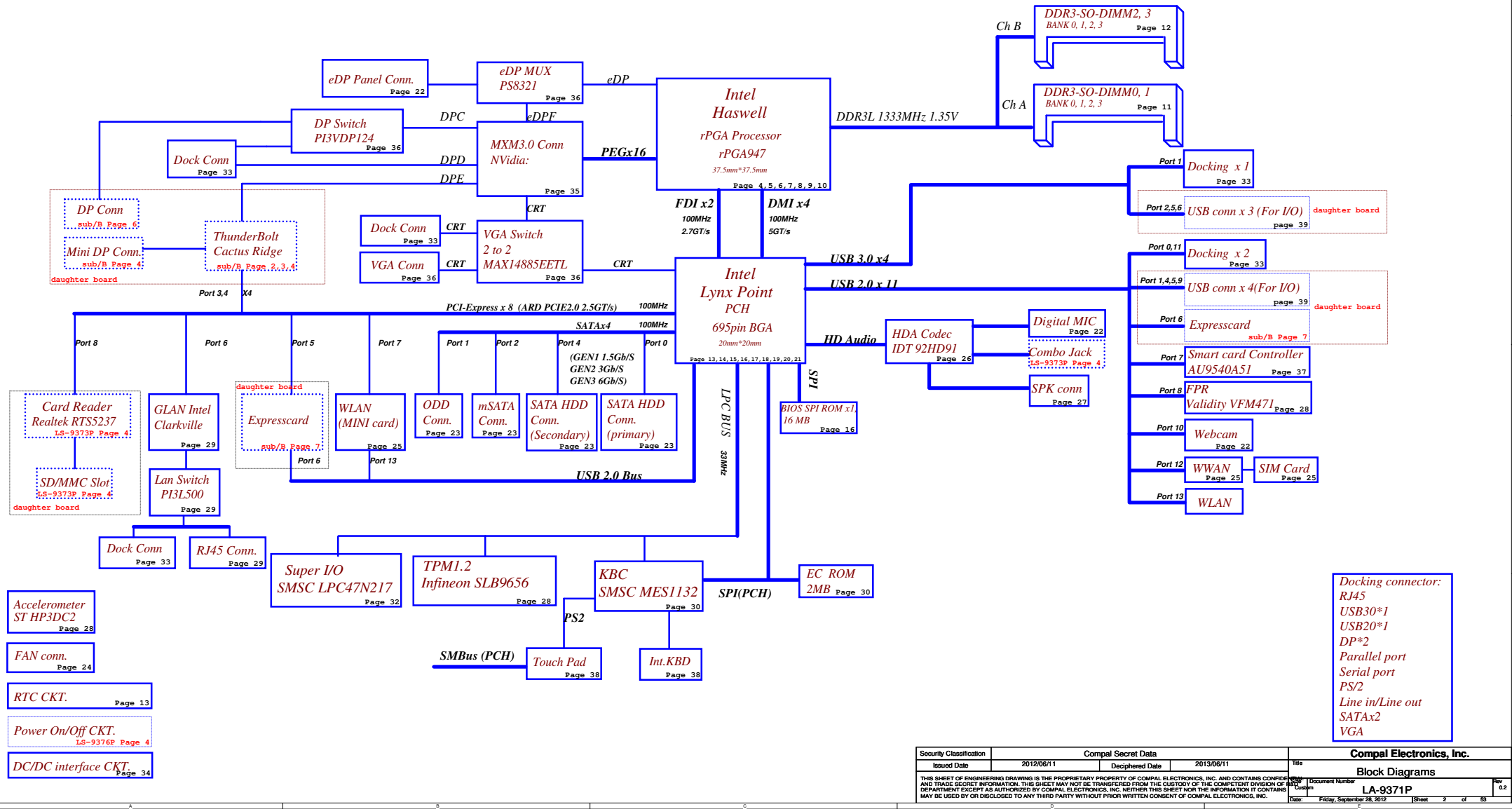
REV : 0.2

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Issued Date	2012/06/11	Deciphered Date	2013/06/11	Title	Cover Page	
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Compal Confidential

Model Name : Afterburn

File Name : LA-9371P



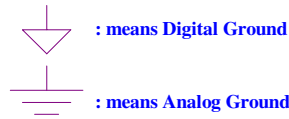
Docking connector:
RJ45
USB30*1
USB20*1
DP*2
Parallel port
Serial port
PS/2
Line in/Line out
SATAx2
VGA

Voltage Rails

(O MEANS ON X MEANS OFF)

power plane State	+RTCVCC	B+	+5VDS +3VDS	+1.35V +0.675VS	+5VS +3VS +1.5VS +VCC_CORE +1.05VS +1.05VM	
S0	O	O	O	O	O	
S1	O	O	O	O	O	
S3	O	O	O	O	X	
S5 S4/AC	O	O	O	X	X	
S5 S4/ Battery only	O	O	X	X	X	
S5 S4/AC & Battery don't exist	O	X	X	X	X	

Symbol Note :



@ : means just reserve , no build

AMT@ : means just install for support iAMT

CONN@ : means ME part.

Layout Notes

07/24 update

: Question Area Mark.(Wait check)

Install below 45 level BOM structure for ver. 0.1

45@ : means just put it in the BOM of 45 level.

Install below 43 level BOM structure for ver. 0.1

DEBUG@ : means just build when PCIE port 80 CARD function enable. *Remove before MP*

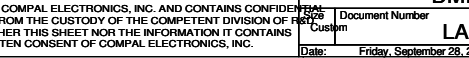
SMBUS Control Table

	SOURCE	BATT	2nd BATT	XDP	SODIMM	G-SENSOR	TP	NIC	NFC	EC	MXM
I2C_MAIN_CLK I2C_MAIN_DAT	SMSC1126	V	X	X	X	X	X	X	X	X	X
I2C_BAY_CLK I2C_BAY_DAT	SMSC1126	X	V	X	X	X	X	X	X	X	X
MEM_SMBCLK MEM_SMBDATA	Haswell	X	X	V	V	V	V	X	X	X	X
LAN_SMBCLK LAN_SMBDATA	Haswell	X	X	X	X	X	X	V	V	X	X
SML1_SMBCLK SML1_SMBDATA	Haswell	X	X	X	X	X	X	X	X	V	V

Stapping Options Flash

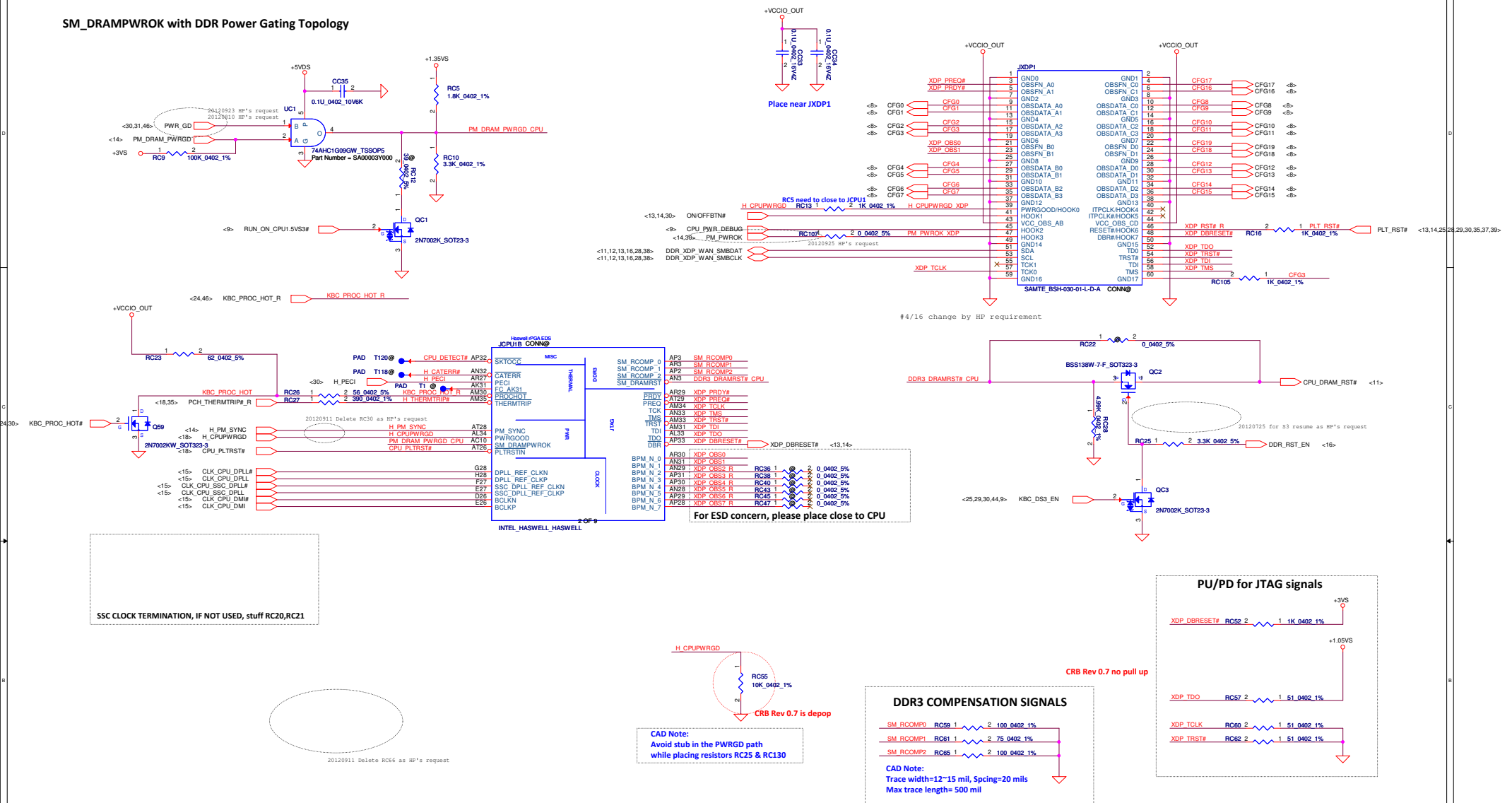
GPIO 51 Bit 1	GPIO 19 Bit 0	Boot BIOS Destination
0	0	Reserved
0	1	RSVD
1	0	SPI
1	1	LPC

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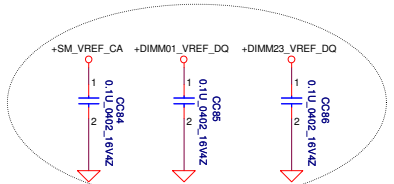
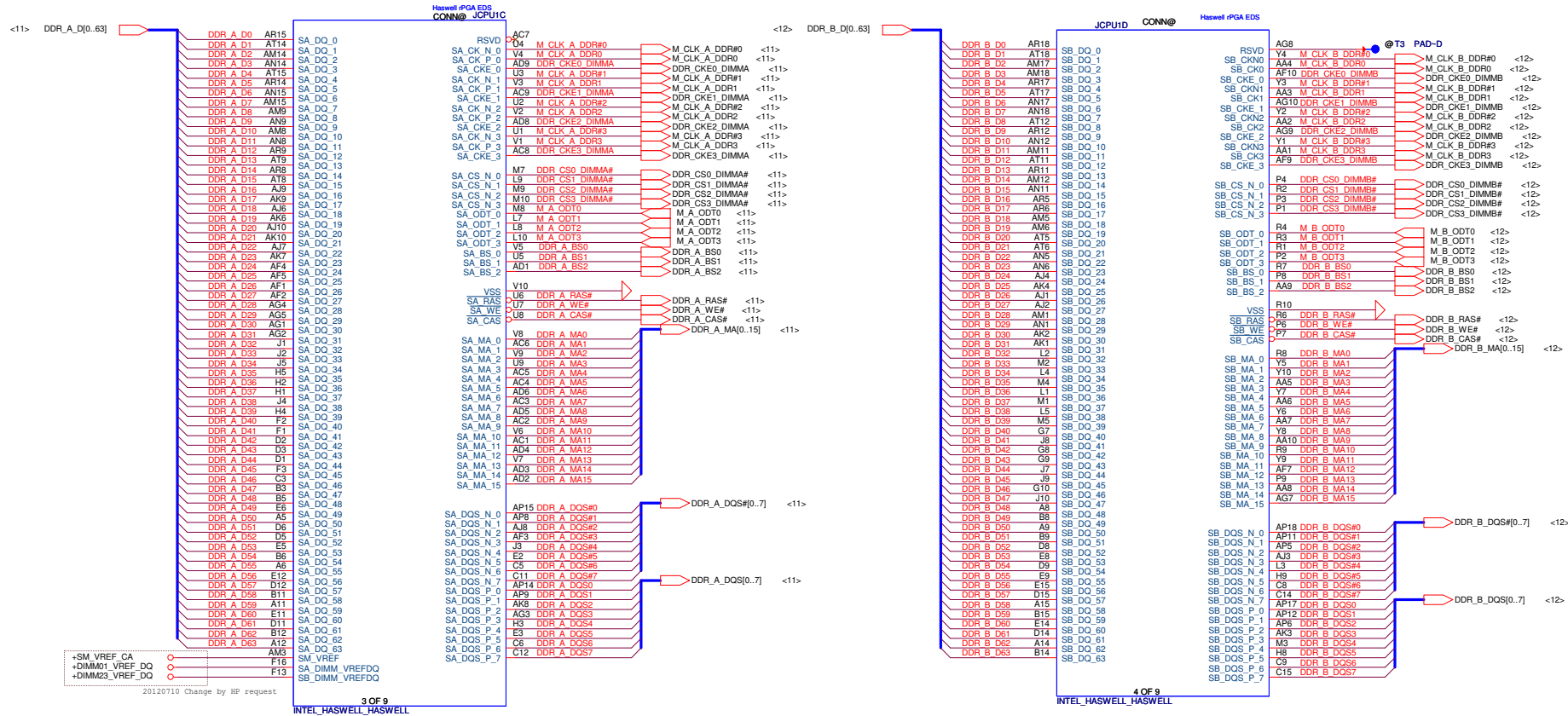


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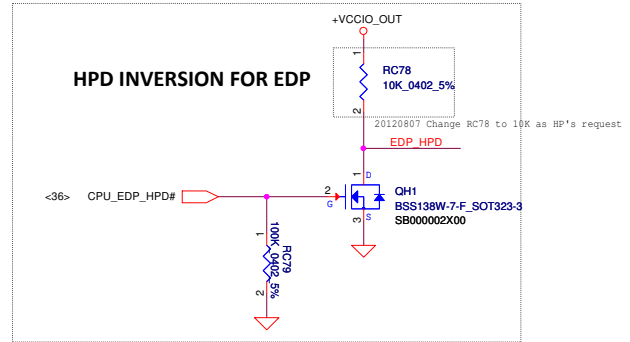
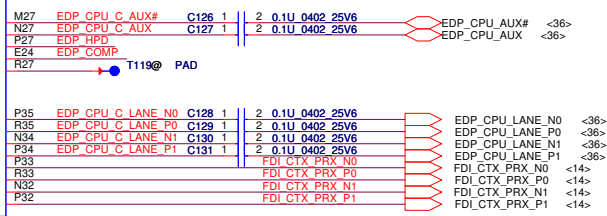
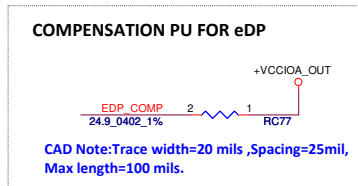
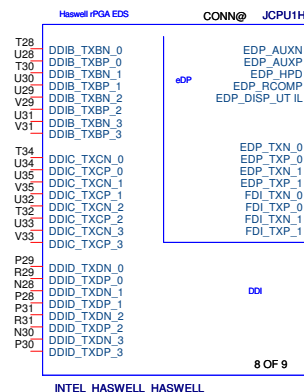
SM_DRAMPWROK with DDR Power Gating Topology



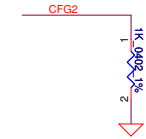
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Issued Date		Deciphered Date		2013/06/11		PM_XDP_CLK	
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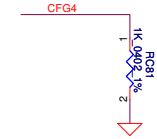
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Issued Date	2012/06/11	Deciphered Date	2013/06/11	Title	DDR III
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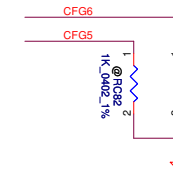
CFG STRAPS for CPU



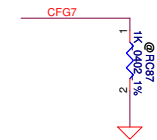
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



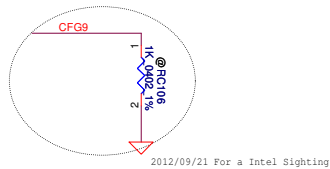
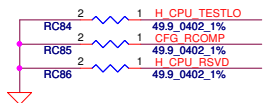
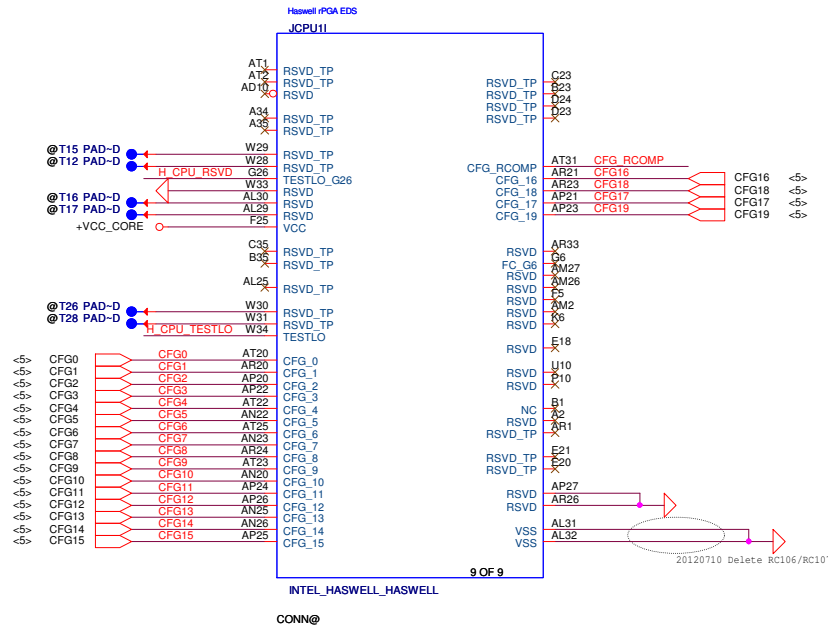
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



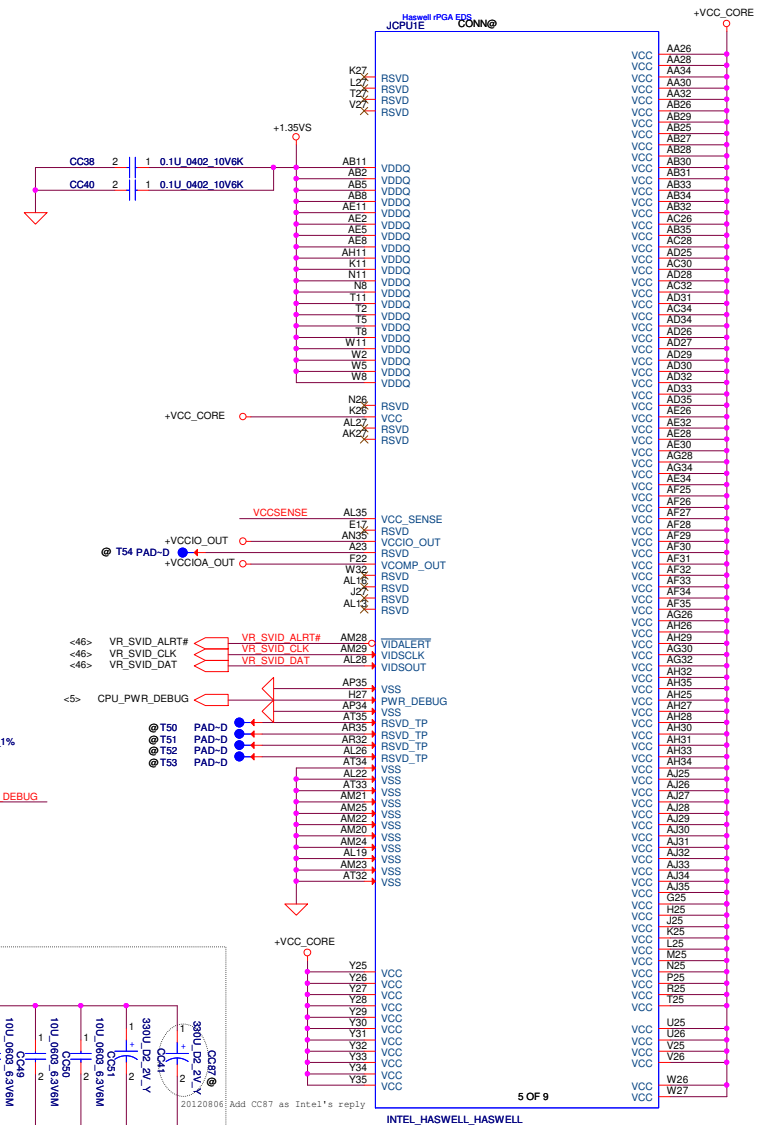
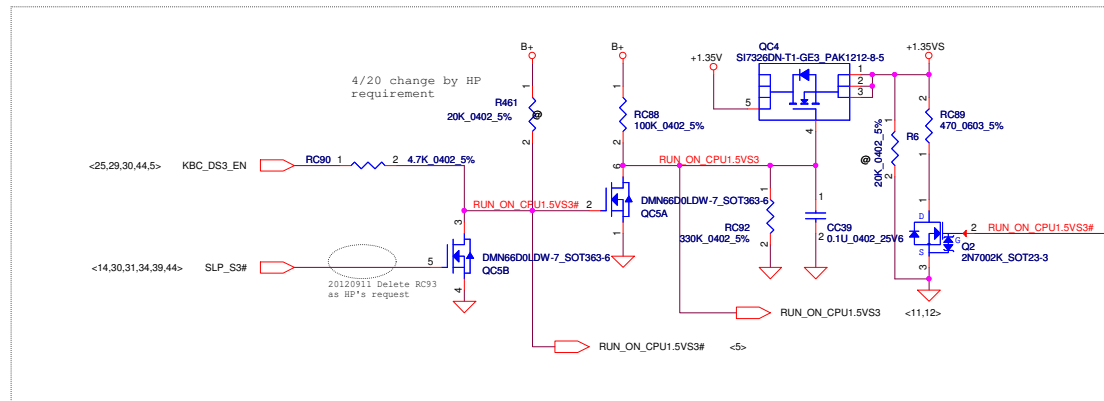
PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



+1.35VS Source

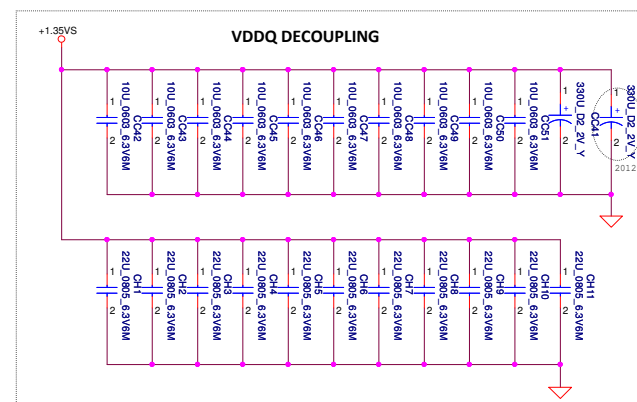
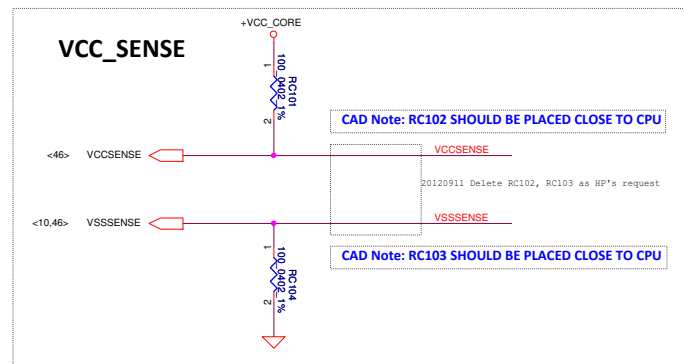


SVID ALERT

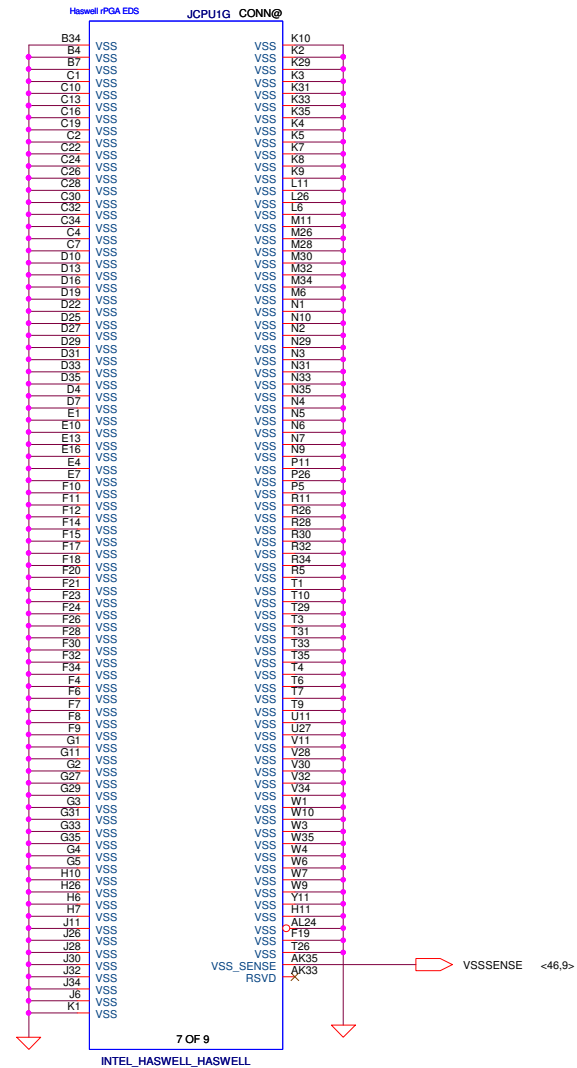
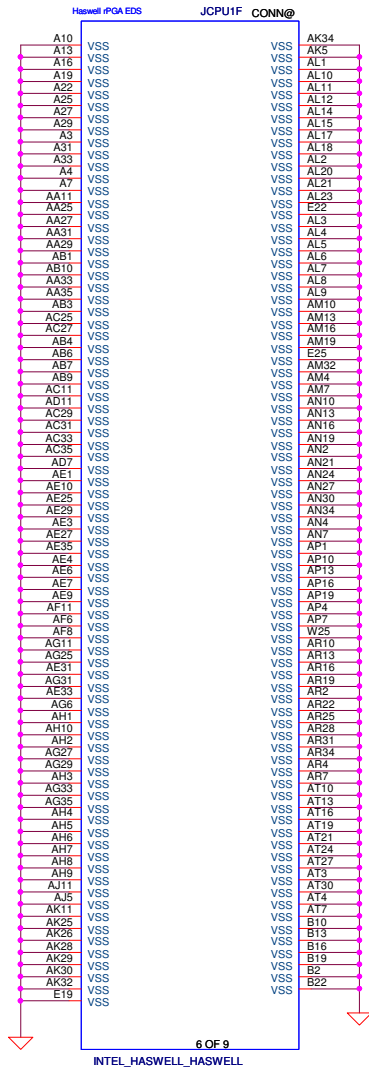
**CAD Note: Place the PU resistors close to CPU
RC60 close to CPU 300 - 1500mils**

SVID DATA

**CAD Note: Place the PU resistors close to CPU
RC63 close to CPU 300 - 1500mils**

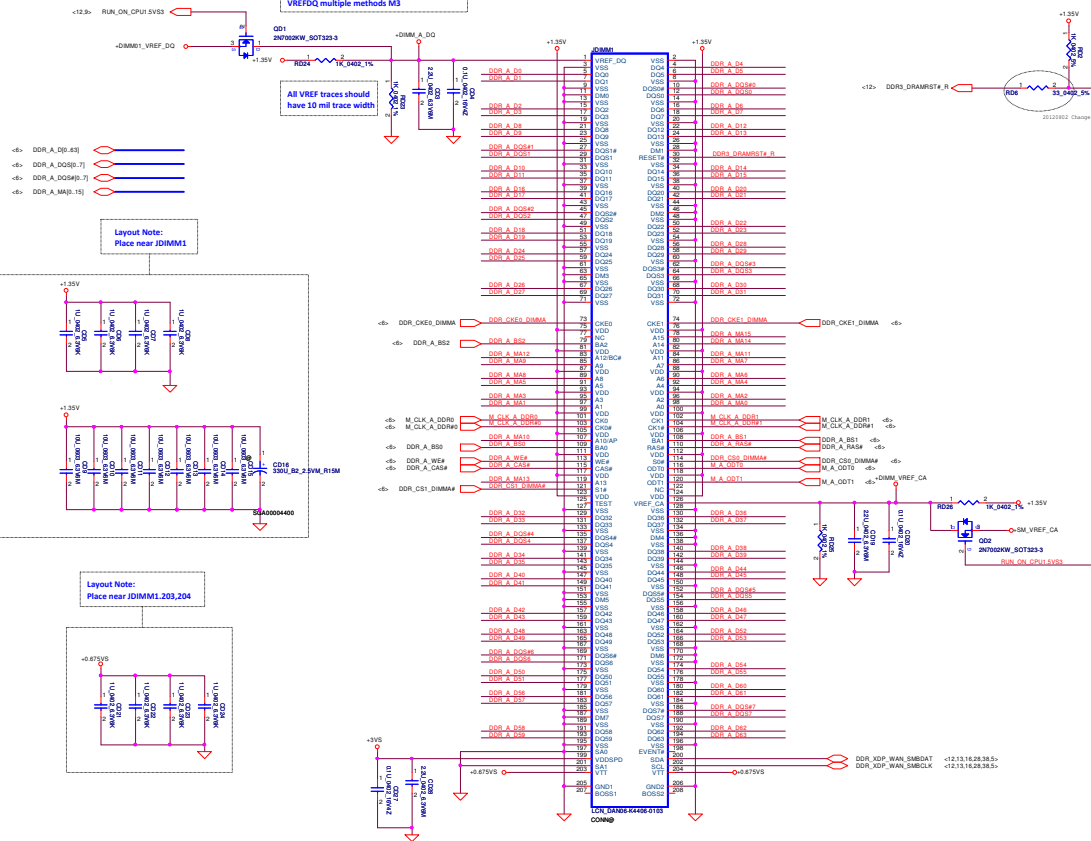


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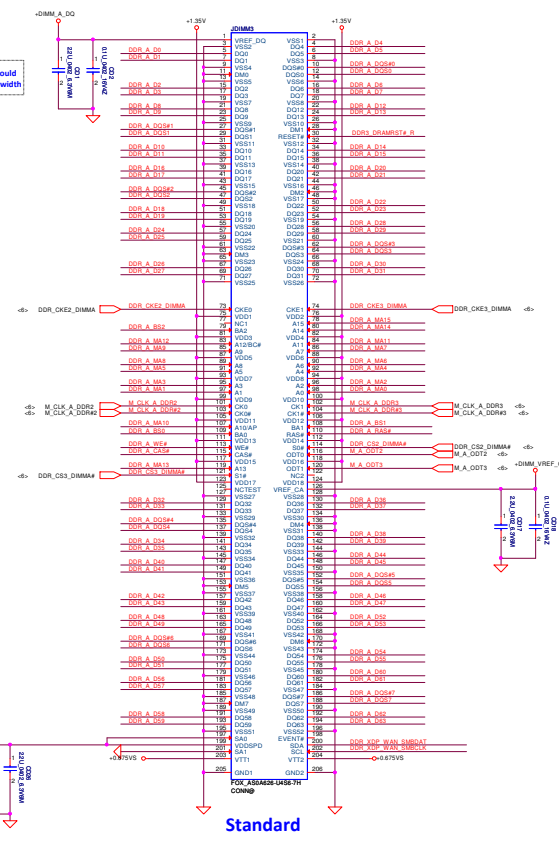


JDIMM3 H=4.0mm BOT

JDIMM1 H=5.2 mm TOL



Reverse

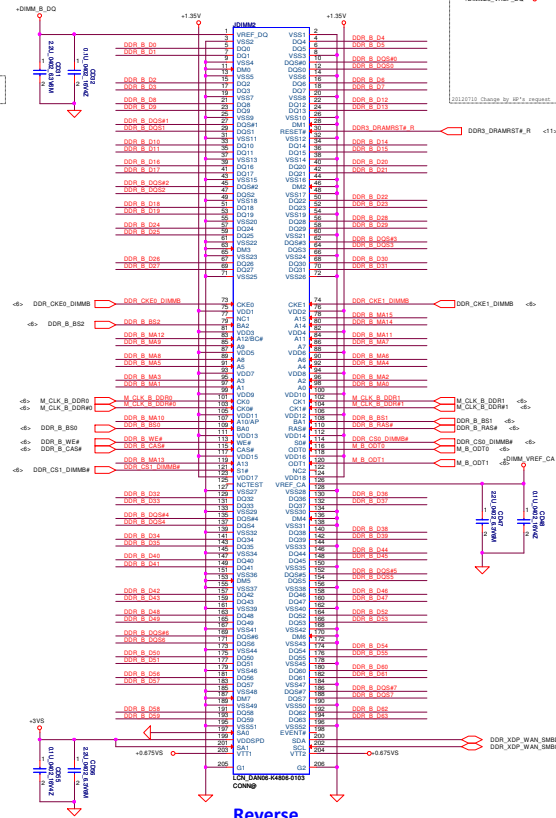


Standard

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06/11/2012				

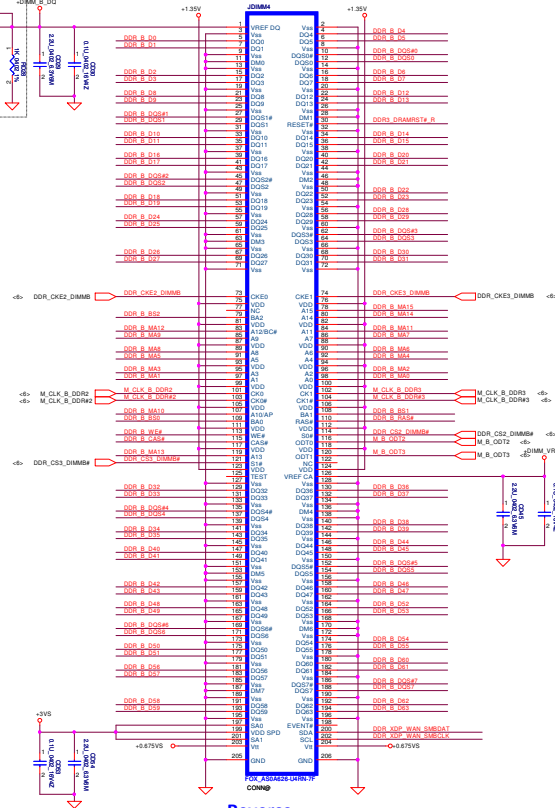
Populate RD4, De-Populate RD8 for Intel DDR3 VREFDQ multiple methods M1
Populate RD8, De-Populate RD4 for Intel DDR3 VREFDQ multiple methods M3

JDIMM2 H=9.2mm TOP



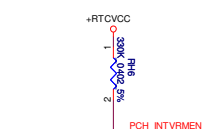
Reverse

JDIMM4 H=4.0mm BOT

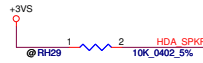


Reverse

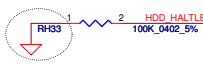
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INTVRMEN - INTEGRATED SUS 1.05V VRM ENABLE
High - Enable Internal VRs
Low - Enable External VRs



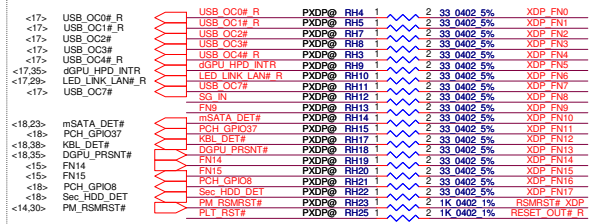
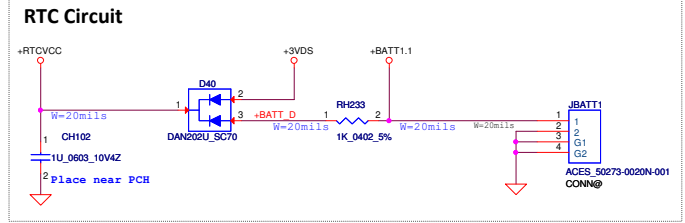
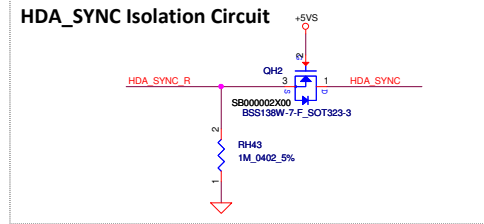
NO REBOOT STRAP
DISABLED WHEN LOW (DEFAULT)
ENABLED WHEN HIGH



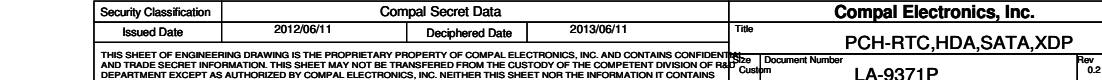
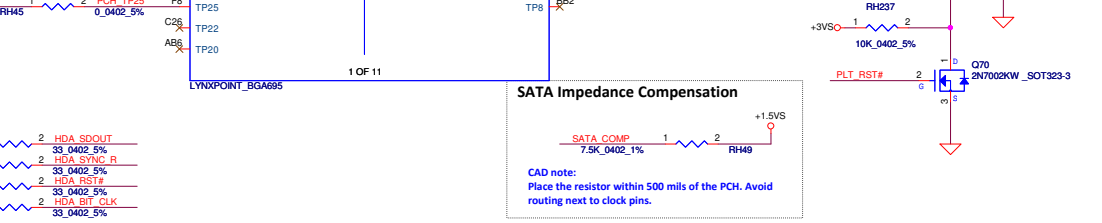
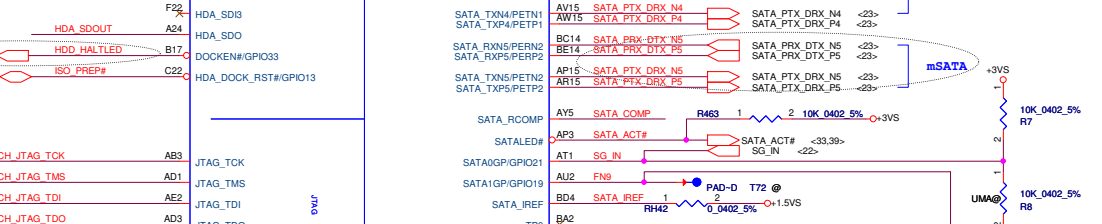
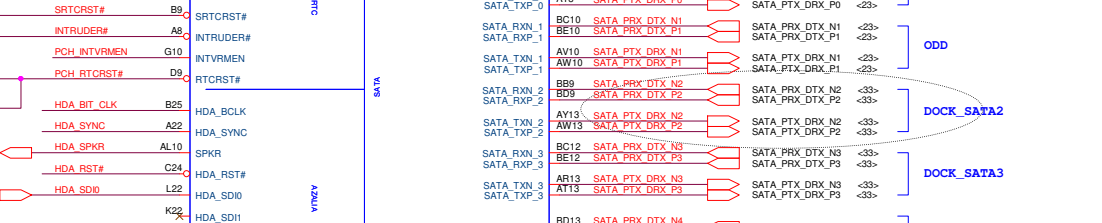
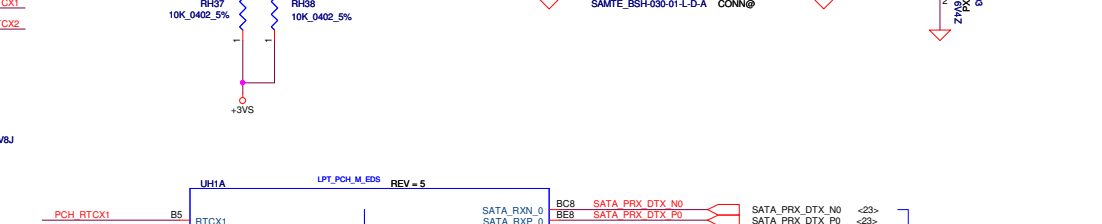
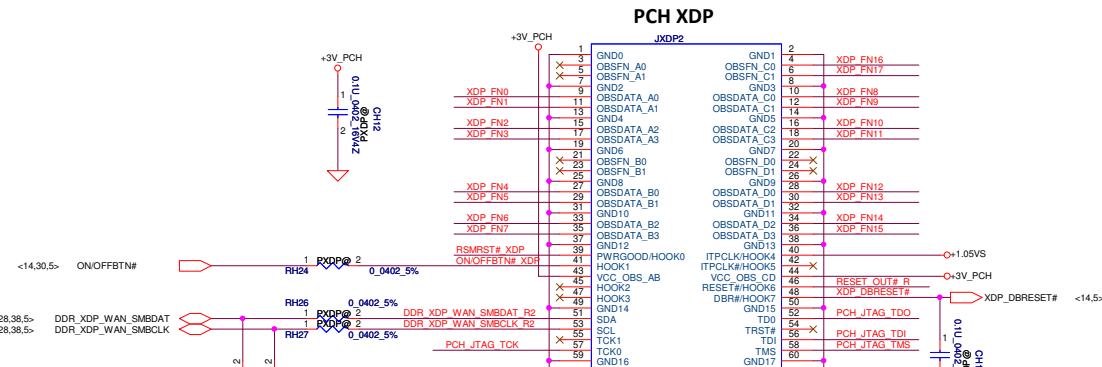
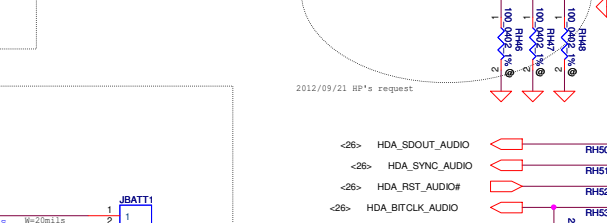
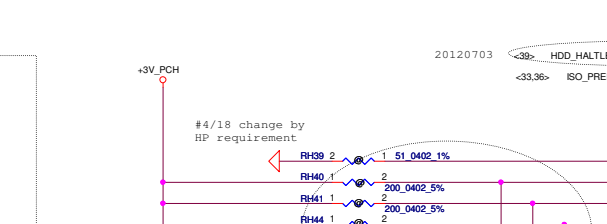
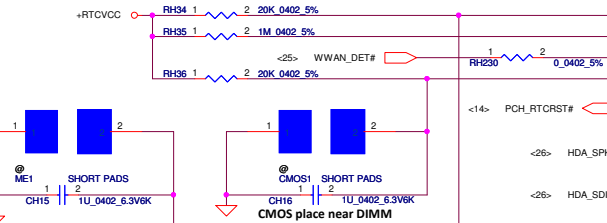
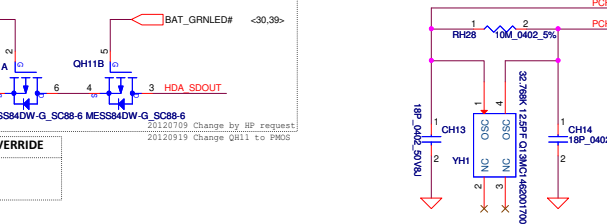
20120802 HP's request

CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

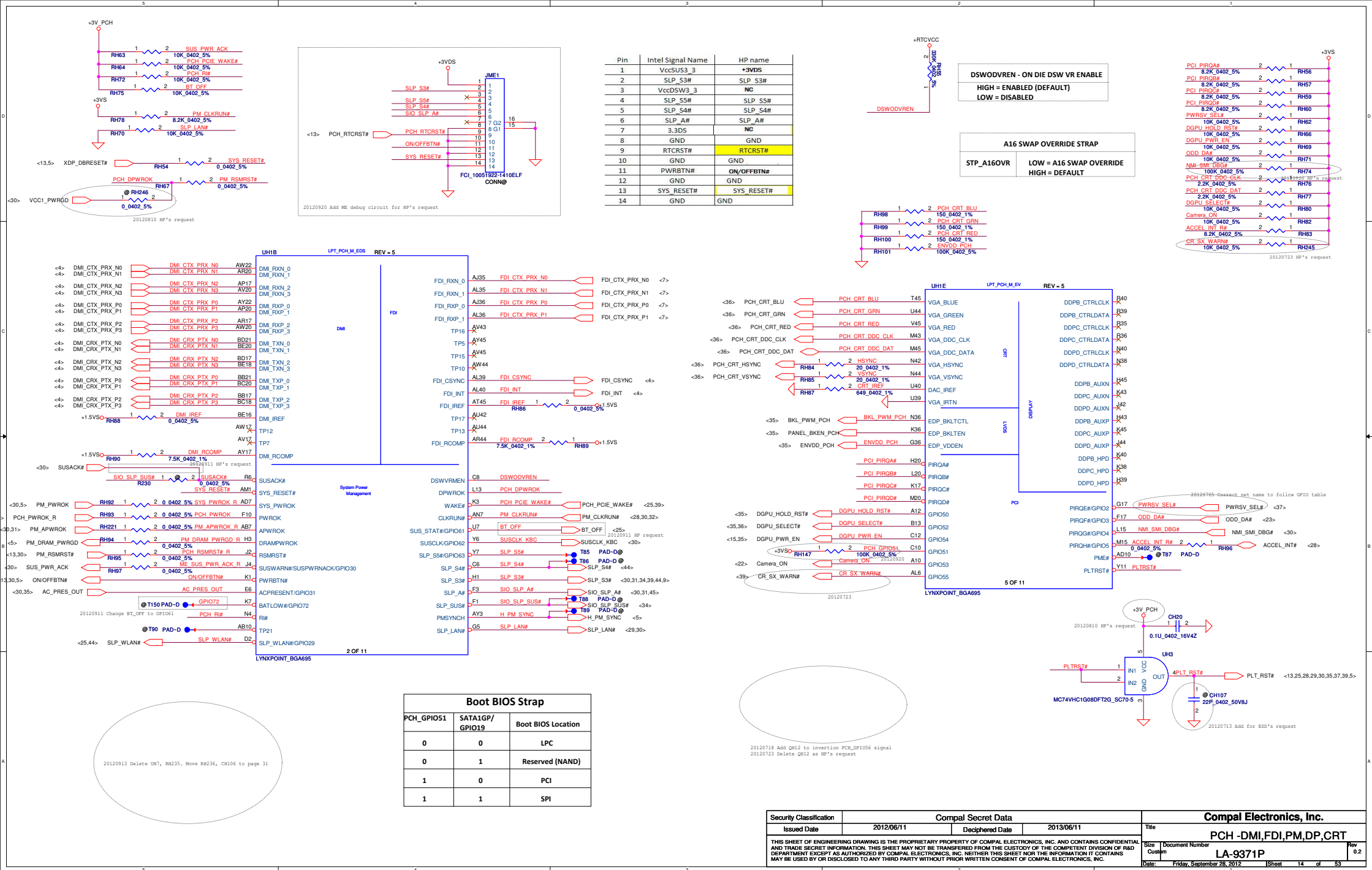
ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers



#4/18 change by HP requirement

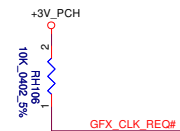


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Boot BIOS Strap		
PCH_GPIOS1	SATA1GP/ GPIO19	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

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CLK_SIO_14M

YH2

RH132

25MHZ_20PF_7A25000112

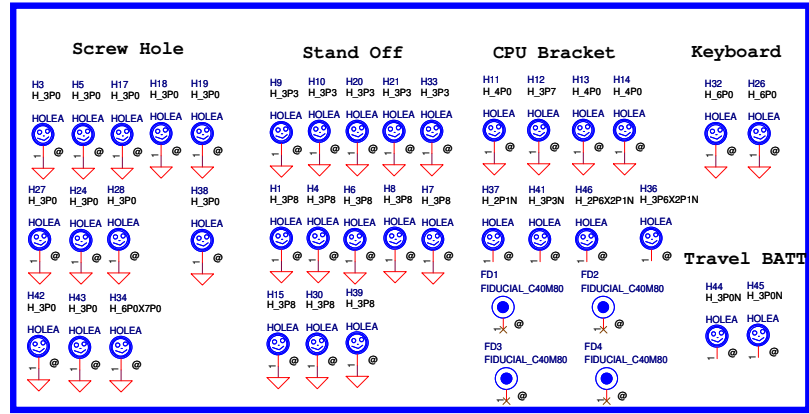
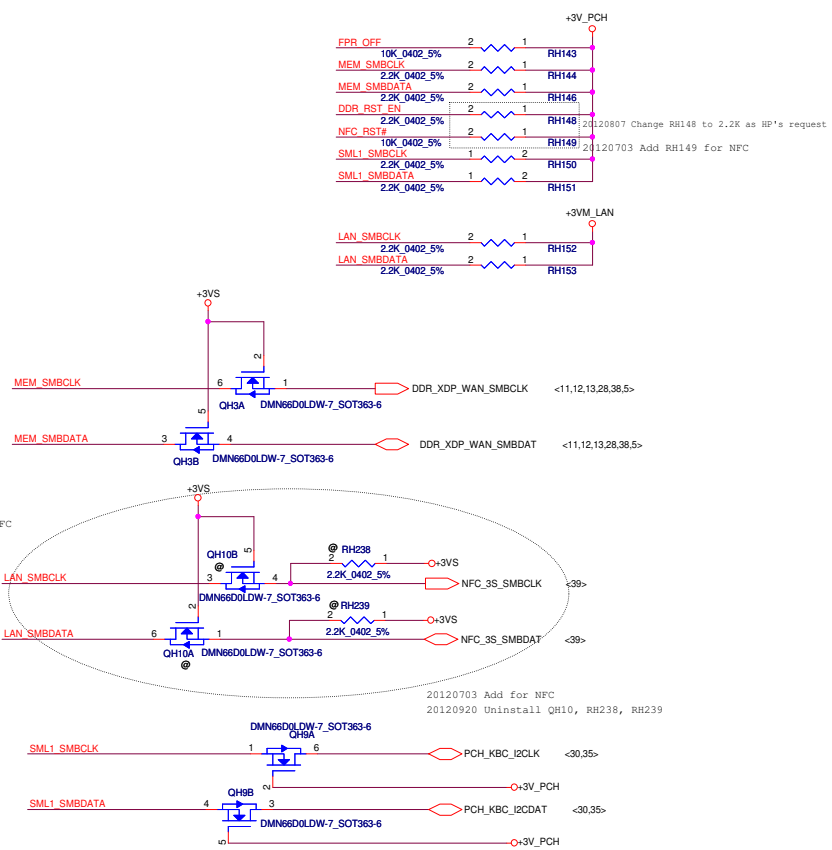
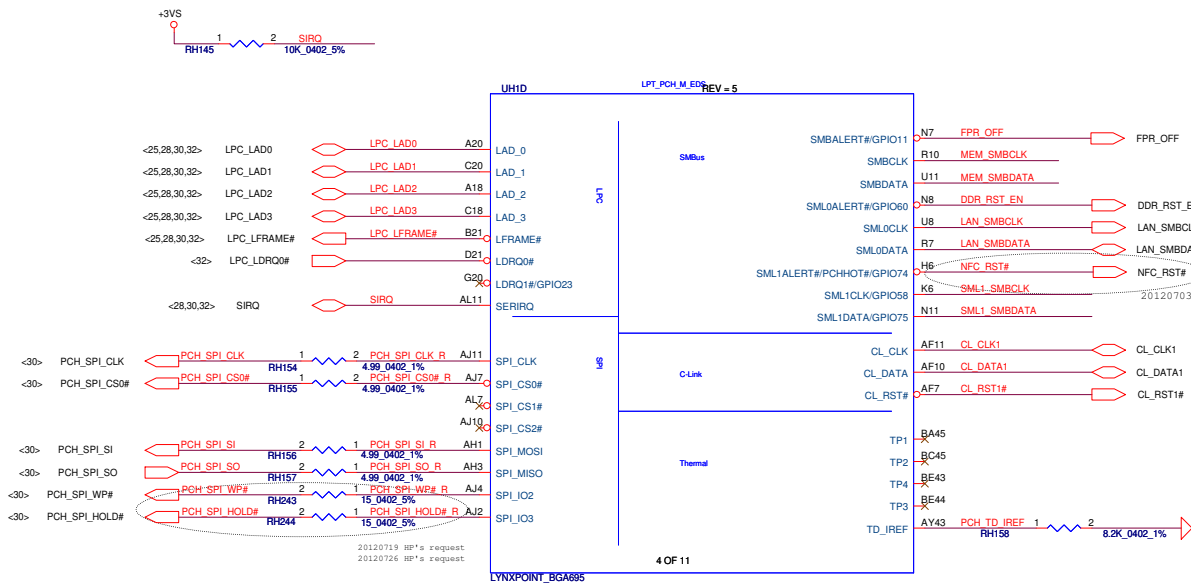
CH21

CH2

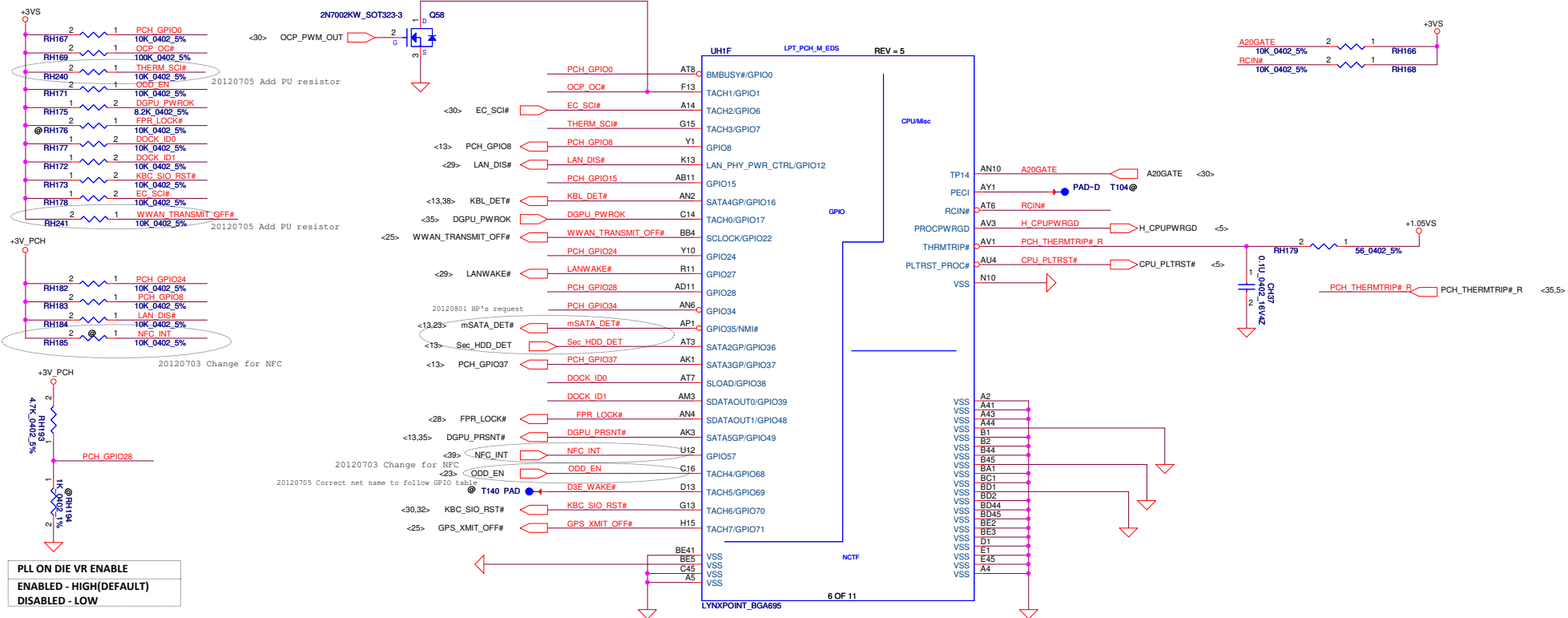
74VHC04_50V8U



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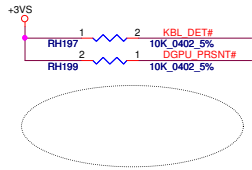
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		Deciphered Date		PCH - SPI, SMBUS, LPC	
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PLL ON DIE VR ENABLE
ENABLED - HIGH(DEFAULT)
DISABLED - LOW

SATA2GP/GPIO36 , SATA3GP/GPIO37 SAMPLED AT RISING EDGE OF PWROK.
WEAK INTERNAL PULL-DOWN.(WEAK INTERNAL PULL-DOWN IS DISABLED AFTER PLRST_N DE-ASSERTS).
NOTE: THIS SIGNAL SHOULD NOT BE PULLED HIGH WHEN STRAP IS SAMPLED.

Config	GPIO16,49
USB X4,PCIEX8,SATAX6	11
USB X6,PCIEX8,SATAX4	01

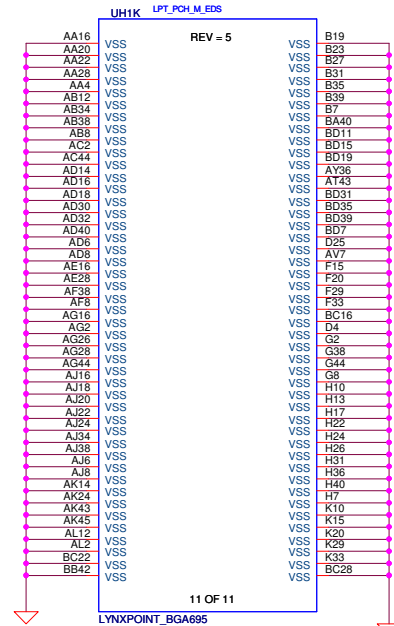
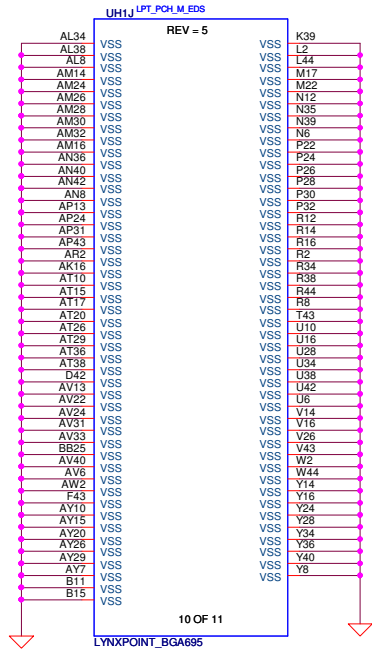


Fixed Signals				Muxed Signals		Fixed Signals						Muxed Signals		Fixed Signals			
USB3 1	USB3 2	USB3 5	USB3 6	PCIE 1	PCIE 2	PCIE 3	PCIE 4	PCIE 5	PCIE 6	PCIE 7	PCIE 8	SATA 4	SATA 5	SATA 0	SATA 1	SATA 2	SATA 3
				(00)	(00)							(00)	(00)				
				USB3 3	USB3 4							PCIE 1	PCIE 2				
				(01)	(01)							(01)	(01)				

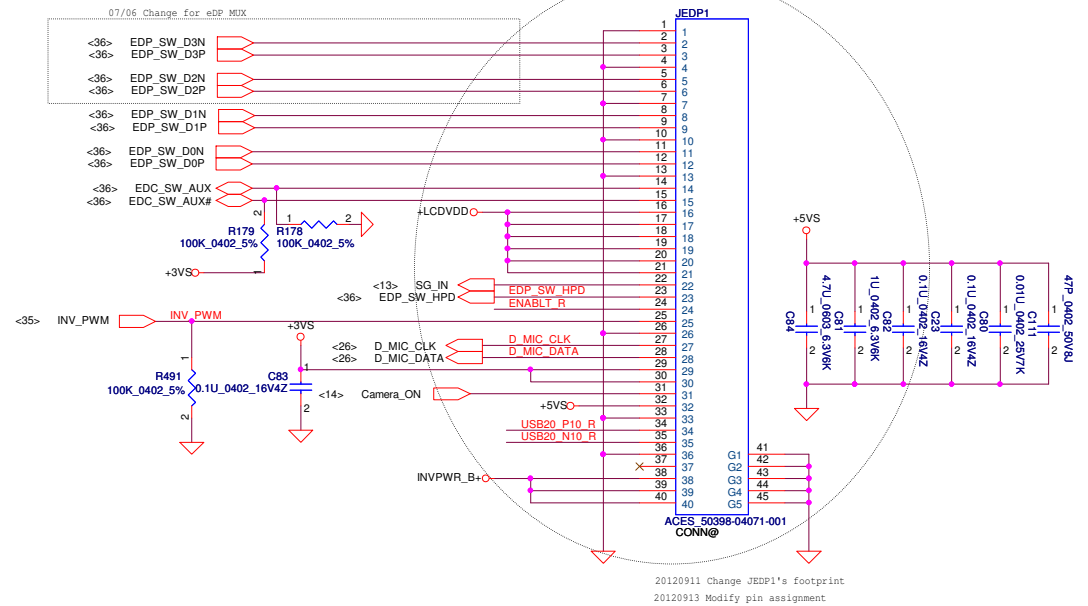
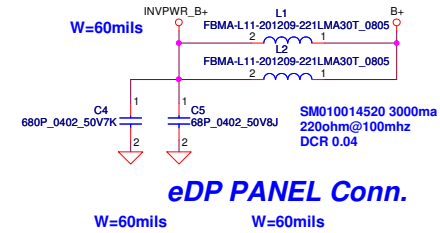
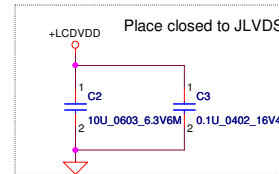
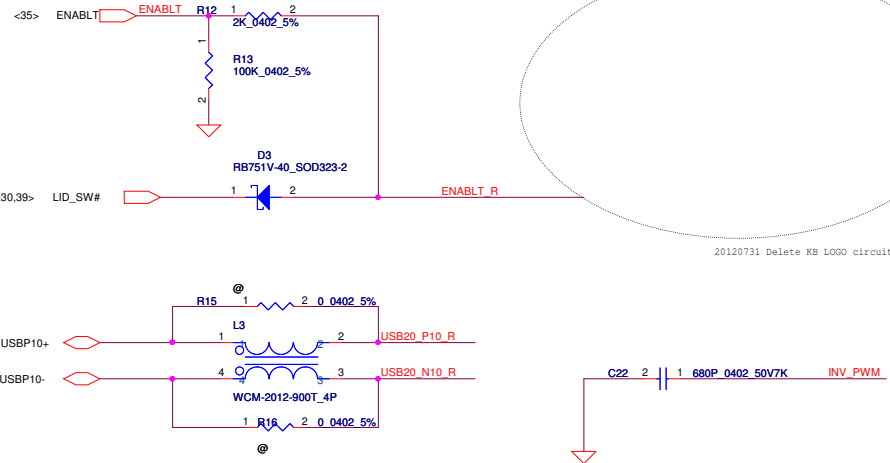
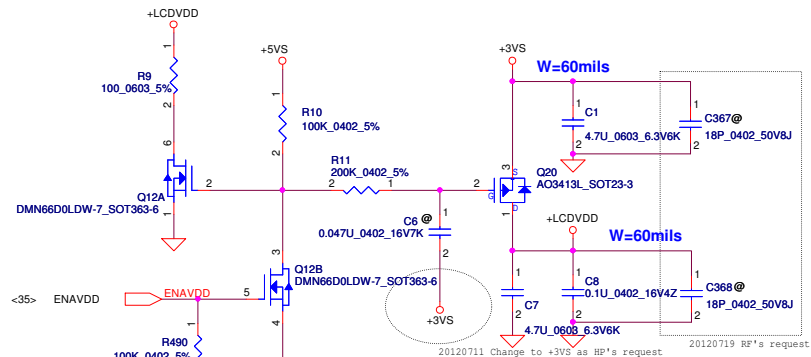
Board ID	BRD_ID1 GPIO15	BRD_ID2 GPIO34	BRD_ID3 GPIO35	BRD_ID4 GPIO40
DB0	0	0	0	0
DB1	0	0	0	1
DB2	0	0	1	0
SI1	0	1	0	0
SI1B	0	1	0	1
SI2	0	1	1	0
PV1	1	0	0	0
MV	1	1	0	0



Rev	0.2
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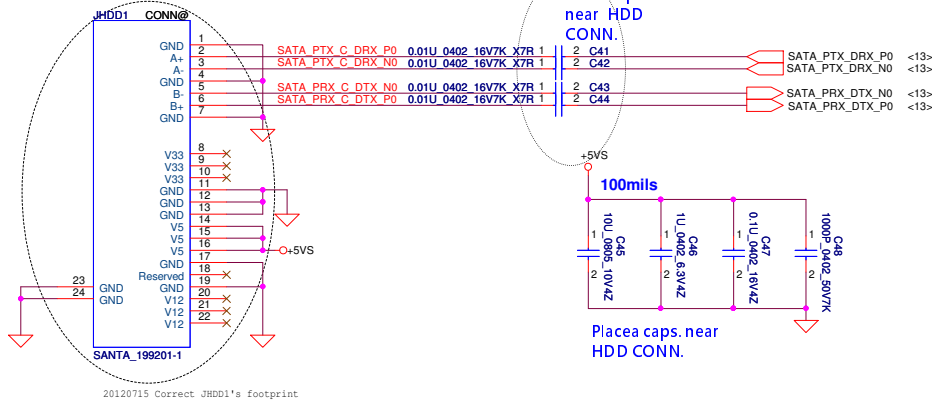


LCD POWER CIRCUIT

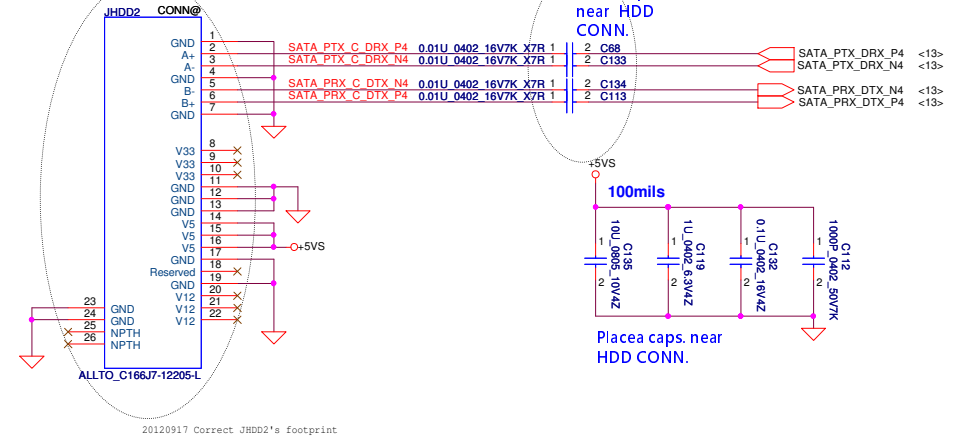


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				eDP/LVDS CONN & Camera	
				Document Number	
				LA-9371P	
				Rev	
				0.2	
				Date: Friday, September 28, 2012	
				Sheet 22 of 53	

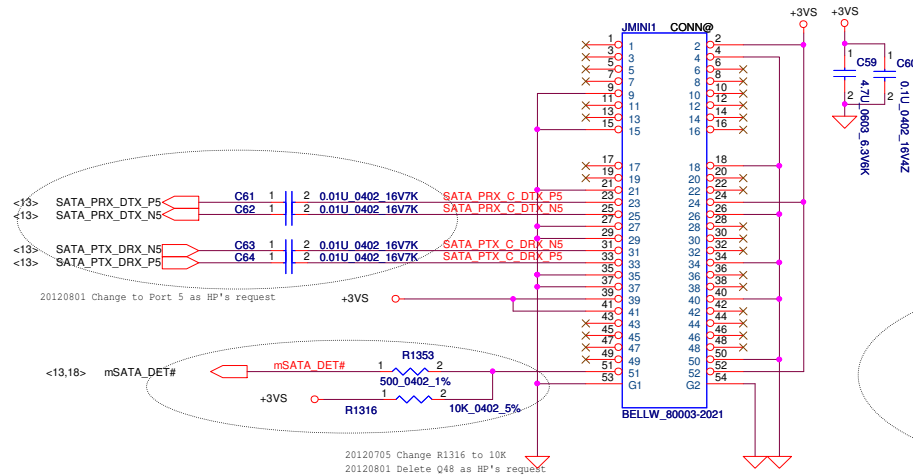
SATA Primary HDD CONN.



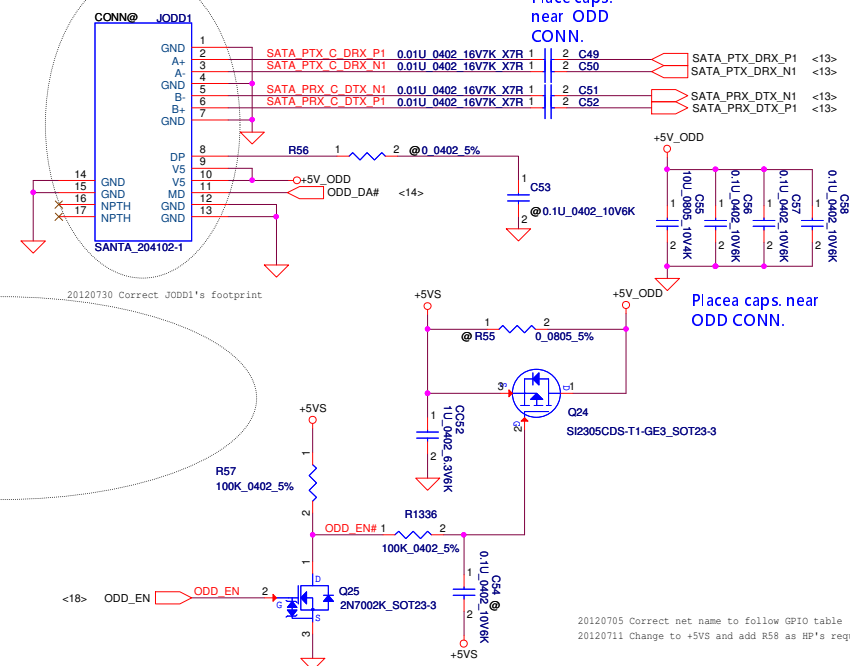
SATA Second HDD CONN.



mSATA Conn.

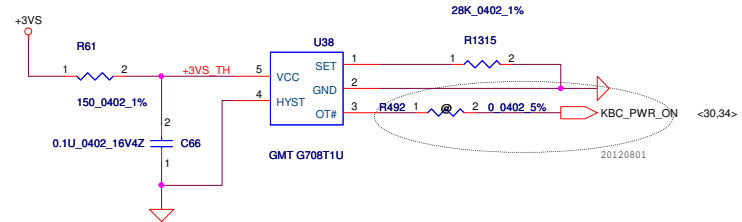
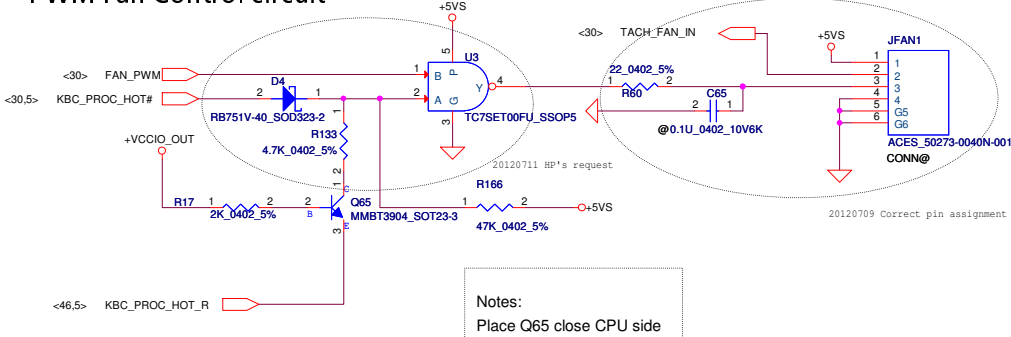


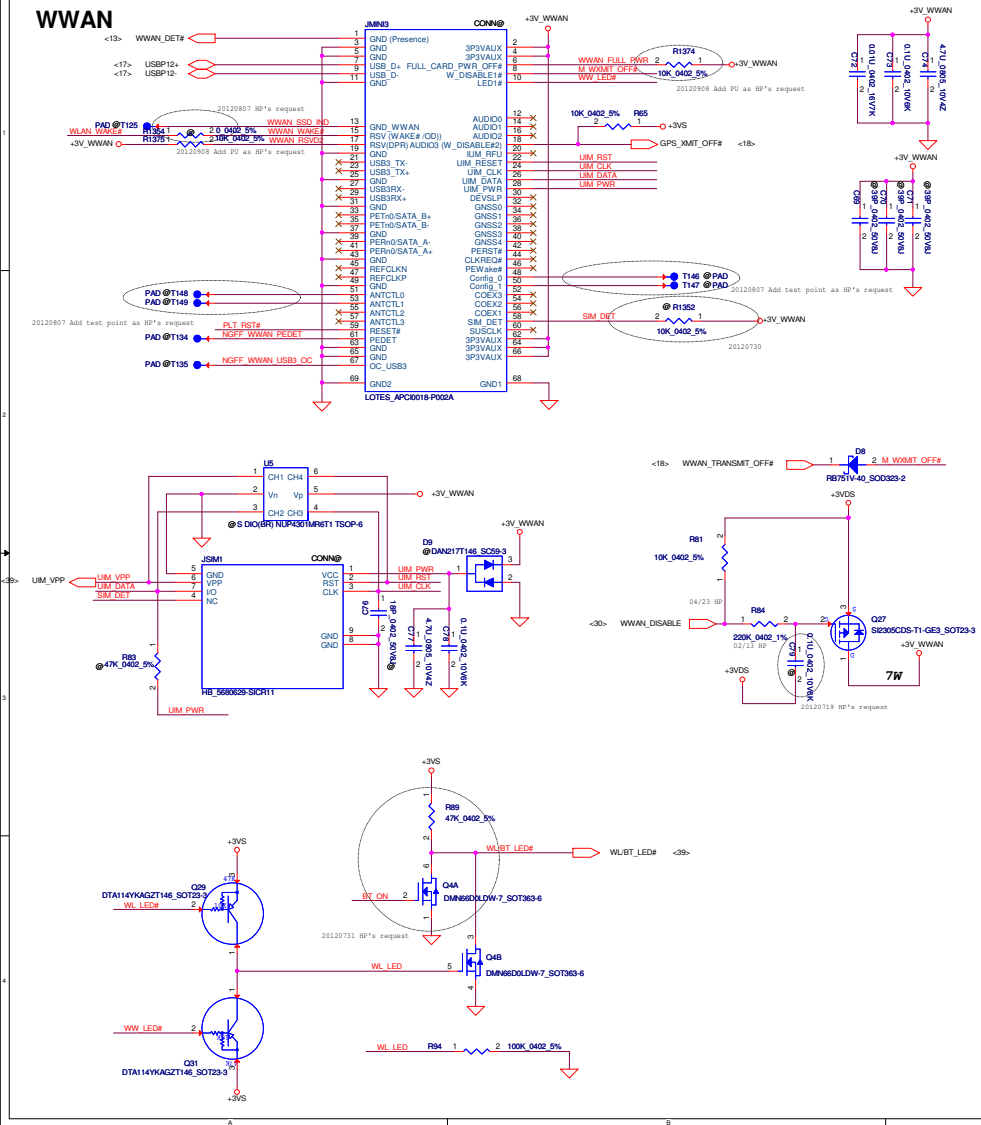
SATA ODD CONN.



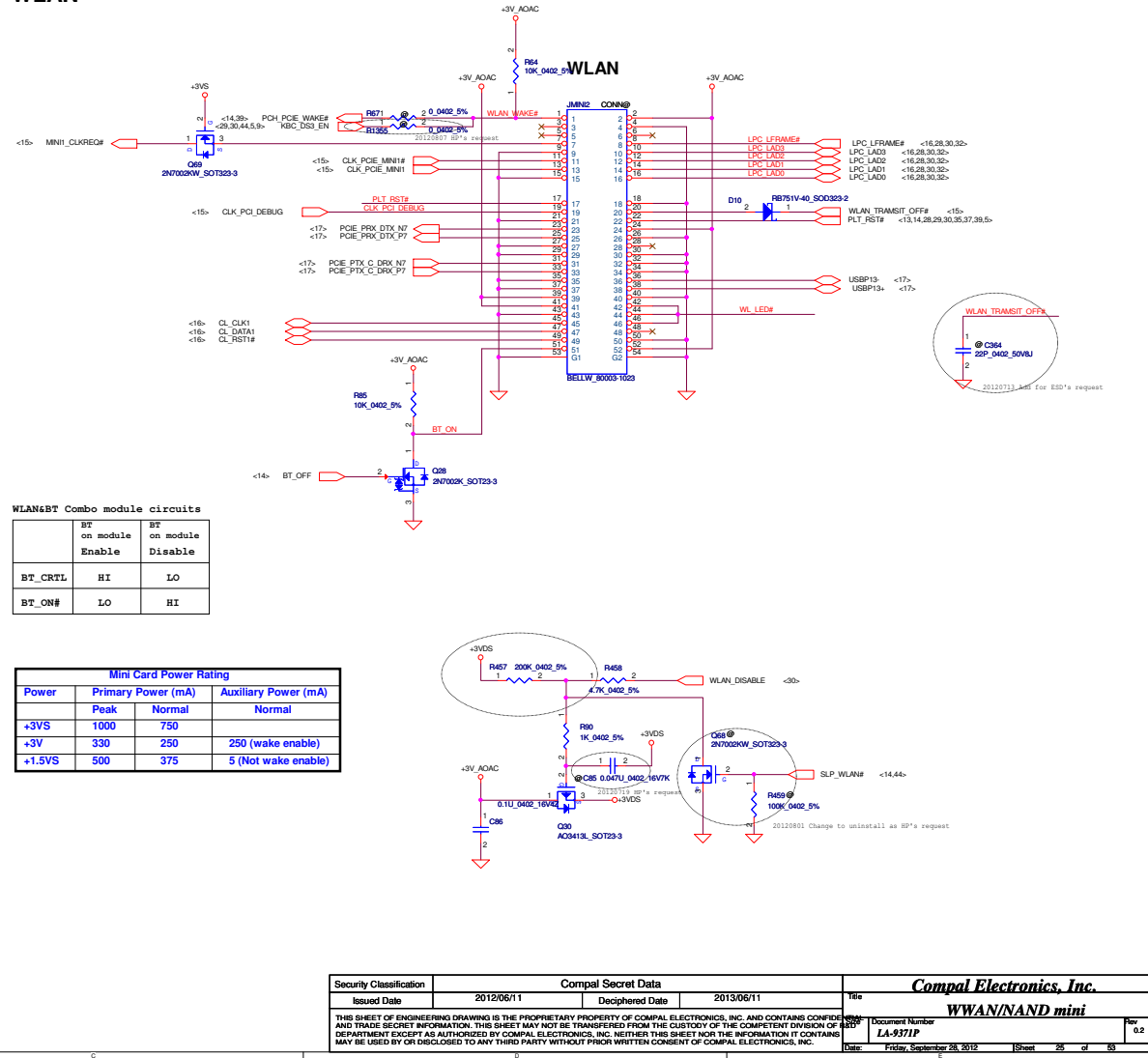
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Issued Date	2012/06/11	Deciphered Date	2013/06/11	Title	IBEX-M(IU/6)-HDA/JTAG/SATA
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PWM Fan Control circuit



WWAN

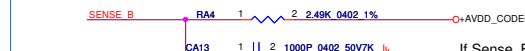
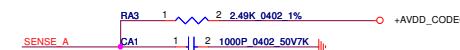
WLAN



Notes:
Keep PVDD supply and speaker traces routed on the DGND plane.
Keep away from AGND and other analog signals

PLACE CLOSE TO U1 PIN 13

If Sense_A total length is greater than 6 inches, change C12 to 0.1uF



PLACE CLOSE TO U1 PIN 14

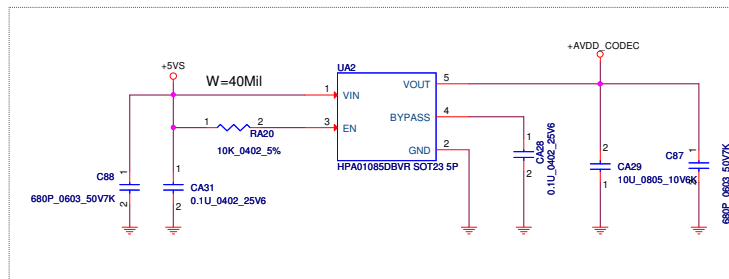
If Sense_B is un-used, then pull high Sense_B to AVDD by 10Kohm resistor

External MIC
Combo Jack
Headphone

Internal SPKR(front stereo speaker)

20120702 Delete MUTE circuit

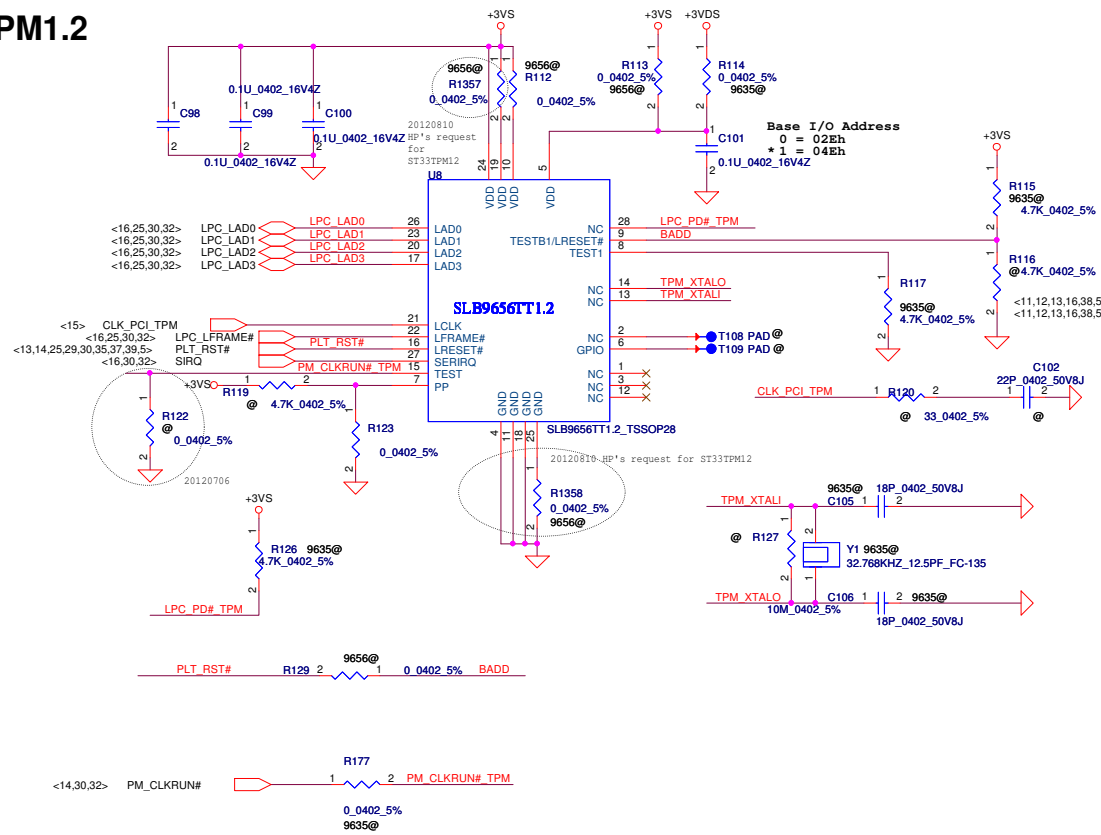
Place C209,C210,CA87,CA89 close to Codec



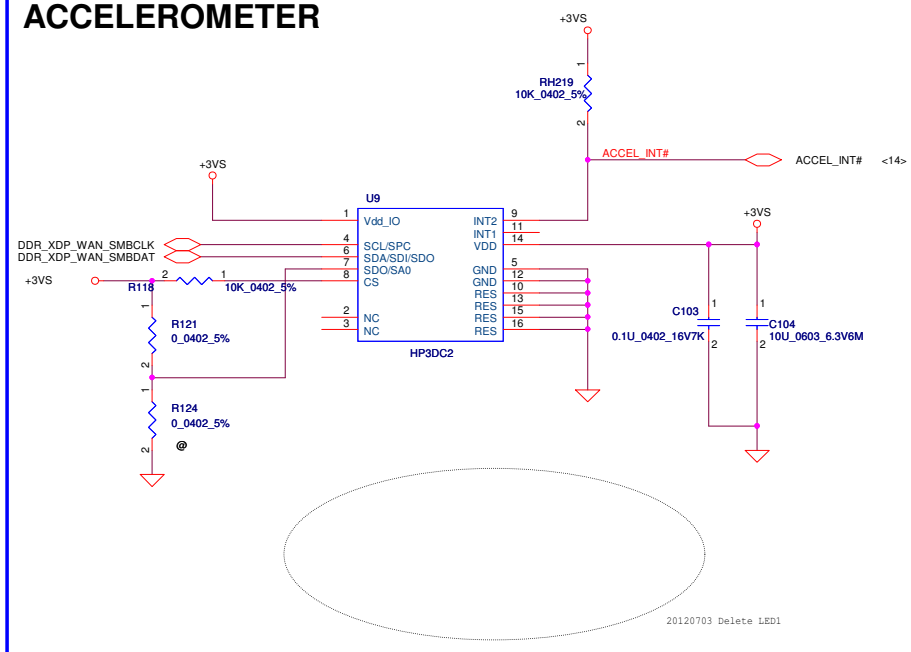
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RA53 need under or near UA1

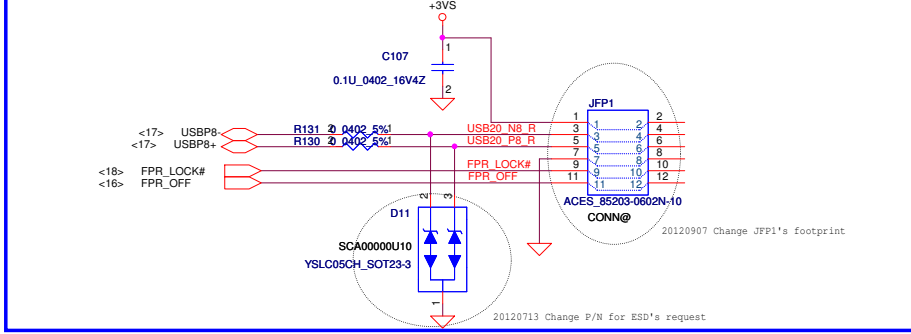
TPM1.2

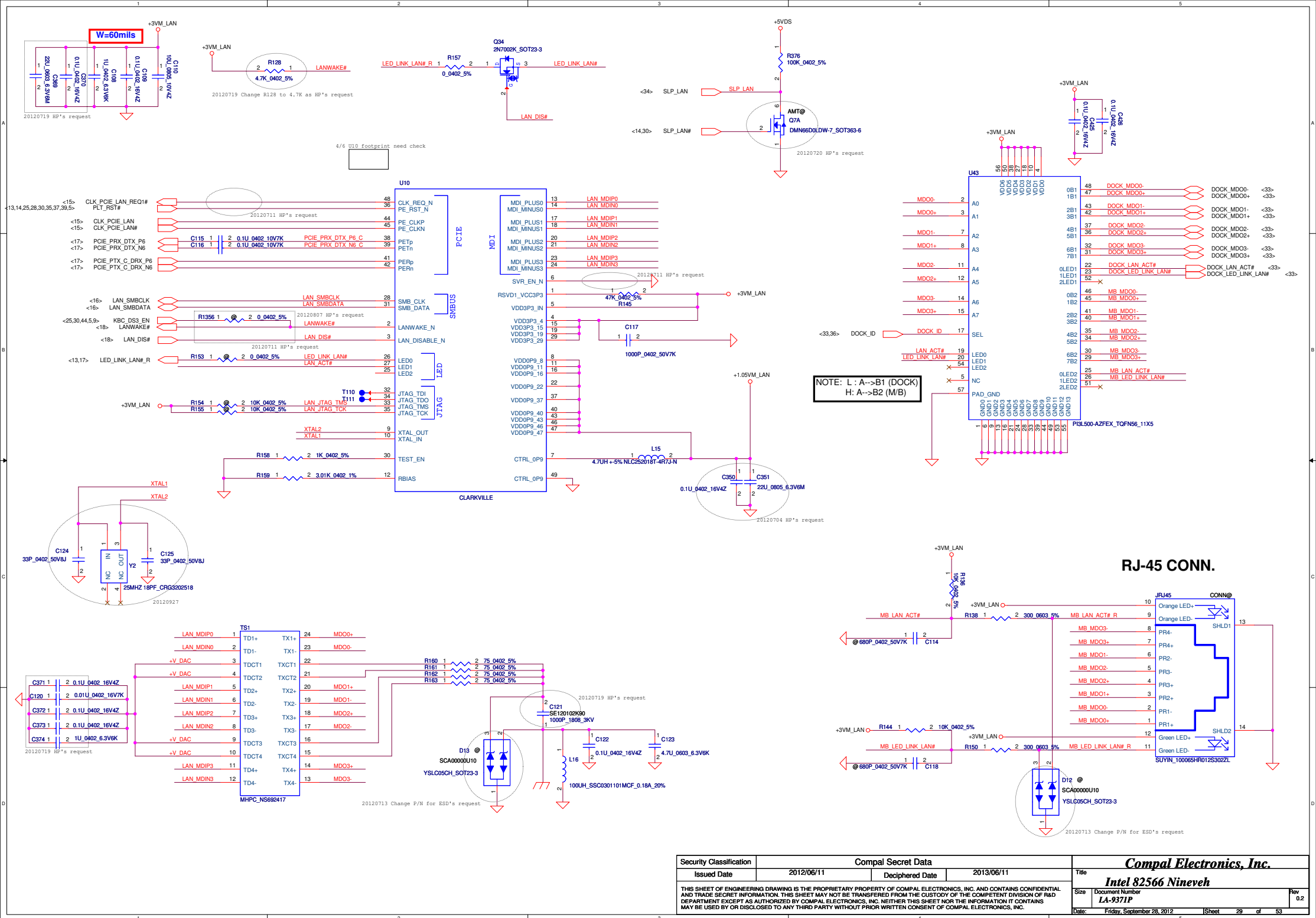


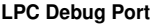
ACCELEROMETER



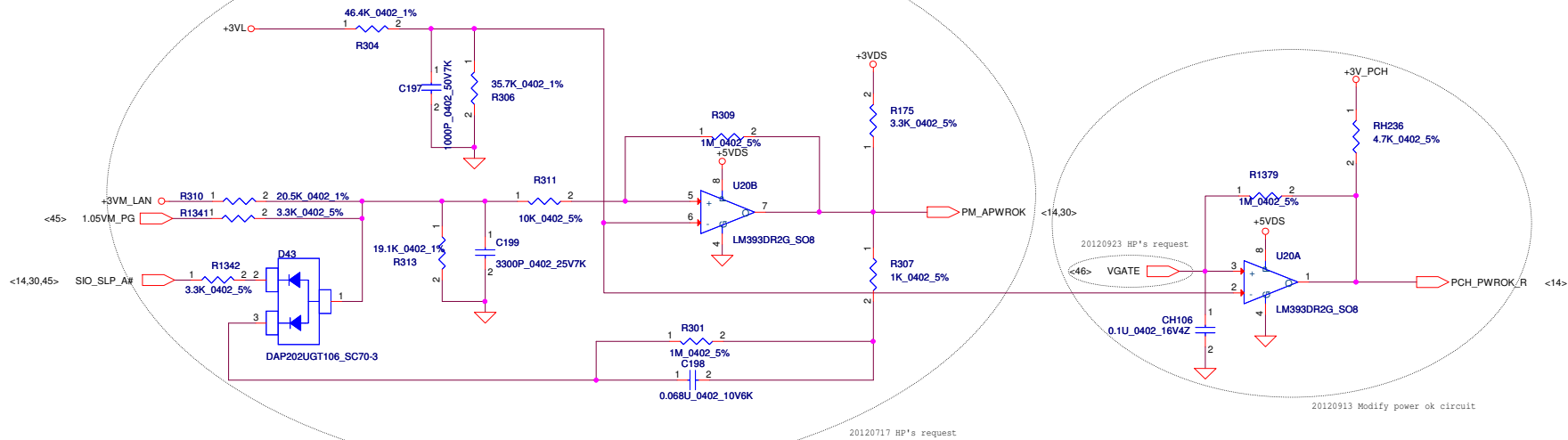
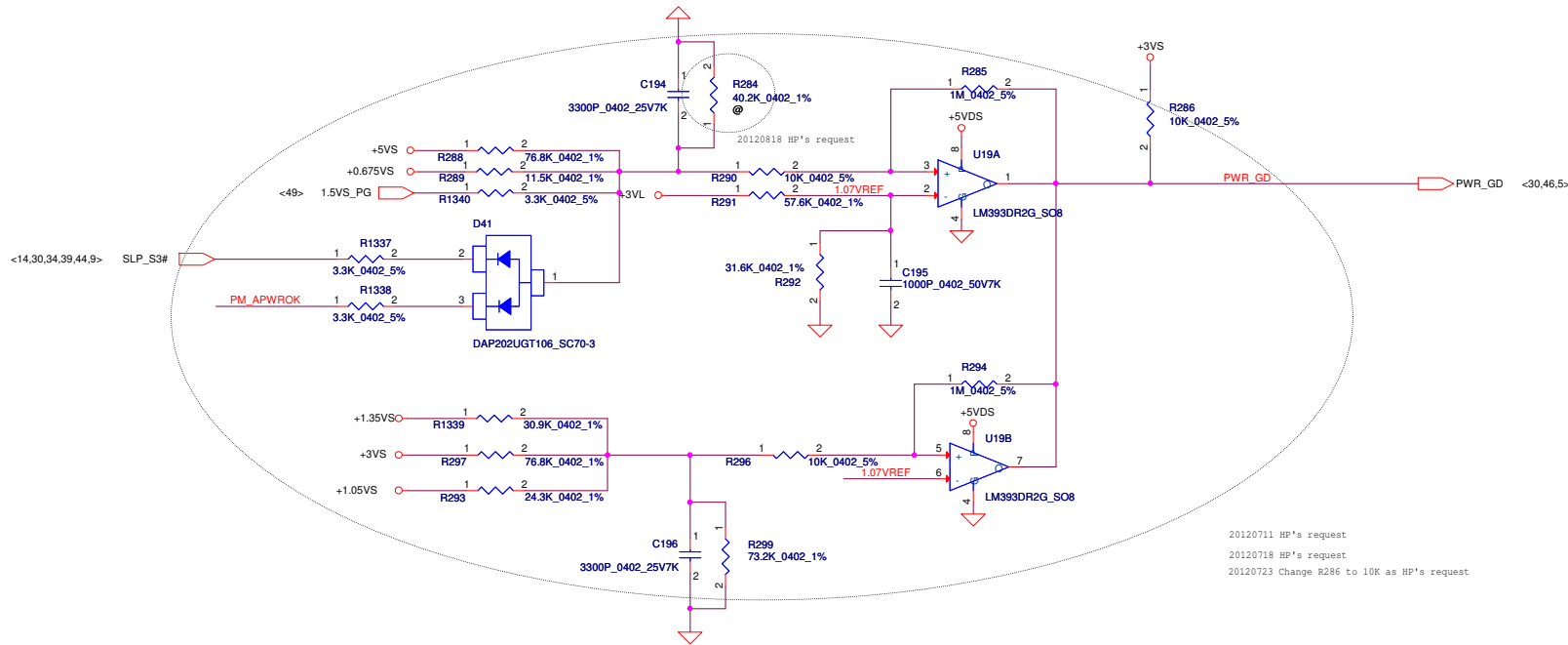
Finger printer





[illegible]

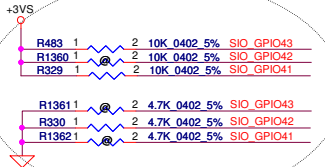
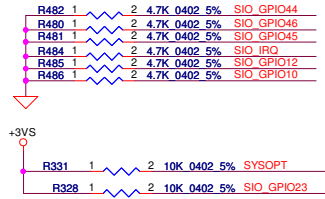
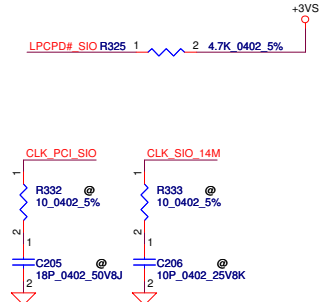
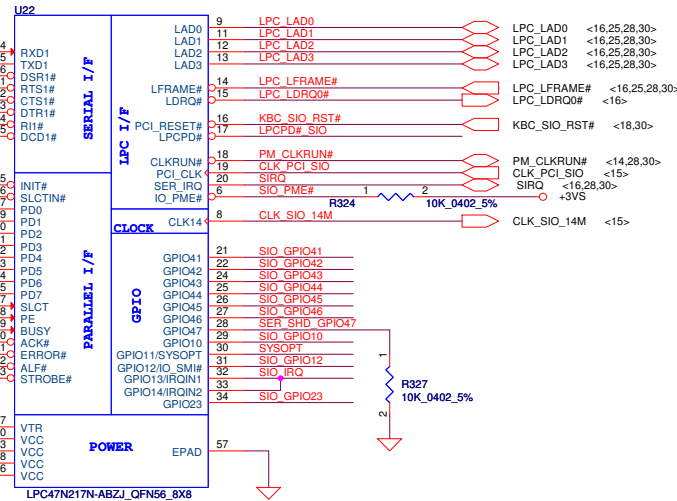
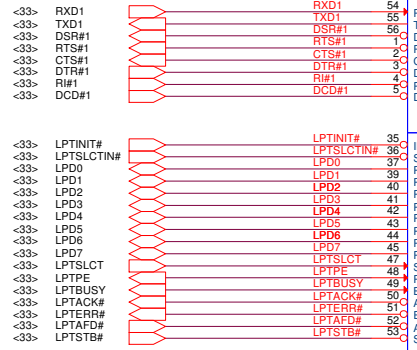
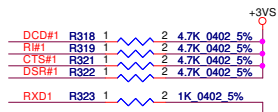
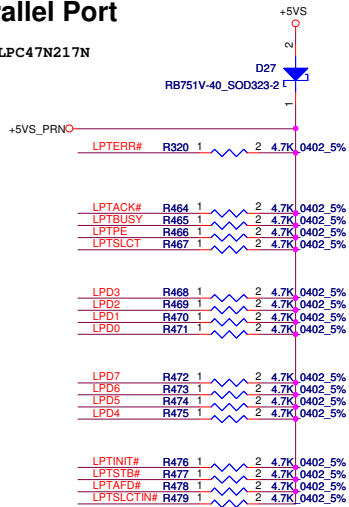
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Parallel Port

TO LPC47N217N



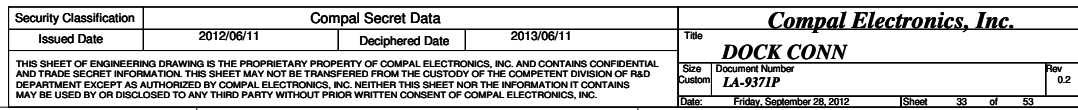
20120720 System ID for HP's request
20120731 System ID for HP's request
20120821 Add R for 2019M & 4019M option

Platform IDs (Super I/O GPIOs)

PLT_ID1	PLT_ID2	PLT_ID3	SYSTEM ID	Series	CPU	Dock	COMMON BIOS
GPIO43	GPIO42	GPIO41					
1	0	1	Afterburner 17" 4 DIMM	W	Haswell	Common	8
1	1	1	Afterburner 17" 2 DIMM	W	Haswell	Common	8

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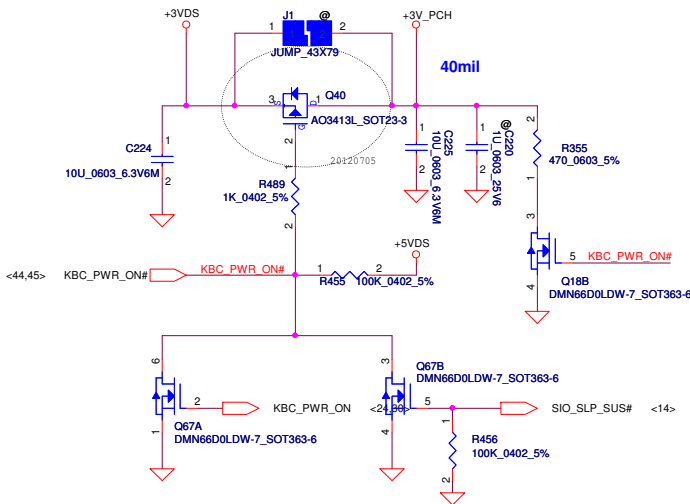
DOCKING CONNECT



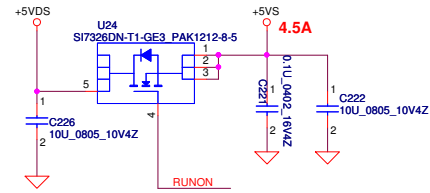
IN	NC<-->COM	NO<-->COM
L	ON	OFF
H	OFF	ON

+3VALW TO +3VALW(PCH AUX Power)

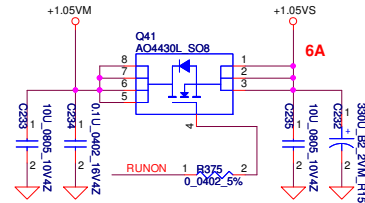
Short J1 for PCH VCCSUS3.3



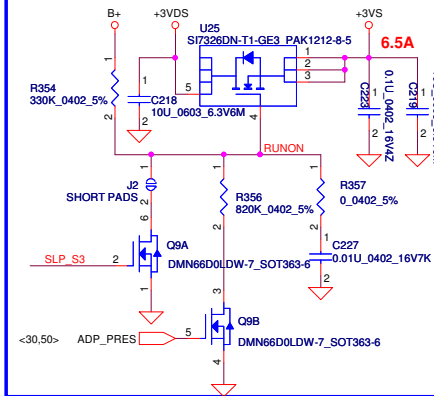
+5VALW to +5VS Transfer



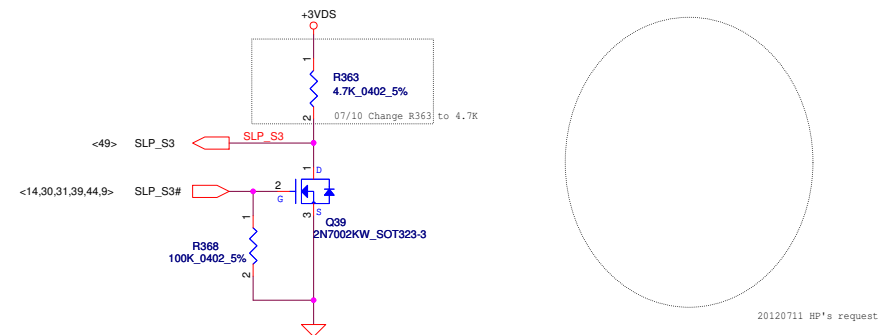
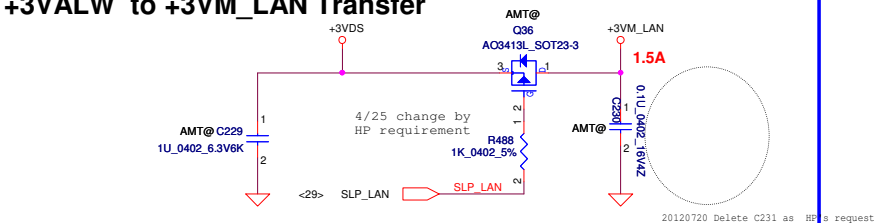
+1.05VM to +1.05VS Transfer



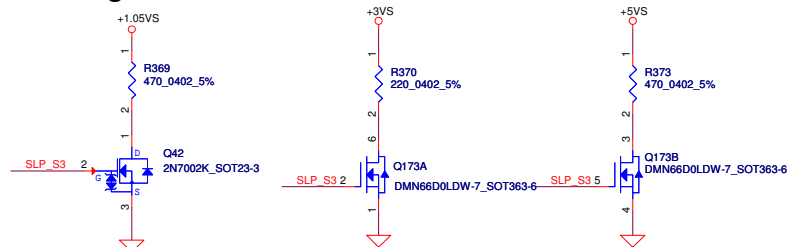
+3VALW to +3VS Transfer



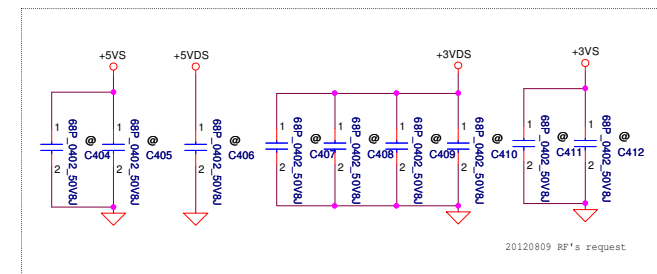
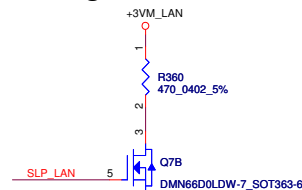
+3VALW to +3VM_LAN Transfer



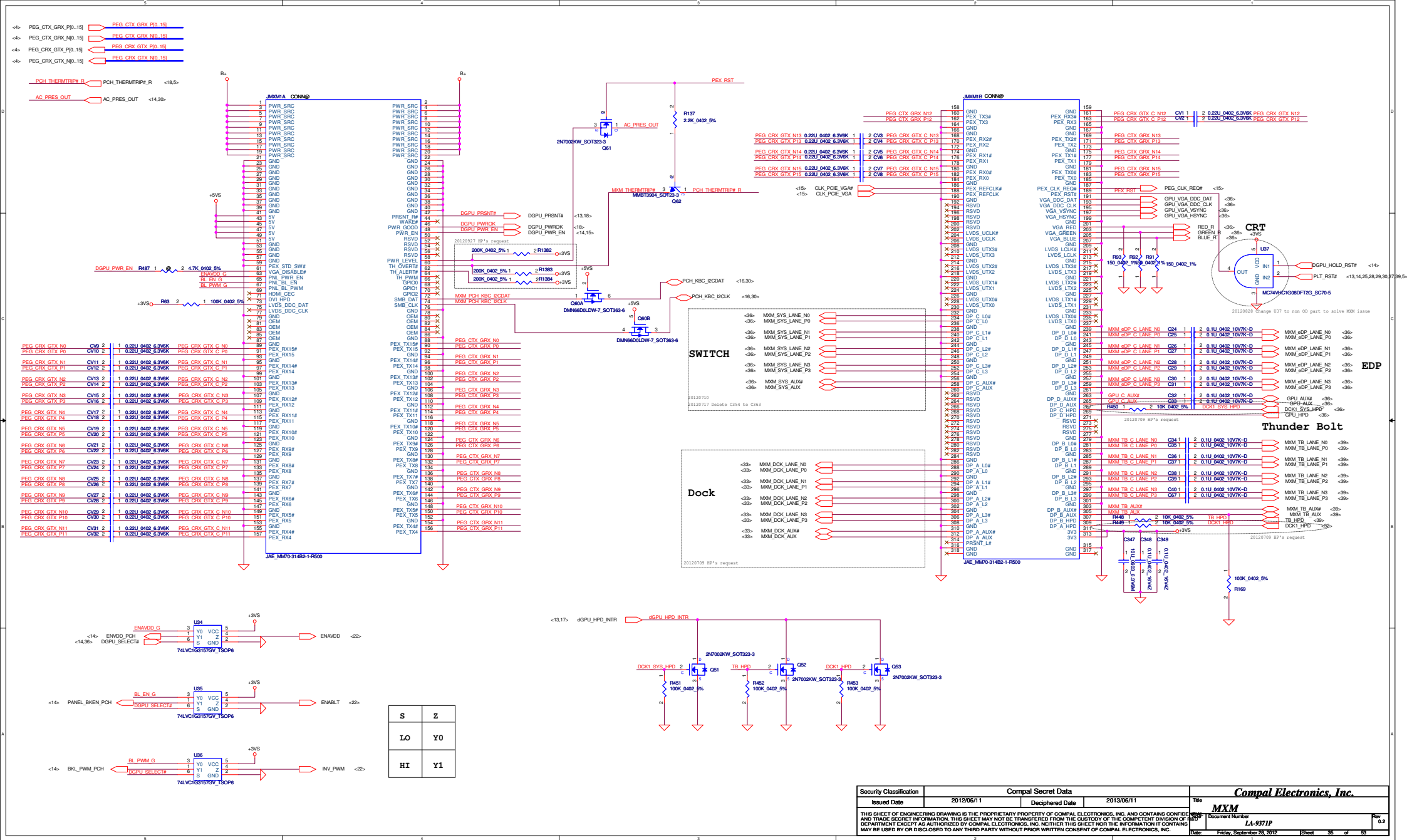
Discharge circuit-1



Discharge circuit-2 for V-M

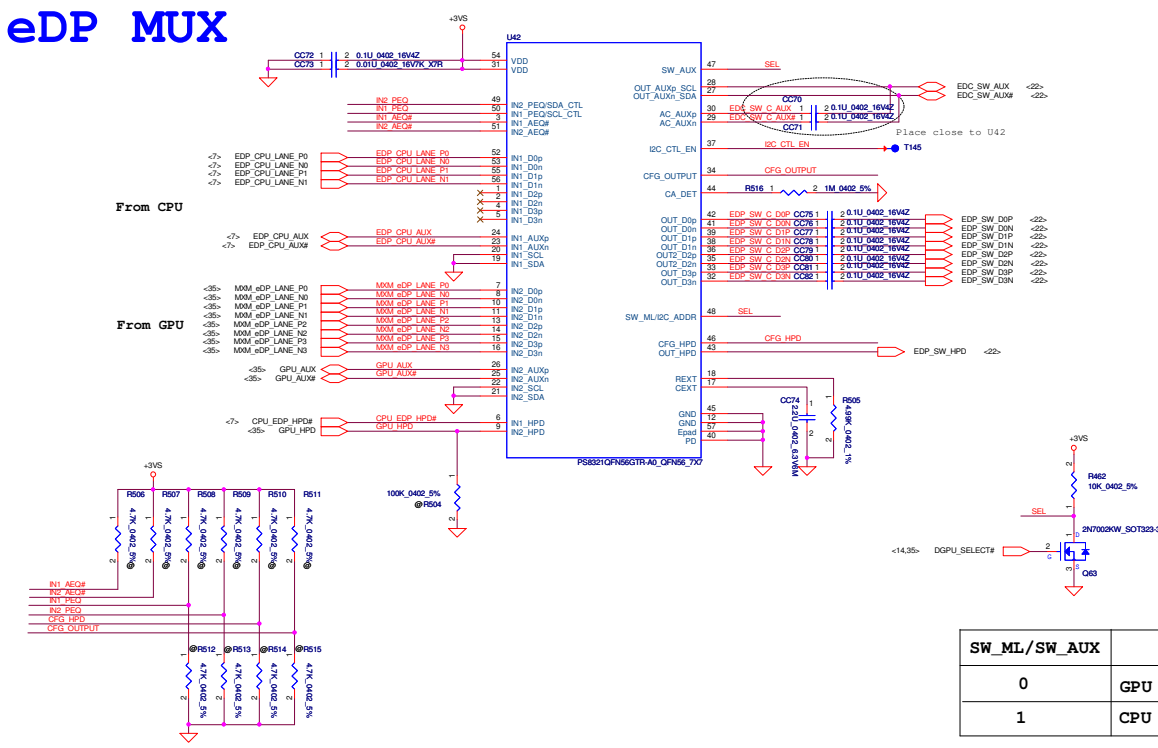


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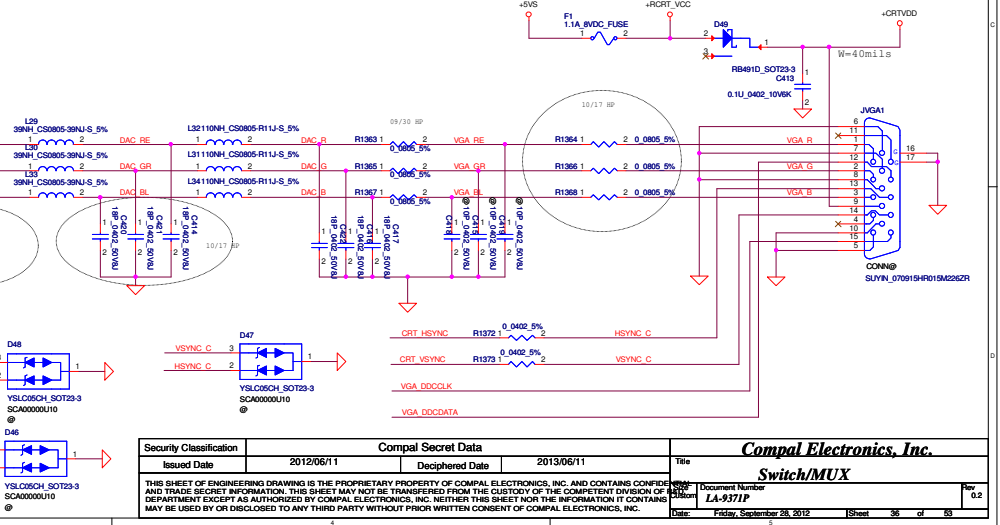
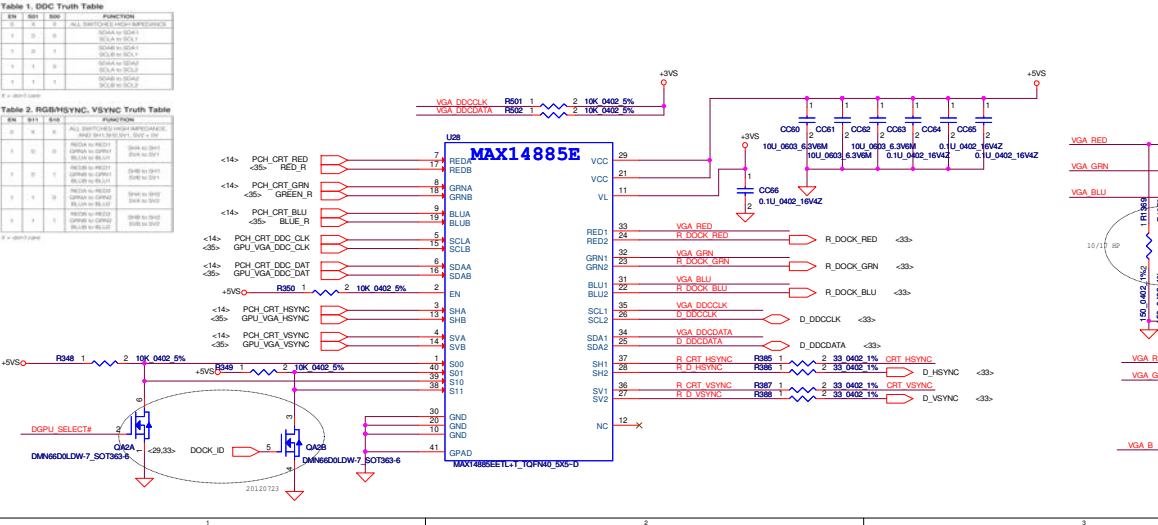
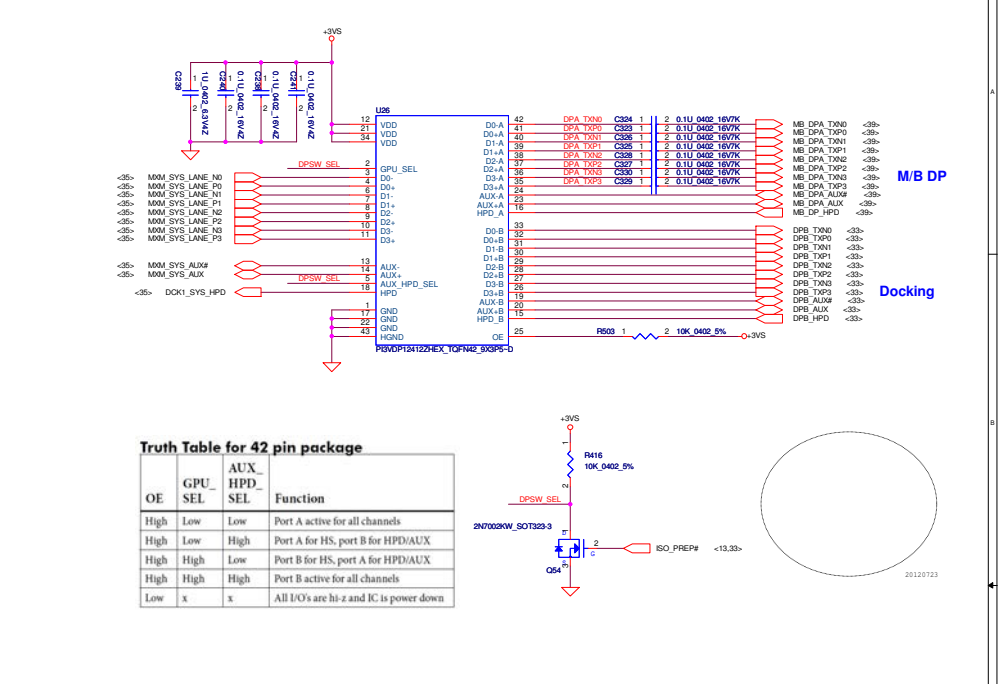


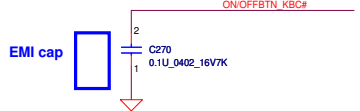
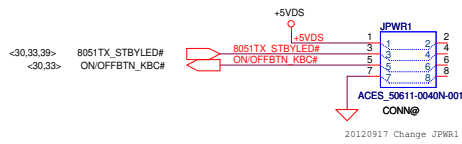
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eDP MUX

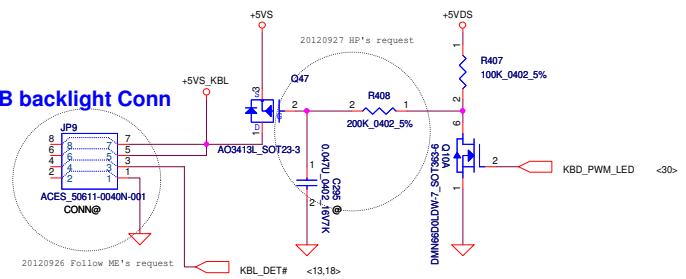


DP Switch

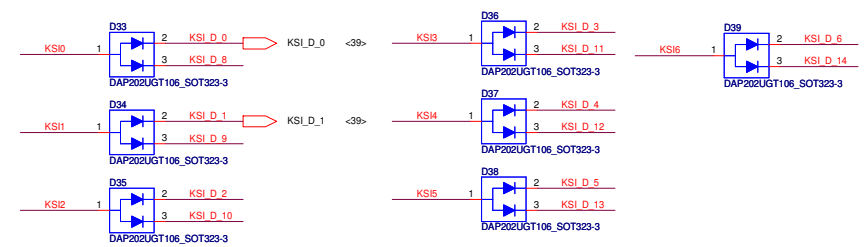
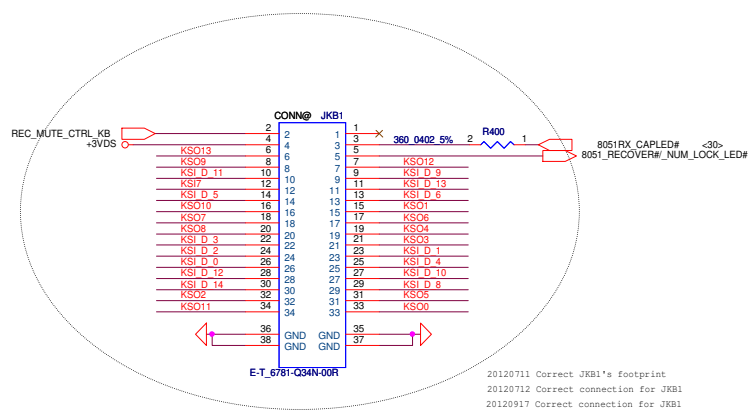
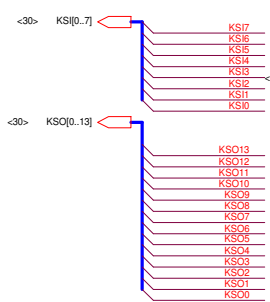
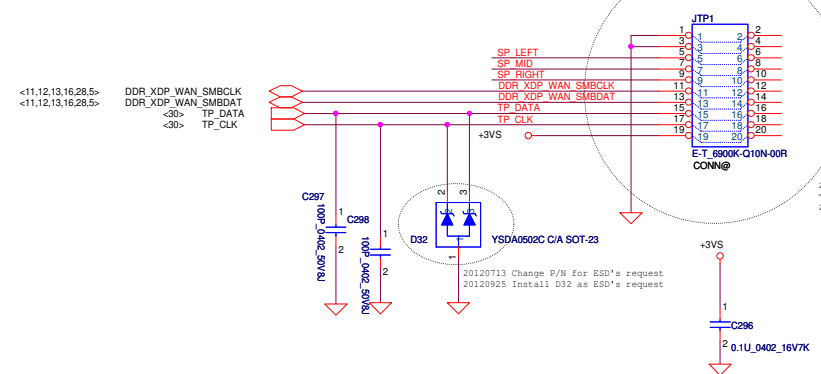




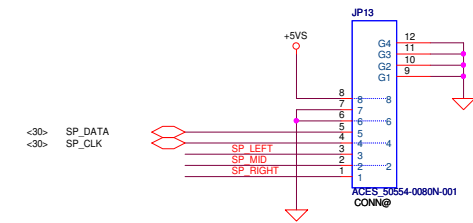
KB backlight Conn



TP/B TO M/B

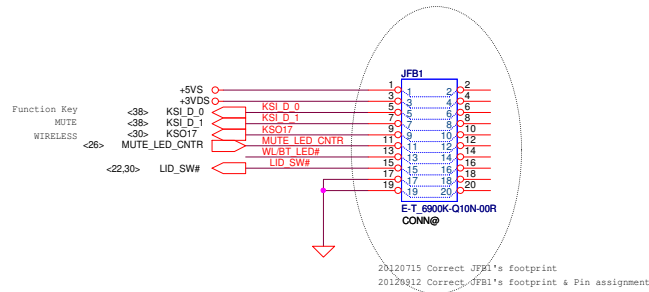


Stick Point CONN

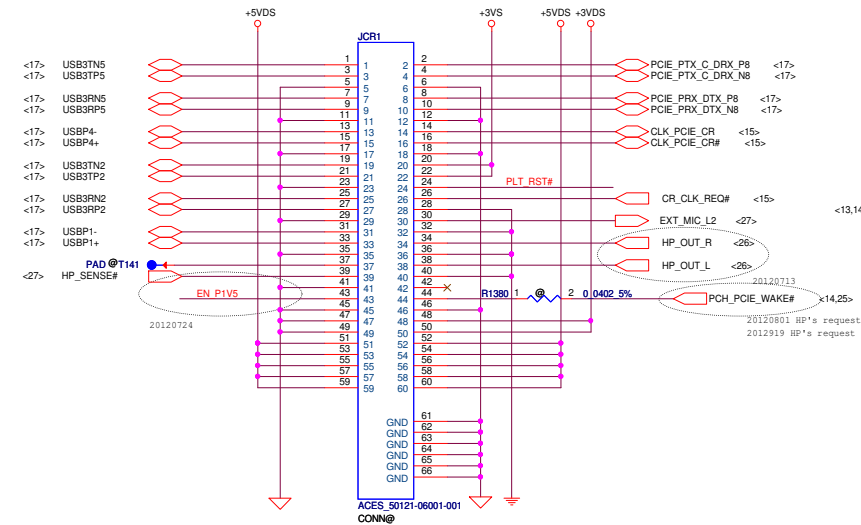


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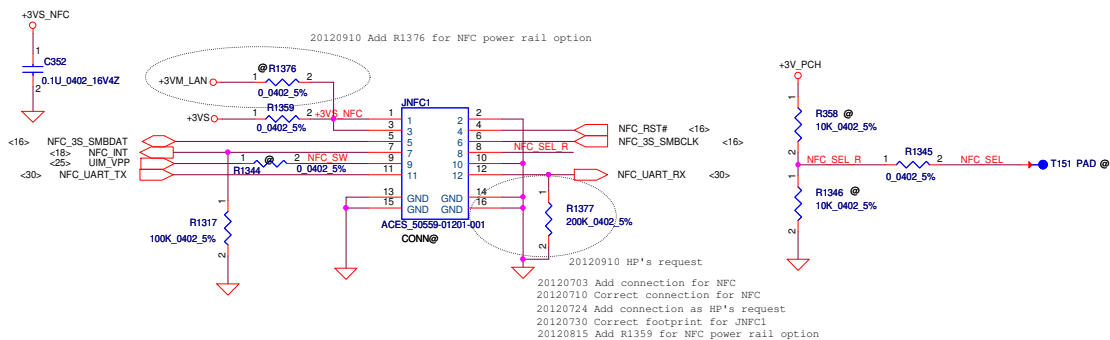
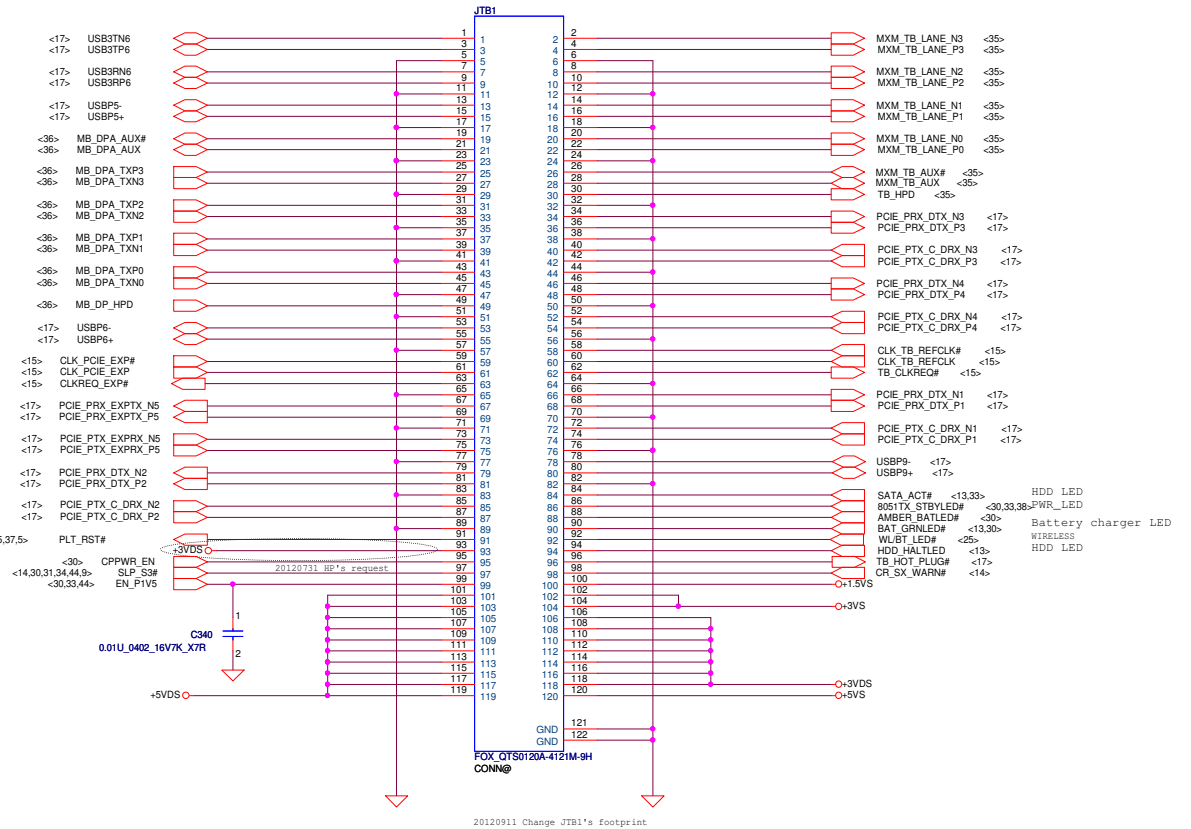
Function Board



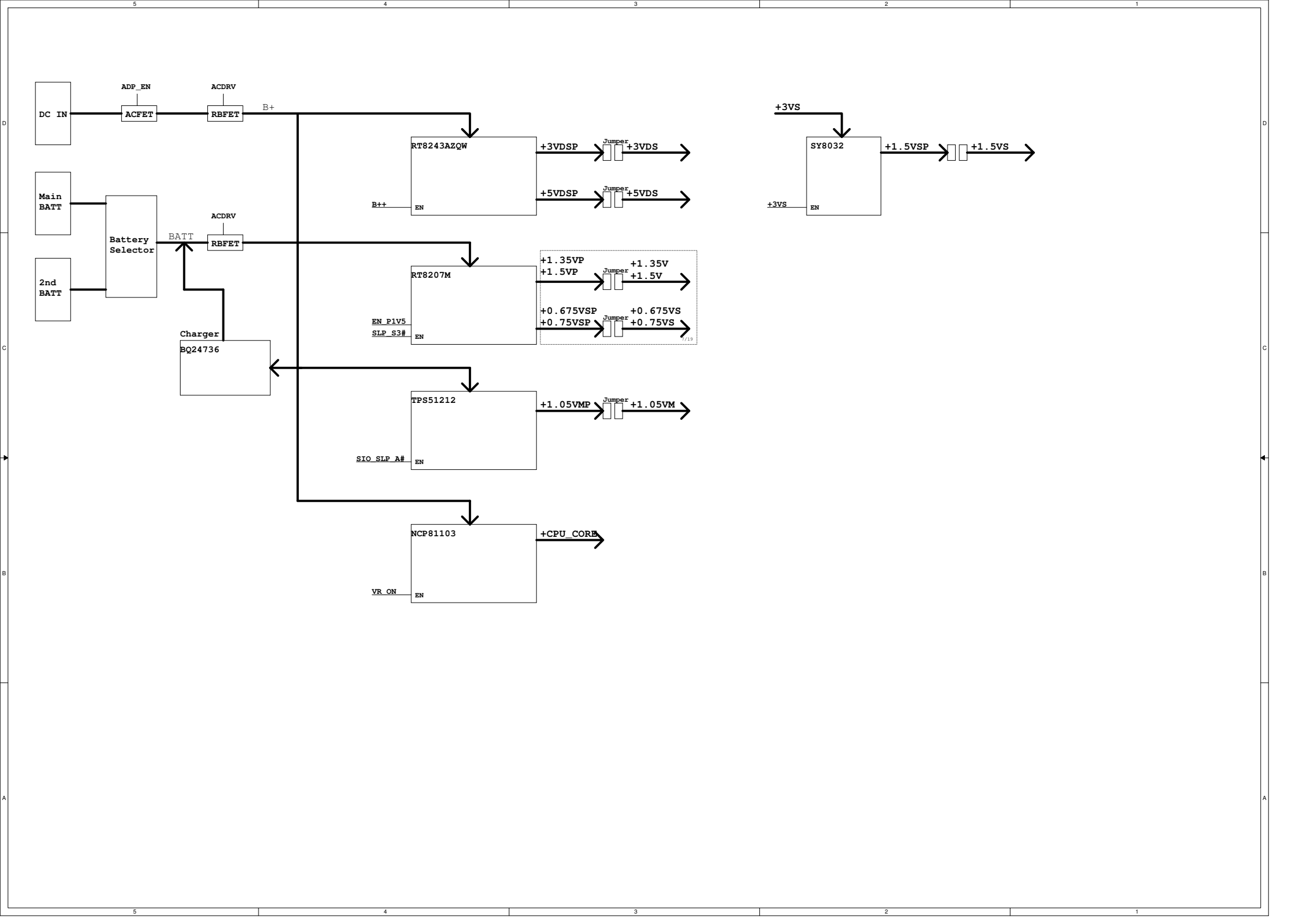
USB & Card Reader Board

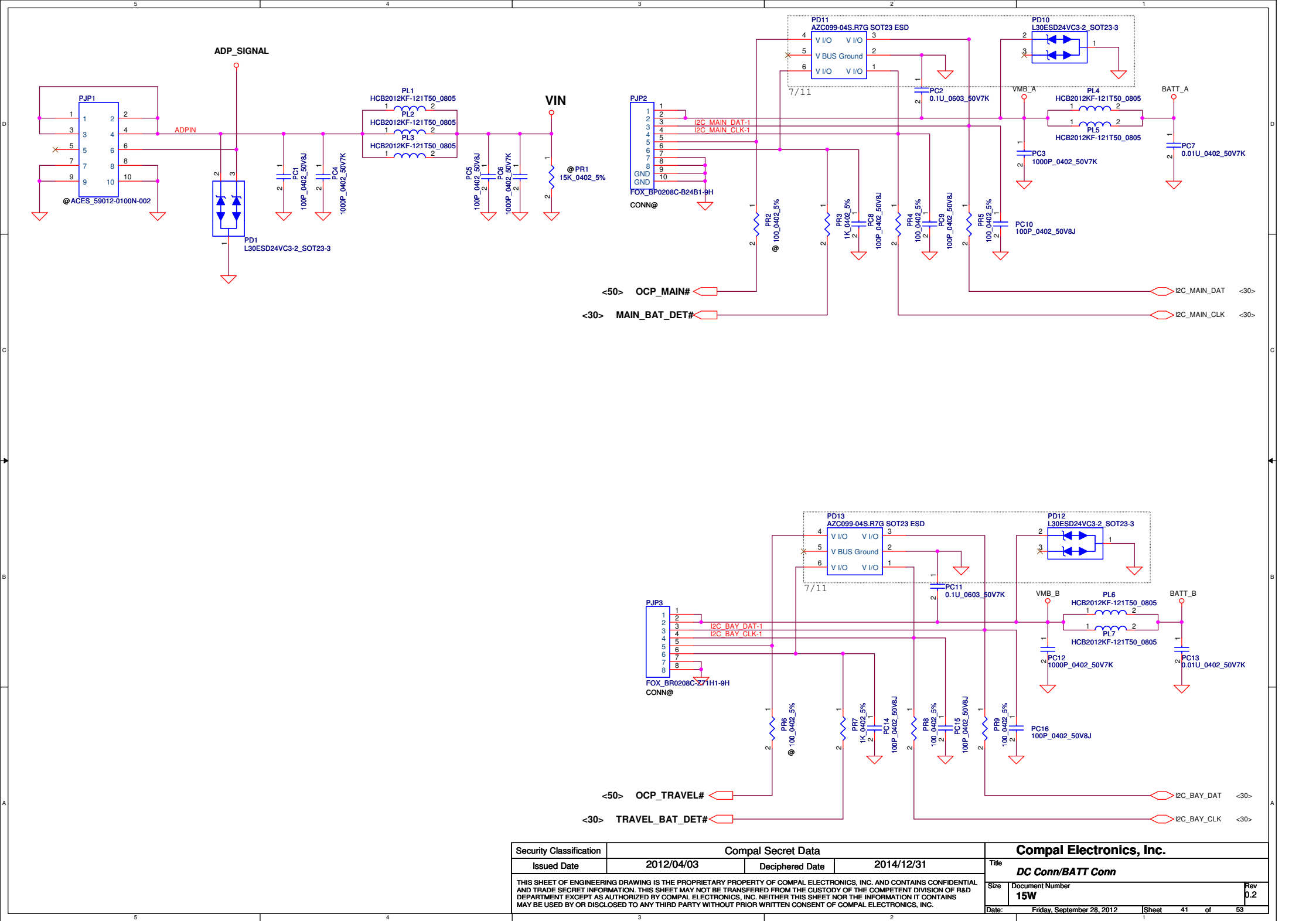


Thunderbolt

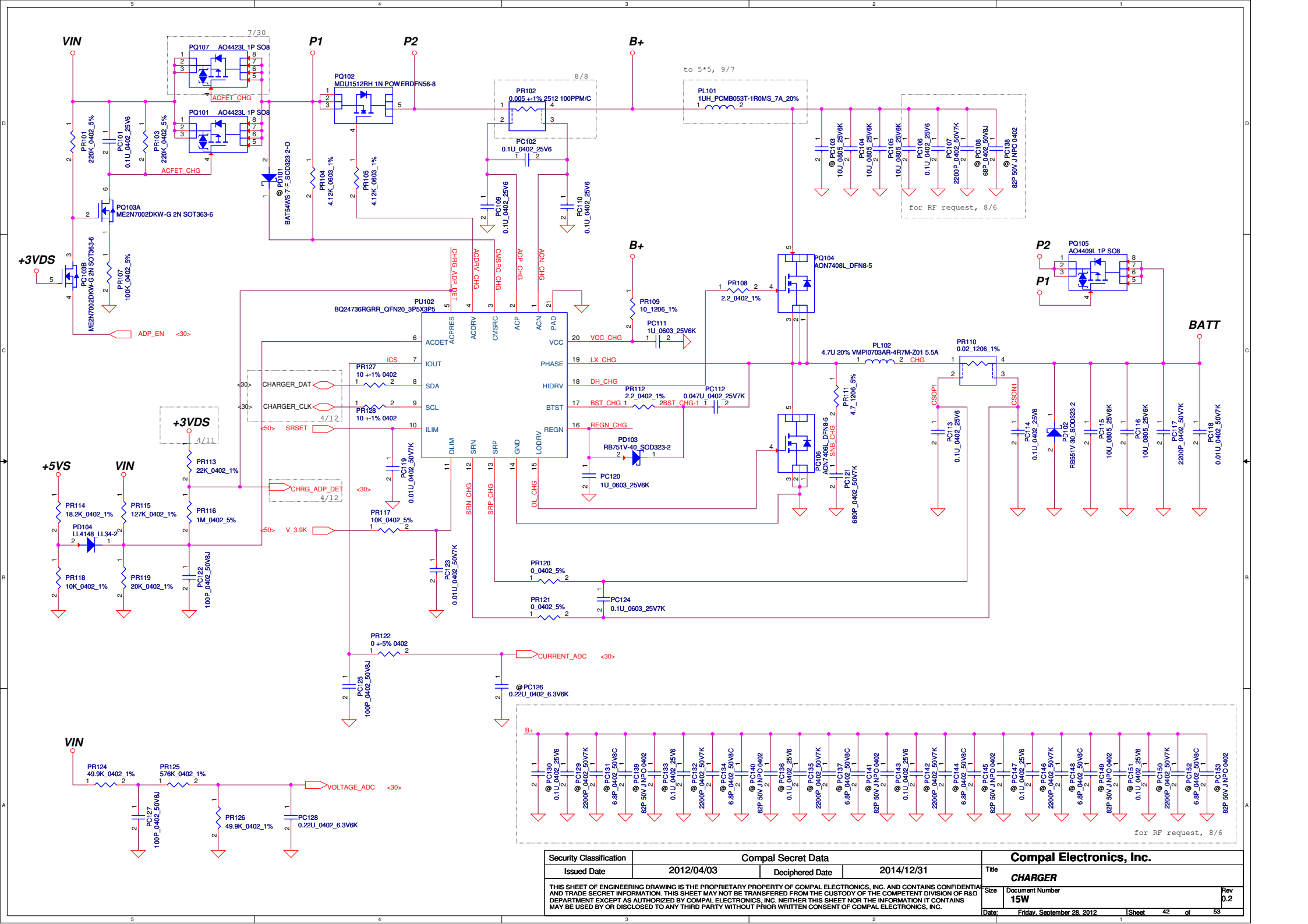


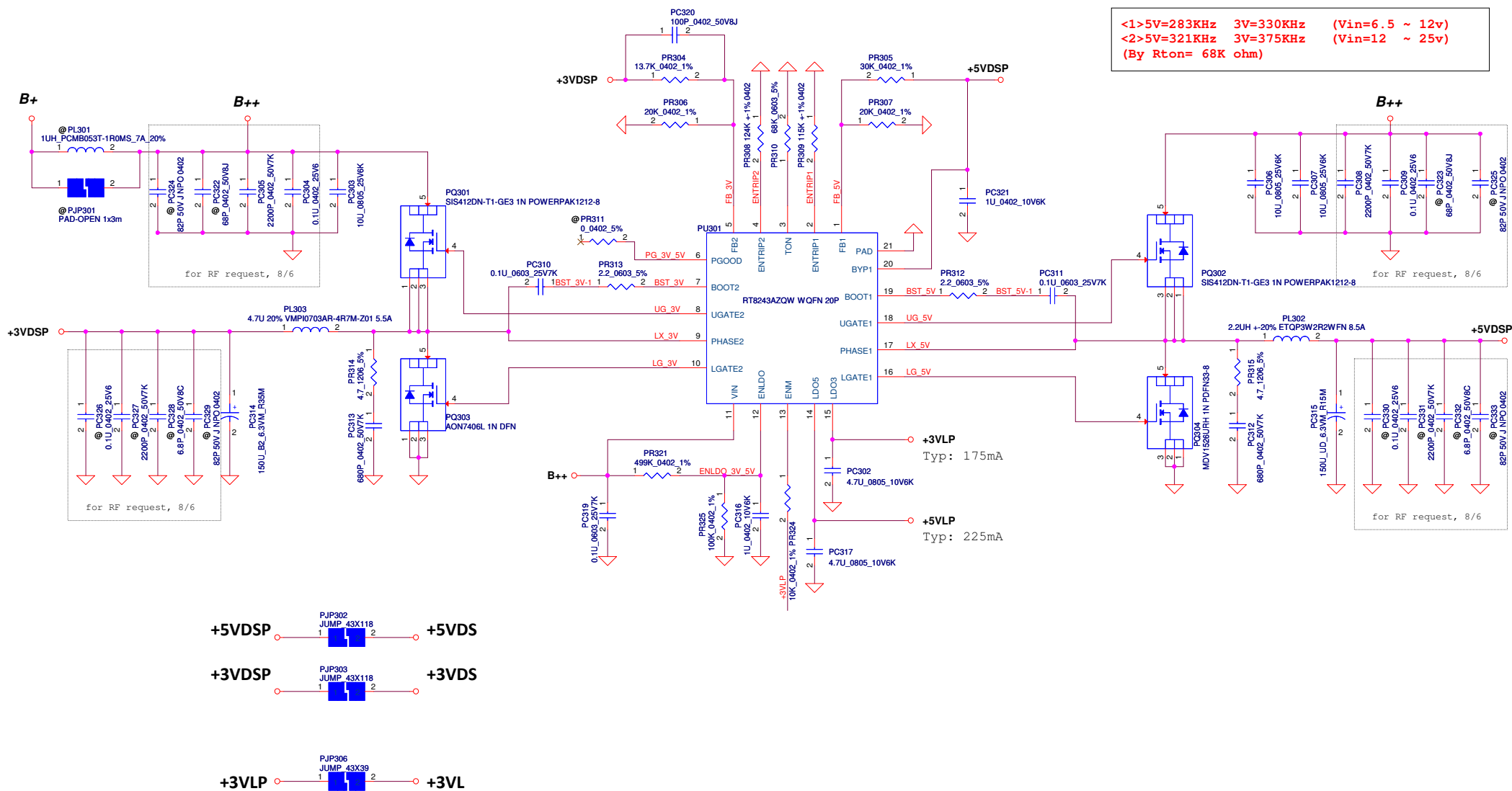
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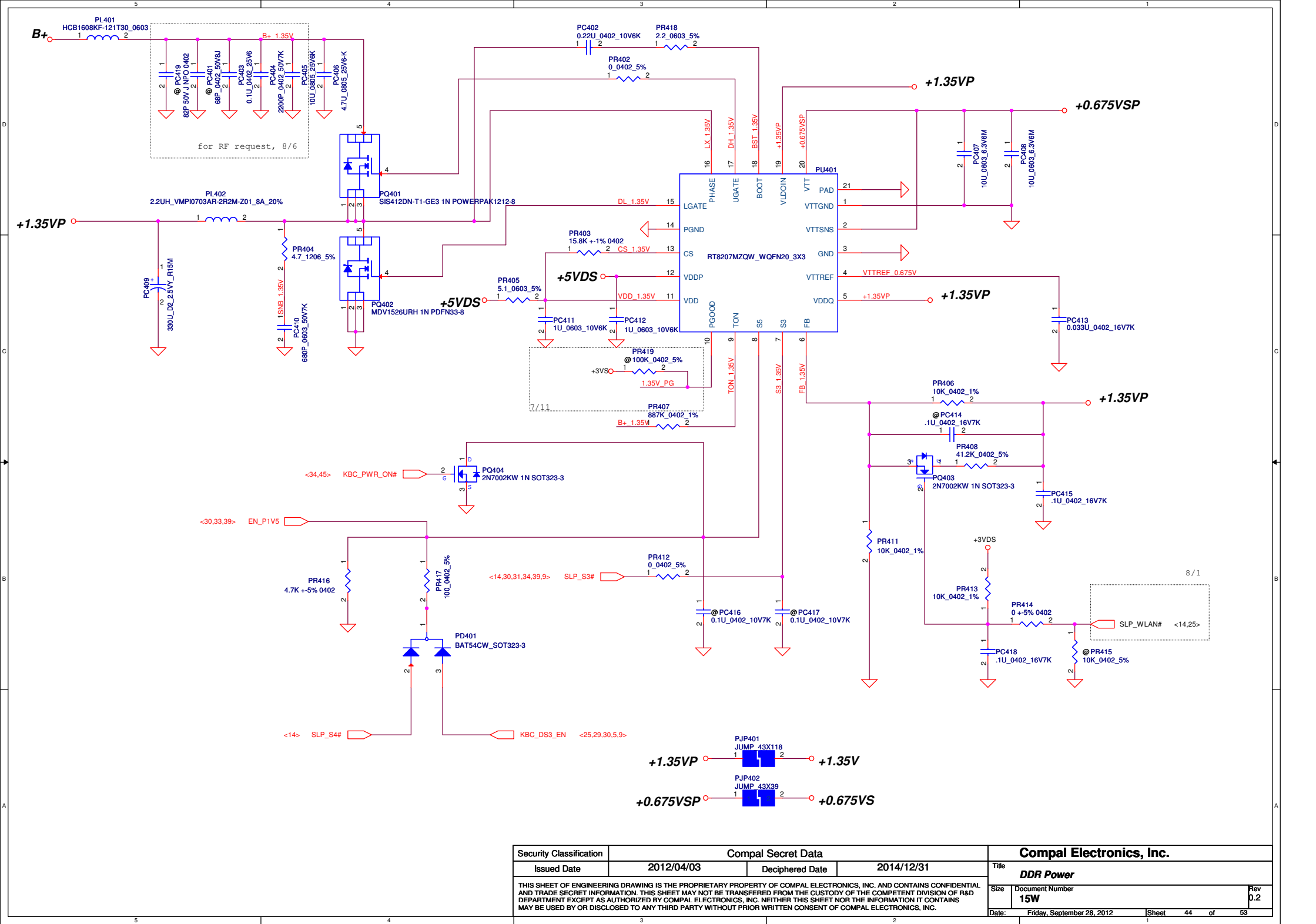


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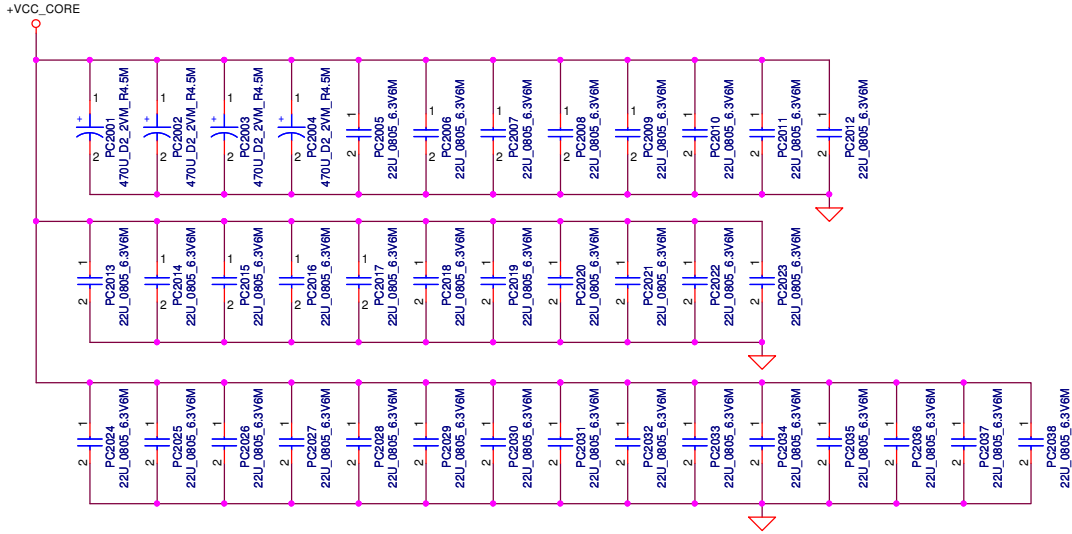


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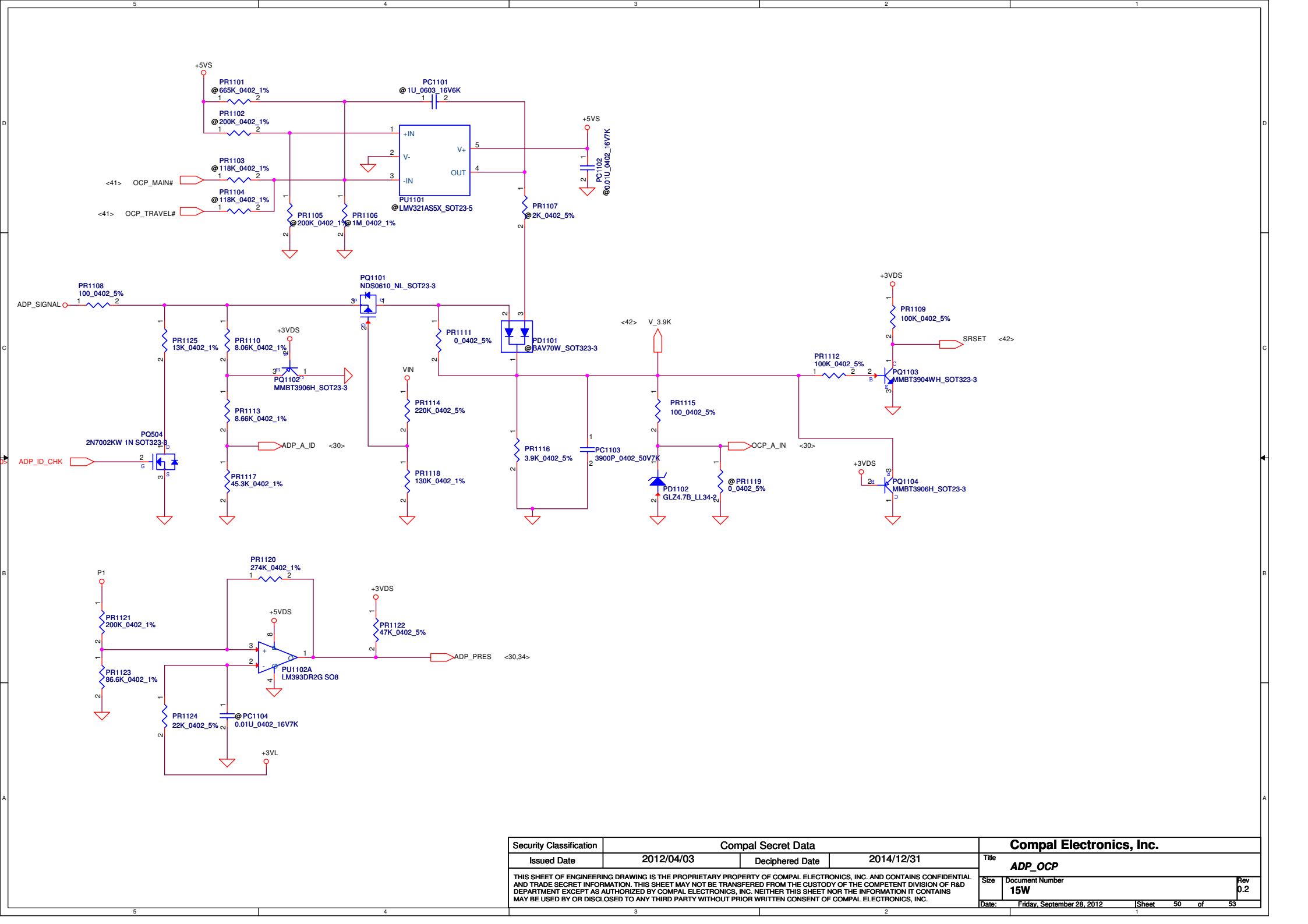


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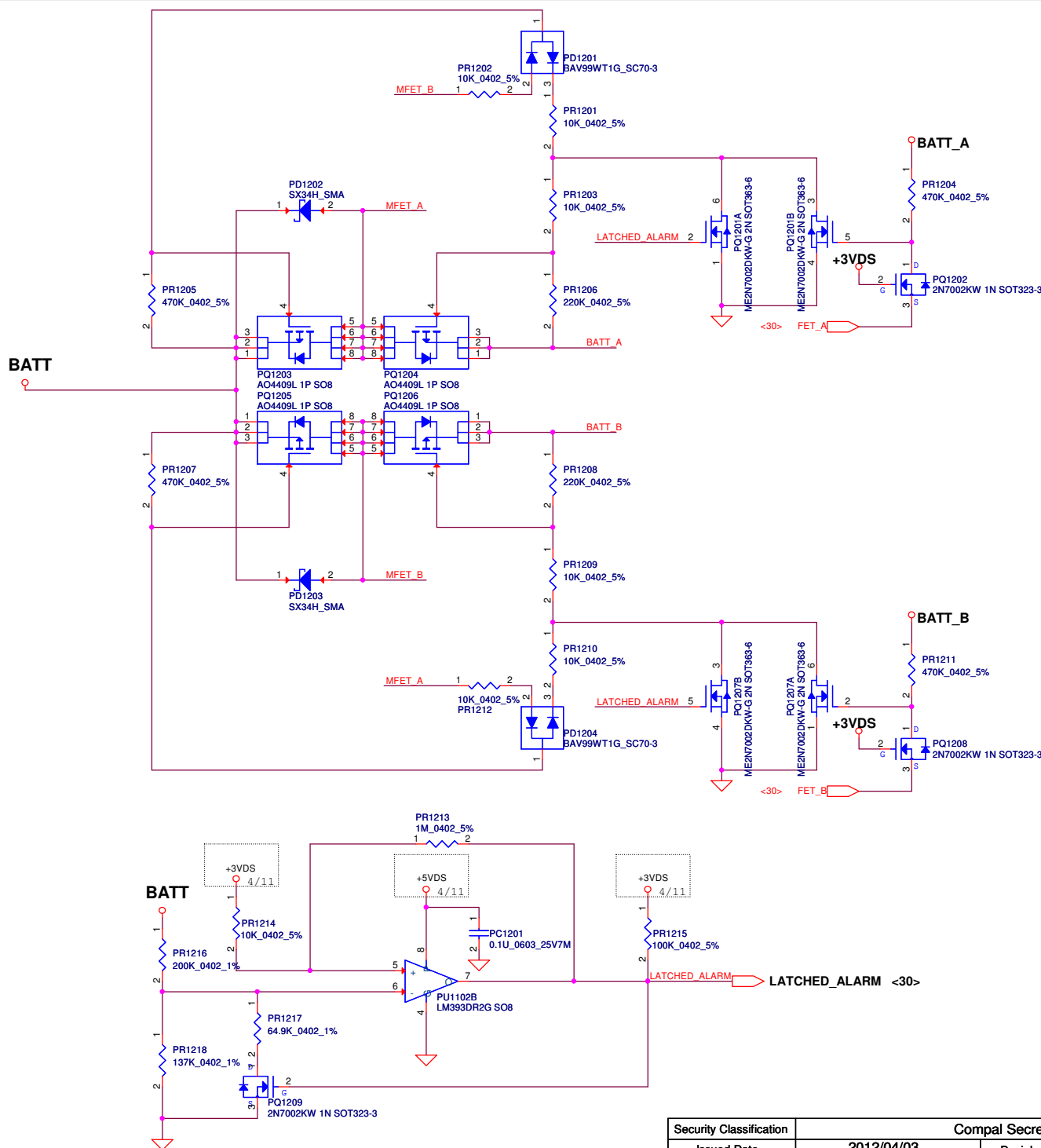
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Version Change List (P. I. R. List) for HW Circuit

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	30	KBC	08/18	HP	The quad-mode does not require any GPIO from KBC	Delete R1348 & R1349 and Add R541 and R542	0.2
2	31	PWR_OK	08/18	HP	Makes the power good circuit working.	Non-install R284	0.2
3	26	MXM	08/28	Compal	MXM Card can't be recognized in OS.	Change U37 to MC74VHC1G08DFT2G (Non-OD type)	0.2
4	36	Switch/MUX	09/07	HP	Move D-Sub connector on M/B	Add VGA filter circuit and connector	0.2
5	30	KBC	09/08	HP	SUSCLK is off during DS3 condition	Add Y4, C423, C424 ; Delete R258, R264	0.2
6	30	KBC	09/08	HP	Simplify the KBC solution for MEC1322	Delete R262, R266, R219, R216, R241, R242, R271, R253	0.2
7	25	NGFF	09/08	HP		Add PU resistor for WWAN_FULL_PWR/WWAN_RSVD2	0.2
8	39	NFC	09/10	HP	KBC detection of NFC module	Add 200K (R1377) PD resistor to NFC_VARI_RX	0.2
9	39	NFC	09/10	HP	Power rail option for NFC module	Add +3VM_LAN (R1376) for NFC module	0.2
10	9	CPU	09/11	HP		Remove RC102 and RC103	0.2
11	20	PCH	09/11	HP	Connect PCH's pin AD12 to +3V_PCH directly	Remove RH226	0.2
12	5	CPU	09/11	HP	Connect CPU_AT26 pin to CPU_PLTRST# directly	Remove RC66	0.2
13	5	CPU	09/11	HP	Connect CPU_AL34 pin to H_CPU_PWRGD directly	Remove RC30	0.2
14	9	CPU	09/11	HP	Connect SLP_S3# to QC5.5 directly.	Remove RC93	0.2
15	33	DOCKING	09/11	HP	Connect EN_P1V5 to JDOCK1.140 directly.	Remove R351	0.2
16	33	DOCKING	09/11	HP	Connect ON/OFFBTN_KBC# to Docking directly.	Remove R336	0.2
17	15	PCH	09/11	HP	Simplify PCH solution for PCIE CLK Group	Remove RH107, RH103, RH114, RH116, RH122 RH124, RH126, RH127, RH129, RH130	0.2
18	14	PCH	09/11	HP	Reassignment GPIO for "BT_OFF"	Change it from GPIO72 to GPIO61	0.2
19	30	KBC	09/11	HP	Reserve for SUSACK# signal	Uninstall R436 and add R1378	0.2
20	18	PCH	09/11	HP	Reassigned BRD_ID4 to GPIO40 for CP support and update table for DB1-R	Connect RH180.1 to +3VS & RPH1.8 to GND	0.2
21	30	KBC	09/12	HP	Simplify the KBC solution for MEC1322	Delete R249, R251, R256, R277	0.2
22	36	Switch/MUX	09/12	HP	eDP trace length over Intel's specification	Change solution to PS8321	0.2

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Version Change List (P. I. R. List) for HW Circuit

<i>Item</i>	<i>Page #</i>	<i>Title</i>	<i>Date</i>	<i>Request Owner</i>	<i>Issue Description</i>	<i>Solution Description</i>	<i>Rev.</i>
D 23	29	LAN	09/12	HP	Avoid IEEE failure with trace stub lines	Add Lan switch solution PI3L500-AZFEX (U43)	0.2
24	39	I/O CONN	09/12	HP	Move Hall sensor IC on Function board	Add +3VDS & LID_SW# pin to JFB1	0.2
25	22	eDP	09/13	Compal	Avoid LVDS Burn out Risk	Rearrange pin assignment of JEDP1	0.2
26	31	POR CKT	09/13	HP	Modify Power OK circuit	Delete UH7, RH235 ; Add R1379	0.2
C 27	39	I/O CONN	09/19	HP	Prevent Card Reader can't be recognized issue	Add R1380 for PCH_PCIE_WAKE#	0.2
28	13	PCH	09/19	HP	Disable the unlock of ME descriptor	Change QH11 to P-MOSFET	0.2
29	37	Smart Card	09/20	HP	RC delay is NOT good as reset	Delete CC67,R393, then connect V30.23 to PLT_RST#.	0.2
C 30	26	CODEC	09/20	HP		Uninstall RA13 and CA20	0.2
31	14	PCH	09/20	HP	KBC appears drives high during S3, so the change to avoid the leakage without losing functionality.	Change RH74 from 10K to 100K Ohm	0.2
32	31	PWR OK	09/23	HP	Modify net name for easy read	Modify VR_ON to PWR_GD and PWR_GOOD_3 to VGATE	0.2
B 33	5	XDP	09/25	HP		Connect PM_PWROK to JXDP1.47 via 0 Ohm (RC107)	0.2
34	30	KBC	09/25	HP	Resolve ME LAN failures	Delete R537, Q73, D21	0.2
35	35	MXM	09/27	HP	There is yellow bang in device manager	Add pull high resistor (R1382,R1383 & R1384) to +3VS	0.2
B 36	38	KB Backlight	09/27	HP		Change R408 to 200K Ohm, and uninstall C295	0.2
A 							

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