Compal Confidential

Schematics Document

AMD/S1/ATI RS485M(C)/SB460

2005 / 12 / 30 Rev:0.1

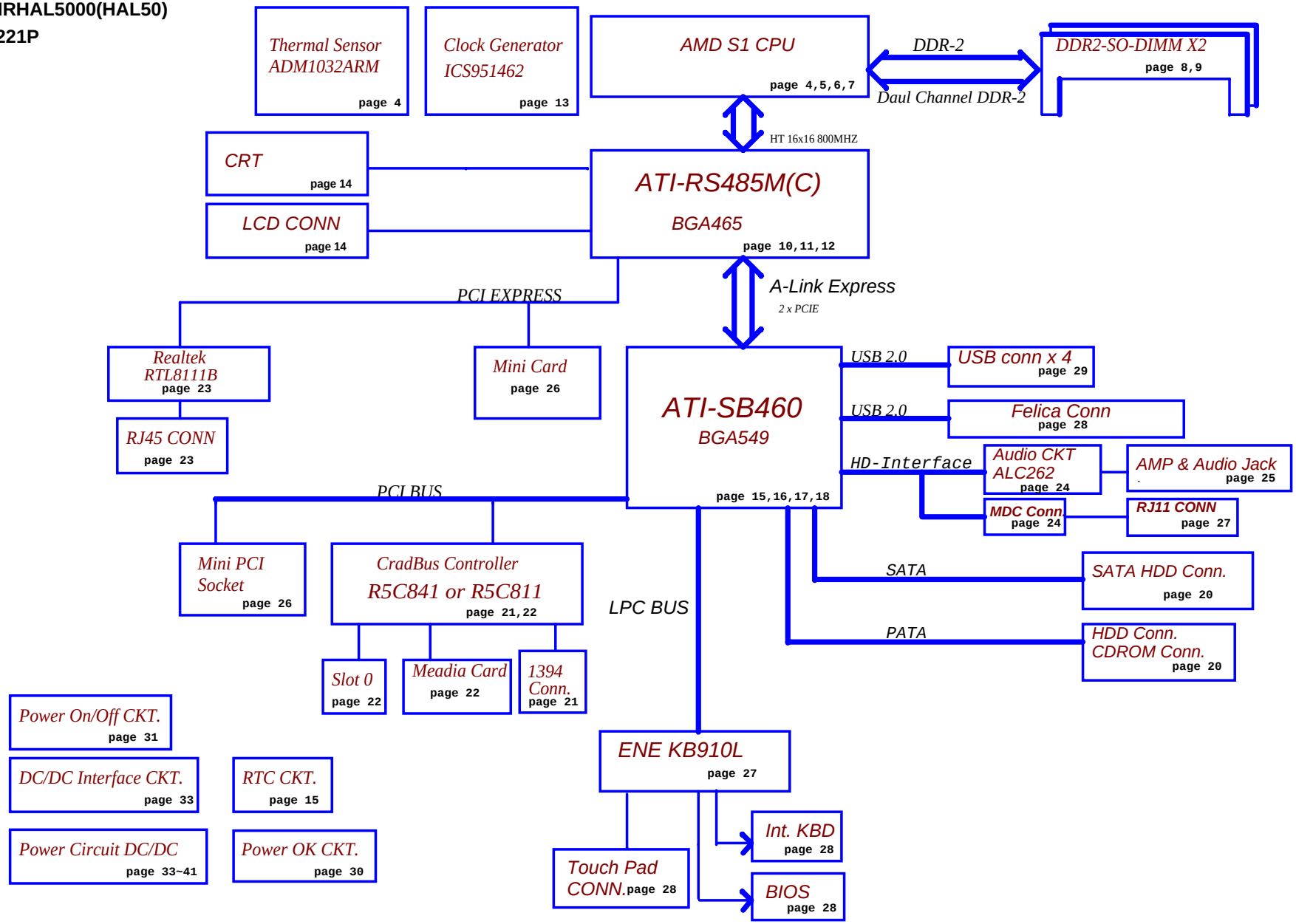
Security Classification	Compal Secret Data		
Issued Date	2005/12/1	Deciphered Date	2006/12/01

Title	Cover Sheet	
Size: Custom	Document Number: LA-3221P	Rev: 0.1
Date: Friday, January 06, 2006	Sheet 1 of 43	

Compal confidential

Project Code: ANRHAL5000(HAL50)

File Name : LA-3221P



Security Classification	Compal Secret Data		
Issued Date	2005/12/1	Deciphered Date	2006/12/01

Title	Block Diagrams		
Size: Custom	Document Number: LA-3221P		Rev: 0.1
Date: Friday, January 06, 2006	Sheet 2 of 43		

Voltage Rails

Power Plane	Description	S1	S3	S4/ S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+1.2V_HT	1.2V switched power rail	ON	OFF	OFF
+0.9V	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.8VALW	1.8V always on power rail	ON	ON	ON
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	ON
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD21	0	PIRQE/PIRQF/PIRQG
Mini-PCI	AD22	1	PIRQF/PIRQG

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b?
EEPROM(24C16/02)	1010 000X b?
(24C04)	1011 000Xb?

EC SM Bus2 address

Device	Address
ADM1032	1001 110X b?

SB460 SM Bus address

Device	Address
Clock Generator (ICS 951462AGT)	1101 001Xb?
DDRII DIMM0	1001 000Xb?
DDRII DIMM2	1001 010Xb?

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra / Rc	100K +/- 5%

Board ID	Rb / Rd	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

BTO Option Table

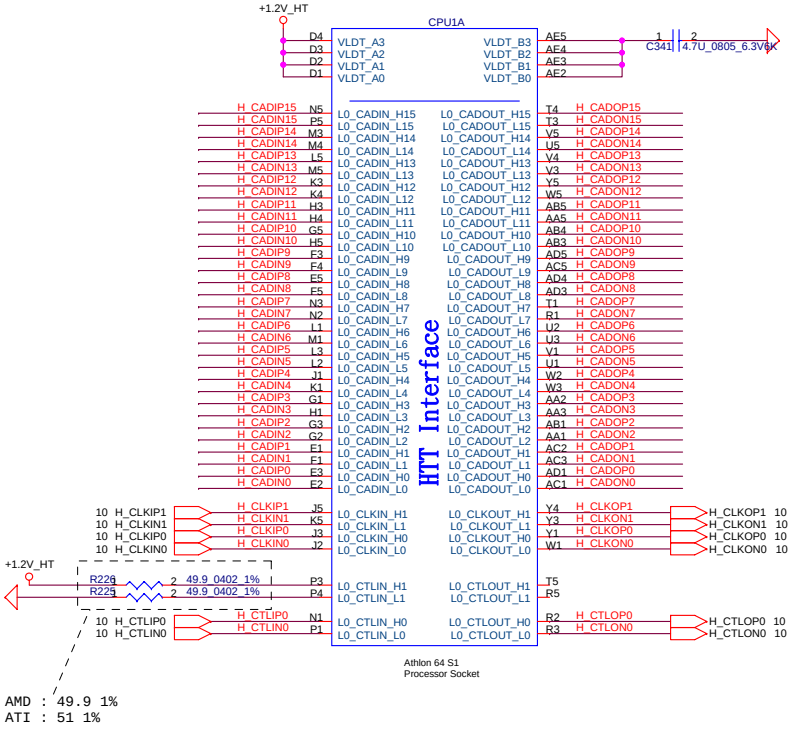
BTO Item	BOM Structure

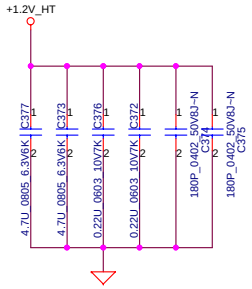
Title	Notes		
Size: Custom	Document Number: LA-3221P		Rev: 0.1
Date: Friday, January 06, 2006	Sheet 3 of 43		

10 H_CADIP[0..15] — H_CADIP[0..15]
10 H_CADIN[0..15] — H_CADIN[0..15]
H_CADOP[0..15] — H_CADOP[0..15] 10
H_CADON[0..15] — H_CADON[0..15] 10

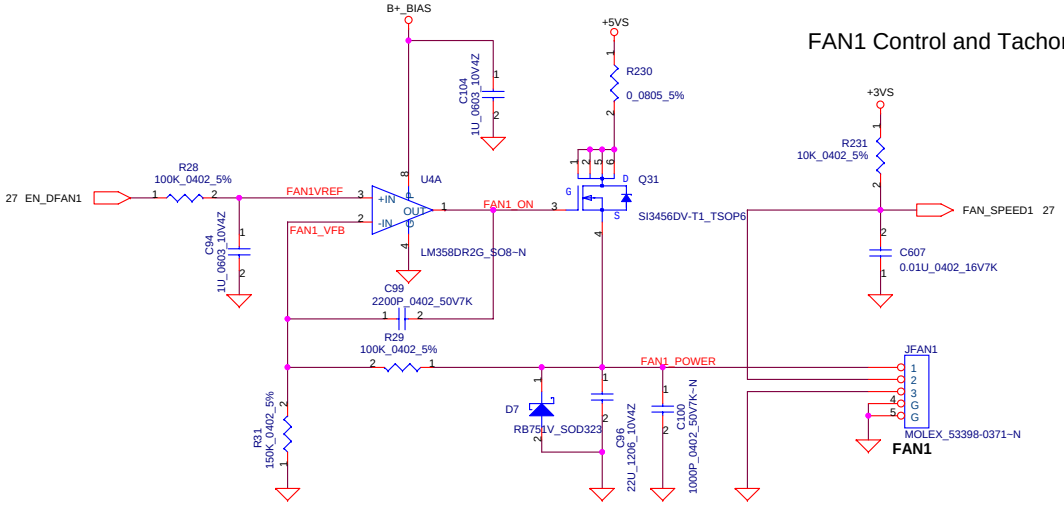
PROCESSOR HYPERTRANSPORT INTERFACE

VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE





FAN1 Control and Tachometer



Security Classification	Compal Secret Data		
Issued Date	2005/12/1	Deciphered Date	2006/12/01

Compal Electronics, Inc.

Title: **ATHLON64 HT I/F**

Size	Document Number	Rev
Custom	LA-3221P	0.1

Date: Friday, January 06, 2006 Sheet 4 of 43

Processor DDR2 Memory Interface

VDD_VTT_SUS_CPU IS CONNECTED TO THE VDD_VTT_SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

PLACE THEM CLOSE TO CPU WITHIN 1"

PLACE CLOSE TO PROCESSOR WITHIN 1.5 INCH

PLACE CLOSE TO PROCESSOR WITHIN 1.5 INCH

LAYOUT:PLACE CLOSE TO CPU

To reverse SODIMM socket

To normal SODIMM socket

Athlon 64 S1g1
uPGA638
Top View

Security Classification	Compal Secret Data		
Issued Date	2005/12/1	Deciphered Date	2006/12/01

Title: AMD CPU DDRII MEMORY I/F

Size	Document Number	Rev
Custom	LA-3221P	0.1

Date: Friday, January 06, 2006 Sheet 5 of 43

ATHLON Control and Debug

LAYOUT: ROUTE VDDA TRACE APPROX. 50 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

place them to CPU within 1"

ROUTE AS 80 Ohm DIFFERENTIAL PAIR PLACE IT CLOSE TO CPU WITHIN 1"

NOTE: HDT TERMINATION IS REQUIRED FOR REV. Ax SILICON ONLY.

HDT Connector

Thermal Sensor ADM1032

SMBus Address: 1001110X (b)

Security Classification	Compal Secret Data		
Issued Date	2005/12/1	Deciphered Date	2006/12/01

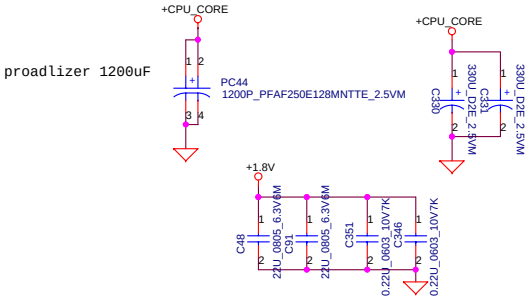
Compal Electronics, Inc.

Title: ATHLON64 CTRL & DEBUG

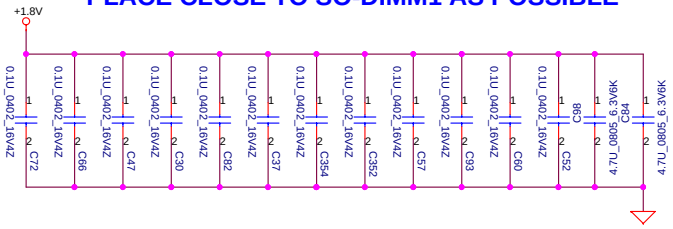
Size: Custom | Document Number: LA-3221P | Rev: 0.1

Date: Friday, January 06, 2006 | Sheet 6 of 43

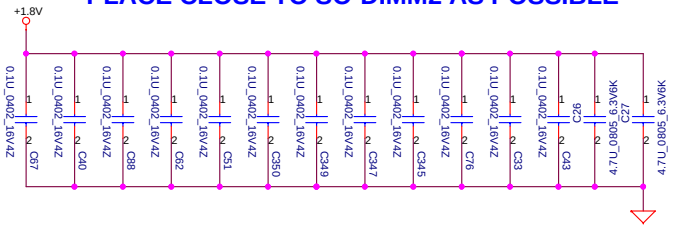
BOTTOMSIDE DECOUPLING

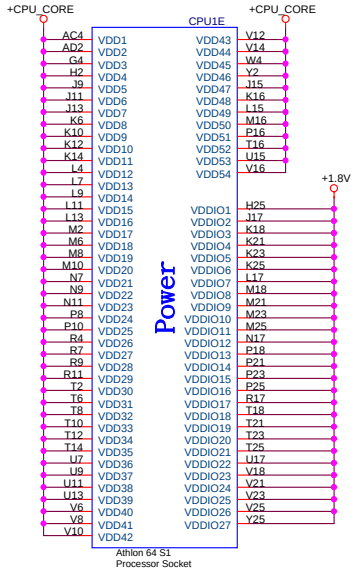


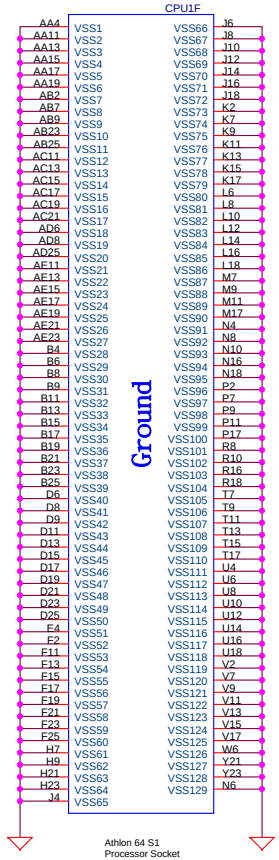
PLACE CLOSE TO SO-DIMM1 AS POSSIBLE



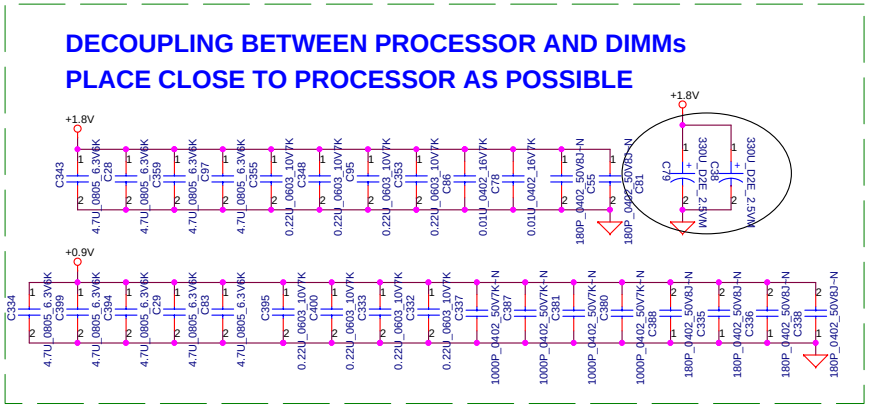
PLACE CLOSE TO SO-DIMM2 AS POSSIBLE







DECOUPLING BETWEEN PROCESSOR AND DIMMs
PLACE CLOSE TO PROCESSOR AS POSSIBLE



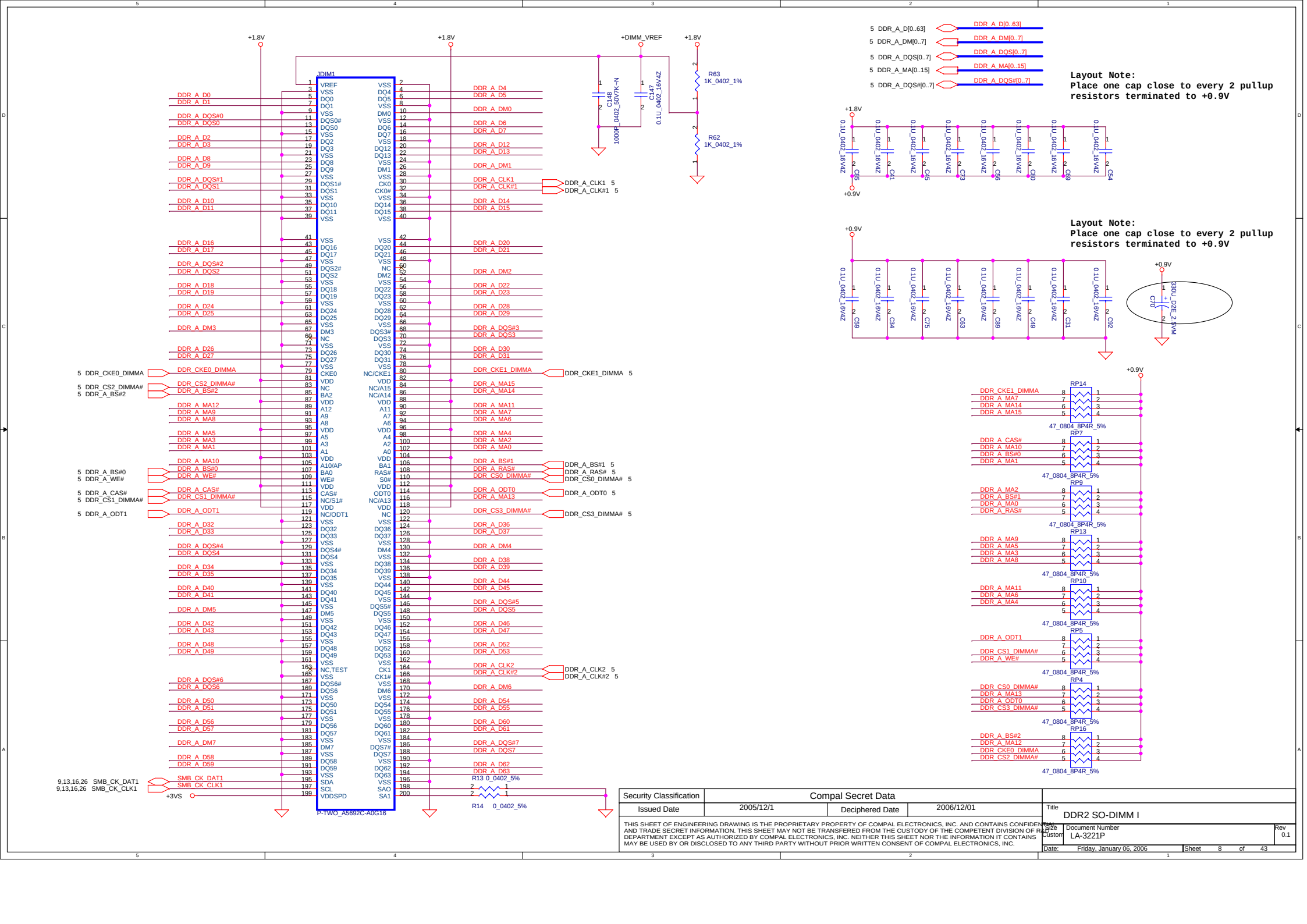
Security Classification	Compal Secret Data		
Issued Date	2005/12/1	Deciphered Date	2006/12/01

Compal Electronics, Inc.

Title: **ATHLON64 PWR & GND**

Size	Document Number	Rev
Custom	LA-3221P	0.1

Date: Friday, January 06, 2006 Sheet 7 of 43

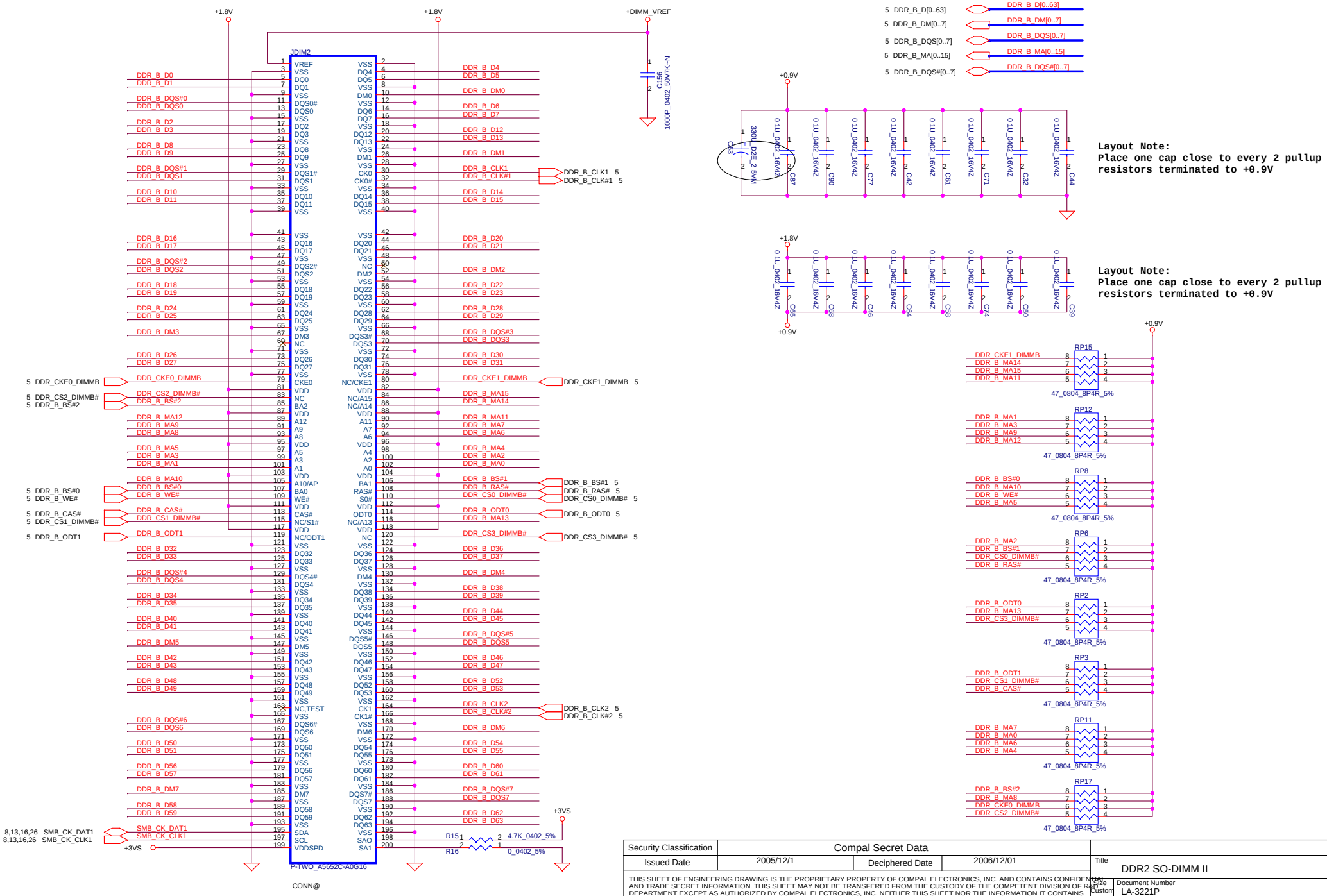


Security Classification	Compal Secret Data		
Issued Date	2005/12/1	Deciphered Date	2006/12/01

Title: DDR2 SO-DIMM I

Size	Document Number	Rev
Custom	LA-3221P	0.1

Date: Friday, January 06, 2006 Sheet 8 of 43

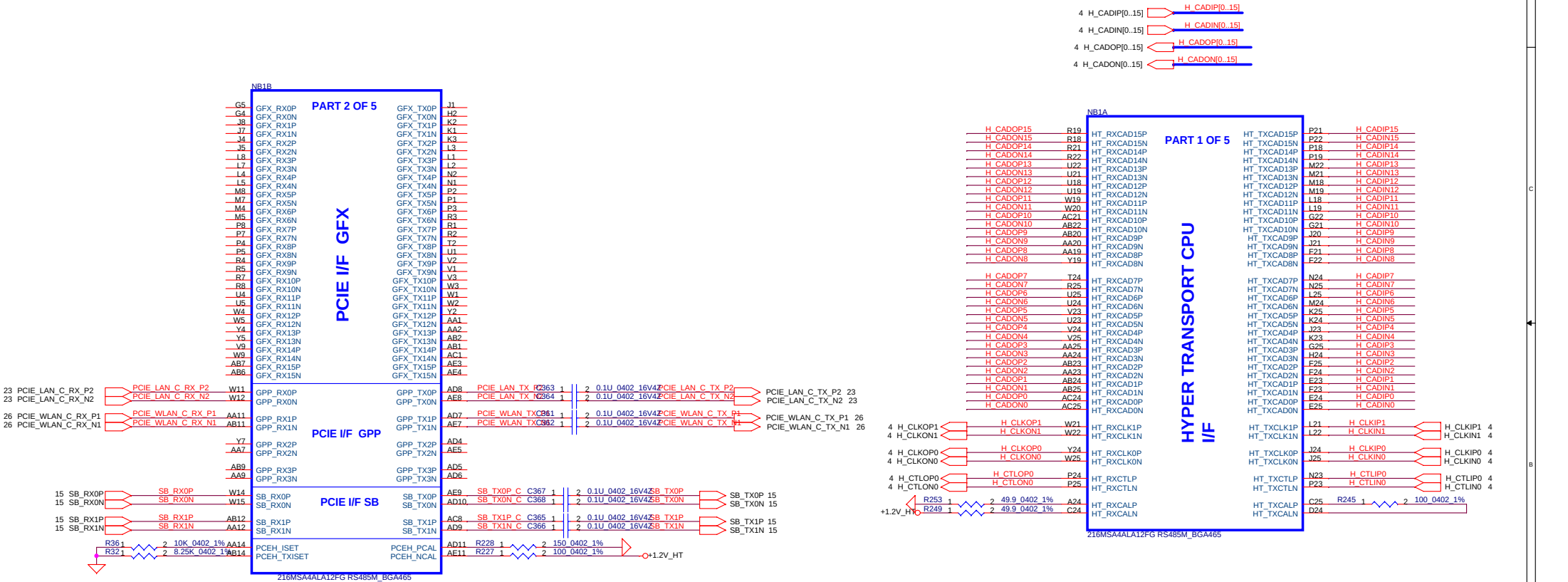


Security Classification	Compal Secret Data		
Issued Date	2005/12/1	Deciphered Date	2006/12/01

Title: DDR2 SO-DIMM II

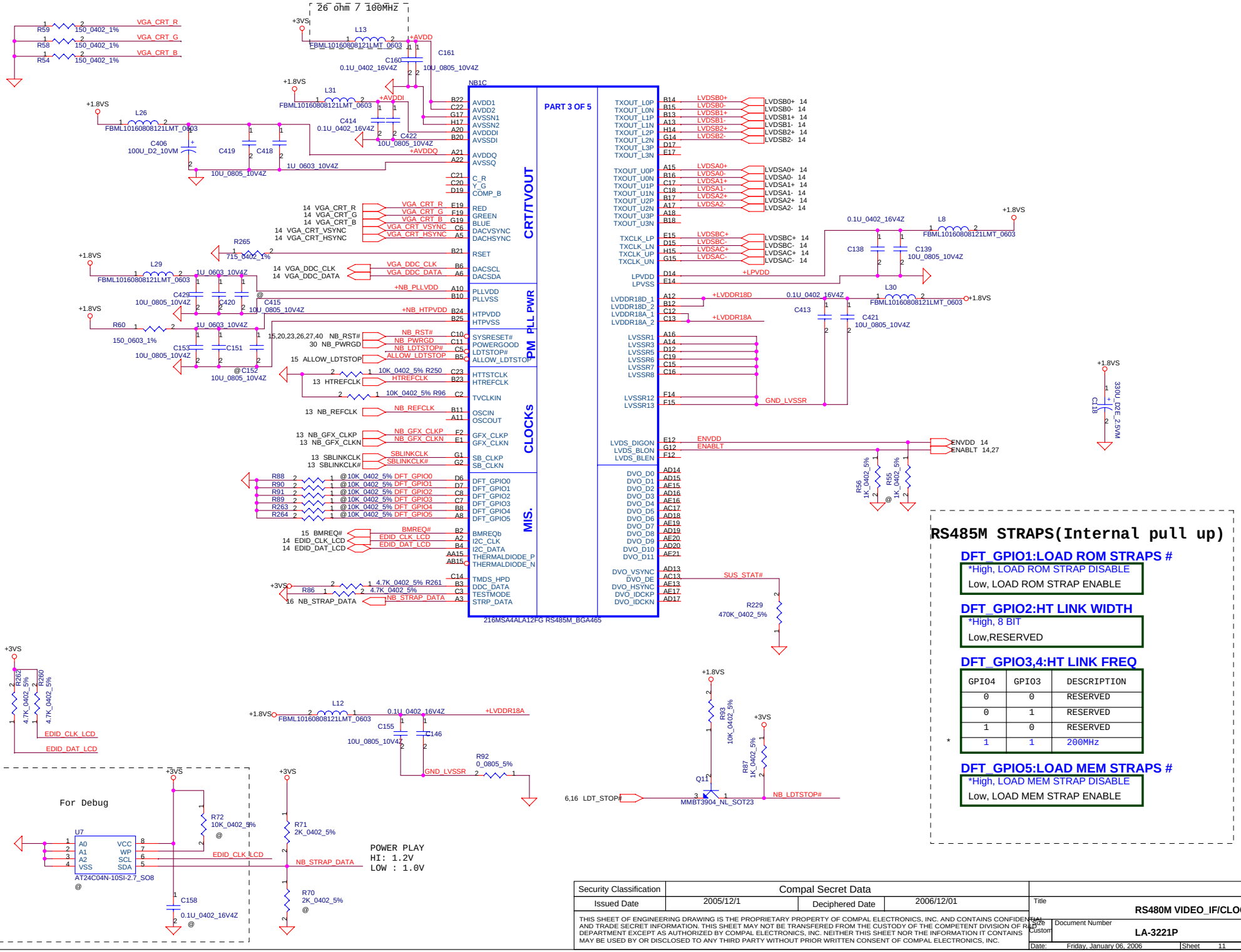
Size	Document Number	Rev
Custom	LA-3221P	0.1

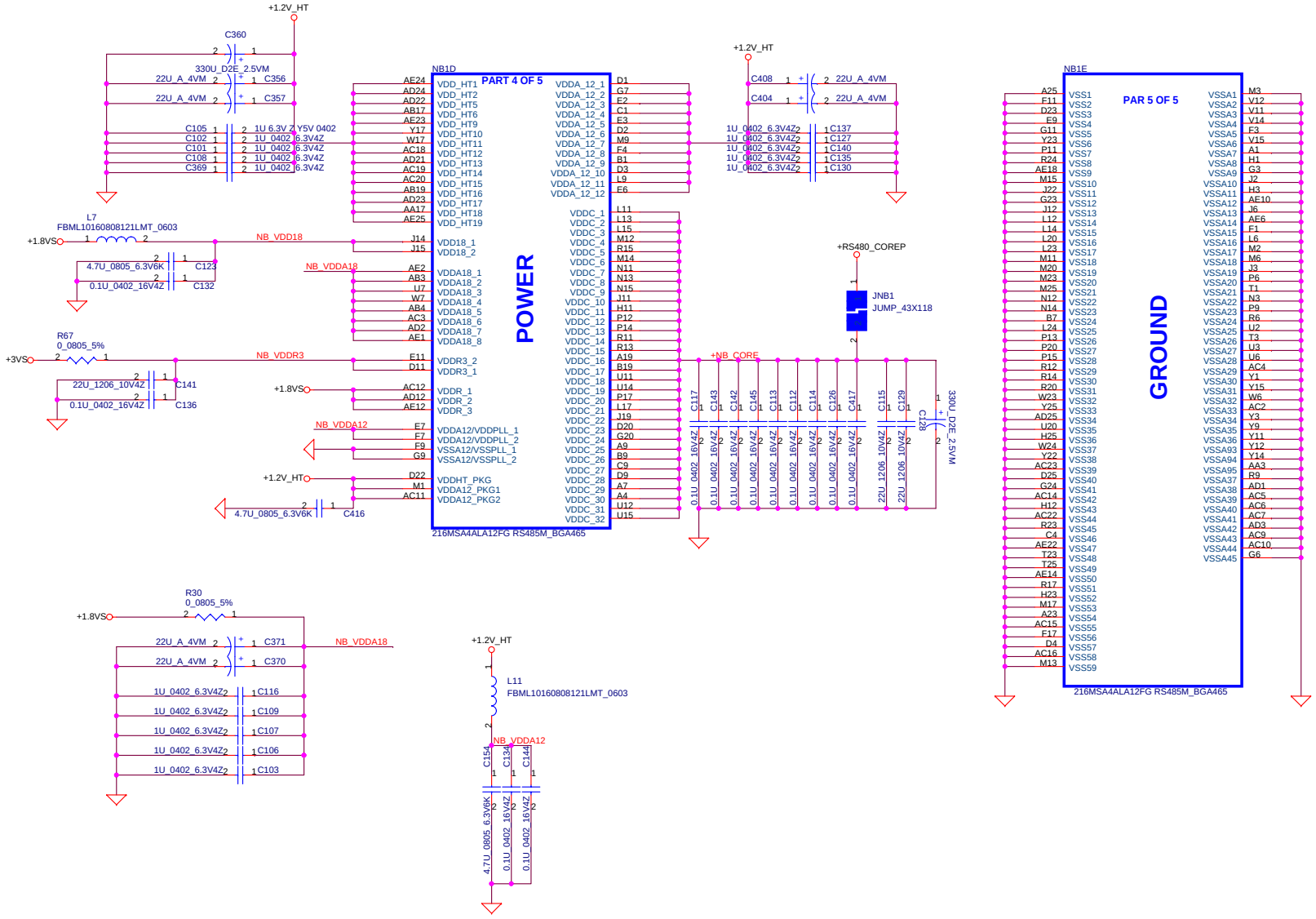
Date: Friday, January 06, 2006 Sheet 9 of 43



Security Classification	Compal Secret Data		
Issued Date	2005/12/1	Deciphered Date	2006/12/01

Title	RS480M-HT/VMEM		
Size: Custom	Document Number: LA-3221P		Rev: 0.1
Date: Friday, January 06, 2006	Sheet 10 of 43		


26 ohm 7 100MHz
NB1C
PART 3 OF 5
CRT/TVOUT
PM_PLL PWR
CLOCKS
MIS.
216MSA4ALA12FG RS485M_BGA465
RS485M STRAPS(Internal pull up)
DFT_GPIO1:LOAD ROM STRAPS #
*High, LOAD ROM STRAP DISABLE
Low, LOAD ROM STRAP ENABLE
DFT_GPIO2:HT LINK WIDTH
*High, 8 BIT
Low,RESERVED
DFT_GPIO3,4:HT LINK FREQ
GPIO4 GPIO3 DESCRIPTION
0 0 RESERVED
0 1 RESERVED
1 0 RESERVED
* 1 1 200MHz
DFT_GPIO5:LOAD MEM STRAPS #
*High, LOAD MEM STRAP DISABLE
Low, LOAD MEM STRAP ENABLE
For Debug
POWER PLAY
HI: 1.2V
LOW : 1.0V
Security Classification
Compal Secret Data
Issued Date
2005/12/1
Deciphered Date
2006/12/01
Title
RS480M VIDEO_IF/CLOCK GEN
Size
Custom
Document Number
LA-3221P
Rev
0.1
Date:
Friday, January 06, 2006
Sheet
11
of
43

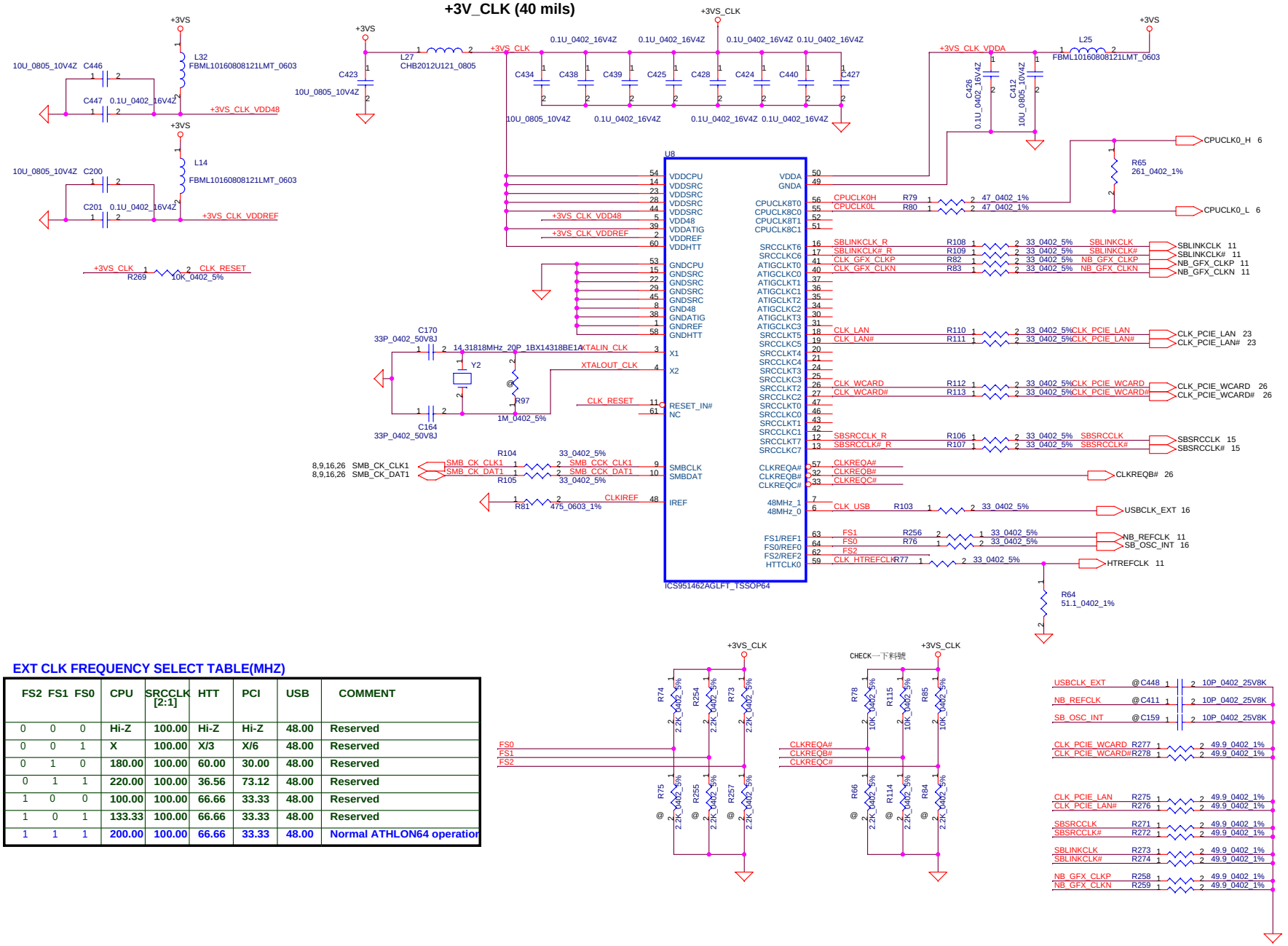


Security Classification	Compal Secret Data		
Issued Date	2005/12/1	Deciphered Date	2006/12/01

Title: RS480M Power/GND

Size: Custom | Document Number: LA-3221P | Rev: 0.1

Date: Friday, January 06, 2006 | Sheet 12 of 43

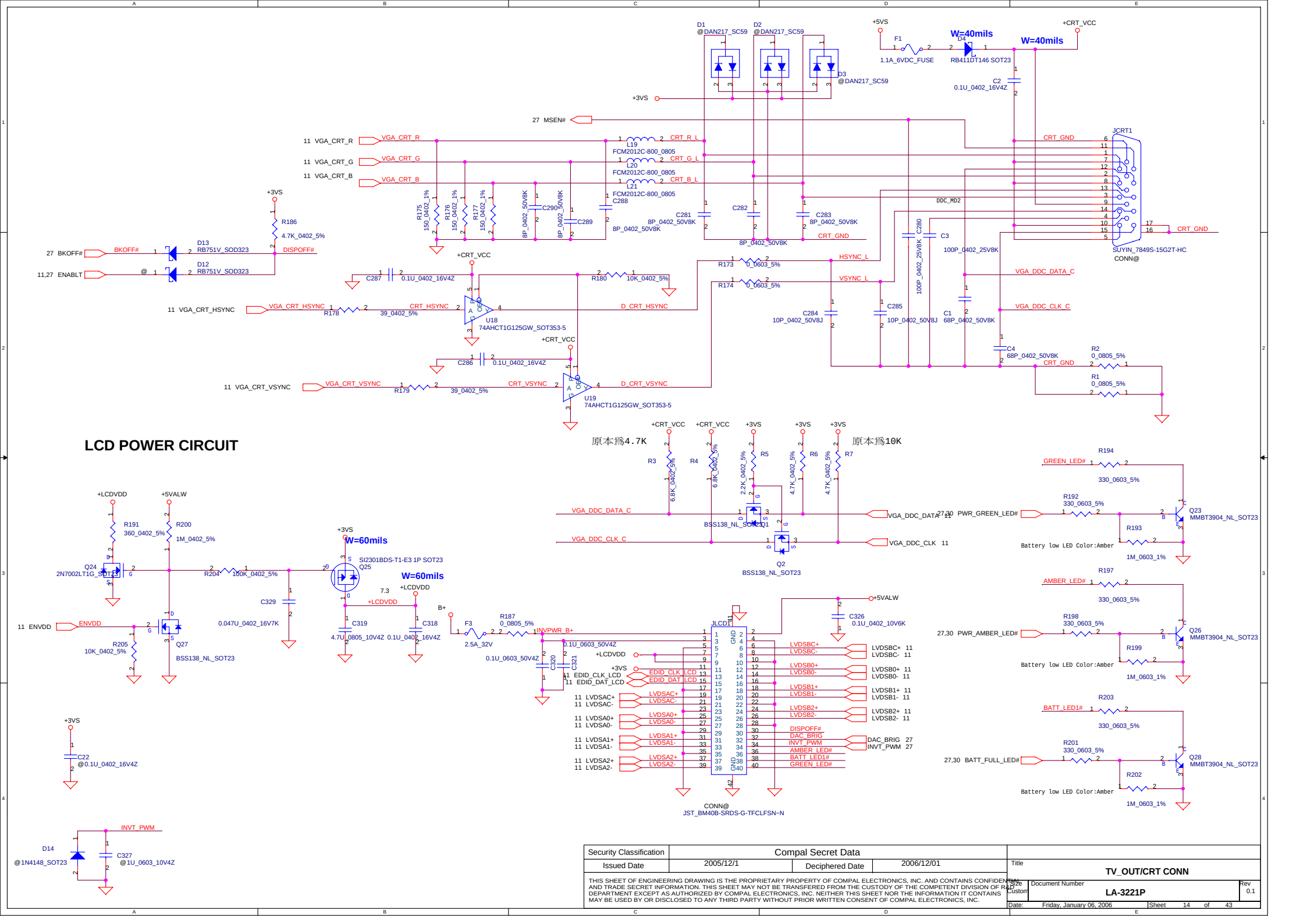


EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

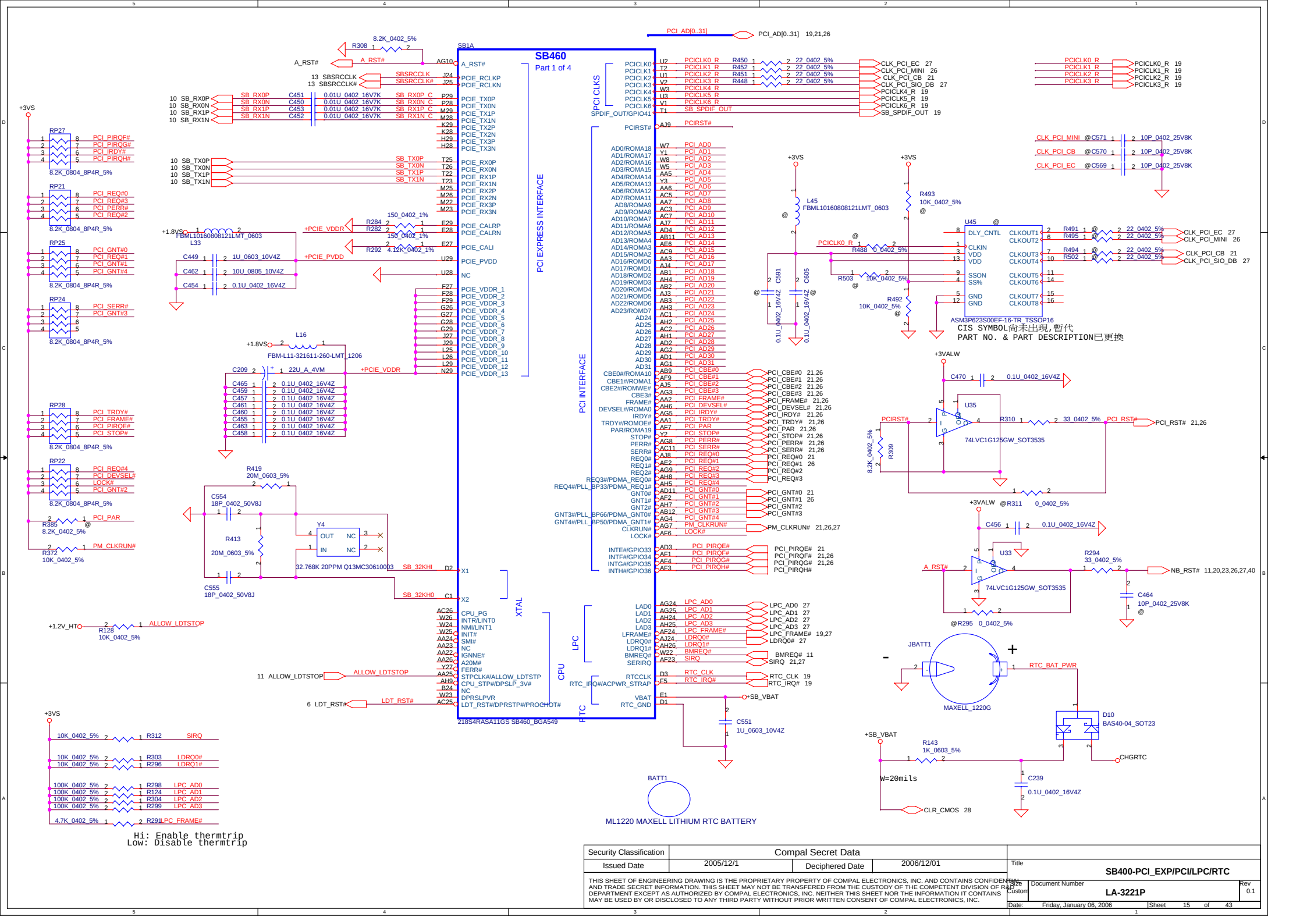
Security Classification	Compal Secret Data		
Issued Date	2005/12/1	Deciphered Date	2006/12/01

Title	Clock Generator		
Size: Custom	Document Number: LA-3221P		Rev: 0.1
Date: Friday, January 06, 2006	Sheet 13 of 43		



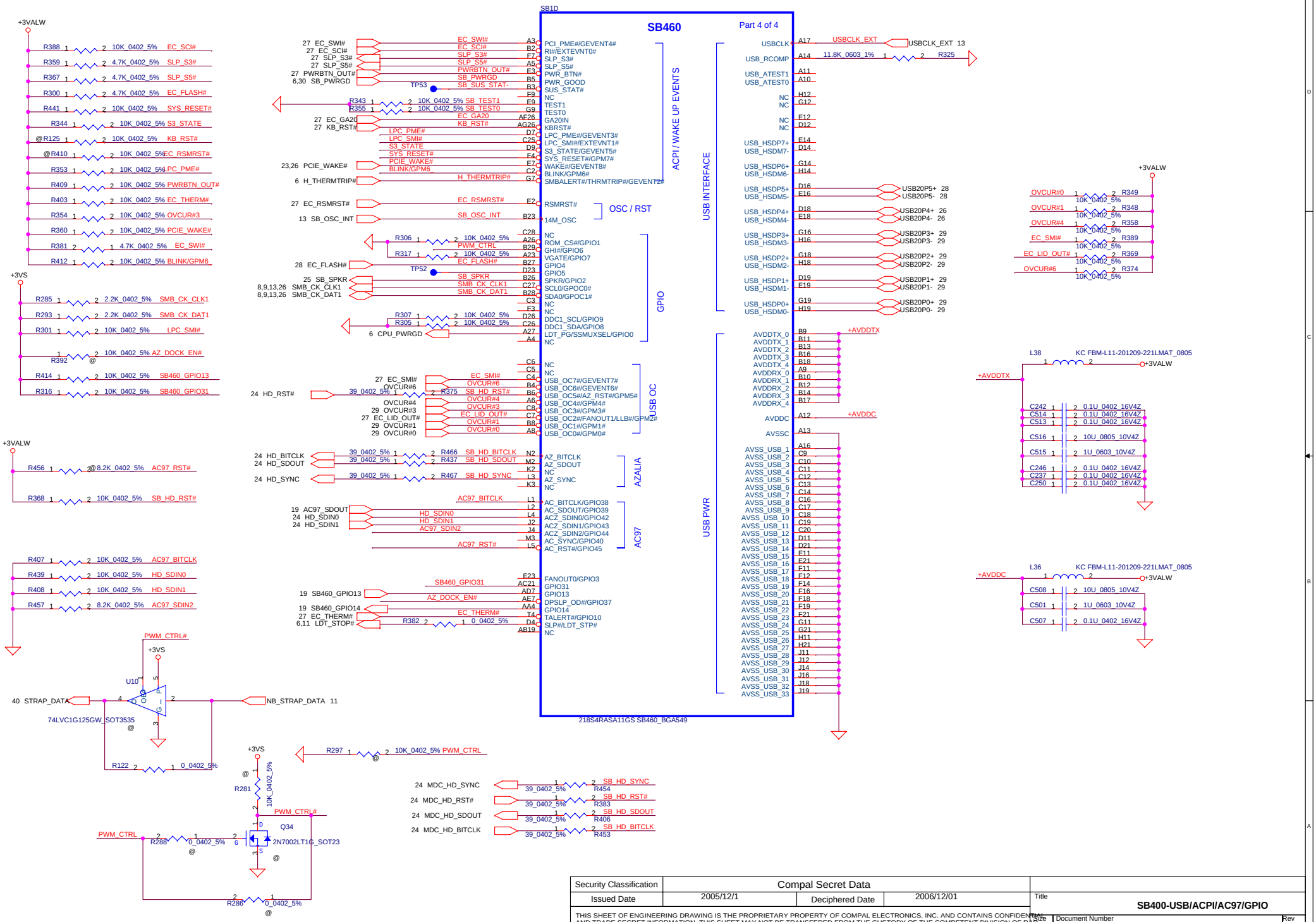
Security Classification	Compal Secret Data		
Issued Date	2005/12/1	Deciphered Date	2006/12/01

Title	TV_OUT/CRT CONN		
Size	Document Number		Rev
Custom	LA-3221P		0.1
Date:	Friday, January 06, 2006	Sheet	14 of 43



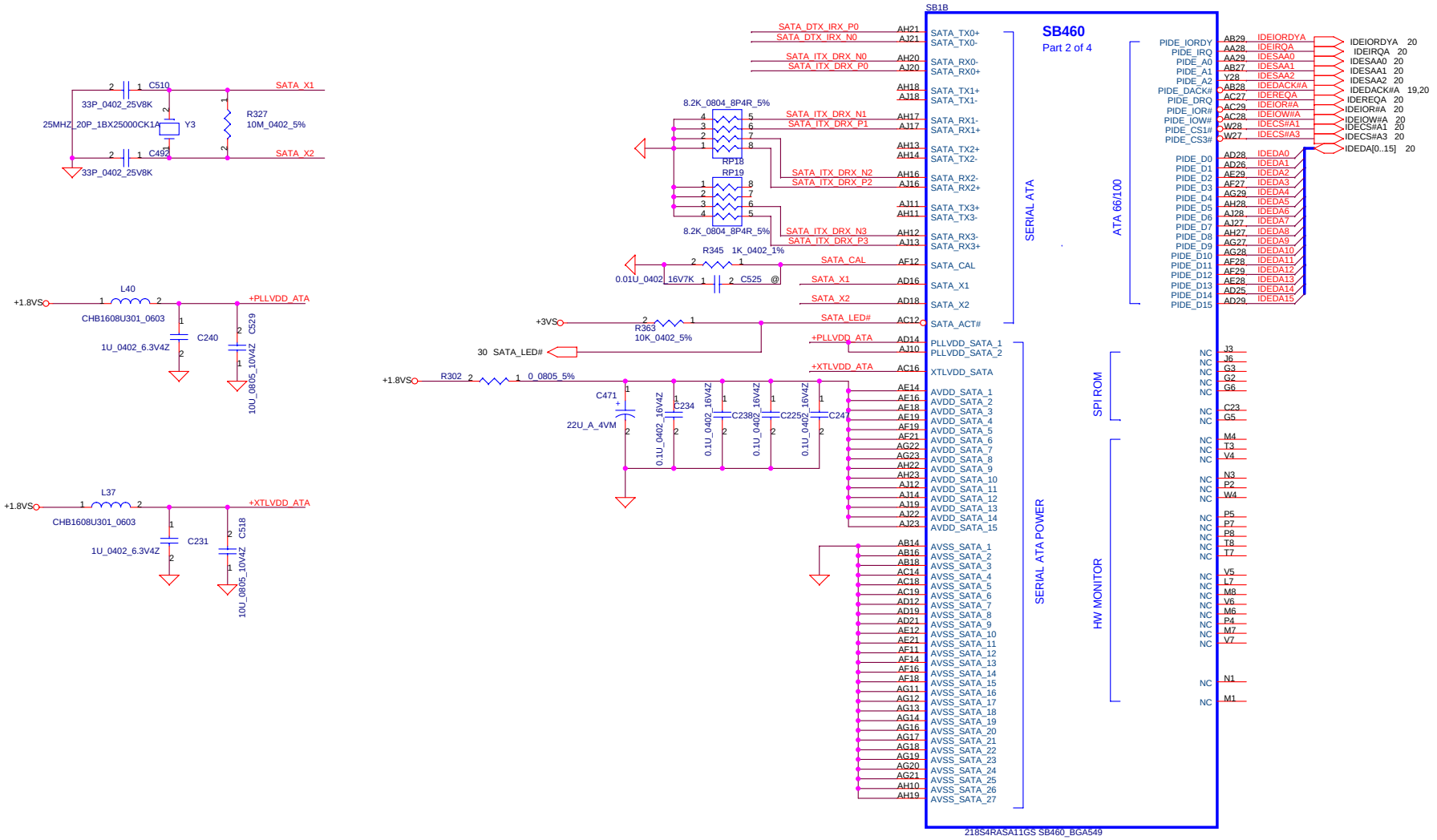
Security Classification	Compal Secret Data		
Issued Date	2005/12/1	Deciphered Date	2006/12/01

Title	SB400-PCI_EXP/PCI/LPC/RTC		
Size: Custom	Document Number: LA-3221P		Rev: 0.1
Date: Friday, January 06, 2006	Sheet 15 of 43		



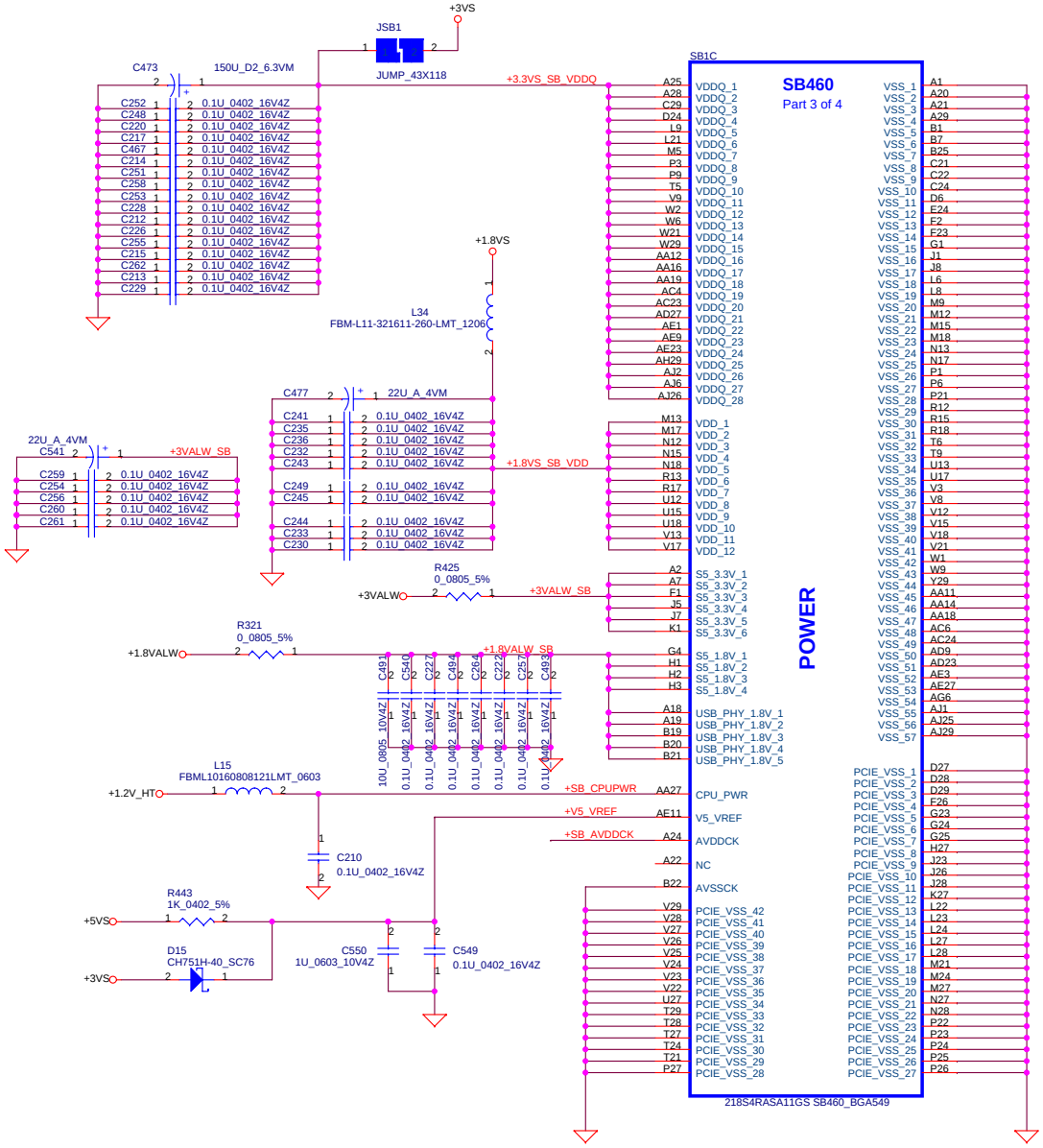
Security Classification	Compal Secret Data		
Issued Date	2005/12/1	Deciphered Date	2006/12/01

Title	SB400-USB/ACPI/AC97/GPIO		
Size	Document Number		Rev
Custom	LA-3221P		0.1
Date:	Friday, January 06, 2006	Sheet	16 of 43



Security Classification	Compal Secret Data		
Issued Date	2005/12/1	Deciphered Date	2006/12/01

Title	SB400-IDE/SATA		
Size: Custom	Document Number: LA-3221P		Rev: 0.1
Date: Friday, January 06, 2006	Sheet 17 of 43		



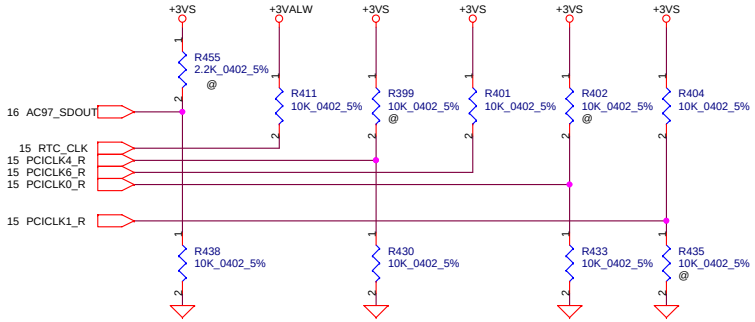
Security Classification	Compal Secret Data		
Issued Date	2005/12/1	Deciphered Date	2006/12/01

Title	SB400-Power/GND		
Size: Custom	Document Number: LA-3221P		Rev: 0.1
Date: Friday, January 06, 2006	Sheet 18 of 43		

REQUIRED STRAPS

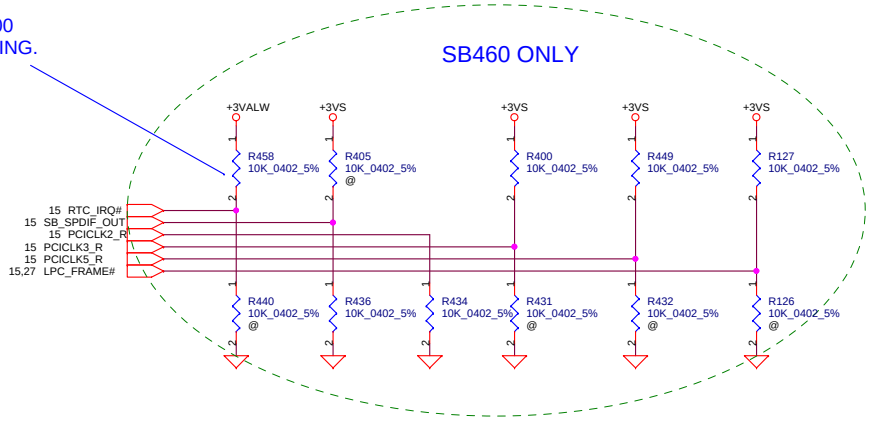
SB600 HAS 15K INTERNAL PD FOR AC_SDATA_OUT, 15K PU FOR RTC_CLK, EXTERNAL PU/PD IS NOT REQUIRED; FOR SB460, EXTERNAL PU/PD ARE REQUIRED

NOTE: R751 PU RESISTOR FOR RTC_IRQ# IS REQUIRED FOR SB600 TO KEEP THE INPUT FROM FLOATING.



	AC97_SDOUT	RTC_CLK	PCICLK4_R	PCICLK6_R	PCICLK1_R PCICLK0_R
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = LPC I ROM DEFAULT L, H = LPC II ROM L, L = FWH ROM NOTE: FOR SB460, PCICLK[8:7] ARE CONNECTED TO SUBSTRATE BALLS PCICLK[1:0]
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ DEFAULT	CPU IF=P4	

SB460 ONLY

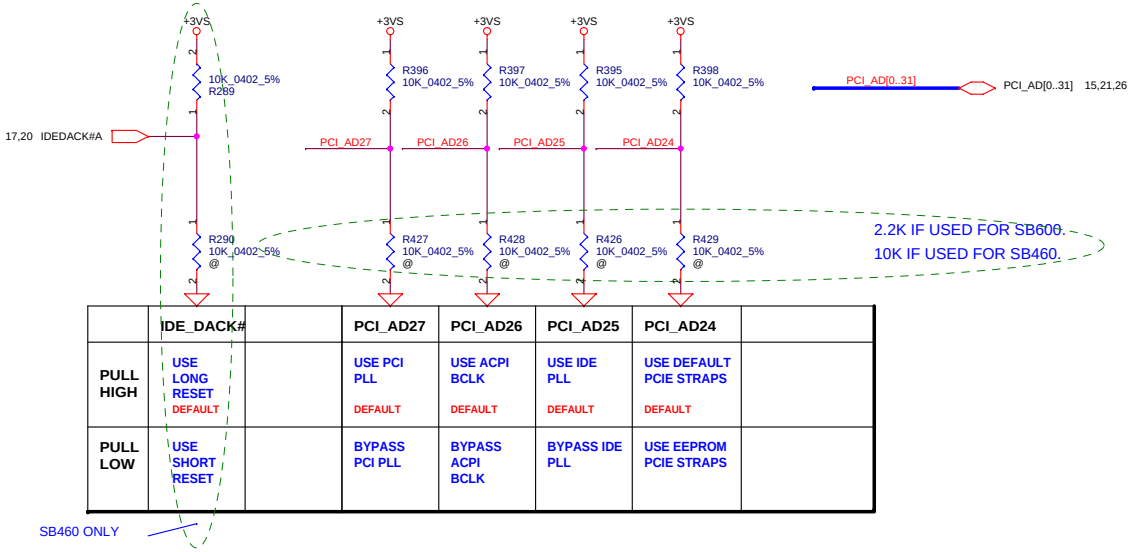


	ACPWRON	SPDIF_OUT	PCI_CLK2	PCI_CLK3	PCI_CLK5	LFRAME#
PULL HIGH	MANUAL PWR ON DEFAULT	SIO 24MHz	XTAL MODE NOT SUPPORTED	USB PHY POWERDOWN DISABLE DEFAULT	PCIE_CM_SET LOW DEFAULT	ENABLE THERMTRIP# DEFAULT
PULL LOW	AUTO PWR ON	SIO 48MHz DEFAULT	48MHZ OSC MODE DEFAULT	USB PHY POWERDOWN ENABLE	PCIE_CM_SET HIGH	DISABLE THERMTRIP#

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

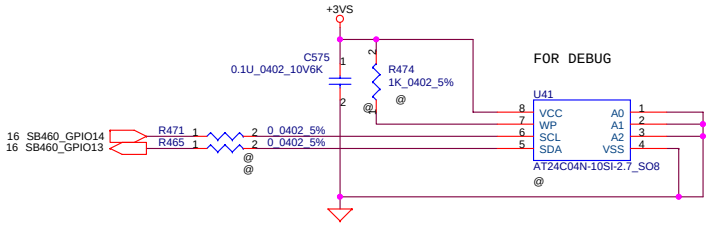
DEBUG STRAPS

SB600 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



	IDE_DACK#		PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	
PULL HIGH	USE LONG RESET DEFAULT		USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	
PULL LOW	USE SHORT RESET		BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

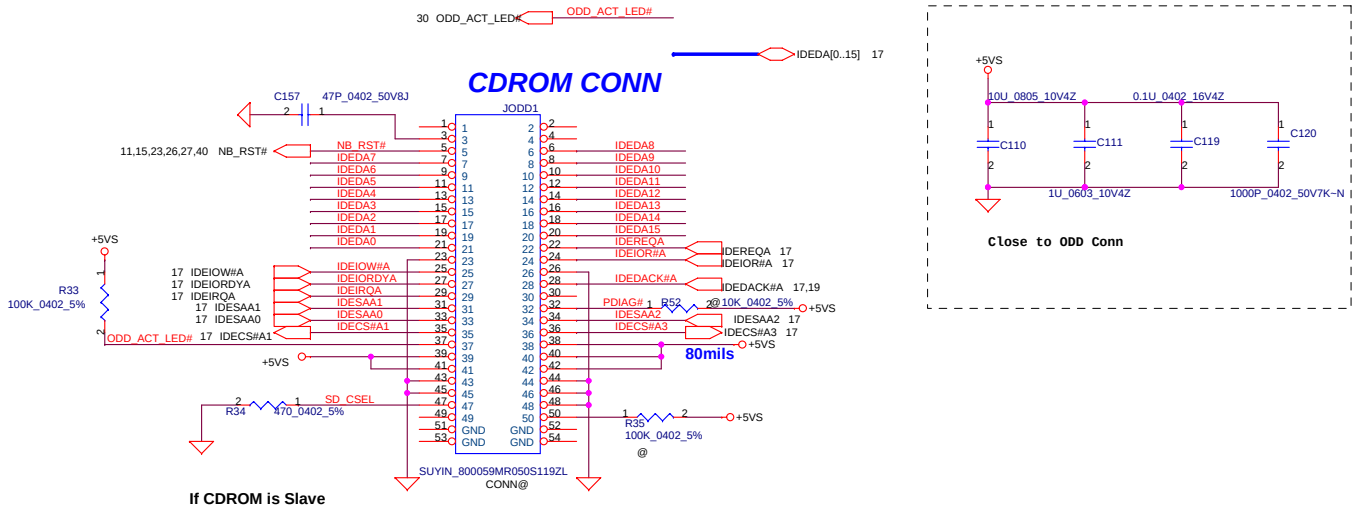
SB460 ONLY

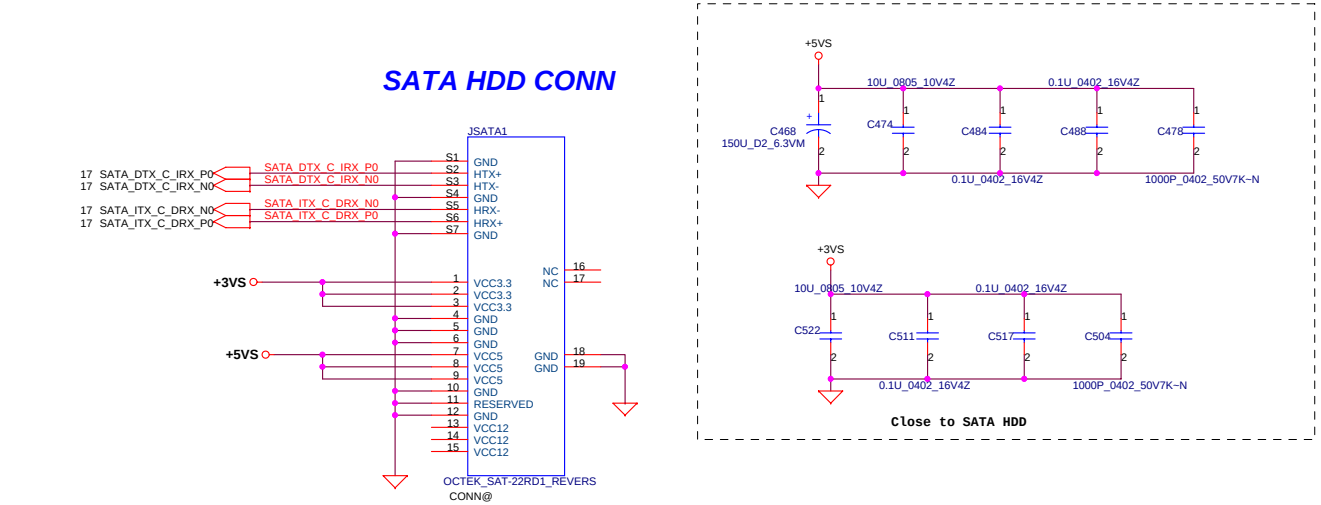


SB PCIE EEPROM STRAPS

Security Classification	Compal Secret Data		
Issued Date	2005/12/1	Deciphered Date	2006/12/01

Title	Hardware Trap		
Size: Custom	Document Number: LA-3221P		Rev: 0.1
Date: Friday, January 06, 2006	Sheet 19 of 43		





Security Classification	Compal Secret Data		
Issued Date	2005/12/1	Deciphered Date	2006/12/01

Title	HDD/CDROM		
Size: Custom	Document Number: LA-3221P		Rev: 0.1
Date: Friday, January 06, 2006	Sheet 20 of 43		

R5C811 & R5C841
PULL DOWN :Disable media card function

R319 10K_0402_5% UDIO3
R320 10K_0402_5% UDIO4

U38A
R5C841
R5C841_CSP208-D

U38B
R5C841
R5C841_CSP208-D

Function Seclect

UDIO3	UDIO4	VPPEN0	SD	MS	
0	0	0	X	X	
0	0	1	X	X	Enable
0	1	0	X	Enable	
0	1	1	X	Enable	Enable
1	0	0	Enable	X	X
1	0	1	Enable	X	Enable
1	1	0	Enable	Enable	X
* 1	1	1	Enable	Enable	Enable

apply same length for set of TPA+,TPA- and TPB+,TPB-

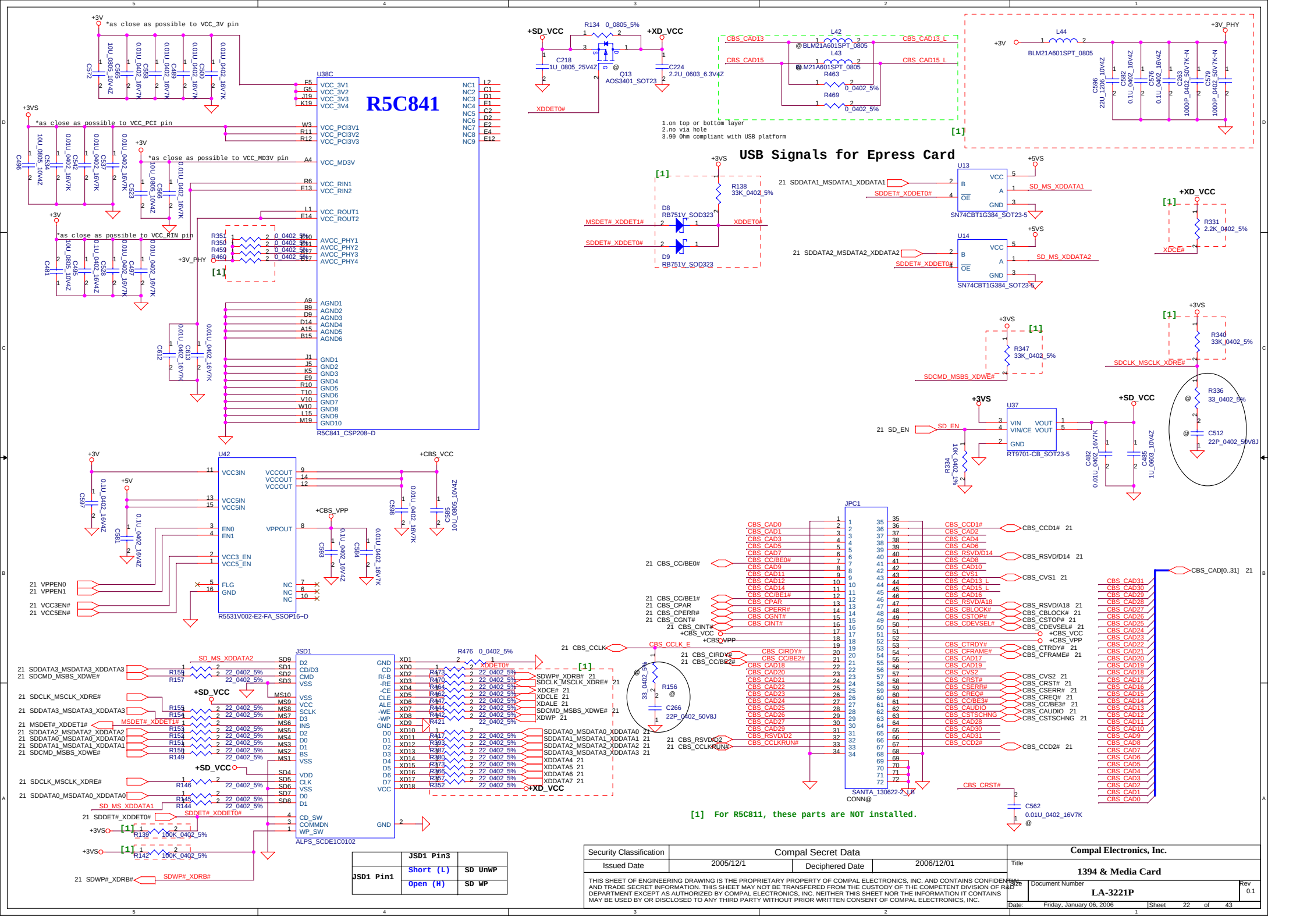
Placement Near Card Bus Controller

[1] For R5C811, these parts are NOT installed.

Security Classification	Compal Secret Data		
Issued Date	2005/12/1	Deciphered Date	2006/12/01

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

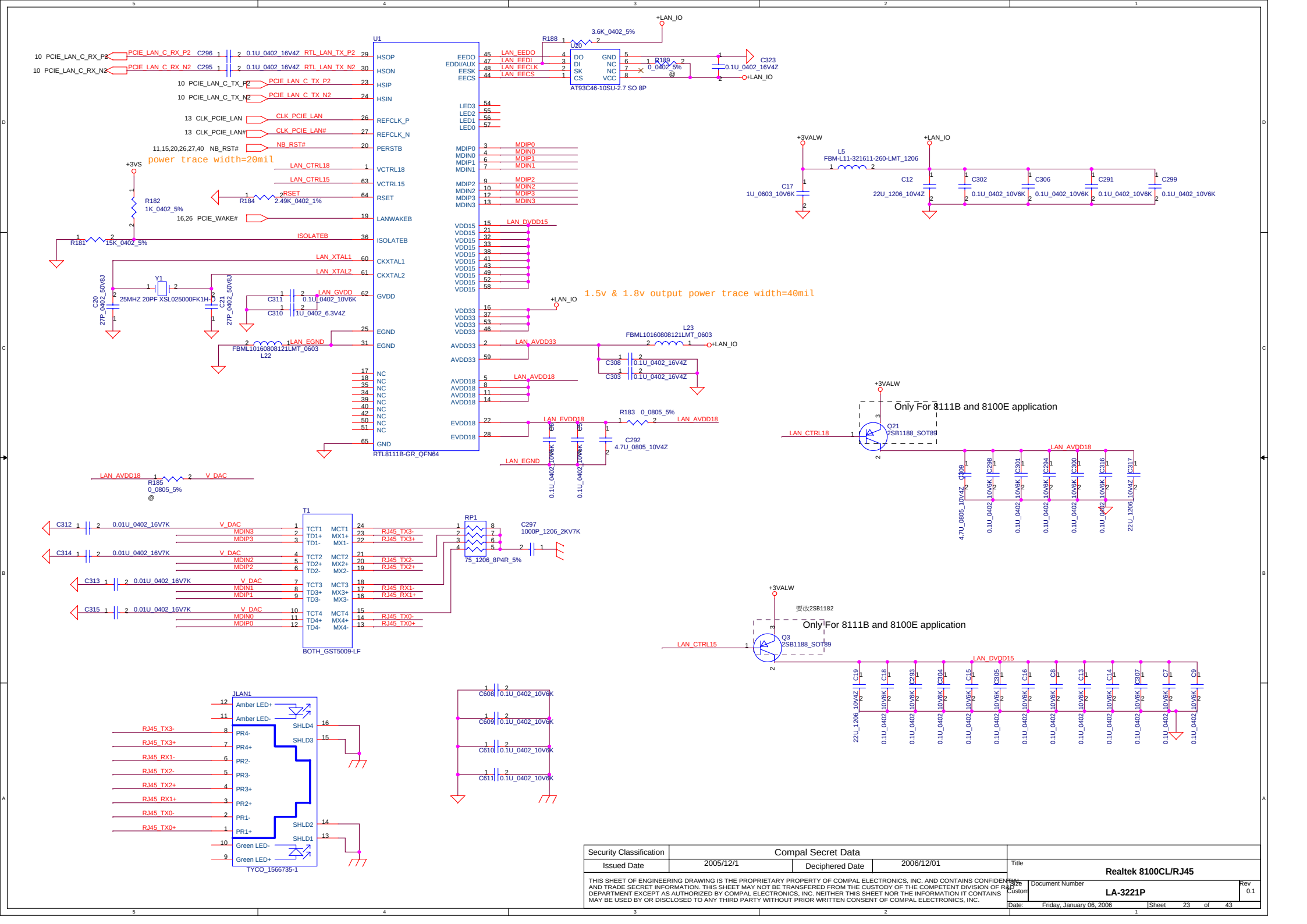
Title: CardBus Controller(R5C841)
Size: B
Document Number: LA-3221P
Rev: 0.1
Date: Friday, January 06, 2006
Sheet 21 of 43



	JSD1 Pin3	
JSD1 Pin1	Short (L)	SD UnWP
	Open (H)	SD WP

Security Classification	Compal Secret Data		
Issued Date	2005/12/1	Deciphered Date	2006/12/01

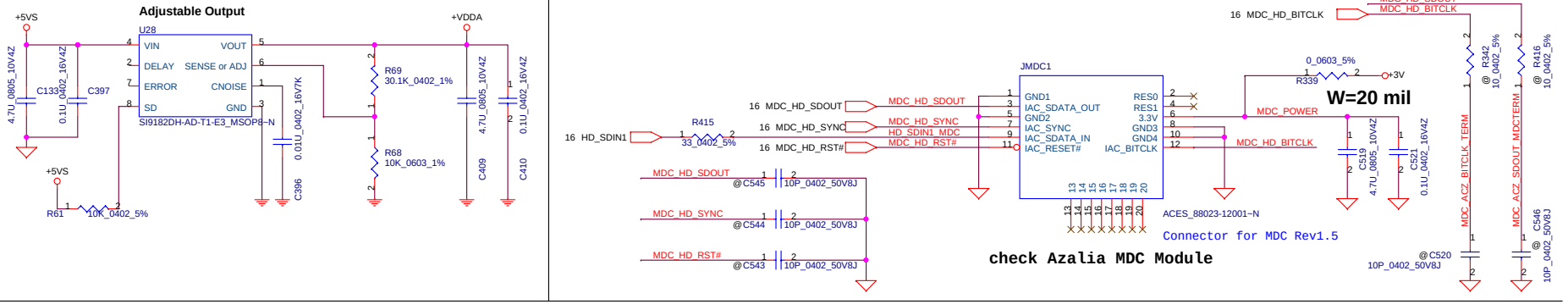
Compal Electronics, Inc.	
Title	1394 & Media Card
Size	Document Number: LA-3221P
Rev	0.1
Date:	Friday, January 06, 2006
Sheet	22 of 43



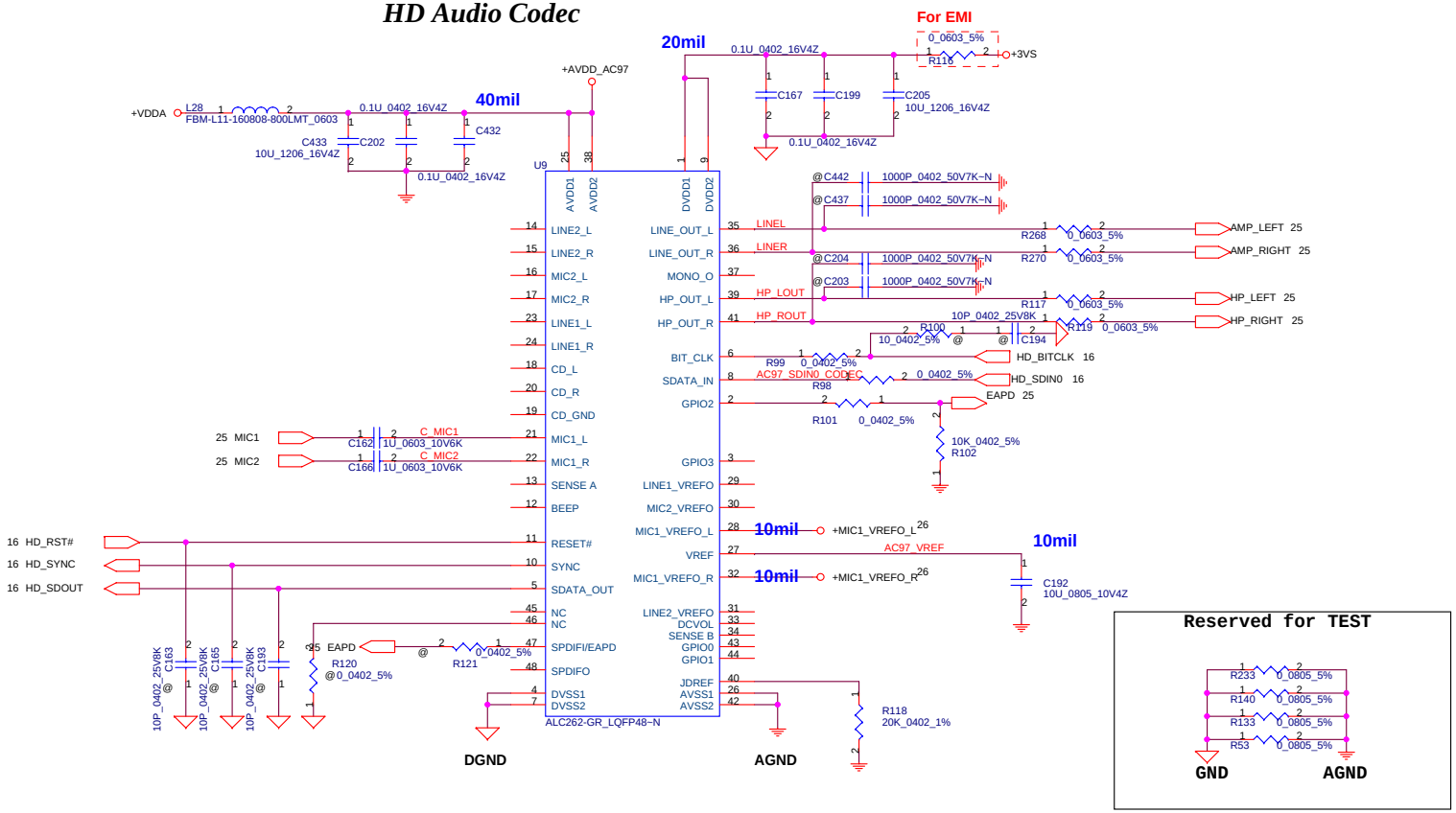
Security Classification	Compal Secret Data		
Issued Date	2005/12/1	Deciphered Date	2006/12/01

Title	Realtek 8100CL/RJ45		
Size: Custom	Document Number: LA-3221P		Rev: 0.1
Date: Friday, January 06, 2006	Sheet 23 of 43		

MDC CONN.



HD Audio Codec



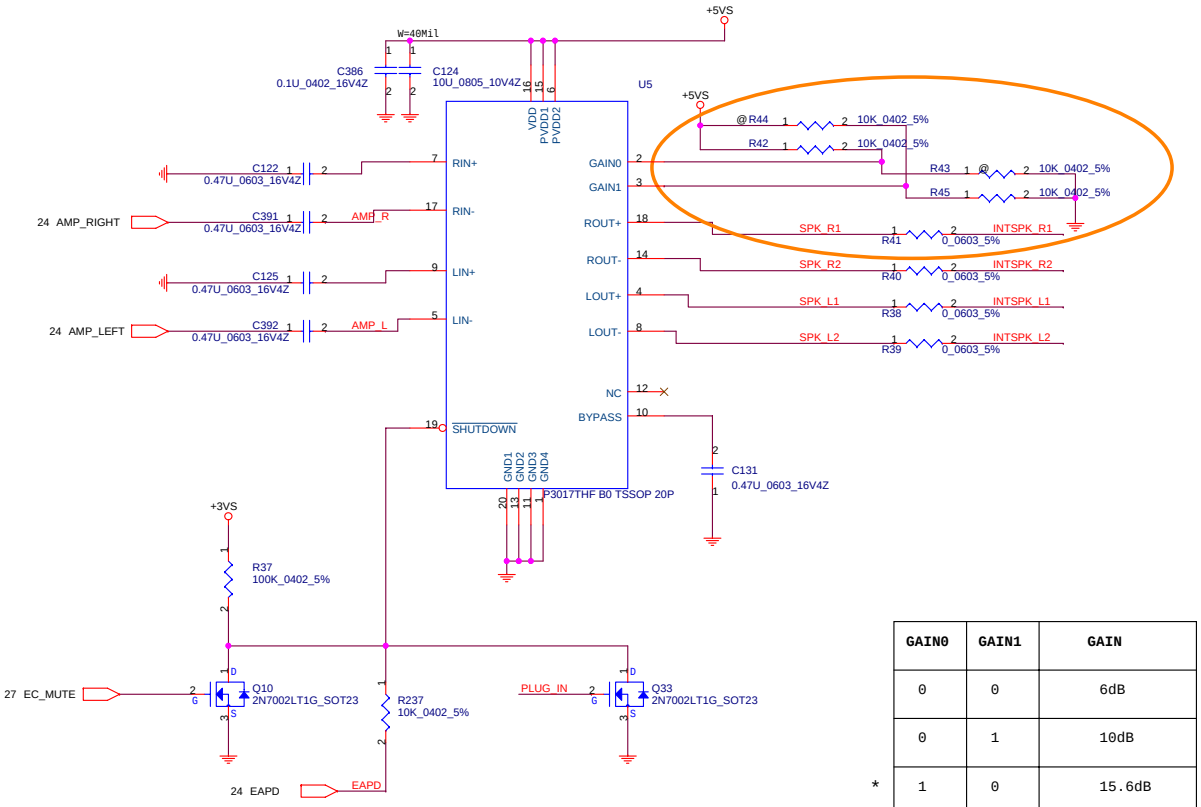
Security Classification	Compal Secret Data		
Issued Date	2005/12/1	Deciphered Date	2006/12/01

Compal Electronics, Inc.

Title: **Codec ALC262**

Size | Document Number: *LA-3221P* | Rev: 0.1

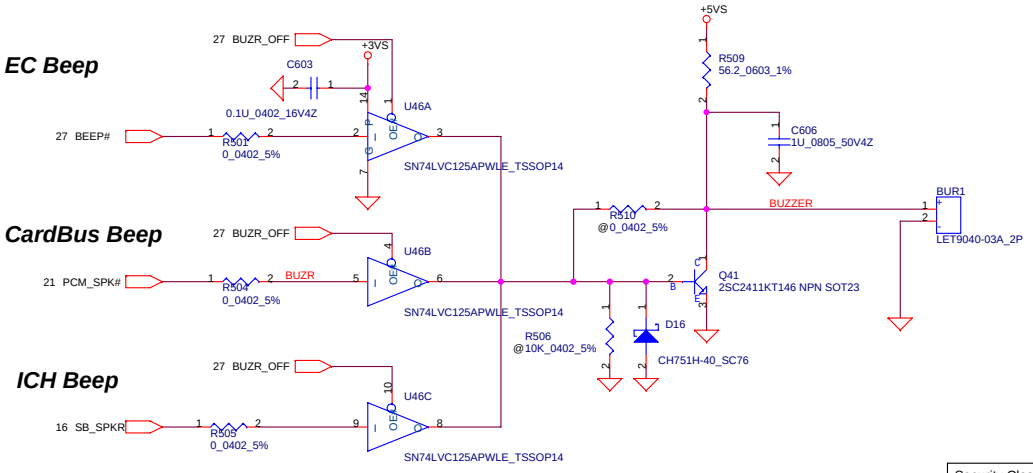
Date: Friday, January 06, 2006 | Sheet 24 of 43



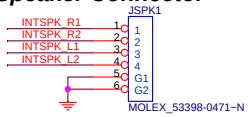
GAIN0	GAIN1	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

*

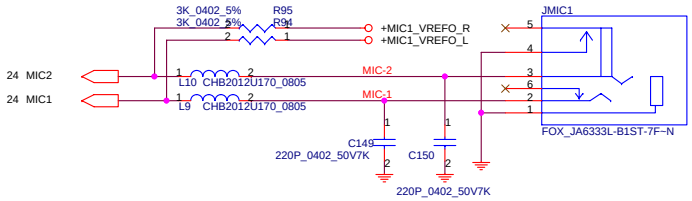
Buzzer need to support ICH/PCM_SPK/Battery_low and WL_on/off



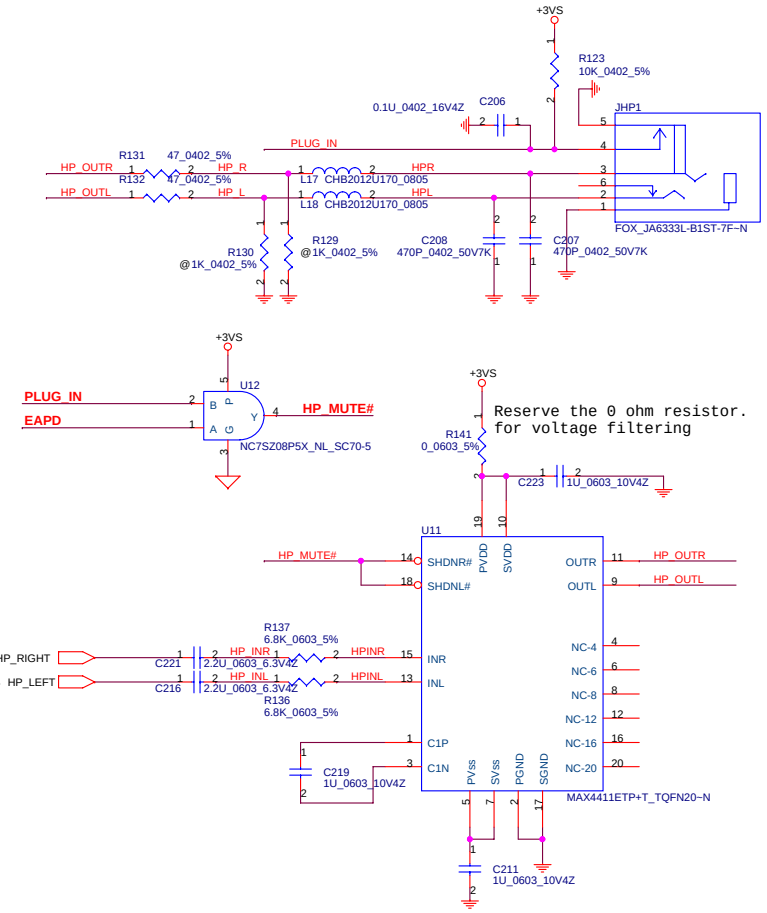
Speaker Connector



MICROPHONE IN JACK



HEADPHONE OUT JACK



Security Classification	Compal Secret Data		
Issued Date	2005/12/1	Deciphered Date	2006/12/01

Compal Electronics, Inc.

Title: **AMP/Audio Jack**

Size | Document Number: **LA-3221P** | Rev: 0.1

Date: Friday, January 06, 2006 | Sheet 25 of 43

Mini-Express Card

IDSEL:PCI_AD22

Wireless_BTN

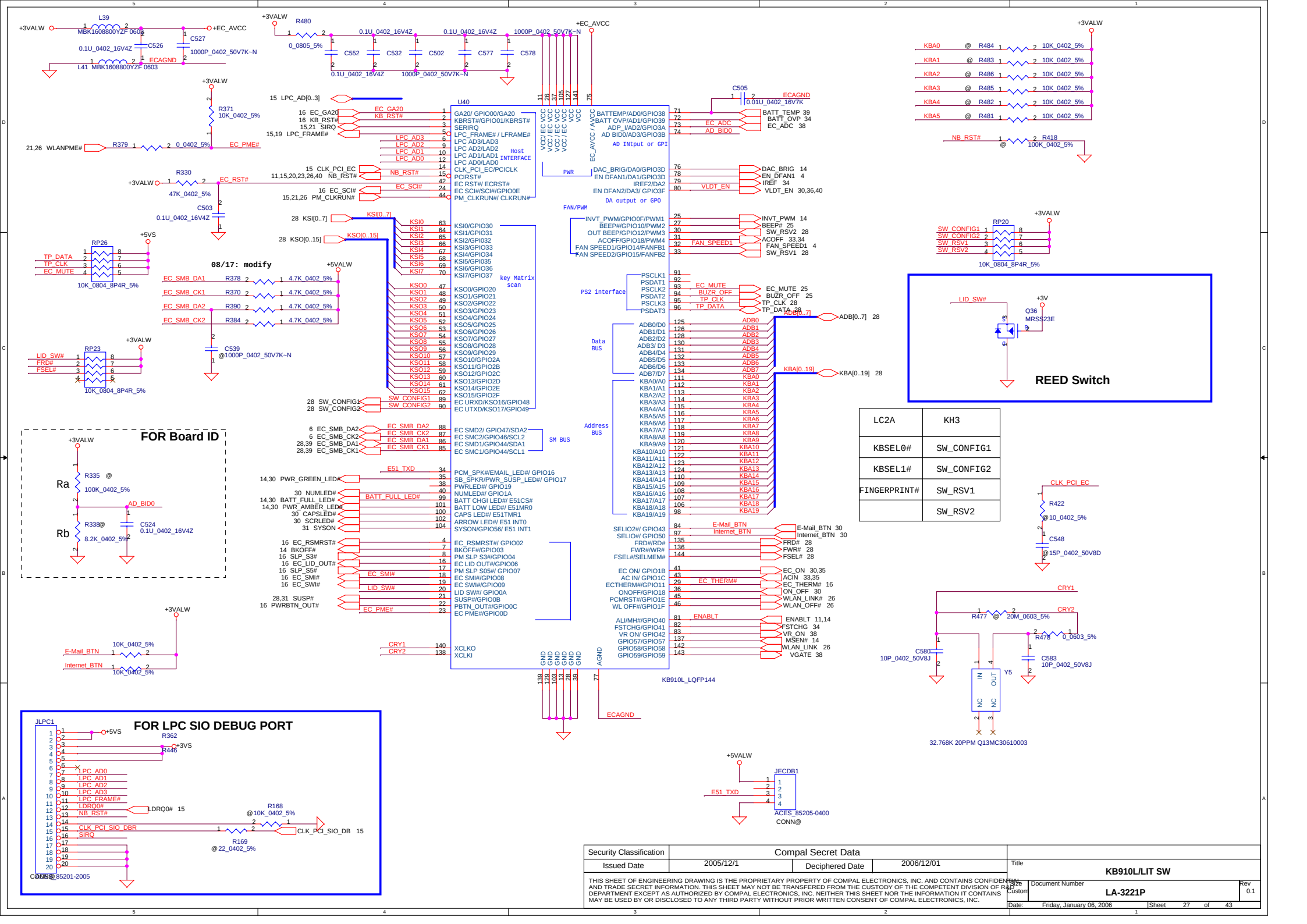
Killer switch

D1 Pin3 Open PAST & MASK layer

WLAN LED

Security Classification	Compal Secret Data		
Issued Date	2005/12/1	Deciphered Date	2006/12/01

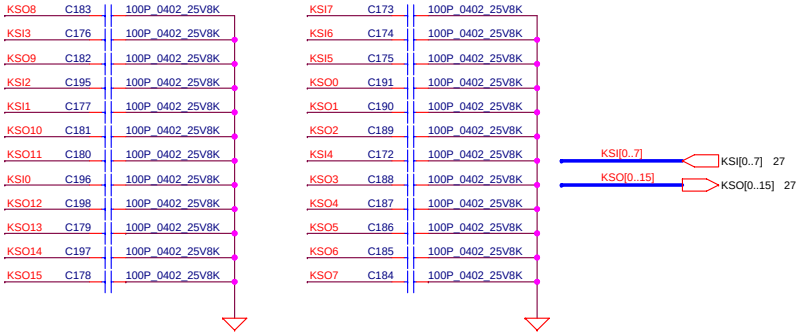
Title	MINI PCI		
Size: Custom	Document Number: LA-3221P		Rev: 0.1
Date: Friday, January 06, 2006	Sheet 26 of 43		



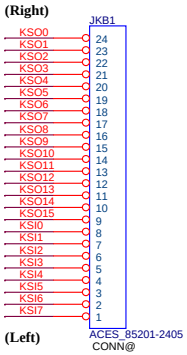
LC2A	KH3
KBSEL0#	SW_CONFIG1
KBSEL1#	SW_CONFIG2
FINGERPRINT#	SW_RSV1
	SW_RSV2

Security Classification	Compal Secret Data		
Issued Date	2005/12/1	Deciphered Date	2006/12/01

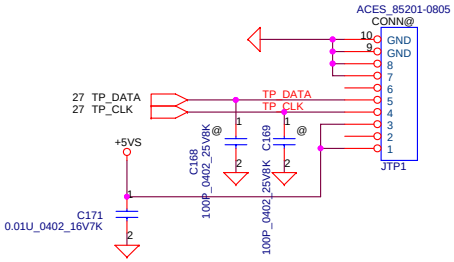
Title	KB910L/LIT SW
Size	Custom
Document Number	LA-3221P
Rev	0.1
Date:	Friday, January 06, 2006
Sheet	27 of 43



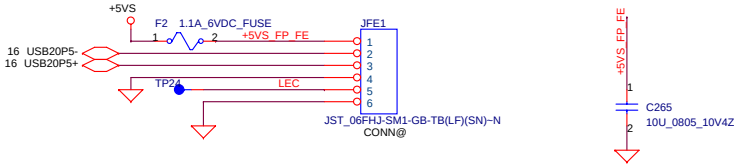
INT_KBD CONN.

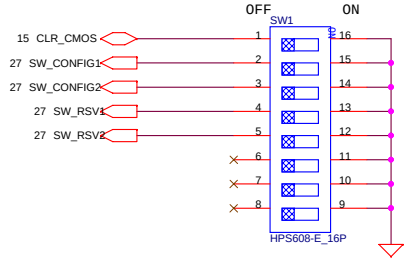


TO M/B

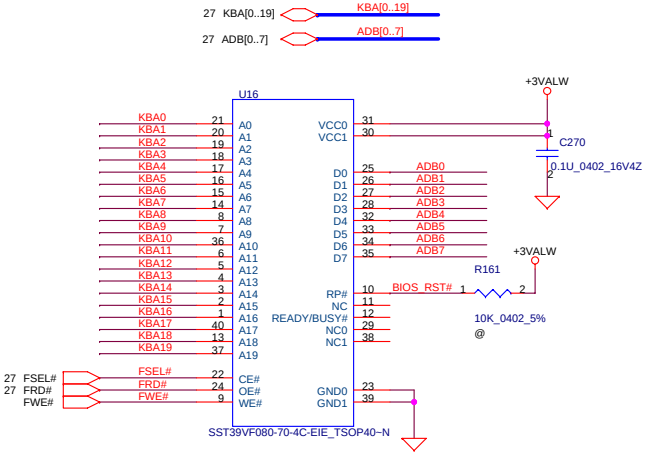


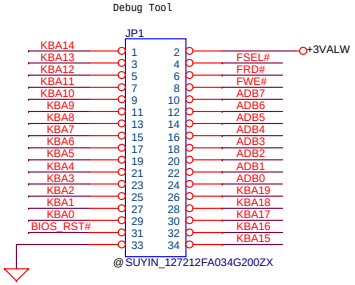
Felica Conn

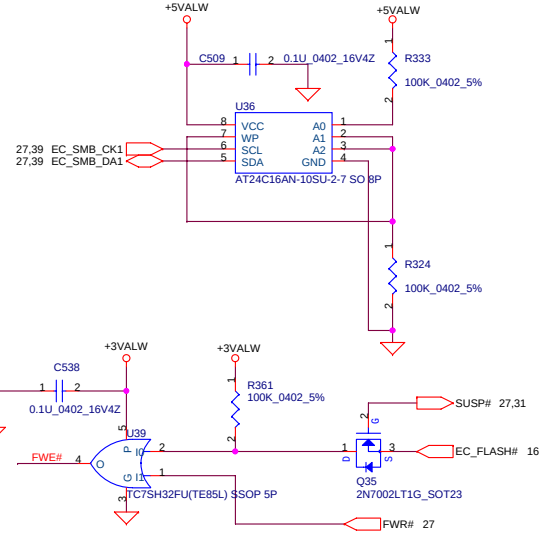




1M Byte BIOS ROM

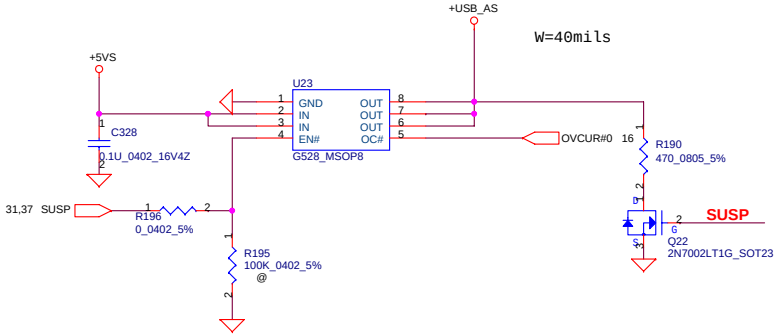


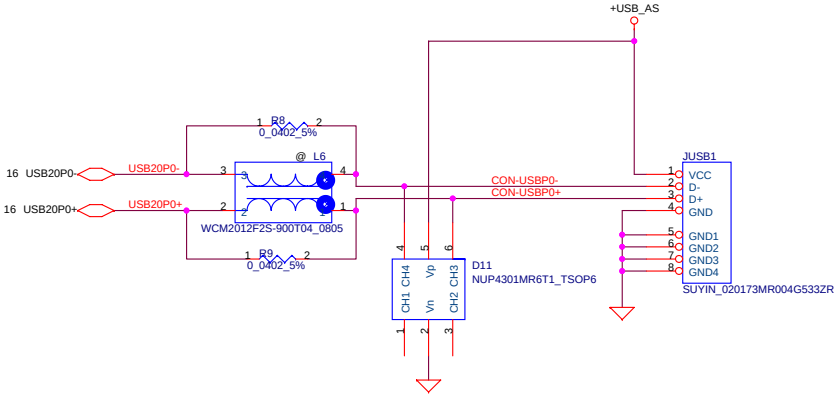


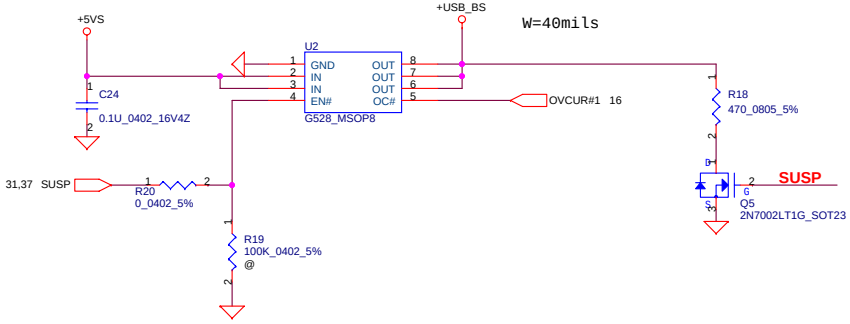


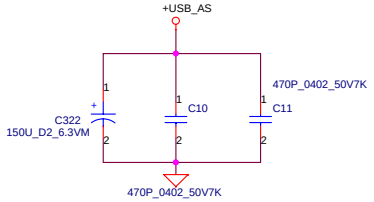
Security Classification	Compal Secret Data		
Issued Date	2005/12/1	Deciphered Date	2006/12/01

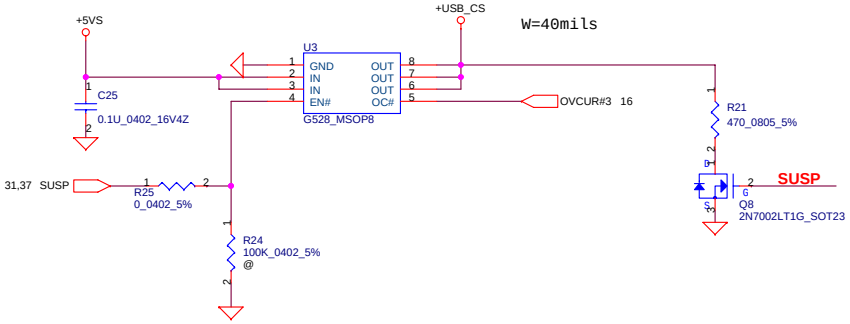
Title	MDA/BT/KBD/TP Conn		
Size: Custom	Document Number: LA-3221P		Rev: 0.1
Date: Friday, January 06, 2006	Sheet 28 of 43		

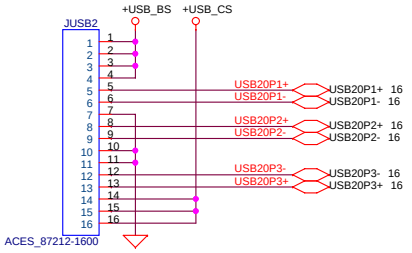












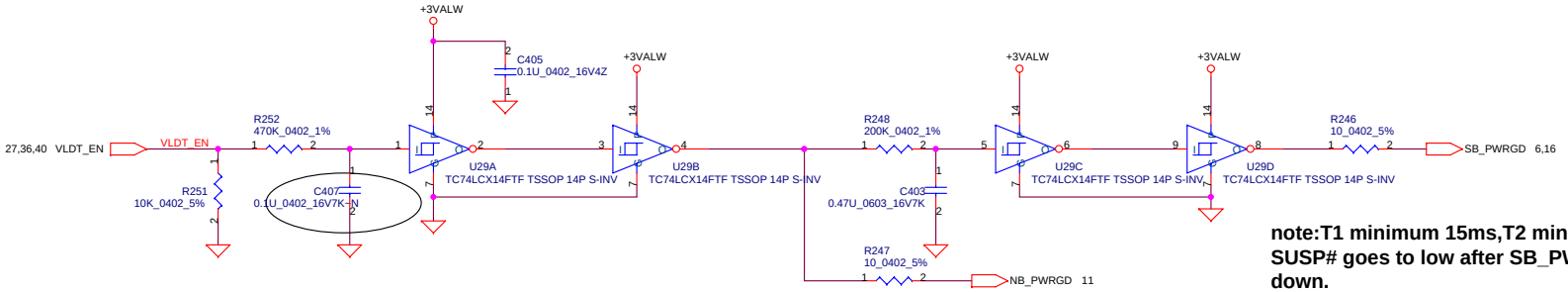
Security Classification	Compal Secret Data		
Issued Date	2005/12/1	Deciphered Date	2006/12/01

Compal Electronics, Inc.

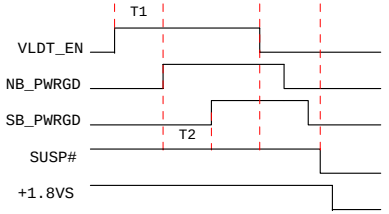
Title: **USB Port**

Size | Document Number: **LA-3221P** | Rev: 0.1

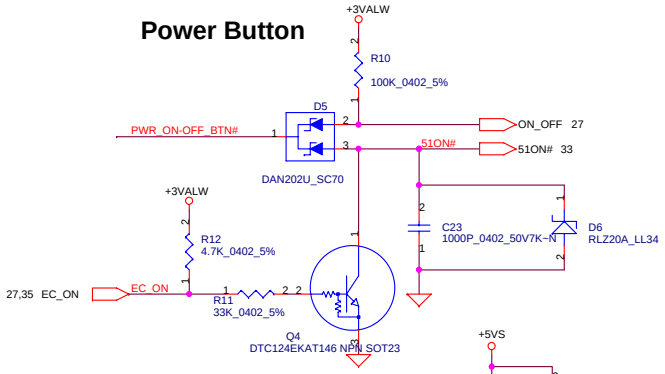
Date: Friday, January 06, 2006 | Sheet 29 of 43

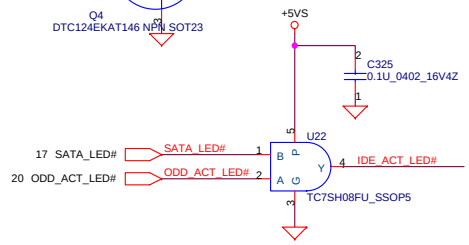


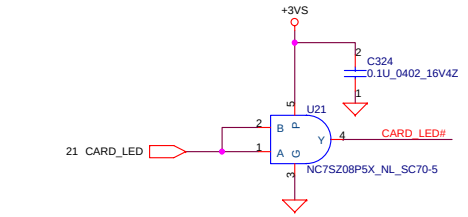
note:T1 minimum 15ms,T2 minimum 33ms/maximum 500ms, SUSP# goes to low after SB_PWRGD goes to low for power down.

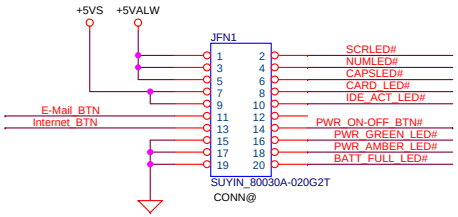


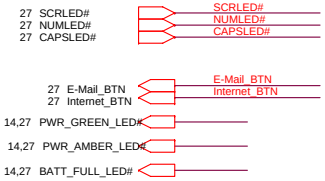
Power Button

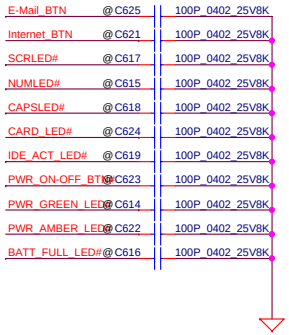








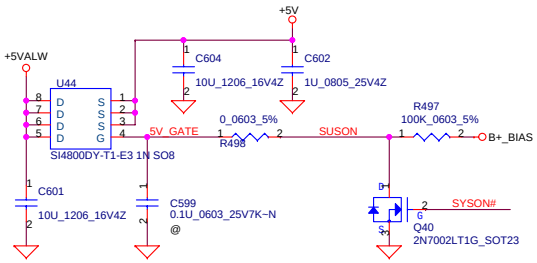




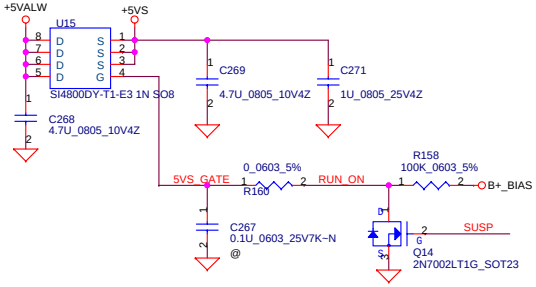
Security Classification	Compal Secret Data		
Issued Date	2005/12/1	Deciphered Date	2006/12/01

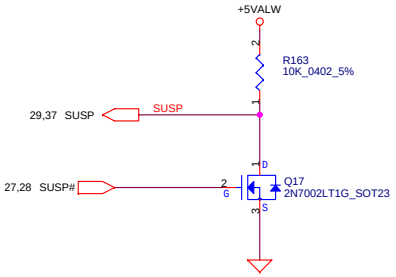
Title	PWR_OK/BTN		
Size: Custom	Document Number: LA-3221P		Rev: 0.1
Date: Friday, January 06, 2006	Sheet 30 of 43		

+5VALW TO +5V

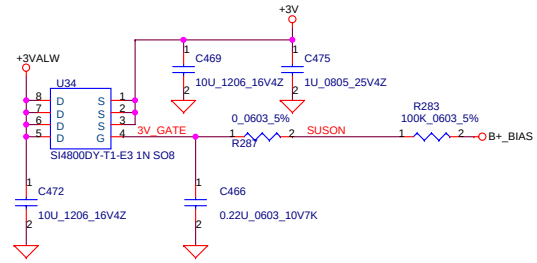


+5VALW TO +5VS

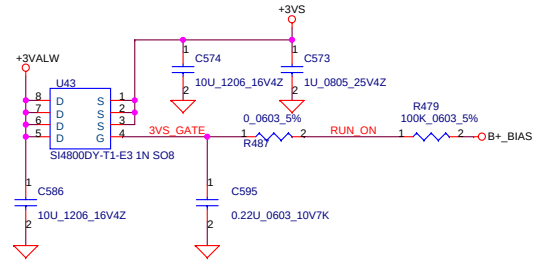


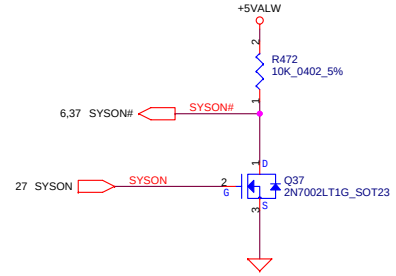


+3VALW TO +3V

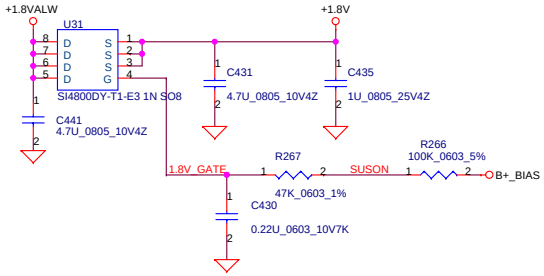


+3VALW TO +3VS

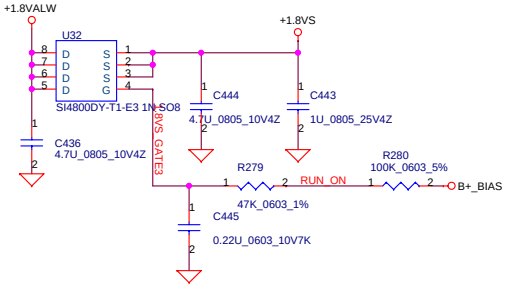


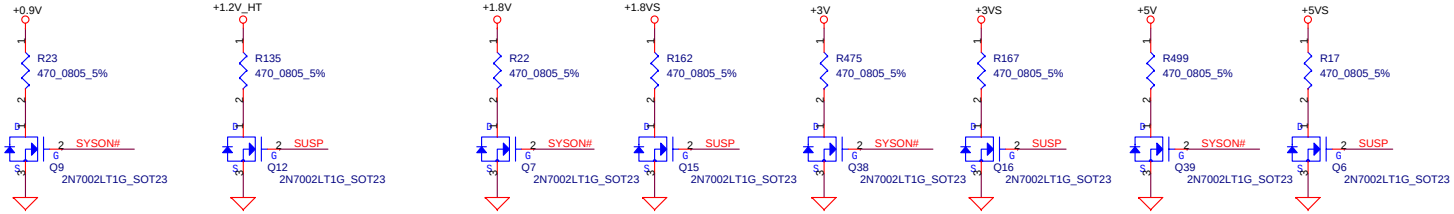


+1.8VALW TO +1.8V



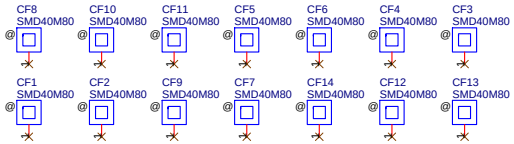
+1.8VALW TO +1.8VS

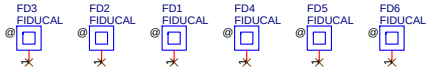


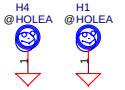


Security Classification	Compal Secret Data		
Issued Date	2005/12/1	Deciphered Date	2006/12/01

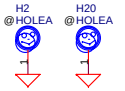
Title	DC Interface		
Size: Custom	Document Number: LA-3221P		Rev: 0.1
Date: Friday, January 06, 2006	Sheet 31 of 43		





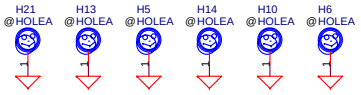


H_R453X394D118P2

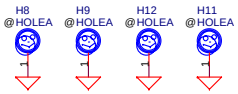


H_S315D118P2

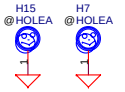
H_C315D197P2



H_S394D118P2

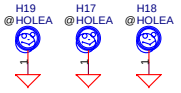


H_C276D165P2--- CPU



H_C236D118BR335X295P2

H_R335X394D118L30P2



H_C236D157P2

H_R354X374D118R20D30P2

H_O177X122D177X122N

H_S315D118U16P2

Chip_Name	Label_Name
EXP_TXP0/SDVOB_RED	PCIE_MTX_C_GRX_P0
EXP_TXN0/SDVOB_RED#	PCIE_MTX_C_GRX_N0
EXP_TXP1/SDVOB_GREEN	PCIE_MTX_C_GRX_P1
EXP_TXN1/SDVOB_GREEN#	PCIE_MTX_C_GRX_N1
EXP_TXP2/SDVOB_BLUE	PCIE_MTX_C_GRX_P2
EXP_TXN2/SDVOB_BLUE#	PCIE_MTX_C_GRX_N2
EXP_TXP3/SDVOB_CLKP	PCIE_MTX_C_GRX_P3
EXP_TXN3/SDVOB_CLKN	PCIE_MTX_C_GRX_N3
EXP_RXP1/SDVO_INT	PCEI_GTX_C_MRX_P1
EXP_RXN1/SDVO_INT#	PCEI_GTX_C_MRX_N1

Security Classification	Compal Secret Data		
Issued Date	2005/12/1	Deciphered Date	2006/12/01

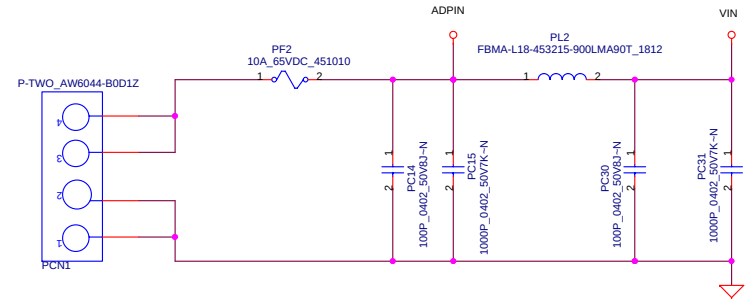
Title: **Screws**

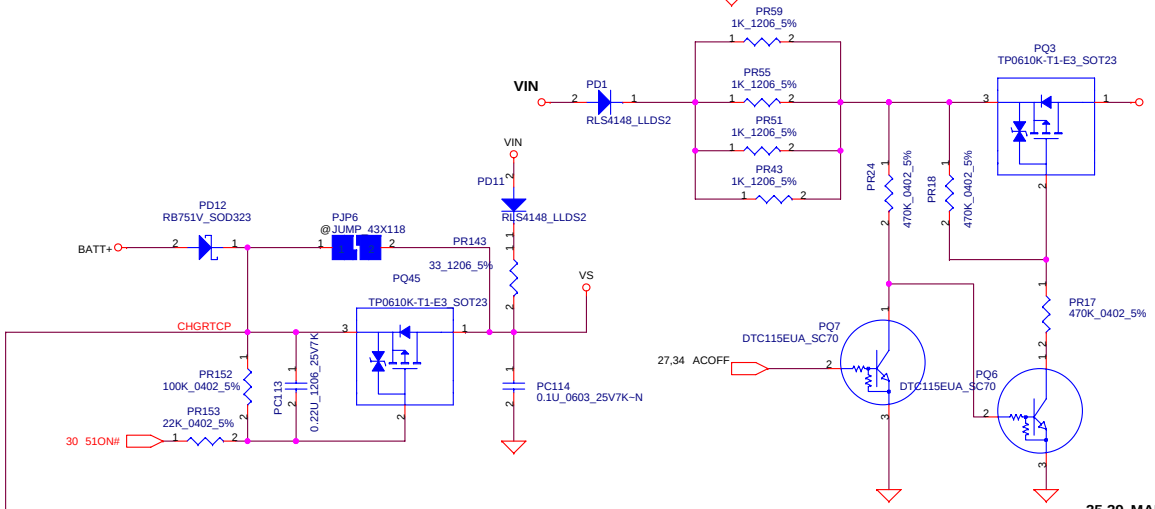
Size: Custom | Document Number: **LA-3221P** | Rev: 0.1

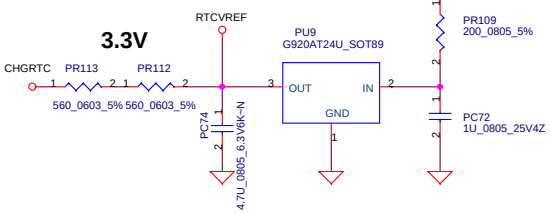
Date: Friday, January 06, 2006 | Sheet 32 of 43

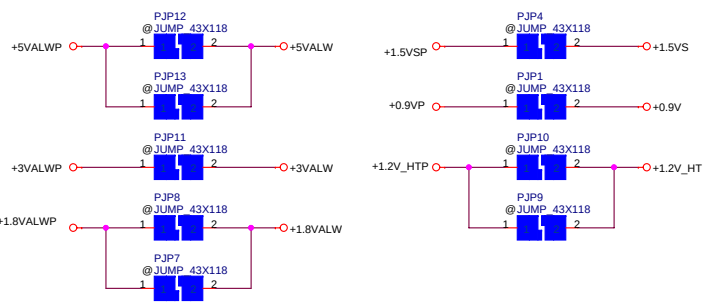
Vin Detector

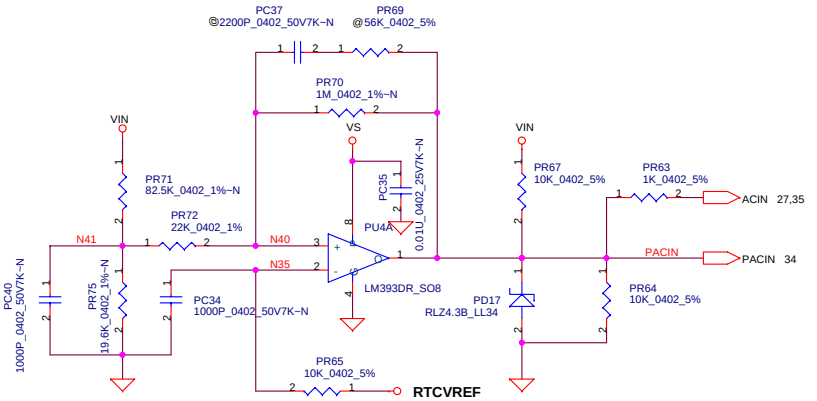
	Max.	typ.	Min.
H-->L	18.234	17.841	17.449
L-->H	17.597	17.210	16.813

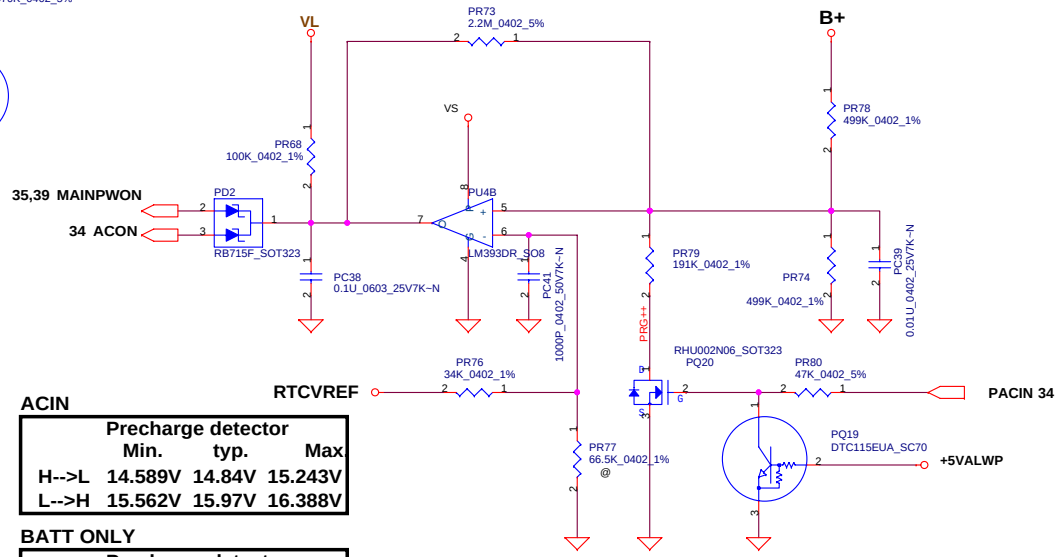












ACIN

Precharge detector

	Min.	typ.	Max
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

Precharge detector

	Min.	typ.	Max
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

Security Classification	Compal Secret Data		
Issued Date	2005/12/1	Deciphered Date	2006/12/01

Title: **DCIN / Precharge**

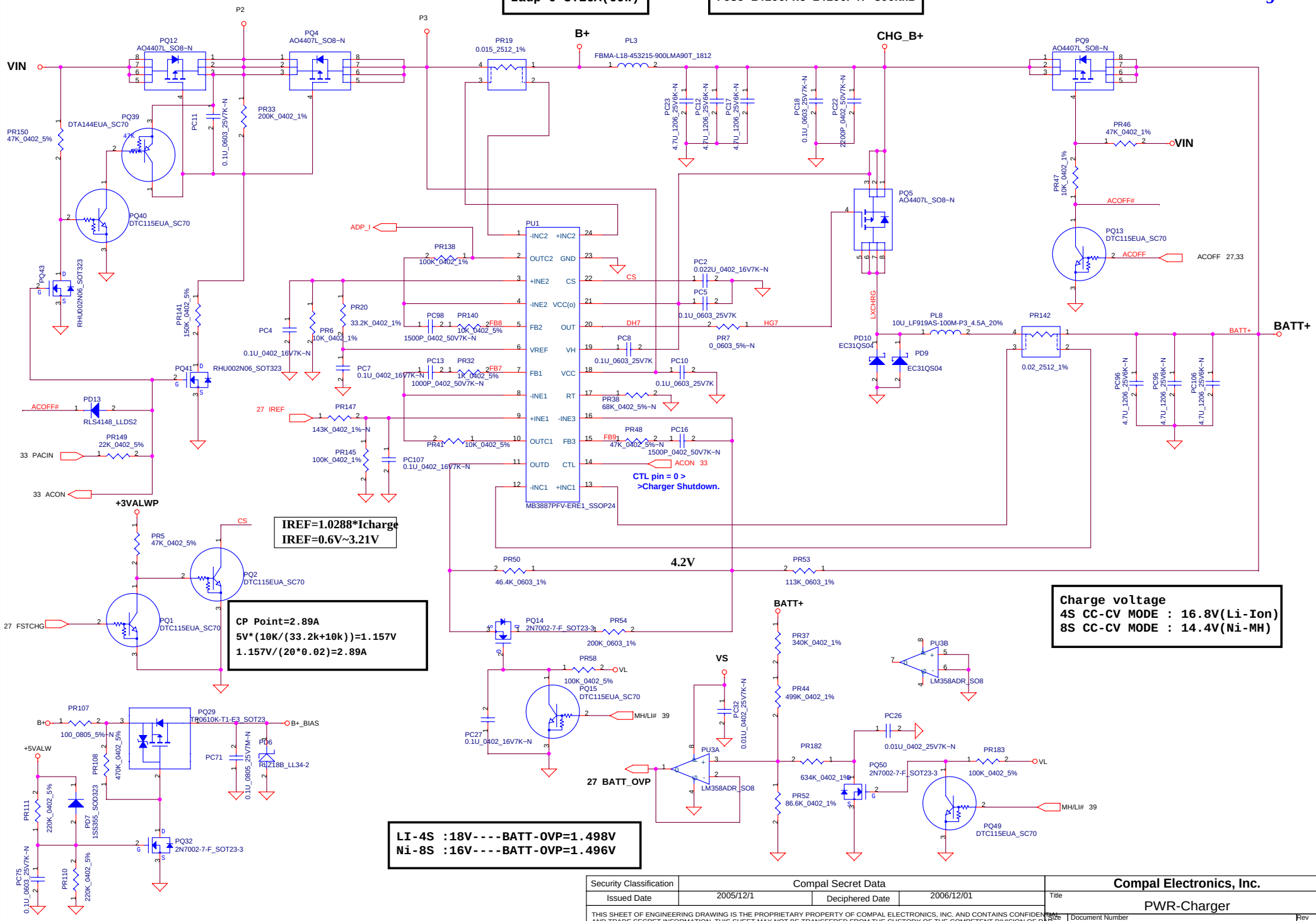
Size	Document Number	Rev
Custom	LA-3221P	0.1

Date: Friday, January 06, 2006 Sheet 33 of 43

Charger

Iadp=0~3.16A(60W)

Fosc=14100/Rt=14100/47=300KHz



Security Classification	Compal Secret Data		
Issued Date	2005/12/1	Deciphered Date	2006/12/01

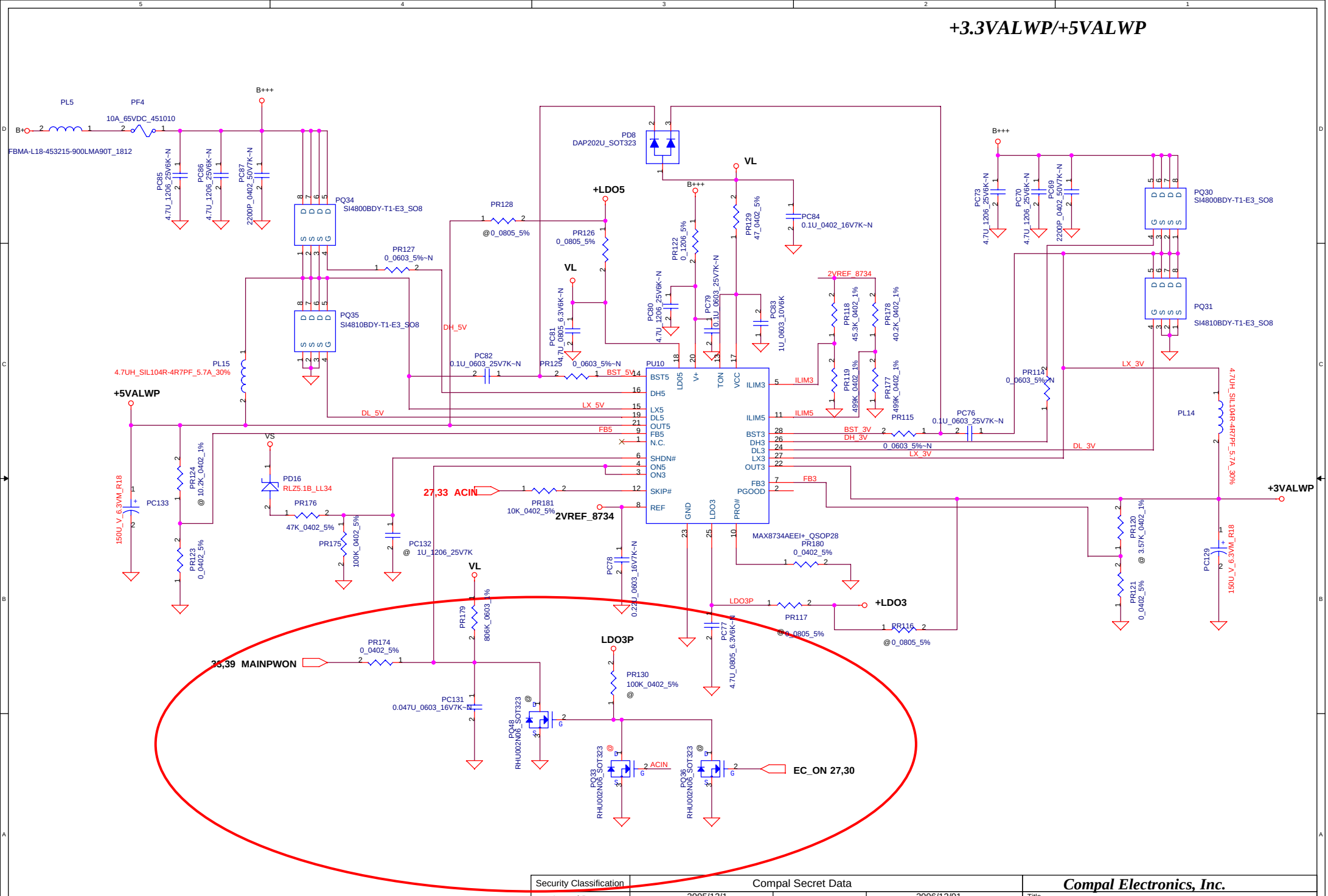
Compal Electronics, Inc.

Title: PWR-Charger

Size: B | Document Number | Rev: 0.1

Date: Friday, January 06, 2006 | Sheet 34 of 43

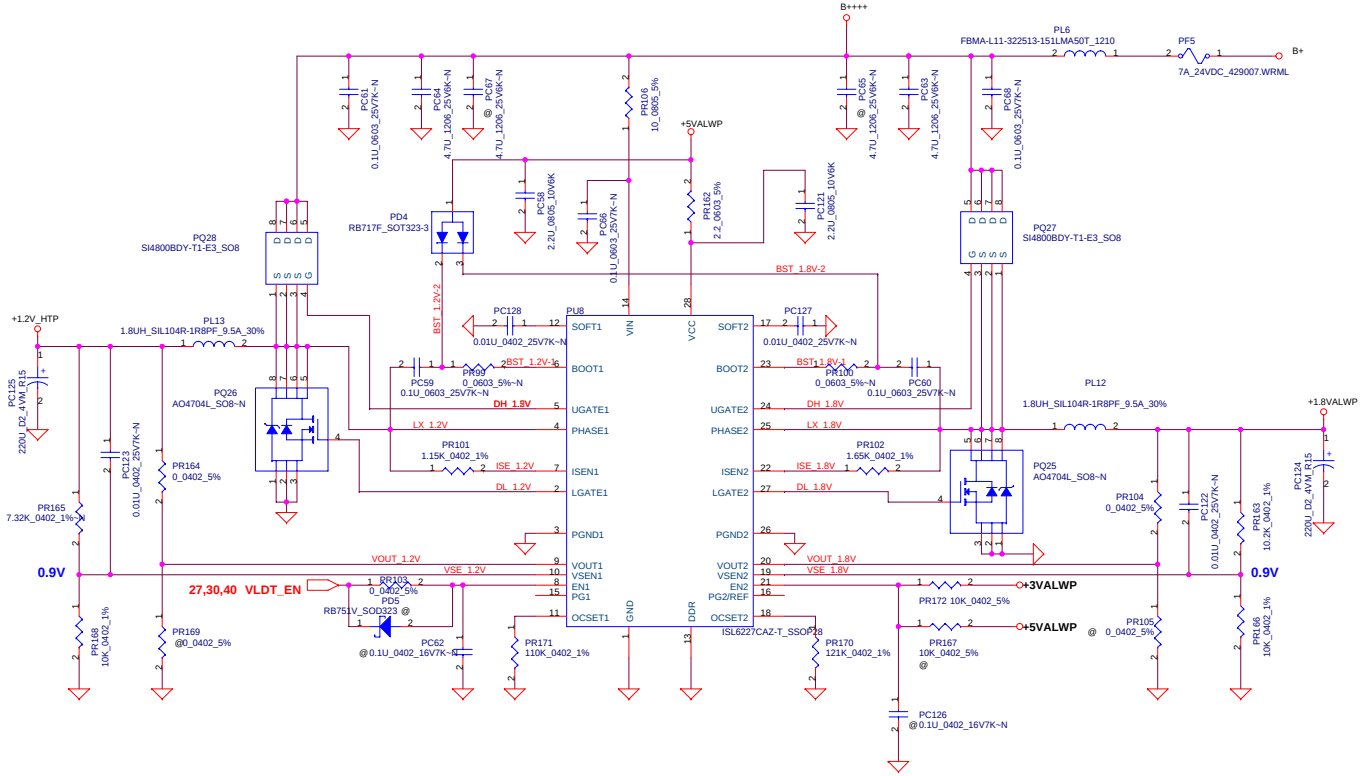
+3.3VALWP/+5VALWP



Security Classification	Compal Secret Data		
Issued Date	2005/12/1	Deciphered Date	2006/12/01

Compal Electronics, Inc.

Title	+5V/+3V		
Size: Custom	Document Number: LA-3221P		Rev: 0.1
Date: Friday, January 06, 2006	Sheet 35 of 43		



Security Classification	Compal Secret Data		
Issued Date	2005/12/1	Deciphered Date	2006/12/01

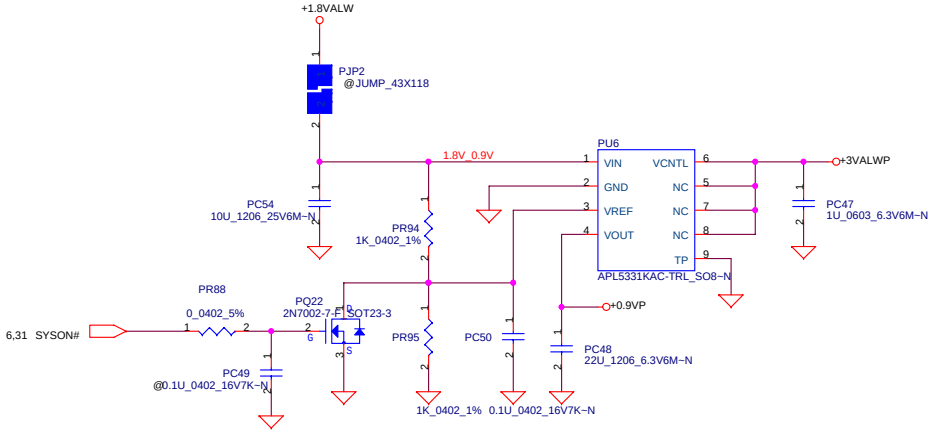
Compal Electronics, Inc.

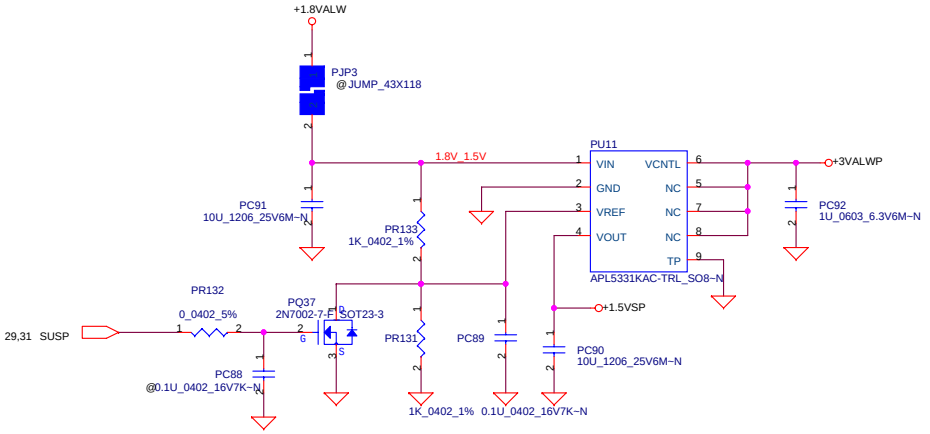
Title: **+1.2V_HTP & +1.8VALWP**

Size	Document Number	Rev
		0.1

Date: Friday, January 06, 2006 Sheet 36 of 43

+1.5VSP/+0.9VSP



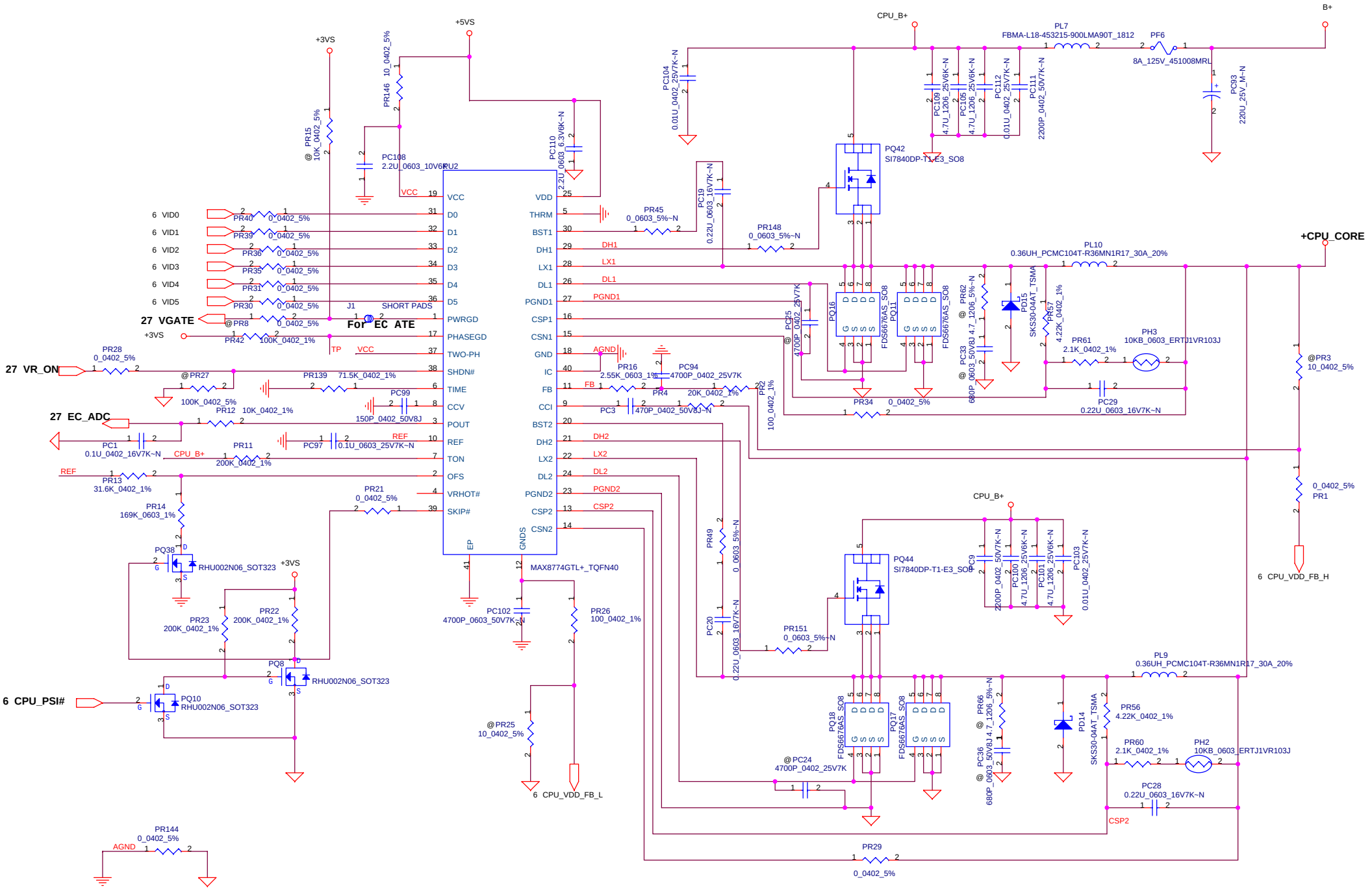


Security Classification	Compal Secret Data		
Issued Date	2005/12/1	Deciphered Date	2006/12/01

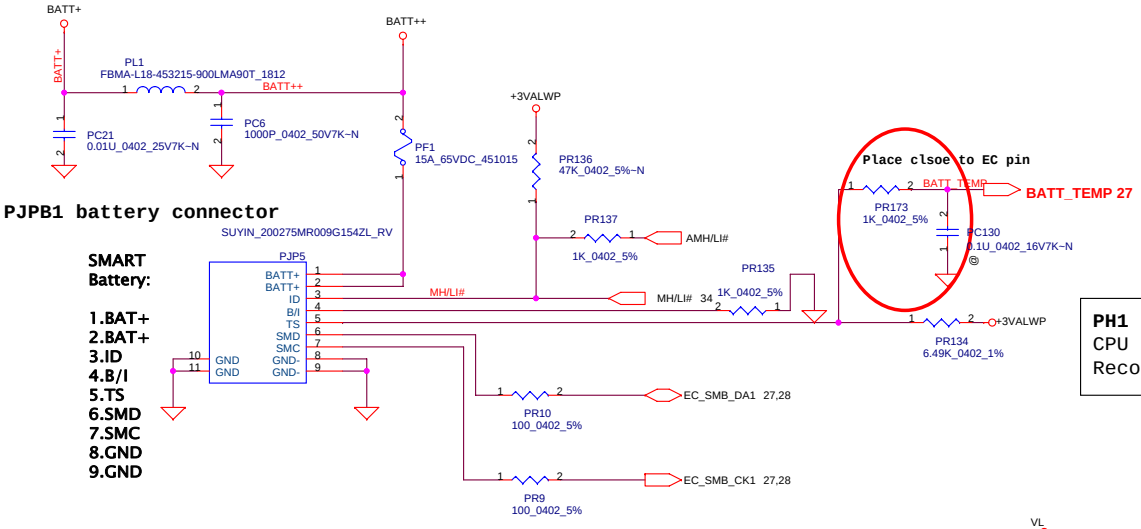
Title: **+1.5VSP/+0.9VP**

Size	Document Number	Rev
Custom	LA-3221P	0.1

Date: Friday, January 06, 2006 Sheet 37 of 43

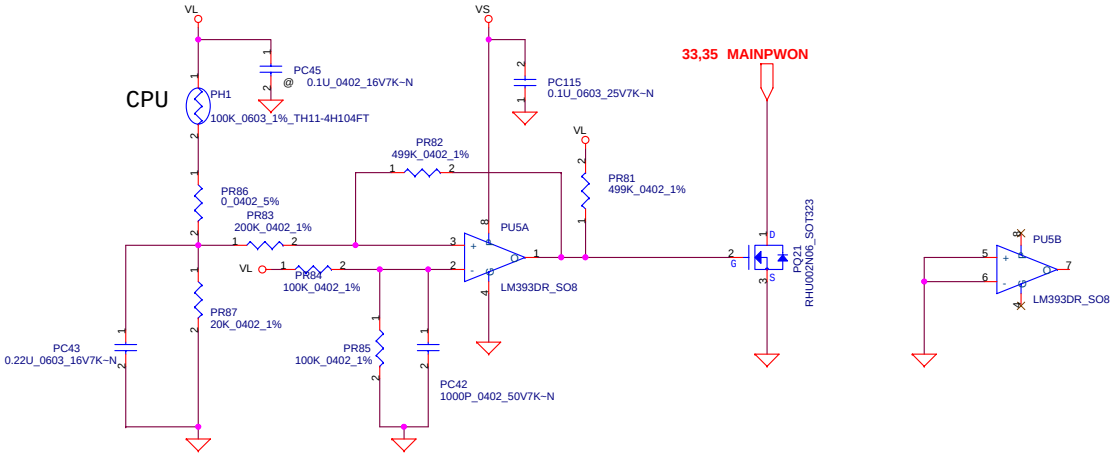

+3VS
+5VS
CPU_B+
B+
+CPU_CORE
MAX8774GTL+_TQFN40
For EC ATE
27 VGATE
27 VR_ON
27 EC_ADC
6 CPU_PSI#
6 CPU_VDD_FB_H
6 CPU_VDD_FB_L
PQ42 SI7840DP-T1-E3_SO8
PQ44 SI7840DP-T1-E3_SO8
PQ38 RHU002N06_SOT323
PQ8 RHU002N06_SOT323
PQ10 RHU002N06_SOT323
PL7 FBMA-L18-453215-900LMA90T_1812
PL10 0.36UH_PCMC104T-R36MN1R17_30A_20%
PL9 0.36UH_PCMC104T-R36MN1R17_30A_20%
PF6 8A_125V_451008MRL
PD15 SK530-04AT_TSMA
PD14 SK530-04AT_TSMA
PH3 10KB_0603_ERTJ1VR103J
PH2 10KB_0603_ERTJ1VR103J
PQ16 FDS6676AS_SO8
PQ11 FDS6676AS_SO8
PQ18 FDS6676AS_SO8
PQ17 FDS6676AS_SO8
J1 SHORT PADS
PR146 10_0402_5%
PR15 10K_0402_5%
PC108 2.2U_0603_10V6K
PC110 2.2U_0603_6.3V6K~N
PR45 0_0603_5%~N
PC19 0.22U_0603_16V7K~N
PR148 0_0603_5%~N
PR16 2.55K_0603_1%
PC94 4700P_0402_25V7K
PR4 20K_0402_1%
PC3 470P_0402_50V8J~N
PR2 100_0402_1%
PC25 4700P_0402_25V7K
PR34 0_0402_5%
PC29 0.22U_0603_16V7K~N
PR61 2.1K_0402_1%
PR57 4.22K_0402_1%
PR62 4.7_1206_5%~N
PC33 680P_0603_50V8J
PR3 10_0402_5%
PR1 0_0402_5%
PR49 0_0603_5%~N
PC20 0.22U_0603_16V7K~N
PR151 0_0603_5%~N
PC24 4700P_0402_25V7K
PR36 4.7_1206_5%~N
PC36 680P_0603_50V8J
PR56 4.22K_0402_1%
PR60 2.1K_0402_1%
PC28 0.22U_0603_16V7K~N
PR29 0_0402_5%
PR144 0_0402_5%
PR21 0_0402_5%
PR26 100_0402_1%
PC102 4700P_0603_50V7K~N
PR25 10_0402_5%
PR23 200K_0402_1%
PR22 200K_0402_1%
PR14 169K_0603_1%
PR13 31.6K_0402_1%
PC1 0.1U_0402_16V7K~N
PR12 10K_0402_1%
PR11 200K_0402_1%
PC97 0.1U_0603_25V7K~N
PC99 150P_0402_50V8J
PR139 71.5K_0402_1%
PR28 0_0402_5%
PR27 100K_0402_5%
PR8 0_0402_5%
PR42 100K_0402_1%
PR40 0_0402_5%
PR39 0_0402_5%
PR36 0_0402_5%
PR35 0_0402_5%
PR31 0_0402_5%
PR30 0_0402_5%
PC104 0.01U_0402_25V7K~N
PC109 4.7U_1206_25V6K~N
PC105 4.7U_1206_25V6K~N
PC112 0.01U_0402_25V7K~N
PC111 2200P_0402_50V7K~N
PC93 220U_25V_M~N
PC9 2200P_0402_50V7K~N
PC100 4.7U_1206_25V6K~N
PC101 4.7U_1206_25V6K~N
PC103 0.01U_0402_25V7K~N
VID0
VID1
VID2
VID3
VID4
VID5
VCC
TP
AGND
CSP2
DH1
LX1
DL1
PGND1
DH2
LX2
DL2
PGND2
CSP1
CSN1
CSP2
CSN2
FB
CCI
REF
CPU_B+
Security Classification
Compal Secret Data
Issued Date
2005/12/1
Deciphered Date
2006/12/01
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.
Title
+CPU_CORE
Size
Custom
Document Number
HCW51 LA-3121P
Rev
0.1
Date:
Friday, January 06, 2006
Sheet
38
of
43

Battery Connect/OTP



CPU

PH1 under CPU botten side :
CPU thermal protection at 90 +-3 degree C
Recovery at 50 +-3 degree C

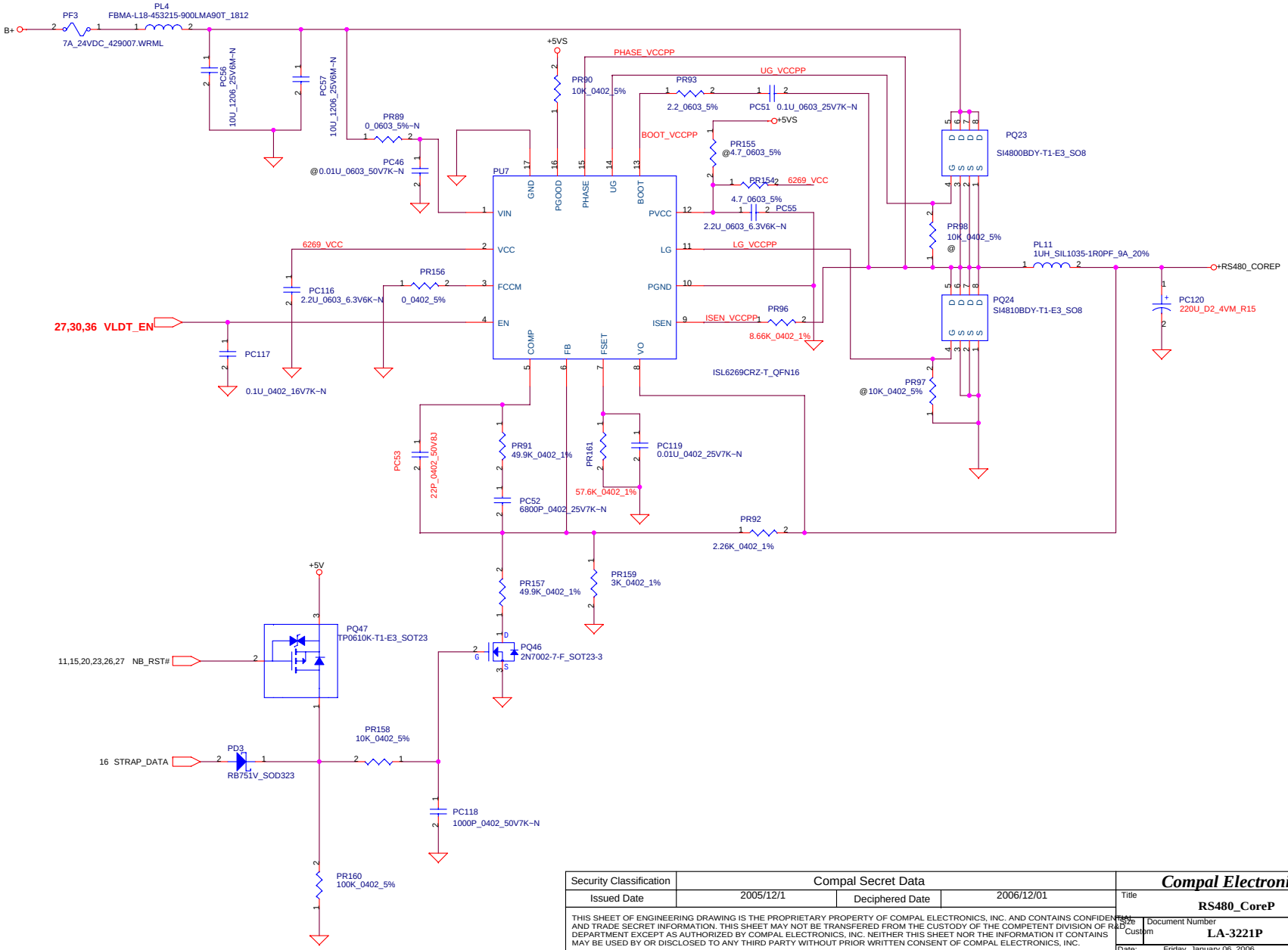


Security Classification	Compal Secret Data		
Issued Date	2005/12/1	Deciphered Date	2006/12/01

Title: **BATTERY CONN**

Size	Document Number	Rev
Custom	LA-3221P	0.1

Date: Friday, January 06, 2006 Sheet 39 of 43



Security Classification	Compal Secret Data		
Issued Date	2005/12/1	Deciphered Date	2006/12/01

Compal Electronics, Inc.

Title	RS480_CoreP		
Size: Custom	Document Number: LA-3221P		Rev: 0.1
Date: Friday, January 06, 2006	Sheet 40 of 43		

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1							
2							
3							
4							
5							
6							
7							
8							
10							
11							
12							
13							
14							
15							
16							
17							

Next: PR238, PC202, PQ56, PD42, PJP21

Compal Electronics, Inc.

Title: EE-PIR

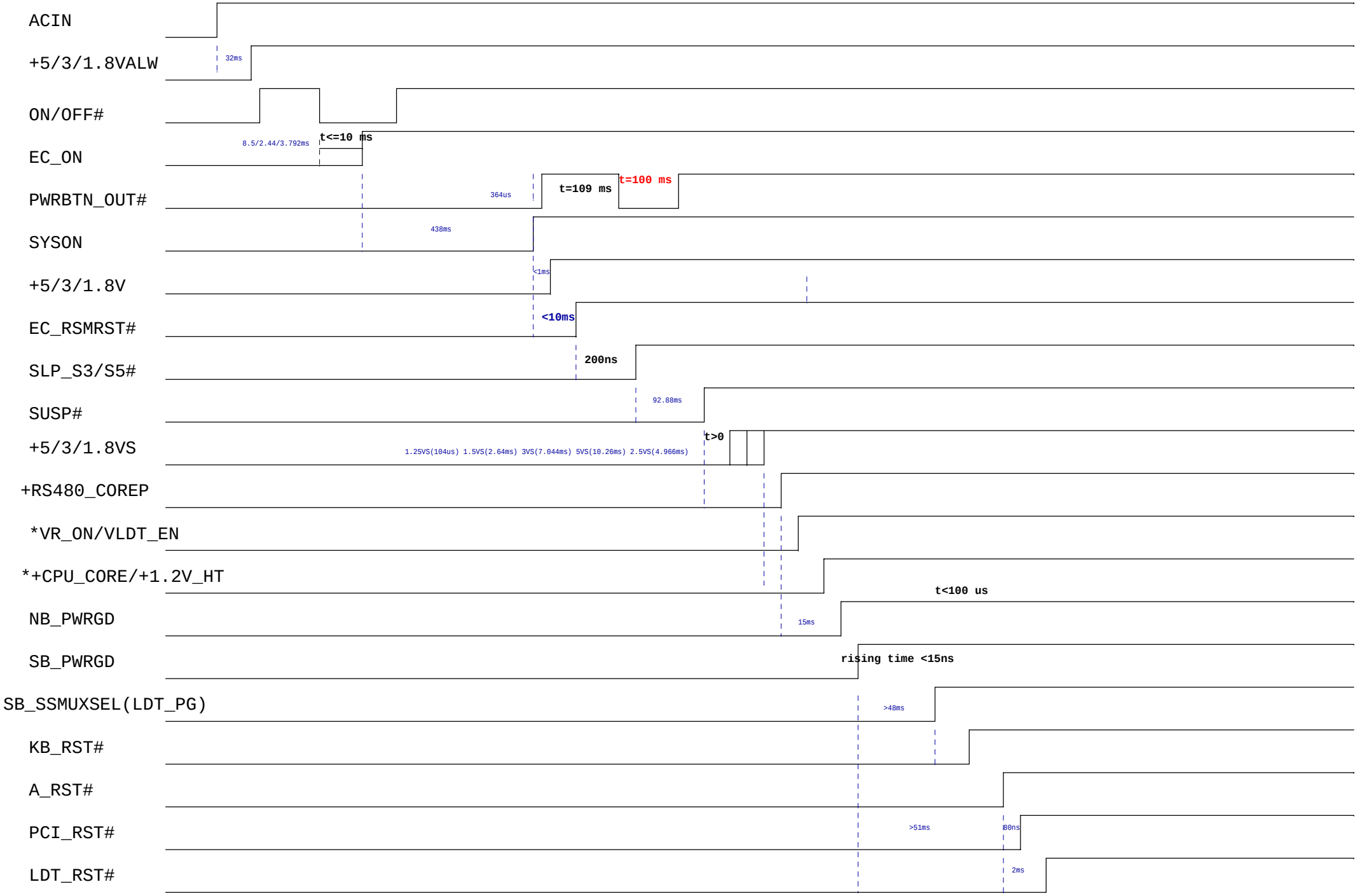
Size: | Document Number: LA-3221P | Rev: 0.1

Date: Friday, January 06, 2006 | Sheet 41 of 43

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	VER	Phase
1		CPU bypass Cap change to Proadlizer 1200uF.		7			
2		Change Felica connector package.		28	From 4pin change to 6 pin.		
3		Change R536 value.		24	R536 change to 10K ohm		
4		Change net (WLAN_ACT) from pin 3 to pin46.		26	Add R516, R538		
5		RS485MC only support 2 lane PCI-E		10,15	A-LINK 4X----->2X Change PCI-E port 2,3 ----->0,1		
6		Part reference rename for layout		All	Part reference change		
7		To support WOL on S3/S4/S5		23	Change the power rail from +3V to +3VALW.		
8		Change R185 BOM structure		23			
9							

Title: PIR (HW)
Size: Custom | Document Number: LA-3221P | Rev: 0.1
Date: Friday, January 06, 2006 | Sheet 42 of 43



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2005/03/11	Deciphered Date	2006/03/11
Title	Power Sequence		
Size	Document Number	LA-3221	Rev 0.1
Date:	Friday, January 06, 2006	Sheet 43 of 43	