Daytona ATI Block Diagram

(RoHS)

Project code: 91.4P901.001
PCB P/N : 06201
REVISION : -1

Clock Generator
ICS951413/CY28RS400
3

Mobile CPU
Yonah
4,5

4X DATA
2X ADDRESS
AGTL+
533/667MHz

SMBus
Thermal Sensor & Fan
G792
20

ATI NB RC415ME
AGTL+ P4 CPU I/F
DDR2 I/F
INTEGRATED GRAPHICS
TVOUT/SVIDEO
LVDM(LVDS)
1 X16 PCIE VIDEO/SDVO I/F
1 X4 PCIE SB I/F
6 X1 PCIE GPP I/F
5,6,7,8,9,10

LCD CONN
XGA/SXGA+
14
LVDS

CRT CONN
13
CRT

DDR2 400/533/667 MHz

UNBUFFERED DDR2 SODIMM
11,12

UNBUFFERED DDR2 SODIMM
11,12

PCI-E

GIGA RTL8111B-GR
23

RJ45 CONN
24

PWR SW
TPS2224A
27

CARDBUS
PCI 1520
GHK
25/B/1
26

CARDBUS
TWO SLOT
27

PCI BUS

PCIE
X4

Mini-Card
802.11a/b/g/n
25

USB 2.0

USB x 4
22

RJ11 CONN
24

MODEM
MDC 1.5 Card
22

AZALIA

SATA

HDD
21

SIDE/PATA

Optical
21

LPC Bus

LINE IN
MIC IN

Audio CODEC
ALC883
30

PS2
34

KBC
ENE KB3910
32

FlashRom
MX29LV800
2M
35

NS SIO
PC87392
36

TPM1.2
28

OP AMP
G1432
31

LINE OUT

2CH SPEAKER

Touch Pad
33

Int. KB
33

SERIAL PORT
29

PRN PORT
29

FDD
21

SYSTEM DC/DC MAX8743A	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S5 1D2V_S3 +15V

SYSTEM DC/DC TPS51120	
INPUTS	OUTPUTS
DCBATOUT	3D3V_S5 5V_S5

MAXIM CHARGER MAX8725	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 4.0A 5V 100mA

CPU DC/DC ISL6262	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 27A

CARD 0D9V (LDO) TPS51100	
INPUTS	OUTPUTS
5V_S5	0D9V_S0

CARD 1D05V (LDO) APL5912	
INPUTS	OUTPUTS
1D2V_S3	1D05V_S0

CPU PLL 1D5V(LDO) APL5308	
INPUTS	OUTPUTS
3D3V_S0	1D5V_S0

PCB LAYER

L1: Signal 1
L2: VCC
L3: Signal 2
L4: Signal 3
L5: GND
L6: Signal 4

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Title: Block Diagram

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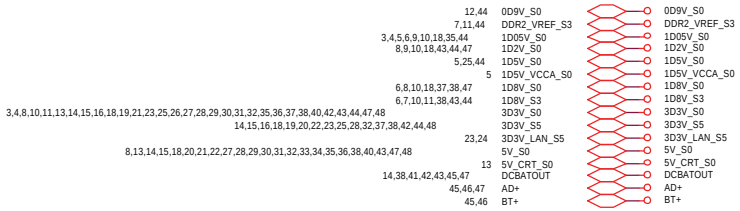
Date: Thursday, June 15, 2006 | Sheet 1 of 48



PCI RESOURCE TABLE

USB Port	Key West Define
USBP[0]	USB CONN2
USBP[1]	USB CONN3
USBP[2]	Mini card used
USBP[3]	NC
USBP[4]	USB CONN4
USBP[5]	NC
USBP[6]	Finger printer
USBP[7]	USB CONN1

DEVICE	IDSEL	PCI IRQ	REQ# / GNT#
Cardbus	AD22	INT_E#	REQ0#/GNT0#

Device	SMBus addr.
Clock Gen.	D2
DDR Module 1	A2
DDR Module 2	A0
Battery	16
Thermal control	7A

PCIE Port	DK1 ATI Define
PE[0]	NC
PE[1]	NC
PE[2]	Mini Card
PE[3]	LAN

<Core Design>

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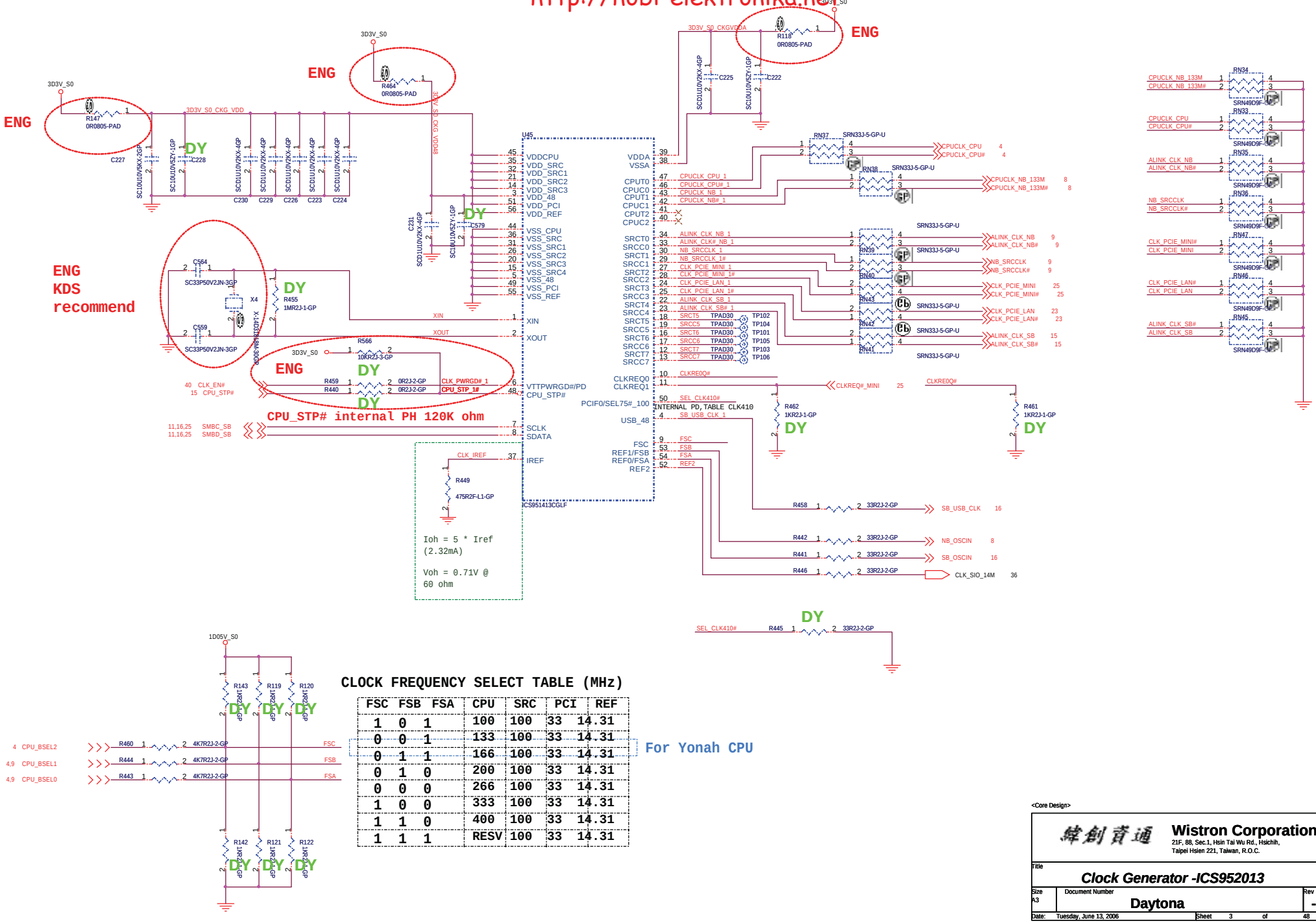
Title: **Table of Content / HISTORY**

Size: A3 | Document Number: Daytona | Rev: -1

Date: Tuesday, June 13, 2006 | Sheet 2 of 48



FSC	FSB	FSA	CPU	SRC	PCI	REF
1	0	1	100	100	33	14.31
0	0	1	133	100	33	14.31
0	1	1	166	100	33	14.31
0	1	0	200	100	33	14.31
0	0	0	266	100	33	14.31
1	0	0	333	100	33	14.31
1	1	0	400	100	33	14.31
1	1	1	RESV	100	33	14.31

<Core Design>

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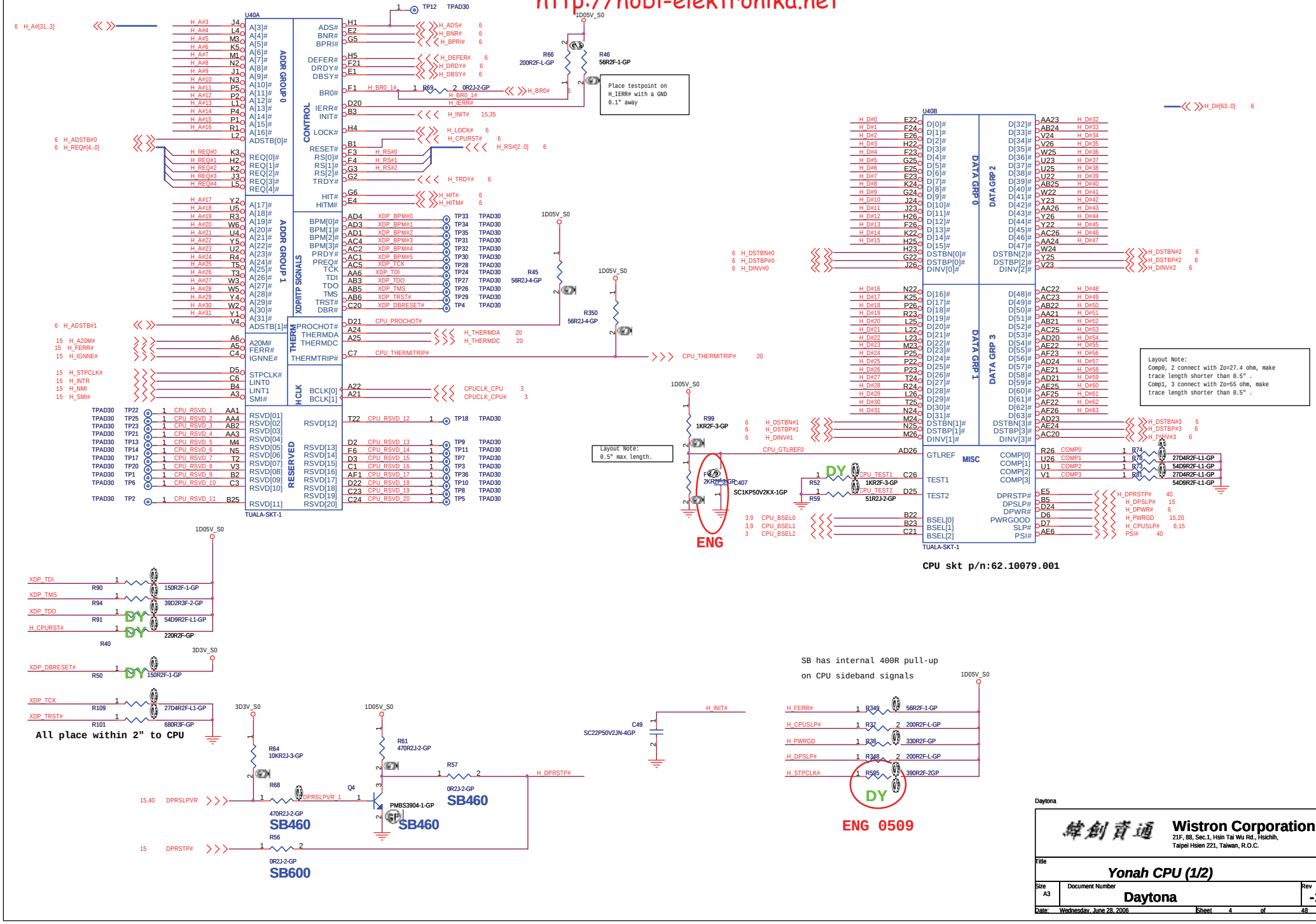
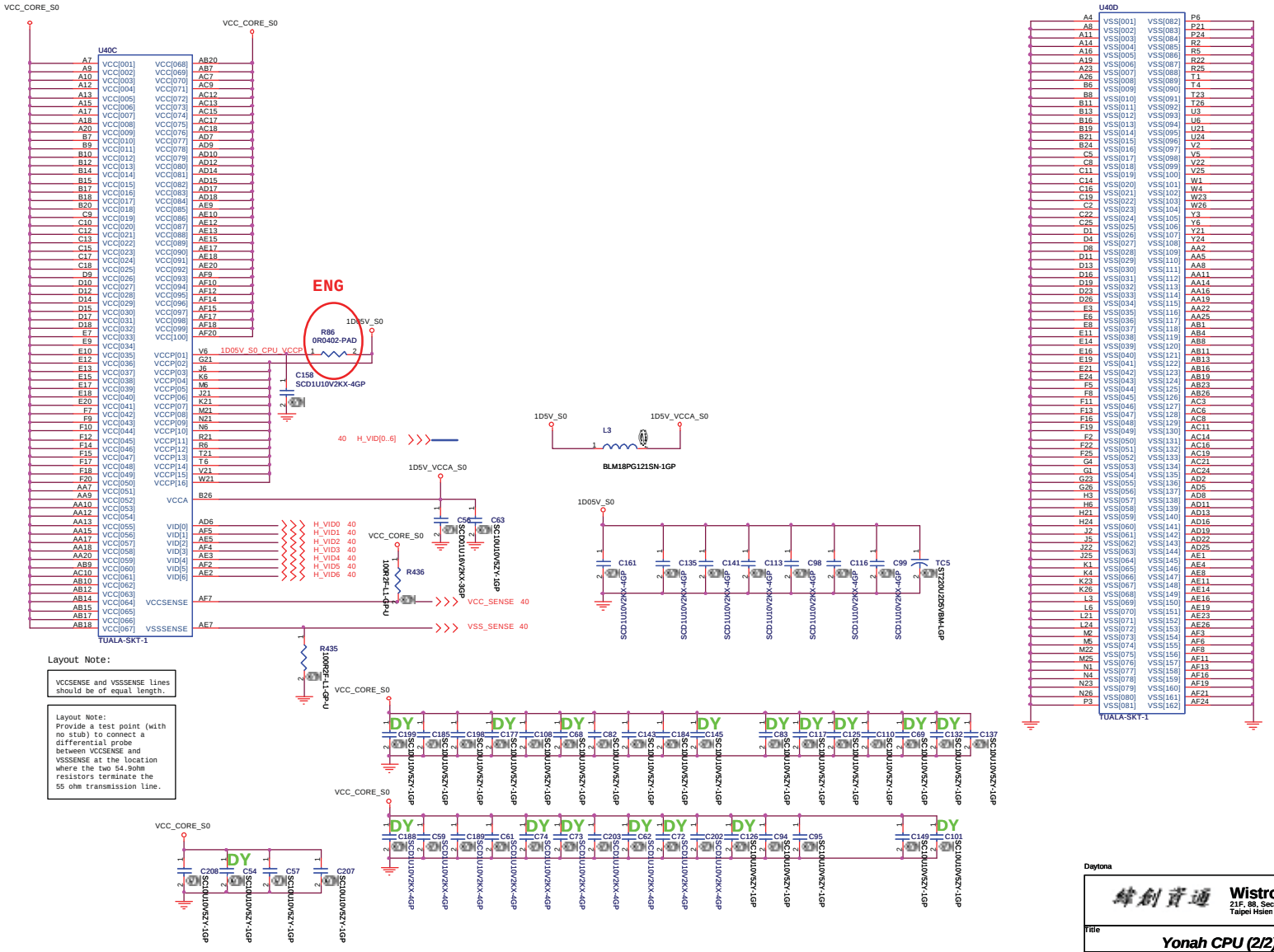
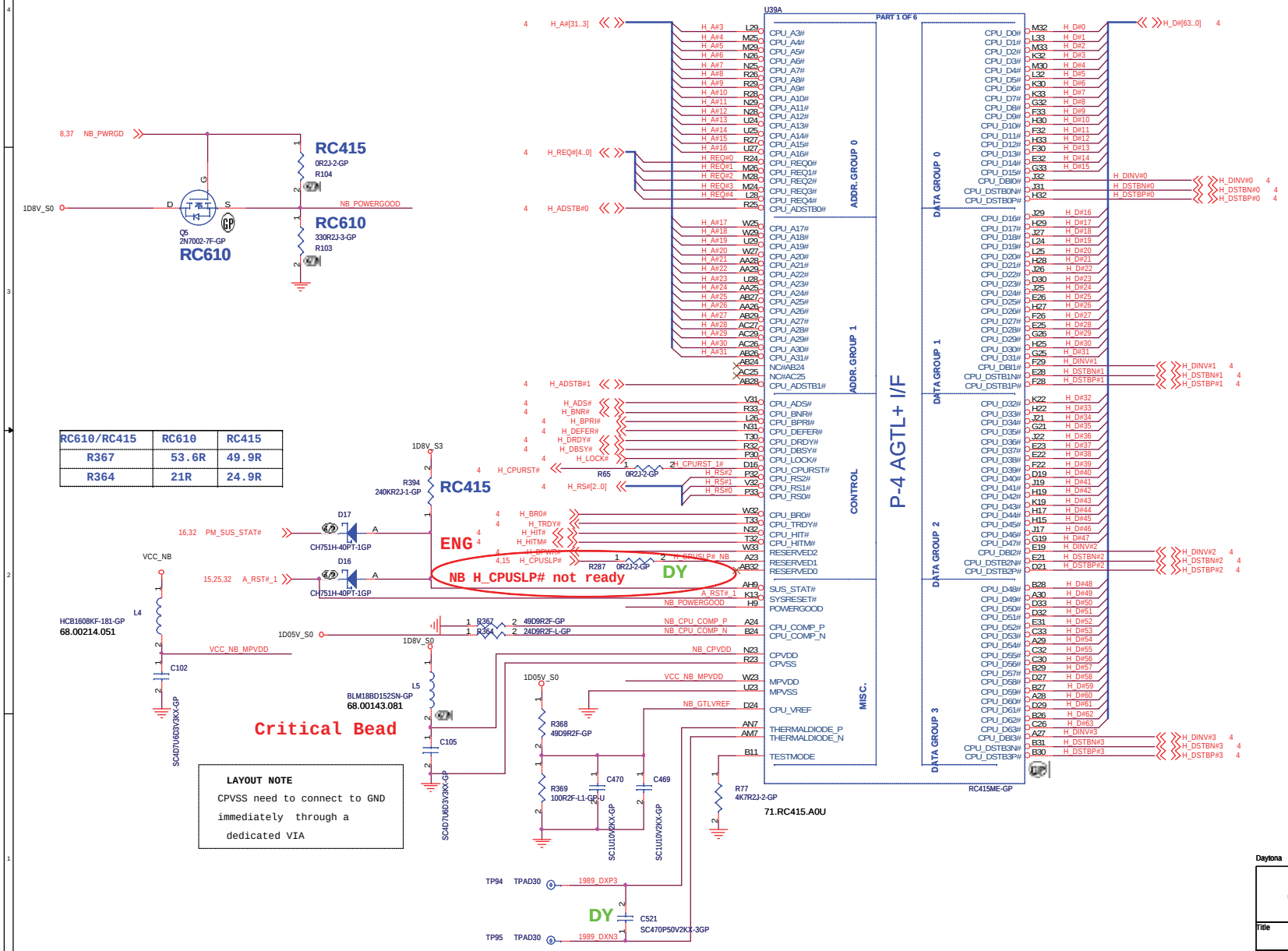
Date: Tuesday, June 13, 2006 | Sheet 3 of 48







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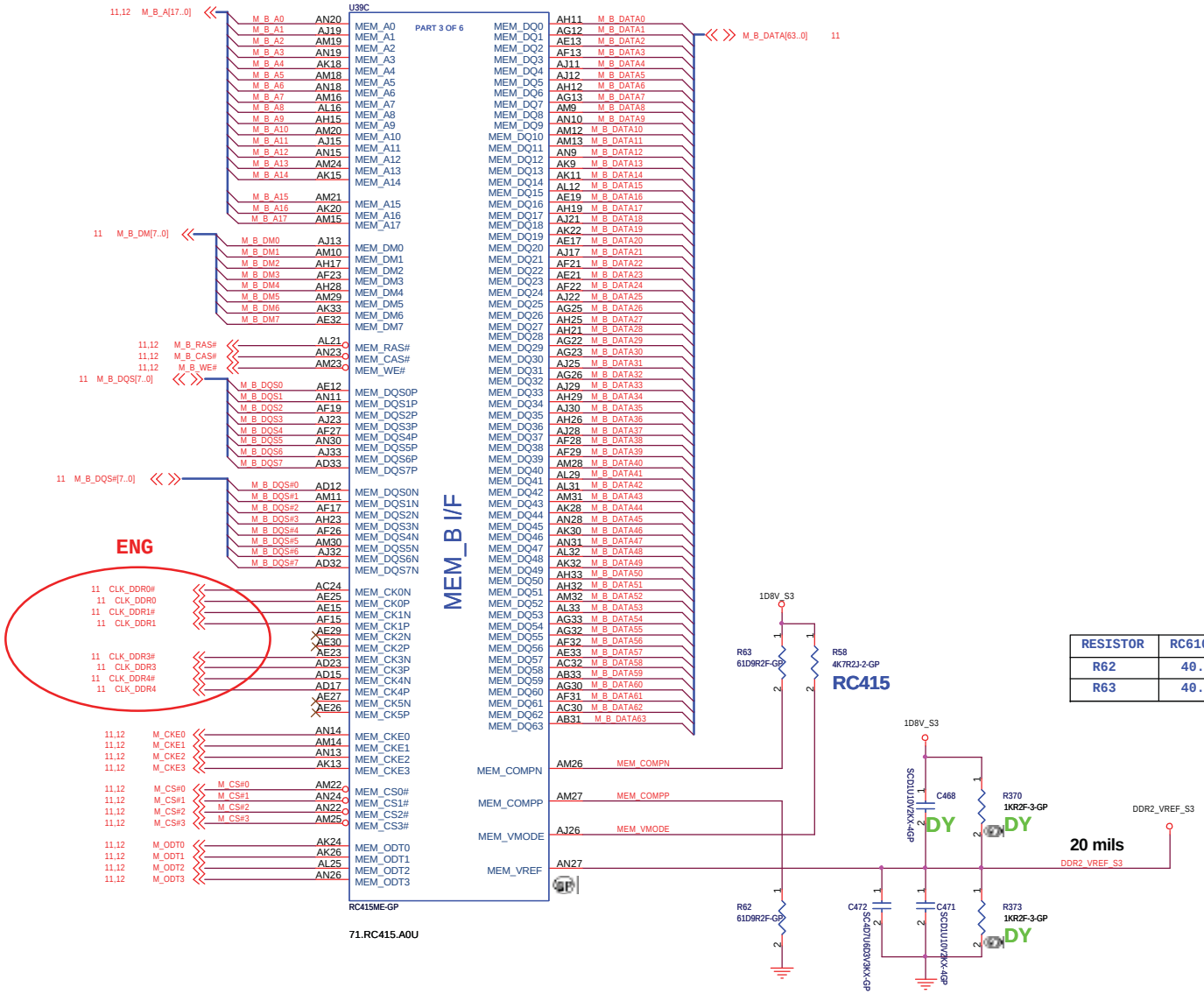
Title: RC415ME (1 of 5) Host I/F

Size	Document Number	Rev
Custom	Daytona	-1

Date: Wednesday, June 28, 2006 Sheet 6 of 48



RESISTOR	RC610	RC415
R62	40.2R	61.9R
R63	40.2R	61.9R

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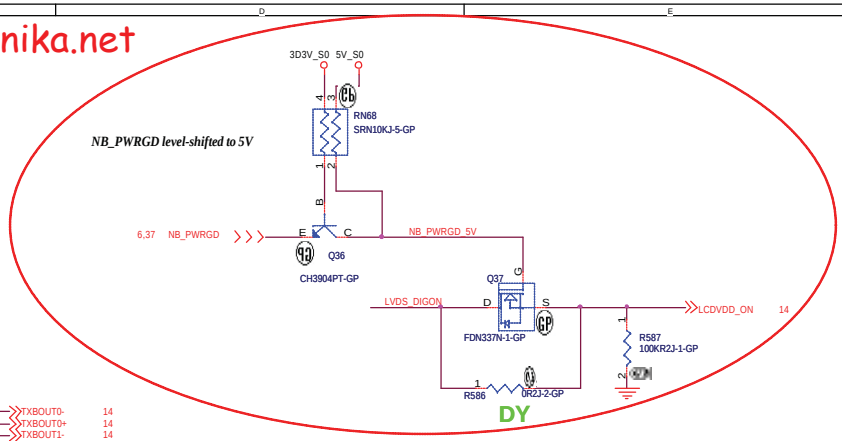
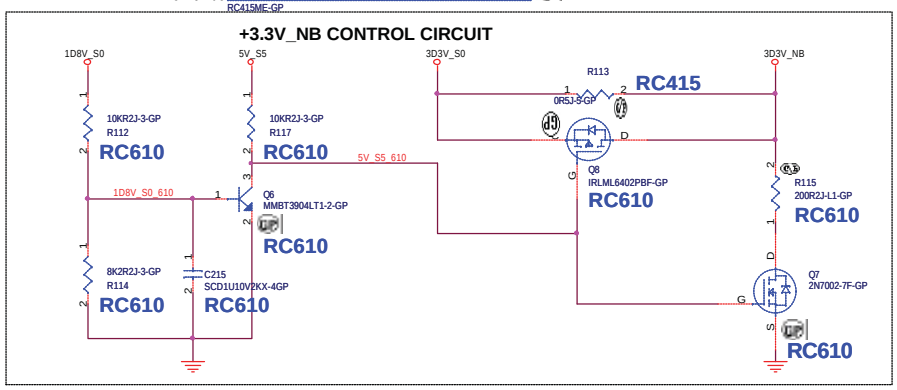
Title: RC415MB (2 of 5) Memory I/F

Size: A3 | Document Number: Daytona | Rev: -1

Date: Wednesday, June 28, 2006 | Sheet 7 of 48

ENG 0424





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Title: RC415ME (3 of 5) Vedio I/F			
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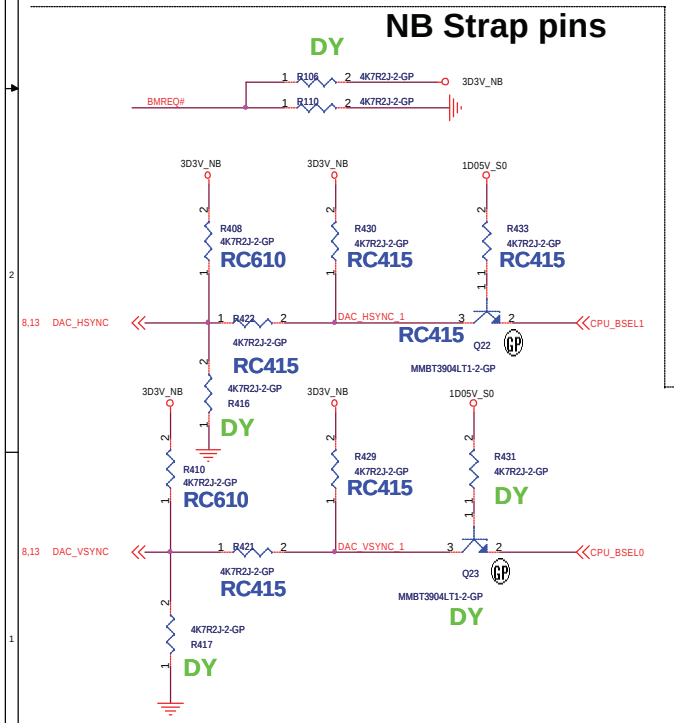
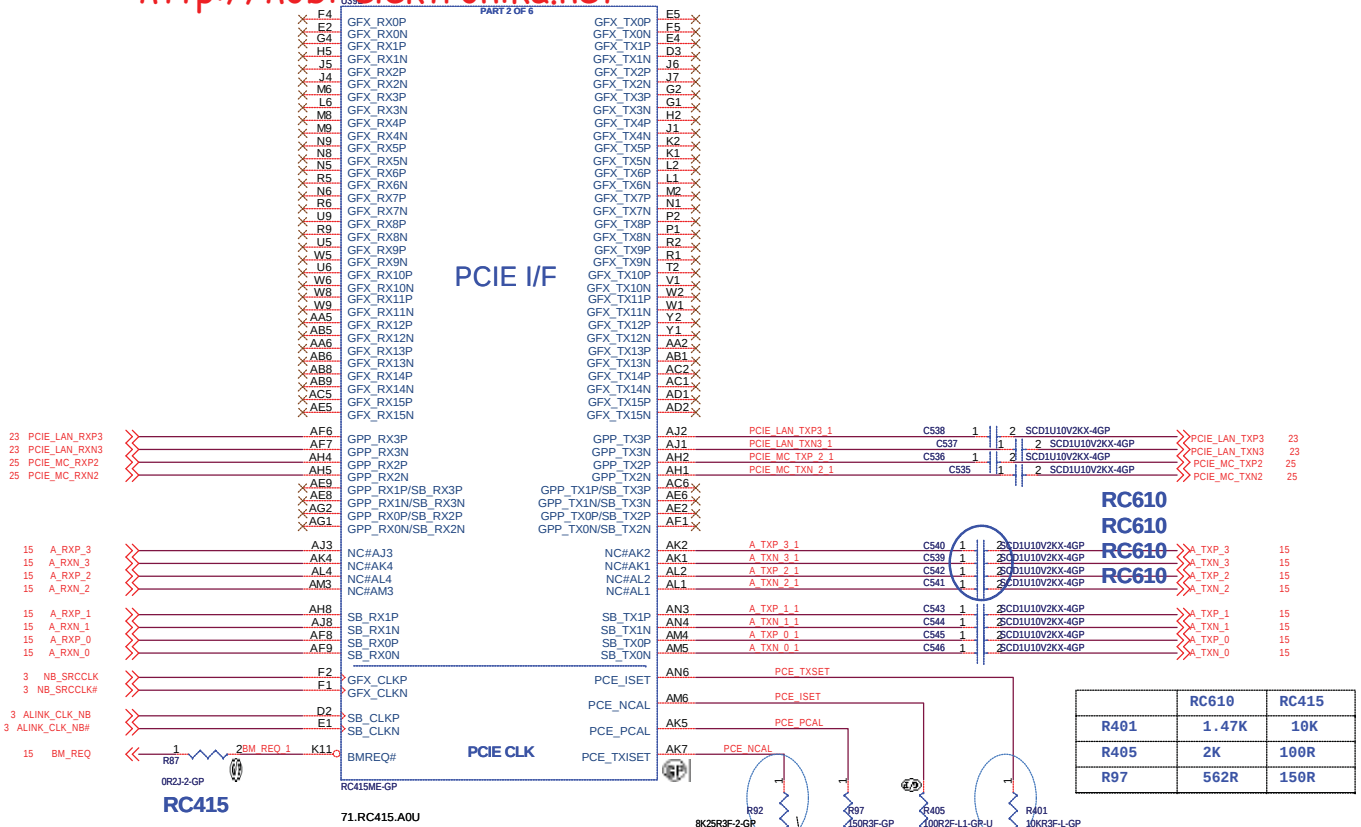
RC610 STRAPS	RC415 STRAPS
DAC_HSYNC: STRP_INTGFX_DISABLE DEFAULT: 0 0: ENABLE 1: DISABLE	BMREQ#&HSYNC&VSYNC: FSB CLK SPEED
DAC_VSYNC: STRAP_MOBILE_GFX DEFAULT: 1 0: DESKTOP GRAPHICS DEVICE 1: MOBILE GRAPHICS DEVICE	BMREQ#&HSYNC&VSYNC: FSB CLK SPEED
	BMREQ#&HSYNC&VSYNC: FSB CLK SPEED
STRP_DATA: STRP_MEMSTRAPS DEFAULT: 1 0: SELECT MEMORY CHA A AS DEBUG BUS 1: NORMAL MODE	STRP_DATA:Debug strap DEFAULT: 1 1: E2PROM STRAPING 0: MEMORY CHANNEL STRAPING
DDC_DATA: STRAP_MEMVMODE DEFAULT: 1 0: DDR3 1: DDR2	
	DAC_SCL: CPU VCC DEFAULT:1 1: DESKTOP 0: MOBILE

NB Strap pins



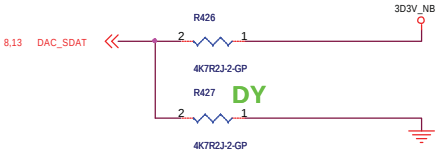
PCIE I/F

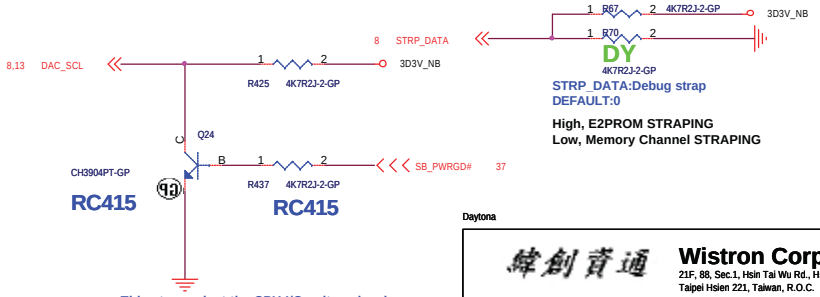


	RC610	RC415
R401	1.47K	10K
R405	2K	100R
R97	562R	150R

FSB SPEED CLK Strap

BMREQ#	HSYNC	VSYNC	Freq.
0	0	0	100MHZ
0	0	1	133MHZ
0	1	0	------
0	1	1	166MHZ





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Title: RC415ME (4 of 5) PCI-E & Strap

Size	Document Number	Rev
A3	Daytona	-1

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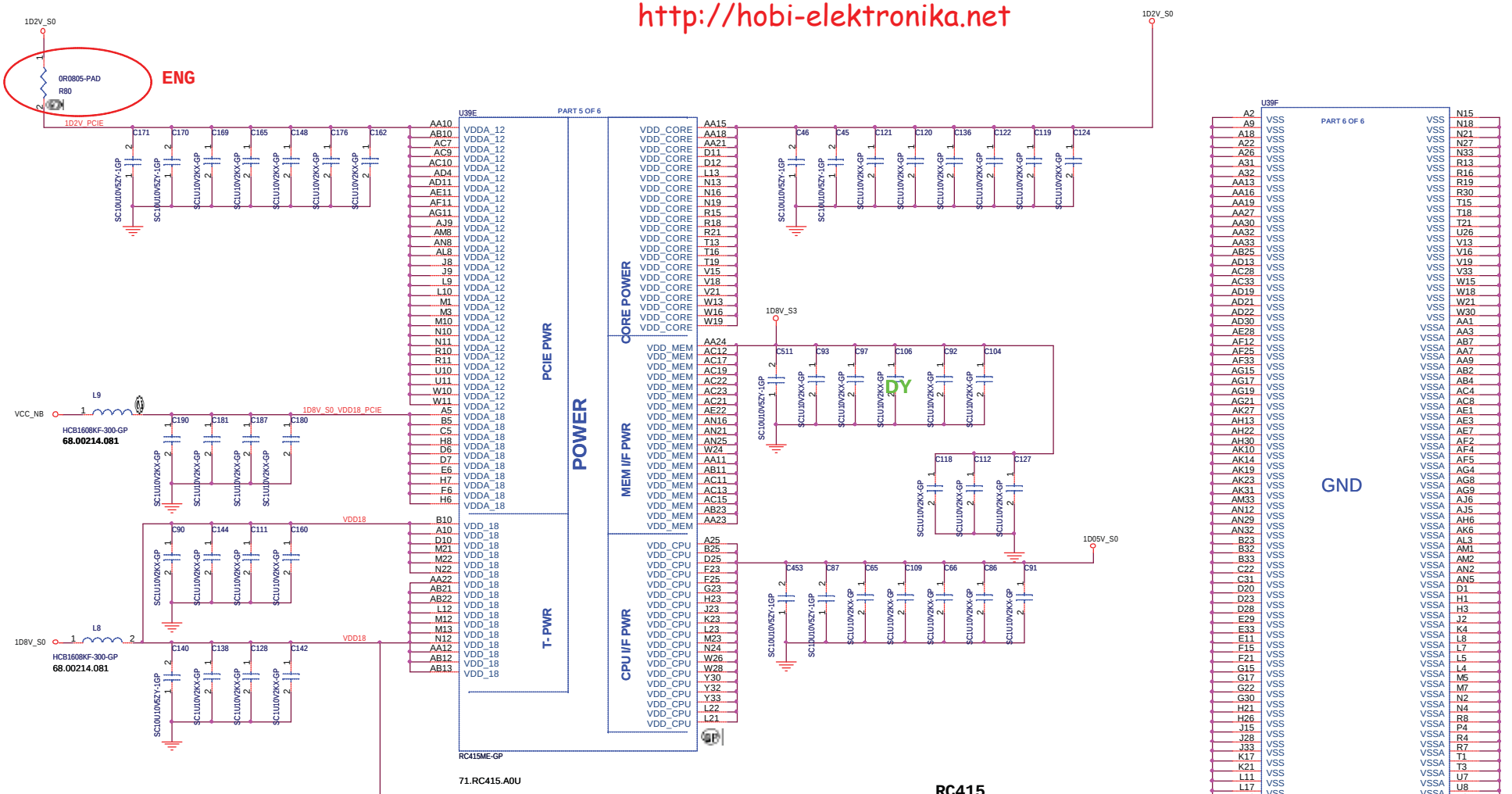

Power Sequence Requirement

	RC415	RC610
3D3V_NB	3D3V_S0	3D3V_S0
1D8V_S3	1D8V_S3	1D8V_S3
1D8V_S0	1D8V_S0	1D8V_S0
VCC_NB	1D8V_S0	1D2V_S0
1D05V_S0	1D05V_S0	1D05V_S0
1D2V_S0 1D2V_PCIE	1D2V_S0	1D2V_S0

RC415

RC610

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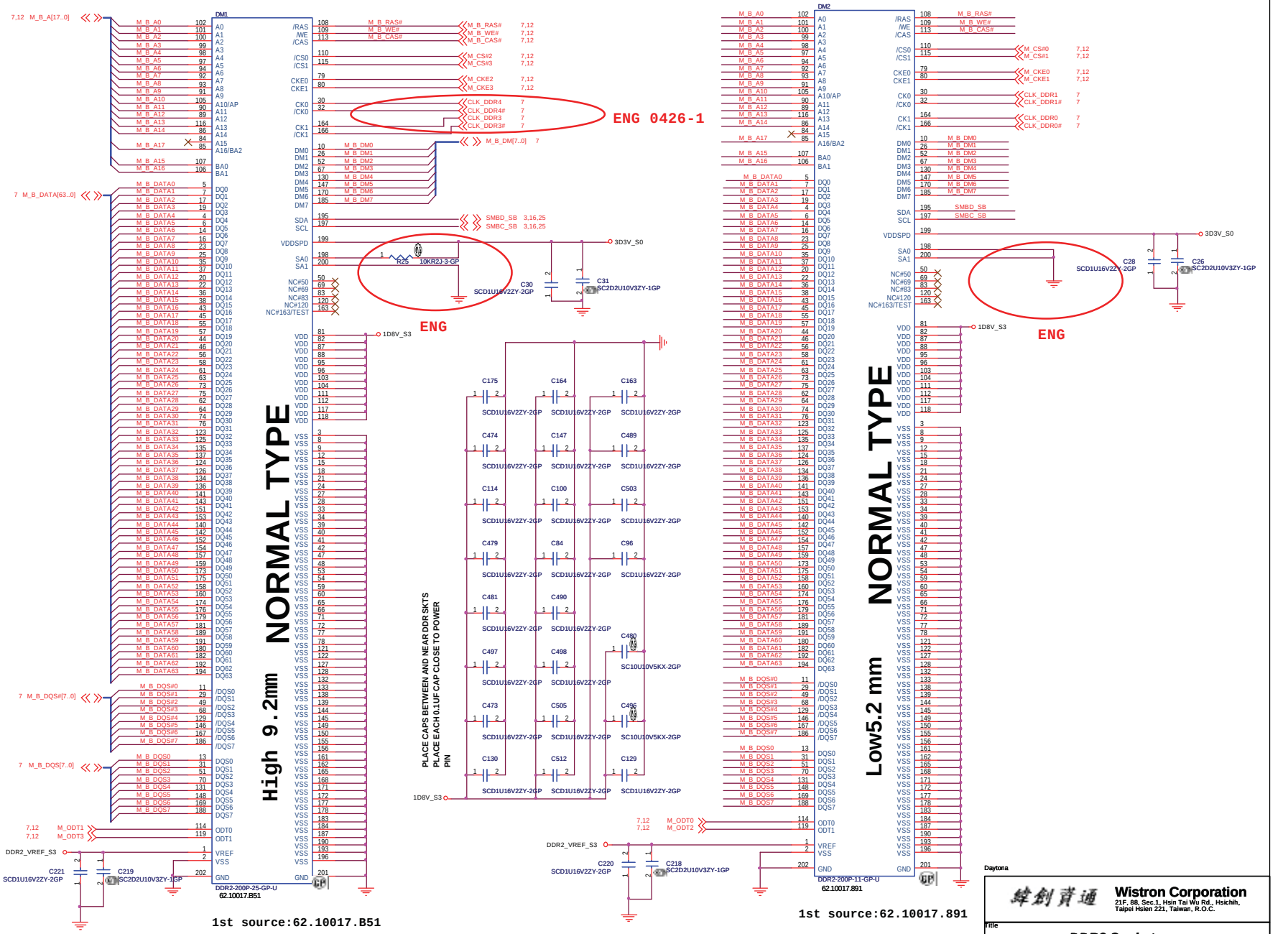
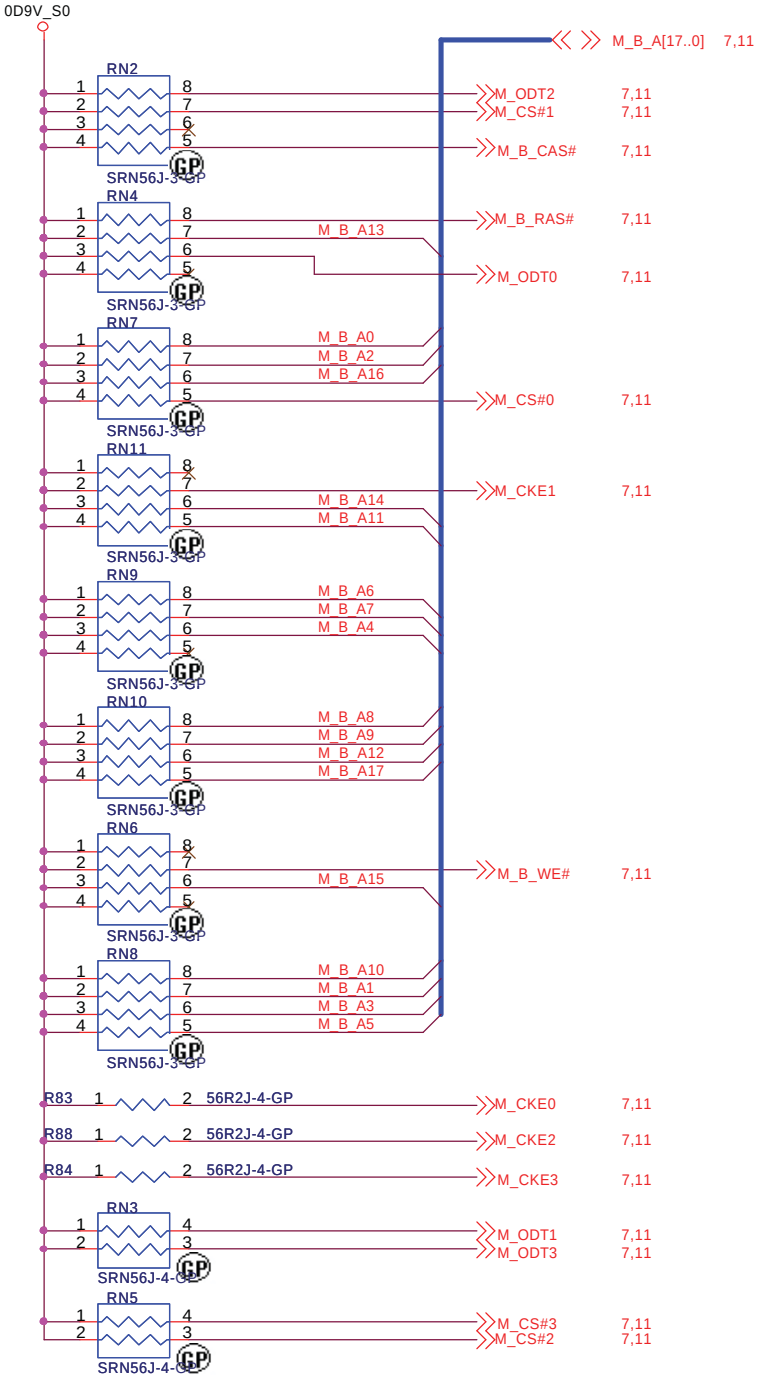
Title: RC415ME (5 of 5) Power

Size: A3 | Document Number: Daytona | Rev: -1

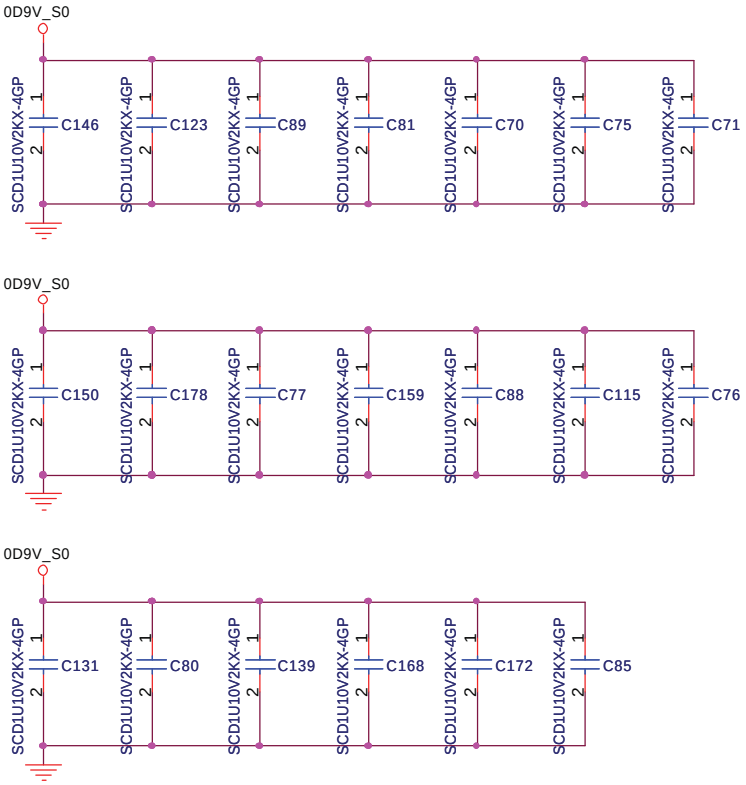
Date: Monday, June 12, 2006 | Sheet 10 of 48



PARALLEL TERMINATION



PLACE 1 CAP FOR EVERY 2 BITS TERMINATED TO 0D9V_S0



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Title: ***DDR2 Terminator Resistor***

Size	Document Number	Rev
A4	Daytona	-1

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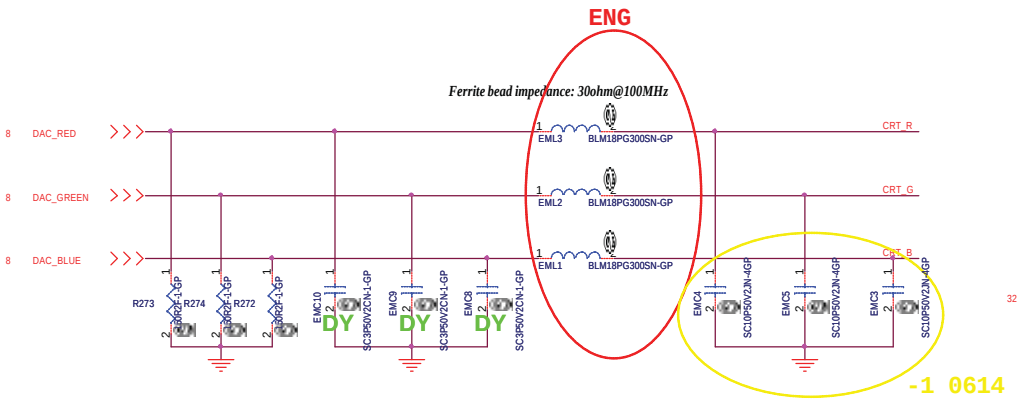
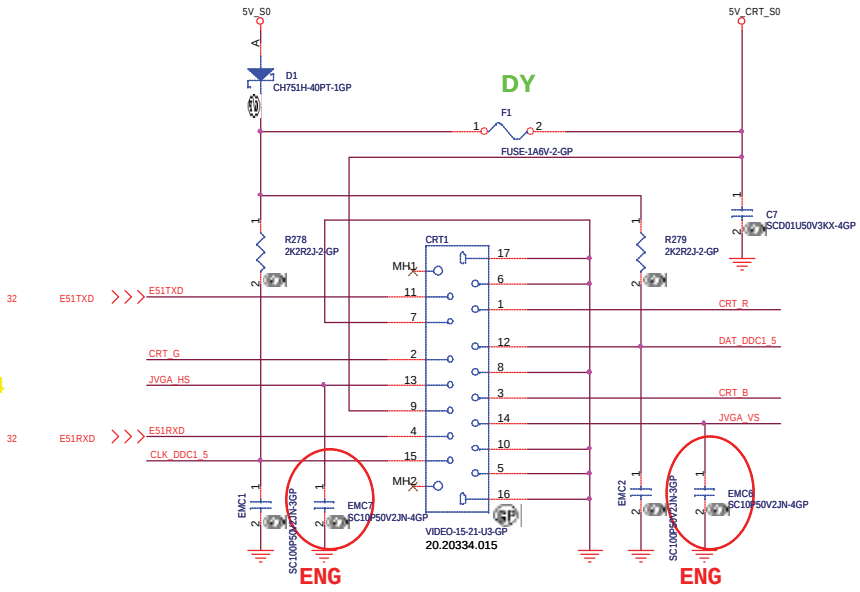
CRT I/F & CONNECTOR

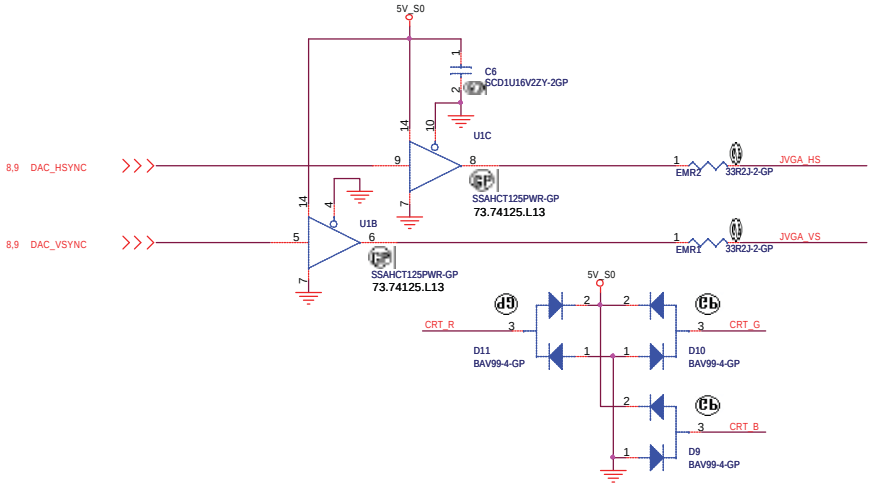




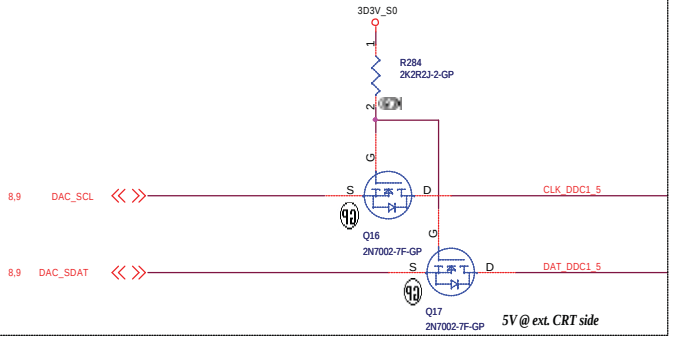
Layout Note:
** Must be a ground return path between this ground and the ground on the VGA connector.*
** 37.4_1% resistors must be placed at the same place as the RGB 75 Ohm pull-down resistors.*

Pi-filter & 75 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift



DAC_CLK & DATA level shift



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Title: CRT Connector

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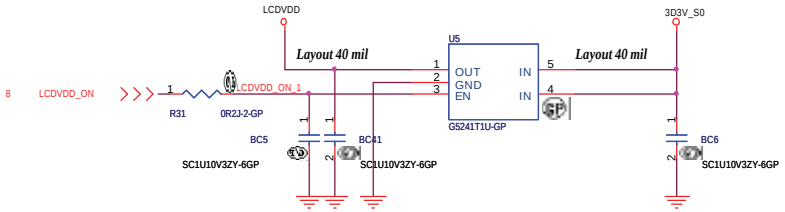
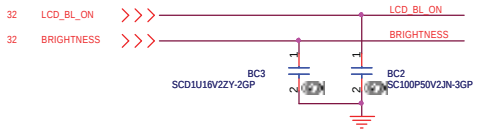
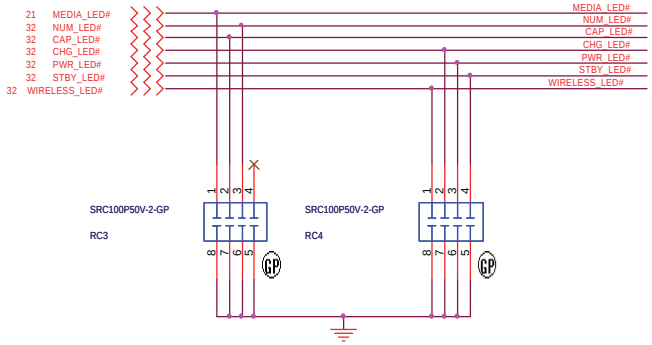
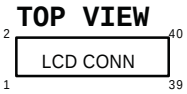
LCD & INVERTER INTERFACE

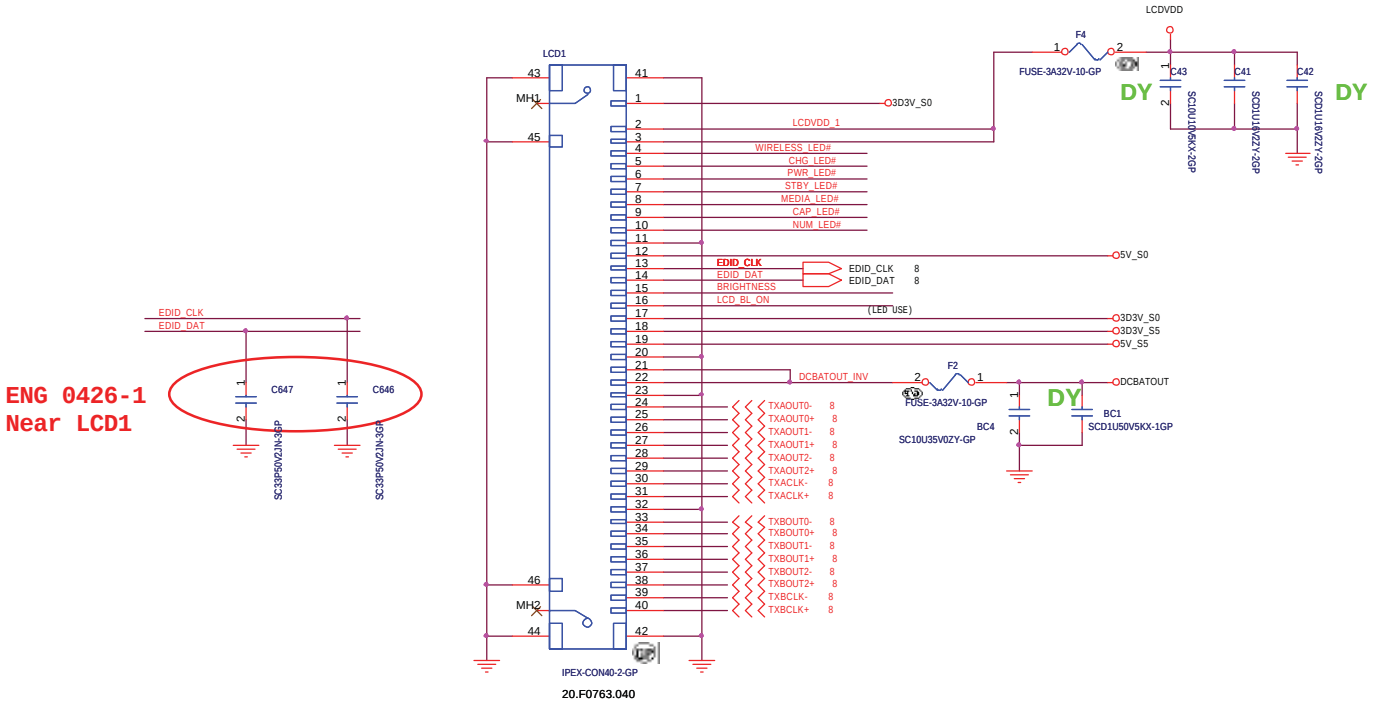






LCD CONN





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Title: LCD & Inverter Connector

Size	Document Number	Rev
A3	Daytona	-1

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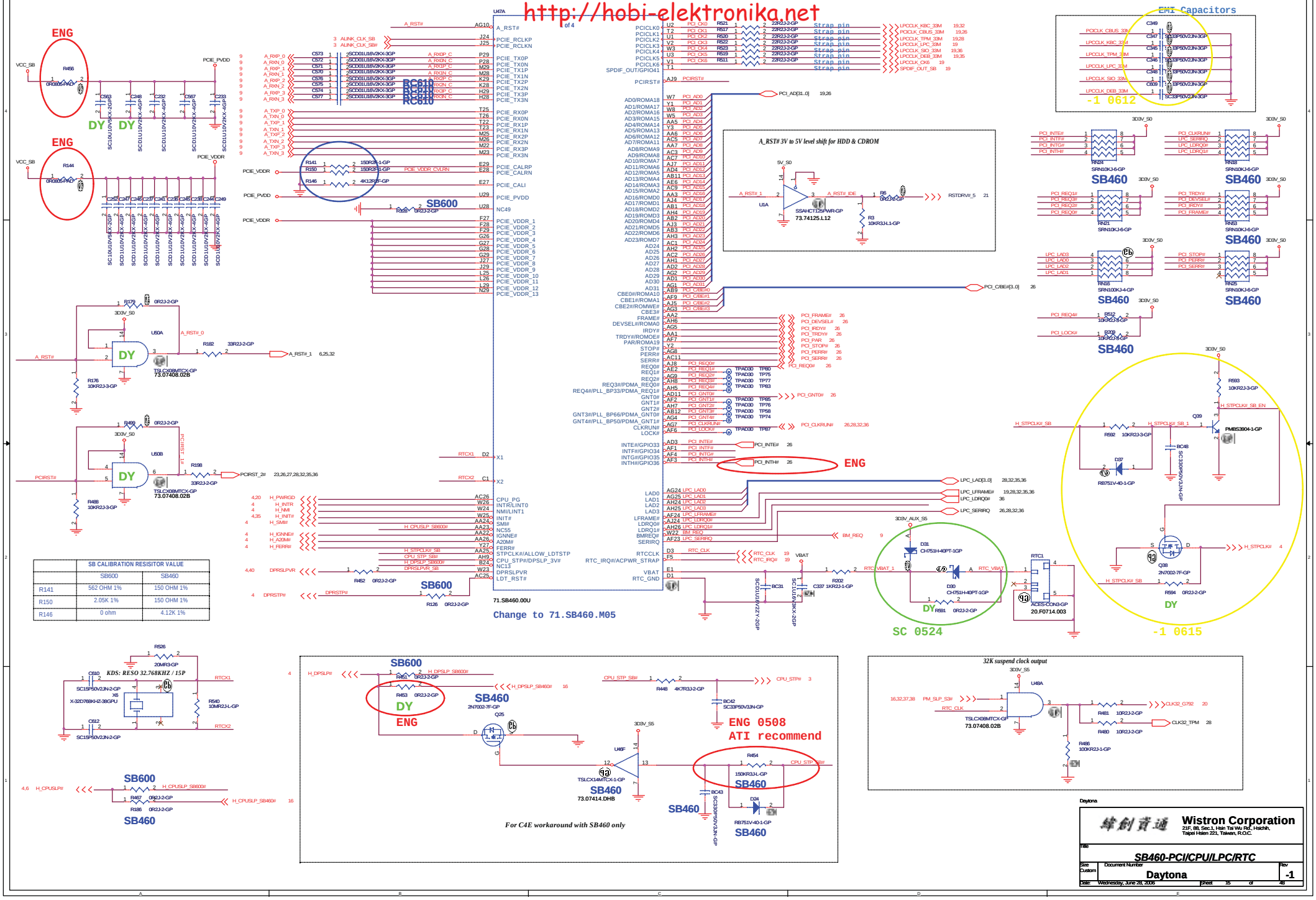

	SB CALIBRATION RESISITOR VALUE	
	SB600	SB460
R141	562 OHM 1%	150 OHM 1%
R150	2.05K 1%	150 OHM 1%
R146	0 ohm	4.12K 1%

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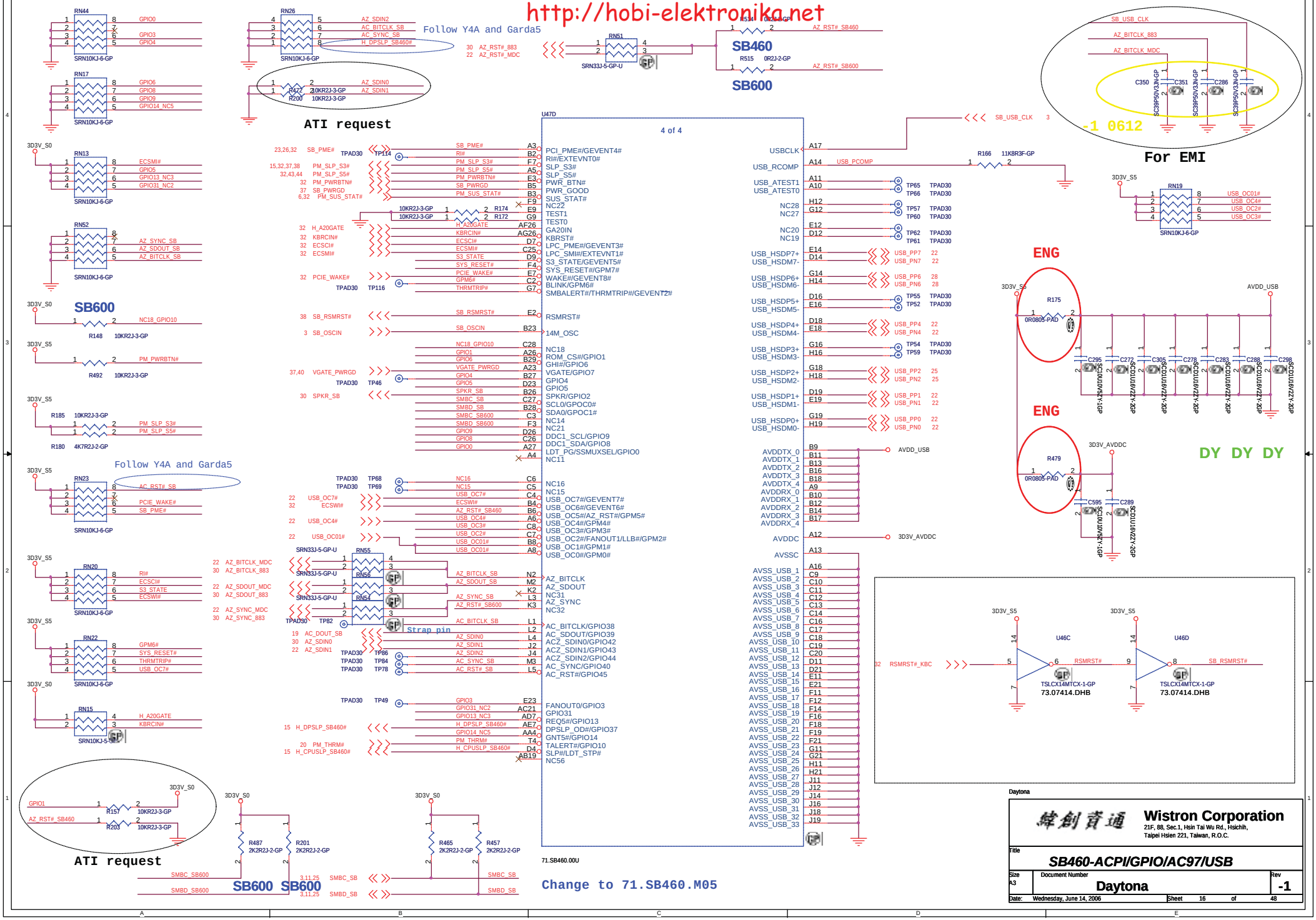
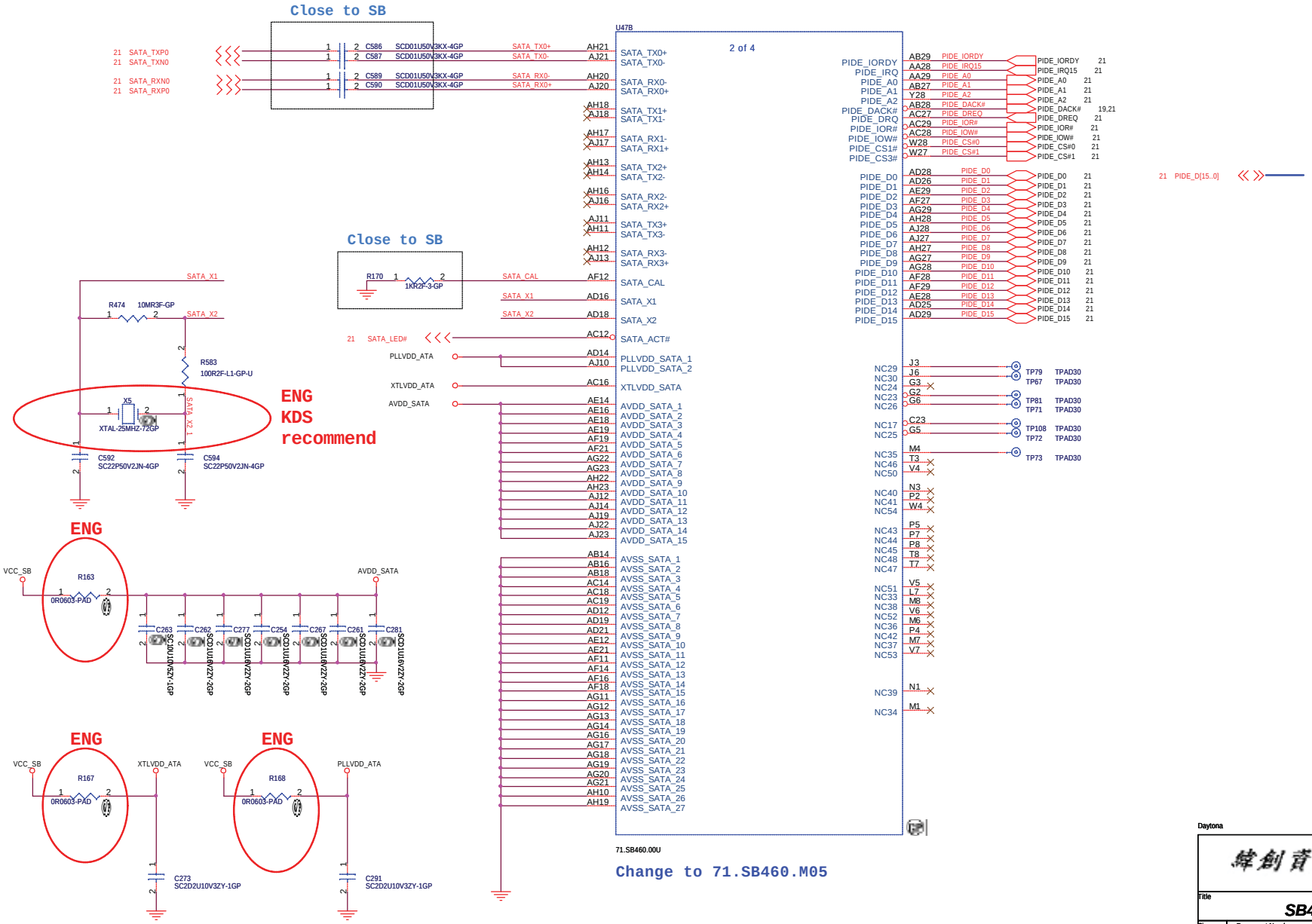
Title	SB460-PCI/CPU/LPC/RTC	
Size: Custom	Document Number: Daytona	Rev: -1
Date: Wednesday, June 28, 2006	Sheet 15 of 48	





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Title: ***SB460-SATA/IDE***

Size	Document Number	Rev
A3	Daytona	-1

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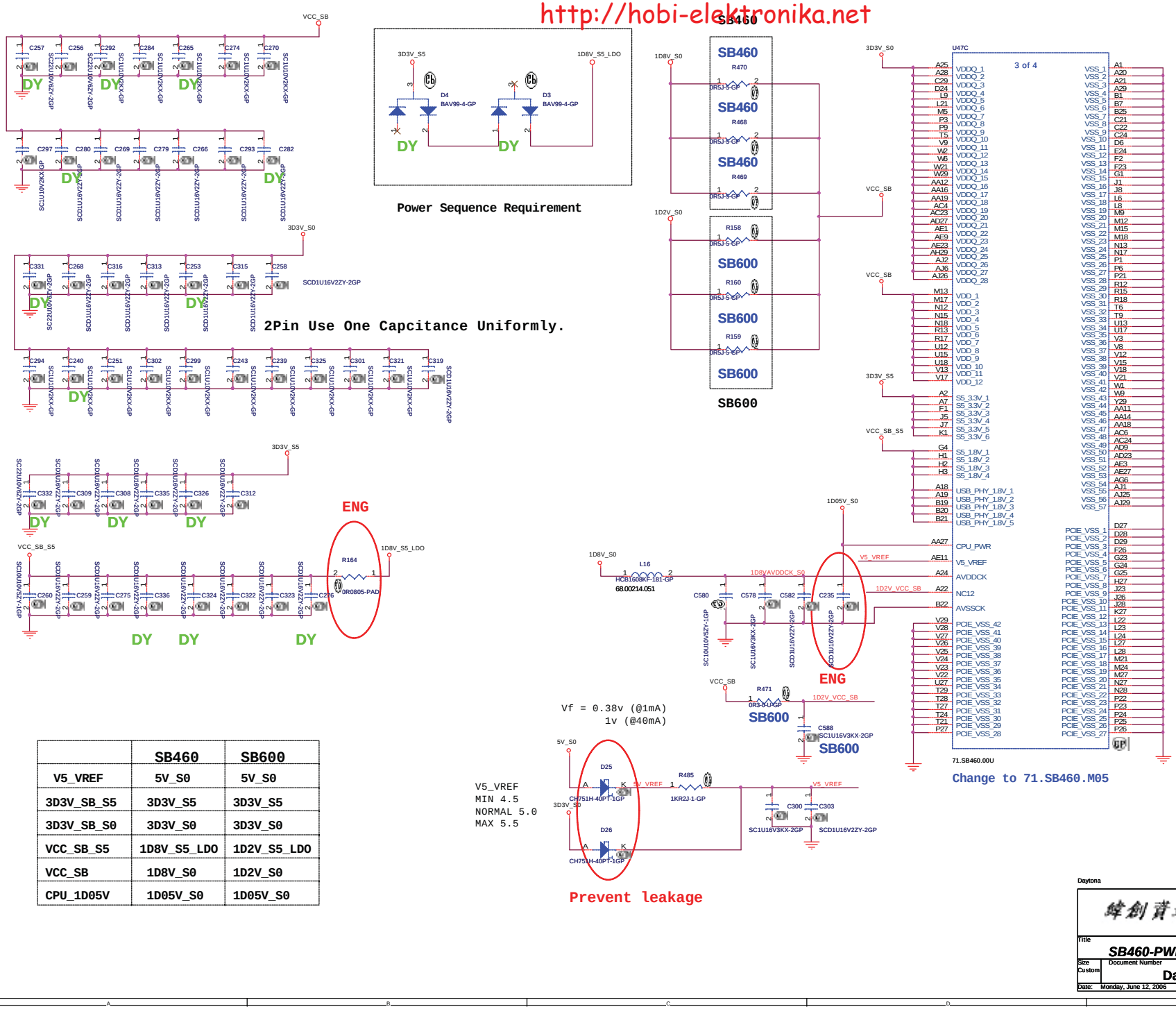

	SB460	SB600
V5_VREF	5V_S0	5V_S0
3D3V_SB_S5	3D3V_S5	3D3V_S5
3D3V_SB_S0	3D3V_S0	3D3V_S0
VCC_SB_S5	1D8V_S5_LDO	1D2V_S5_LDO
VCC_SB	1D8V_S0	1D2V_S0
CPU_1D05V	1D05V_S0	1D05V_S0

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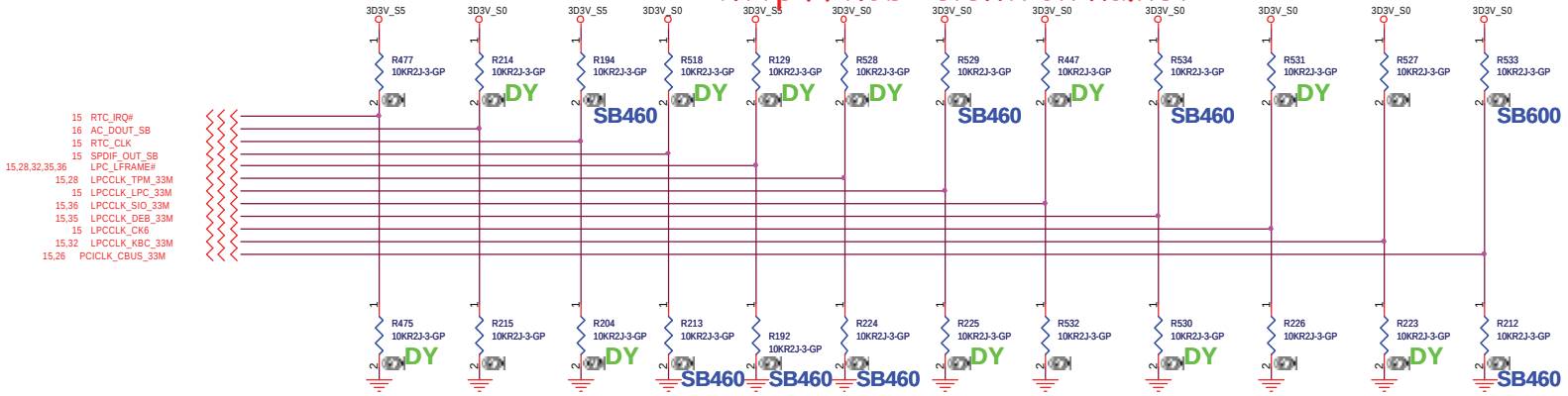
Title: SB460-PWR & DECOUPLING

Size: Custom | Document Number: Daytona | Rev: -1

Date: Monday, June 12, 2006 | Sheet 18 of 48



REQUIRED STRAPS

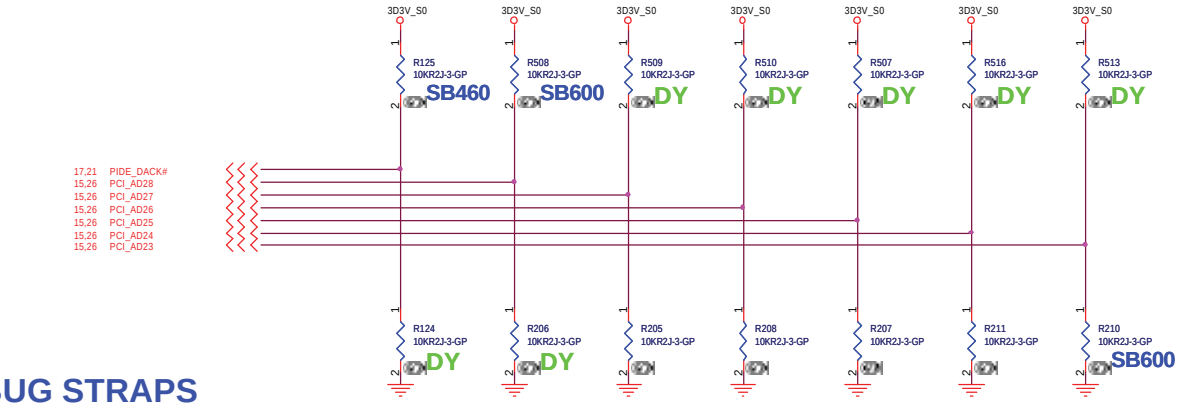
	AC_DOUT_SB	RTC_CLK	PCI_CLK4	PCI_CLK6	SB600 PCI_CLK0 / PCI_CLK1	SB460 PCI_CLK0 / PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. PLL48	CPU IF=K8	ROM TYPE: H, H = PCI ROM; H, L = SPI ROM; L, H = LPC ROM DEFAULT; L, L = FWH ROM	ROM TYPE: H, H = PCI ROM; H, L = LPC I ROM DEFAULT; L, H = LPC II ROM; L, L = FWH ROM. NOTE: FOR SB460, PCICLK[8:7] ARE CONNECTED TO SUBSTRATE BALLS PCICLK[1:0]
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ DEFAULT	CPU IF=P4 DEFAULT		

PCI_CLK0 LPCCLK_KBC_33M
PCI_CLK1 PCICLK_CBUS_33M
PCI_CLK2 LPCCLK_TPM_33M
PCI_CLK3 LPCCLK_LPC_33M
PCI_CLK4 LPCCLK_SIO_33M
PCI_CLK5 LPCCLK_DEB_33M
PCI_CLK6 LPCCLK_CK6

SB460 ONLY STRAPS

	ACPWRON	SPDIF_OUT	PCI_CLK2	PCI_CLK3	PCI_CLK5	LPC_LFRAME#
PULL HIGH	MANUAL PWR ON DEFAULT	SIO 24MHz	XTAL MODE NOT SUPPORTED	USB PHY POWERDOWN DISABLE DEFAULT	PCIE_CM_SET LOW DEFAULT	ENABLE THERMTRIP# DEFAULT
PULL LOW	AUTO PWR ON	SIO 48MHz DEFAULT	48MHZ OSC MODE DEFAULT	USB PHY POWERDOWN ENABLE	PCIE_CM_SET HIGH	DISABLE THERMTRIP#
	SB460 ONLY	SB460 ONLY	SB460 ONLY	SB460 ONLY	SB460 ONLY	SB460 ONLY

SB600 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



2.2K IF USED FOR SB600.
10K IF USED FOR SB460.

DEBUG STRAPS

	PIDE_DACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOTFAILTIMER DISABLED DEFAULT
PULL LOW	USE SHORT RESET	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED
	SB460 ONLY	SB600 ONLY					SB600 ONLY

NOTE: FOR SB460, PCI_AD23 IS RESERVED

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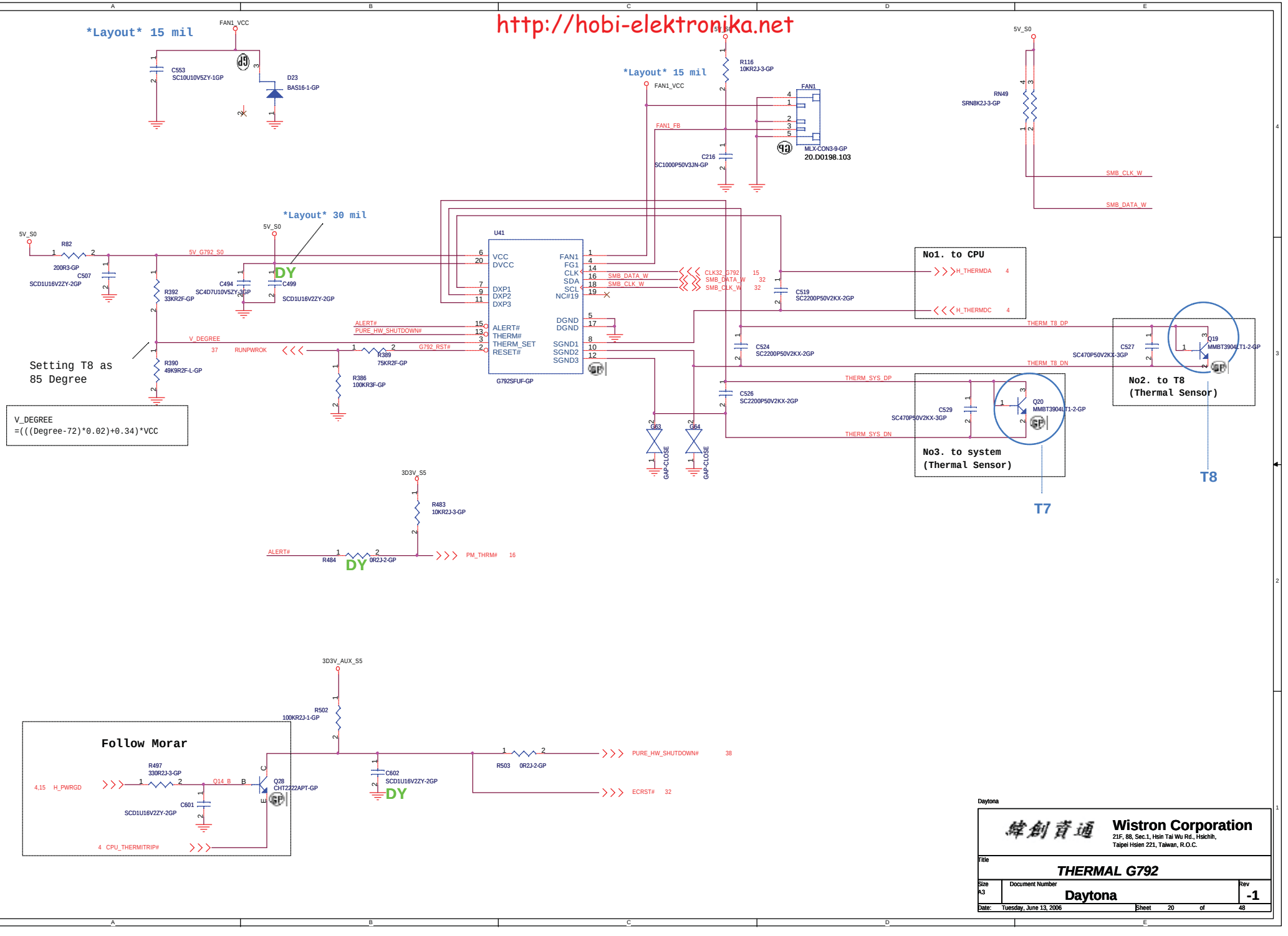
Title: SB450-STRAPPING(5 of 5)

Size: A3 | Document Number: Daytona | Rev: -1

Date: Tuesday, June 13, 2006 | Sheet 19 of 48


http://hobi-elektronika.net
Layout 15 mil
FAN1_VCC
C553
SC10U10V5ZY-1GP
D23
BAS16-1-GP
Layout 15 mil
FAN1_VCC
R116
10KR2J-3-GP
FAN1
MLX-CON3-9-GP
20.D0198.103
FAN1_FB
C216
SC1000P50V3JN-GP
5V_S0
RN49
SRN8K2J-3-GP
SMB_CLK_W
SMB_DATA_W
Layout 30 mil
5V_S0
R82
200R3-GP
C507
SCD1U16V2ZY-2GP
5V_G792_S0
R392
33KR2F-GP
C494
SC4D7U10V5ZY-3GP
C499
SCD1U16V2ZY-2GP
DY
U41
VCC
DVCC
DXP1
DXP2
DXP3
ALERT#
THERM#
THERM_SET
RESET#
FAN1
FG1
CLK
SDA
SCL
NC#19
DGND
DGND
SGND1
SGND2
SGND3
G792SFUF-GP
SMB_DATA_W
SMB_CLK_W
CLK32_G792
C519
SC2200P50V2KX-2GP
No1. to CPU
H_THERMDA
H_THERMDC
ALERT#
PURE_HW_SHUTDOWN#
V_DEGREE
RUNPWROK
G792_RST#
R389
75KR2F-GP
R386
100KR3F-GP
R390
49K9R2F-L-GP
Setting T8 as
85 Degree
V_DEGREE
=(((Degree-72)*0.02)+0.34)*VCC
THERM_T8_DP
THERM_T8_DN
C524
SC2200P50V2KX-2GP
C527
SC470P50V2KX-3GP
Q19
MMBT3904LT1-2-GP
No2. to T8
(Thermal Sensor)
T8
THERM_SYS_DP
THERM_SYS_DN
C526
SC2200P50V2KX-2GP
C529
SC470P50V2KX-3GP
Q20
MMBT3904LT1-2-GP
No3. to system
(Thermal Sensor)
T7
G63
G64
GAP-CLOSE
3D3V_S5
R483
10KR2J-3-GP
ALERT#
R484
0R2J-2-GP
PM_THRM#
16
3D3V_AUX_S5
R502
100KR2J-1-GP
Follow Morar
R497
330R2J-3-GP
4,15 H_PWRGD
Q14_B
Q28
CHT2222APT-GP
C601
SCD1U16V2ZY-2GP
4 CPU_THERMITRIP#
C602
SCD1U16V2ZY-2GP
R503
0R2J-2-GP
PURE_HW_SHUTDOWN#
38
ECRST#
32
Daytona
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title
THERMAL G792
Size
A3
Document Number
Daytona
Rev
-1
Date: Tuesday, June 13, 2006
Sheet 20 of 48

SATA HDD Connector

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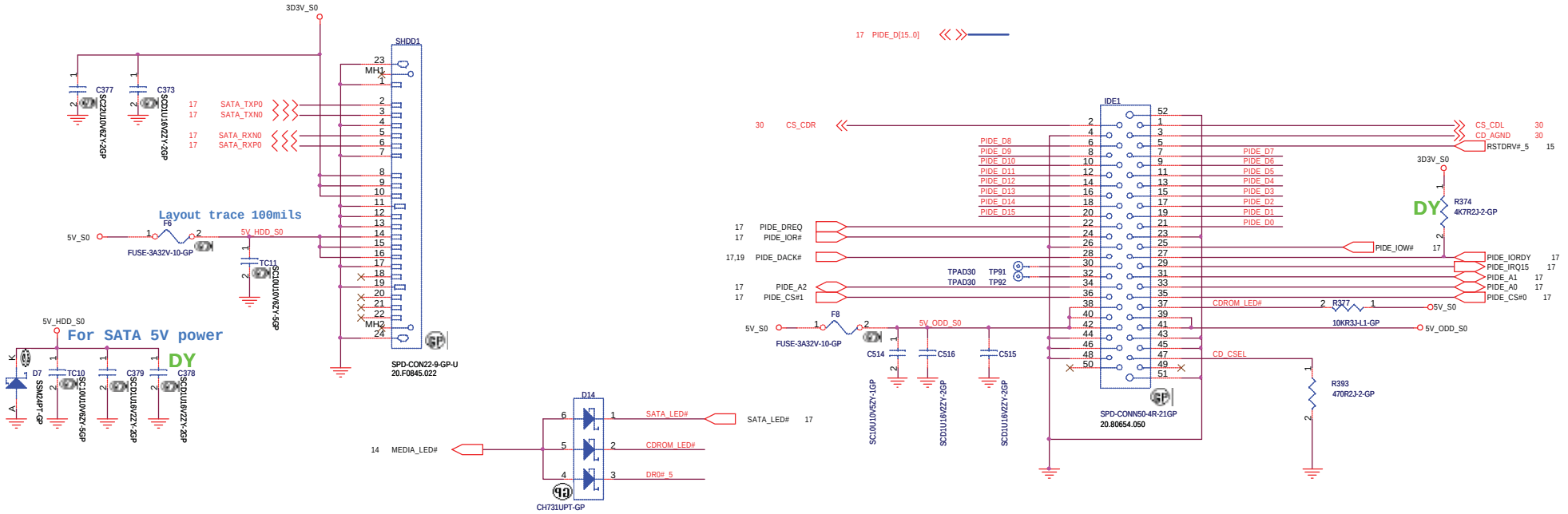
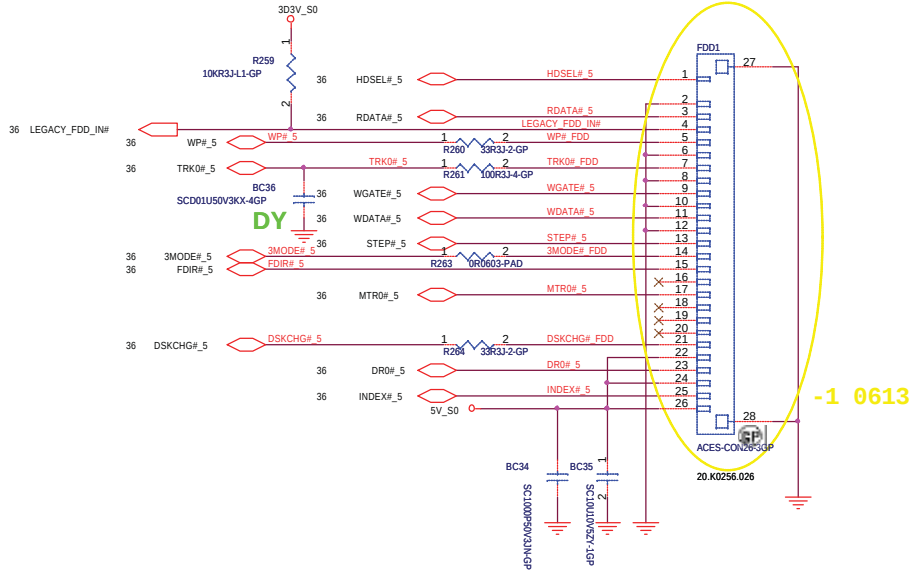
CD-ROM CONN



FDD Connector

ENG FDD PIN DEFIND SWAP



緯創資通 Wistron Corporation
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Title: HDD / ODD / FDD CONN

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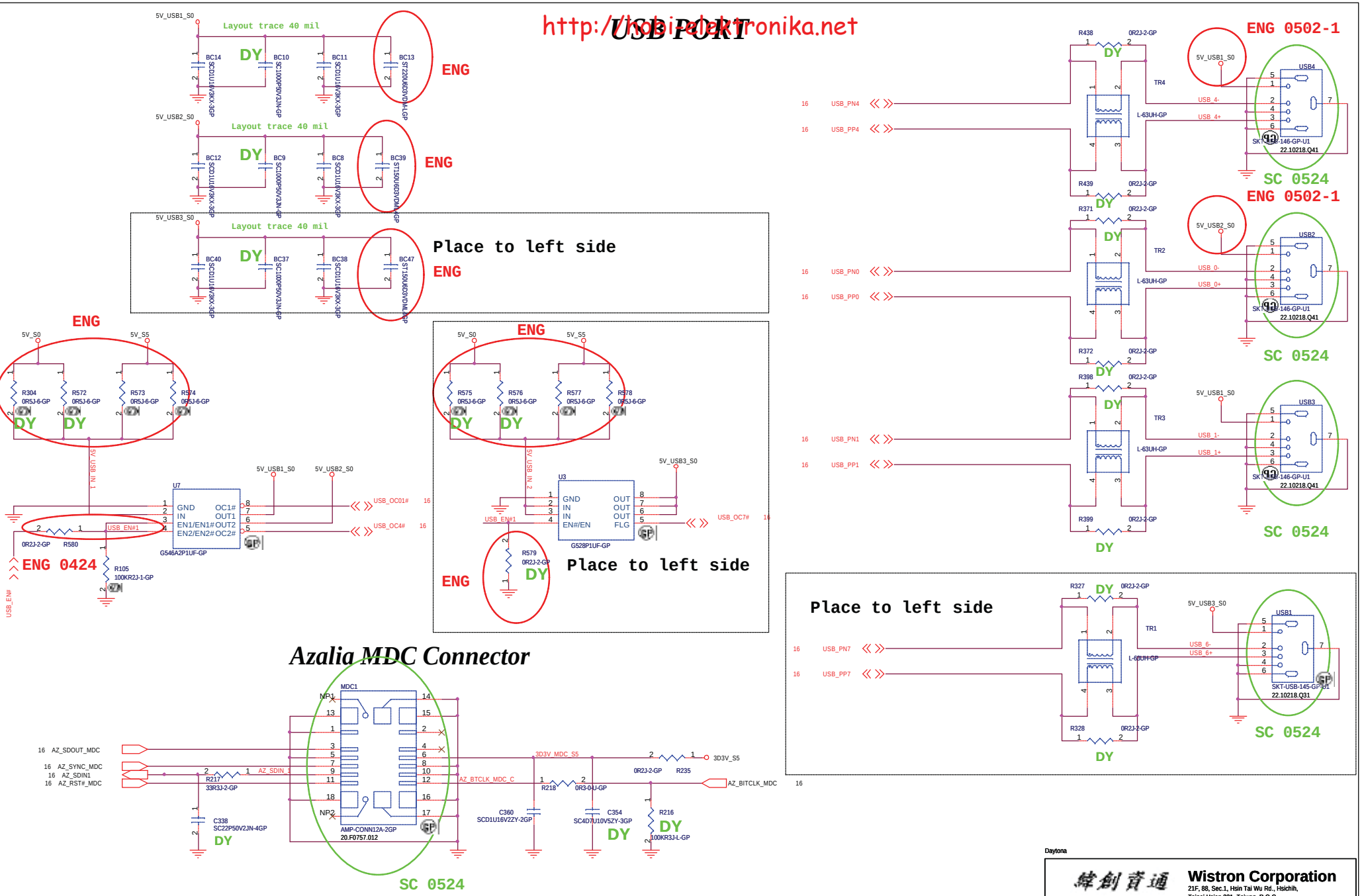
USB PORT



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Taipei Hsien 221, Taiwan, R.O.C.

Title: USB and MDC Connector

Size	Document Number	Rev
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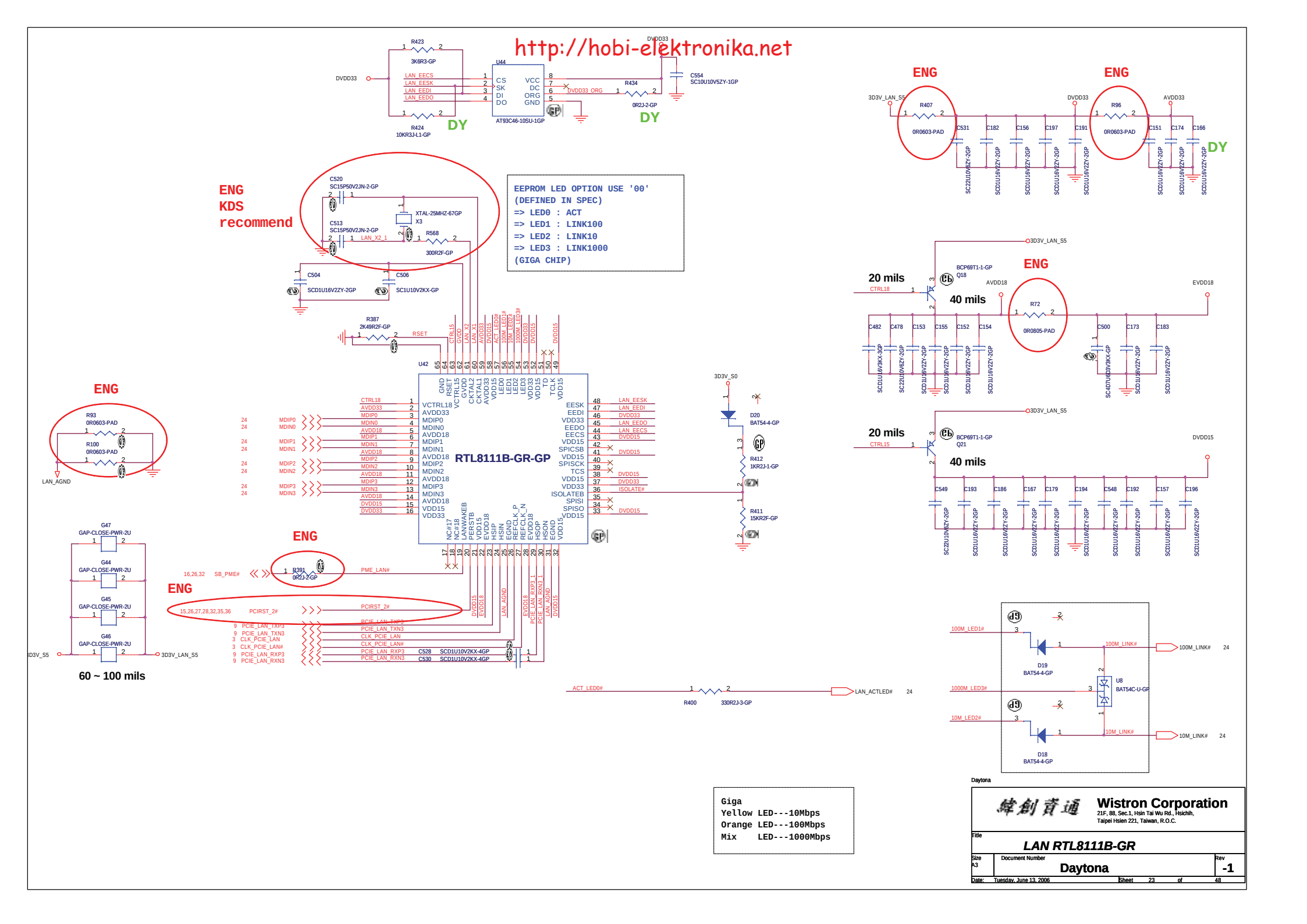
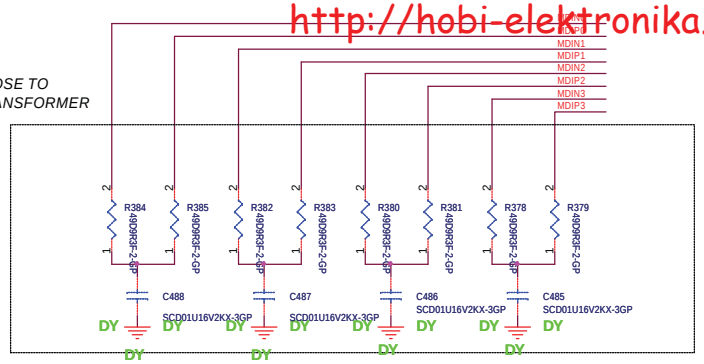
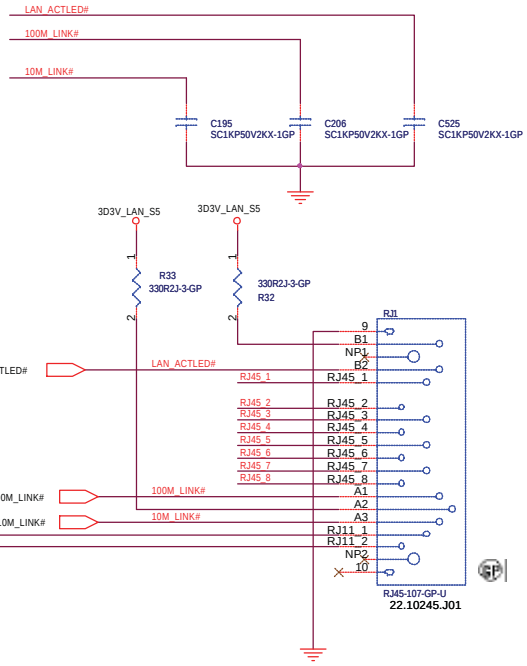


LAN Connector

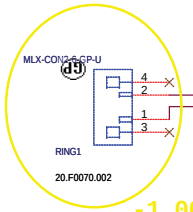
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

CLOSE TO TRANSFORMER

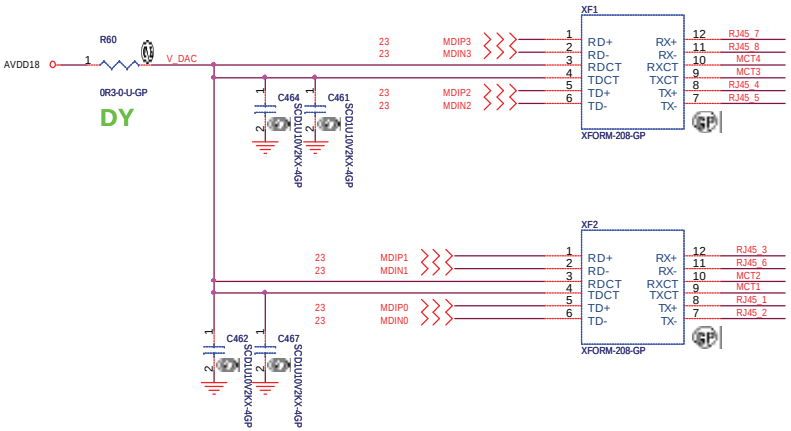




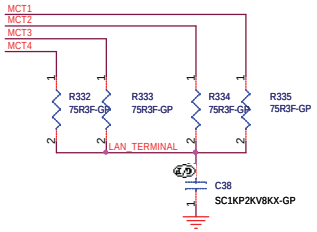
10/100/1000Mbps Lan Transformer



-1 0615



DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers



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Title	LAN Connector	
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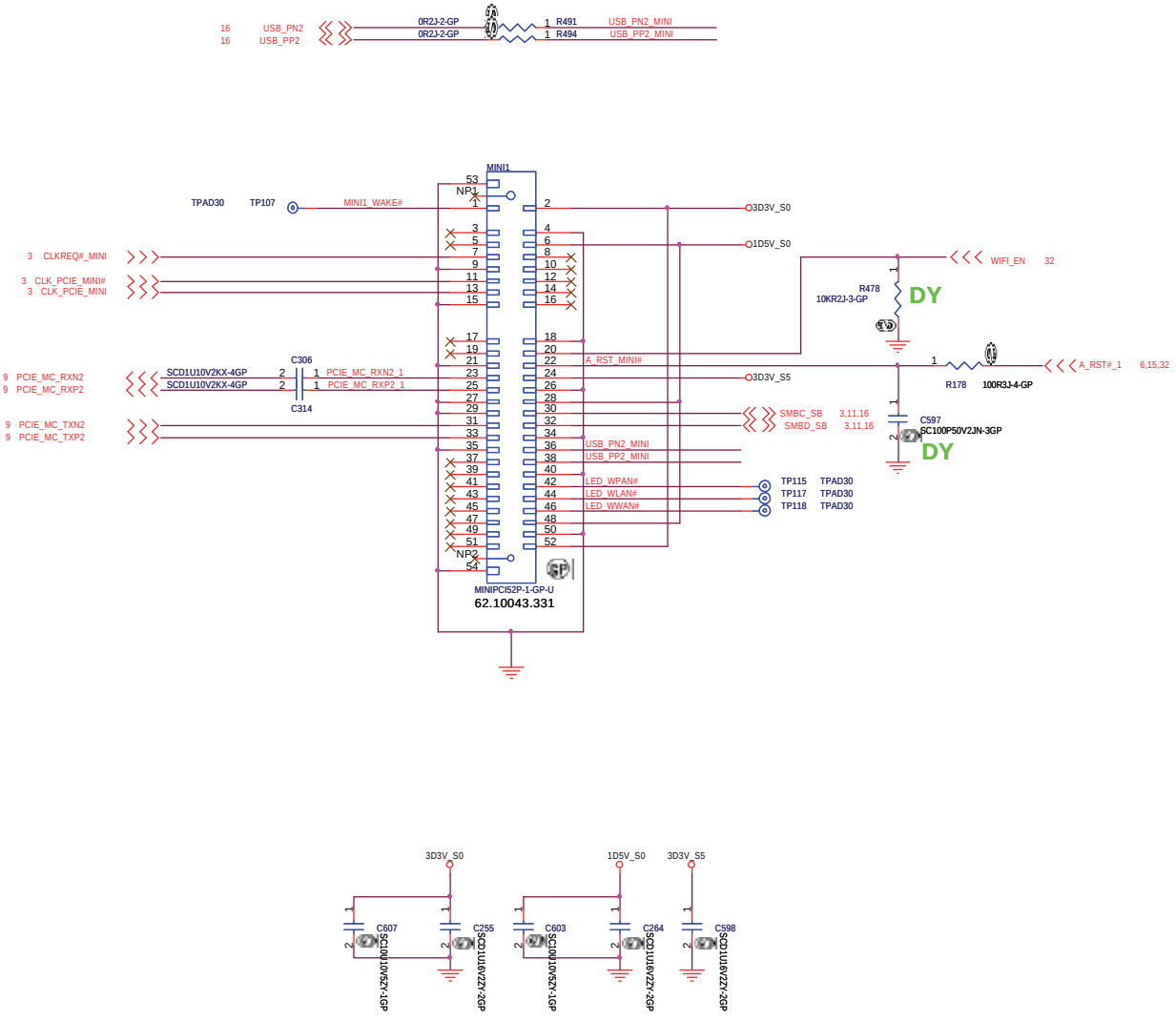
Mini Card Connector



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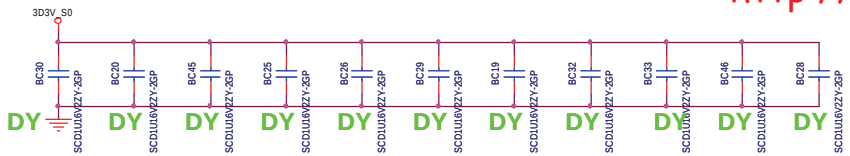
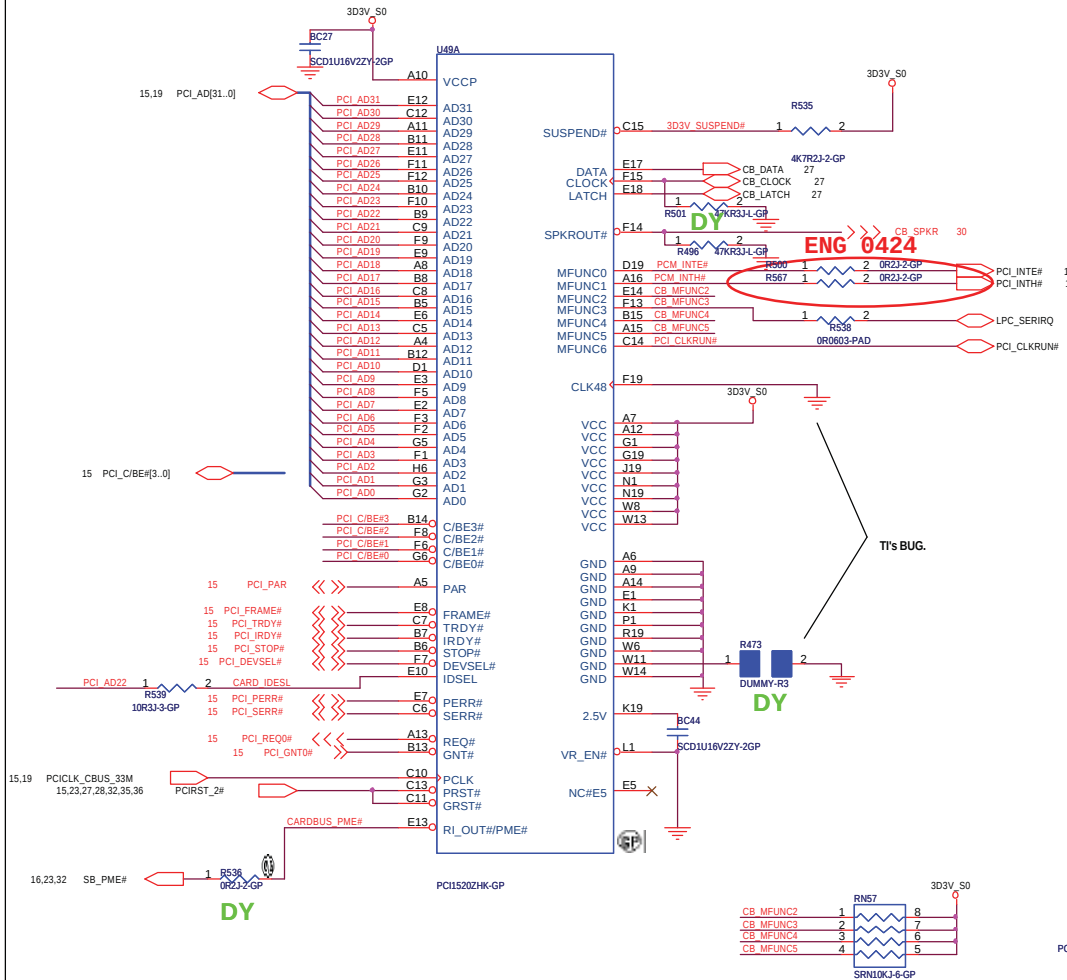
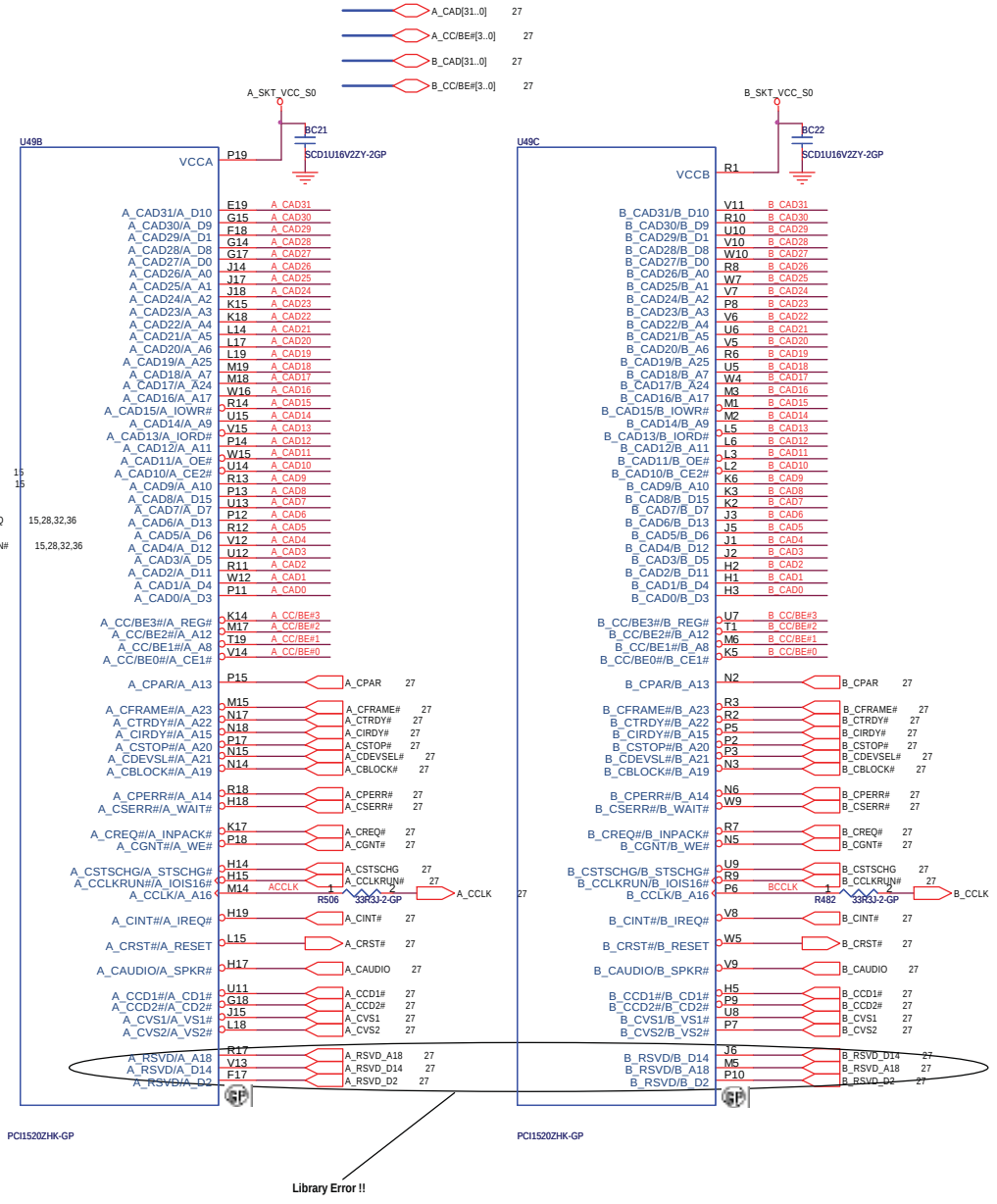
Title	***MINI CARD***	
Size A3	Document Number **Daytona**	Rev **-1**
Date: Tuesday, June 13, 2006	Sheet 25 of 48	







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Title: **CARDBUS TI1520**

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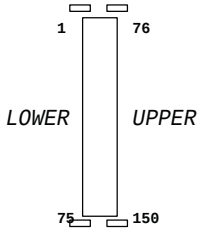
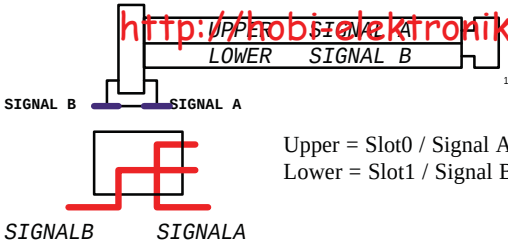
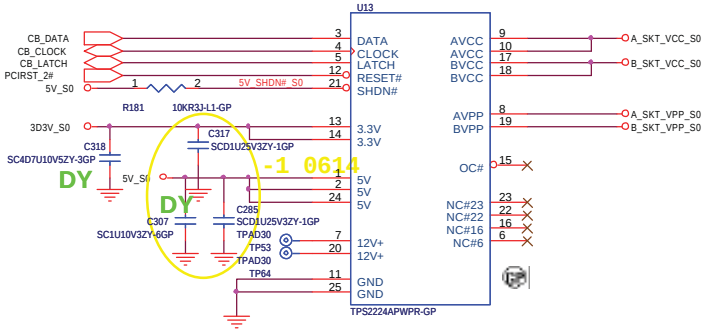
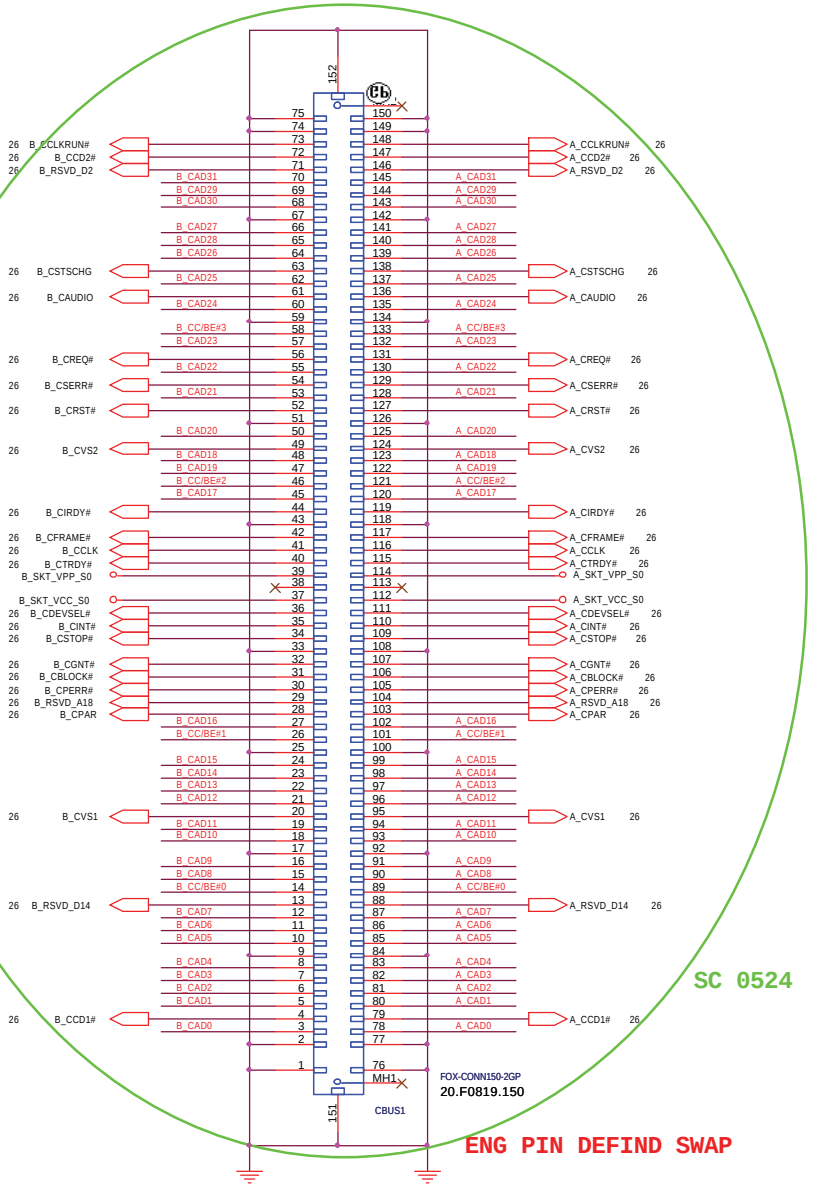
Date: Wednesday, June 28, 2006 Sheet 26 of 48





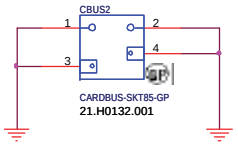
Upper = Slot0 / Signal A = Conn B
Lower = Slot1 / Signal B = Conn A

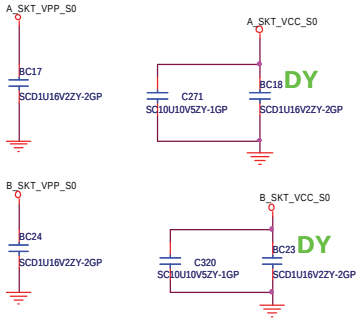




SC 0524

ENG PIN DEFIND SWAP





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Title: CARDBUS CONN / PWR SW

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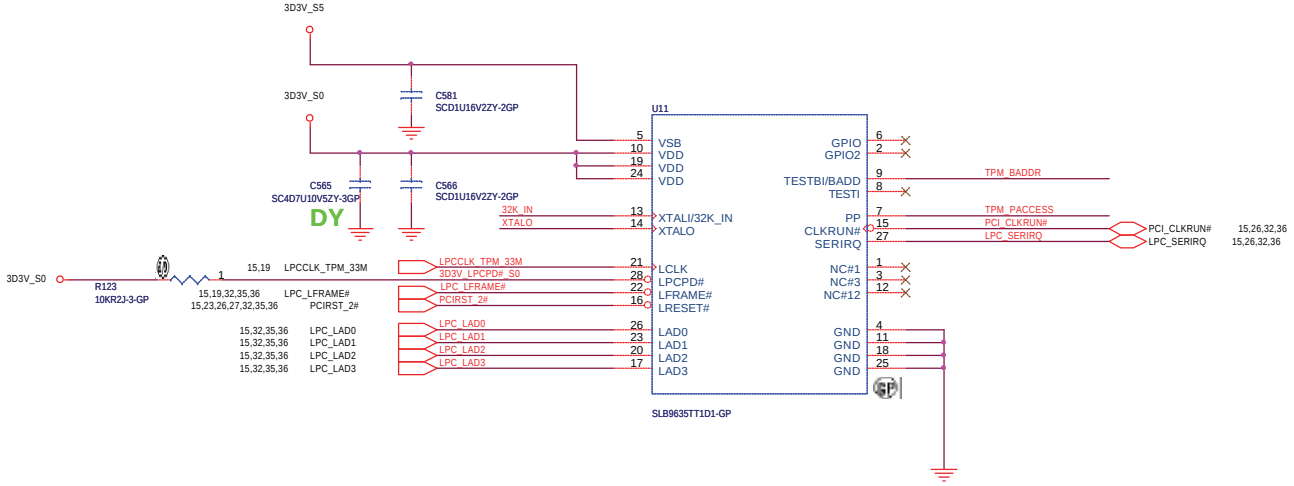
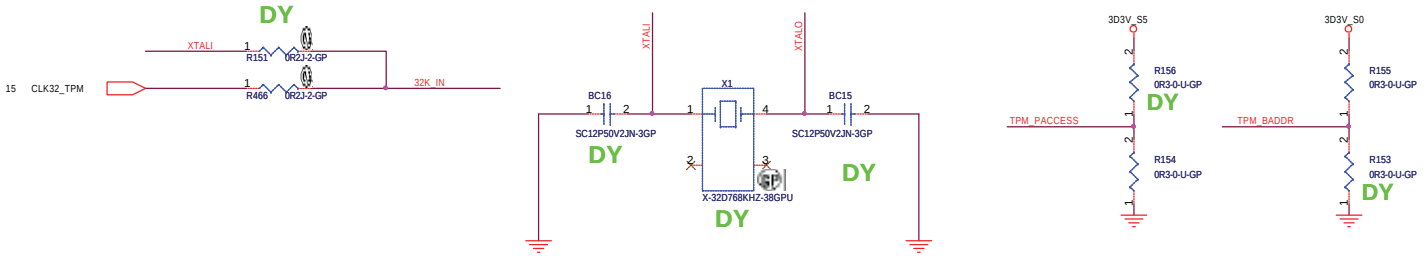
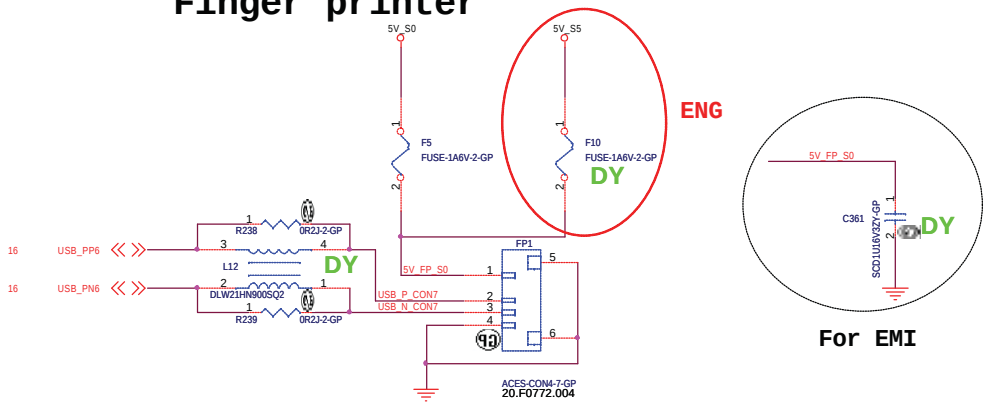
TPM 1.2





Finger printer



For EMI

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Title	***TPM 1.2 / FP***	
Size A3	Document Number **Daytona**	Rev **-1**
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SERIAL PORT

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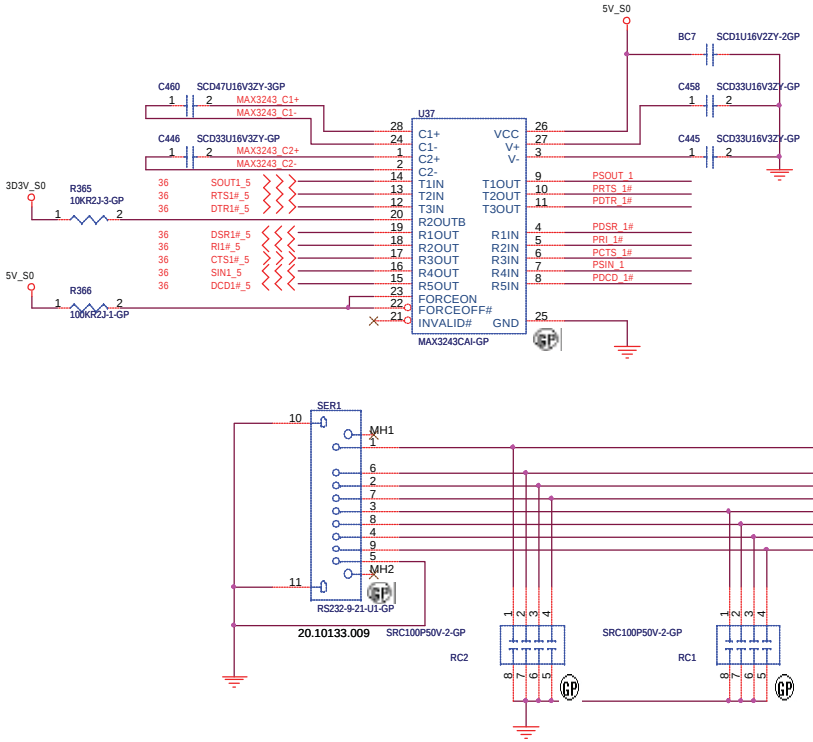
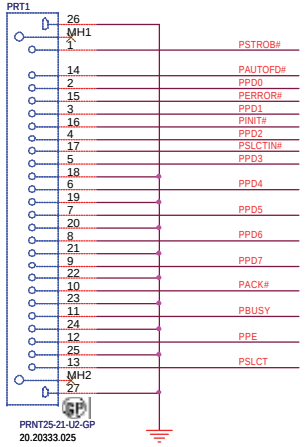
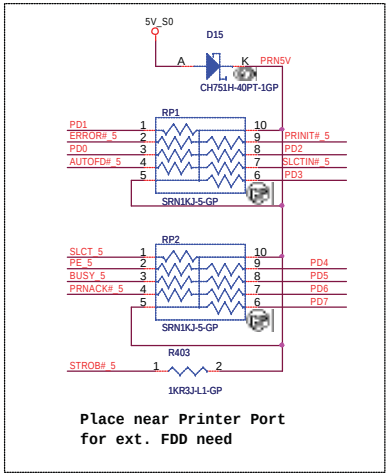
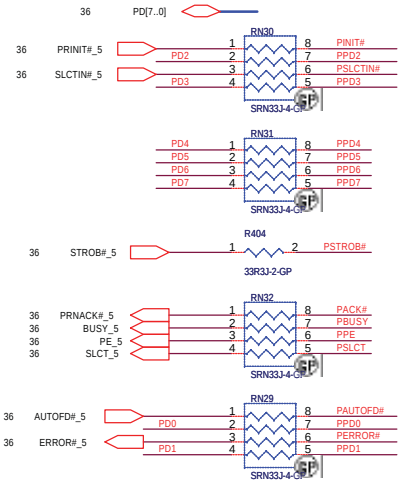
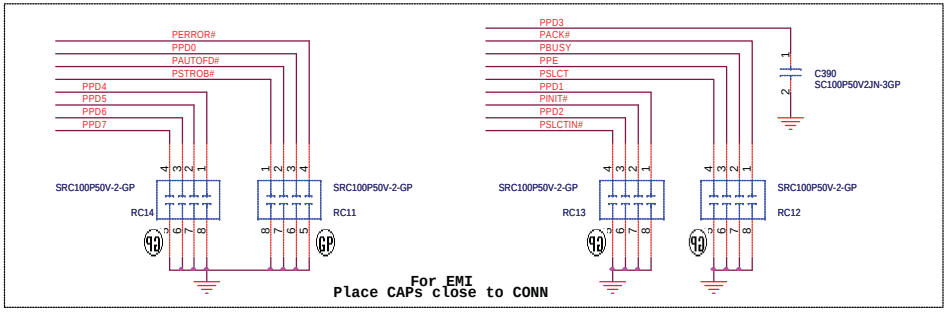


PRINTER PORT









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Title: ***Parallel Port / Serial Port***

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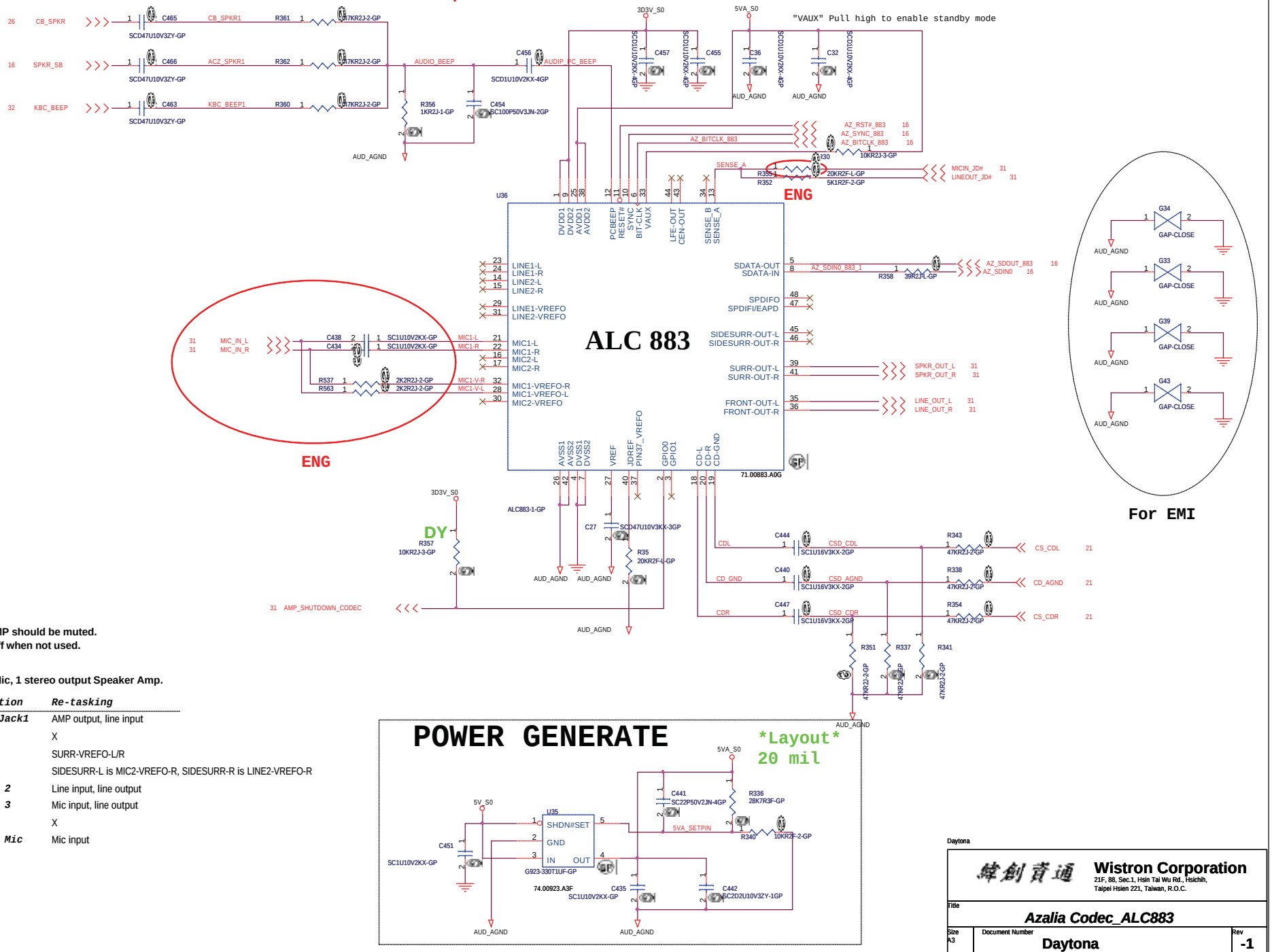

1) When GPIO0 is assered, AMP should be muted.
2) SPDIFO should be turned off when not used.

Configuation:
(3 External Jacks, 1 internal Mic, 1 stereo output Speaker Amp.

Pin	*Symbol*	*Location*	*Re-tasking*
35/36	***FRONT***	***AMP,Jack1***	AMP output, line input
39/41	***SURR***	***X***	X
43/44	***CEN/LEFT***	***X***	SURR-VREFO-L/R
45/46	***SIDESURR***	***X***	SIDESURR-L is MIC2-VREFO-R, SIDESURR-R is LINE2-VREFO-R
23/24	***LINE1***	***Jack 2***	Line input, line output
21/22	***MIC1***	***Jack 3***	Mic input, line output
14/15	***LINE2***	***X***	X
16/17	***MIC2***	***Int. Mic***	Mic input

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Title: ***Azalia Codec_ALC883***

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AUDIO OP AMPLIFIER

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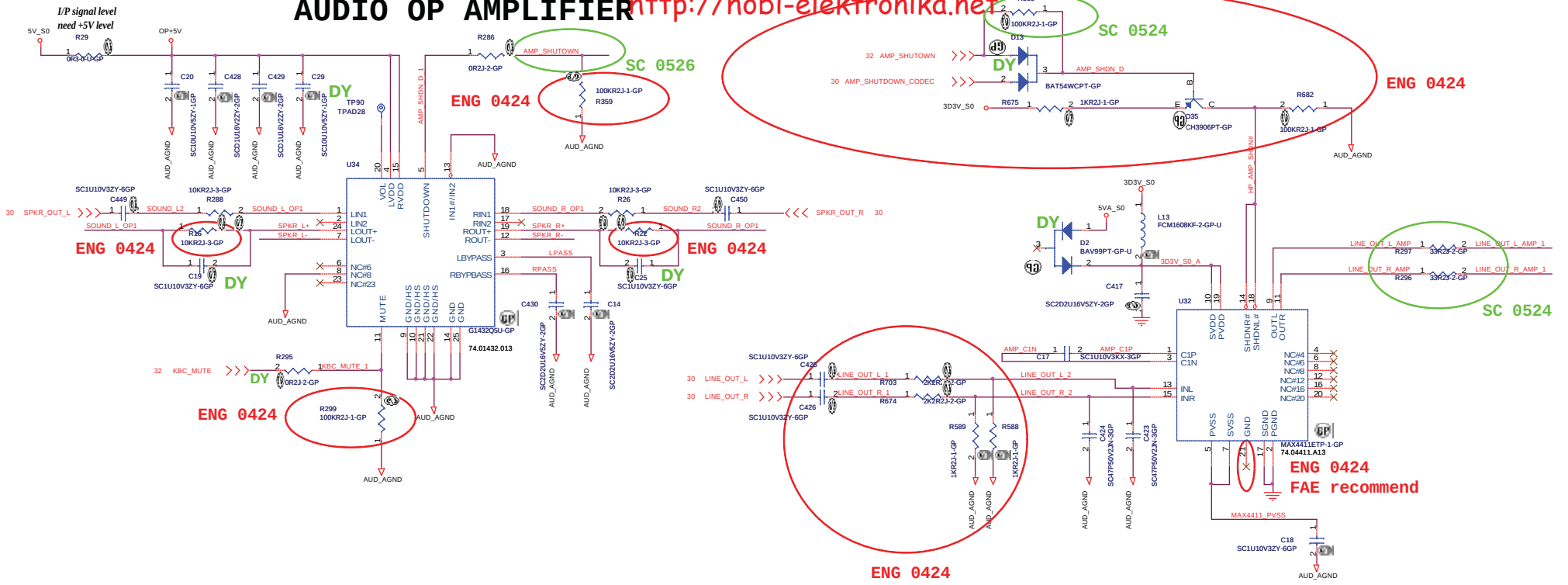
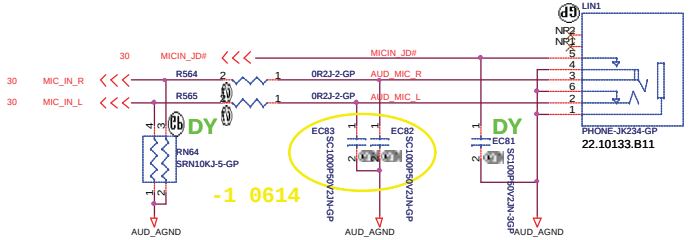


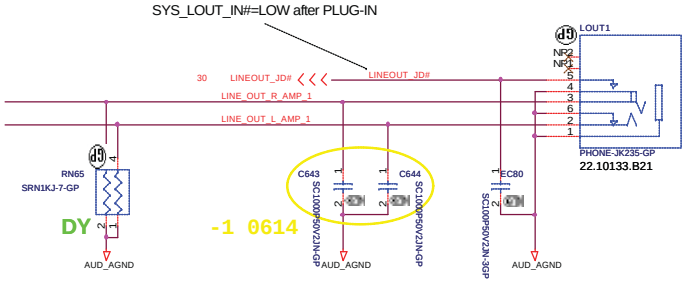
MIC IN

ENG Modify

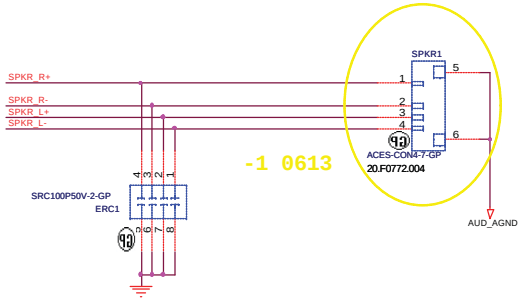


LINE OUT

ENG Modify



Internal Speaker



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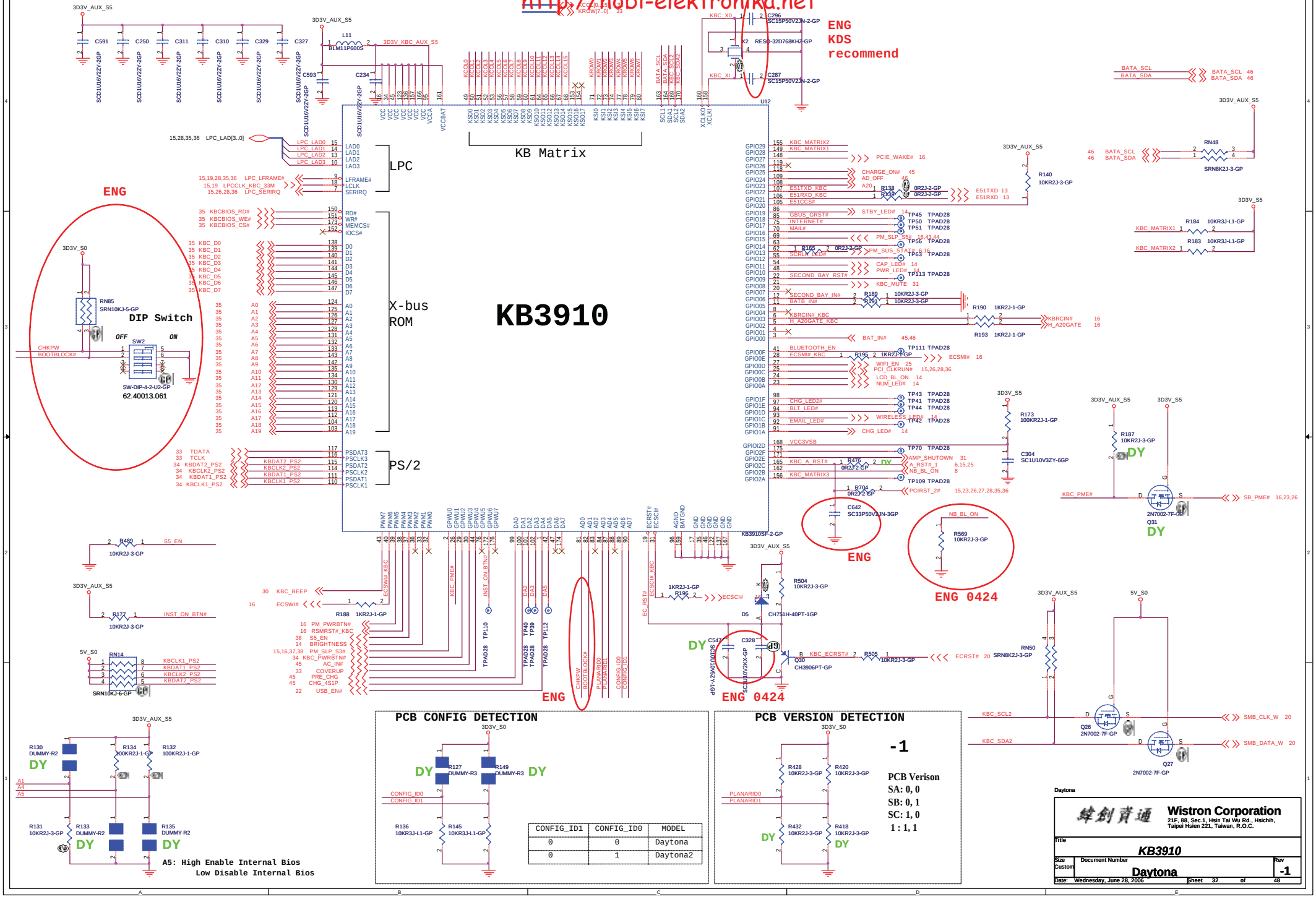
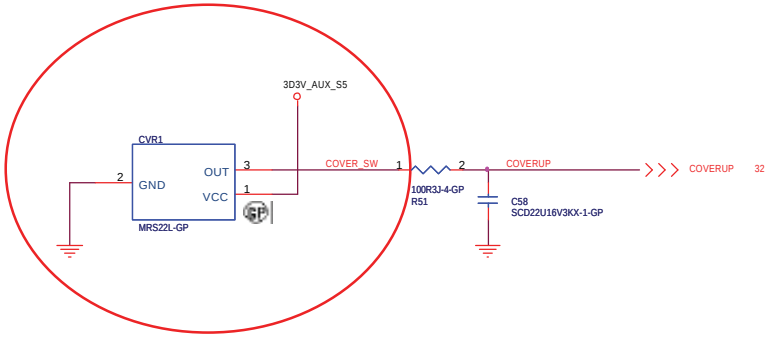
Taipei Hsien 221, Taiwan, R.O.C.

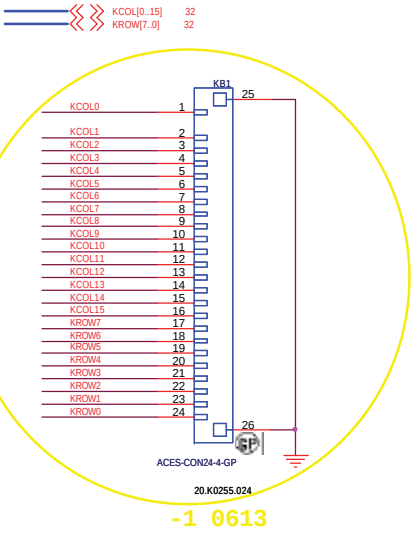
Title	Audio AMP and Jack	
Size: Custom	Document Number: Daytona	Rev: -1
Date: Tuesday, July 25, 2006	Sheet 31 of 48	

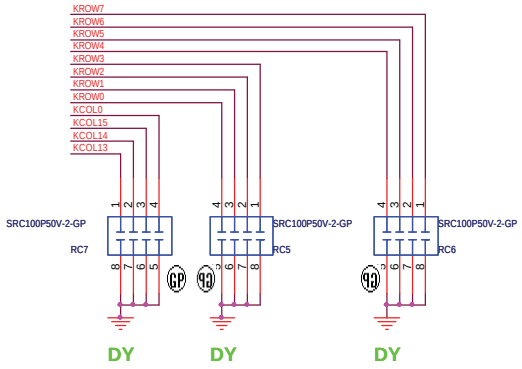


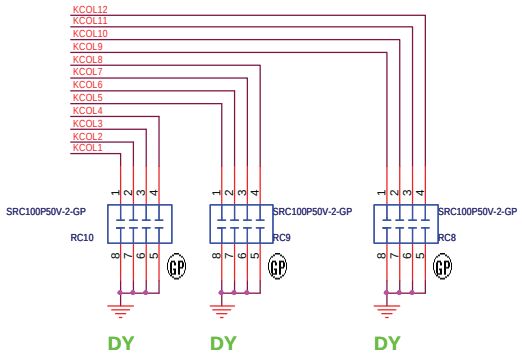
Internal KeyBoard Connector

ENG 0502

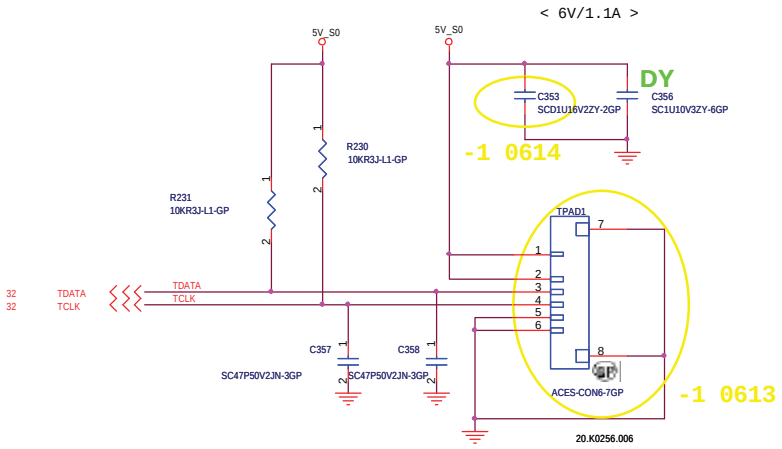








TouchPad Connector



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Title: KB/TOUCH_PAD

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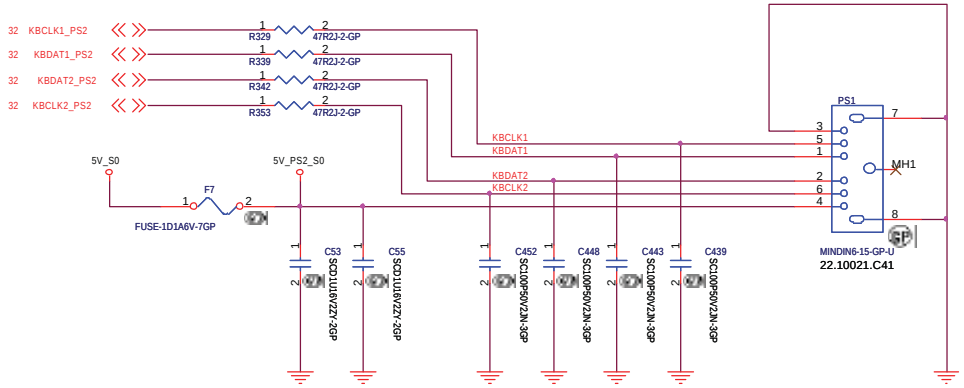
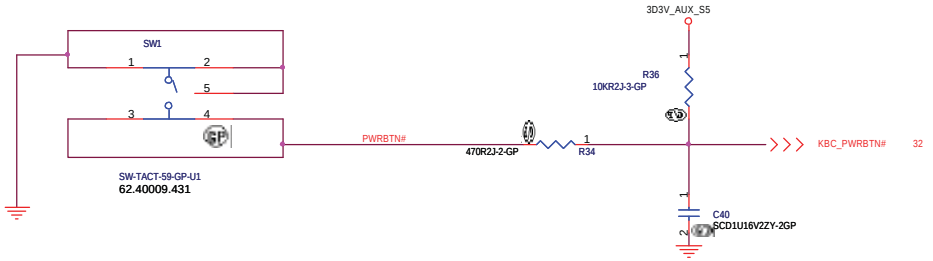
PS/2 CONN



POWER BUTTON



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Title	PS2/LAUCH CONN	
Size: A3	Document Number: Daytona	Rev: -1
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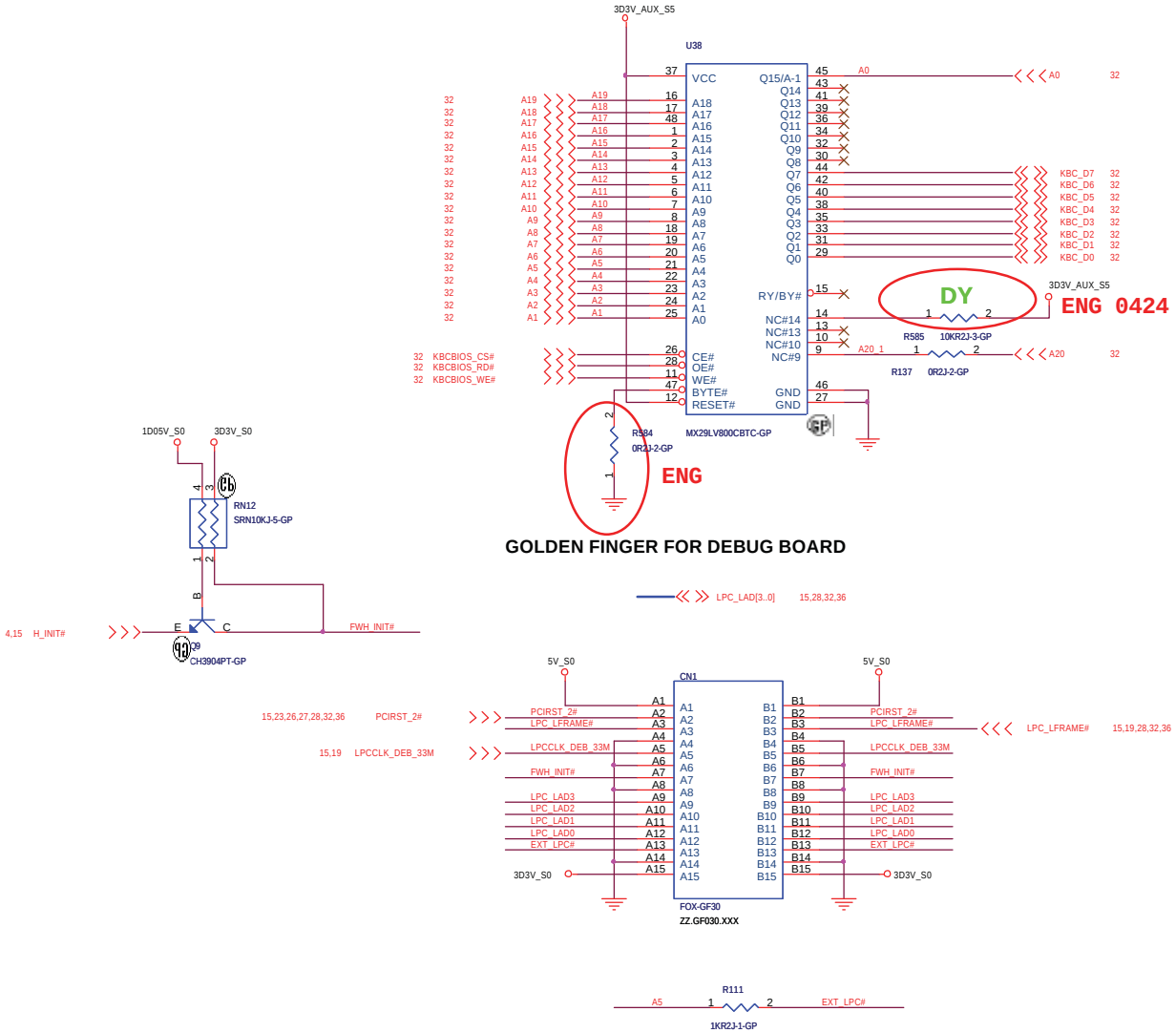

PLCC 32pin ST: 72.50040.003
PLCC 32pin SST:
72.49004.B03

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Title: ***LPC / Debug Port***

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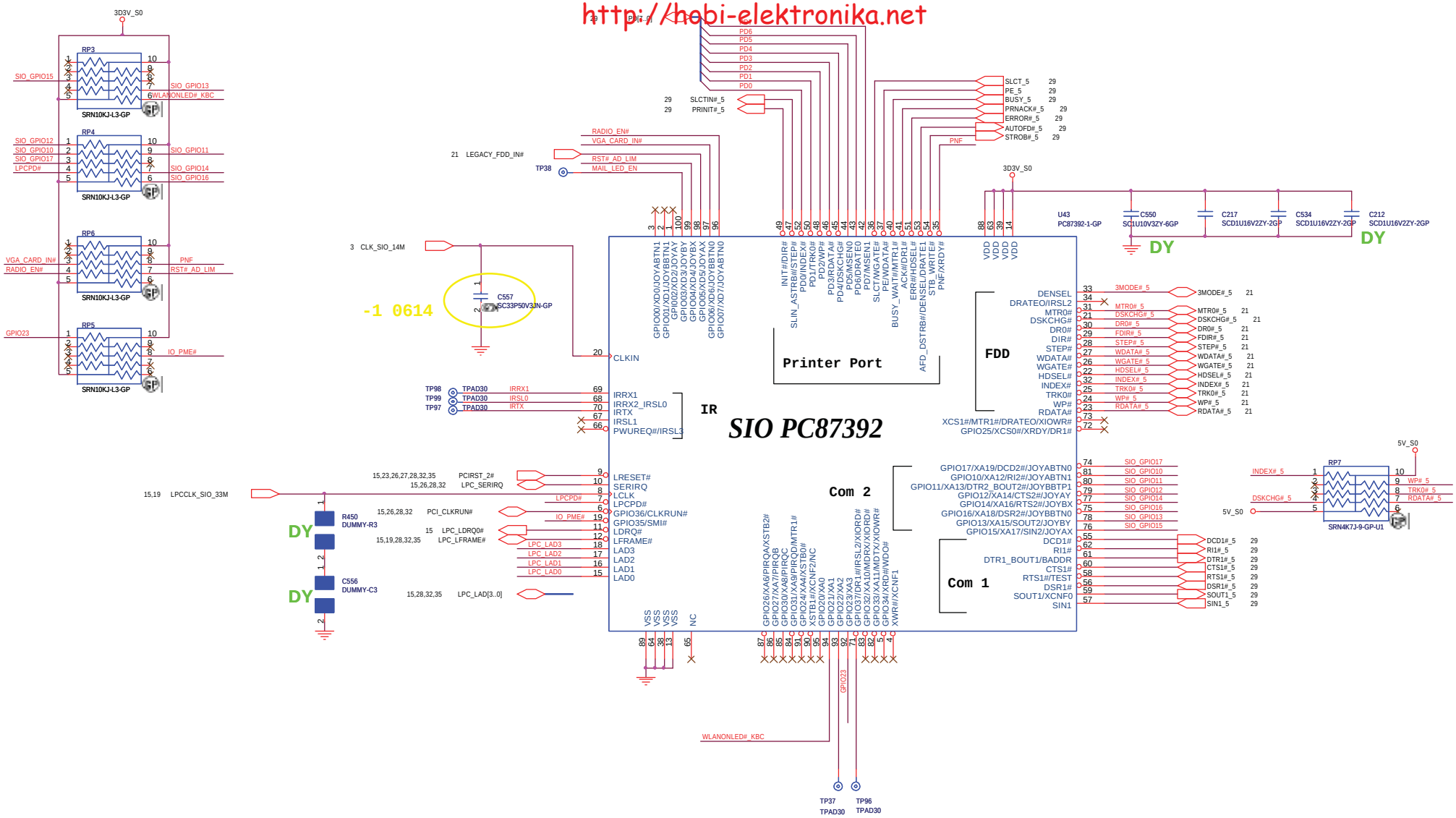

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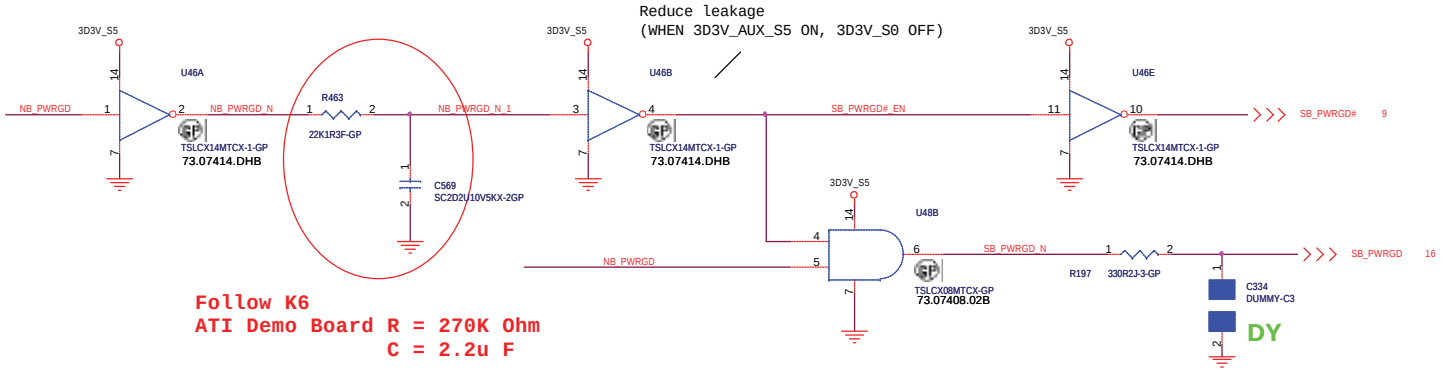
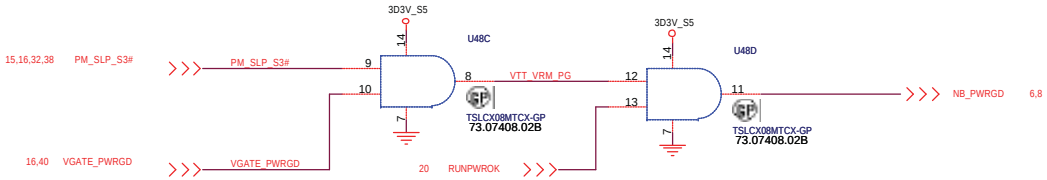
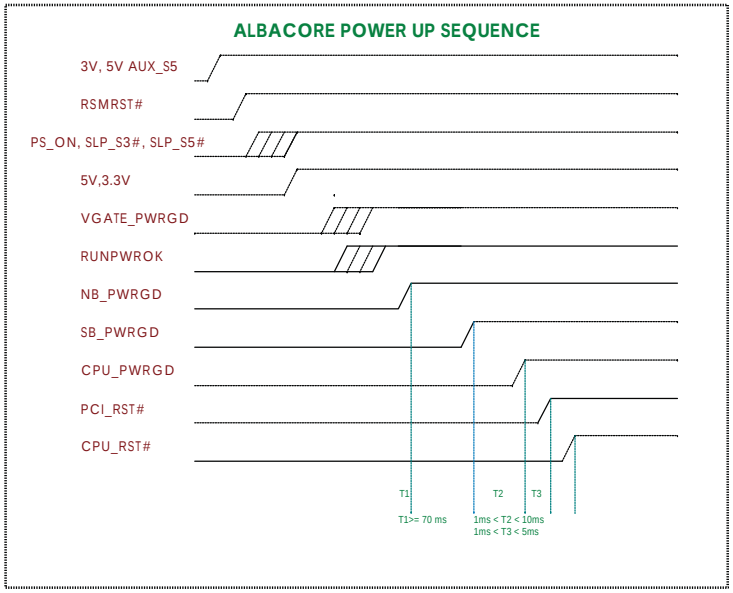
Title	***SIO_87392***	
Size A3	Document Number **Daytona**	Rev **-1**
Date: Wednesday, June 28, 2006	Sheet 36 of 48	

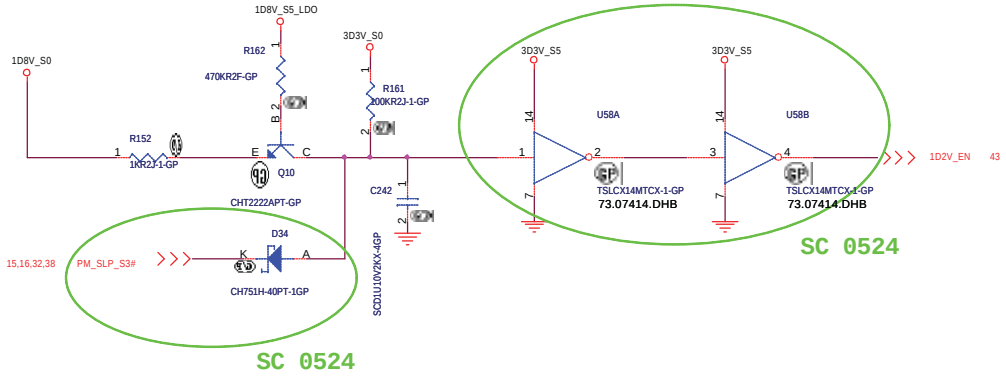


For RC415, SB_PWRGD need to be 65ms after NB_PWRGD





1D2V_S0 should not exceed 1D8V_S0 by more than 0.6V.



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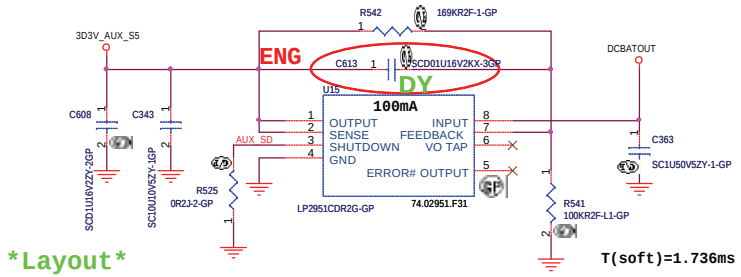
Title: POWER_ON_LOGIC		
Size: A3	Document Number: Daytona	Rev: -1
Date: Tuesday, June 13, 2006	Sheet 37 of 48	

Aux Power

http://hobi-elektronika.net

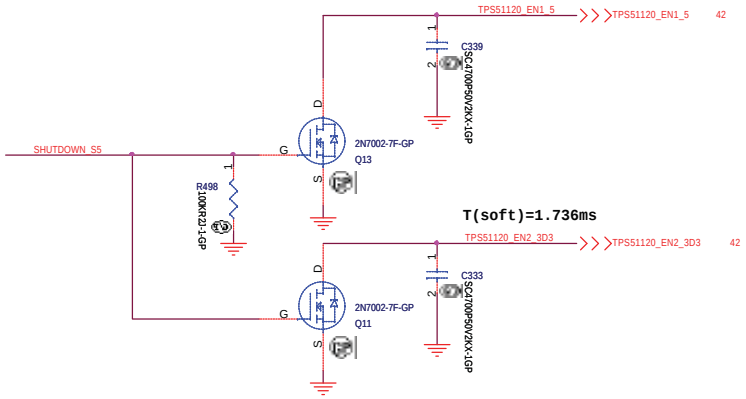


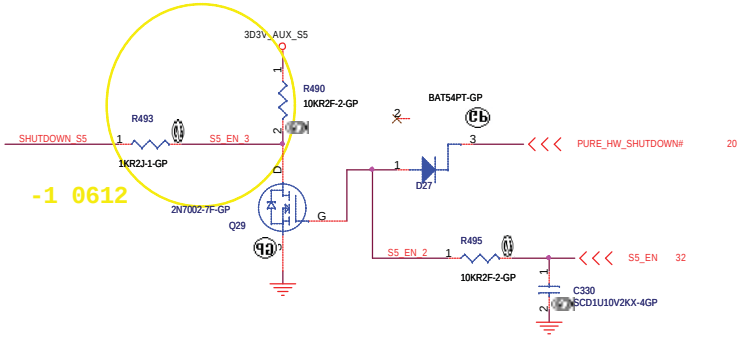
Vout = Vref*(1 + R1/R2)
Vref = 1.235V

T(soft)=1.736ms

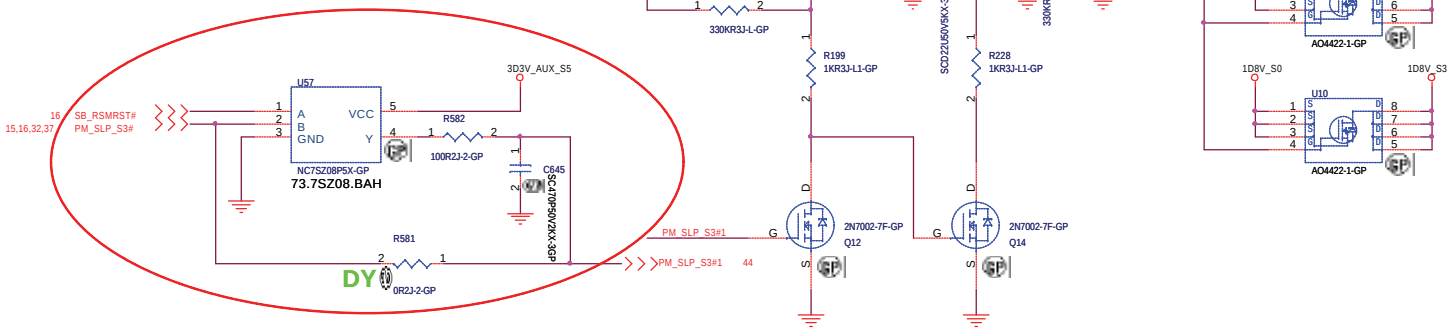
Layout
15 mil

KBC KB3910 need 3D3V_AUX_S5





Run Power



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Title: **PWRPLANE&RESETLOGIC**

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CPU_CORE
Intersil ISL6262

H_VID0
H_VID1
H_VID2
H_VID3
H_VID4
H_VID5
H_VID6

PSI#
CPUCORE_ON
PM_DPRSLPVR
H_DPRSTP#

VCC_SENSE
VSS_SENSE

DCBATOUT_6262
5V_S0
3D3V_S0

VID Setting
VID0(I / 1.05V)
VID1(I / 1.05V)
VID2(I / 1.05V)
VID3(I / 1.05V)
VID4(I / 1.05V)
VID5(I / 1.05V)
VID6(I / 1.05V)

Input Signal
PSI# (I / 3.3V)
PGD_IN (I / 3.3V)
DPRSLPVR (I / 3.3V)
DPRSTP# (I / 3.3V)

Voltage Sense
VSEN(I / Vcore)
RTN(I / Vcore)

Input Power
VCC(I)
VCC(I)
VCC(I)

Output Signal
PGOOD(OD / 3.3V) → 6262_PWRGOOD
CLK_EN#(O) → CLK_EN#

Output Power
VCC_CORE_PWR(O) → VCC_CORE_S0(Imax=48A)

TPS51124
1D8V/1D05V

5V_S5
DCBATOUT_TPS51124

TPS51124_EN1
TPS51124_EN2

CPUCORE_ON
CPUCORE_ON

Input Power
VCC
VIN

Input Signal
EN1
EN2

Output Signal
PGOOD1
PGOOD2

Output Power
1D8V (O) → 1D8V_S0 (7A)
1D05V(O) → 1D05V_S0 (7A)

Charger MAX8725

AD+
AD+

Input Signal
ACSET

Input Power
DCIN

Output Signal

Output Power
VDD → ISL6255_VDD
VOUT (O) → BT+

TPS51120
5V/3D3V

TPS51120_EN1_5
TPS51120_EN2_3D3

DCBATOUT_TPS51120

Input Signal
EN1
EN2

Input Power
VIN

Output Signal
PGOOD1(OD / 5V) → CPUCORE_ON
PGOOD2(OD / 5V) → CPUCORE_ON

Output Power
5V(O) → 5V_DC_S5 (6A)
3D3V(O) → 3D3V_DC_S5 (5A)

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Title: **POWER BLOCK DIAGRAM**

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A3	Daytona	-1

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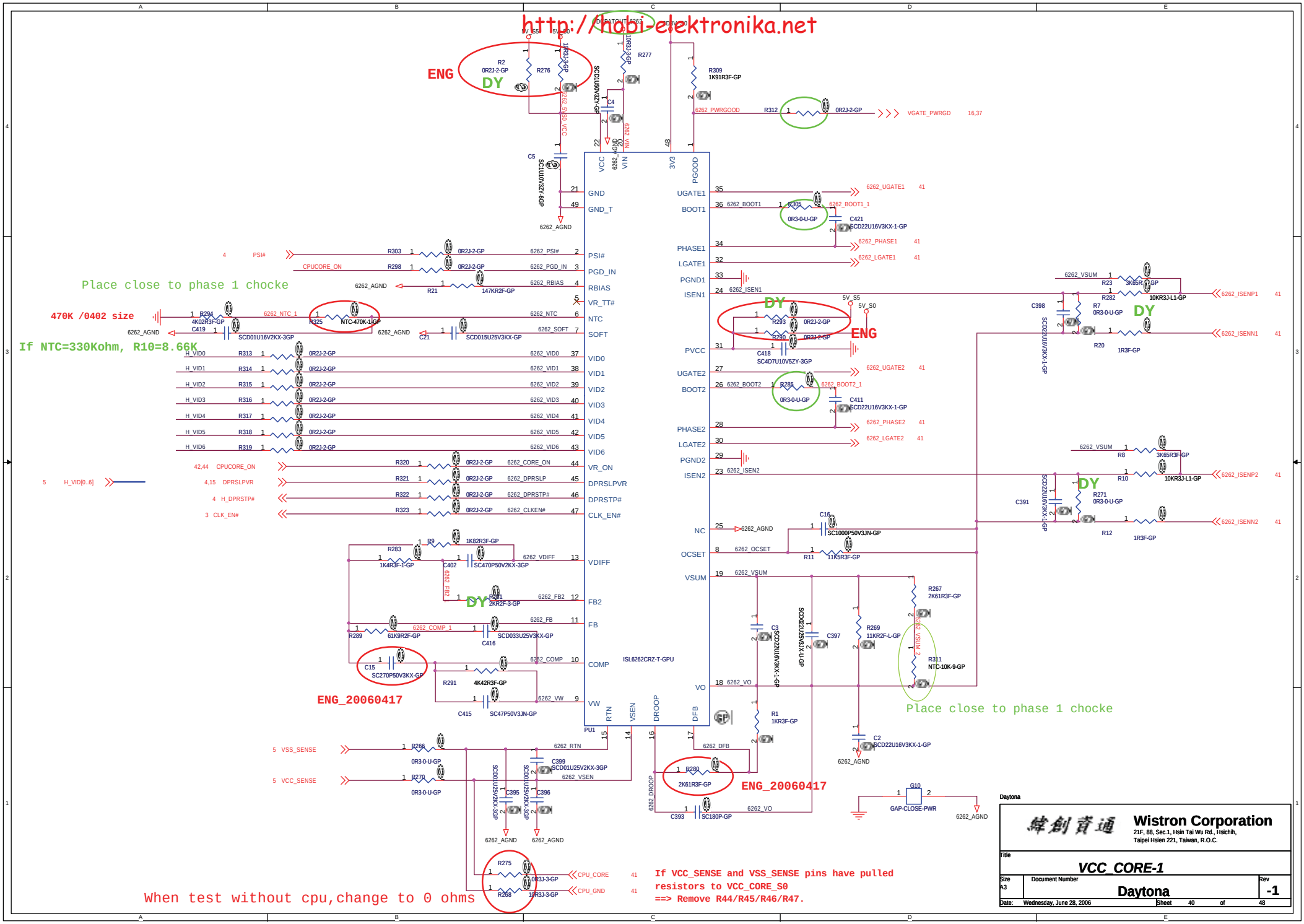

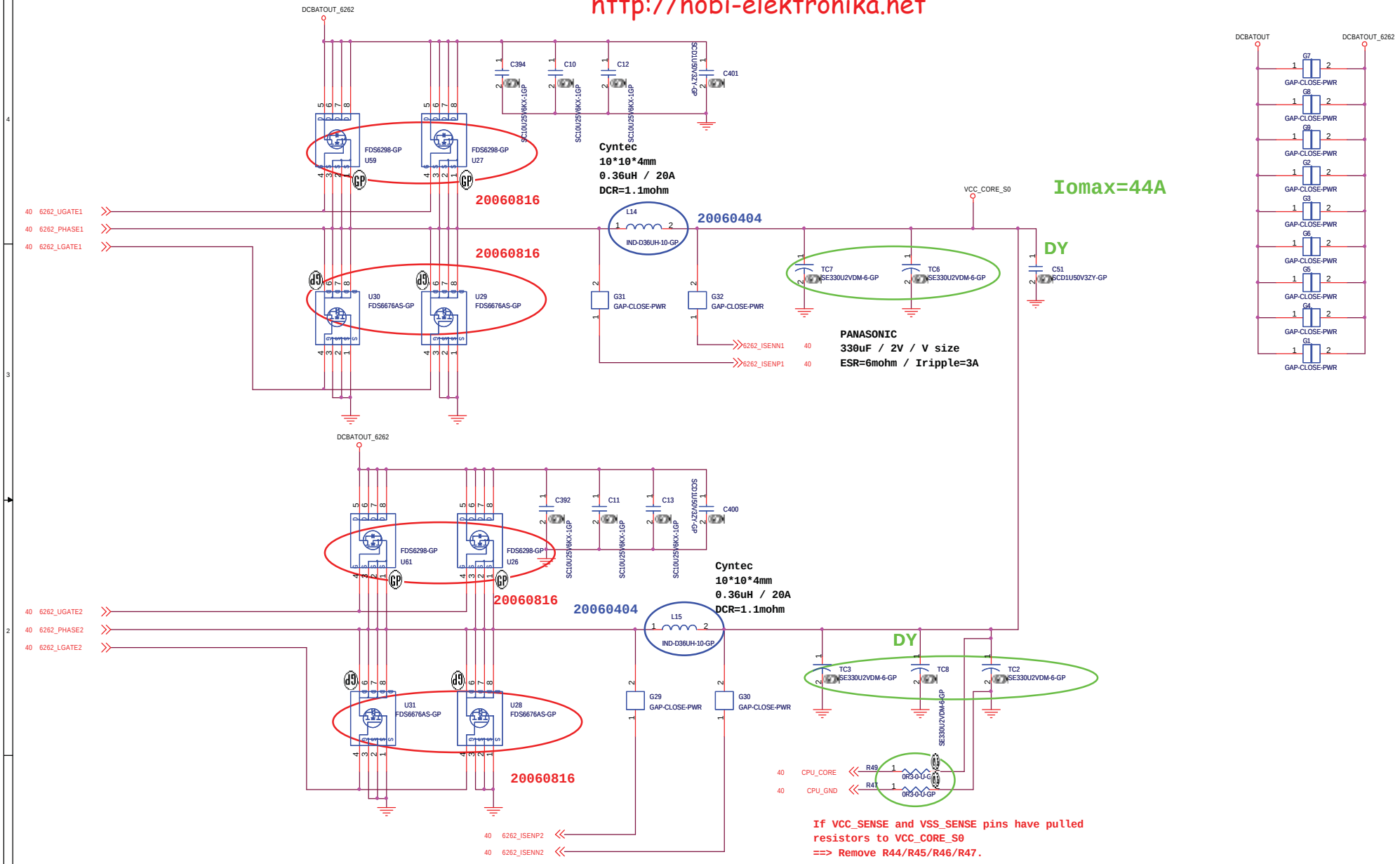

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Title: VCC_CORE_2

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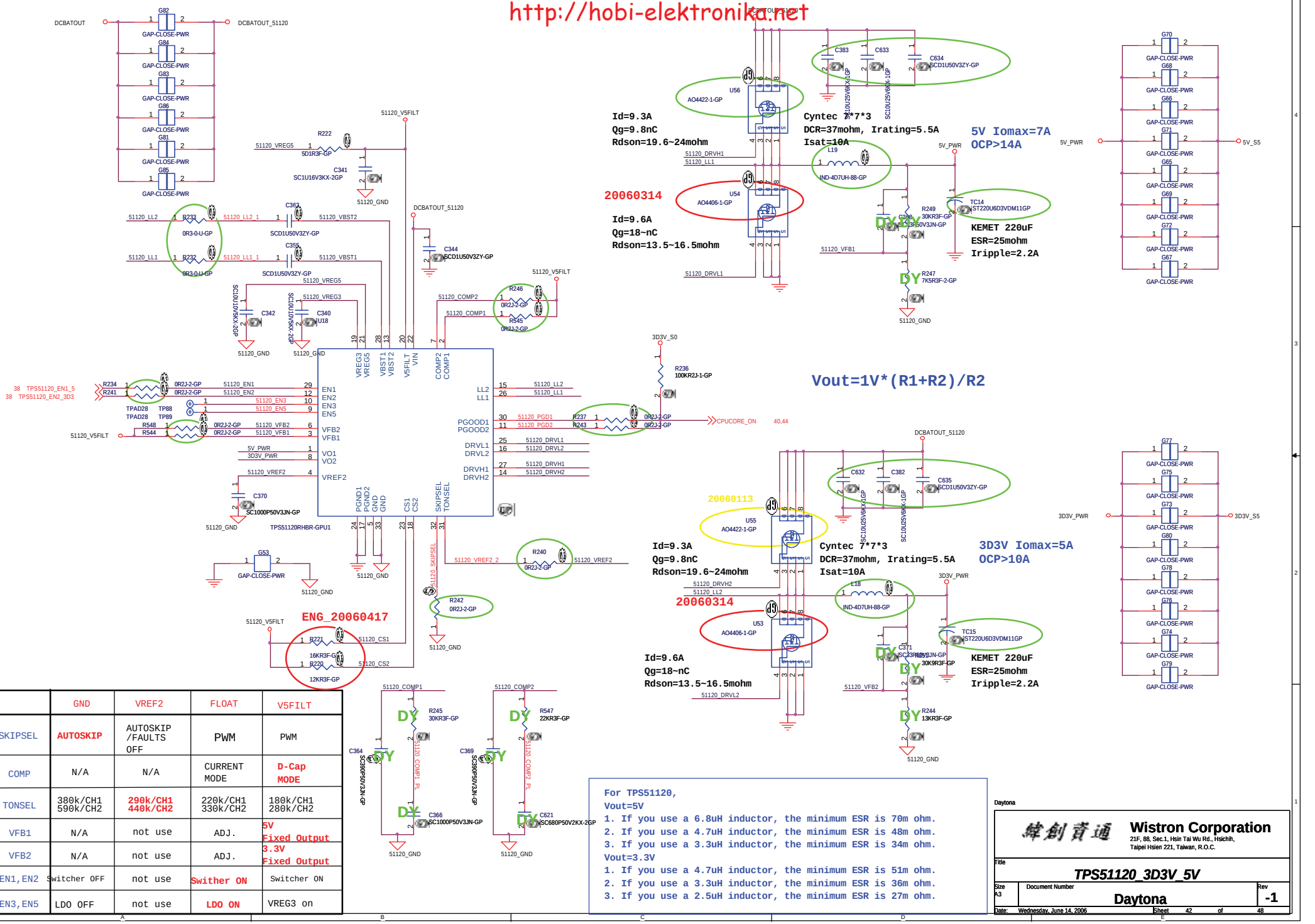

	GND	VREF2	FLOAT	V5FILT
SKIPSEL	**AUTOSKIP**	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	**D-Cap MODE**
TONSEL	380k/CH1 590k/CH2	**290k/CH1 440k/CH2**	220k/CH1 330k/CH2	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	**5V Fixed Output**
VFB2	N/A	not use	ADJ.	**3.3V Fixed Output**
EN1,EN2	Switcher OFF	not use	**Swither ON**	Switcher ON
EN3,EN5	LDO OFF	not use	**LDO ON**	VREG3 on

For TPS51120,
Vout=5V
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.
Vout=3.3V
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

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Title: TPS51120_3D3V_5V

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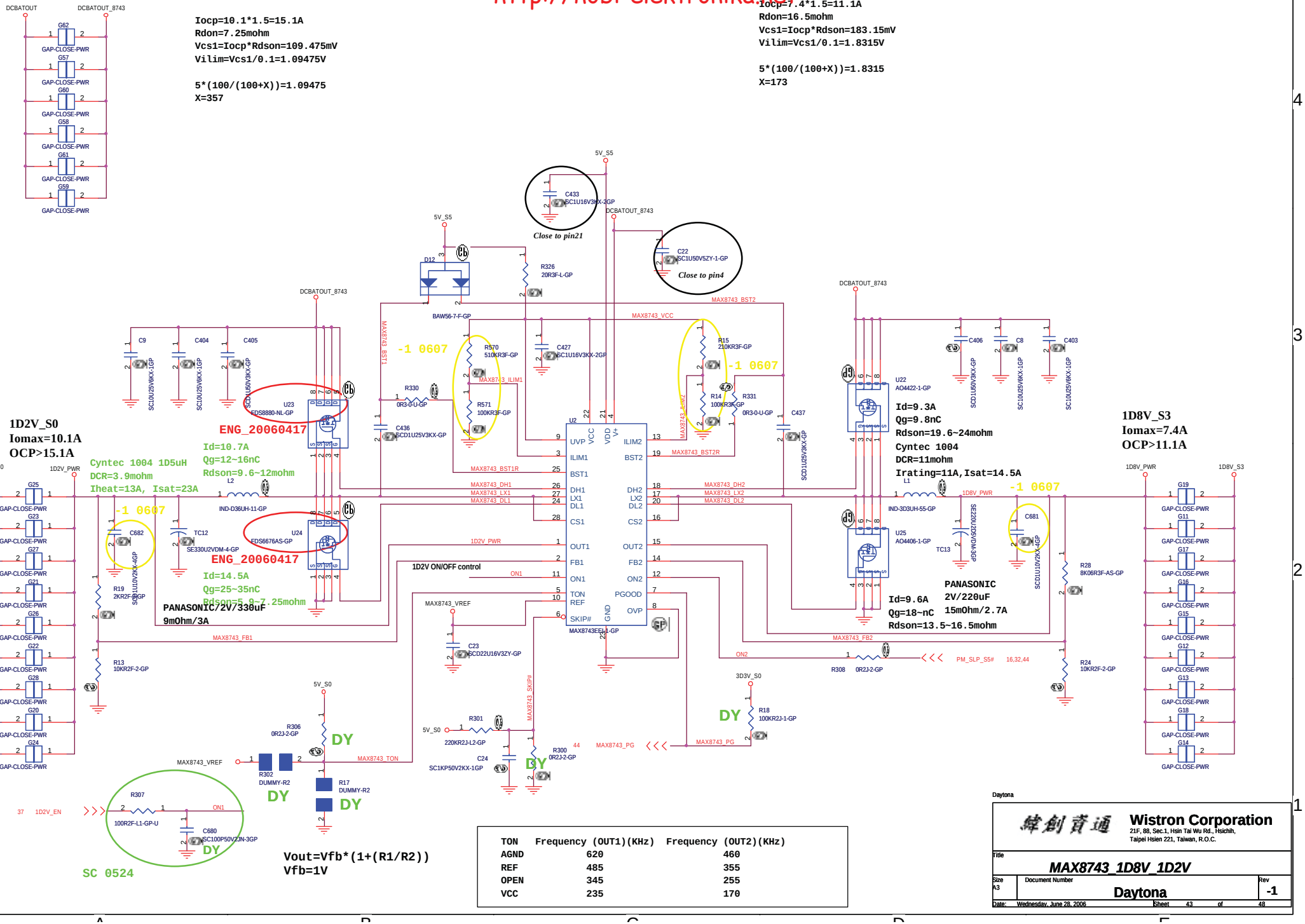
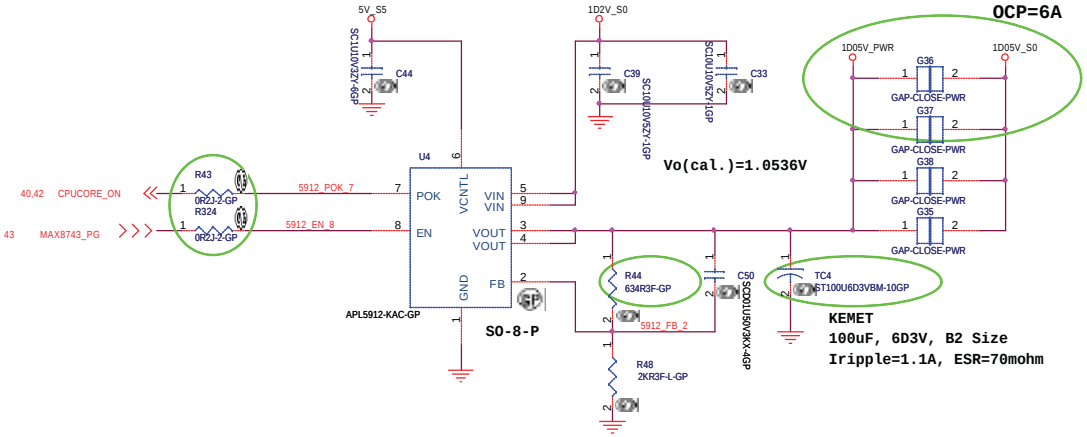
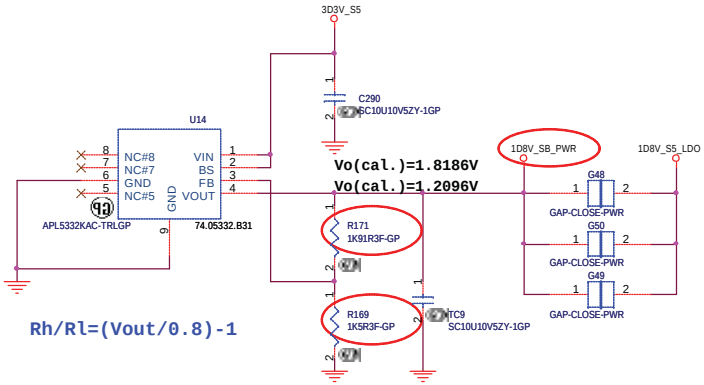


1D05V_S0
Iomax=3A



Vo=0.8*(1+(R1/R2))

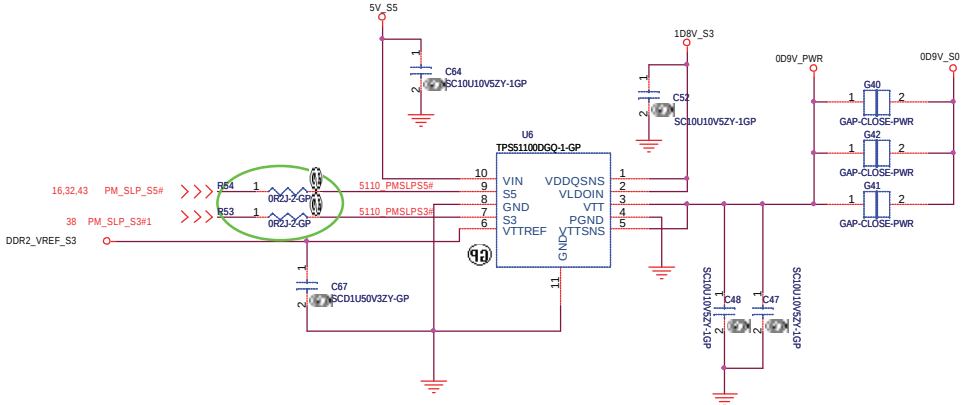
1D8V or 1D2V
Iomax=0.2A



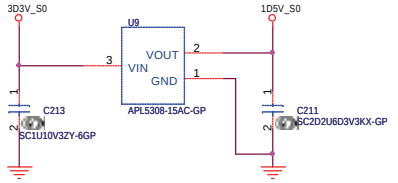
Rh/Rl=(Vout/0.8)-1

SB460=>1D8V (Rh=1K91ohm ,Rl=1K5ohm)
SB600=>1D2V (Rh=768ohm ,Rl=1K5ohm)

0D9V
Iomax=1.5A



1D5V_S0
Iomax=120mA



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Title: 1D5V/0D9V/1D05V/1D8V

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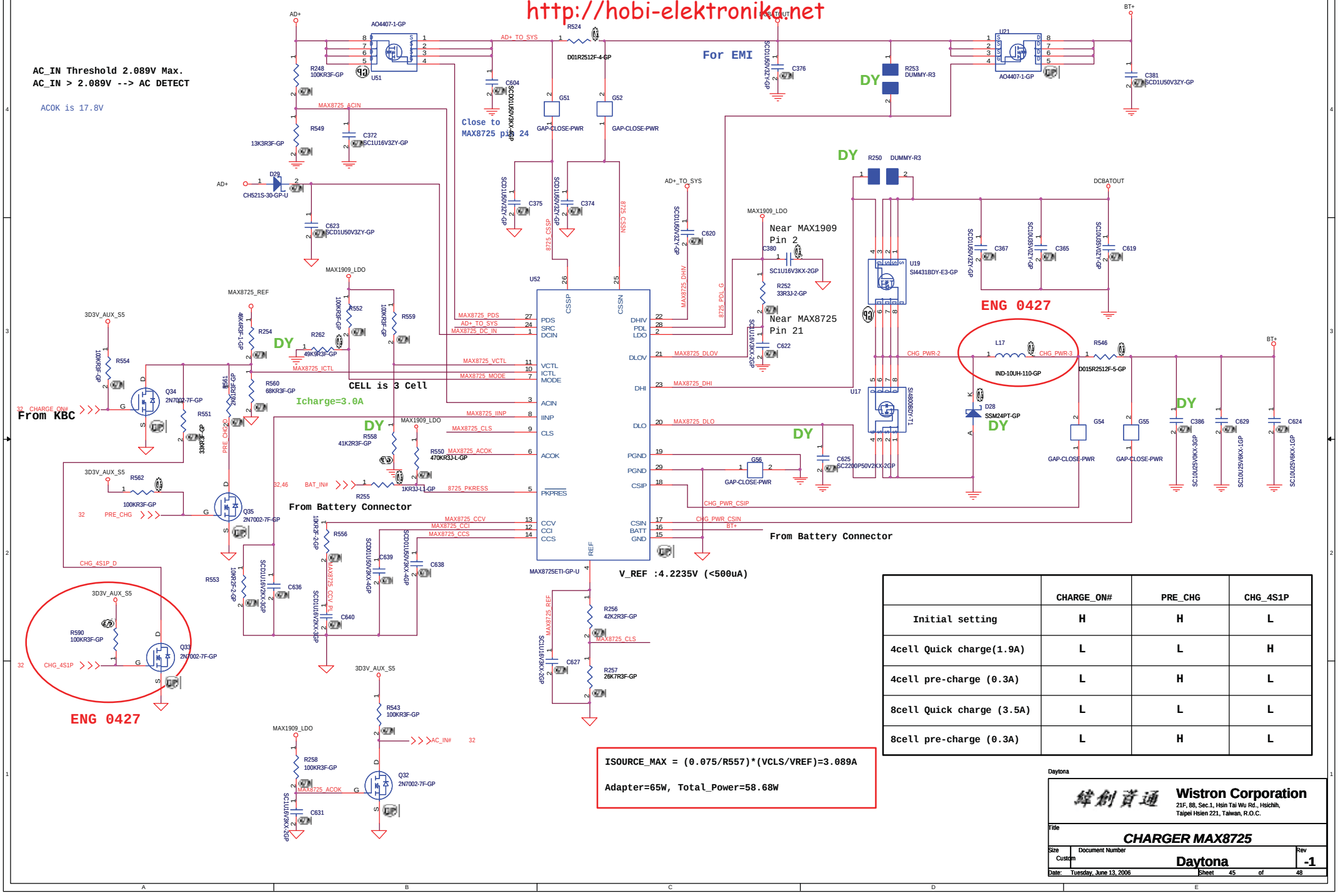

	CHARGE_ON#	PRE_CHG	CHG_4S1P
Initial setting	H	H	L
4cell Quick charge(1.9A)	L	L	H
4cell pre-charge (0.3A)	L	H	L
8cell Quick charge (3.5A)	L	L	L
8cell pre-charge (0.3A)	L	H	L

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Title: CHARGER MAX8725

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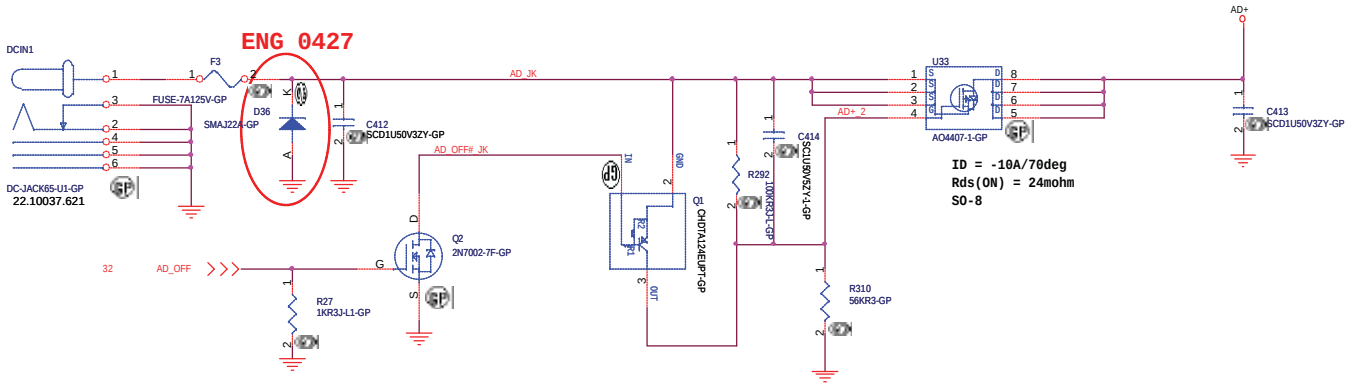
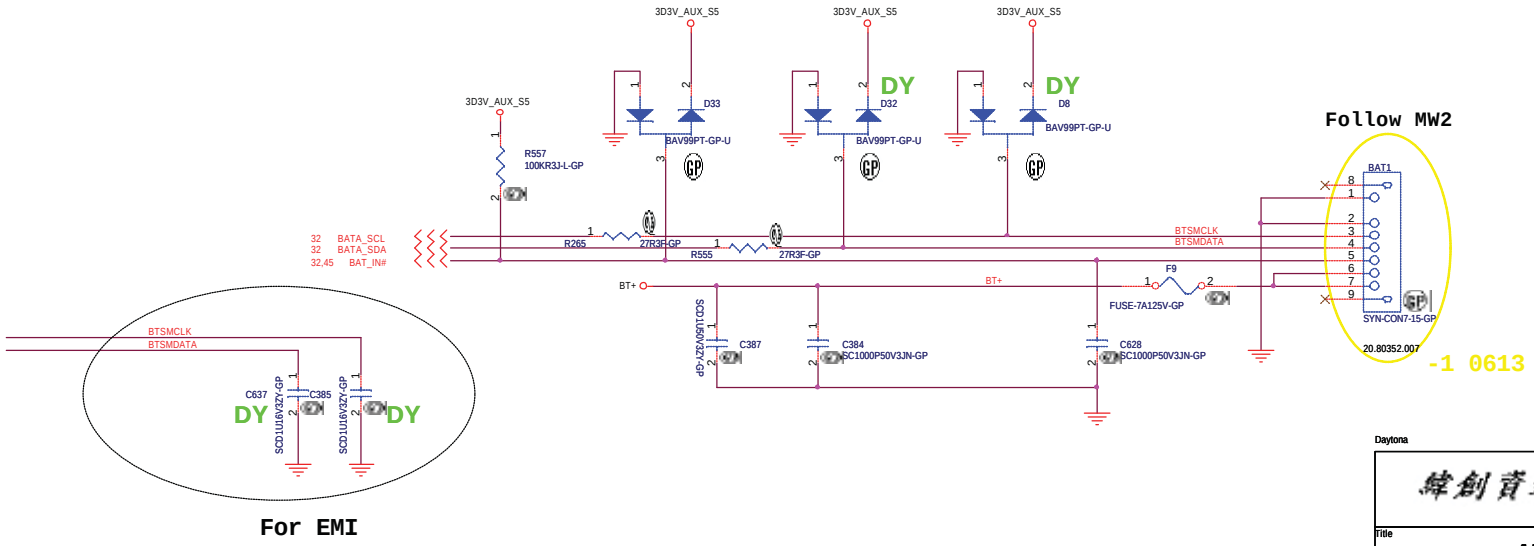
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



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Title: AD/BAT CONN

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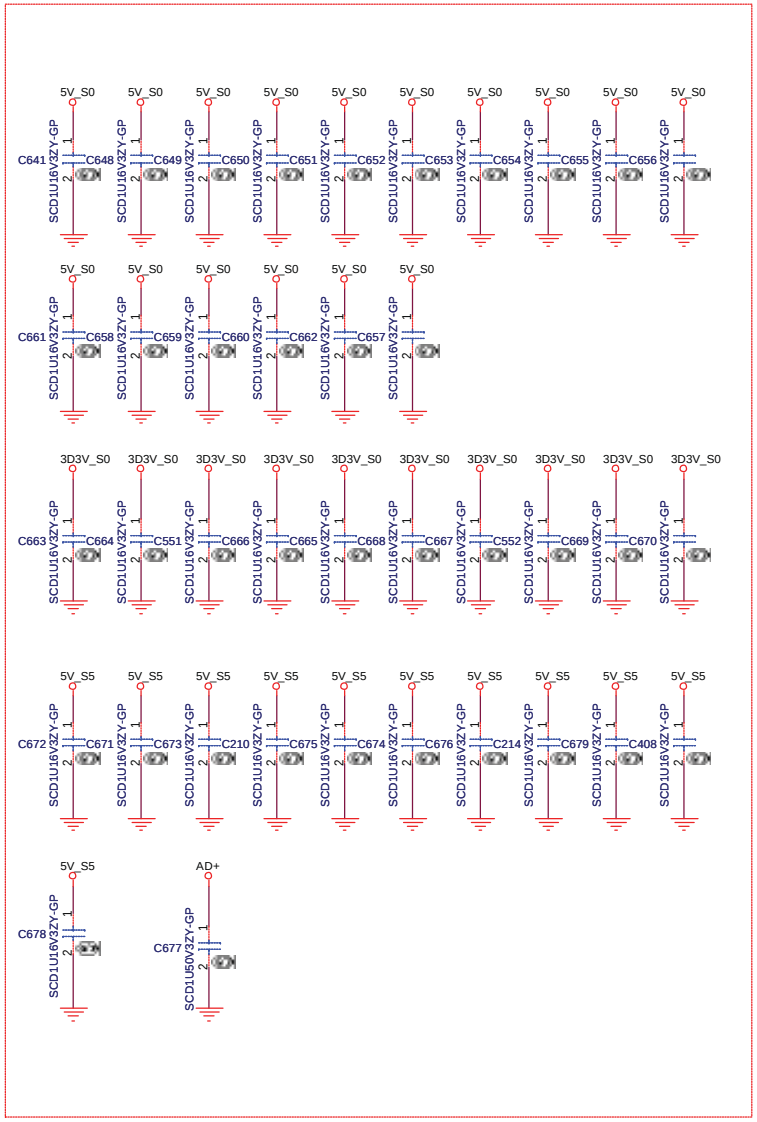
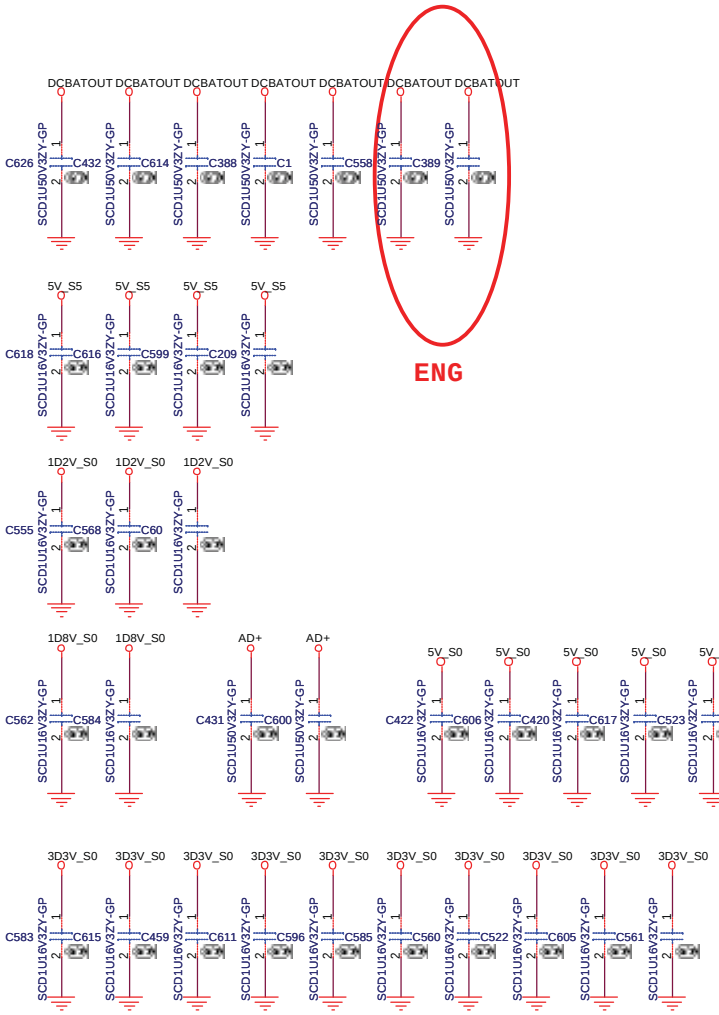


ENG 0509-1 for EMI



ENG

Daytona

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Title: ***EMI***		
Size: Custom	Document Number: **Daytona**	Rev: **-1**
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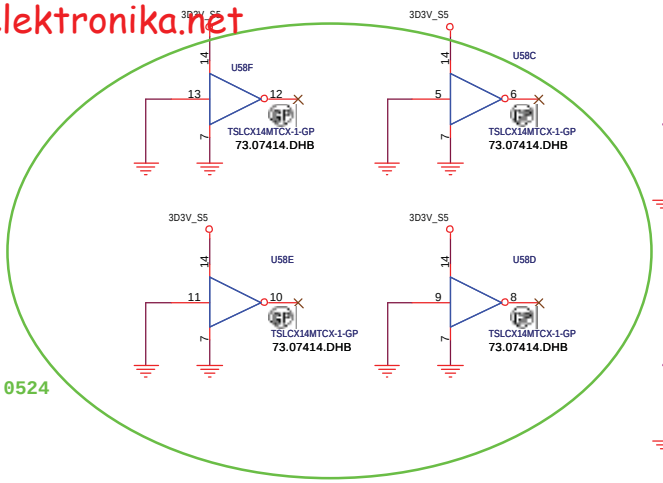
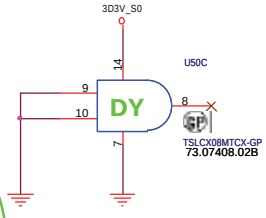
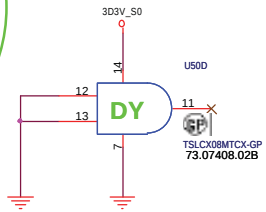
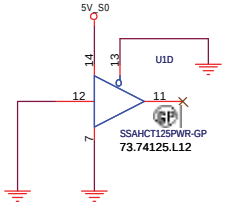
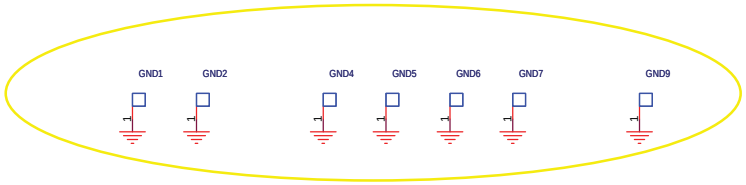


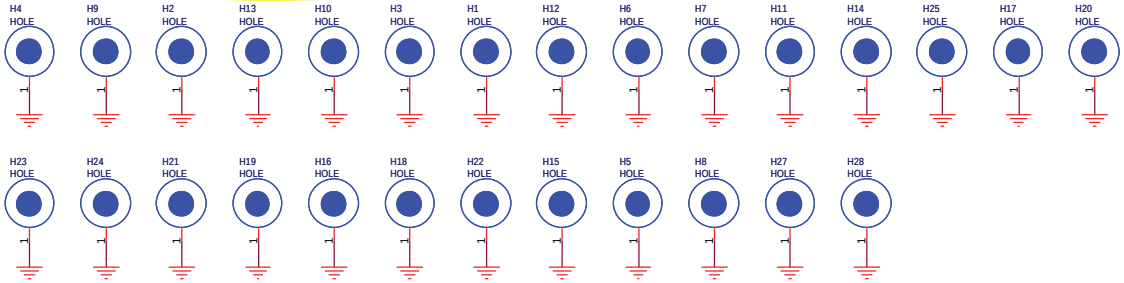






-1 0614





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Title	***MISC***	
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