Dellen Block Diagram

Project code: 91.4V401.001
PCB P/N : 48.4T307.0SA
Revision : 06259-SA

CLK GEN.
RTM865T-433
71.00865.B0W 3

Mobile CPU
Yonah 478
Celeron M
62.10079.001 4, 5

G792 19

HOST BUS 400/533/667MHz@1.05V

DDR2 533/667 MHz 11,12
DDR2 533/667 MHz 11,12
533/667MHz
533/667MHz

Calistoga
AGTL+ CPU I/F
DDR Memory I/F
INTEGRATED GRAHPICS
LVDS, CRT I/F
71.CALIS.00U 6,7,8,9,10

X4 DMI 400MHz
C-Link0

TV Out 14
CRT 14
LCD 14
DVI 43
MXM conn. 27

PCB STACKUP
TOP
VCC
S
S
GND
BOTTOM

Line In
MIC In 14
31 INT.SPKR
Line Out (No-SPDIF)
Codec ALC268 29
AZALIA
OP AMP G1431Q 30
OP AMP G1412 30
RJ11
MODEM MDC Card 21

ICH7M
4 PCIe ports
PCI/PCI BRIDGE
ACPI 2.0
2 SATA
1 PATA 66/100
8 USB 2.0/1.1 ports
ETHERNET (10/100/1000MbE)
High Definition Audio
LPC I/F
Serial Peripheral I/F
71.ICH7M.00U 15,16,17,18

PCI BUS
PCIex1
LPC BUS

PCMCIA I/F
TI PCI7412 Cardbus Cardreader 24,25
PWR SW CP2211F 25
PCMCIA SLOT Support TypeII 26
1394 CONN 26
MS/MS Pro/xD/ MMC/SD 5 in 1 26
LAN GIGA BCM5787M 22
TXFM 23
RJ45 23
Mini Card Kedron a/b/g/n 28

New card 28
PCI Express
SATA
PATA
USB
P2231NFC1 28
HDD 20
ODD 20
MINI USB BlueTooth 21
Finger Pad 32
USB 4 Port 21
CCD 13

KBC Winbond WPC8768L 31
SPI I/F
BIOS W25X80-VSS 33
LPC DEBUG CONN. 33
Touch Pad 32
INT. KB 32
FIR 31

SYSTEM DC/DC MAX8744 37	
INPUTS	OUTPUTS
DCBATOUT	3D3V_S5(6A) 5V_S5 (6A) 5V_AUX_S5

SYSTEM DC/DC Max8717 38	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(12A) 1D8V_S3(8.5A)

TPS51100 39	
1D8V_S3	DDR_VREF_S0 (1.5A) DDR_VREF_S3

APL531230 39	
3D3V_S0	2D5V_S0(130 mA

APL5912 39	
1D8V_S3	1D5V_S0(5A)

ISL CHARGER ISL6255 41	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 4.0A UP+5V 5V 100mA

CPU DC/DC MAX8770 35,36	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 47A

UMA

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Title: BLOCK DIAGRAM
Size: A3 | Document Number: Dellen | Rev: SA
Date: Tuesday, January 16, 2007 | Sheet 1 of 43

ICH7M Integrated Pull-up and Pull-down Resistors

ICH7-M EDS 17837 1.5V1

EE_DIN, EE_DOUT, GNT[3:0], GPIO[25], GNT[4]#/GPIO48, GNT[5]#/GPO17, PME#, LAD[3:0]#/FHW[3:0]#, LAN_RXD[2:0] LDRQ[0], LDRQ[1]/GPIO[41], PWRBTN#, TP[3]	ICH7 internal 20K pull-ups
DD[7], DDREQ	ICH7 internal 11.5K pull-downs
ACZ_BIT_CLK, ACZ_RST#, ACZ_SDIN[2:0], ACZ_SDOUT, ACZ_SYNC, DPRSLPVR/GPIO16, EE_CS, SPI_ARB, SPI_CLK, SPKR,	ICH7 internal 20K pull-downs
USB[7:0][P,N]	ICH7 internal 15K pull-downs
SATALED#	ICH7 internal 15K pull-up
LAN_CLK	ICH7 internal 100K pull-down

ICH7M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

ICH7M Functional Strap Definitions

page 16

Signal	Usage/When Sampled	Comment
ACZ_SDOUT	XOR Chain Entrance/ PCIE Port Config bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h)
ACZ_SYNC	PCIE bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
EE_CS	Reserved	This signal should not be pull high.
EE_DOUT	Reserved	This signal should not be pull low.
GNT2#	Reserved	This signal should not be pull low.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT5#/ GPIO17#, GNT4#/ GPIO48	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT5# is MSB, 01-SPI, 10-PCI, 11-LPC.
DPRSLPVR	Reserved	This signal should not be pull high.
GPIO25	Reserved. Rising Edge of RSMRST#.	This signal should not be pull low.
INTVRMEN	Integrated VccSus1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05 VRM when sampled high
LINKALERT#	Reserved	Requires an external pull-up resistor.
REQ[4:1]#	XOR Chain Selection. Rising Edge of PWROK.	TBD, Chapter 8.
SATALED#	Reserved	This signal should not be pull low.
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH7 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.

ICH8M Integrated Pull-up and Pull-down Resistors

ICH8-M EDS 21762 2.0V1

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 10K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	PULL-UP 13K

History

PCI Routing

page 17

	IDSEL	INT	REQ	GNT
TI7412	AD22	G:CARDBUS B:1394 F:Flash Media G:SD Host	0	0

PCIE Routing

LANE1	LAN BCM5787M
LANE2	MiniCard WLAN
LANE3	NewCard WLAN

USB Table

USB ports definition	
Pair	Device
0	USB1
1	USB3
2	USB2
3	USB4
4	FingerPad
5	BlueTooth
6	CCD
7	NewCard

Calistoga Strapping Signals and Configuration

EDS 17050 0.71 page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 =Mobile CPU(Default)
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG17	Global R-comp Disable (All R-comps)	0 = All R-comp Disable 1 = Normal Operation (Default)
CFG18	VCC Select	0 = 1.05V (Default) 1 = 1.5V
CFG19	DMI Lane Reversal	0 = Normal operation (Default):lane Numbered in order 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	0 = Only SDVO or PCIE x1 is operational (Default) 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCRTL_DATA	SDVO Present	0 = No SDVO Card present (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading edge of the Calistoga GMCH PWORK in signal.

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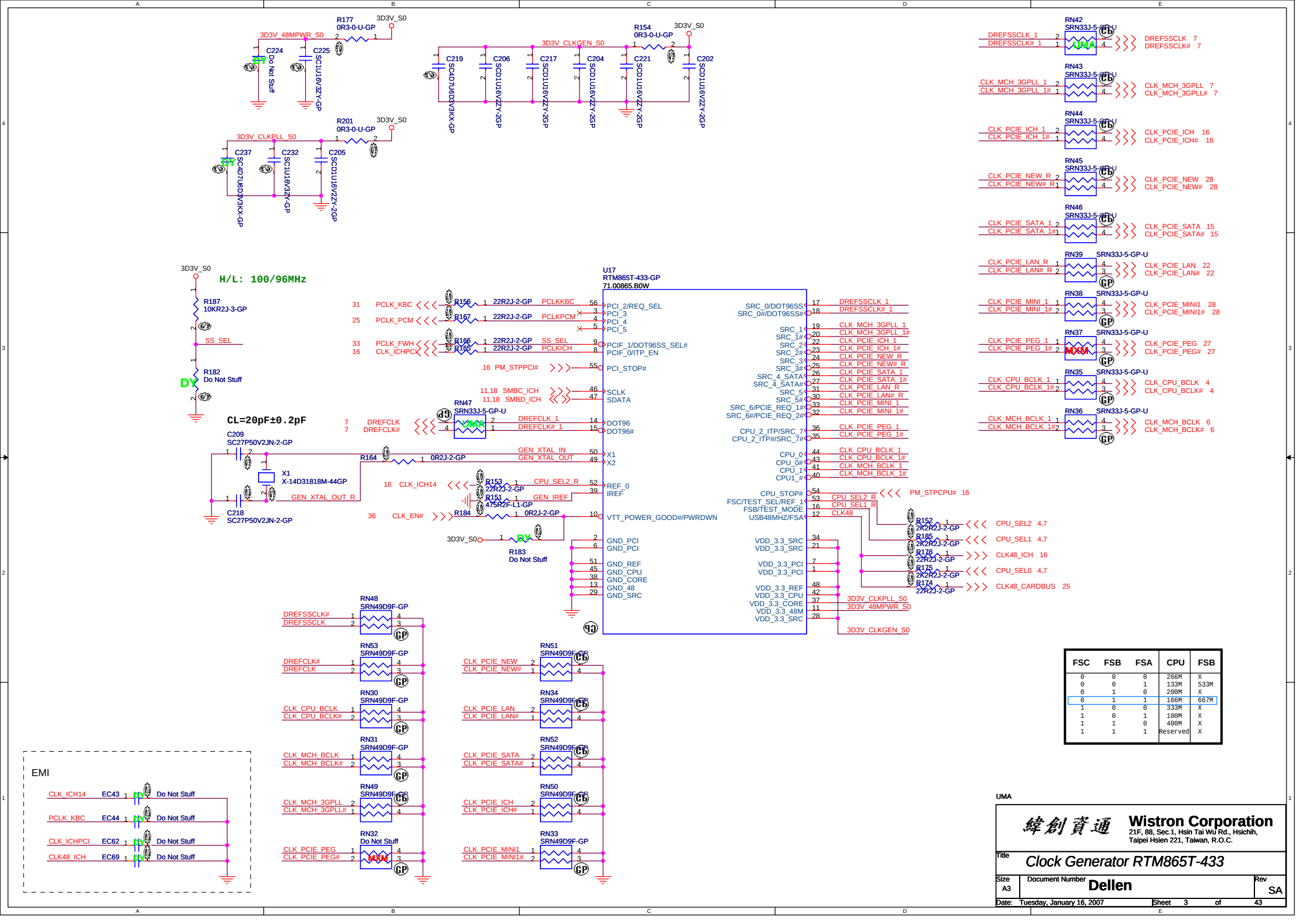
Title: Reference

Size: A3 | Document Number: Dellen | Rev: SA

Date: Tuesday, January 16, 2007 | Sheet 2 of 43



FSC	FSB	FSA	CPU	FSB
0	0	0	266M	X
0	0	1	133M	533M
0	1	0	200M	X
0	1	1	166M	667M
1	0	0	333M	X
1	0	1	100M	X
1	1	0	400M	X
1	1	1	Reserved	X

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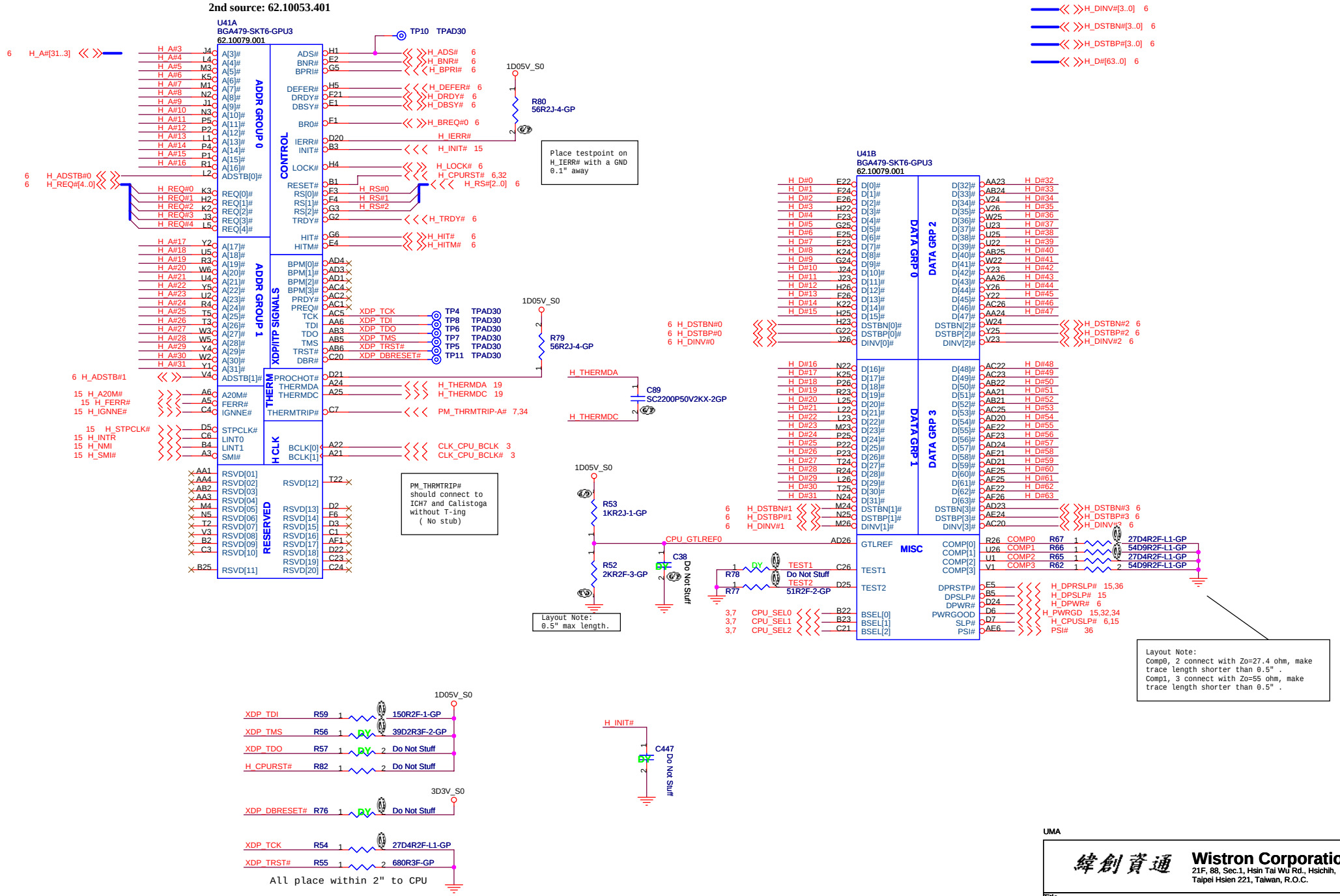
Title: *Clock Generator RTM865T-433*

Size: A3 | Document Number: **Dellen** | Rev: SA

Date: Tuesday, January 16, 2007 | Sheet 3 of 43

2nd source: 62.10053.401



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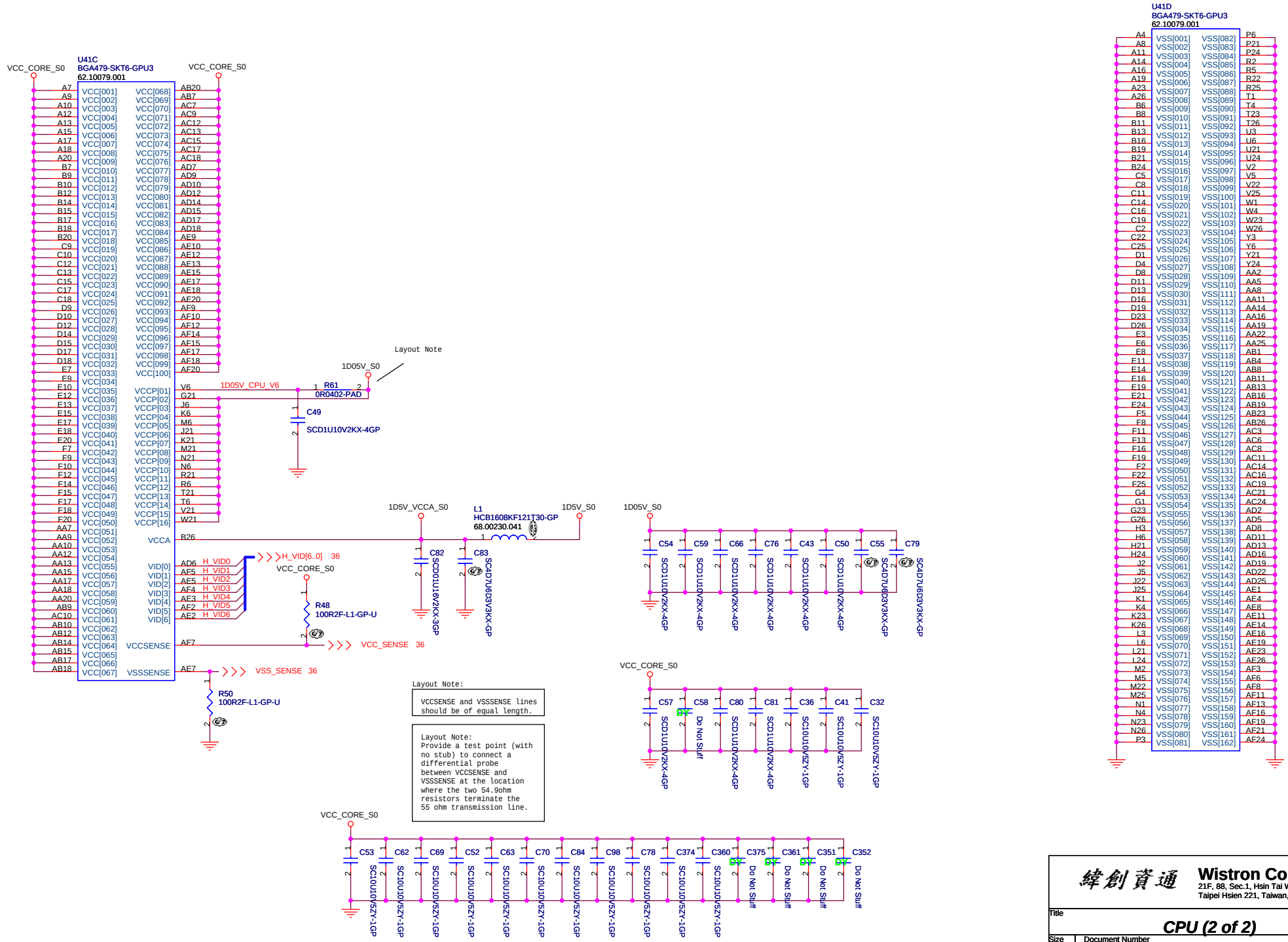
Title: CPU (1 of 2)

Size: A3 | Document Number: Dellen | Rev: SA

Date: Tuesday, January 16, 2007 | Sheet 4 of 43



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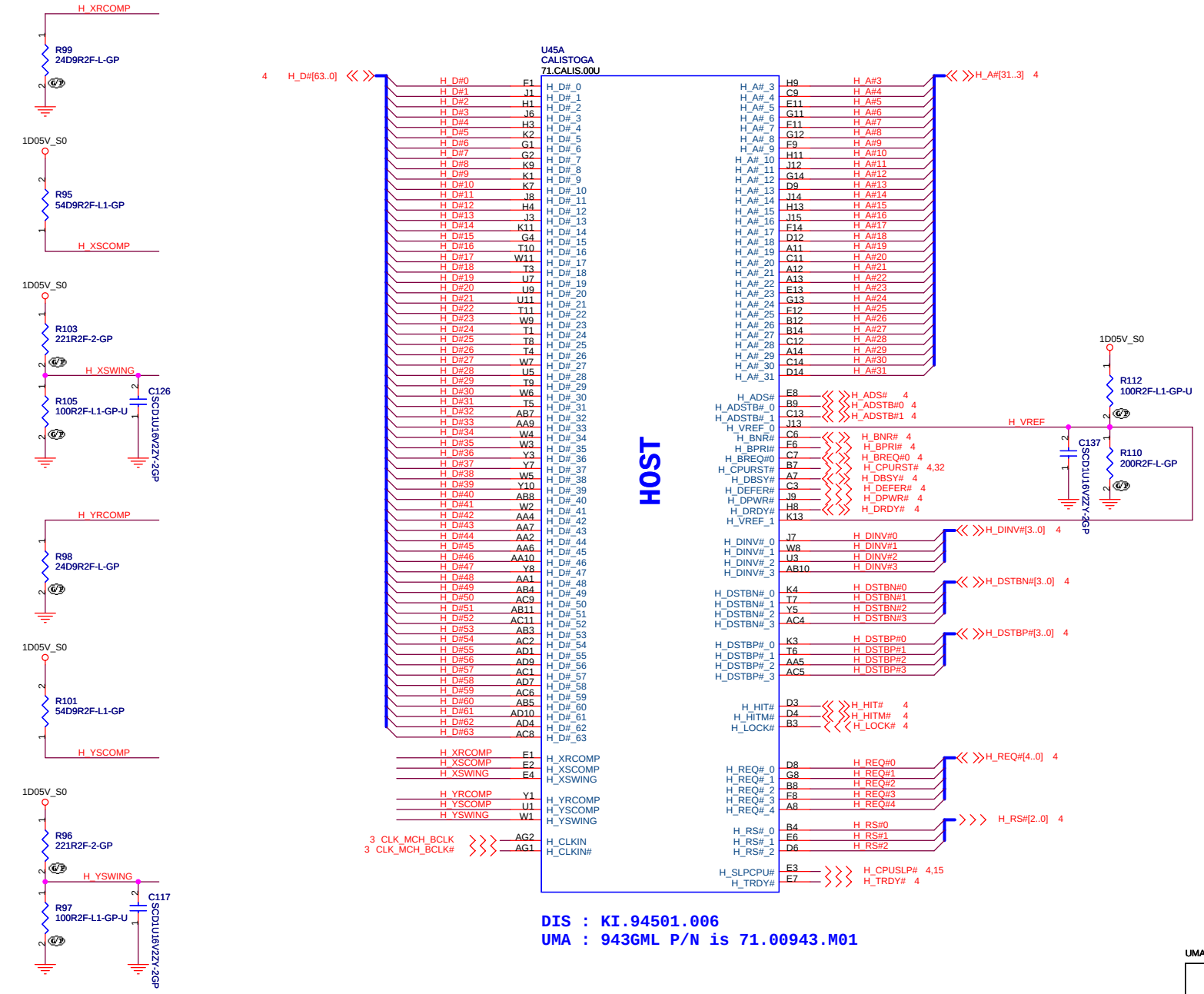
Size: A3	Document Number: **Dellen**	Rev: SA
Date: Tuesday, January 16, 2007	Sheet 5 of 43	



DIS : KI.94501.006
UMA : 943GML P/N is 71.00943.M01

Place them near to the chip (< 0.5")

UMA

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Title: ***GMCH (1 of 5)***

Size	Document Number	Rev
A3	Dellen	SA

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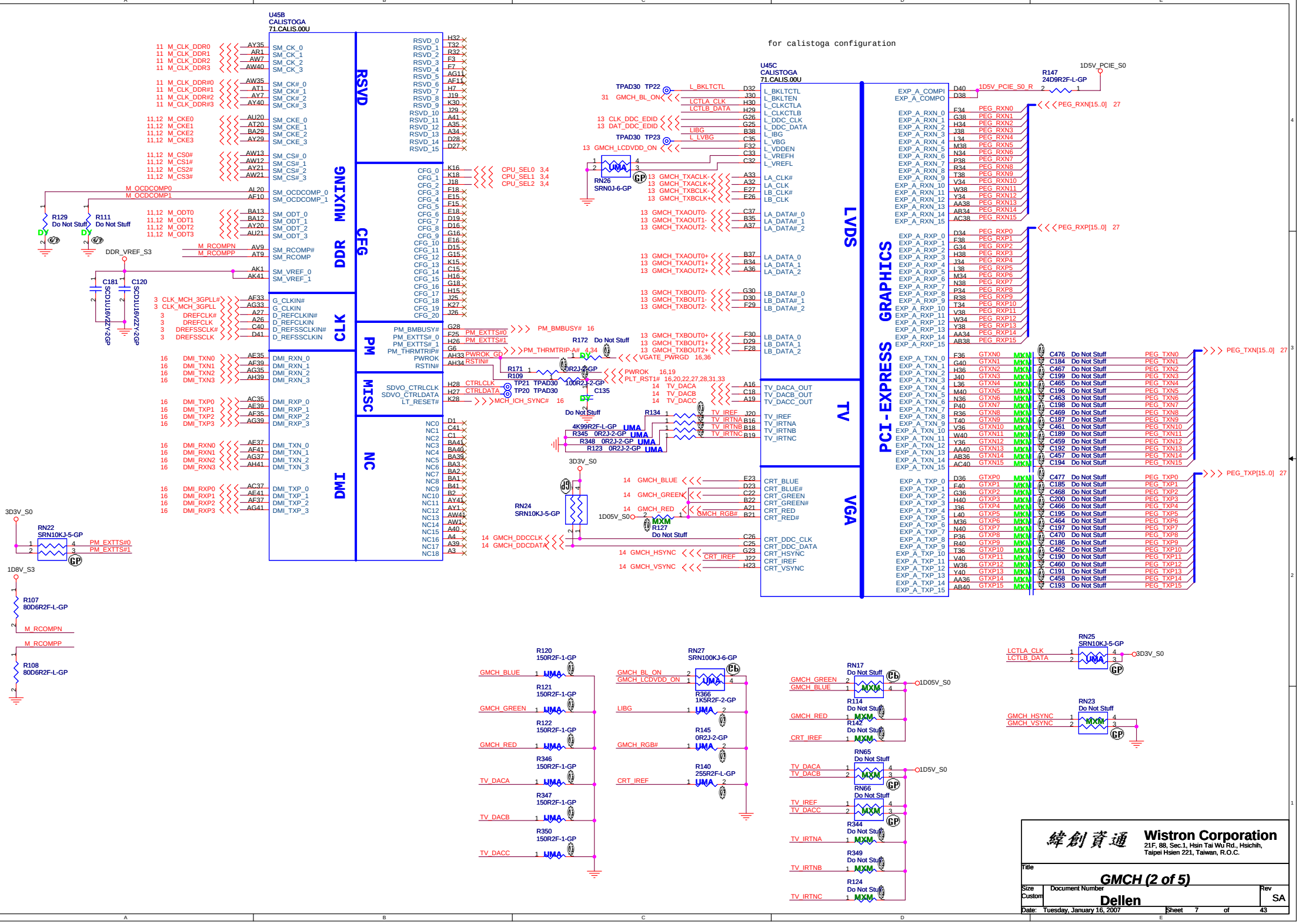
for calistoga configuration
U45B
CALISTOGA
71.CALIS.00U
RSVD
CFG
DDR MUXING
CLK
PM
MISC
NC
DMI
U45C
CALISTOGA
71.CALIS.00U
LVDS
TV
VGA
PCI-EXPRESS GRAPHICS
M_CLK_DDR0
M_CLK_DDR1
M_CLK_DDR2
M_CLK_DDR3
M_CLK_DDR#0
M_CLK_DDR#1
M_CLK_DDR#2
M_CLK_DDR#3
M_CKE0
M_CKE1
M_CKE2
M_CKE3
M_CS0#
M_CS1#
M_CS2#
M_CS3#
M_ODT0
M_ODT1
M_ODT2
M_ODT3
M_OCDCOMP0
M_OCDCOMP1
R129 Do Not Stuff
R111 Do Not Stuff
DDR_VREF_S3
M_RCOMPN
M_RCOMPP
C181
C120
CLK_MCH_3GPLL#
CLK_MCH_3GPLL
DREFCLK#
DREFCLK
DREFSSCLK#
DREFSSCLK
DMI_RXN_0
DMI_RXN_1
DMI_RXN_2
DMI_RXN_3
DMI_TXP0
DMI_TXP1
DMI_TXP2
DMI_TXP3
DMI_RXN0
DMI_RXN1
DMI_RXN2
DMI_RXN3
DMI_RXP0
DMI_RXP1
DMI_RXP2
DMI_RXP3
DMI_TXN_0
DMI_TXN_1
DMI_TXN_2
DMI_TXN_3
DMI_TXP_0
DMI_TXP_1
DMI_TXP_2
DMI_TXP_3
3D3V_S0
RN22
SRN10KJ-5-GP
PM_EXTTS#0
PM_EXTTS#1
1D8V_S3
R107
80D6R2F-L-GP
R108
80D6R2F-L-GP
CPU_SEL0 3,4
CPU_SEL1 3,4
CPU_SEL2 3,4
PM_BMBUSY# 16
PM_EXTTS#0
PM_EXTTS#1
PM_THRMTRIP# 4,34
PWROK
RSTIN#
R172 Do Not Stuff
R171
R109
100R2J-2-GP
PWROK 16,19
PLT_RST1# 16,20,22,27,28,31,33
VGATE_PWRGD 16,36
SDVO_CTRLCLK
SDVO_CTRLDATA
LT_RESET#
MCH_ICH_SYNC# 16
TP21 TP20
C135
4K99R2F-L-GP
R345 0R2J-2-GP
R348 0R2J-2-GP
R123 0R2J-2-GP
R134
TV_IREF
TV_IRTNA
TV_IRTNB
TV_IRTNC
TV_DACA
TV_DACB
TV_DACC
TPAD30 TP22
TPAD30 TP23
GMCH_BL_ON
GMCH_LCDVDD_ON
LCTLA_CLK
LCTLB_DATA
CLK_DDC_EDID
DAT_DDC_EDID
LIBG
L_LVBG
RN26
SRN0J-6-GP
GMCH_TXACLK-
GMCH_TXACLK+
GMCH_TXBCLK-
GMCH_TXBCLK+
GMCH_TXAOUT0-
GMCH_TXAOUT1-
GMCH_TXAOUT2-
GMCH_TXAOUT0+
GMCH_TXAOUT1+
GMCH_TXAOUT2+
GMCH_TXBOUT0-
GMCH_TXBOUT1-
GMCH_TXBOUT2-
GMCH_TXBOUT0+
GMCH_TXBOUT1+
GMCH_TXBOUT2+
TV_DACA_OUT
TV_DACB_OUT
TV_DACC_OUT
TV_IREF
TV_IRTNA
TV_IRTNB
TV_IRTNC
CRT_BLUE
CRT_BLUE#
CRT_GREEN
CRT_GREEN#
CRT_RED
CRT_RED#
CRT_DDC_CLK
CRT_DDC_DATA
CRT_HSYNC
CRT_IREF
CRT_VSYNC
GMCH_BLUE
GMCH_GREEN
GMCH_RED
GMCH_RGB#
GMCH_DDCCLK
GMCH_DDCDATA
GMCH_HSYNC
GMCH_VSYNC
RN24
SRN10KJ-5-GP
1D05V_S0
R127
Do Not Stuff
R147
24D9R2F-L-GP
1D5V_PCIE_S0
1D5V_PCIE_S0_R
PEG_RXN[15..0] 27
PEG_RXP[15..0] 27
PEG_TXN[15..0] 27
PEG_TXP[15..0] 27
R120
150R2F-1-GP
R121
150R2F-1-GP
R122
150R2F-1-GP
R346
150R2F-1-GP
R347
150R2F-1-GP
R350
150R2F-1-GP
RN27
SRN100KJ-6-GP
R366
1K5R2F-2-GP
R145
0R2J-2-GP
R140
255R2F-L-GP
RN17
Do Not Stuff
R114
Do Not Stuff
R142
Do Not Stuff
RN65
Do Not Stuff
RN66
Do Not Stuff
R344
Do Not Stuff
R349
Do Not Stuff
R124
Do Not Stuff
RN25
SRN10KJ-5-GP
RN23
Do Not Stuff
LCTLA_CLK
LCTLB_DATA
GMCH_HSYNC
GMCH_VSYNC
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Title
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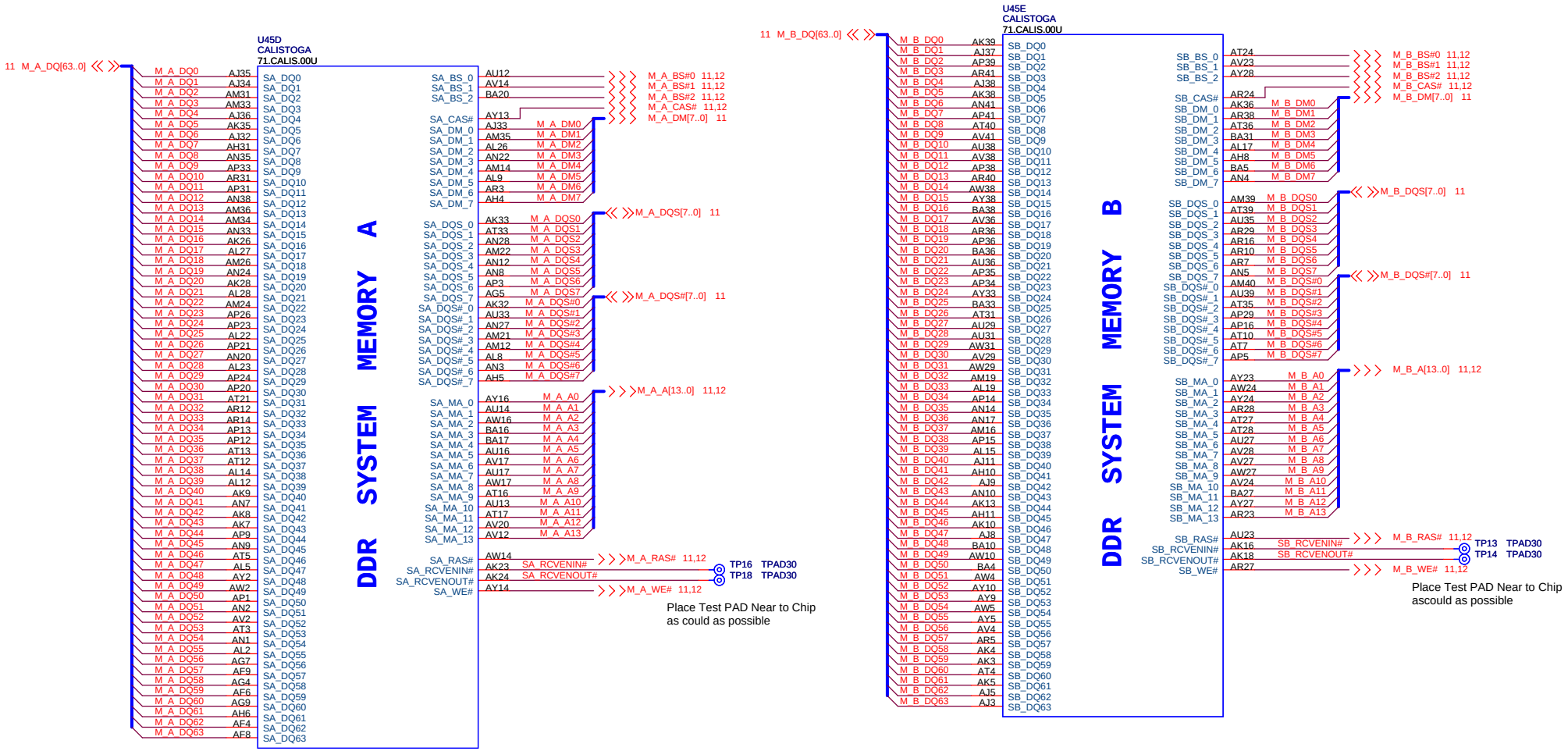
Size
Custom
Document Number
Dellen
Rev
SA
Date: Tuesday, January 16, 2007
Sheet 7 of 43



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Size: A3 | Document Number: Dellen | Rev: SA

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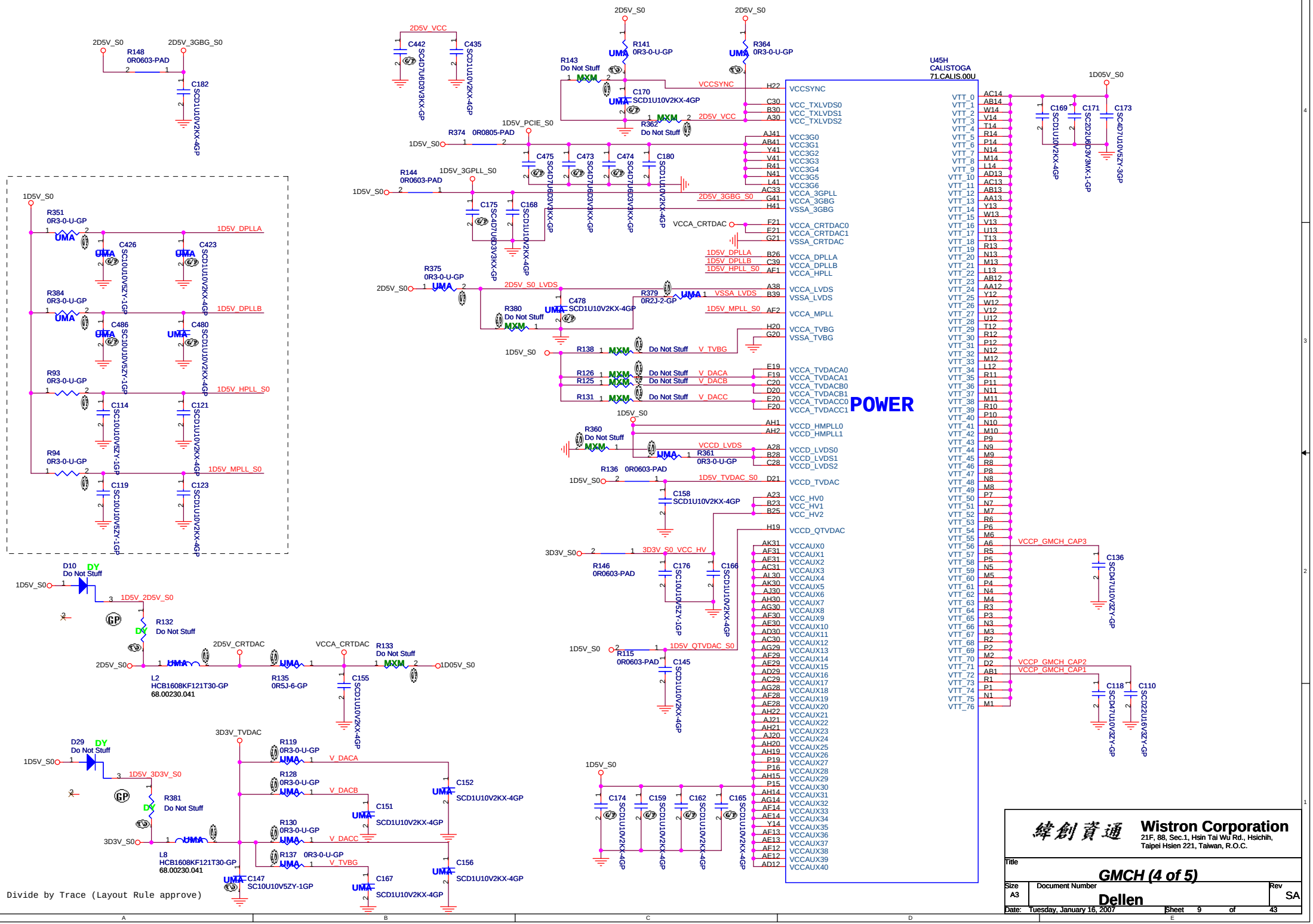
POWER
U45H
CALISTOGA
71.CALIS.00U
Divide by Trace (Layout Rule approve)
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Title
GMCH (4 of 5)
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Document Number
Dellen
Rev
SA
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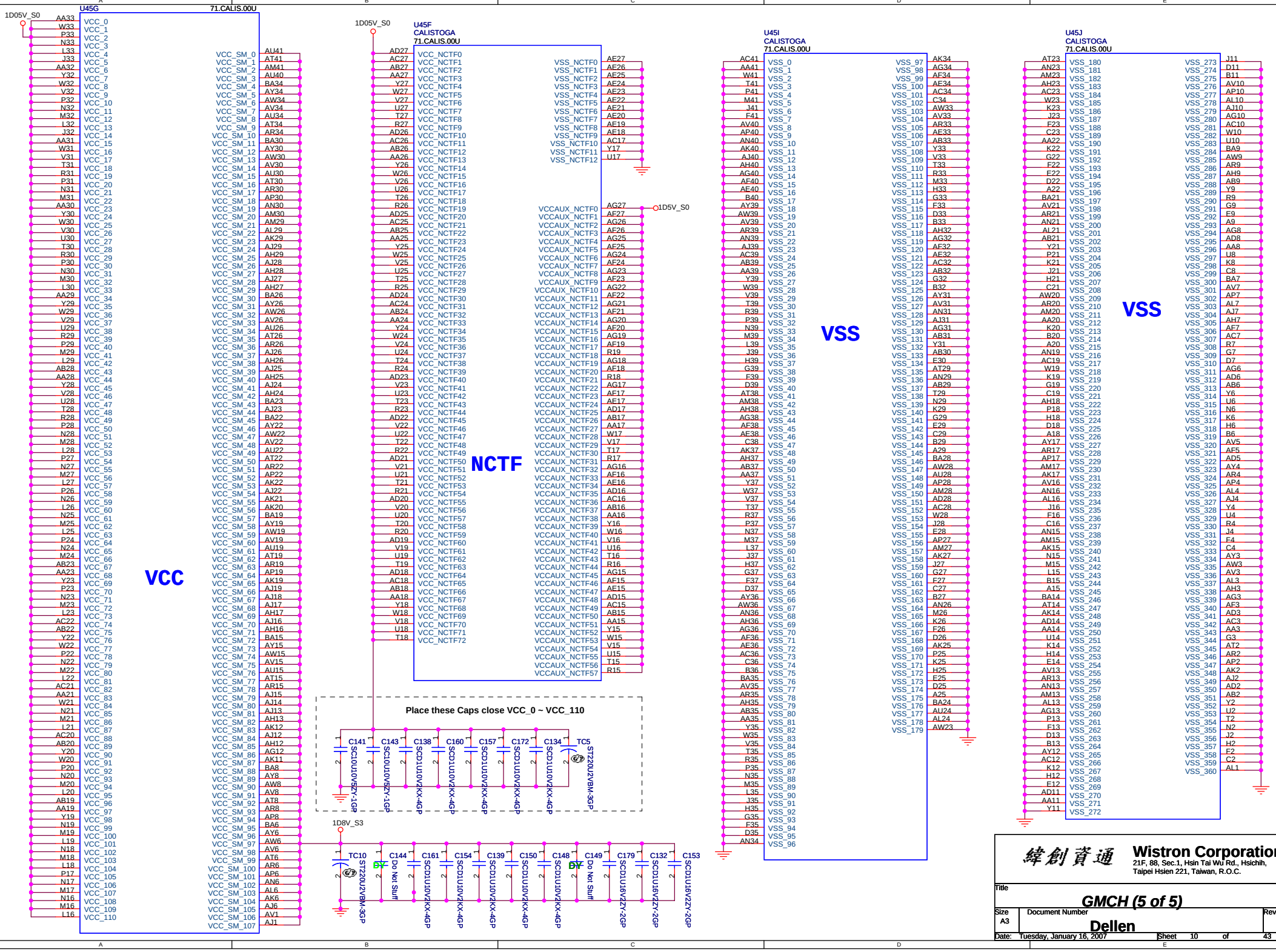
Sheet 9 of 43



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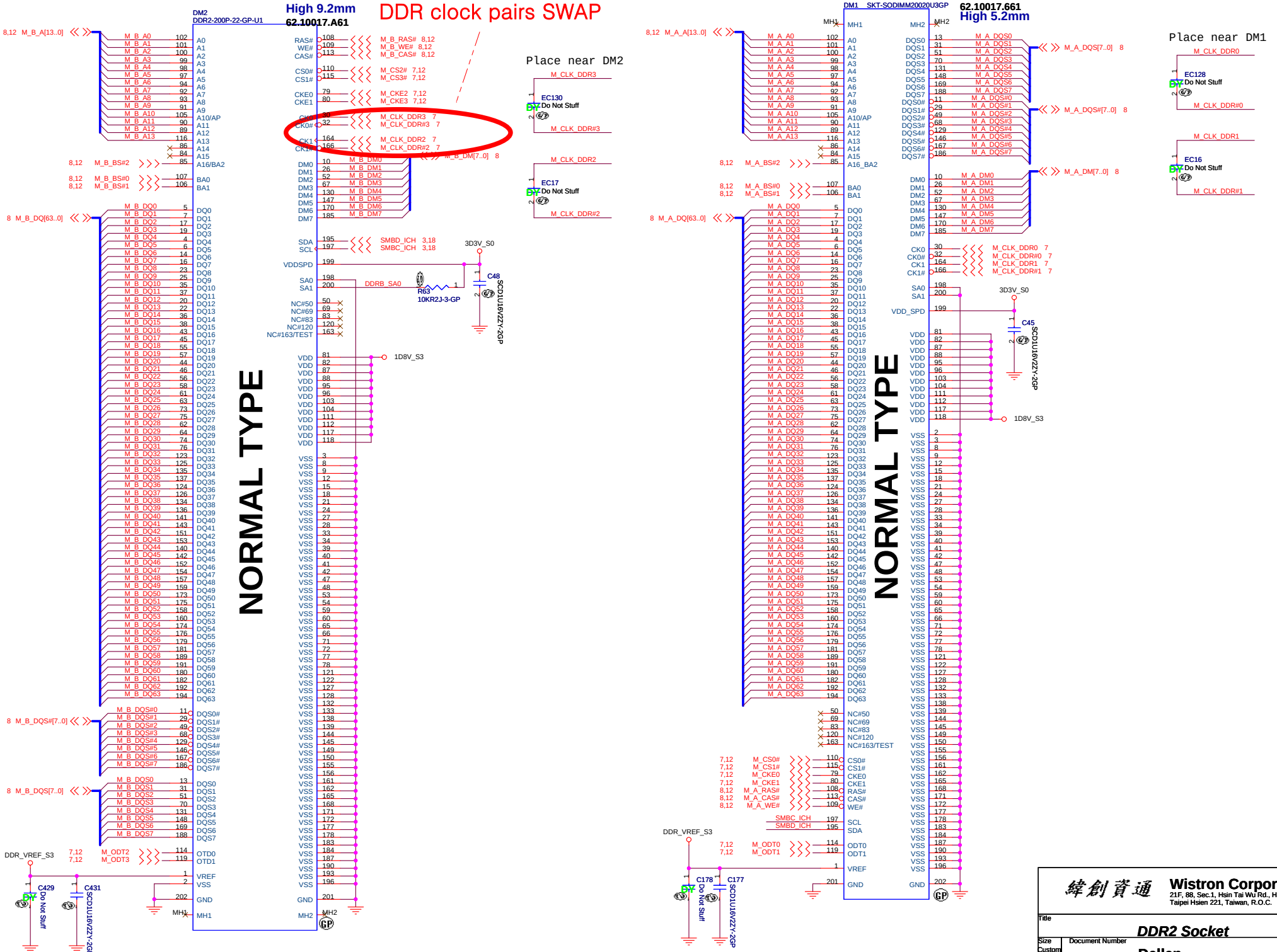
Title	GMCH (5 of 5)
Size A3	Document Number Dellen
Rev	SA
Date: Tuesday, January 16, 2007	Sheet 10 of 43


DM2
DDR2-200P-22-GP-U1
High 9.2mm
62.10017.A61
DDR clock pairs SWAP
NORMAL TYPE
Place near DM2
M_CLK_DDR3
EC130
DT
Do Not Stuff
M_CLK_DDR#3
M_CLK_DDR2
EC17
DT
Do Not Stuff
M_CLK_DDR#2
3D3V_S0
C48
SCD1U16V2ZY-2GP
R63
10KR2J-3-GP
DDRB_SA0
1D8V_S3
DDR_VREF_S3
C429
DT
Do Not Stuff
C431
SCD1U16V2ZY-2GP
DM1 SKT-SODIMM20020U3GP
62.10017.661
High 5.2mm
NORMAL TYPE
Place near DM1
M_CLK_DDR0
EC128
DT
Do Not Stuff
M_CLK_DDR#0
M_CLK_DDR1
EC16
DT
Do Not Stuff
M_CLK_DDR#1
C45
SCD1U16V2ZY-2GP
C178
DT
Do Not Stuff
C177
SCD1U16V2ZY-2GP
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Title
DDR2 Socket
Size
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Document Number
Dellen
Rev
SA
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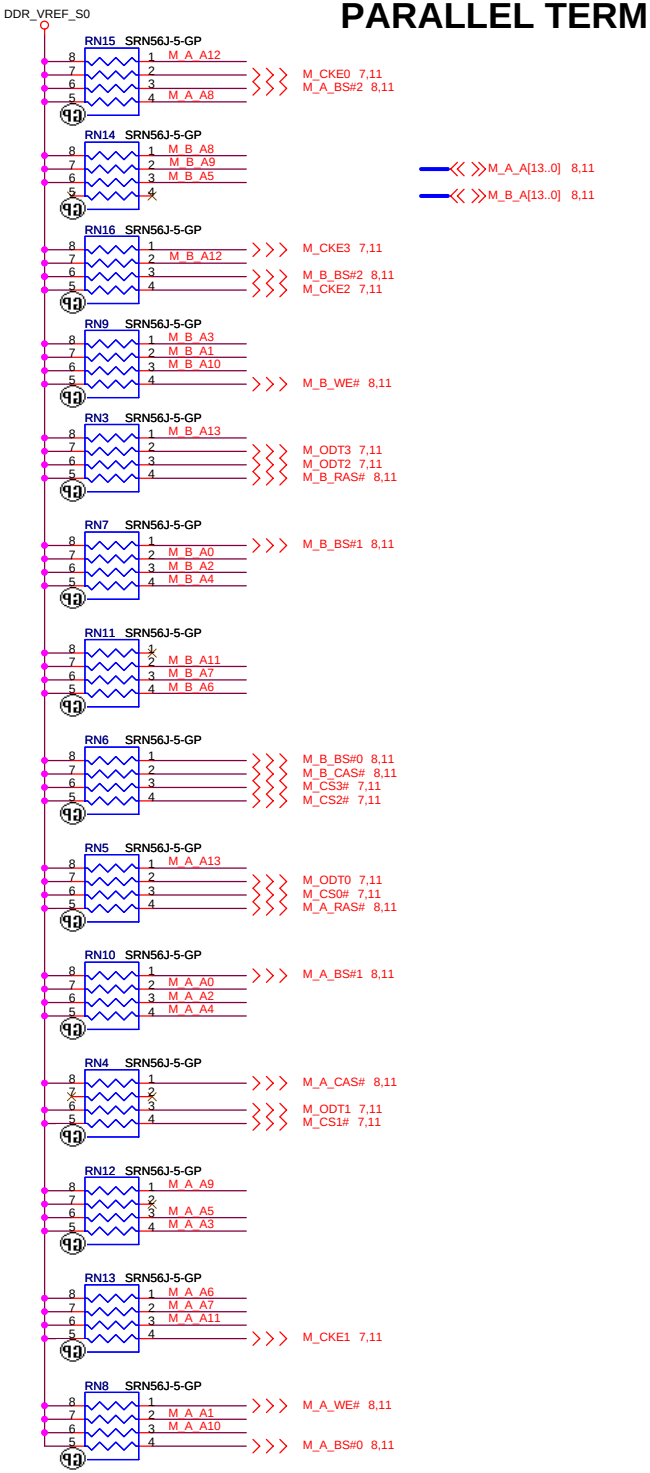
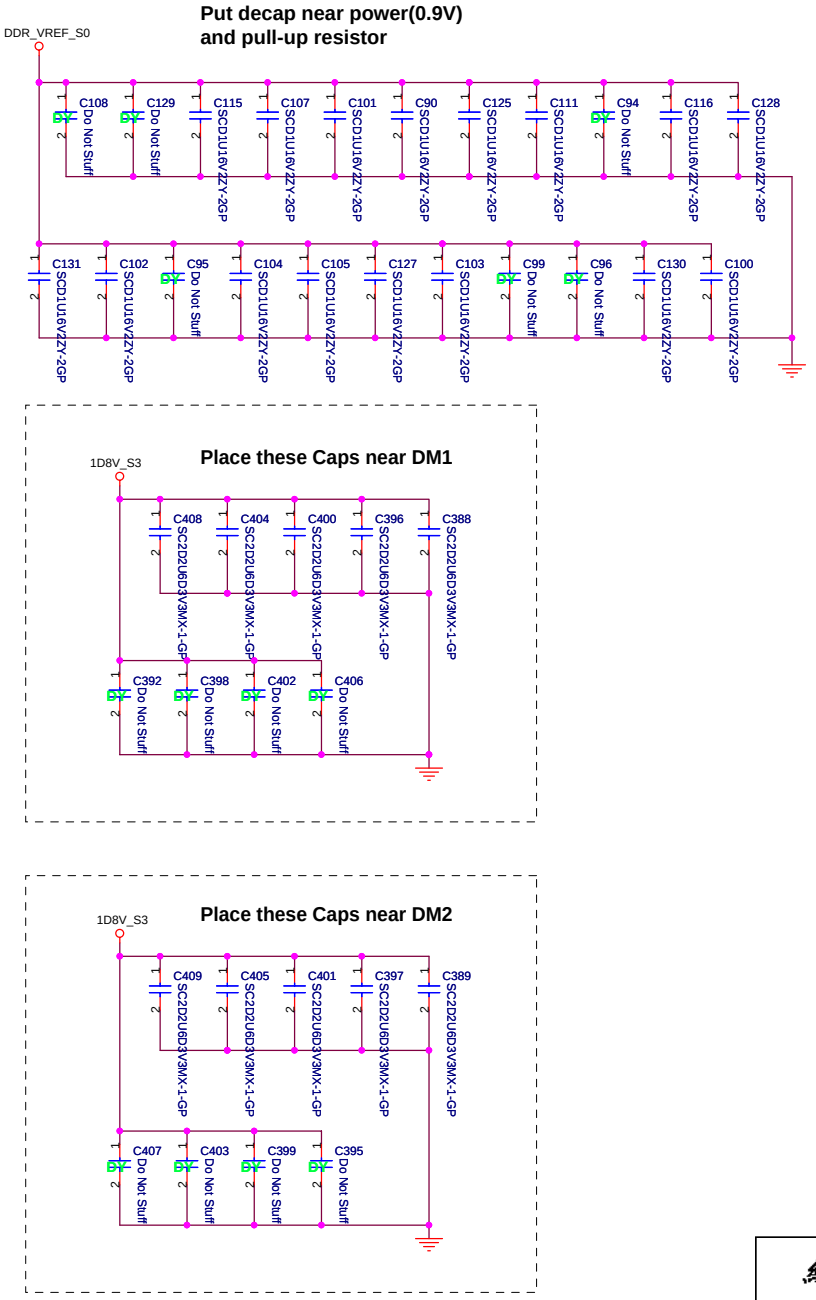
PARALLEL TERMINATION



Decoupling Capacitor



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Title: **DDR2 Termination Resistor**

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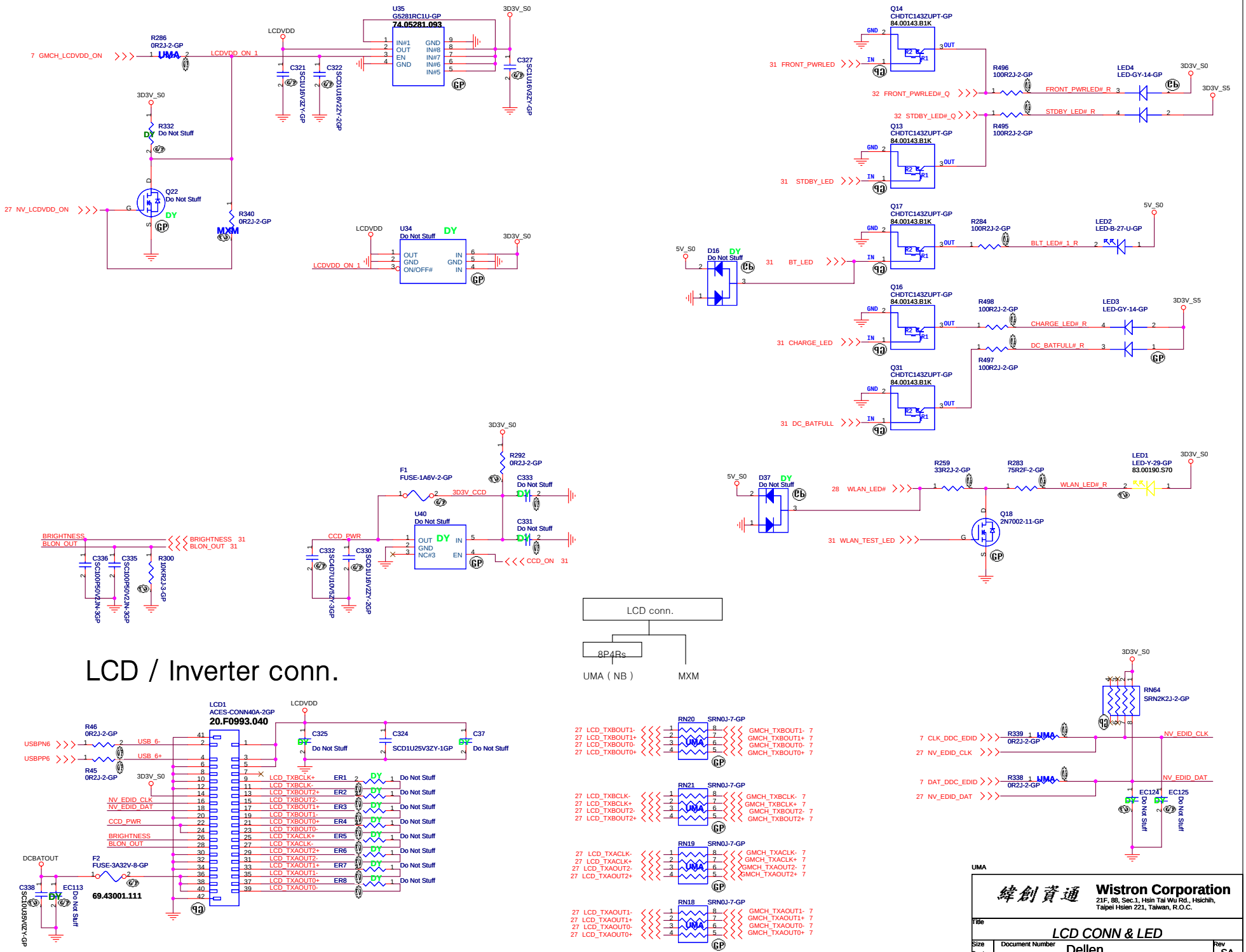
LCD / Inverter conn.
LCD conn.
8P4Rs
UMA (NB)
MXM
U35
G5281RC1U-GP
74.05281.093
U34
Do Not Stuff
LCDVDD
3D3V_S0
5V_S0
R286
0R2J-2-GP
R332
Do Not Stuff
Q22
Do Not Stuff
R340
0R2J-2-GP
C321
SCD1U16V2ZY-GP
C322
SCD1U16V2ZY-2GP
C327
SCD1U16V2ZY-GP
7 GMCH_LCDVDD_ON
LCDVDD_ON_1
27 NV_LCDVDD_ON
Q14
CHDTC143ZUPT-GP
84.00143.B1K
Q13
Q17
Q16
Q31
R496
100R2J-2-GP
R495
R284
100R2J-2-GP
R498
100R2J-2-GP
R497
100R2J-2-GP
LED4
LED-GY-14-GP
LED2
LED-B-27-U-GP
LED3
LED-GY-14-GP
3D3V_S5
31 FRONT_PWRLED
32 FRONT_PWRLED#_Q
32 STDBY_LED#_Q
31 STDBY_LED
FRONT_PWRLED#_R
STDBY_LED#_R
D16
Do Not Stuff
31 BT_LED
BLT_LED#_1_R
31 CHARGE_LED
CHARGE_LED#_R
DC_BATFULL#_R
31 DC_BATFULL
D37
Do Not Stuff
28 WLAN_LED#
WLAN_LED#_R
31 WLAN_TEST_LED
Q18
2N7002-11-GP
R259
33R2J-2-GP
R283
75R2F-2-GP
LED1
LED-Y-29-GP
83.00190.S70
F1
FUSE-1A6V-2-GP
3D3V_CCD
R292
0R2J-2-GP
C333
Do Not Stuff
C331
Do Not Stuff
U40
Do Not Stuff
CCD_PWR
CCD_ON 31
C332
SC4D7U10V5ZY-3GP
C330
SCD1U16V2ZY-2GP
BRIGHTNESS
BLON_OUT
BRIGHTNESS 31
BLON_OUT 31
C336
SC100P50V2JN-3GP
C335
SC100P50V2JN-3GP
R300
10KR2J-3-GP
LCD1
ACES-CONN40A-2GP
20.F0993.040
R46
0R2J-2-GP
R45
0R2J-2-GP
USBPN6
USBPP6
USB_6-
USB_6+
C325
Do Not Stuff
C324
SCD1U25V3ZY-1GP
C37
Do Not Stuff
LCD_TXBCLK+
LCD_TXBCLK-
LCD_TXBOUT2+
LCD_TXBOUT2-
LCD_TXBOUT1+
LCD_TXBOUT1-
LCD_TXBOUT0+
LCD_TXBOUT0-
LCD_TXACLK+
LCD_TXACLK-
LCD_TXAOUT2+
LCD_TXAOUT2-
LCD_TXAOUT1+
LCD_TXAOUT1-
LCD_TXAOUT0+
LCD_TXAOUT0-
ER1
ER2
ER3
ER4
ER5
ER6
ER7
ER8
NV_EDID_CLK
NV_EDID_DAT
CCD_PWR
BRIGHTNESS
BLON_OUT
DCBATOUT
F2
FUSE-3A32V-8-GP
69.43001.111
C338
SCD1U35V3ZY-GP
EC113
Do Not Stuff
RN20
RN21
RN19
RN18
SRN0J-7-GP
GMCH_TXBOUT1-
GMCH_TXBOUT1+
GMCH_TXBOUT0-
GMCH_TXBOUT0+
GMCH_TXBCLK-
GMCH_TXBCLK+
GMCH_TXBOUT2-
GMCH_TXBOUT2+
GMCH_TXACLK-
GMCH_TXACLK+
GMCH_TXAOUT2-
GMCH_TXAOUT2+
GMCH_TXAOUT1-
GMCH_TXAOUT1+
GMCH_TXAOUT0-
GMCH_TXAOUT0+
RN64
SRN2K2J-2-GP
7 CLK_DDC_EDID
27 NV_EDID_CLK
7 DAT_DDC_EDID
27 NV_EDID_DAT
R339
0R2J-2-GP
R338
0R2J-2-GP
EC124
EC125
Do Not Stuff
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
LCD CONN & LED
Size
Custom
Document Number
Dellen
Rev
SA
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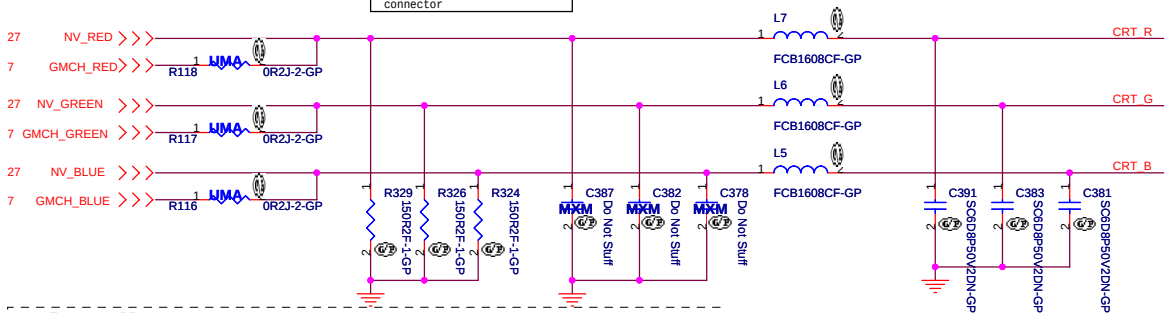
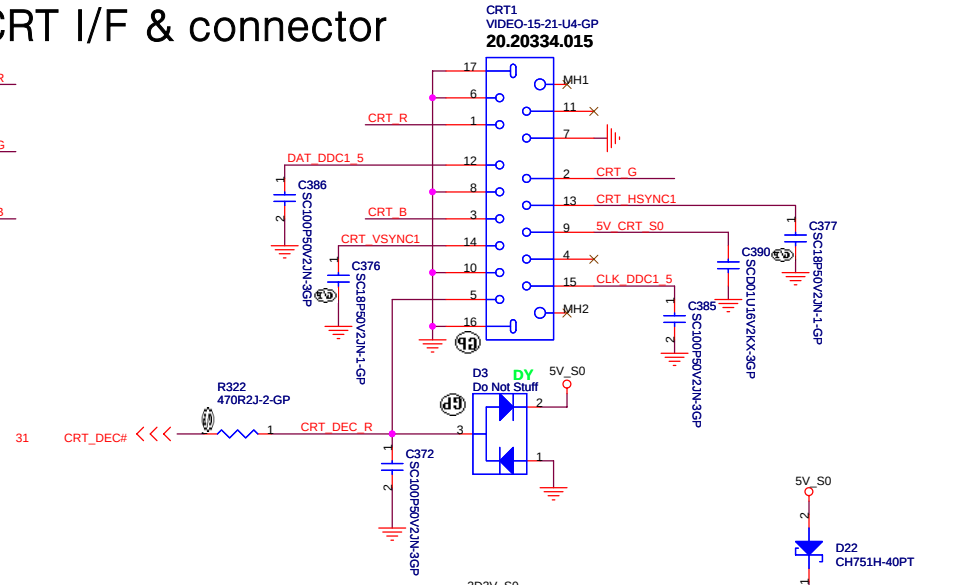
CRT I/F & connector

Layout Note:
Place these resistors close to the CRT-out connector

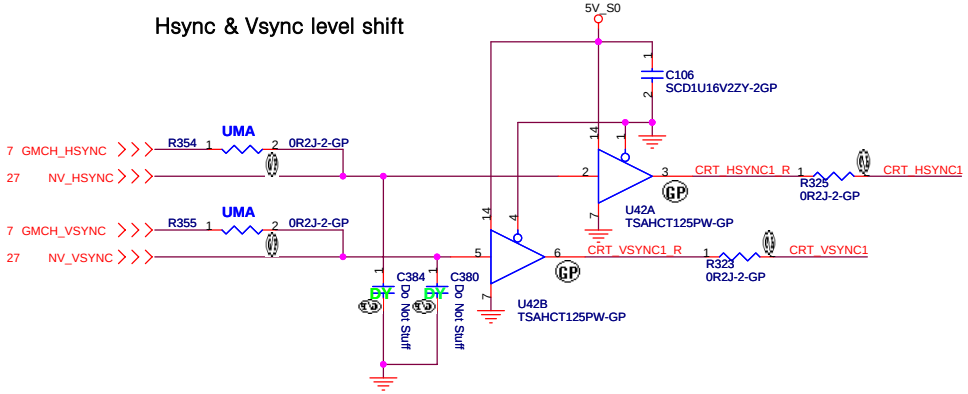
Ferrite bead impedance: 10 ohm@100MHz



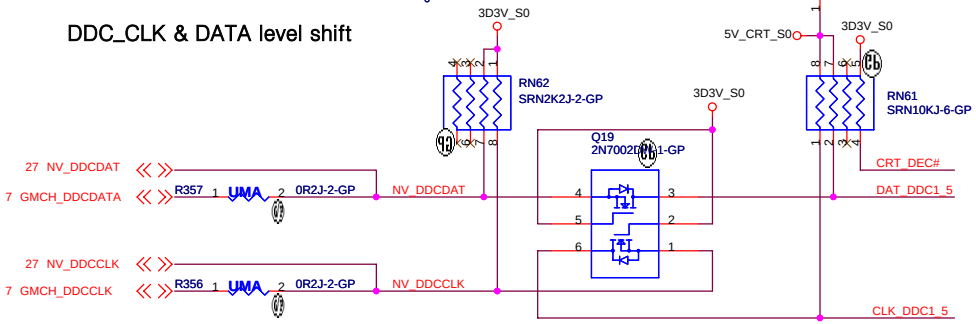
Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



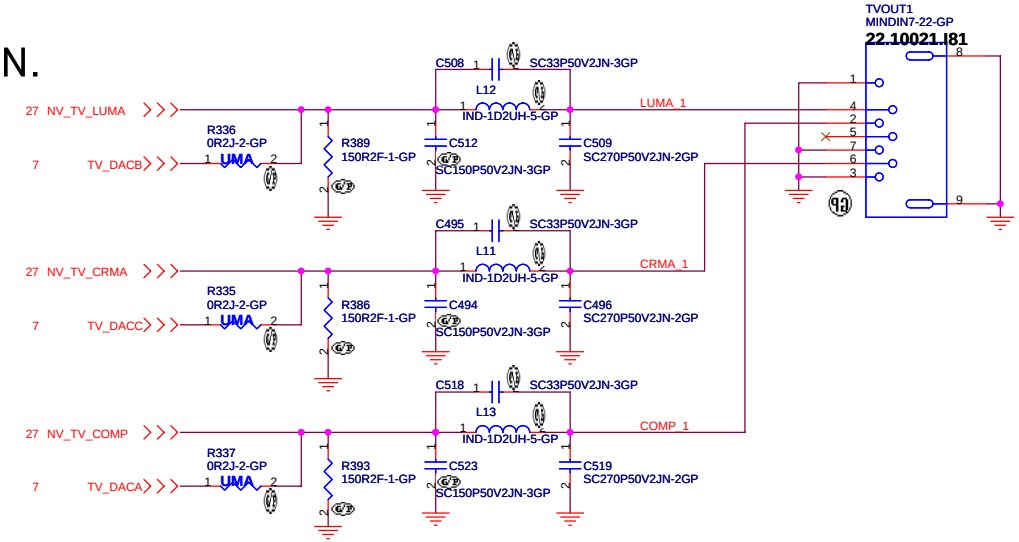
Hsync & Vsync level shift

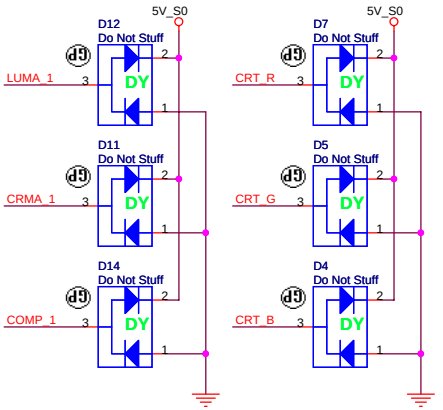


DDC_CLK & DATA level shift



TV CONN.





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Title: *CRT/TV Connector*

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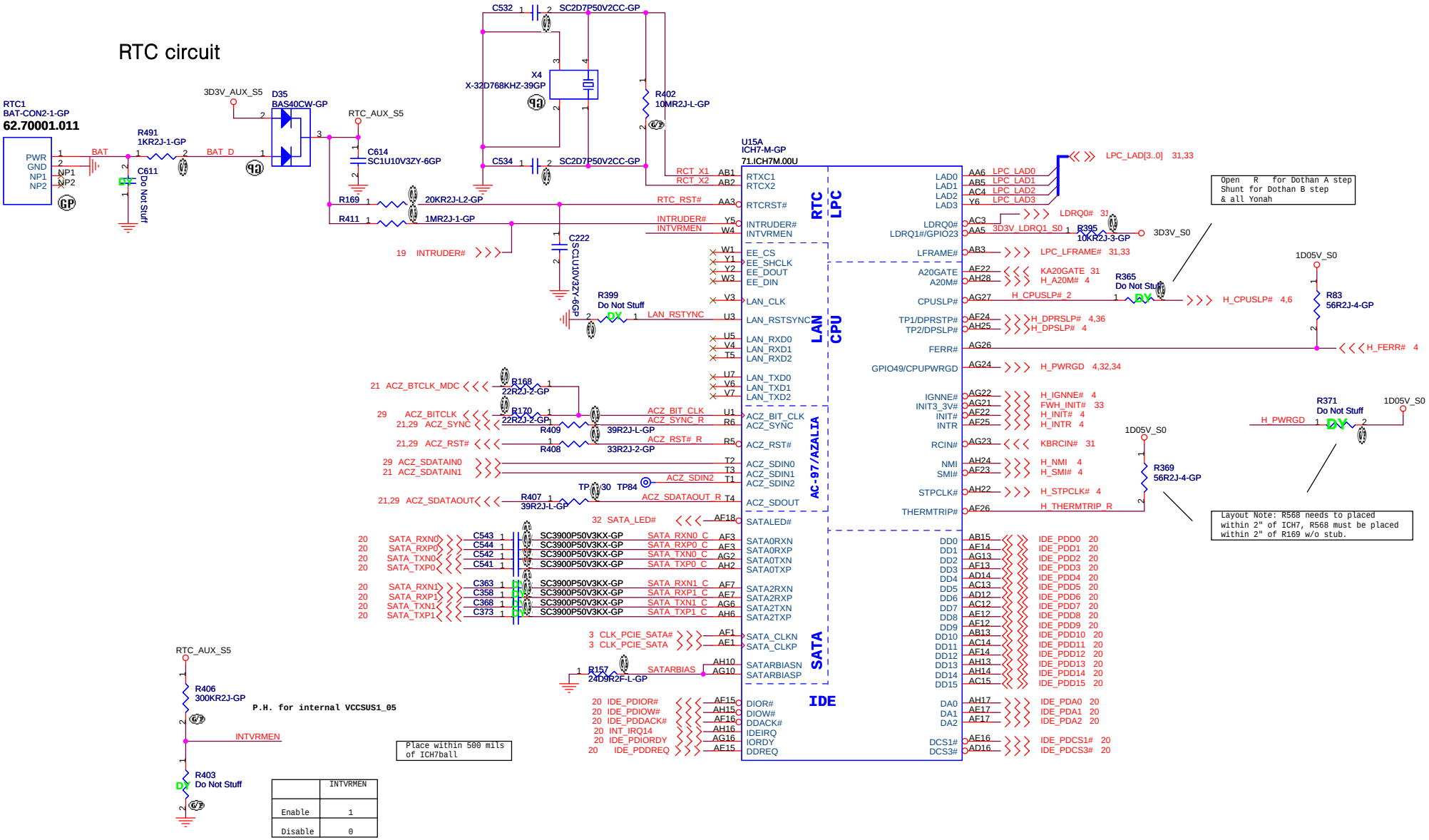
RTC circuit



UMA

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Title: *ICH7-M (1 of 4)*

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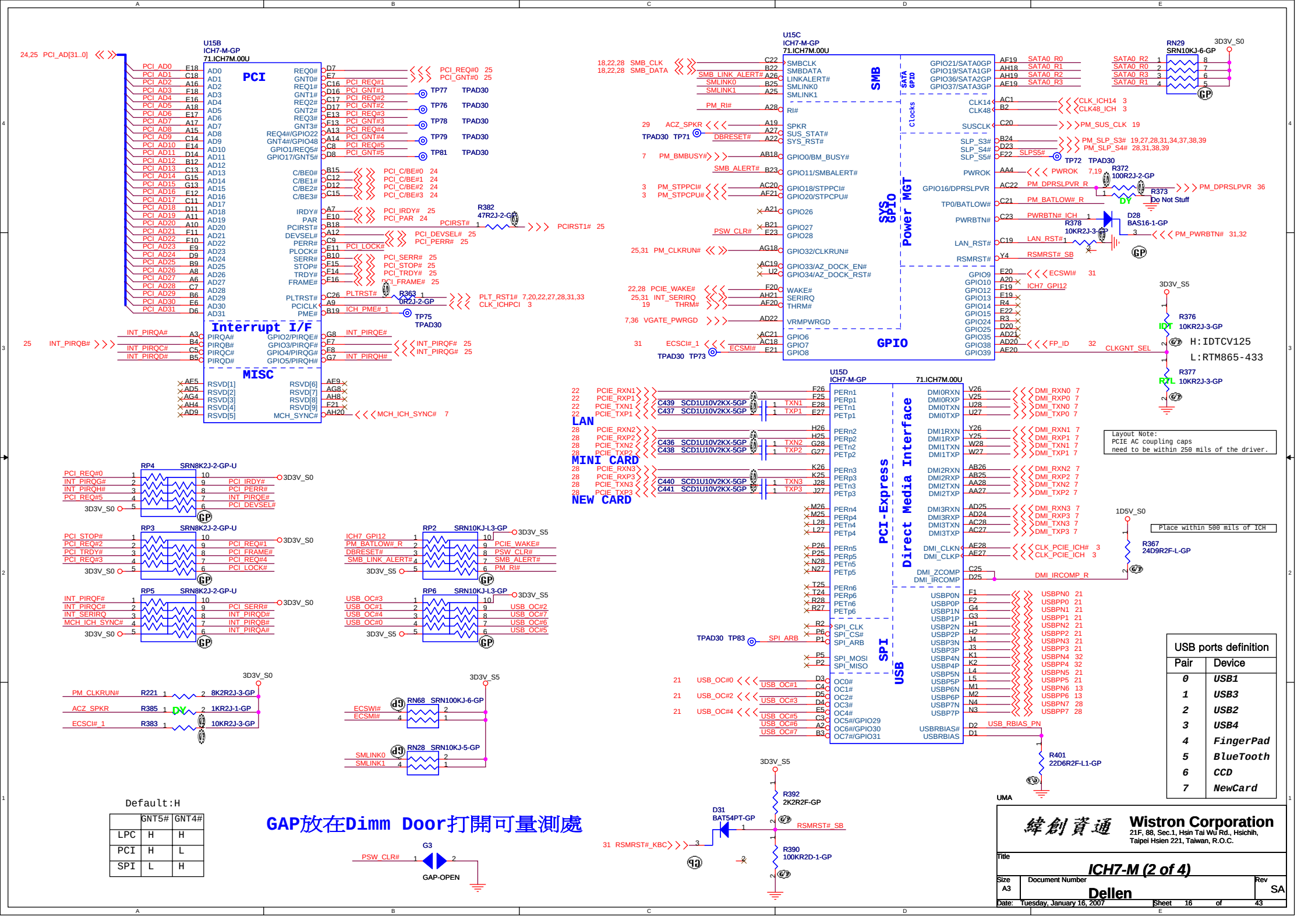
U15B
ICH7-M-GP
71.ICH7M.00U
PCI
Interrupt I/F
MISC
U15C
SMB
SYS GPIO
Power MGT
GPIO
U15D
PCI-Express
Direct Media Interface
SPI
USB
LAN
MINI CARD
NEW CARD
GAP放在Dimm Door打開可量測處
GAP-OPEN
Default:H
GNT5# GNT4#
LPC H H
PCI H L
SPI L H
USB ports definition
Pair Device
0 USB1
1 USB3
2 USB2
3 USB4
4 FingerPad
5 BlueTooth
6 CCD
7 NewCard
Layout Note:
PCIE AC coupling caps
need to be within 250 mils of the driver.
Place within 500 mils of ICH
H:IDTCV125
L:RTM865-433
UMA
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Title
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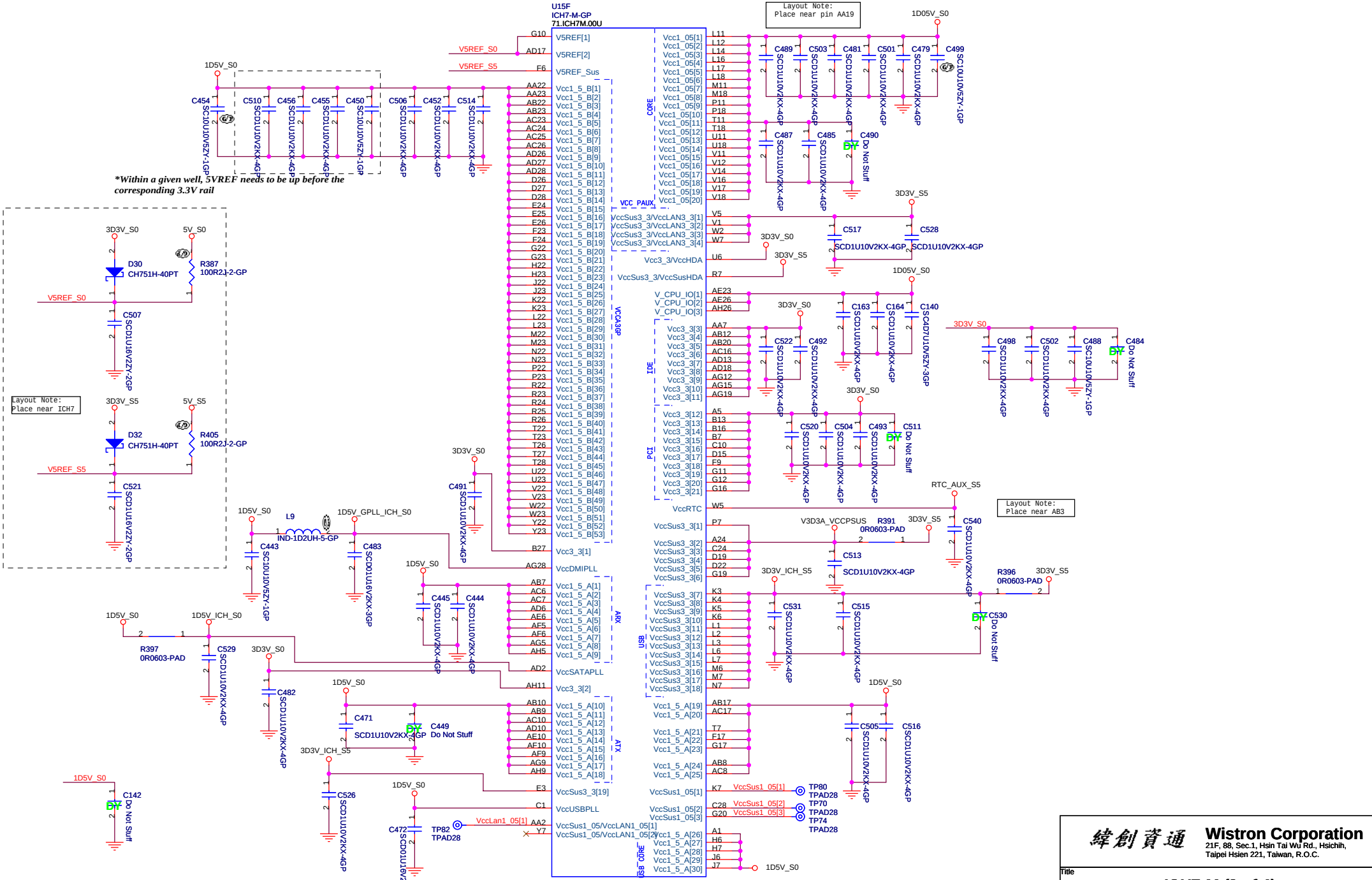
U15F
ICH7-M-GP
71.ICH7M.00U
Layout Note:
Place near pin AA19
Layout Note:
Place near ICH7
Layout Note:
Place near AB3
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
V5REF_S0
V5REF_S5
1D05V_S0
3D3V_S0
3D3V_S5
5V_S0
5V_S5
3D3V_ICH_S5
1D5V_S0
1D5V_ICH_S0
1D5V_GPLL_ICH_S0
RTC_AUX_S5
V3D3A_VCCPSUS
VccLan1_05[1]
VccSus1_05[1]
VccSus1_05[2]
VccSus1_05[3]
D30
CH751H-40PT
D32
CH751H-40PT
R387
100R2J-2-GP
R405
100R2J-2-GP
L9
IND-1D2UH-5-GP
R391
0R0603-PAD
R396
0R0603-PAD
R397
0R0603-PAD
TP80
TPAD28
TP70
TPAD28
TP74
TPAD28
TP82
TPAD28
Do Not Stuff
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
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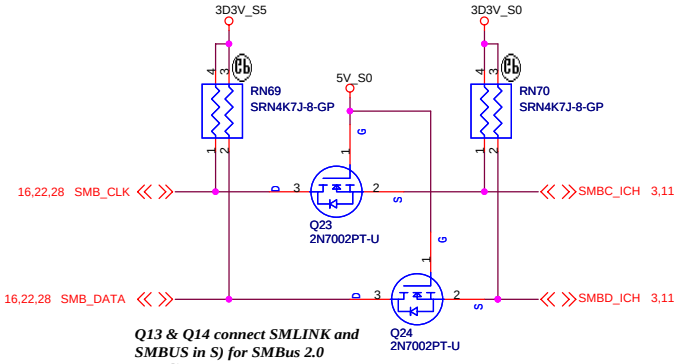
U15E
ICH7-M-GP
71.ICH7M.00U

A4	VSS[1]	VSS[98]	P28
A23	VSS[2]	VSS[99]	R1
B1	VSS[3]	VSS[100]	R11
B8	VSS[4]	VSS[101]	R12
B11	VSS[5]	VSS[102]	R13
B14	VSS[6]	VSS[103]	R14
B17	VSS[7]	VSS[104]	R15
B20	VSS[8]	VSS[105]	R16
B26	VSS[9]	VSS[106]	R17
B28	VSS[10]	VSS[107]	R18
C2	VSS[11]	VSS[108]	T6
C6	VSS[12]	VSS[109]	T12
C27	VSS[13]	VSS[110]	T13
D10	VSS[14]	VSS[111]	T14
D13	VSS[15]	VSS[112]	T15
D18	VSS[16]	VSS[113]	T16
D21	VSS[17]	VSS[114]	T17
D24	VSS[18]	VSS[115]	U4
E1	VSS[19]	VSS[116]	U12
E2	VSS[20]	VSS[117]	U13
E4	VSS[21]	VSS[118]	U14
E8	VSS[22]	VSS[119]	U15
E15	VSS[23]	VSS[120]	U16
F3	VSS[24]	VSS[121]	U17
F4	VSS[25]	VSS[122]	U24
F5	VSS[26]	VSS[123]	U25
F12	VSS[27]	VSS[124]	U26
F27	VSS[28]	VSS[125]	V2
F28	VSS[29]	VSS[126]	V13
G1	VSS[30]	VSS[127]	V15
G2	VSS[31]	VSS[128]	V24
G5	VSS[32]	VSS[129]	V27
G6	VSS[33]	VSS[130]	V28
G9	VSS[34]	VSS[131]	W6
G14	VSS[35]	VSS[132]	W24
G18	VSS[36]	VSS[133]	W25
G21	VSS[37]	VSS[134]	W26
G24	VSS[38]	VSS[135]	Y3
G25	VSS[39]	VSS[136]	Y24
G26	VSS[40]	VSS[137]	Y27
H3	VSS[41]	VSS[138]	Y28
H4	VSS[42]	VSS[139]	AA1
H5	VSS[43]	VSS[140]	AA24
H24	VSS[44]	VSS[141]	AA25
H27	VSS[45]	VSS[142]	AA26
H28	VSS[46]	VSS[143]	AB4
J1	VSS[47]	VSS[144]	AB6
J2	VSS[48]	VSS[145]	AB11
J5	VSS[49]	VSS[146]	AB14
J24	VSS[50]	VSS[147]	AB16
J25	VSS[51]	VSS[148]	AB19
J26	VSS[52]	VSS[149]	AB21
K24	VSS[53]	VSS[150]	AB24
K27	VSS[54]	VSS[151]	AB27
K28	VSS[55]	VSS[152]	AB28
L13	VSS[56]	VSS[153]	AC2
L15	VSS[57]	VSS[154]	AC5
L24	VSS[58]	VSS[155]	AC9
L25	VSS[59]	VSS[156]	AC11
L26	VSS[60]	VSS[157]	AD1
M3	VSS[61]	VSS[158]	AD3
M4	VSS[62]	VSS[159]	AD4
M5	VSS[63]	VSS[160]	AD7
M12	VSS[64]	VSS[161]	AD8
M13	VSS[65]	VSS[162]	AD11
M14	VSS[66]	VSS[163]	AD15
M15	VSS[67]	VSS[164]	AD19
M16	VSS[68]	VSS[165]	AD23
M17	VSS[69]	VSS[166]	AE2
M24	VSS[70]	VSS[167]	AE4
M27	VSS[71]	VSS[168]	AE8
M28	VSS[72]	VSS[169]	AE11
N1	VSS[73]	VSS[170]	AE13
N2	VSS[74]	VSS[171]	AE18
N5	VSS[75]	VSS[172]	AE21
N6	VSS[76]	VSS[173]	AE24
N11	VSS[77]	VSS[174]	AE25
N12	VSS[78]	VSS[175]	AF2
N13	VSS[79]	VSS[176]	AF4
N14	VSS[80]	VSS[177]	AF8
N15	VSS[81]	VSS[178]	AF11
N16	VSS[82]	VSS[179]	AF27
N17	VSS[83]	VSS[180]	AF28
N18	VSS[84]	VSS[181]	AG1
N24	VSS[85]	VSS[182]	AG3
N25	VSS[86]	VSS[183]	AG7
N26	VSS[87]	VSS[184]	AG11
P3	VSS[88]	VSS[185]	AG14
P4	VSS[89]	VSS[186]	AG17
P12	VSS[90]	VSS[187]	AG20
P13	VSS[91]	VSS[188]	AG25
P14	VSS[92]	VSS[189]	AH1
P15	VSS[93]	VSS[190]	AH3
P16	VSS[94]	VSS[191]	AH7
P17	VSS[95]	VSS[192]	AH12
P24	VSS[96]	VSS[193]	AH23
P27	VSS[97]	VSS[194]	AH27

SMBUS



Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

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Title: ***ICH7-M (4 of 4)***

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TEMP.	Digital Output Data Bits			
	Sign	MSB	LSB	EXT
+127.875	0	111	1111	111
+126.375	0	111	1110	011
+25.5	0	001	1001	100
+1.75	0	000	0001	110
+0.5	0	000	0000	100
+0.125	0	000	0000	001
-0.125	1	111	1111	111
-1.125	1	111	1110	111
-25.5	1	110	0110	100
-55.25	1	100	1000	110
-65.000	1	011	1111	000

Layout 15 mil

Layout 15 mil

Layout 30 mil

3.HW T8 sensor

2.System Sensor, Put between CPU and NB.

1.For CPU Sensor

Setting T8 as 90 Degree

V_DEGREE =(((Degree-72)*0.02)+0.34)*VCC

DXP1:108 Degree (CPU)
DXP2:H/W Setting 100(System)
DXP3:105 Degree (SYSTEM)

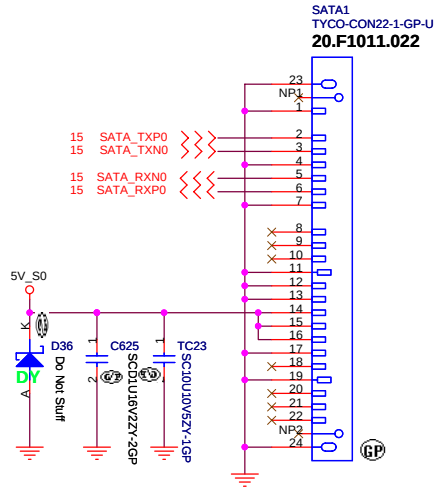
Place near chip as close as possible

32K suspend clock output

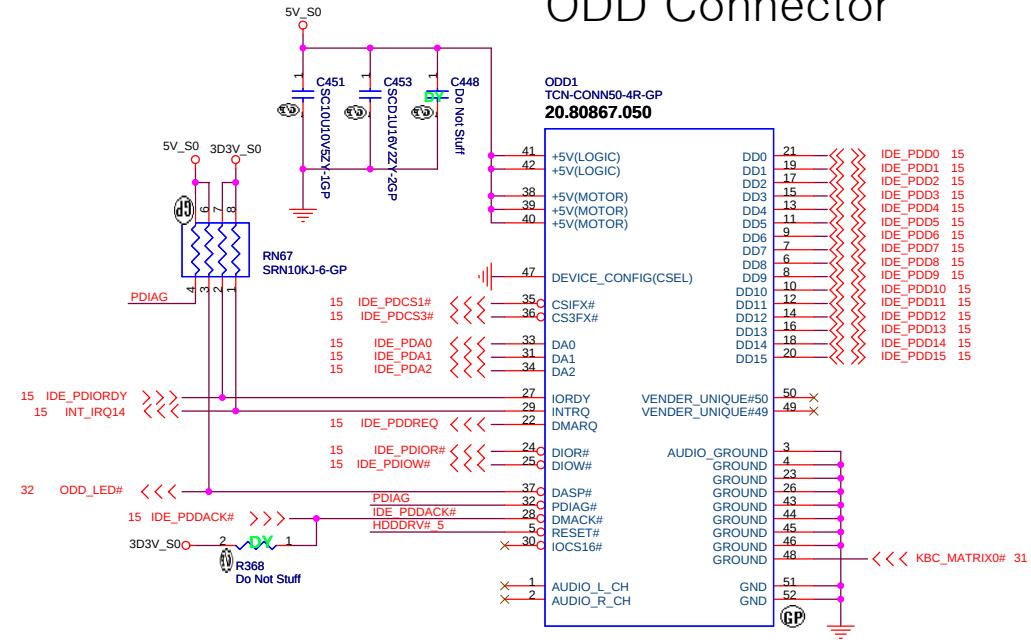
Output type: Open-Drain RESET#

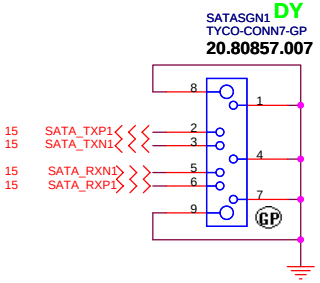
Wistron Corporation	Title: Thermal / Fan Controllor		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	Size: A3	Document Number: Dellen	Rev: SA
	Date: Tuesday, January 16, 2007	Sheet 19 of 43	

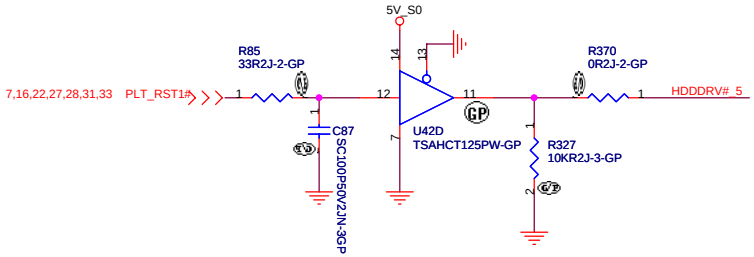
SATA HD Connector

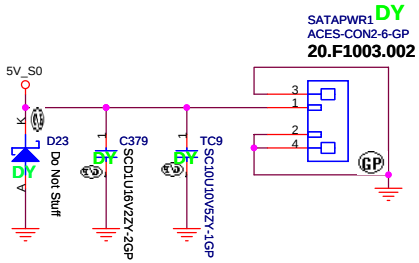


ODD Connector









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Title: ***HDD and CDROM***

Size	Document Number	Rev
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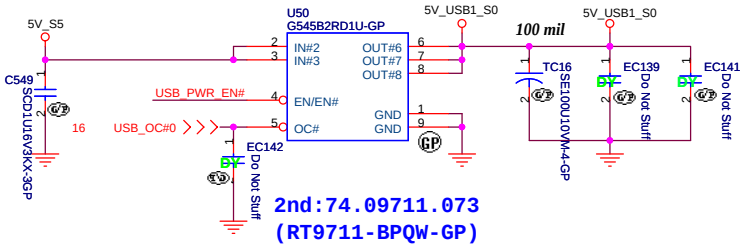
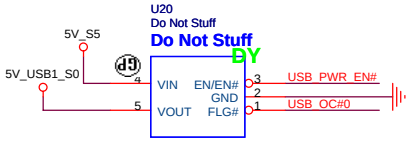
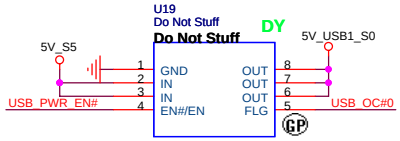
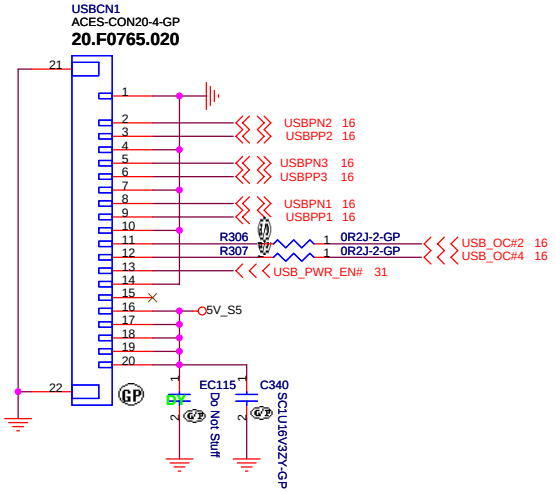
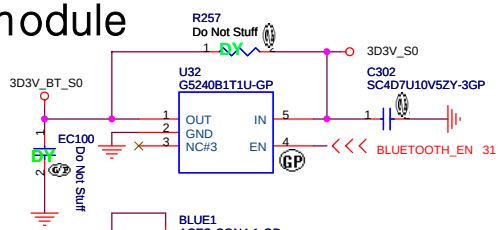


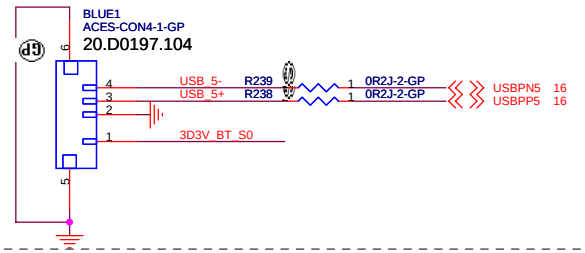




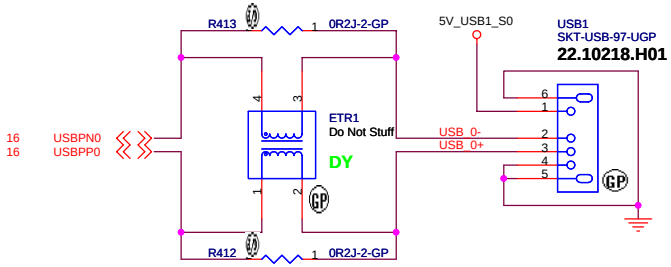


Bluetooth module

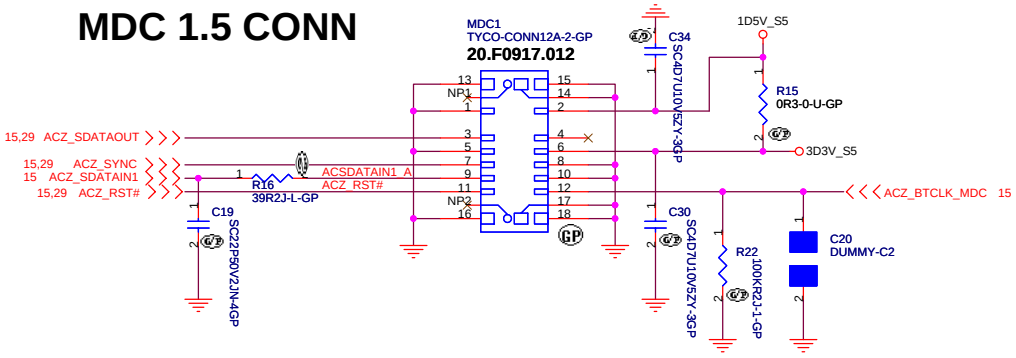


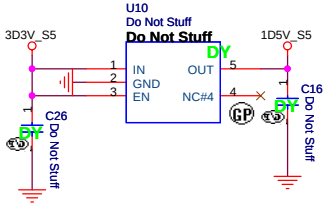


EC21 put near BLUE1 / all USB put one choke near connector by EMI request



MDC 1.5 CONN





UMA

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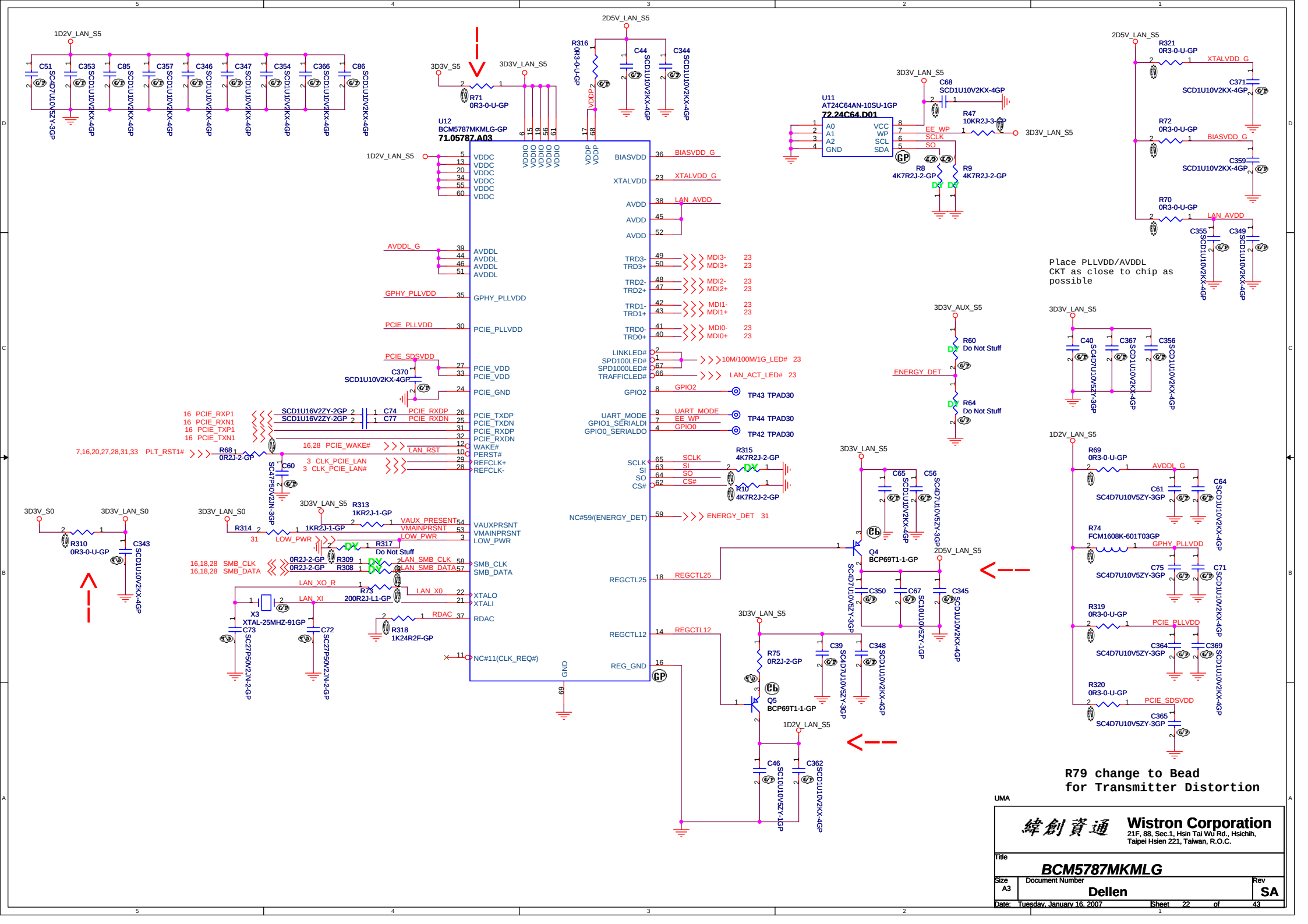
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB / MDC / BLUETOOTH

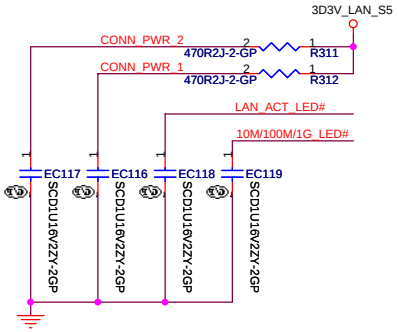
Size	Document Number	Rev
A3	Dellen	SA

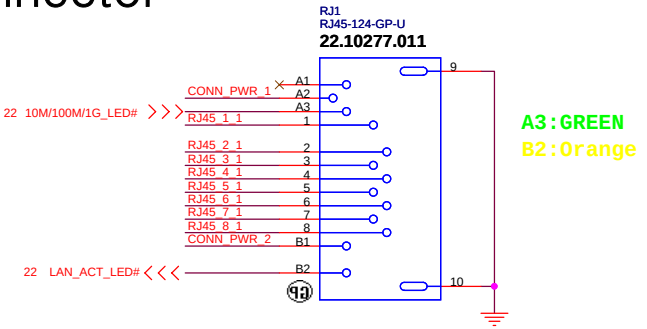
Date: Tuesday, January 16, 2007 Sheet 21 of 43


U12
BCM5787MKMLG-GP
71.05787.A03
U11
AT24C64AN-10SU-1GP
72.24C64.D01
Place PLLVDD/AVDDL
CKT as close to chip as
possible
R79 change to Bead
for Transmitter Distortion
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
BCM5787MKMLG
Size
A3
Document Number
Dellen
Rev
SA
Date: Tuesday, January 16, 2007
Sheet 22 of 43

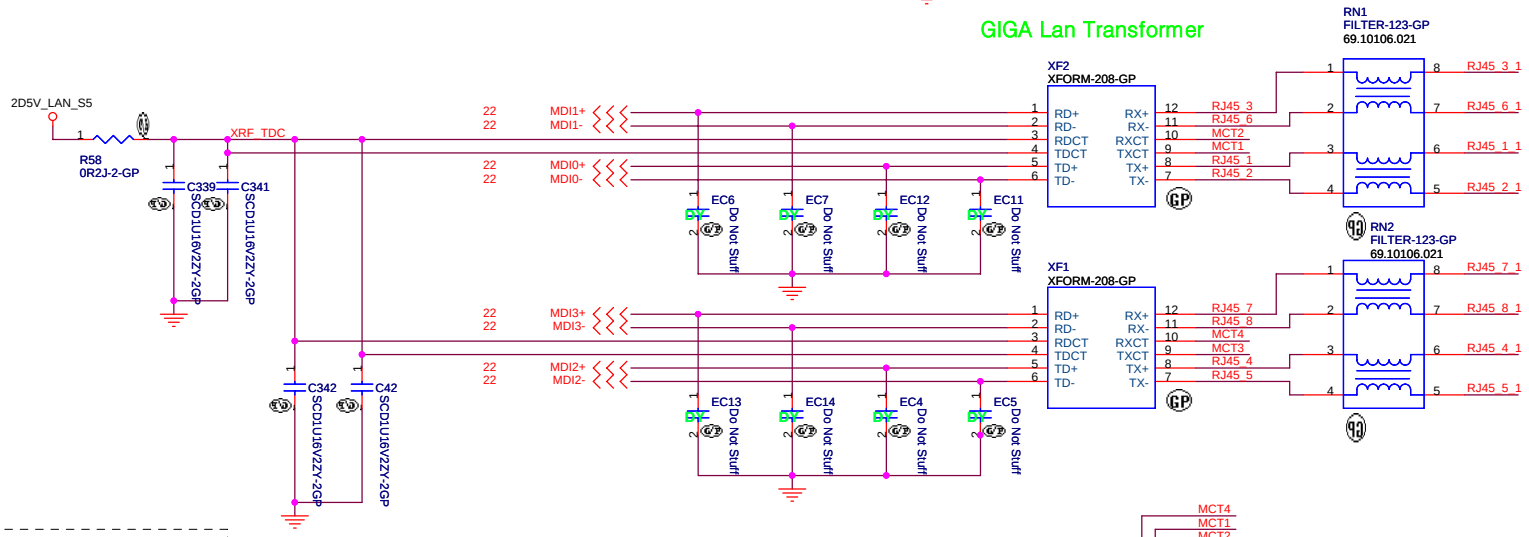
LAN Connector

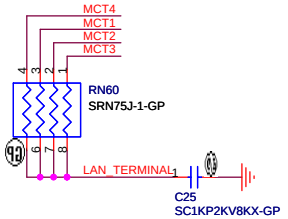
Voltage Rail	4401E	5789	5787
VDDIO_PCI	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDC	1D8V_LAN_S5	1D2V_LAN_S5	
VDDIO	3D3V_LAN_S5	3D3V_LAN_S5	
VESD	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDP	Don't Care	2D5V_S5	
3D3V_2D5V_S5	3D3V_S5	2D5V_S5	
1D8V_1D2V_S5	1D8V_LAN_S5	1D2V_S5	





GIGA Lan Transformer





LAN Link: Green(A3), behavior is the same for 10/100/1000 bits

LAN Data: Yellow(B2), when LAN is transfering data.

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

UMA

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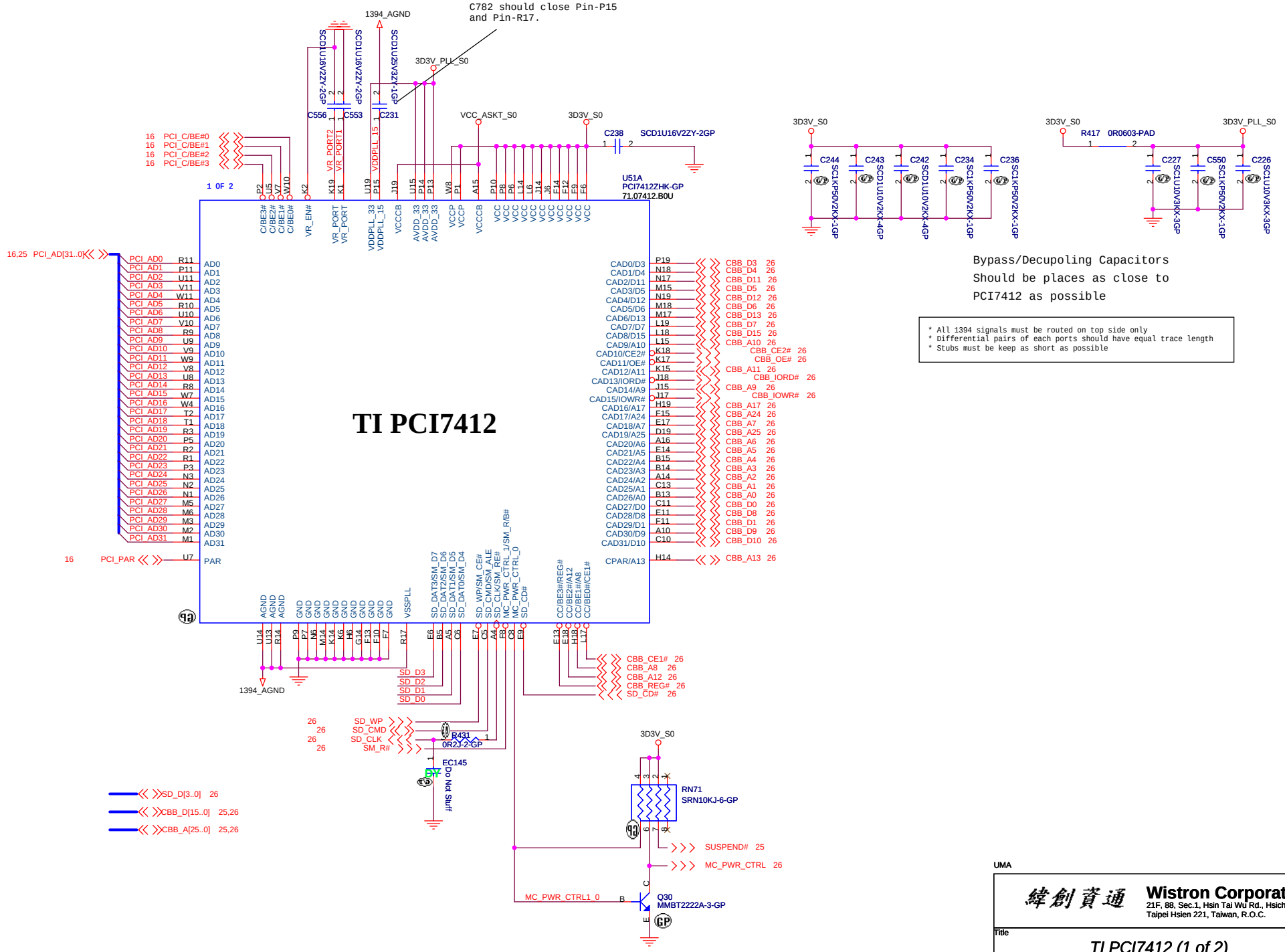
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN Connector**

Size	Document Number	Rev
A3	Dellen	SA

Date: Tuesday, January 16, 2007 Sheet 23 of 43



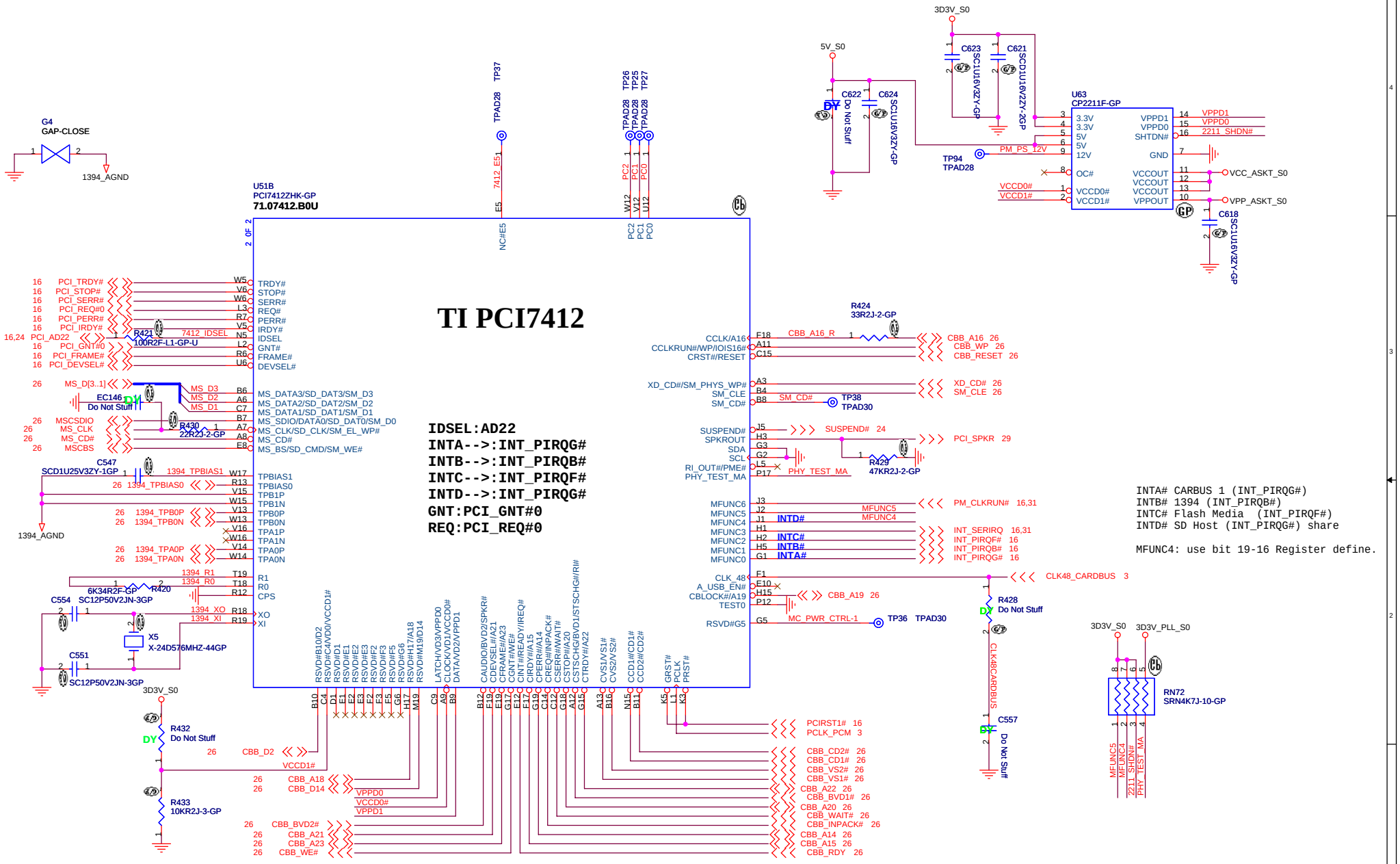
UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *TI PCI7412 (1 of 2)*

Size	Document Number	Rev
A3	Dellen	SA

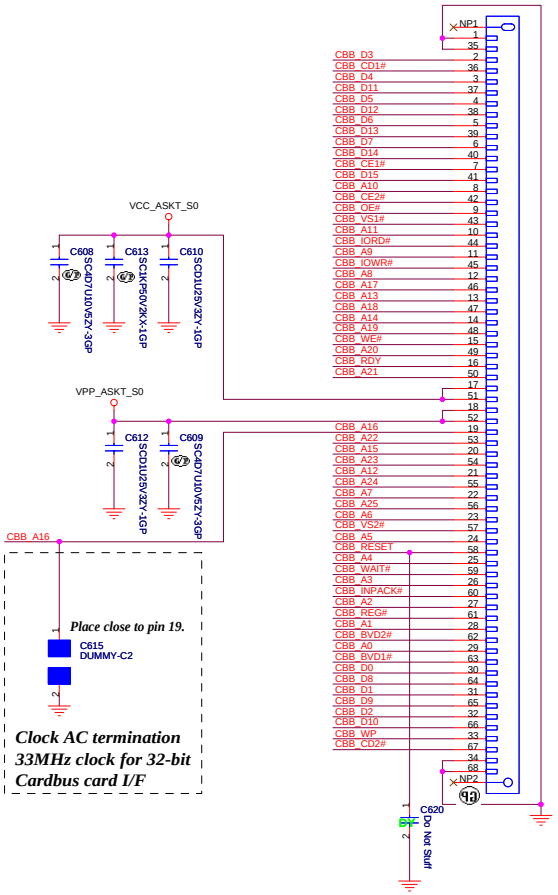
Date: Tuesday, January 16, 2007 Sheet 24 of 43



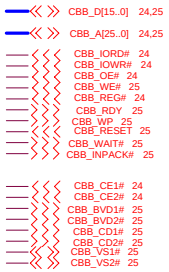
UMA

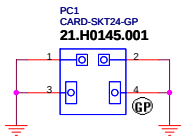
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	TI PCI7412 (2 of 2)	
Size A3	Document Number Dellen	Rev SA
Date: Tuesday, January 16, 2007	Sheet 25 of 43	

PCMCIA Socket

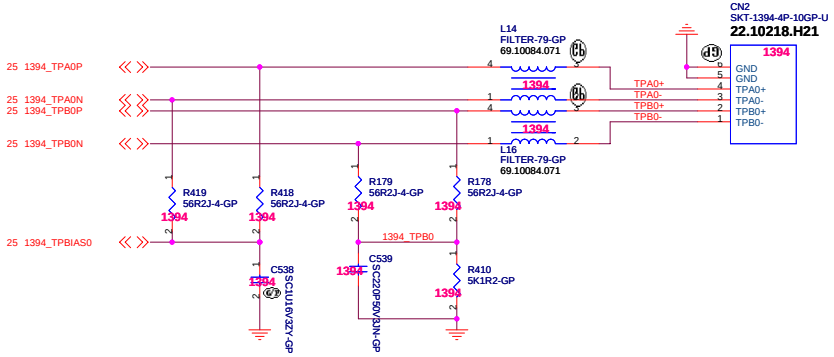


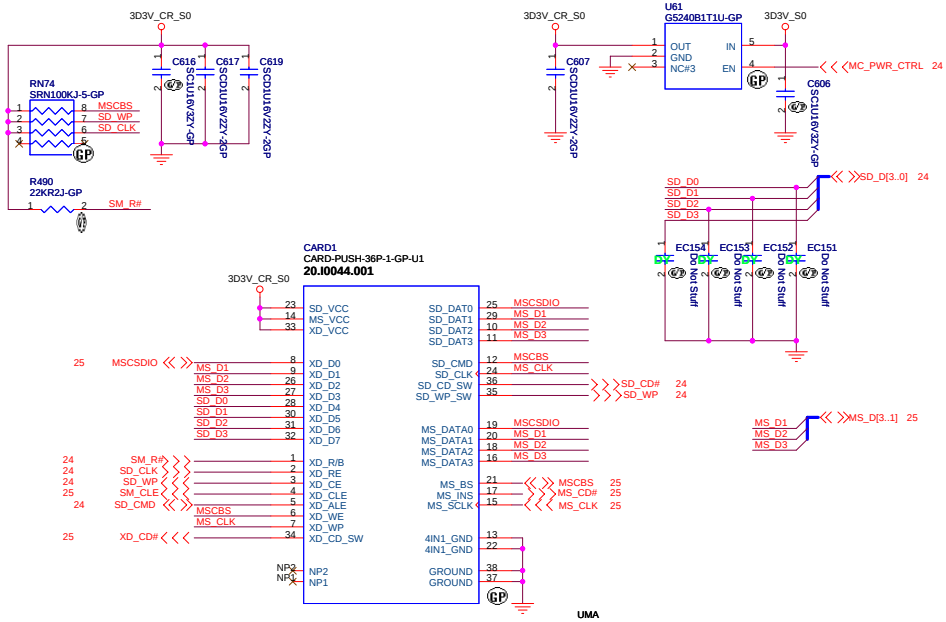
Cardbus I/F





1394 Connector





UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*PCMCIA / 1394 / CARD READER*	
Size: Custom	Document Number: Dellen	Rev: SA
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NV SMBus
A(pin143&145) : VGA(CRT) / DOCK
B(pin218&220) : DVI
C(pin208&210) : HDMI / TPI / LVDS

Put near graphic connector

7 PEG_TXP[15..0]
7 PEG_TXN[15..0]
7 PEG_RXP[15..0]
7 PEG_RXN[15..0]

5V_S0
Do Not Stuff
C416
R343 Do Not Stuff
R333 Do Not Stuff
36,37,38,39 CPUCORE_ON
16,19,28,31,34,37,38,39 PM_SLP_S3#
1D8V_S3
C420 Do Not Stuff
C419 Do Not Stuff
DCBATOUT
C434 Do Not Stuff
C433 Do Not Stuff
C432 Do Not Stuff
C427 Do Not Stuff
C430 Do Not Stuff

13 LCD_TXBOUT0+
13 LCD_TXBOUT0-
13 LCD_TXBOUT1+
13 LCD_TXBOUT1-
13 LCD_TXBOUT2+
13 LCD_TXBOUT2-
13 LCD_TXBCLK+
13 LCD_TXBCLK-
14 NV_BLUE
14 NV_GREEN
14 NV_RED
14 NV_TV_COMP
14 NV_TV_LUMA
14 NV_TV_CRMA

LCD_TXACLK- 13
LCD_TXACLK+ 13
LCD_TXAOUT2- 13
LCD_TXAOUT2+ 13
LCD_TXAOUT1- 13
LCD_TXAOUT1+ 13
LCD_TXAOUT0- 13
LCD_TXAOUT0+ 13
NV_EDID_DAT 13
NV_EDID_CLK 13
NV_LCDVDD_ON 13
NV_BLON 31
NV_DVI_DAT 42
NV_DVI_CLK 42

2D5V_S0
R113 NV Do Not Stuff
C417 Do Not Stuff
3D3V_S0
C415 MXM Do Not Stuff
MXM1 Do Not Stuff
MXM
Do Not Stuff

EMI REQUEST
TMDS_A_TX0+_1 ERN4 TMDS_A_TX0+ 42
TMDS_A_TX0-_1 TMDS_A_TX0- 42
Do Not Stuff
TMDS_A_TX1+_1 ERN3 TMDS_A_TX1+ 42
TMDS_A_TX1-_1 TMDS_A_TX1- 42
Do Not Stuff
TMDS_A_TX2+_1 ERN2 TMDS_A_TX2+ 42
TMDS_A_TX2-_1 TMDS_A_TX2- 42
Do Not Stuff
TMDS_A_TXC+_1 ERN1 TMDS_A_TXC+ 42
TMDS_A_TXC-_1 TMDS_A_TXC- 42
Do Not Stuff
ERN77~ERN80要靠近MXM1

DVI_A_HPD 42

TMDS_B_TX0+ TP69 TPAD30
TMDS_B_TX0- TP68 TPAD30
TMDS_B_TX1+ TP55 TPAD30
TMDS_B_TX1- TP54 TPAD30
TMDS_B_TX2+ TP62 TPAD30
TMDS_B_TX2- TP61 TPAD30
G72_27MHZ TP58 TPAD30
G72_27MHZSS TP66 TPAD30
DVI_B_HPD TP64 TPAD30
TMDS_B_TXC+ TP53 TPAD30
TMDS_B_TXC- TP52 TPAD30

3 CLK_PCIE_PEG#
3 CLK_PCIE_PEG
R359 Do Not Stuff
7,16,20,22,28,31,33 PLT_RST1#
PLT_RST1#_MXM
C428 MXM Do Not Stuff

19,31 SMBD_G792
R139 Do Not Stuff
SMBD_MXM
19,31 SMBC_G792
R358 Do Not Stuff
SMBC_MXM

34 MXM_THER
14 NV_HSYNC
14 NV_VSYNC
14 NV_DDCCLK
14 NV_DDCDAT

TPAD30 TP17 SPDIF_HDMI
TPAD30 TP63 GPU_BUFRST#
TPAD30 TP67 MP_INT
TPAD30 TP65 GPU_PRGM#

TPAD30 TP56 IGP_UTX2#
TPAD30 TP57 IGP_UTX2
TPAD30 TP60 TMDS_GPIO6_SW
TPAD30 TP19

UMA

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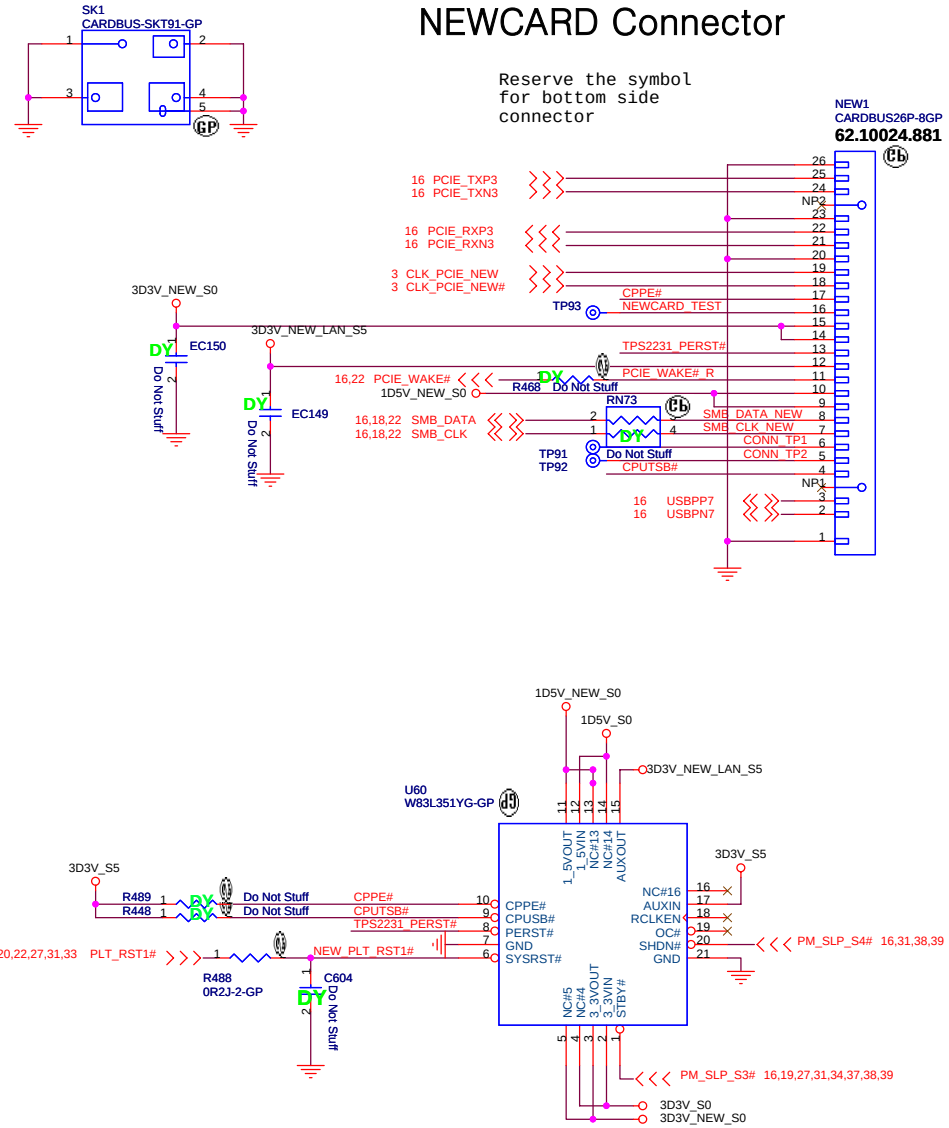
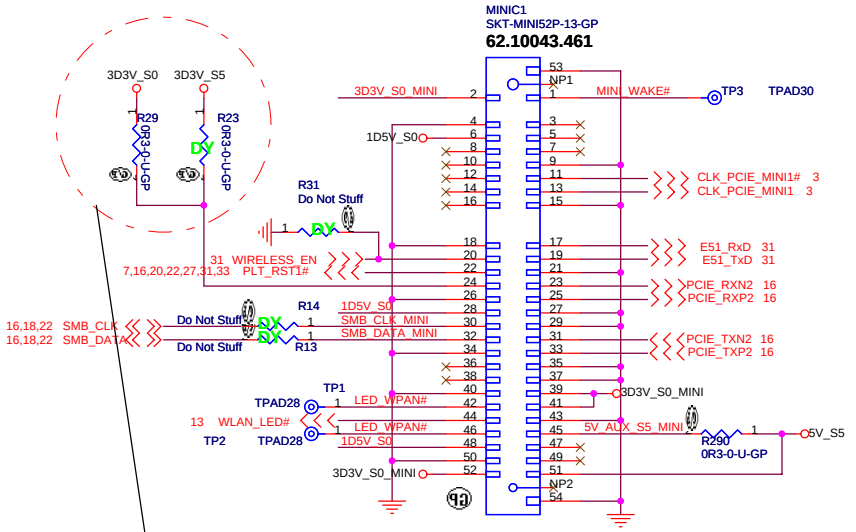
Title: Graphic MXM CONN
Size: A3 | Document Number: Dellen | Rev: SA
Date: Tuesday, January 16, 2007 | Sheet 27 of 43

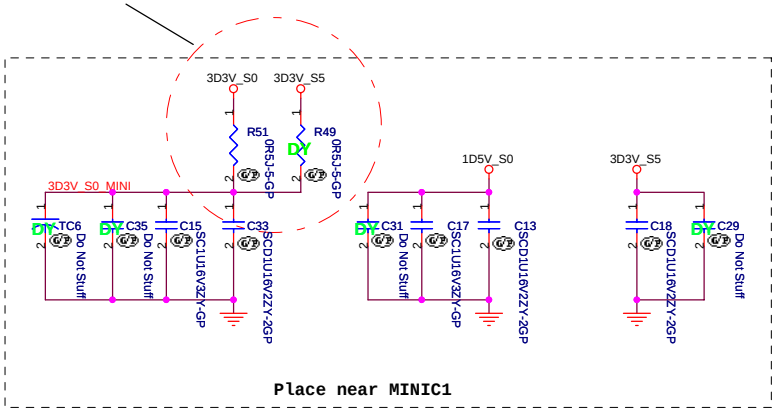
NEWCARD Connector

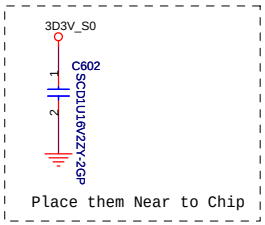


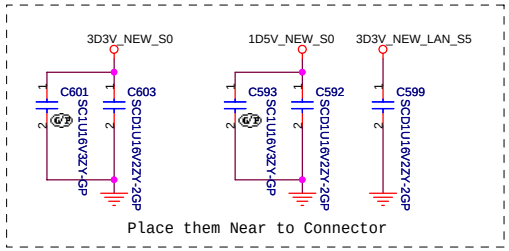
Mini Card Connector



PCIE Mini Card For WLA W/O iAMT, TV or 3G







UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MINI CARD / NEW CARD		
Size: A3	Document Number: Dellen	Rev: SA
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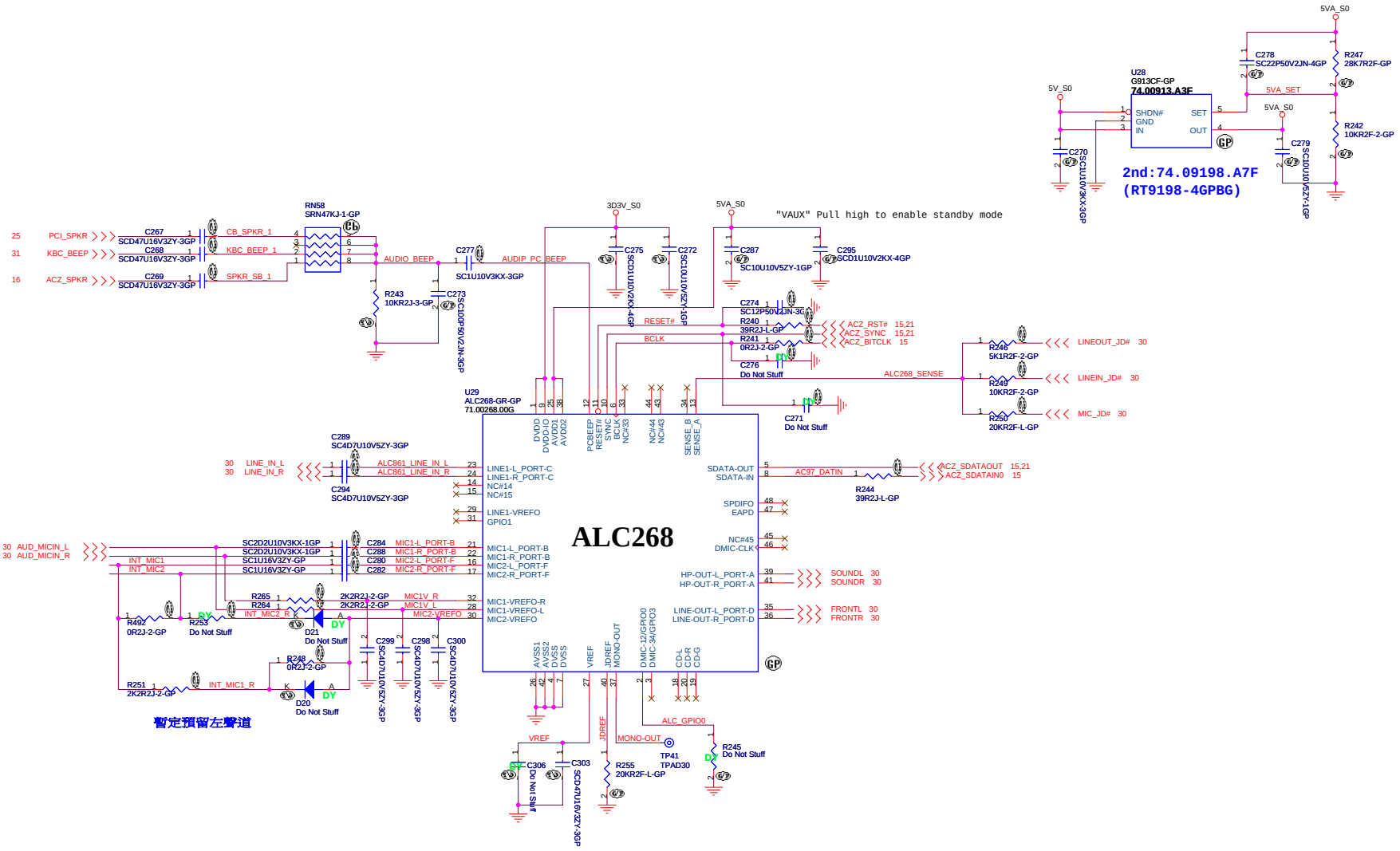

UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *AZALIA CODEC - ALC268*

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Custom	Dellen	SA

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AUDIO OP AMPLIFIER

```
R,L 1.5W Speaker
  mount R274,R281
  R269->63.36334.1DL
  R268->63.33334.1DL
R,L 1W Speaker
  mount R280,R281
  R269->63.15334.1DL
  R268->63.12334.1DL
R,L 1.2W Speaker
  mount R280,R281
  R269->63.10334.1DL
  R268->63.68234.1DL
```

KBC_MUTE_GPIO8

Internal Speaker

MIC IN

LINE IN

LINE OUT

UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title	AUDIO AMP AND JACK	
Size: Custom	Document Number: Dellen	Rev: SA
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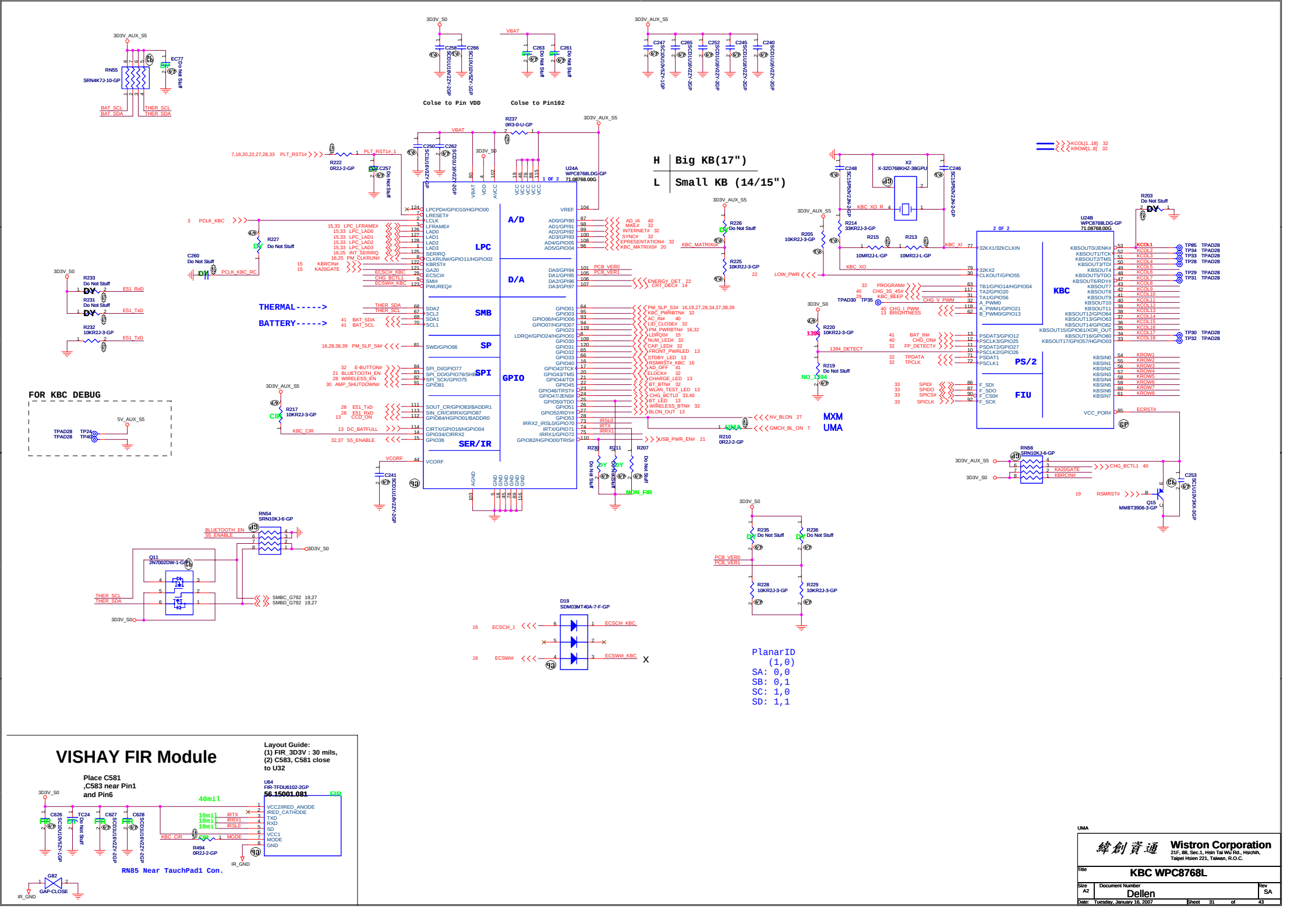
H | Big KB(17")
L | Small KB (14/15")
FOR KBC DEBUG
THERMAL----->
BATTERY----->
Colse to Pin VDD
Colse to Pin102
U24A WPC8768LDG-GP 71.08768.00G
U24B WPC8768LDG-GP 71.08768.00G
A/D
LPC
D/A
SMB
SP
SPI
GPIO
SER/IR
KBC
PS/2
FIU
MXM
UMA
NON_FIR
X2 X-32D768KHZ-38GPU
RN55 SRN4K7J-10-GP
RN54 SRN10KJ-6-GP
RN56 SRN10KJ-6-GP
Q11 2N7002DW-1-GP
Q15 MMBT3906-3-GP
D19 SDM03MT40A-7-F-GP
PlanarID (1,0)
SA: 0,0
SB: 0,1
SC: 1,0
SD: 1,1
VISHAY FIR Module
Place C581 ,C583 near Pin1 and Pin6
Layout Guide:
(1) FIR_3D3V : 30 mils,
(2) C583, C581 close to U32
40mil
RN85 Near TauchPad1 Con.
U64 FIR-TFDU6102-2GP 56.15001.081
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC8768L
Size A2
Document Number Dellen
Rev SA
Date: Tuesday, January 16, 2007
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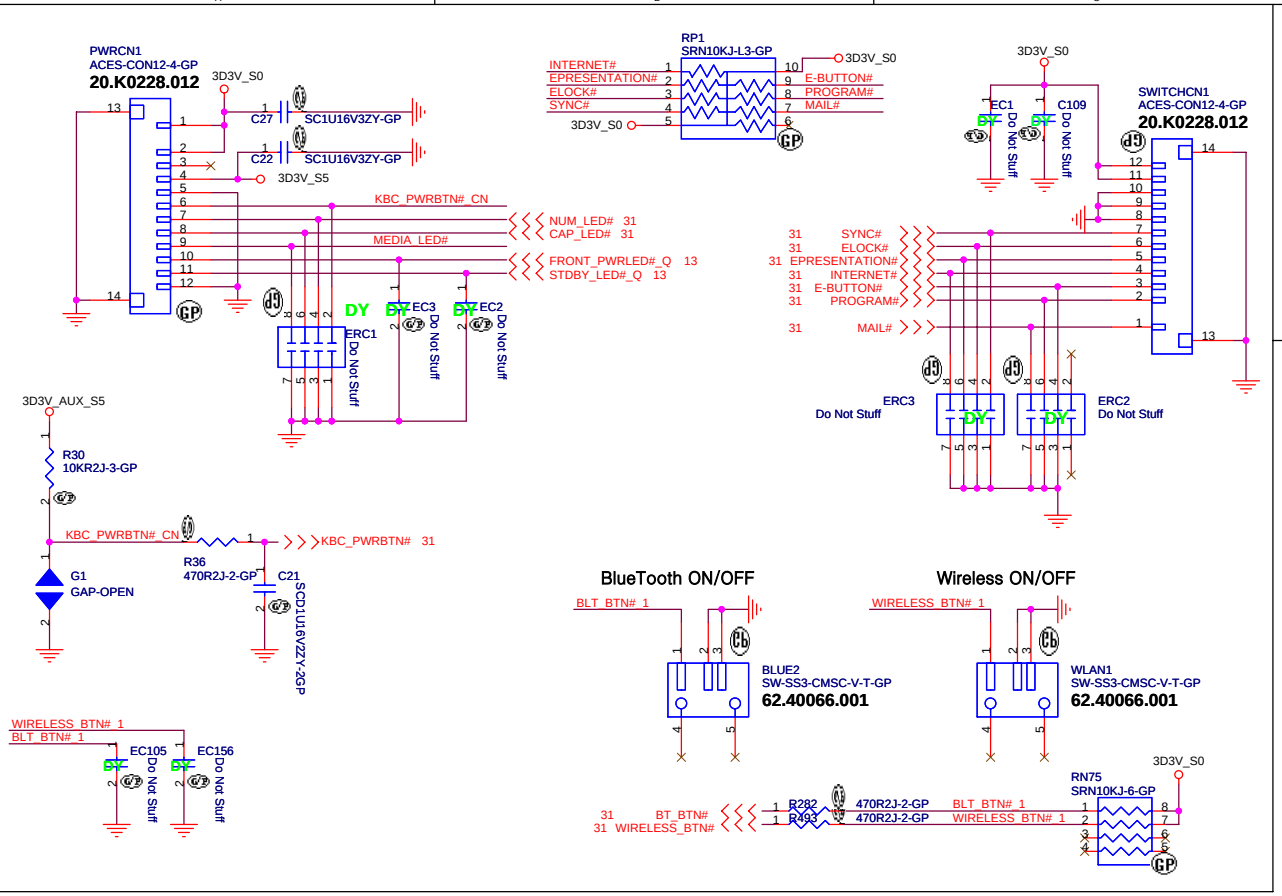
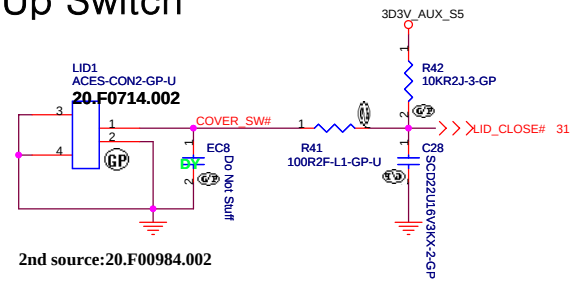
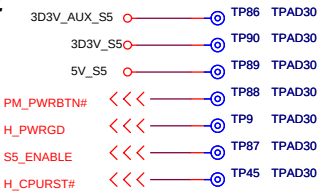


Cover Up Switch

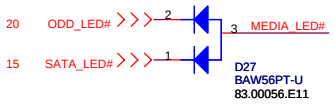


2nd source:20.F00984.002

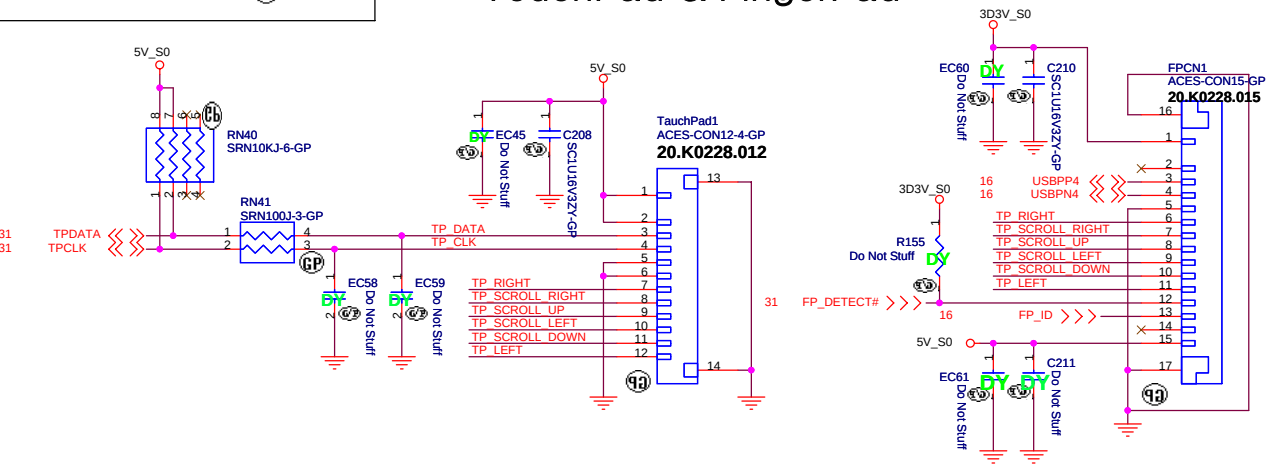
Check test point



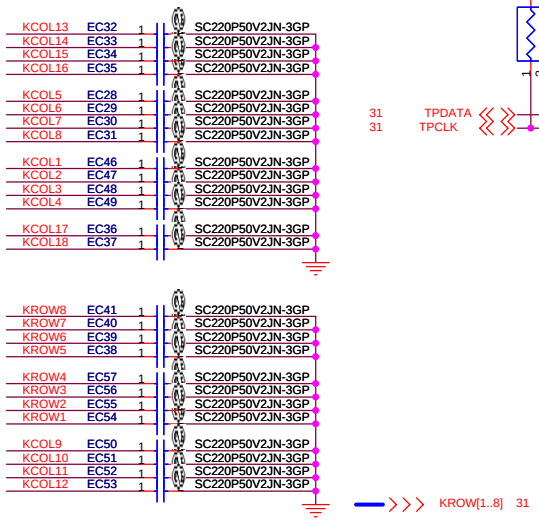
Test Point放在Dimm Door打開可量測處

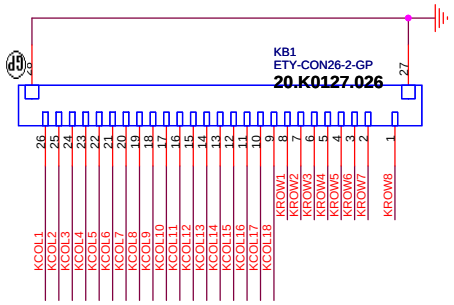


TouchPad & FingerPad



EMI Bypass cap.





Internal KeyBoard conn.

1 25

CHECK KB SPEC. AND PIN DEFINE

UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *BUTTONs / KB / TOUCHPAD / FP*

Size	Document Number	Rev
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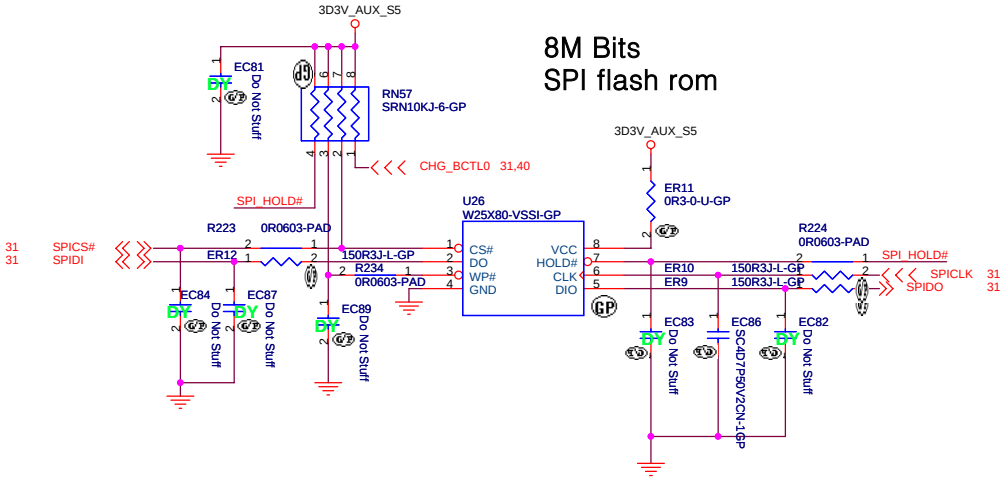

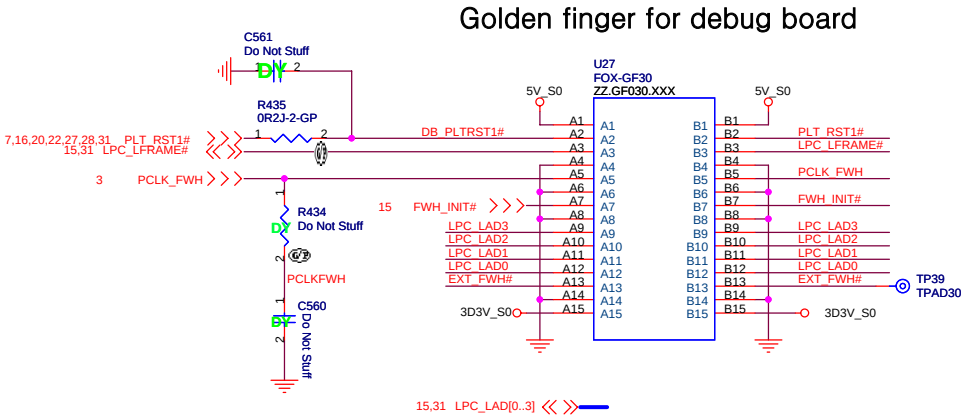

UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title		
BIOS		
Size: A3	Document Number: Dellen	Rev: SA
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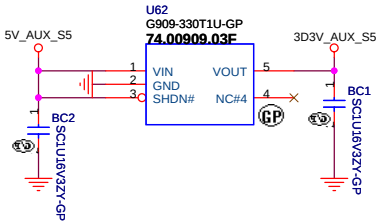
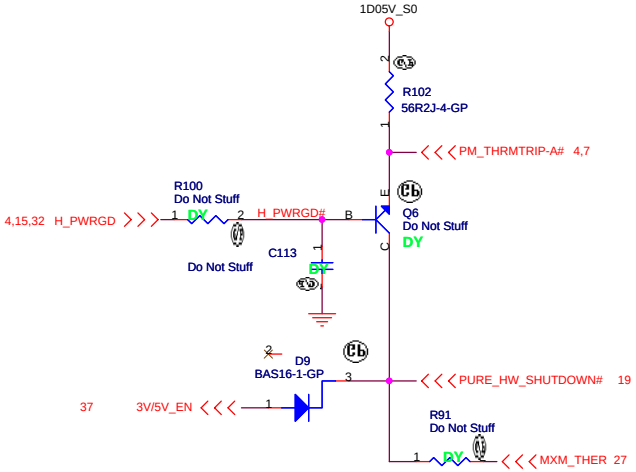
Aux Power

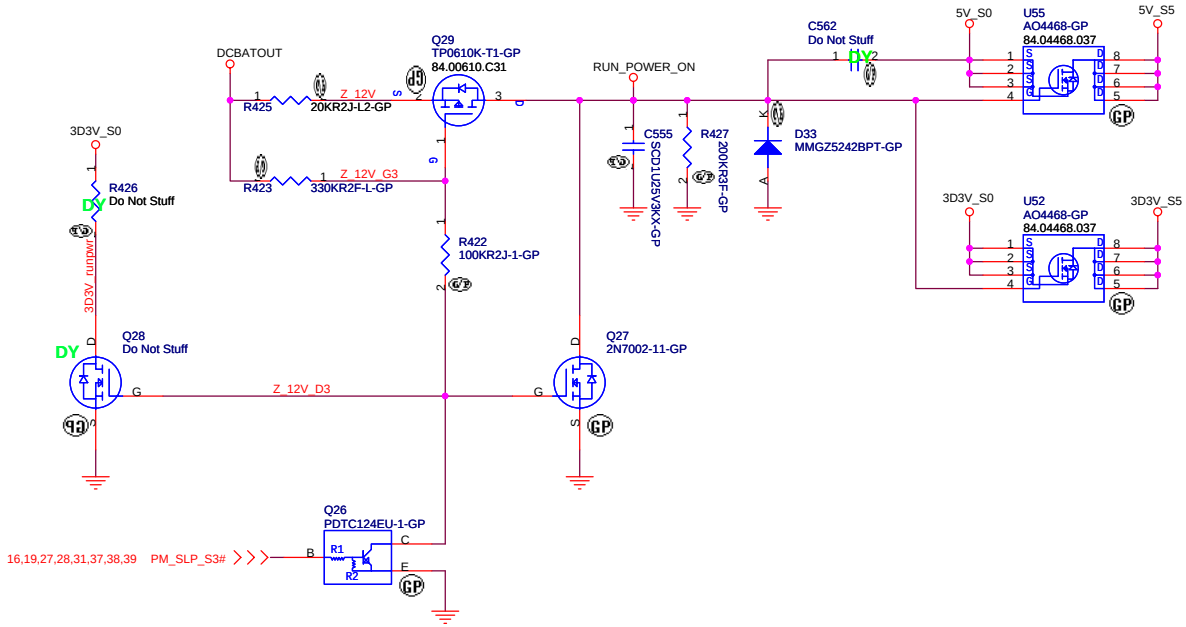
3D3V_AUX_S5

I max = 150 mA





Run Power



5V_S0

3D3V_S0

UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: 3D3V_AUX_S5 / 3D3V_S0 / 5V_S0		
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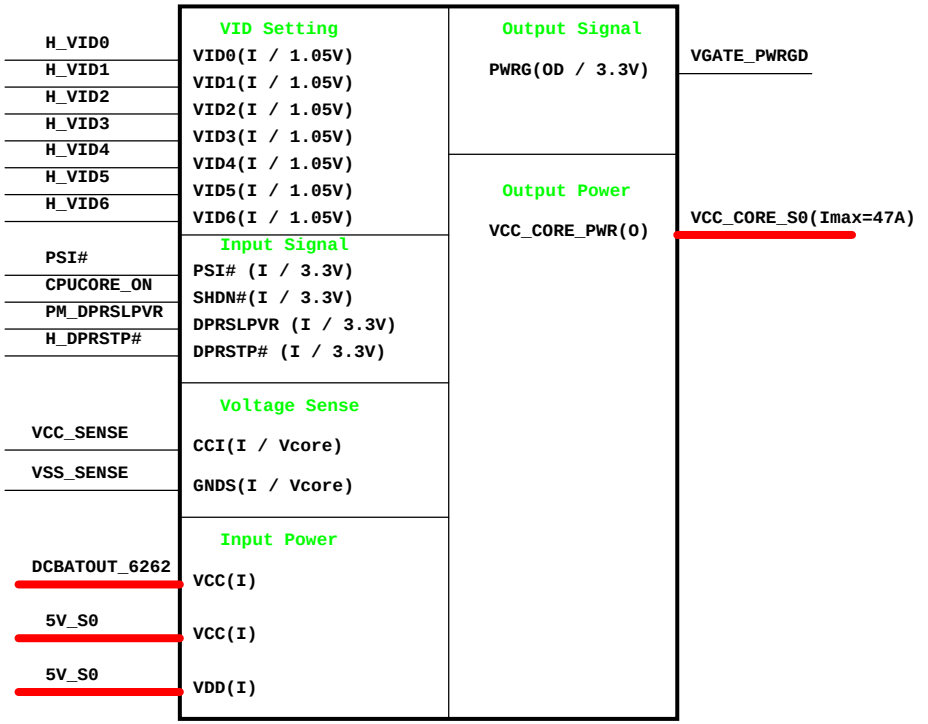
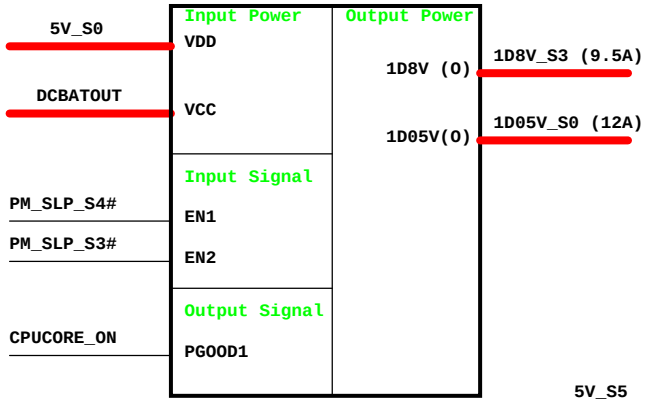
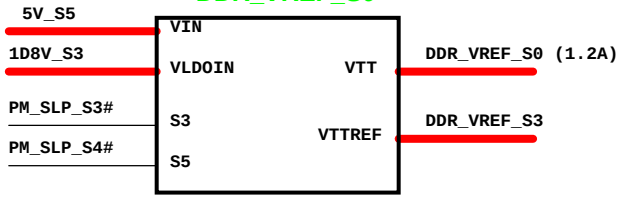
CPU_CORE
MAX8770



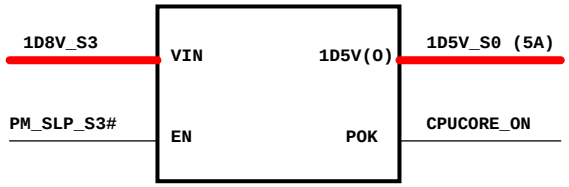
MAX8717
1D8V_S3 / 1D05V_S0



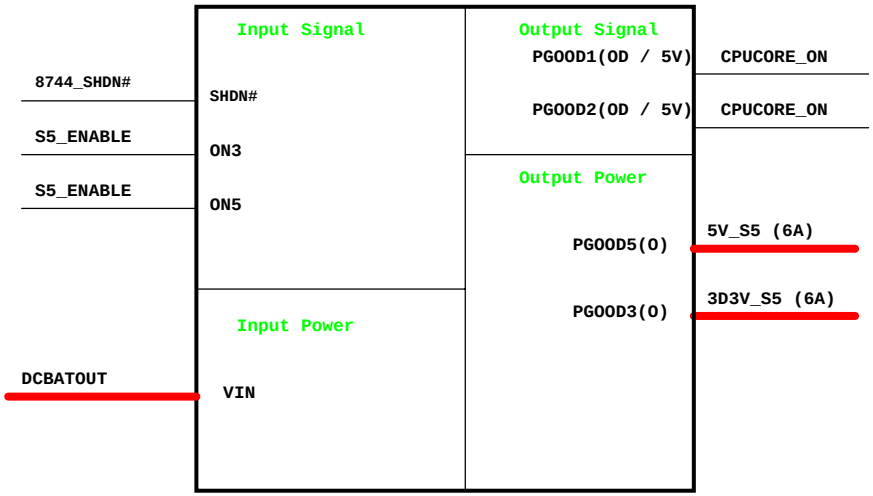
TPS51100
DDR_VREF_S0



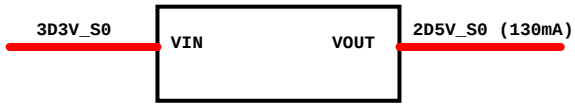
APL5912
1D5V_S0



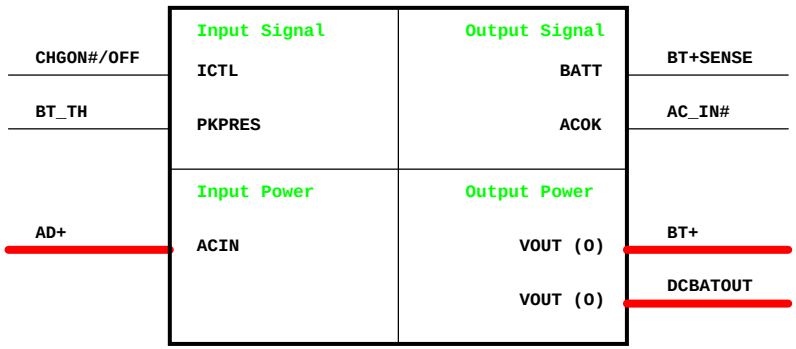
MAX8744
5V_S5 / 3D3V_S5



APL5312
2D5V_S0



Charger ISL6255



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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Power Block Diagram***

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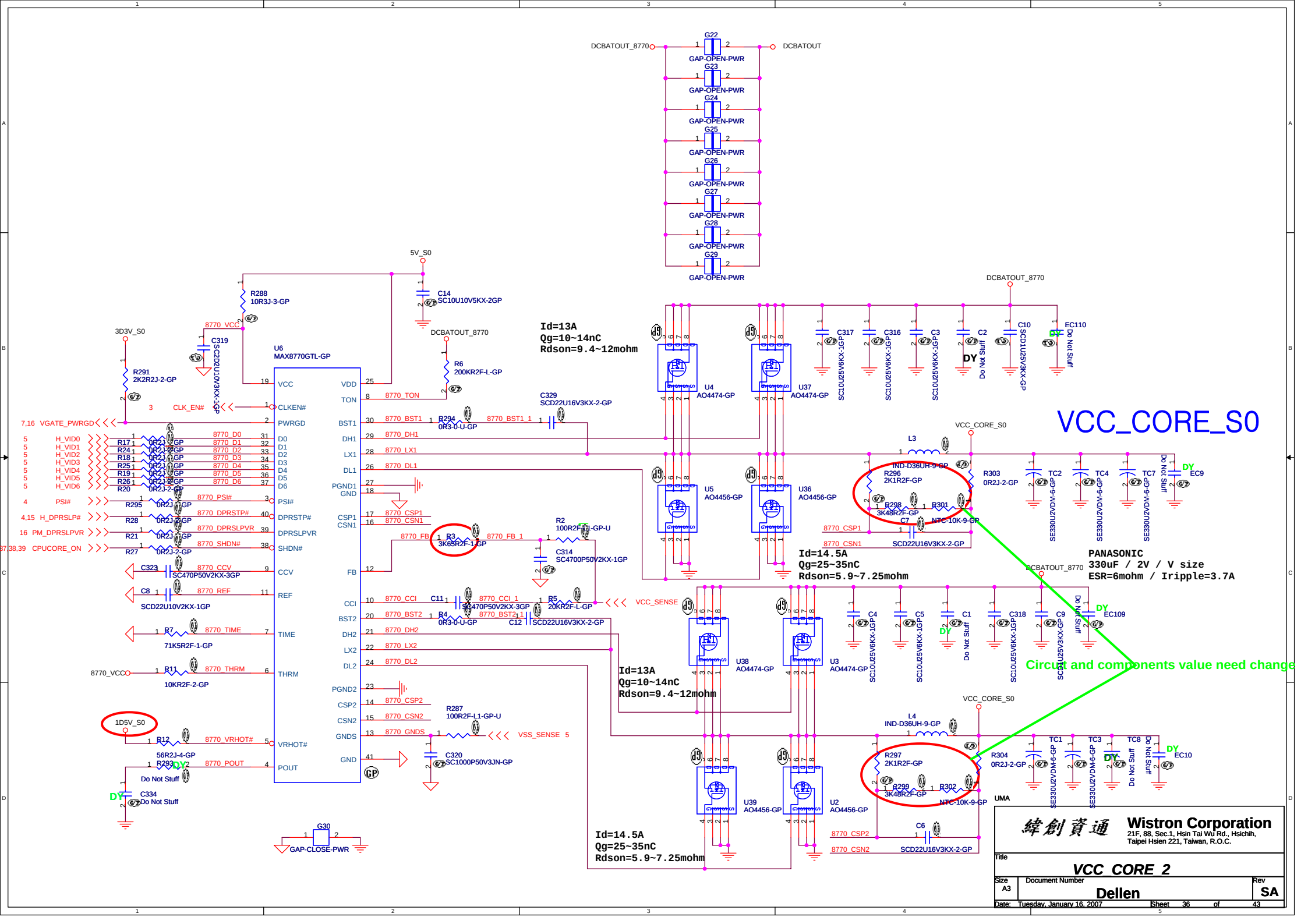
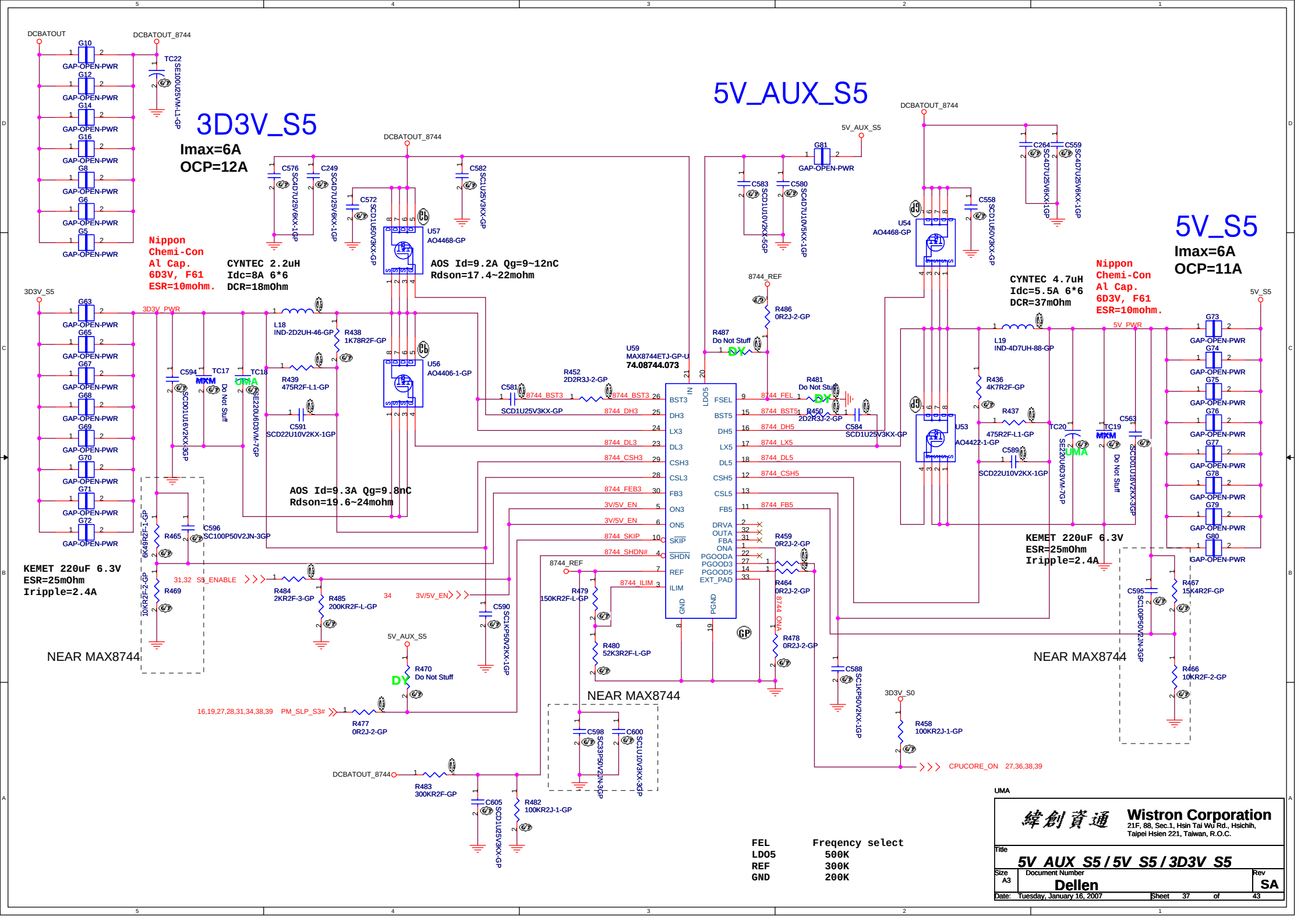

VCC_CORE_S0
U6
MAX8770GTL-GP
Id=13A
Qg=10~14nC
Rdson=9.4~12mohm
Id=14.5A
Qg=25~35nC
Rdson=5.9~7.25mohm
PANASONIC
330uF / 2V / V size
ESR=6mohm / Iripple=3.7A
Circuit and components value need change
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
VCC_CORE_2
Dellen
Tuesday, January 16, 2007



Company	Wistron Corporation, 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	5V_AUX_S5 / 5V_S5 / 3D3V_S5
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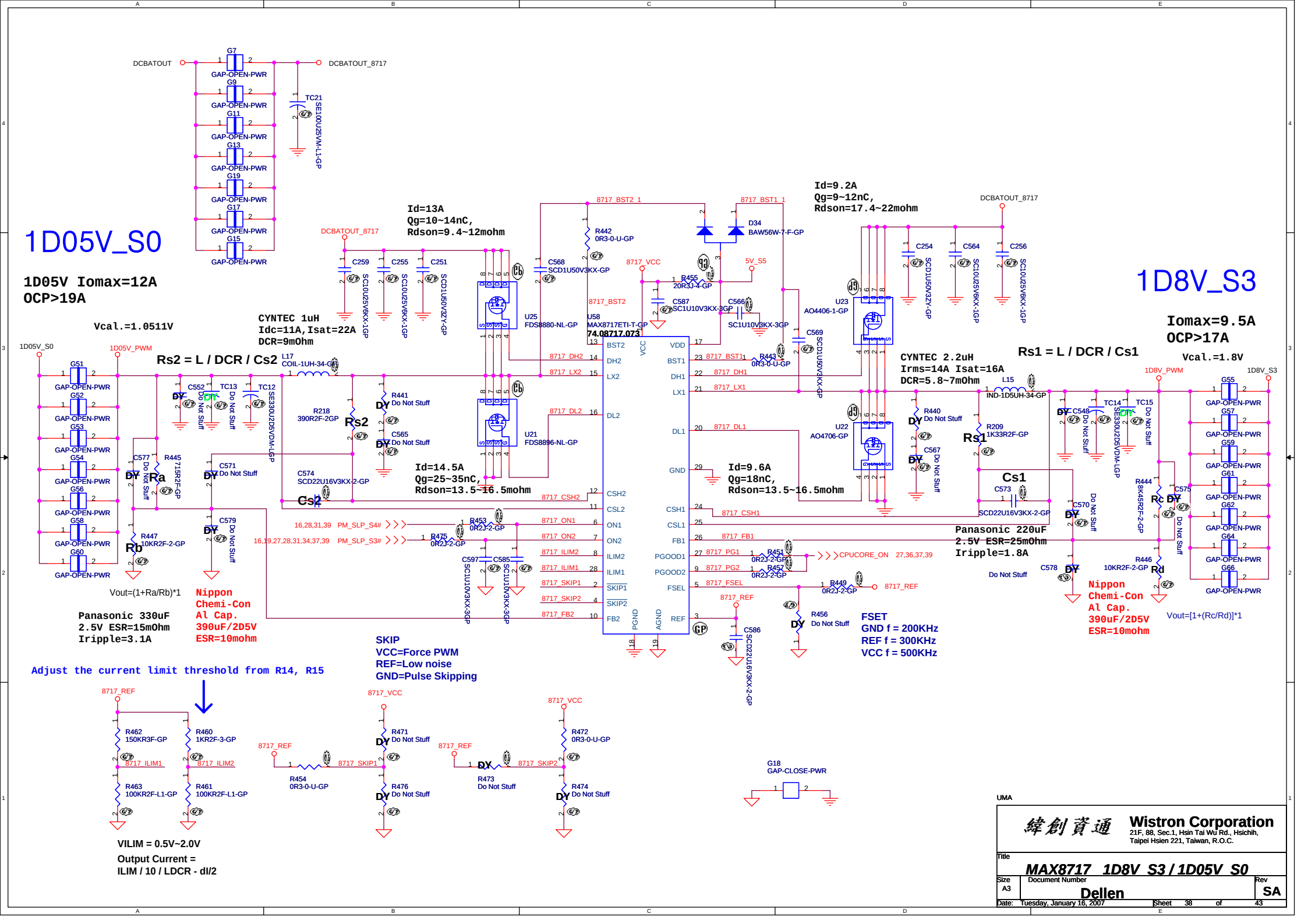
1D05V_S0
1D05V Iomax=12A
OCP>19A
Vcal.=1.0511V
Rs2 = L / DCR / Cs2
CYNTEC 1uH
Idc=11A,Isat=22A
DCR=9mOhm
Id=13A
Qg=10~14nC,
Rdson=9.4~12mohm
Id=14.5A
Qg=25~35nC,
Rdson=13.5~16.5mohm
Id=9.2A
Qg=9~12nC,
Rdson=17.4~22mohm
Id=9.6A
Qg=18nC,
Rdson=13.5~16.5mohm
1D8V_S3
Iomax=9.5A
OCP>17A
Vcal.=1.8V
Rs1 = L / DCR / Cs1
CYNTEC 2.2uH
Irms=14A Isat=16A
DCR=5.8~7mOhm
Vout=(1+Ra/Rb)*1
Panasonic 330uF
2.5V ESR=15mOhm
Iripple=3.1A
Nippon
Chemi-Con
Al Cap.
390uF/2D5V
ESR=10mohm
Panasonic 220uF
2.5V ESR=25mOhm
Iripple=1.8A
Nippon
Chemi-Con
Al Cap.
390uF/2D5V
ESR=10mohm
Vout=[1+(Rc/Rd)]*1
SKIP
VCC=Force PWM
REF=Low noise
GND=Pulse Skipping
FSET
GND f = 200KHz
REF f = 300KHz
VCC f = 500KHz
Adjust the current limit threshold from R14, R15
VILIM = 0.5V~2.0V
Output Current =
ILIM / 10 / LDCR - dI/2
U58
MAX8717ETI-T-GP
74.08717.073
U25
FDS8880-NL-GP
U21
FDS8896-NL-GP
U23
AO4406-1-GP
U22
AO4706-GP
D34
BAW56W-T-F-GP
L17
COIL-1UH-34-GP
L15
IND-1D5UH-34-GP
DCBATOUT
DCBATOUT_8717
1D05V_PWM
1D8V_PWM
8717_VCC
5V_S5
8717_BST2_1
8717_BST1_1
8717_BST2
8717_BST1
8717_DH2
8717_DH1
8717_LX2
8717_LX1
8717_DL2
8717_DL1
8717_CSH2
8717_CSH1
8717_ON1
8717_ON2
8717_ILIM2
8717_ILIM1
8717_SKIP1
8717_SKIP2
8717_FB2
8717_FB1
8717_PG1
8717_PG2
8717_FSEL
8717_REF
PM_SLP_S4#
PM_SLP_S3#
CPUCORE_ON
BST2
DH2
LX2
DL2
CSH2
CSL2
ON1
ON2
ILIM2
ILIM1
SKIP1
SKIP2
FB2
BST1
DH1
LX1
DL1
CSH1
CSL1
FB1
PGOOD1
PGOOD2
FSEL
REF
VDD
VCC
GND
PGND
AGND
Ra
Rb
Rs2
Cs2
Rs1
Cs1
Rc
Rd
R218 390R2F-2GP
R441 Do Not Stuff
R565 Do Not Stuff
R445 715R2F-GP
R447 10KR2F-2-GP
R453 0R2J-2-GP
R475 0R2J-2-GP
R442 0R3-0-U-GP
R443 0R3-0-U-GP
R455 20R3J-4-GP
R451 0R2J-2-GP
R457 0R2J-2-GP
R449 0R2J-2-GP
R456 Do Not Stuff
R440 Do Not Stuff
R567 Do Not Stuff
R209 1K33R2F-GP
R444 8K45R2F-2-GP
R446 10KR2F-2-GP
R462 150KR3F-GP
R460 1KR2F-3-GP
R463 100KR2F-L1-GP
R461 100KR2F-L1-GP
R454 0R3-0-U-GP
R471 Do Not Stuff
R476 Do Not Stuff
R473 Do Not Stuff
R472 0R3-0-U-GP
R474 Do Not Stuff
C552 Do Not Stuff
C577 Do Not Stuff
C571 Do Not Stuff
C579 Do Not Stuff
C574 SCD22U16V3KX-2-GP
C597 SC1U10V3KX-3GP
C585 SC1U10V3KX-3GP
C568 SCD1U50V3KX-GP
C587 SC1U10V3KX-3GP
C566 SC1U10V3KX-3GP
C569 SCD1U50V3KX-GP
C586 SCD22U16V3KX-GP
C573 SCD22U16V3KX-2-GP
C548 Do Not Stuff
C570 Do Not Stuff
C578 Do Not Stuff
C575 Do Not Stuff
C259 SC10U25V6KX-1GP
C255 SC10U25V6KX-1GP
C251 SCD1U50V3ZY-GP
C254 SCD1U50V3ZY-GP
C564 SC10U25V6KX-1GP
C256 SC10U25V6KX-1GP
TC21 SE100U25VM-L1-GP
TC13 Do Not Stuff
TC12 SE330U2D5VDM-LGP
TC14 SE330U2D5VDM-LGP
TC15 Do Not Stuff
G18 GAP-CLOSE-PWR
GAP-OPEN-PWR
UMA
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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title
MAX8717 1D8V_S3 / 1D05V_S0
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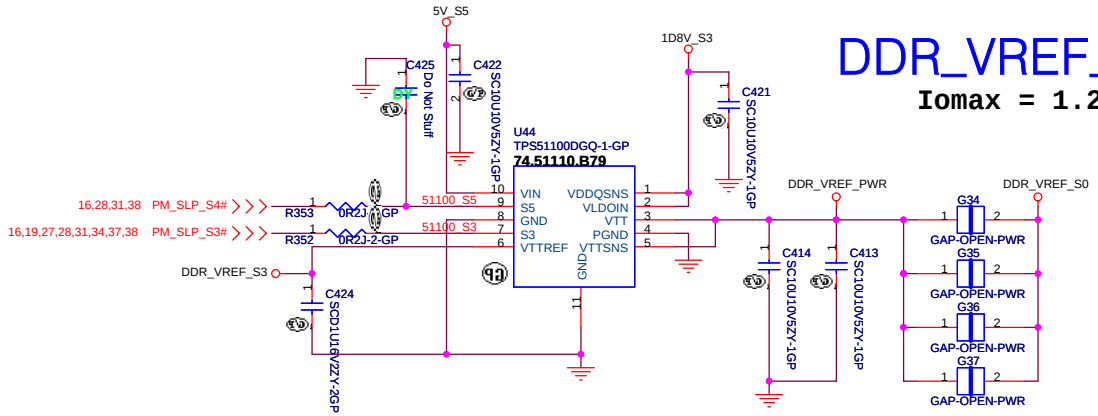

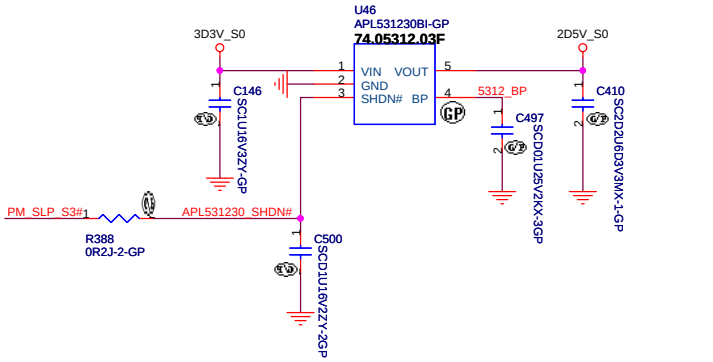

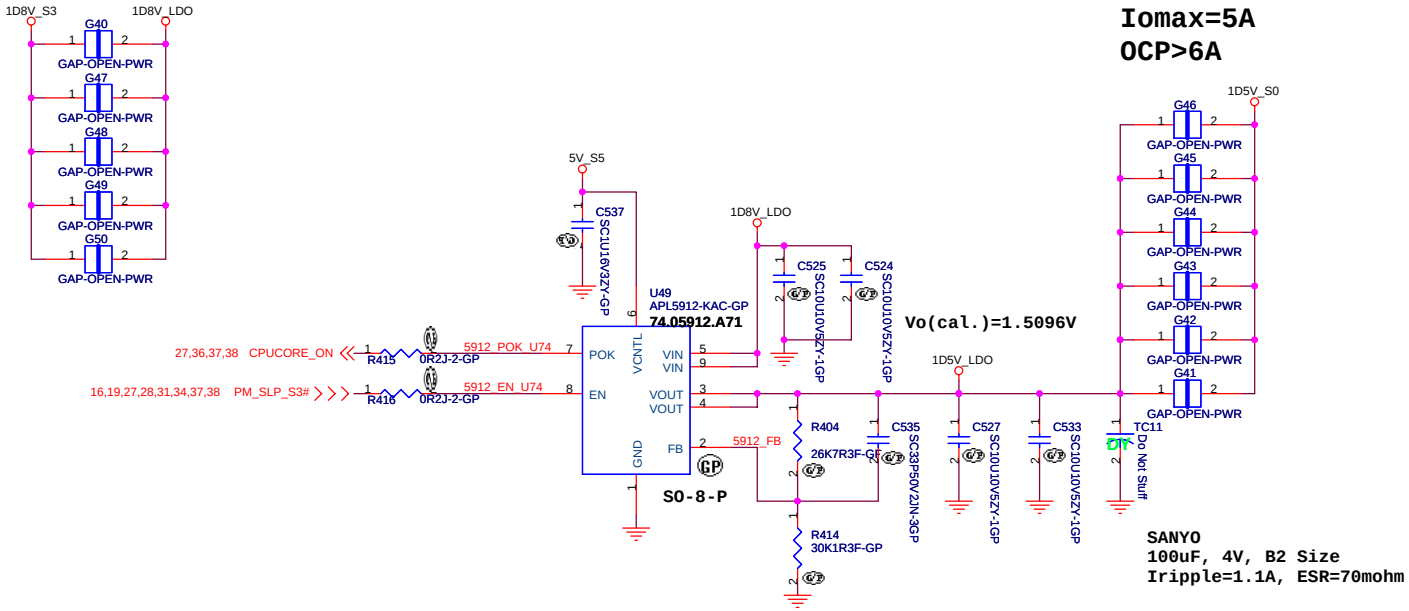

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Title: 1D5V_S0 / 2D5V_S0 / DDR_VREF_S0

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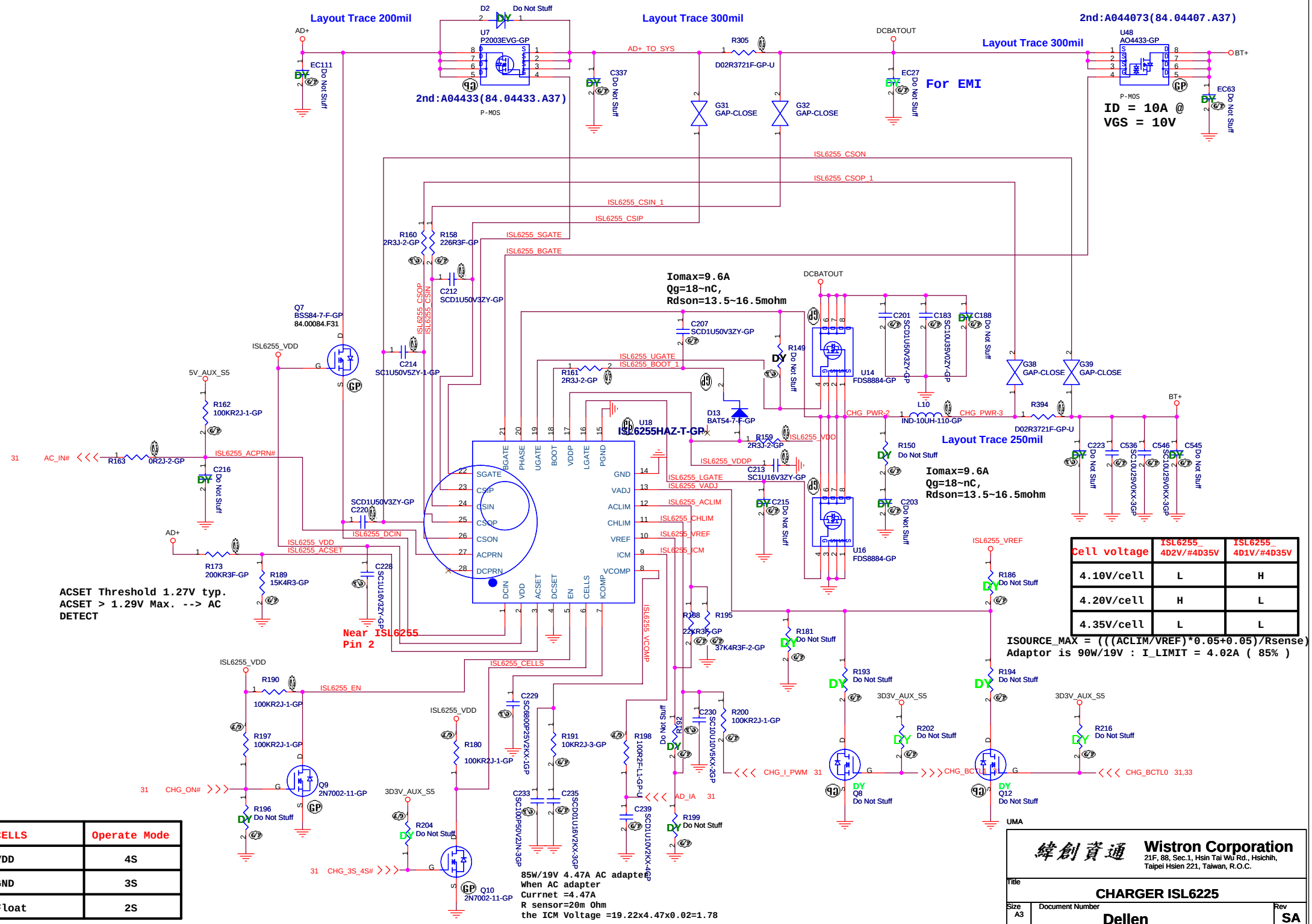

Cell voltage	ISL6255_4D2V/#4D35V	ISL6255_4D1V/#4D35V
4.10V/cell	L	H
4.20V/cell	H	L
4.35V/cell	L	L

CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S

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Title: CHARGER ISL6225

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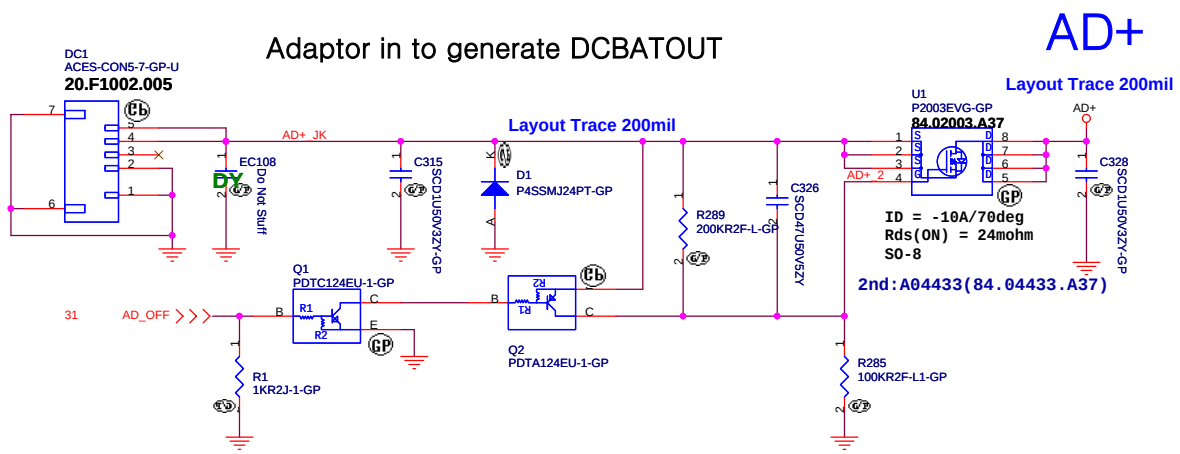

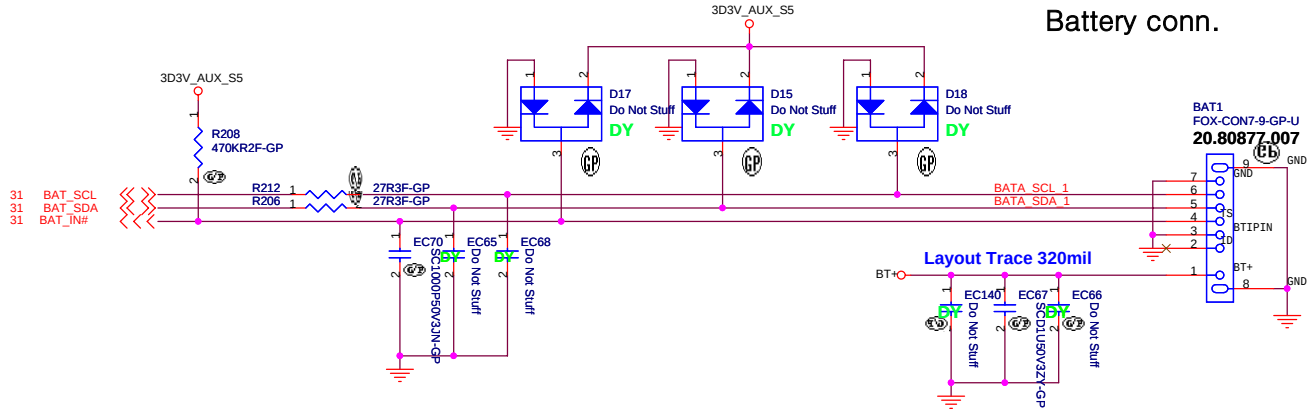

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Title	AD / BATT conn.	
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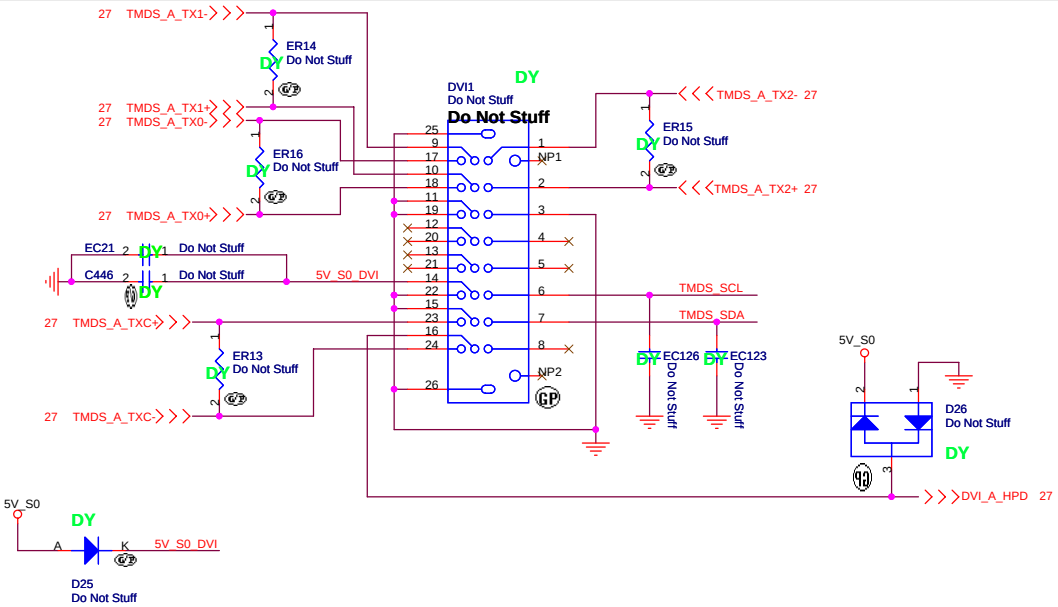

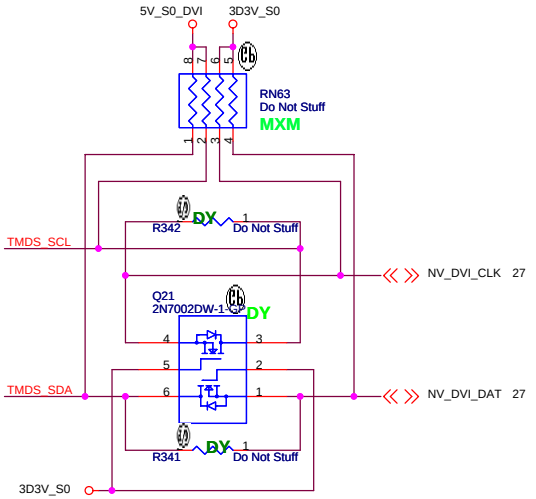

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Title: DVI CONNECTOR		
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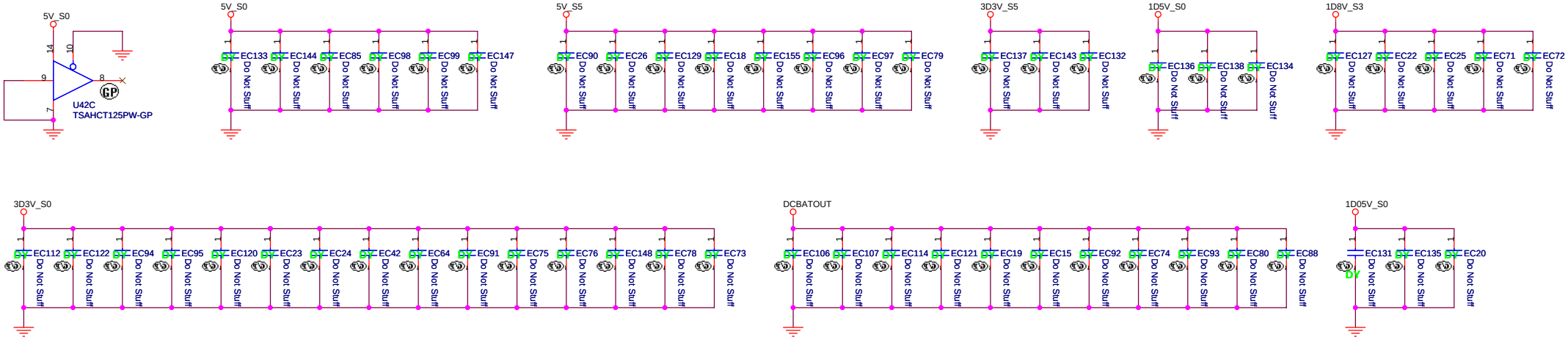

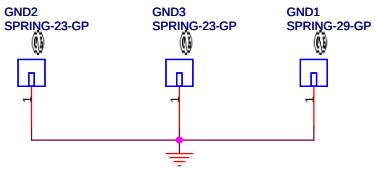

Spring

GND 1 : 34.42T14.001
GND 2/3 : 34.39S07.003

MINI CARD

H13 HOLE	H19 HOLE	H18 HOLE	H14 HOLE	H25 HOLE	H24 HOLE	H16 HOLE	H15 HOLE	H21 HOLE	H20 HOLE	H23 HOLE	H17 HOLE	H22 HOLE	H6 HOLE	H2 HOLE	H1 HOLE	H9 HOLE	H5 HOLE	H3 HOLE	H8 HOLE
34.4G502.001	34.4G502.001	34.42Y01.011	34.42Y01.011	34.4G805.001	34.4G805.001	34.42Y01.011	34.42Y01.011	34.42Y01.011	34.42Y01.011	34.42Y01.011	34.42Y01.011	34.42Y01.011							

Fan

H4 HOLE	H7 HOLE	H10 HOLE	H11 HOLE	H12 HOLE															

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***EMI / Spring / Boss***

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