

TIGA Main Board Rev.04

Index System Block

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Revision History

Rev	Date	Description
01	2005.08.30	Official Release.
02	2005.10.07	Change P24,28. ECO No. F0205A14919.
03	2005.10.11	Change P12. ECO No. F0205A15271.
04	2005.12.02	Change P10,17,50,51,56. ECO No. F0205A18869.
05	2005.12.12	Change P4-6,12,22,23,38,44. ECO No. F0205A19559.
06	2006.03.14	Change P23. ECO No. F0206A04590.

Power Block

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49	Power/DDC/3.3V/1.8V
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51	Power/DDC/5V
52	Power/DDC/Charger
53	Power/DDC/0.9VTerm
54	Power/LDO/System
55	Power/LDO/PMU
56	Power/Node/DCIn
57	Power/Node/Battery
58	Power/Node/PWR_1
59	Power/Node/Switch
60	Power/PMU/LUNA1 (PMU)
61	Power/PMU/LUNA2 (EC)
62	Power/PMU/VolMeter
63	Power/PMU/Scont
64	Power/PMUEtc1
65	Power_SEQUENCE
66	TEST PAD

System resource assign

USB Channel		PCI INTERRUPT	
Port#	Device	PCIINT#	Device
USB0	System #1	INT#0	PCIC USB#1 / IDE
USB1	System #2	INT#1	PCIC SMBus/AC-97
USB2	System #3	INT#2	Mini-PCI USB#3
USB3	Bay	INT#3	Mini-PCI USB#2
USB4	Finger-Print	INT#4	On Board LAN
USB5	P-R (to USB Hub)	INT#5	UNUSED
USB6	Reserve(TP)	INT#6	Unused
USB7	BlueTooth	INT#7	Unused

#05
Add and Correct Configuration

SMBus		PCI BUS #1	
SMBCNT[2:0]	Device	IDSEL	Dev.ID Device
0,0,0	uDIMM0,THRM	AD16	00h
0,0,1	PMU	AD17	01h
0,1,0	PLL	AD18	02h
0,1,1	uDIMM1,THRM	AD19	03h PCMCIA/IEEE1394
		AD20	04h Internal LAN
		AD21	05h miniPCI
		AD22	06h
		AD23	07h

PCI REQ#/GNT#	
REQ#/GNT#	Device
REQ#0	PCMCIA
REQ#1	UNUSED
REQ#2	Unused
REQ#3	On Board LAN
REQ#4	Mini PCI
REQ#5	Unused

Main Board Model Configurations

Model	Destination	CPU	PR	Int. Mic	TPM	BT	TP	ODD	4in1
VB238AA	Overseas	Pentium-M 753 ULV	○	○	○	○	×	○	○
VB238AB	Overseas	Celeron-M 383 ULV	○	○	○	○	×	○	○
VB238AC	Japan Retail	Pentium-M 753 ULV	×	×	×	×	×	○	○
VB238AD	Japan Retail	Celeron-M 383 ULV	×	×	×	×	×	○	○
VB238AE	Overseas(FKL)	Celeron-M 383 ULV	×	×	×	○	×	○	○
VB238AF	Japan Customized	Pentium-M 753 ULV	×	×	○	×	○	×	×
VB238AG	Japan Retail	Pentium-M 773 ULV	×	×	×	×	×	○	○
VB238AH	Japan Retail	Celeron-M 383 ULV	×	×	×	×	×	○	○

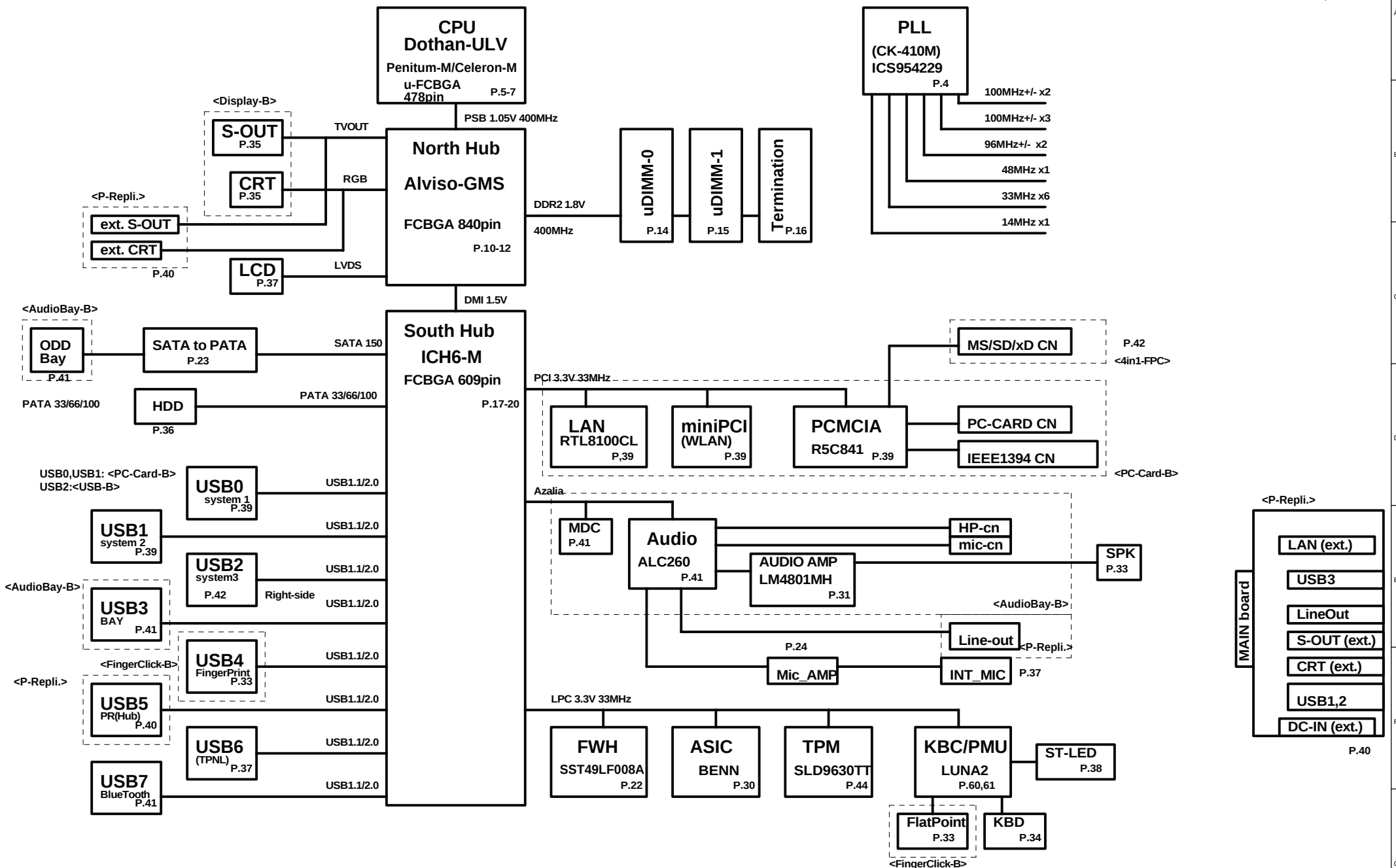
Refernce drawings.

DWG#	Description
C1CP250060-XX	Schematics ; PC-CARD Board (VB238BA)
C1CP250079-XX	Schematics ; Audio Bay Board (VB238FA)
C1CP250077-XX	Schematics ; Fingerprint Sensor board (VB238EA)
C1CP254631-XX	Schematics ; 4in1 FPC (VB238XA)
C1CP250066-XX	Schematics ; Port Replicator Board (VB238CA)
A3CP254680-01	Hardware specification.

System block diagram

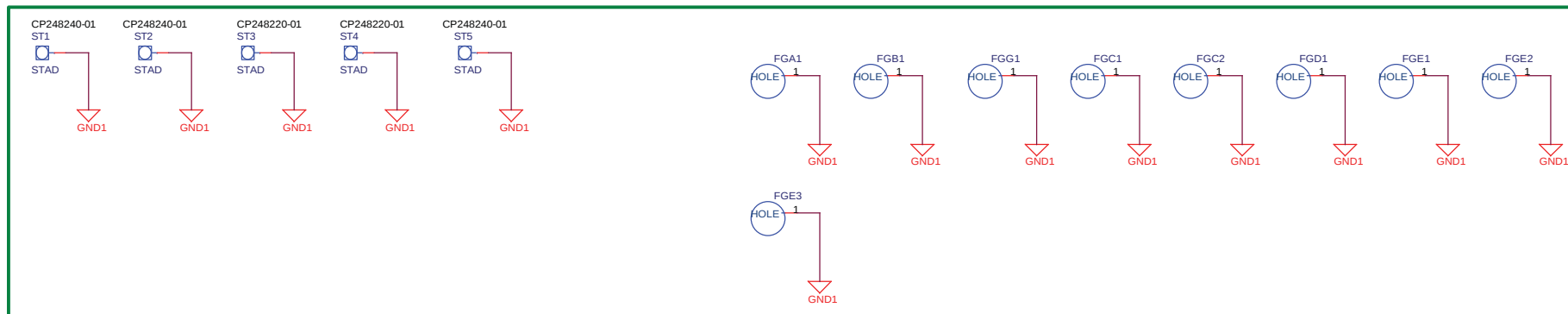
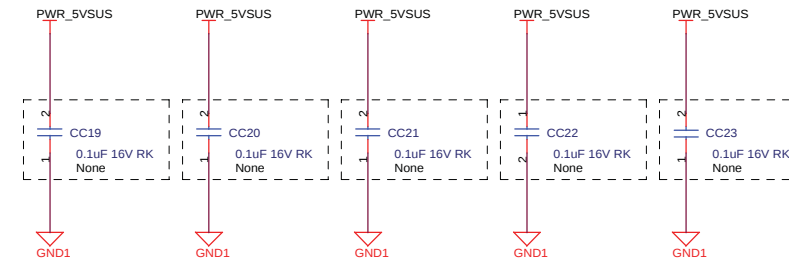
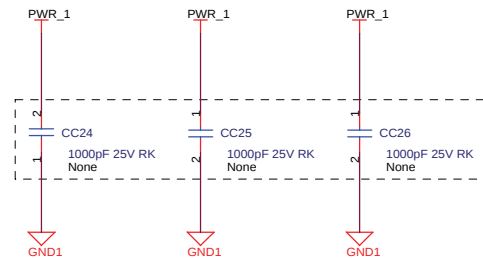
<http://hobi-elektronika.net>

FUJITSU CONFIDENTIAL Dolphin External I/F



[BLOCK DIAGRAM]

REV	DATE	DESIGN	CHECK	APPR	DESCRIPTION	TITLE	Draw. NO.	CUST.
						Tiga Main board	C1CP250040-X4	
						FUJITSU LTD.	2 / 66	



[EMI]

										TITLE Tiga Main board		
										DRAW. NO.	C1CP250040-X4	CUST.
REV.	DATE	DESIGN	CHECK	APPR.						DESCRIPTION		
DATE		DESIGN	CHECK	APPR.						FUJITSU LTD.		
										SHEET 3 / 66		

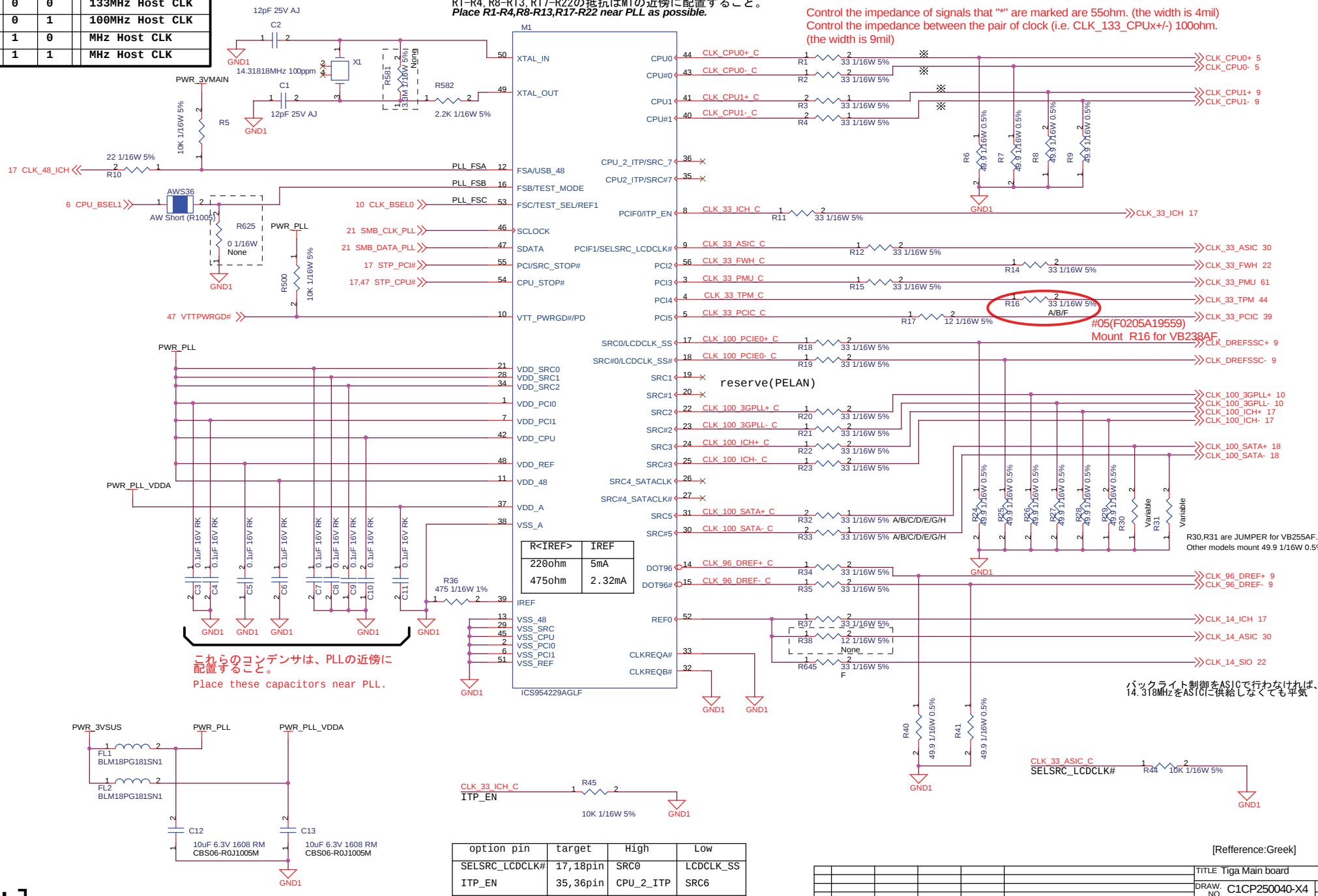
CK-410M Spec

FSA	FSB	FSC	Function
1	0	0	133MHz Host CLK
1	0	1	100MHz Host CLK
1	1	0	MHz Host CLK
1	1	1	MHz Host CLK

R1-R4, R8-R13, R17-R22の抵抗はM1の近傍に配置すること。
Place R1-R4, R8-R13, R17-R22 near PLL as possible.

※のパターン。また、各対のクロックライン同士の間隔(CLK_133_CPUx+/-# 間)は、信号線間インピーダンス100Ωで引くこと (9mil幅)。

Control the impedance of signals that "*" are marked are 55ohm. (the width is 4mil)
Control the impedance between the pair of clock (i.e. CLK_133_CPUx+/-) 100ohm. (the width is 9mil)



これらのコンデンサは、PLLの近傍に配置すること。
Place these capacitors near PLL.

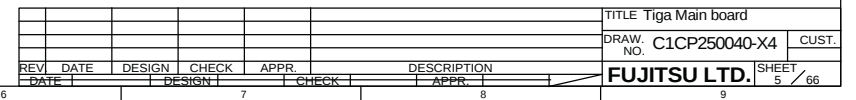
バックライト制御をASICで行わなければ、14.318MHzをASICに供給しなくても平気

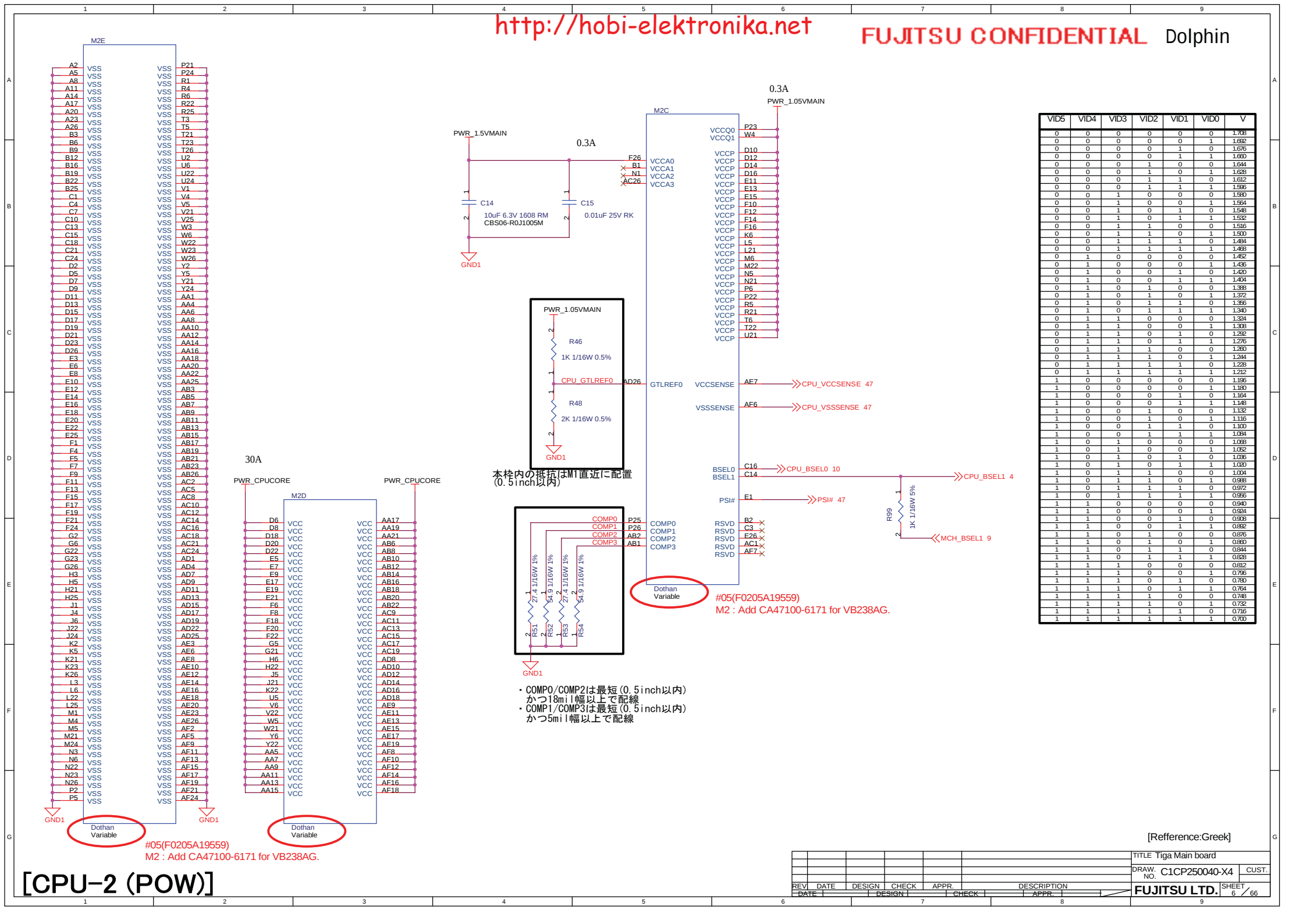
[PLL]

option pin	target	High	Low
SELSRC_LCDCLK#	17, 18pin	SRC0	LCDCCLK_SS
ITP_EN	35, 36pin	CPU_2_ITP	SRC6

REV	DATE	DESIGN	CHECK	APPR	DESCRIPTION
1					

[Reference:Greek]	
TITLE Tiga Main board	
DRAW. NO. C1CP250040-X4	CUST.
FUJITSU LTD. SHEET 4 / 66	





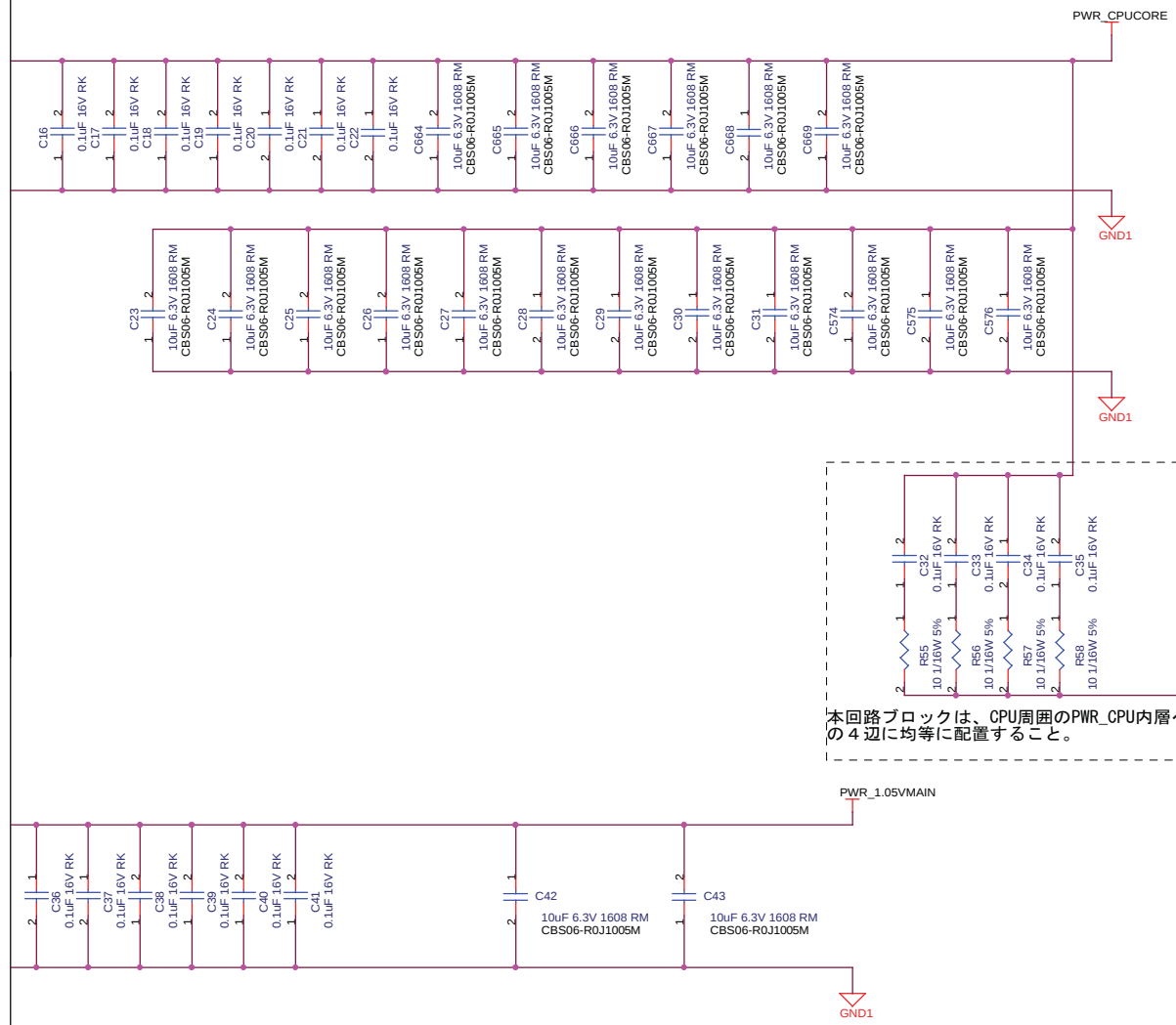
[CPU-2 (POW)]

REV				DATE				DESIGN				CHECK				APPR				DESCRIPTION			
DATE				DESIGN				CHECK				APPR				DESCRIPTION				SHEET			
																				6 / 66			

[Reference:Greek]

#05(F0205A19559)
M2 : Add CA47100-6171 for VB238AG.

M2
Pentium-M
Celeron-M

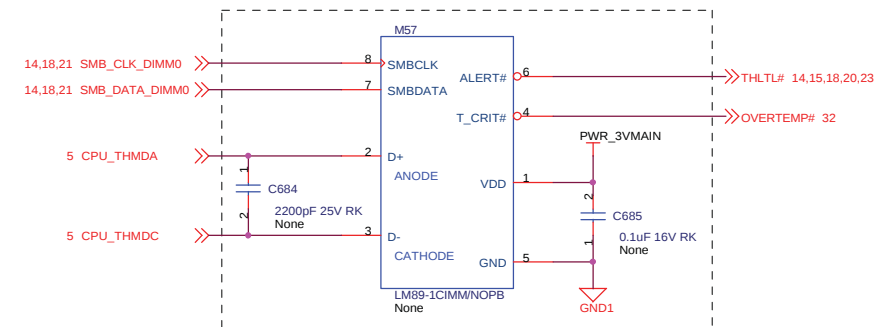
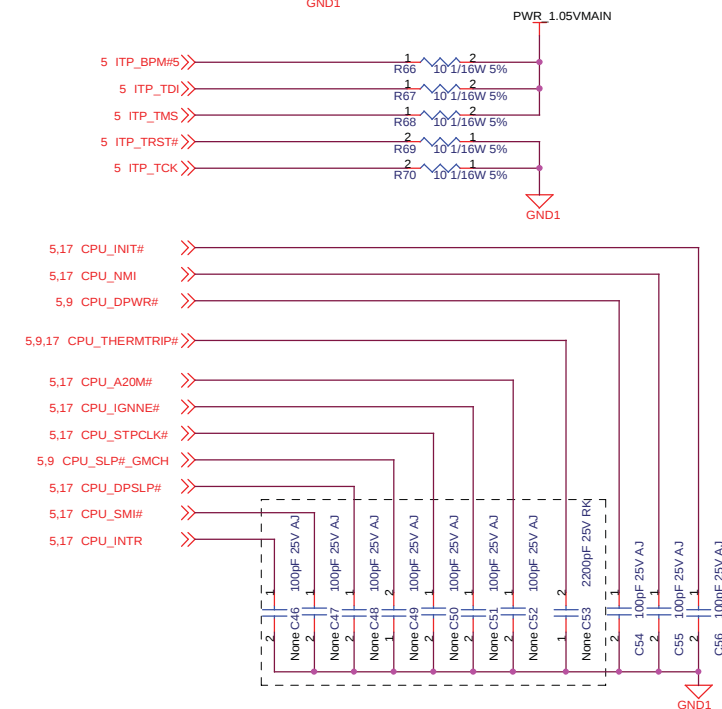
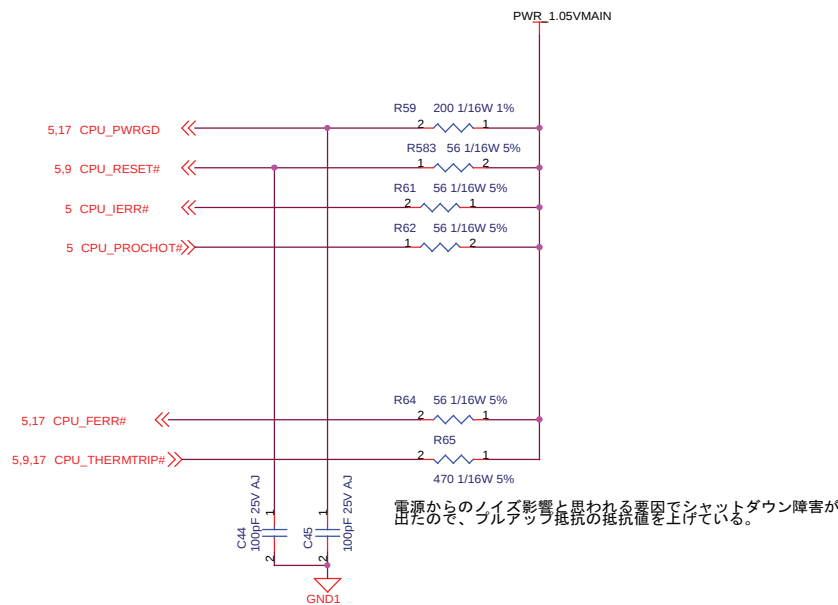


本回路ブロックは、CPU周囲のPWR_CPU内層ベタの4辺に均等に配置すること。

[CPU CAP]

[Reference:Greek]

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DATE	DESIGN	CHECK	APPR			SHEET 7 / 66	

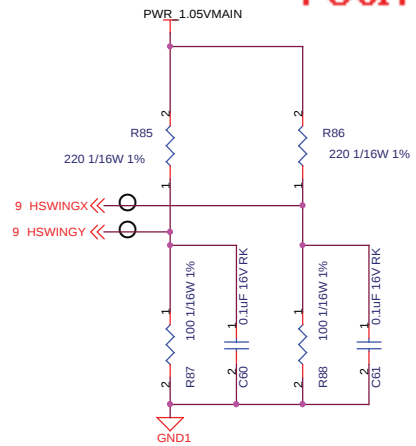
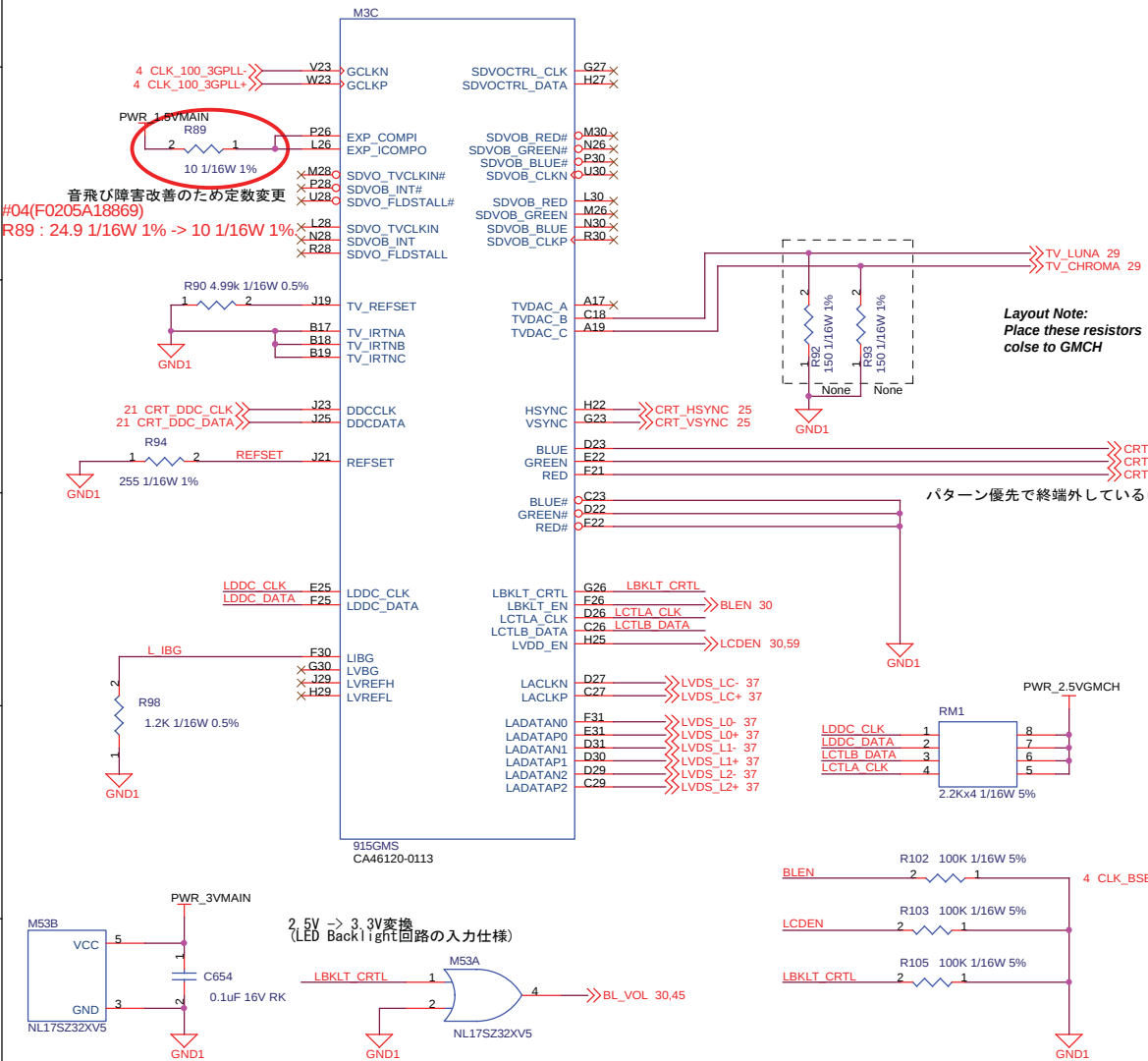


[CPU PU/etc.]

[Reference:Greek]

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NO.						DRAW.	C1CP250040-X4
DATE		DESIGN	CHECK	APPR		CUST.	
						FUJITSU LTD.	8 / 66



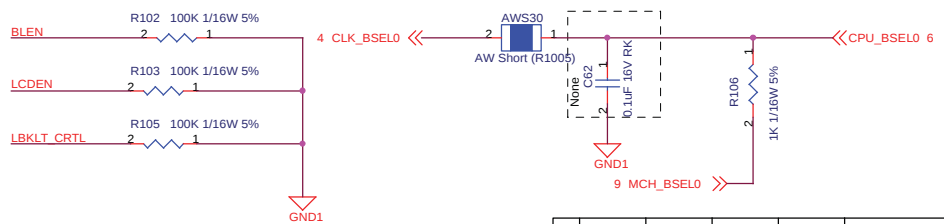


上記の部品は、GMCHから3inch以内に配置すること。
○の付いた信号は25mil以上の幅で配線し、左右と下をGND1で囲むこと。

GMCH Strapping Option

PIN	Function
CFG5	Low = DMI x 2 High = DMI x 4
CFG6	Low = DDR2 High = DDR1
CFG7 (CPU Strap)	Low = DT/Transportable CPU High = Mobile CPU
CFG9 (PEG Lane)	Low = Reverse Lane High = Normal operation
CFG[13:12] (XOR/ALL Z test straps)	00 = Reserved 01 = XOR Mode Enable 10 = All Z Mode Enabled 11 = Normal Operation
CFG16 (FSB Dynamic ODT)	Low = Dynamic ODT Disabled High = Dynamic ODT Enabled
CFG18 (VCC Select)	Low = 1.05V High = 1.5V
CFG19 (VTT Select)	Low = 1.05V High = 1.2V

CK410 BSEL Settings:
00 = PSB533 (BSEL0=0, BSEL1=0)
10 = PSB400 (BSEL0=1, BSEL1=0)
11 = Reserved (BSEL0=1, BSEL1=1)

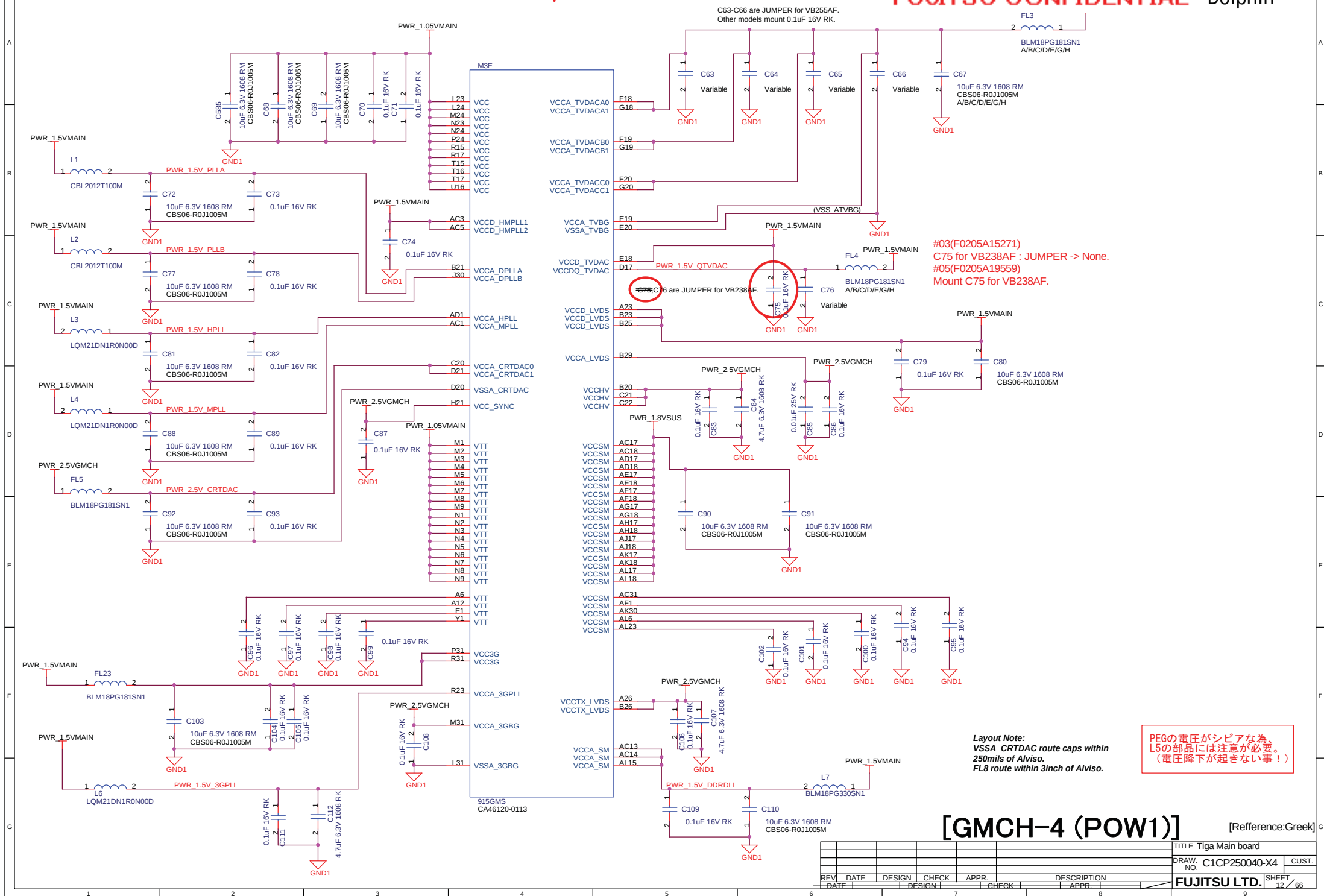


[GMCH-2 (VGA/etc.)]



[Reference:Greek]

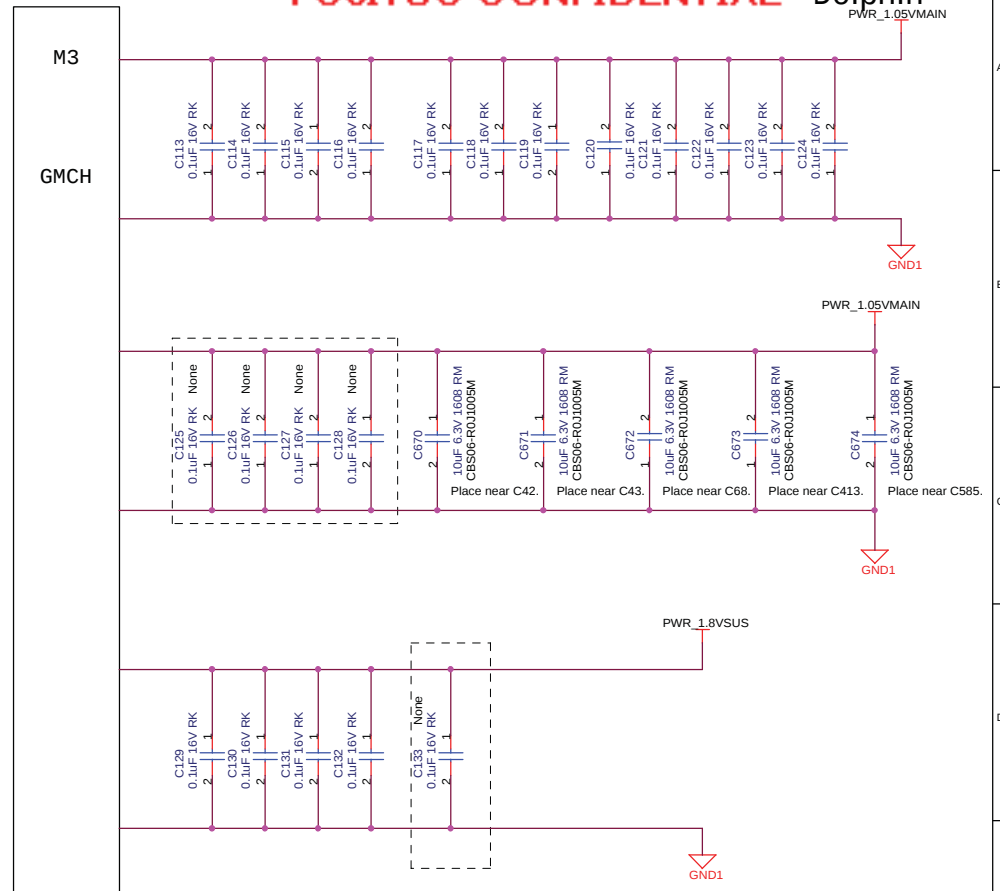
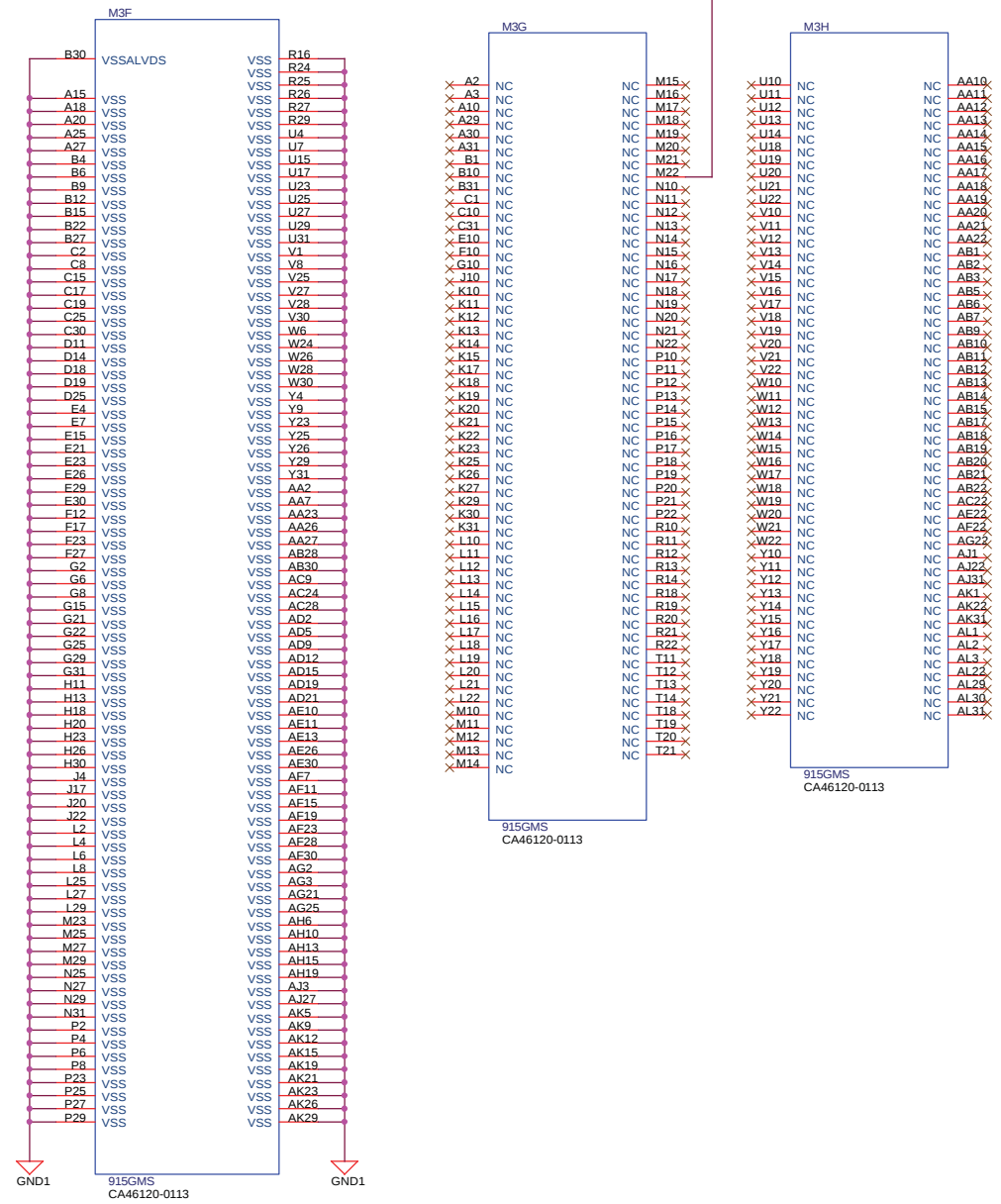
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REV.		DATE		DESIGN		CHECK		APPR.		DESCRIPTION	
DATE		DESIGN		CHECK		APPR.				FUJITSU LTD.	
6		7		7		8		9		SHEET 11/66	



[GMCH-4 (POW1)]

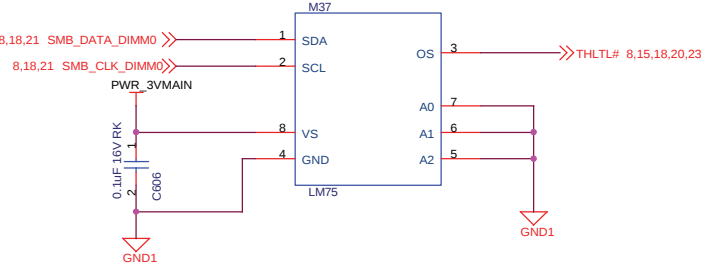
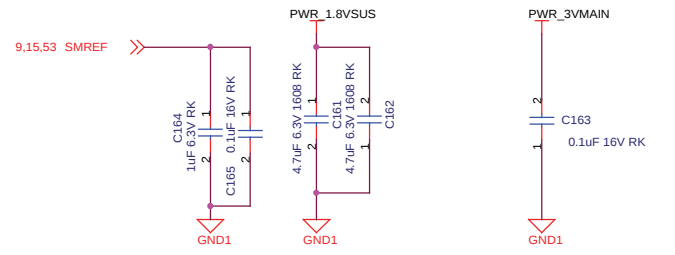
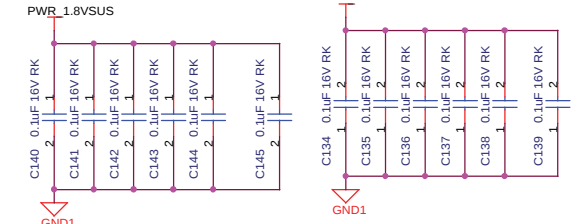
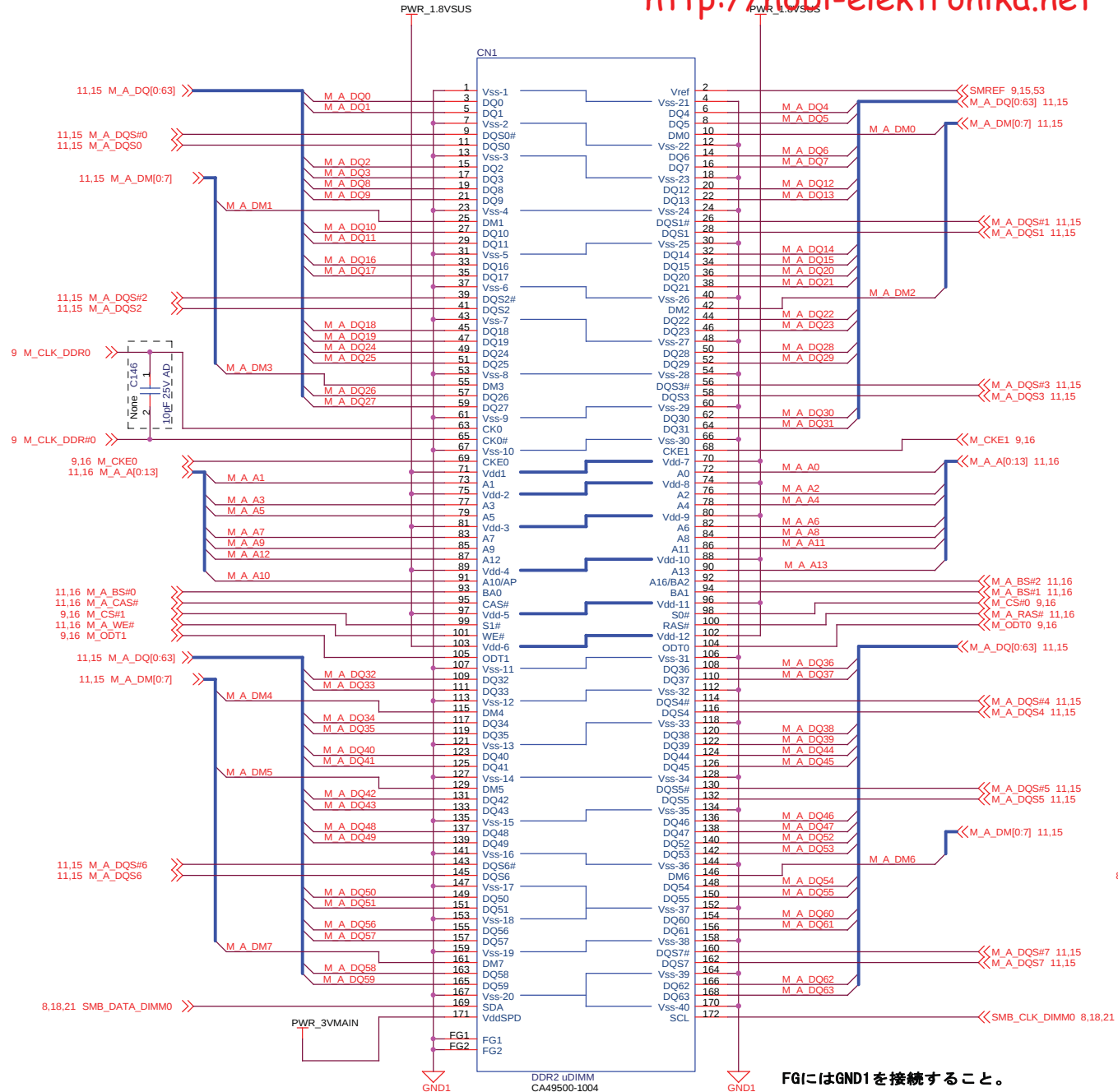
[Reference:Greek] G

										TITLE: Tiga Main board					
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REV1		DATE		DESIGN		CHECK		APPR.		DESCRIPTION					
DATE				DESIGN				CHECK				APPR.			
										FUJITSU LTD.				SHEET 12 / 66	



[GMCH-5 (POW2)]

					TITLE Tiga Main board	
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					CUST.	
REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION	FUJITSU LTD.
DATE		DESIGN	CHECK	APPR.		
					SHEET 13 / 66	

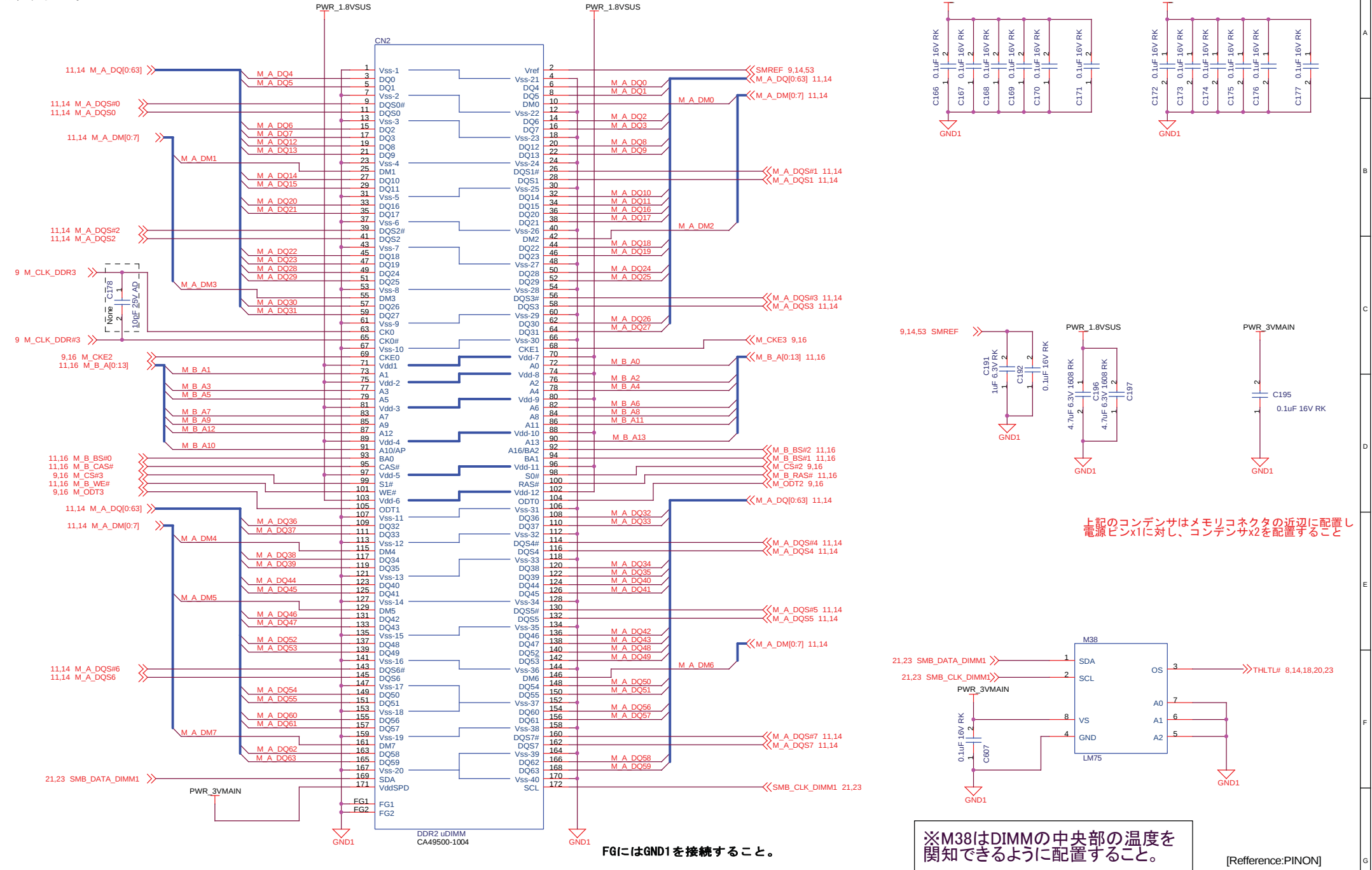


※M37はDIMMの中央部の温度を
関知できるように配置すること。

[DDR2 SLOTT0]

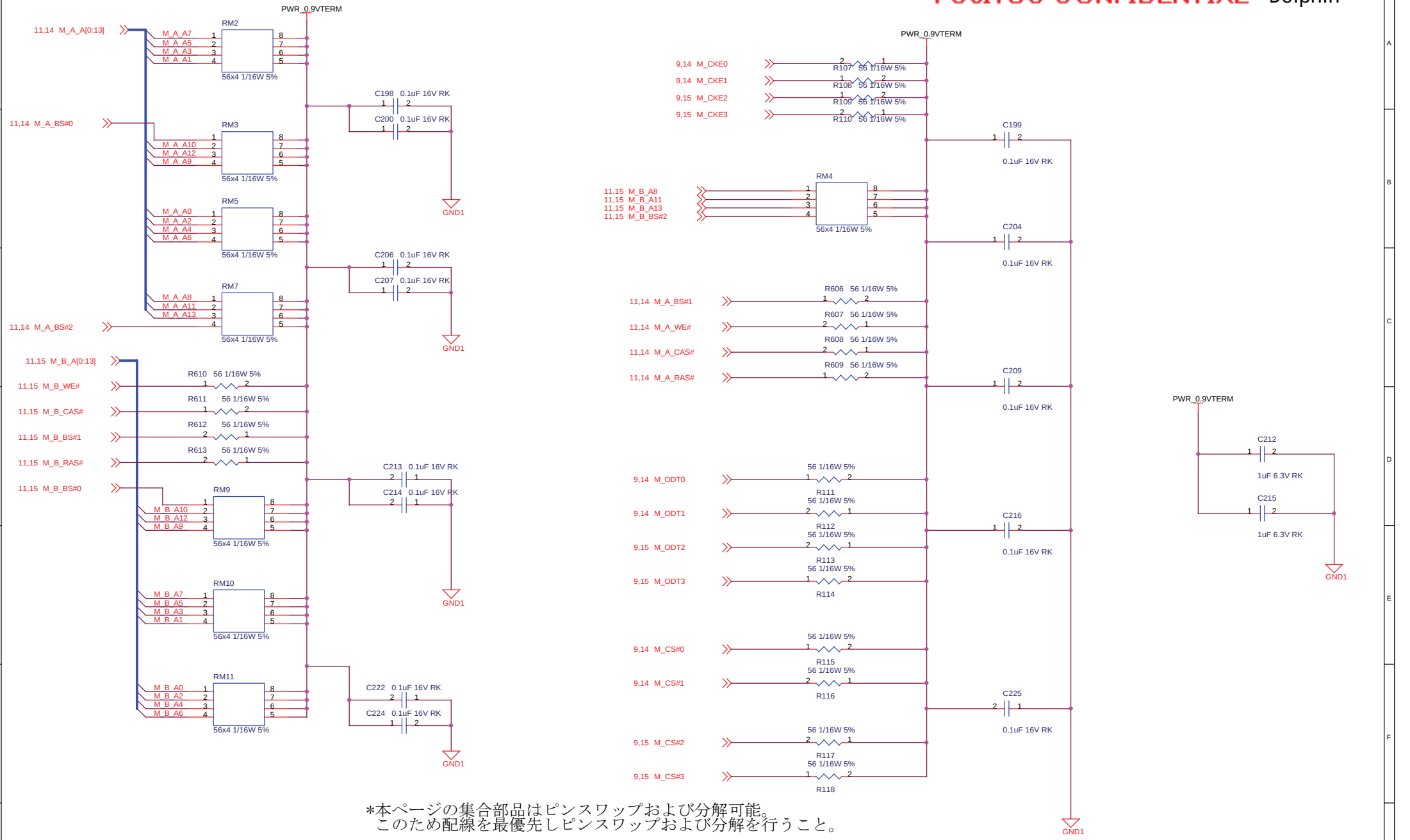
								[Reference:Pinon]	
								TITLE Tiga Main board	
								DRAW. NO. C1CP250040-X4	
								CUST.	
								FUJITSU LTD.	
								SHEET 14 / 66	

右記の抵抗はREF_MEMの
スタブが最小になるように
配置すること。



[DDR2 SLOT1]

TITLE				Tiga Main board	
DRAW. NO.				C1CP250040-X4	CUST.
DATE				DESIGN	15/66
REVISION				DATE	DESIGN
CHECK				DATE	DESIGN
APPR				DATE	DESIGN
DESCRIPTION				DATE	DESIGN
F				DATE	DESIGN
G				DATE	DESIGN
SHEET				15	66
FUJITSU LTD.					



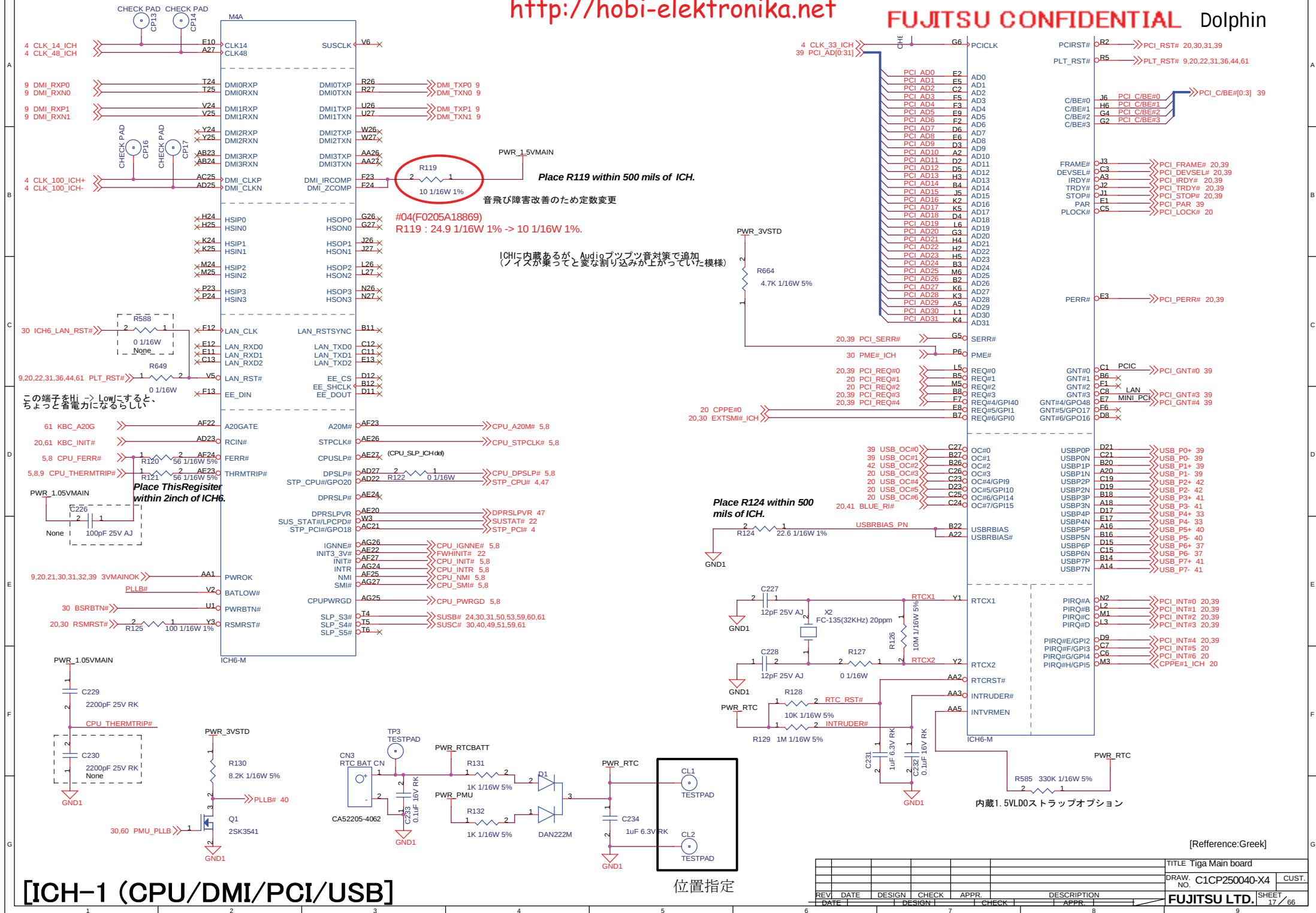
*本ページの集合部品はピンスワップおよび分解可能。
このため配線を最優先しピンスワップおよび分解を行うこと。

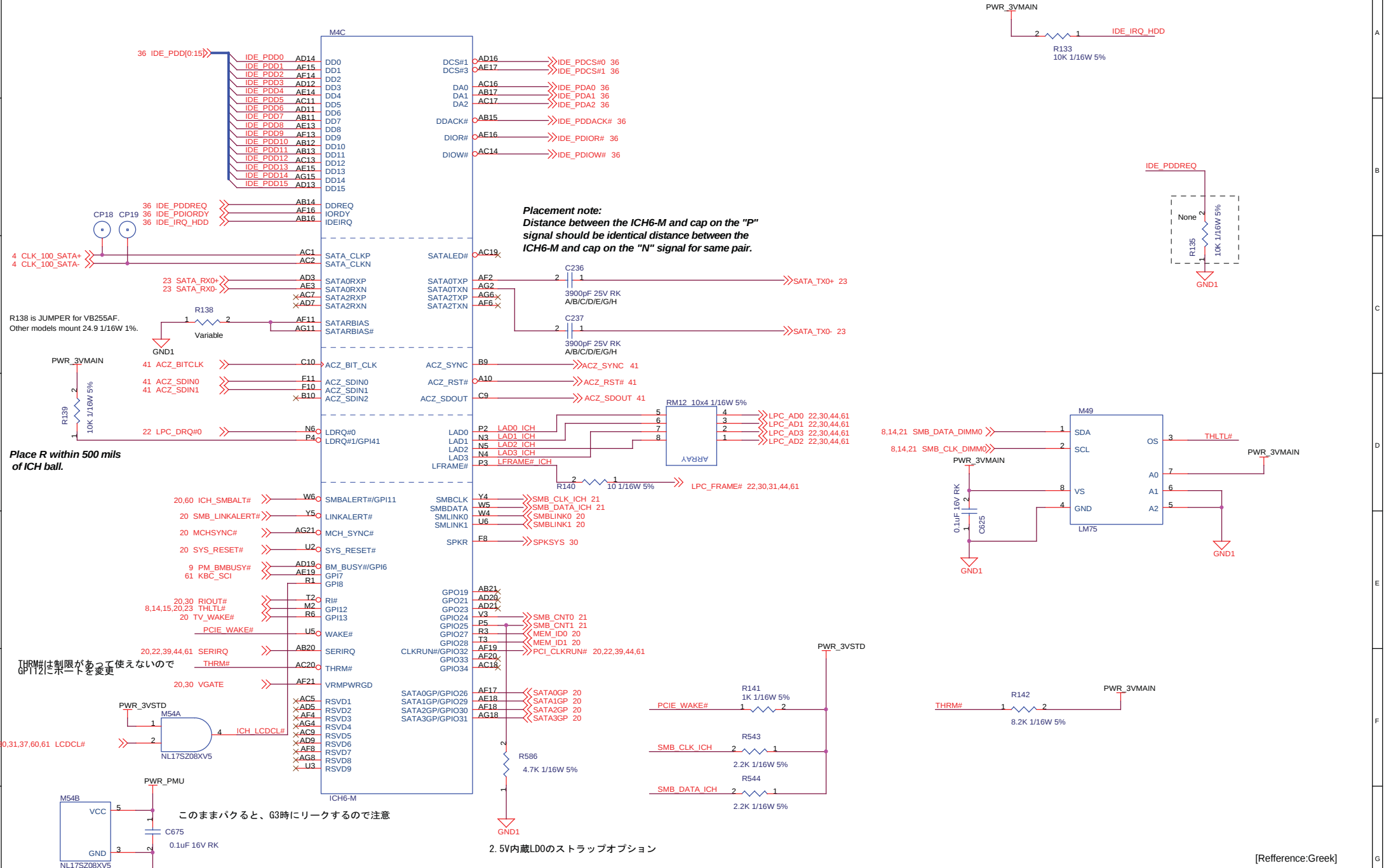
特に、アドレス部はモジュール間でのピン変更。集合部品の
分解および再集合が可能。

*本ページのパソコンは抵抗2つに対し1つ配置すること
(集合抵抗はx8, x4に対し、各々4つ, 2つ)

[DDR2 REF/TERM]

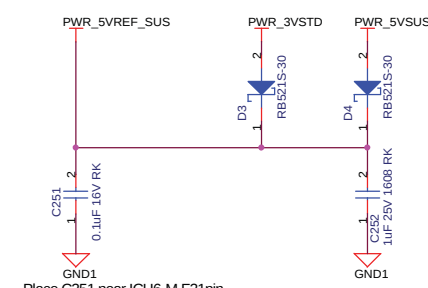
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REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION	FUJITSU LTD.	
DATE		DESIGN	CHECK	APPR.		SHEET 16 / 66	
		7		8		9	





[ICH-2 (SATA/PATA/AC97)]

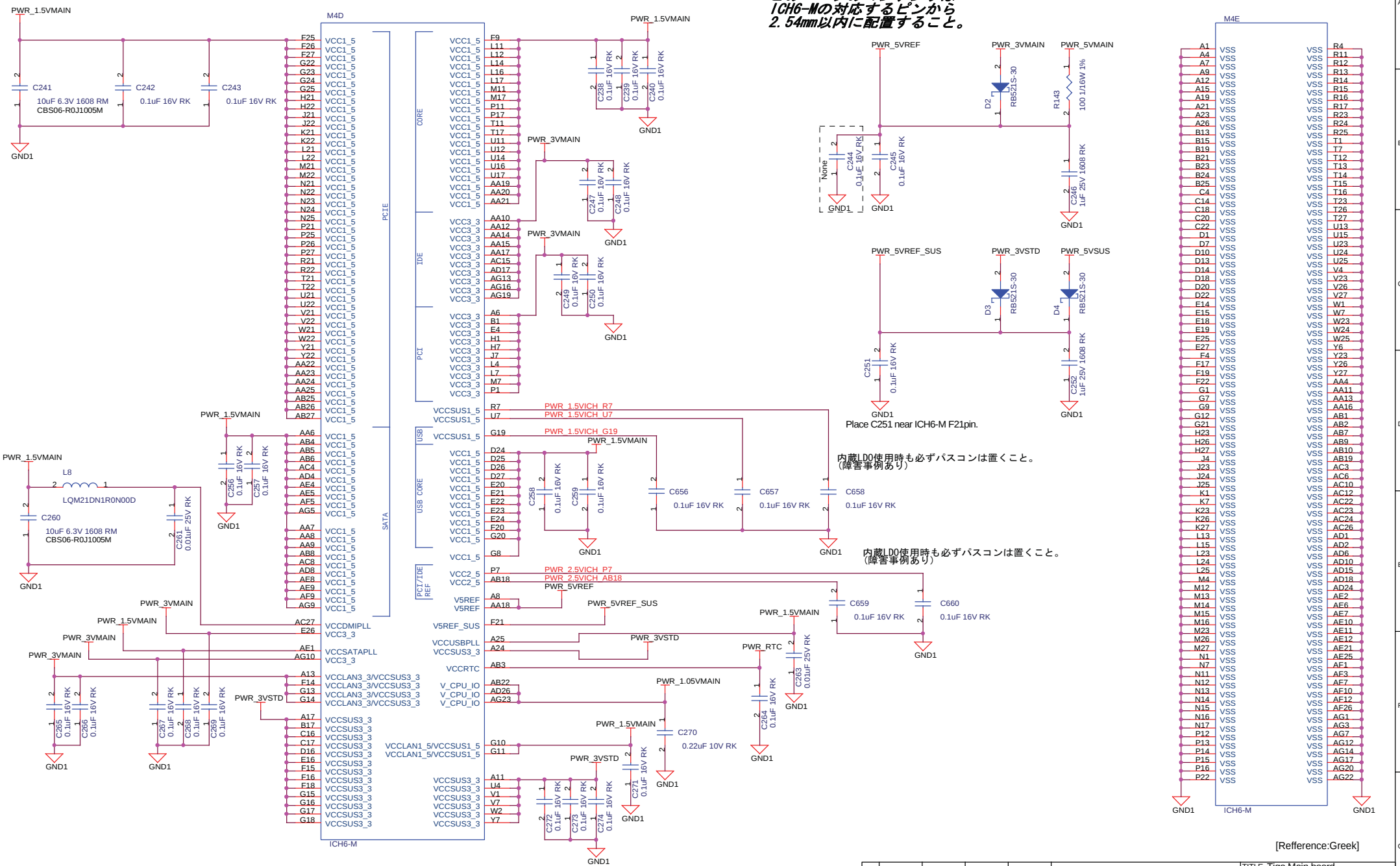
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REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION			
DATE		DESIGN		CHECK	APPR.	FUJITSU LTD.		SHEET 18 / 66
		7		8		9		



Place C251 near ICH6-M F21pin.

内蔵LD0使用時も必ずパソコンは置くこと。
(障害事例あり)

内蔵LDO使用時も必ずパスコンは置くこと。
(障害事例あり)

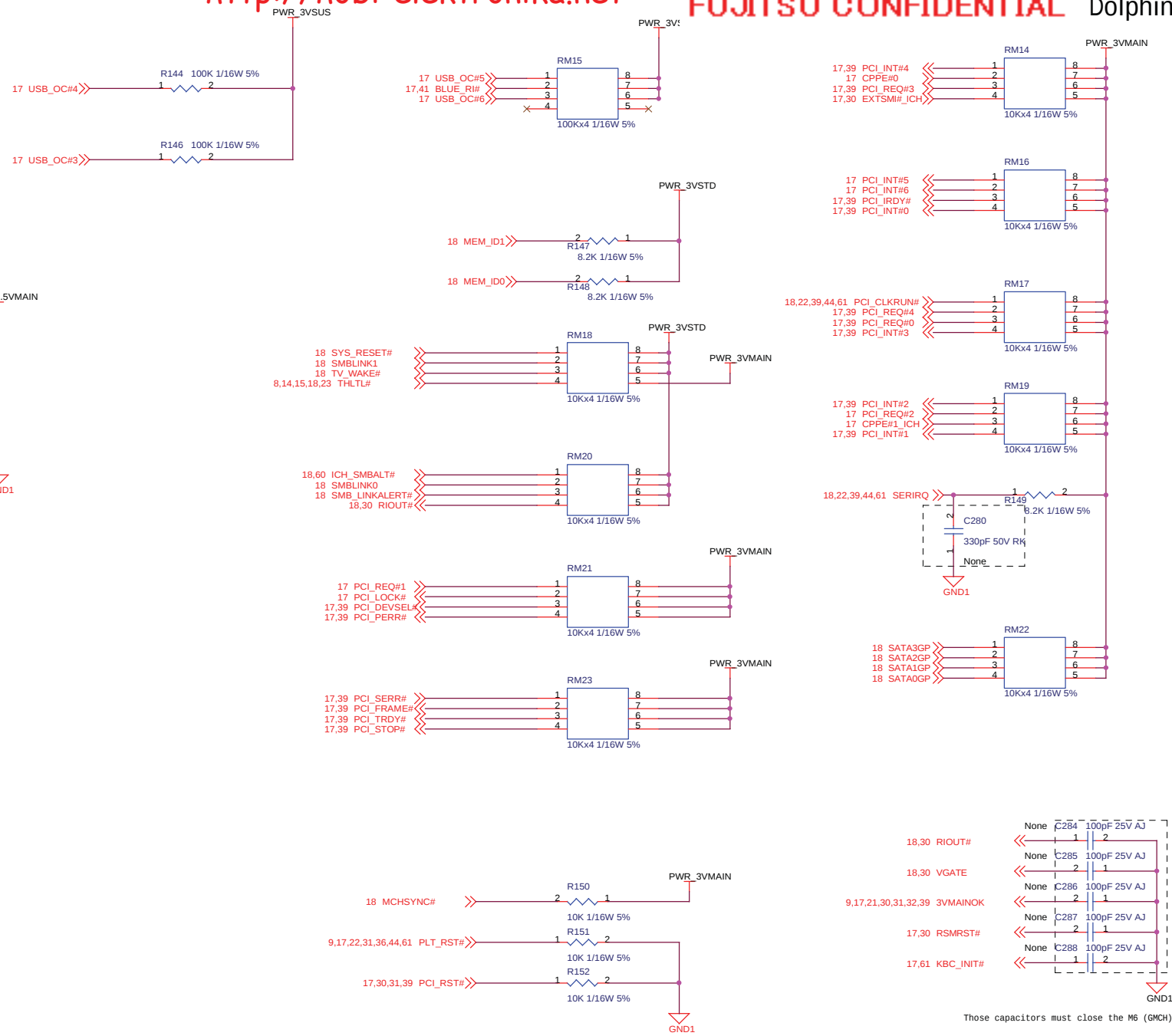


[Reference:Greek

[ICH-3 (POW)]

										TITLE Tiga Main board	
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										CUST.	
REV.	DATE	DESIGN	CHECK	APPR.	DESCRIPTION					SHEET	
DATE		DESIGN	CHECK	APPR.						19 / 66	
FUJITSU LTD.											

M7
ICH6-M

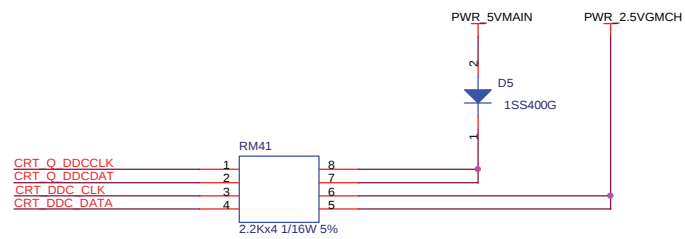
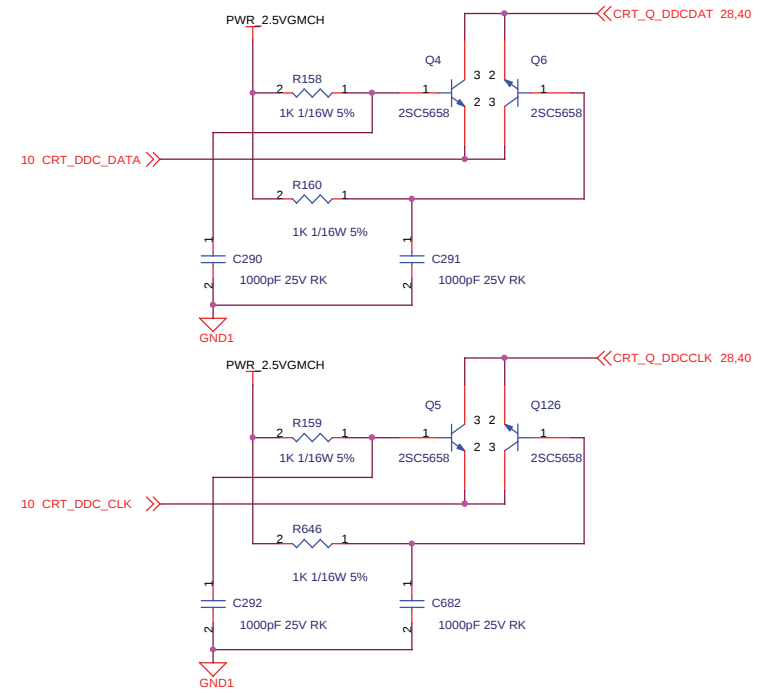
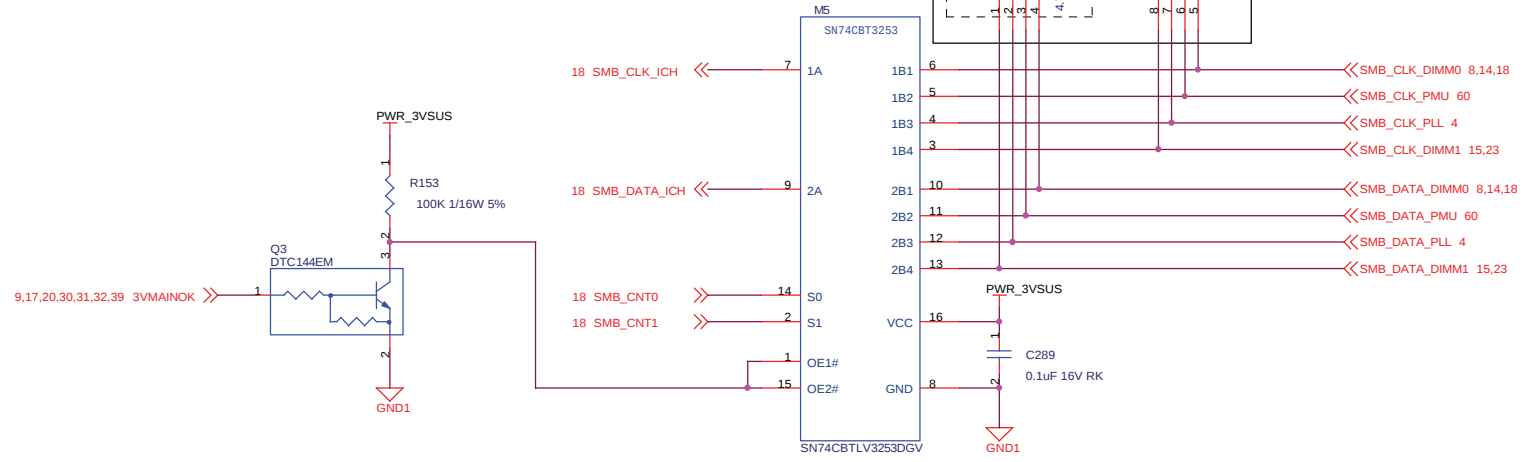


[ICH PU,CAP/PCI PU]

						TITLE TIGA Main board	
						DRAW. NO. C1CP250040-X4	CUST.
						FUJITSU LTD.	
REV	DATE	DESIGN	CHECK	APPR	DESCRIPTION	SHEET 20 / 66	
DATE		DESIGN		CHECK			

Those capacitors must close the M6 (GMCH)

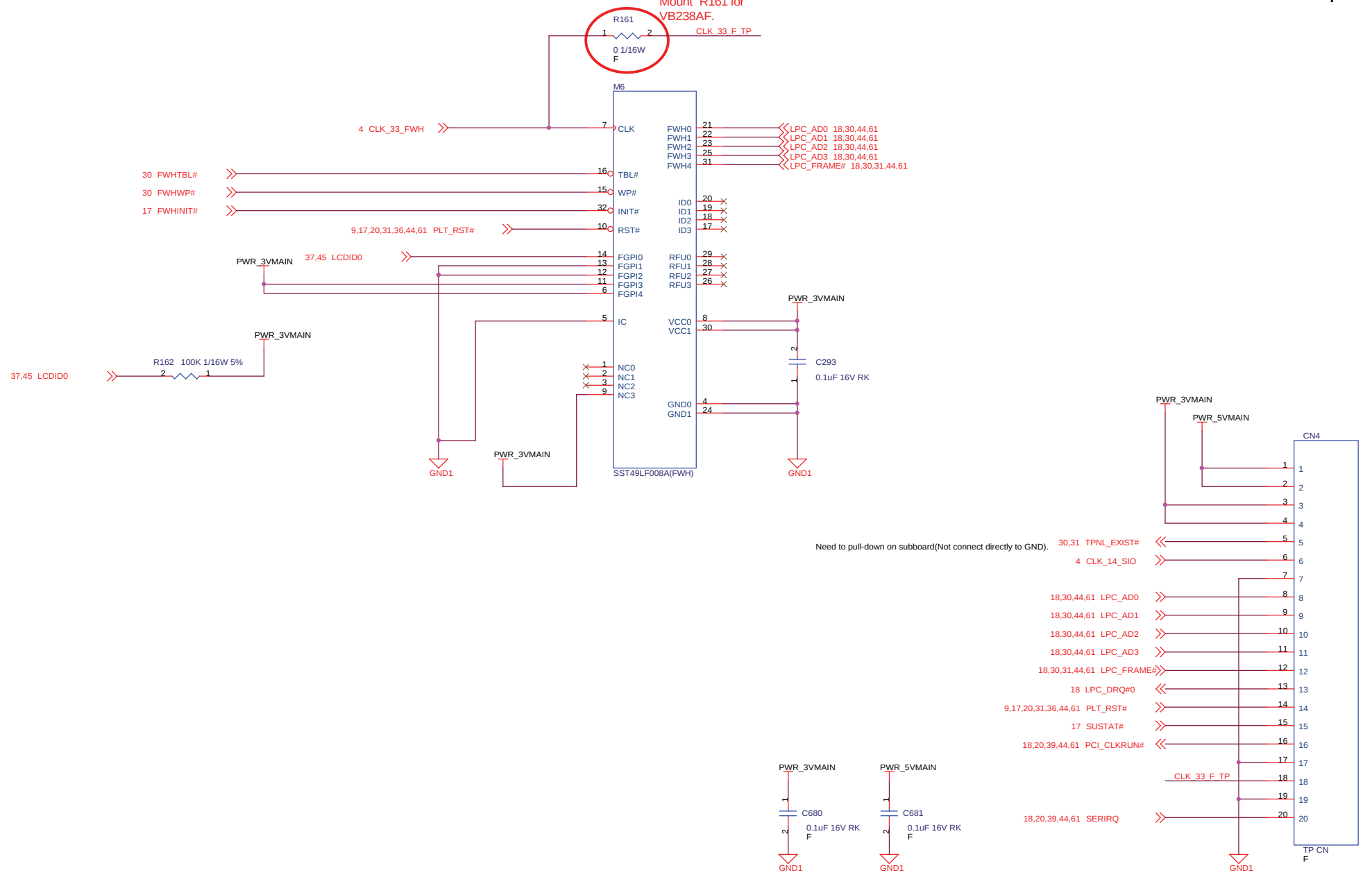
[Reference:Greek]



[SMBus]

						TITLE Tiga Main board	
						DRAW. NO. C1CP250040-X4	
						CUST.	
REV.	DATE	DESIGN	CHECK	APPR.	DESCRIPTION		
DATE	DESIGN		CHECK	APPR.	FUJITSU LTD.		SHEET 21 / 66

#00(F0205A19859)
Mount R161 for
VB238AF.

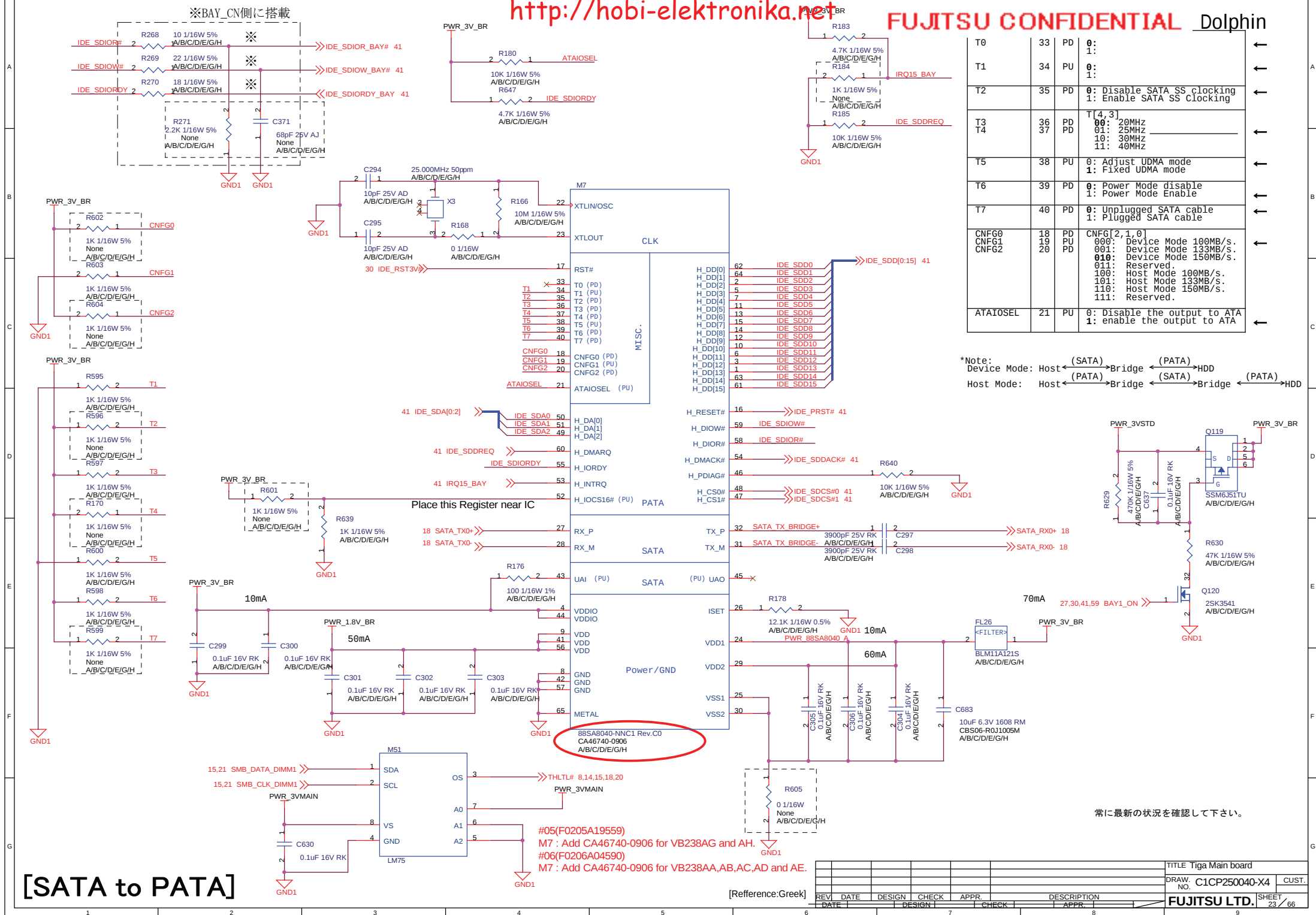


Need to pull-down on subboard(Not connect directly to GND).

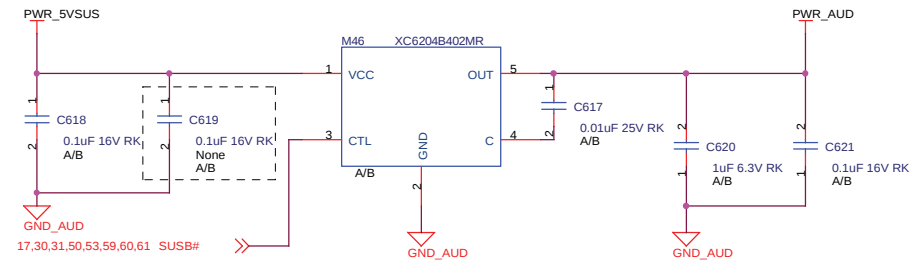
[Reference:Greek]

[FWH/TP]

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DATE		DESIGN	CHECK	APPR.	FUJITSU LTD.		
			7		8	9	SHEET 22 / 66

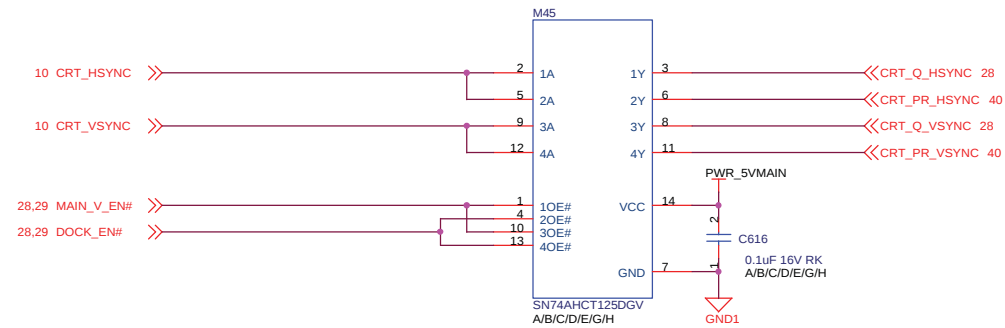


[SATA to PATA]



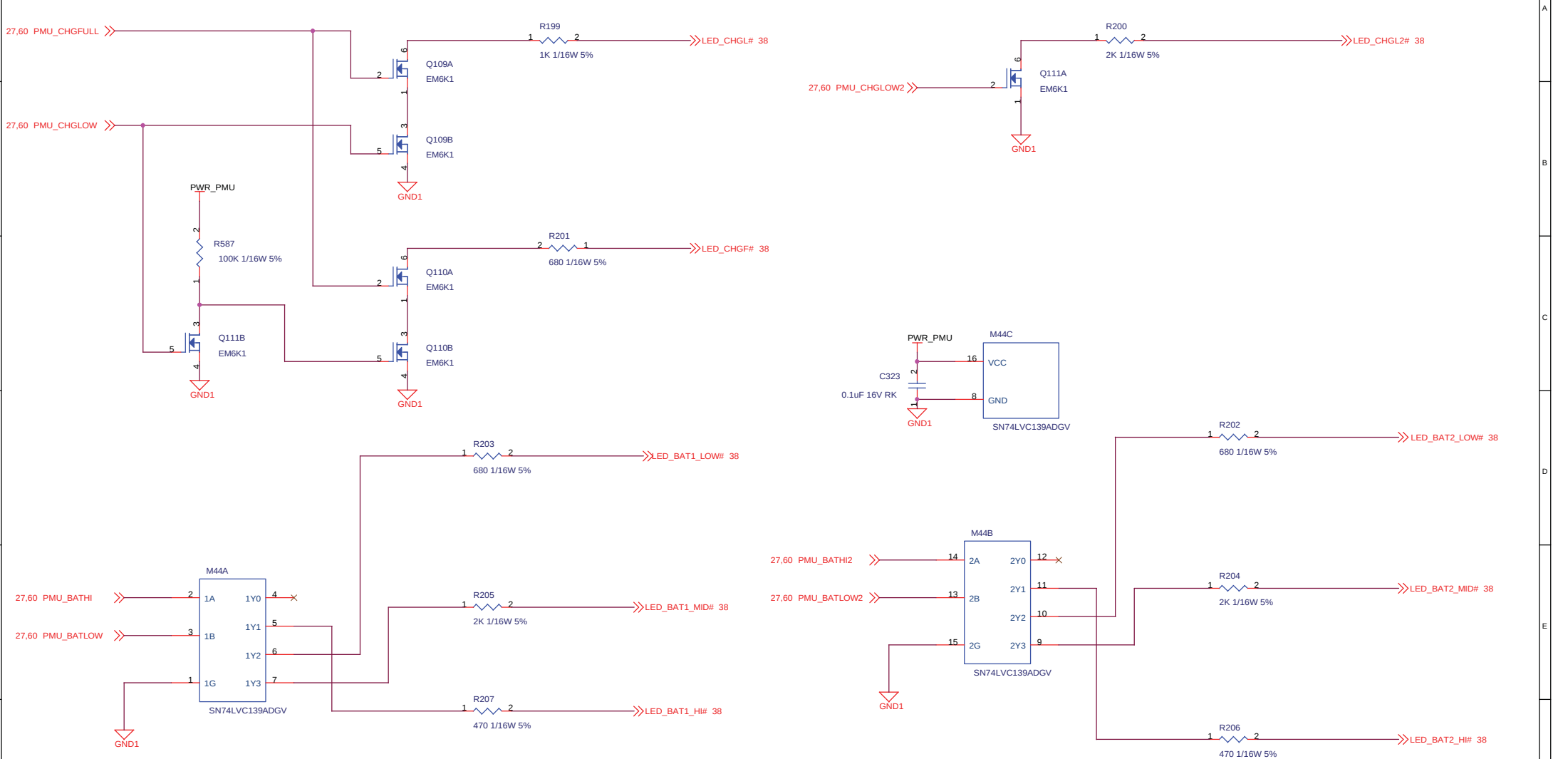
Int-Mic AMP

										TITLE Tiga Main board		
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REV.	DATE	DESIGN	CHECK	APPR.	DESCRIPTION							
DATE		DESIGN		CHECK		APPR.						
										FUJITSU LTD.		SHEET 24 / 66



[Level Shift Buffer]

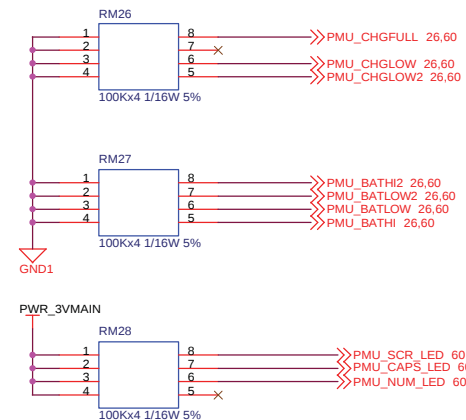
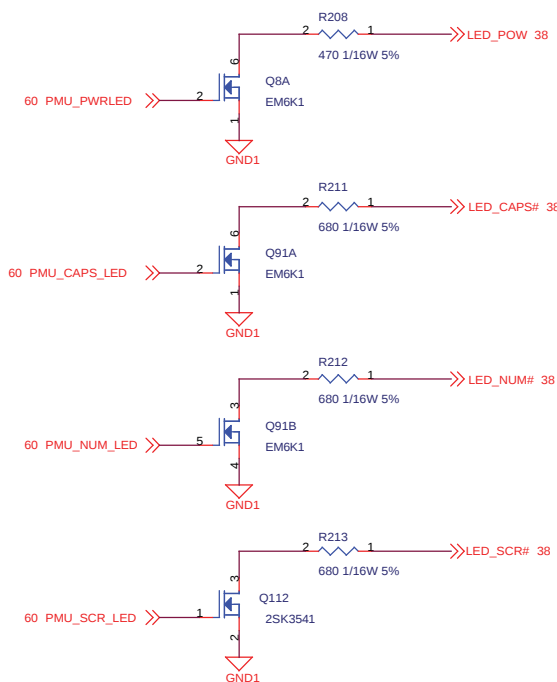
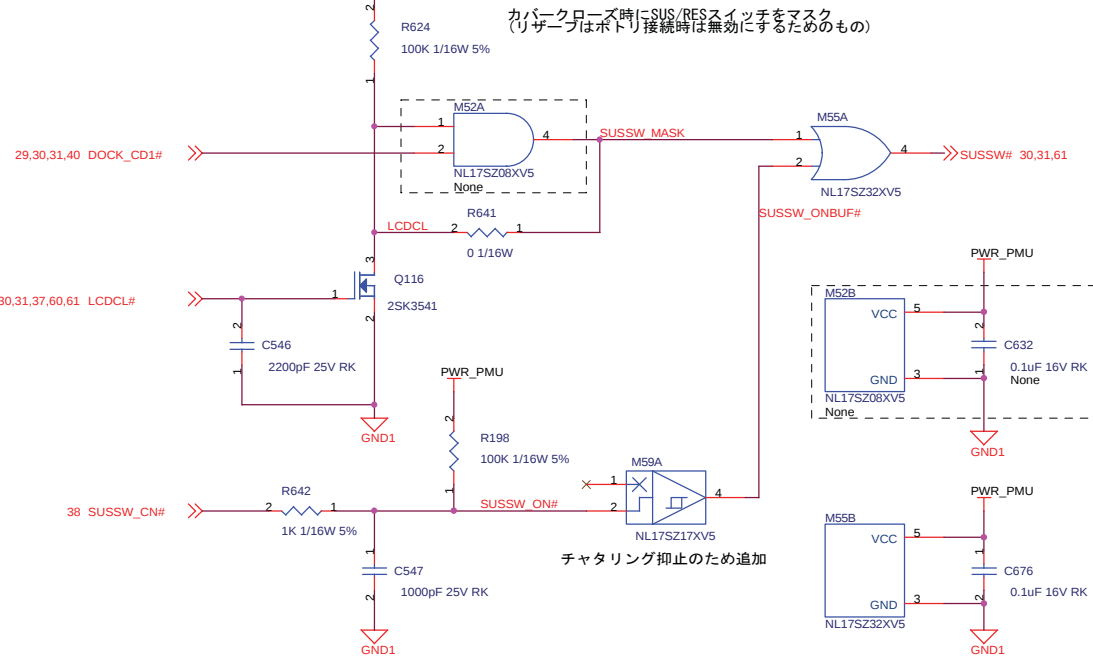
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REV	DATE	DESIGN	CHECK	APPR	DESCRIPTION	FUJITSU LTD.	
DATE		DESIGN		CHECK		APPR	SHEET 25 / 66



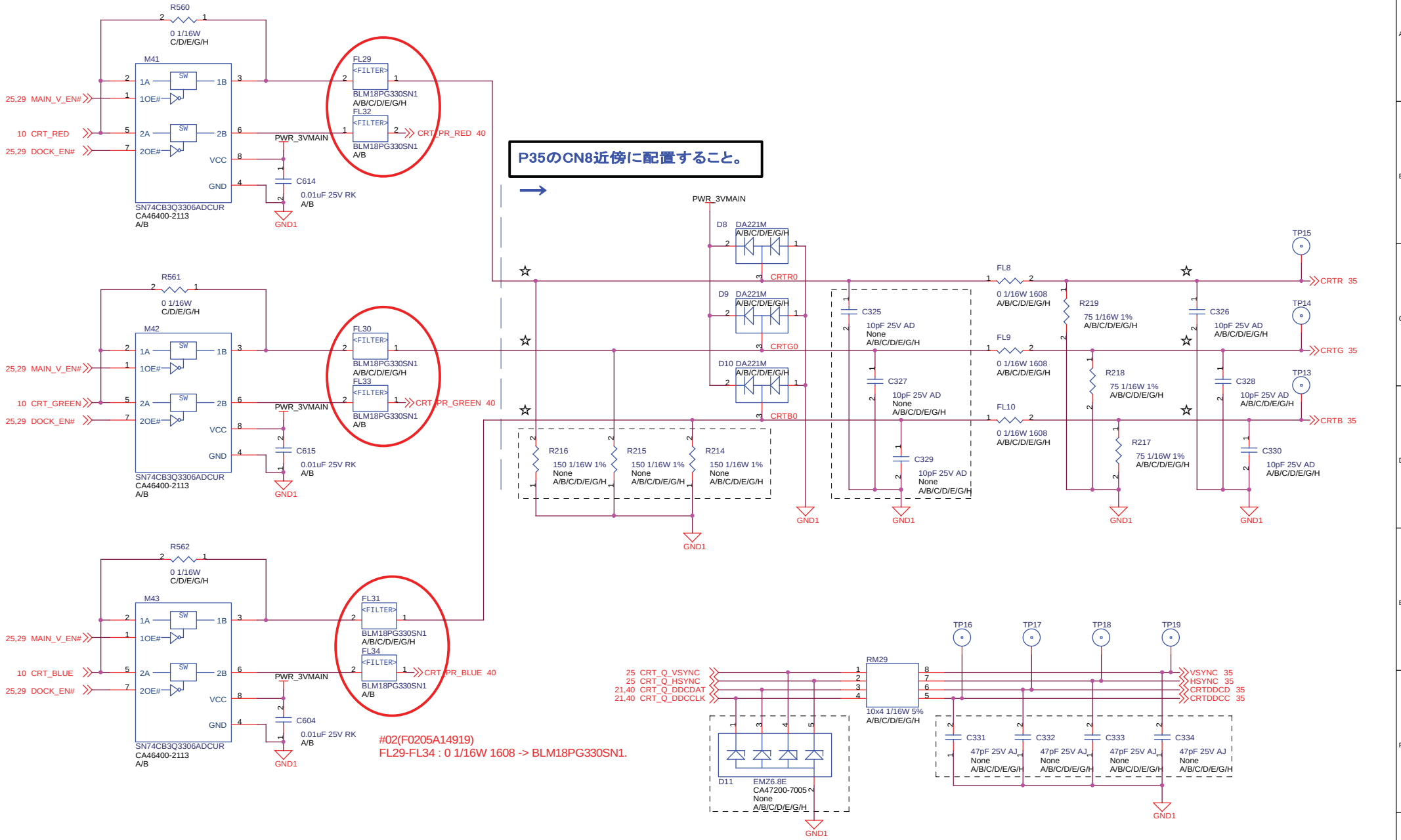
[Status LED Signal1]

REV	DATE	DESIGN	CHECK	APPR	DESCRIPTION	TITLE Tiga Main board
NO.	NO.	NO.	NO.	NO.	NO.	DRAW. NO. C1CP250040-X4 CUST.
DATE	DATE	DESIGN	CHECK	APPR	APPR	FUJITSU LTD. SHEET 26 / 66

カバークローズ時にSUS/RESスイッチをマスク
(リザーブはボトリ接続時は無効にするためのもの)



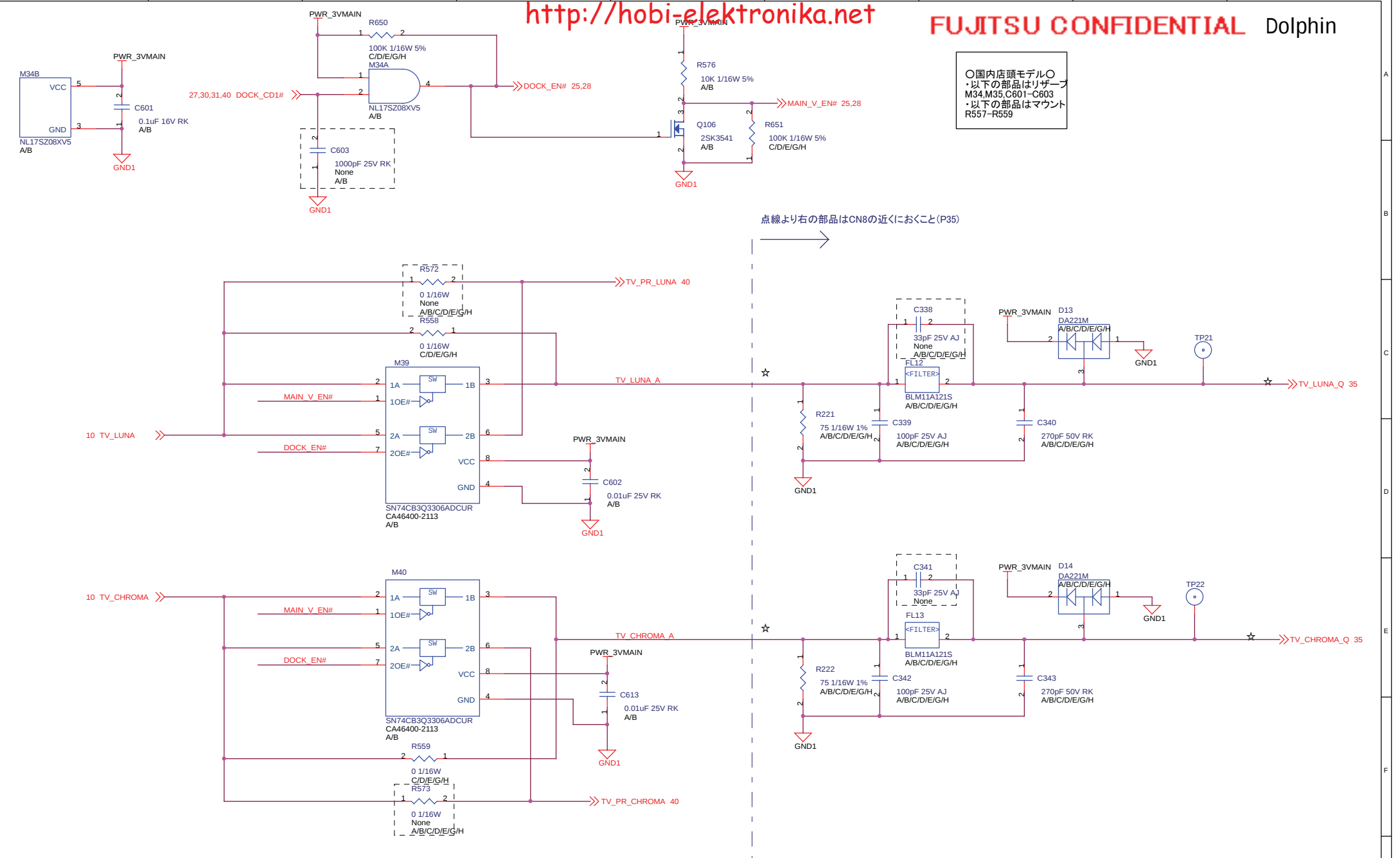
										TITLE Tiga Main board			
										DRAW. NO. C1CP250040-X4		CUST.	
REV	DATE	DESIGN	CHECK	APPR	DESCRIPTION								
DATE		DESIGN		CHECK		APPR						FUJITSU LTD.	SHEET 27 / 66



[CRT]

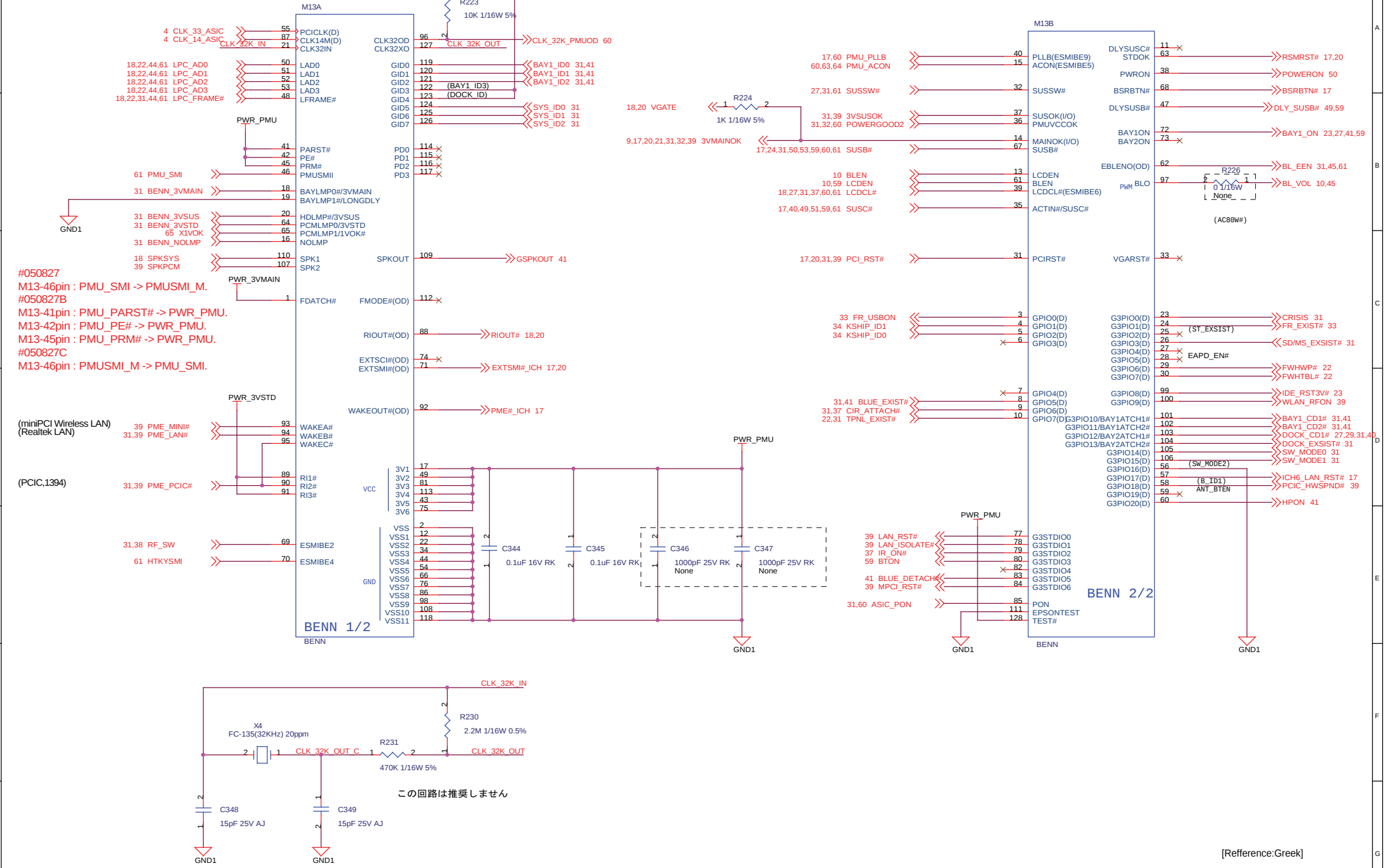
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○国内店頭モデル○
・以下の部品はリザーブ
M34,M35,C601-C603
・以下の部品はマウント
R557-R559



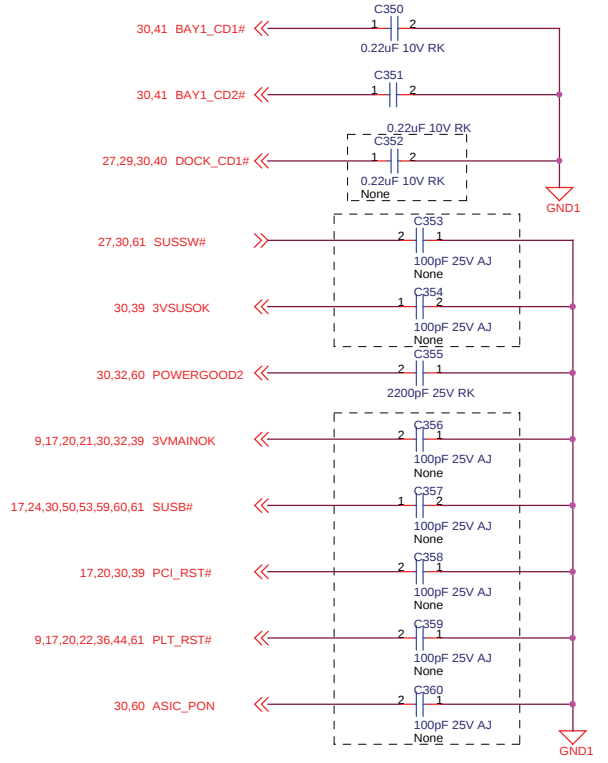
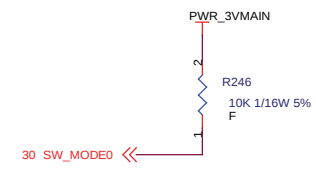
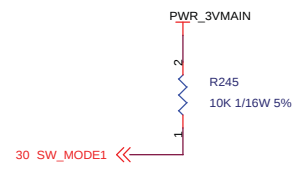
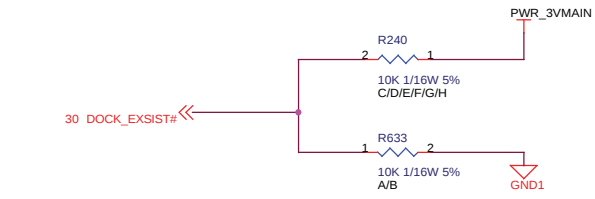
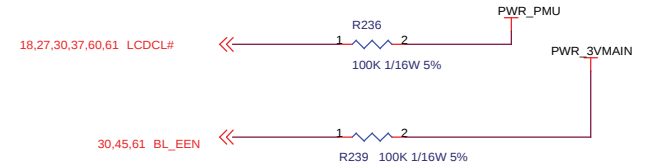
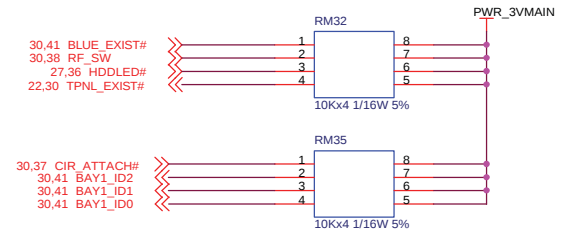
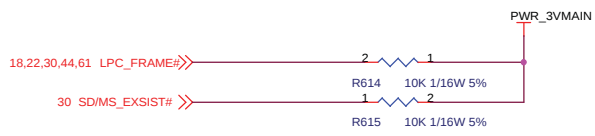
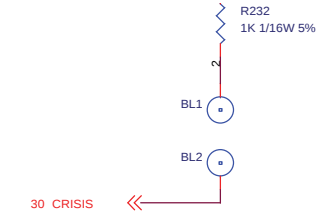
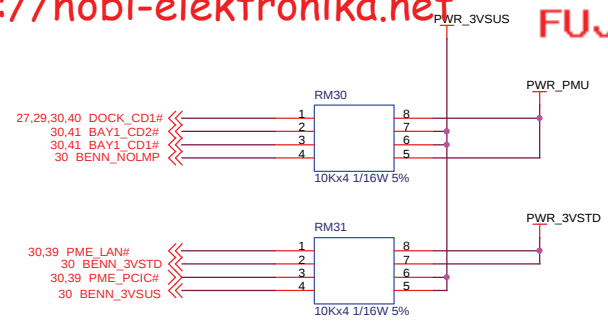
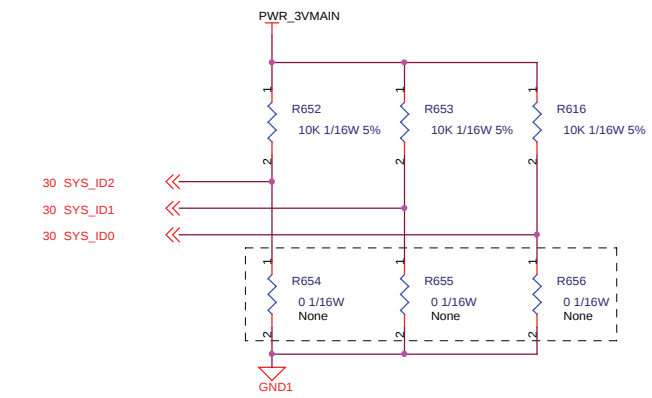
[S-out]

TITLE TIGA Main board							
DRAW. NO. C1CP250040-X4 CUST.							
FUJITSU LTD. SHEET 29 / 66							
REV	DATE	DESIGN	CHECK	APPR	DESCRIPTION		



[ASIC]

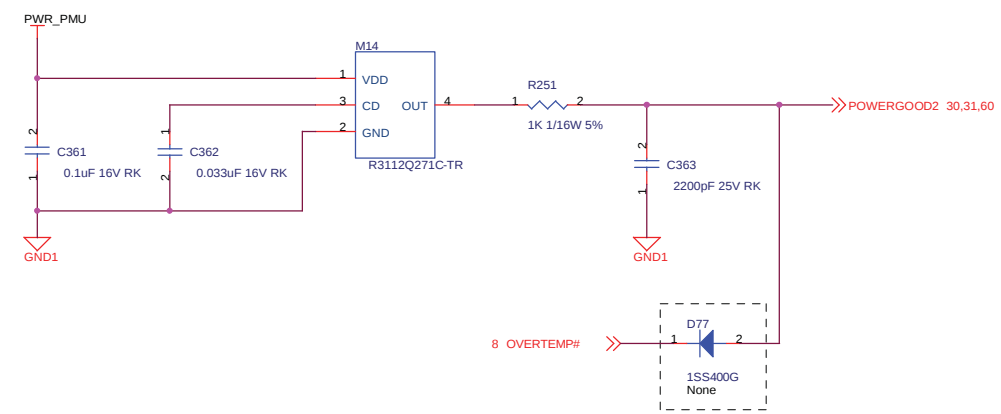
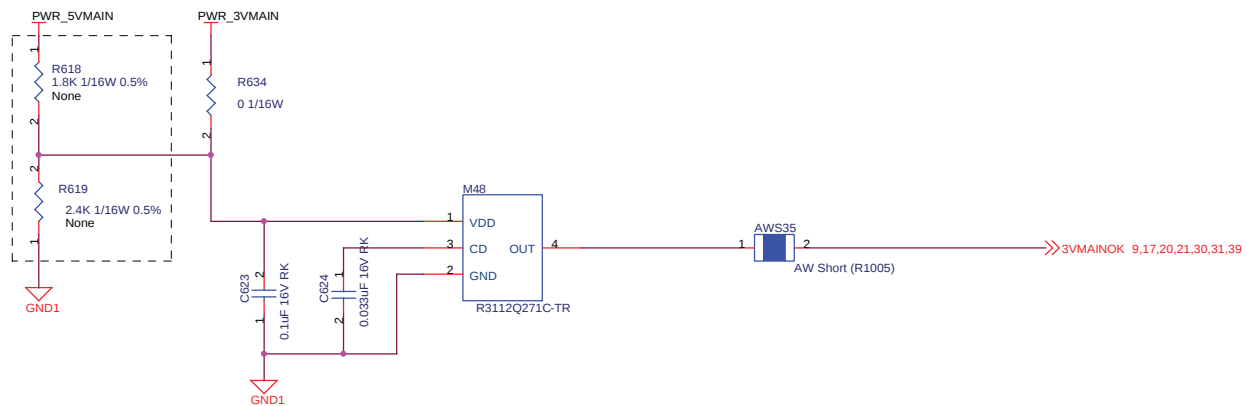
						[Reference:Greek]	
						TITLE TIGA Main board	
						DRAW. NO. C1CP250040-X4	
						CUST.	
						FUJITSU LTD.	
						SHEET 30 / 66	



[ASIC PU]

SW_MODE[2,0]
000 : Security SW搭載
001 : APPLI -SW
搭載 (店頭モデル)
010 : TVボタン搭載
011 : SW無しモデル

										TITLE Tiga Main board			
										DRAW. NO. C1CP250040-X4		CUST.	
										FUJITSU LTD.		SHEET 31 / 66	
REV		DATE		DESIGN		CHECK		APPR.		DESCRIPTION			
DATE				DESIGN		CHECK		APPR.					
				7						8		9	

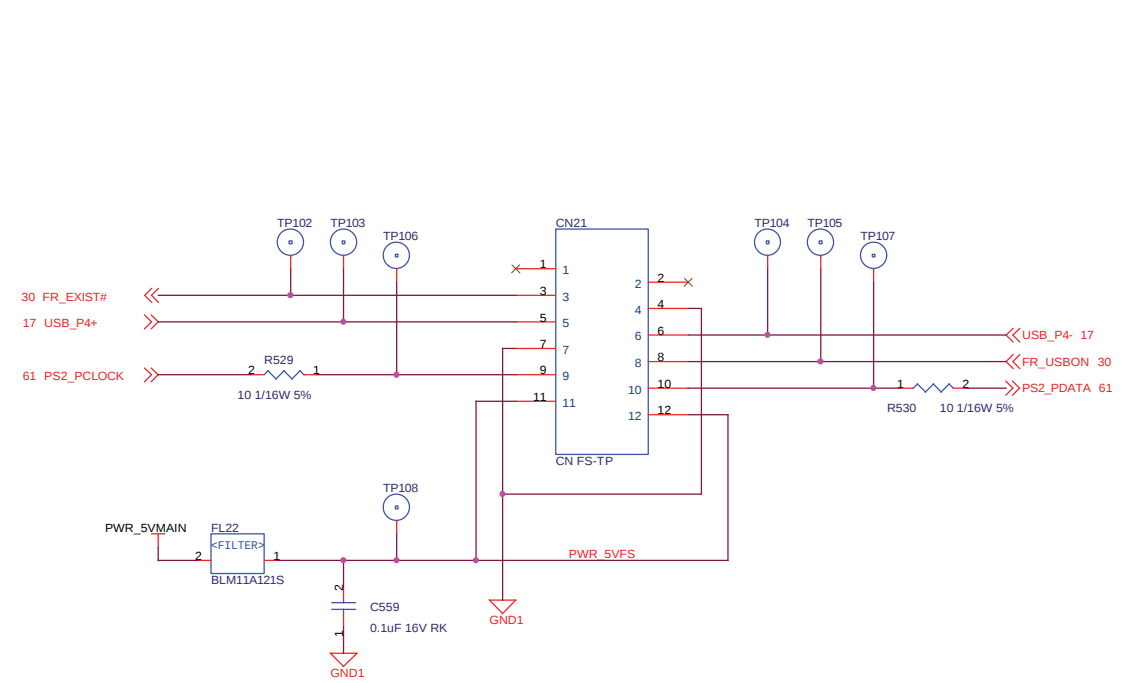


[RESET IC]

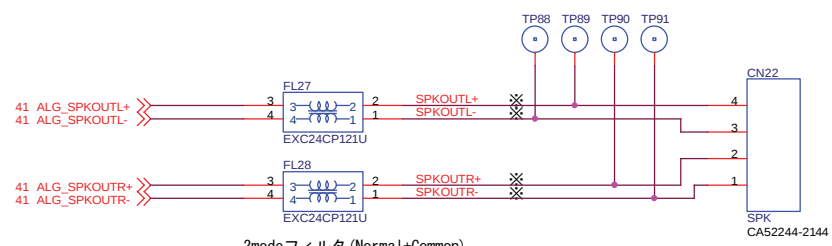
[Reference:Greek]

						TITLE Tiga Main board	
						DRAW. NO. C1CP250040-X4	CUST.
REV	DATE	DESIGN	CHECK	APPR	DESCRIPTION	FUJITSU LTD.	
DATE		DESIGN		CHECK		APPR	SHEET 32 / 66

こっちにプルアップを置いておくと、LUNA側に5V引っ張らなくて良い



制御していない

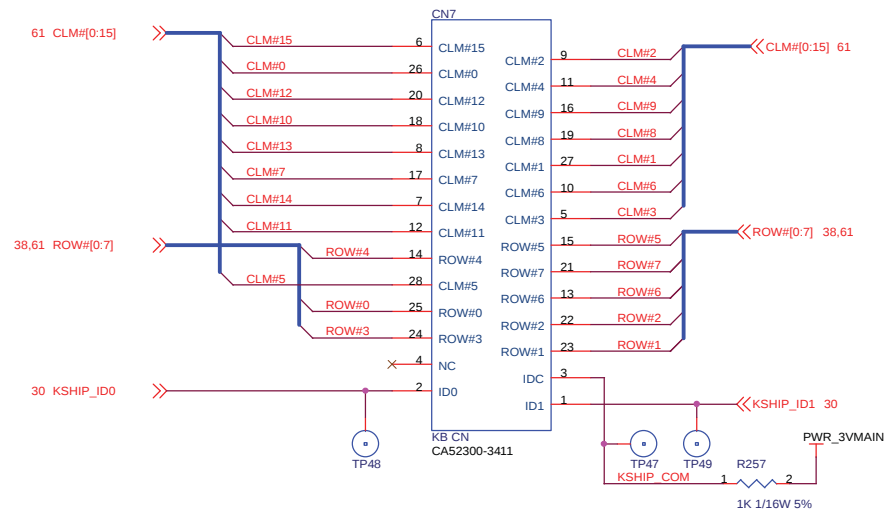


2modeフィルタ (Normal+Common)
ケータイを近づけた時にノイズを拾うような場合には効果あり

[CN FS_TP-SPK]

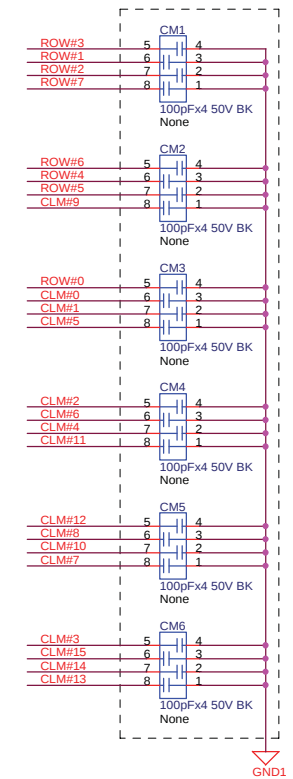
						TITLE Tiga Main board	
						DRAW. NO. C1CP250040-X4	CUST.
REV	DATE	DESIGN	CHECK	APPR	DESCRIPTION	FUJITSU LTD.	
DATE		DESIGN		CHECK		SHEET 33 / 66	

KeyBoard Connector



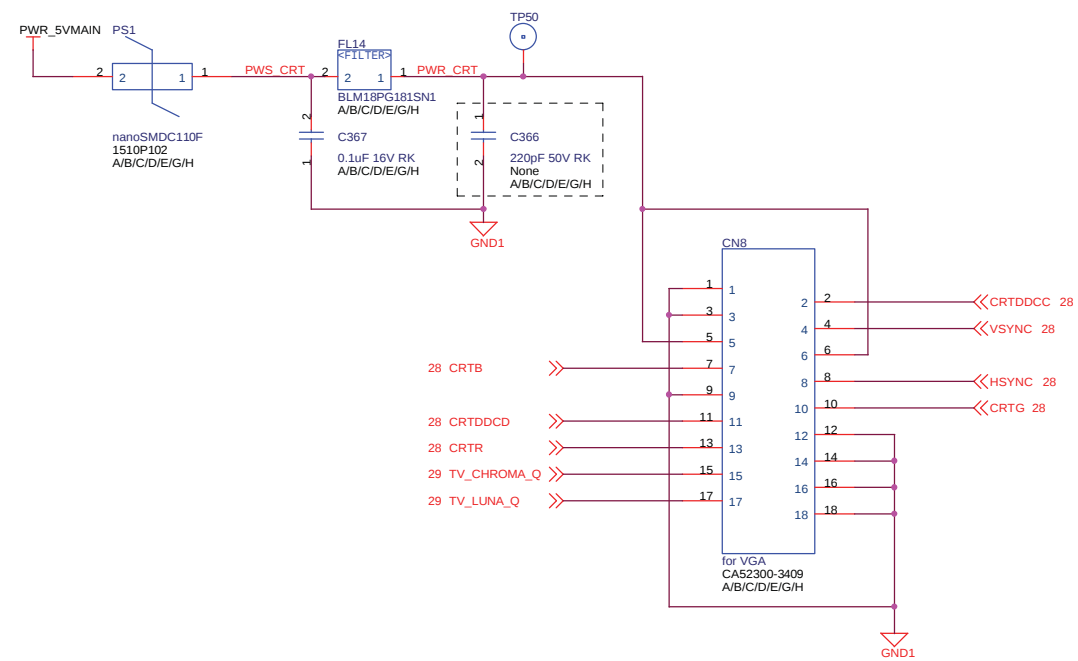
TPはコネクタからはなれた場所でもかまいません。
ただし、すべて同一面に搭載すること。

Keyboard Strap (N86C-7664-0203-E)
ID1: ID0 (KBC Side)
JP 1 1
US 1 0
UK 0 1



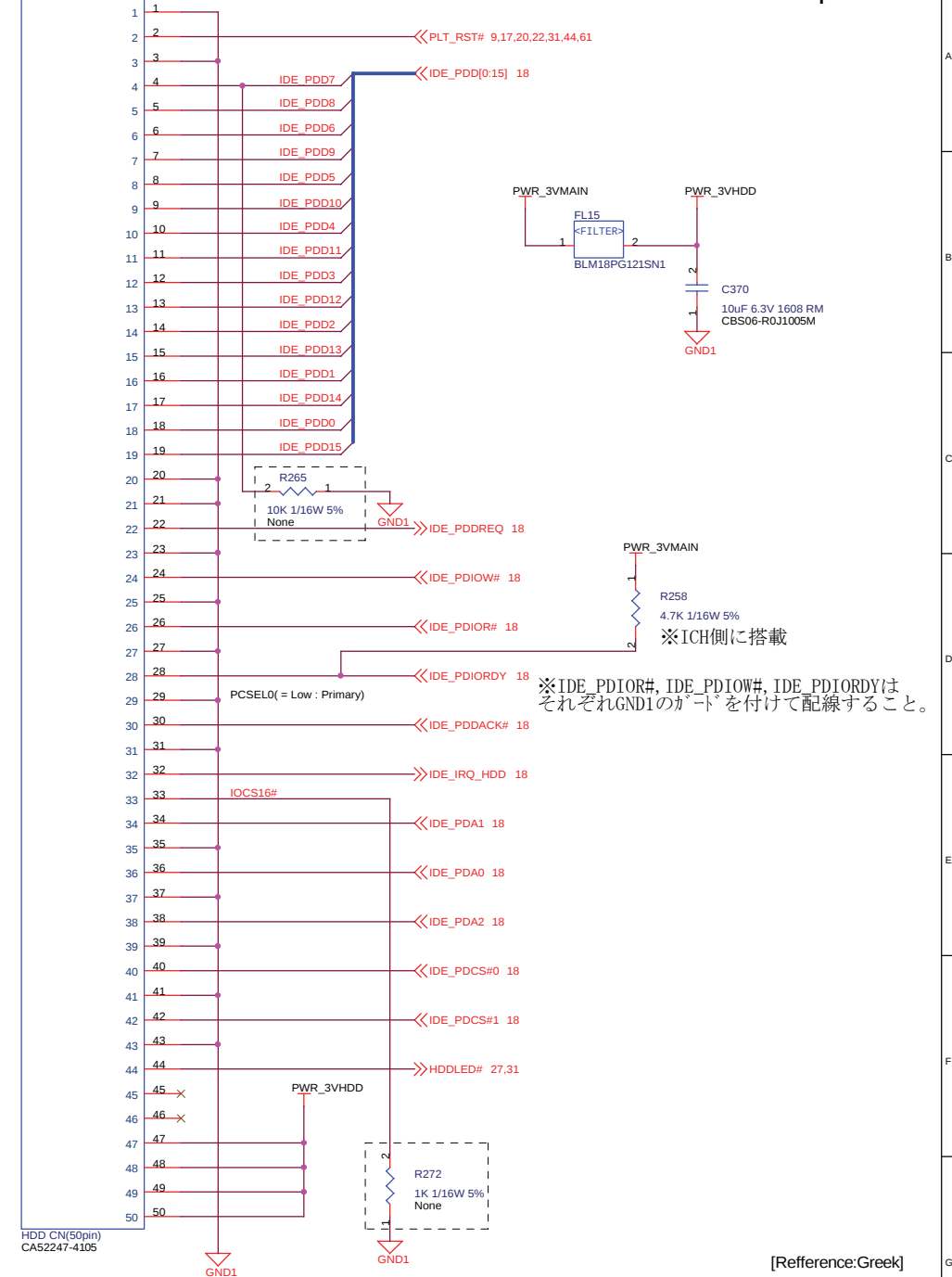
[CN Keyboard]

						[Reference:Zest]	
						TITLE Tiga Main board	
						DRAW. NO. C1CP250040-X4	
						CUST.	
						FUJITSU LTD.	
						SHEET 34 / 66	



[CN VGA/S-out]

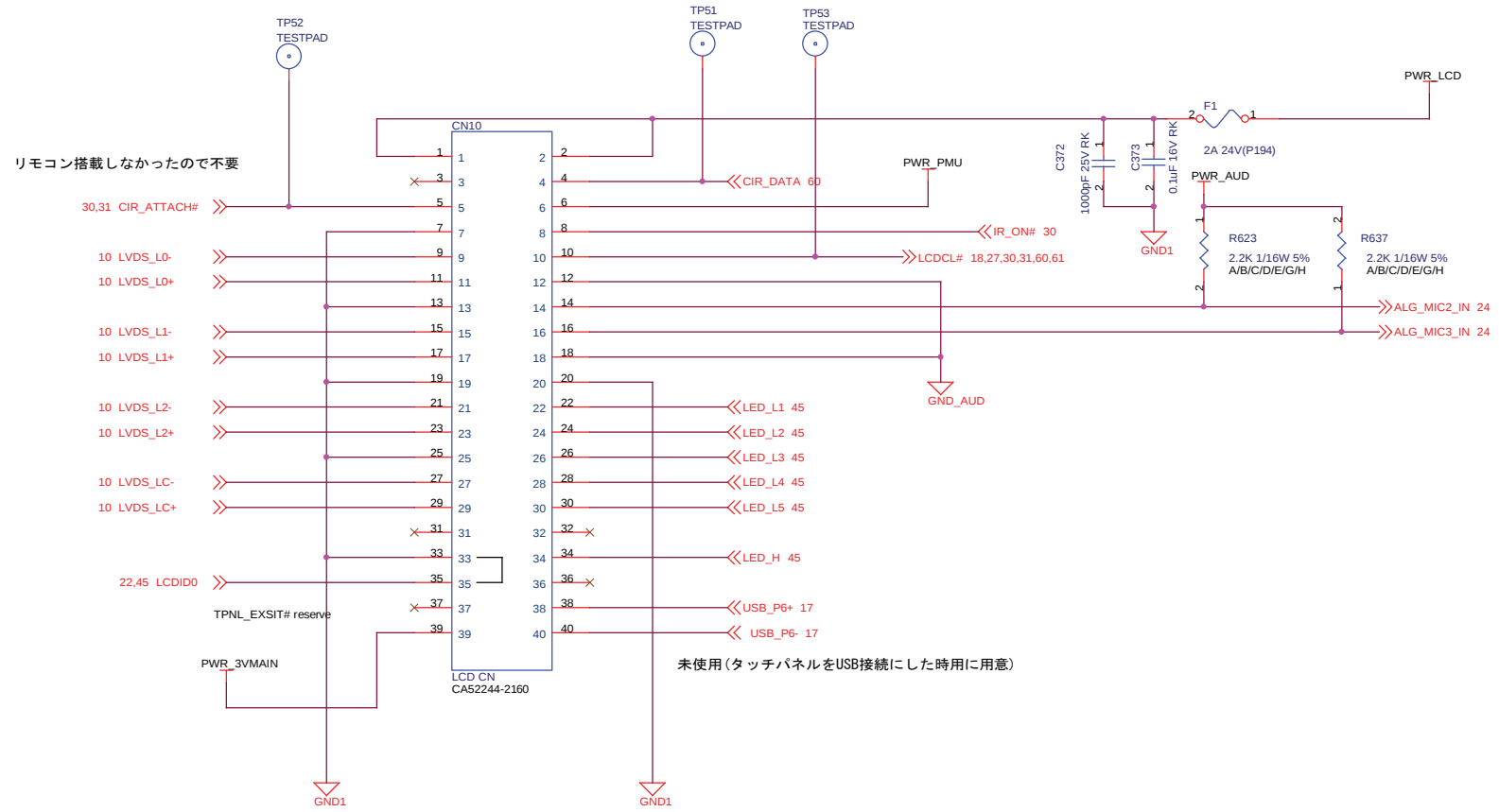
REV	DATE	DESIGN	CHECK	APPR	DESCRIPTION	TITLE	Draw. No.	CUST.
						Tiga Main board	C1CP250040-X4	
DATE		DESIGN	CHECK	APPR		FUJITSU LTD.	SHEET	35 / 66



[CN HDD(PATA)]

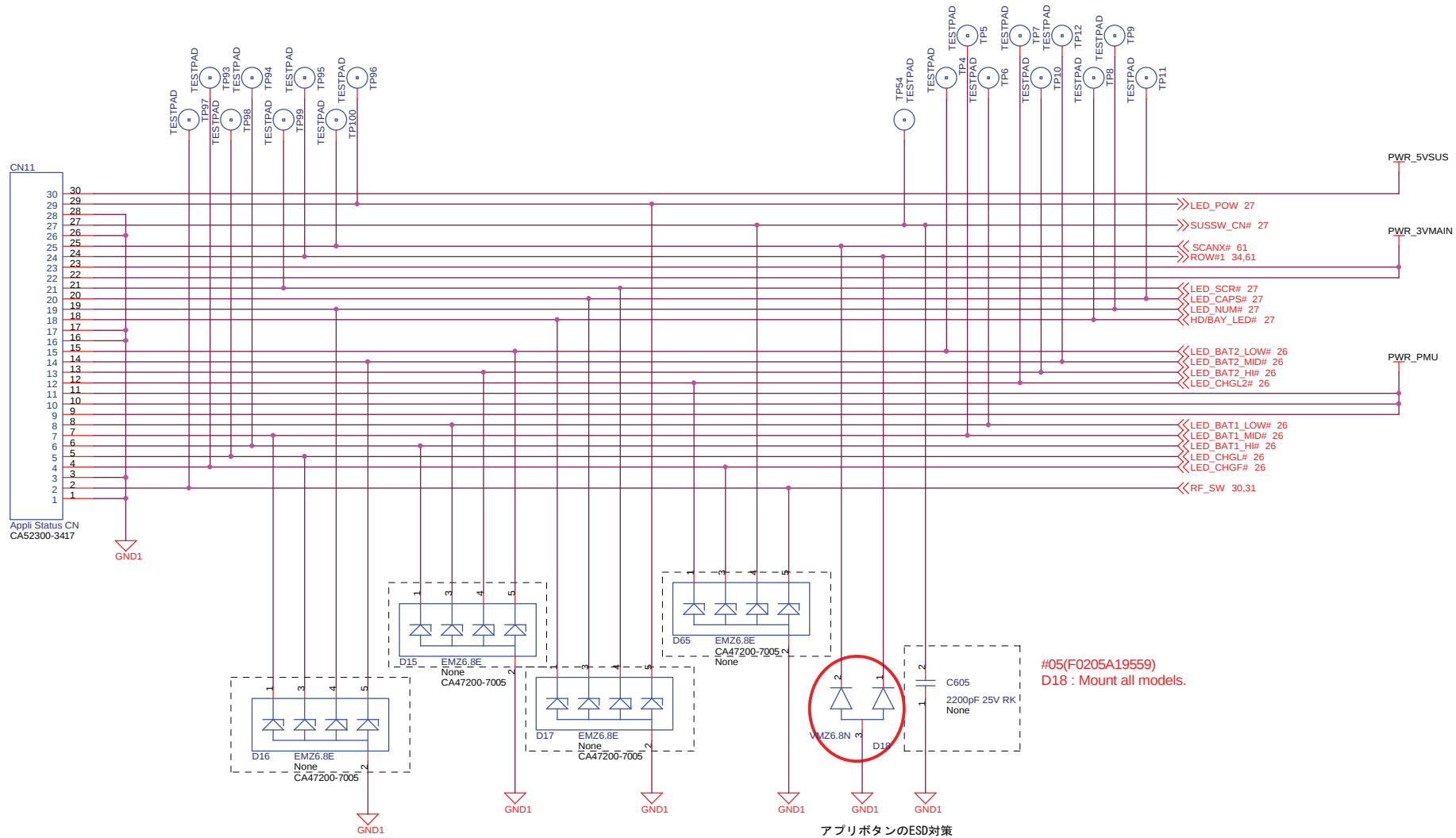
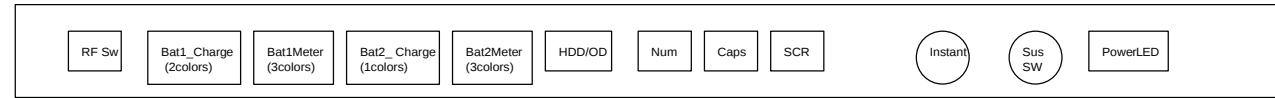
[Reference:Greek]

						TITLE Tiga Main board	
						DRAW. NO. C1CP250040-X4	CUST.
REV	DATE	DESIGN	CHECK	APPR	DESCRIPTION	FUJITSU LTD.	
DATE		DESIGN		CHECK		36	66



[CN LCD INV]

REV	DATE	DESIGN	CHECK	APPR	DESCRIPTION	TITLE	Draw. NO.	CUST.
1						Tiga Main board	C1CP250040-X4	
DATE		DESIGN	CHECK	APPR		FUJITSU LTD.	SHEET	37 / 66

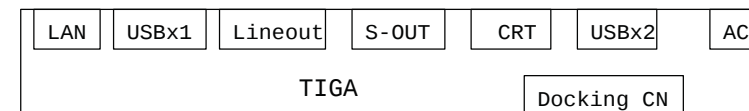


アプリボタンのESD対策

[Reference:Pumpkin]

[CN APPLI ST-LED]

TITLE Tiga Main board						DRAW. NO. C1CP250040-X4		CUST.
REV. DATE DESIGN CHECK APPR. DESCRIPTION						FUJITSU LTD.		SHEET 38 / 66

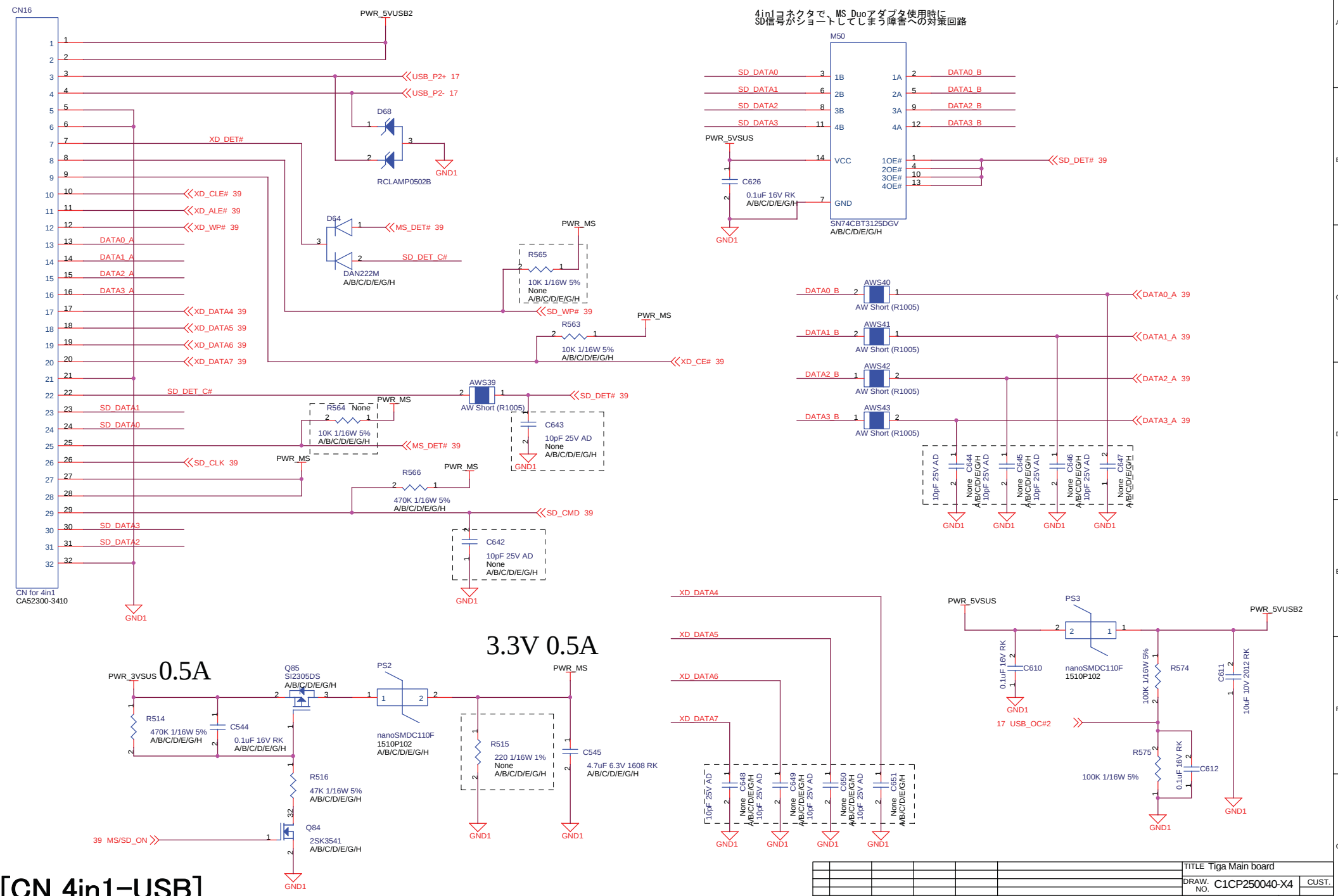


[CN DOCK]

										TITLE Tiga Main board	
										DRAW. NO. C1CP250040-X4	
										CUST.	
REV.	DATE	DESIGN	CHECK	APPR.	DESCRIPTION					FUJITSU LTD.	
DATE		DESIGN	CHECK	APPR.							
6										7	
										8	
										9	
										SHEET 40 / 66	



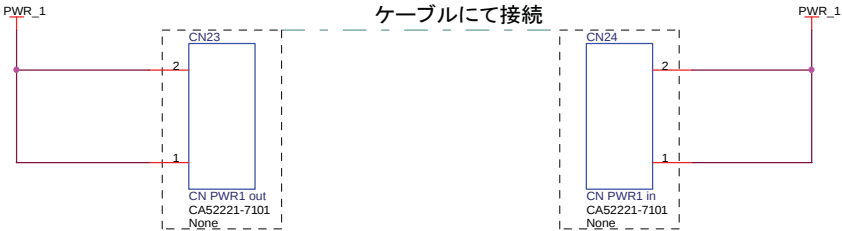
										TITLE Tiga Main board	
										DRAW NO. C1CP250040-X4	
										CUST	
REV	DATE	DESIGN	CHECK	APPR	DESCRIPTION						
DATE		DESIGN		CHECK						FUJITSU LTD.	
										SHEET 41/66	



[CN 4in1-USB]

REV				DATE				DESIGN				CHECK				APPR				DESCRIPTION				TITLE TIGA Main board				DRAW. NO. C1CP250040-X4				CUST.			
DATE				DESIGN				CHECK				APPR				DESCRIPTION				FUJITSU LTD.				SHEET 42 / 66											

※CN23はD51,D52近傍に配置すること



内層パターン補強用で用意(製品未使用)

[CN PWR1]

						TITLE T1ga Main board	
						DRAW. NO. C1CP250040-X4	CUST.
REV	DATE	DESIGN	CHECK	APPR	DESCRIPTION	FUJITSU LTD.	
DATE		DESIGN	CHECK	APPR		43	66

	High	Low
TPM_BADDR	4E/4Fh	2E/2Fh
TPM_BACCESS	Physical Presence ON	Physical Presence OFF

位置指定

ON OFF

場所の実装のこと

4 CLK_33_TPM

18,20,22,39,61 SERIRQ

9,17,20,22,31,36,61 PLT_RST#

18,20,22,39,61 PCI_CLKRUN#

TPM_BADDR

TPM_PPRESNCE

PWR_3VMAIN

R519 4.7K 1/16W 5% A/B/F

R520 4.7K 1/16W 5% None A/B/F

R521 4.7K 1/16W 5% None A/B/F

C552 100pF 25V A/J None A/B/F

C548 0.1uF 16V R/K A/B/F

C549 0.1uF 16V R/K A/B/F

C550 0.1uF 16V R/K A/B/F

C551 0.1uF 16V R/K A/B/F

M31

8 LCLK

12 SERIRQ

20 LRESET#

26 LPCPD#

28 LFRAME#

2 LAD0

3 LAD1

6 LAD2

7 LAD3

13 LPC_AD0

18,22,30,61 LPC_AD1

18,22,30,61 LPC_AD2

18,22,30,61 LPC_AD3

18,22,30,61 LPC_FRAME#

19 VDDC

5 VDD

11 VDD

25 VDD

4 GND

10 GND

18 GND

24 GND

21 PACCESS

22 PENABLE

16 TESTIO

17 TESTEN

9 RSVD

NC1

NC2

NC3

NC4

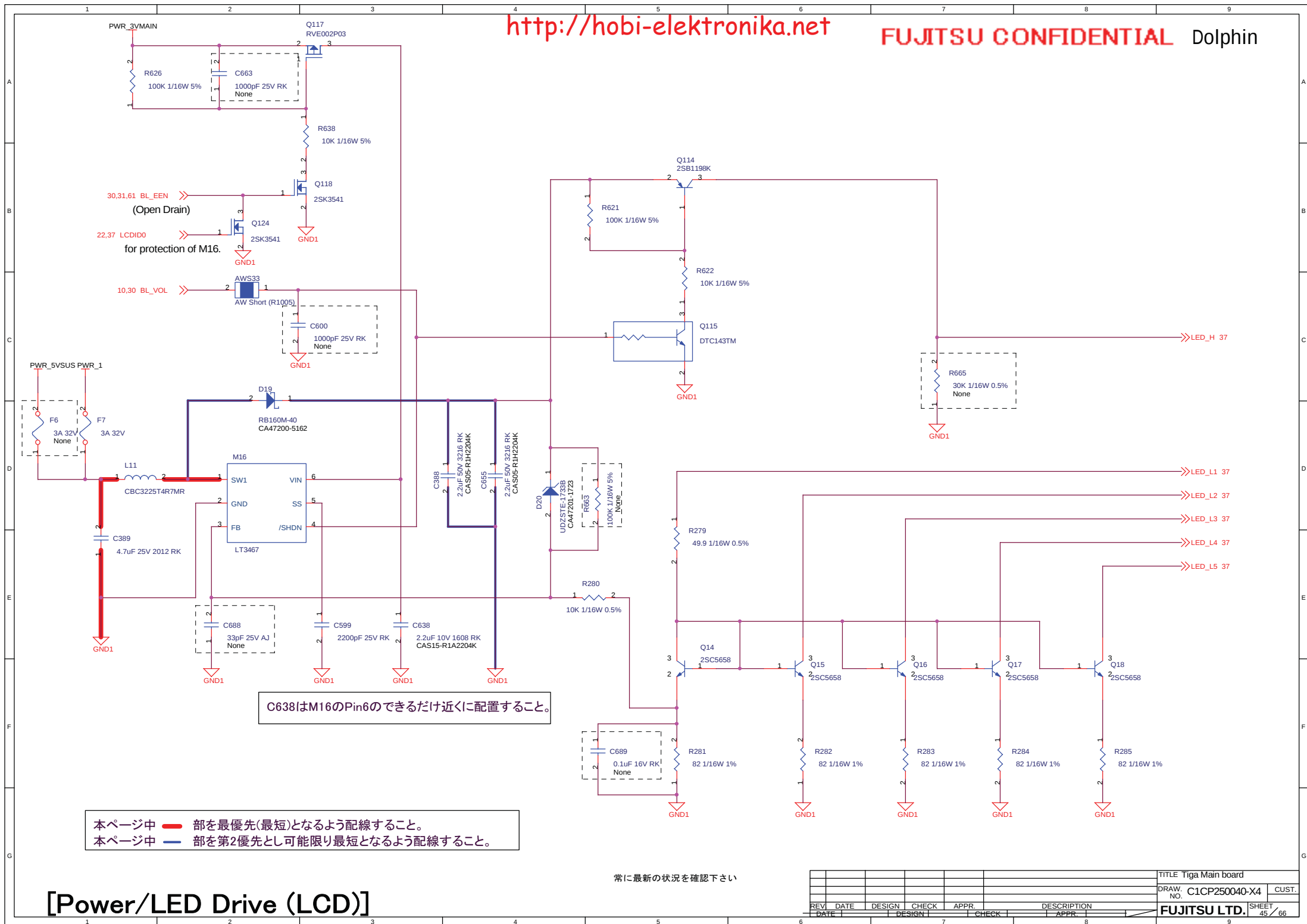
SLD6630T11.1

CA46120-0092

A/B/F

[TPM]

										TITLE Tiga Main board	
										DRAW. NO. C1CP250040-X4	
										CUST.	
REV.	DATE	DESIGN	CHECK	APPR.	DESCRIPTION						
1											
FUJITSU LTD. SHEET 44 / 66											



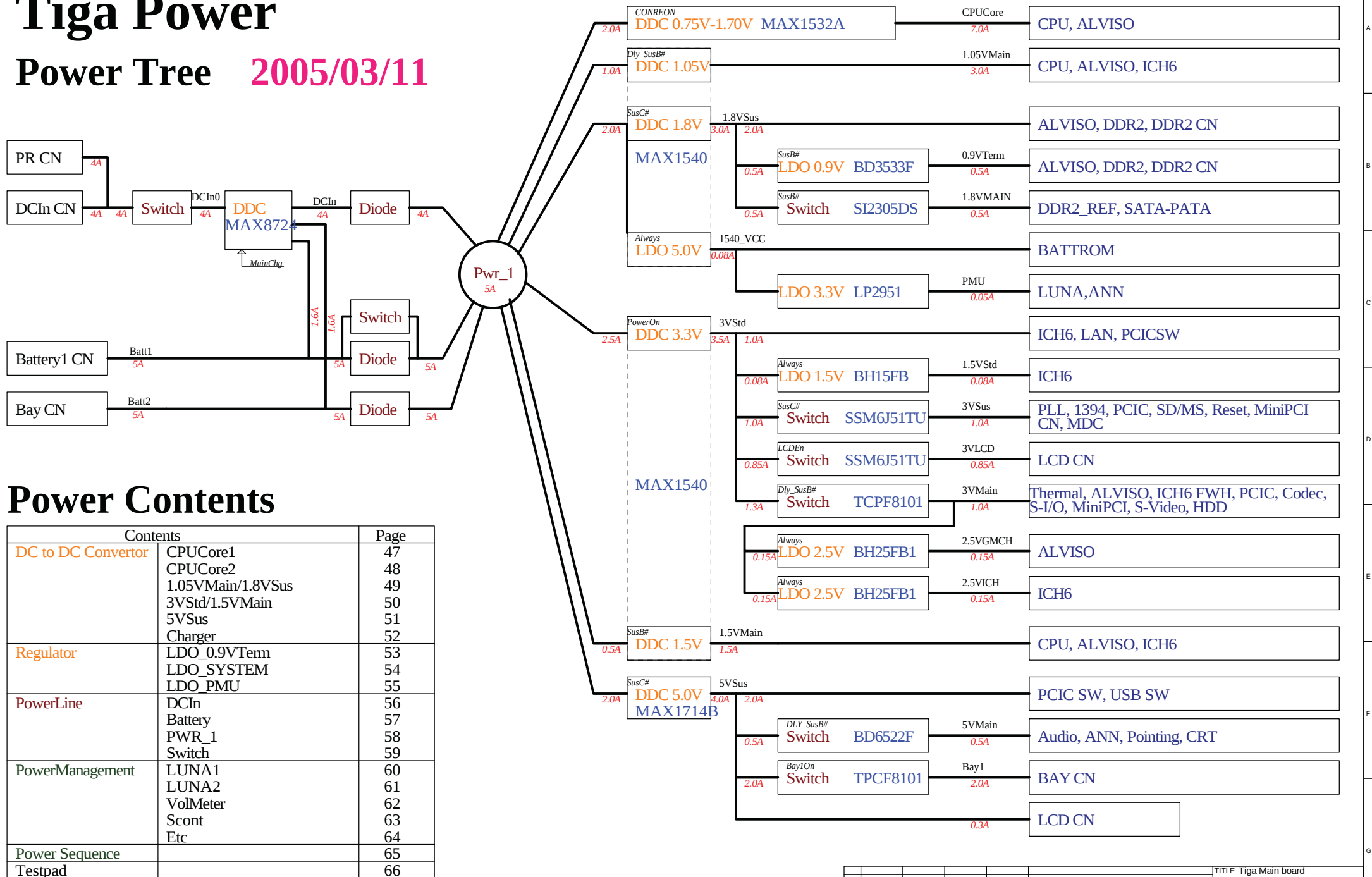
Tiga Power

Power Tree 2005/03/11

<http://hobi-elektronika.net>

FUJITSU CONFIDENTIAL

DC Converter Dolphin



Power Contents

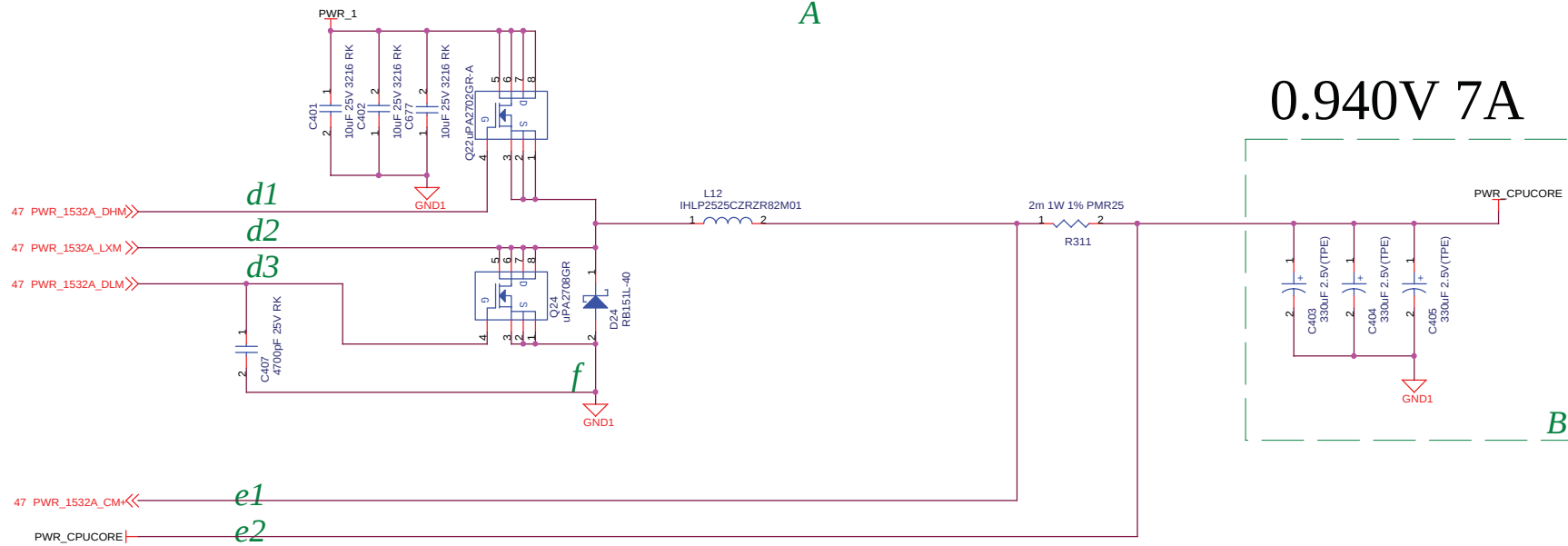
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Power/ TopPage

REV	DATE	DESIGN	CHECK	APPR	DESCRIPTION	TITLE Tiga Main board	DRAW. NO. C1CP250040-X4	CUST.
DATE	DESIGN	CHECK	APPR			FUJITSU LTD.	46 / 66	



										TITLE Tiga Main board	
										DRAW. NO. C1CP250040-X4	
										CUST.	
REV.	DATE	DESIGN	CHECK	APPR.	DESCRIPTION						
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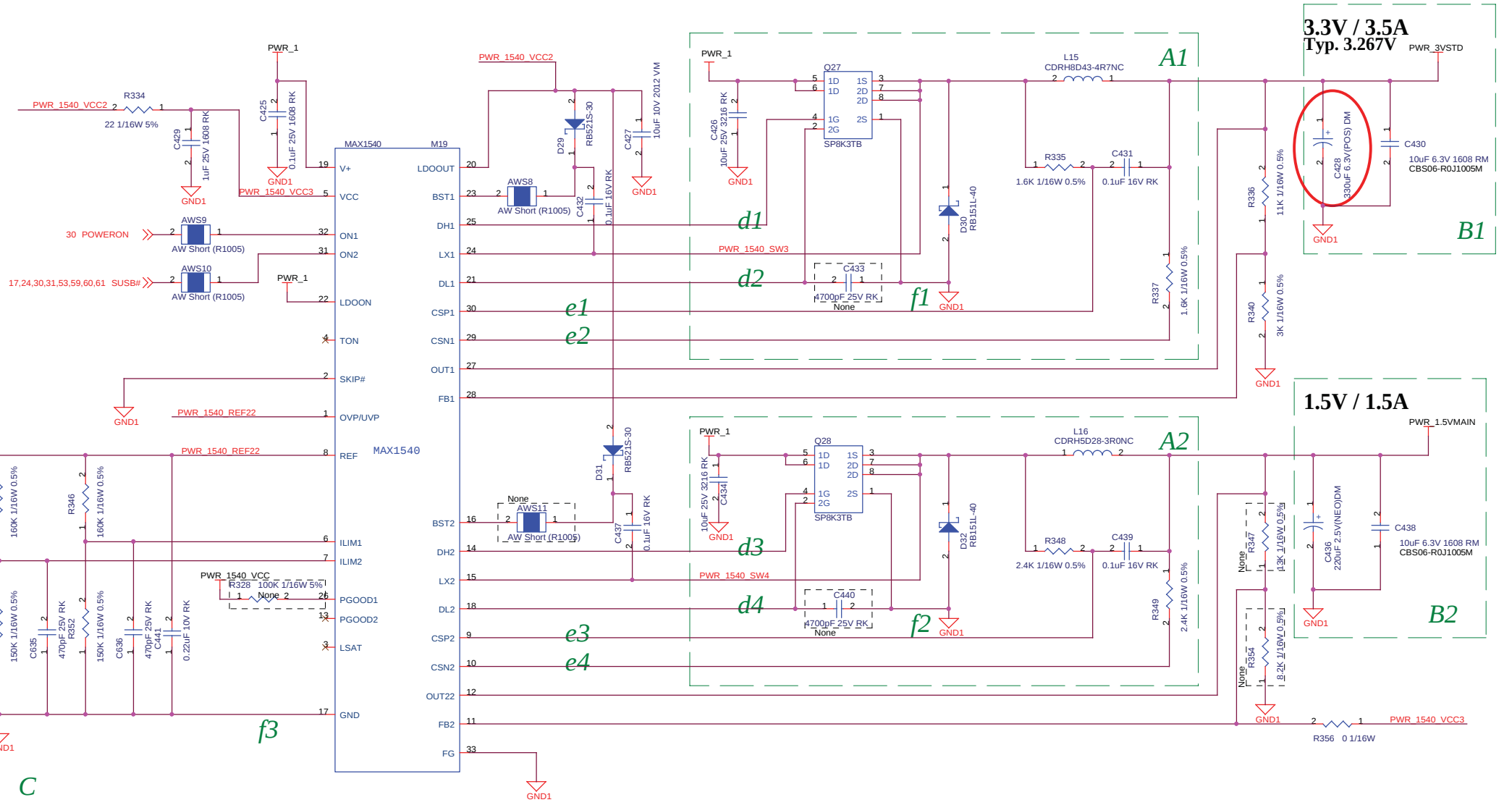
Power/ DDC/ CPUCore2

										TITLE Tiga Main board						
										DRAW. NO. C1CP250040-X4			CUST.			
										FUJITSU LTD.					SHEET 48 / 66	
REV		DATE		DESIGN		CHECK		APPR		DESCRIPTION						
DATE				DESIGN		CHECK		APPR								
6								7				8		9		

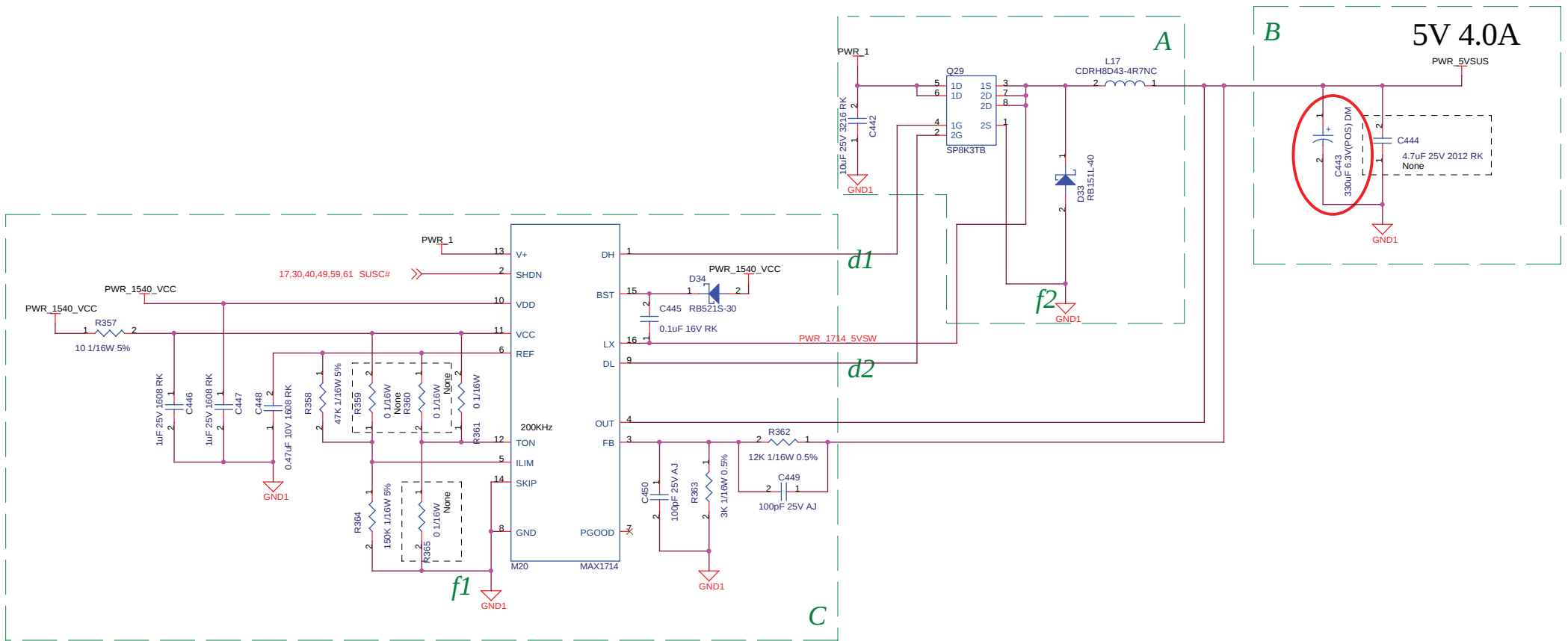


										TITLE TIGA Main board	
										DRAW. NO. C1CP250040-X4	
										CUST.	
REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION						
DATE		DESIGN		CHECK		APPR.				FUJITSU LTD.	
										SHEET 49/66	

#04(F0205A18869)
C428 : CAJ02-POJ3300M -> CAT35-POJ3300M(for RoHS).



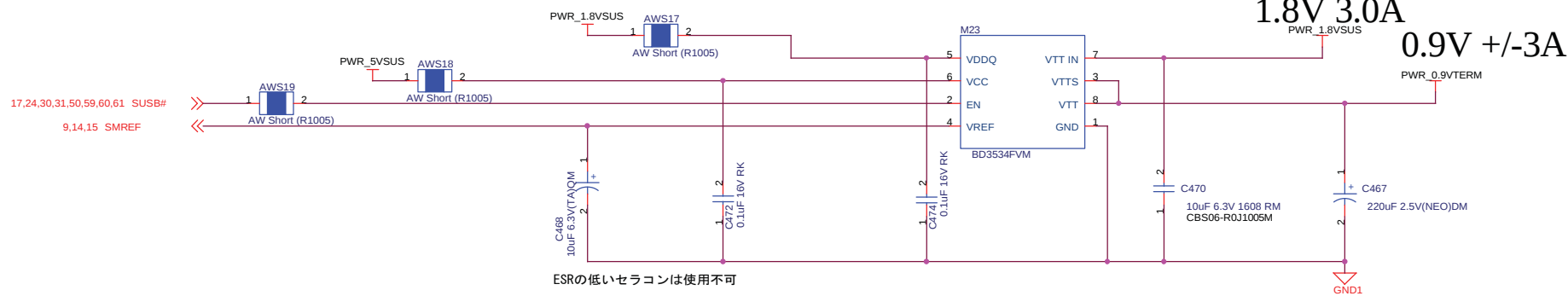
#04(F0205A18869)
C443 : CAJ02-P0J3300M -> CAT35-P0J3300M(for RoHS).



Power/ DDC/ 5VSUS

REV	DATE	DESIGN	CHECK	APPR	DESCRIPTION	TITLE	Tiga Main board
DATE	DESIGN	CHECK	APPR	DESCRIPTION	DRAW. NO.	C1CP250040-X4	CUST.
DATE	DESIGN	CHECK	APPR	DESCRIPTION	FUJITSU LTD.	SHEET	51 / 66

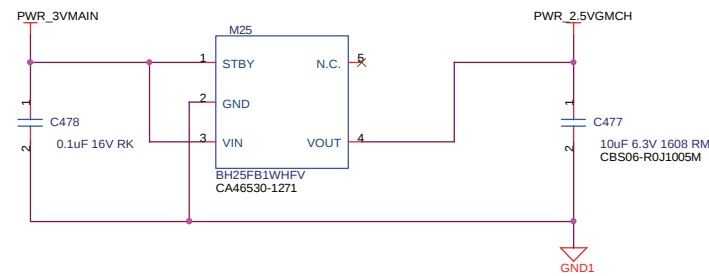




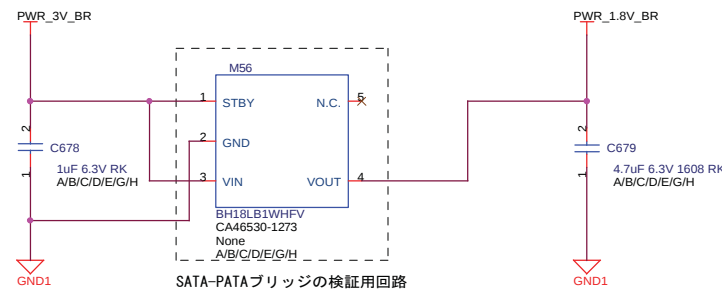
Power/ DDC/ 1.25VSus

						TITLE TIGA Main board	
						DRAW. NO. C1CP250040-X4	CUST.
REV	DATE	DESIGN	CHECK	APPR	DESCRIPTION	FUJITSU LTD.	
DATE		DESIGN	CHECK		APPR	SHEET 53 / 66	

2.5V 0.15A

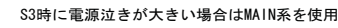


1.8V 0.1A

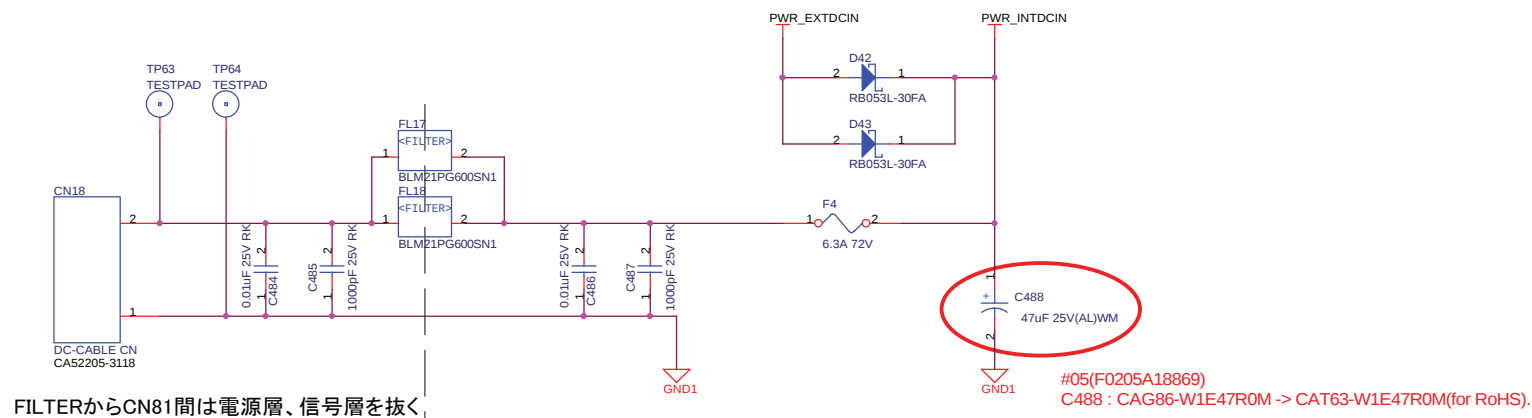


Power/ LDO/ System

						TITLE Tiga Main board		
						DRAW. NO. C1CP250040-X4		CUST.
REV	DATE	DESIGN	CHECK	APPR		DESCRIPTION		
DATE		DESIGN	CHECK			APPR		
						FUJITSU LTD.		SHEET 54 / 66



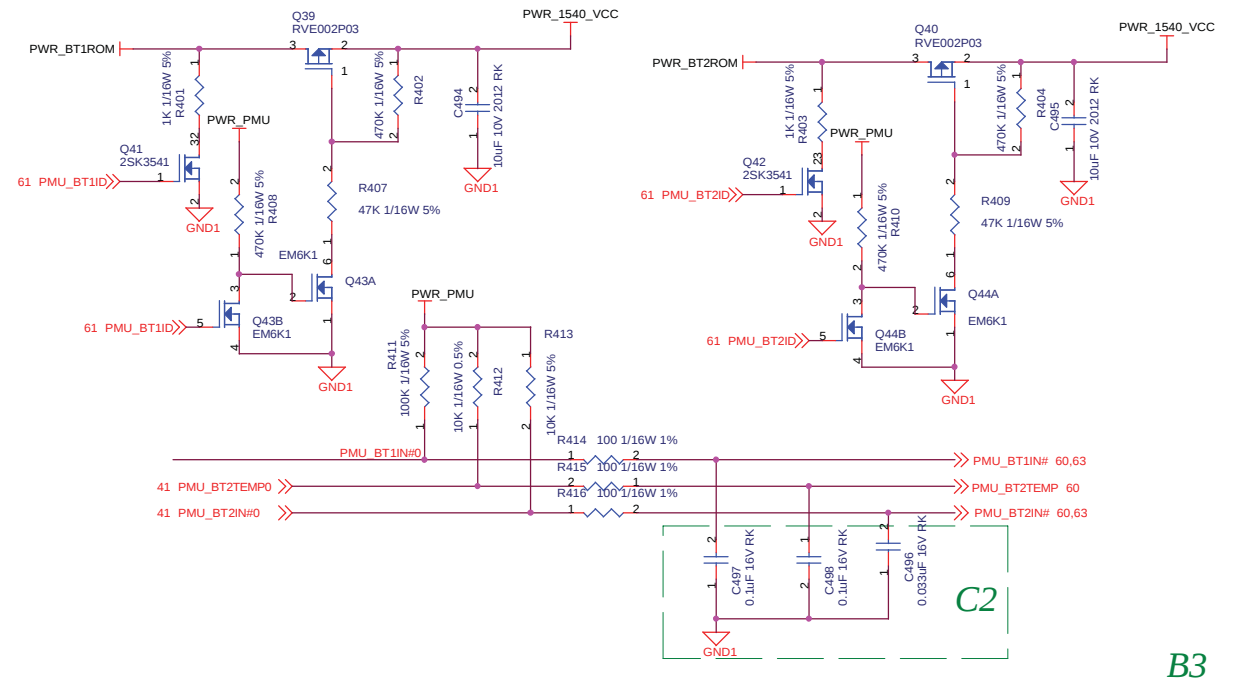
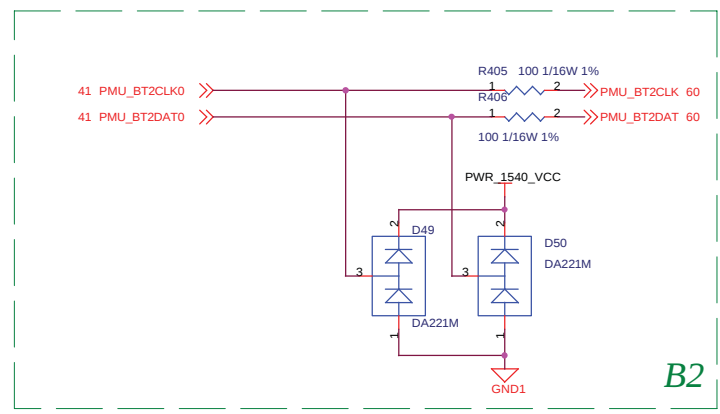
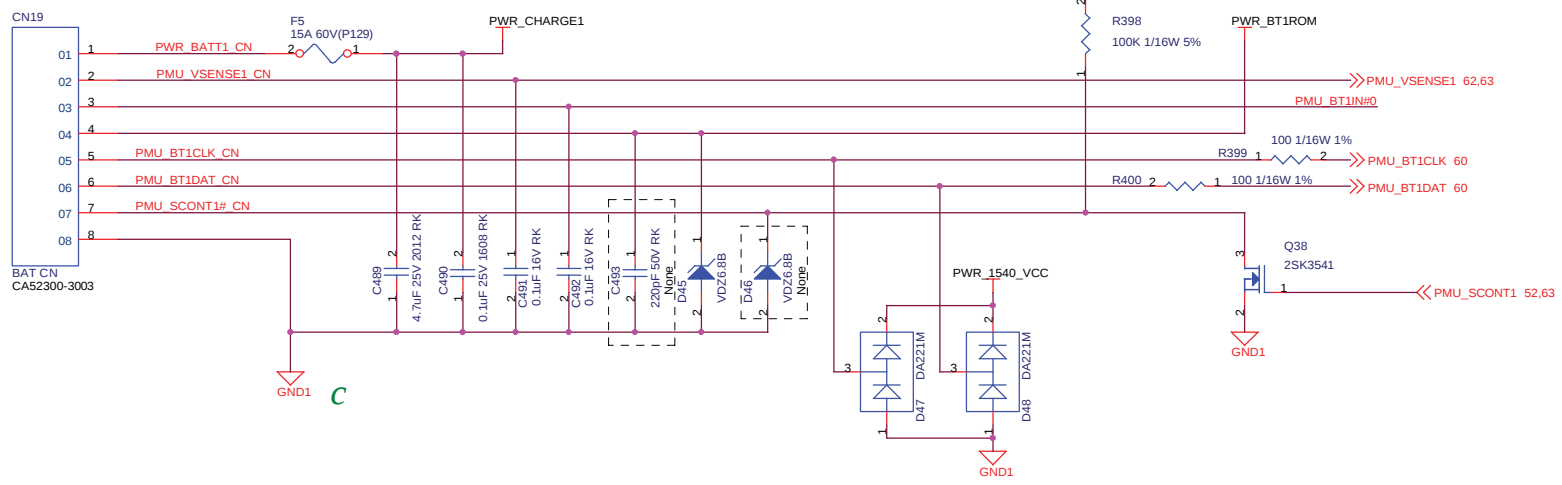
					TITLE	Tiga Main board	
					DRAW.	C1CP250040-X4	CUST.
REV.	DATE	DESIGN	CHECK	APPR.	DESCRIPTION		
6	DATE	DESIGN	7	CHECK	8	FUJITSU LTD.	
						SHEET	55 / 66



FILTERからCN81間は電源層、信号層を抜く

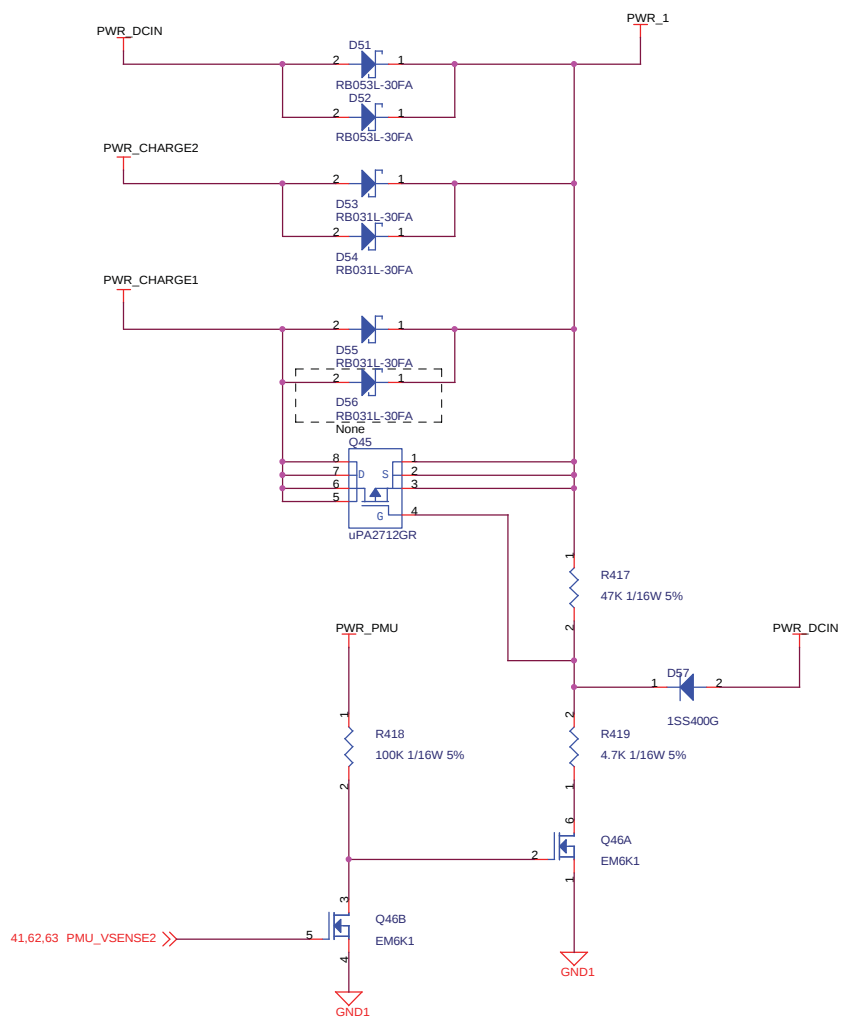
Power/ Node/ DCIn

						TITLE Tiga Main board	
						DRAW. NO. C1CP250040-X4	CUST.
REV	DATE	DESIGN	CHECK	APPR	DESCRIPTION	FUJITSU LTD.	
DATE		DESIGN		CHECK		APPR	SHEET 56 / 66



Power/ Node/ Battery

						TITLE Tiga Main board	
						DRAW. NO. C1CP250040-X4	CUST.
REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION		
DATE		DESIGN	CHECK	APPR.	FUJITSU LTD.		
			7		8	9	
						SHEET 57 / 66	



Power/ Node/ PWR_1

						TITLE Tiga Main board		
						DRAW. NO. C1CP250040-X4		CUST.
REV	DATE	DESIGN	CHECK	APPR	DESCRIPTION	FUJITSU LTD.		SHEET 58 / 66
DATE		DESIGN		CHECK				

3.3V 2.0A

3.3V 2.0A

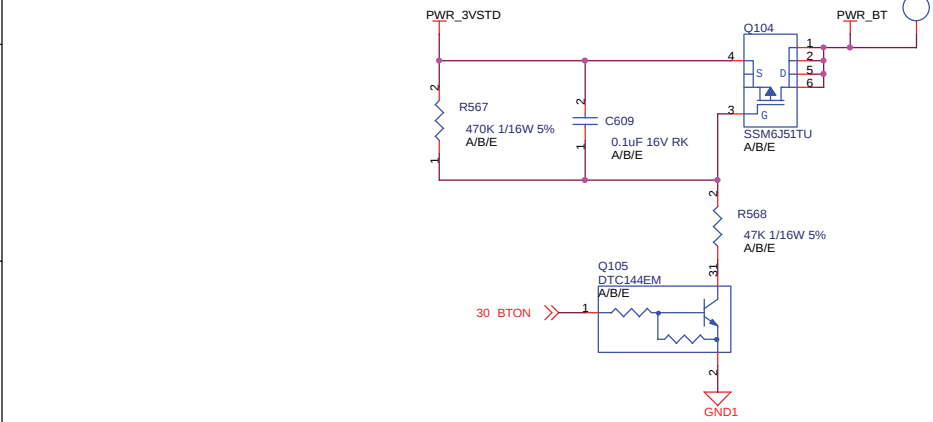
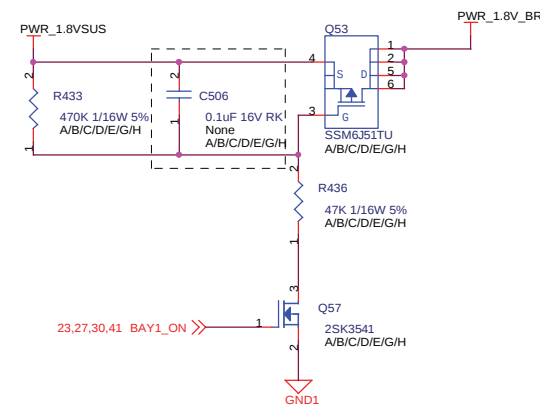
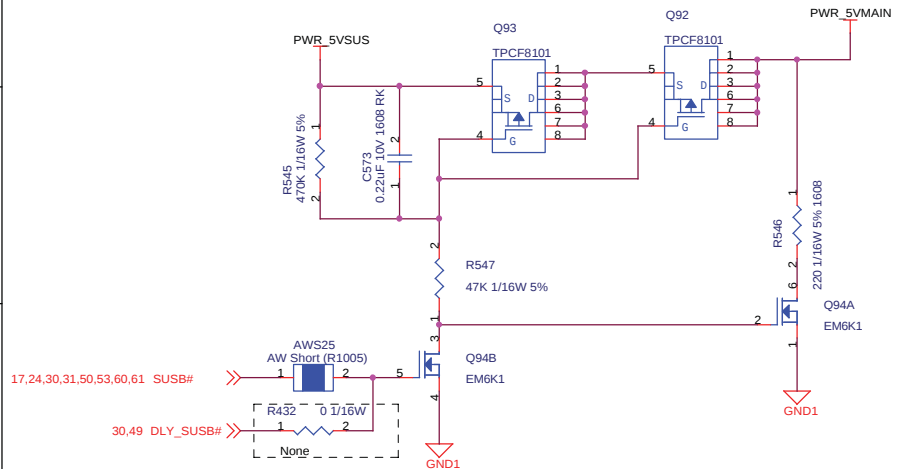
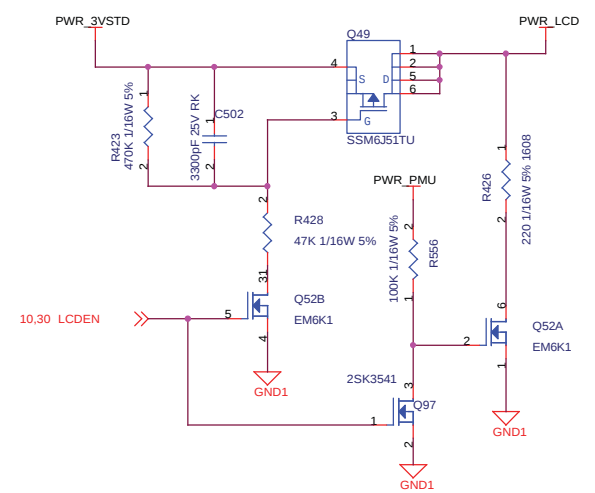
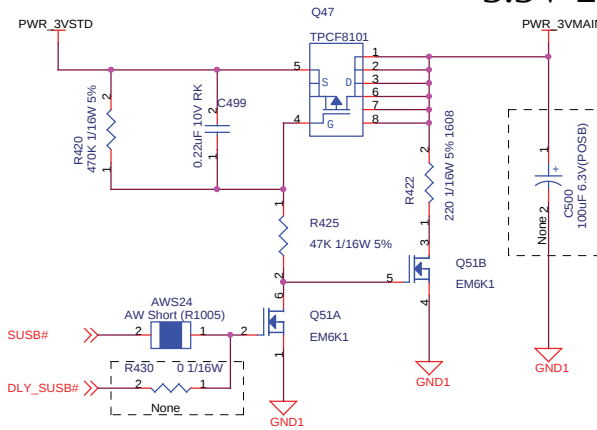
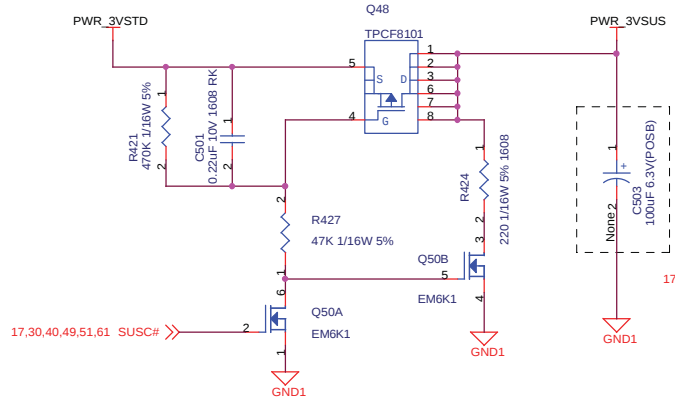
3.3V 1.0A

5.0V 0.5A

1.8V 0.1A

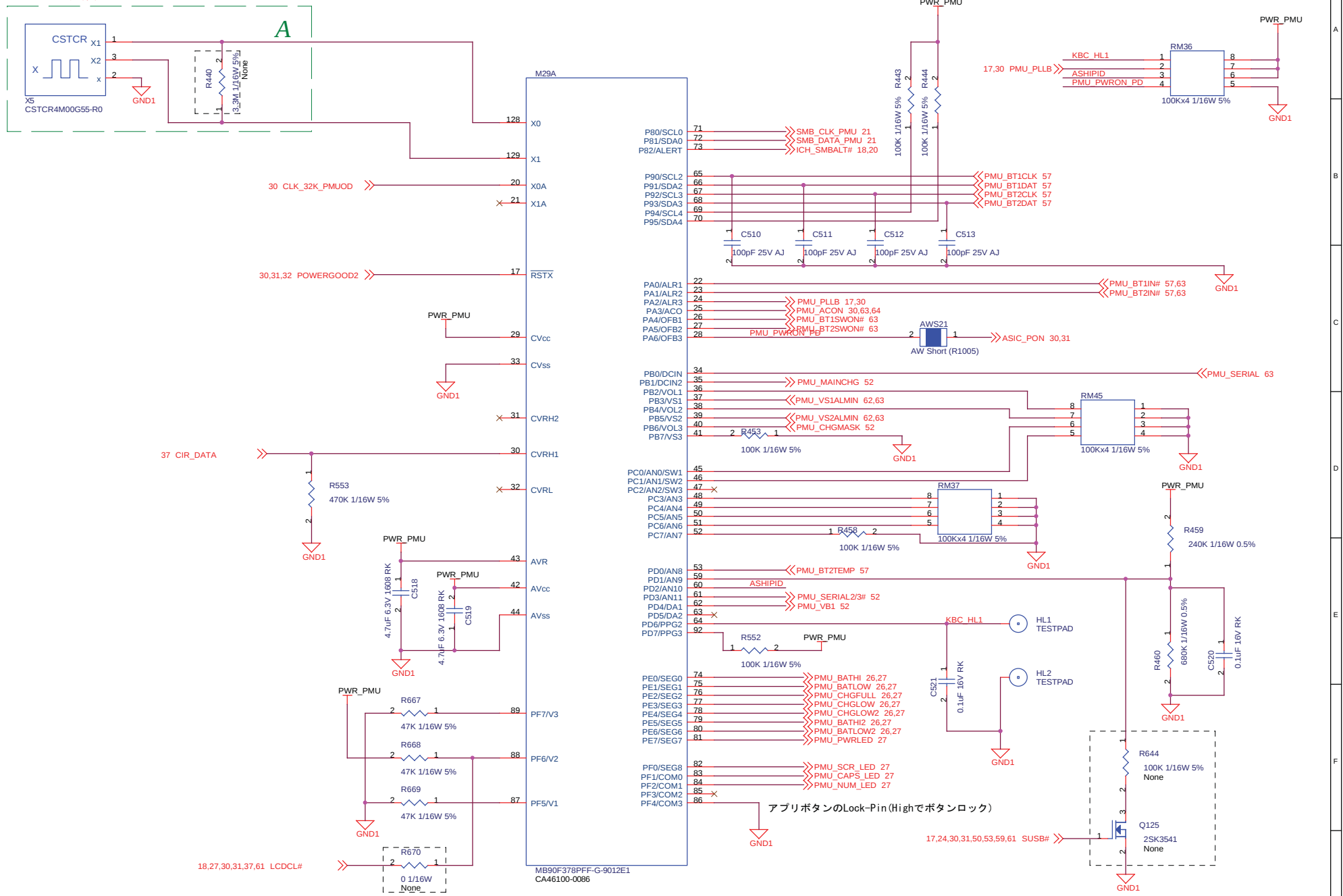
3.3V 1A

Power/ Node/ Switc



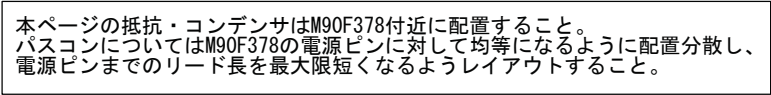
REV								TITLE Tiga Main board	
DATE								DRAW. NO. C1CP250040-X4	
DESIGN								CUST.	
CHECK								FUJITSU LTD.	
APPR								SHEET 59 / 66	
DESCRIPTION									

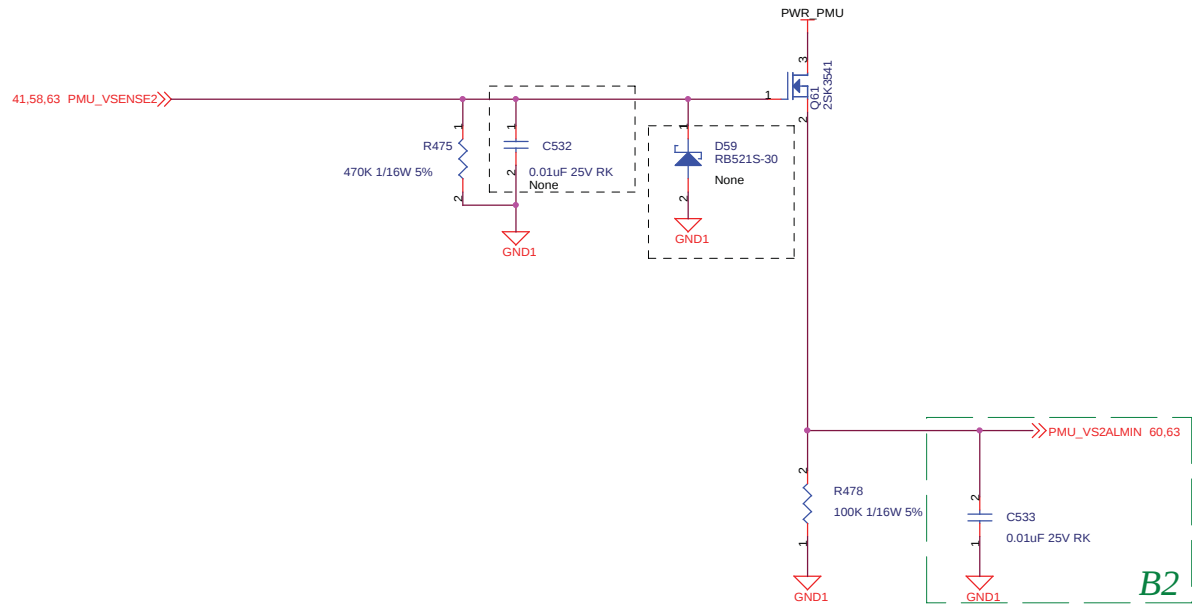
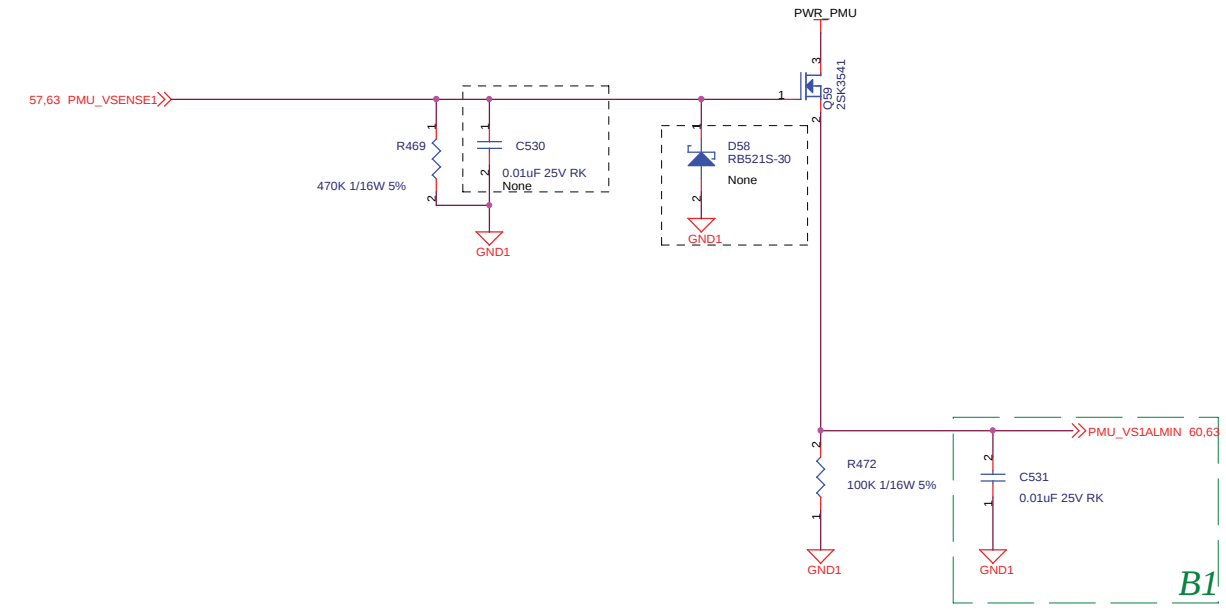
本クロックはノイズに弱いため
上下層に高速な信号が走らないように
配線すること



Power/ PMU/ LUNA1

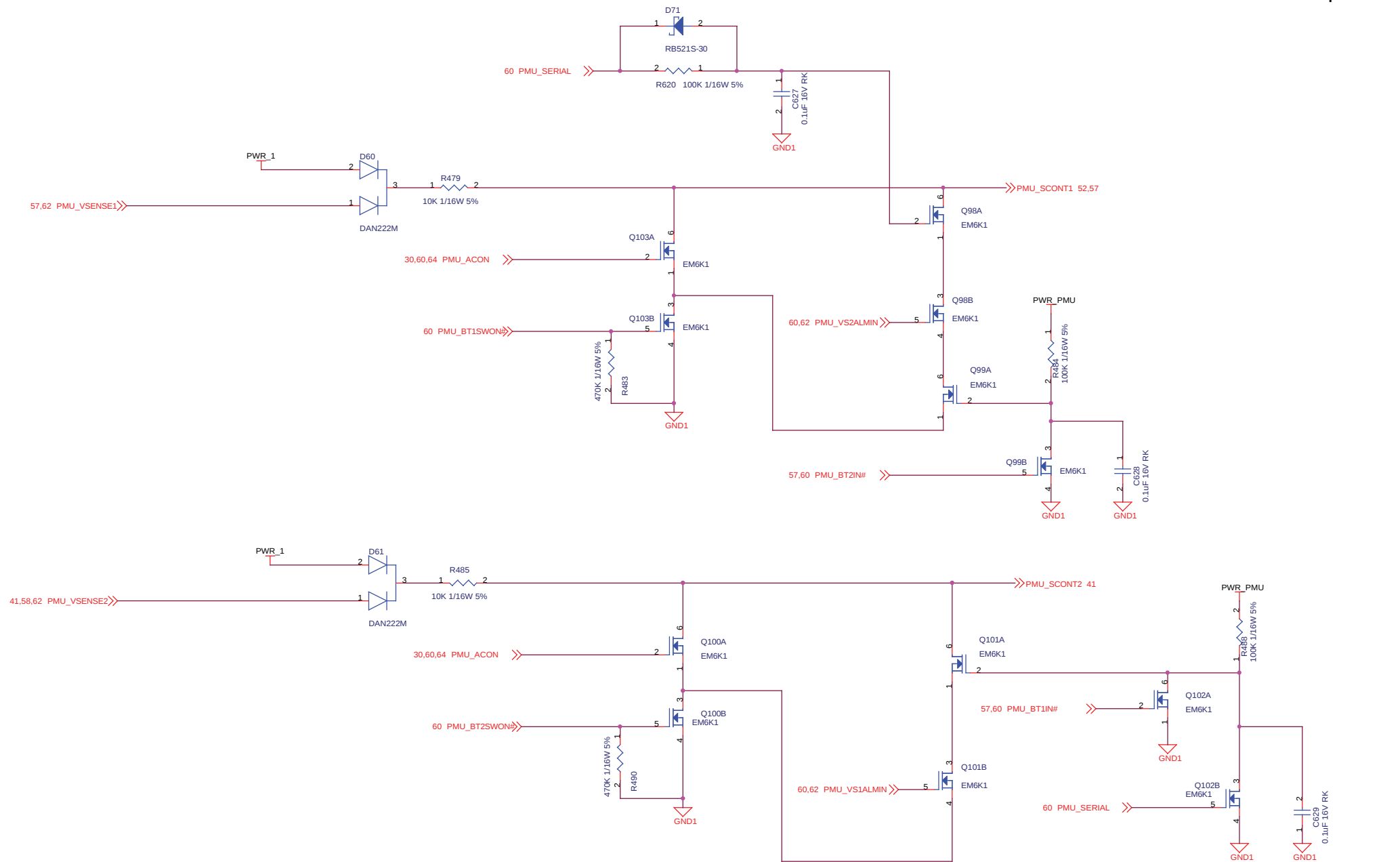
						TITLE TIGA Main board	
						DRAW. NO. C1CP250040-X4	CUST.
REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION	FUJITSU LTD.	
DATE		DESIGN		CHECK	APPR.	SHEET 60 / 66	
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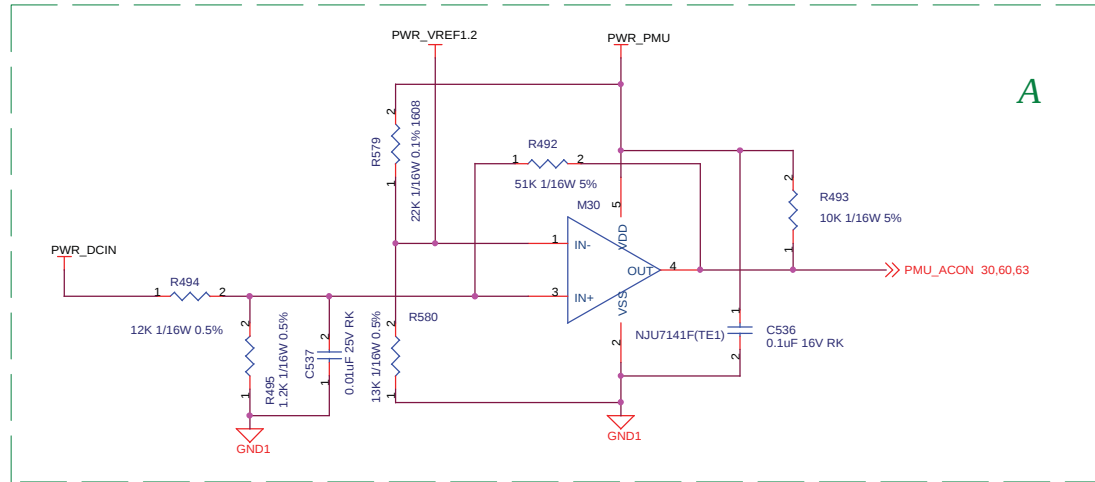
Power/ PMU/ VolMeter

						TITLE Tiga Main board	
						DRAW. NO. C1CP250040-X4	CUST.
REV	DATE	DESIGN	CHECK	APPR	DESCRIPTION	FUJITSU LTD.	
DATE		DESIGN		CHECK		SHEET 62 / 66	



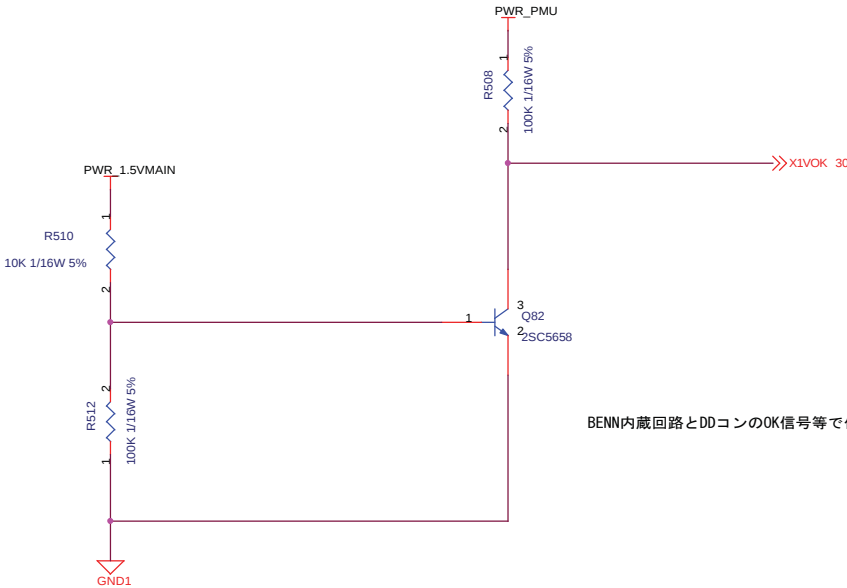
Power/ PMU/ Scont

REV	DATE	DESIGN	CHECK	APPR	DESCRIPTION	TITLE Tiga Main board
NO.	NO.	NO.	NO.	NO.	NO.	DRAW. NO. C1CP250040-X4 CUST.
DATE	DESIGN	CHECK	APPR	DESCRIPTION	FUJITSU LTD.	SHEET 63 / 66



Power/ PMU/ Etc1

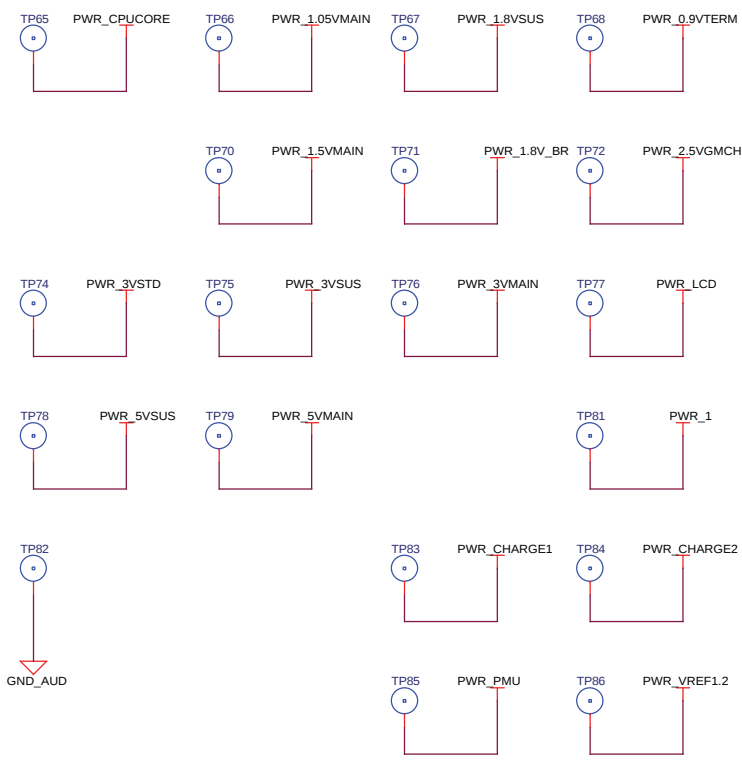
						TITLE Tiga Main board	
						DRAW. NO. C1CP250040-X4	CUST.
REV	DATE	DESIGN	CHECK	APPR	DESCRIPTION	FUJITSU LTD.	
DATE		DESIGN	CHECK	APPR		SHEET 64 / 66	



BENN内蔵回路とDDコンのOK信号等で代替によりシンプル化

POWER_SEQUENCE

						TITLE Tiga Main board	
						DRAW. NO. C1CP250040-X4	CUST.
REV	DATE	DESIGN	CHECK	APPR	DESCRIPTION	FUJITSU LTD.	
DATE		DESIGN	CHECK	APPR		SHEET 65 / 66	



[TestPad]

						TITLE Tiga Main board	
						DRAW. NO. C1CP250040-X4	CUST.
REV	DATE	DESIGN	CHECK	APPR	DESCRIPTION	FUJITSU LTD.	
DATE		DESIGN		CHECK		APPR	SHEET 66 / 66