Inventec Corporation
R&D Division

Board name : Mother Board Schematic

Project : Z11D (Santa Rosa)

Version : 0.4

Initial Date : March 02 , 2007

Inventec Corporation
5F, No. 35, Section 2, Zhongyang South Road
Beitou District, Taipei 11270, Taiwan
<OrgAddr4> TEL:+886-2-2881-0721

Title: Z11D (Merom+Crestline+ICH8M)

Size: C | Document Number: Title | Rev: 0.4

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1. Schematic Page Description :

Santa Rosa Schematic Ver : 0.4

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41. GPU_Core
42. Dual Battery
43. WLAN&New Card&MDC
44. 3G&Cardreader
45. Audio Board
46. USB Board
47. Glidepad Board
48. SW Board

2. PCI & IRQ & DMA Description :

IDSEL	CHIP
AD17	
AD27	
AD29	

PCIINT	CHIP
IRQA	
IRQB	
IRQC	
IRQD	

BUSMASTER

REQ	CHIP
REQ0 / GNT0	
REQ1 / GNT1	
REQ2 / GNT2	
REQ3 / GNT3	
REQ4 / GNT4	

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<OrgAddr4>
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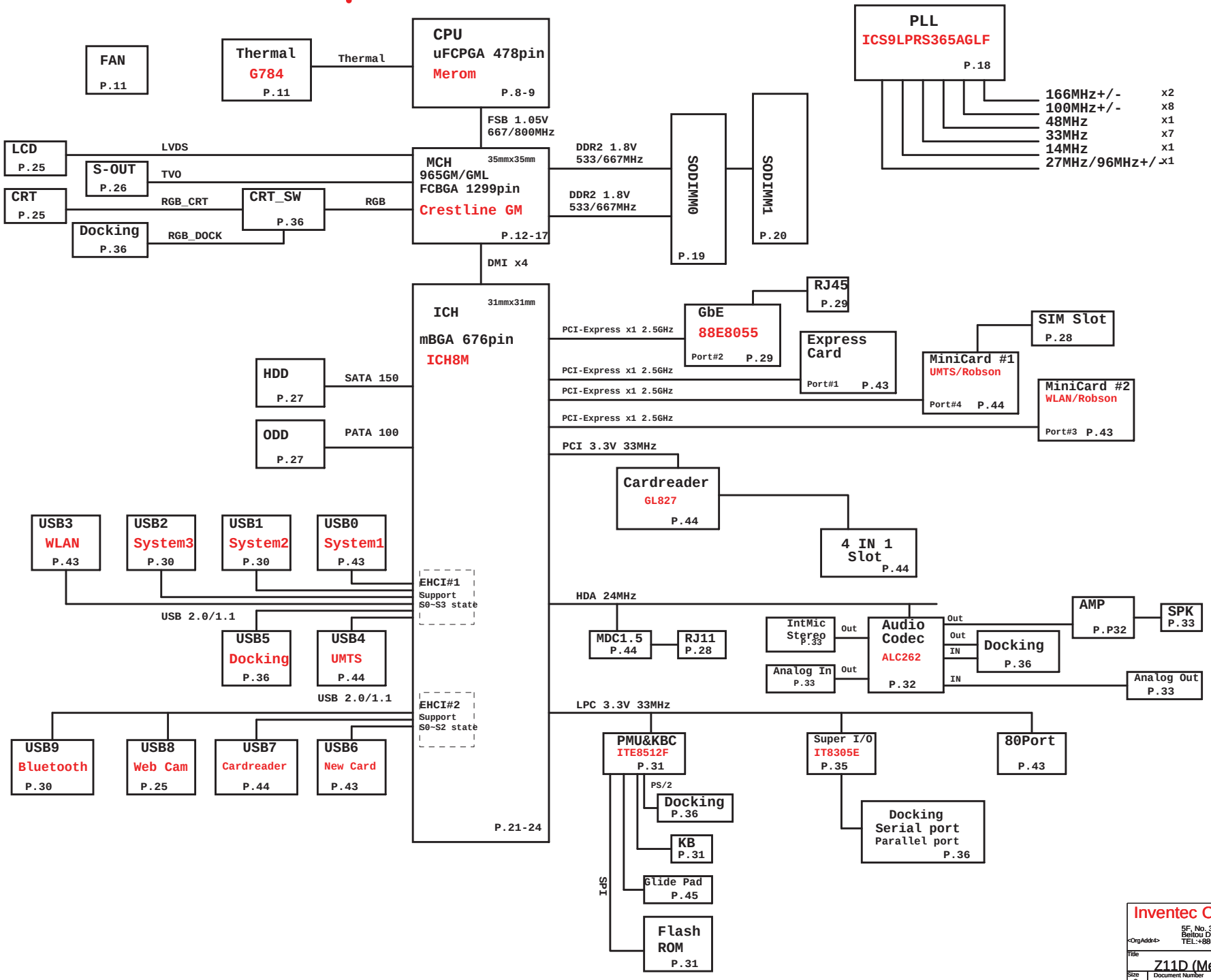
3. Block Diagram :



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5F, No. 35, Section 2, Zhongyang South Road
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TEL:+886-2-2881-0721

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4. Net name Description

Voltage Rails

DCIN	Primary DC system power supply
+5VLA	5.0V always on power rail by LATCH or ACIN
+5VA	5.0V always on power rail by ECPWON
+3VA	3.3V always on power rail by ECPWON
+5VS	5.0V switched power rail by SLP_S3#_3R
+3VS	3.3V switched power rail by SLP_S3#_3R
+1.8VS	1.8V switched power rail by SLP_S3#_3R
VCC_CORE	Core Voltage for CPU
+1.05VS	1.05V power rail for AGTL+ termination/Core for GMCH by SLP_S3#_3R
+1.25VS	1.25V switched power rail by SLP_S3#_3R
+1.5VS	1.5V power rail for CPU PLL/DMI;PCIE;DDRII DLLs for GMCH/Core;PCIE for ICH8m by SLP_S3#_3R
+1.8V	1.8V power rail for DDRII by SLP_S5#_3R
0.9VDDT_DDRII	0.9V DDRII Termination Voltage by SLP_S3#_3R

Part Naming Conventions

C	=	Capacitor
CN	=	Connector
D	=	Diode
F	=	Fuse
L	=	Inductor
Q	=	Transistor
R	=	Resistor
RP	=	Resistor Pack
U	=	Arbitrary Logic Device
Y	=	Crystal and Osc

Net Name Suffix

#	=	Active Low signal

5. Board Stack up Description

PCB Layers

Layer 1	Component Side, Microstrip signal Layer
Layer 2	Ground Plane
Layer 3	Stripline Layer
Layer 4	Power Plane
Layer 5	Stripline Layer
Layer 6	Stripline Layer
Layer 7	Ground Plane
Layer 8	Solder Side,Microstrip signal Layer

	Differential Impedance for Microstrip(5-mils)	Differential Impedance for Stripline(4-mils)
Host Clock	95 ohm +/- 20%	100 ohm +/- 20%
PCI-E Clock	95 ohm +/- 20%	100 ohm +/- 20%
DDR2 CLK	70 ohm +/- 20%	70 ohm +/- 20%
DDR2 Strobe	85 ohm +/- 20%	90 ohm +/- 20%
DMI Bus	95 ohm +/- 20%	100 ohm +/- 20%
PCIE Bus	95 ohm +/- 20%	100 ohm +/- 20%
SDVO	95 ohm +/- 20%	100 ohm +/- 20%
SATA	95 ohm +/- 20%	100 ohm +/- 20%
USB	90 ohm +/- 20%	95 ohm +/- 20%
LVDS		100 ohm +/- 20%
Lan	95 ohm +/- 20%	100 ohm +/- 20%

Power Rail	Destination	Voltage	S0 Current
VCC_CORE	Merom HFM:	1.3319V~1.4375V~1.4591V	36A
	LFM:	0.9221V~0.9625V~0.9739V	
+1.05VS	Merom: AGTL+ termination	0.997V~1.05V~1.102V	2.5A
	965GM: Core	1.0V~1.05V~1.1V	4.6A
	965GM: AGTL+ termination	0.9475V~1.05V~1.1025V	1.4A
	ICH8m:		
+1.5VS	Merom PLL	1.425V~1.5V~1.575V	120mA
	965GM: PCIE	1.425V~1.5V~1.575V	1.5A
	965GM: LVDS	1.425V~1.5V~1.575V	60mA
	965GM: TVDAC	1.425V~1.5V~1.575V	24mA
	965GM: Various PLLS analog supply	1.425V~1.5V~1.575V	320mA
	965GM: DDR DLLS,DDRII,FSB HSIO	1.425V~1.5V~1.575V	1.885A
	ICH8m:		
	ICH8m:		
	ICH8m:		
	ICH8m:		
	Mini Card:		
	Express Card:		
+1.8V	965GM: DDRII System Memory	1.7V~1.8V~1.9V	3.1A
	SO-DIMM:		
0.9VDDT_DDRII	DDRII Terminator:	0.855V~0.9V~0.945V	1.0A
+2.5VS	965GM: PCIE analog	2.32V~2.5V~2.625V	2mA
	965GM: LVDS analog	2.375V~2.5V~2.625V	10mA
	965GM: LVDS I/O	2.375V~2.5V~2.625V	60mA
	965GM: CRT DAC	2.32V~2.5V~2.625V	70mA
+3VS	965GM: HV CMOS	3.135V~3.3V~3.465V	40mA
	965GM: TVDAC analog	3.135V~3.3V~3.465V	120mA
	ICH8m:		
	ICH8m:		
	ICH8m:		
	ICH8m:		
	ICH8m:		
	Mini Card: UMTS		
	Express Card:		
	CLK Generator: ICS9LPRS365AGLF	3.135V~3.3V~3.465V	400mA
	Mini Card: WirelessLan		
	Bluetooth:		
	Super I/O: IT8305E		
	Azalia Codec: ALC262	3.0V~3.3V~3.6V	
	Azalia MDC:		
	HDD: SATA		
1.8VS	DVI: Sil1364		
+3VA	Thermal Sensor:		
	Lan: Marvell 88E8055B0		
	Azalia MDC:		
	EC: ITE8512F		
	ICH8m: RTC		
	Flash ROM: BIOS		
	LCD:	3.0V~3.3V~3.6V	1.0A
+5VS	Cardreader: GL827		
	Azalia Codec: ALC262	3.0V~3.3V~3.6V	
	FAN:		
	HDD: SATA	4.75V~5.0V~5.25V	Max: 1.0A ; R/W: 460mA ; STDBY: 70mA
	ODD: PATA	4.75V~5.0V~5.25V	Max: 1.8A ; R/W: 900mA ; STDBY: 45mA
	Audio AMP: G1432		
	Woofer AMP: None		
	Inverter:		
+5VA	USB: x 3 ports	5VA	1.5A
+5VLA	Control Power		

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6.Schematic modify Item and History:

V01--------V02

1.ADD R623 0-5%-1/16W-0402 (60130B0000ZT), R634 10K-1%-1/16W-0402 (60130B10029Z)
2.R243 from 47K-5%-1/16W-0402 (60130B4730ZT)change to 1K-5%-1/16W-0402 (60130B1020ZT)
3.R246 from 4.7K-5%-1/16W-0402 (60130B4720ZT)change to 0-5%-1/16W-0402 (60130B0000ZT)
4.R234 10-5%-1/16W-0402,C302 1uF 6.3V 10% 0402 X5R,C308 0.01uF 16V 10% 0402 X7R(NU)
5.R599 change to 39.2K-1%-1/10W-0603(60130B39229T)
6.ADD Q62 NPN PDTC144EU 50V 100mA SOT223 (6015B0030601)
7.R385 change to 10K-1%-1/16W-0402 (60130B10029Z)
8.R13,R14,R15 from 2.2K-5%-1/16W-0402 change to 220 ohm(60130B2210ZT)
9.C487,C488 from 12pF 50V 5% 0603 NPO change to 15pF 5% 50V 0402(6010071502AT)
10.C586,C588 from 18pF 50V 5% 0402 NPO change to 22pF 50V 5% 0402 NPO(6010072202AT)

12.ADD C692,C693,C690,C691 (6010B0000501) ,C706(6010A0036305)
13.ADD C675,C676,C677,C678 (6010B0047301)
14.ADD R625(60130B47400Z),R624(60130B1010ZT) ,C652 (6010071012AT)
15.ADD C712(60100768120Z),C686(6010A0025301),C650(601007A0018T)
16.ADD C1106(601007A0018T)
17.C15,C1103 change to 150uF(601007A0018T)
18.ADD C651,C653,C654,C655,C656,C657,C658,C659,C660(6010B0000501)
19.ADD C704,C702,C703,C664,C665,C666,C667,C668,C669,C670,C671,C672,C673,C713,C714,C696,C697,C682,C683,C684,C685,C698,C709,C1005,C1006,C708,C681,C701,C705,C689,C694

20.L4,L5,L6 from 17ohm 25% 600mA 0805(FBM-11-201209-170T)change to 10ohm 25% 500mA 0603(BLM18BB100SN1D) (6014B0005601)
21.C9,C10,C12 10pF 50V 0.5% 0402 NPO(NU)
22.C3,C4,C5 from 22pF 50V 5% 0402 NPO change to 18pF 50V 5% 0402 NPO(6010A0036105)
23.C6,C333 from 12pF 50V 5% 0603 NPO change to 22pF 5% 50V 0603 NPO 60100722020Z

V02--------V03

1.ADD C715 0.1uF 10V 10% 0402 X7R (6010B0031401),R635 100K 1% 1/16W 0402 (6013A0014701)
2.ADD R637,R641 0ohm 5% 1/16W 0402 (60130B0000ZT)
3.ADD R638 10K 5% 1/16W 0402 (60130B1030ZT)
4.Change U10 from 6019B0312301 change to 6019B0406201
5.DEL C138 T330uF 2V 9m 7343 PANASONIC (6010B0008501)
6.ADD C375 T330uF 2V 9m 7343 PANASONIC (6010B0008501)

7.DEL R253 10K-5%-1/16W-0402 (60130B1030ZT)
8.DEL C87 AL 68uF 25V 20% 105C 6.3X6 (60100M68658T)
9.ADD C321,C87 T5.6uF 25V 100m 3528 SANYO (6010B0048601)
10.ADD D37 PACDN042Y3R SOT23 (6011B0074901)
11.Change CN22 From 6012B0174101 to 6012B0198401
12.F2,F3 From 7A-125V-R451007 (6036A0004901) Change to 10A 125V R451010 (6036A0002901)
13.F1 From 5A 125V R451005-5A/125V(6036A0004001) Change to 7A-125V-R451007 (6036A0004901)
14.DEL R333,R337,R340 120 0.5% 1/16W 0402 (6013A0052101)
15.ADD C716,C717,C718 3pF 50V 0.25% 0402 C0G (6010B0070501)
16.DEL C3,C4,C5 18pF 50V 5% 0402 NPO (6010A0036105)
17.ADD C3,C4,C5 5.6pF 0.25% 50V C0G 0402 (6010A0013801)
18.DEL R7,R9,R10 220-5%-1/16W-0402 (60130B2210ZT)
19.ADD R7,R9,R10 75-5%-1/16W-0402 (60130B7500ZT)
20.DEL R13,R14,R15 220-5%-1/16W-0402 (60130B2210ZT)
21.DEL C596,C597,C106,C107 100pF 50V 5% 0402 NPO (6010071012AT)
22.ADD R647,R649,R651 75-5%-1/16W-0402 (60130B7500ZT)
23.DEL R503 0-5%-1/16W-0402 (60130B0000ZT)
24.ADD R492 0-5%-1/10W-0603 (60130B00000Z)

25.DEL CN14 FPC 20P 6700-F20C-00R ENTERY (6012B0170701)
26.ADD CN14 88214-20001 (6012B0199801)
27.DEL U1 TRANSFORMER LG-2413S-1 100/1000 SOP 24P (6016B0003202)
28.ADD U1 TRANSFORMER (6016B0000201)

V03--------V04

1.ADD R655 0 ohm 5% 1/8W 0805 (60130BA0003T)
2.ADD R652,R653,R654 0 ohm 5% 1/16W 0402 (60130B0000ZT)
3.ADD R118 0 ohm 5% 1/16W 0402 (60130B0000ZT)
4.ADD R170 1K 5% 1/16W 0402 (60130B1020ZT)
5.DEL R154 1K 5% 1/16W 0402 (60130B1020ZT)
6.DEL R49 0 0hm 5% 1/10W 0603 (60130B00000Z)
7.ADD R51 10K 5% 1/16W 0402 (60130B1030ZT)
8.DEL R492 0 ohm 5% 1/10W 0603(60130B00000Z)
9.ADD R503 0 ohm 5% 1/10W 0603 (60130B00000Z)
10.ADD C1302,C1303 0.01uF 25V 10% 0402 X7R(6010B0009101)

11. L12,L14,L11,L10,L7,L13,L15 from 100 ohm 25% 2A 0.1ohm 0603(6014B0006301) Change to
300ohm 25% 500mA 0.7ohm 0603(6014B0018101)

Inventec Corporation
<OrgAddr4>
5F, No. 35, Section 2, Zhongyang South Road
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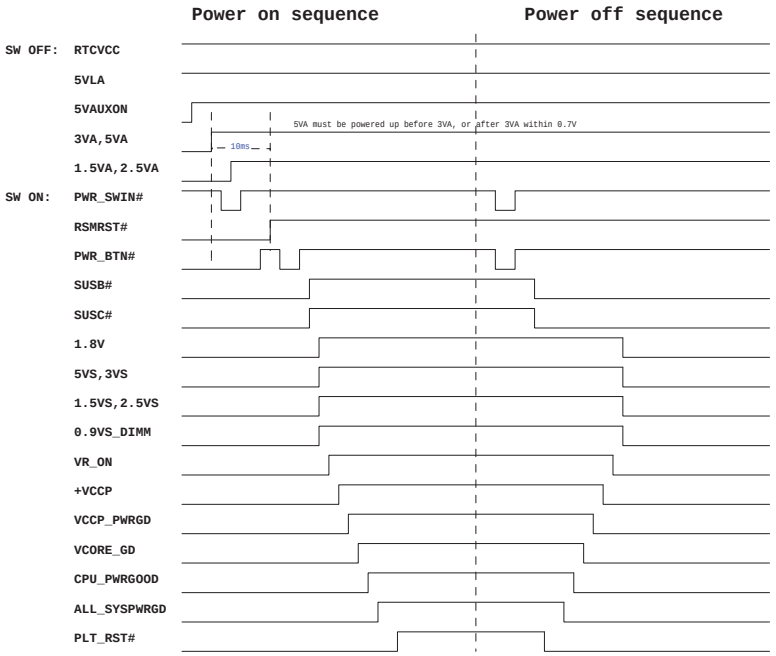
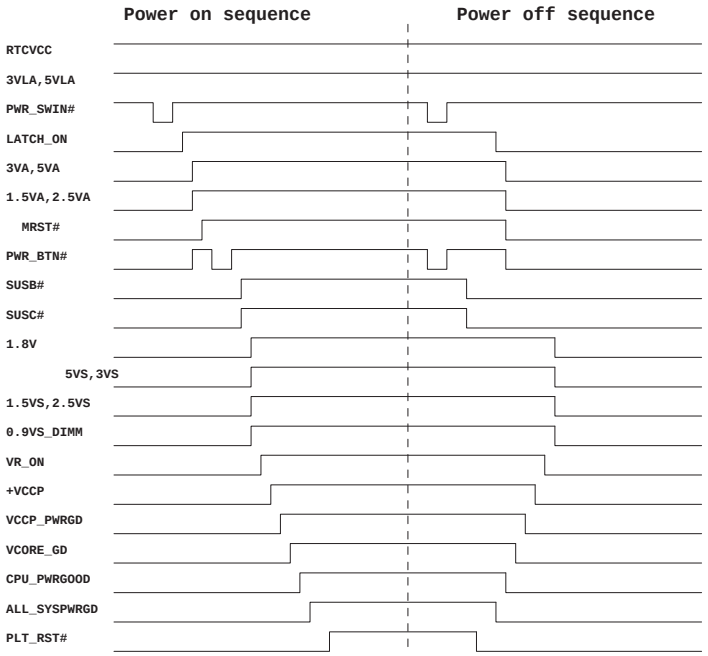
SYSTEM POWER ON/OFF SEQUENCE

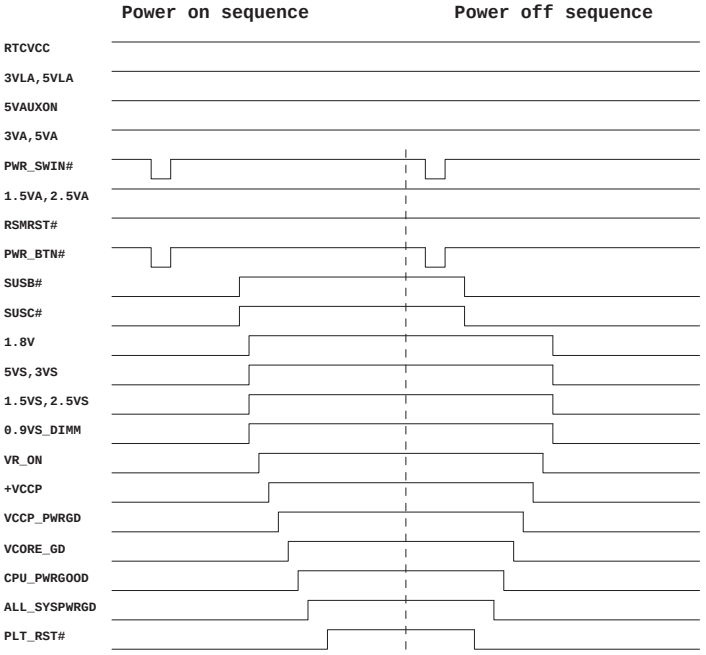
Power on/off sequence AC insert(First)



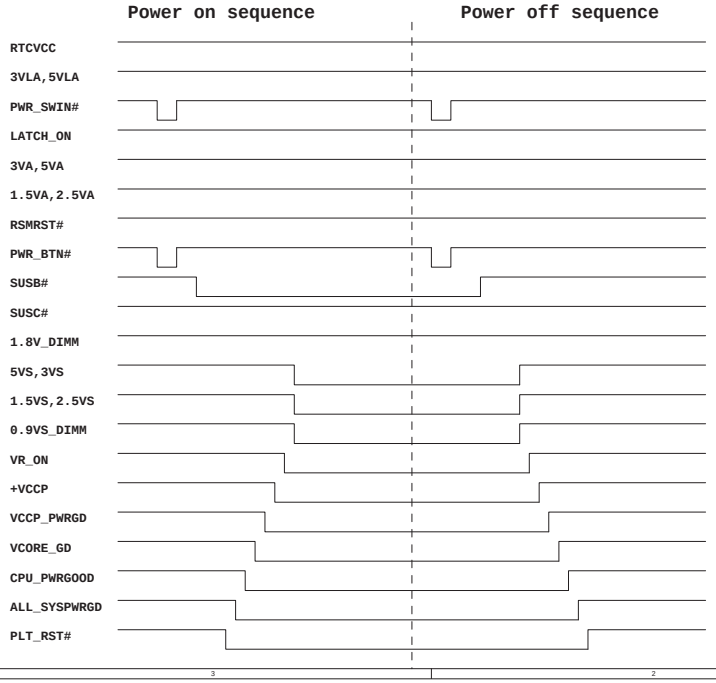
Battery only Power on/off sequence



Power on/off sequence AC insert(S4)



Suspend resume sequence(S3)



Inventec Corporation
<OrgAddr4>
5F, No. 35, Section 2, Zhongyang South Road
Beitou District, Taipei 11270, Taiwan
TEL:+886-2-2881-0721

Title: Z11D (Merom+Crestline+ICH8M)
Timing Diagram

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8. Layout Guideline

Crestline DDRII Layout Guidelines

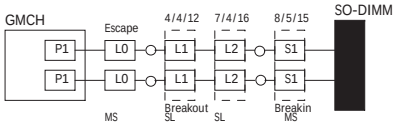
DDRII Signal Groups

Group	Signal Name
Data	M_A_DQ[63..0]/M_B_DQ[63..0] M_A_DM[7..0]/M_B_DM[7..0] M_A_DQS[7..0]/M_A_DQS#[7..0] M_B_DQS[7..0]/M_B_DQS#[7..0]
Address	M_A_A[13..0]/M_B_A[13..0] M_A_BS[2..0]/M_B_BS[2..0] M_A_RAS#/M_B_RAS# M_A_CAS#/M_B_CAS# M_A_WE#/M_B_WE#
Control	M_CS#[3..0] M_CKE[3..0] M_ODT[3..0]
Clock	M_CLK_DDR[3..0] M_CLK_DDR#[3..0]
FeedBack	SA_RCVEN#/SB_RCVEN#

Length Matching and Length Formulas

Signal Group	Minimum Length	Maximum Length
Control-to-Clock	Clock - 1.0"	Clock - 0.0"
Command-to-Clock	Clock - 1.0"	Clock + 1.0"
Strobe-to-Clock	Clock - 0.5"	Clock + 1.0"
Data-to-Strobe	Strobe - 220mils	Strobe - 180mils

CLK group : M_CLK_DDR[3..0],M_CLK_DDR#[3..0]

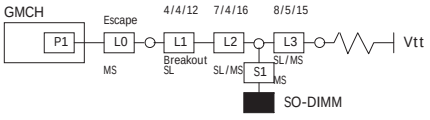


Topology	Differential Pair Point-to-Point
Reference Plane	Ground
Single Ended Trace Impedance	42 +/- 15%
Differential Mode Impedance	70 +/- 20%
Minimum Serpentine Spacing	Inner Layer : 12 mils Outer Layer : 15 mils
Package Length Range - P1	350 mils ~ 625 mils
Min. Serpentine Spacing	25 mils
Trace Length Limit - L0 (MS)	Nominal Trace Width : 5mils, 4mils Length Limit: Max = 50 mils (Escape) Min. Trace Spacing : 5mils, 4mils
Trace Length Limit - L1 (SL) (Breakout length segment)	Length Limit: Max = 700 mils Nominal Trace Width : 4mils Min. Trace Spacng (pair) : 4mils Min. Trace Spacng (Other) : 12 mils
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1	Min = 500 mils Max = 4000 mils
Total Length - P1 + L0 + L1 + L2 + S1	Max = 4500 mils Total Length for Channel A : X0 Total Length for Channel B : X1
Maximim Via Count	2 (Per side)
SCK to SCK# Length Matching	Match total length to within 5 mils
Clock to Clock Length Match (Total Length)	Match Channel A clocks to X0 +/- 20mils Match Channel A clocks to X1 +/- 20mils
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 4/12 mils to other DDR2 Outer Layer : 5/15 mils to other DDR2 Max. breakout length is 500 mils
Breakin Exceptions (Reduce geometries for SO-DIMM break-in region)	CK to CK# spacing rule waived at connector spacing of 15 mils to other DDR2 Max. breakin length is 200 mils

Feedback group : SA_RCVENIN#],SA_RCVENOUT#,SB_RCVENIN#],SB_RCVENOUT#

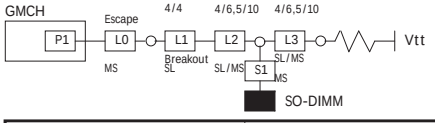
These signals are routed internally on the GMCH package and don't require any routing on the MB. As a result, can be left as NC.

Control group : SM_CKE[3..0],SM_CS#[3..0],SM_ODT[3..0]



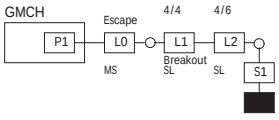
Topology	Point-to-Point with parallel termination
Reference Plane	Ground
Characteristic Trace Impedance	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils
Minimum CTRL Trace Spacing	Inner Layer : 8 mils Outer Layer : 10 mils
Minimum Spacing to Other DDR2	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length P1	750 mils +/- 200 mils
Trace Length Limit - L0	Max = 50 mils (Escape)
Trace Length Limit - L1	Max = 500 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1 - From GMCH ball to SO-DIMM pad	Min = 500 mils Max = 4500 mils
Total Length - P1 + L0 + L1 + L2 + S1 - From GMCH die to SO-DIMM pad	Max = 5000 mils
Trace Length L3	Max = 1500 mils
Parallel Termination Resistor	56 +/- 5%
Maximim Via Count	3
CTRL to SCK/SCK# Length Matching (Total Length including package)	(CLK-1.0") </= CTRL </= (CLK-0.0")
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 4 mils spacing allowed Outer Layer : 5 mils spacing allowed Max. breakout length is 500 mils

Command group : SA_MA[13..0],SB_MA[13..0],SA_BS[2..0],SB_BS[2..0],SA_RAS#, SB_RAS#,SA_CAS#,SB_CAS#,SA_WE#,SB_WE#



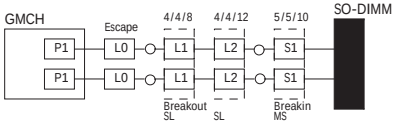
Topology	Point-to-Point with parallel termination
Reference Plane	Ground
Characteristic Trace Impedance	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils
Minimum CMD Bus Trace Spacing	Inner Layer : 6 mils Outer Layer : 10 mils
Minimum Spacing to Other DDR2	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length P1	750 mils +/- 350 mils
Trace Length Limit - L0	Max = 50 mils (Escape)
Trace Length Limit - L1	Max = 500 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1 - From GMCH ball to SO-DIMM pad	Min = 500 mils Max = 4500 mils
Total Length - P1 + L0 + L1 + L2 + S1 - From GMCH die to SO-DIMM pad	Max = 5000 mils
Trace Length L3	Max = 1500 mils
Parallel Termination Resistor	56 +/- 5%
Maximim Via Count	3
CTRL to SCK/SCK# Length Matching (Total Length including package)	(CLK-1.0") </= CMD </= (CLK+1.0")
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 4 mils spacing allowed Outer Layer : 5 mils spacing allowed Max. breakout length is 500 mils

Data group : SA_DQ[63..0],SB_DQ[63..0],SA_DM[7..0],SB_DM[7..0]



Topology	Point-to-Point
Reference Plane	Ground
Characteristic Trace Impedance	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils
Minimum DQ Bus Trace Spacing	Inner Layer : 6 mils Outer Layer : 8 mils
Minimum Serpentine Spacing	Same as DQ-to-DQ routing
Minimum Spacing to Other DDR2	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length P1	750 mils +/- 350 mils
Trace Length Limit - L0	Max = 50 mils (Escape)
Trace Length Limit - L1	Max = 500 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1 - From GMCH ball to SO-DIMM pad	Min = 500 mils Max = 4500 mils
Total Length - P1 + L0 + L1 + L2 + S1 - From GMCH die to SO-DIMM pad	Max = 5000 mils
Trace Length L3	Max = 1500 mils
Maximim Via Count	2
DQ/DM to DQS Length Matching (Total Length including Package)	Match DQ/DM to [SDQS - 200mils] +/- 20mils, per byte lane
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 4 mils spacing allowed Outer Layer : 5 mils spacing allowed Max. breakout length is 500 mils

Data Strobe group : SA_DQS[7..0],SA_DQS[7..0]#,SB_DQS[7..0],SB_DQS[7..0]#



Topology	Differential Pair Point-to-Point
Reference Plane	Ground
Single Ended Trace Impedance	55 +/- 15%
Differential Mode Impedance	85 +/- 20%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils
Nominal DQS to DQS# Spacing (edge to edge)	Inner Layer : 4 mils Outer Layer : 5 mils
Minimum DQS to DQ Spacing	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Serpentine Spacing	Inner Layer : 8 mils Outer Layer : 10 mils
Minimum Spacing to Other DDR2	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length Range - P1	750 mils +/- 350 mils
Trace Length Limit - L0	Max = 50 mils (Escape)
Trace Length Limit - L1	Max = 500 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1 - From GMCH ball to SO-DIMM pad	Min = 500 mils Max = 4500 mils
Total Length - P1 + L0 + L1 + L2 + S1 - From GMCH die to SO-DIMM pad	Max = 5000 mils
Maximim Via Count	2 (Per side)
DQS to DQS# Length Matching	Match total length to within 5 mils
Clock to Clock Length Match (Total Length include package)	(CLK-0.5") </= DQS </= (CLK+1.0")
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 8 mils to other DDR2 Outer Layer : 10 mils to other DDR2 Max. breakout length is 500 mils
Breakin Exceptions (Reduce geometries for SO-DIMM break-in region)	DQS to DQS# spacing rule waived at connector spacing of 10 mils to other DDR2 Max. breakin length is 200 mils

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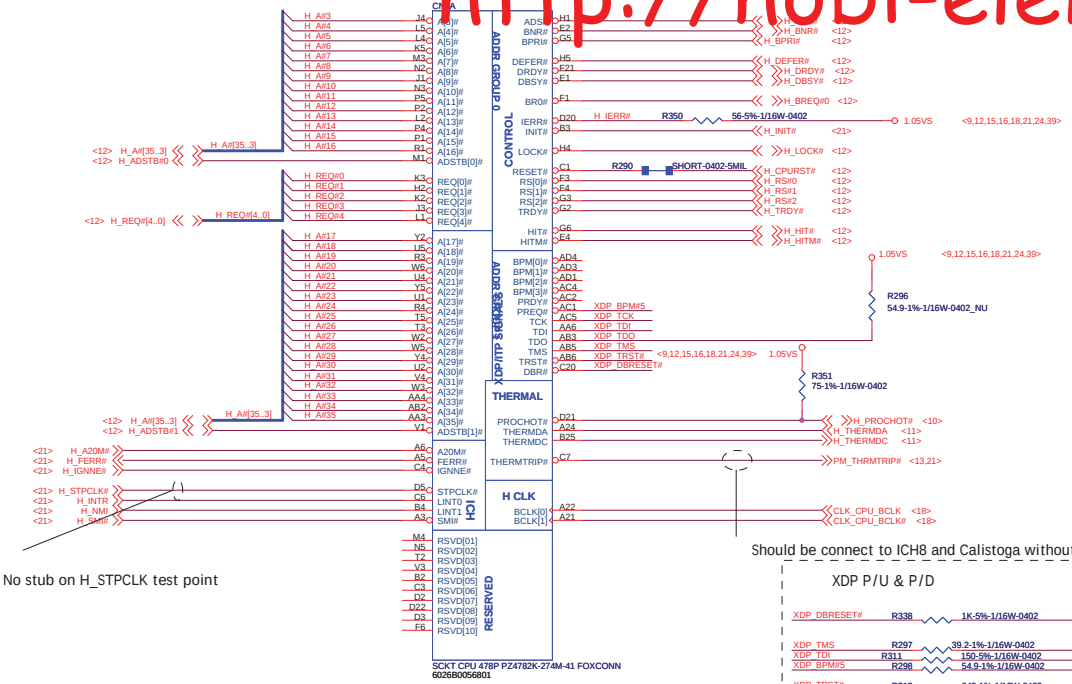
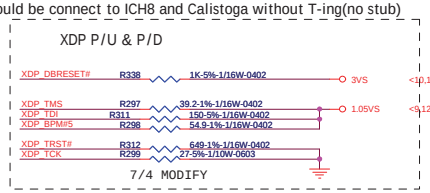
Title: Z11D (Merom+Crestline+ICH8M)
Size: C | Document Number: DDRII Layout Guideline | Rev: 0.4
Date: Tuesday, July 31, 2007 | Sheet 7 of 48



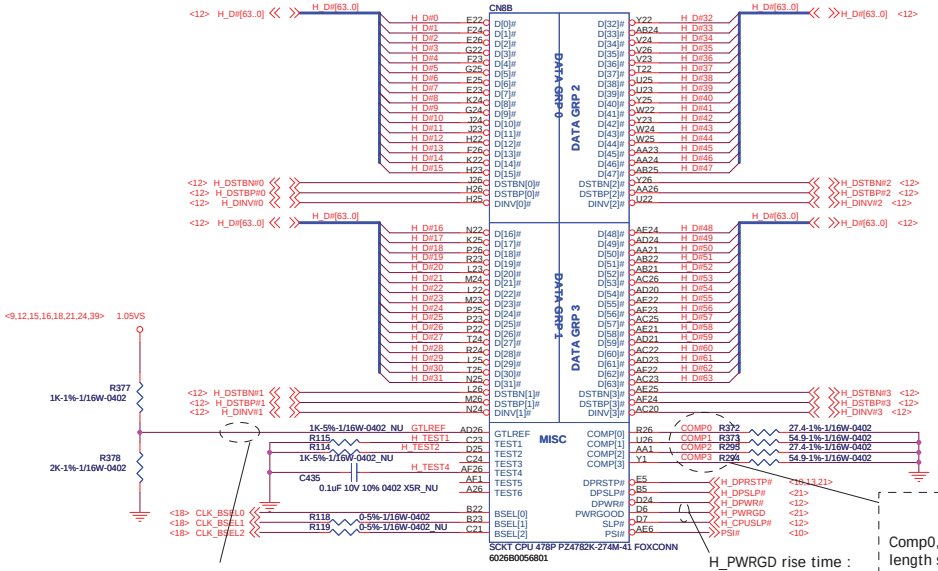
No stub on H_STPCLK test point

Rout to TP via and place gnd via w/in 100mils

Should be connect to ICH8 and Calistoga without T-ing(no stub)



A#[32-39], APM#[0-1]:Leave escape routing on for future functionality



Zo=55ohm, 0.5" max for GTLREF, Space any other switch signals away from GTLREF with a minimum of 25mils.

Don't allow the GTLREF routing to create splits or discontinuities in the reference planes of the FSB signals

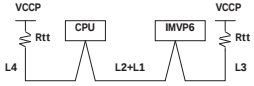
H_PWRGD rise time : Max : 15ns

Comp0,2 connect with Zo=27.4ohm, make trace length shorter than 0.5" and width is 18mils.

Comp1,3 connect with Zo=55ohm, make trace length shorter than 0.5" and width is 5mils

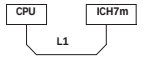
Topology : ERR#

L1	L2	Rtt	Transmission Line
0.5" - 12"	0" - 3.0"	56 +/-5%	Micro-strip
0.5" - 12"	0" - 3.0"	56 +/-5%	Strip-line



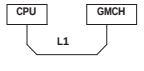
L1	L2	L3	L4	Rtt	Transmission Line
0.5" - 6.5"	0.5" - 6.5"	0" - 3.0"	0" - 3.0"	70 +/-5%	Micro-strip
0.5" - 6.5"	0.5" - 6.5"	0" - 3.0"	0" - 3.0"	70 +/-5%	Strip-line

Topology : PWRGOOD



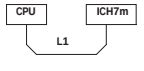
L1	Transmission Line
0.5" - 12"	Micro-strip
0.5" - 12"	Strip-line

Topology : CPUSLP#



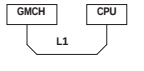
L1	Transmission Line
0.5" - 12"	Micro-strip
0.5" - 12"	Strip-line

Topology : INTR , NMI , A20M# , DPSLP# , IGNNE# , INIT# , SMI# , STPCLK#



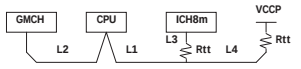
L1	Transmission Line
0.5" - 12"	Micro-strip
0.5" - 12"	Strip-line

Topology : RESET#



L1	Transmission Line
1" - 6"	Micro-strip
1" - 6"	Strip-line

Topology : THERMTRIP#



L1	L2	L1+L3	L3	L4	Rss	Rtt	Transmission Line
1" - 12"	1" - 6"	1" - 12"	0" - 3.0"	0" - 3.0"	24 +/-5%	56 +/-5%	Micro-strip
1" - 12"	1" - 6"	1" - 12"	0" - 3.0"	0" - 3.0"	24 +/-5%	56 +/-5%	Strip-line

FSB Common Clock Signal Layout Guide :

H_ADS# , H_BNR# , H_BPRI# , H_BRO# , H_DBSY# , H_DEFER# , H_DPWR# , H_DRDY# , H_HIT# , H_HITM# , H_LOCK# ,H_RS#[2..0] , H_TRDY# , H_CPURST#.

Transmission Line Type	Total Trace Length	Normal Impedance	Spacing (mils)
Strip-line(Int. Layer)	1.0 ~ 6.5 inch	55+/-15%	W=4 & S=8 mils
Micro-strip(Ext. Layer)			W=5 & S=10 mils

FSB Source Synchronous Data Length Variation and Strobe Matching Requirements :

Signals Name	Signals Matching	Strobes associated with the group	Strobe-to-Strobe Complement Matching
H_D#[15..0] , H_DINV#0	+/- 100 mils	H_DSTBP#0, H_DSTBN#0	+/- 25 mils
H_D#[31..16] , H_DINV#1	+/- 100 mils	H_DSTBP#1, H_DSTBN#1	+/- 25 mils
H_D#[47..32] , H_DINV#2	+/- 100 mils	H_DSTBP#2, H_DSTBN#2	+/- 25 mils
H_D#[63..48] , H_DINV#3	+/- 100 mils	H_DSTBP#3, H_DSTBN#3	+/- 25 mils

FSB Source Synchronous Data Signal Routing Topology#1 :

Signal Name	Transmission Line Type	Total Trace Length	Normal Impedance	Width & Spacing (mils)	
				Data-to-Data,Strobe-to-strobe	Strobe-to-Data
H_DINV#[3..0]	Strip-line	0.5 ~ 5.5 inch	55+/-15%	W=4 & S=8 mils	N/A
H_DATA#[63..0]	Strip-line	0.5 ~ 5.5 inch	55+/-15%	W=4 & S=8 mils	N/A
H_DSTBN#[3..0]	Strip-line	0.5 ~ 5.5 inch	55+/-15%	W=4 & S=4 mils	W=4 & S=12 mils
H_DSTBP#[3..0]	Strip-line	0.5 ~ 5.5 inch	55+/-15%	W=4 & S=4 mils	W=4 & S=12 mils

FSB Source Synchronous Address Length Variation and Strobe Matching Requirements :

Signals Name	Signals Matching	Strobes associated with the group	Strobe to Assoc. Address Signal Matching
H_A#[16..3] , H_REQ#[4..0]	+/- 200 mils	H_ADSTB#0	+/- 200 mils
H_A#[35..17]	+/- 200 mils	H_ADSTB#1	+/- 200 mils

*** No length matching requirements exist between H_ADSTB#0 and H_ADSTB#1

FSB Source Synchronous Address Signal Routing :

Signal Name	Transmission Line Type	Total Trace Length	Normal Impedance	Width & Spacing (mils)
H_A#[35..3]	Strip-line	0.5 ~ 6.5 inch	55+/-15%	W=4 & S=8 mils
H_REQ#[4..0]	Strip-line	0.5 ~ 6.5 inch	55+/-15%	W=4 & S=8 mils
H_ADSTB#[1..0]	Strip-line	0.5 ~ 6.5 inch	55+/-15%	W=4 & S=12 mils

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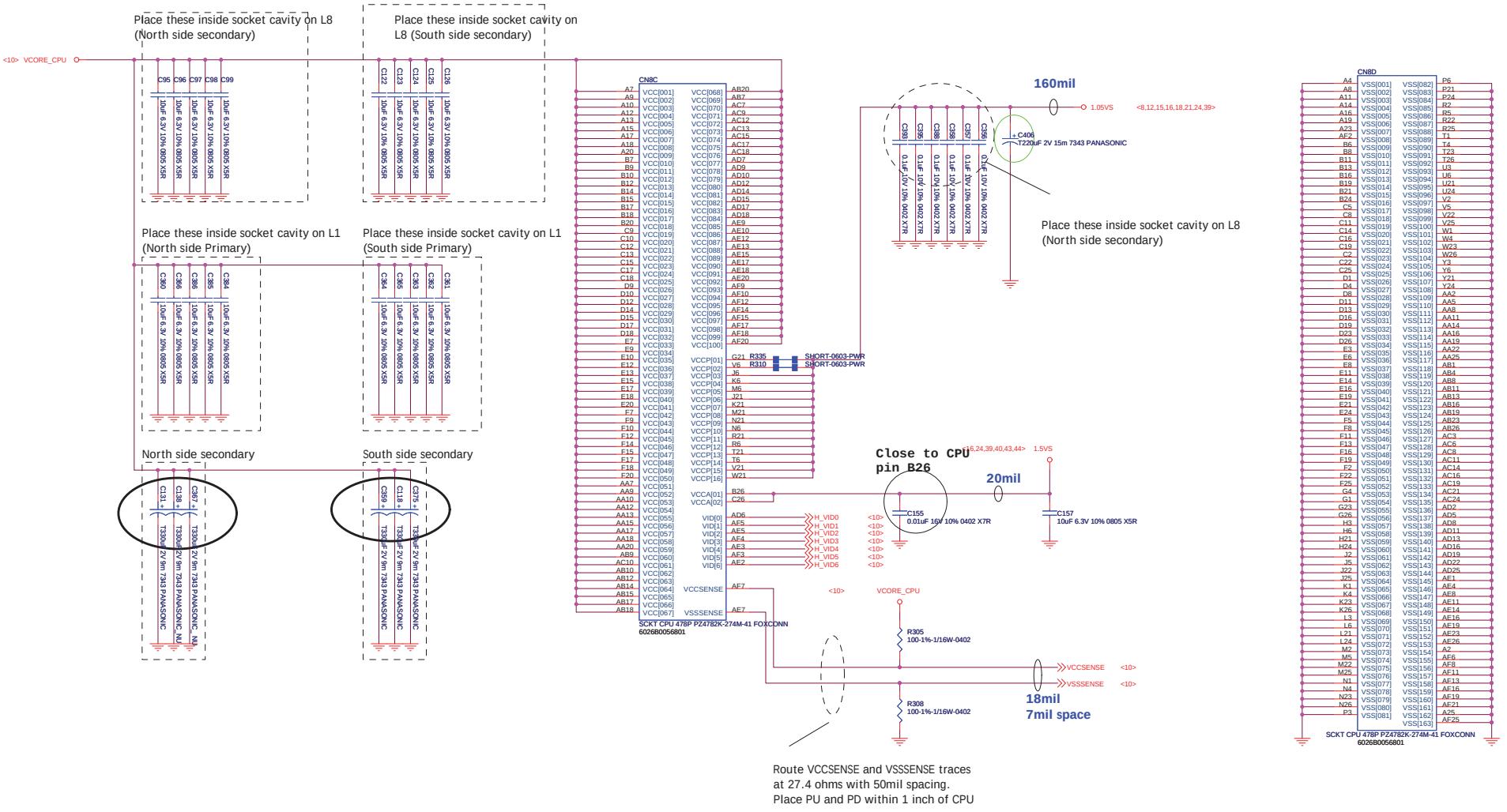
Title: Z11D (Merom+Crestline+ICH8M)

Size: C | Document Number: Merom Processor(1/2) | Rev: 0.4

Date: Tuesday, July 31, 2007 | Sheet 8 of 48



Route VCCSENSE and VSSSENSE traces
at 27.4 ohms with 50mil spacing.
Place PU and PD within 1 inch of CPU

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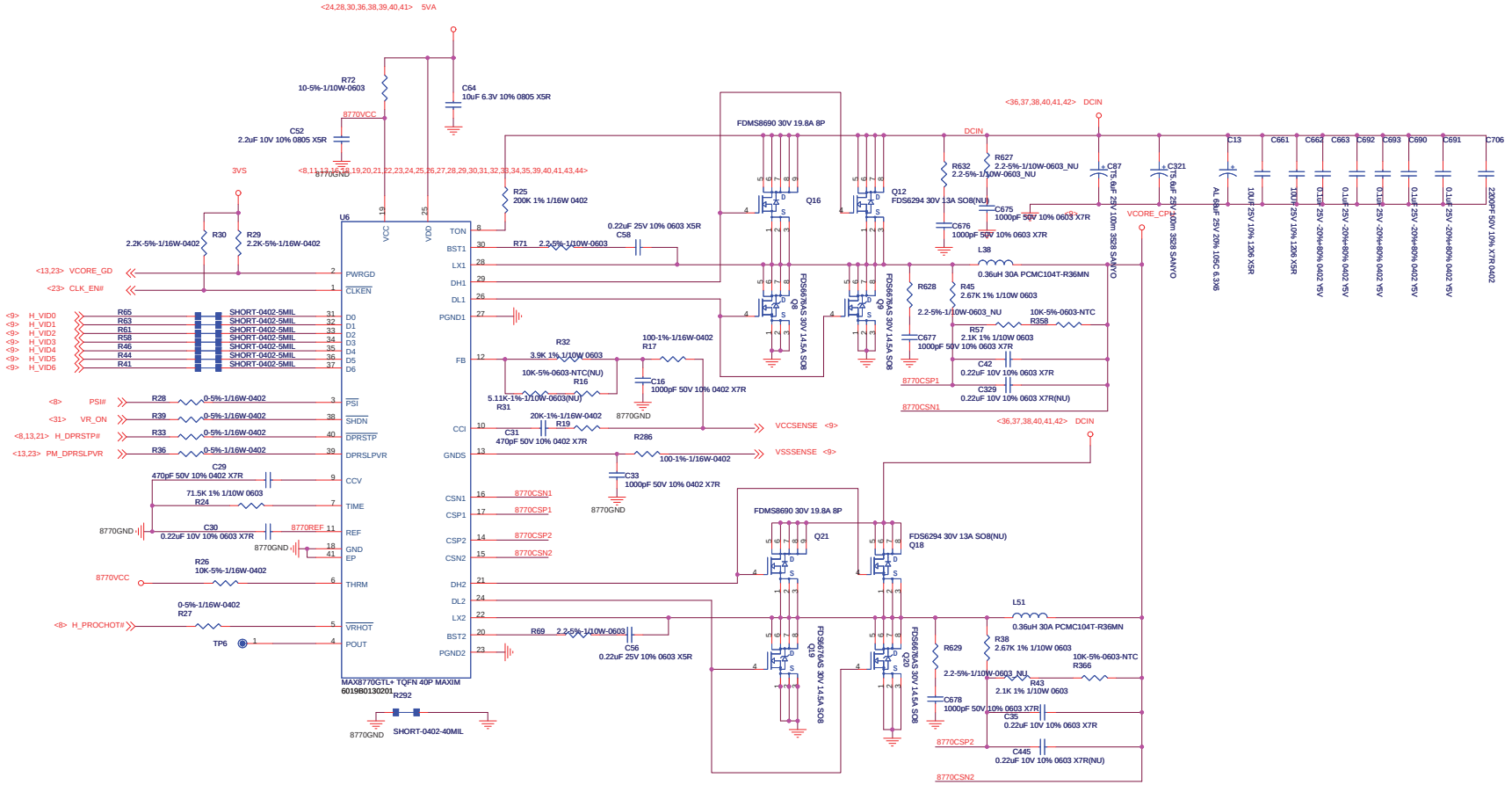
Size: C | Document Number: Merom Processor(2/2) | Rev: 0.4
Date: Tuesday, July 31, 2007 | Sheet 9 of 48



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<OrgAddr4>
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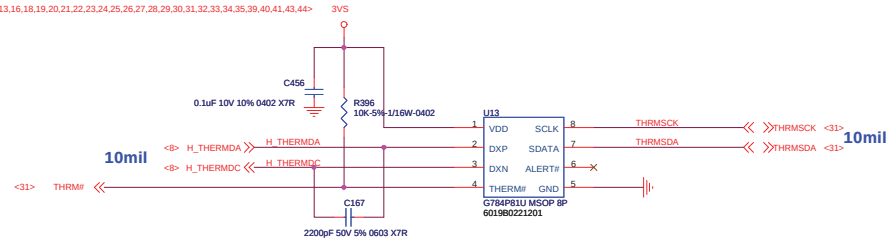
Title
Z11D (Merom+Crestline+ICH8M)

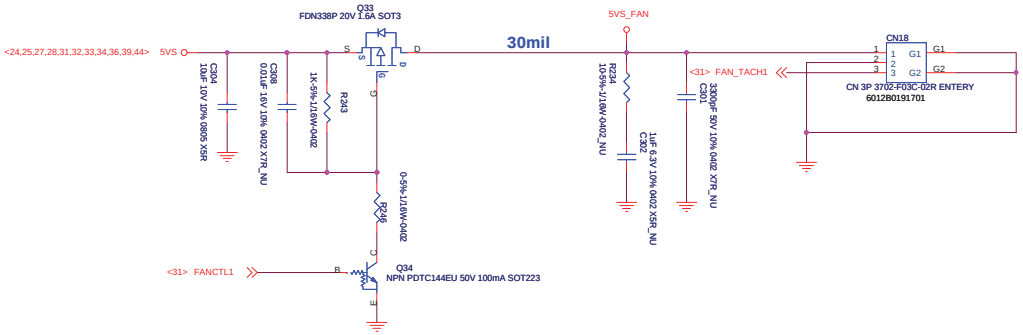
Size: Custom | Document Number: CPU Core Power | Rev: 0.4

Date: Tuesday, July 31, 2007 | Sheet 10 of 48

THERMAL SENSOR



Fan control



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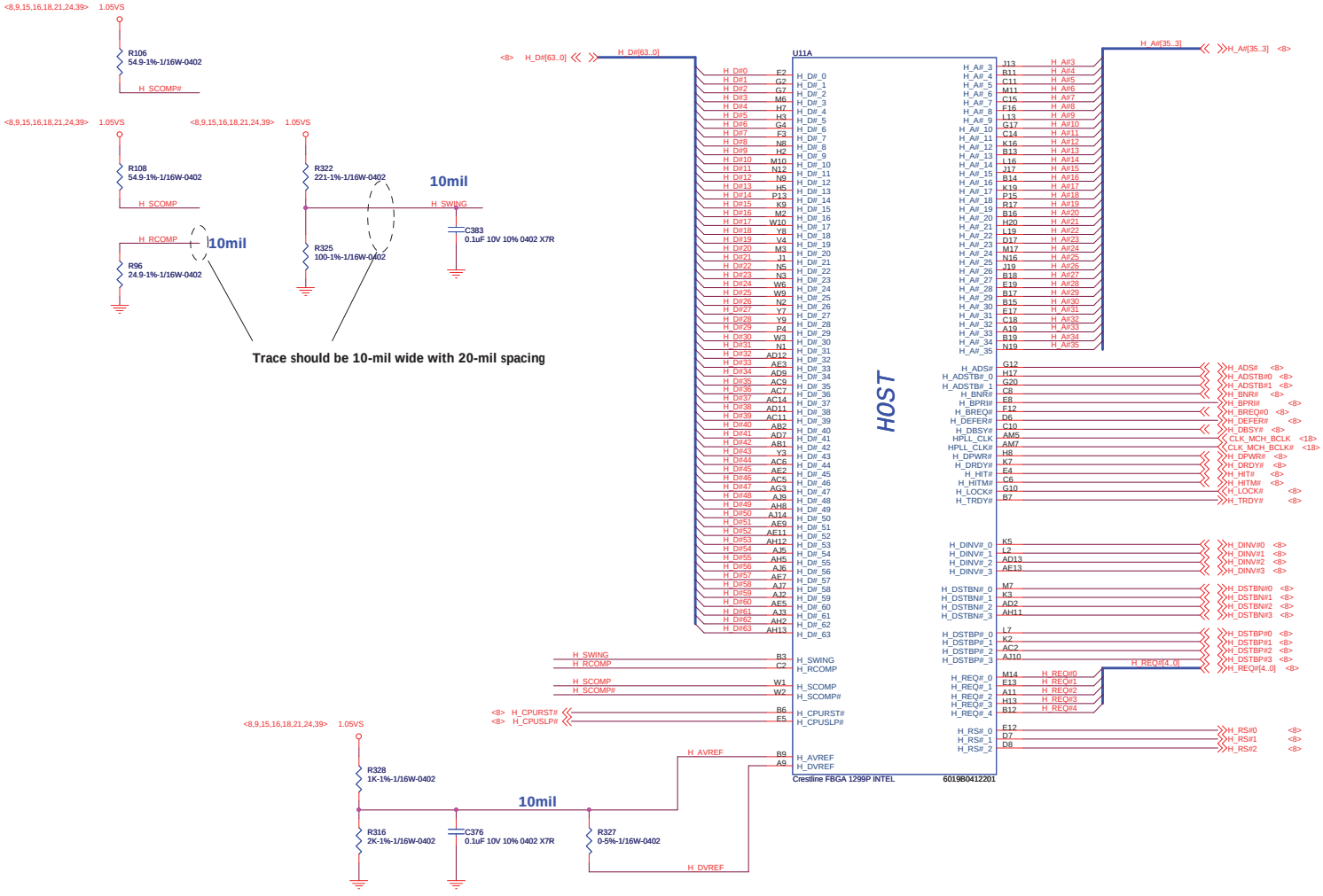
Title: Z11D (Merom+Crestline+ICH8M)
Size: C | Document Number: CPU Thermal | Rev: 0.4
Date: Tuesday, July 31, 2007 | Sheet 11 of 48



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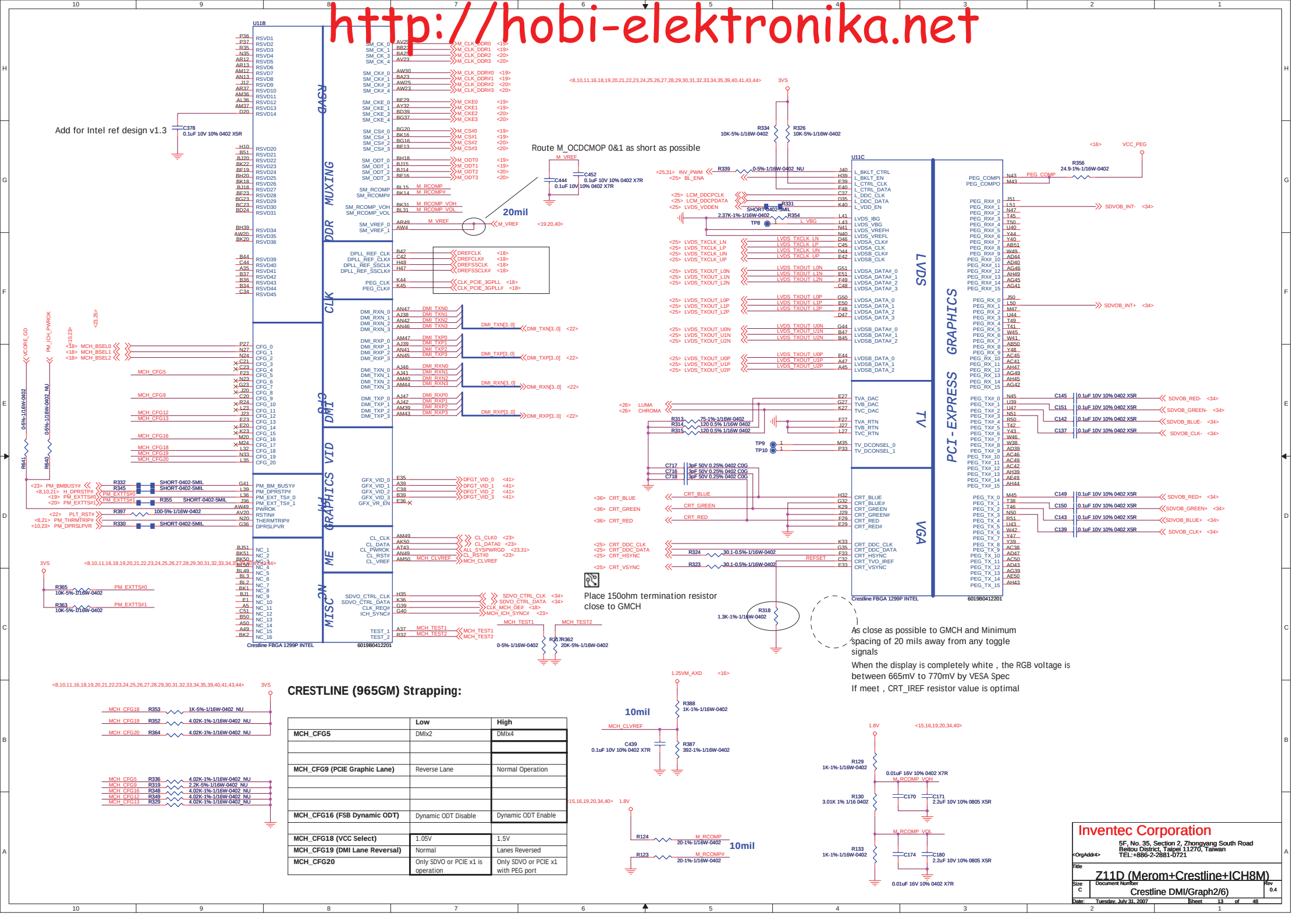
Title: Z11D (Merom+Crestline+ICH8M)	
Size: C	Document Number: Crestline Host(1/6)
Rev: 0.4	
Date: Tuesday, July 31, 2007	Sheet 12 of 48



	Low	High
MCH_CFG5	DMIx2	DMIx4
MCH_CFG9 (PCIE Graphic Lane)	Reverse Lane	Normal Operation
MCH_CFG16 (FSB Dynamic ODT)	Dynamic ODT Disable	Dynamic ODT Enable
MCH_CFG18 (VCC Select)	1.05V	1.5V
MCH_CFG19 (DMI Lane Reversal)	Normal	Lanes Reversed
MCH_CFG20	Only SDVO or PCIE x1 is operation	Only SDVO or PCIE x1 with PEG port

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5F, No. 35, Section 2, Zhongyang South Road
Beitou District, Taipei 11270, Taiwan
TEL:+886-2-2881-0721
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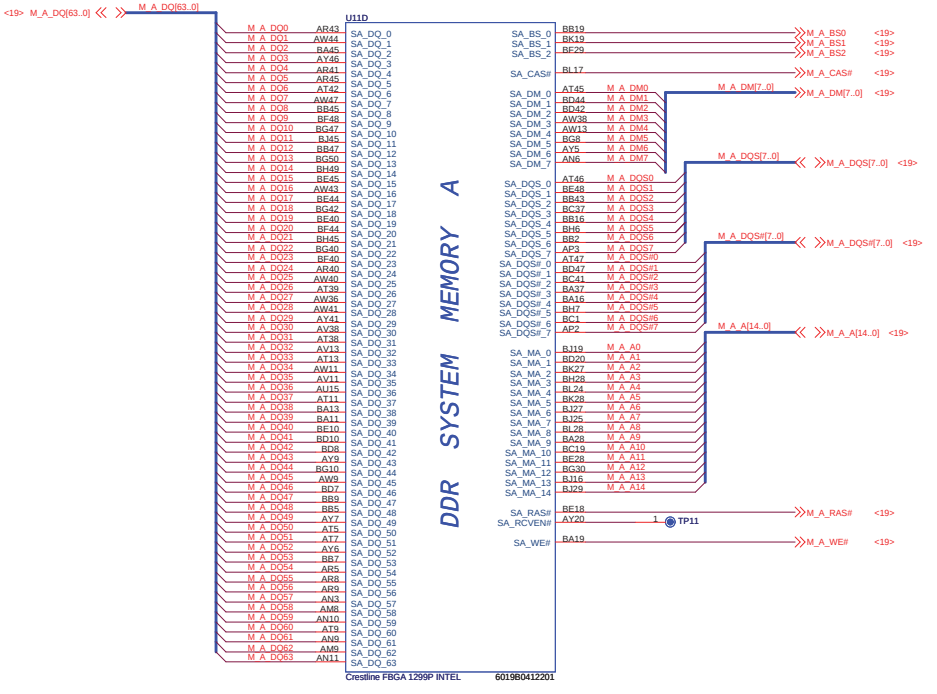
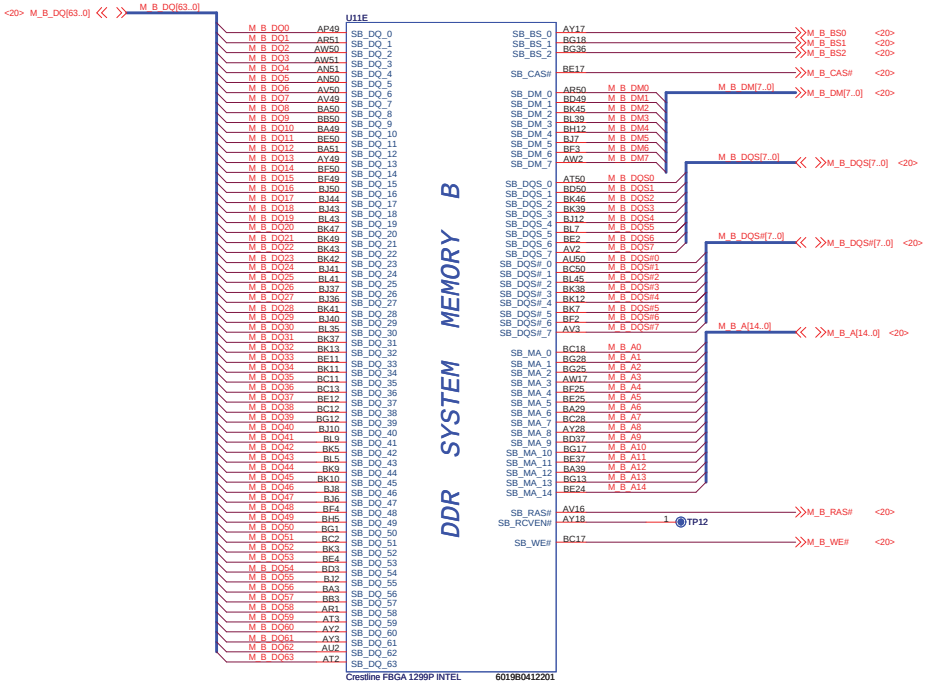
Title: Z11D (Merom+Crestline+ICH8M)
Size: C | Document Number: Crestline DMI/Graph2/6) | Rev: 0.4
Date: Tuesday, July 31, 2007 | Sheet 13 of 48





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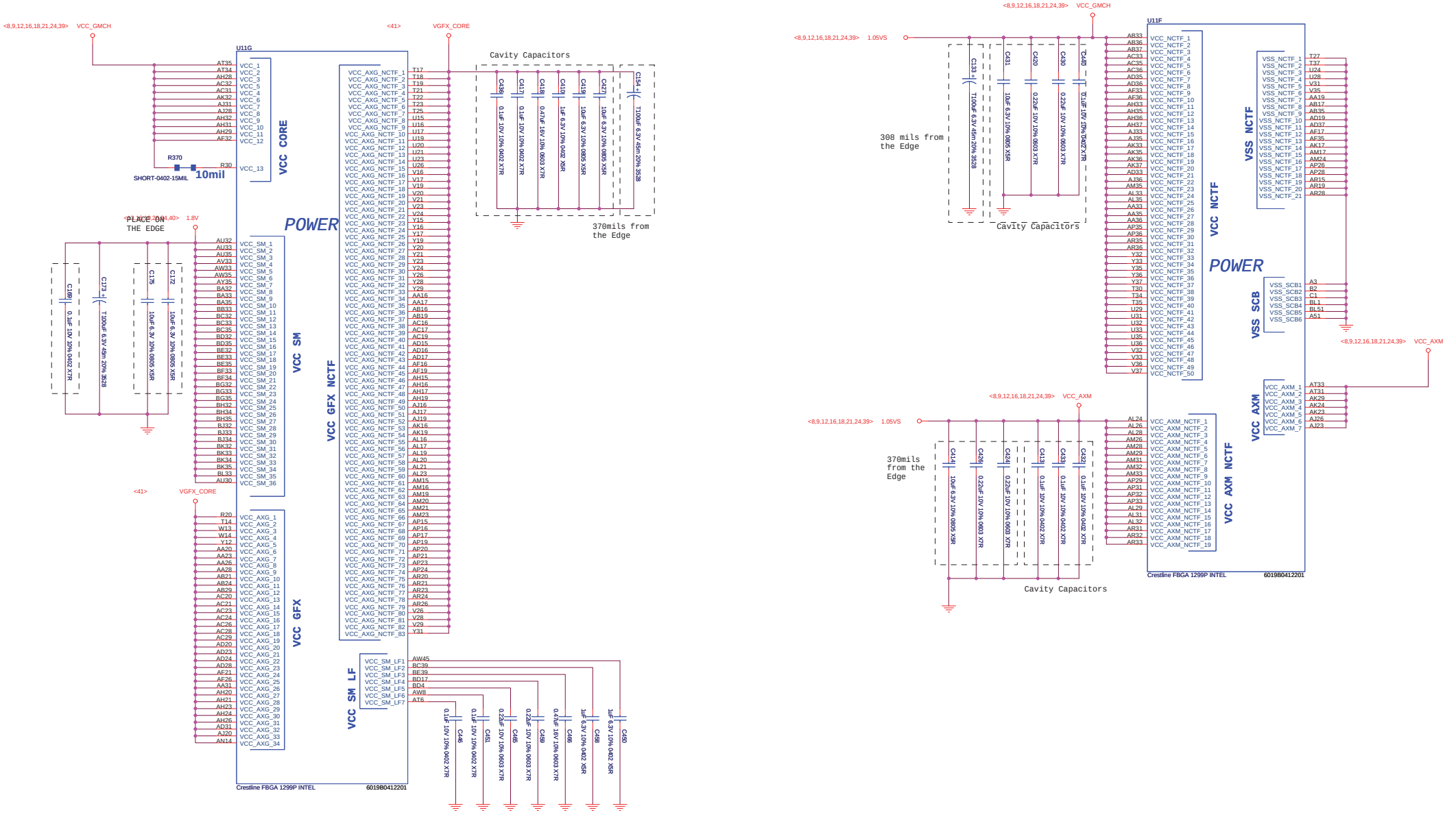
Title: Z11D (Merom+Crestline+ICH8M)

Size: C | Document Number: Crestline DDRII(3/6) | Rev: 0.4

Date: Tuesday, July 31, 2007 | Sheet 14 of 48



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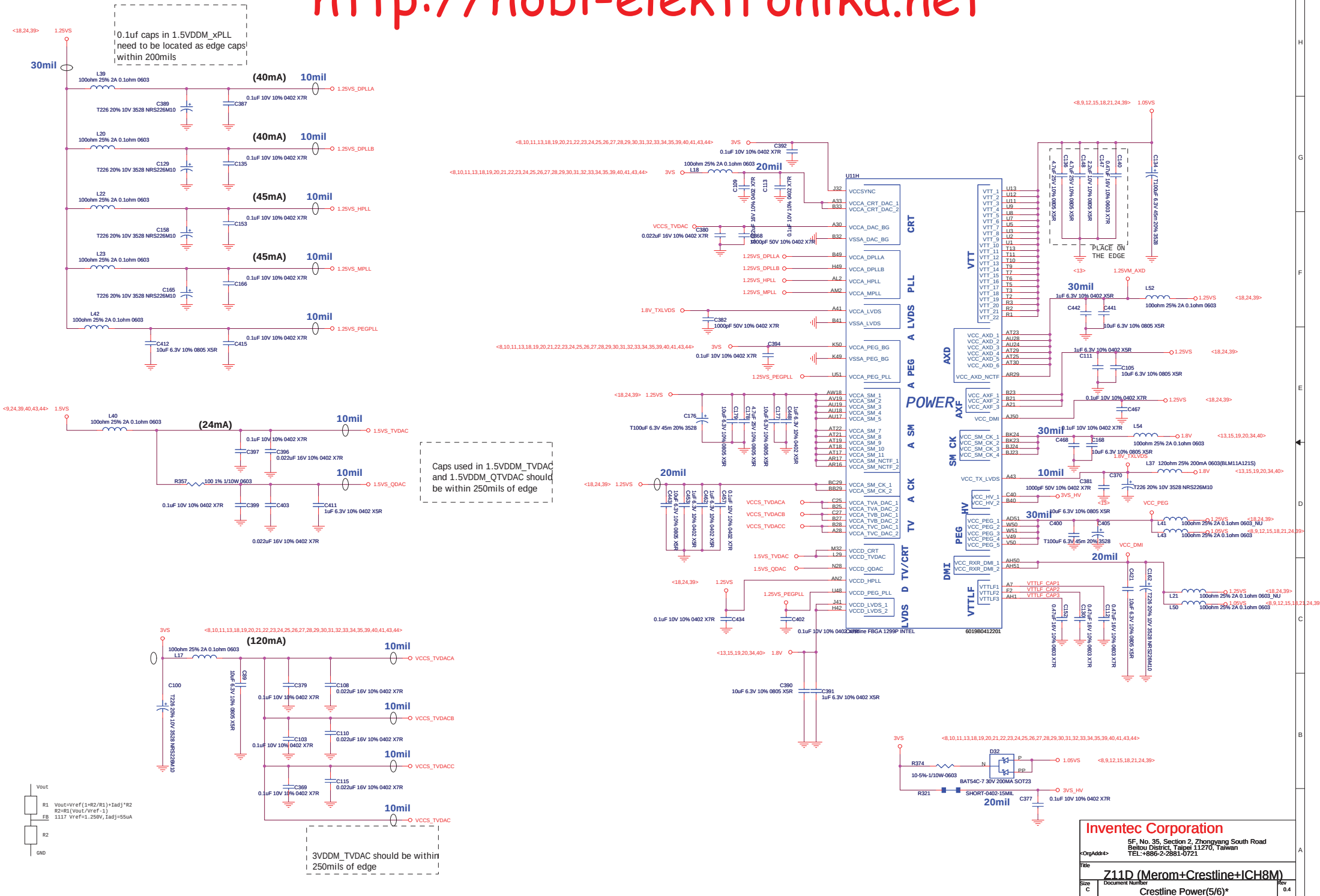
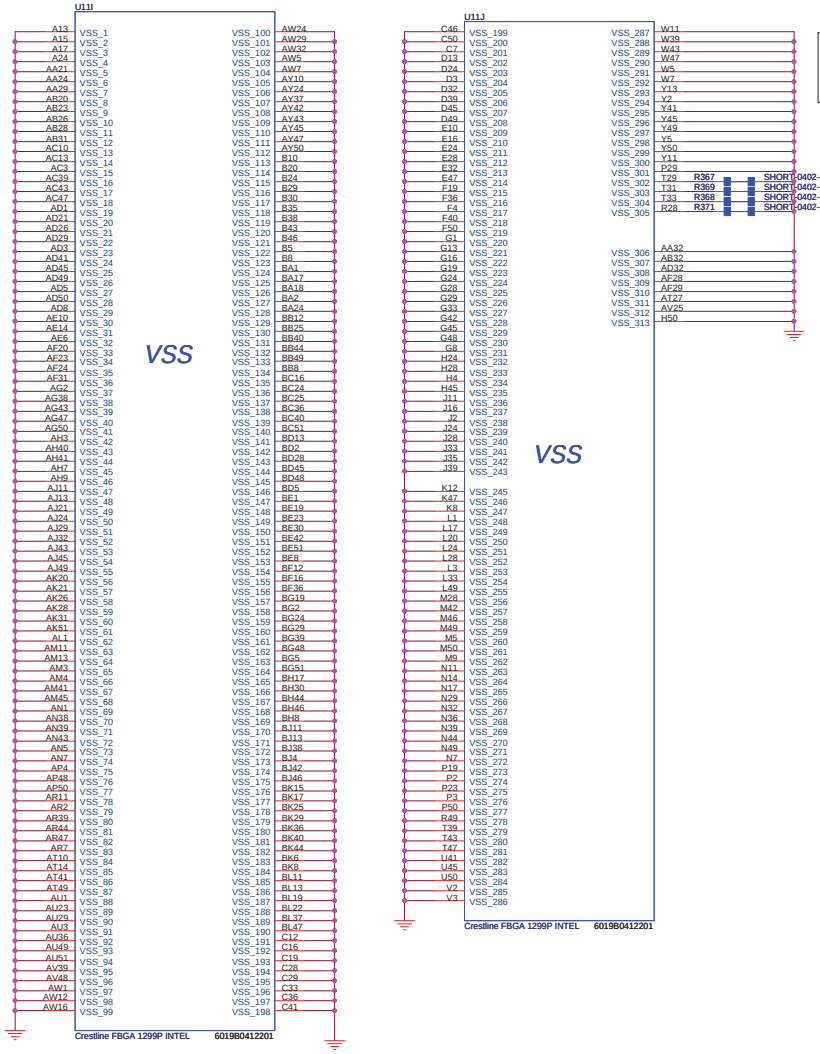
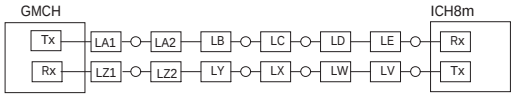
Size: C | Document Number: Crestline Power(4/6) | Rev: 0.4
Date: Tuesday, July 31, 2007 | Sheet 15 of 48





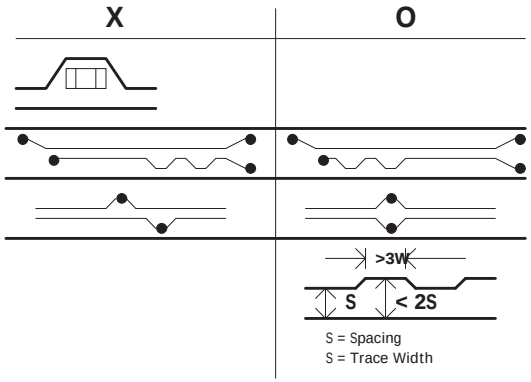
DMI Routing Guideline



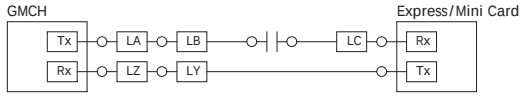
Breakout/in LA/LZ	Main Route LB/LY		Breakout/in LE/LV
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip

Parameter	Main Route Guideline	Breakout Guideline
Uncoupled Single End Impedance	55 +/- 15%	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils	
Nominal Didderential Pair-Pitch	Inner Layer : 7 mils Outer Layer : 7 mils	Inner Layer : 4 mils Outer Layer : 5 mils
Pair-to-Pair Pitch	Inner Layer : 37 mils Outer Layer : 37 mils	Inner Layer : 27 mils Outer Layer : 27 mils
Bus-to-Bus Pitch	Inner Layer : 22 mils Outer Layer : 20 mils	Inner Layer : 15 mils Outer Layer : 12 mils
Reference Plane	Ground	Ground
Splits/Voids	No routing over plane splits No routing over voids	
Trace Length-LA (GMCH Breakout)	Max = 250 mils	
Trace Length-LB (GMCH Breakout to Via2)	Max = 3600 mils	
Trace Length-LC (Via2 to Via3)	Max = 5900 mils	
Trace Length-LD (Via3 to ICH7m Breakout)	Max = 3600 mils	
Trace Length-LE (ICH7m Breakout)	Max = 400 mils	
Trace Length-L1 (LA+LB+LC+LD+LE)	Max = 8000 mils	
Trace Length-LV (ICH7m Breakout)	Max = 400 mils	
Trace Length-LW (ICH7m Breakout to Via2)	Max = 3600 mils	
Trace Length-LX (Via2 to Via3)	Max = 5900 mils	
Trace Length-LY (Via3 to GMCH Breakout)	Max = 3600 mils	
Trace Length-LZ (GMCH Breakout)	Max = 400 mils	
Trace Length-L2 (LV+LW+LX+LY+LZ)	Max = 8000 mils	

*** When routing near the edge of their reference plane , trace should maintain at least 40 mils space to the edge of the plane
*** Match the trace lengths of the complementary signals within each differential pair to +/- 5 mils



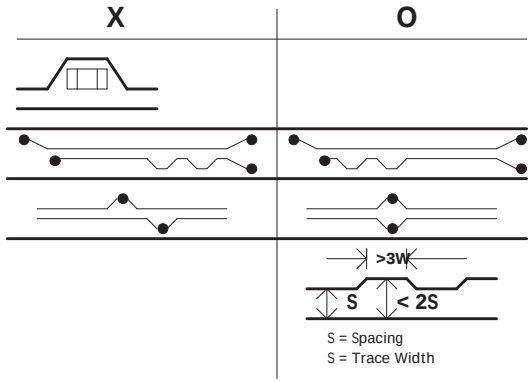
PCIE Routing Guideline



Breakout/in LA/LZ	Main Route LB/LC/LY	Main Route LD/LW	Breakout/in LE/LV
Stripline	Microstrip	Same Routing layer as LE/LV	Microstrip

Parameter	Main Route Guideline	Breakout Guideline
Uncoupled Single End Impedance	55 +/- 15%	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils	
Nominal Differential Trace Space	Inner Layer : 7 mils Outer Layer : 7 mils	Inner Layer : 4 mils Outer Layer : 5 mils
Pair-to-Pair Pitch	Inner Layer : 37 mils Outer Layer : 37 mils	Inner Layer : 27 mils Outer Layer : 27 mils
Bus-to-Bus Pitch	Inner Layer : 20 mils Outer Layer : 20 mils	Inner Layer : 15 mils Outer Layer : 12 mils
Reference Plane	Ground	Ground
Splits/Voids	No routing over plane splits No routing over voids	
Trace Length-LA (ICH7m Breakout)	Max = 400 mils	
Trace Length-LB (ICH7m Breakout to AC cap)	Max = 10750 mils	
Trace Length-LC (AC cap to PCIe CN)	Max = 10750 mils	
Trace Length-L1 (LA+LB+LC)	Max = 12000 mils	
Trace Length-LY (PCIe CN to ICH7m Breakout)	Max = 11950 mils	
Trace Length-LZ (ICH7m Breakout)	Max = 400 mils	
Trace Length-L2 (LY+LZ)	Max = 12000 mils	

*** When routing near the edge of their reference plane , trace should maintain at least 40 mils space to the edge of the plane
*** Match the trace lengths of the complementary signals within each differential pair to +/- 5 mils



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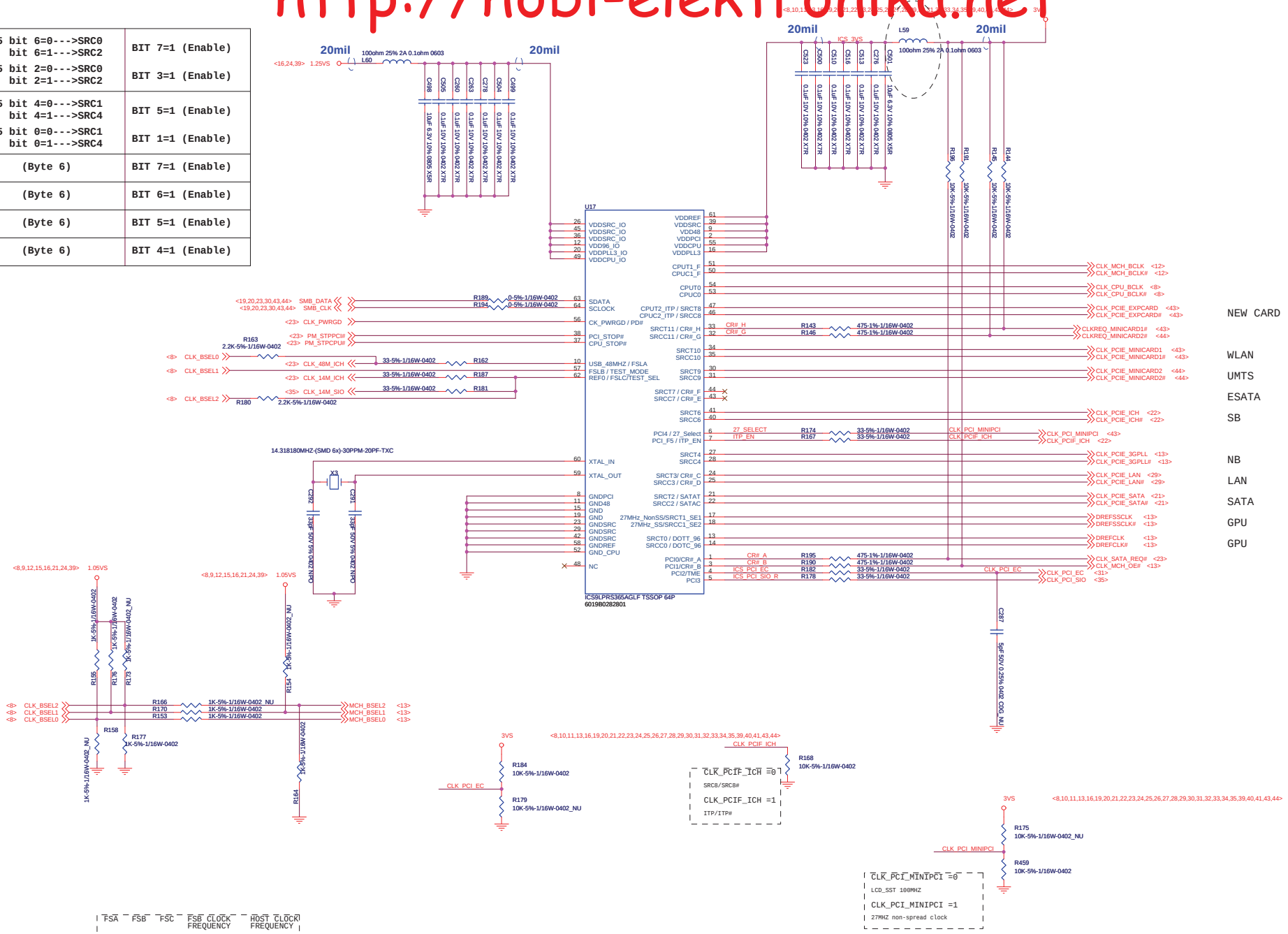
Title: Z11D (Merom+Crestline+ICH8M)
Size: C | Document Number: Crestline Ground(6/6) | Rev: 0.4
Date: Tuesday, July 31, 2007 | Sheet 17 of 48

MODIFY L11A471S

CR#_A: CR#_C:	Byte 5 bit 6=0--->SRC0 bit 6=1--->SRC2 Byte 5 bit 2=0--->SRC0 bit 2=1--->SRC2	BIT 7=1 (Enable) BIT 3=1 (Enable)
CR#_B: CR#_D:	Byte 5 bit 4=0--->SRC1 bit 4=1--->SRC4 Byte 5 bit 0=0--->SRC1 bit 0=1--->SRC4	BIT 5=1 (Enable) BIT 1=1 (Enable)
CR#_E:	SRC6 (Byte 6)	BIT 7=1 (Enable)
CR#_F:	SRC8 (Byte 6)	BIT 6=1 (Enable)
CR#_G:	SRC9 (Byte 6)	BIT 5=1 (Enable)
CR#_H:	SRC10 (Byte 6)	BIT 4=1 (Enable)



FSA	FSB	FSC	FSB CLOCK FREQUENCY	HOST CLOCK FREQUENCY	
1	1	0	667	166	
0	1	0	800	200	*

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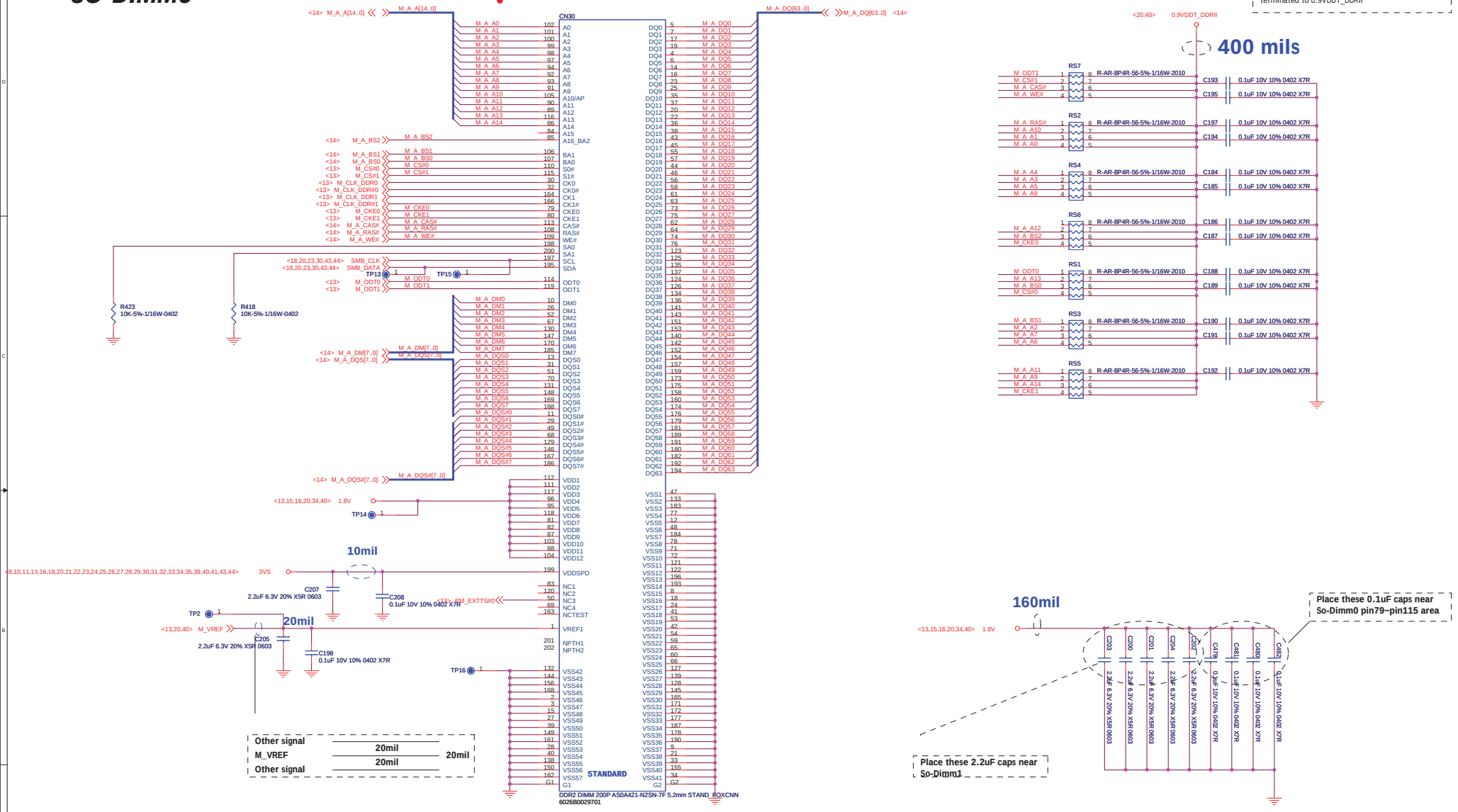
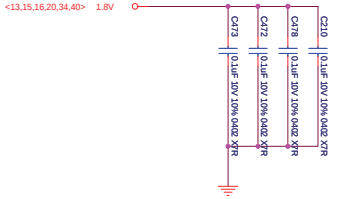
Size: C | Document Number: Clock Generator | Rev: 0.4
Date: Tuesday, July 31, 2007 | Sheet 18 of 48

SO-DIMM0



Place one cap close to every 2 pullup resistors terminated to 0.9VDDT_DDRII



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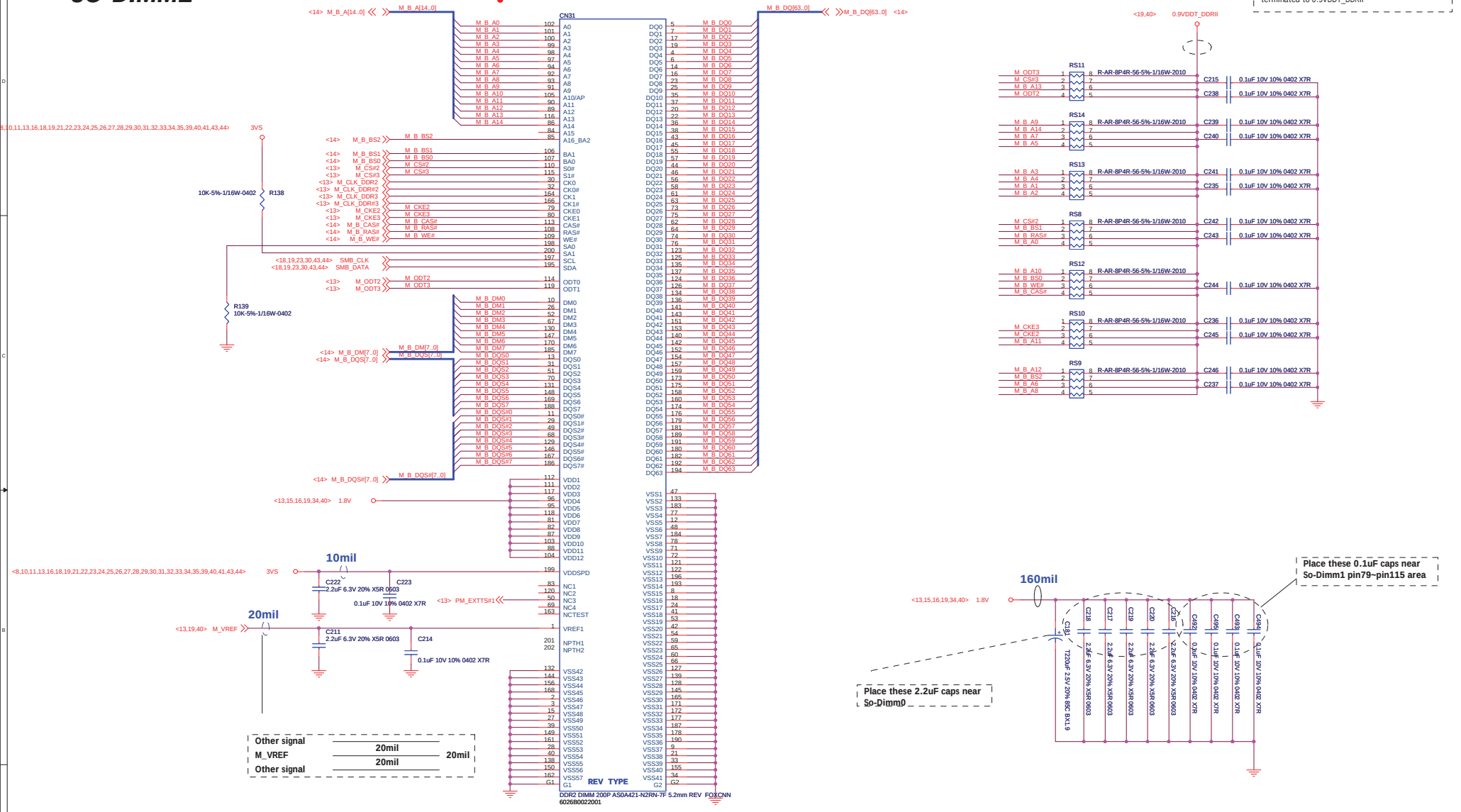
Title: Z11D (Merom+Crestline+ICH8M)	
Size: C	Document Number: DDR2 SDRAM SO-DIMM0 — Rev: 0.4
Date: Tuesday, July 31, 2007	Sheet 19 of 48

SO-DIMM1



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Title: Z11D (Merom+Crestline+ICH8M)

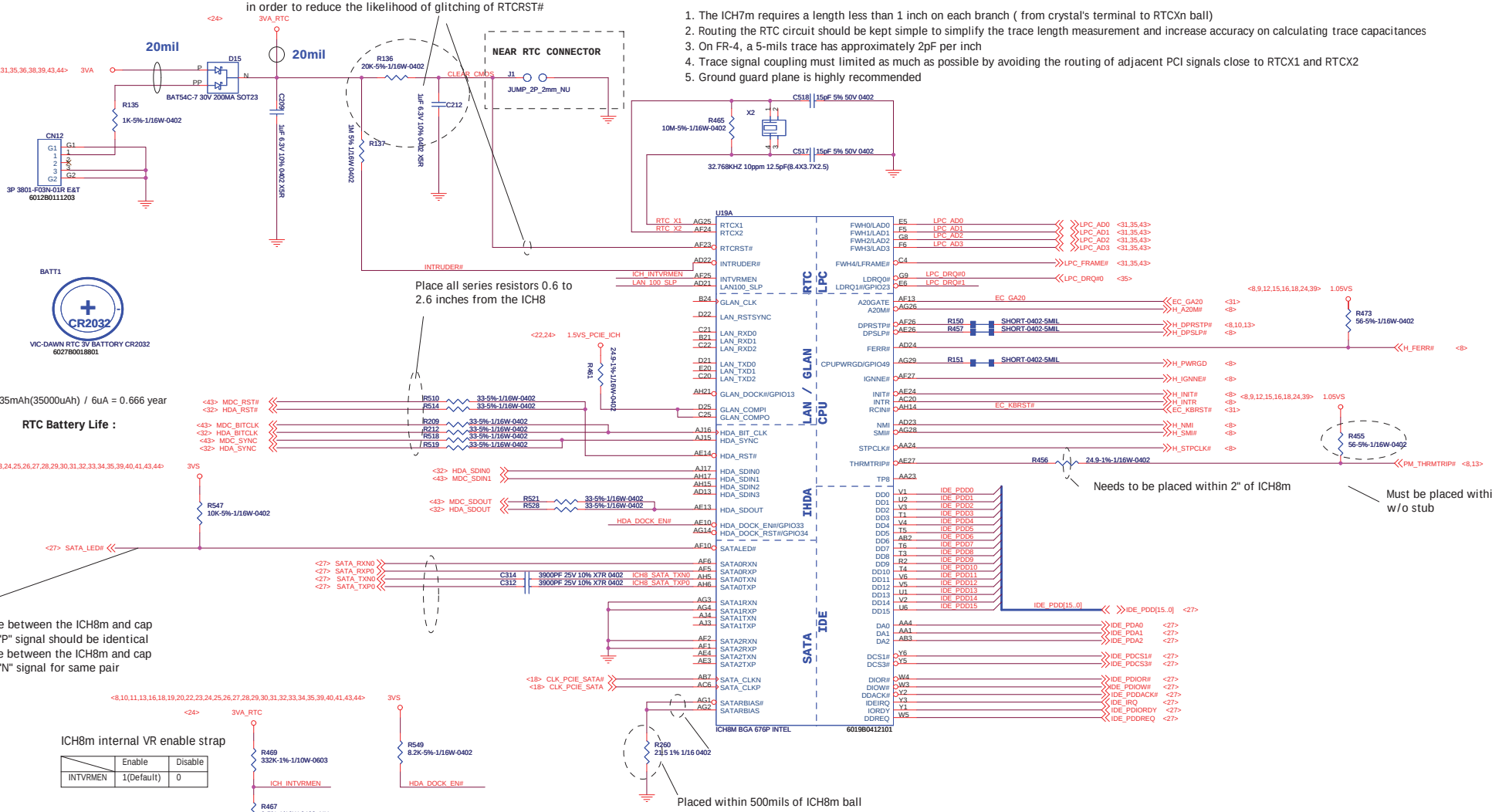
Size: C | Document Number: DDR2 SDRAM SO-DIMM1 | Rev: 0.4

Date: Tuesday, July 31, 2007 | Sheet 20 of 48

RTC Circuit

1. RC delay time should be in the range of 18~25ms
2. It is recommended that this larger capacitor and small resistor value in order to reduce the likelihood of glitching of RTCRST#

1. The ICH7m requires a length less than 1 inch on each branch (from crystal's terminal to RTCXn ball)
2. Routing the RTC circuit should be kept simple to simplify the trace length measurement and increase accuracy on calculating trace capacitances
3. On FR-4, a 5-mils trace has approximately 2pF per inch
4. Trace signal coupling must limited as much as possible by avoiding the routing of adjacent PCI signals close to RTCX1 and RTCX2
5. Ground guard plane is highly recommended



	Enable	Disable
INTVRMEN	1(Default)	0

ICH8-M LAN100_SLP Strap
(Internal VR for VccLAN1_05 and VccCL1_05)

LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled (Default)

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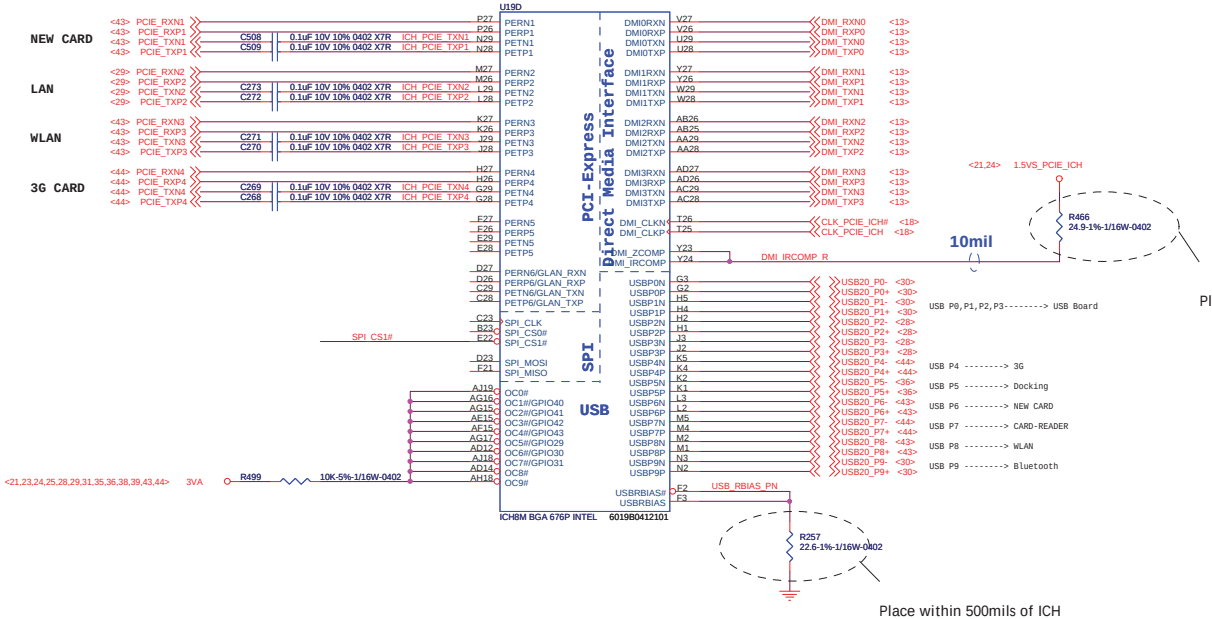
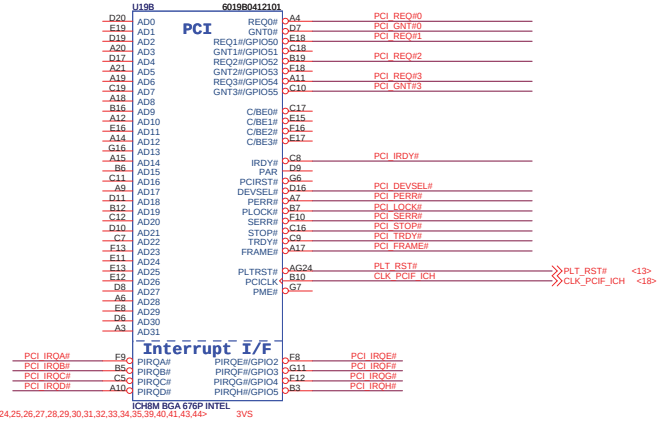
Size: C | Document Number: ICH8M CPU/IDE/SATA(1/4) | Rev: 0.4
Date: Tuesday, July 31, 2007 | Sheet 21 of 48

PCIE AC coupling caps need to be within 250mils of the driver

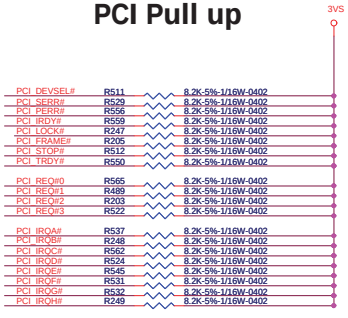


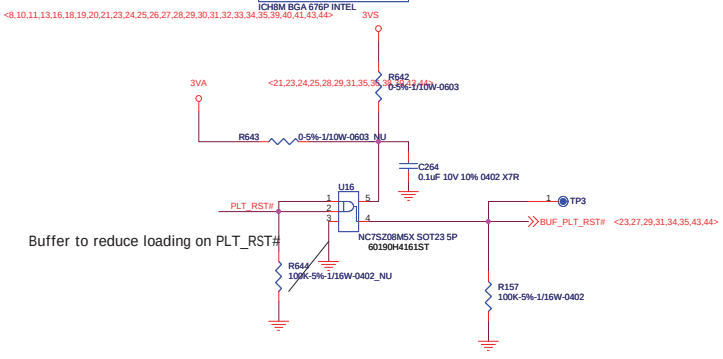
Place within 500mils of ICH

Place within 500mils of ICH
5/5 mils spacing on microstrip



PCI Pull up





Buffer to reduce loading on PLT_RST#

PCI_GNT#3	No stuff : by default Stuff : For A16 swap override

PCI_GNT#0	SPI_CS1#	
1	1	LPC
1	0	PCI
0	1	SPI

Check BIOS type

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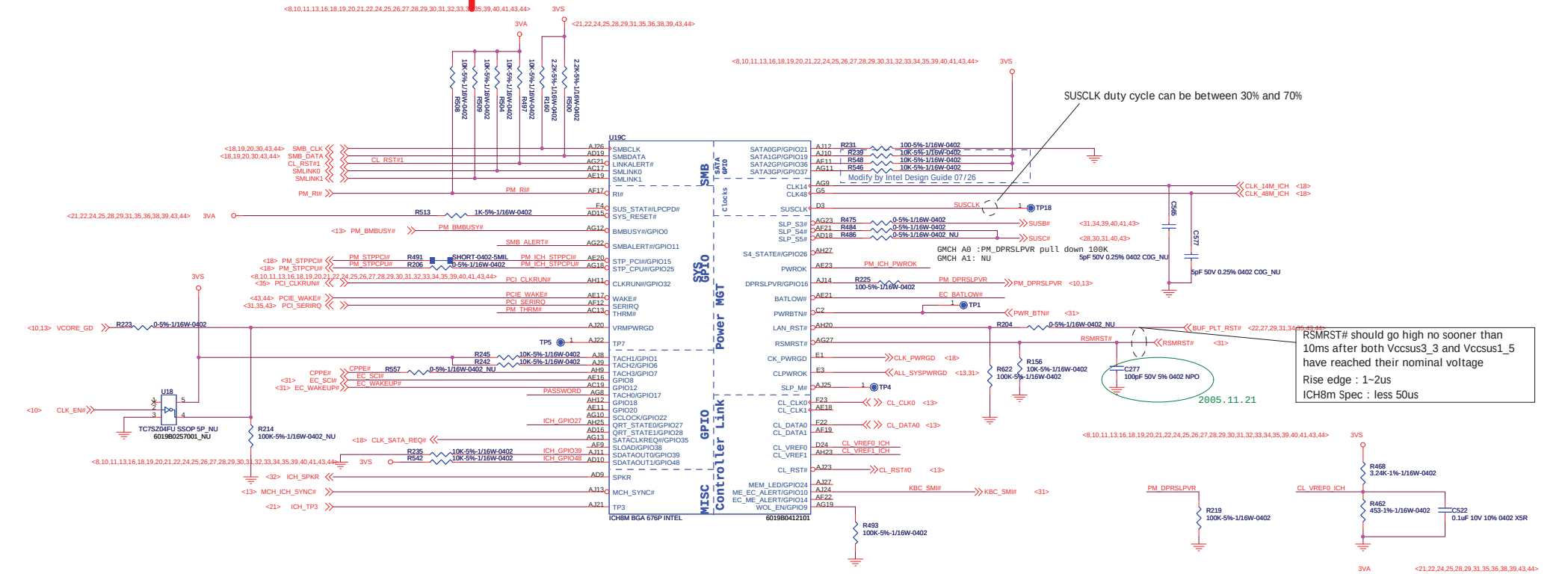
Size: C | Document Number: ICH8M PCI/PCIE/DMI/USB(2/4) | Rev: 0.4
Date: Tuesday, July 31, 2007 | Sheet 22 of 48



ICH8m strap

ACZ_SPKR	No stuff : by default Stuff : For NO reboot

ICH_SPKR R543 1K-5%-1/16W-0402_NU

ICH_GPIO27 R165 10K-5%-1/16W-0402

R171 0-5%-1/16W-0402_NU

Default is 1-X
Add 0ohm for BIOS Recovery

PMU P/U

EC_WAKEUP# R487 10K-5%-1/16W-0402
EC_SCI# R507 10K-5%-1/16W-0402
EC_BATLOW# R490 8.2K-5%-1/16W-0402
PCIE_WAKE# R515 1K-5%-1/16W-0402
SMB_ALERT# R485 10K-5%-1/16W-0402

KBC_SMI# R482 10K-5%-1/16W-0402

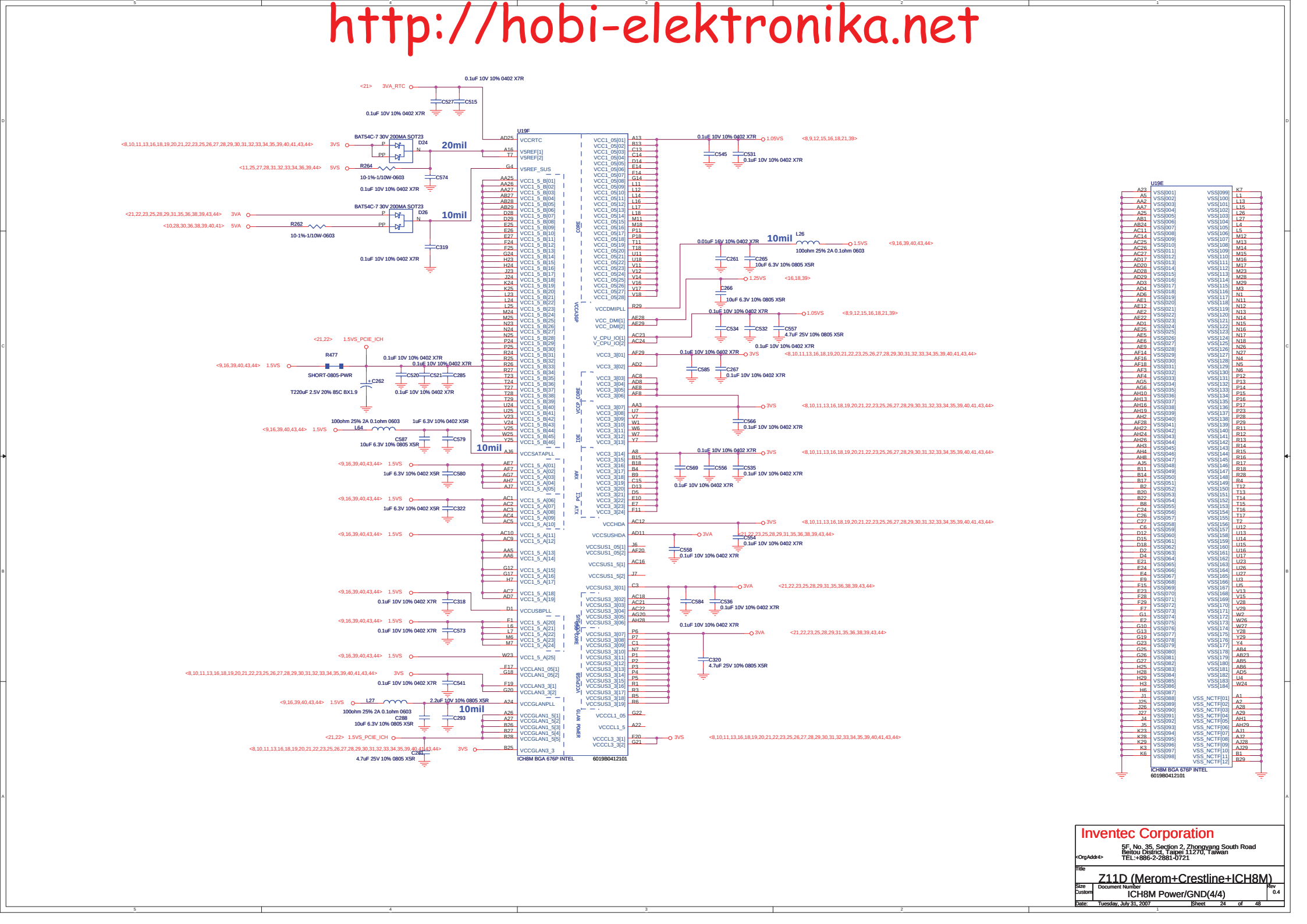
PM_THRM# R525 8.2K-5%-1/16W-0402
PCI_CLKRUN# R539 8.2K-5%-1/16W-0402

PM_STPPCI# R501 10K-5%-1/16W-0402_NU
PM_STPCPU# R208 10K-5%-1/16W-0402_NU
PCI_SERIRQ R555 10K-5%-1/16W-0402

PASSWORD CLEAR

R229 10K-5%-1/16W-0402
PASSWORD
J2 JUMP_2P_2mm_NU

Please close to door



LVDS Interface

LCD brightness control

INVERT CONTROL

Please as close as possible to the LVDS CONN

For VESA SPEC , R/G/B should be 665mV ~ 770mV

LENGTH MAX=0.5''

LENGTH MAX=0.5''

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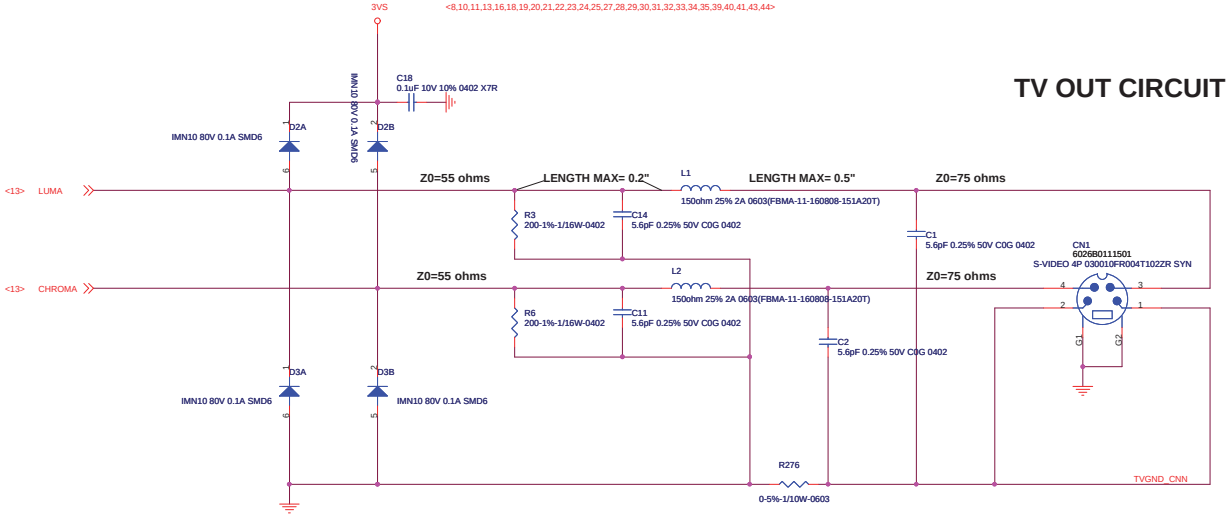
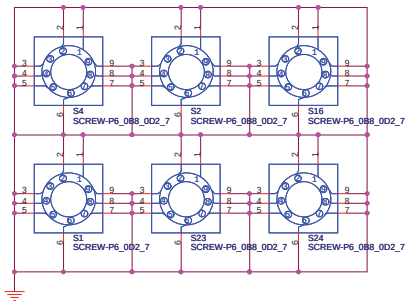
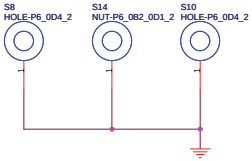
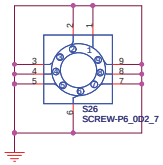
Size: Custom | Document Number: LCD&CRT | Rev: 0.4
Date: Tuesday, July 31, 2007 | Sheet 25 of 48

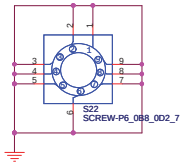
TV OUT CIRCUIT

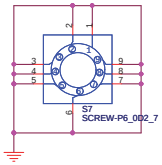


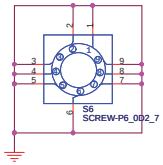












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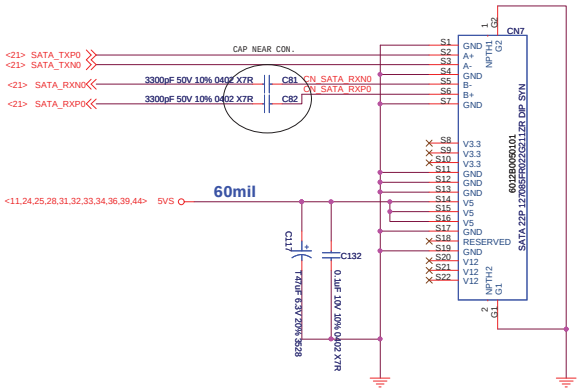
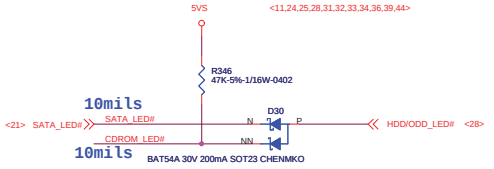
Size: Custom | Document Number: TV Connector | Rev: 0.4

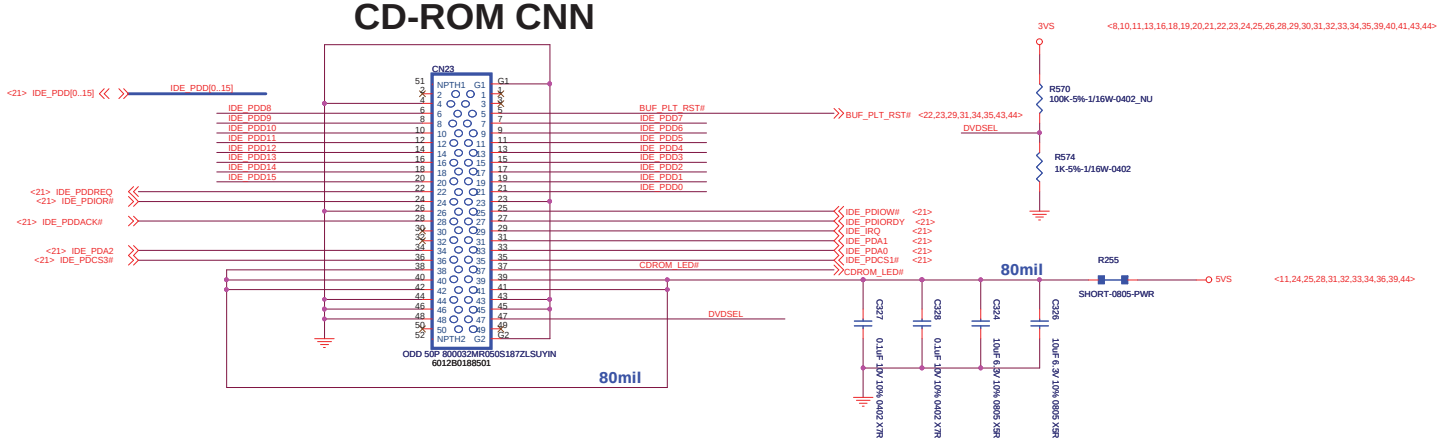
Date: Tuesday, July 31, 2007 | Sheet 26 of 48

HDD I/F





CD-ROM CNN



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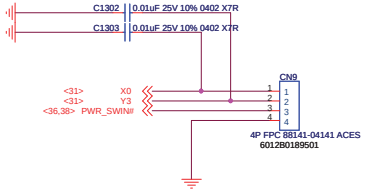
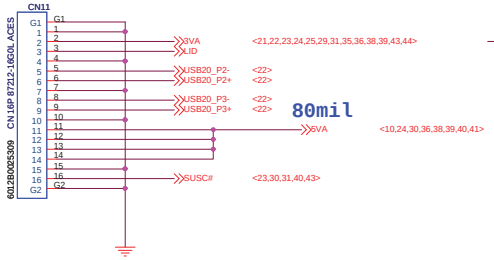
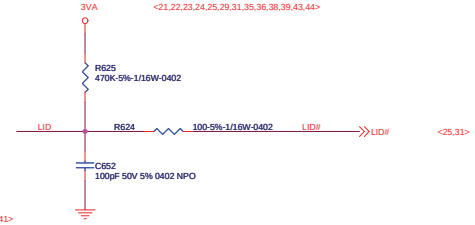
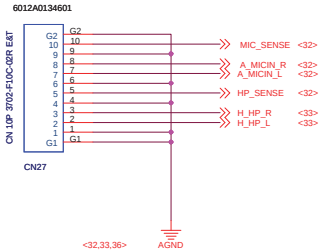
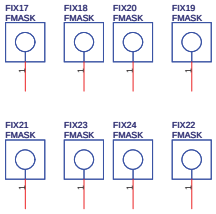
Size: Custom | Document Number: IDE&SATA | Rev: 0.4
Date: Tuesday, July 31, 2007 | Sheet 27 of 48











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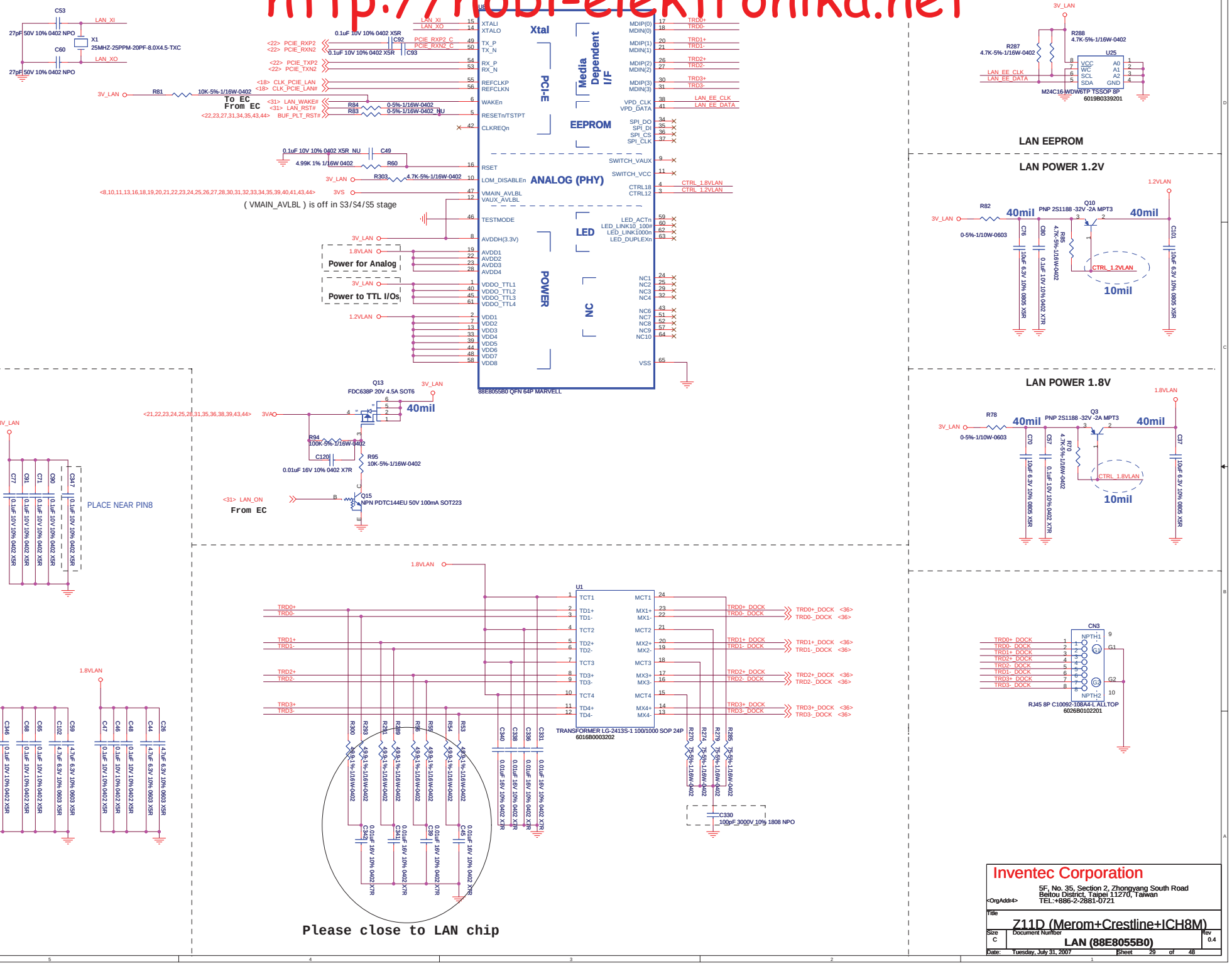
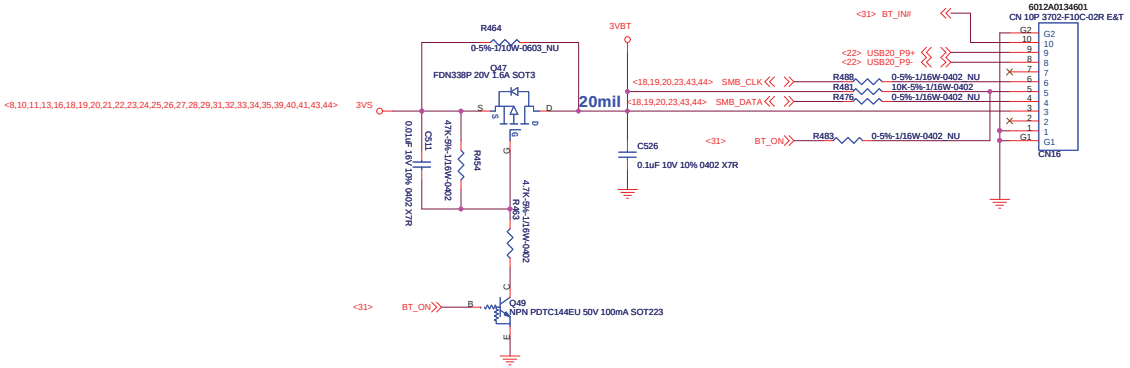
Size: Custom | Document Number: I/O Board CN(MB) | Rev: 0.4

Date: Tuesday, July 31, 2007 | Sheet 28 of 48



Bluetooth CON.



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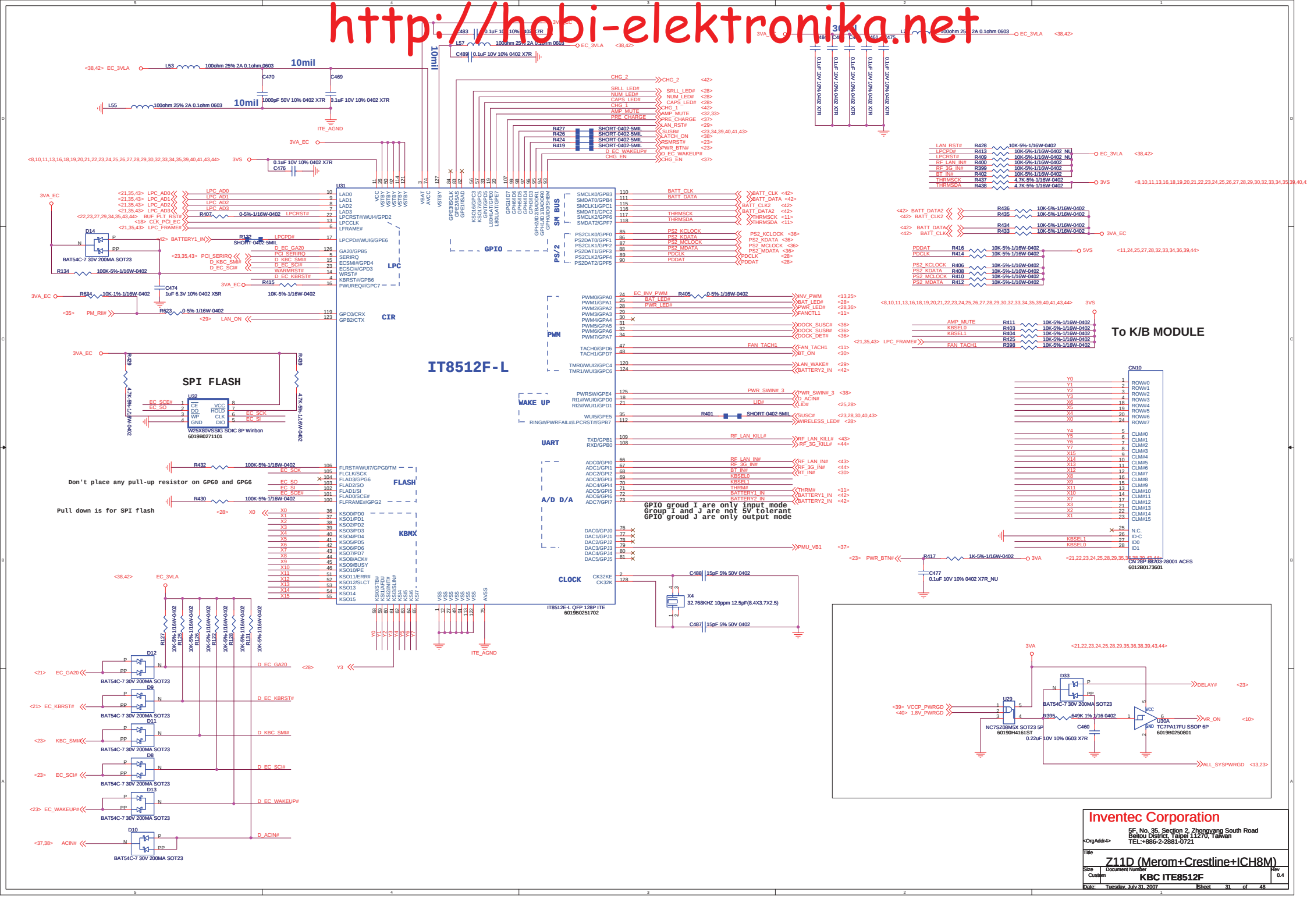
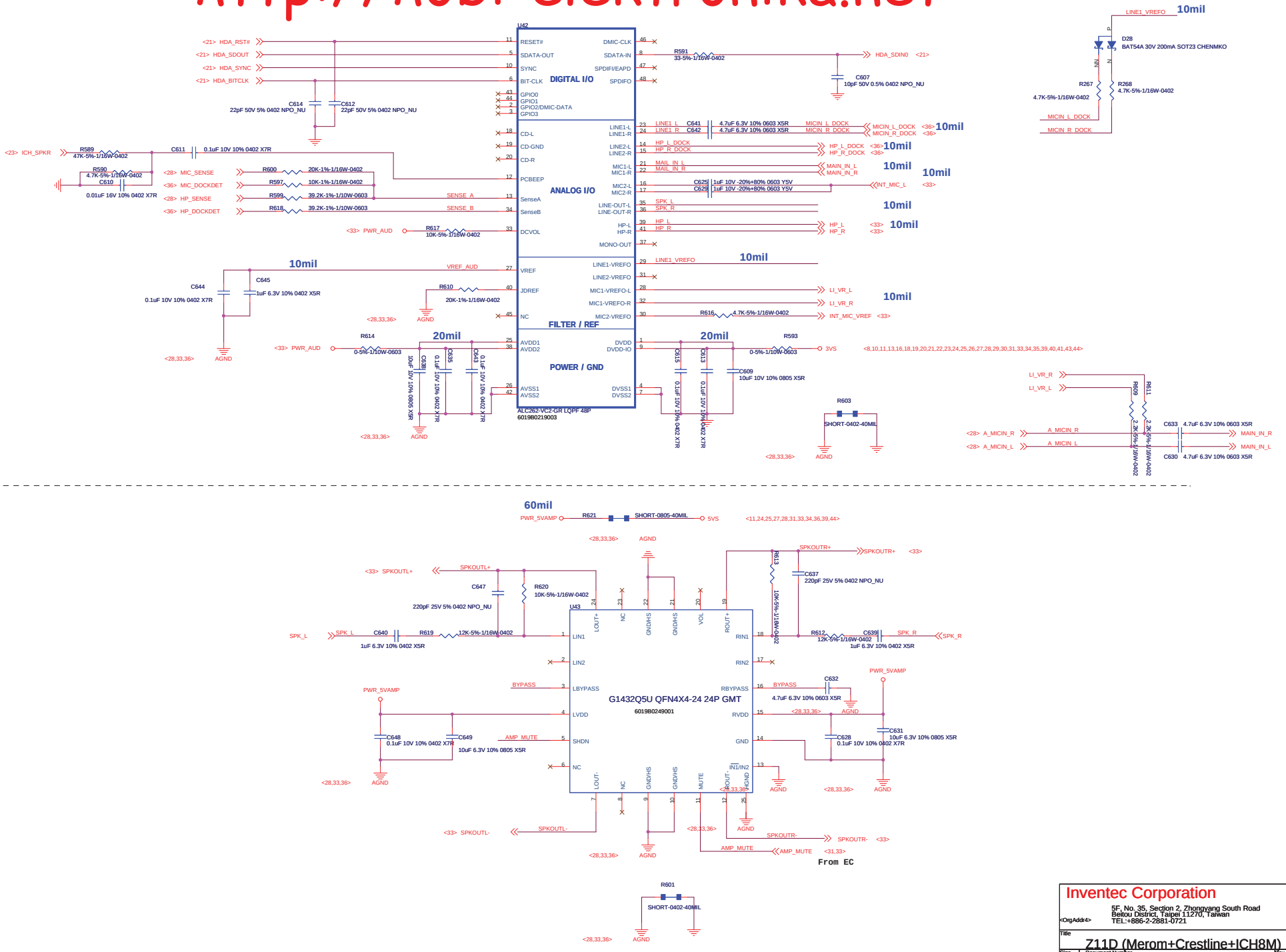
Title: Z11D (Merom+Crestline+ICH8M)

Size: Custom | Document Number: USB&Bluetooth Connector | Rev: 0.4

Date: Tuesday, July 31, 2007 | Sheet 30 of 48





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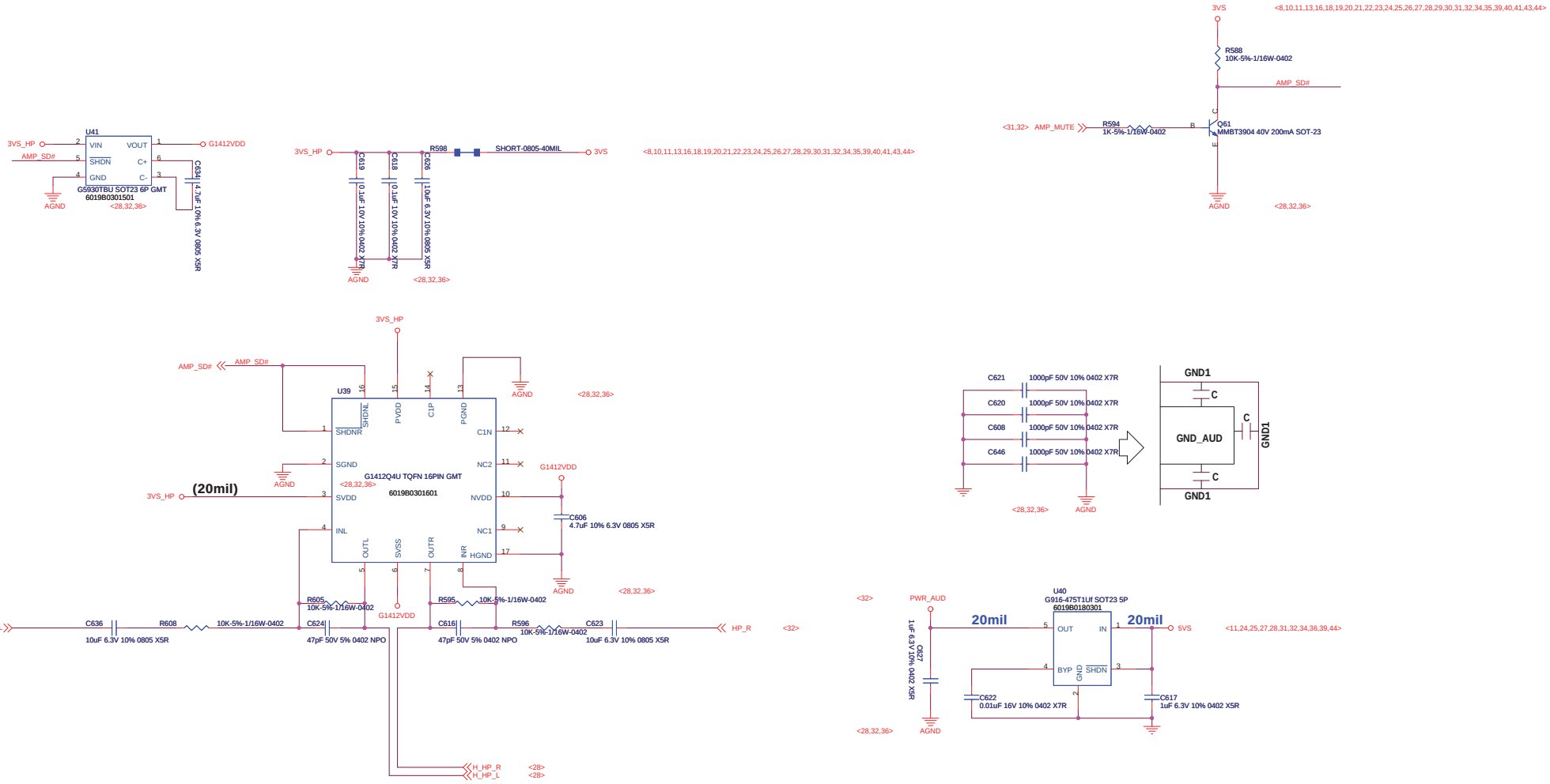
Title: Z11D (Merom+Crestline+ICH8M)

Size: Custom | Document Number: Audio Codec ALC262/AMP | Rev: 0.4

Date: Tuesday, July 31, 2007 | Sheet 32 of 48



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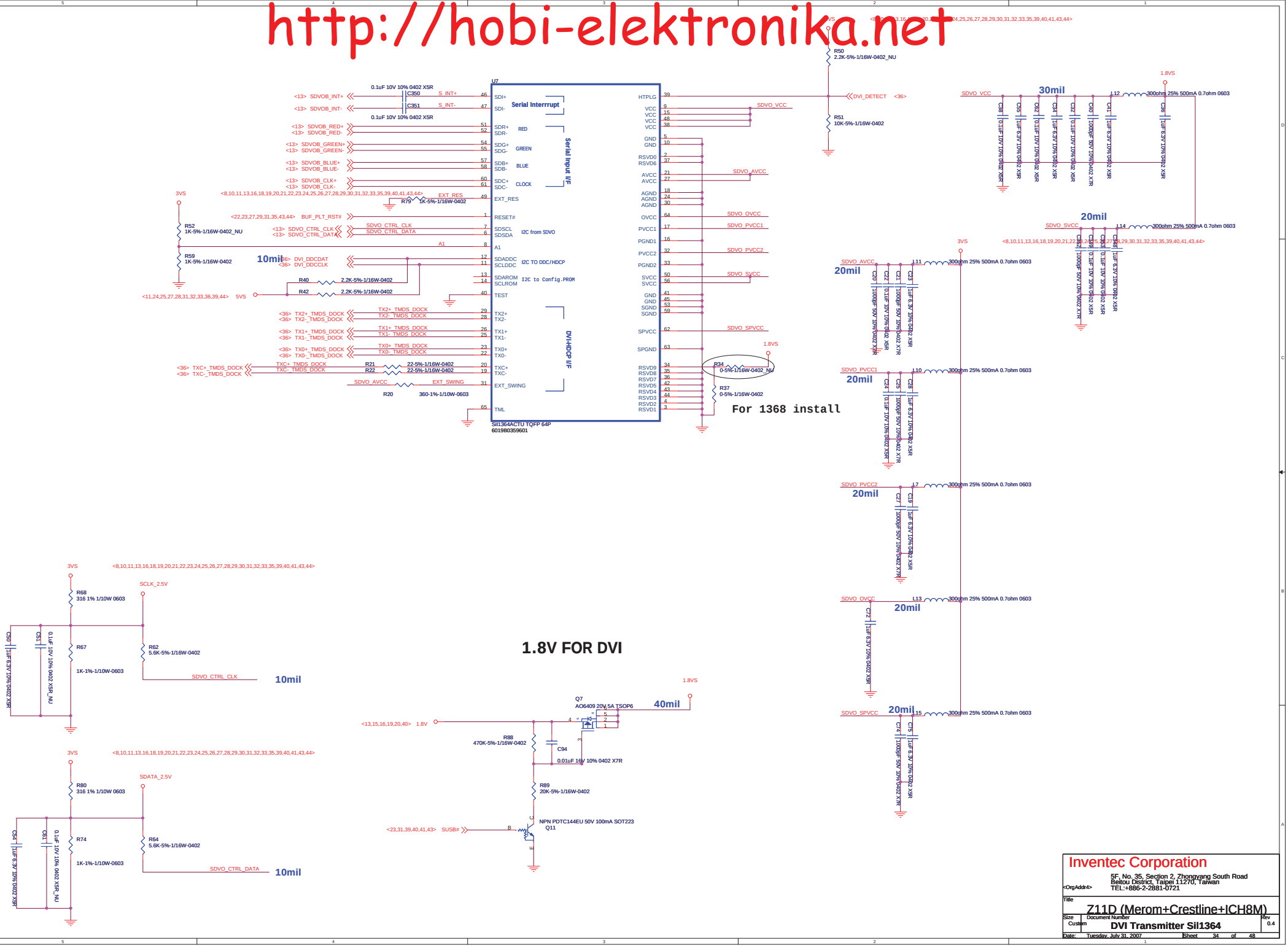
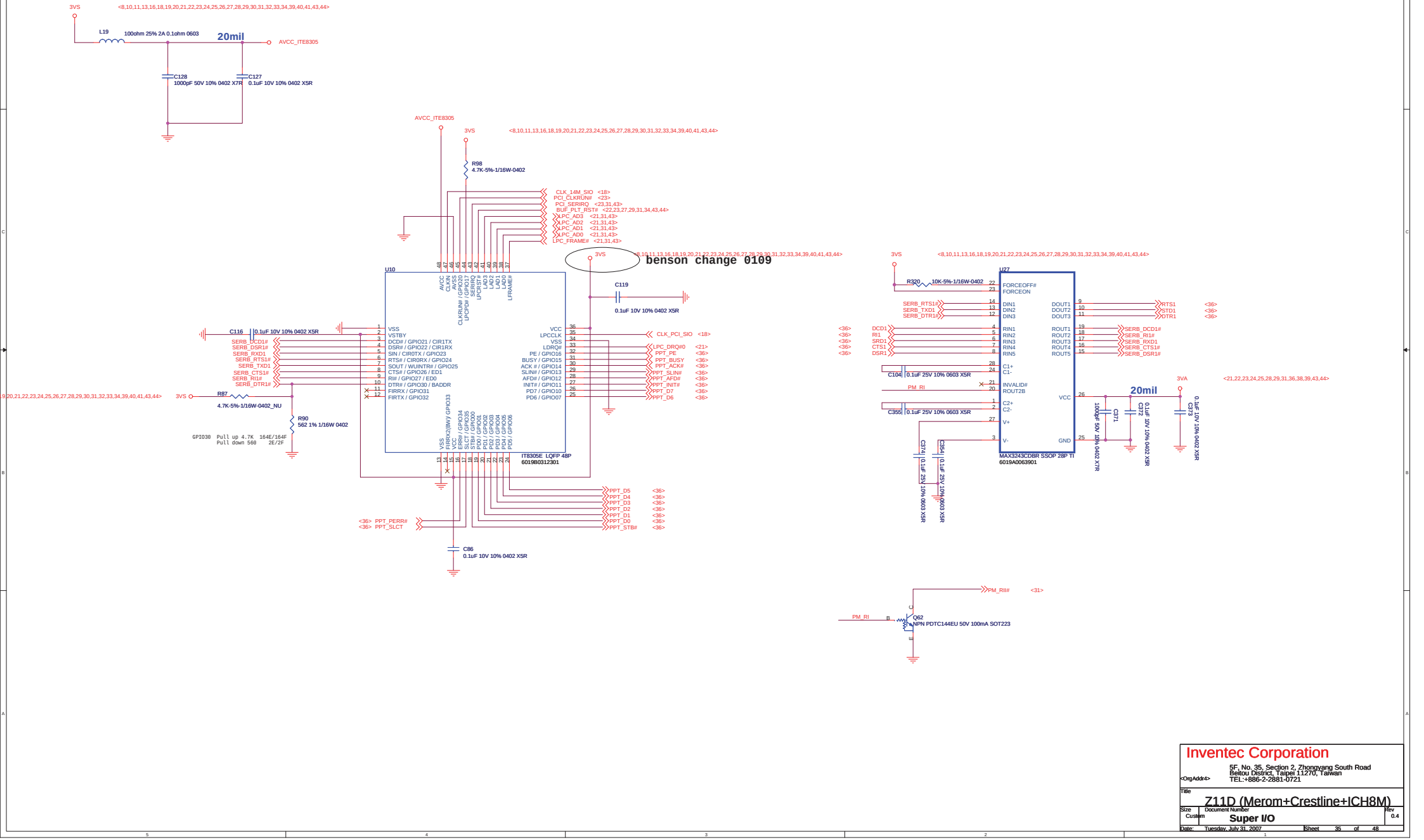
Title: Z11D (Merom+Crestline+ICH8M)

Size: C | Document Number: Audio Jack | Rev: 0.4

Date: Tuesday, July 31, 2007 | Sheet 33 of 48





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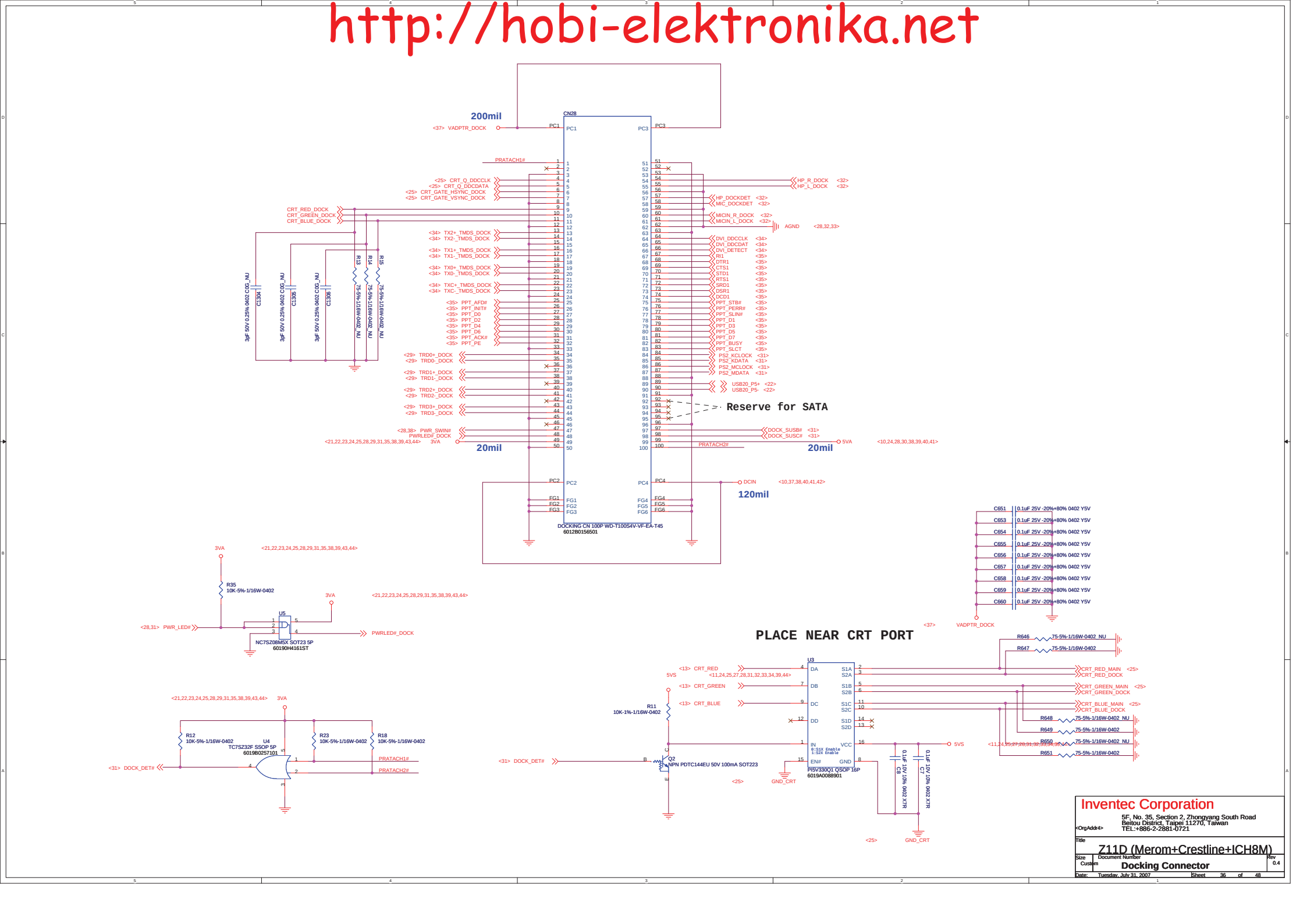
Title	Z11D (Merom+Crestline+ICH8M)
Size: Custom	Document Number: Super I/O
Rev: 0.4	
Date: Tuesday, July 31, 2007	Sheet 35 of 48



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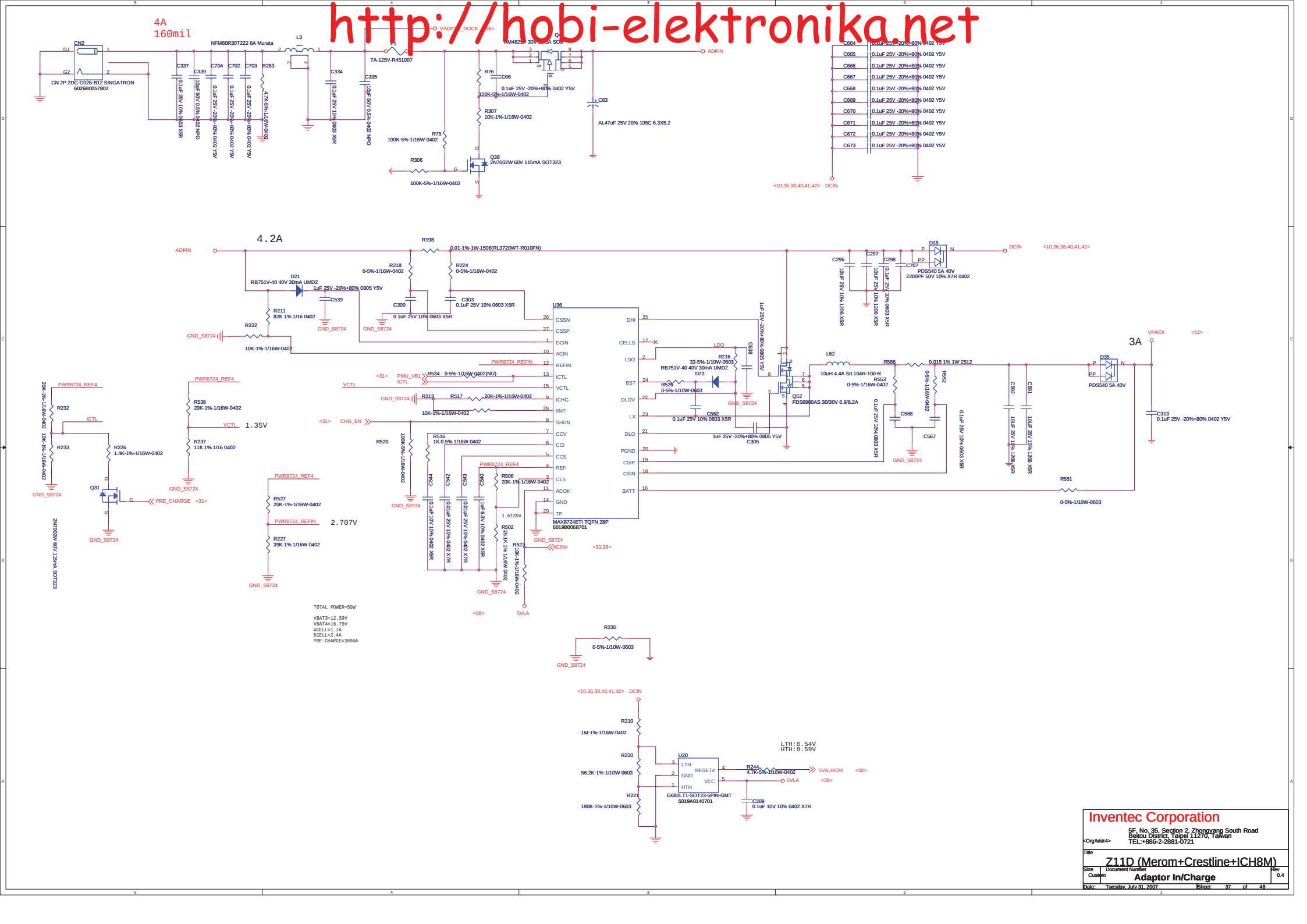
Title	Z11D (Merom+Crestline+ICH8M)
Size: Custom	Document Number: Docking Connector
Rev: 0.4	
Date: Tuesday, July 31, 2007	Sheet 36 of 48



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Title: Z11D (Merom+Crestline+ICH8M)
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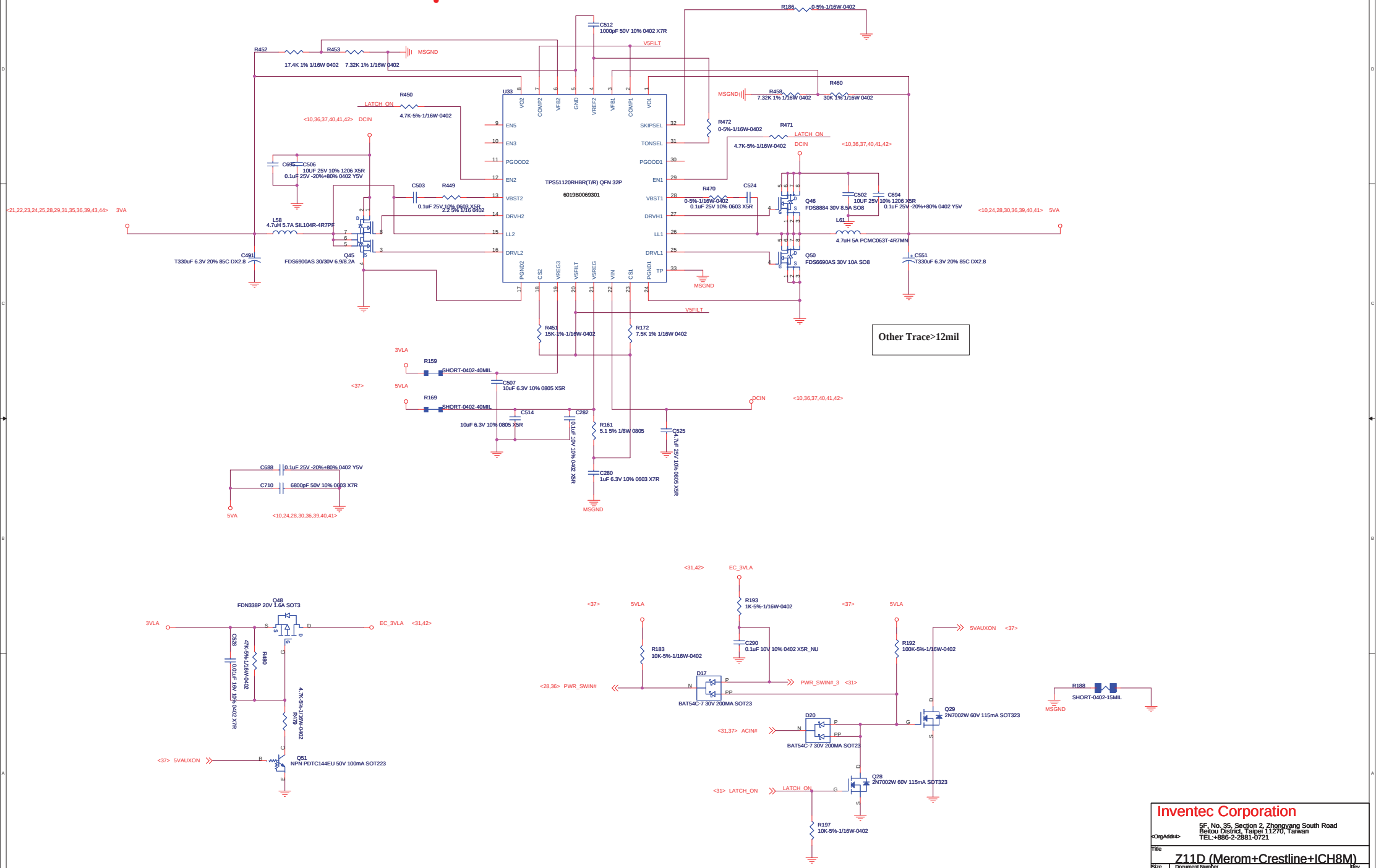

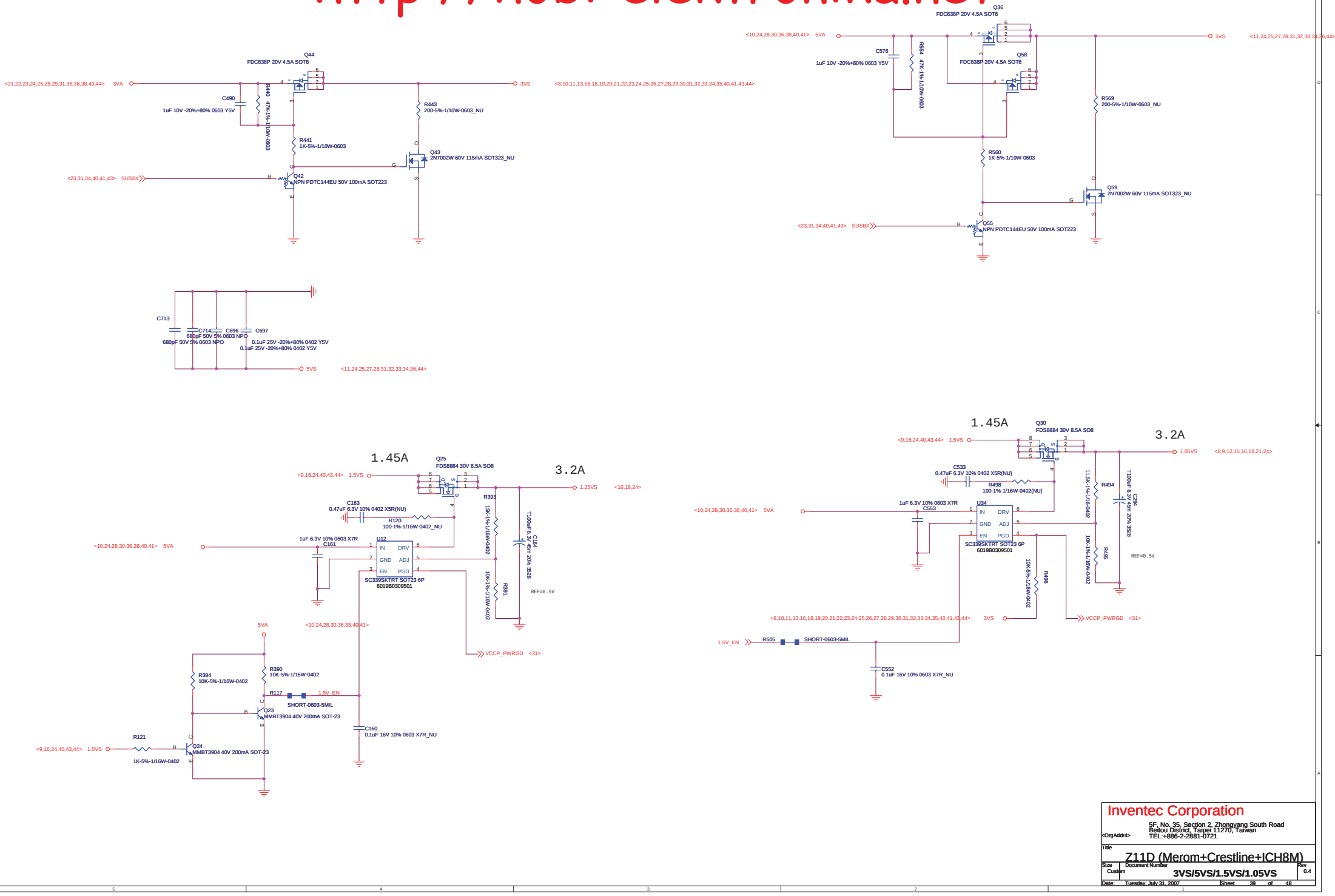

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Size: Custom | Document Number: 3VS/5VS/1.5VS/1.05VS | Rev: 0.4

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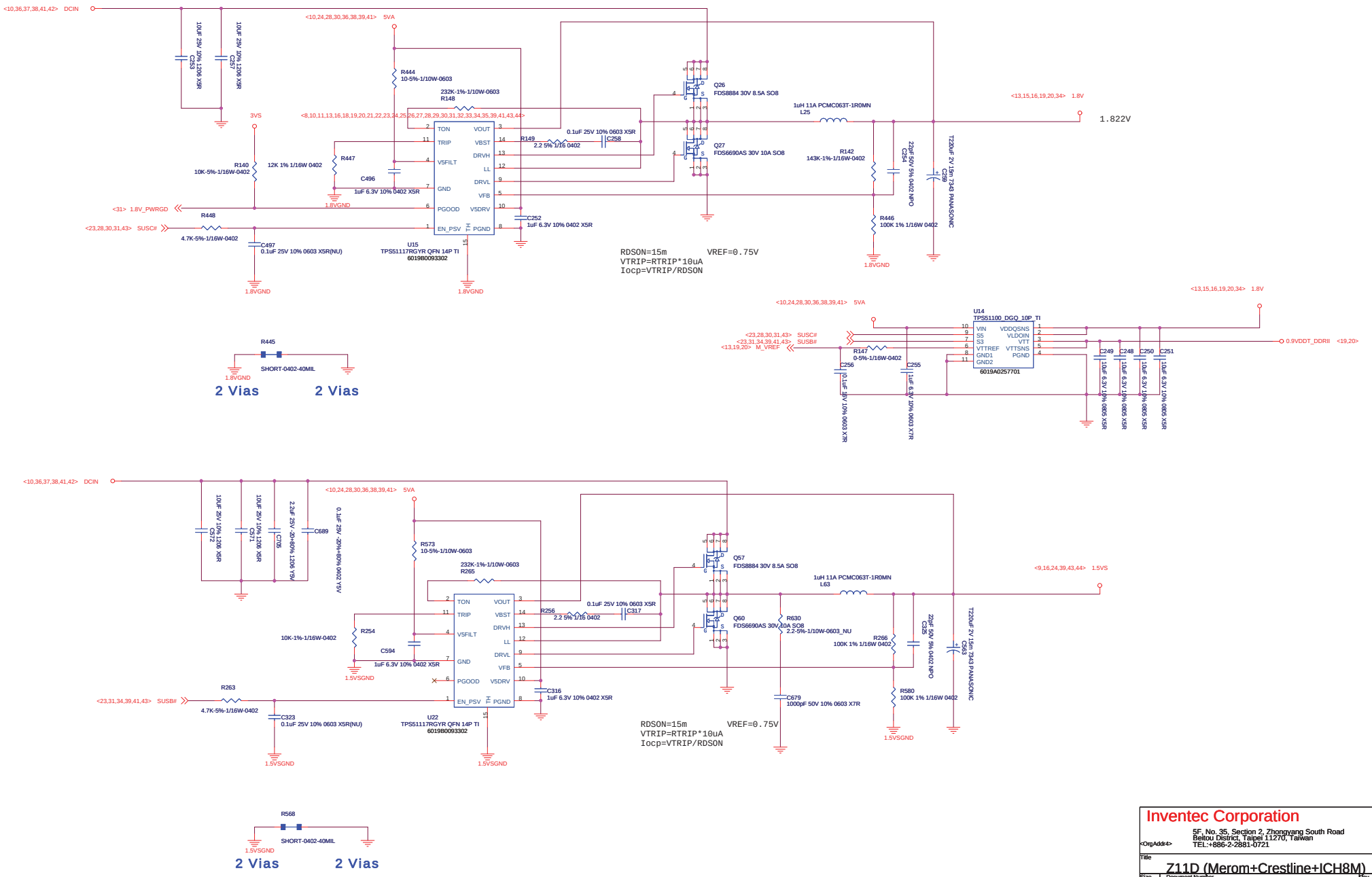

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Beitou District, Taipei 11270, Taiwan
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Size: Custom | Document Number: 1.25VS/1.8V | Rev: 0.4

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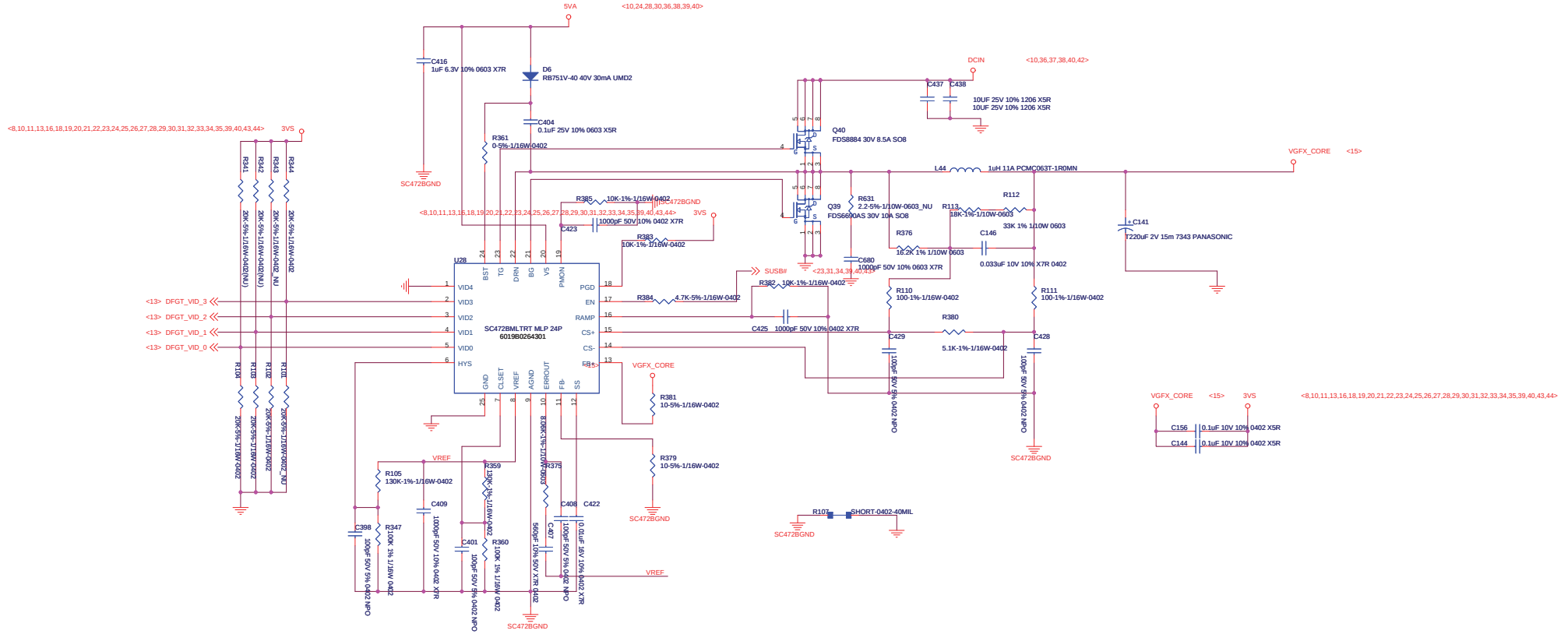

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Title	Z11D (Merom+Crestline+ICH8M)	
Size: Custom	Document Number: GPU_Core	Rev: 0.4
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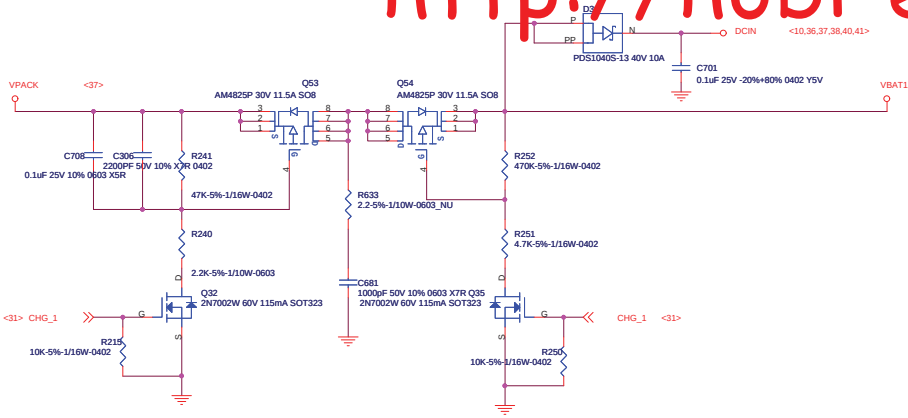

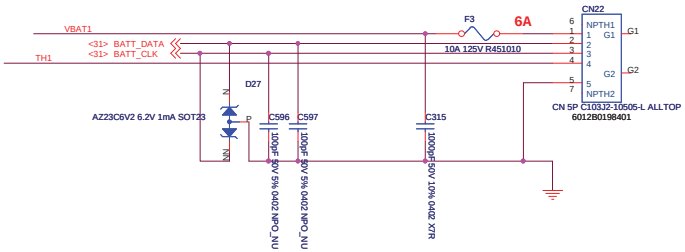

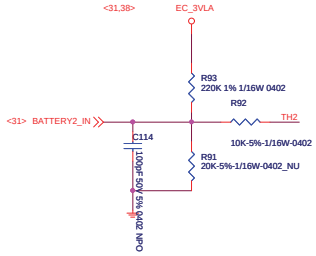

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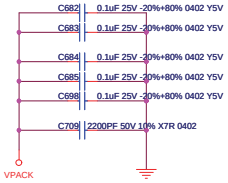

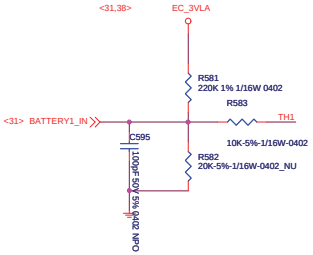

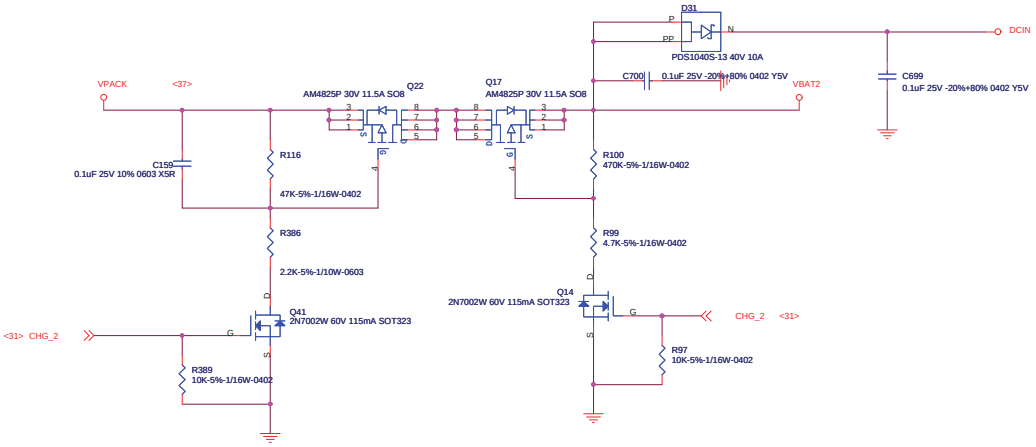

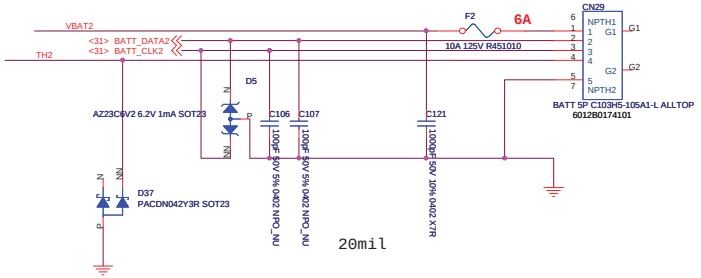

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<OrgAddr4>
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Beitou District, Taipei 11270, Taiwan
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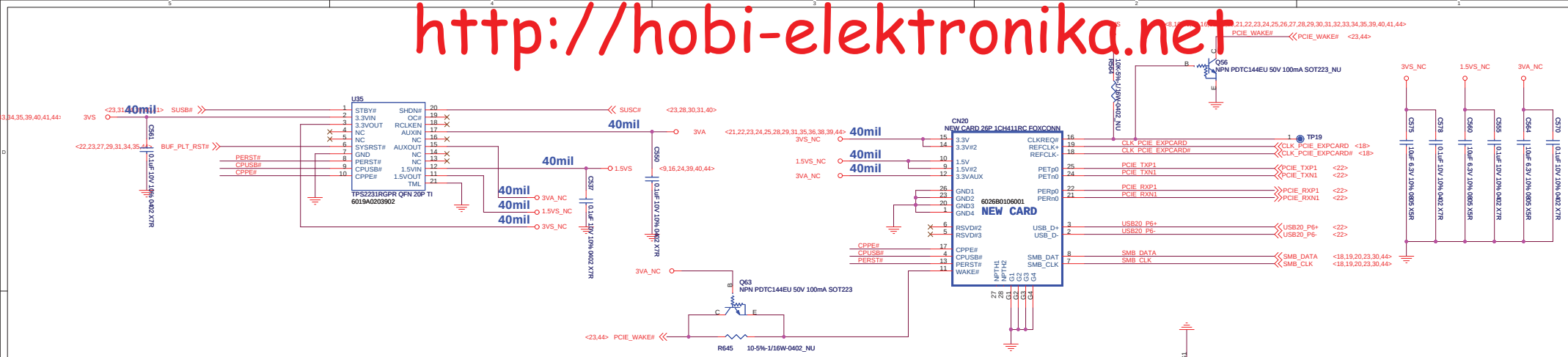

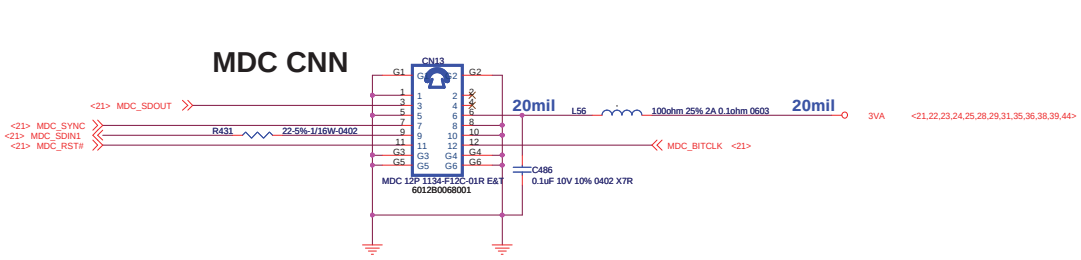

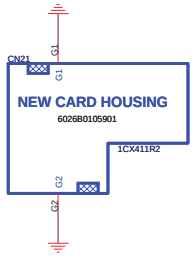

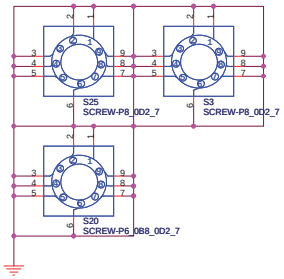

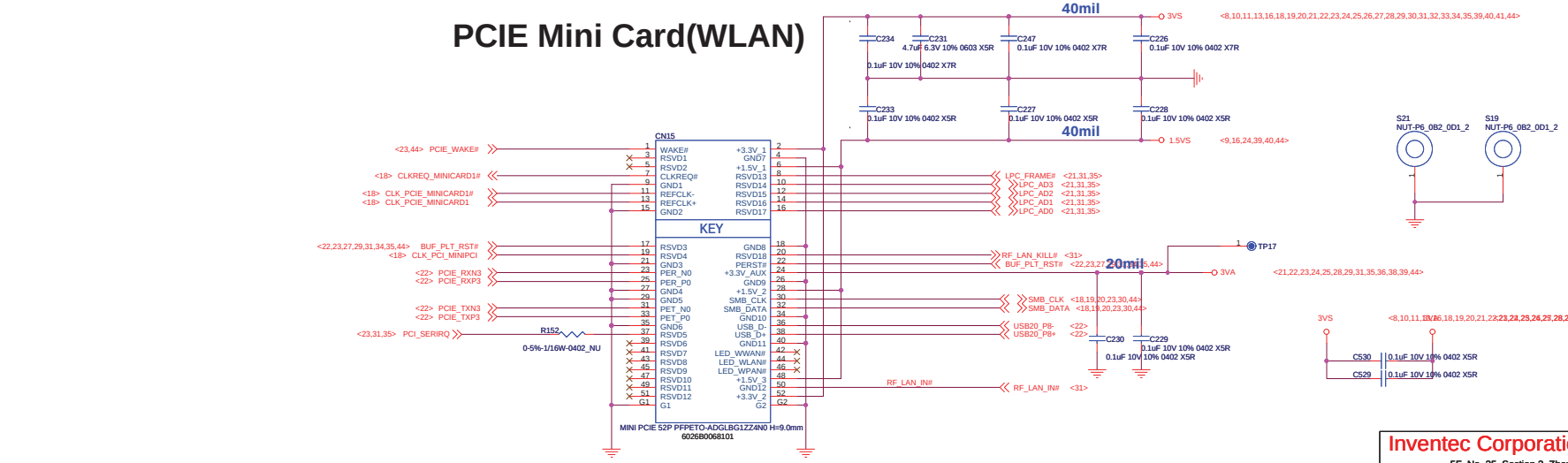

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PCIE Mini Card for 3G

R1 is optional for xD Certification

Optional , if you use GL827 masked type and don't need customized VID/PID functions and use GL827 internal setting instead, you can remove the EEPROM.

inquired for SM/xD Interface

93C46_SK: SD clock selection

R16 R17: 00 24M Hz
01 20M Hz
10 15M Hz

93C46_DO: Source clock selection for Note Book embedded clock input

R18 R19: 00 12M Hz
01 12M Hz
10 48M Hz

On Chip 5V to 3.3V regulator. No external regulator required
On-Chip power MOSFETs for supplying flash media card power.

93C46_DO: Source clock selection for Note Book embedded clock input

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Size: Custom	Document Number: 3G/Cardreader
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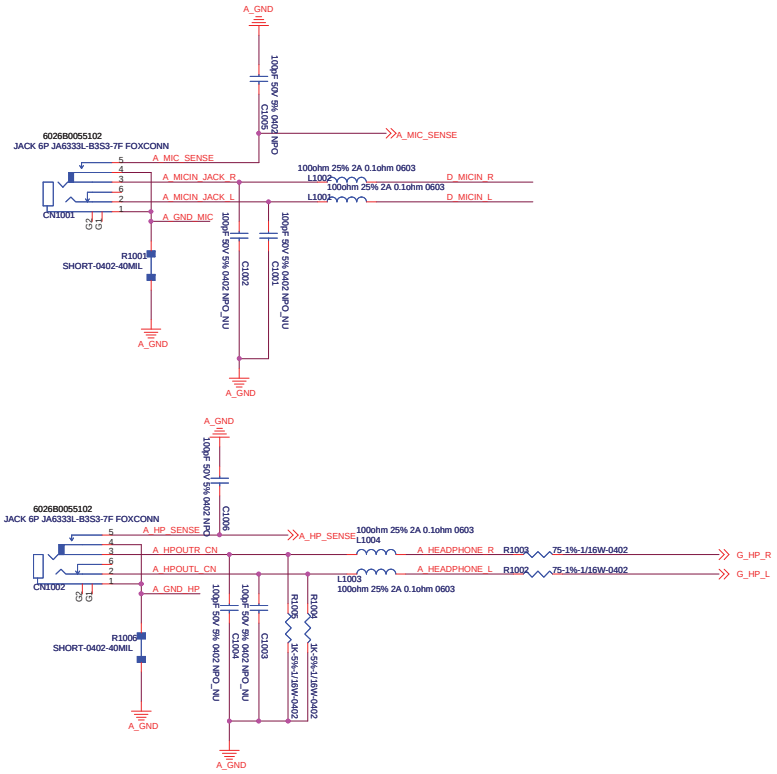
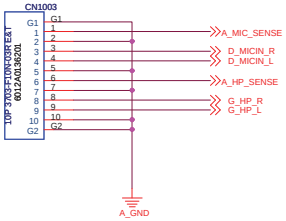
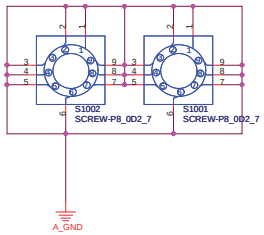
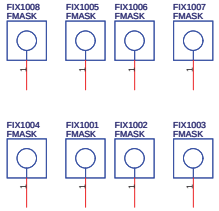
AUDIO BOARD









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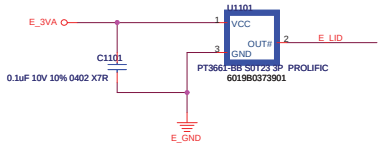
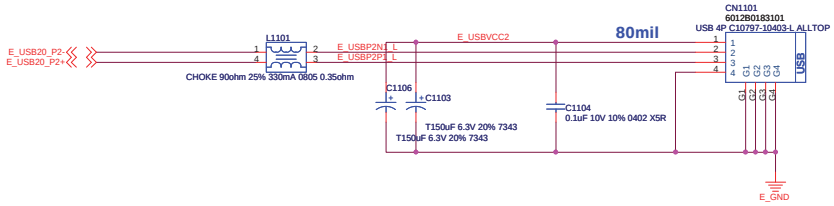
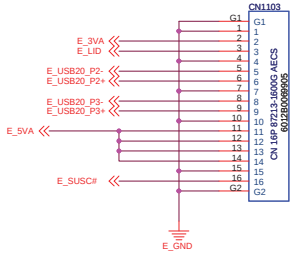
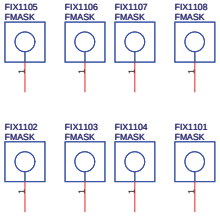
USB BOARD

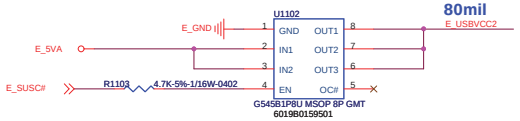
LID Switch

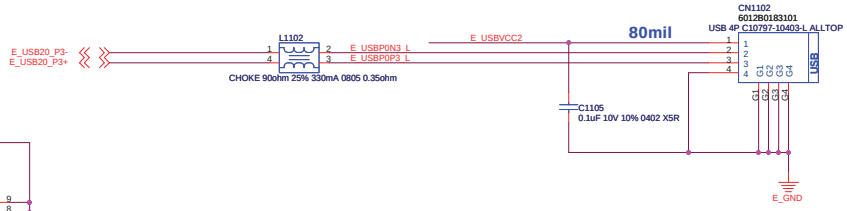


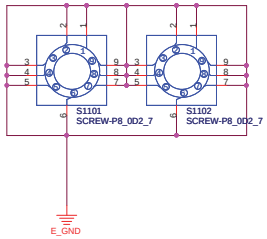












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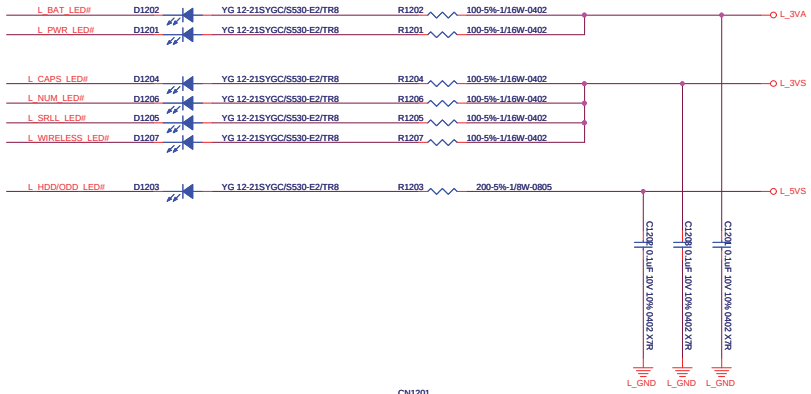
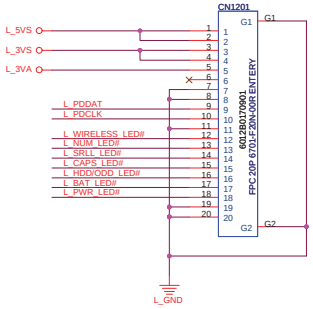
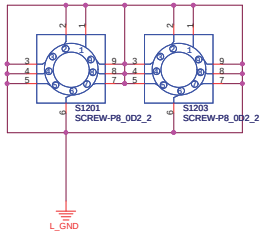
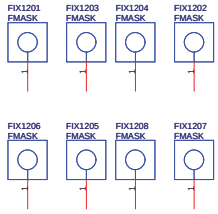
LED

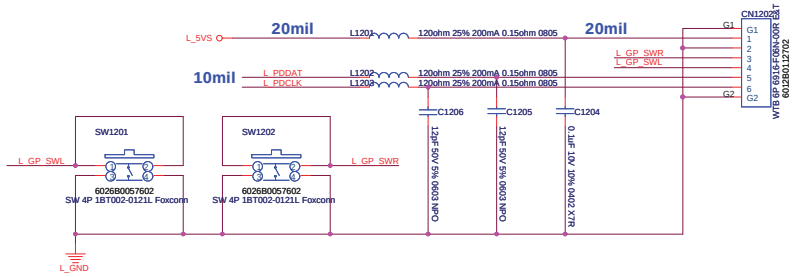








GP CNN



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Size: Custom	Document Number: Glide Board	Rev: 0.4
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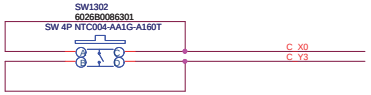
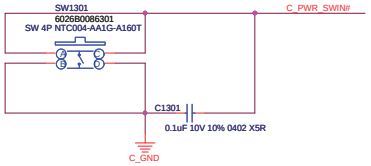
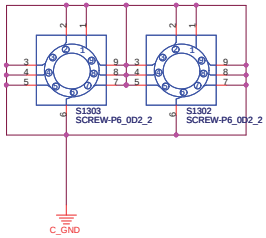
SW BOARD

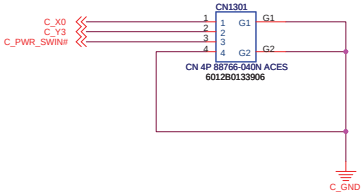
WIRELESS LAN BUTTOM

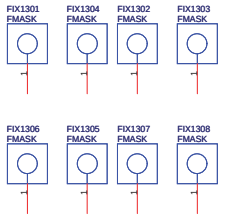


POWER SWITCH









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