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# FIRENZE II

CPU : Intel Yonah (533/667MHz)

Chip Set : RC410MD & SB450

Remarks : Mobility Platform

Model Name : FIRENZE II

PBA Name : MAIN

PCB Code : GCE : BA41-00659A  
TPT : BA41-00671A

Dev. Step : PRR

Revision : X03

T.R. Date : 2006.03.30

| DRAW  | CHECK  | APPROVAL |
|-------|--------|----------|
| TERMI | HJ KIM | SJ PARK  |
|       |        |          |

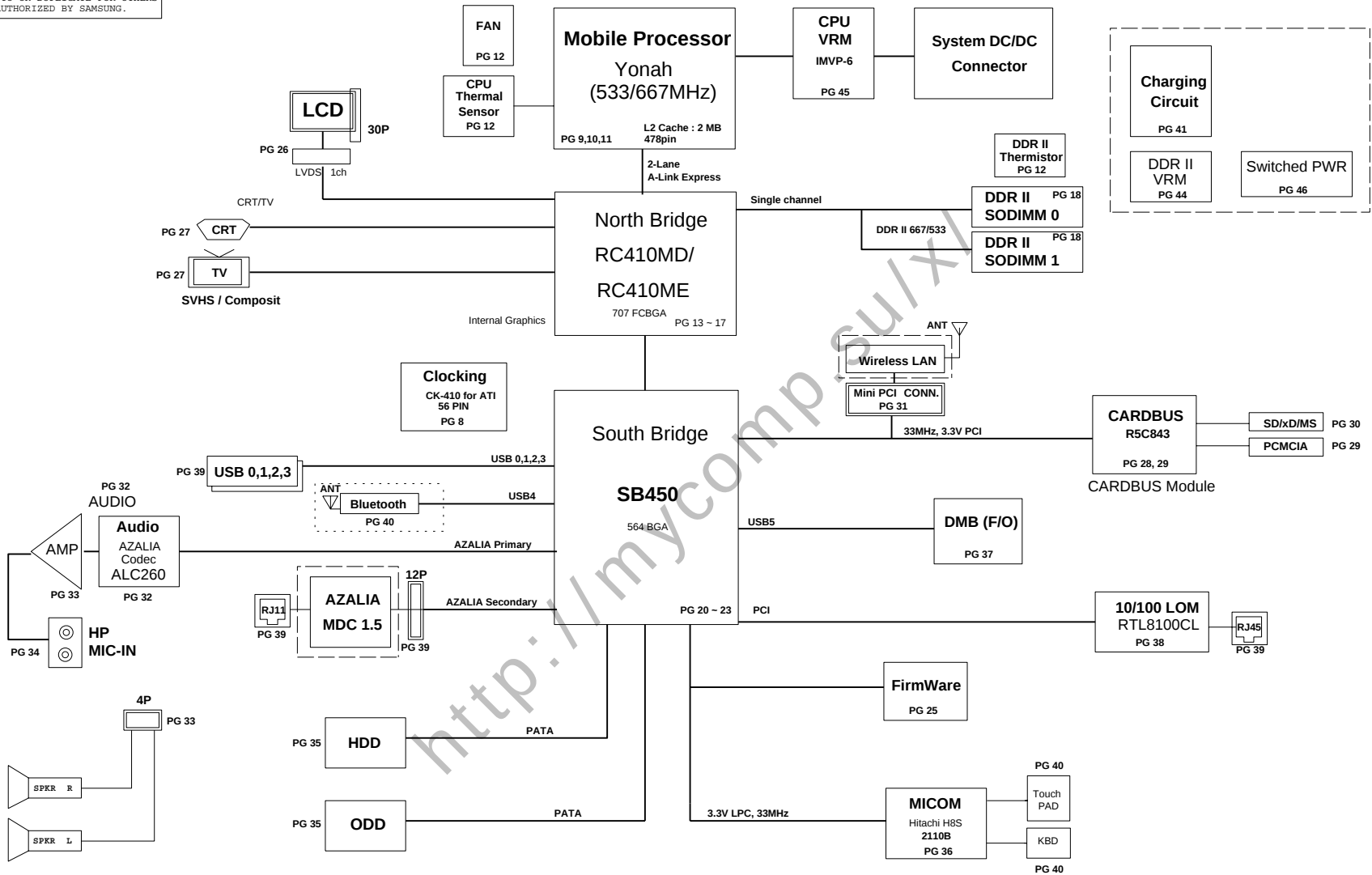
Owner : SEC Mobile R & D Signature : X

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|             |            |           |          |                          |            |                                                   |
|-------------|------------|-----------|----------|--------------------------|------------|---------------------------------------------------|
| DRAW        | TERMI KWON | DATE      | 4/5/2006 | TITLE                    | FIRENZE II | SAMSUNG<br>ELECTRONICS<br>PART NO.<br>BA41-00659A |
| CHECK       | HJ KIM     | DEV. STEP | SR       |                          | COVER      |                                                   |
| APPROVAL    | SJ PARK    | REV       | 1.0      |                          |            |                                                   |
| MODULE CODE |            | LAST EDIT |          |                          |            |                                                   |
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| DRAW                     | TERMI KWON | DATE      | 4/5/2006 | TITLE                   | FIRENZE II<br>MAIN | SAMSUNG<br>ELECTRONICS<br>PART NO. BA41-00659A |
| CHECK                    | HJ KIM     | DEV. STEP | SR       | OPERATION BLOCK DIAGRAM |                    |                                                |
| APPROVAL                 | SJ PARK    | REV       | 1.0      |                         |                    |                                                |
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# Power Diagram

KBC3\_LANPWRON KBC3\_SUSPWR KBC3\_PWRON KBC3\_VRON VCCP3\_PWRGD

AC Adapter

Battery DC

VDC

P5.0V\_ALW

MICOM\_P3.3V

P1.8V\_ALW

P1.8V\_AUX

P5.0V\_AUX

P3.3V\_AUX

P2.5V\_LAN

MEM1\_REF

P1.8V

P1.5V

P0.9V

P5.0V

P3.3V

P1.2V

P1.05V  
(VCCP)  
YONAH  
NB  
SB

VCC\_CORE

YONAH

VCC\_NB  
P1.2V NB

| Rail<br>State | +V*Always | +V*AUX | +V  | SUSPWR | PWRON | VRON |
|---------------|-----------|--------|-----|--------|-------|------|
| Full On       | ON        | ON     | ON  | H      | H     | H    |
| S3            | ON        | ON     | OFF | H      | L     | L    |
| S4            | ON        | ON     | OFF | H      | L     | L    |
| S5            | ON        | OFF    | OFF | L      | L     | L    |

S5 / S4

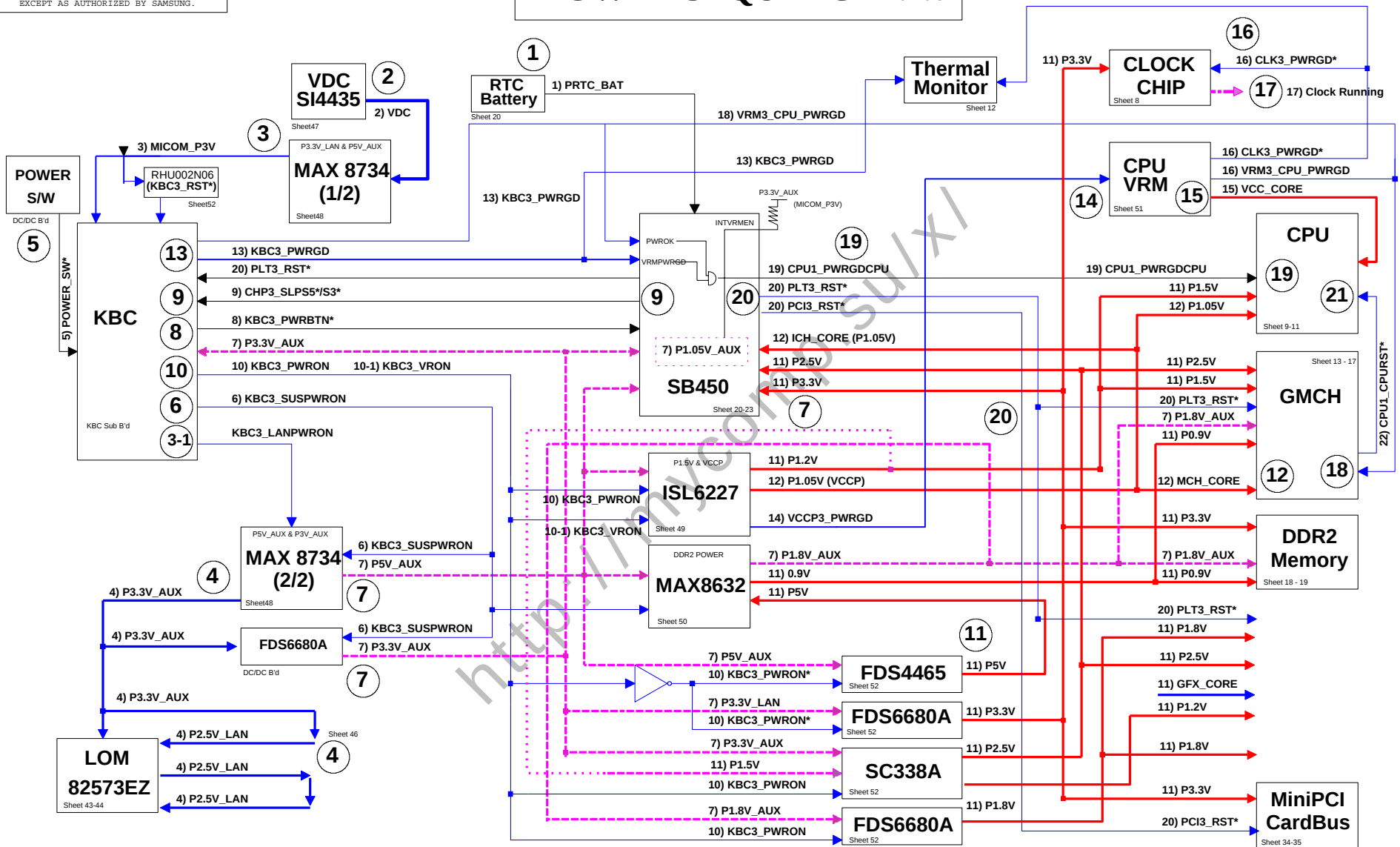
S3

S0

|                          |            |           |          |       |               |                                                |
|--------------------------|------------|-----------|----------|-------|---------------|------------------------------------------------|
| DRAW                     | TERMI KWON | DATE      | 4/5/2006 | TITLE | FIRENZE II    | SAMSUNG<br>ELECTRONICS<br>PART NO. BA41-00659A |
| CHECK                    | HJ KIM     | DEV. STEP | SR       | MAIN  | POWER DIAGRAM |                                                |
| APPROVAL                 | SJ PARK    | REV       | 1.0      |       |               |                                                |
| MODULE CODE              |            | LAST EDIT |          |       |               |                                                |
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# POWER SEQUENCE Rev. 0.8

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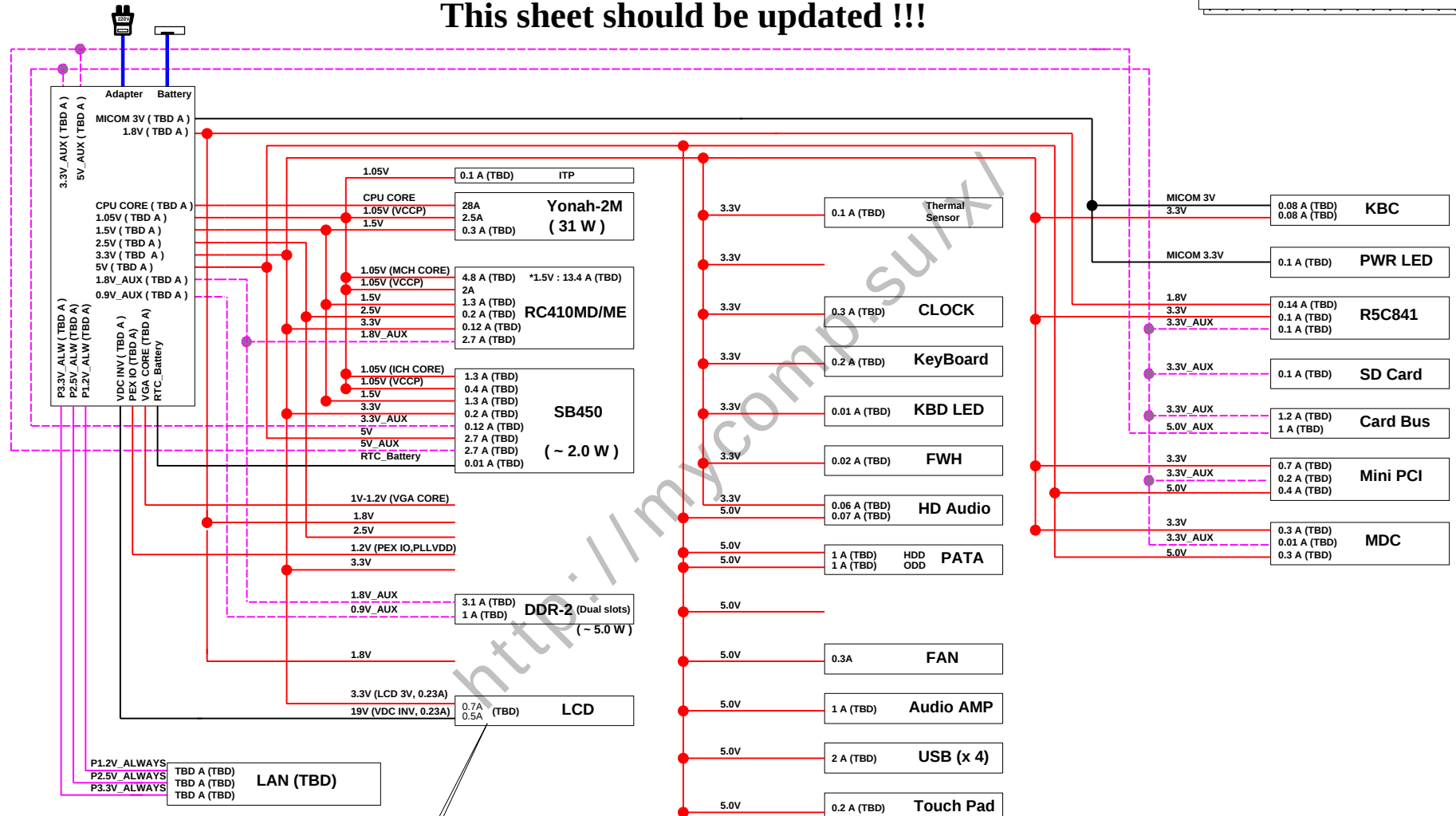
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|-------------|------------|-----------|----------|--------------------------|------------|-------------|
| DRAW        | TERMI KWON | DATE      | 4/5/2006 | TITLE                    | FIRENZE II | SAMSUNG     |
| CHECK       | HJ KIM     | DEV. STEP | SR       |                          |            | ELECTRONICS |
| APPROVAL    | SJ PARK    | REV       | 1.0      | POWER SEQUENCE           | PART NO.   | BA41-00659A |
| MODULE CODE |            | LAST EDIT |          | April 5, 2006 8:18:08 PM | PAGE       | 4 OF 52     |

# POWER RAILS ANALYSIS

Rev. 0.8

—— S0 - S5  
..... S0 - S3  
—— OFF IN S3 - S5

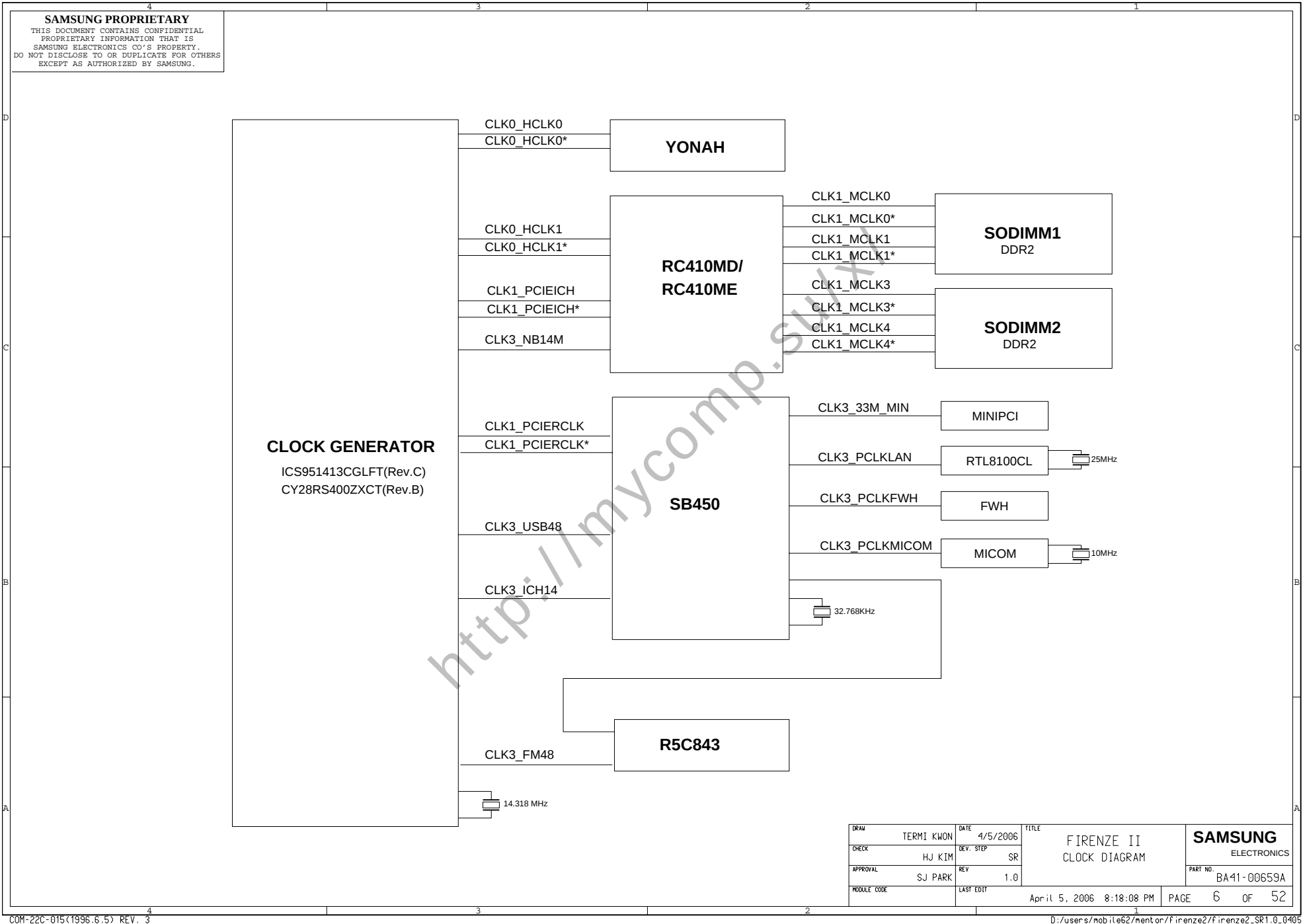
This sheet should be updated !!!



Value by Datasheet/Application notes (Value by measurement)

|             |            |           |          |       |                           |                         |
|-------------|------------|-----------|----------|-------|---------------------------|-------------------------|
| DRAW        | TERMI KWON | DATE      | 4/5/2006 | TITLE | FIRENZE II<br>POWER BLOCK | SAMSUNG<br>ELECTRONICS  |
| CHECK       | HJ KIM     | DEV. STEP | SR       |       |                           | PART NO.<br>BA41-00659A |
| APPROVAL    | SJ PARK    | REV       | 1.0      |       |                           |                         |
| MODULE CODE |            | LAST EDIT |          |       |                           |                         |

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SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

| Devices                   | IDSEL#         | REQ/GNT# | Interrupts |
|---------------------------|----------------|----------|------------|
| Cardbus                   | AD25           | 0        | E,F,G      |
| LAN                       | AD21           | 1        | C          |
| MINIPCI                   | AD23           | 2        | A,B        |
| USB                       | AD30(internal) | -        | -          |
| Hub to PCI                | AD31(internal) | -        | -          |
| LPC bridge/IDE/AC97/SMBUS | AD31(internal) | -        | --         |
| Internal MAC              | AD31(internal) | -        | -          |
| AC Link                   | -              | -        | -          |

Voltage Rails

|            |                                                                                   |
|------------|-----------------------------------------------------------------------------------|
| VDC        | Primary DC system power supply (7 to 21V)                                         |
| VCC_CORE   | Core voltage for DOTHAN (1.308~1.068V)                                            |
| VTT        | DOTHAN/ALVISO Processor System Bus(PSB) Termination (1.05V)<br>MCH-M Core Voltage |
| P0.9V      | 0.9V switched power rail (off in S3-S5)                                           |
| P1.2V      | 1.2V switched power rail (off in S3-S5)                                           |
| P1.5V      | 1.5V switched power rail (off in S3-S5)                                           |
| P1.5V_AUX  | 1.5V power rail (off in S4-S5)                                                    |
| P1.8V      | 1.8V switched power rail (off in S3-S5)                                           |
| P1.8V_AUX  | 1.8V power rail(off in S4-S5)                                                     |
| P2.5V      | 2.5V switched power rail (off in S3-S5)                                           |
| MICOM_P3V  | 3.3V always on power rail for MICOM                                               |
| P3.3V      | 3.3V switched power rail (off in S3-S5)                                           |
| P3.3V_AUX  | 3.3V power rail (off in S4-S5)                                                    |
| P3.3V_DTV  | 3.3V power rail (off in S4-S5)                                                    |
| P5V        | 5.0V switched power rail (off in S3-S5)                                           |
| P5V_AUX    | 5.0V power rail (off in S4-S5)                                                    |
| P3.3V_ALWS | 3.3V power rail (Always On)                                                       |
| P2.5V_ALWS | 2.5V power rail (Always On)                                                       |
| P1.2V_ALWS | 1.2V power rail (Always On)                                                       |

I C / SMB Address

| Devices                  | Address   | Hex | Bus                                |
|--------------------------|-----------|-----|------------------------------------|
| SB450                    | Master    | -   | SMBUS Master                       |
| SODIMM0                  | 1010 0000 | A0h | -                                  |
| SODIMM1                  | 1010 001X | A2h | -                                  |
| CK-410 (Clock Generator) | 1101 001X | D2h | Clock, Unused Clock Output Disable |

USB PORT Assign

| PORT NUMBER | ASSIGNED TO   |
|-------------|---------------|
| 0, 1        | SYSTEM PORT A |
| 2, 3        | SYSTEM PORT B |
| 4           | BLUETOOTH     |
| 5           | DMB           |

System Power States

CHP3\_SLPS1\* S1, Powered-On-Suspend(POS) : In this state, all clocks(except the 32.768KHz clock) are stopped.  
The system context is maintained in system DRAM. Power is maintained to PCI, the CPU, memory controller, memory, and all other critical subsystems.  
Note that this state does not preclude power being removed from non-essential devices, such as disk drives. During this state, CPU can be selected for either Deep Sleep or Deeper Sleep.  
In Deeper Sleep, CPU voltage reduced in this state to reduce the leakage power.  
CHP3\_SLPS3\* S3, Suspend-To-RAM(STR) : The system context is maintained in system DRAM, but power is shut off to non-critical circuits.  
Memory is retained, and refreshes continue. All clocks stop except RTC clock.  
CHP3\_SLPS4\* S4, Suspend-To-Disk(STD) : The Context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume.  
Externally appears same as S5, but may have different wake events.  
CHP3\_SLPS5\* S5, Soft Off(SOFF) : System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.

Crystal / Oscillator

| TYPE    | FREQUENCY | DEVICE          | USAGE           |
|---------|-----------|-----------------|-----------------|
| Crystal | 32.768KHz | SB450           | Real Time Clock |
| Crystal | 10MHz     | MICOM           | HGS-2110B       |
| Crystal | 14.318MHz | CLOCK-Generator | CK-410M         |
| Crystal | 25MHz     | LAN             | LOM             |

CPU Core Voltage Table

| VID(5:0)    | Voltage | VID(5:0)    | Voltage |
|-------------|---------|-------------|---------|
| 0 0 0 0 0 0 | 1.708 V | 1 0 0 0 0 0 | 1.196 V |
| 0 0 0 0 0 1 | 1.692 V | 1 0 0 0 0 1 | 1.180 V |
| 0 0 0 0 1 0 | 1.676 V | 1 0 0 0 1 0 | 1.164 V |
| 0 0 0 0 1 1 | 1.660 V | 1 0 0 0 1 1 | 1.148 V |
| 0 0 0 1 0 0 | 1.644 V | 1 0 0 1 0 0 | 1.132 V |
| 0 0 0 1 0 1 | 1.628 V | 1 0 0 1 0 1 | 1.116 V |
| 0 0 0 1 1 0 | 1.612 V | 1 0 0 1 1 0 | 1.100 V |
| 0 0 0 1 1 1 | 1.596 V | 1 0 0 1 1 1 | 1.084 V |
| 0 0 1 0 0 0 | 1.580 V | 1 0 1 0 0 0 | 1.068 V |
| 0 0 1 0 0 1 | 1.564 V | 1 0 1 0 0 1 | 1.052 V |
| 0 0 1 0 1 0 | 1.548 V | 1 0 1 0 1 0 | 1.036 V |
| 0 0 1 0 1 1 | 1.532 V | 1 0 1 0 1 1 | 1.020 V |
| 0 0 1 1 0 0 | 1.516 V | 1 0 1 1 0 0 | 1.004 V |
| 0 0 1 1 0 1 | 1.500 V | 1 0 1 1 0 1 | 0.988 V |
| 0 0 1 1 1 0 | 1.484 V | 1 0 1 1 1 0 | 0.972 V |
| 0 0 1 1 1 1 | 1.468 V | 1 0 1 1 1 1 | 0.956 V |
| 0 1 0 0 0 0 | 1.452 V | 1 1 0 0 0 0 | 0.940 V |
| 0 1 0 0 0 1 | 1.436 V | 1 1 0 0 0 1 | 0.924 V |
| 0 1 0 0 1 0 | 1.420 V | 1 1 0 0 1 0 | 0.908 V |
| 0 1 0 0 1 1 | 1.404 V | 1 1 0 0 1 1 | 0.892 V |
| 0 1 0 1 0 0 | 1.388 V | 1 1 0 1 0 0 | 0.876 V |
| 0 1 0 1 0 1 | 1.372 V | 1 1 0 1 0 1 | 0.860 V |
| 0 1 0 1 1 0 | 1.356 V | 1 1 0 1 1 0 | 0.844 V |
| 0 1 0 1 1 1 | 1.340 V | 1 1 0 1 1 1 | 0.828 V |
| 0 1 1 0 0 0 | 1.324 V | 1 1 1 0 0 0 | 0.812 V |
| 0 1 1 0 0 1 | 1.308 V | 1 1 1 0 0 1 | 0.796 V |
| 0 1 1 0 1 0 | 1.292 V | 1 1 1 0 1 0 | 0.780 V |
| 0 1 1 0 1 1 | 1.276 V | 1 1 1 0 1 1 | 0.764 V |
| 0 1 1 1 0 0 | 1.260 V | 1 1 1 1 0 0 | 0.748 V |
| 0 1 1 1 0 1 | 1.244 V | 1 1 1 1 0 1 | 0.732 V |
| 0 1 1 1 1 0 | 1.228 V | 1 1 1 1 1 0 | 0.716 V |
| 0 1 1 1 1 1 | 1.212 V | 1 1 1 1 1 1 | 0.700 V |

HFM Voltage  
770:1.26V->1.372V  
730,740,750,760:1.26->1.356V

|             |            |           |          |                           |                    |                        |
|-------------|------------|-----------|----------|---------------------------|--------------------|------------------------|
| DRAW        | TERMI KWON | DATE      | 4/5/2006 | TITLE                     | FIRENZE II<br>MAIN | SAMSUNG<br>ELECTRONICS |
| CHECK       | HJ KIM     | DEV. STEP | SR       | BOARD INFORMATION         | PART NO.           | BA41-00659A            |
| APPROVAL    | SJ PARK    | REV       | 1.0      | Apr 11 5, 2006 8:18:08 PM | PAGE               | 7 OF 52                |
| MODULE CODE |            | LAST EDIT |          |                           |                    |                        |

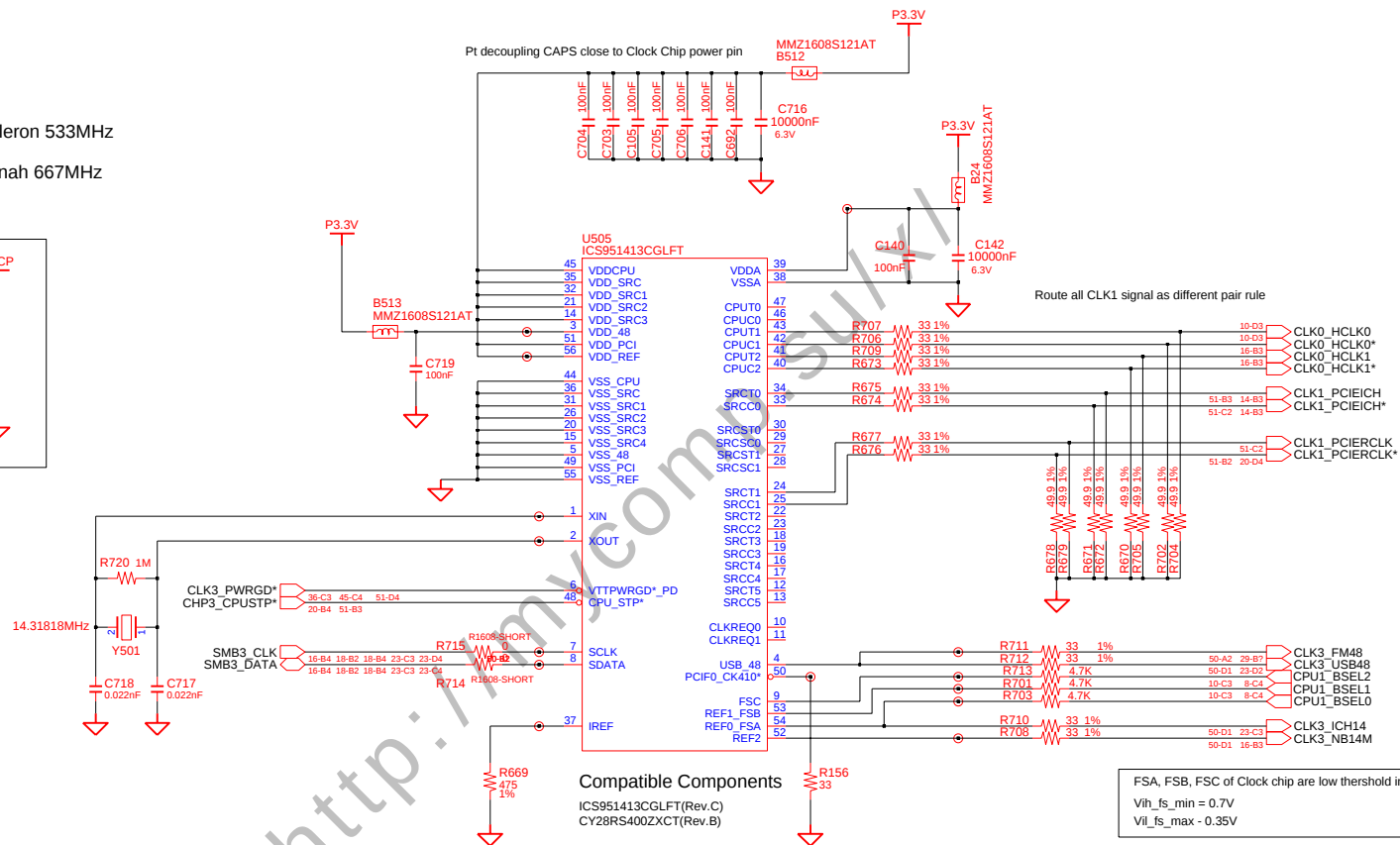
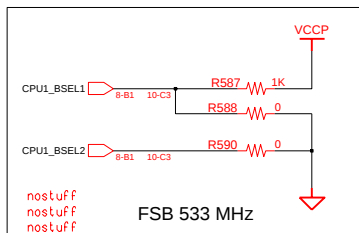
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| FSA   | FSB   | FSC   | HOST CLK |
|-------|-------|-------|----------|
| BSEL0 | BSEL1 | BSEL2 |          |
| 0     | 0     | 0     | 266 MHz  |
| 0     | 0     | 1     | 333 MHz  |
| 0     | 1     | 0     | 200 MHz  |
| 0     | 1     | 1     | 400 MHz  |
| 1     | 0     | 0     | 133 MHz  |
| 1     | 0     | 1     | 100 MHz  |
| 1     | 1     | 0     | 166 MHz  |
| 1     | 1     | 1     | RSVD     |

Celeron 533MHz

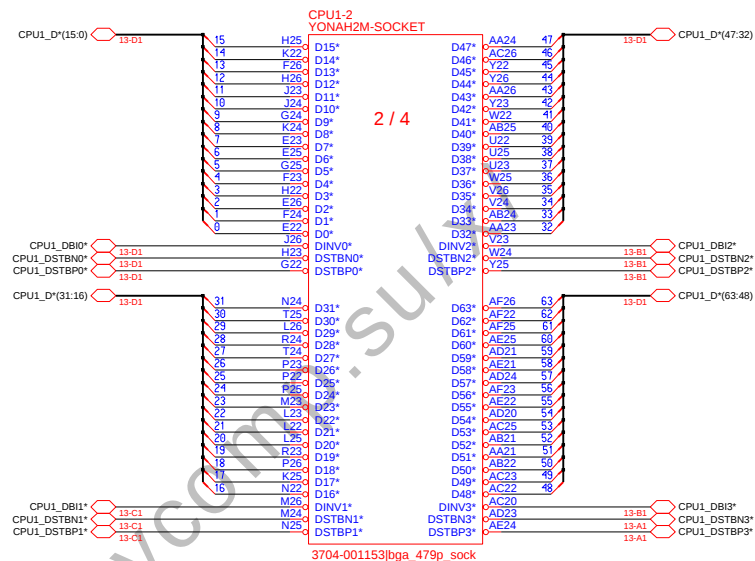
Yonah 667MHz



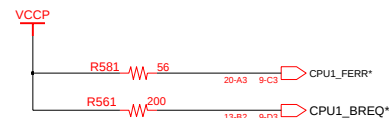
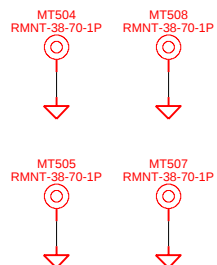
Place all te serias termination resistor as close as Clock Chip as possible

|             |            |           |          |                          |                                       |                         |
|-------------|------------|-----------|----------|--------------------------|---------------------------------------|-------------------------|
| DRAW        | TERMI KWON | DATE      | 4/5/2006 | TITLE                    | FIRENZE II<br>MAIN<br>CLOCK GENERATOR | SAMSUNG<br>ELECTRONICS  |
| CHECK       | HJ KIM     | DEV. STEP | SR       |                          |                                       | PART NO.<br>BA41-00659A |
| APPROVAL    | SJ PARK    | REV       | 1.0      |                          |                                       |                         |
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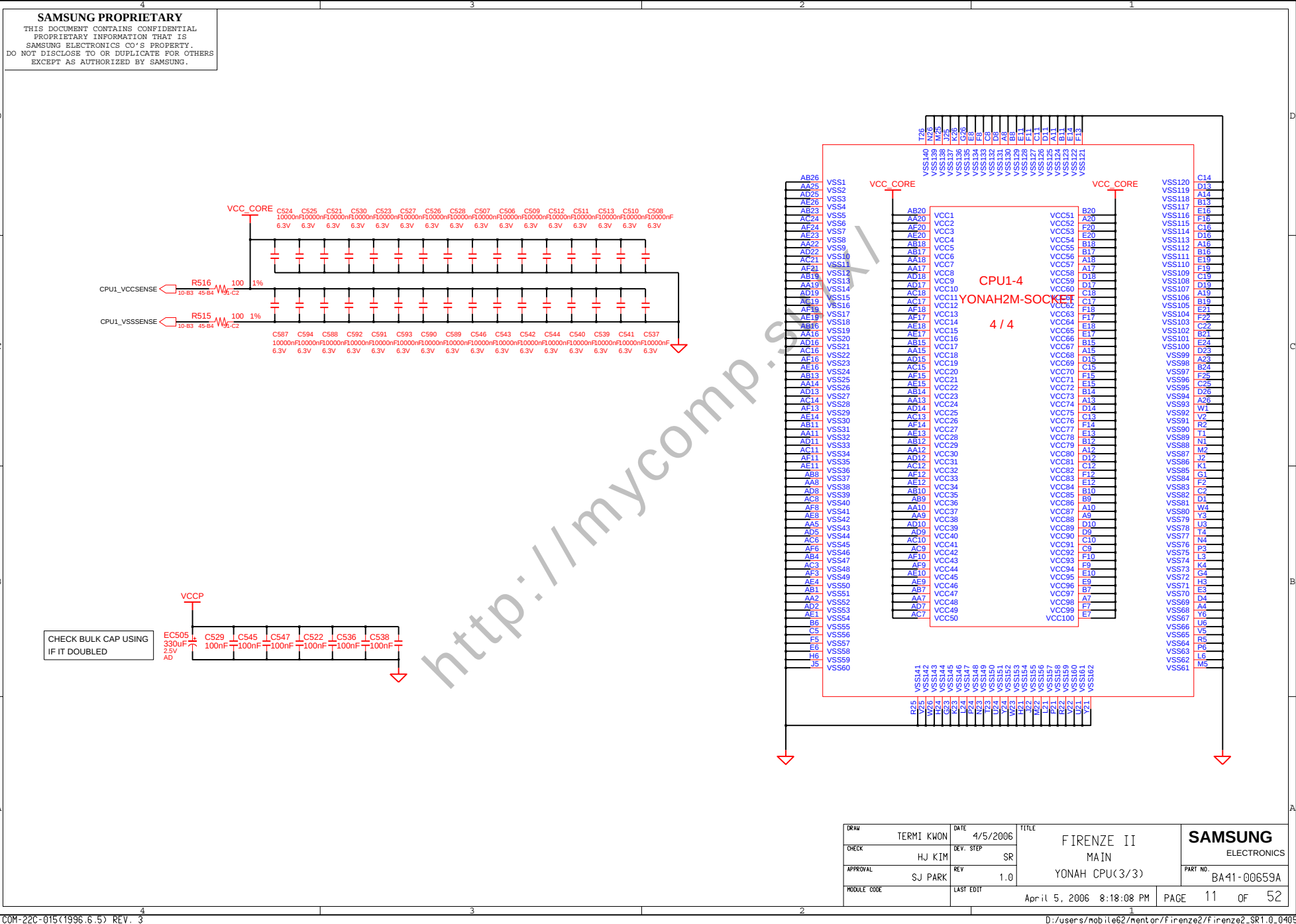
RHE SUPPORTER



|             |            |           |                          |                                                |  |                                                |  |
|-------------|------------|-----------|--------------------------|------------------------------------------------|--|------------------------------------------------|--|
| DRW         | TERMI KWON | DATE      | 4/5/2006                 | TITLE<br>FIRENZE II<br>MAIN<br>YONAH CPU (1/3) |  | SAMSUNG<br>ELECTRONICS<br>PART NO. BA41-00659A |  |
| CHECK       | HJ KIM     | DES. STEP | SR                       |                                                |  |                                                |  |
| APPROVAL    | SJ PARK    | REV       | 1.0                      |                                                |  |                                                |  |
| MODULE CODE | LAST EDIT  |           | April 5, 2006 8:18:08 PM |                                                |  |                                                |  |

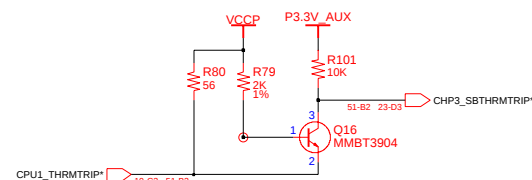
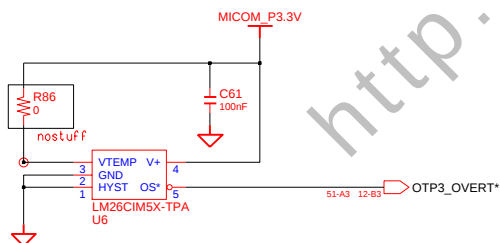
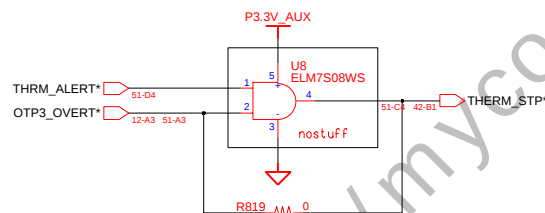


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|-------------|------------|-----------|----------|--------------------------|--------------------------------------|-------------------------|
| DRAW        | TERMI KWON | DATE      | 4/5/2006 | TITLE                    | FIRENZE II<br>MAIN<br>YONAH CPU(3/3) | SAMSUNG<br>ELECTRONICS  |
| CHECK       | HJ KIM     | DEV. STEP | SR       |                          |                                      | PART NO.<br>BA41-00659A |
| APPROVAL    | SJ PARK    | REV       | 1.0      |                          |                                      |                         |
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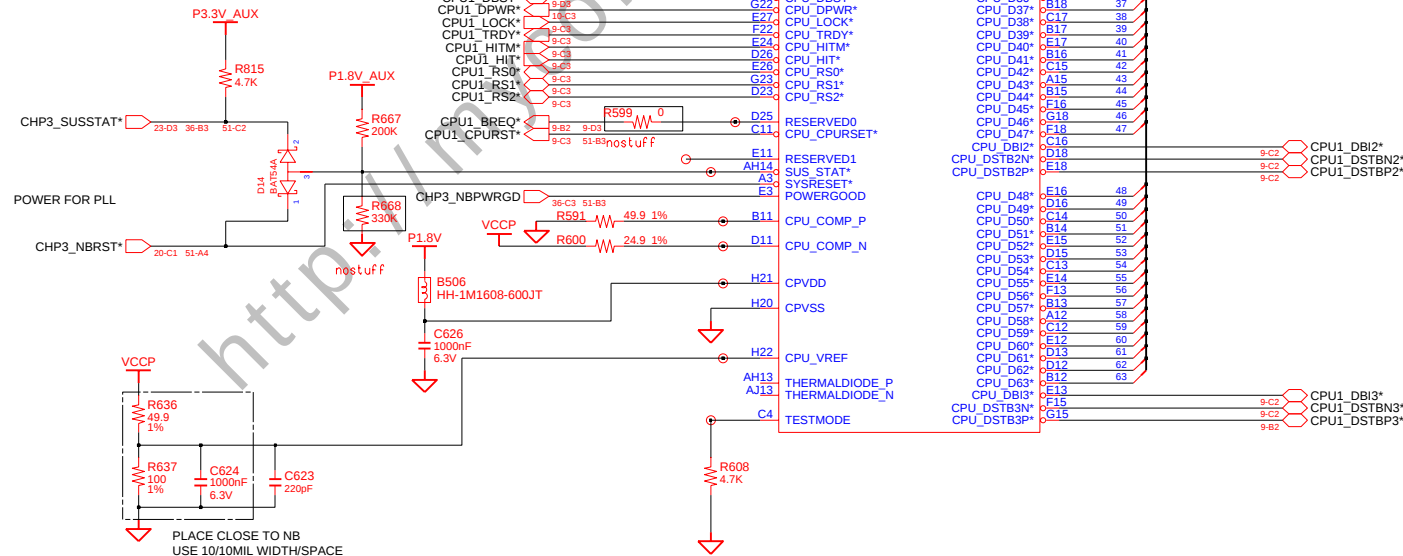
- Refer To Thermal Sensor Layout Guidelines.
- Place the Thermal Sensor close to a remote diode.
  - Keep traces away from high voltage (+12V bus)
  - Keep traces away from fast data buses and CRT signal.
  - Use recommended trace widths and spacings (10mil)
  - Place a ground plane under the traces.
  - Use guard traces flanking DXP and DXN and connecting to GND

|             |            |           |                          |                           |      |            |    |             |  |
|-------------|------------|-----------|--------------------------|---------------------------|------|------------|----|-------------|--|
| DRWN        | TERMI KWON | DATE      | 4/5/2006                 | TITLE                     |      | FIRENZE II |    | SAMSUNG     |  |
| CHECK       | HJ KIM     | DEV. STEP | SR                       |                           |      | MAIN       |    | ELECTRONICS |  |
| APPROVAL    | SJ PARK    | REV       | 1.0                      | THERMAL SENSOR/FAN CONTRL |      | PART NO.   |    | BA41-00659A |  |
| MODULE CODE | LAST EDIT  |           | April 5, 2006 8:18:08 PM |                           | PAGE | 12         | OF | 52          |  |

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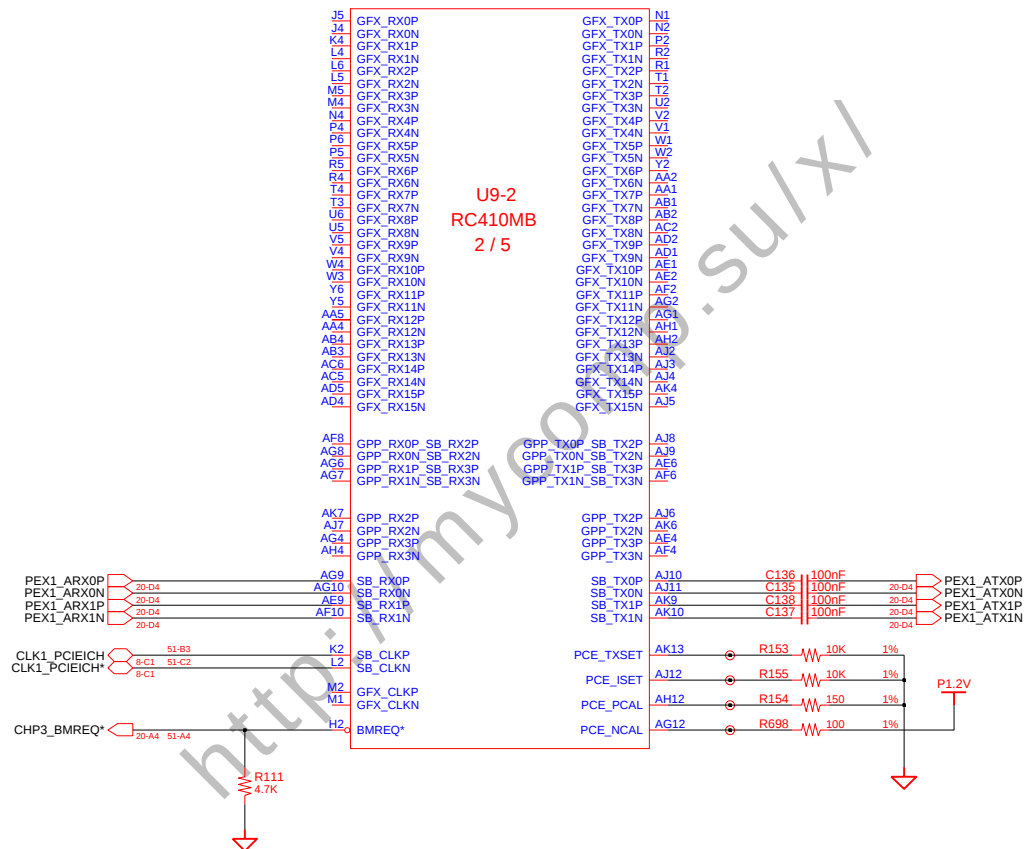
## DUCT + FAN SUPPORTER



|             |            |           |          |                         |             |                        |
|-------------|------------|-----------|----------|-------------------------|-------------|------------------------|
| DRAW        | TERMI KWON | DATE      | 4/5/2006 | TITLE                   | FIRENZE II  | SAMSUNG<br>ELECTRONICS |
| CHECK       | HJ KIM     | DEV. STEP | SR       | MAIN                    |             |                        |
| APPROVAL    | SJ PARK    | REV       | 1.0      | RC410MD(1/5)            | PART NO.    |                        |
| MODULE CODE |            | LAST EDIT |          | Apr 15, 2006 8:18:08 PM | BA41-00659A |                        |

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| DRAW        | TERMI KWON | DATE      | 4/5/2006 | TITLE                    | FIRENZE II<br>MAIN<br>RC410MD(2/5) | SAMSUNG<br>ELECTRONICS |
| CHECK       | HJ KIM     | DEV. STEP | SR       |                          |                                    | PART NO. BA41-00659A   |
| APPROVAL    | SJ PARK    | REV       | 1.0      |                          |                                    |                        |
| MODULE CODE |            | LAST EDIT |          | April 5, 2006 8:18:08 PM | PAGE 14                            | OF 52                  |

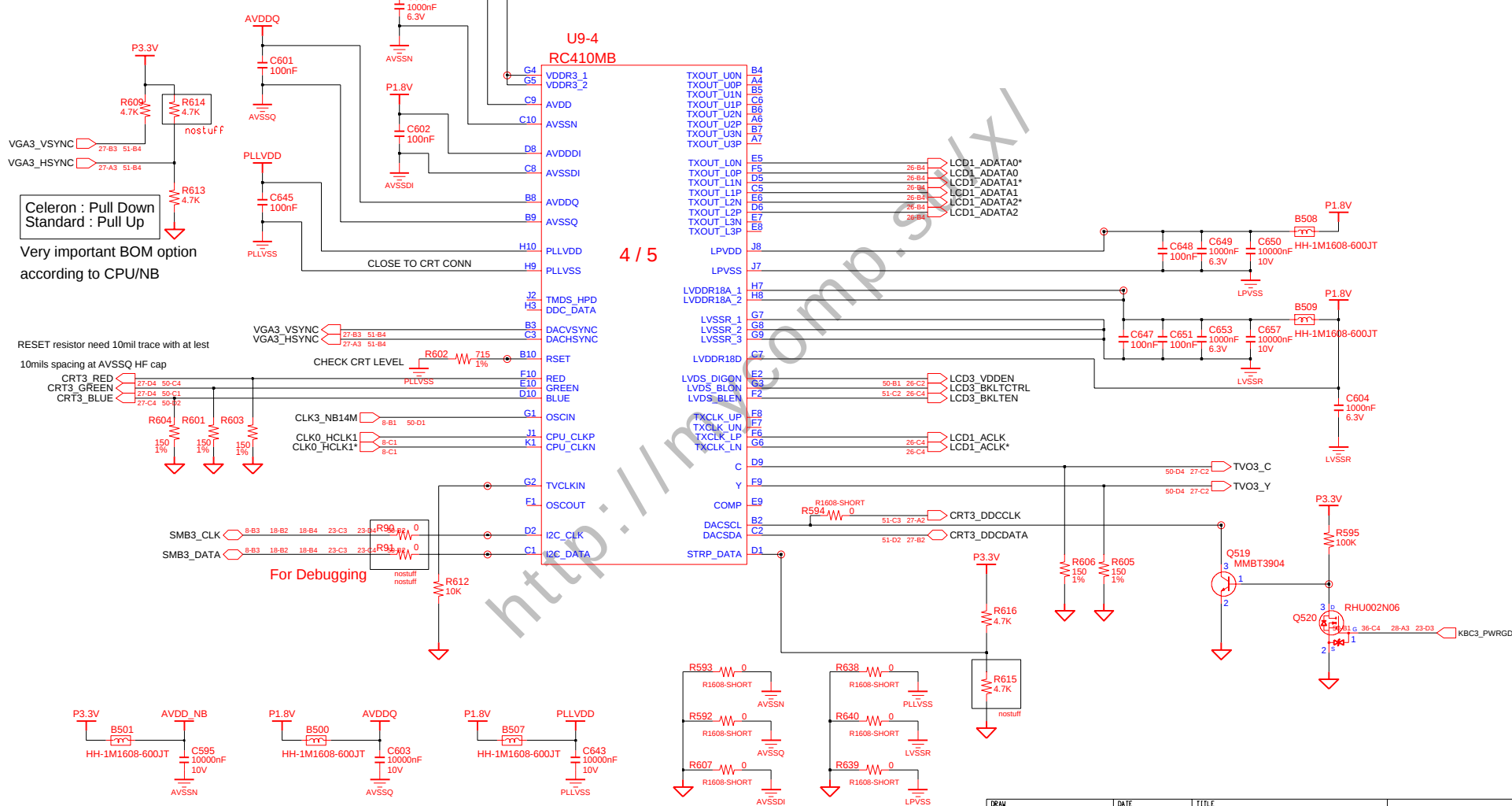
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Put the AVDD,AVDDI,AVDDQ,PLVDD  
decoupling CAPS on the bottom side close to BALLS



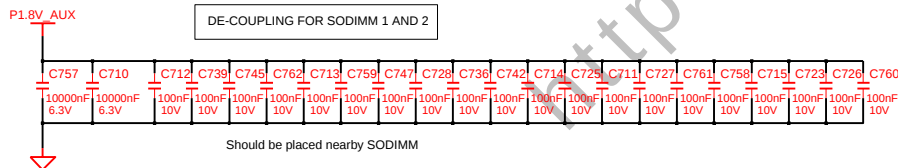
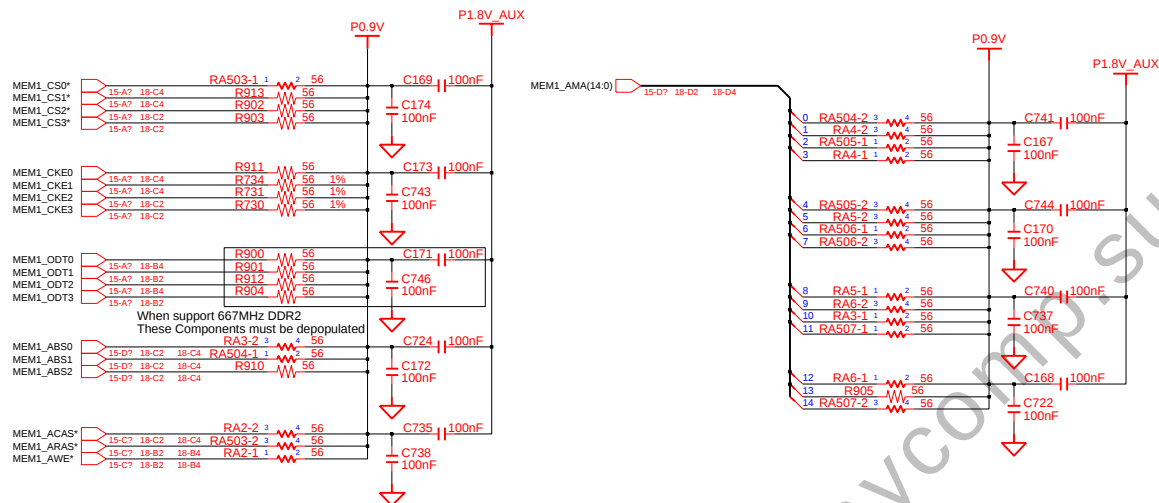
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| DATE                     | 4/5/2006  | TITLE     | FIRENZE II<br>MAIN<br>RC410MD(4/5) | <b>SAMSUNG</b><br>ELECTRONICS<br>PART NO. BA41-00659A |
| CHECK                    | HJ KTM    | DEV. STEP | SR                                 |                                                       |
| APPROVAL                 | SJ PARK   | REV       | 1.0                                |                                                       |
| MODULE CODE              | LAST EDIT |           |                                    |                                                       |
| April 5, 2006 8:18:08 PM |           |           |                                    | PAGE 16 OF 52                                         |

|  |   |   |   |   |                                                       |
|--|---|---|---|---|-------------------------------------------------------|
|  | 4 | 3 | 2 | 1 | D:/users/nobile62/mentor/firenze2/firenze2_SR1.0_0405 |
|--|---|---|---|---|-------------------------------------------------------|

D:/users/mobile62/mentor/firenze2/firenze2\_SR1.0\_0405

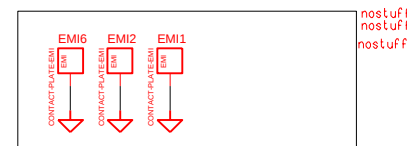
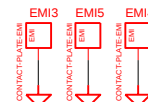
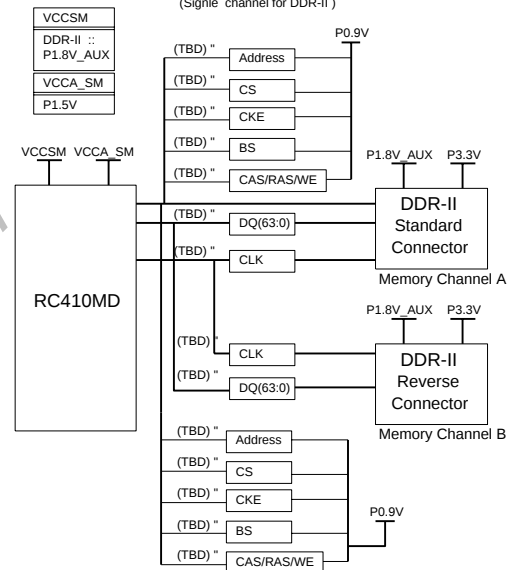
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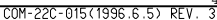
## Memory Topology

(Single channel for DDR-II)



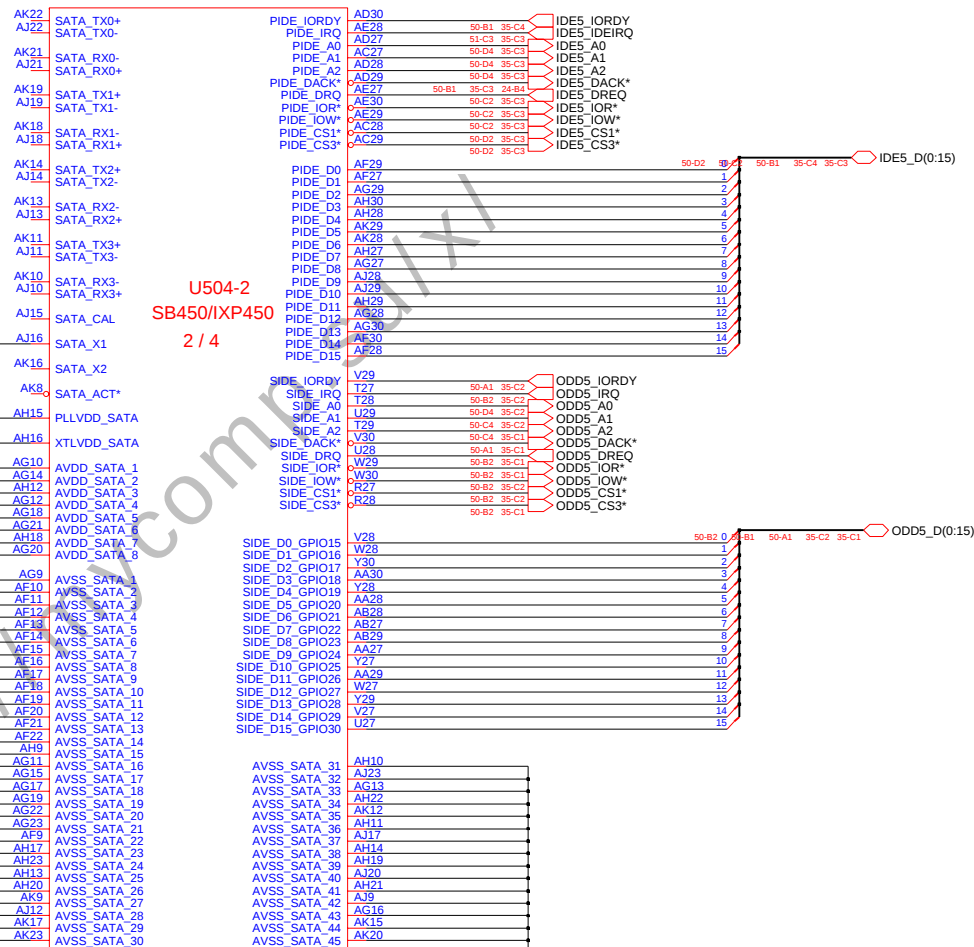
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| DRAW        | TERMI KWON | DATE      | 4/5/2006                 | TITLE              | FIRENZE II | SAMSUNG     |
| CHECK       | HJ KIM     | DEV. STEP | SR                       | MAIN               | MAIN       | ELECTRONICS |
| APPROVAL    | SJ PARK    | REV       | 1.0                      | DDR2 - TERMINATION | PART NO.   | BA41-00659A |
| MODULE CODE |            | LAST EDIT | April 5, 2006 8:18:08 PM | PAGE               | 19         | OF 52       |

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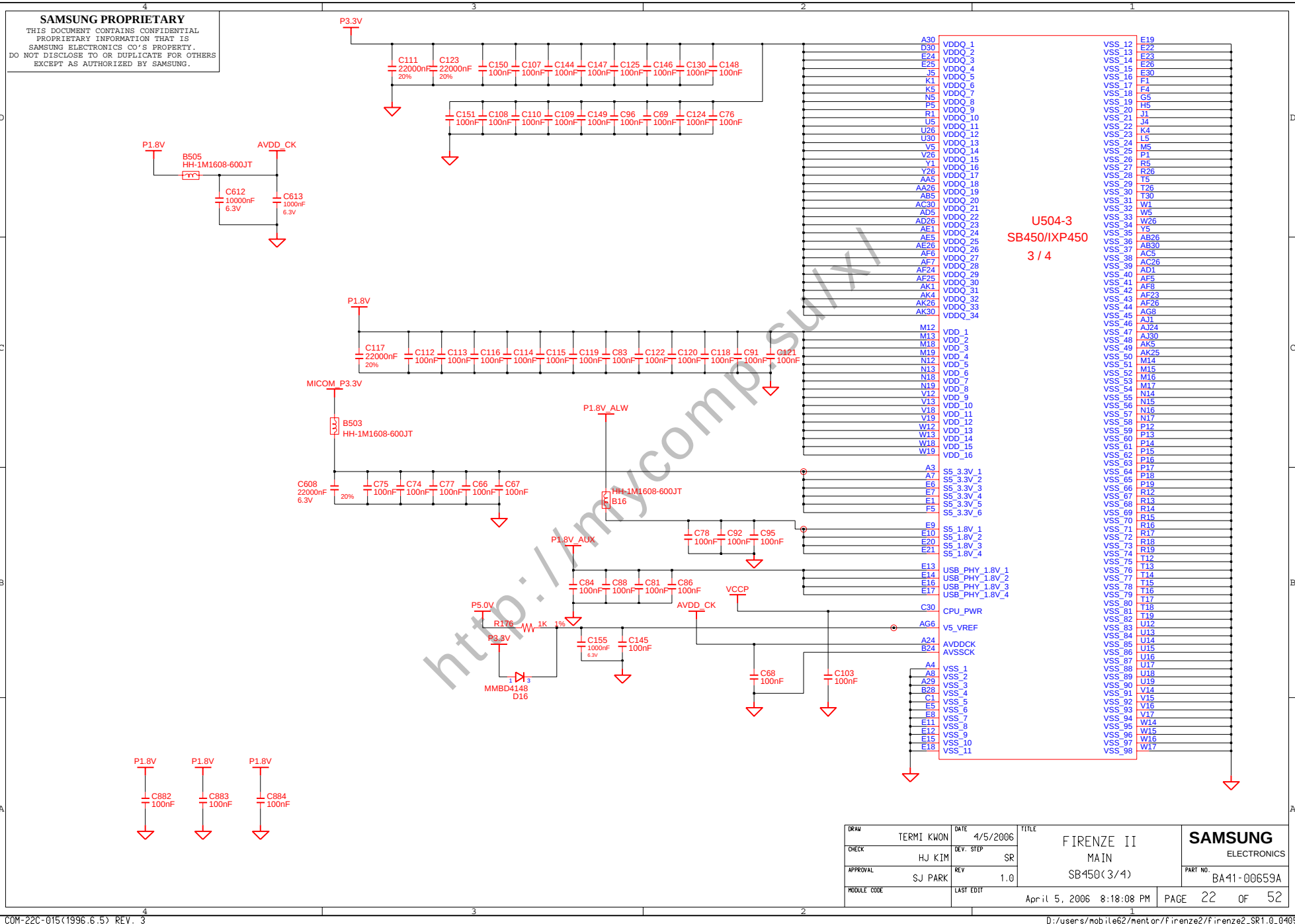


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|-------------|------------|-----------|----------|--------------------------|-----------------------------------|------------------------|
| DRAW        | TERMI KWON | DATE      | 4/5/2006 | TITLE                    | FIRENZE II<br>POWER<br>SB450(2/4) | SAMSUNG<br>ELECTRONICS |
| CHECK       | HJ KIM     | DEV. STEP | SR       |                          |                                   | PART NO. BA41-00659A   |
| APPROVAL    | SJ PARK    | REV       | 1.0      |                          |                                   |                        |
| MODULE CODE |            | LAST EDIT |          | April 5, 2006 8:18:08 PM | PAGE 21 OF 52                     |                        |



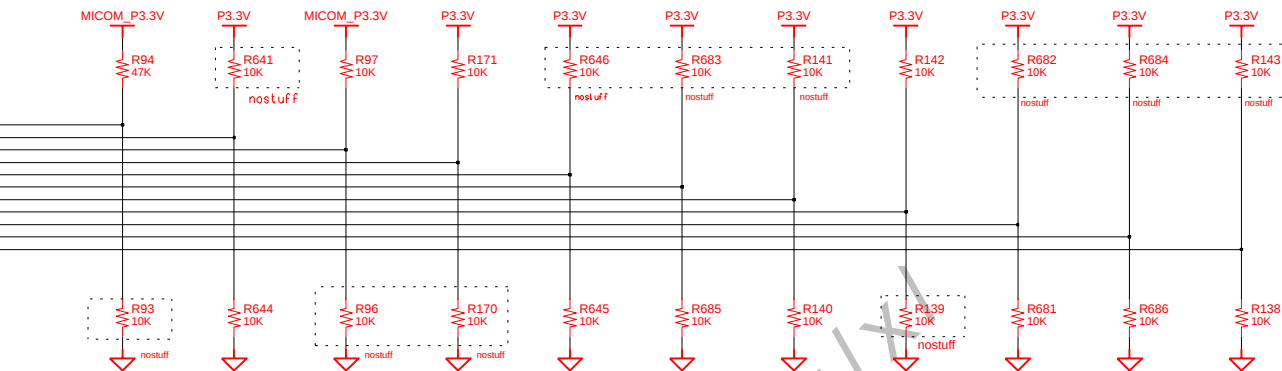


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## REQUIRED SYSTE STRAPS

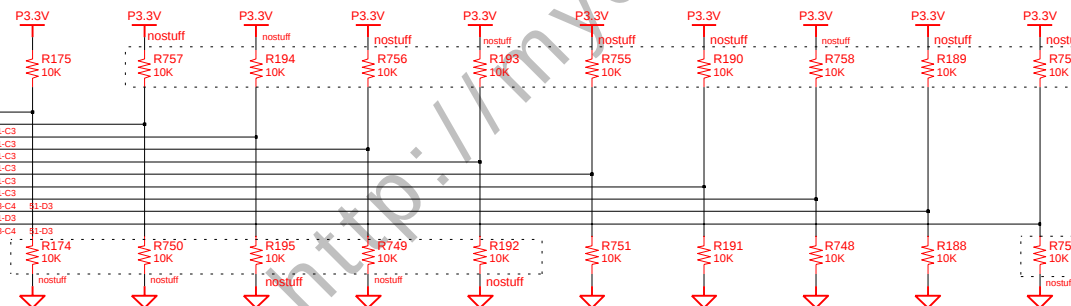
AUTO\_ON\*  
 AC\_SDOUT  
 RTC\_CLK  
 LPC3\_LFRAME\*  
 CLK3\_PCLKCB  
 CLK3\_PCLKSIO\_DS  
 CLK3\_PCLKSIO  
 CLK3\_PCLKFWH  
 CLK3\_PCLKMICOM  
 CLK3\_DBGIPC  
 PCI3\_CLK8



|            | AUTO_ON       | AC_SDOUT            | RTC_CLK      | LPC3_FRAME                     | PCI3_CLK2       | PCI3_CLK3               | PCI3_CLK4      | PCI3_CLK5              | PCI3_CLK6    | PCI3_CLK7, PCI3_CLK8                                                          |
|------------|---------------|---------------------|--------------|--------------------------------|-----------------|-------------------------|----------------|------------------------|--------------|-------------------------------------------------------------------------------|
| STRAP HIGH | MANUAL PWR ON | USE DEBUG STRAPS    | INTERNAL RTC | Enable thermtrip* on power up  | 48MHZ XTAL MODE | USB PHY PWRDOWN DISABLE | USE USB PLL    | PCI-E lane auto detect | CPU I/F = KB | ROM TYPE<br>H,H = PCI ROM<br>H,L = LPCROM I<br>LPC ADDRESS MAPPED             |
| STRAP LOW  | AUTO PWR ON   | IGNORE DEBUG STRAPS | EXRERNAL RTC | Disable thermtrip* on power up | 48MHZ OSC MODE  | USB PHY PWRDOWN ENABLE  | BYPASS USB PLL | Force PCI-E to lane2   | CPU I/F = P4 | BELOW 1 M<br>LPC ADDRESS MAPPED TO TOP 4G<br>L,H = LPC ROM II<br>LL = FWH ROM |

## DEBUS STRAPS

IDE5\_DACK\*  
 PCI3\_AD(31)  
 PCI3\_AD(30)  
 PCI3\_AD(29)  
 PCI3\_AD(28)  
 PCI3\_AD(27)  
 PCI3\_AD(26)  
 PCI3\_AD(25)  
 PCI3\_AD(24)  
 PCI3\_AD(23)



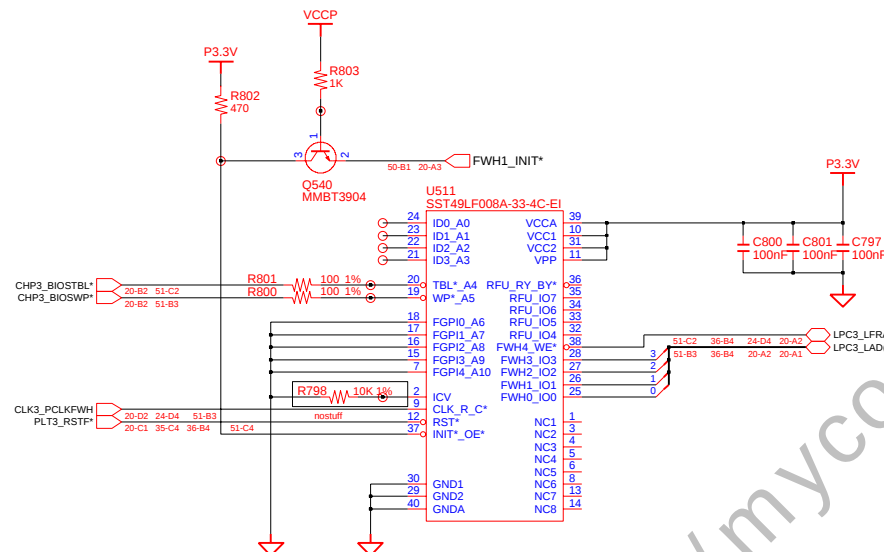
|            | IDE5_DACK*      | PCI3_AD(31) | PCI3_AD(30) | PCI3_AD(29) | PCI3_AD(28) | PCI3_AD(27)    | PCI3_AD(26)      | PCI3_AD(25)    | PCI3_AD(24)               | PCI3_AD(23) |
|------------|-----------------|-------------|-------------|-------------|-------------|----------------|------------------|----------------|---------------------------|-------------|
| STRAP HIGH | USE LONG RESET  | RESERVED    | RESERVED    | RESERVED    | RESERVED    | BYPASS PCI PLL | BYPASS ACPI BCLK | BYPASS IDE PLL | BYPASS EEPROM PCIE STRAPS | RESERVED    |
| STRAP LOW  | USE SHORT RESET |             |             |             |             | USE PCI PLL    | USE ACPI BCLK    | USE IDE PLL    | USE DEFAULT PCIE STRAPS   |             |

|             |            |           |          |       |            |                                                |
|-------------|------------|-----------|----------|-------|------------|------------------------------------------------|
| DRAW        | TERMI KWON | DATE      | 4/5/2006 | TITLE | FIRENZE II | SAMSUNG<br>ELECTRONICS<br>PART NO. BA41-00659A |
| CHECK       | HJ KIM     | DEV. STEP | SR       |       |            |                                                |
| APPROVAL    | SJ PARK    | REV       | 1.0      |       | STRAPS     |                                                |
| MODULE CODE |            | LAST EDIT |          |       |            |                                                |

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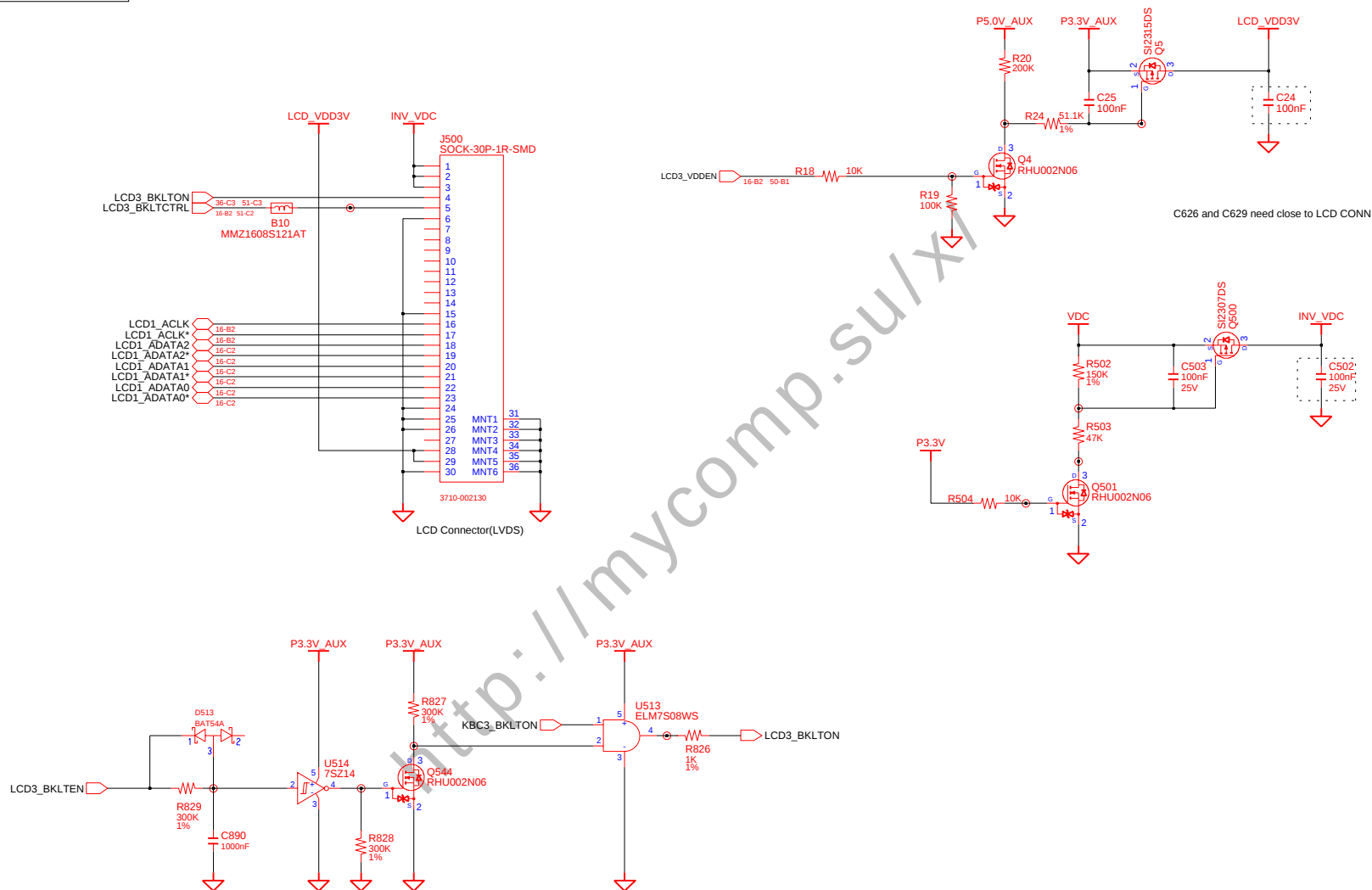


- |    |                                                 |    |                                 |
|----|-------------------------------------------------|----|---------------------------------|
| 02 | VERIFY REAL MODE                                | 66 | CONFIGURE ADVANCE CACHE REG.    |
| 03 | DISABLE NMI                                     | 6A | DISPLAY EXTERNAL CACHE SIZE     |
| 04 | GET CPU TYPE                                    | 6C | DISPLAY SHADOW MESSAGE          |
| 06 | INIT. SYSTEM H/W                                | 6E | DISPLAY NON-DISPOSABLE SEGMENT  |
| 08 | INIT. CHIPSET REG.                              | 70 | DISPLAY ERROR MESSAGE           |
| 09 | SET IN POST FLAG                                | 72 | CHECK FOR CONFIGURATION ERROR   |
| 0A | INIT CPU.REG                                    | 74 | TEST REAL-TIME CLOCK            |
| 0B | CPU CACHE ON                                    | 76 | CHECK FOR KEYBOARD EERROR       |
| 0C | INIT.CACHE TO POST                              | 7C | SETUP HARDWARE INTERRUPT VECTOR |
| 0E | INIT. I/O VALUE                                 | 7E | TEST COPROCESSOR IF PRESENT     |
| 0F | ENABLE THE L-BUS IDE                            | 80 | DISABLE ON-BOARD I/O PORT       |
| 10 | INIT. POWER MANAGER                             | 82 | DETECT AND INSTALL EXT.RS232C   |
| 11 | LOAD ALTERNATE REG.                             | 84 | DETECT AND INSTALL EXT.PARALLEL |
| 13 | PCI BUS MASTER RESET<br>WITH INITIAL POST VALUE | 86 | RE-INIT. ON-BOARD I/O PORT      |
| 14 | INIT. KEYBOARD CONTROLLER                       | 88 | INIT. BIOS DATA ROM             |
| 16 | CHECK CHECKSUM                                  | 8A | INIT.EXTENDED BIOS DATA AREA    |
| 18 | 8254 TIMER INIT.                                | 8C | INIT. FDD CONTROLLER            |
| 1A | 8237 DMA CONTROLLER INIT.                       | 9A | SHADOW OPTION ROMS              |
| 1C | RESET INTERRUPT CONTROLLER                      | 9C | SETUP POWER MANAGEMENT          |
| 20 | TEST DRAM REFRESH                               | 9E | ENABLE H/W INTERRUPT            |
| 22 | TEST 8742 KEYBOARD CONTROLLER                   | A0 | SET TIME OF DAY                 |
| 24 | SET ES SEGMENT REG. TO 4GB                      | A4 | INIT. TYPEMATIC RATE            |
| 26 | ENABLE A20                                      | A8 | ERASE F2 PROMPT                 |
| 28 | AUTO SIZING DRAM                                | AA | SCAN FOR F2 KEY STROKE          |
| 32 | COMPUTE THE CPU SPEED                           | AC | ENTER SETUP                     |
| 34 | TESET CMOS RAM                                  | AE | CLEAR IN POST FLAG              |
| 38 | SHADOW SYSTEM BIOS ROM                          | B0 | CHECK FOR ERRORS                |
| 3A | AUTO SIZING CACHE                               | B2 | POST DONE-PREPARE TO BOOT O/S   |
| 3C | CONFIGURE ADVANCED CHIPSET REG.                 | B4 | ONE BEEP                        |
| 3D | LOAD ALTER REG. WITH CMOS VALUE                 | B6 | CHECK PASSWORD (OPTION)         |
| 42 | INIT. INTERRUPT VECTOR                          | B7 | ACPI INIT                       |
| 44 | INIT. BIOS INTERRUPT                            | BA | DMI INIT                        |
| 46 | CHECK ROM COPYRIGHT NOTICE                      | BE | CLEAR SCREEN                    |
| 47 | INIT. I20 SUPPORT IF INSTALLED                  | C0 | TRY BOOT WITH INT19             |
| 48 | CHECK VIDEO CONFIGURE AGAINST CMOS              | D0 | INTERRUPT HANDLER ERROR         |
| 49 | INIT. PCI BUS AND DEVICE                        | D2 | UNKNOWN INTERRUPT ERROR         |
| 4A | INIT. ALL VIDEO BIOS ROM                        | D4 | PENDING INTERRUPT ERROR         |
| 4C | SHADOW VIDEO BIOS ROM                           | D6 | SHUTDOWN 5                      |
| 50 | DISPLAY CPU TYPE AND SPEED                      | D8 | SHUTDOWN ERROR                  |
| 52 | TEST KEYBOARD                                   | DA | EXTENDED BLOCK MOVE             |
| 54 | SET KEYCLICK IF ENABLED                         | DC | SHUTDOWN 10                     |
| 56 | ENABLE KEYBOARD                                 | 89 | ENABLE NMI                      |
| 58 | TEST FOR UNEXPECTED INTERRUPTS                  | 90 | INIT. HDD CONTROLLER            |
| 5A | DISPLAY "PRESS ..... SETUP"                     | 91 | INIT. LOCAL BUS HDD CONTROLLER  |
| 5C | TEST RAM BETWEEN 512K AND 640K                  | 92 | JUMP TO USER PATCH 2            |
| 60 | TEST EXTENDED MEMORY                            | 94 | DISABLE A20 ADDRESS LINE        |
| 62 | TEST EXTENDED MEMORY ADDRESS LINE               | 96 | CLEAR HUGE ES SEGMENT REG.      |
| 64 | JUMP TO USER PATCH 1                            | 98 | SEARCH FOR OPTION ROMS          |

|             |            |           |          |                          |                    |                         |
|-------------|------------|-----------|----------|--------------------------|--------------------|-------------------------|
| DRAW        | TERMI KWON | DATE      | 4/5/2006 | TITLE                    | FIRENZE II<br>MAIN | SAMSUNG<br>ELECTRONICS  |
| CHECK       | HJ KIM     | DEV. STEP | SR       |                          |                    |                         |
| APPROVAL    | SJ PARK    | REV       | 1.0      | FIRMWARE HUB             |                    | PART NO.<br>BA41-00659A |
| MODULE CODE |            | LAST EDIT |          | April 5, 2006 8:18:08 PM | PAGE               | 25 OF 52                |

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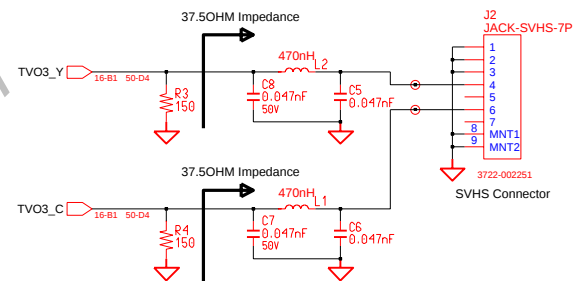
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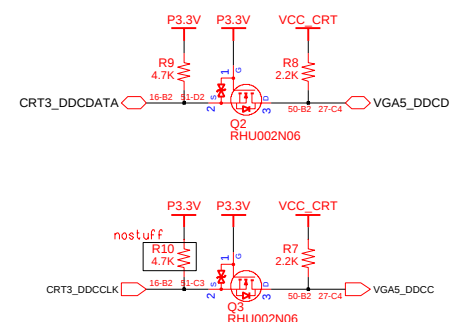
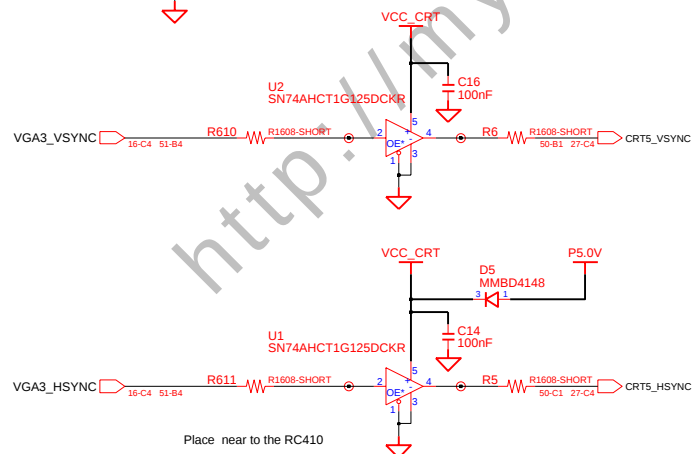
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| DRAW        | TERMI KWON | DATE      | 4/5/2006 | TITLE | FIRENZE II      | SAMSUNG<br>ELECTRONICS<br>PART NO. BA41-00659A |
| CHECK       | HJ KIM     | DEV. STEP | SR       |       | LCD Connector & |                                                |
| APPROVAL    | SJ PARK    | REV       | 1.0      |       | SPREAD SPECTRUM |                                                |
| MODULE CODE |            | LAST EDIT |          |       |                 |                                                |

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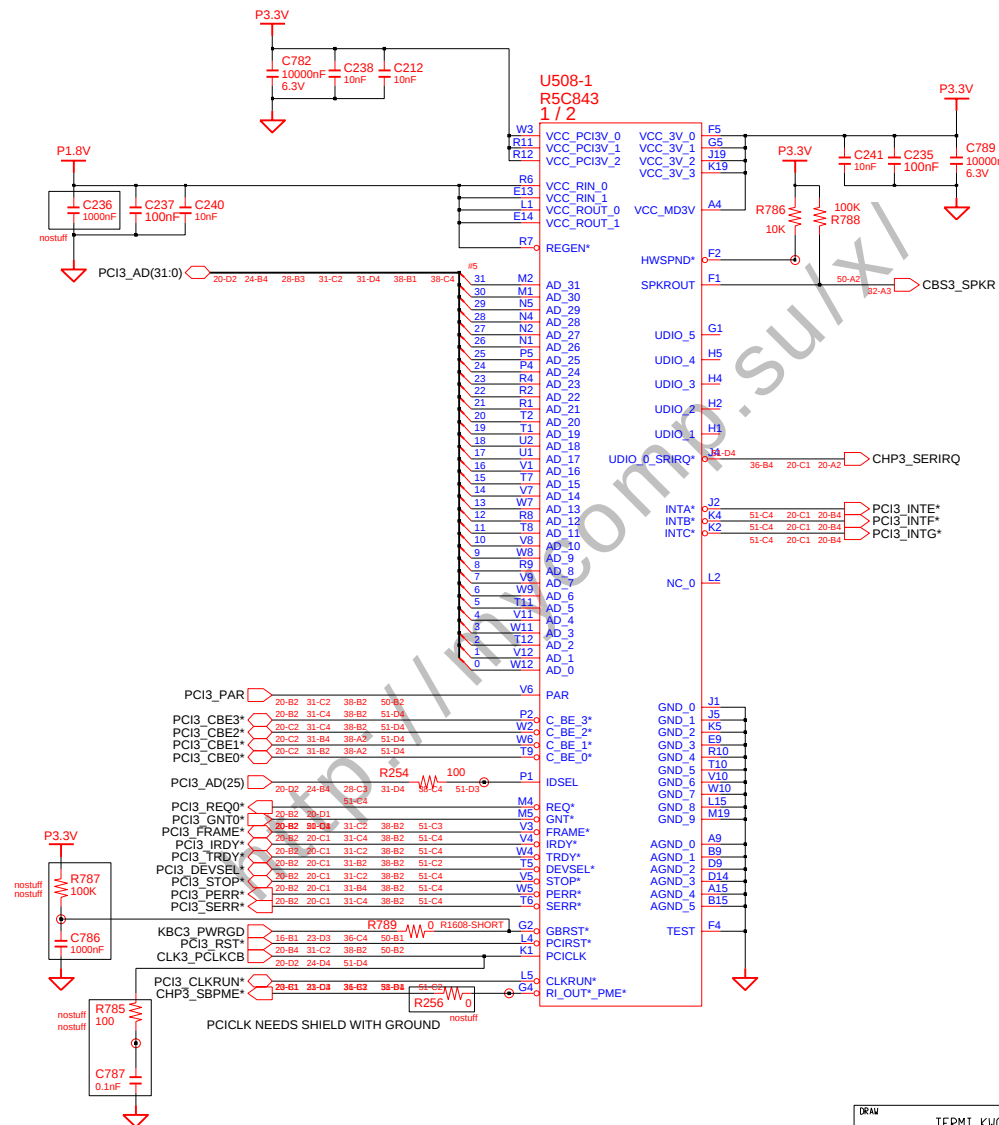
TV-OUT(S-VHS,COMPOSIT)



|             |            |           |                          |                |            |                        |             |    |
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| DRAM        | TERMI KWON | DATE      | 4/5/2006                 | TITLE          | FIRENZE II | SAMSUNG<br>ELECTRONICS |             |    |
| CHECK       | HJ KIM     | DEV. STEP | SR                       |                |            |                        |             |    |
| APPROVAL    | SJ PARK    | REV       | 1.0                      |                |            |                        |             |    |
| MODULE CODE | LAST EDIT  |           | April 5, 2006 8:18:08 PM |                |            |                        | PAGE        | 27 |
|             |            |           |                          | CRT AND TV-OUT |            | PART NO.               | BA41-00659A |    |

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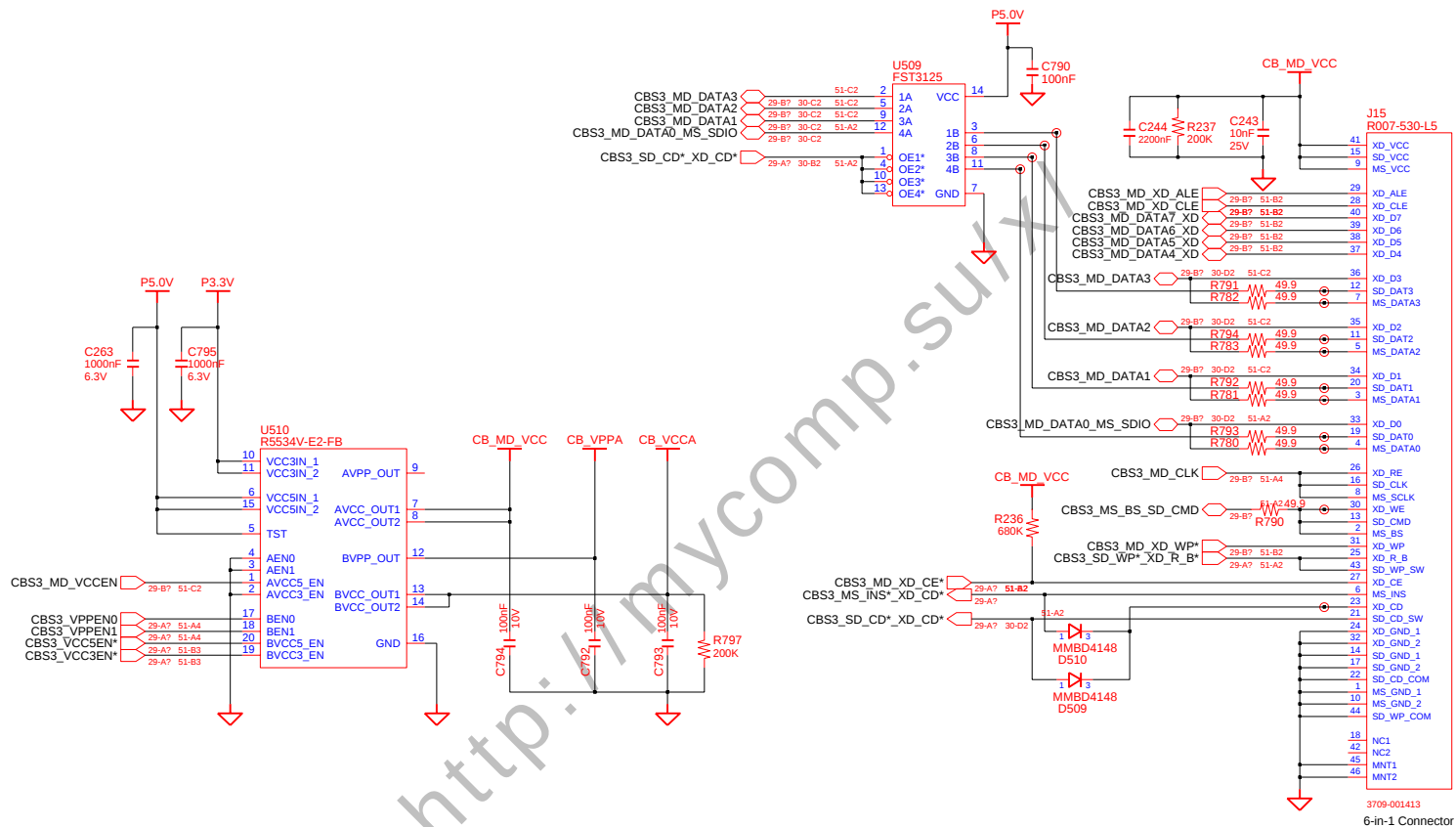


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| DRAW        | TERMI KWON | DATE      | 4/5/2006 | TITLE                    | FIRENZE II    | SAMSUNG<br>ELECTRONICS<br>PART NO. BA41-00659A |
| CHECK       | HJ KIM     | DEV. STEP | SR       |                          |               |                                                |
| APPROVAL    | SJ PARK    | REV       | 1.0      |                          | CARDBUS(1/2)  |                                                |
| MODULE CODE |            | LAST EDIT |          | April 5, 2006 8:18:08 PM | PAGE 28 OF 52 |                                                |



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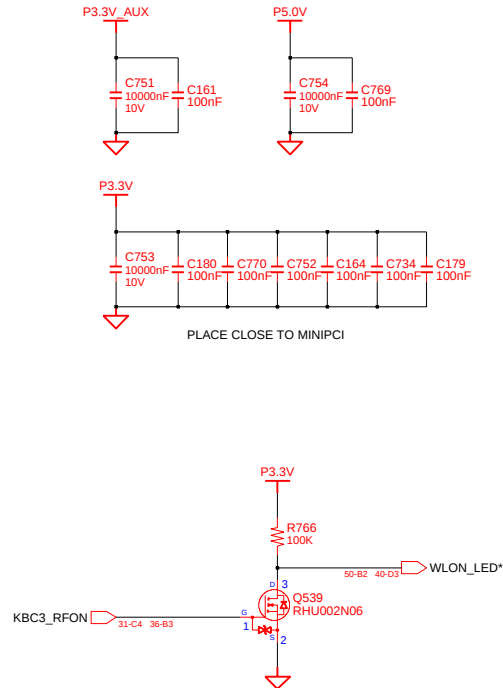
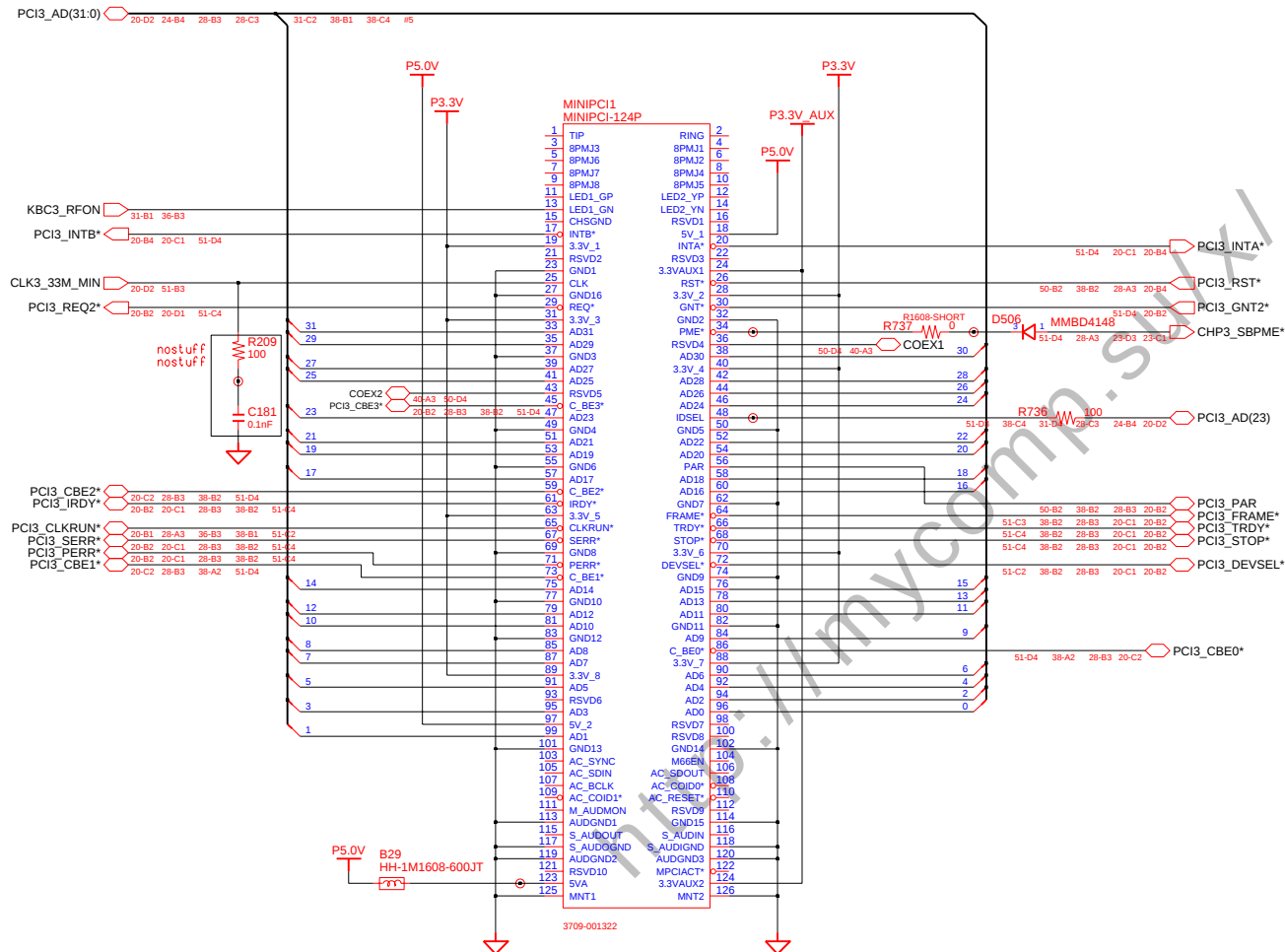
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|-------------|------------|-----------|----------|-------------------------|---------------|------------------------------------------------|
| DRAW        | TERMI KWON | DATE      | 4/5/2006 | TITLE                   | FIRENZE II    | SAMSUNG<br>ELECTRONICS<br>PART NO. BA41-00659A |
| CHECK       | HJ KTM     | DEV. STEP | SR       |                         |               |                                                |
| APPROVAL    | SJ PARK    | REV       | 1.0      |                         | 5 in 1 Socket |                                                |
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|             |            |           |          | Apr 15, 2006 8:18:08 PM | PAGE          | 30 OF 52                                       |

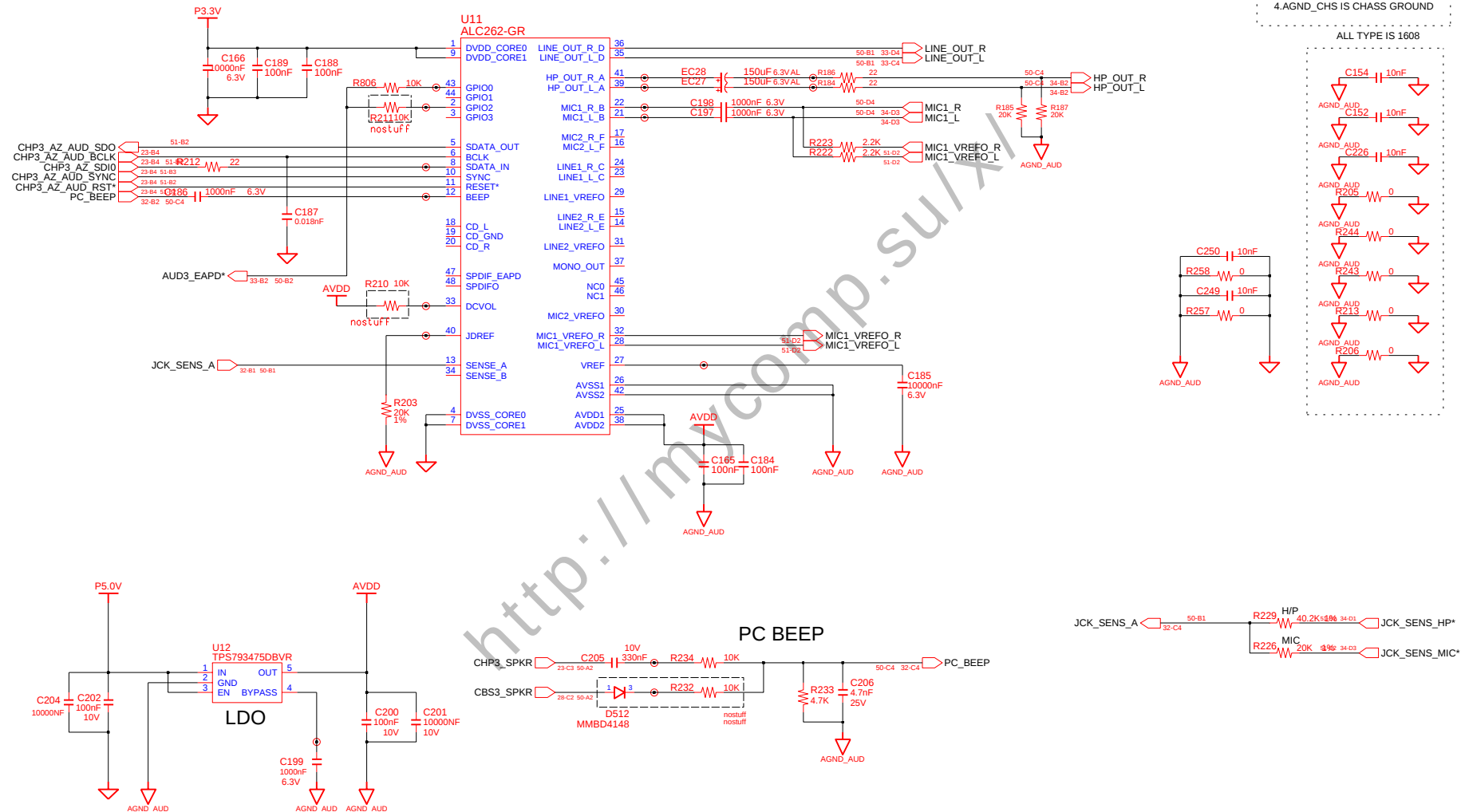
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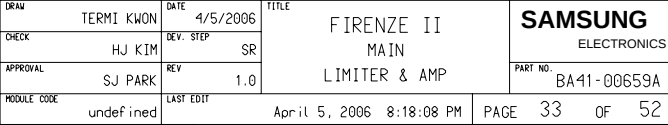
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| CHECK       | HJ KIM     | DEV. STEP | SR                       |       |                                |                        |
| APPROVAL    | SJ PARK    | REV       | 1.0                      |       |                                |                        |
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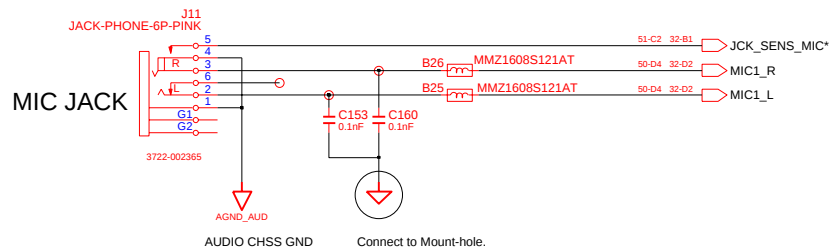
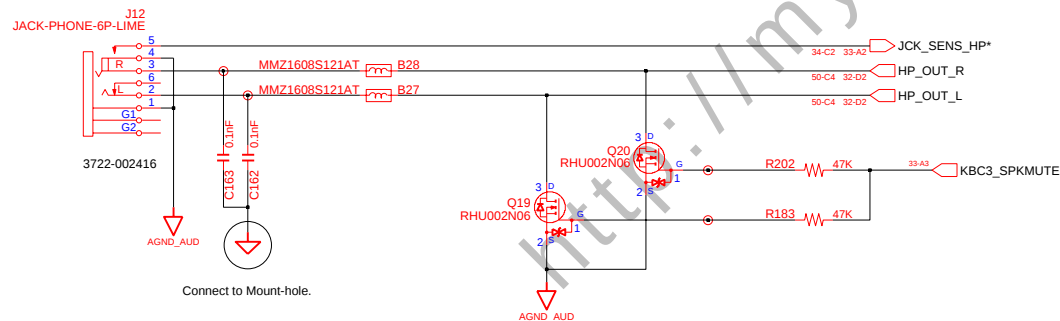
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| DRWN        | TERMI KWON | DATE      | 4/5/2006                 | TITLE    | FIRENZE II<br>MAIN<br>AUDIO CODEC | <b>SAMSUNG</b><br>ELECTRONICS |             |
| CHECK       | HJ KIM     | DEV. STEP | SR                       |          |                                   |                               |             |
| APPROVAL    | SJ PARK    | REV       | 1.0                      | PART NO. |                                   |                               | BA41-00659A |
| MODULE CODE | undefined  | LAST EDIT | April 5, 2006 8:18:08 PM | PAGE     |                                   |                               | 32 OF 52    |

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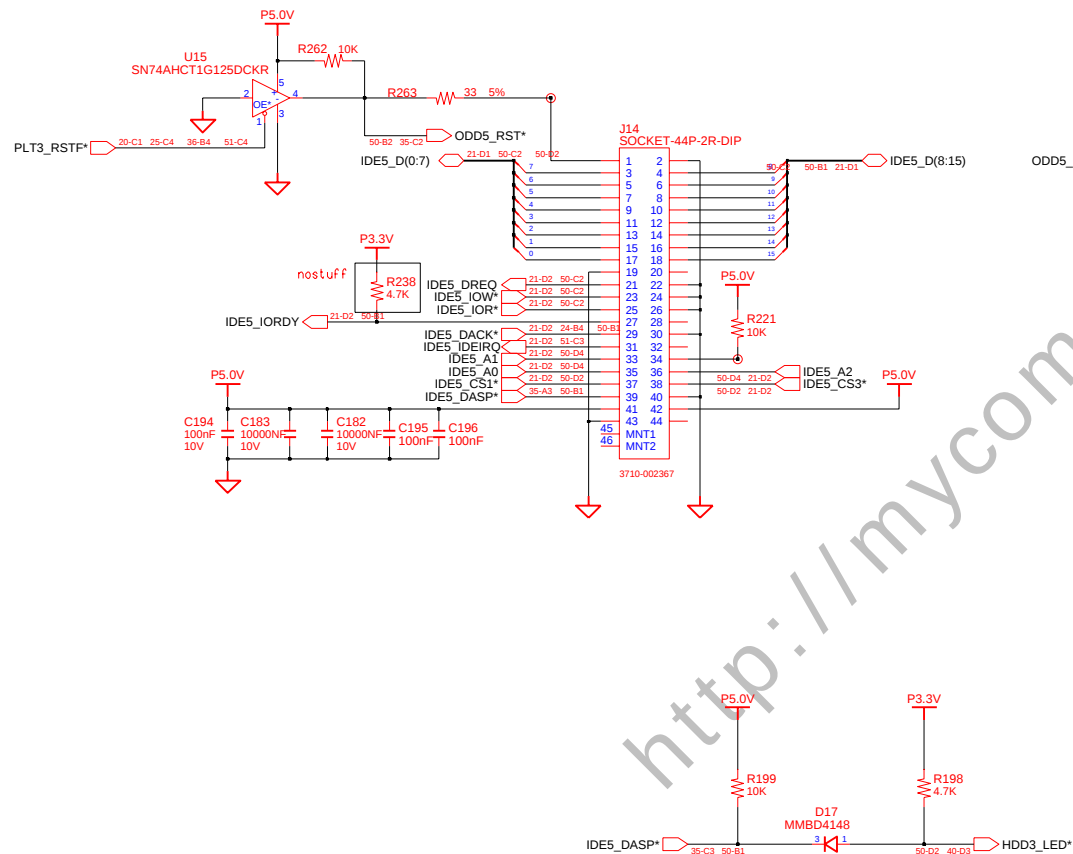
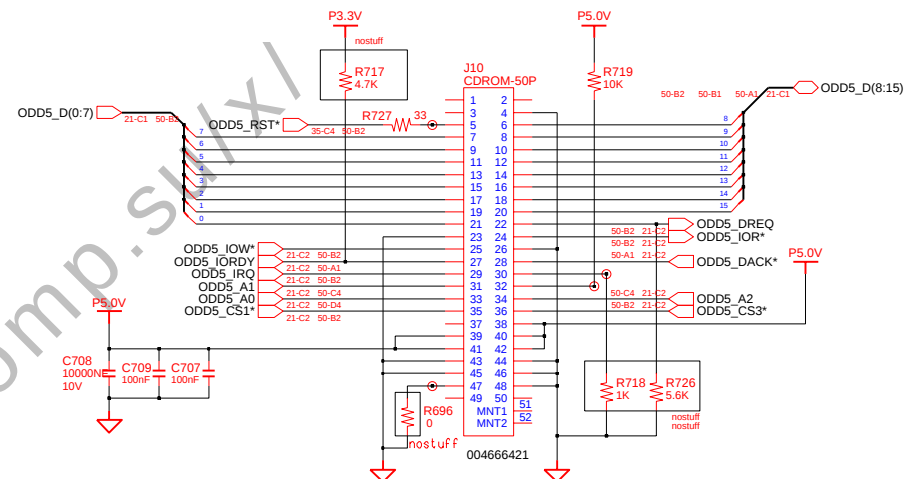
**HEADPHONE**

The traces led to Audio Jacks have the width over 10mil

|             |            |           |          |                          |                    |                                                       |
|-------------|------------|-----------|----------|--------------------------|--------------------|-------------------------------------------------------|
| DRAW        | TERMI KWON | DATE      | 4/5/2006 | TITLE                    | FIRENZE II         | <b>SAMSUNG</b><br>ELECTRONICS<br>PART NO. BA41-00659A |
| CHECK       | HJ KIM     | DEV. STEP | SR       |                          | MAIN               |                                                       |
| APPROVAL    | SJ PARK    | REV       | 1.0      |                          | UPPER & AUDIO CONN |                                                       |
| MODULE CODE | undefined  | LAST EDIT |          | April 5, 2006 8:18:08 PM | PAGE 34 OF 52      |                                                       |

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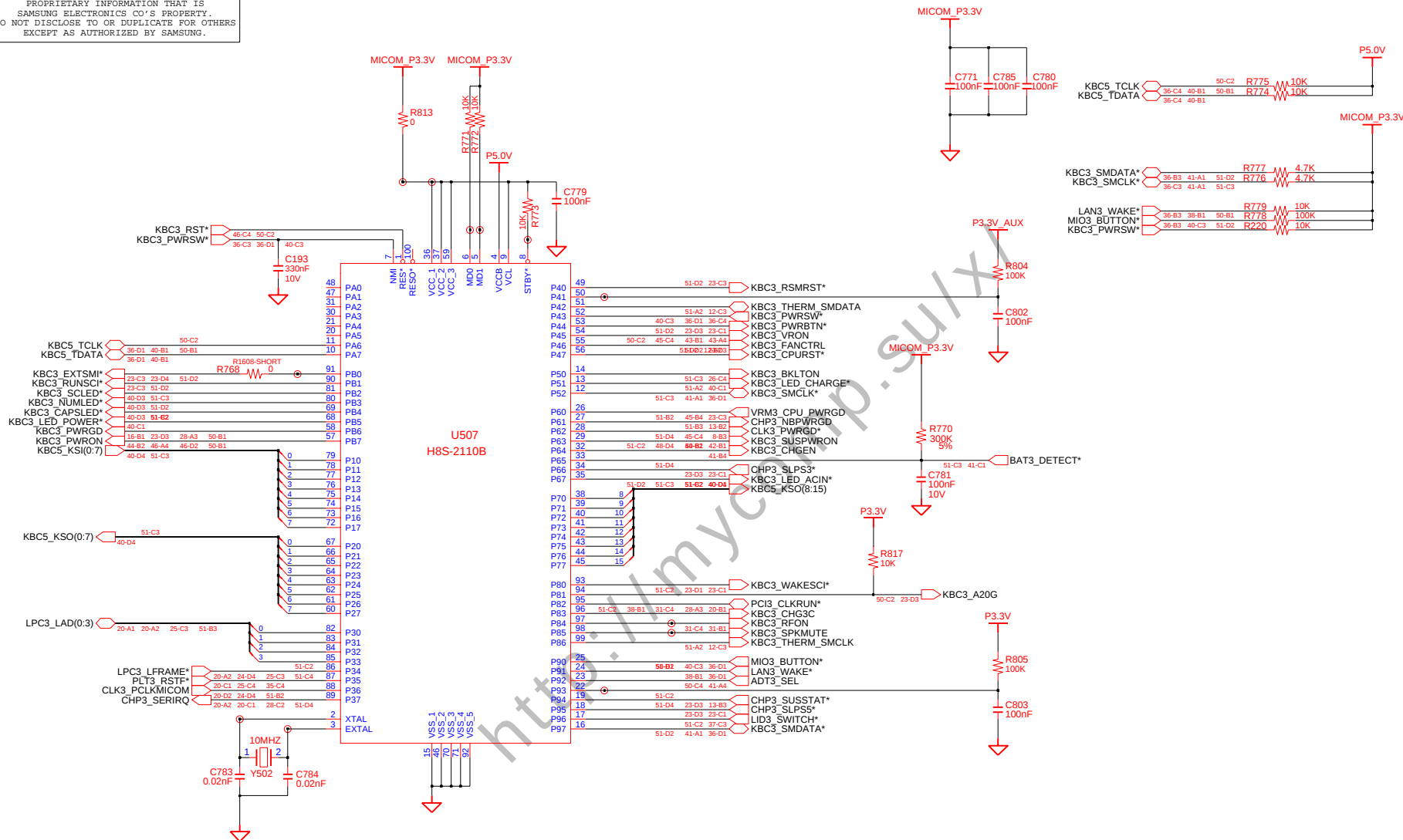
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**Main to HDD****Main to ODD**

|             |            |           |          |                          |                                  |                                                |
|-------------|------------|-----------|----------|--------------------------|----------------------------------|------------------------------------------------|
| DRAW        | TERMI KWON | DATE      | 4/5/2006 | TITLE                    | FIRENZE II<br>POWER<br>HDD & ODD | SAMSUNG<br>ELECTRONICS<br>PART NO. BA41-00659A |
| CHECK       | HJ KIM     | DEV. STEP | SR       |                          |                                  |                                                |
| APPROVAL    | SJ PARK    | REV       | 1.0      |                          |                                  |                                                |
| MODULE CODE | undefined  | LAST EDIT |          |                          |                                  |                                                |
|             |            |           |          | April 5, 2006 8:18:08 PM | PAGE 35 OF 52                    |                                                |

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## MICOM Crisis Update

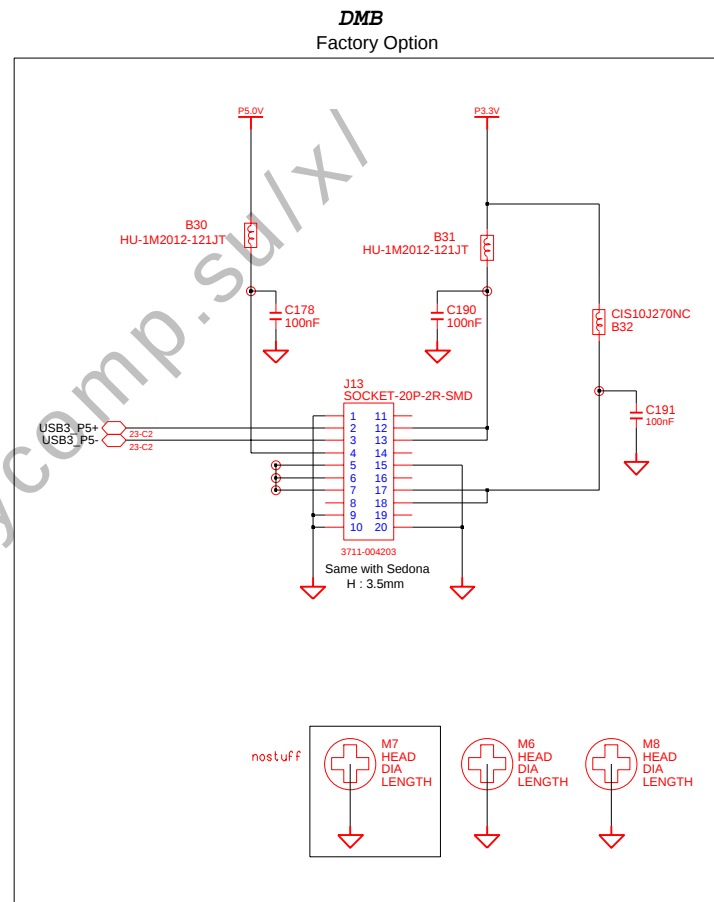
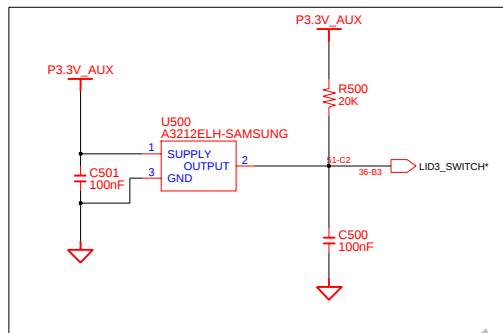
Condition: P90=P91=P92=High(MICOM\_P3V)  
MD0=MD1=Low(0V)  
Serial Port: P84 & P85

The removed signal compared from 144pin

KBC5\_CAL\_THRM\*  
THRM\_ALERT\*  
LCD3\_BKLTEN  
FAN3\_FDBACK\*  
THERM\_STP\*

|             |            |           |                          |       |                              |                         |
|-------------|------------|-----------|--------------------------|-------|------------------------------|-------------------------|
| DRAW        | TERMI KWON | DATE      | 4/5/2006                 | TITLE | FIRENZE II<br>POWER<br>MICOM | SAMSUNG<br>ELECTRONICS  |
| CHECK       | HJ KTM     | DEV. STEP | SR                       |       |                              | PART NO.<br>BA41-00659A |
| APPROVAL    | SJ PARK    | REV       | 1.0                      |       |                              |                         |
| MODULE CODE | undefined  | LAST EDIT | April 5, 2006 8:18:08 PM | PAGE  | 36                           | OF 52                   |

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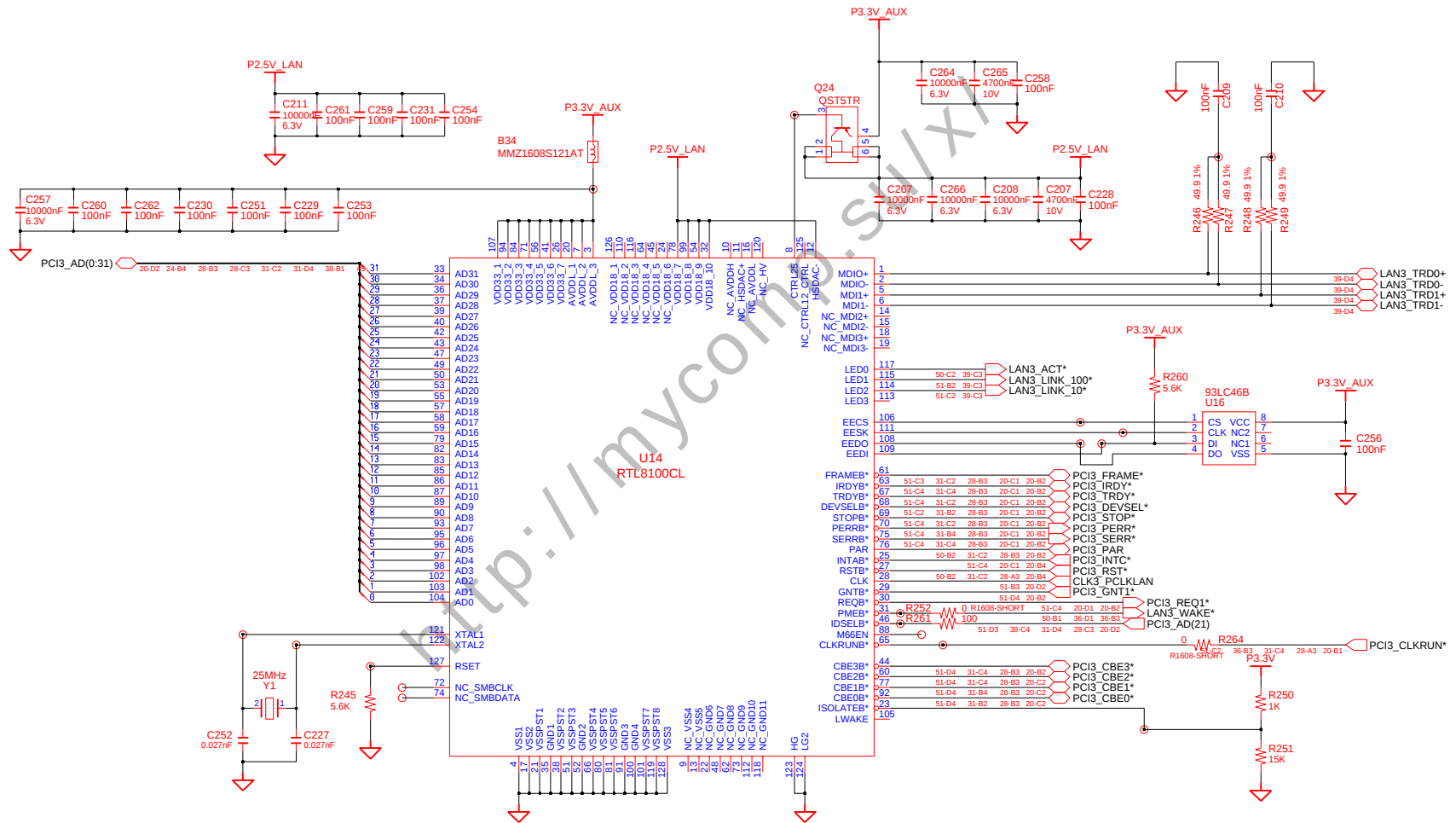


|                                                                                          |                                                                                            |                                    |                                                          |
|------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------|------------------------------------|----------------------------------------------------------|
| DRAW<br>TERM1 KWON<br>CHECK<br>HU KIM<br>APPROVAL<br>SU PARK<br>MODULE CODE<br>undefined | DATE<br>4/5/2006<br>DEV. STEP<br>SR<br>REV<br>1.0<br>LAST EDIT<br>April 5, 2006 8:18:08 PM | TITLE<br>FIRENZE II<br>MAIN<br>LPC | <b>SAMSUNG</b><br>ELECTRONICS<br>PART NO.<br>BA41-00659A |
|                                                                                          |                                                                                            | PAGE 37                            | OF 52                                                    |

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# LAN Controller (Only 10/100M)

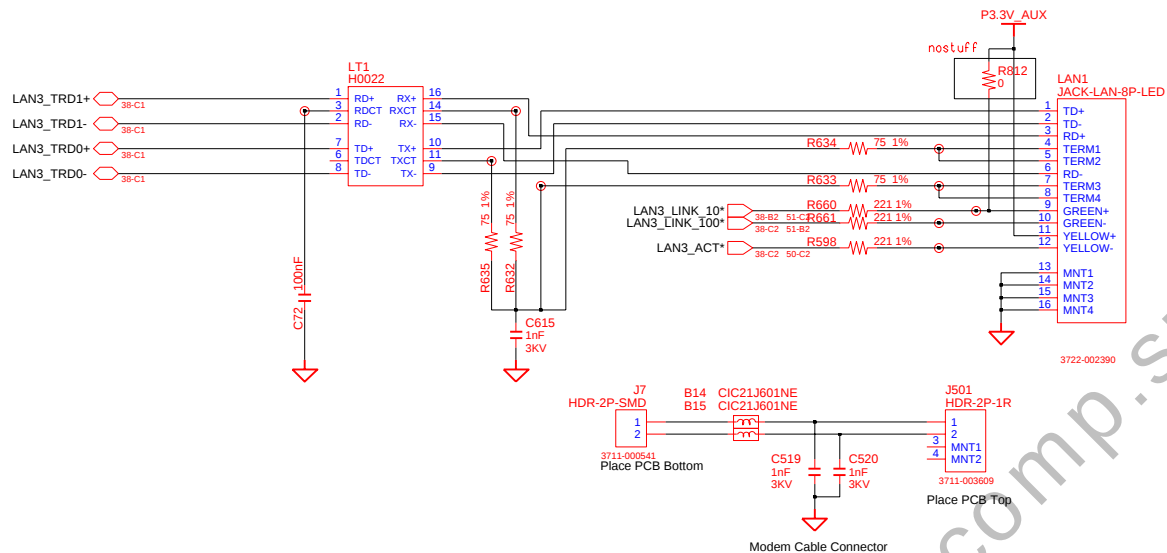


|             |            |           |                          |       |            |                                                |
|-------------|------------|-----------|--------------------------|-------|------------|------------------------------------------------|
| DRAW        | TERMI KWON | DATE      | 4/5/2006                 | TITLE | FIRENZE II | SAMSUNG<br>ELECTRONICS<br>PART NO. BA41-00659A |
| CHECK       | HJ KIM     | DEV. STEP | SR                       | MAIN  | LAN        |                                                |
| APPROVAL    | SJ PARK    | REV       | 1.0                      |       |            |                                                |
| MODULE CODE | undefined  | LAST EDIT | April 5, 2006 8:18:08 PM | PAGE  | 38 OF 52   |                                                |

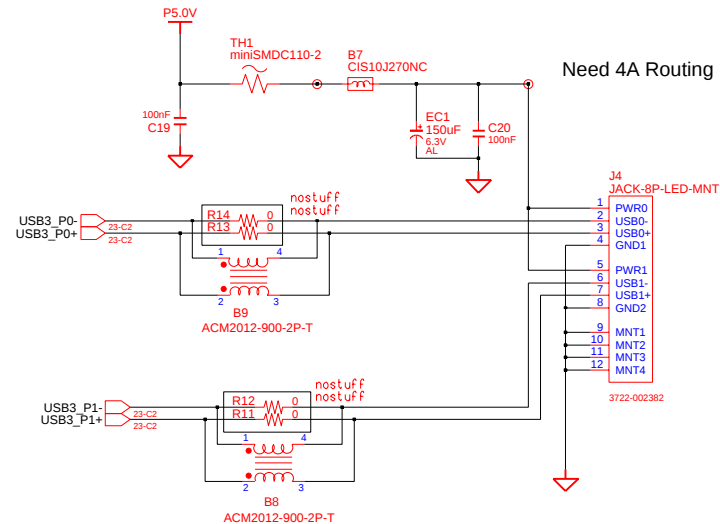
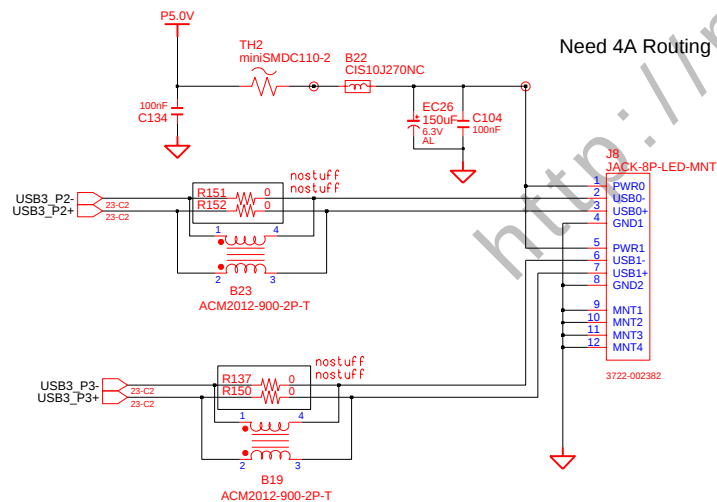
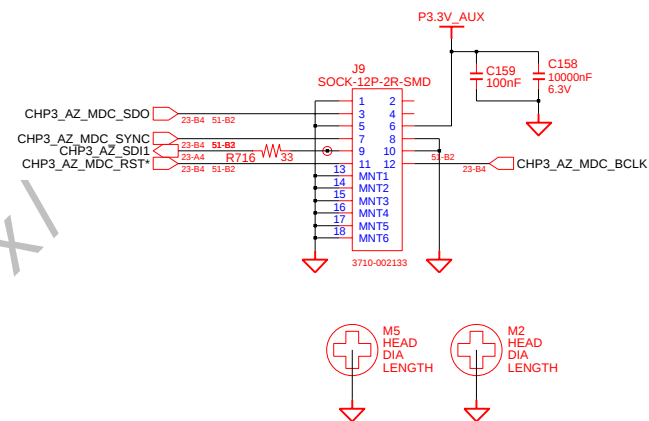
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## LAN Connector



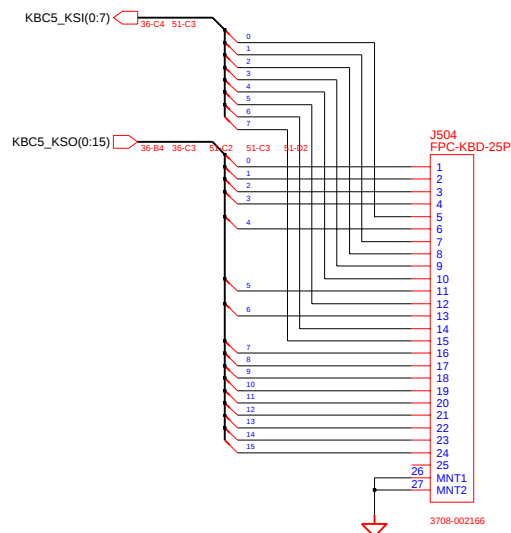
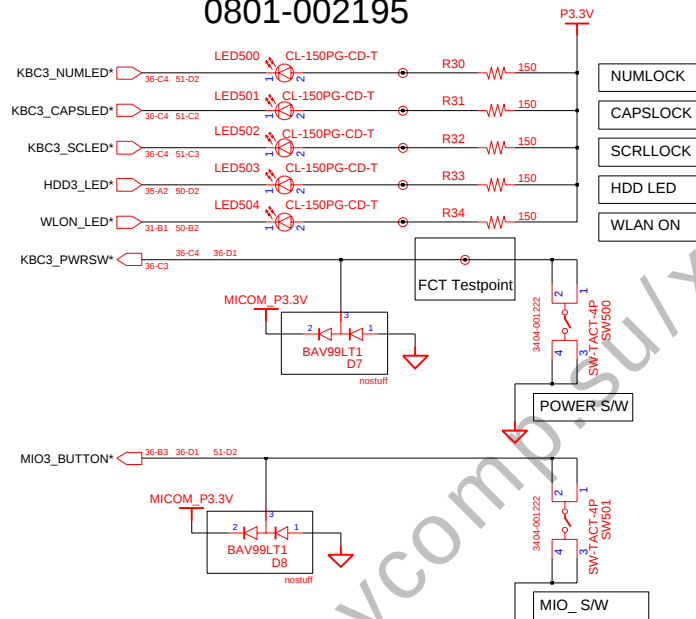
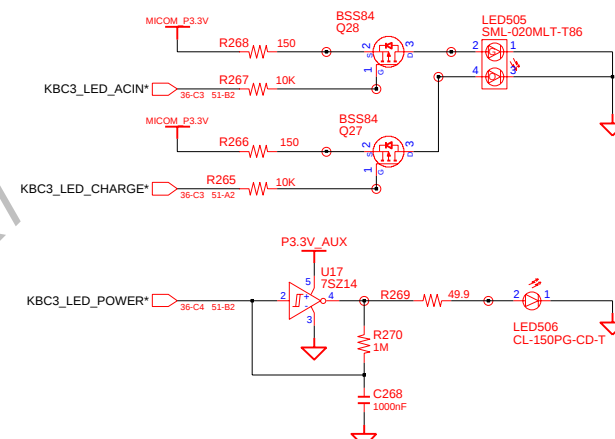
## MDC Connector



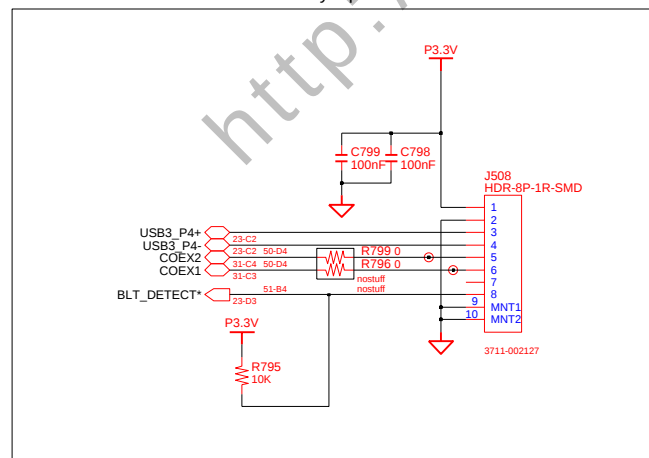
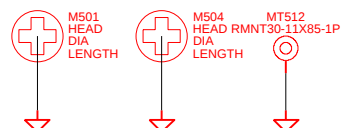
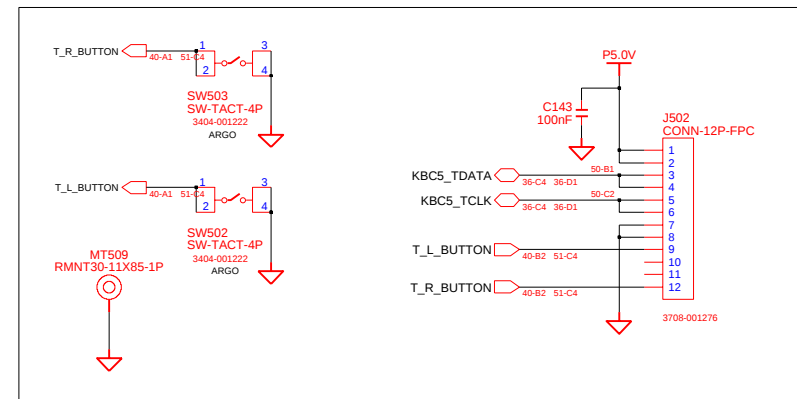
|             |            |           |          |                         |                          |                      |
|-------------|------------|-----------|----------|-------------------------|--------------------------|----------------------|
| DRAW        | TERMI KWON | DATE      | 4/5/2006 | TITLE                   | FIRENZE II               | SAMSUNG              |
| CHECK       | HJ KIM     | DEV. STEP | SR       | MAIN                    | LAN & USB0 & MODEM Conn. | ELECTRONICS          |
| APPROVAL    | SJ PARK    | REV       | 1.0      |                         |                          | PART NO. BA41-00659A |
| MODULE CODE | undefined  | LAST EDIT |          | Apr 15, 2006 8:18:08 PM | PAGE                     | 39 OF 52             |

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**KEYBOARD**  
Same connector with Sedona**LED**  
0801-002195**ADAPTERIN/CHARGING LED****Bluetooth Interface**

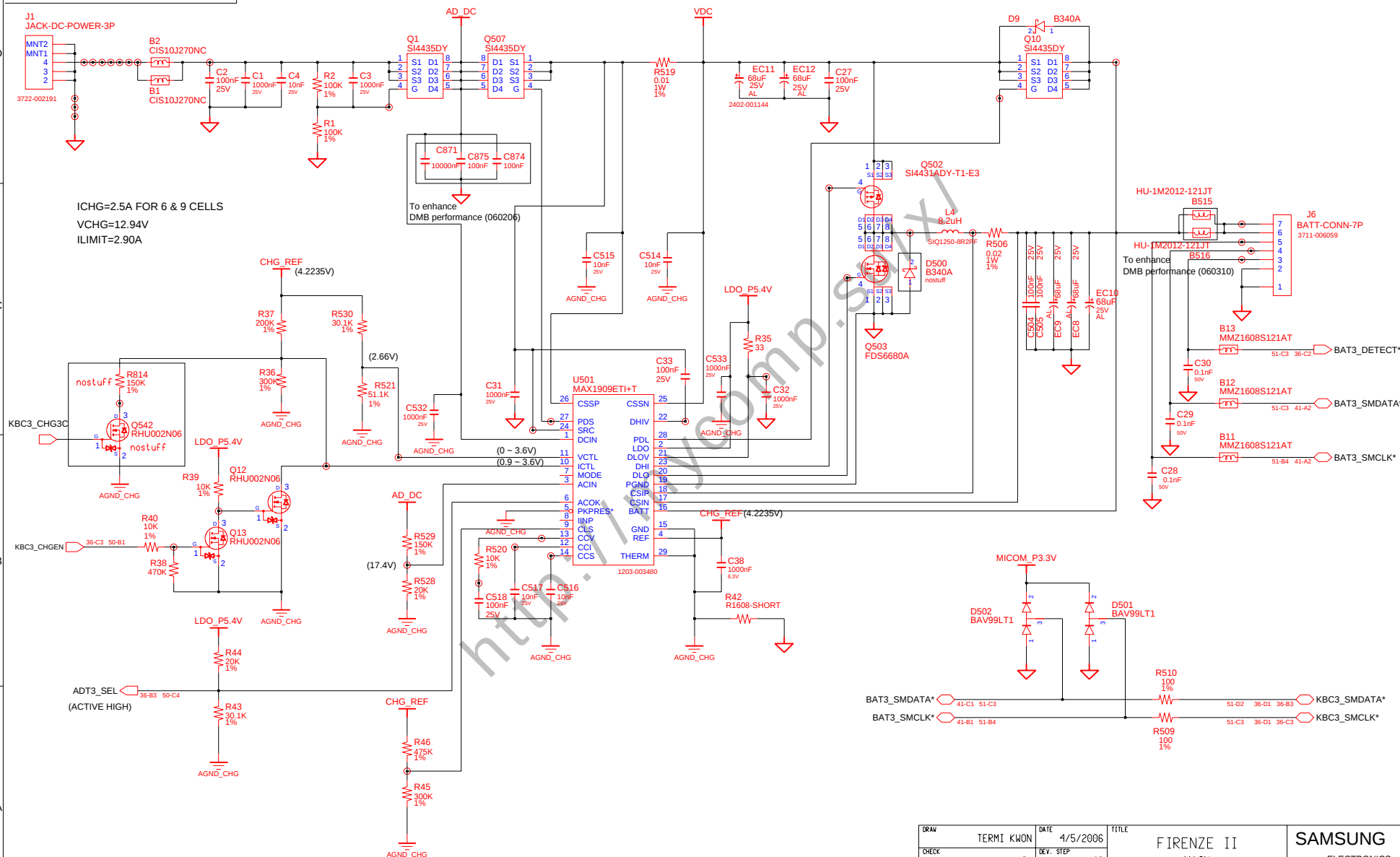
Factory Option

**TOUCHPAD**

|             |            |           |                          |                      |            |                        |
|-------------|------------|-----------|--------------------------|----------------------|------------|------------------------|
| DRAW        | TERMI KWON | DATE      | 4/5/2006                 | TITLE                | FIRENZE II | SAMSUNG<br>ELECTRONICS |
| CHECK       | HJ KIM     | DEV. STEP | SR                       | MAIN                 |            |                        |
| APPROVAL    | SJ PARK    | REV       | 1.0                      | B'D TO B'D CONNECTOR | PART NO.   | BA41-00659A            |
| MODULE CODE | undefined  | LAST EDIT | April 5, 2006 8:18:08 PM | PAGE                 | 40         | OF 52                  |

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## CHARGER & POWER MANAGEMENT

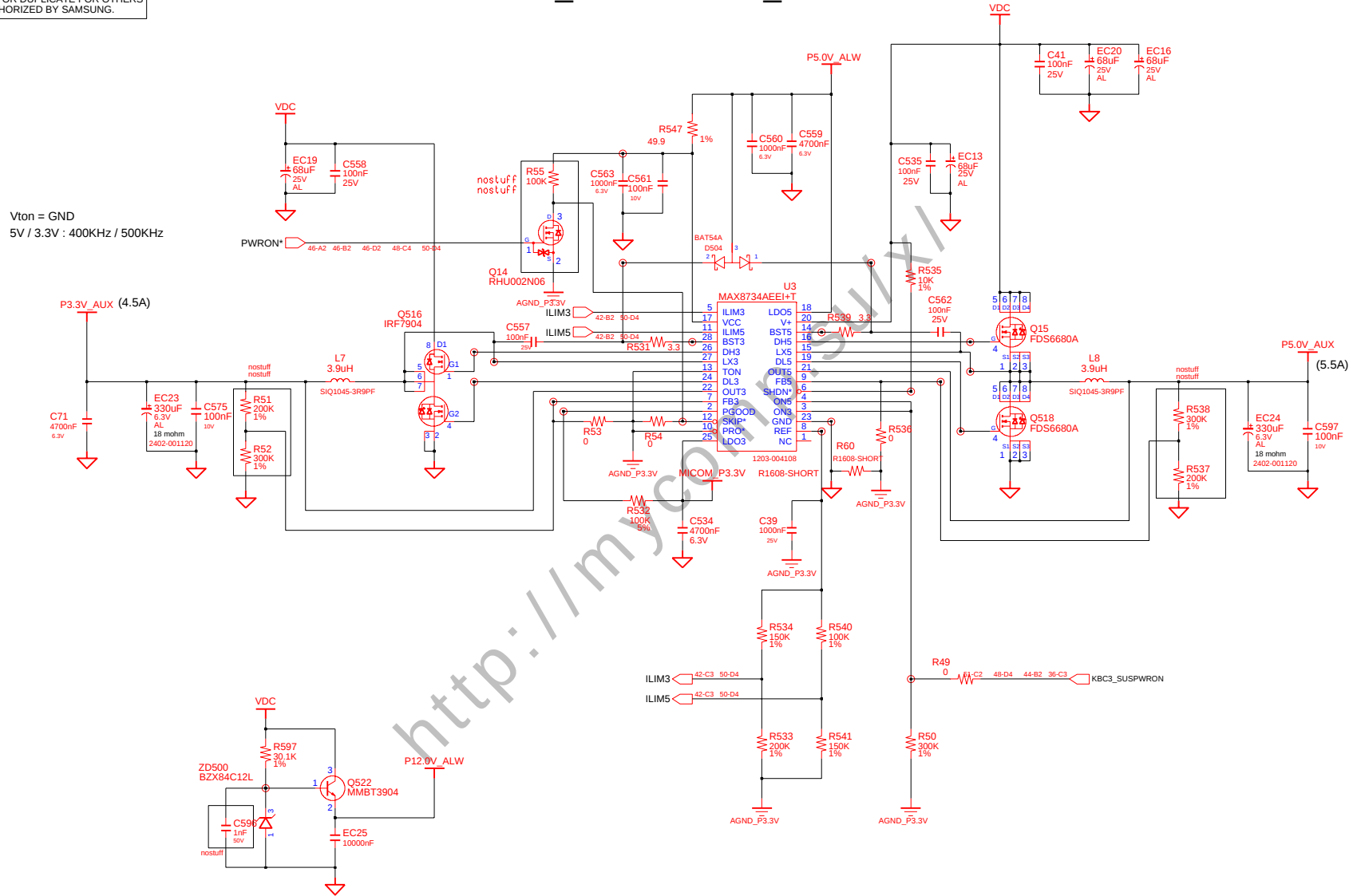


|             |            |           |           |       |                          |  |             |             |
|-------------|------------|-----------|-----------|-------|--------------------------|--|-------------|-------------|
| DRAW        | TERMI KWON | DATE      | 4/5/2006  | TITLE | FIRENZE II               |  | SAMSUNG     |             |
| CHECK       | HJ KIM     | DEV. STEP | SR        |       | MAIN                     |  | ELECTRONICS |             |
| APPROVAL    | SJ PARK    | REV       | 1.0       |       | CHARGER                  |  | PART NO.    | BA41-00659A |
| MODULE CODE | undefined  |           | LAST EDIT |       | April 5, 2006 8:18:08 PM |  | PAGE        | 41 OF 52    |

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# P3.3V\_AUX & P5.0V\_AUX

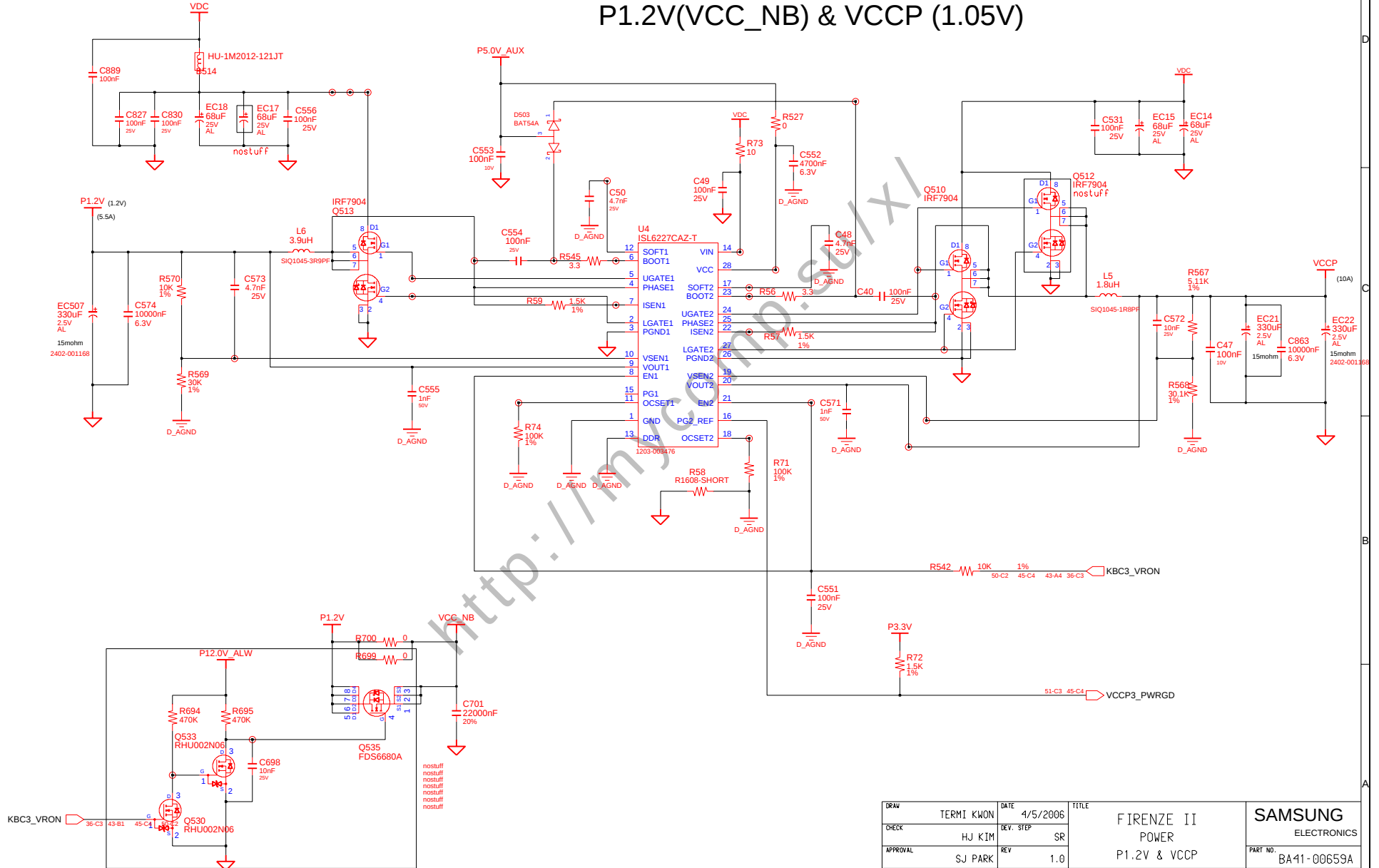
Vton = GND  
5V / 3.3V : 400KHz / 500KHz



|             |            |           |          |           |                          |                        |
|-------------|------------|-----------|----------|-----------|--------------------------|------------------------|
| DRAW        | TERMI KWON | DATE      | 4/5/2006 | TITLE     | FIRENZE II<br>POWER      | SAMSUNG<br>ELECTRONICS |
| CHECK       | HJ KIM     | DEV. STEP | SR       | REV       | 1.0                      | PART NO. BA41-00659A   |
| APPROVAL    | SJ PARK    | REV       | 1.0      | LAST EDIT | April 5, 2006 8:18:08 PM | PAGE 42 OF 52          |
| MODULE CODE | undefined  |           |          |           |                          |                        |

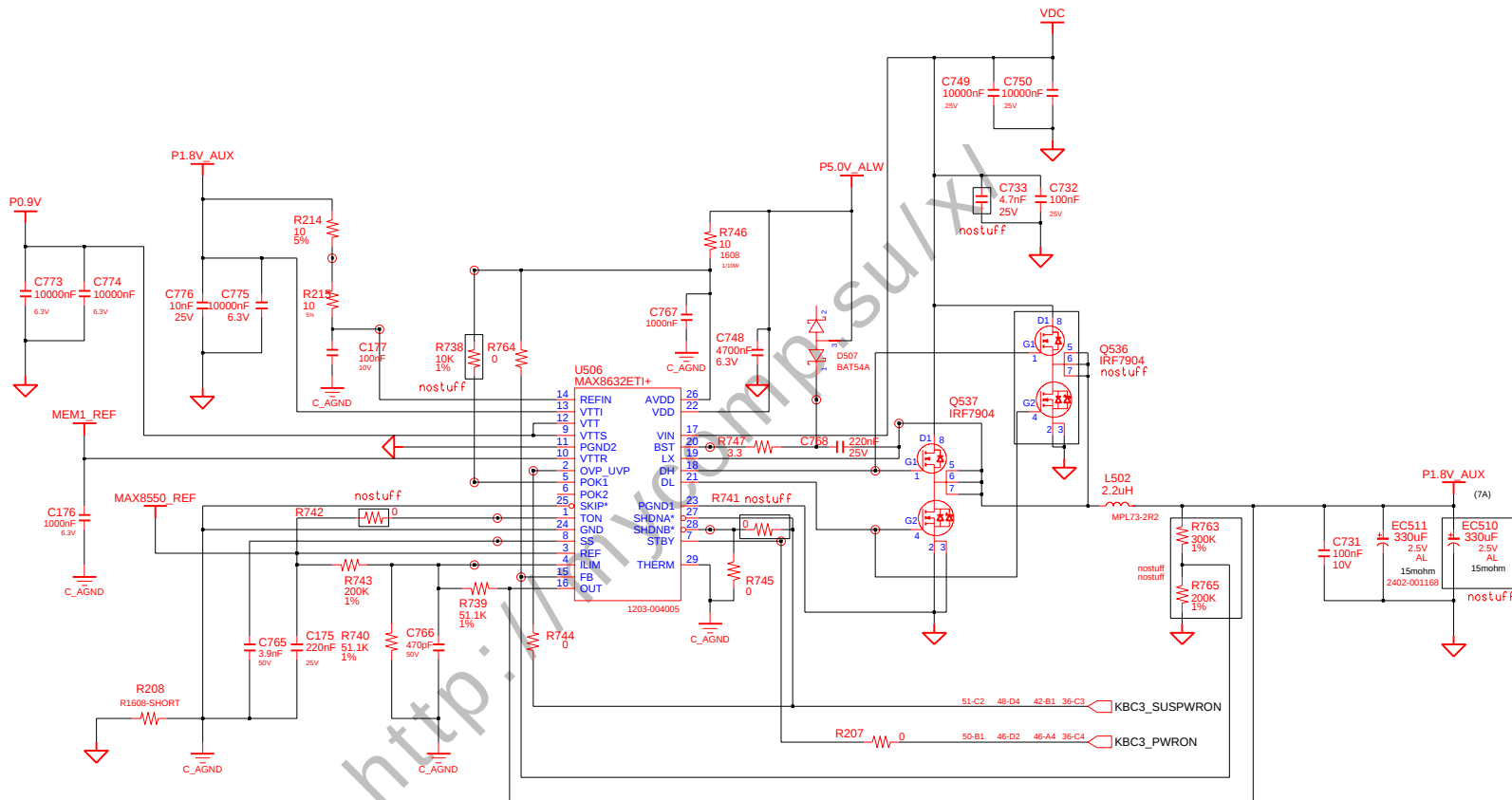
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## P1.2V(VCC\_NB) & VCCP (1.05V)



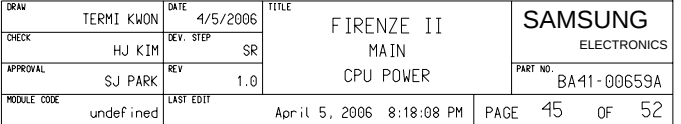
|             |            |           |          |                          |                                     |                         |
|-------------|------------|-----------|----------|--------------------------|-------------------------------------|-------------------------|
| DRAW        | TERMI KWON | DATE      | 4/5/2006 | TITLE                    | FIRENZE II<br>POWER<br>P1.2V & VCCP | SAMSUNG<br>ELECTRONICS  |
| CHECK       | HJ KIM     | REV. STEP | SR       |                          |                                     | PART NO.<br>BA41-00659A |
| APPROVAL    | SJ PARK    | REV       | 1.0      |                          |                                     |                         |
| MODULE CODE | undefined  | LAST EDIT |          | April 5, 2006 8:18:08 PM | PAGE                                | 43 OF 52                |

# DDR2 Power



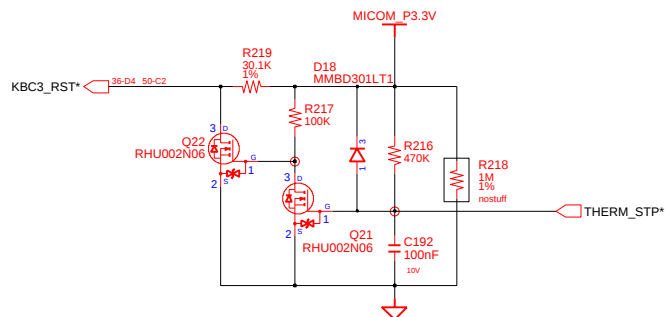
|             |            |           |          |                          |                                 |                         |
|-------------|------------|-----------|----------|--------------------------|---------------------------------|-------------------------|
| DRAW        | TERMI KWON | DATE      | 4/5/2006 | TITLE                    | FIRENZE II<br>MAIN<br>DDR POWER | SAMSUNG<br>ELECTRONICS  |
| CHECK       | HJ KIM     | DEV. STEP | SR       |                          |                                 | PART NO.<br>BA41-00659A |
| APPROVAL    | SJ PARK    | REV       | 1.0      |                          |                                 |                         |
| MODULE CODE | undefined  | LAST EDIT |          | April 5, 2006 8:18:08 PM | PAGE                            | 44 OF 52                |

CPU VRM [SEMTECH]

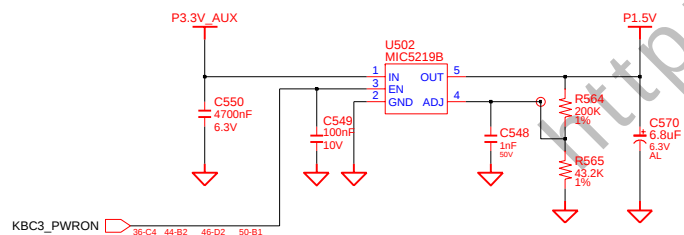


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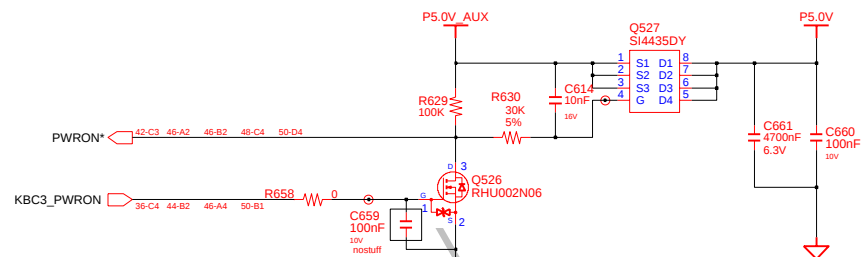
## MICOM RESET



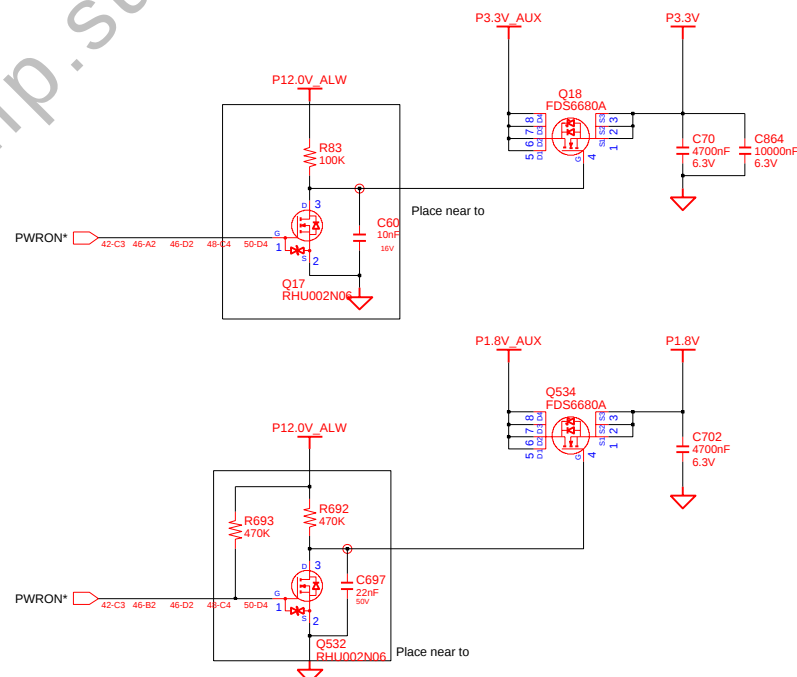
## P1.5V POWER



## Switched Power On (P5V)

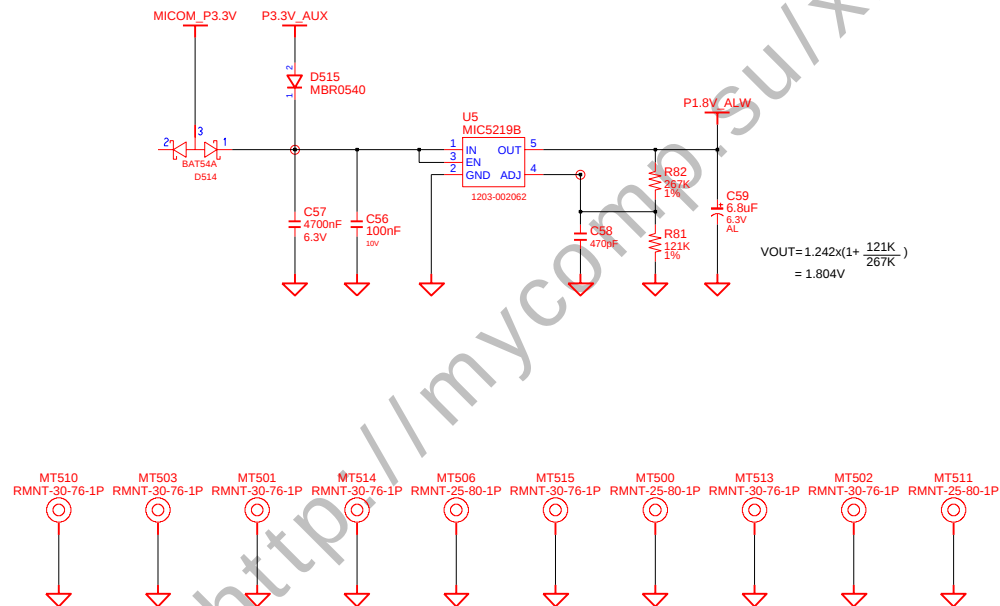


## Switched Power On (P3.3V & 1.8V)



|             |            |           |          |                          |                        |                        |
|-------------|------------|-----------|----------|--------------------------|------------------------|------------------------|
| DRAWN       | TERMI KWON | DATE      | 4/5/2006 | TITLE                    | FIRENZE II             | SAMSUNG<br>ELECTRONICS |
| CHECK       | HJ KIM     | REV.      | STEP     | SR                       | MAIN                   |                        |
| APPROVAL    | SJ PARK    | REV       | 1.0      |                          | MICOM & SWITCHED POWER |                        |
| MODULE CODE | undefined  | LAST EDIT |          |                          |                        |                        |
|             |            |           |          | April 5, 2006 8:18:08 PM | PAGE                   | 46 OF 52               |

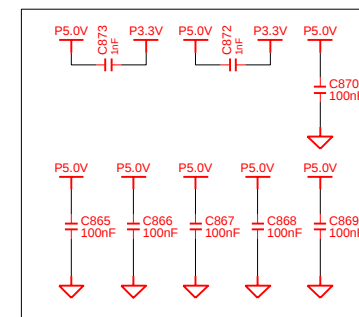
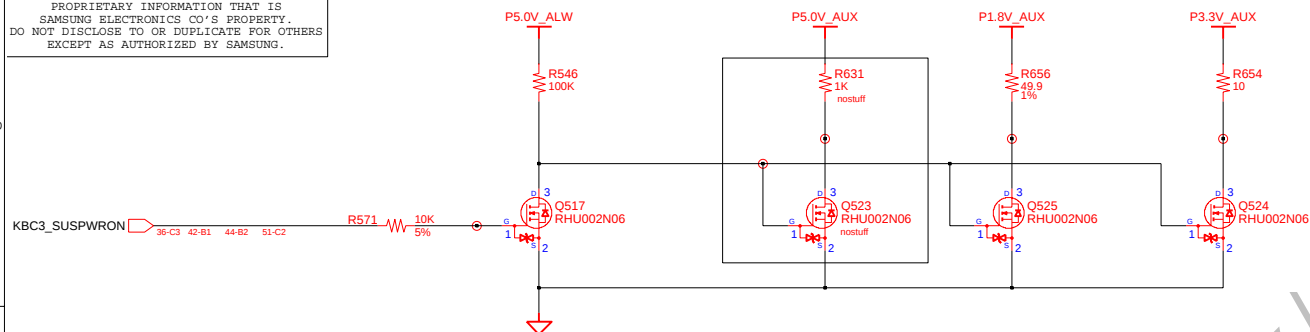
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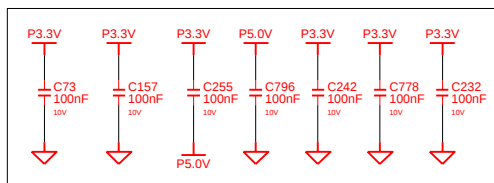
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|-------------|------------|-----------|--------------------------|-------------------------|----------------------|---------------------|
| DRAW        | TERMI KWON | DATE      | 4/5/2006                 | TITLE                   | FIRENZE II           | SAMSUNG ELECTRONICS |
| CHECK       | HJ KIM     | DEV. STEP | SR                       |                         |                      |                     |
| APPROVAL    | SJ PARK    | REV       | 1.0                      | P1.2V & P2.5V AUX POWER | PART NO. BA41-00659A |                     |
| MODULE CODE | undefined  | LAST EDIT | April 5, 2006 8:18:08 PM | PAGE                    | 47                   | OF 52               |

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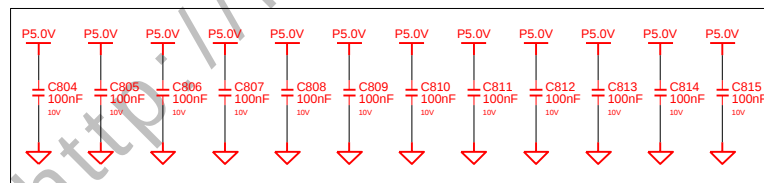
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To enhance DMB performance(060206)

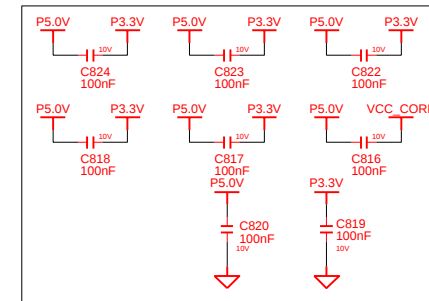


STICHING CAP

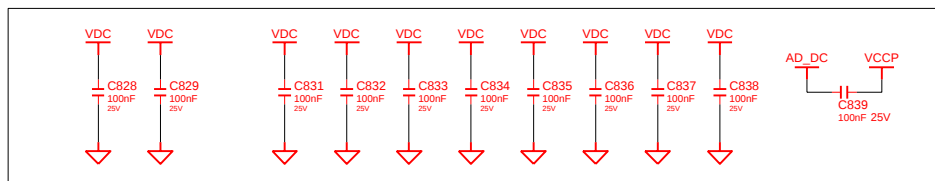


Decap for P5.0V Plane

To reduce BB noise(120 ~ 230MHz) from Power Line (2006/01/24 relate on EMI)



Stiching Cap for Power partition  
To reduce BB noise(120 ~ 230MHz) from Power Partition points (2006/01/24 relate on EMI)



Decap for VDC

To reduce BB noise(120 ~ 230MHz) from Power Line (2006/01/24 relate on EMI)

|             |            |           |                          |       |                                     |                        |
|-------------|------------|-----------|--------------------------|-------|-------------------------------------|------------------------|
| DRAW        | TERMI KWON | DATE      | 4/5/2006                 | TITLE | FIRENZE II<br>MAINBD<br>POWER ADAPT | SAMSUNG<br>ELECTRONICS |
| CHECK       | HJ KIM     | DEV. STEP | SR                       |       |                                     | PART NO.               |
| APPROVAL    | SJ PARK    | REV       | 1.0                      |       |                                     | BA41-00659A            |
| MODULE CODE | undefined  | LAST EDIT | April 5, 2006 8:18:08 PM | PAGE  | 48                                  | OF 52                  |

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| PCB REVISION CONTROL (ICT) |            |               |          |      |
|----------------------------|------------|---------------|----------|------|
| NO                         | CONNECTION | DATE(Y/MM/DD) | REVISION | STEP |
| 1                          | N.C.       |               |          |      |
| 2                          | 1-2        |               |          |      |
| 3                          | 2-3        |               |          |      |
| 4                          | 3-1        |               |          |      |
| 5                          | 1-2-3      |               |          |      |
| 6                          | N.C.       |               |          |      |
| 7                          | 1-2        |               |          |      |
| 8                          | 2-3        |               |          |      |
| 9                          | 3-1        |               |          |      |
| 10                         | 1-2-3      |               |          |      |

REV500

10

20 03

|             |           |           |                          |    |                               |             |
|-------------|-----------|-----------|--------------------------|----|-------------------------------|-------------|
| DRAW        |           | DATE      | TITLE                    |    | <b>SAMSUNG</b><br>ELECTRONICS |             |
| TERMI KWON  |           | 4/5/2006  | FIRENZE II               |    |                               |             |
| CHECK       | HJ KIM    | REV. SFEF | SR                       |    |                               |             |
| APPROVAL    | SJ PARK   | REV       | 1.0                      | TP | PART NO.                      | BA41-00659A |
| MODULE CODE | LAST EDIT |           | April 5, 2006 8:18:08 PM |    | PAGE                          | 49 OF 52    |

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○C0EX1  
○C0EX2  
○ILIM3  
○ILIM5  
○MIC1\_L  
○MIC1\_R  
○PWRON\*  
○TV03\_C  
○TV03\_Y  
○IDES\_A0  
○IDES\_A1  
○IDES\_A2  
○ODDS\_A0  
○ODDS\_A1  
○ODDS\_A2  
○PC\_BEEP  
○RTC\_CLK  
○AC\_SDOOUT  
○ADT3\_SEL  
○AUTO\_ON\*

○CPU1\_ICK  
○CPU1\_ID1  
○CPU1\_TMS  
○CRT3\_RED

○HP\_OUT\_L  
○HP\_OUT\_R

○CLK3\_I0H14  
○CLK3\_IN14M  
○CLK3\_USB48

○CRT3\_BLUE  
○HDD3\_LED\*  
○IDES\_CS1\*  
○IDES\_CS3\*  
○IDES\_D(0)  
○IDES\_D(1)  
○IDES\_D(2)  
○IDES\_D(3)  
○IDES\_D(4)  
○IDES\_D(5)  
○IDES\_D(6)  
○IDES\_D(7)  
○IDES\_D(8)  
○IDES\_D(9)  
○IDES\_DREQ  
○IDES\_IOR\*  
○IDES\_IOW\*  
○KBC3\_A20G  
○KBC3\_RST\*  
○KBC3\_VRON  
○KBC5\_TCLK  
○LAN3\_ACT\*

○ODDS\_IRO  
○PC13\_PAR  
○SMB3\_CLK

○CBS3\_CCLK  
○CBS3\_CPAR  
○CBS3\_CVS1  
○CBS3\_CVS2  
○CBS3\_SPKR  
○CHP3\_SPKR  
○CLK3\_FM48

○ODDS\_CS1\*  
○ODDS\_CS3\*  
○ODDS\_D(0)  
○ODDS\_D(1)  
○ODDS\_D(2)  
○ODDS\_D(3)  
○ODDS\_D(4)  
○ODDS\_D(5)  
○ODDS\_D(6)  
○ODDS\_D(7)  
○ODDS\_D(8)  
○ODDS\_D(9)  
○ODDS\_DREQ  
○ODDS\_IOR\*  
○ODDS\_IOW\*  
○ODDS\_RST\*  
○PC13\_CLK8  
○PC13\_RST\*  
○SMB3\_DATA  
○VGAS\_DDC  
○VGAS\_DDCD  
○WLAN\_LED\*  
○AUD3\_EAPD  
○CBS3\_A\_D2  
○CBS3\_CCD1\*  
○CBS3\_CCD2\*  
○CBS3\_CGNT\*  
○CBS3\_CGNT\*  
○CBS3\_CGNT\*  
○CBS3\_CGNT\*  
○CBS3\_CGNT\*  
○CBS3\_CGNT\*

○CRT3\_GREEN  
○CRT5\_HSYNC  
○CRT5\_VSYNC  
○FWH1\_INIT\*  
○IDES\_D(10)  
○IDES\_D(11)  
○IDES\_D(12)  
○IDES\_D(13)  
○IDES\_D(14)  
○IDES\_D(15)  
○IDES\_DACK\*  
○IDES\_DASP\*  
○IDES\_IORDY  
○JCK\_SENS\_A  
○KBC3\_CHGEN  
○KBC3\_PWRON  
○KBC3\_PWRON  
○KBC5\_TDATA

○LAN3\_WAKE\*  
○LCD3\_VDDEN  
○LINE\_OUT\_L  
○LINE\_OUT\_R

○ODDS\_D(10)  
○ODDS\_D(11)  
○ODDS\_D(12)  
○ODDS\_D(13)  
○ODDS\_D(14)  
○ODDS\_D(15)  
○ODDS\_DACK\*  
○ODDS\_IORDY  
○PC13\_AD(0)  
○PC13\_AD(1)  
○PC13\_AD(2)  
○PC13\_AD(3)

|             |            |           |          |                          |                      |                        |
|-------------|------------|-----------|----------|--------------------------|----------------------|------------------------|
| DRAW        | TERMI KWON | DATE      | 4/5/2006 | TITLE                    | FIRENZE II           | SAMSUNG<br>ELECTRONICS |
| CHECK       | HJ KIM     | DEV. STEP | SR       |                          |                      |                        |
| APPROVAL    | SJ PARK    | REV       | 1.0      | TP                       | PART NO. BA41-00659A |                        |
| MODULE CODE |            | LAST EDIT |          | April 5, 2006 8:18:08 PM | PAGE 50 OF 52        |                        |

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[illegible]

- VCC\_CORE
- VCC\_CORE
- VCC\_CORE
- VCC\_CORE
- VCC\_CORE

