

Service Manual



Service Manual

LG-C305



Model : LG-C305

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1. INTRODUCTION

1.1 Purpose

This manual provides the information necessary to repair, calibration, description and download the features of this model.

1.2 Regulatory Information

A. Security

Toll fraud, the unauthorized use of telecommunications system by an unauthorized part (for example, persons other than your company's employees, agents, subcontractors, or person working on your company's behalf) can result in substantial additional charges for your telecommunications services. System users are responsible for the security of own system. There are may be risks of toll fraud associated with your telecommunications system. System users are responsible for programming and configuring the equipment to prevent unauthorized use. The manufacturer does not warrant that this product is immune from the above case but will prevent unauthorized use of common-carrier telecommunication service of facilities accessed through or connected to it.

The manufacturer will not be responsible for any charges that result from such unauthorized use.

B. Incidence of Harm

If a telephone company determines that the equipment provided to customer is faulty and possibly causing harm or interruption in service to the telephone network, it should disconnect telephone service until repair can be done. A telephone company may temporarily disconnect service as long as repair is not done.

C. Changes in Service

A local telephone company may make changes in its communications facilities or procedure. If these changes could reasonably be expected to affect the use of the this phone or compatibility with the network, the telephone company is required to give advanced written notice to the user, allowing the user to take appropriate steps to maintain telephone service.

D. Maintenance Limitations

Maintenance limitations on this model must be performed only by the manufacturer or its authorized agent. The user may not make any changes and/or repairs expect as specifically noted in this manual. Therefore, note that unauthorized alternations or repair may affect the regulatory status of the system and may void any remaining warranty.

1. INTRODUCTION

E. Notice of Radiated Emissions

This model complies with rules regarding radiation and radio frequency emission as defined by local regulatory agencies. In accordance with these agencies, you may be required to provide information such as the following to the end user.

F. Pictures

The pictures in this manual are for illustrative purposes only; your actual hardware may look slightly different.

G. Interference and Attenuation

Phone may interfere with sensitive laboratory equipment, medical equipment, etc. Interference from unsuppressed engines or electric motors may cause problems.

H. Electrostatic Sensitive Devices

ATTENTION

Boards, which contain Electrostatic Sensitive Device (ESD), are indicated by the sign. Following information is ESD handling:



- Service personnel should ground themselves by using a wrist strap when exchange system boards.
- When repairs are made to a system board, they should spread the floor with anti-static mat which is also grounded.
- Use a suitable, grounded soldering iron.
- Keep sensitive parts in these protective packages until these are used.
- When returning system boards or parts like EEPROM to the factory, use the protective package as described.

1.3 Abbreviations

For the purposes of this manual, following abbreviations apply:

APC	Automatic Power Control
BB	Baseband
BER	Bit Error Ratio
CC-CV	Constant Current – Constant Voltage
DAC	Digital to Analog Converter
DCS	Digital Communication System
dBm	dB relative to 1 milli watt
DSP	Digital Signal Processing
EEPROM	Electrical Erasable Programmable Read-Only Memory
ESD	Electrostatic Discharge
FPCB	Flexible Printed Circuit Board
GMSK	Gaussian Minimum Shift Keying
GPIO	General Purpose Interface Bus
GSM	Global System for Mobile Communications
IPUI	International Portable User Identity
IF	Intermediate Frequency
LCD	Liquid Crystal Display
LDO	Low Drop Output
LED	Light Emitting Diode
OPLL	Offset Phase Locked Loop

1. INTRODUCTION

PAM	Power Amplifier Module
PCB	Printed Circuit Board
PGA	Programmable Gain Amplifier
PLL	Phase Locked Loop
PSTN	Public Switched Telephone Network
RF	Radio Frequency
RLR	Receiving Loudness Rating
RMS	Root Mean Square
RTC	Real Time Clock
SAW	Surface Acoustic Wave
SIM	Subscriber Identity Module
SLR	Sending Loudness Rating
SRAM	Static Random Access Memory
PSRAM	Pseudo SRAM
STMR	Side Tone Masking Rating
TA	Travel Adapter
TDD	Time Division Duplex
TDMA	Time Division Multiple Access
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator
VCTCXO	Voltage Control Temperature Compensated Crystal Oscillator
WAP	Wireless Application Protocol

2. PERFORMANCE

2.1 H/W Features

Item	Feature	Comment
Standard Battery	Li-ion, 3.7V 900mAh	
Talk time	Up to 8 hrs : GSM850 & EGSM,TX Level : 10	
Stand by time	Up to 500 hrs : Paging Period 9	
Charging time	Under 3 hrs	
RX Sensitivity	GSM, EGSM: -109dBm, DCS: -109dBm	c
TX output power	GSM, EGSM: 33 dBm(Level 5), DCS , PCS: 30 dBm(Level 0)	
GPRS compatibility	Class 12	
SIM card type	3.0V / 1.8V	
Display	MAIN : 2.4" TFT 240 × 320 QVGA	
Status Indicator	Hard icons. Key Pad (Qwerty) A ~ Z, 0 ~ 9, #, *, Up/Down Left/Right OK Key Send Key, PWR Key, Soft Key (Left/Right), Side key (Volume Up/Volume Down)	
ANT	Internal type (QUAD band)	
EAR Phone Jack	Yes (Stereo)	
PC Synchronization	Yes	
Speech coding	EFR/FR/HR/NB-AMR	
Data and Fax	Yes	
Vibrator	Yes	
Loud Speaker	Yes	
Voice Recoding	Yes	
Microphone	Yes	

2. PERFORMANCE

Item	Feature	Comment
Speaker/Receiver	Speaker DIS 16 mm, 3.4T spring / Receiver 1207*2.5T	
Travel Adapter	Yes	
MIDI	SW decoded max. 32 poly	
Camera	2.0 Mpxls, FF	
FM Radio	87.5 ~ 108MHz supported	
Bluetooth / WLAN	BT 2.1 + EDR / WLAN IEEE 802.11b/g/n	

2.2 Technical Specification

Item	Description	Specification					
1	Frequency Band	GSM850 TX: 824 ~ 849 MHz RX: 869 ~ 894 MHz DCS TX: 1710 ~ 1785 MHz RX: 1805 ~ 1880 MHz PCS TX: 1850 ~ 1910 MHz RX: 1930 ~ 1990 MHz					
2	Phase Error	RMS < 5 degrees Peak < 20 degrees					
3	Frequency Error	< 0.1 ppm					
4	Power Level	GSM850/EGSM					
		Level	Power	Toler.	Level	Power	Toler.
		5	33dBm	±2dB	13	17dBm	± 3dB
		6	31dBm	±3dB	14	15dBm	± 3dB
		7	29dBm	±3dB	15	13dBm	± 3dB
		8	27dBm	±3dB	16	11dBm	± 5dB
		9	25dBm	±3dB	17	9dBm	± 5dB
		10	23dBm	±3dB	18	7dBm	± 5dB
		11	21dBm	±3dB	19	6dBm	± 5dB
		12	19dBm	±3dB			
		DCS/PCS					
		Level	Power	Toler.	Level	Power	Toler.
		0	30dBm	±2dB	8	14dBm	± 3dB
		1	28dBm	±3dB	9	12dBm	± 4dB
		2	26dBm	±3dB	10	10dBm	± 4dB
		3	24dBm	±3dB	11	8dBm	± 4dB
		4	22dBm	±3dB	12	6dBm	± 4dB
		5	20dBm	±3dB	13	4dBm	± 4dB
		6	18dBm	±3dB	14	2dBm	± 5dB
		7	16dBm	±3dB	15	0dBm	± 5dB

2. PERFORMANCE

Item	Description	Specification	
5	Output RF Spectrum (due to modulation)	GSM850/ EGSM	
		Offset from Carrier (kHz).	Max. dBc
		100	+0.5
		200	-30
		250	-33
		400	-60
		600~ <1,200	-60
		1,200~ <1,800	-60
		1,800~ <3,000	-63
		3,000~ <6,000	-65
		6,000	-71
		DCS/PCS	
		Offset from Carrier (kHz).	Max. dBc
		100	+0.5
		200	-30
		250	-33
		400	-60
		600~ <1,200	-60
		1,200~ <1,800	-60
		1,800~ <3,000	-65
		3,000~ <6,000	-65
		6,000	-73
6	Output RF Spectrum (due to switching transient)	GSM850/ EGSM	
		Offset from Carrier (kHz).	Max. dBm
		400	-19
		600	-21
		1,200	-21
		1,800	-24

2. PERFORMANCE

Item	Description	Specification		
6	Output RF Spectrum (due to switching transient)	DCS/PCS		
		Offset from Carrier (kHz).		Max. dBm
		400		-22
		600		-24
		1,200		-24
		1,800		-27
7	Spurious Emissions	Conduction, Emission Status		
8	Bit Error Ratio	GSM850, EGSM BER (Class II) < 2.439% @-102 dBm DCS,PCS BER (Class II) < 2.439% @-102 dBm		
9	RX Level Report Accuracy	±3 dB		
10	SLR	15±3 dB		
11	Sending Response	Frequency (Hz)	Max.(dB)	Min.(dB)
		100	-12	-
		200	0	-
		300	0	-12
		1,000	0	-6
		2,000	4	-6
		3,000	4	-6
		3,400	4	-9
		4,000	0	-
12	RLR	4±3 dB		

2. PERFORMANCE

Item	Description	Specification		
13	Receiving Response	Frequency (Hz)	Max.(dB)	Min.(dB)
		100	-12	-
		200	0	-
		300	2	-7
		500	*	-5
		1,000	0	-5
		3,000	2	-5
		3,400	2	-10
		4,000	2	
		* Mean that Adopt a straight line in between 300 Hz and 1,000 Hz to be Max. level in the range.		
14	STMR	17 ± 5 dB		
15	Stability Margin	> 6 dB		
16	Distortion	dB to ARL (dB)		Level Ratio (dB)
		-35		17.5
		-30		22.5
		-20		30.7
		-10		33.3
		0		33.7
		7		31.7
		10		25.5
17	Side Tone Distortion	Three stage distortion < 10%		
18	System frequency (13 MHz) tolerance	≤ 2.5 ppm		
19	32.768KHz tolerance	≤ 30 ppm		
20	Ringer Volume	At least 55 dBspl under below conditions: 1. Ringer set as ringer. 2. Test distance set as 1 m		

2. PERFORMANCE

Item	Description	Specification	
21	Charge Current	Constant Charge Current : <. 400 mA Total Charging Time : < 3 hours (Battery 900mA)	
22	Antenna Display	Bar Number	Power
		7	-92 Max.
		7 -> 5	-93 $\pm$ 3
		5 -> 4	-98 $\pm$ 3
		4 -> 2	-101 $\pm$ 3
		2 -> 1	-104 $\pm$ 3
		1 -> 0	-106 $\pm$ 3
		0 -> OFF	-106 Min.
23	Battery Indicator	Battery Bar Number	Voltage
		3	$\geq 3.73 \pm 0.05$ V
		3 -> 2	3.61 ± 0.05 V
		2 -> 1	3.46 ± 0.05 V
		1 -> 0	3.35 ± 0.05 V
24	Low Voltage Warning (Blinking Bar)	$\leq 3.46 \pm 0.05$ V (Call), 1 time per 1 minute (Receiver)	
		$\leq 3.46 \pm 0.05$ V (Standby), 1 time per 3 minutes(Speaker)	
25	Forced shut down Voltage	3.35 ± 0.05 V	
26	Sustain RTC without battery	Over 50 hours	
27	Battery Type	Lithium-Ion Battery, Inner pack Standard Voltage = 3.7 V Battery full charge voltage = 4.2 V Capacity: 900mAh	
28	Travel Charger	Switching-mode charger Input: 100 ~ 240V, 50/60 Hz Output: 4.8V, 700mA	

3. TECHNICAL BRIEF

3. TECHNICAL BRIEF

3.1 Digital Main Processor

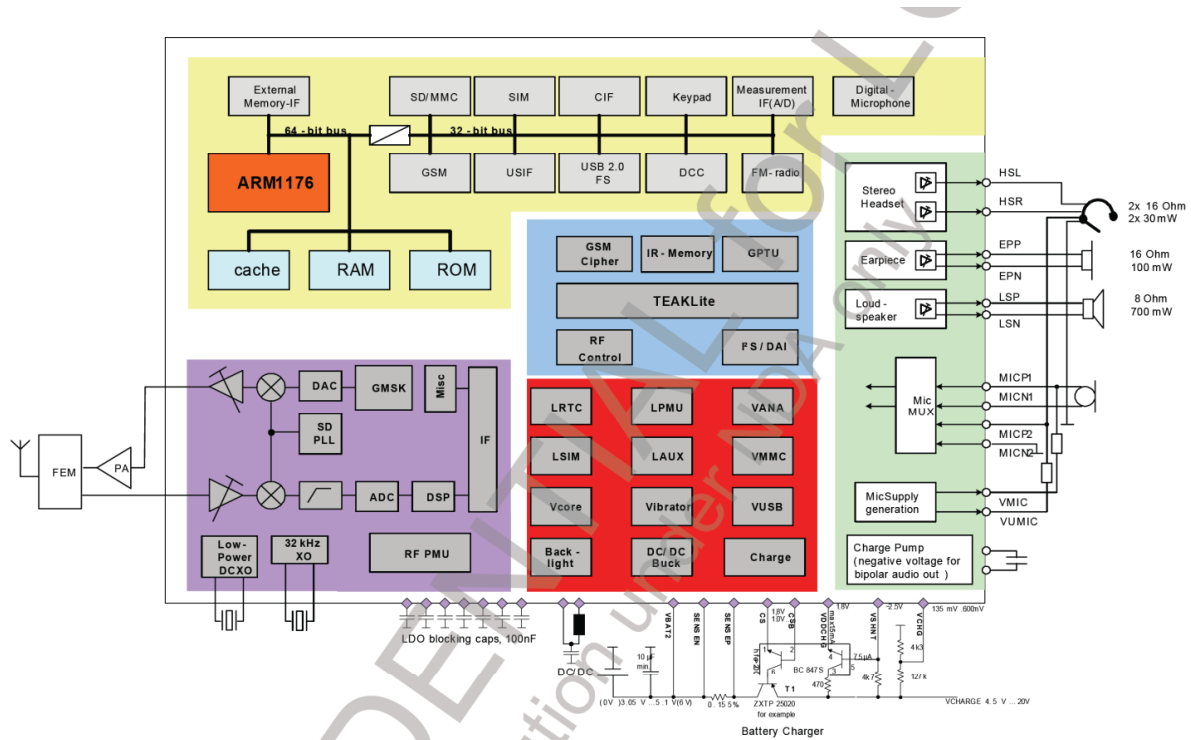


Figure. 3.1.1 X-Gold tm 213 Hardware Block Diagram

3.1.1 General

- Technology:
 - SoC, Monolithic, 65 nm CMOS
- Package:
 - eWLB, 8x8x0.8 mm
 - 0.5 mm pitch
 - 217 balls / 6-layer PCB

3.1.2 RF Transceiver

- Dual-band direct conversion receiver
- Tri/Quad-band possible with external circuitry
- Fully integrated digital controlled XO
- Additional buffer for 2 external system clocks
- Fully digital RF-Synthesizer incl. $\Sigma\Delta$ -Transmitter

3.1.3 Baseband

- DSP:
 - 156 MHz TeakLite™
- MCU:
 - ARM1176® @ 208 MHz
- MCU RAM:
 - 3.00Mbit
- Memory I/F:
 - 512 Mbit
- Modem:
 - GPRS class 12, (RX/TX CS1-CS4)
 - EGPRS class 12, (RX MCS1-MCS9, TX MCS1-MCS4)
- Cipher Units:
 - A51/2/3
 - GEA-1/2/3
- Security:
 - OMTP TR0
 - Secure Boot
 - RSA(ROM)/SHA-1(HW accel.)
 - OCDS disabling
 - Certificate Management

3. TECHNICAL BRIEF

- Speech Codec:
 - FR / HR / EFR / NB-AMR
- Audio Codec (running on ARM1176):
 - SP-MIDI
 - SB-ADPCM
 - MP3
 - WB-AMR
 - AAC/AAC+/eAAC+
- Others:
 - DARP (SAIC)
 - TTY
- Customization:
 - E-Fuses

3.1.4 External Memory

- External Bus Unit
 - 25-bit address bus (512 Mbit)
 - 16-bit data bus
 - 1.8V & 2.8V support
- Flash / RAM
 - NOR Type
 - Serial Flash SPI and SPI-4
 - Parallel Flash (Page & Burst Mode)
 - 16-bit Demultiplexed
 - 16-bit AD-multiplexed
 - 16-bit AAD-multiplexed
 - iNAND Type e.g. oneNAND
- Memory card
 - SD/MMC card interface with 1 or 4 data lines

3.1.5 Connectivity

- 3xUSIF (configurable either as SPI or UART), I2C, I2S; Interfaces @ 1.8V
- Direct (U)SIM 1.8/3V
- USB2.0 up to 480 Mbit/s (High Speed) w/ external USB Phy over ULPI interface
- Stereo Headset (Amplifier integrated)
- 3 external analog measurement PIN's
- Bluetooth

3.1.6 Mixed Signal

- Improved audio performance
- Loudspeaker Audio Class D Amplifier, 700 mW@8 Ω mono for hands-free and ringing
- Stereo Headset 2x30 mW@16 Ω w/o coupling C
- Mono Earpiece 100 mW@16 Ω
- Digital microphone supported
- Differential microphone inputs

3.1.7 FM Radio

- Integrated FM radio
 - FM Stereo RDS Receiver
 - Sensitivity 2 μ V EMF
 - Support for US & EU bands
 - Stereo recording

3.1.8 Power Management

- Direct-to-Battery Connection
 - LDOs (incl. capless)
 - DC/DC step-down converter
 - DC/DC step-up for white LED supply
- Battery Type
 - Li-Polymer
- Charging control
 - Battery temperature
 - Watchdog protection
 - Start-up on flat battery
- External Charger
 - Switch mode
- USB battery charging
 - USB charging spec 1.0 compliant
- Backlight
 - Up to 5 serial white LEDs (integrated LDO)

3. TECHNICAL BRIEF

3.1.10 Main LCD Display

- Type
 - 240*320, QVGA, 262k color (parallel)
- Interface
 - Parallel 8bit MIPI-DBI Type B
 - Serial MIPI-DBI Type C
 - Interf. voltage at 1.8V or 2.8V
- gRacr - Display Controller (Hardware)
 - 30 fps Display update without DMA (up to 60 fps) (full or partial)
 - Video post processing Scaling, Rotation (90° steps), Mirroring
 - Overlay with alpha blending
 - Color conversion YUV -> RGB
 - 2D vector graphics (Lines, filled rectangles, Bit block transfer (e.g. sprites, scrolling, antialiased bitmap fonts)

3.1.11 Camera

- 2.0 Mpxls, FF
- Frame Rate : 15@UXGA, 30@SVGA
- 39 MHz Pixel Rate
- 15 fps@2.0 Mpx full resolution

3.1.12 Video Capabilities

- Video Decoding MPEG-4/H.263
 - QCIF@30 fps
 - QVGA@15fps
- Video Encoding MPEG-4/H.263
 - QCIF@15 fps

3.1.13 Audio Capabilities

- Polyphonic ring tones
 - 64 voices MIDI, SP-MIDI
 - FM synthesizer
- AMR-WB
- True ring tones (MP3)
- MP3, eAAC+
- G.722 SB-ADPCM encoding/decoding

3.2 Power Management

A mobile platform requires power supplies for different functions. These power supplies are generated in the integrated power management Unit (PMU). The PMU is designed to deliver the power for a typical standard phone.

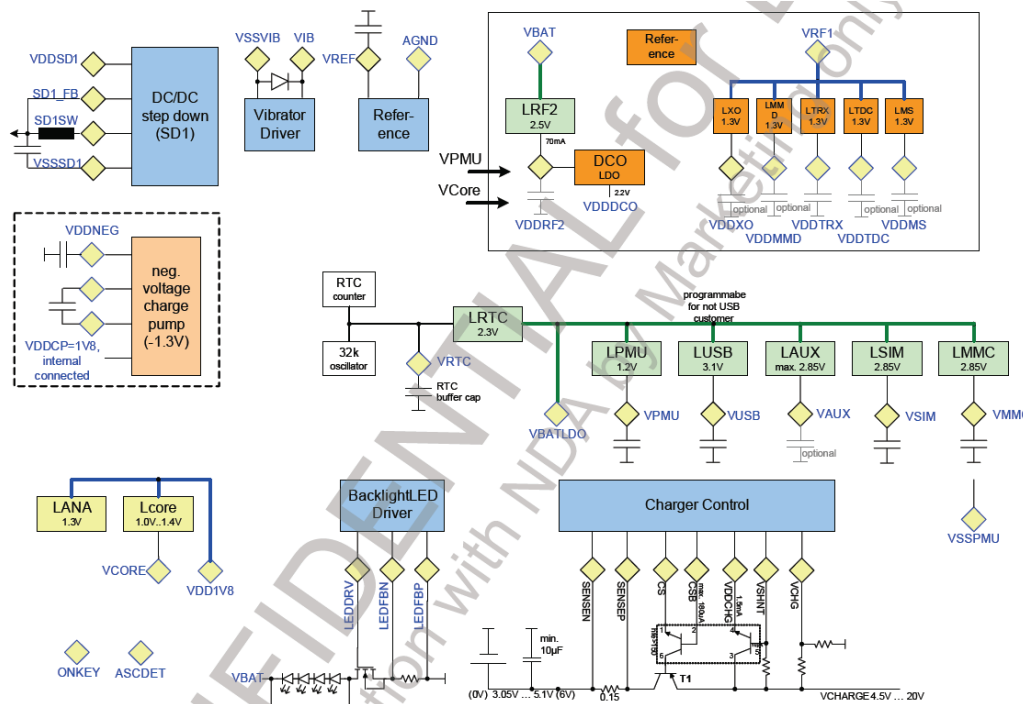


Figure. 3-2-1 Block Figure of the PMU Modules X-Gold tm 213

3. TECHNICAL BRIEF

- **DC/DC Step Down Converter for 1.8V (SD1)**

The DC/DC converter generates a 1.8V supply rail. This voltage rail is used to supply main parts of the system, like the digital core of the chip (via LDO LDCORE), some parts of the mixed signal macro, parts of the RF macro and the external memory if a 1.8V memory is used. The efficiency of the DC/DC converter is optimized for an average load current of 100mA. That is the load current estimated for the GSM talk mode.

- **Linear voltage Regulators (low dropout) LDOs**

The LDOs are used to generate the supply for the different supply domains not directly supplied out of the DC/DC converter.

The VSIM output current is high enough to drive USB SIM cards.

- **LDCORE**

The LDCORE LDO provides the VDCORE supply used for most of the digital parts of the chip

- **LPMU**

The LPMU provides VPMU supply for the PMU supply, e.g. for the startup state machine and analog parts like ADC, sense amplifier etc.

- **LUSB**

The LUSB LDO generates the supply for the USB transceiver (output driver and input). If no USB interface is required, LUSB can be used as general purpose LDO.

- **LAUX**

The LAUX generates VAUX. It is a general purpose LDO and can be used for different functions depending on the phone application, e.g. for the display or Camera.

- **LMMC**

The LMMC generates VMMC. It is a general purpose LDO and can be used e.g. for memory cards

- **LSIM**

The LSIM LDO generates the VSIM supply for the SIM card and interface. It is designed to supply Standard SIM cards.

- **Other LDOs**

The RF module has implemented several LDO's for different RF Power domain.

The mixed signal module has some LDO's for the audio driver and microphone supply.

Supply Domain LDO Name	Voltage	Max. Current	Output Cap	Input Domain	Comment
VBAT	0 ... 6.0 V				Operating range is 3.05 V ... 5.5 V, system emergency switch off voltage is about 2.8 V
VDD1V8	1.8 V	450 mA	22 μ F	VBAT	This voltage is generated by the DC/DC converter with 3.3 μ H inductor, The voltage is used for: Memory supply, and via LDO's for digital core supply, mixed signal supply and RF supply.
LCORE	1.2 V	300 mA	2x100 nF	VDD1V8	
LANA	1.3 V	10 mA	No	VDD1V8	No ball
LRTC	2.3 V	2 mA	≥ 100 nF	VBAT	This supply is only used for the HPBG, the 32.768 kHz oscillator and the real-time clock counter required during the sleep- and low-power mode.
LPMU	1.2 V	15 mA	100 nF	VBAT	Supply for the digital part of the PMU including digital control of DC/DC converter. This voltage is also used for the N-DEMOS driver of DC/DC converter and the class-D amplifier and the core PLL.
LUSB	3.1 V	40 mA	100 nF	VBAT	Used for the USB driver supply or as general purpose LDO with programmable output voltages (2.5 V, 2.85 V, 3.1 V)
LAUX	1.5 V ... 2.85 V	150 mA	470 nF	VBAT	General purpose LDO for e.g. Display, Bluetooth, Camera etc. Programmable output voltages are (1.5 V, 1.8 V, 2.5 V, 2.85 V)
LSIM	1.8 V / 2.85 V	30 mA	≥ 100 nF	VBAT	LDO dedicated to the SIM-Card supply. It is chip internal connected to the SIM interface driver.
LMMC	1.5 V ... 2.85 V	150 mA	≥ 470 nF	VBAT	General purpose LDO, targeted for MMC/SD card supply.
VDDNEG	-1.3 V	100 mA	100 nF	VDD1V8	Negative voltage for the bipolar headset audio driver. Generated by a charge pump.

Table. 3-2-1 Power supply Domains (without RF)

3. TECHNICAL BRIEF

3.2.1 Power on and startup

▪ Analog startup Circuit

Because the POR circuit and the LPBG are directly connected to the battery, it is not possible to switch them off. If the battery voltage exceed the power on reset threshold (2.5V), the power on reset is released, the LPMU regulator and the LRTC voltage regulator are switched on. The LPMU regulator starts in its ultra-low power mode.

The LPMU regulator generates a control signal (lpmu_OK) that enables the 50KHZ PMU oscillator. The output clock of the oscillator is checked with a fully coded counter. A counter overflow releases the reset (vpmu_rst_n) signal for the small PMU state-machine.

▪ Small first digital State-Machine

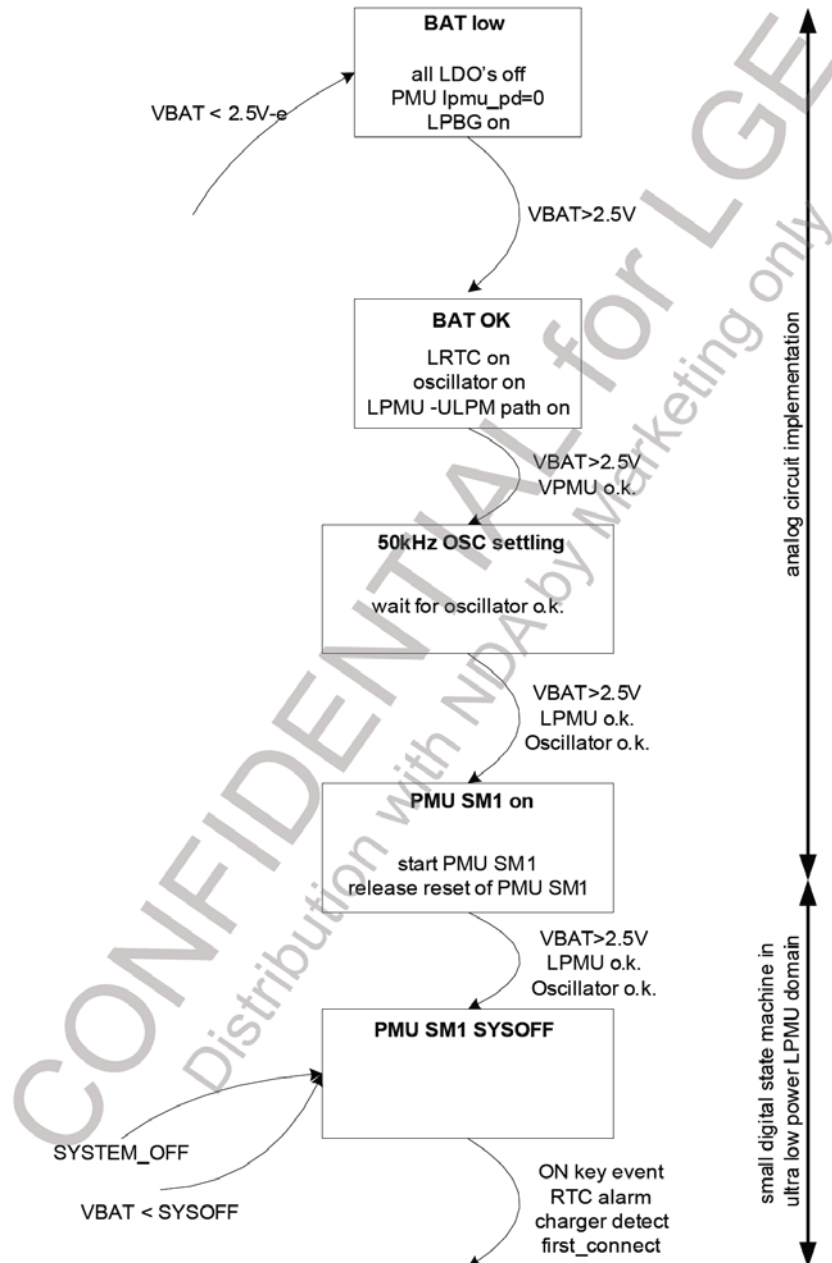
The small PMU state-machine is always connected to VPMU. After starting from reset the small startup state machine enters the SYSTEM OFF state and only continuous the startup procedure if a switch on event like first connect, on-key, wake up or charge detect occurs.

▪ PMU-main State-Machine

The main PMU state-machine is always connected to VPMU also. The power up sequence driven by the PMU state-machine can be seen in Figure18. After enabling the reference (HPGB) and waiting for the settling time, the battery voltage is measured and compared with the power on threshold. If the battery voltage is high enough, the SD1 DC/DC converter and the LCORE LDO are started. A timer ensures that the supply voltage will be stable before the DCXO is enabled. The DCXO settling time is ensured using a fixed timer. After an overflow of this timer, the reset is released for the rest of the system. The PMU state machine remains in this System-ON state until the system is switched into the OFF state. For example the system sleep mode is completely configured by software (for example switching off the LDO's, switching of the DCXO etc.) and controlled by the VCXO_enable signal. The reason for the startup is stored in the ResetSourceRead register.

▪ Battery Measurement

The ADC and the oscillator for the ADC needs the VDD_ADC supply voltage from the LADC LDO. LADC uses either the charger voltage VDD_CHARGE or VDDRTC as input voltage. The input voltage is selected automatically by a bulk switch circuit. LADC, the ADC and the oscillator are enabled on request for every battery measurement if the charger unit is not running. This is handled by an ADC control block in one of the state-machines. If the charger unit is running the ADC is controlled by the charger state-machine



**Figure.3.2.1 First Part of the State Machine,
Running in Different Power Domains than the Second Part**

3. TECHNICAL BRIEF

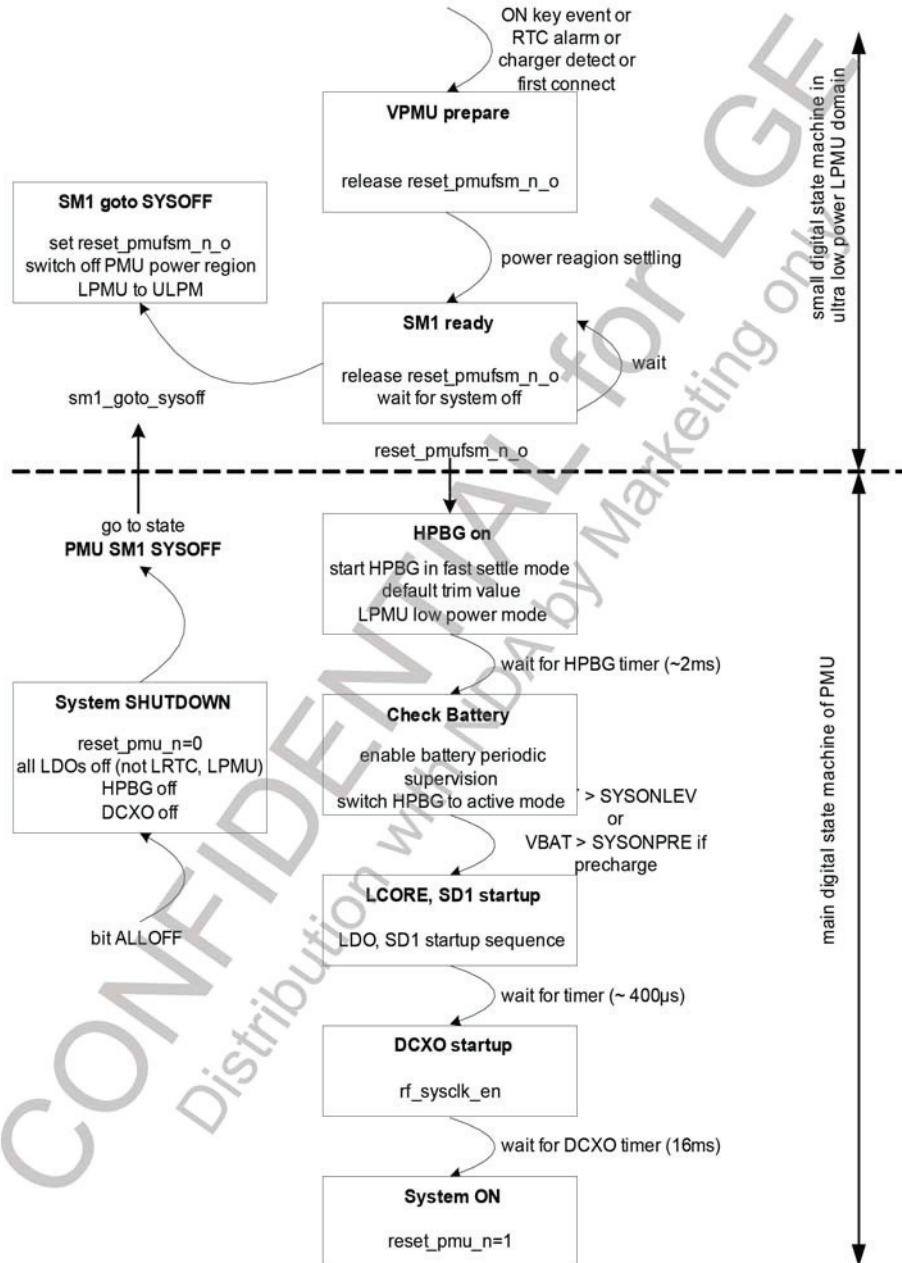


Figure 3.2.2 Second (Main) Part of the Startup State Machine in the VPMU Domain

3.2.2 Switching on due to first connect

If the battery voltage is connected the first time, that means the system enters the first time the SYSOFF state, this is stored in a first connect flag. If the first connect flag is set, the system will start immediately and not wait for any other system on event in the SYSOFF state.

3.2.3 Switching on due to on-Key event

The on key is connected to the ONKEY pad. The ESD protection and the input structure of this pad are connected to VRTC. If the ONKEY pad is forced to VRTC by an external key or similar circuit, the system starts. The ONKEY is sampled with the PMU clock. It has to be sampled four times high before a valid on event is generated. The status of the ON key can be read in the PMU registers, so it can be used as a functional key during phone operation also.

3.2.4 Switching on due to RTC alarm

The real time clock can generate a wakeup signal called RTC alarm. This signal is sampled from the state-machine and after successfully detecting a high, the system is switched on.

3.2.5 Switching on due to charging

When a battery with a voltage below the SSONLEV level is inserted, the state machine will not start the system. As long as the battery voltage stays lower than SYSONLEV the system will stay off. The only possibility to start up the system is due to an external charger.

If an external charger is connected and detected and the battery is charged above the SYSONPRE voltage level the system will start up.

The PMU main state machine waits in the Check battery state until the battery voltage condition is fulfilled. The charger state machine provides the necessary pre-charge indication signal. This pre-charge signal is denounced in a small counter to have a stable signal. This is important, especially in half/full-wave charging where the charger detection is switching between charger detected/not detected according the AC supply frequency. Reasons for details on pre-charging see the charger chapter. The charger is controlled by an independent state machine. The pre-charge signal is used to trigger the pre-charge signal is used to trigger the pre-charge functionality. The charger state machine fully control the pre-charge, the PMU-state machine now changes to state HPBG on state and the system starts. This state change is indicated to the charger state-machine to enable the charger watchdog for safety

3.2.6 Power Supply Start-up sequence

In order to avoid an excessive drop on the battery voltage caused by in-rush current during system power-on, possibly leading to system instability and "hick-ups" a staggered turn-on approach for the regulators is implemented. The regulators are turned on in a well defined sequence, thus spreading the in-rush current transients over time.

The IO's of X-GOLD TM 213 are isolated in OFF mode (core supply is off). The isolation signal is controlled by the PMU state machine. This ensures that the PADs are in a well defined state during core supply settling. This allows to power up the LCORE core regulator and wait for the core to reach reset state before powering up the I/O supply regulators.

3. TECHNICAL BRIEF

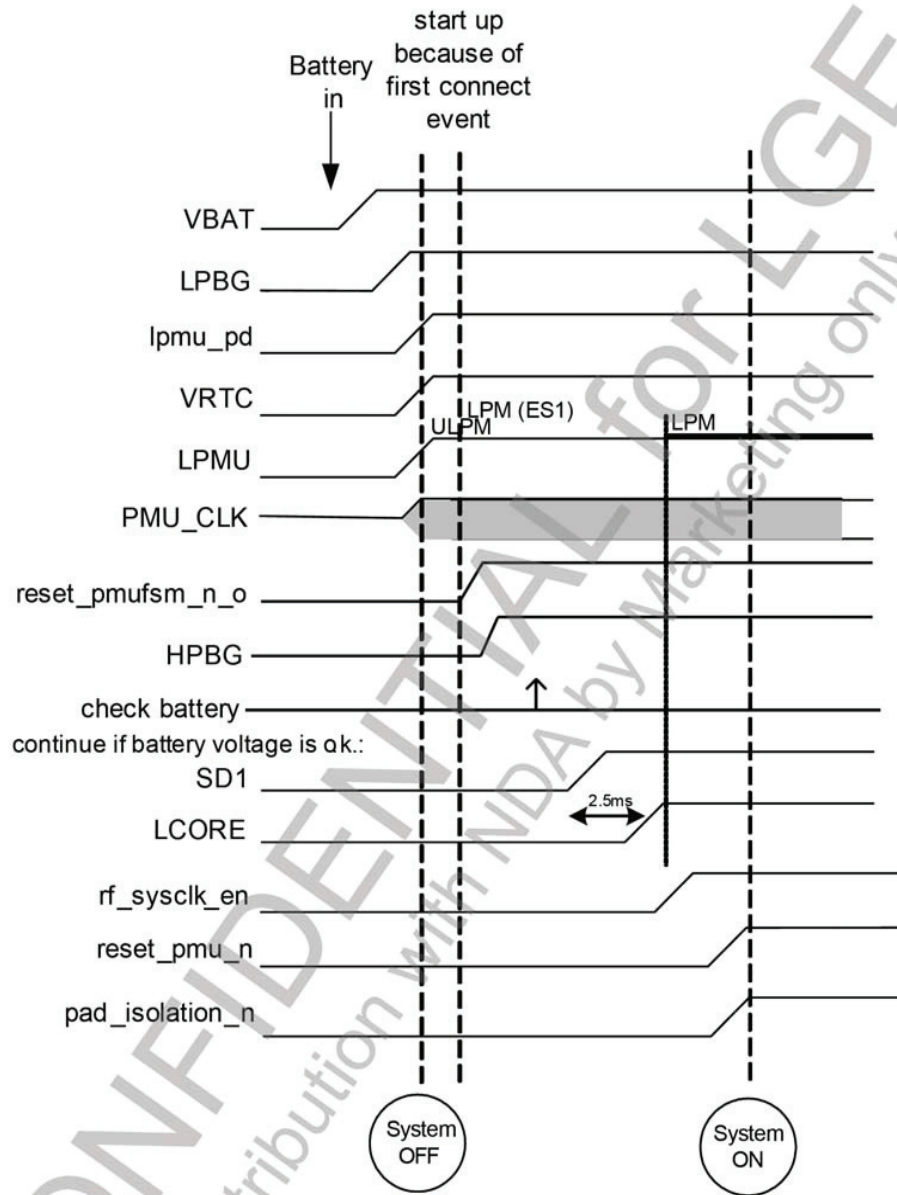


Figure 3.2.3 Start Up Sequence (triggered by First Connect Event)

3.2.7 External Reset Handling

The chip reset can be controlled by an external RESET_N ball. If this ball is pulled low, the chip will be reset. All PMU registers are reset during the external reset including LSIM control bits. The PMU statemachines are also not reset from the external reset. An SW or watchdog reset will not reset the PMU registers. A SW and Watchdog reset is seen on the reset_n pad to allow the reset of external devices. Basically there are three reset sources, first the reset signal controlled by the PMU (reset_pmu_n_o), second the reset signal controlled by the SCU (resetout_o) and third the external reset (RESET_N). The SCU reset is triggered by SW (for example due to a SW reset or watchdog reset). The PMU reset is controlled by the PMU state machine. The output of the reset handling block is the reset_postscu_n_o signal. This signal controls for example the μ C subsystem and releases reset for the controller. During normal start up, the PMU releases the reset_pmu_n_o signal after entering the SYSTEM ON state. At this time the resetout_o signal is high, the RESET_N pad is not pulled low and therefore the reset_postscu_n_o signal follows the reset_pmu_n_o signal. That means the μ C reset will be released and the μ C starts operation. If the SW triggers an external reset via the SCU, signal resetout_o will be forced to low for a certain time and RESET_N will be forced to low by the open drain driver. At the same time the feedback to the SCU will be masked to not reset the baseband. The RESET_N pad is in the VDDRTC domain but the internal pull up is connected to the VDD_VDIG1 (1.8V) domain. That allows the pad to be used as reset for external devices running in the VDD1V8 domain. The RESET_N pad can also be used to monitor the chip internal reset condition during startup.

The open drain driver is a weak driver, that means it can be forced to high during debug from external pushing some current into the pad. In testmode signal reset_pmu_n_o is high, that means the chip reset is fully controlled from external .

3. TECHNICAL BRIEF

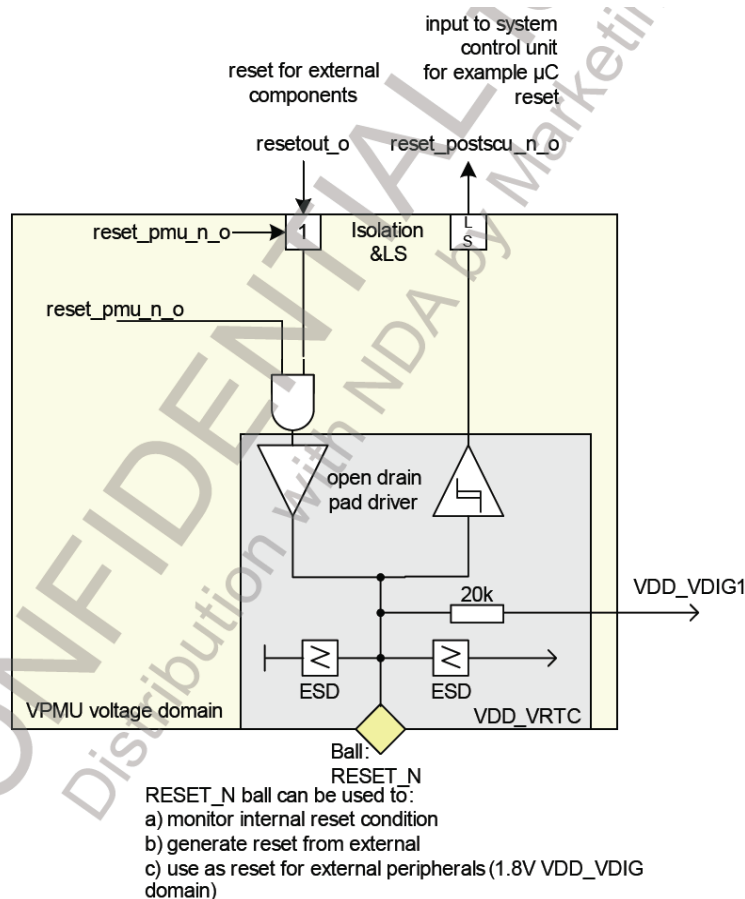


Figure 3.2.4 PMU, CGU and External Reset

3.2.8 Sysclock Switching

The PMU controls the rf_sysclk_en signal of the DCXO in the RF macro. During startup the PMU enables the DCXO. After the system is running the DCXO is controlled by the SCU of the baseband by using the vcxo_enable signal. This is handled by a dedicated logic in the PMU, see **Figure 21**. As long as rf_sysclk_en_pmu, the output of the PMU state-machine is high, vcxo_enable controls the rf_sysclk_en signal to the RF. If rf_sysclk_en_pmu is low, the DXCO is switched off, independent from vcxo_enable.

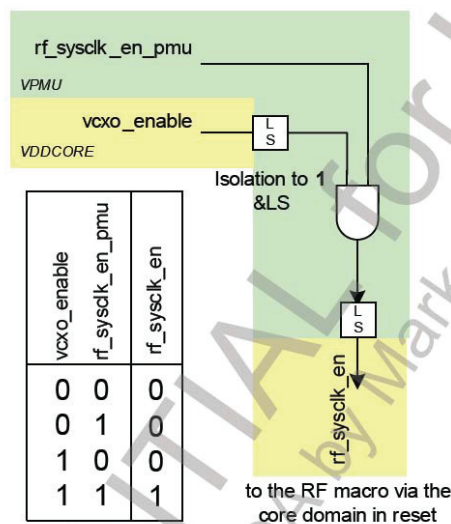


Figure 3.4.2 How sysclock Enable is Routed in the PMU

3.2.9 Undervoltage Shutdown

In active mode the PMU periodically measures the battery voltage using the ADC from the charger unit. If the battery is measured to be below the programmable shut-down level (called SYSOFF), the system changes to OFF mode. This is done via the SHUTDOWN state of the PMU state machine. (see chapter switch OFF)

3.2.10 Software Reset

A software reset does not affect any PMU register. The PMU register are reset with the `reset_pmufsm_n_o` signal. That means all PMU register are reset in OFF state. For details about the SW reset see chapter **External Reset Handling**.

3. TECHNICAL BRIEF

3.2.11 PMU Clock

During the first startup (for example plugging in a battery) a PMU internal oscillator is used for generation of the PMU clock (pmu_clock). The frequency is slightly above 32 kHz (typ. 50 kHz) to be out of the audio band also for worst case devices. After first startup the software shall enable the 32 kHz crystal oscillator. It is not possible to use the 32 kHz oscillator during first startup, because the settling time of the oscillator can be quite long. After the 32 kHz oscillator is running and settled the software shall switch the PMU clock to the 32 kHz clock and disable the internal PMU oscillator for power saving reasons. The 32 kHz oscillator shall never be disabled after the PMU clock has been switched. The ADC in the charger unit has its own oscillator generating a frequency of about 10 MHz. This oscillator is running during charging and during battery measurements triggered by the PMU. It is off otherwise.

3.2.12 System Sleep Mode

The sleep mode is controlled by using the VCXO_enable signal. This signal is used to switch the LDO's and the DC/DC converter SD1 in a programmable way into its low power mode (PFM). In addition DC/DC converter SD1 can be configured to change the output voltage to a lower value for additional power saving. VCXO_enable is also used to deactivate the HPBG and setting LDO LPMU in the ultra-low-power mode. In addition the DCXO is switched off by the VCXO_enable signal. The VCXO_enable signal is also used to switch some LDO's (software configured) to sleep and/or off mode or to change the output voltages of said LDO's. The state of the main PMU state machine is not changed due to VCXO_enable.

3.2.13 DC/DC Pre-Load Register Handling

The DC/DC converter works in different modes. If the mode is switched from PFM to PWM the pulse-width of the DC/DC converter depends on the current battery voltage (and on the output voltage). The PMU state-machine knows the battery voltage because of the battery supervision function. Depending on this value it selects a startup pulse-width for the DC/DC converter out of a register table. (4-values)

3.2.14 Power Down Sequence

Setting bit OFF in the GeneralControl register switches the system into OFF mode. After the turn off event, the state-machine switches to the SHUTDOWN state. The reset_pmu_n_o signal changes to low, the I/O pads are isolated using the padisolation_n signal, the LDO LPMU and the SD1 DC/DC converter are switched off, the LDO LPMU is switched to ultra-low power mode, the DCXO is turned off and the bandgap buffer is disabled. Before switching OFF the software shall have enabled the 32 kHz oscillator and has switched the PMU clock to the 32 kHz clock to archive the target OFF current .

3.3 FEM with integrated Power Amplifier Module (RF7161, U301)

3.3.1 Internal Block Diagram

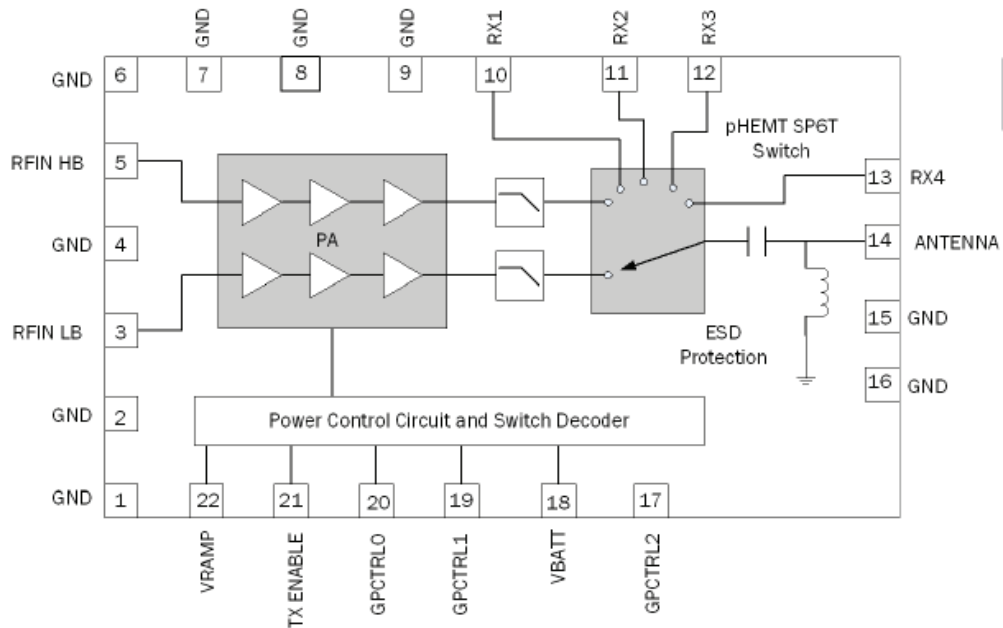


Figure. 3-3-1 RF7161 FUNCTIONAL BLOCK DIAGRAM

3. TECHNICAL BRIEF

3.3.2 General Description

The RF7161 is a quad-band (GSM850/EGSM900/DCS1800/PCS1900) GSM/GPRS, Class 12 compliant transmit module with four interchangeable receive ports. This transmit module builds upon RFMD's leading power amplifier with PowerStar® integrated power control technology, pHEMT switch technology, and integrated transmit filtering for best-in-class harmonic performance. The results are high performance, reduced solution size, and ease of implementation. The device is designed for use as the final portion of the transmitter section in a GSM850/EGSM900/DCS1800/PCS1900 handset and eliminates the need for a PA-toantenna switch module matching network. The device provides 50 Ω matched input and output ports requiring no external matching components.

The RF7161 features RFMD's latest integrated power-flattening circuit which significantly reduces current and power variation into load mismatch. Additionally, a VBATT tracking feature is incorporated to maintain switching performance as supply voltage decreases. The RF7161 also integrates an ESD filter to provide excellent ESD protection at the antenna port. The RF7161 is designed to provide maximum efficiency at rated POUT.

MODE	VLOGIC	TX_EN	BS1	BS2
STANDBY	LOW	LOW	LOW	LOW
EGSM_RX	HIGH	LOW	LOW	LOW
GSM850_RX	LOW	LOW	LOW	HIGH
PCS_RX	LOW	LOW	HIGH	HIGH
DCS_RX	LOW	LOW	HIGH	LOW
LB_TX	LOW	HIGH	LOW	HIGH
HB_TX	LOW	HIGH	HIGH	HIGH

1. RX1, RX2, RX3, and RX4 are broadband receive ports and each supports the EGSM, GSM850, PCS, and DCS bands.

Figure 3.3.2 Band SW Logic Table

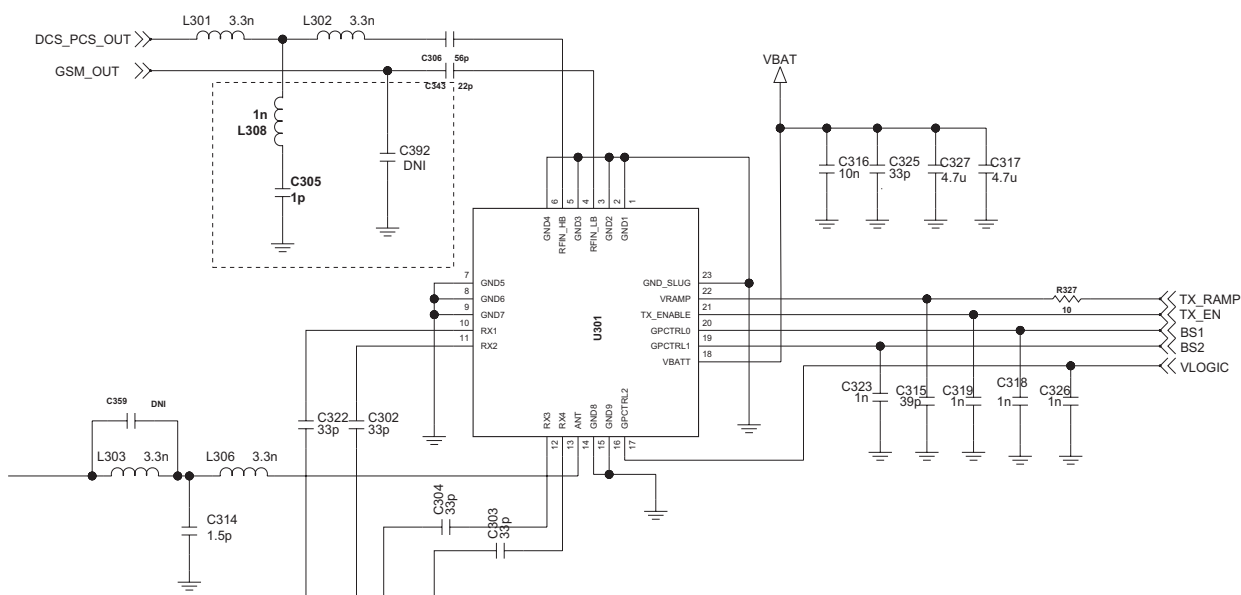


Figure 3.3.3 FEM CIRCUIT DIAGRAM

3. TECHNICAL BRIEF

3.4 Crystal(26 MHz, X102)

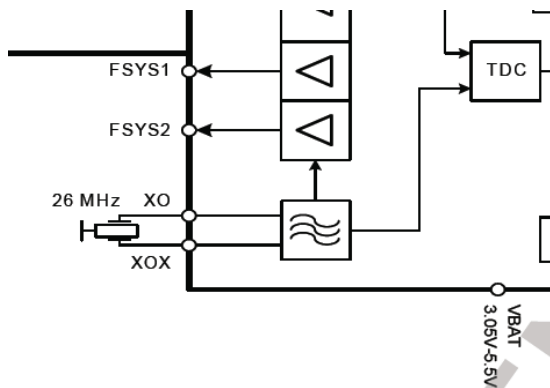


Figure. 3.4.1 Crystal Oscillator External Connection

The X-GOLDTM213 RF-Subsystem contains a fully integrated 26 MHz digitally controlled crystal oscillator, designed for 8 pF crystals. The only external part of the oscillator is the crystal itself. Overall pulling range of the DCXO is approximately ± 55 ppm, controllable by a 13-bit tuning word.

This frequency serves as comparison frequency within the RF-PLL and as clock frequency for the digital circuitry. The 26 MHz reference clock can also be applied to external components like Bluetooth or GPS, via the two buffered output signals FSYS1 and FSYS2.

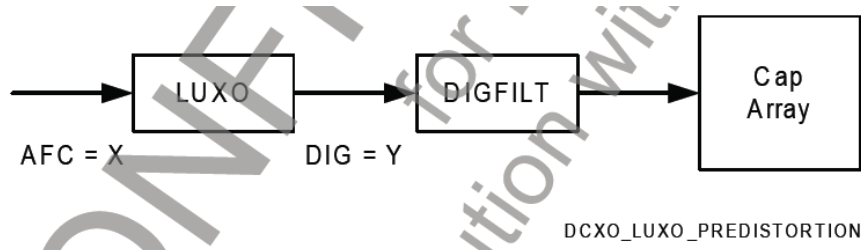


Figure. 3.4.2 Digital PREDISTORTION with LUXO

The DCXO tuning characteristic should be a first order linear function of the programming word AFC. The variable capacitance array is a first order linear function of the digital word DIG, which leads to a nonlinear curve ppm vs. DIG (and also a nonlinear ppm vs. AFC for DIG=AFC). In order to linearize the ppm vs. AFC curve the implementation of a predistortion is necessary.

To get the wanted linear ppm vs. AFC tuning curve some digital predistortion of the AFC word is required. This predistortion is performed by the linearization unit for crystal oscillator (LUXO). The LUXO calculates the corresponding DIG value according to the given AFC value.

3.5 RF Subsystem of PMB8810 (U101)

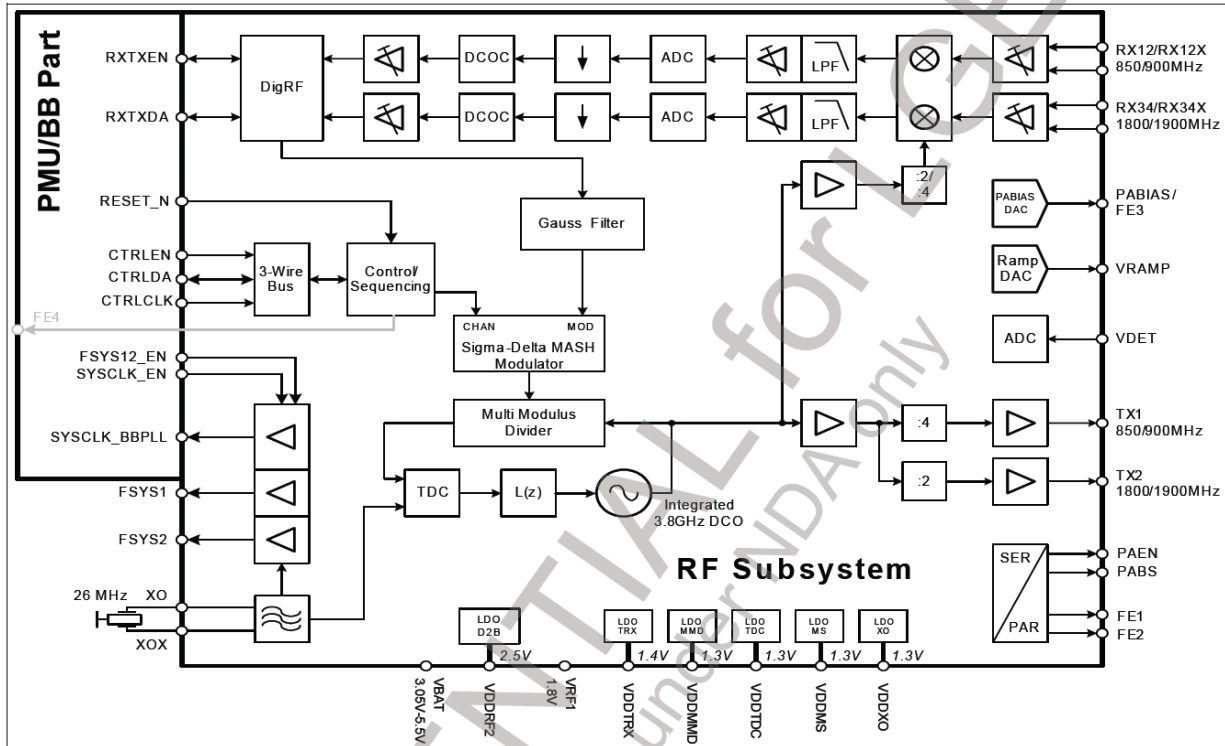


Figure. 3-5-1 Block DIAGRAM of RF Subsystem

3.5.1 GENERAL DESCRIPTION

The PMB8810 RF subsystem is designed for dual-band GSM voice and data applications (GPRS class 12). The system can be configured to support one low band, GSM850 or EGSM900, and one high band, DCS1800 or PCS1900. A block diagram of the RF subsystem is given in Figure 3-5-1.

3. TECHNICAL BRIEF

3.5.2 FUNCTIONAL DESCRIPTION

3.5.2.1 Receiver

The X-GOLD™213 dual-band receiver is based on a Direct Conversion Receiver (DCR) architecture. Input impedance of the LNAs is optimized to achieve a matching without (external) high quality inductors. By use of frequency dividers (by 2/4) the LO frequency is derived from the RF frequency synthesizer. The receive path is fully differential to suppress the on-chip interferences and reduce DC-offsets. The analog chain of the receiver contains two LNAs (low/high band), a quadrature mixer followed by an analog baseband filter and 14-bit continuous-time delta-sigma analog-to-digital converter. The filtered and digitized signal is fed into the digital signal processing chain, which provides decimation, DC offset removal and programmable gain control.

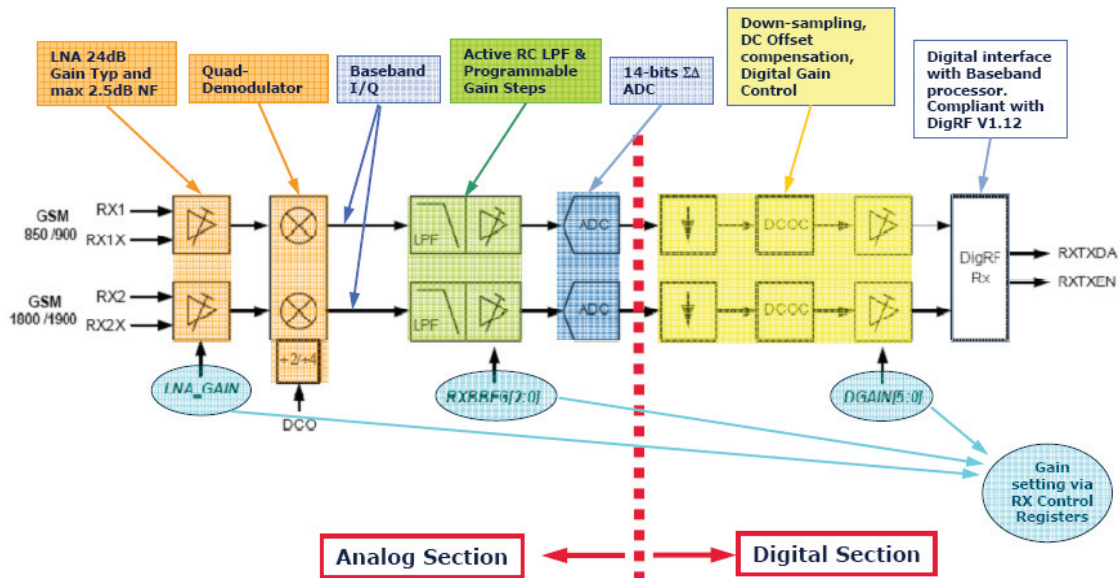


Figure. 3.5.2 RECEIVER CHAIN BLOCK DIAGRAM

3.5.2.2 Transmitter

The GMSK transmitter supports power class 4 for GSM850 or GSM900 as well as power class 1 for DCS1800 or PCS1900. The digital transmitter architecture is based on a fractional-N sigma-delta synthesizer for constant envelope GMSK modulation. This configuration allows a very low power design without any external components.

Up- and down-ramping is performed via the ramping DAC connected to VRAMP.

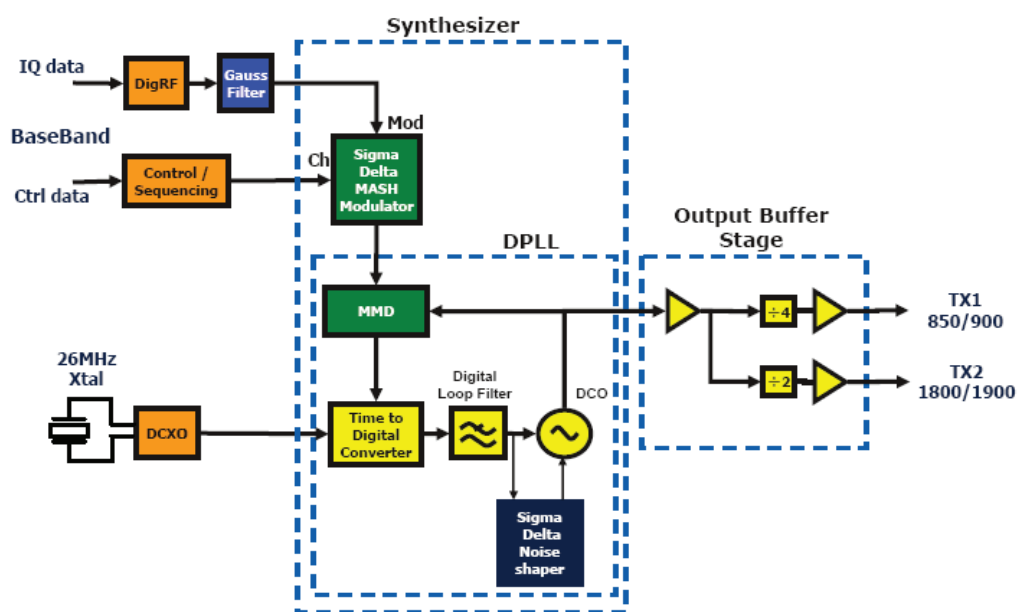


Figure. 3.5.3 TRANSMITTER CHAIN BLOCK DIAGRAM

RF synthesizer

The RF subsystem contains a fractional-N sigma-delta synthesizer for the frequency synthesis. Respective to the chosen band of operation the phase locked loop (PLL) operates at twice or forth of the target signal frequency. In receive operation mode the divided output signal of the digital controlled oscillator output (DCO) serves as local oscillator signal for the balanced mixer. For transmit operation the fractional-N sigma-delta synthesizer is used as modulation loop to process the phase/frequency signal. The 26 MHz reference signal of the phase detector incorporated in the PLL is provided by the reference oscillator.

3. TECHNICAL BRIEF

3.5.2.3 Front-end/PA Control Interface

Two outputs (FE1, FE2) for direct control of antenna switch modules enable to select RX- and TX-mode as well as low- and high-band operation.

An extra band select signal PABS for the power amplifier is used, to support discrete PA and switching modules. Time accurate power dissipation of the PA is achieved by the control signal PAEN.

A minor set of power amplifiers require a bias voltage to enhance power efficiency. Support of this power amplifiers is achieved by the implemented bias DAC.

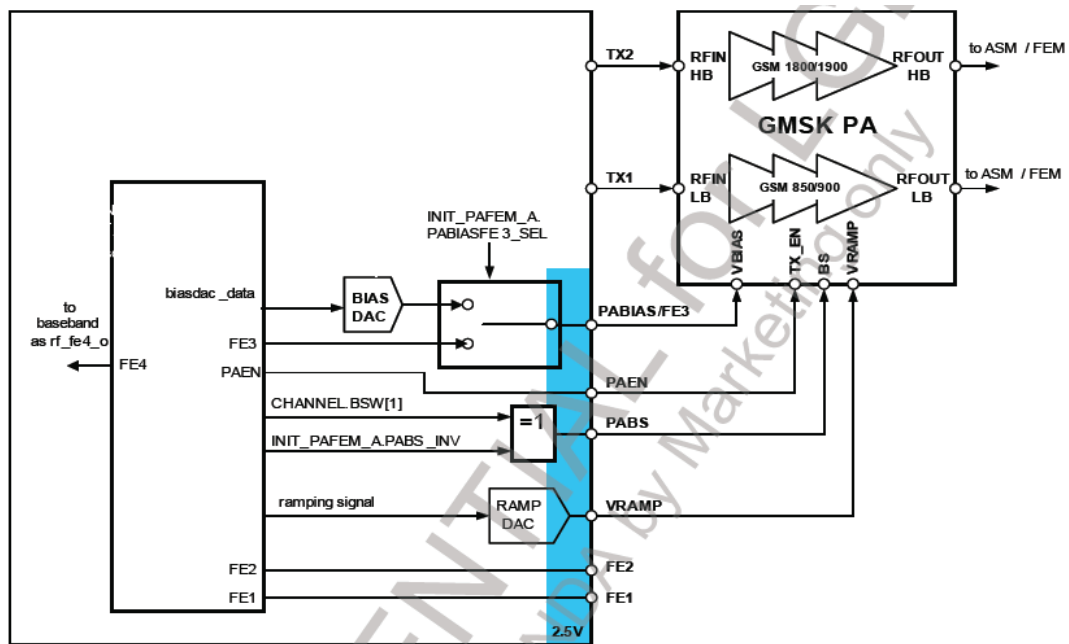


Figure. 3.5.4 PA AND FEM CONTROL BLOCK DIAGRAM

3.5.2.4 Power Supply

To increase power efficiency most parts of the RF subsystem are supplied by the DCDC converter situated in the PMU subsystem. Conversion of the 1.8 V output voltage of the DCDC to the 1.3 V/1.4 V circuit supply voltages is achieved by several Low-DropOut regulators (LDO). One embedded direct-to-battery LDO provides the 2.5 V supply voltage for the remaining circuits.

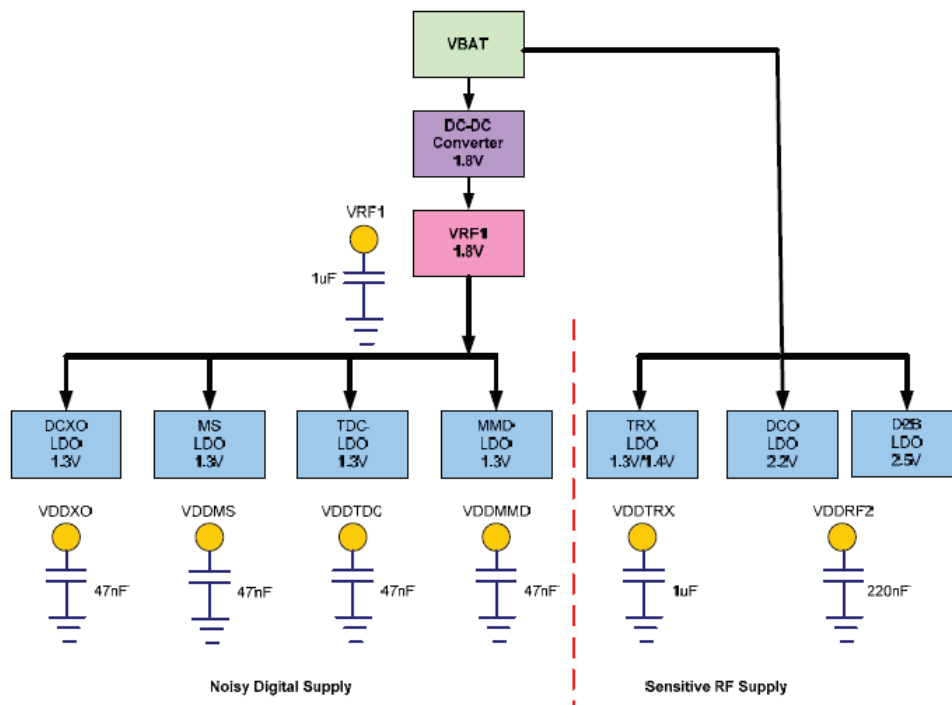


Figure. 3.5.5 POWER SUPPLY BLOCK DIAGRAM

3. TECHNICAL BRIEF

3.6 MEMORY(PF38F6066M0Y3DE, U102)

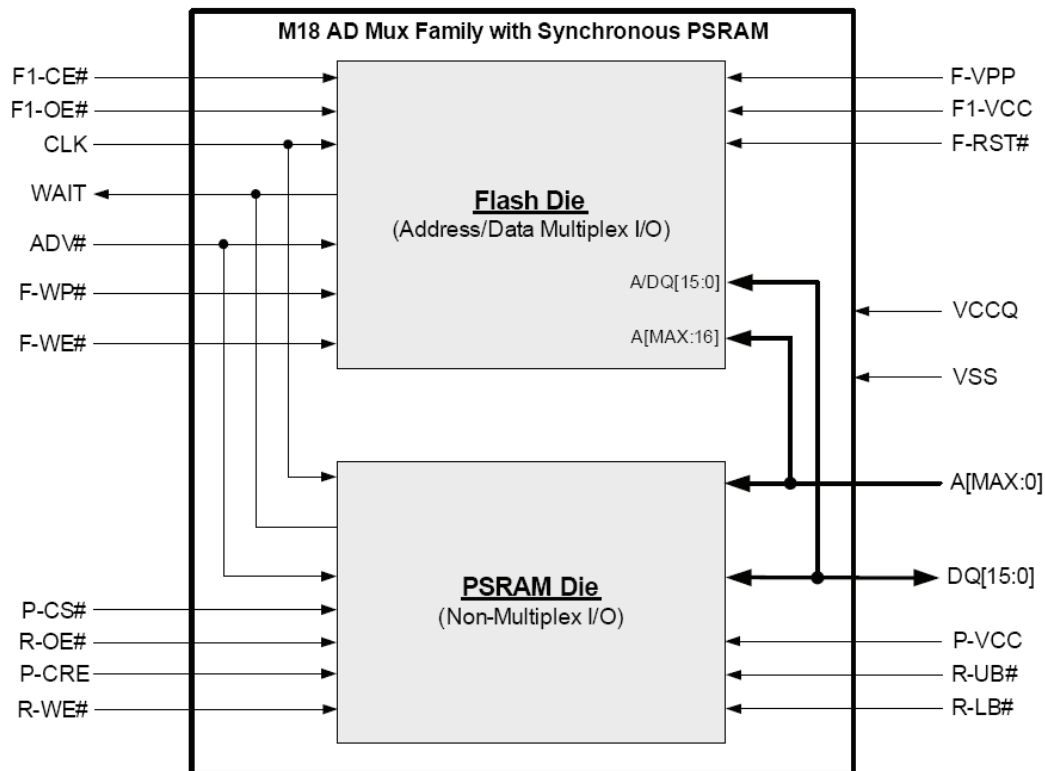


Figure. 3.6.1 MEMORY BLOCK DIAGRAM

The Numonyx™ StrataFlash® Cellular Memory (M18) device provides high read and write performance at low voltage on a 16-bit data bus.

The flash memory device has a multi-partition architecture with read-while-program and read-while-erase capability.

The device supports synchronous burst reads up to 108 MHz using ADV# and CLK address-latching (legacy-latching) on some litho/density combinations and up to 133 MHz using CLK address-latching only on some litho/density combinations. It is listed below in the following table.

.

Litho (nm)	Density (Mbit)	Supports frequency up to (MHz)	Sync read address-latching
90	256	133	CLK-latching
	512	108	Legacy-latching
65	128	133	CLK-latching
	256	133	CLK-latching
	512	108	Legacy-latching
	512	133	CLK-latching
	1024	108	Legacy-latching
	1024	133	CLK-latching

Table 3_6_1 M18 Frequency combinations

In continuous-burst mode, a data Read can traverse partition boundaries.

Upon initial power-up or return from reset, the device defaults to asynchronous arrayread mode. Synchronous burst-mode reads are enabled by programming the Read Configuration Register. In synchronous burst mode, output data is synchronized with a user-supplied clock signal. A WAIT signal provides easy CPU-to-flash memory synchronization.

Designed for low-voltage applications, the device supports read operations with VCC at 1.8 V, and erase and program operations with VPP at 1.8 V or 9.0 V. VCC and VPP can be tied together for a simple, ultra-low power design. In addition to voltage flexibility, a dedicated VPP connection provides complete data protection when VPP is less than VPPLK.

A Status Register provides status and error conditions of erase and program operations.

One-Time-Programmable (OTP) registers allow unique flash device identification that can be used to increase flash content security. Also, the individual block-lock feature provides zero-latency block locking and unlocking to protect against unwanted program or erase of the array.

The flash memory device offers three power savings features:

- Automatic Power Savings (APS) mode: The device automatically enters APS following a read-cycle completion.
- Standby mode: Standby is initiated when the system deselects the device by deasserting CE#.
- Deep Power-Down (DPD) mode: DPD provides the lowest power consumption and is enabled by programming in the Enhanced Configuration Register. DPD is initiated by asserting the DPD pin.

3. TECHNICAL BRIEF

3.7 BT + WLAN module (U304)

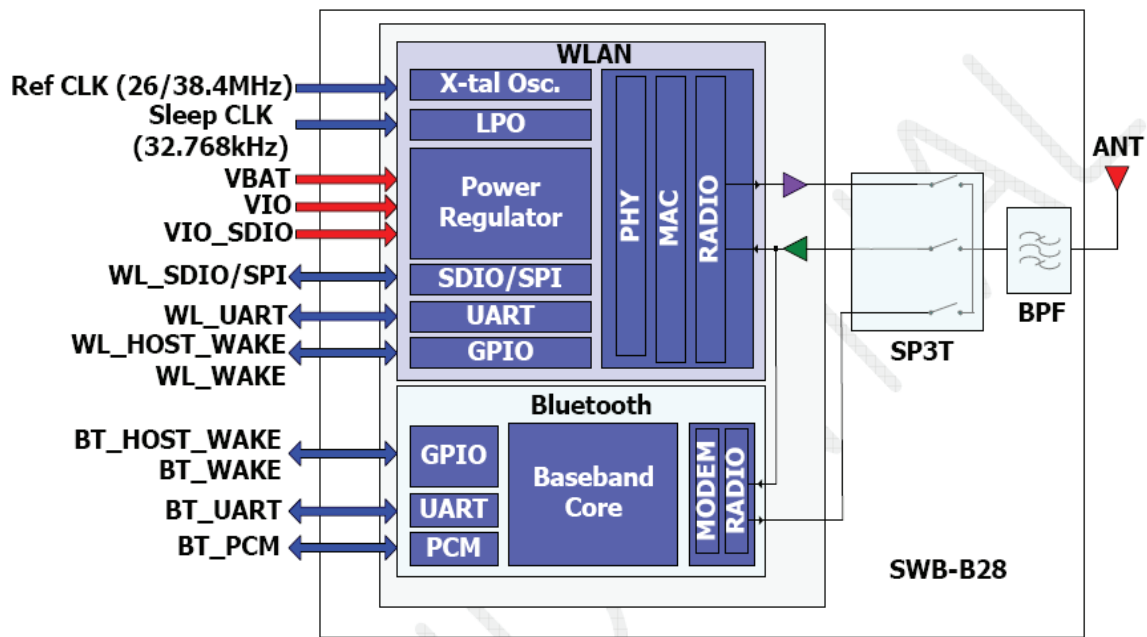


Figure 3_7_1. BT BLOCK DIAGRAM

This module has an integrated radio transceiver that has been optimized for use in 2.4GHz Bluetooth & WLAN Wireless systems. It has been designed to provide low-power, robust communications for applications Operating in the globally available 2.4GHz unlicensed ISM band. It is fully compliant with the Bluetooth Radio Specification and enhanced data rate specification and meets or exceed the requirement to provide the highest communication link quality of service.

3.7.1 Transmitter path

This module features a fully integrated zero IF transmitter. The baseband transmitted data is digitally modulated in the modem block and up-converted to the 2.4GHz ISM band in the transmitter path. The transmitter path consists of signal filtering, I/Q up-conversion, high-output power amplifier(PA), and RF filtering. It also incorporates modulation schemes P/4-DQPSK for 2 Mbps and 8-DPSK for 3 Mbps to support enhanced data rate.

- **Digital modulator**

The digital modulator performs the data modulation and filtering required for the GFSK, $\pi/4$ DQPSK, and 8-DPSK signal. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal and is much more stable than direct VCO modulation schemes.

- **Power Amplifier**

The integrated PA for the BCM4329 is configurable for Class 2 operation, transmitting up to +4 dBm as well as Class 1 operation and transmit power up to +12 dBm at the chip, GFSK, >2.5V supply. Due to the linear nature of the PA, combined with some integrated filtering, no external filters are required for meeting Bluetooth and regulatory harmonic and spurious requirements. For integrated mobile handset applications, where Bluetooth is integrated next to the cellular radio, minimal external filtering can be applied to achieve near thermal noise levels for spurious and radiated noise emissions. Using a highly linearized, temperature compensated design the PA can transmit +12 dBm for basic rate and +10 dBm for enhanced data rates(2 to 3 Mbps). A flexible supply voltage range allows the PA to operate from 1.2V to 3.0V. The minimum supply voltage at VDDTF is 1.8V to achieve +10dBm of transmit power.

3.7.2 Receiver path

The receiver path uses a low IF scheme to down-convert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, an extended dynamic range, and high order on-chip channel filtering to ensure reliable operation in the noisy 2.4GHz ISM band. The front-end topology, with built-in out-of-band attenuation, enables the device to be used in most applications with no off-chip filtering.

For integrated handset operation where the Bluetooth function is integrated close to the cellular transmitter, minimal external filtering is required to eliminate the desensitization of the receiver by the cellular transmit signal.

3. TECHNICAL BRIEF

3.8 SIM Card Interface

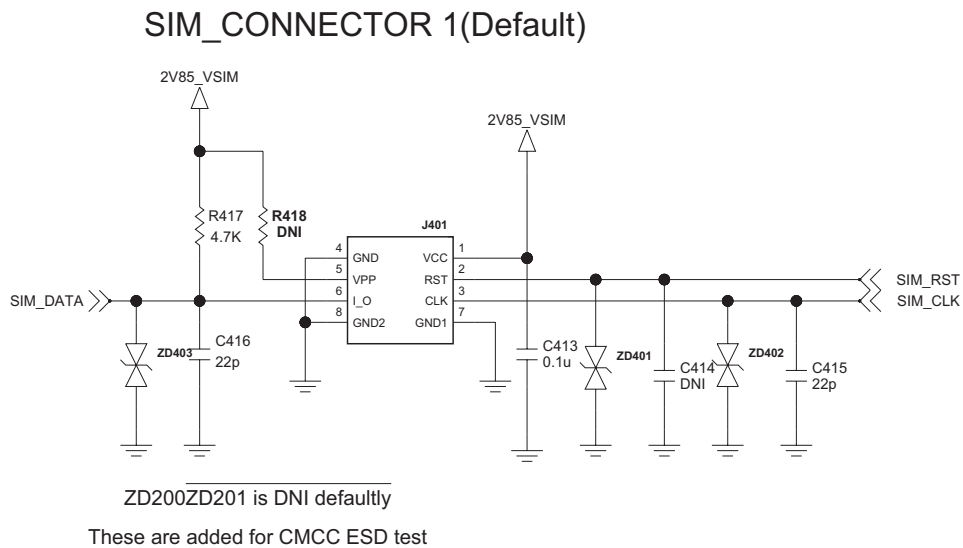


Figure 3-8-1. SIM CARD Interface

The Main Base Band Processor(XMM2130) provides SIM Interface Module.
The XMM2130 checks status Periodically During established call mode whether SIM card is inserted or not, but it doesn't check during deep sleep mode. In order to communicate with SIM card, 3 signals SIM_DATA, SIM_CLK, SIM_RST.
And This model supports 1.8/3V SIM Card.

Signal	Description
SIM_RST	This signal makes SIM card to HW default status.
SIM_CLK	This signal is transferred to SIM card.
SIM_DATA	This signal is interface datum.

3.9 LCD Interface

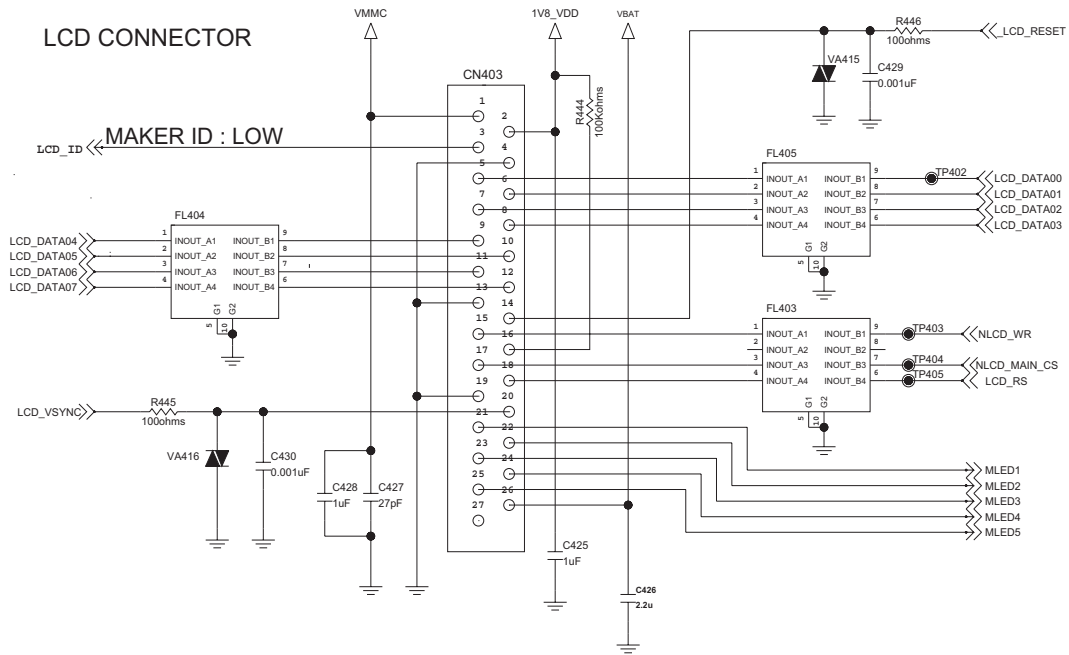


Figure 3-9-1. LCD Interface of LCD FPCB

3. TECHNICAL BRIEF

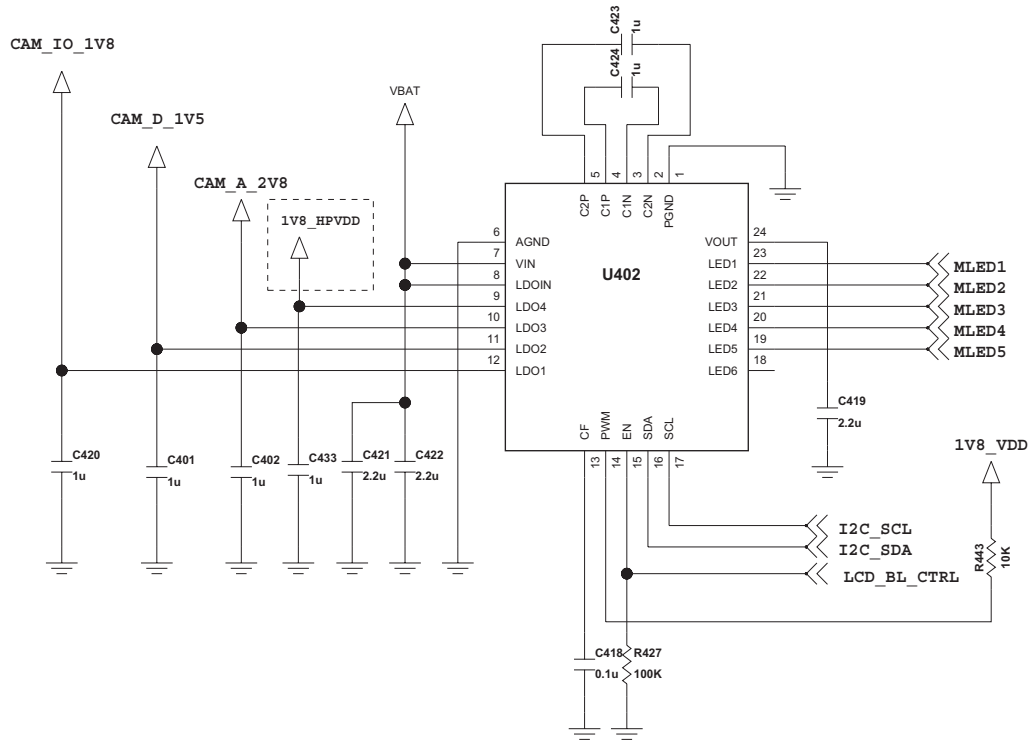


Figure 3-9-2. RT9396 CIRCUIT DIAGRAM

The RT9396 is an integrated solution for backlighting and phone camera input supply. The part contains a charge pump white LED driver and dual low dropout linear regulators. This IC can be shutdown by pulling ENA low.

In the section of charge pump, The RT9396 can power up 5 white LEDs with regulated constant current for uniform intensity. Each channel (LED1-LED5) can support up to 25mA. The part maintains highest efficiency by utilizing a x1/x1.5/x2 fractional charge pump and low dropout current regulators. An internal 5-bit DAC is used for brightness control. Users can easily configure up to 32-step of LED current by I2C interface.

In the section of linear regulator, The RT9396 comprises a dual channel, low noise, and low dropout regulator sourcing up to 300mA at each channel. The range of output voltage can be configured from 1.1V to 3.3V by I2C interface. The outputs of LDO offer 3% accuracy and low dropout voltage of 250mV @300mA. The LDO also provides current limiting and output short circuit thermal folded back protection.

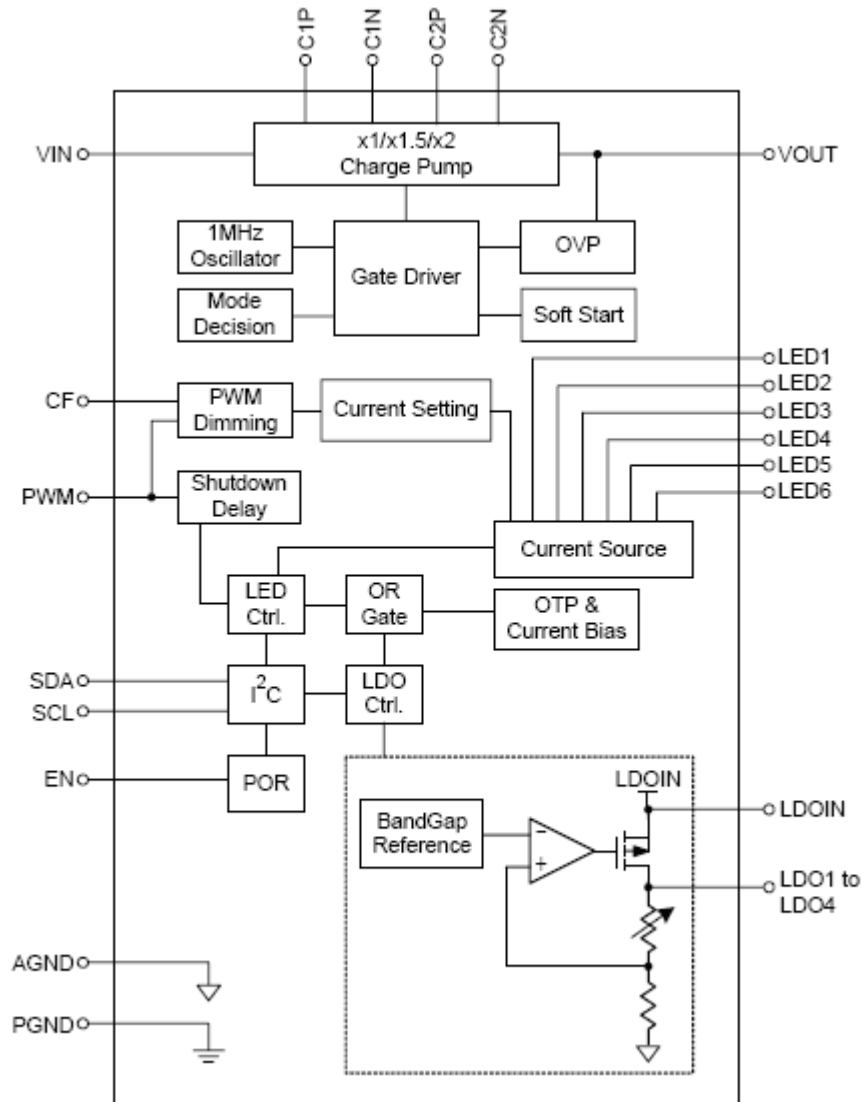


Figure 3-9-3. RT9396C FUNCTION BLOCK DIAGRAM

3. TECHNICAL BRIEF

3.10 Battery Charger Interface

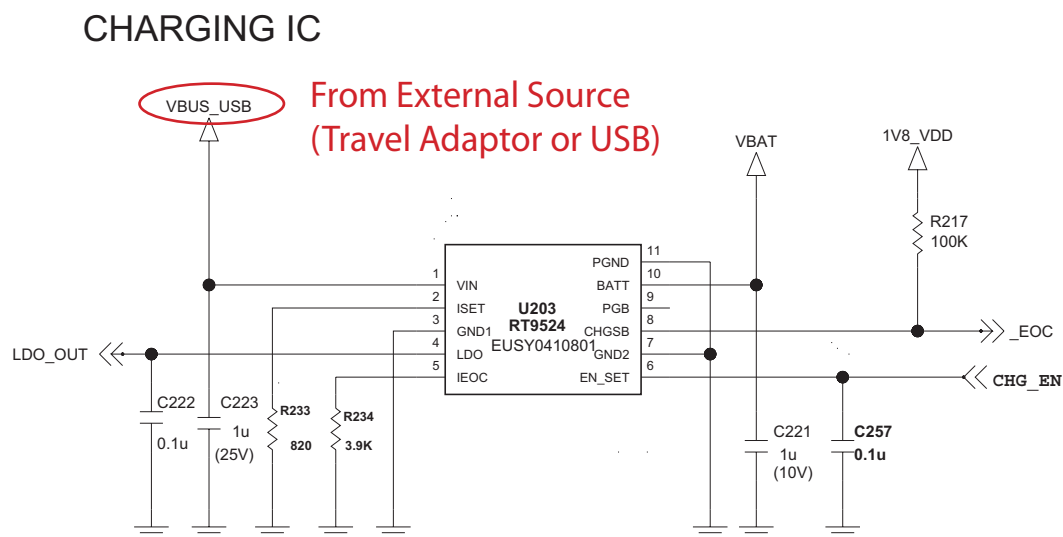


Figure 3-10-1 BATTERY CHARGER BLOCK

The RT9524 is a fully integrated single-cell Li-Ion battery charger IC ideal for portable applications. The RT9524 optimizes the charging task by using a control algorithm including pre-charge mode, fast charge mode and constant voltage mode. The input voltage range of the VIN pin can be as high as 30V. When the input voltage exceeds the OVP threshold, it will turn off the charging MOSFET to avoid overheating of the chip.

In RT9524, the maximum charging current can be programmed with an external resistor. For the USB application, user can set the current to 100mA/500mA through EN/SET pin. For the factory mode, the RT9524 can allow 4.2V/2.3V power pass through to support system operation. It also provides a 50mA LDO to support the power of peripheral circuit. The internal thermal feedback circuit regulates the die temperature to optimize the charge rate for all ambient temperatures. The RT9524 provides protection functions such as under voltage protection, over voltage protection for VIN supply and thermal protection for battery temperature.

The RT9524 is available in a WDFN-10L 2x3 package to achieve optimized solution for PCB space and thermal considerations.

3.11 Keypad Interface

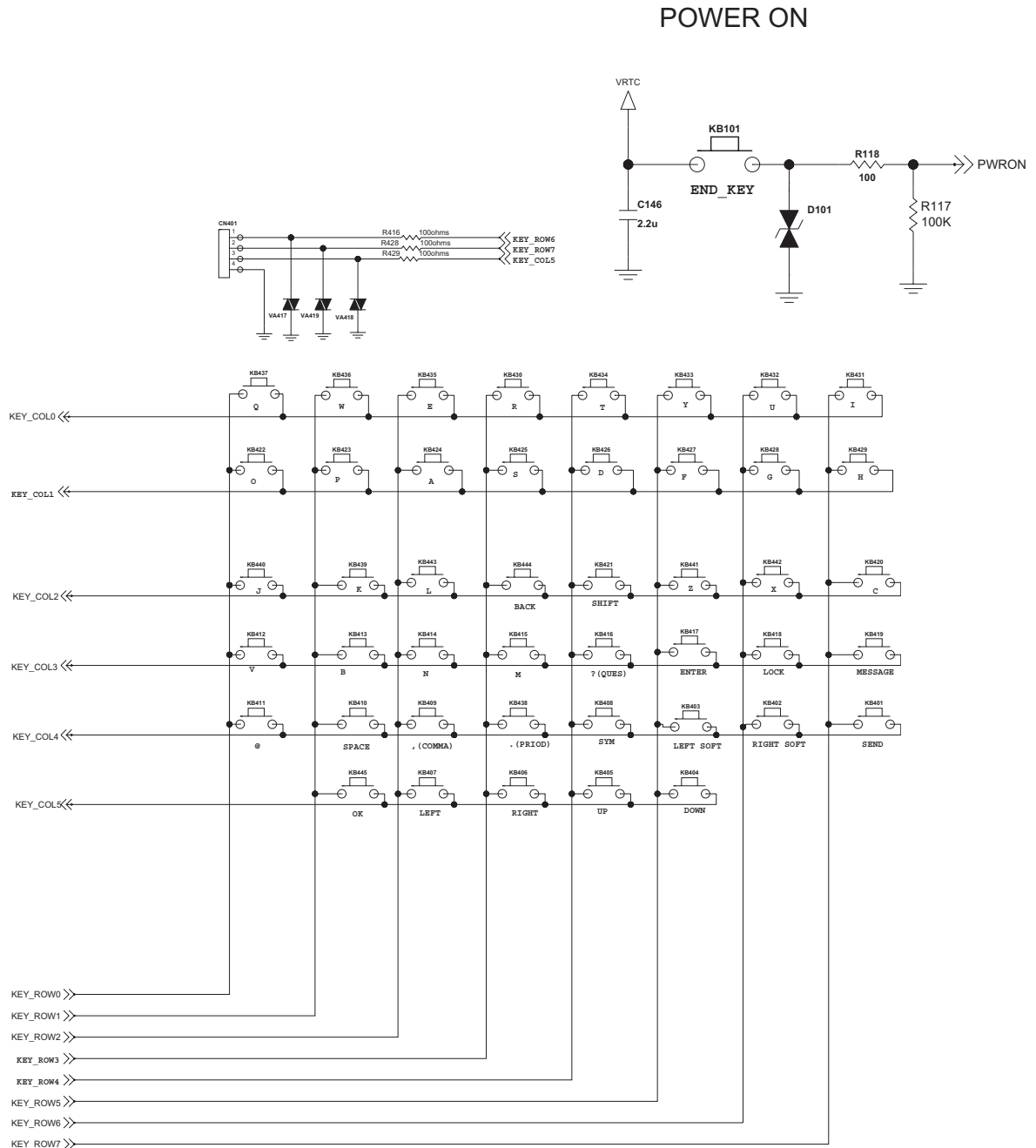


Figure 3-11-1 MAIN KEY STRUCTURE

3. TECHNICAL BRIEF

The Keypad Interface is a peripheral controller, which can be used for scanning external keypad matrices with up to 8 rows and 8 columns (that is 64 standard keys). By adding an additional row of keys connected to ground the number of keys can be extended by up to 8 keys. This results in a maximum number of 72 keys to be identified by the Keypad Interface Controller.

The Keypad Scan Module reduces the number of interrupts and polling through the processor and therefore reduces the power consumption. The module is able to debounce and scan the external keypad matrix automatically without any software intervention. After debouncing it generates an interrupt. The interface controller contains information about the key (or key combination) that was pressed and how long it was pressed.

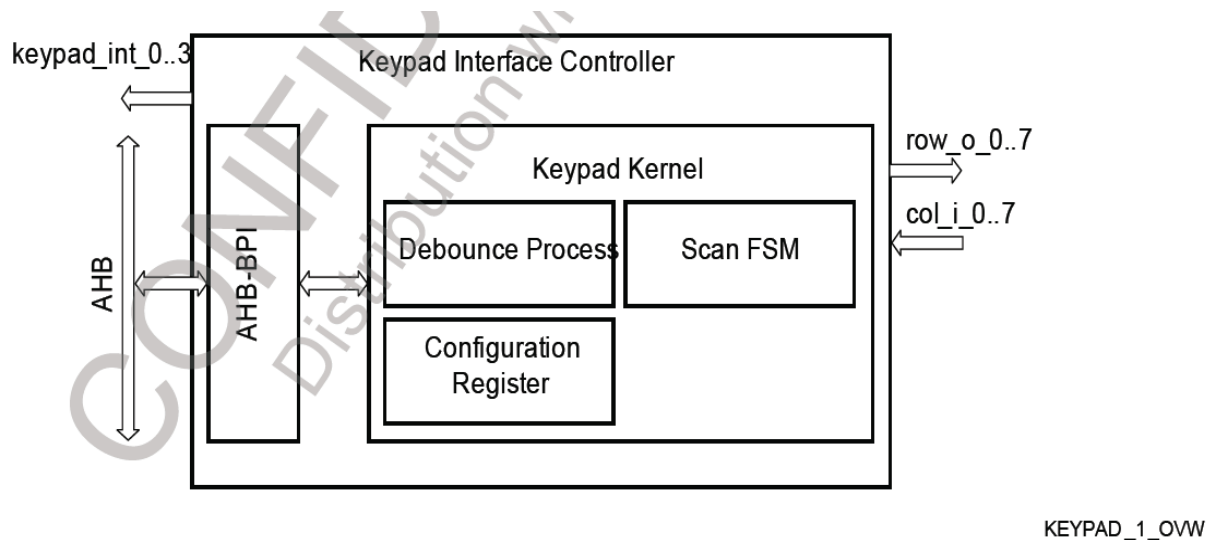


Figure 3-11-3 Block Diagram and System Integration of the KPD

3.12 Audio Front-End

3.12.1 Functional Overview

The audio front-end of X-GOLD™213 offers the digital and analog circuit blocks for both receive and transmit audio operation, from a mobile phone perspective (called audio-in and audio-out subsequently). It features a high-quality, stereo digital-to-analog path with amplifier stages for connecting acoustic transducers to X-GOLD™213. In audio-in path the supply voltage generation for electret microphones, a low-noise amplifier and analog to digital conversion are integrated in X-GOLD™213. A more detailed functional description will be given in the following sections.

The audio front-end itself can be considered to be organized in three sub-blocks:

- Interface to processor cores (TEAKLite® and - indirectly - ARM)
- Digital filters
- Analog part

The following figure shows an architecture overview of the Audio section.

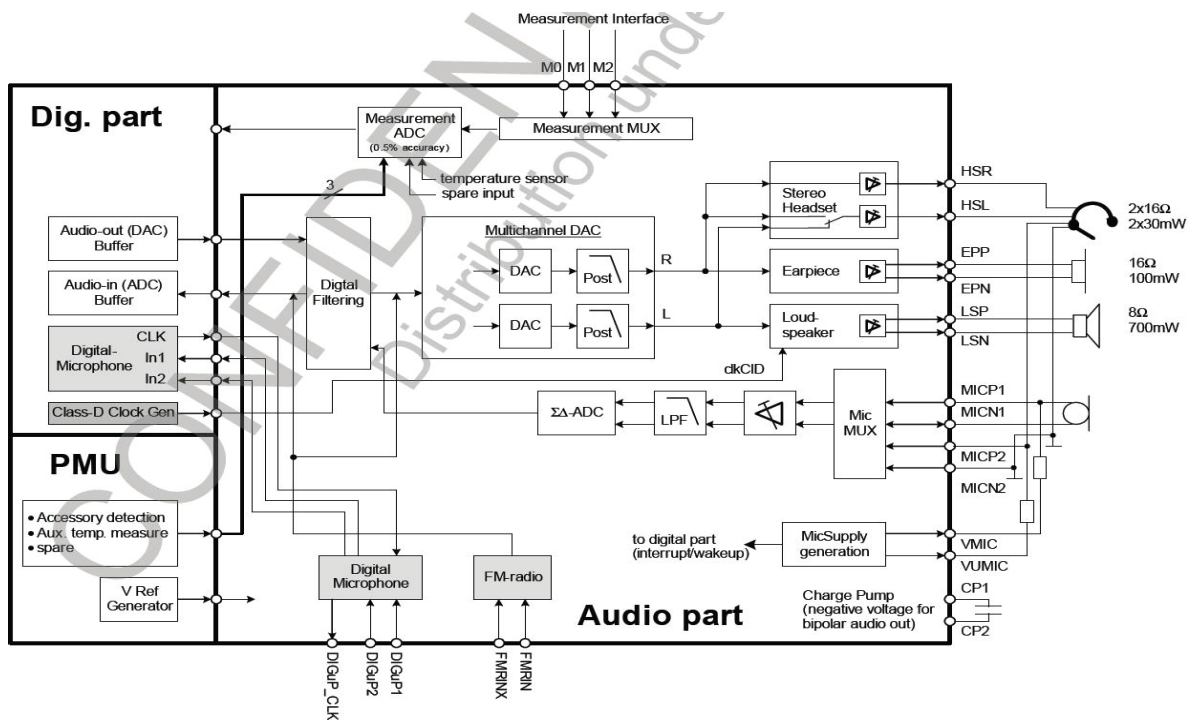


Figure 3.12.1 Audio Section Overview

3. TECHNICAL BRIEF

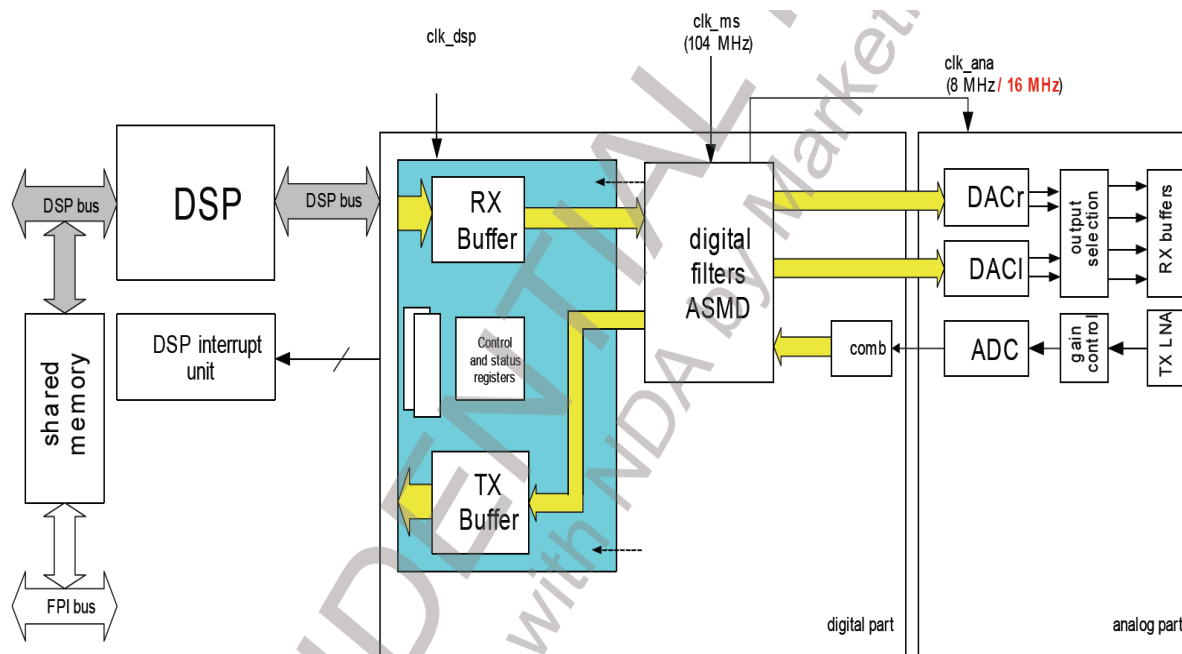


Figure 3.12.2 Overview of Clocking and Interfaces of Audio Front End

The audio front-end of X-GOLD™213 has the following major operation modes:

- Power-down: All analog parts are in power down and all clocks of the digital part are switched off.
- Audio mode: Digital decimation/interpolation filters are connected to the interface buffers and the analog part is enabled.

These major modes can be modified by certain control register settings.

- Due to the new gain settings in the TX path, the maximum input voltage is limited to 0.8 Vpp.
- In both voiceband paths, the value range for voice samples is confined to 97.5%, i.e. to [-31948, 31947] or [8334H, 7CCBH] in X-GOLD™213.
- On the TX path, 83% "1"s on the VTPDM line correspond to a 16-bit value of 7CCBH and 17% "1"s correspond to a 16-bit value of 8334H at the digital filter output. Thus the usable range is 66%. This range can be scaled to 100% by Firmware.
- The high-pass functions of the voiceband filters have to be implemented in firmware on TEAKLite®.

3.12.2 Digital Part

The digital part of the X-GOLD™213 audio front-end comprises an interface to the TEAKLite® bus, interfaces to the interrupt units of TEAKLite®, digital interpolation filters for oversampling digital-to-analog conversion, digital decimation filters for analog-to-digital conversion and an interface to the analog part of the audio front-end. For the digital microphone all the filtering is done in a dedicated hardware. The output sample stream is then fed in a duplicated ring buffer structure like the data from the analog microphone path (after A/D conversion and subsequent digital filtering).

▪ Interpolation Filter

The interpolation path of the X-GOLD™213 audio front-end increases the sampling rate of the audio samples to the rate of the digital-to-analog converter. Because the input sampling rates can vary between 8 kHz and 47.619 kHz the filter characteristic and oversampling ratio can be adjusted to the respective sampling rate. The requirements for the interpolation filters depend on the sampling rate, because a sufficient out-of-band discrimination in the audio frequency band (20 Hz,...,20 kHz) has to be ensured.

▪ Decimation Filter

The digital decimation filter on X-GOLD™213 has two operating modes: 8 kHz output sampling rate and 16 kHz output sampling rate (or 16 kHz output sample rate and 16kHz bandwidth in case of doubled ASMD clock).

3.12.3 Analog Part

The analog part of the X-GOLD™213 audio front-end in audio-out direction consists of a stereo digital to analog converter (multi-bit oversampling converter) which transforms the output of the digital interpolation filter into analog signals. It is followed by the gain control/amplifier section. The DAC outputs can be switched to several output buffers. In audio-in section there is an input multiplexer which selects either one of two differential microphone inputs to be connected to the low-noise amplifier and analog pre-filter. The signals from the analog pre-filter are input to a second-order sigma-delta analog-to-digital converter. In addition there is a connection for FM-radio playing.

▪ Audio-out Part

The analog audio-out part consists of two multi-bit digital-to-analogue converters (DAC) and an output stage. The signal sources are switched to the output drivers in the output stage. The output drivers consist of: a) one mono, differential class-D Loudspeaker driver, b) one mono, differential Earpiece driver and c) one stereo, single-ended (with uni- or bipolar signals), Headset driver.

3. TECHNICAL BRIEF

▪ Digital-to-analog converters

The multi-bit oversampling DACs of the X-GOLD™213 audio front-end convert the 16-bit data words coming from the digital interpolation filters to analogue signals.

▪ Output Amplifier

The different output buffers in X-GOLD™213 are driven by the outputs of the selection block. The differential earpiece driver can be used to drive a 16 Ω earpiece and works in differential. The two single ended headset drivers can be used to drive a 16 Ω headset. They can work unipolar mode, where an AC coupling of the headset might be needed, or can work also in bipolar mode. The differential loudspeaker driver can be used to drive a 8 Ω loudspeaker. As it is a class-D amplifier the needed suppression of the higher harmonics of the switching signals has to be achieved by the external circuitry. The buffers are designed to be short circuit protected.

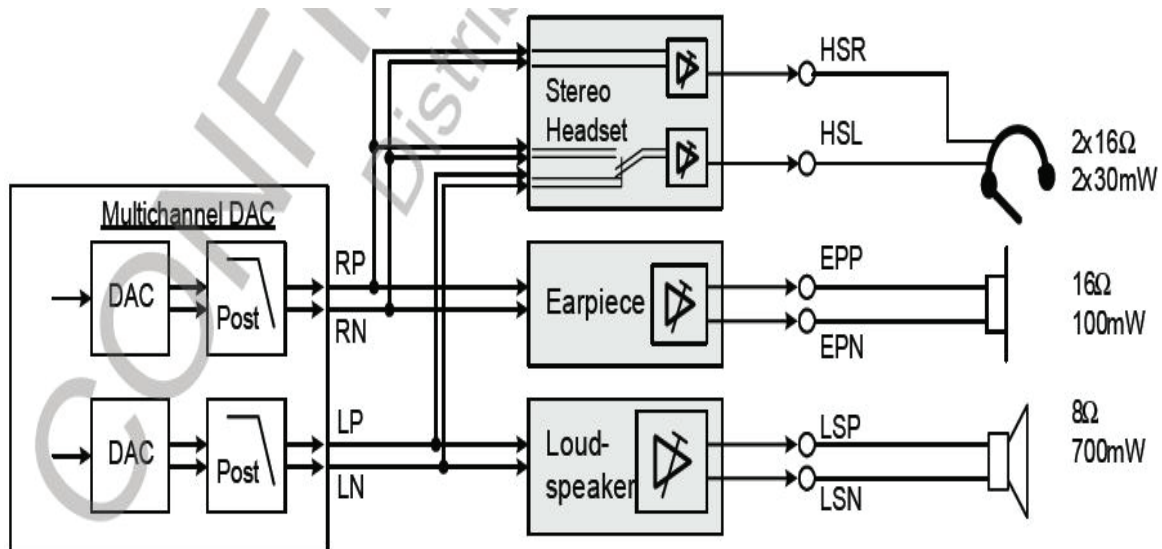


Figure 3.12.3 Switching for R/L DACs onto Buffers

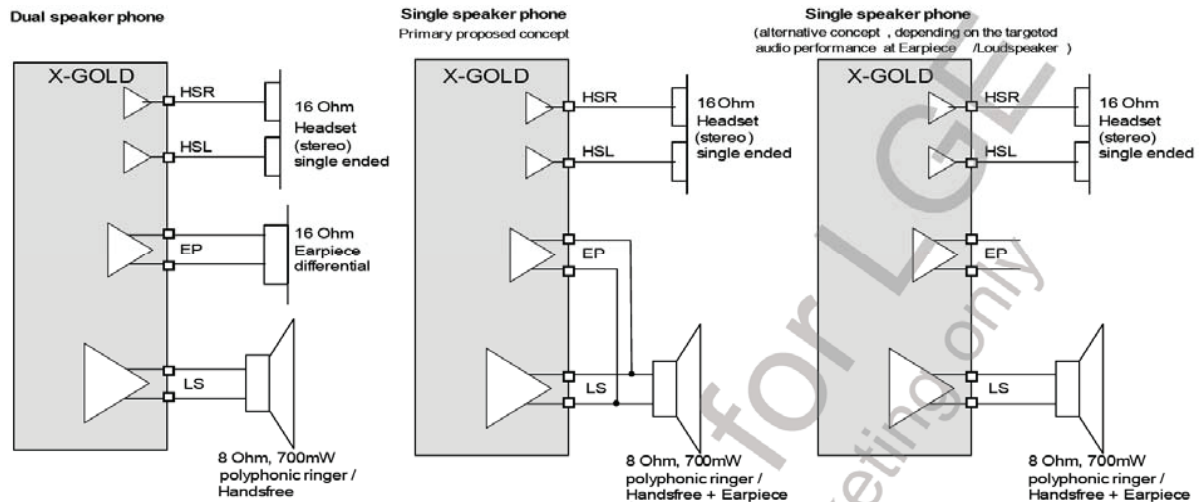


Figure 3.12.4 Different Application Scenarios

In order to achieve the single-speaker concept by parallel connection of Earpiece and Headset amplifier the Earpiece amplifier have to sustain the up to 5 V voltage of the class-D amplifier.

▪ Audio-in Path

The audio-in path of X-GOLD™213 provides two differential microphone input sources, MIC1 and MIC2.

- The inputs for microphone MIC1 are MICP1 and MICN1.
- The inputs for microphone MIC2 are MICP2 and MICN2.

The audio-in path consists of an input selector, a low noise amplifier and following pre-filter with gain control, a second order $\Sigma\Delta$ -converter and a digital decimation filter. It supports both standard GSM (bandwidth 3.5 kHz) and wideband (bandwidth 7 kHz) speech bands.

The differential input signal from the microphone first passes a low noise amplifier and following pre-filter and an anti-aliasing pre-filtering stage achieving an overall variable gain ranging from 0 dB to +39 dB.

The signal is then modulated by a second order $\Sigma\Delta$ -converter which is clocked with the same clock rate as the digital to analog converters. The $\Sigma\Delta$ -converter delivers a 1-bit pulse density modulated data stream at a rate of 2 MHz to the digital decimation filter which reduces the rate to 8 kHz or 16 kHz, depending on the current mode.

To improve SNR the sample frequency can be doubled in dedicated modes and the modulated data stream is 4MHz instead of 2 MHz.

3. TECHNICAL BRIEF

▪ Microphone Supply

X-GOLD™213 has a single ended power-supply concept for electret microphones:

For both modes a minimal load capacitance of t.b.d. nF is necessary to guarantee stable operation of the buffer.

The maximal load capacitance must not exceed t.b.d. nF.

2 microphone supplies VMIC and VUMIC are available. The supply VUMIC has a ultra-low-power mode, where the current consumption is minimum, whilst at the same time the noise performance is reduced.

For this purpose the VUMIC is directly supplied out of the VMIC regulator, the Mic-Buffer can be switched off and only the quiescent current of the VMIC regulator is present. This mode can be used to supply a headset and allow accessory detection with highly reduced current consumption For normal operation the supply can be switched to normal operation mode with improved noise performance. In case of an digital microphone VMIC can be used for supplying this microphone.

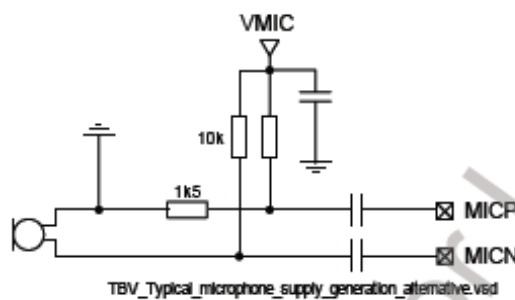


Figure 3.12.5 Typical Microphone Supply Generation (alternative)

3.13 Camera Interface(2M Fixed Focus Camera)

3.13.1 PMB8810 Camera Interface

The Camera Interface (CIF) represents a complete video and still picture input interface (see Figure 3.13.1).

The CIF contains image processing, scaling, and compression functions. The integrated image processing unit supports image sensors with integrated YCbCr processing.

Scaling is used for downsizing the sensor data for either displaying them on the LCD, or for generating data streams for MPEG-4 compression. In general, YCbCr 4:2:2 JPEG compressed images should use the full sensor resolution, but they can also be downscaled to a lower resolution for smaller JPEG files. Scaling also can be used for digital zoom effects, because the scalers are capable of up-scaling as well.

CIF all data is transmitted via the memory interface to an AHB bus system using a bus master interface. Programming is done by register read/write transactions using an AHB slave interface.

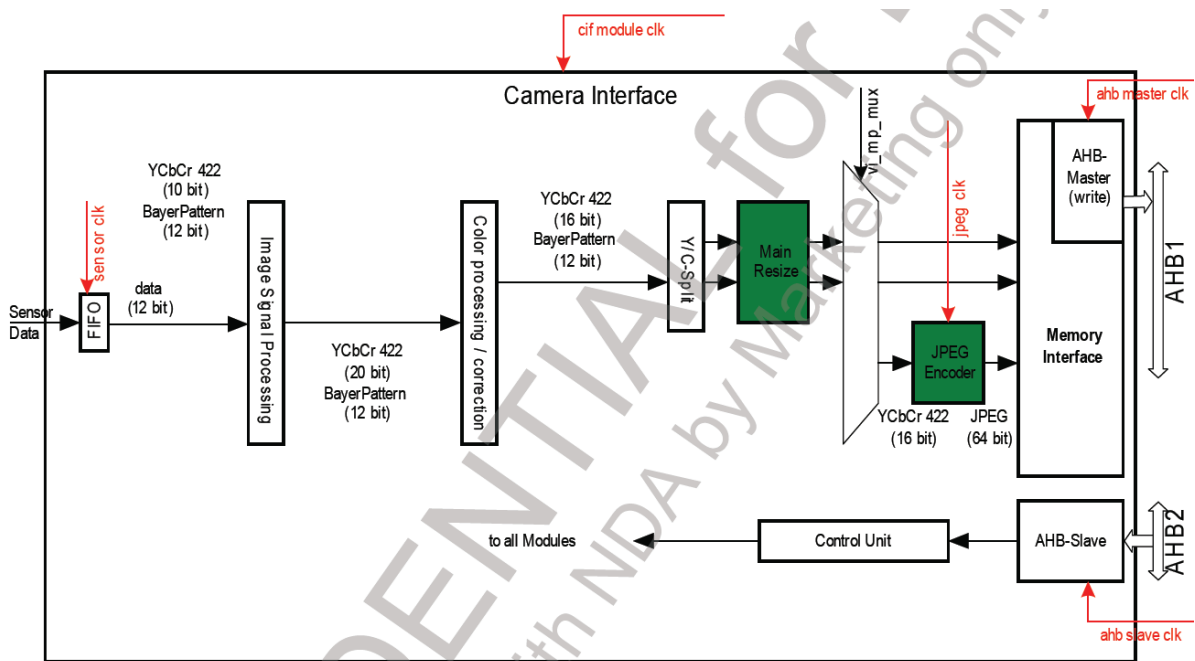


Figure 3.13.1 Block Diagram of Camera Interface

3. TECHNICAL BRIEF

Functional Overview of CIF

The following list gives an overview over the CIF's functionality:

- 78 MHz system clock
- 78 MHz sensor clock
- 78 MHz JPEG encoder clock
- 32-bit AHB slave programming interface
- ITU-R BT 601 compliant video interface supporting $YCbCr$
- ITU-R BT 656 compliant video interface supporting $YCbCr$ data
- 8-bit camera interface
- 12-bit resolution per color component internally
- $YCbCr$ 4:2:2 processing
- Hardware JPEG encoder incl. JFIF1.02 stream generator and programmable quantization and Huffman tables
- Windowing and frame synchronization
- Continuous resize support
- Frame skip support for video (e.g. MPEG-4) encoding
- Macro block line, frame end, capture error, data loss interrupts and sync. (h_start, v_start) interrupts
- Programmable polarity for synchronization signals
- Luminance/chrominance and chrominance blue/red swapping for YUV input signals
- Maximum input resolution of 3 Mpixels (2048x1536 pixels)
- Main scaler with pixel-accurate up- and down-scaling to any resolution between 3 MP (2048x1536) and 32x16
- pixel in processing mode
- Buffer in system memory organized as ring-buffer
- Buffer overflow protection for raw data and JPEG files
- Asynchronous reset input, software reset for the entire IP and separate software resets for all sub-modules
- Interconnect test support
- Semi planar storage format
- Color processing (contrast, saturation, brightness, hue)
- Power management by software controlled clock disabling of currently not needed sub-modules

3.14 KEY BACKLIGHT LED Interface

Key Backlight LED is controlled by switch (Q401). If KEY_BL_EN is high, Current is flowing from VBAT to LED. Then Light emitted from The LED.

KEY_BL_EN is operating PWM. It is reducing current consumption.

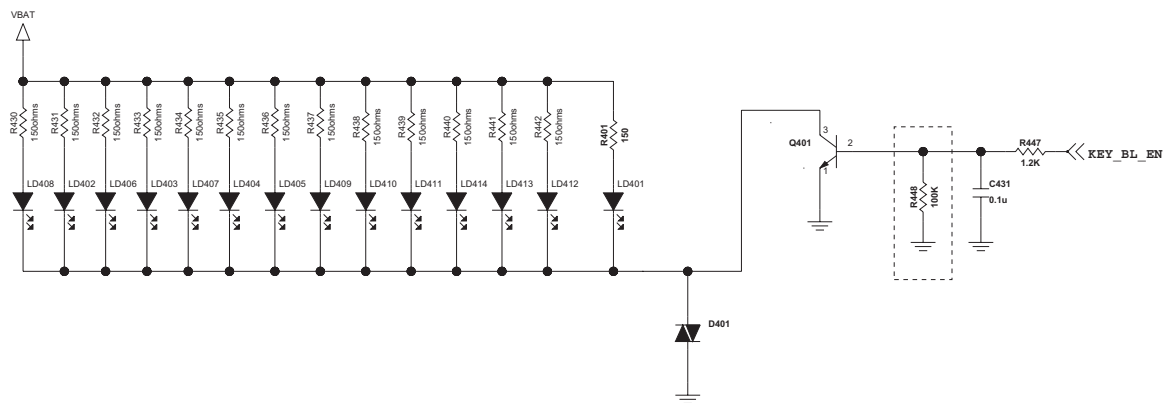


Figure 3-14-1 Key Backlight Block

3. TECHNICAL BRIEF

3.15 Vibrator Interface

Support PWM signal which generated by hardware itself via register control direct connect to the VIB and VSSVIB pin from XMM2130 without any external component required it is capable to driver the vibrator motor up to 150mA.

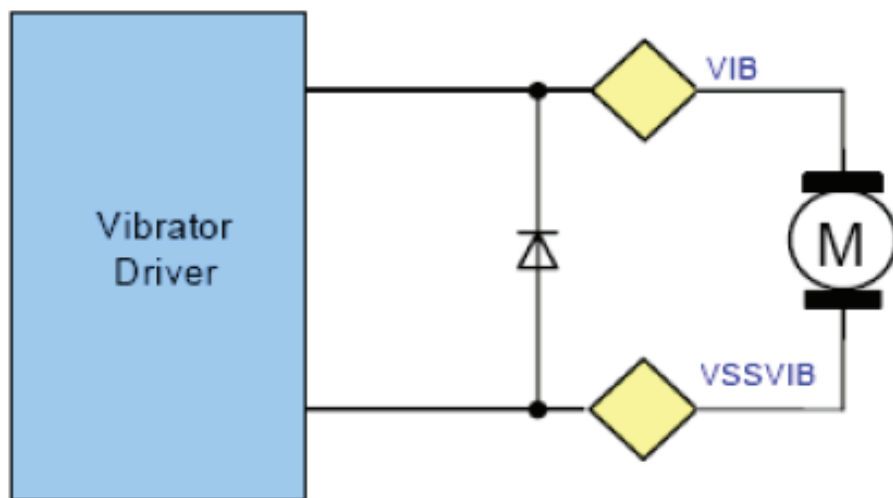


Figure 3-15-1 Vibrator Driver Block Diagram

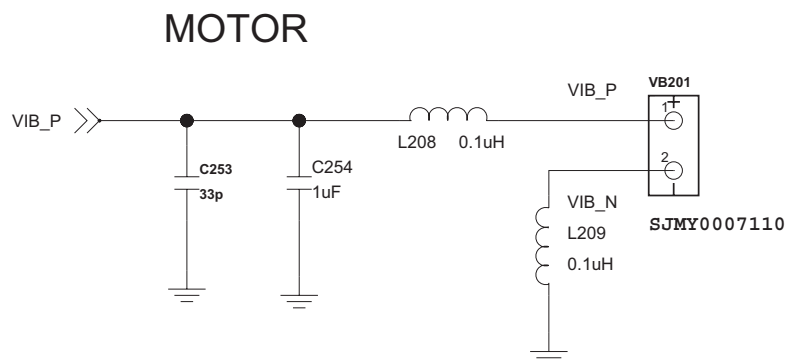


Figure 3-15-2 Vibrator Driver Block

4. TROUBLE SHOOTING

4.1 RF Component

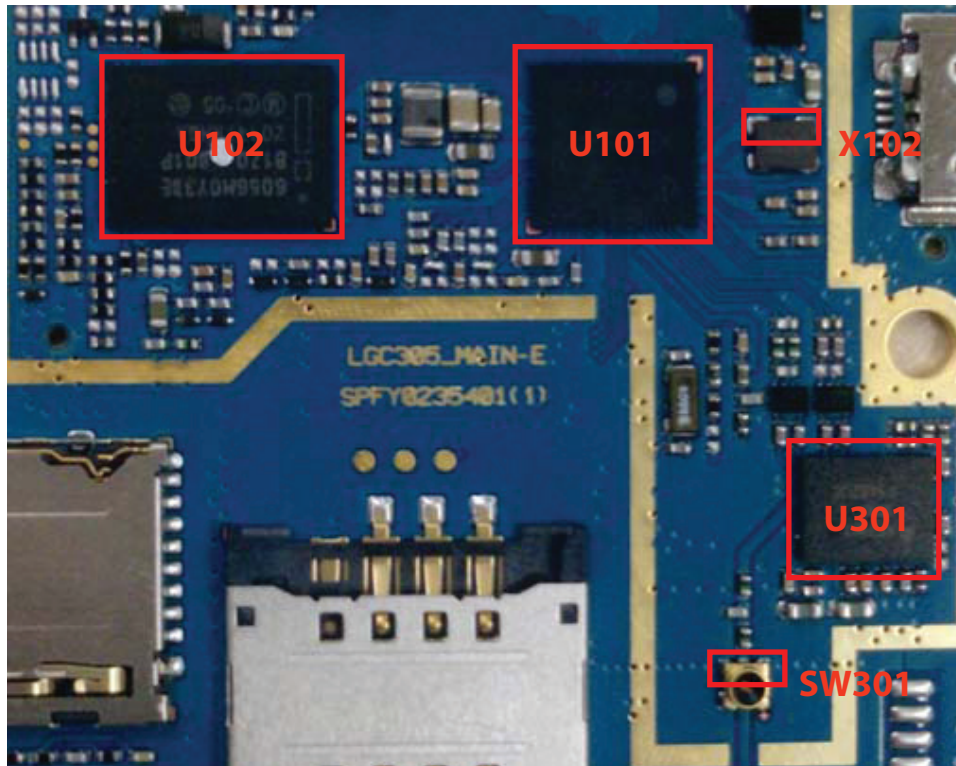


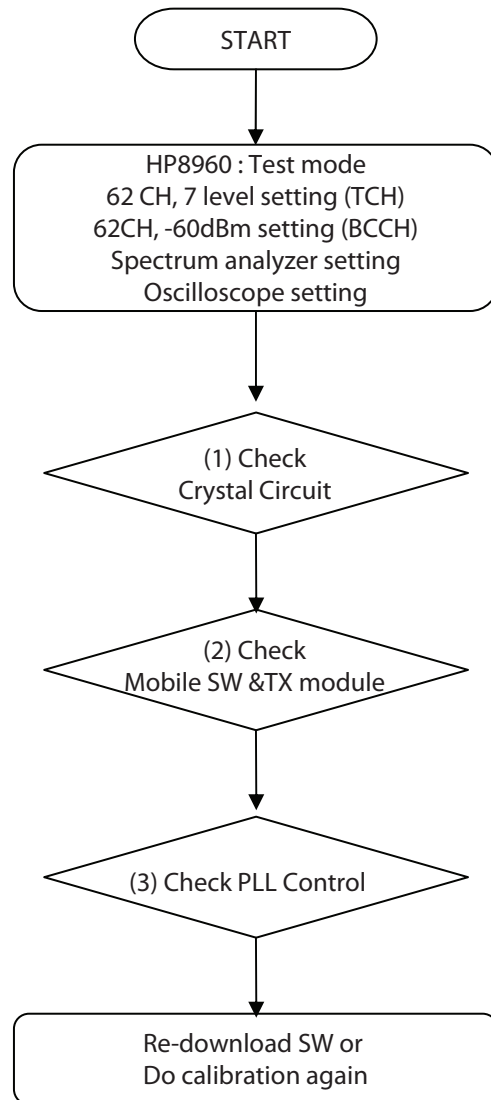
Figure 4.1

U102	Memory(512NOR/128pSDRAM) PF38F5060M0Y3DF
U101(PMB8810)	Main Chip (A-GOLDRADIO)
U301	FEM(Tx Module)
X102	Crystal, 26MHz Clock

4. TROUBLE SHOOTING

4.2 RX Trouble

CHECKING FLOW



(1) Checking Crystal Circuit

TEST POINT

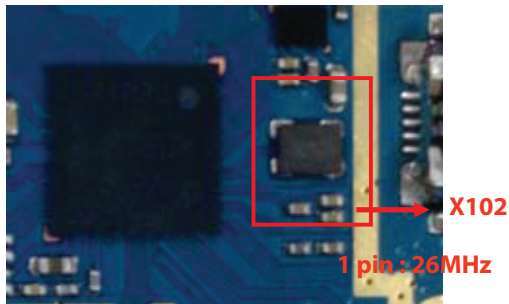
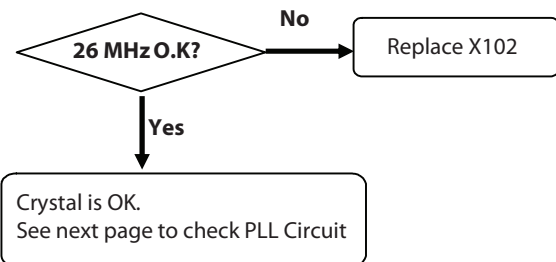


Figure 4.2.1

CHECKING FLOW



CIRCUIT

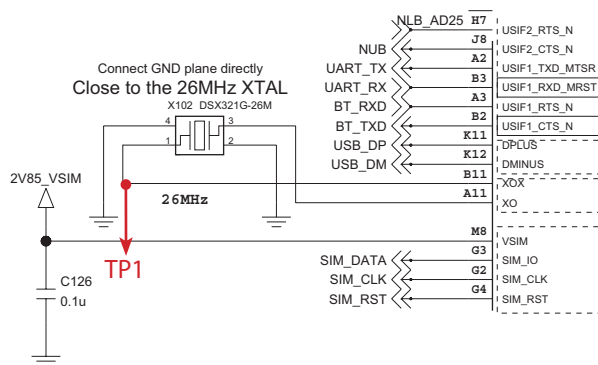


Figure 4.2.2

WAVEFORM

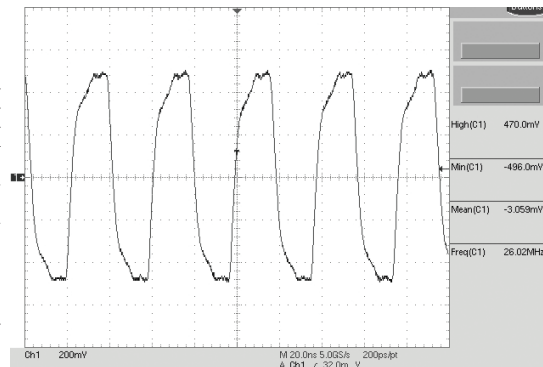


Figure 4.2.3

4. TROUBLE SHOOTING

(2) Checking Mobile SW & FEM

TEST POINT

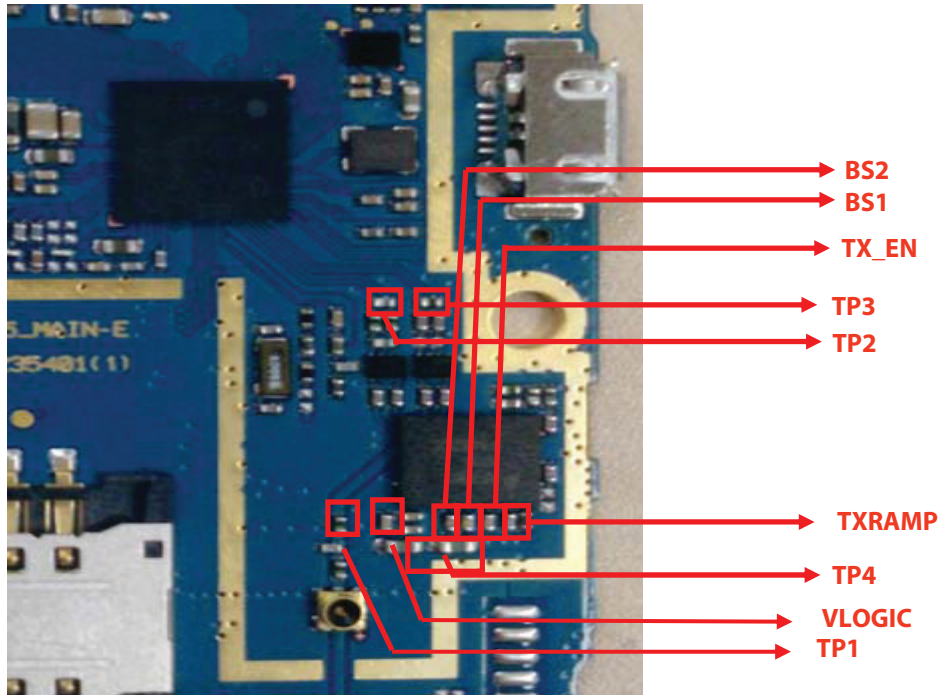
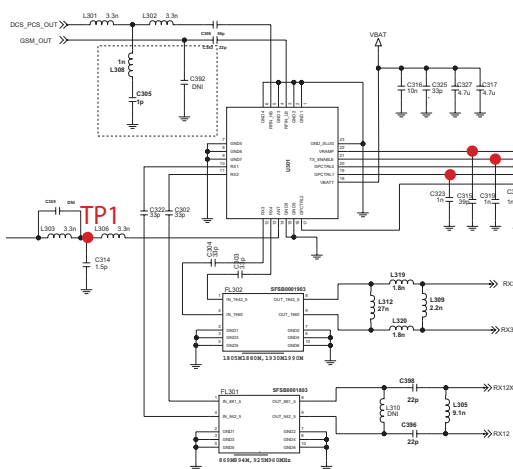


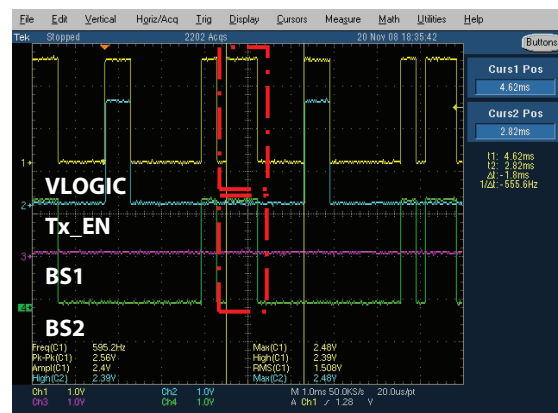
Figure 4.2.4

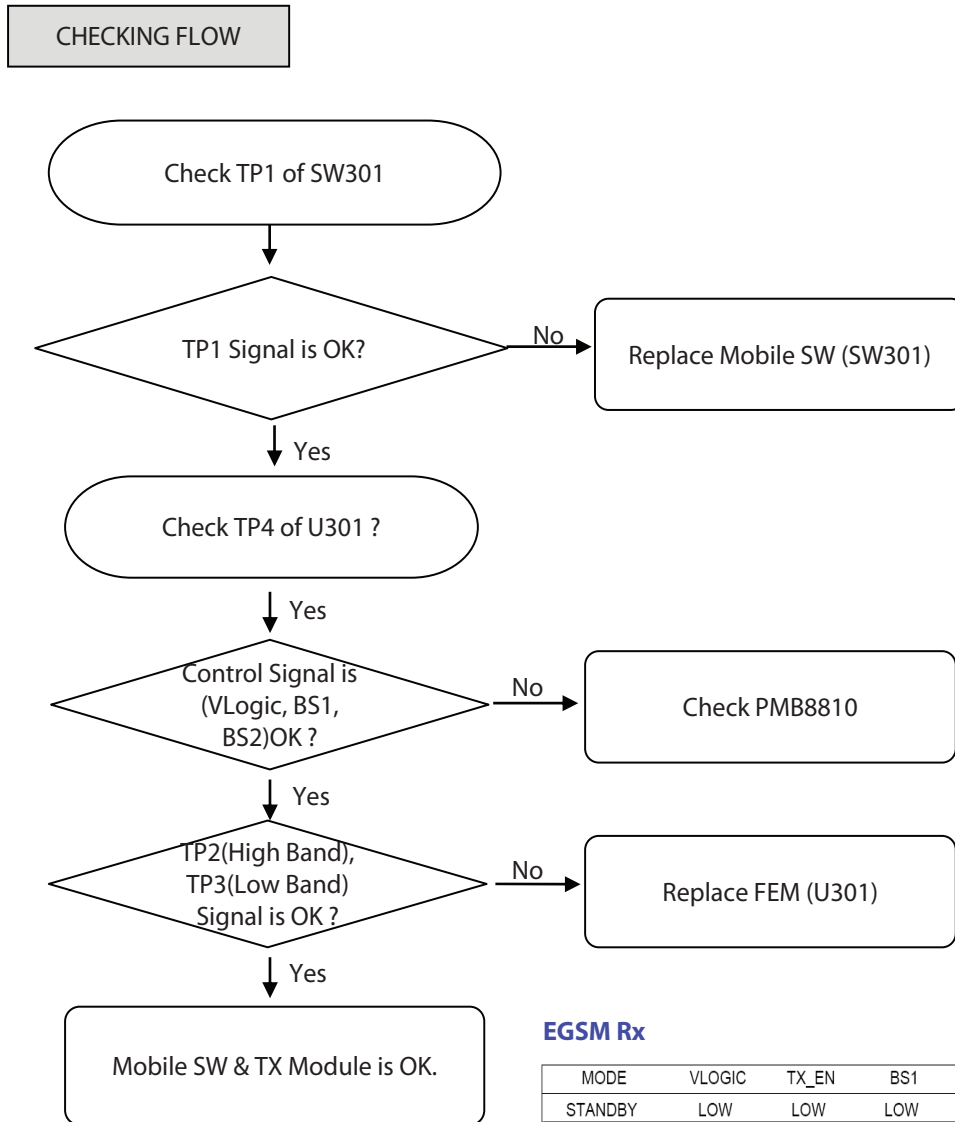
CIRCUIT



CONTROL LOGIC

EGSM Rx





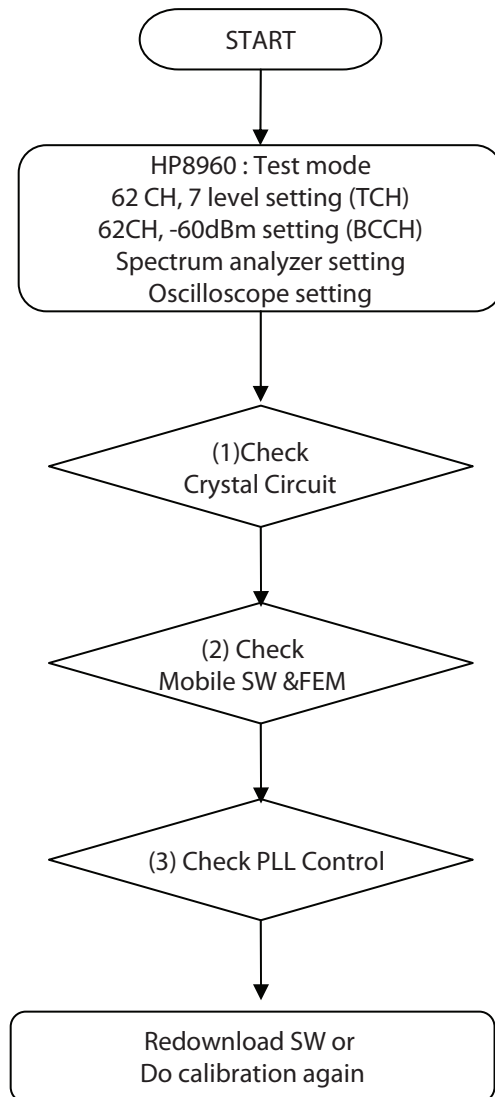
EGSM Rx

MODE	VLOGIC	TX_EN	BS1	BS2
STANDBY	LOW	LOW	LOW	LOW
EGSM_RX	HIGH	LOW	LOW	LOW
GSM850_RX	LOW	LOW	LOW	HIGH
PCS_RX	LOW	LOW	HIGH	HIGH
DCS_RX	LOW	LOW	HIGH	LOW
LB_TX	LOW	HIGH	LOW	HIGH
HB_TX	LOW	HIGH	HIGH	HIGH

4. TROUBLE SHOOTING

4.3 TX Trouble

CHECKING FLOW



(1) Checking Crystal Circuit

TEST POINT

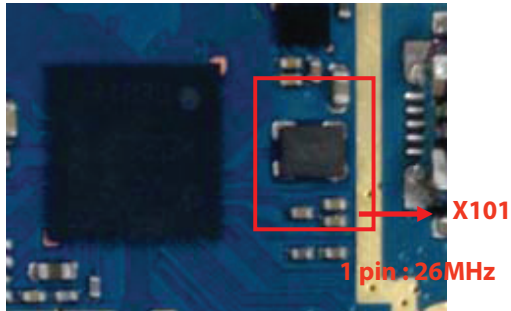
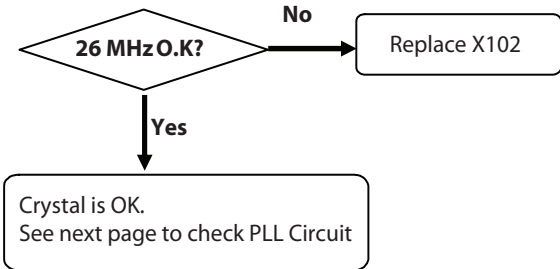


Figure 4.3.1

CHECKING FLOW



CIRCUIT

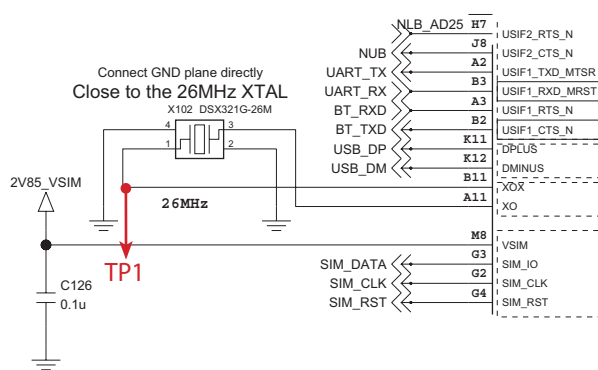


Figure 4.3.2

WAVEFORM

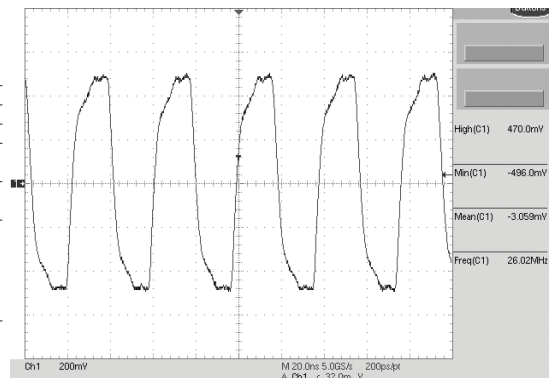
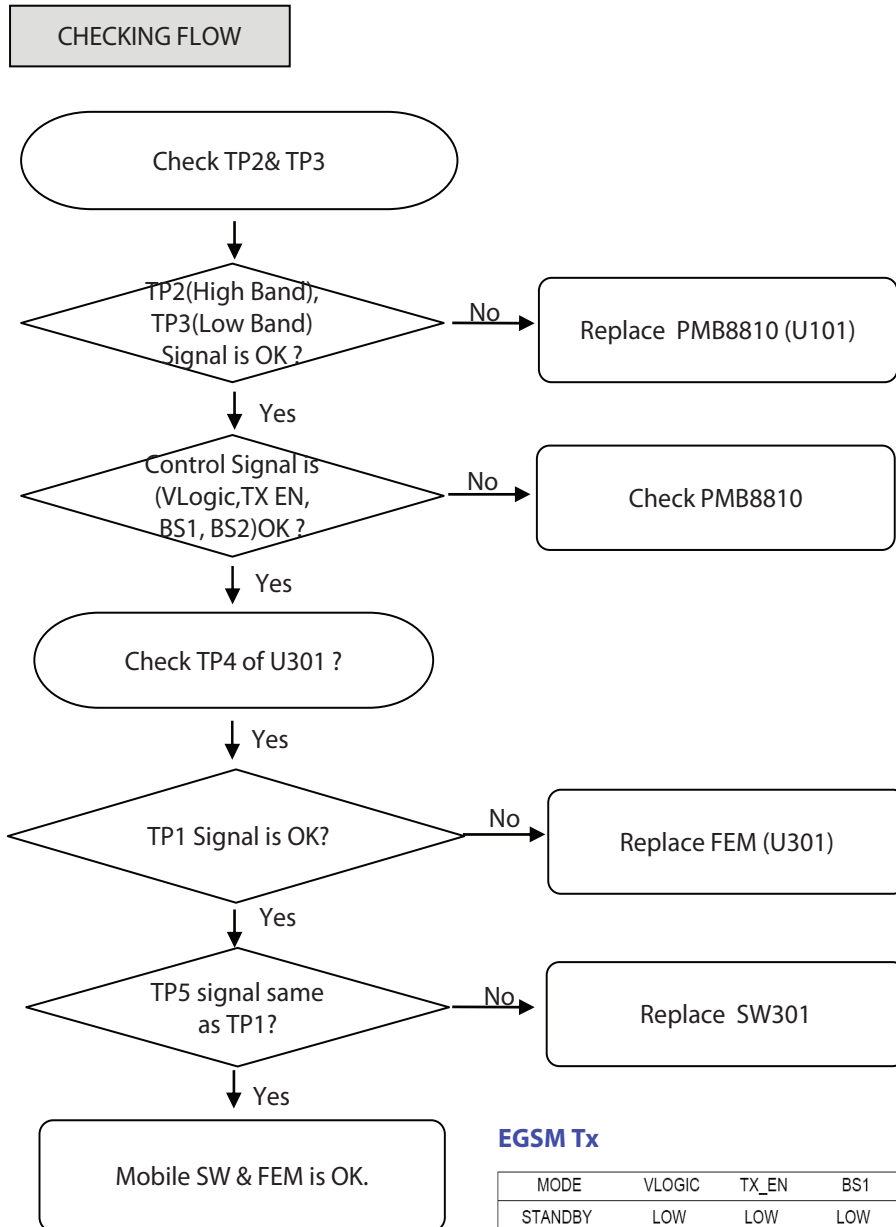


Figure 4.3.3

TEST POINT





EGSM Tx

MODE	VLOGIC	TX_EN	BS1	BS2
STANDBY	LOW	LOW	LOW	LOW
EGSM_RX	HIGH	LOW	LOW	LOW
GSM850_RX	LOW	LOW	LOW	HIGH
PCS_RX	LOW	LOW	HIGH	HIGH
DCS_RX	LOW	LOW	HIGH	LOW
LB_TX	LOW	HIGH	LOW	HIGH
HB_TX	LOW	HIGH	HIGH	HIGH

4. TROUBLE SHOOTING

4.4 Power On Trouble

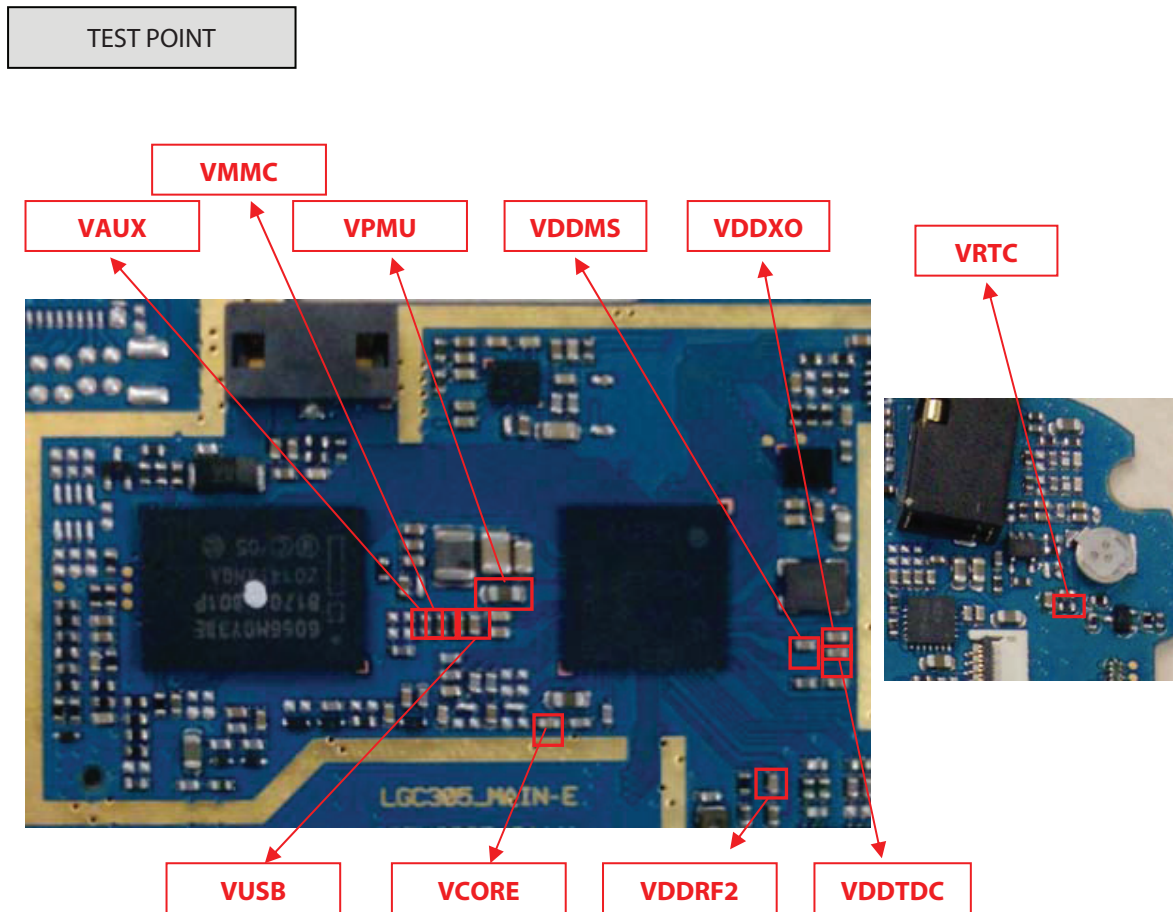
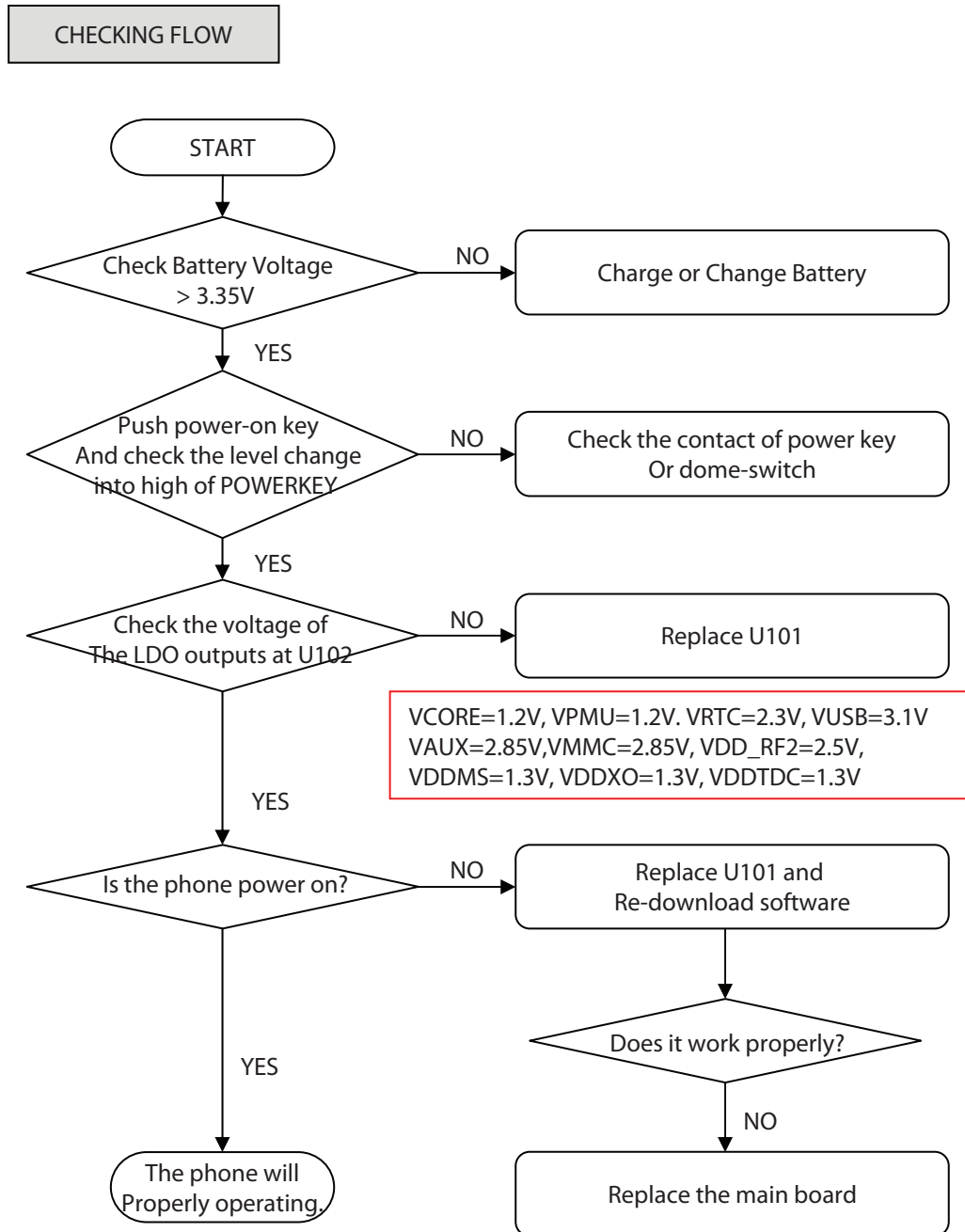


Figure 4.1

CIRCUIT



4. TROUBLE SHOOTING



4.5 Charging Trouble

TEST POINT

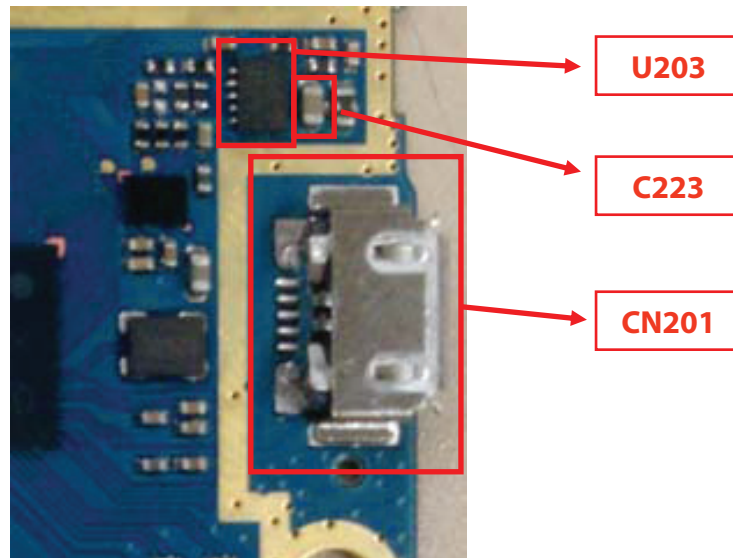
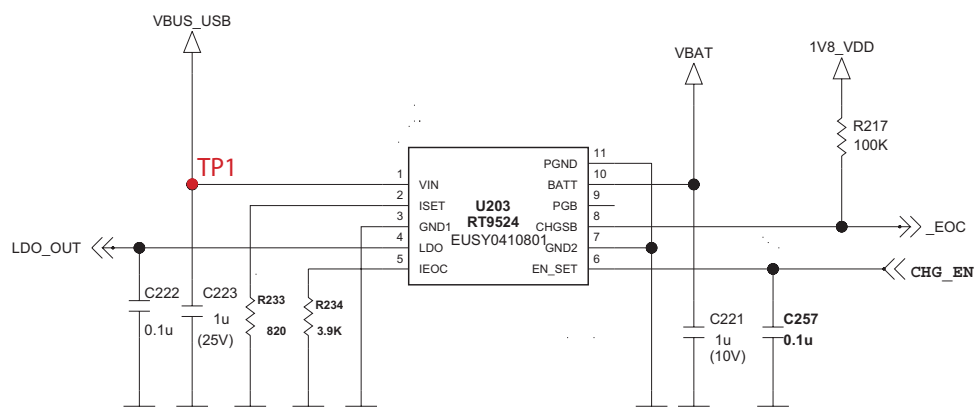


Figure 4.5

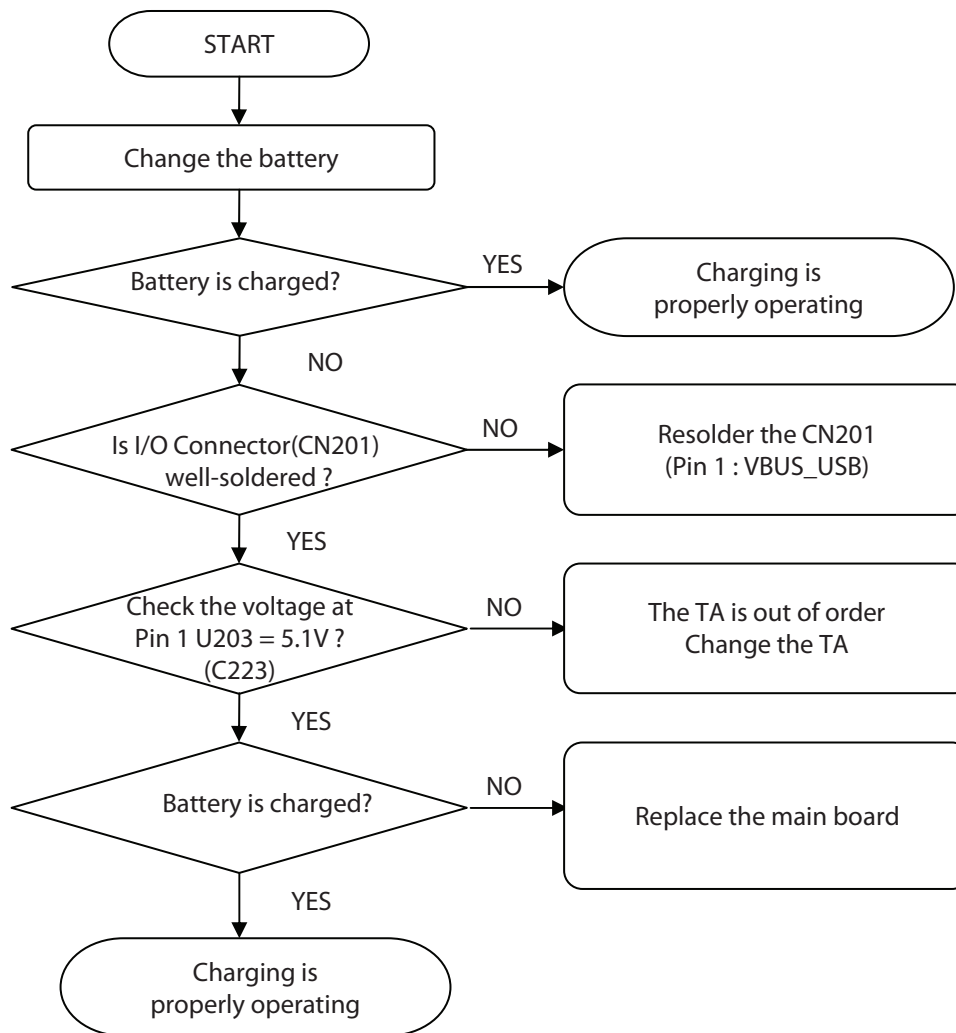
CIRCUIT

CHARGING IC



4. TROUBLE SHOOTING

CHECKING FLOW



4.6 Vibrator Trouble

TEST POINT

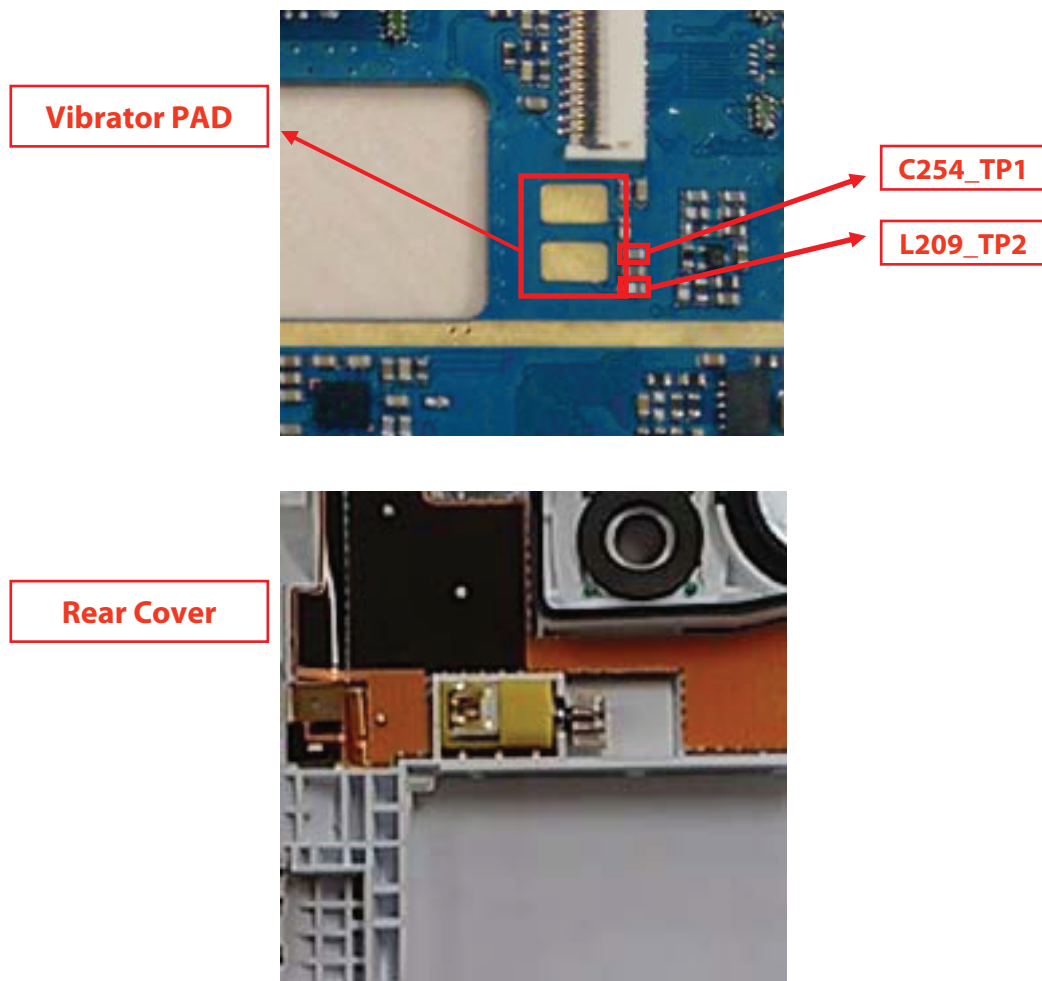
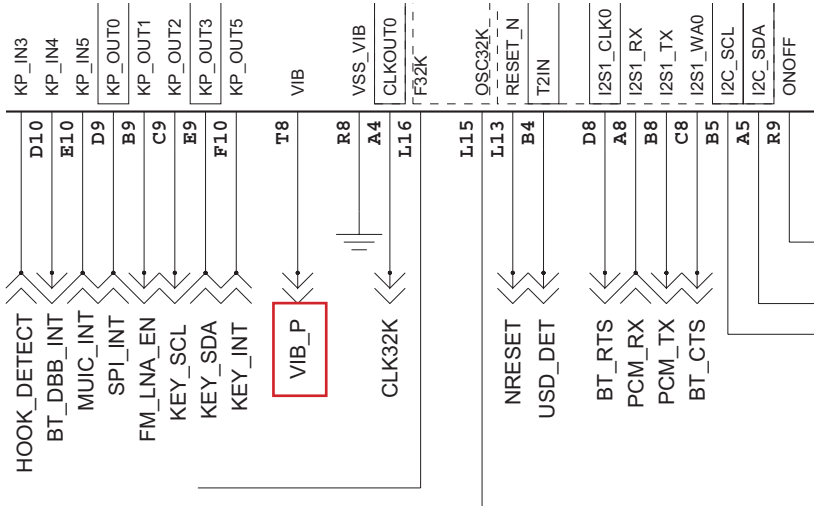


Figure 4.6

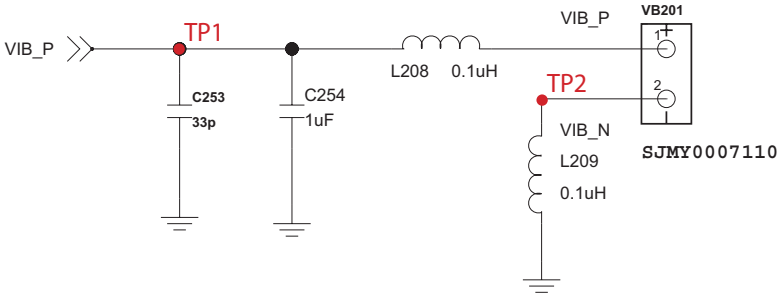
4. TROUBLE SHOOTING

CIRCUIT

Main IC (U101)



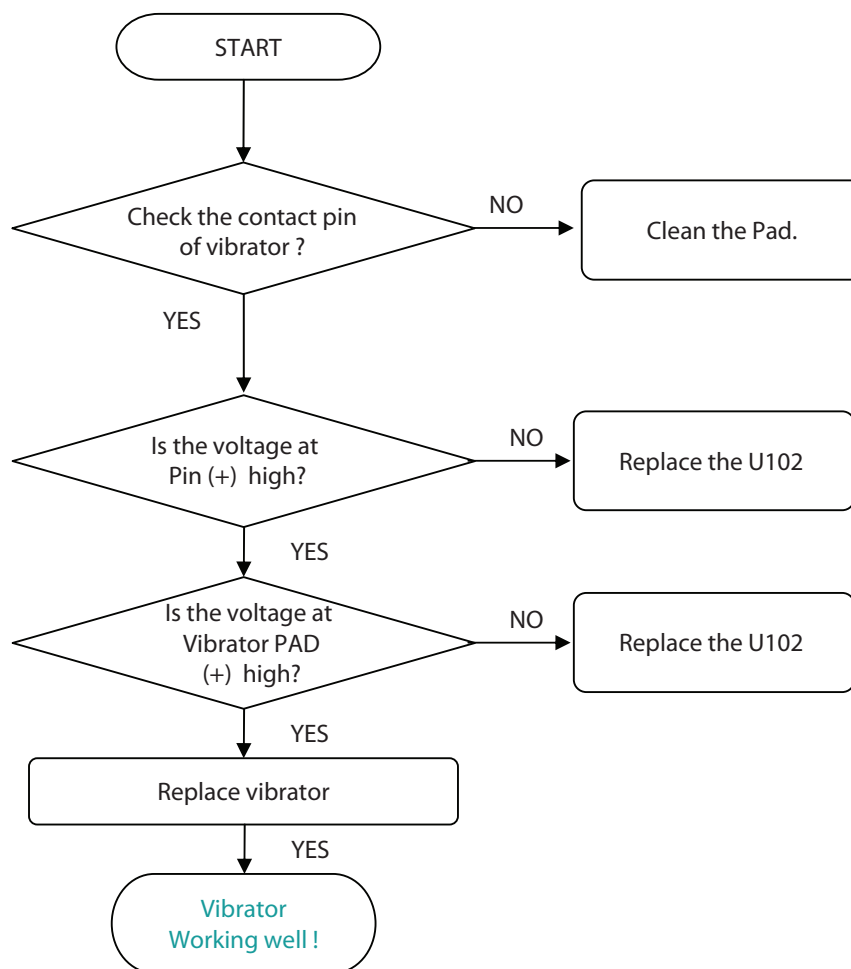
MOTOR



4. TROUBLE SHOOTING

CHECKING FLOW

SETTING : Enter the engineering mode, and set vibrator on at vibration of BB test menu



4. TROUBLE SHOOTING

4.7 LCD Trouble

TEST POINT

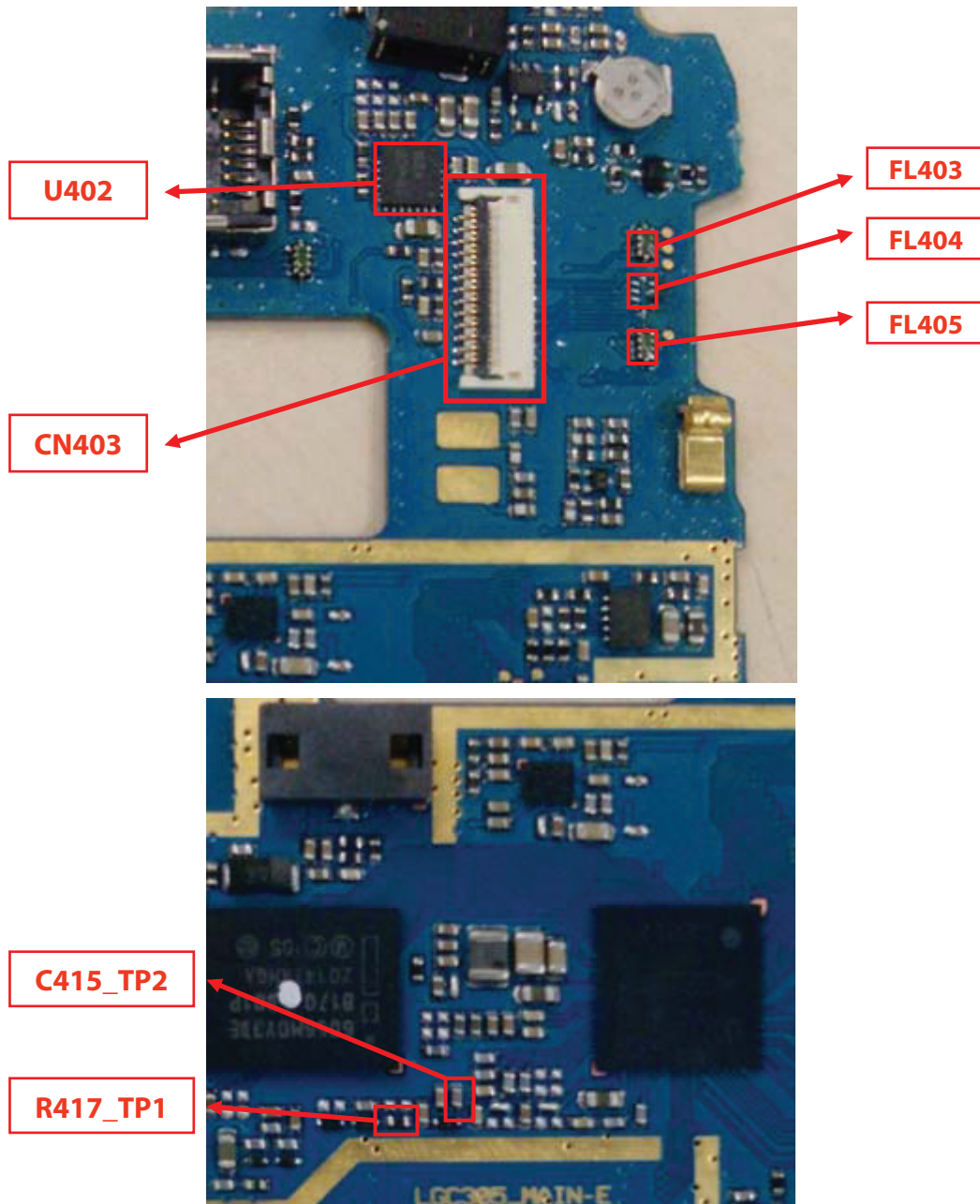
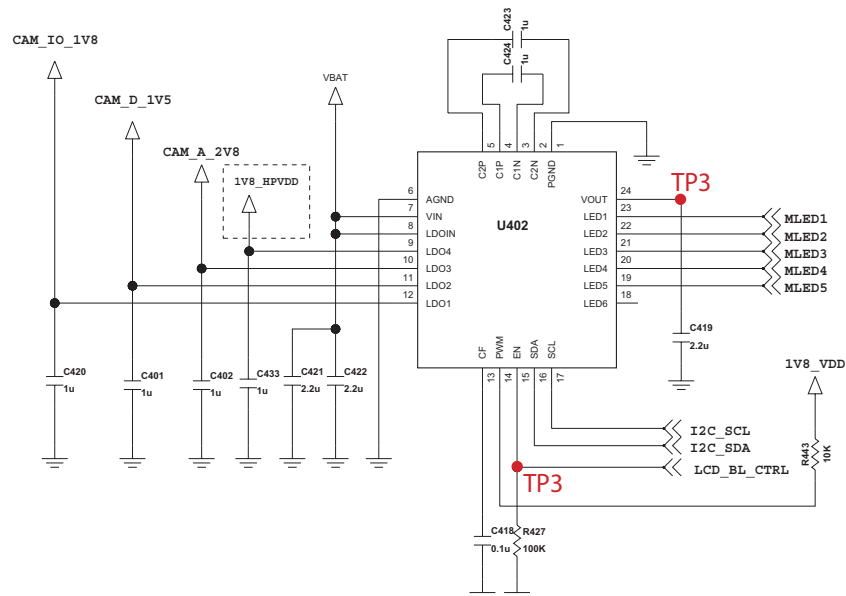
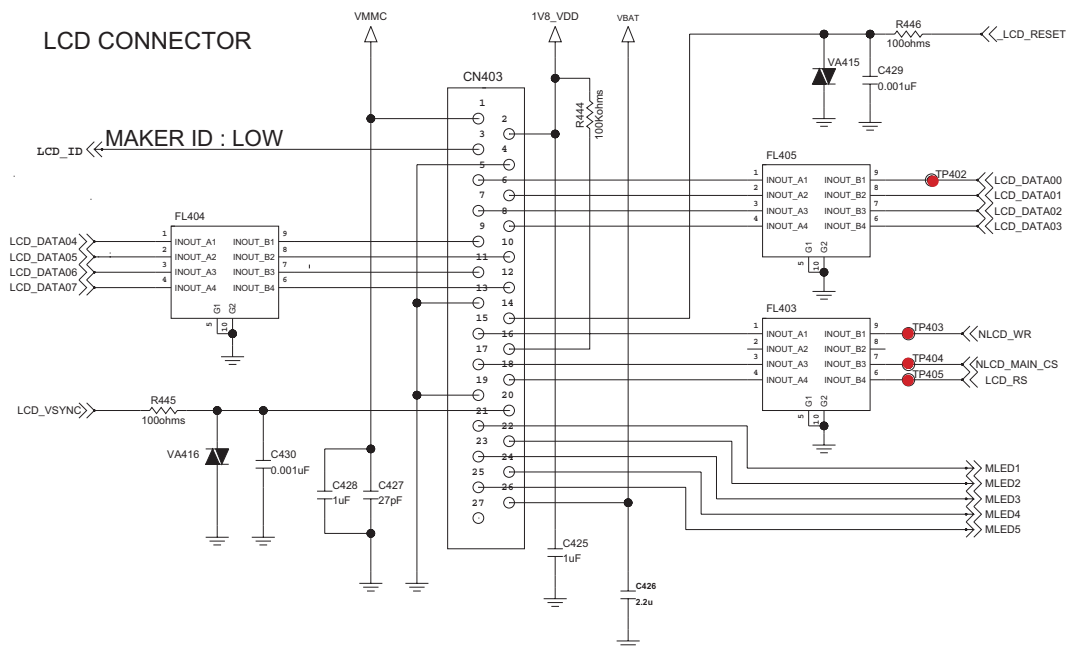


Figure 4.7

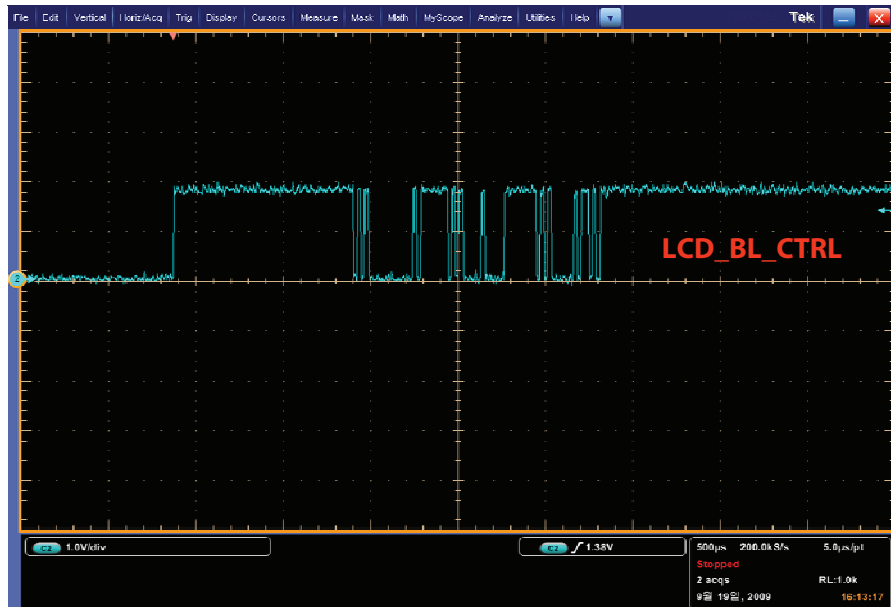
4. TROUBLE SHOOTING

CIRCUIT

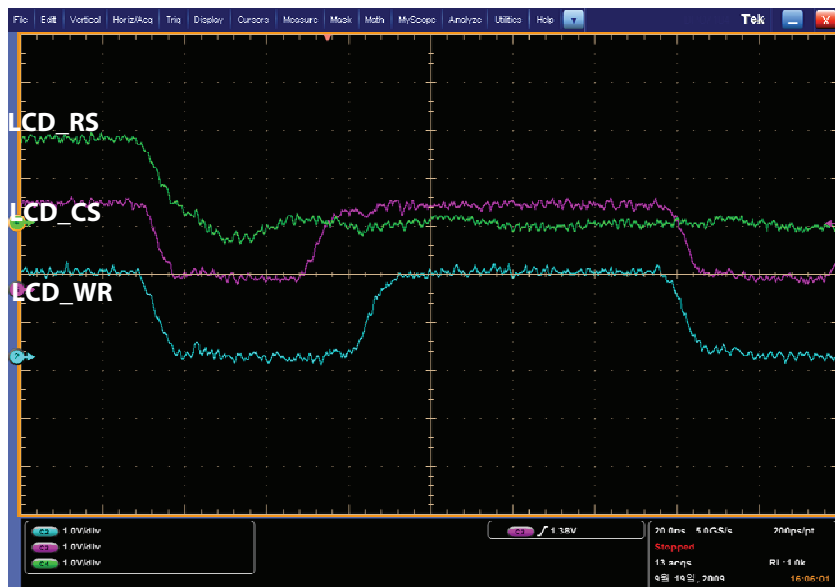


4. TROUBLE SHOOTING

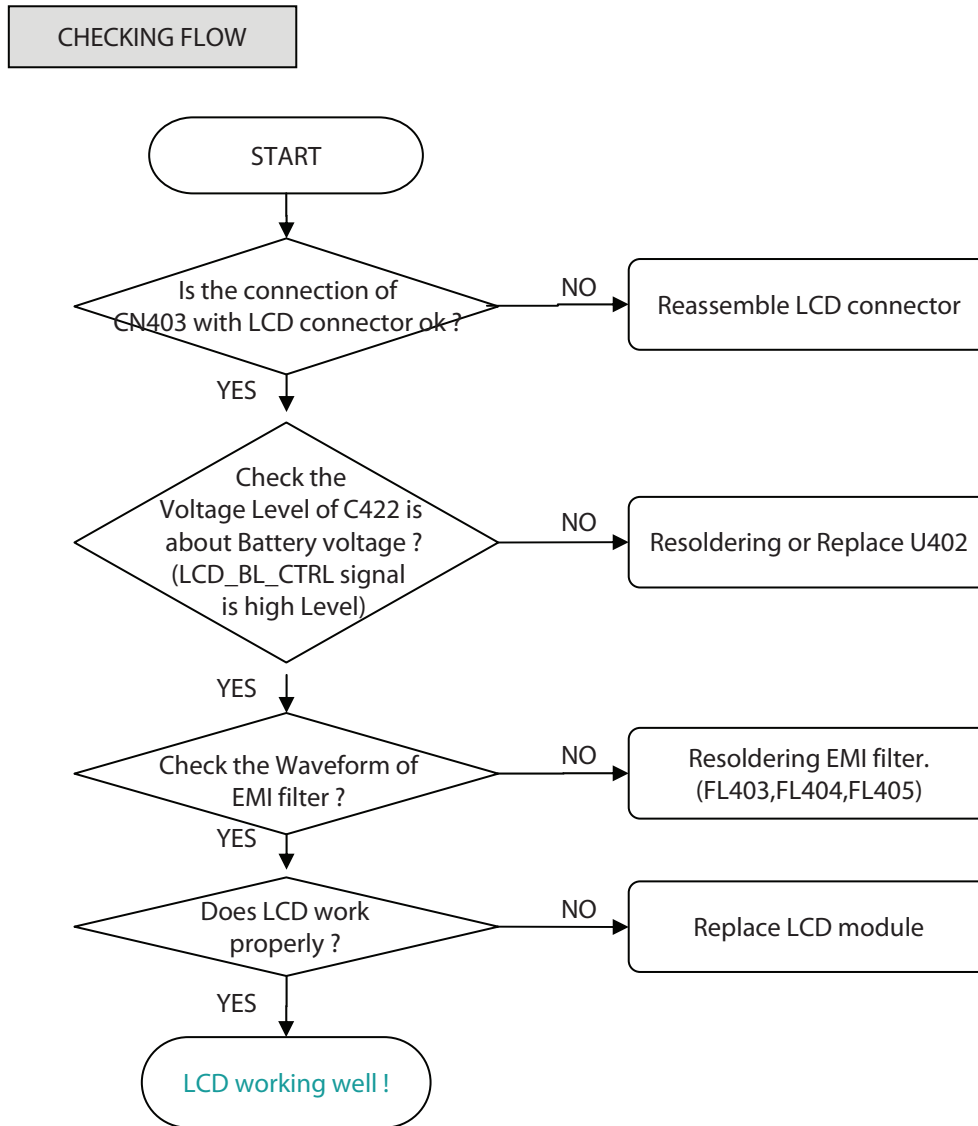
Waveform



Graph 4.7.1. LCD Backlight Control Signal Waveform



Graph 4.7.2. LCD Data Waveform



4. TROUBLE SHOOTING

4.8 Camera Trouble

TEST POINT

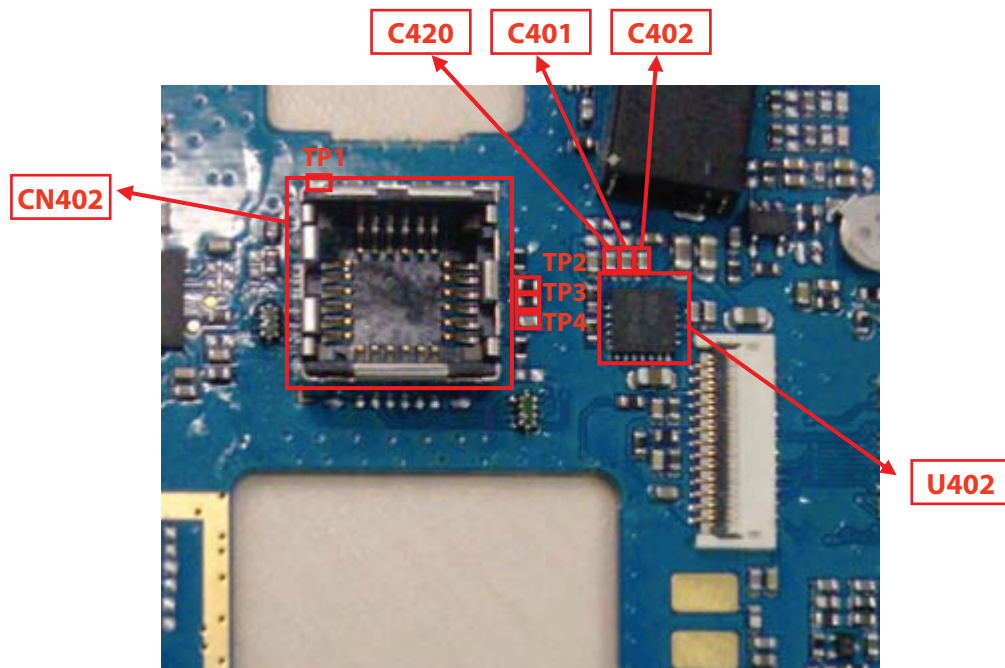
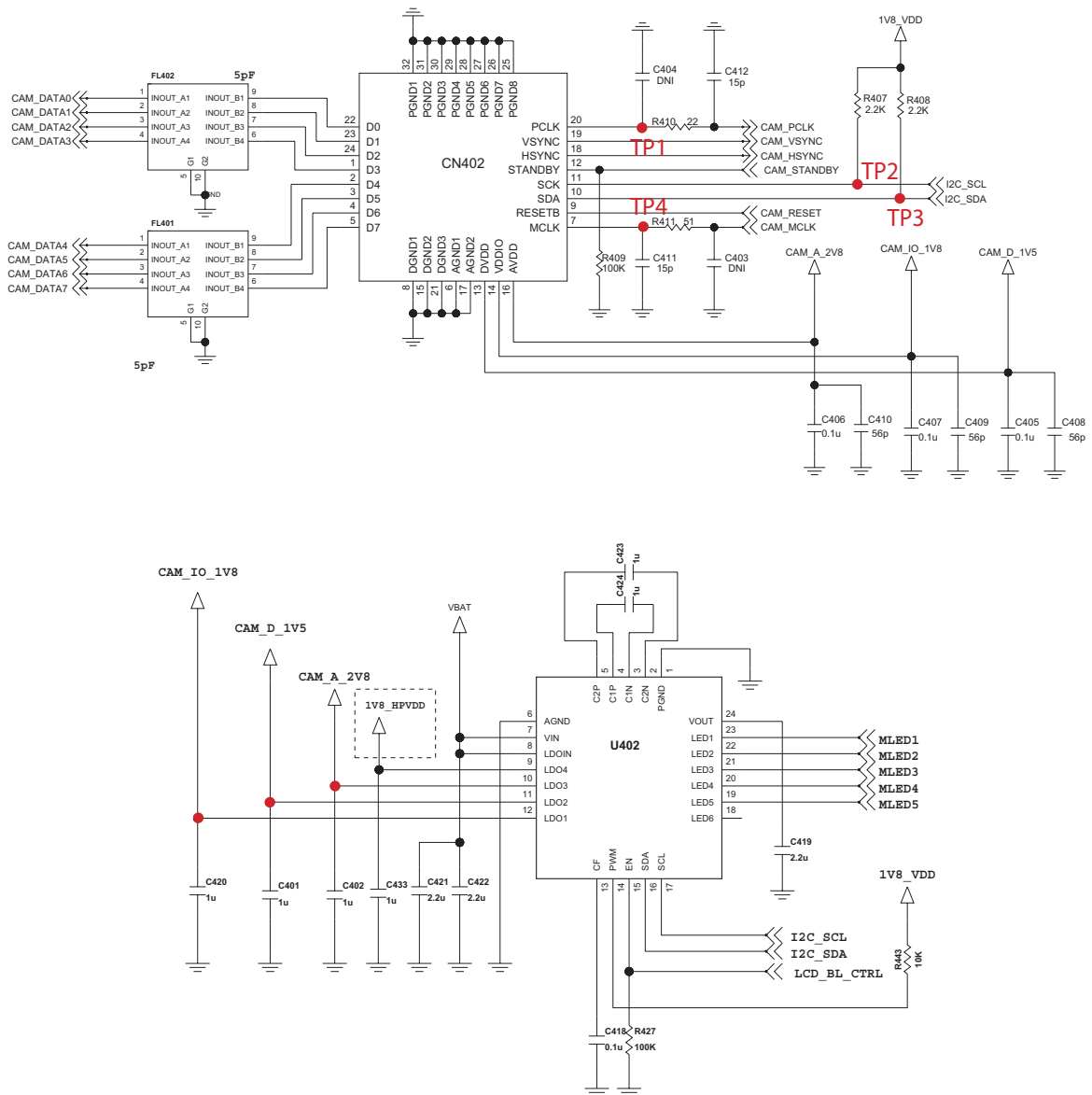


Figure 4.8

4. TROUBLE SHOOTING

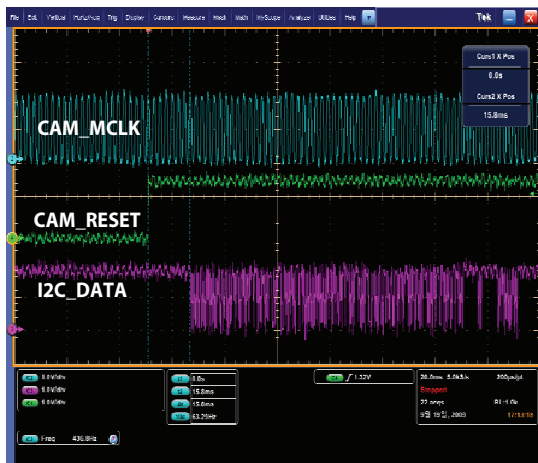
CIRCUIT

CAMERA INTERFACE

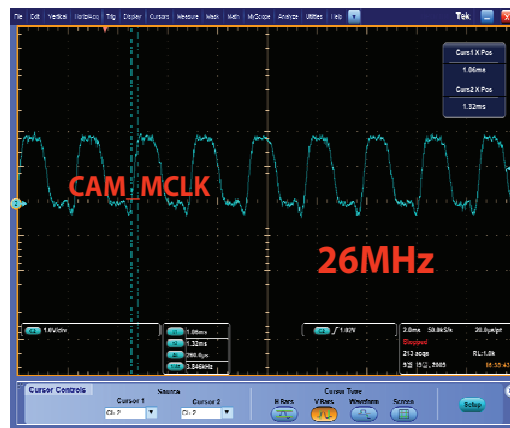


4. TROUBLE SHOOTING

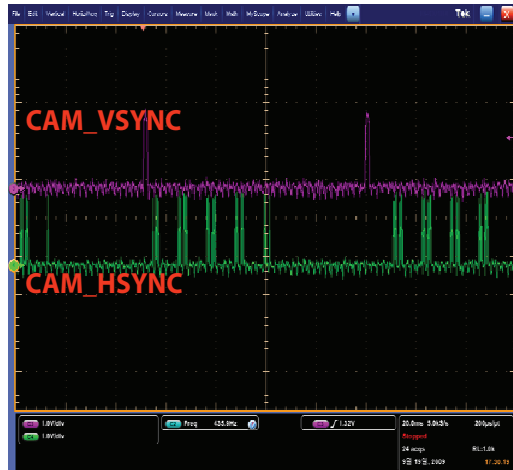
Waveform



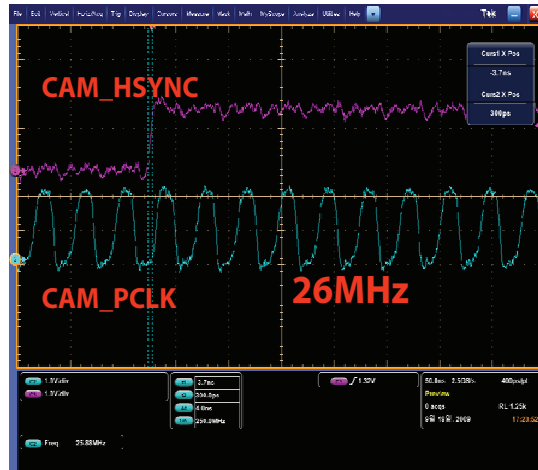
Graph 4.8.1. I2C Data Waveform



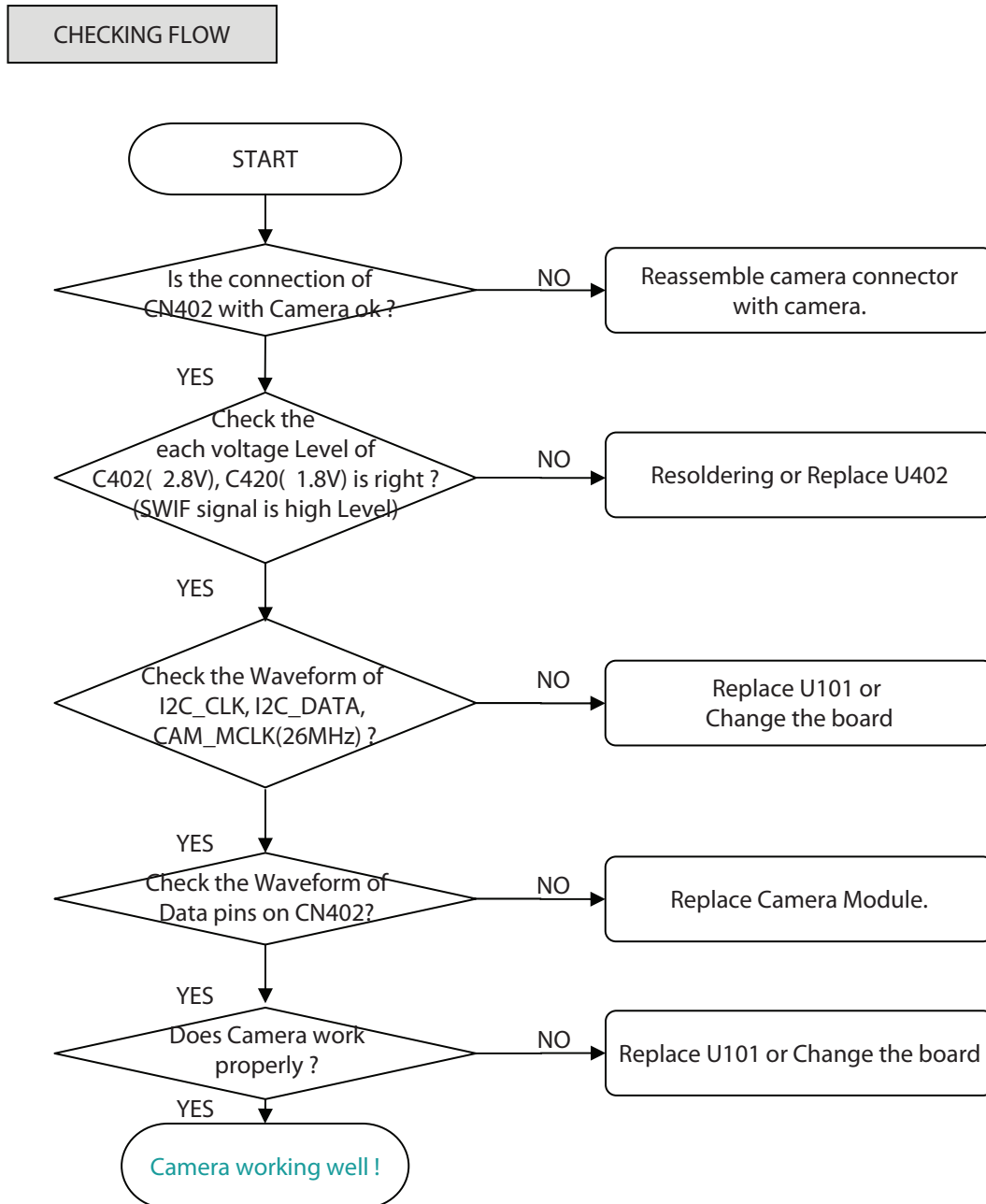
Graph 4.8.2. MCLK Waveform



Graph 4.8.3. CAM_VSYNC vs.
CAM_HSYNC Waveform



Graph 4.8.4. CAM_HSYNC vs.
CAM_PCLK Waveform



4. TROUBLE SHOOTING

4.9 Speaker Trouble

TEST POINT

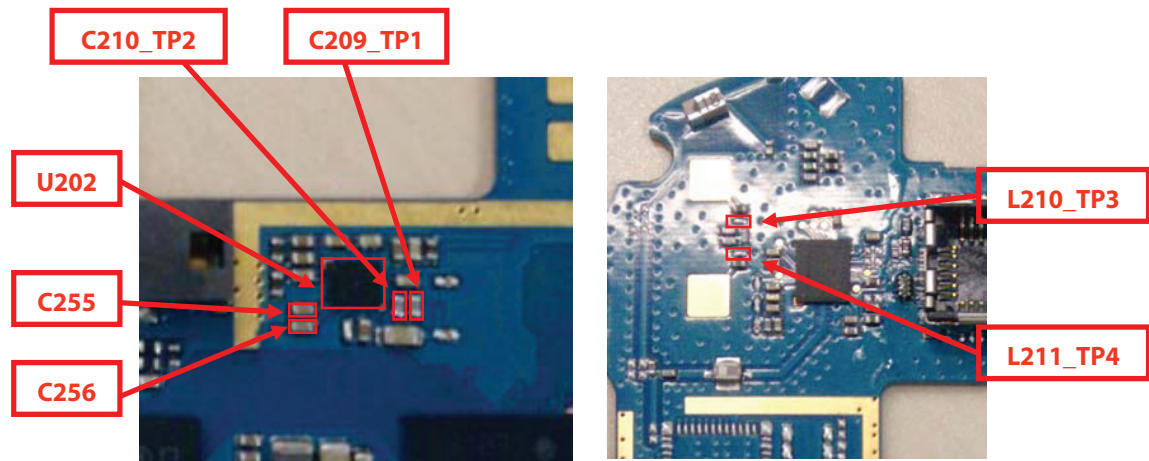
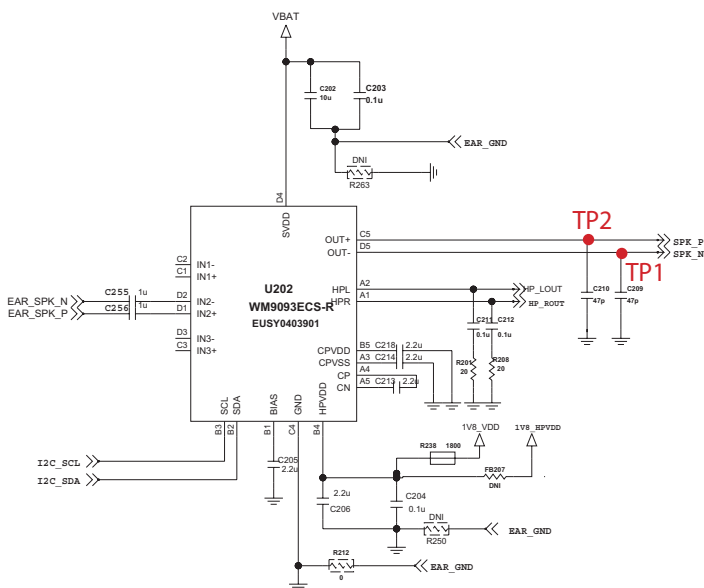
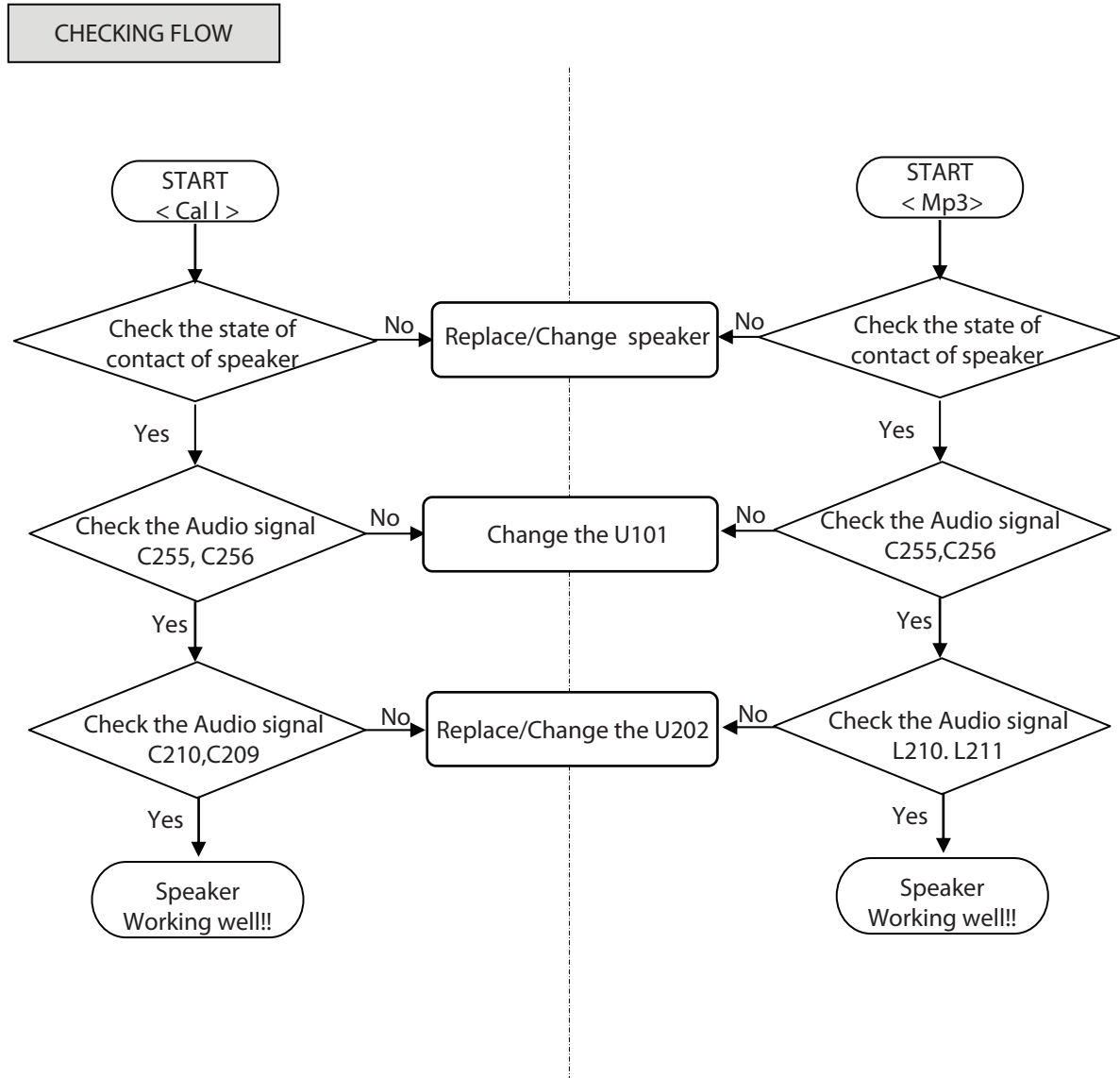


Figure 4.11.1

CIRCUIT

AUDIO AMP SUB SYSTEM & SIGNAL DISTRIBUTOR



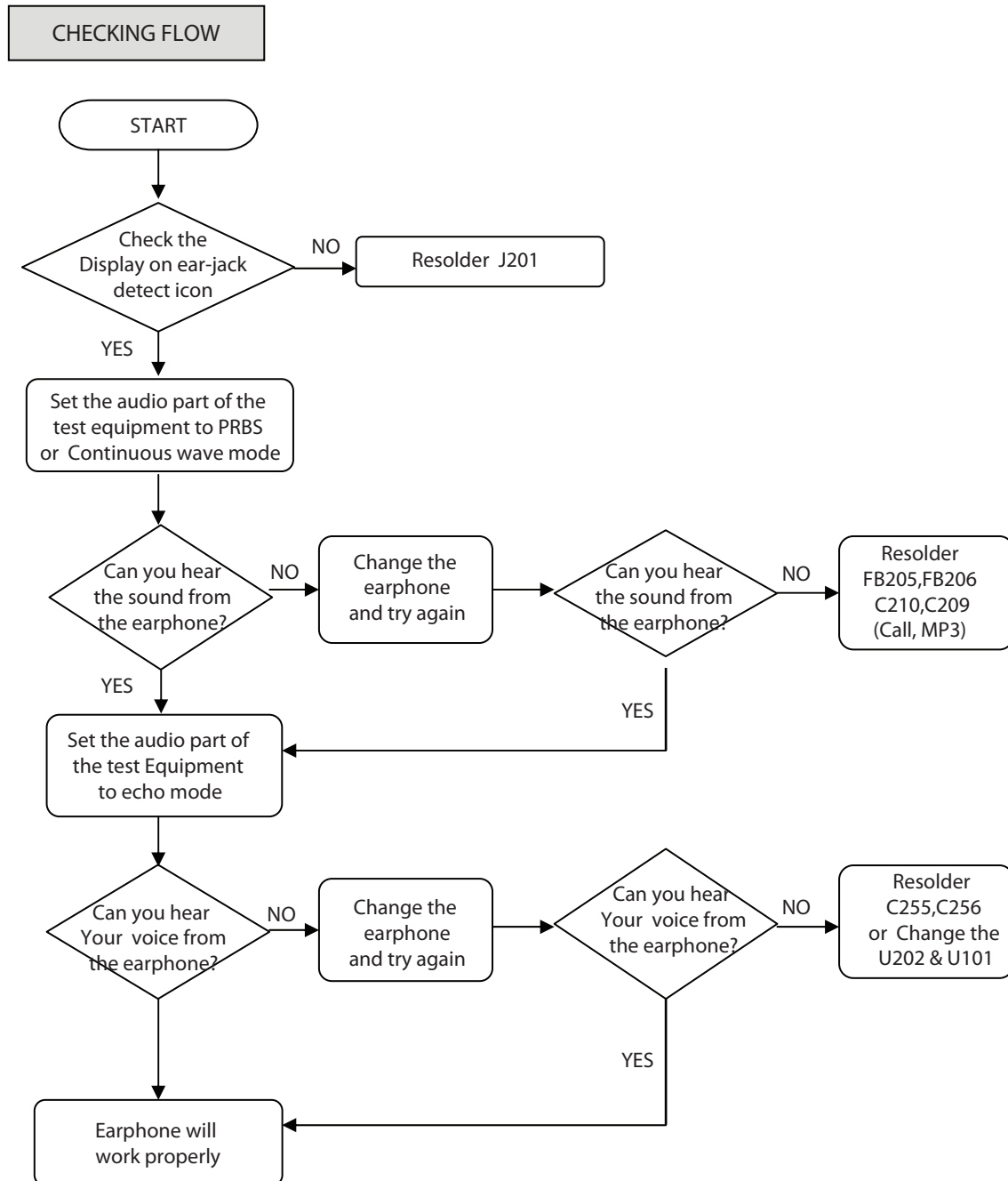


TEST POINT



AUDIO AMP SUB SYSTEM & SIGNAL DISTRIBUTOR





4. TROUBLE SHOOTING

4.11 Receiver Trouble

TEST POINT

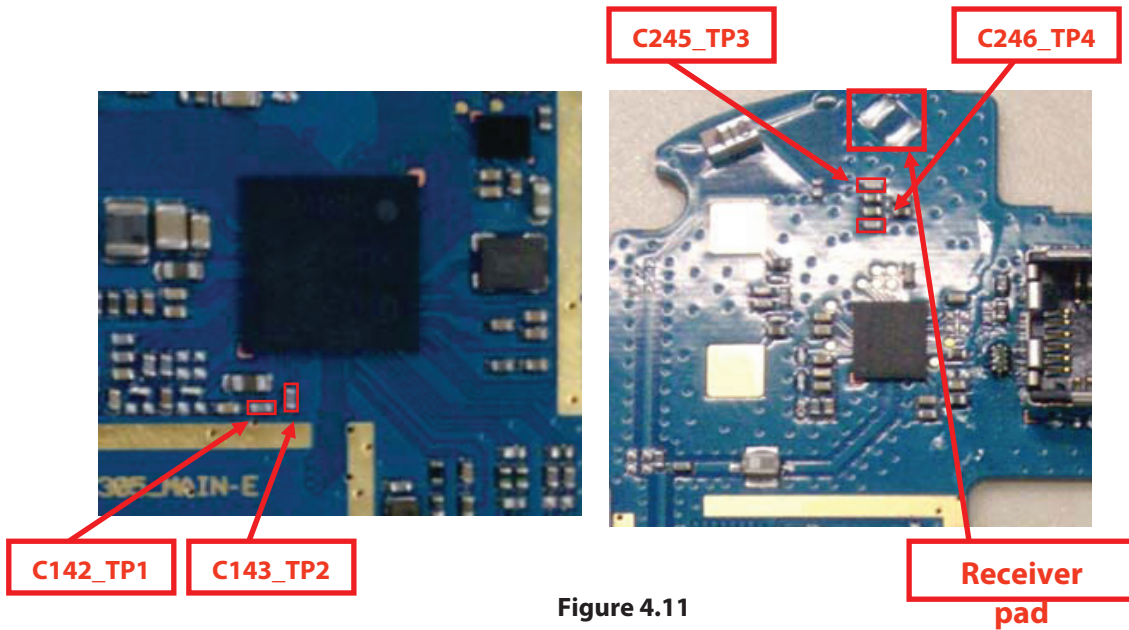
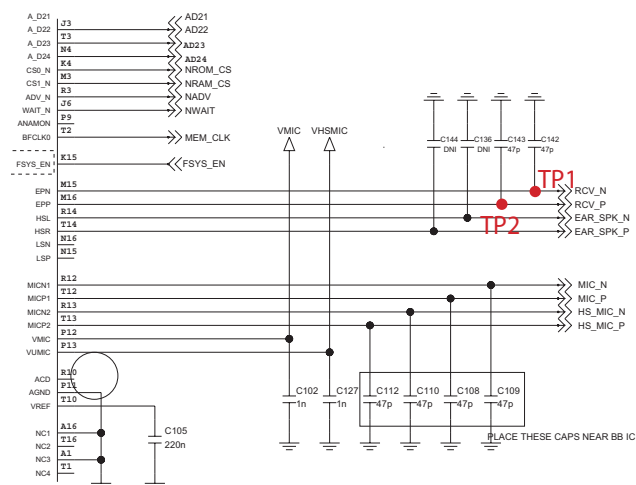
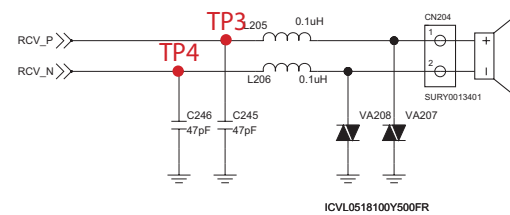


Figure 4.11

CIRCUIT

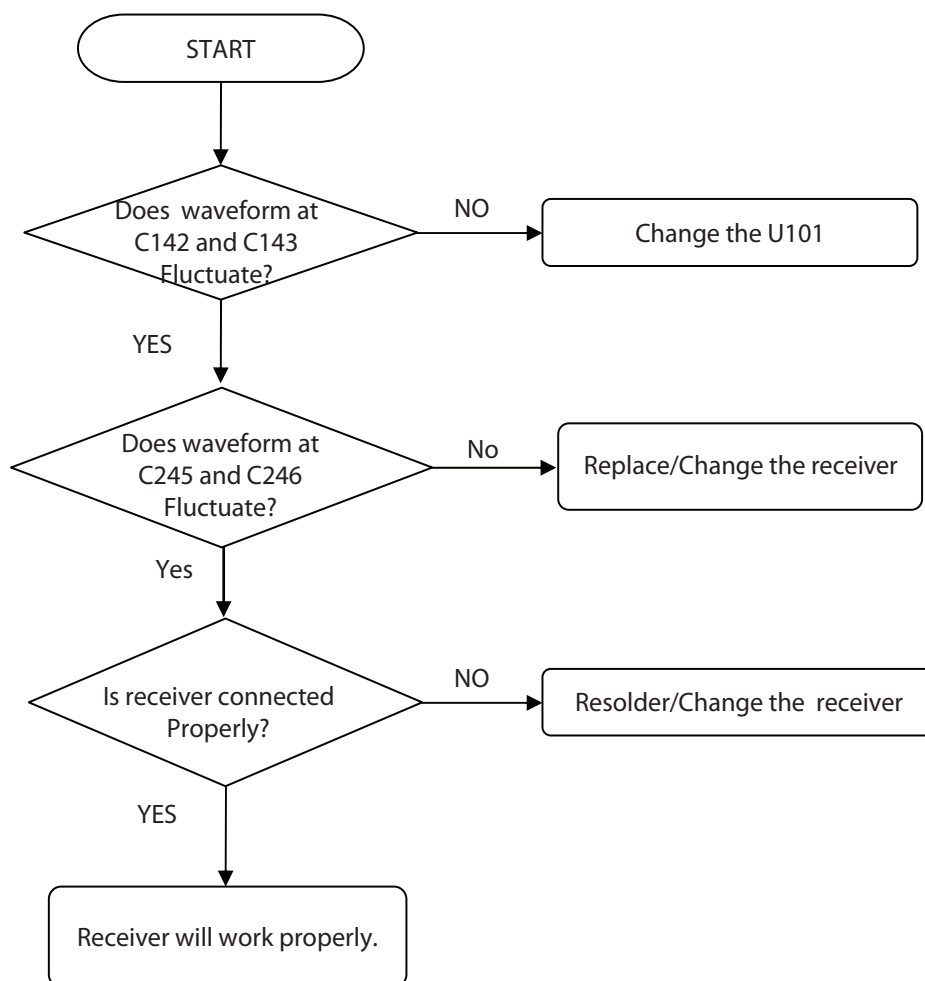


MAIN RECEIVER



CHECKING FLOW

SETTING : After initialize Agilent 8960, Test EGSM900, DCS mode (or GSM850, PCS mode)
Set the property of audio as PRBS or continuous wave. Set the receiving volume of mobile as Max.



4. TROUBLE SHOOTING

4.12 Microphone Trouble

TEST POINT

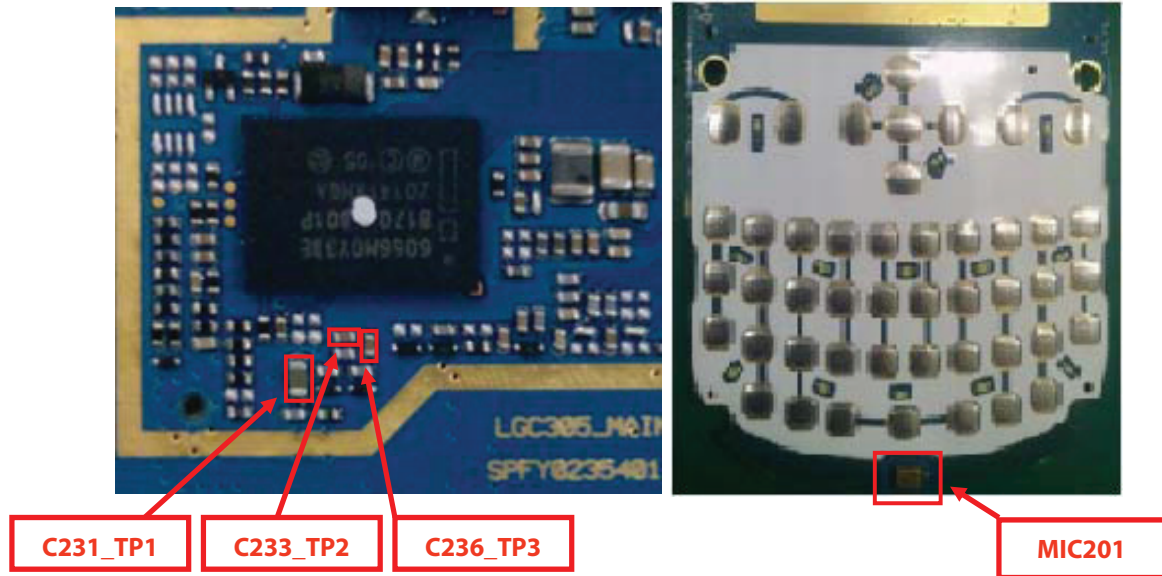
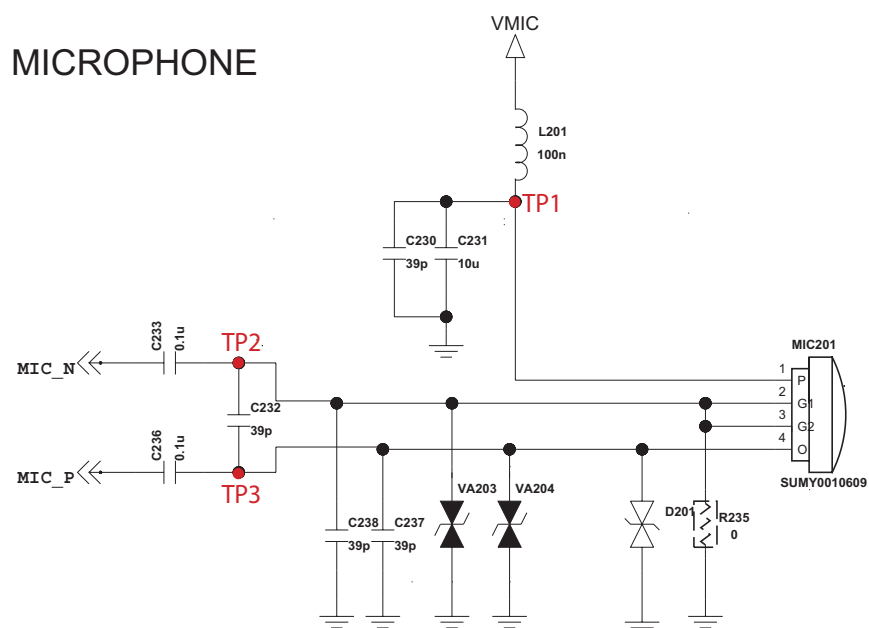


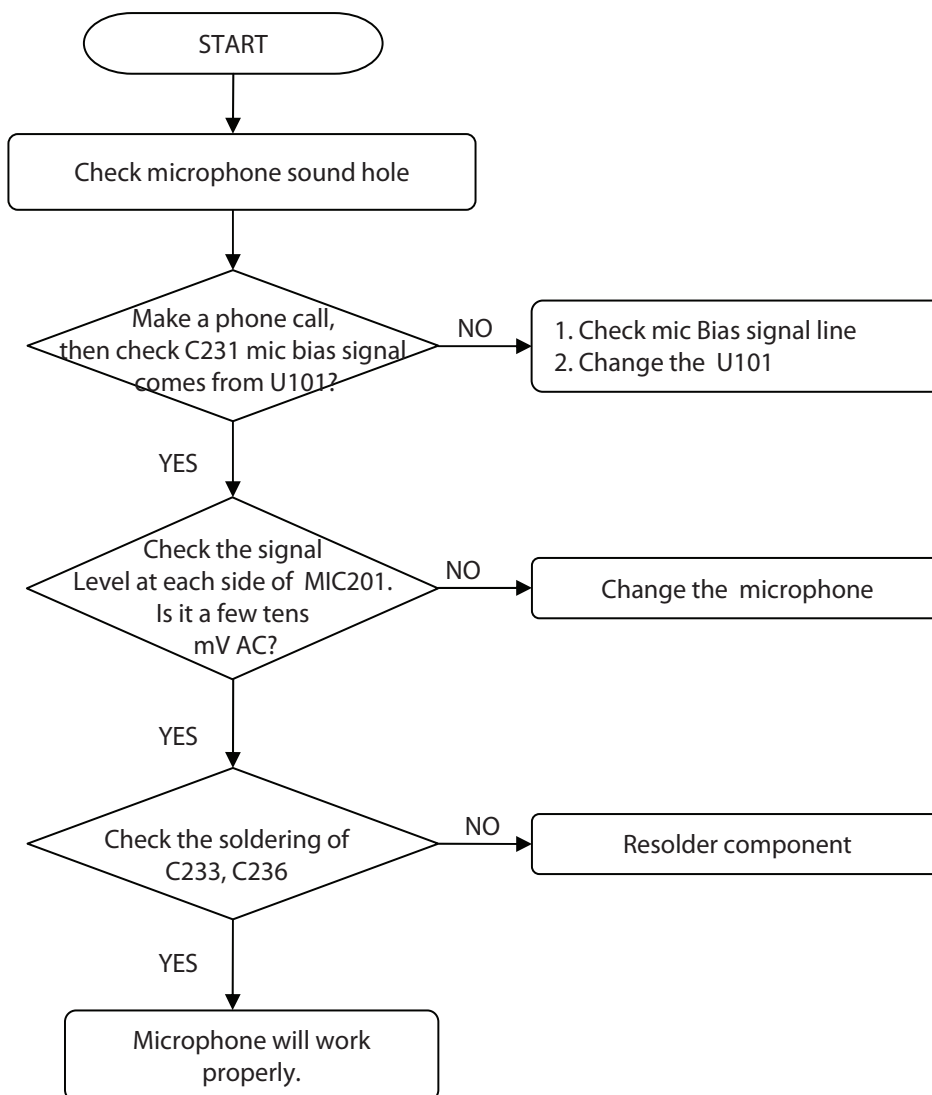
Figure 4.12

CIRCUIT



CHECKING FLOW

SETTING : After initialize Agilent 8960, Test EGSM900, DCS mode (or GSM850, PCS mode)



4. TROUBLE SHOOTING

4.13 SIM Card Interface Trouble

TEST POINT

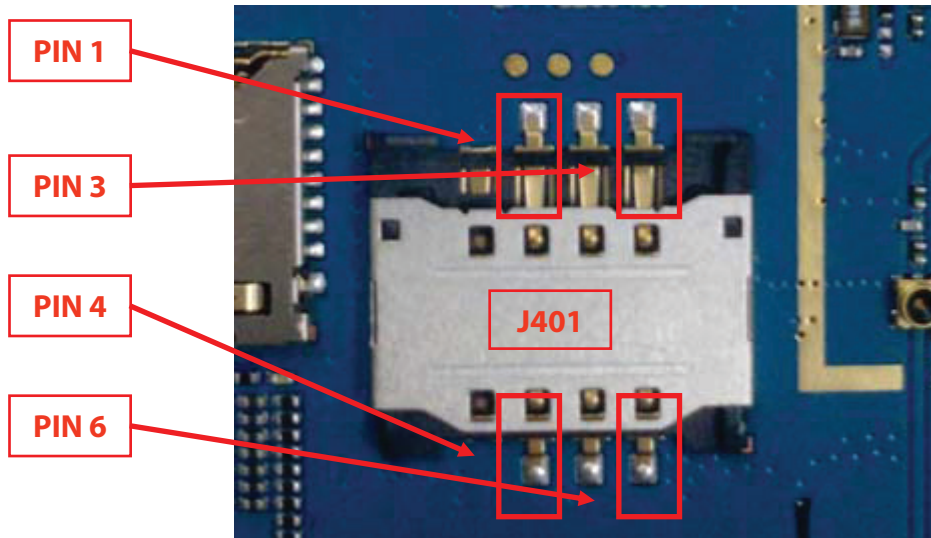
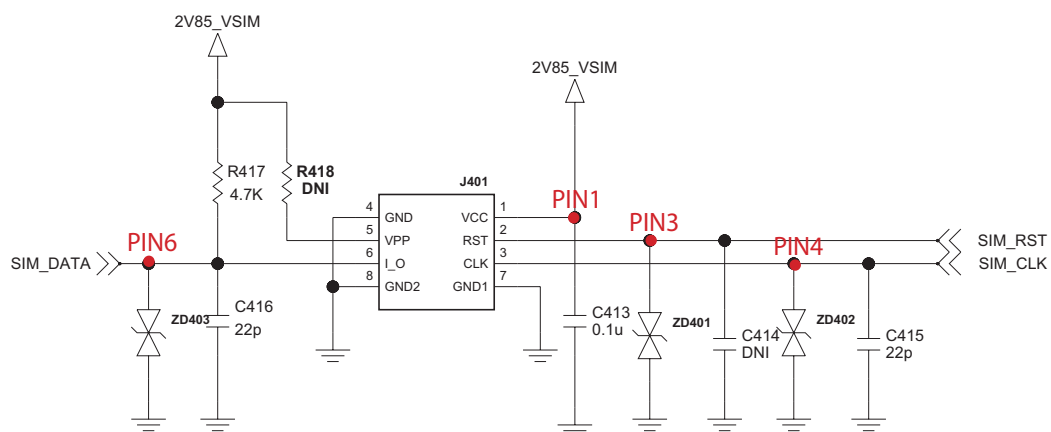


Figure 4.13

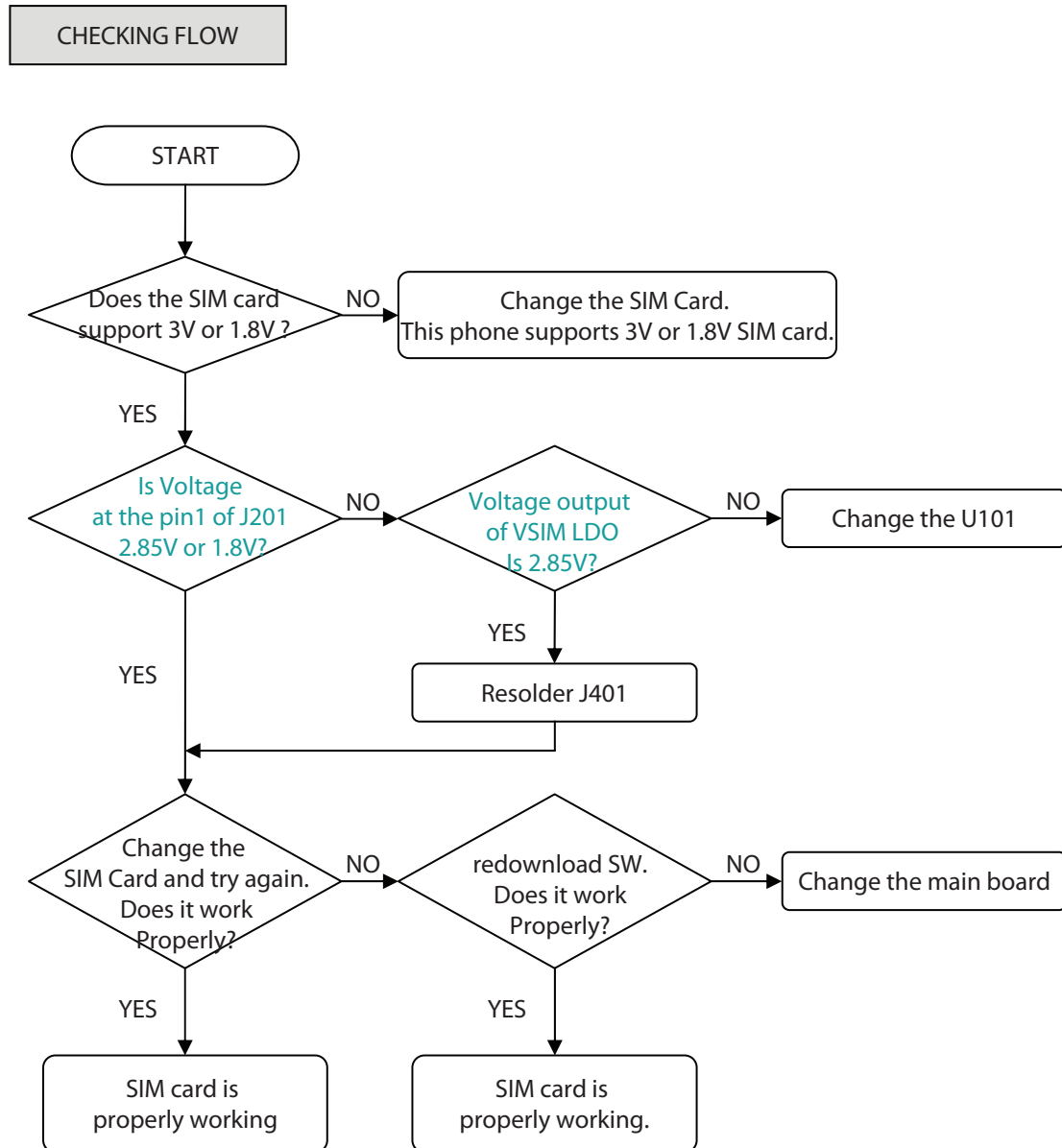
CIRCUIT

SIM_CONNECTOR 1(Default)



ZD200ZD201 is DNI defaultly

These are added for CMCC ESD test



4. TROUBLE SHOOTING

4.14 KEY backlight Trouble

TEST POINT

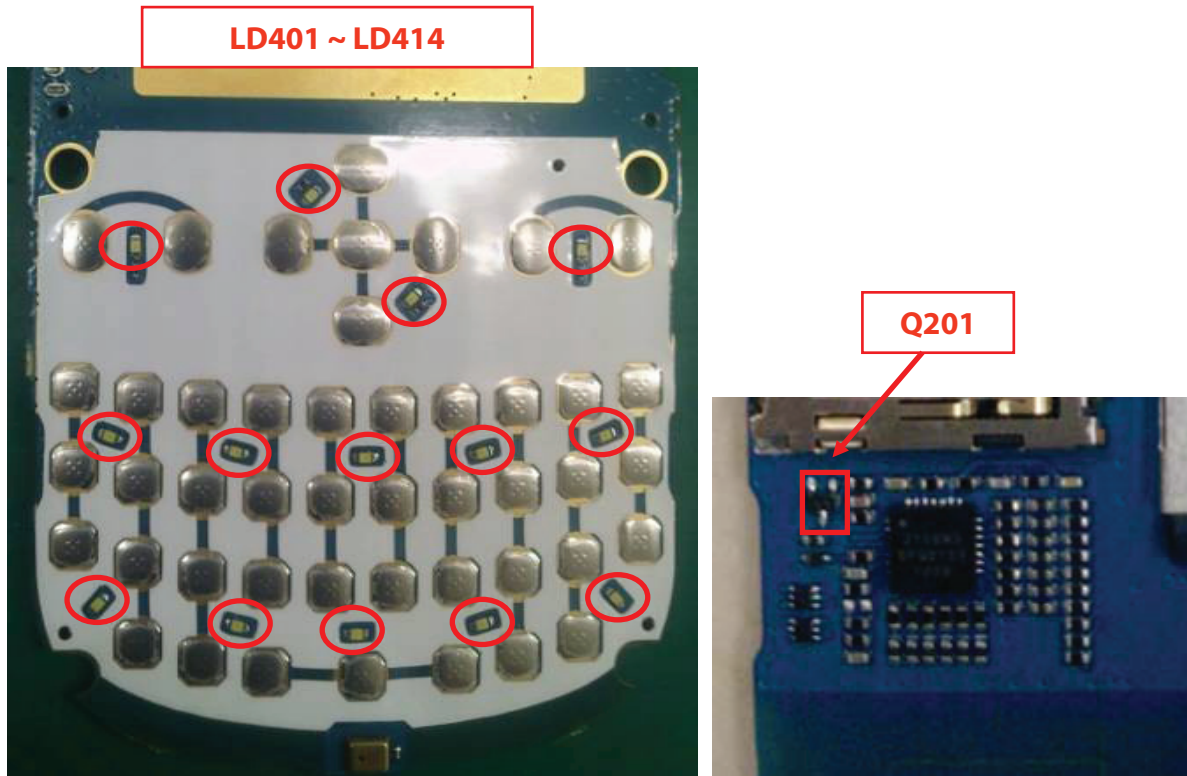
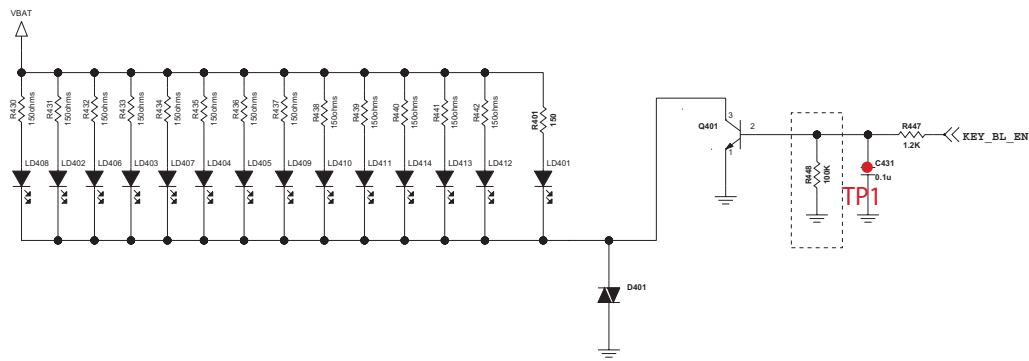
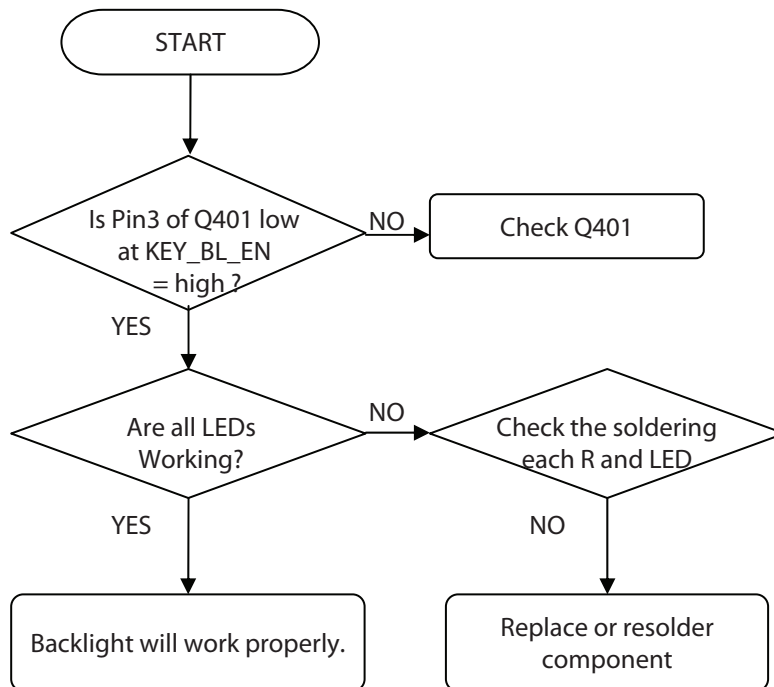


Figure 4.14

CIRCUIT



CHECKING FLOW



4. TROUBLE SHOOTING

4.15 Micro SD (uSD) Trouble

TEST POINT

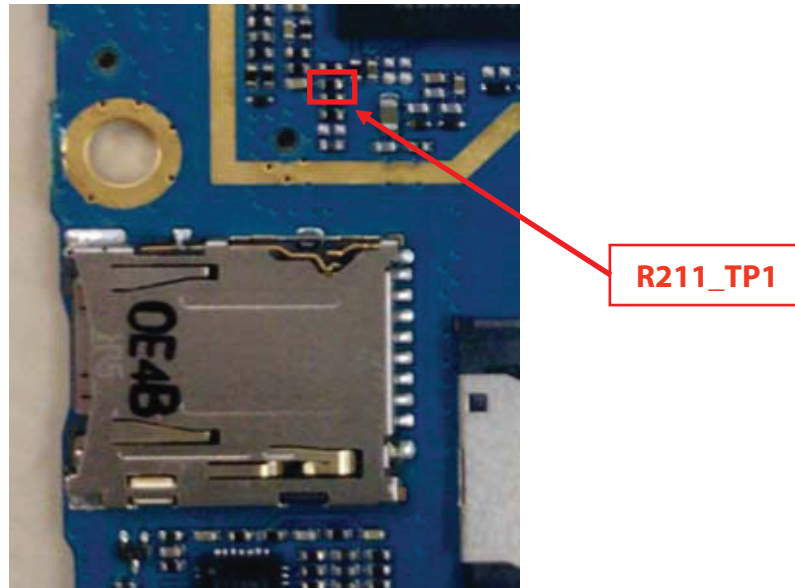
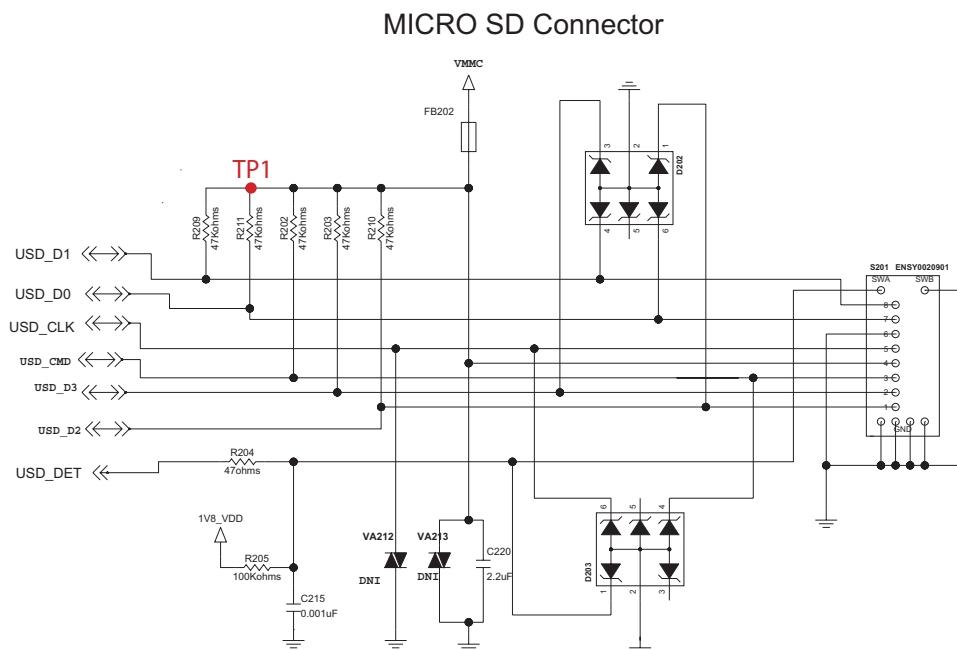
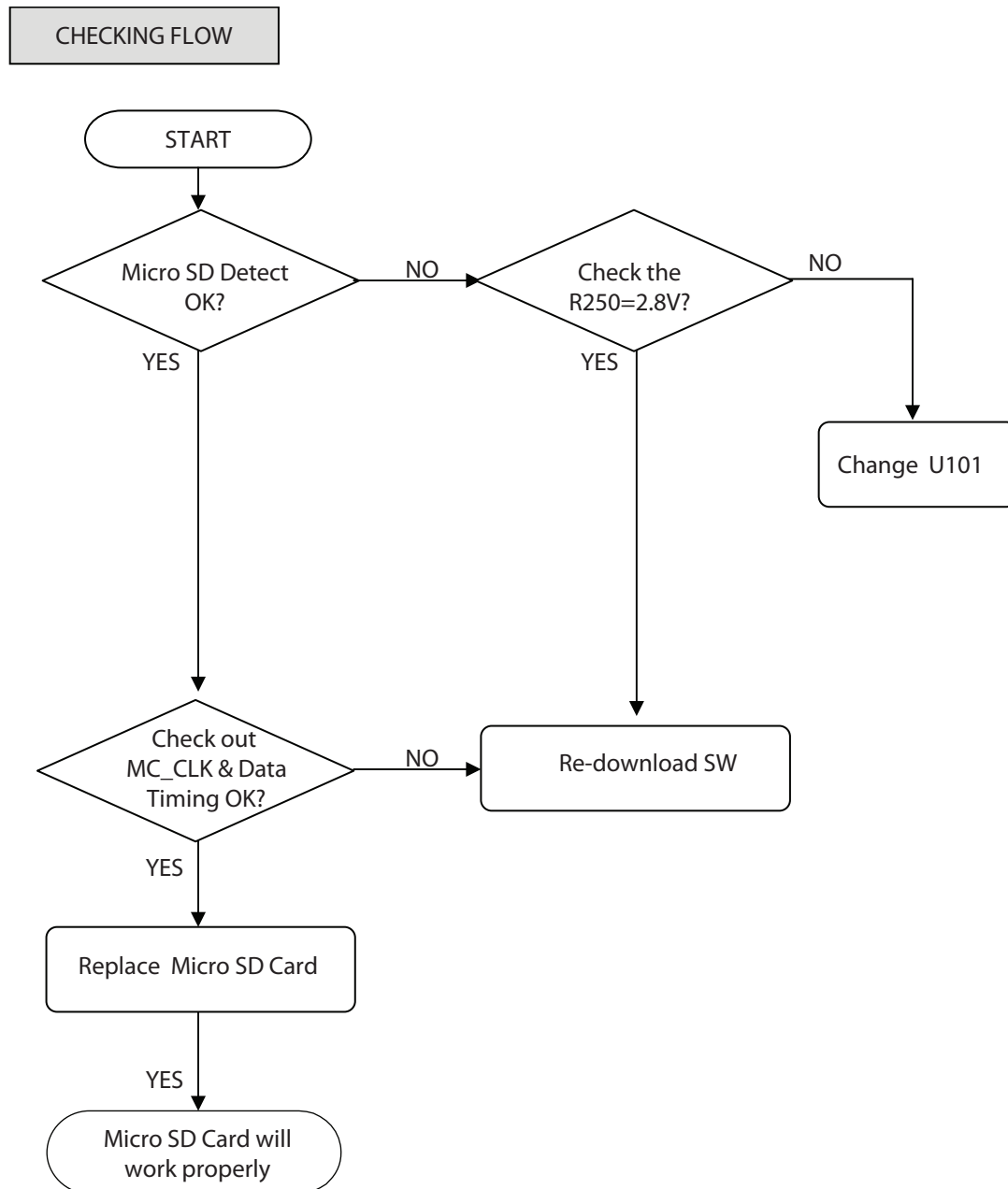


Figure 4.15

CIRCUIT





4. TROUBLE SHOOTING

4.16 Bluetooth & WLAN Trouble

TEST POINT

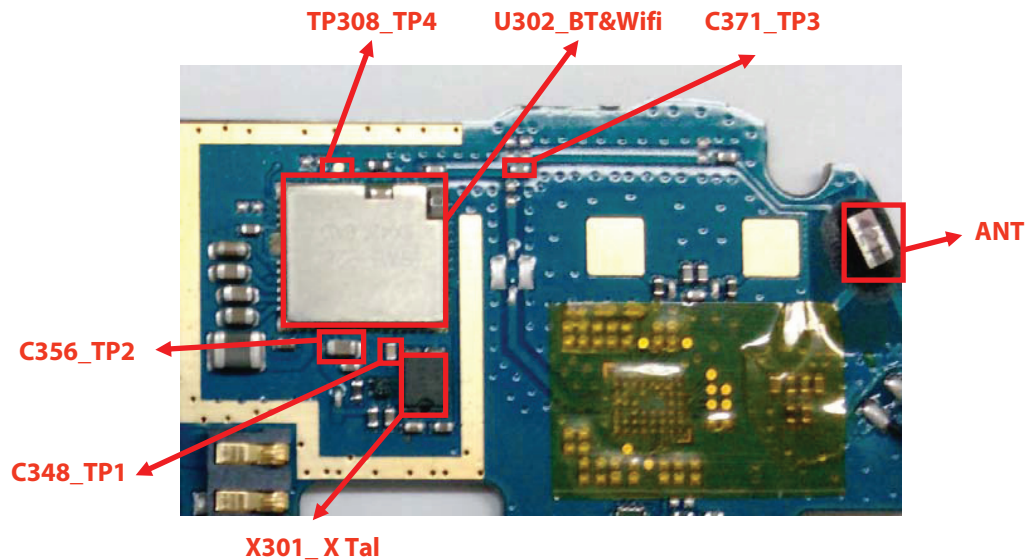
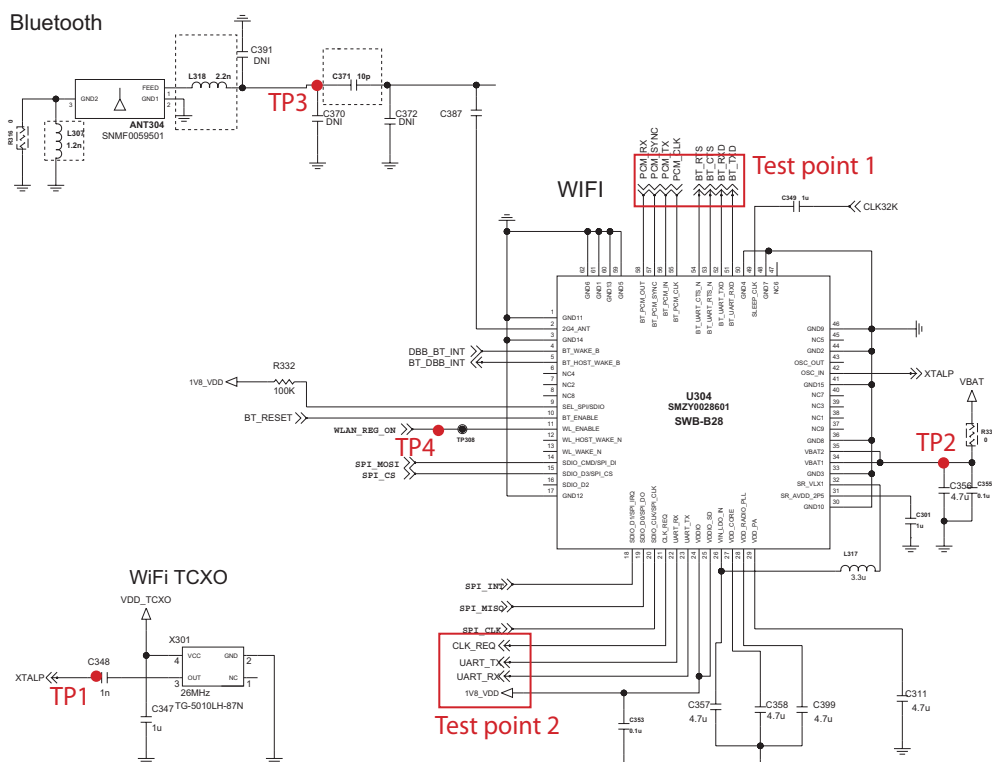
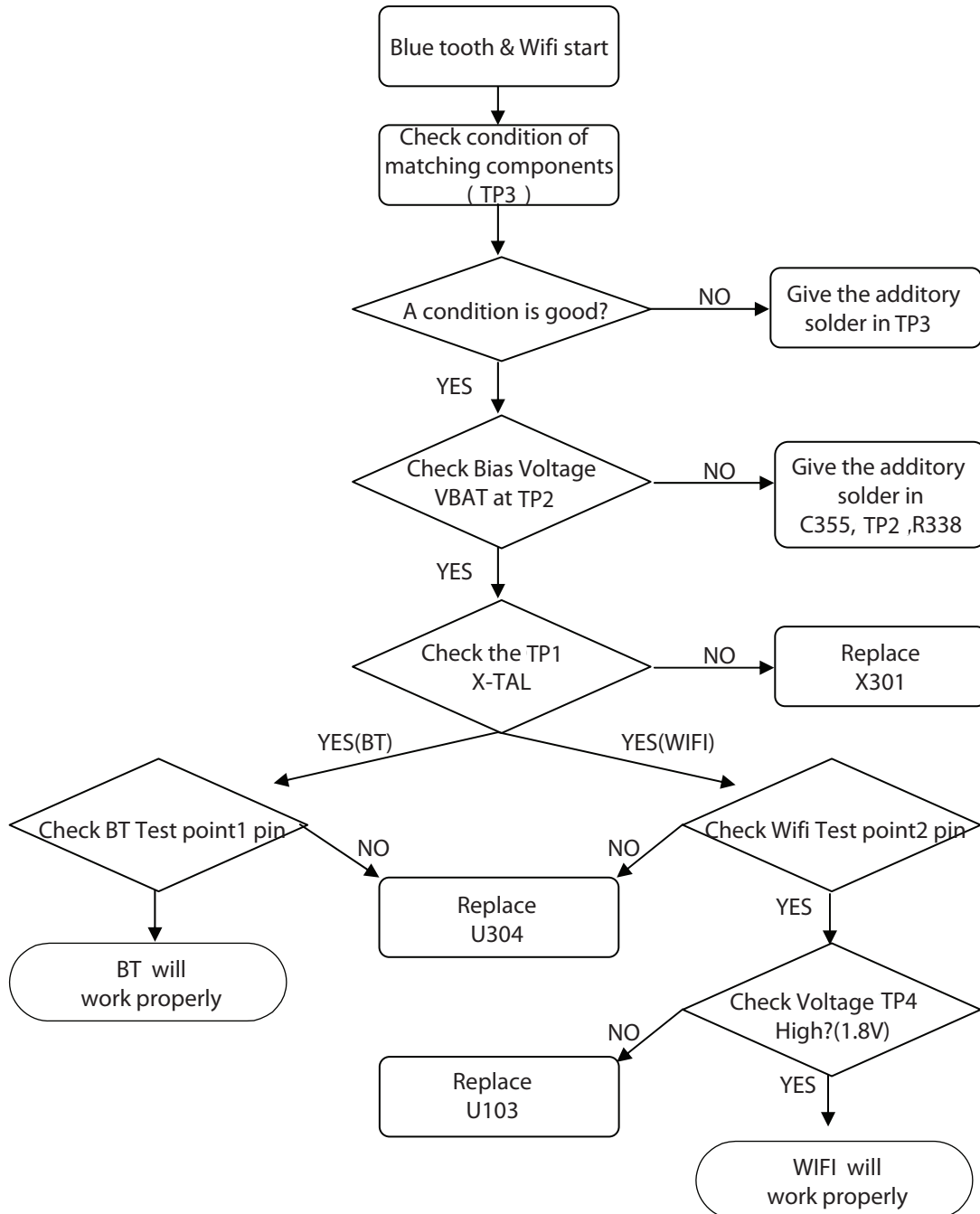


Figure 4.16.1

CIRCUIT



CHECKING FLOW



4. TROUBLE SHOOTING

4.17 FM Radio Trouble

TEST POINT

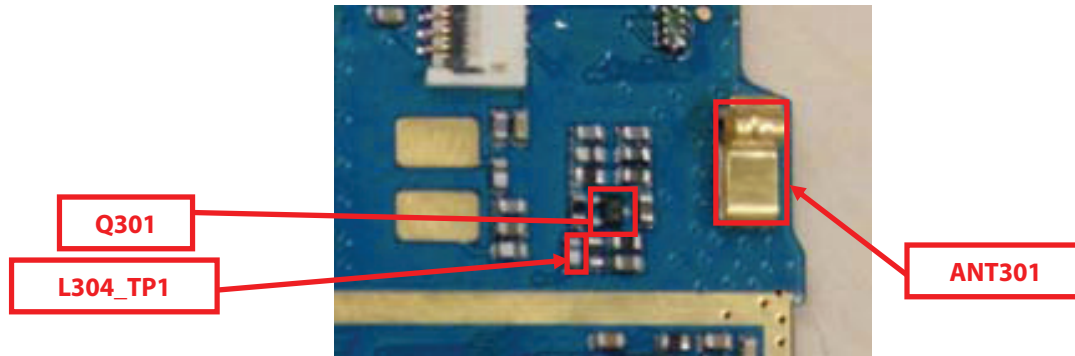
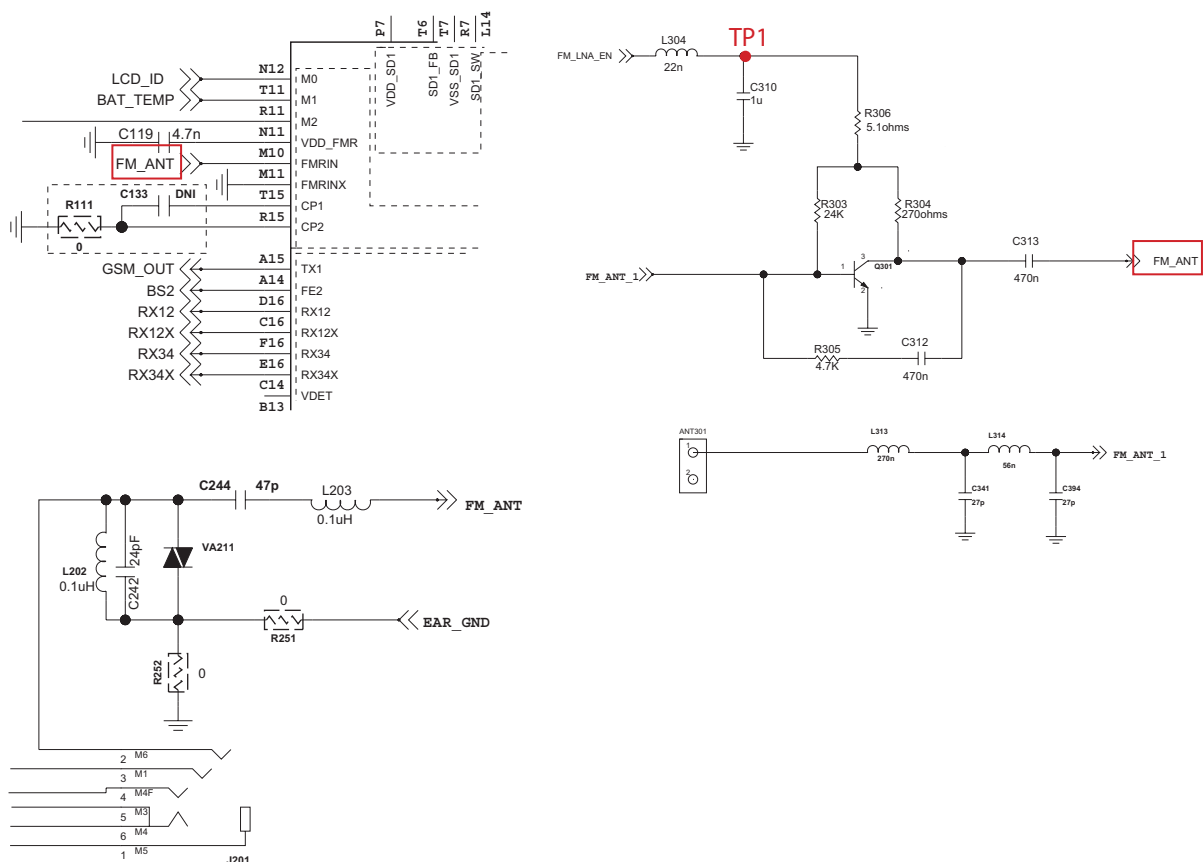
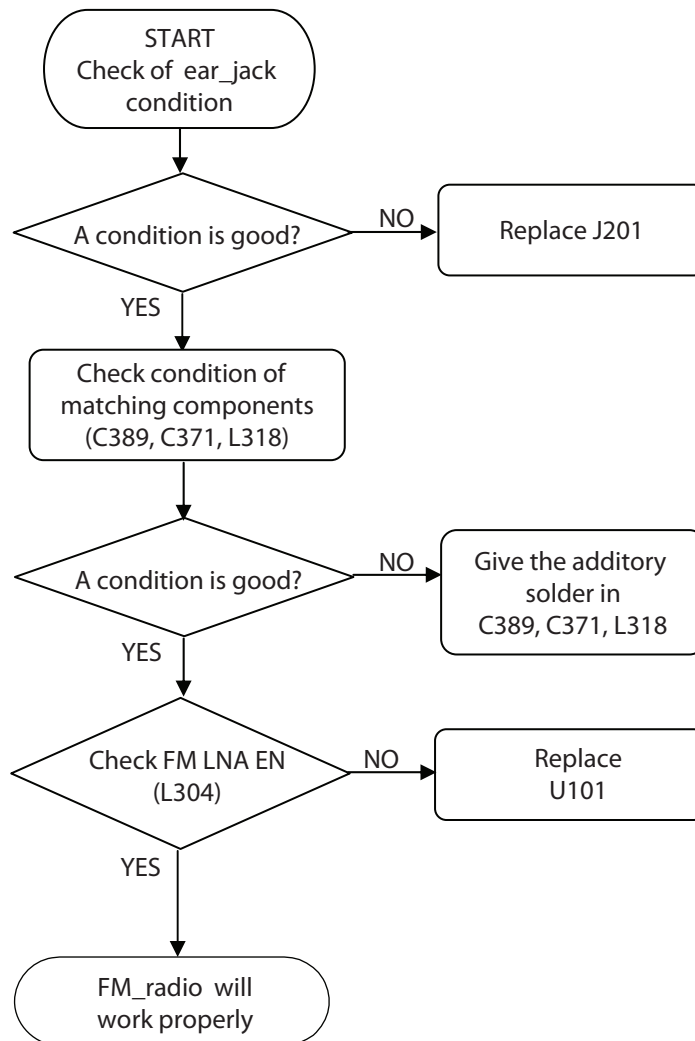


Figure 4.17

CIRCUIT

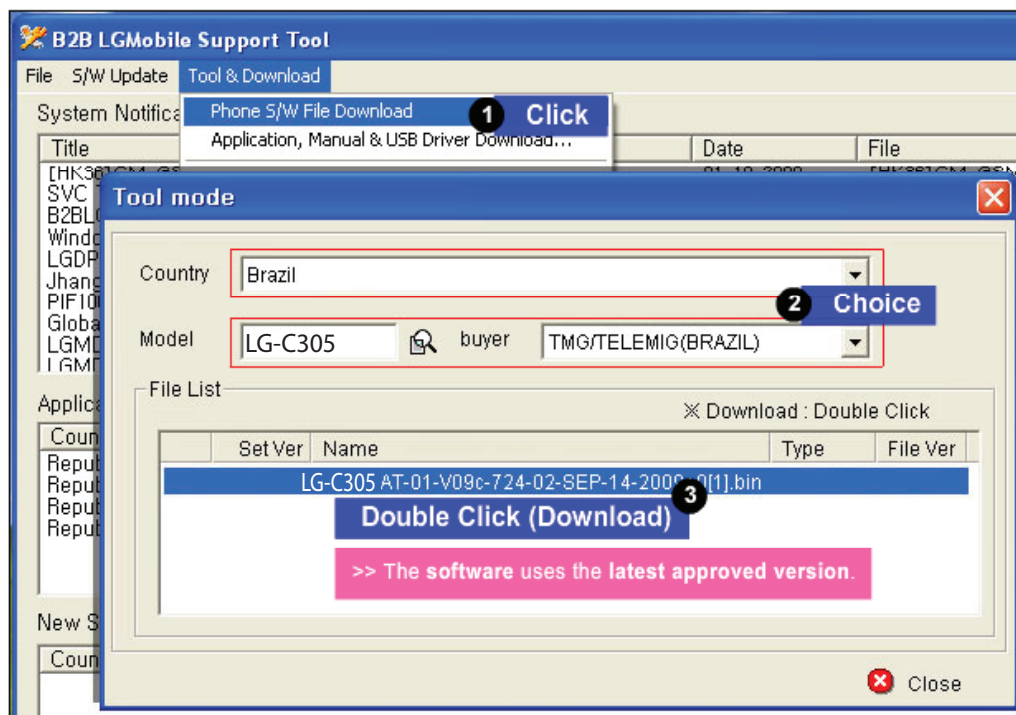
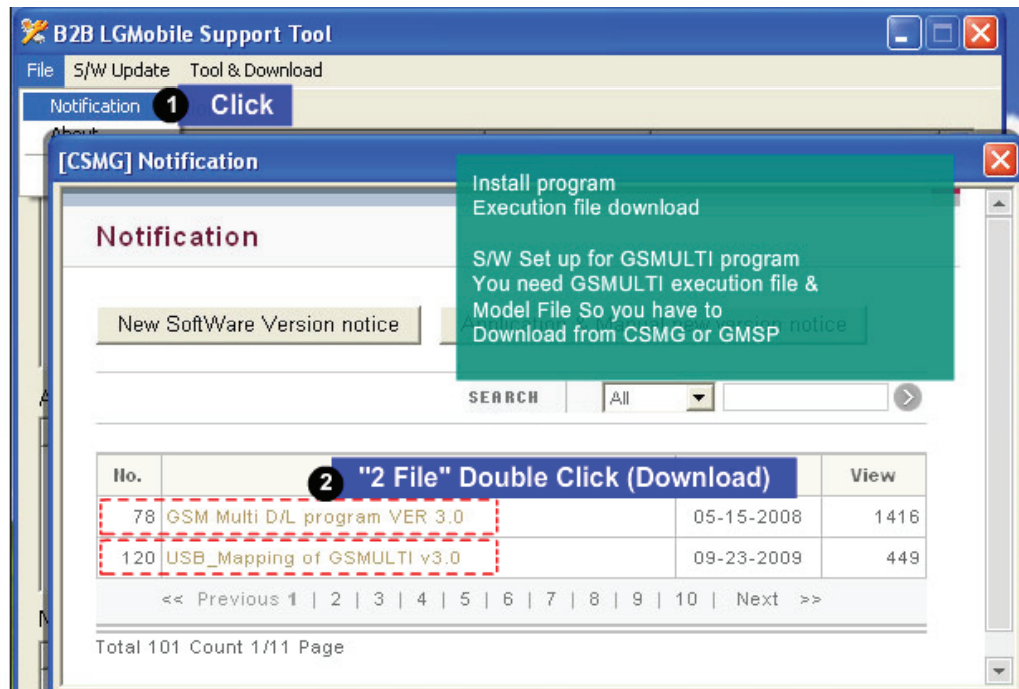


CHECKING FLOW

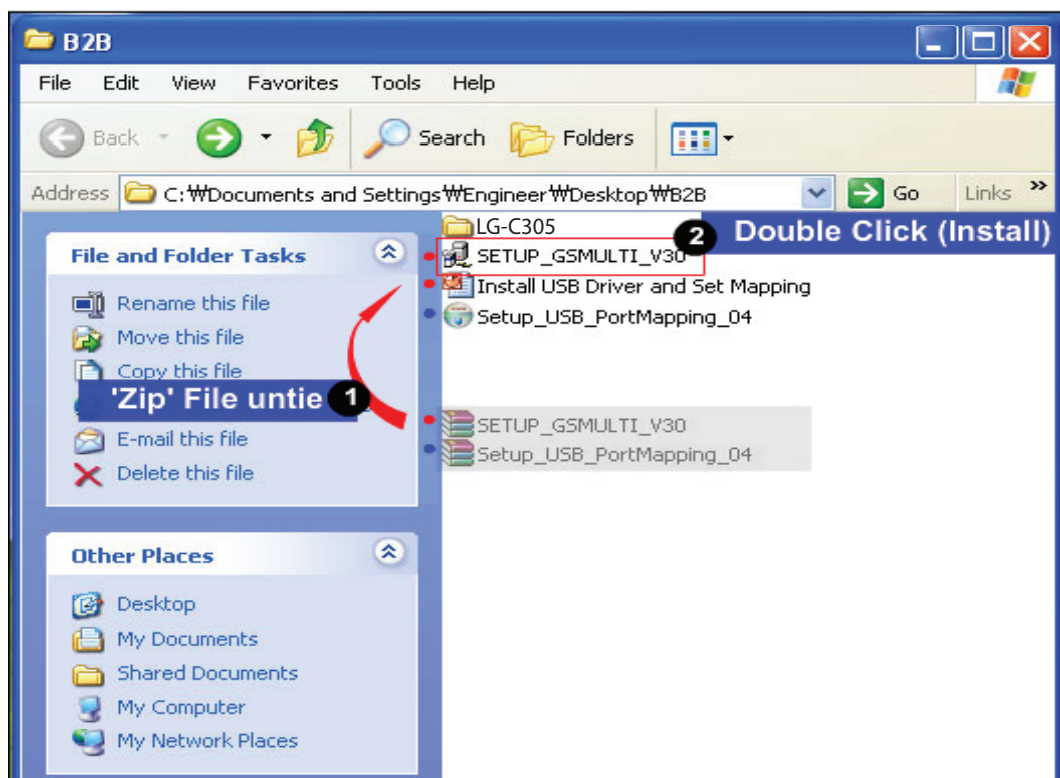
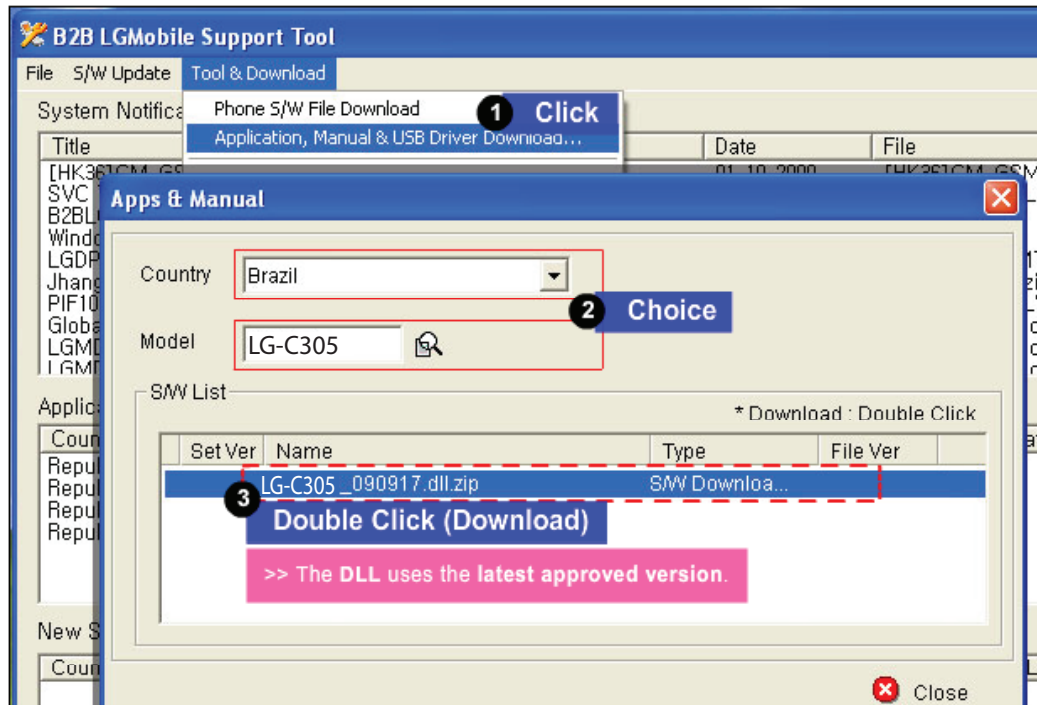


5. DOWNLOAD

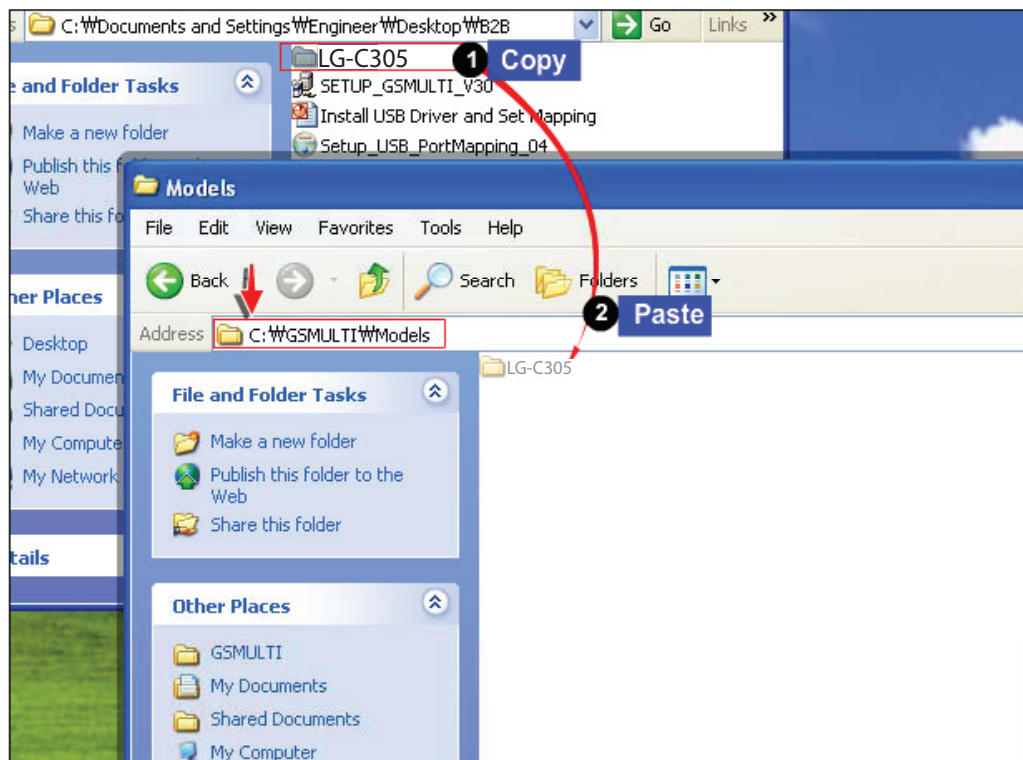
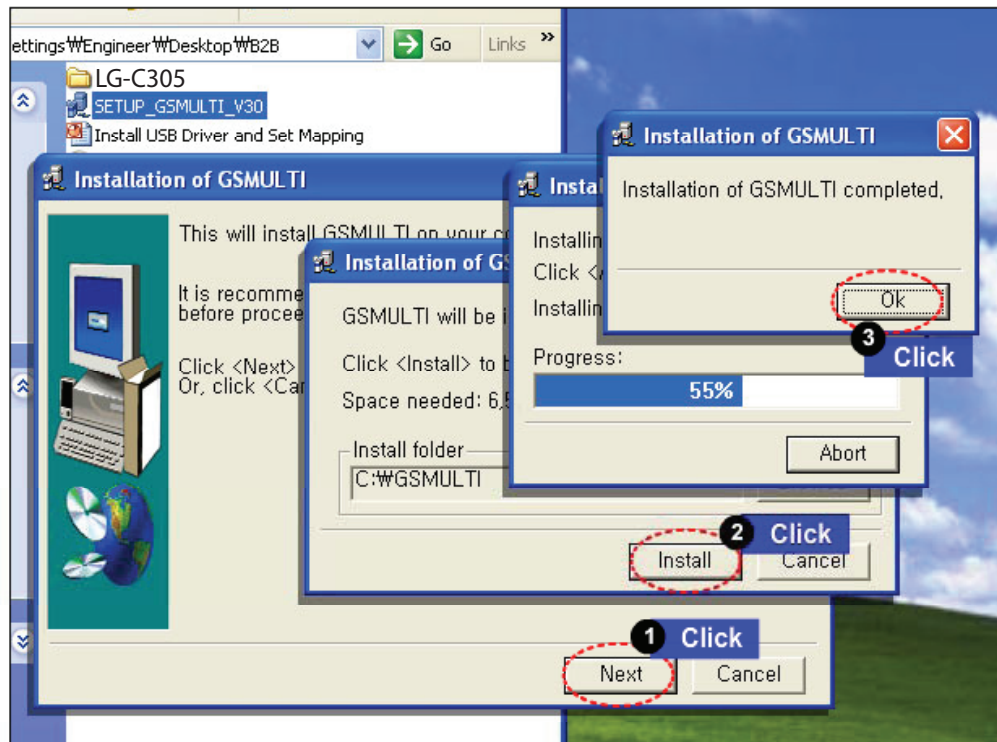
5. DOWNLOAD



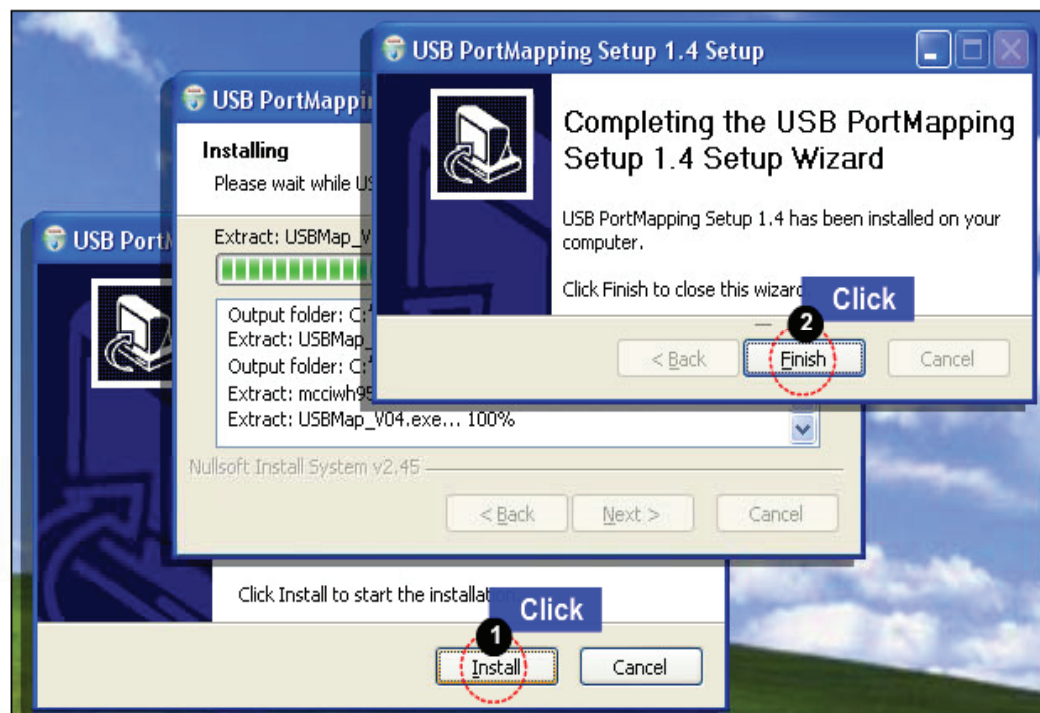
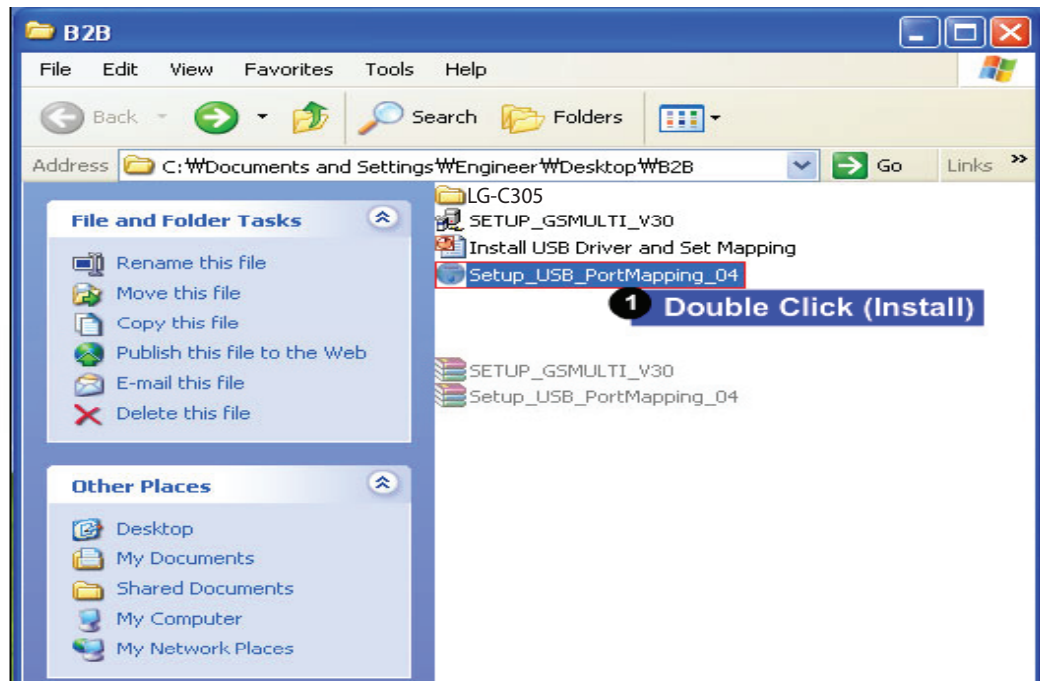
5. DOWNLOAD



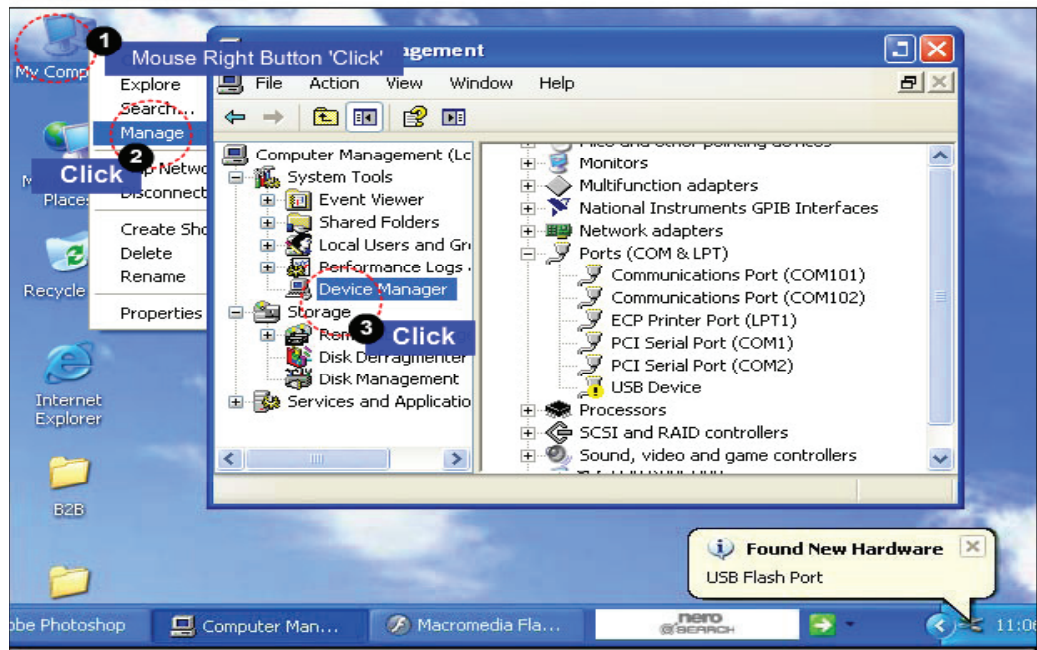
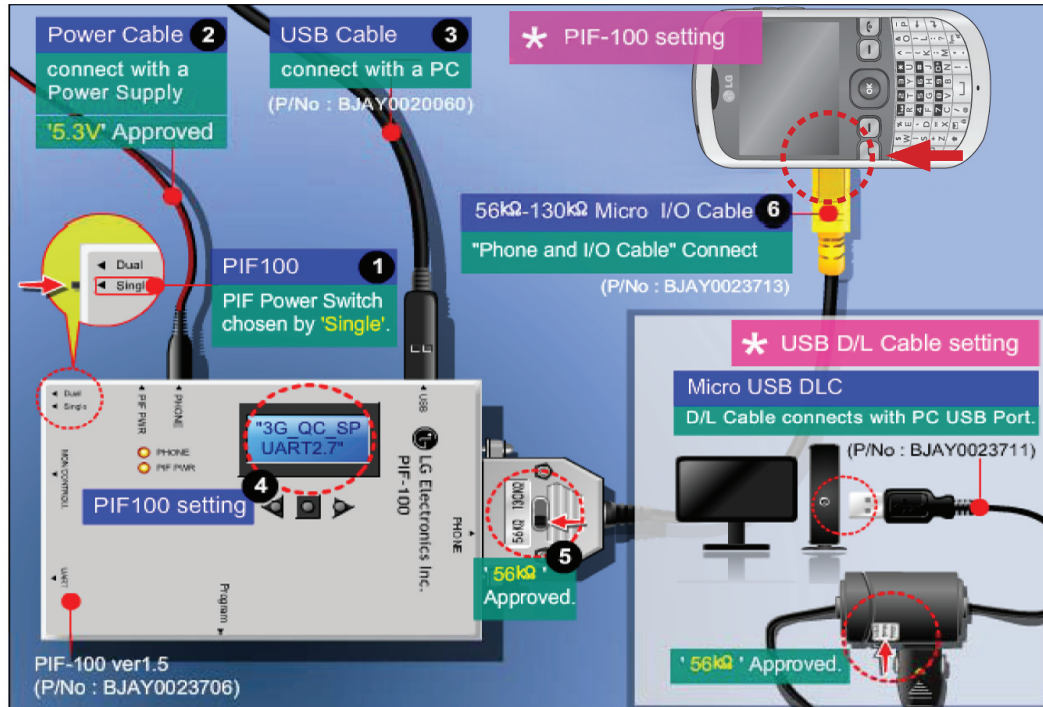
5. DOWNLOAD

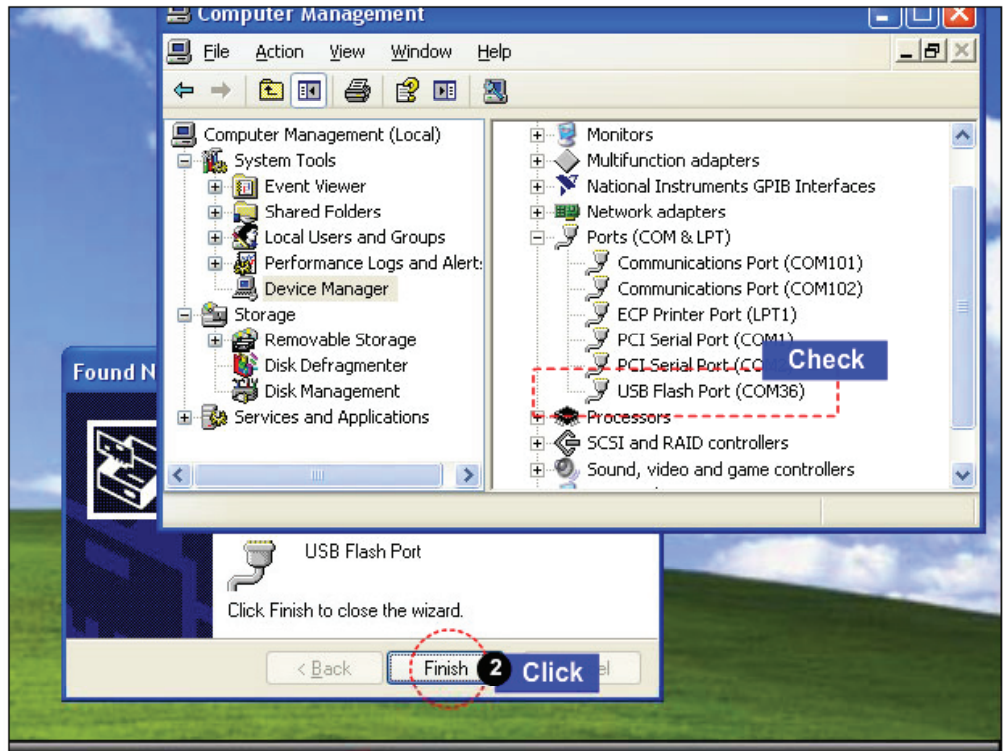
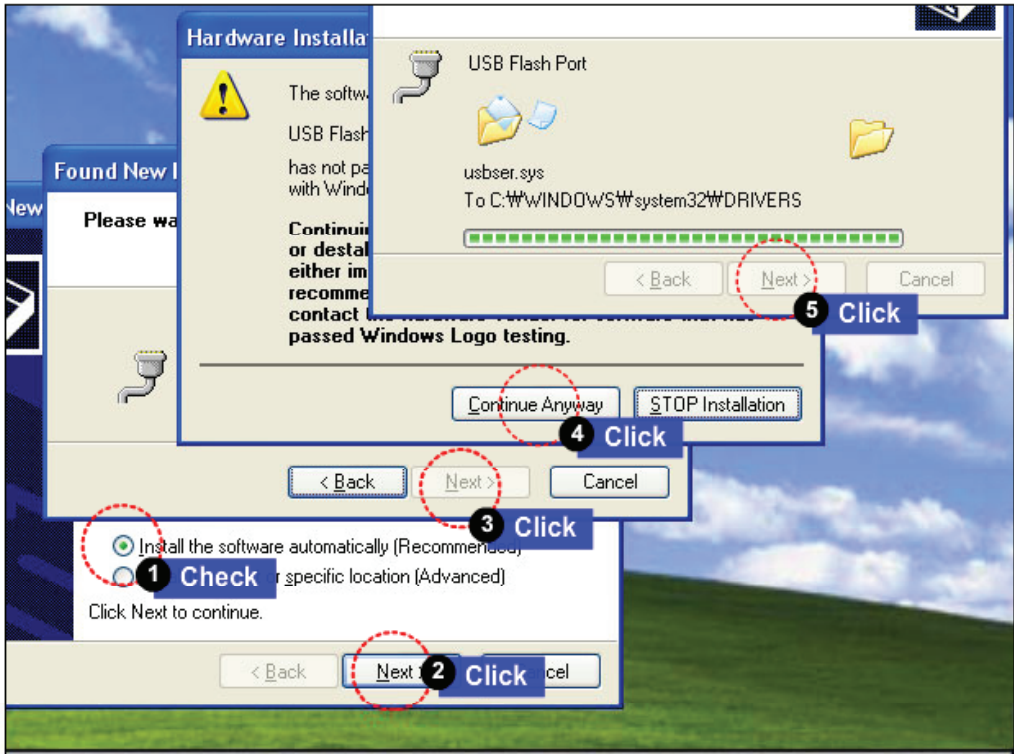


5. DOWNLOAD

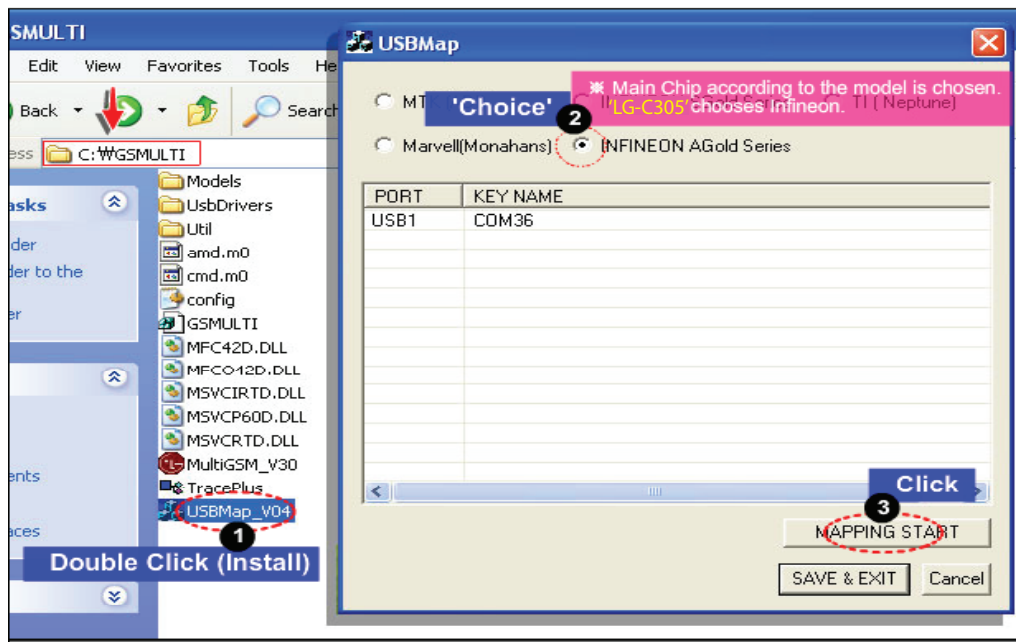


5. DOWNLOAD





5. DOWNLOAD





1 When usb port is caught, 'Save & Exit', click.

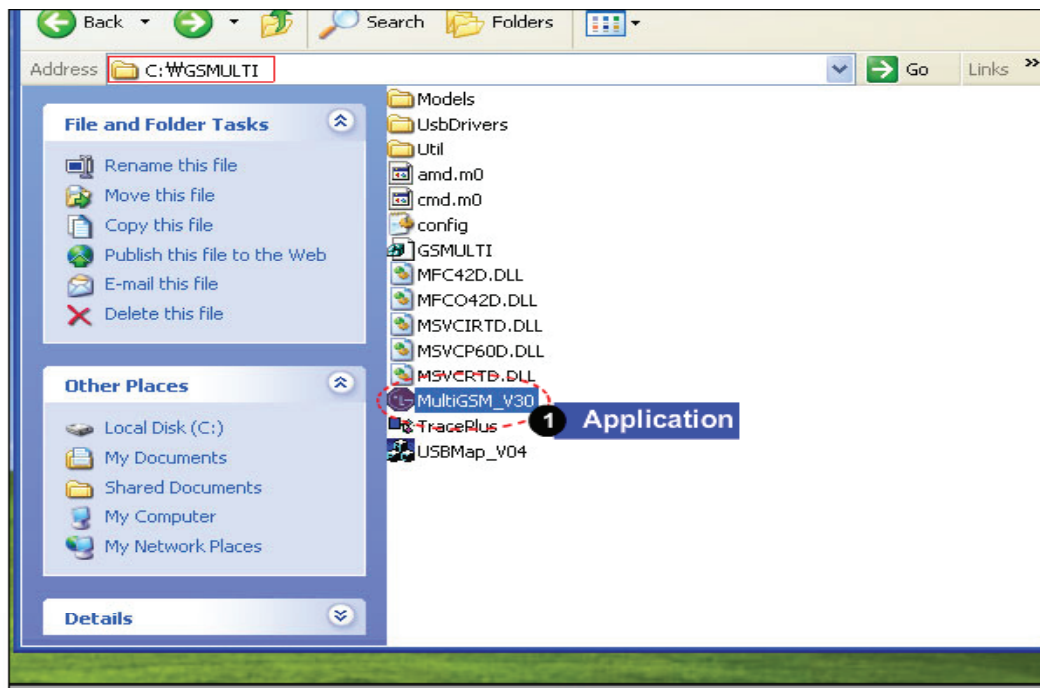
❖ **Note:**

When the phone is connected for a while under USB Map, it will be recognized as a removable disk. Hence if the USB device item is properly set, click the "Save & Exit" button.

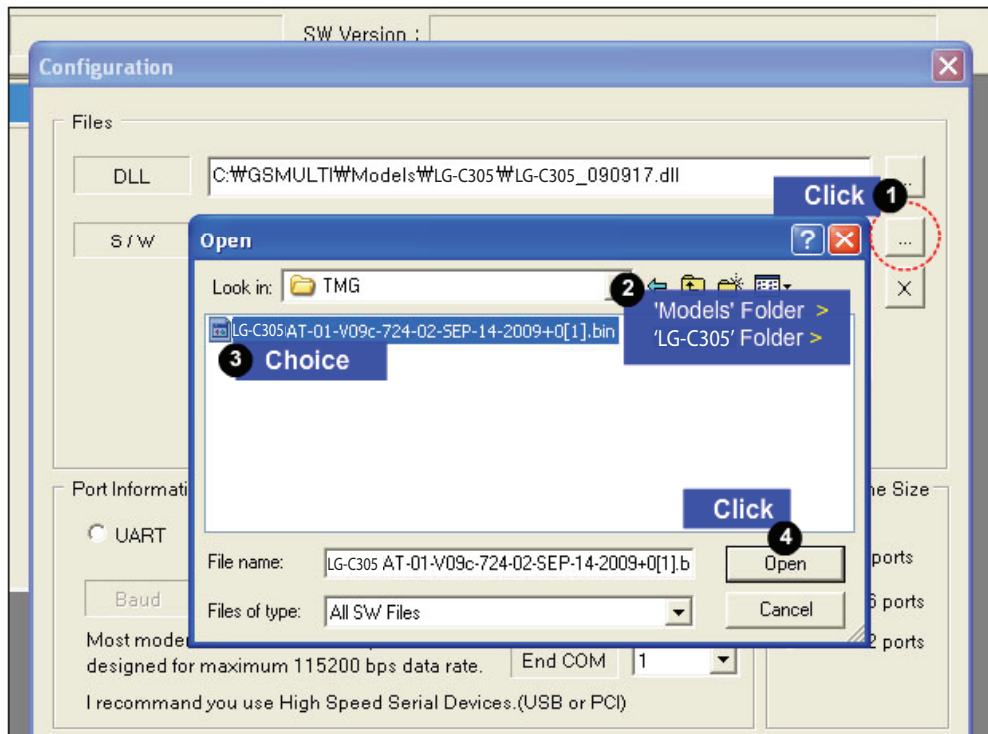
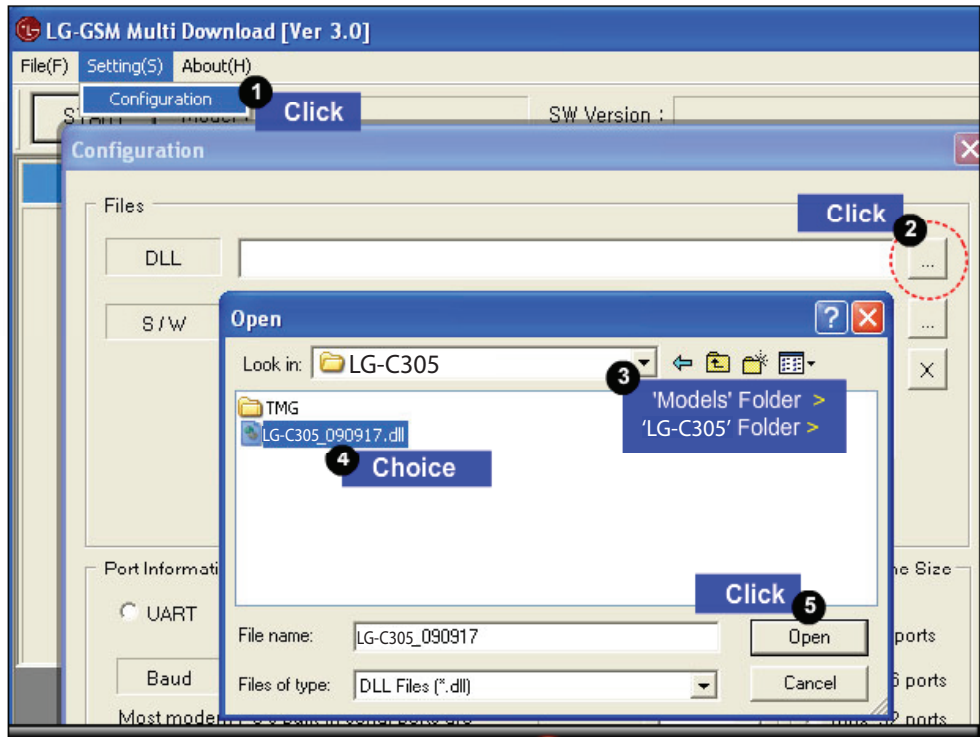
Click 2

2. **SAVE & EXIT**

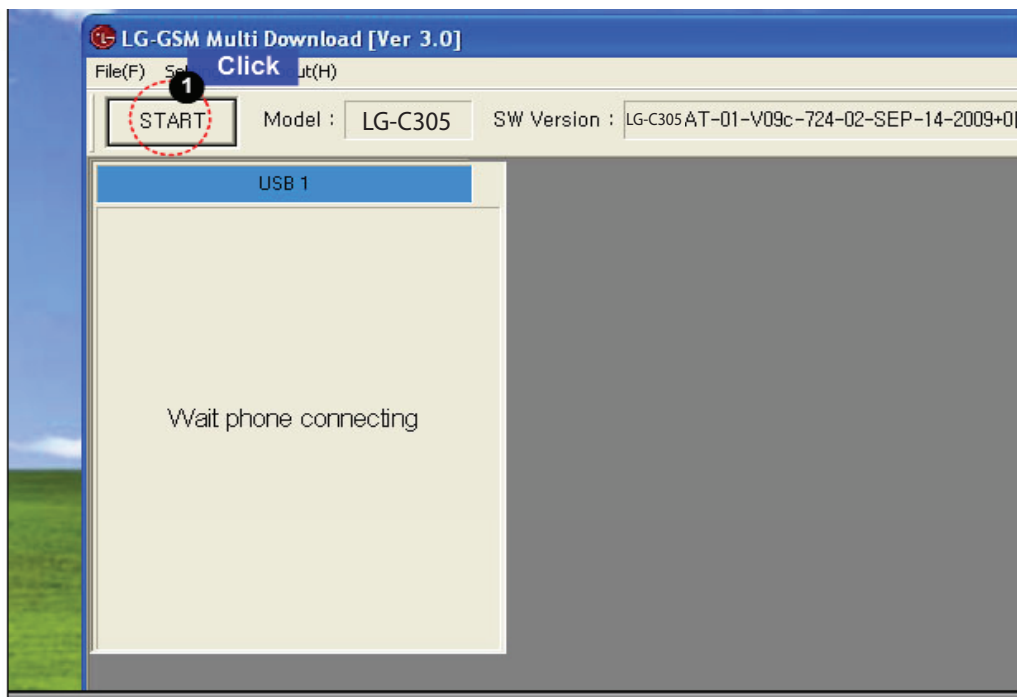
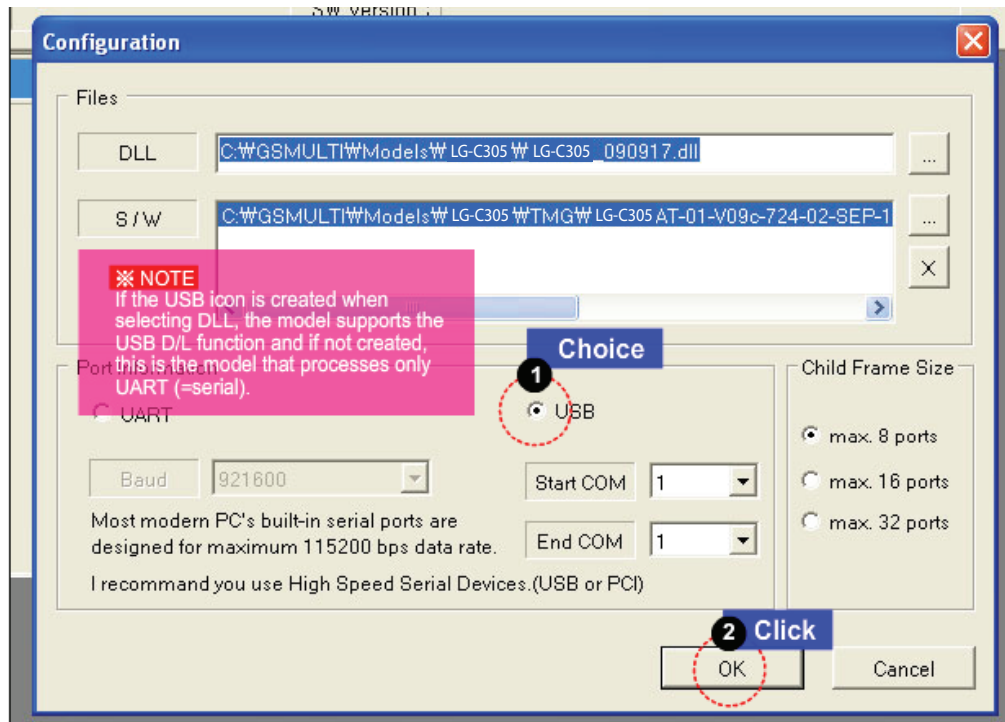
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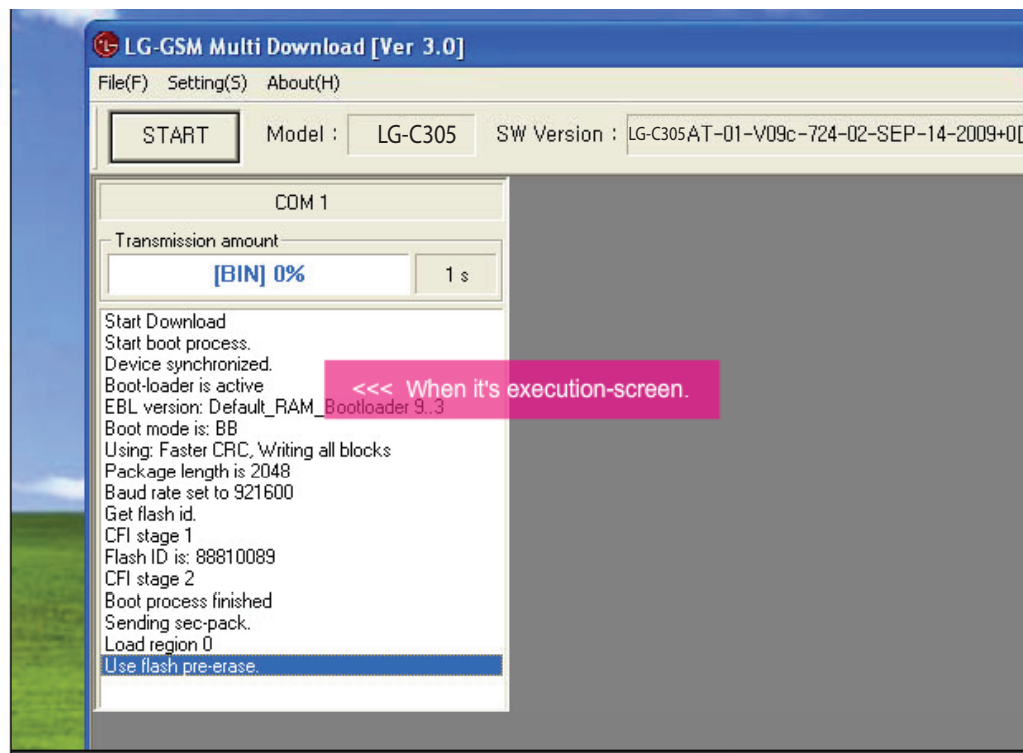
5. DOWNLOAD



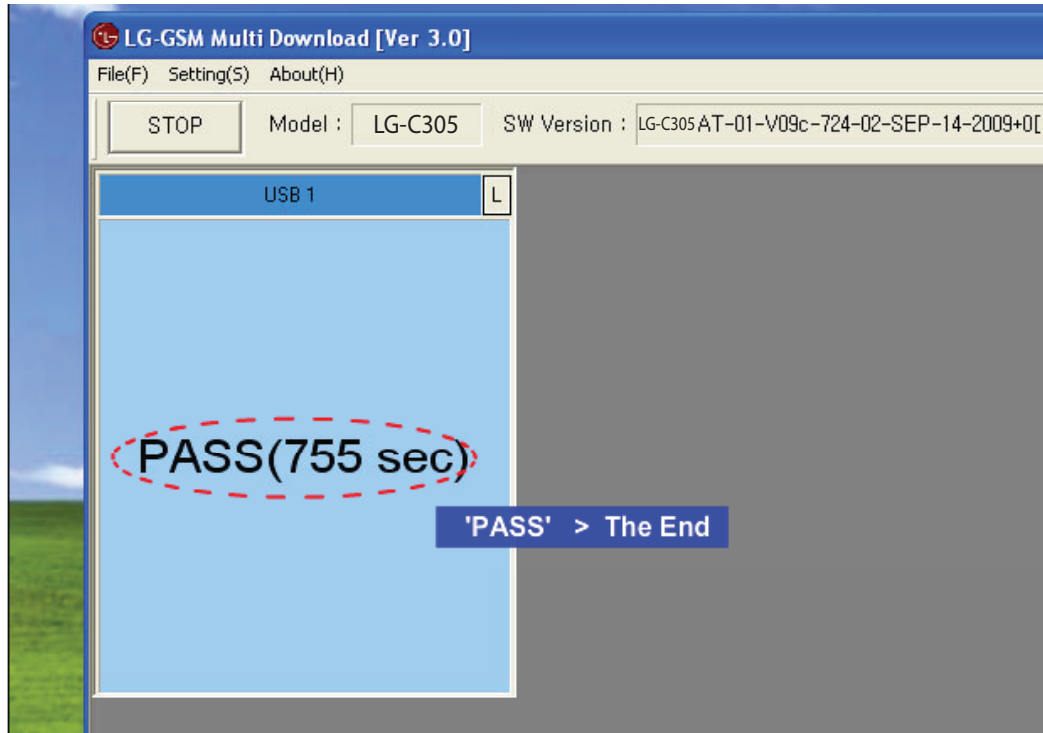
5. DOWNLOAD



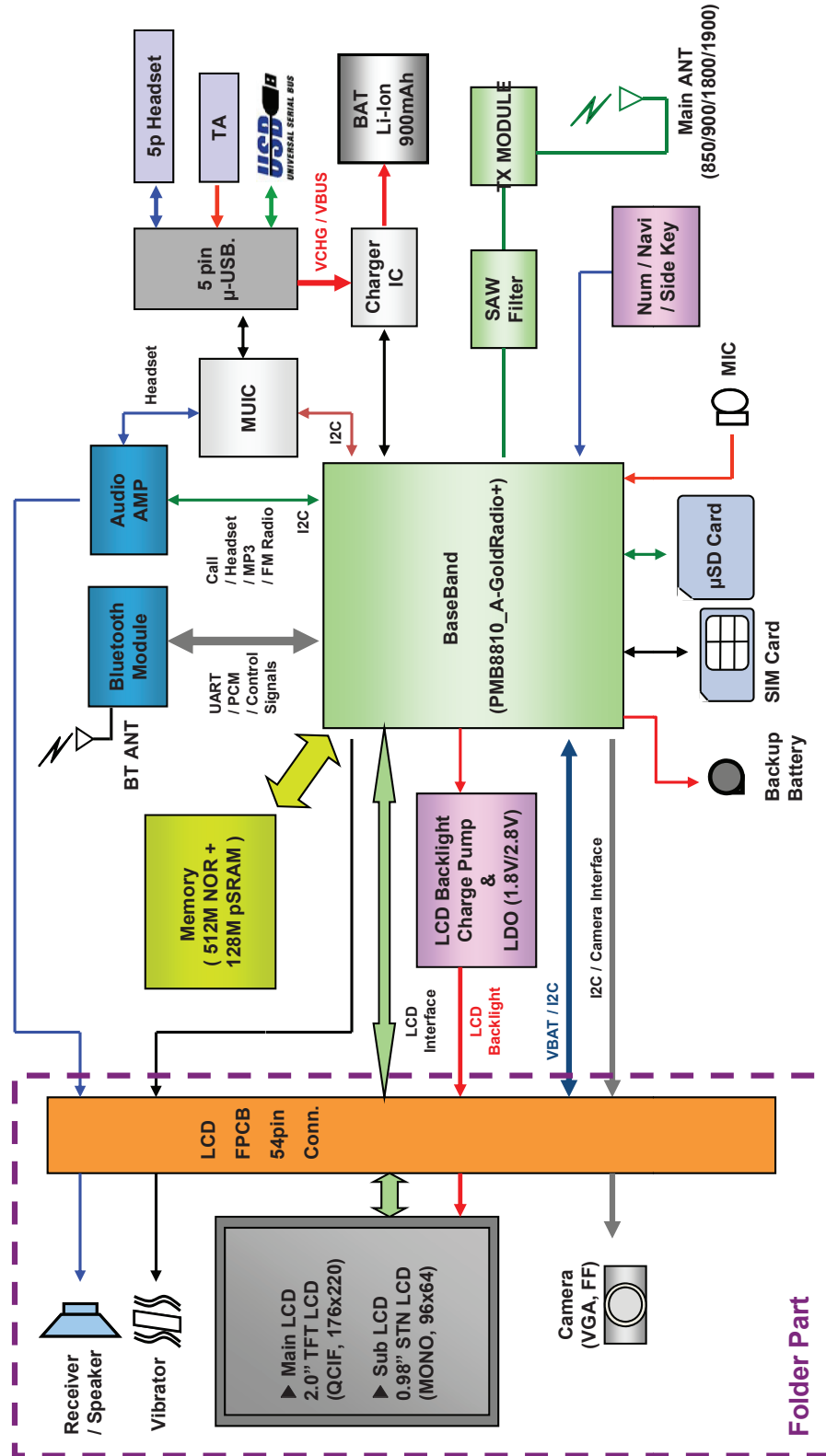
5. DOWNLOAD



5. DOWNLOAD

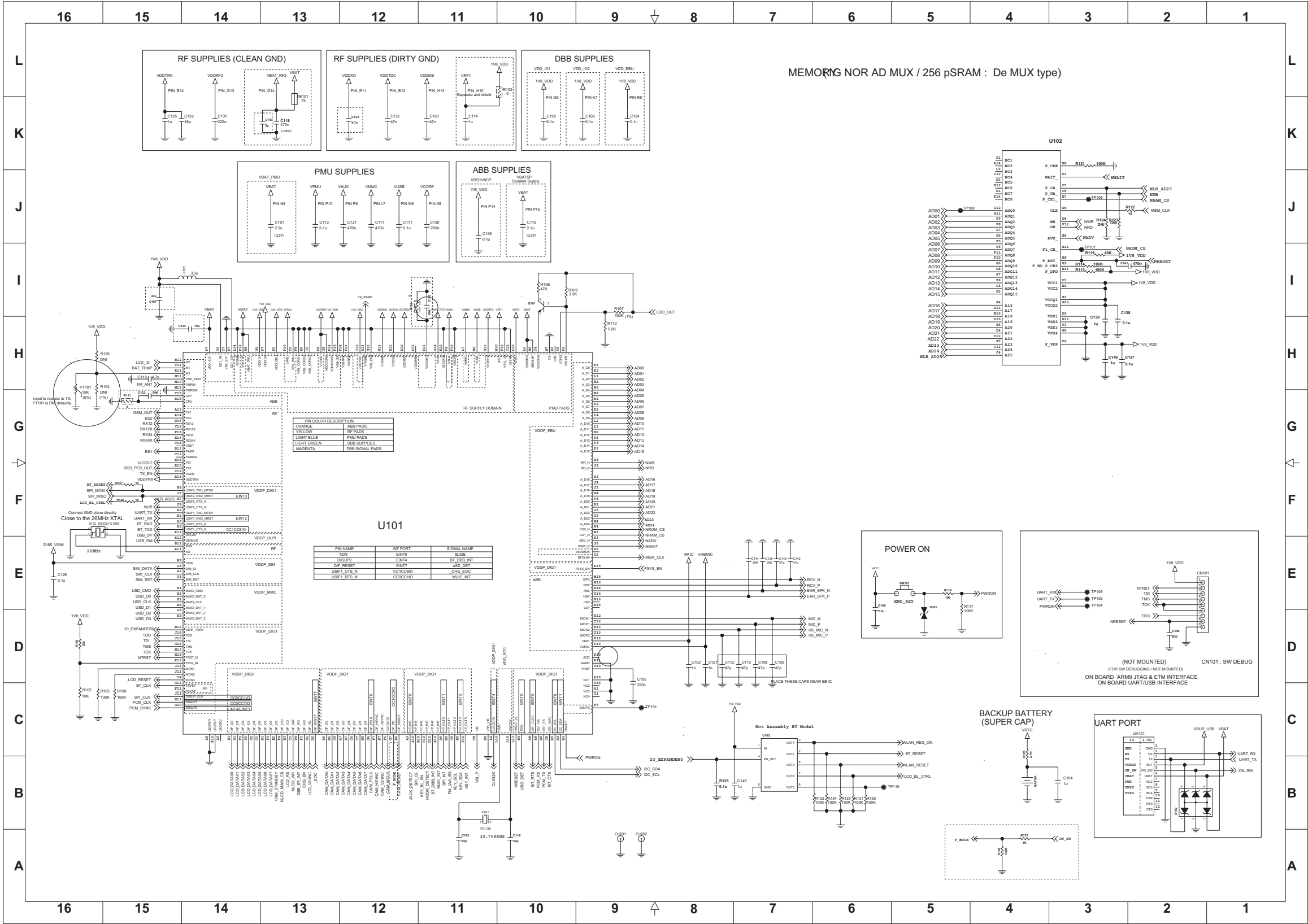


6. BLOCK DIAGRAM

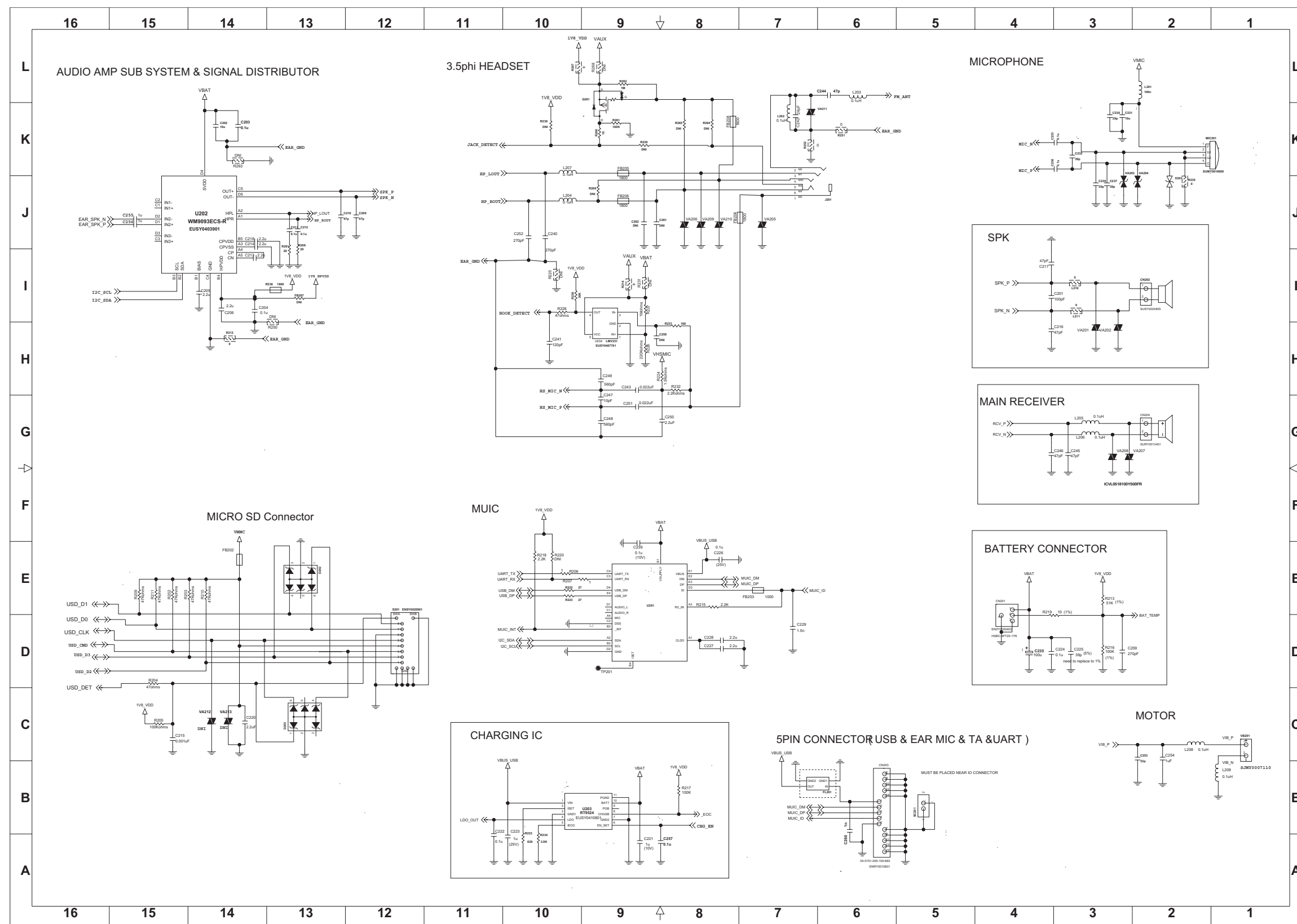




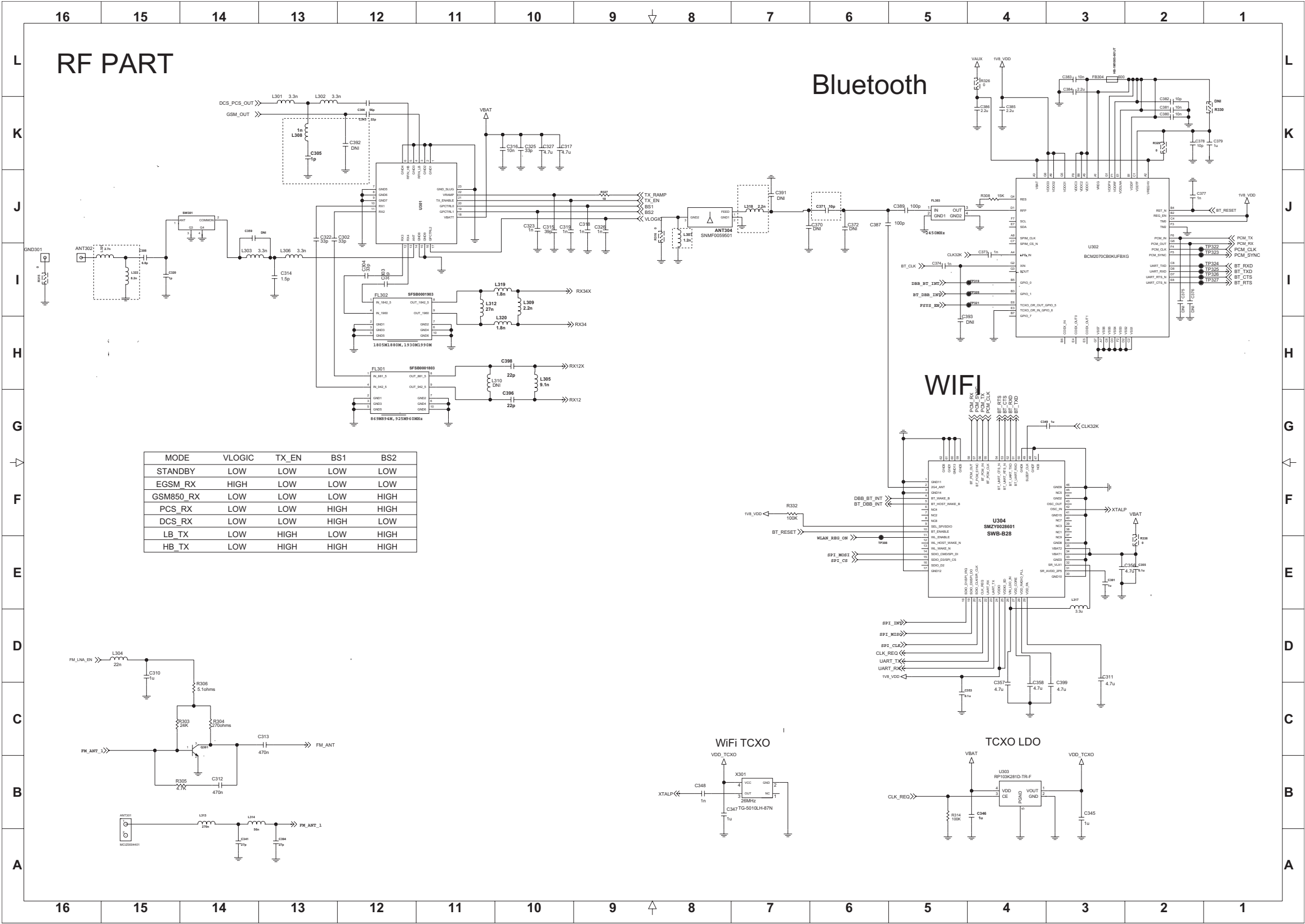
7. CIRCUIT DIAGRAM



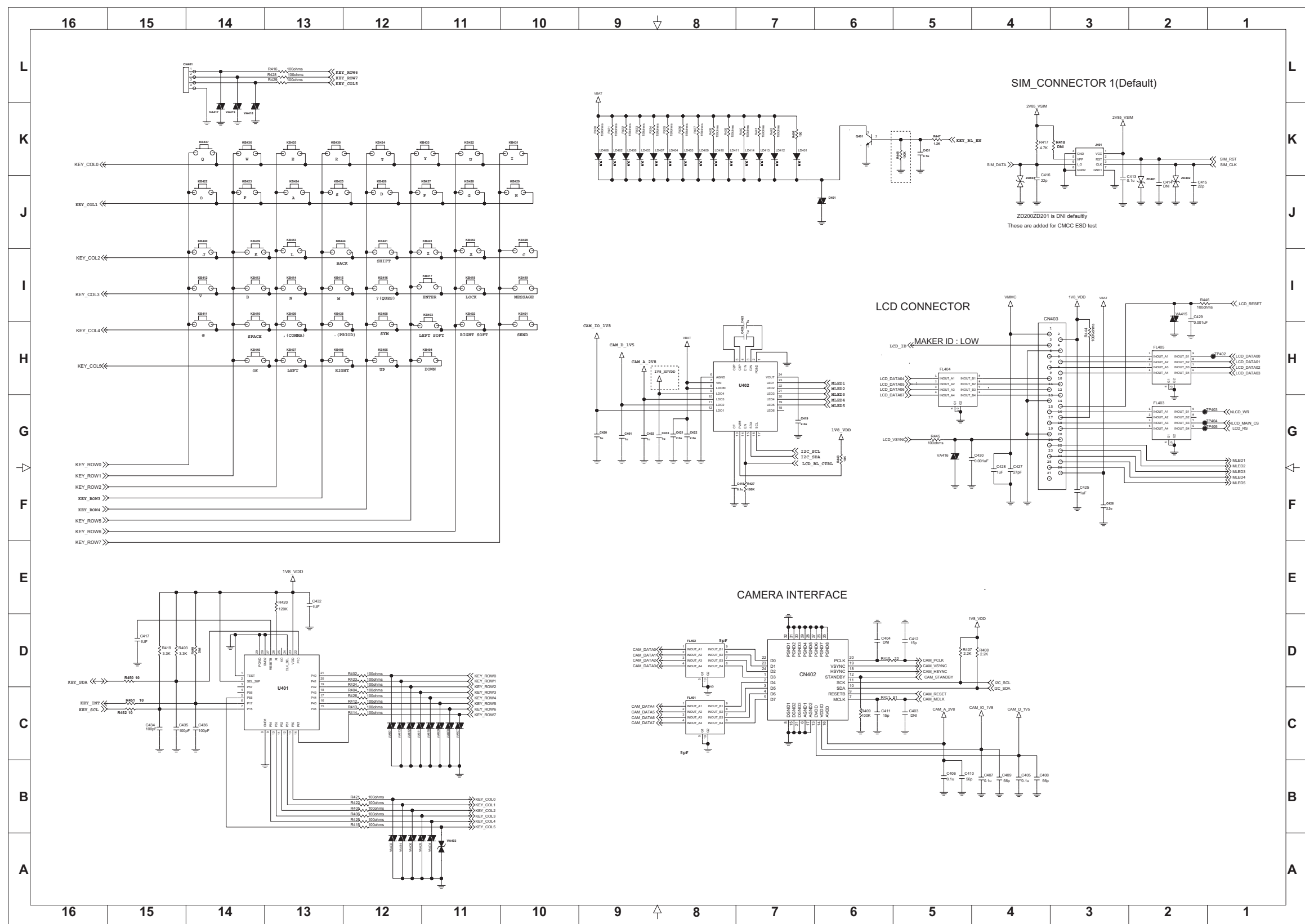
7. CIRCUIT DIAGRAM



7. CIRCUIT DIAGRAM



7. CIRCUIT DIAGRAM



8. BGA PIN MAP

BGA IC pin check (U102)

BGA IC pin check (U101)

▪ Ball Diagram (Top View), PMB8810(A-GOLDRADIO+)

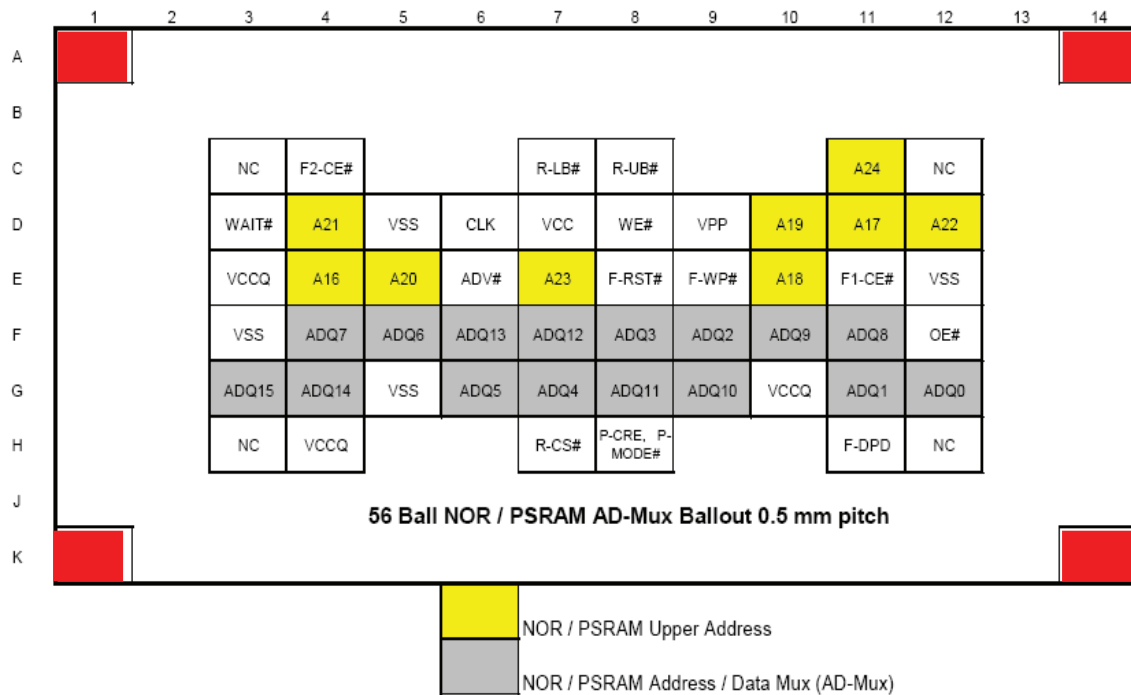
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T		
16	VSSRF2	FE1	RX12X	RX12	RX34X	RX34	TMS	TCK	TDI	TRIG_IN	F32K	EPP	LSN	VBATSP	VDDNEG		16	
15	TX1	TX2	VSSRF			VSSLO		TRST_n	TDO	FSYS_EN	OSC32K	EPN	LSP	VSSLSR	CP2	CP1	15	
14	FE2	VDDTRX	VDET			VSSTRX	VBAT				VSSMS			VDD1V8CP	HSL	HSR	14	
13	VRAMP	PABS	PABIAS			VSSRX	VDDRF2	VDDMS	MON1		RESET_N			VUMIC	MICN2	MICP2	13	
12	VDDMMD	VDDTDC	PAEN		VSSDCO	VSSXO	VSSDIG	SWIF_TXRX	MON2	DMINUS			MO	VMIC	MICN1	MICP1	12	
11	XO	XOX			VDDXO	FSYS2	FSYS1	DIGuP1	DIGuP_CLK	DPLUS		FMRINX	VDD_FMR	AGND	M2	M1	11	
10	KP_IN1	KP_IN2	KP_IN3	KP_IN4	KP_IN5	KP_OUT5	DIGuP2	VRF1	VDD1V81	LEDFBP	VRTC	FMRIN		VPMU	ACD	VREF	10	
9	KP_IN0	KP_OUT1	KP_OUT2	KP_OUT0	KP_OUT3	VDDF3	VDDIO1	VSSCORE2	VSSCORE3		LEDDR	VUSB		ANAMON	ONOFF	VSS_PMU	9	
8	I2S1_RX	I2S1_TX	I2S1_WA0	I2S1_CLK0	CIF_D7	VSSCORE1	VDDCORE	USIF2_TXD_MTSR	USIF2_CTS_n	VCORE	LEDVBN	VSIM	VBAT_PMU	VAUX	VSS_VIB	VIB	8	
7	CIF_D3	CIF_D4	CIF_D6		CIF_VSYNC	CIF_HSYNC	CIF_PD	USIF2_RTS_n	USIF2_RXD_MRST	VDDIO2	VMMC	CS		VDD_SD1	SD1SW	VSS_SD1	7	
6	CIF_D0	CIF_D1	CIF_D5		CIF_RESET	CLKOUT2	CIF_PCLK	MMCI_DAT1	WAIT_n	VSHNT	SENSEN	SENSEP			CSB	SD1_FB	6	
5	I2C_SDA	I2C_SCL	CIF_D2				MMCI_DAT2			MMCI_DAT3				A/D13	VDD_EBU	VCHG	5	
4	CLKOUT0	T2IN	MON3	DIF_RD		DIF_CS1	CC_RST	A19	A17	CS0_n	A/D9		A24	A20	WR_n	VDDCHG	4	
3	USIF1_RTS_n	USIF1_RXD_MRST	DIF_WR	DIF_D3	DIF_CD	DIF_D7	CC_IO	MMCI_DAT0		A22	A/D0	A/D11	CS1_n	A/D4	A/D15	ADV_n	A23	3
2	USIF1_TXD_MTSR	USIF1_CTS_n	DIF_D4	DIF_RESET	DIF_D8	DIF_D2	CC_CLK	MMCI_CLK	A18	A/D1	A/D10	A/D5	A/D12	A/D7	A21	BFCLKO	2	
1	VSSCORE4	DIF_D6	DIF_D5	DIF_D1	DIF_D0	DIF_HD	DIF_VD	MMCI_CMD	RD_n	A/D8	A/D2	A/D3	A/D6	A/D14	A16		1	
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T		

 : not in use

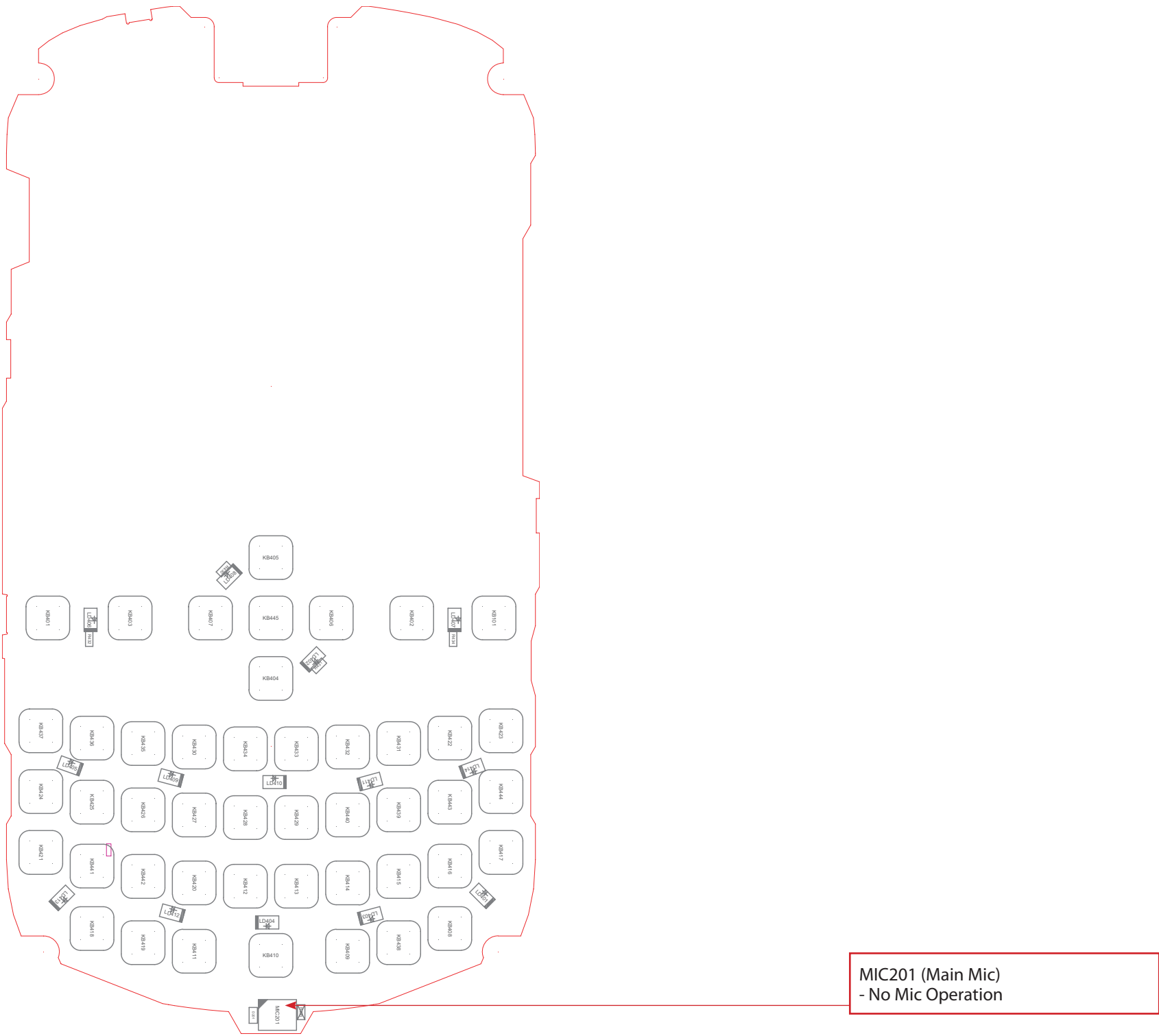
8. BGA PIN MAP

BGA IC pin check (U101)

▪ Ball Diagram (Top View), PF38F6066M0Y3DE



9. PCB LAYOUT



LG-C305_MAIN_SPFY0229001-1.0_TOP

9. PCB LAYOUT



LG-C305_MAIN_SPFY0229001-1.0_BOT

10.ENGINEERING MODE

Engineering mode is designed to allow a service man/engineer to view and test the basic functions provided by a handset. The key sequence for switching the engineering mode on is "1809##300#" Select. Pressing END will switch back to non-engineering mode operation. Use Up and Down key to select a menu and press 'select' key to progress the test. Pressing 'back key will switch back to the original test menu.

1. Factory Mode

[1] DEVICE TEST

- [1-1] Auto All Test
- [1-2] Main LCD
- [1-3] Sub LCD
- [1-4] LCD Backlight
- [1-5] Key Backlight
- [1-6] Speaker
- [1-7] Vibrator
- [1-8] Camera
- [1-9] Sub Camera
- [1-10] Mic Loopback
- [1-11] Key Press Test
- [1-12] Speaker Vib Test

[2] ELT Mode

[3] SW Sanity Test

- [3-1] FPRI Test
- [3-2] DB Check
- [3-3] E Serial NO
- [3-4] UA.String
- [3-5] Unlock SIM

[4] Version

[5] Factory Reset

2. Eng Mode

[1] Usage Info

[2] Eng Mode

- [2-1] Band Selection
- [2-2] Battery Info
- [2-3] Audio Tunning
- [2-4] UART Setting
- [2-5] BT Testing
- [2-6] Defect Report System

[3] Band Select

- [3-1] Auto
- [3-2] GSM 850
- [3-3] GSM900
- [3-4] DCS 1800
- [3-5] PCS 1900

[4] Network Info

- [3-1] Cell Env. (Idle)
- [3-2] Cell Env. (Ded)
- [3-3] PS Log Save
- [3-4] TCPIP Debug
- [3-5] PCS 1900

[5] Other

- [5-1] Bluetooth Test Menu
- [5-2] PS Attach Mode
- [5-3] MMS Test
- [5-4] SIM Info

[6] Debug Setting

- [5-1] Variable Watch
- [5-2] Heap Freesize
- [5-3] Heap Leakage
- [5-4] Heap Assert
- [6-5] QM Heap Freesize
- [6-6] Developer Debug

11. STAND ALONE TEST

11. STAND ALONE TEST

11.1 Introduction

This manual explains how to examine the status of RX and TX of the model.

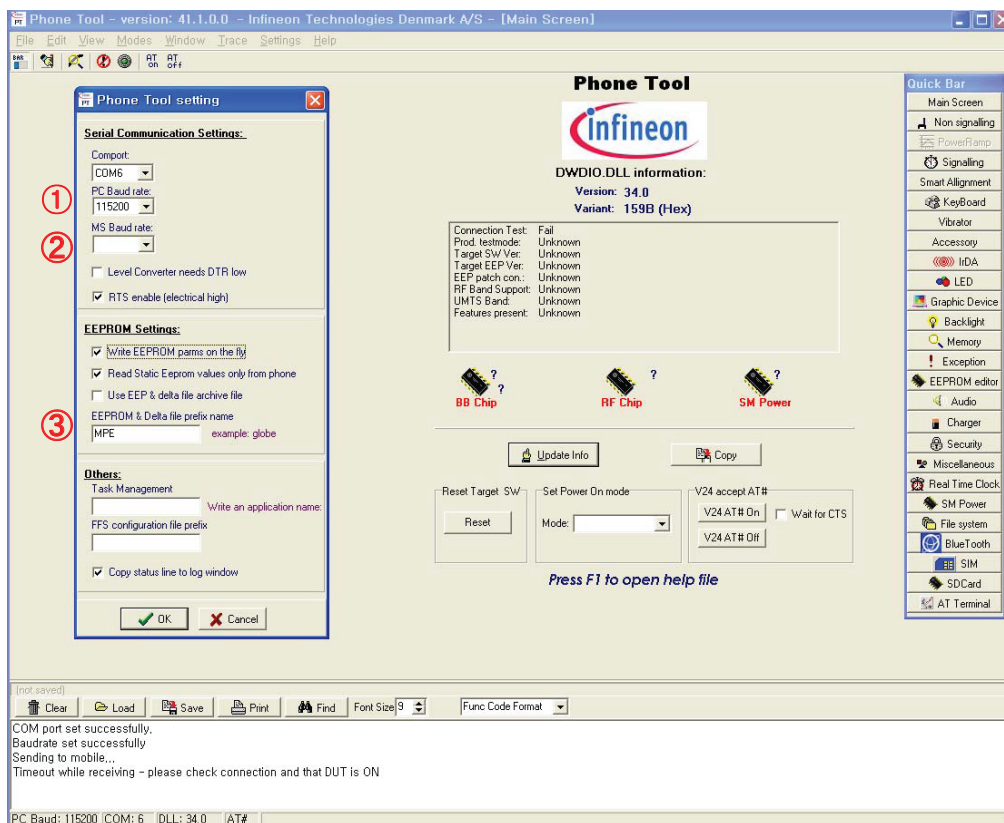
A. Tx Test

TX test - this is to see if the transmitter of the phones is activating normally.

B. Rx Test

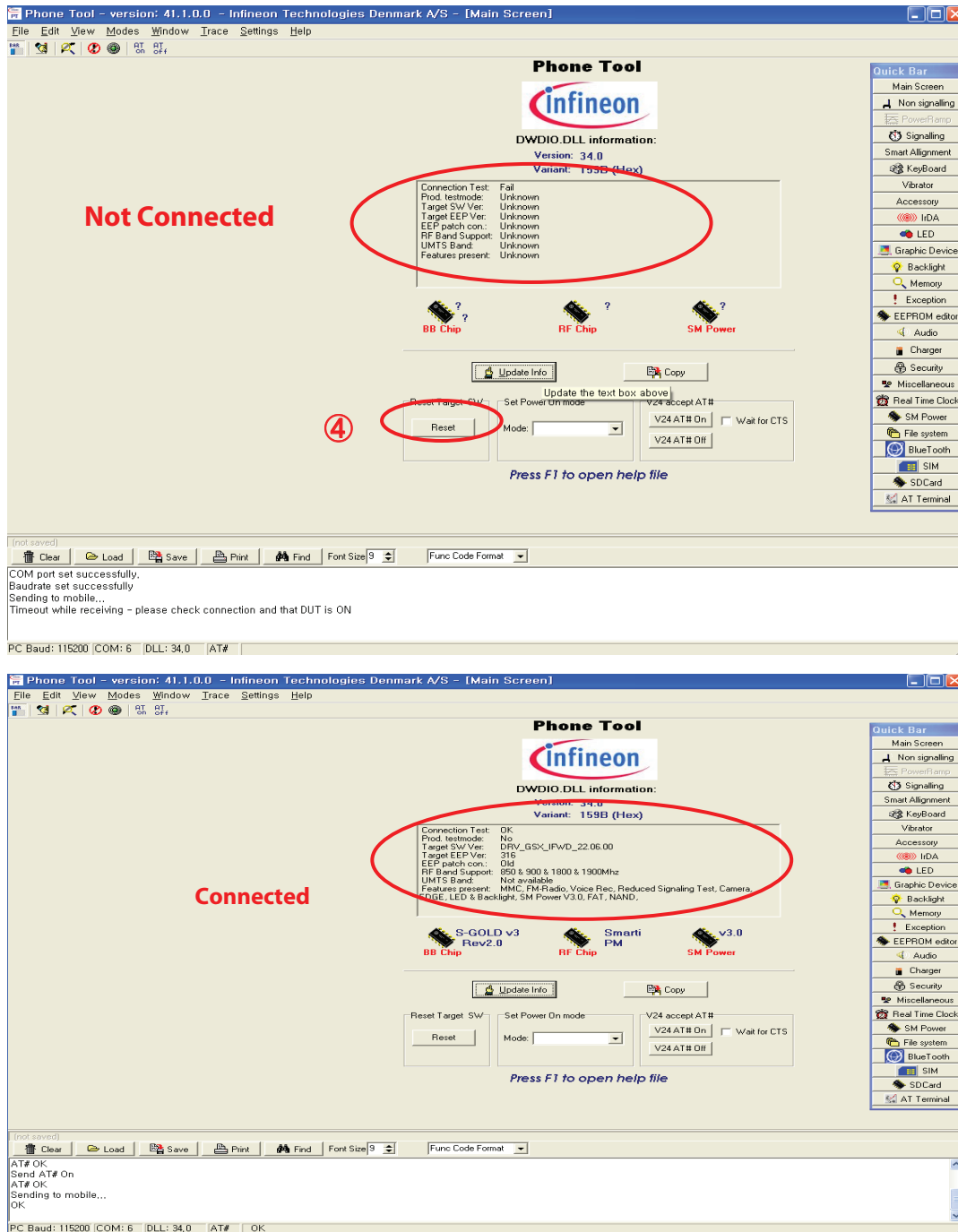
RX test - this is to see if the receiver of the phones is activating normally.

11.2 Setting Method



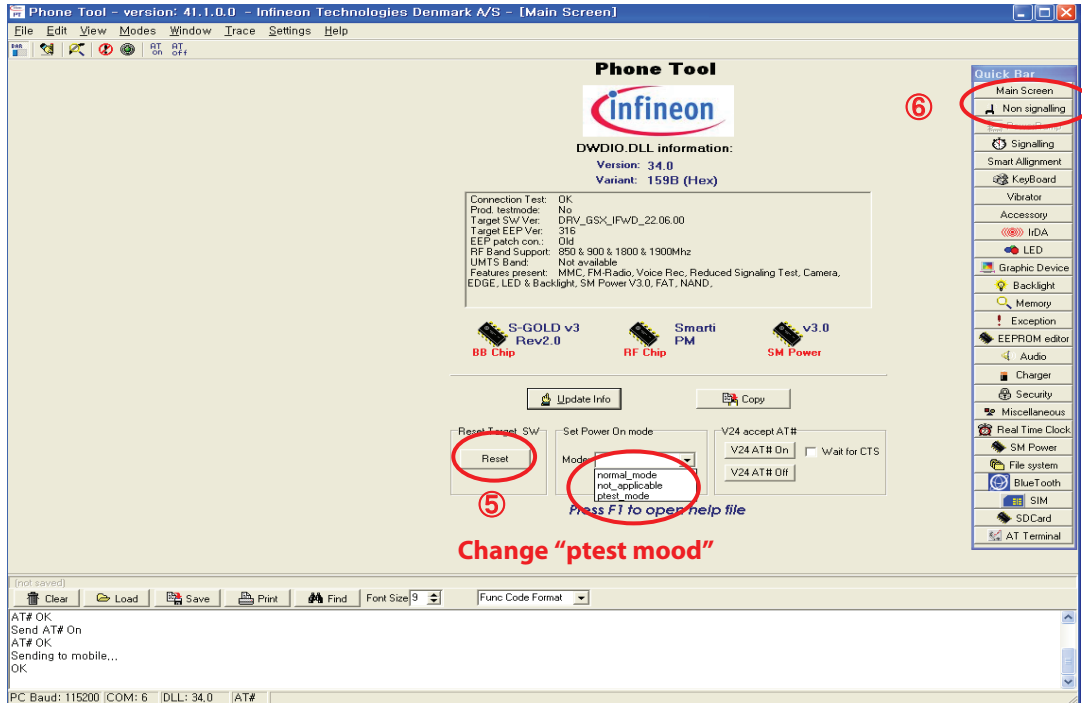
1. Set COM Port
2. Check PC Bau Rate
3. Confirm EEPROM & Delta file prefix name

11. STAND ALONE TEST



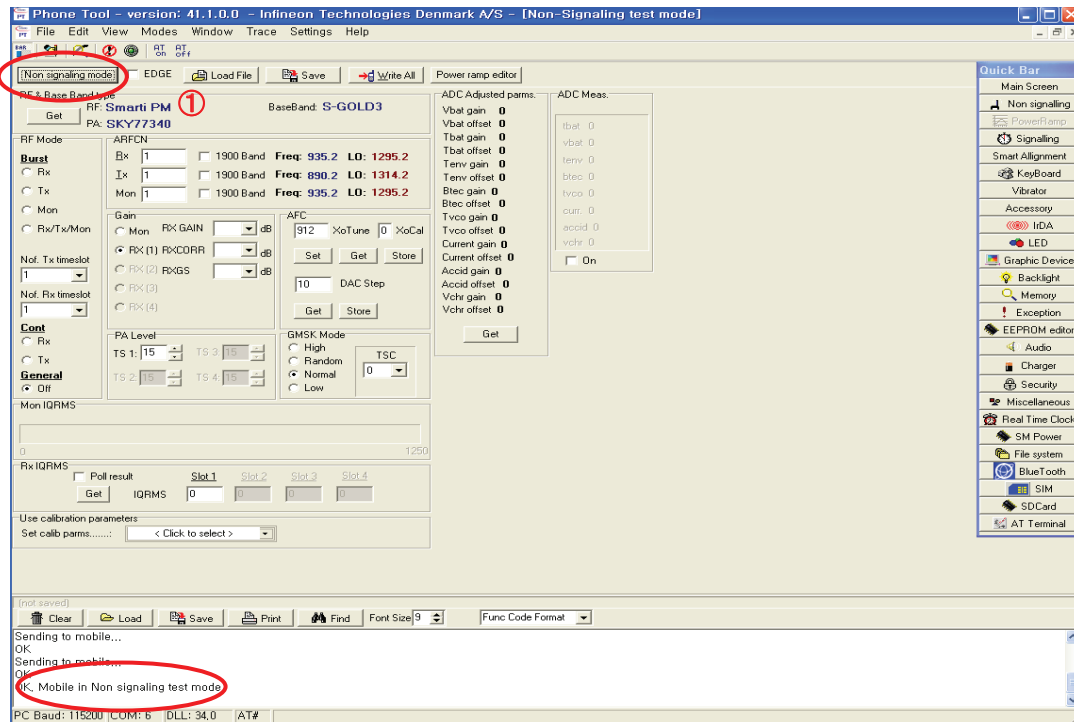
4. Click "Update Info" for communicating Phone and Test-Program

11. STAND ALONE TEST



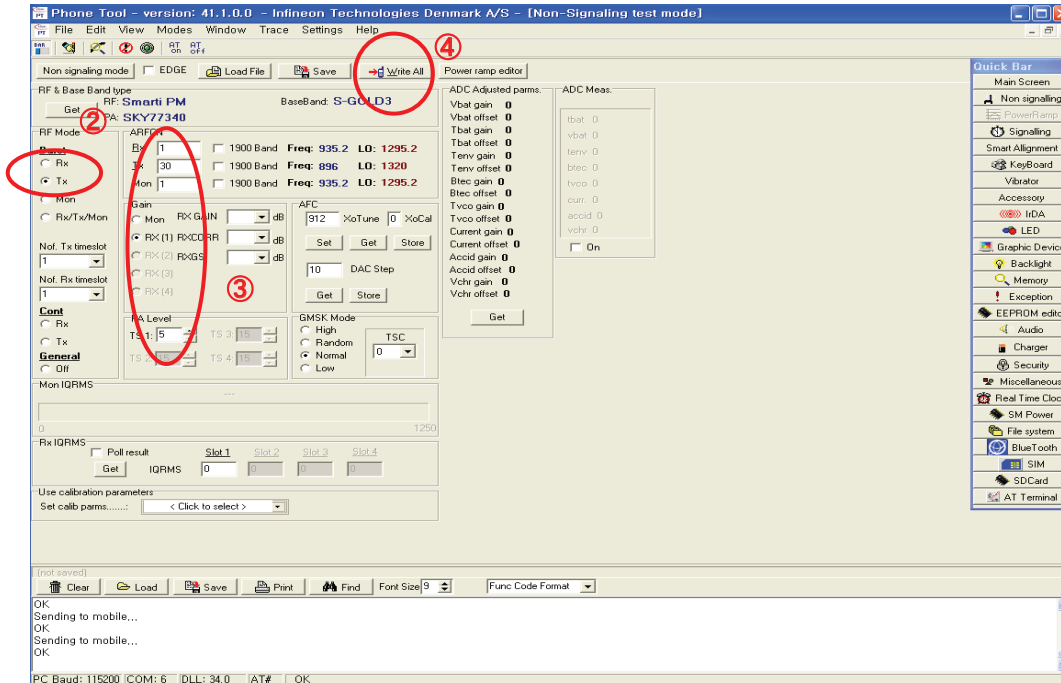
5. For the purpose of the Standalone Test, Change the Phone to "ptest mode" and then Click the "Reset" bar.
6. Select "Non signaling" in the Quick Bar menu. Then Standalone Test setup is finished.

11.3 Tx Test



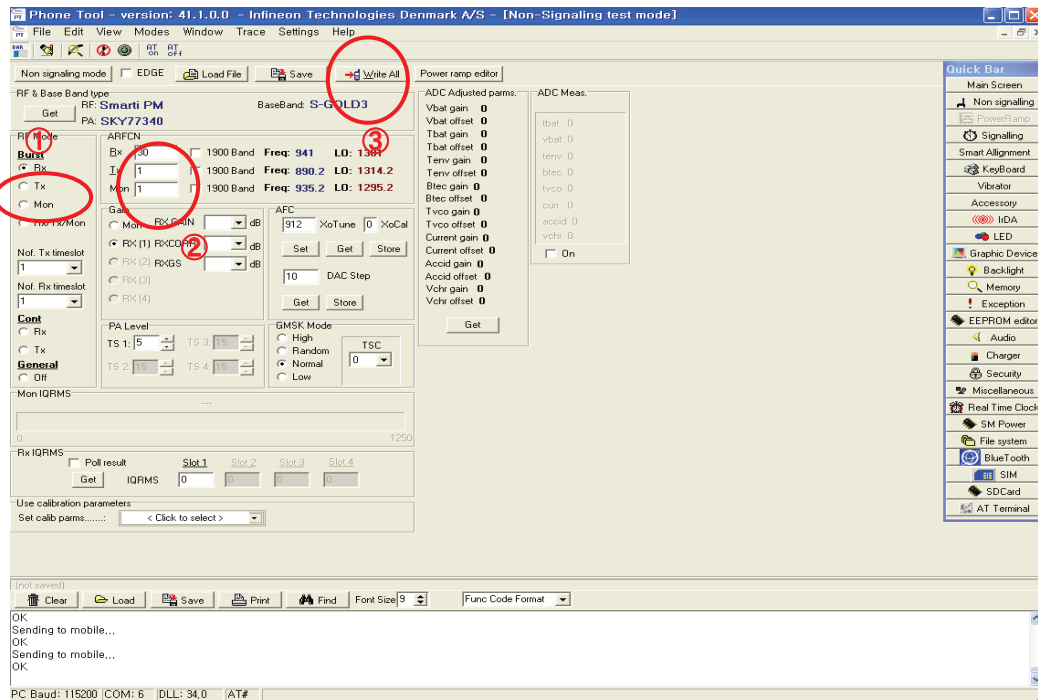
1. "Non signaling mode" bar and then confirm "OK" text in the command line.

11. STAND ALONE TEST



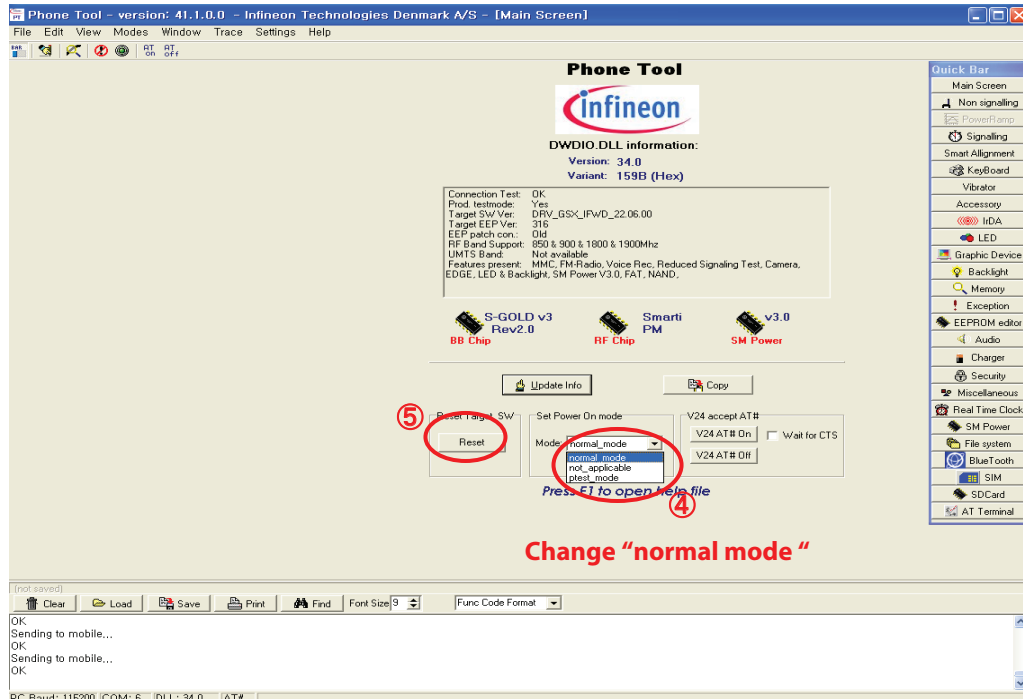
2. Put the number of TX Channel in the ARFCN
3. Select "Tx" in the RF mode menu and "PCL" in the PA Level menu.
4. Finally, Click "Write All" bar and try the efficiency test of Phone.

11.4 Rx Test



1. Put the number of RX Channel in the ARFCN.
2. Select "Rx" in the RF mode menu.
3. Finally, Click "Write All" bar and try the efficiency test of Phone.

11. STAND ALONE TEST



4. The Phone must be changed "normal mode" after finishing Test.
5. Change the Phone to "normal mode" and then Click the "Reset" bar.

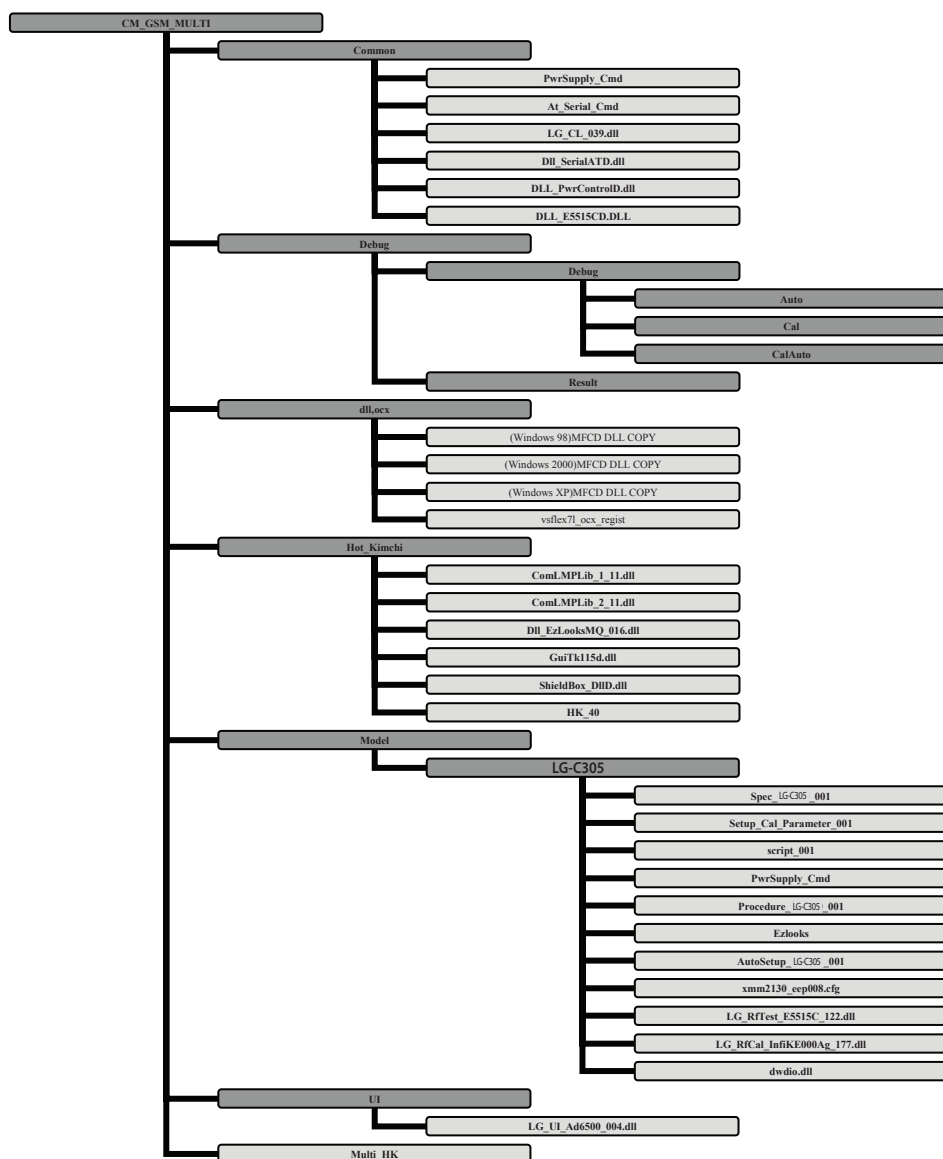
12.AUTO CALIBRATION

12.1 Overview

Auto-cal (Auto Calibration) is the PC side Calibration tool that perform Tx, Rx and Battery Calibration with Agilent 8960(GSM call setting instrument) and Tektronix PS2521G(Programmable Power supply).

Auto-cal generates calibration data by communicating with phone and measuring equipment then write it into calibration data block of flash memory in GSM phone.

12.2 Configuration of HotKimchi



12.AUTO CALIBRATION

12.3 Description of Basic File

12.1 Common

- **LG_CL_039.dll** : Common logic dll, Module In Charge of Reading PID & S/W Version, Booting.
- **Dll_SerialATD.dll** : Serial Communication Module From Phone by AT Command.
- **DLL_PwrControlD.dll** : Communication Module From Power supply.
- **DLL_E5515CD.DLL** : Communication Module From Agilent 8960(Test Set).
- **At_Serial_Cmd.xml** : Definition File of AT Command.
- **PwrSupply_Cmd.xml** : Definition File of Power supply command.

12.2 Debug

- **Debug** - Cal : Result File of Calibration.
Auto : Result File of Auto Test.
CalAuto : Result File of Cal & Auto Test.

12.3 dll, ocx

- **vsflex7l_ocx_regist** : Registration File for System use
- **Windows XXX)MFCD DLL** : Registration File for System use

12.4 HotKimchi

- **HK_40.exe** : Execute File, HK_XX → XX is File Version.
- **ComLMPLib_1_11.dll** : Communication Module With PLC or Shield Box In Automation Rack.
Support to J&S Shield Box and Tescom TC-5981A.
- **ComLMPLib_2_11.dll** : Communication Module With PLC or Shield Box In Automation Rack.
Support to J&S Shield Box and Tescom TC-5981A.
- **Dll_EzLooksMQ_005.dll** : Communication Module with ezTray Installed In Local PC.
- **GuiTk115d.dll** : control library
- **ShieldBox_DIID.dll** : Communication with Shield Box. Support to Tescom TC-5952B.

12.5 Model

- **LG_RfCal_InfiKE000Ag_177.dll** : Main Module of Calibration
- **LG_RfTest_E5515C_122.dll** : Main Module of Auto Test
- **Xmm2130_eep008.cfg** : Cal Data Save binary Module.
- **AutoSetup_LG-C305_100.xml** : RF TEST Setup Module.
- **Ezlooks.xml** : Calibration ezLooks Item & Cal Spec Definition Module.
- **Procedure_LG-C305_001.xml** : RF TEST Procedure Definition Module.
- **Script_001.xml** : RF TEST Setup & calibration Setup Module.
- **Spec_LG-C305_001.xml** : Definition Module of Auto Test Spec
- **Setup_Cal_Parameter_001.xml** : Calibration Definition Module.

12.6 UI

- **LG_UI_Ad6500_002.dll** : ADI Model UI DLL.

12.7 Multi_HK

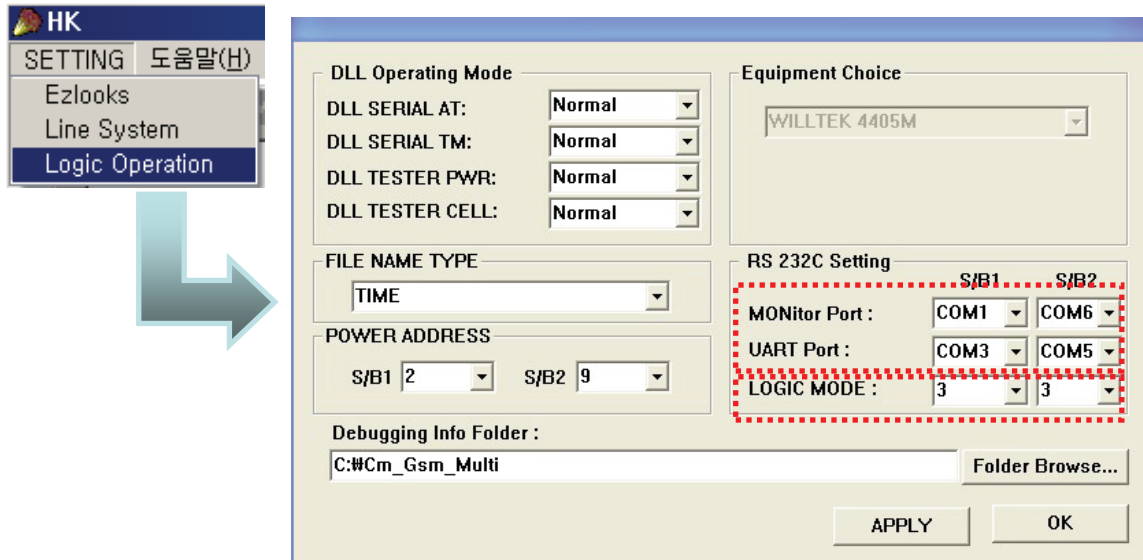
- Registration File For System Setting.

1. Connect as Fig 6-2(RS232 serial cable is connected between COM port of PC and MON port of TEST JIG, in general)
2. Set the Power Supply 4.0V
3. Set the 3rd, 4th of DIP SW ON state always
4. Press the Phone power key, if the Remote ON is used, 1st ON state

12.4 Procedure

1. Copy the file to C:\Cm_Gsm_Multi
2. Copy the files of((Windows XXX)MFCD DLL, vsflex7l_ocx_regist to C:\Cm_Gsm_Multi\dll,ocx
3. Select MFCD DLL of your computer OS
4. Click on "vsflex7l_ocx_regist"
5. Click on "Multi_HK reg"
6. Connect as Fig 11-2 (RS232 serial cable is connected between COM port of PC, in general.)
7. . Run HK_40exe to start calibration.
8. Click " Logic Operation" of "SETTING" menu bar

12.AUTO CALIBRATION



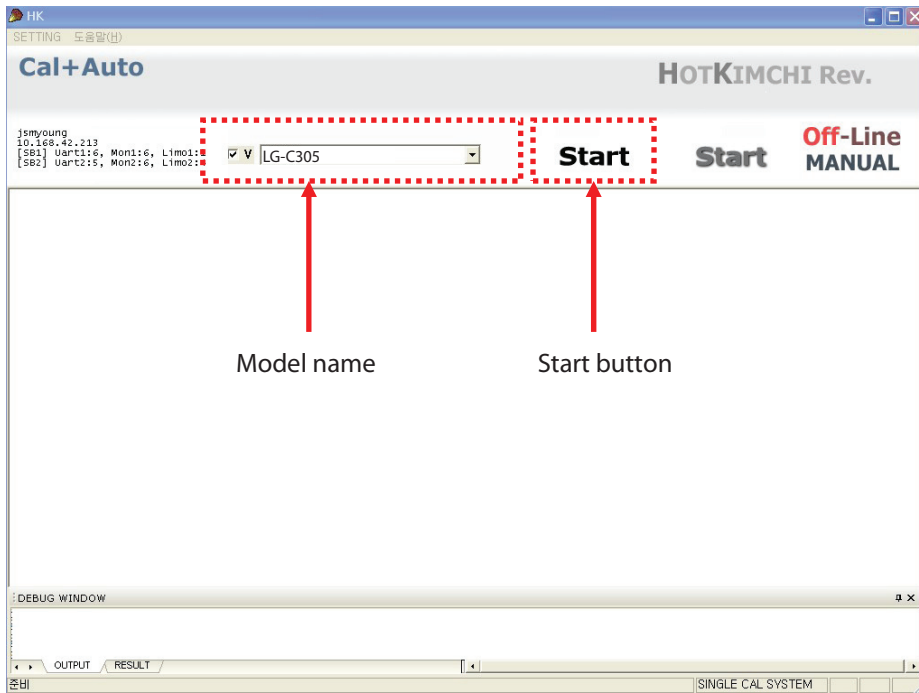
9. Set PORT (using RS232 cable) that PC can communicate with the phone

10. Select " LOGIC MODE" that you want

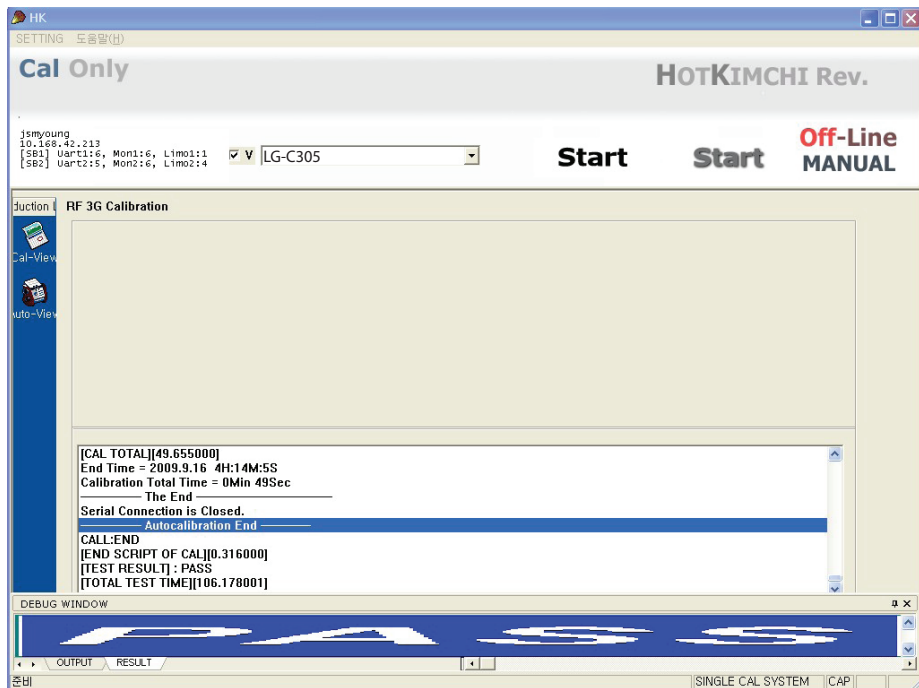
Logic mode: 1-> Calibration only
2-> Auto test only
3-> Cal & Auto

12.AUTO CALIBRATION

11. Select the model name "LG-C305"



12. Click "start" button



12.AUTO CALIBRATION

12.5 AGC

This procedure is for Rx calibration.

In this procedure, We can get RSSI correction value. Set band EGSM and press Start button the result window will show correction values per every power level and gain code and the same measure is performed per every frequency.

12.6 APC

This procedure is for Tx calibration.

In this procedure you can get proper scale factor value and measured power level.

12.7 ADC

This procedure is for battery calibration.

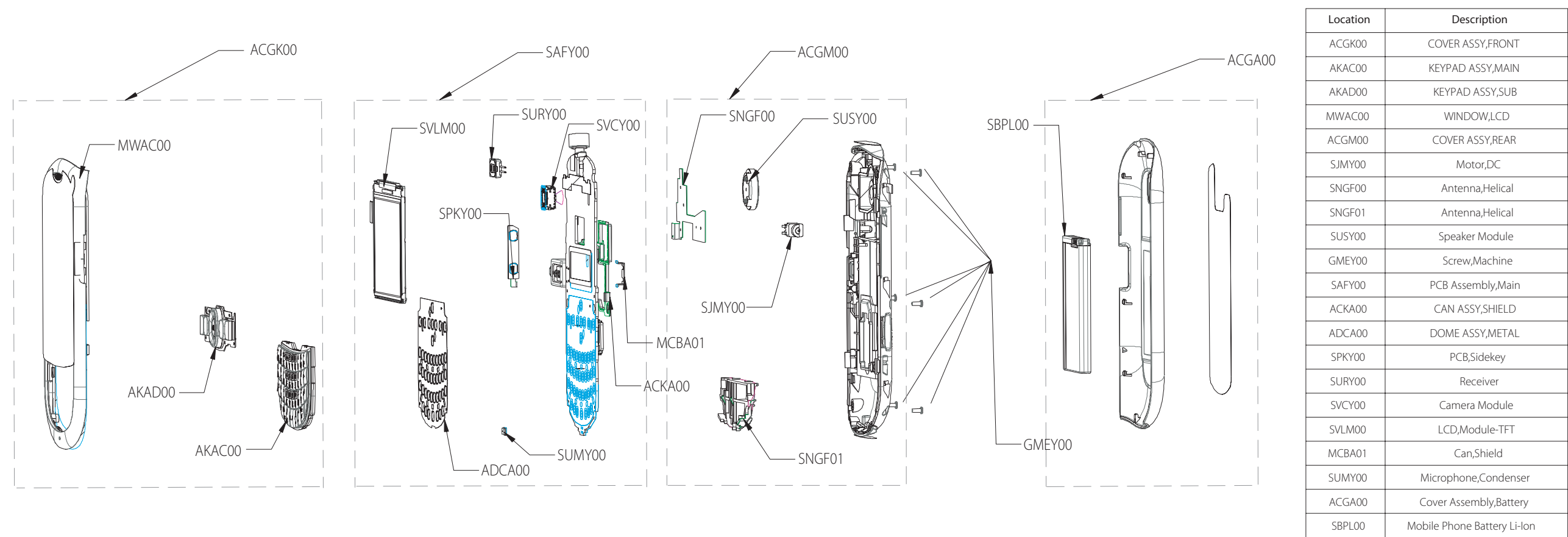
You can get main Battery Config Table and temperature Config Table will be reset.

12.8 Target Power

BAND	Description	Low	Middle	High
GSM 850	Channel	128	191	251
	Frequency	824.2 MHz	836.8 MHz	848.8 MHz
	Max power	32.3dBm	32.3dBm	32.3dBm
EGSM 900	Channel	975	37	124
	Frequency	880.2 MHz	897.4 MHz	914.8 MHz
	Max power	32.3dBm	32.3dBm	32.3dBm
DCS1800	Channel	512	699	885
	Frequency	1710.2 MHz	1747.6 MHz	1784.8 MHz
	Max power	29.5dBm	29.5dBm	29.5dBm
PCS 1900	Channel	512	661	810
	Frequency	1850.2 MHz	1880 MHz	1909.8 MHz
	Max power	29dBm	29dBm	29dBm

13. EXPLODED VIEW & REPLACEMENT PART LIST

13.1 EXPLODED VIEW



13. EXPLODED VIEW & REPLACEMENT PART LIST

13.2 Replacement Parts <Mechanic component>

Note: This Chapter is used for reference, Part order is ordered by SBOM standard on GCSC

Level	Location No.	Description	Part Number	Spec	Remark
1	AAAY00	Addition Assembly	AAAY0486304 7	LG-C305 TURWA WA:White -	
2	AMBA00	Manual Assembly,Operation	AMBA0187501	LG-C305 TURWA ZZ:Without Color LG-C305 manual assy for TUR	
1	APAY00	Package Assembly	APAY0151005 7	LG-C305 TURWA ZZ:Without Color LG-C305 STD(EU1W/Peel)	
2	APLY00	Pallet Assembly	APLY0003901 3	GD510 BALBK ZZ:Without Color EU1 TYPE_Body(SW)+Cap(EU)+AL_1200EA	
3	MBEC00	Box,Carton	MBEC0003601	COMPLEX GD510 CZESV ZZ:Without Color -	
3	MCCL00	Cap,Box	MCCL0002501	COMPLEX GD510 CZESV ZZ:Without Color -	
3	MPCY00	Pallet	MPCY0012403	COMPLEX KG800 FRABK DB:DARK BLUE -	
2	MBAD00	Bag,Vinyl	MBAD0005204	COMPLEX LG-LX260 SPRAG ZZ:Without Color -	
2	MBEE00	Box,Master	MBEE0061001	COMPLEX GD510 CZESV ZZ:Without Color -	
2	MBEF00	Box,Unit	MBEF0148903	COMPLEX LG-C305 TURWA ZZ:Without Color BOXTW, LG-C305 STD(EU1W)	
2	MLAC00	Label,Barcode	MLAC0003018	COMPLEX HB620T O2DBK ZZ:Without Color -	
2	MLAJ00	Label,Master Box	MLAJ0004402	COMPLEX CG300 CGR ZZ:Without Color LABEL,MASTER BOX(for CGR TDR 2VER. mbox_label)	
2	MLAZ01	Label	MLAZ0050901	COMPLEX KU990 GBRBK ZZ:Without Color -	
1	APEY	Phone Assembly	APEY0939804 2	LG-C305 TURWA WA:White -	
2	ACGY00	Cover Assembly,EMS	ACGY0045704 2	LG-C305 TURWA WA:White -	
3	GMEY00	Screw,Machine	GMEY0009201	GMEY0009201 BH + 2.7mM 3.5mM MSWR3 FZB N NLG ELECTRONICS INC.	
5	ACKA00	Can Assembly,Shield	ACKA0037201 2	LG-C300 FRA ZZ:Without Color -	
6	MAAA00	Absorber,Electromagnetic Wave	MAAA0007501	COMPLEX LG-C300 FRA ZZ:Without Color COMPLEX, (empty), , , ,	
6	MCBA00	Can,Shield	MCBA0077401	COMPLEX LG-C300 FRA ZZ:Without Color PRESS, STS, , , ,	
5	ADCA00	Dome Assembly,Metal	ADCA0114601	LG-C300 FRA ZZ:Without Color -	
5	MIDZ00	Insulator	MIDZ0255401	COMPLEX LG-C300 FRA ZZ:Without Color -	
5	MIDZ01	Insulator	MIDZ0255501	COMPLEX LG-C300 FRA ZZ:Without Color -	
5	MIDZ02	Insulator	MIDZ0280901	COMPLEX LG-C300 FRA ZZ:Without Color COMPLEX, (empty), , , ,	
5	MPBZ00	Damper	MPBZ0355701	COMPLEX LG-C300 FRA ZZ:Without Color COMPLEX, (empty), , , ,	

13. EXPLODED VIEW & REPLACEMENT PART LIST

Level	Location No.	Description	Part Number	Spec	Remark
5	MSAZ00	Sheet	MSAZ0073801	COMPLEX LG-C300 FRA ZZ:Without Color COMPLEX, (empty), , , , ,	
5	MTAC00	Tape,Shield	MTAC0094601	COMPLEX GW300 ORFAQ TR:Transparent -	
5	MTAZ00	Tape	MTAZ0317701	COMPLEX LG-C300 FRA ZZ:Without Color -	
6	SC201	Can,Shield	MCBA0059201	COMPLEX GD350 CLP ZZ:Without Color -	
6	ANT301	Contact	MCIZ0004401	COMPLEX LG-C300 FRA ZZ:Without Color -	
2	MLAA00	Label,Approval	MLAA0062316	COMPLEX GU280 OREBK ZZ:Without Color COMPLEX, (empty), , , , ,	

13. EXPLODED VIEW & REPLACEMENT PART LIST

13.2 Replacement Parts <Main component>

Note: This Chapter is used for reference, Part order is ordered by SBOM standard on GCSC

Level	Location No.	Description	Part Number	Spec	Remark
3	SAFY	PCB Assembly,Main	SAFY0383203 2	LG-C305 TURWA MAIN A	
4	SAFB00	PCB Assembly,Main,Insert	SAFB0121301 14	LG-C300 FRA MAIN,1.0	
5	BRAH00	Resin,PC	BRAH0001301	UF-1060	
5	SPKY00	PCB,Sidekey	SPKY0090601	KR045580 POLYI Multi MULTI-2 0.18 EXTRA,SIDEKEY,B,POLYI,0.18 mm,MULTI-2DAE DUCK GDS CO. LTD	
5	SURY00	Receiver	SURY0010120	KR120703W1P ASSY,dB,ohm,1207*2.5T,10mm,WIRE, KIRYN TELECOM CO., LTD	
5	SVCY00	Camera Module	SVCY0026901	C2FK-H313A C2FK-H313A 2M FF, Hynix(1/5"), 7x7x4.1t, SocketLG Innotek.com	
5	SVLM00	LCD,Module-TFT	SVLM0034001	LS024Q3UX12 Main,2.4",320*240,54.3*46.8*1.7t,262K,TFT,TM,NT35399,Landscape LCD, SHARP CORPORATION.	
4	SAFF	PCB Assembly,Main,SMT	SAFF0285203 2	LG-C305 TURWA MAIN A	
5	SAFC00	PCB Assembly,Main,SMT Bottom	SAFC0153101 139	LG-C305 IDNWA MAIN,I	
6	C247	Capacitor,Ceramic,Chip	ECCH0000110	MCH155A100D 10pF 0.25PF 50V NP0 -55TO+125C 1005 R/TP - ROHM CO.,LTD.	
6	C411,C412	Capacitor,Ceramic,Chip	ECCH0000112	MCH155C150J 15pF 5% 50V NP0 -55TO+125C 1005 R/TP -ROHM CO.,LTD.	
6	C132	Capacitor,Ceramic,Chip	ECCH0000113	MCH155A180J 18pF 5% 50V NP0 -55TO+125C 1005 R/TP -ROHM CO.,LTD.	
6	C103,C116, C343,C396, C398,C415, C416	Capacitor,Ceramic,Chip	ECCH0000115	MCH155A220JK 22pF 5% 50V NP0 -55TO+125C 1005 R/TP - ROHM CO.,LTD.	
6	C341,C394, C427	Capacitor,Ceramic,Chip	ECCH0000117	CL05C270JB5NNNC 27pF 5% 50V NP0 -55TO+125C 1005 R/TP 0.5SAMSUNG ELECTRO-MECHANICS CO., LTD.	
6	C225,C230, C232,C237, C238,C315	Capacitor,Ceramic,Chip	ECCH0000120	MCH155A390J 39pF 5% 50V NP0 -55TO+125C 1005 R/TP -ROHM CO.,LTD.	
6	C108,C109, C110,C112, C142,C143, C209,C210, C216,C217, C244,C245, C246	Capacitor,Ceramic,Chip	ECCH0000122	MCH155A470JK 47pF 5% 50V NP0 -55TO+125C 1005 R/TP - ROHM CO.,LTD.	
6	C241	Capacitor,Ceramic,Chip	ECCH0000129	MCH155A121JK 0.12nF 5% 50V NP0 -55TO+125C 1005 R/TP - ROHM CO.,LTD.	

13. EXPLODED VIEW & REPLACEMENT PART LIST

Level	Location No.	Description	Part Number	Spec	Remark
6	C102,C127, C215,C260, C318,C319, C323,C326, C348,C429, C430	Capacitor,Ceramic,Chip	ECCH0000143	MCH155CN102KK 1nF 10% 50V X7R -55TO+125C 1005 R/TP - ROHM CO.,LTD.	
6	C229	Capacitor,Ceramic,Chip	ECCH0000145	MCH155CN152KK 1.5nF 10% 50V X7R -55TO+125C 1005 R/TP - ROHM CO.,LTD.	
6	C119,C123	Capacitor,Ceramic,Chip	ECCH0000151	CL05B472KB5NNNC 4.7nF 10% 25V X7R -55TO+125C 1005 R/TP - SAMSUNG ELECTRO-MECHANICS CO., LTD.	
6	C228,C316	Capacitor,Ceramic,Chip	ECCH0000155	MCH153CN103KK 10nF 10% 16V X7R -55TO+125C 1005 R/TP - ROHM CO.,LTD.	
6	C243,C251	Capacitor,Ceramic,Chip	ECCH0000179	GRM155R71C223K 22nF 10% 16V X5R -55TO+85C 1005 R/TP - MURATA MANUFACTURING CO.,LTD.	
6	C203,C204, C257,C353	Capacitor,Ceramic,Chip	ECCH0000182	GRM155R61A104K 0.00001F 10% 10V X5R -55TO+85C 1005 R/TP - MURATA MANUFACTURING CO.,LTD.	
6	L318	Capacitor,Ceramic,Chip	ECCH0000195	GRM1555C1H3R9C 3.9pF 0.25PF 50V NP0 -55TO+125C 1005 R/TP -MURATA MANUFACTURING CO.,LTD.	
6	C146,C205, C206,C213, C214,C218, C220	Capacitor,Ceramic,Chip	ECCH0000198	CL05A225MQ5NSNC 2.2uF 20% 6.3V X5R -55TO+85C 1005 R/TP - SAMSUNG ELECTRO-MECHANICS CO., LTD.	
6	C308	Capacitor,Ceramic,Chip	ECCH0001001	C1005C0G1H6R8CT000F 6.8pF 0.5PF 50V NP0 -55TO+125C 1005 R/TP -TDK CORPORATION	
6	C211,C212	Capacitor,Ceramic,Chip	ECCH0002001	C1005JB0J104KT000F 100nF 10% 6.3V Y5P -30TO+85C 1005 R/TP -TDK CORPORATION	
6	C120,C122	Capacitor,Ceramic,Chip	ECCH0002002	C1005X7R1A473KT000F 47nF 10% 10V Y5P -30TO+85C 1005 R/TP -TDK CORPORATION	
6	C104,C114, C125,C139, C140,C145, C254,C301, C310,C345, C347,C349, C401,C402, C420,C433	Capacitor,Ceramic,Chip	ECCH0004904	GRM155R60J105K 0.001F 10% 6.3V X5R -55TO+85C 1005 R/TP - MURATA MANUFACTURING CO.,LTD.	
6	C101,C115, C250,C419, C421,C422, C426	Capacitor,Ceramic,Chip	ECCH0005603	GRM188R61A225K 2.2uF 10% 10V X5R -55TO+85C 1608 R/TP - MURATA MANUFACTURING CO.,LTD.	
6	C231	Capacitor,Ceramic,Chip	ECCH0005604	GRM188R60J106M 10000000 pF,6.3V,M,X5R,TC,1608,R/TP,0.8 mm MURATA MANUFACTURING CO.,LTD.	
6	C311,C356, C357,C358, C399	Capacitor,Ceramic,Chip	ECCH0006201	C1608X5R0J475KT000N 4.7uF 10% 6.3V X5R -55TO+85C 1608 R/TP -TDK CORPORATION	
6	C317,C327	Capacitor,Ceramic,Chip	ECCH0007802	CV105X5R475M10AT 4.7uF 20% 10V X5R -55TO+85C 1608 R/TP - KYOCERA CORPORATION	
6	C134,C202	Capacitor,Ceramic,Chip	ECCH0007803	CL10A106MP8NNNC 0F 20% 10V X5R -55TO+85C 1608 R/TP 0.8MMSAMSUNG ELECTRO-MECHANICS CO., LTD.	

13. EXPLODED VIEW & REPLACEMENT PART LIST

Level	Location No.	Description	Part Number	Spec	Remark
6	C235	Capacitor,TA,Conformal	ECTH0002703	TCTAL1A107M8R 0.0001F 20% 10V 50UA -55TO+125C 0OHM 3.2x1.6x1.1 NONE SMD R/TPROHM CO.,LTD.	
6	C305,C320	Capacitor,Ceramic,Chip	ECZH0000802	C1005C0G1H010CT 1pF 0.25PF 50V NP0 -55TO+125C 1005 R/TP -TDK CORPORATION	
6	C147	Capacitor,Ceramic,Chip	ECZH0000806	C1005C0G1H050CT000F 5pF 0.25PF 50V NP0 -55TO+125C 1005 R/TP -TDK CORPORATION	
6	C201,C387, C434,C435, C436	Capacitor,Ceramic,Chip	ECZH0000813	C1005C0G1H101JT 100pF 5% 50V NP0 -55TO+125C 1005 R/TP -TDK CORPORATION	
6	C314,C371	Capacitor,Ceramic,Chip	ECZH0000822	C1005C0G1H1R5CT000F 1.5pF 0.25PF 50V NP0 -55TO+125C 1005 R/TP -TDK CORPORATION	
6	C253,C302, C303,C304, C322,C325	Capacitor,Ceramic,Chip	ECZH0000830	C1005C0G1H330JT000F 33pF 5% 50V NP0 -55TO+125C 1005 R/TP -TDK CORPORATION	
6	C306,C408, C409,C410	Capacitor,Ceramic,Chip	ECZH0000841	C1005C0G1H560JT000F 56pF 5% 50V NP0 -55TO+125C 1005 R/TP -TDK CORPORATION	
6	C242	Capacitor,Ceramic,Chip	ECZH0000901	C1005C0G1H240JT000F 24pF 5% 50V NP0 -55TO+125C 1005 R/TP -TDK CORPORATION	
6	C259	Capacitor,Ceramic,Chip	ECZH0001116	C1005X7R1H271KT000F 270pF 10% 50V X7R -55TO+125C 1005 R/TP -TDK CORPORATION	
6	C118	Capacitor,Ceramic,Chip	ECZH0001210	C1005Y5V1A474ZT000F 470nF -20TO+80% 10V Y5V -30TO+85C 1005 R/TP -TDK CORPORATION	
6	C221,C255, C256,C346, C417,C423, C424,C425, C428,C432	Capacitor,Ceramic,Chip	ECZH0001215	C1005X5R1A105KT000F 1uF 10% 10V X5R -55TO+85C 1005 R/TP -TDK CORPORATION	
6	C105,C130, C131	Capacitor,Ceramic,Chip	ECZH0001216	C1005X5R1A224KT000E 220nF 10% 10V X5R -55TO+85C 1005 R/TP -TDK CORPORATION	
6	C117,C121, C141,C312, C313	Capacitor,Ceramic,Chip	ECZH0001217	GRM155R60J474K 470nF 10% 6.3V X5R -25TO+70C 1005 BK-DUP -MURATA MANUFACTURING CO.,LTD.	
6	C106,C111, C113,C124, C126,C128, C129,C137, C138,C222, C224,C233, C236,C239, C355,C405, C406,C407, C413,C418, C431	Capacitor,Ceramic,Chip	ECZH0003103	GRM36X7R104K10PT 100nF 10% 10V X7R -55TO+125C 1005 R/TP -MURATA MANUFACTURING CO.,LTD.	
6	C248,C249	Capacitor,Ceramic,Chip	ECZH0003118	GRM155R71H561K 560pF 10% 50V X7R -55TO+125C 1005 R/TP -MURATA MANUFACTURING CO.,LTD.	
6	C223	Capacitor,Ceramic,Chip	ECZH0003503	GRM188R61E105K 1uF 10% 25V X5R -55TO+85C 1608 R/TP -MURATA MANUFACTURING CO.,LTD.	
6	C226	Capacitor,Ceramic,Chip	ECZH0003504	GRM188R71E104K 100nF 10% 25V X7R -55TO+125C 1608 R/TP -MURATA MANUFACTURING CO.,LTD.	

13. EXPLODED VIEW & REPLACEMENT PART LIST

Level	Location No.	Description	Part Number	Spec	Remark
6	C107	Capacitor,Ceramic,Chip	ECZH0025502	GRM219R60J226M GRM219R60J226M,22000000 pF,6.3V ,M ,X5R ,HD ,2012 ,R/TP MURATA MANUFACTURING CO.,LTD.	
6	ZD401,ZD402,ZD403	Diode,TVS	EDTY0008606	PRSB6.8C 4.7V 5.7 -- 10W - R/TP 2P 1PROTEK DEVICES INC.	
6	D102,D202,D203	Diode,TVS	EDTY0009801	VSMF05LCC 5V 6V 12V 2A 25W SOT-963 R/TP 6P 5PROTEK DEVICES INC.	
6	D101,VA203,VA204,VA403	Diode,TVS	EDTY0010101	ESD9B5.0ST5G ESD9B5.0ST5G,SOD-923,5 V,300 mW,R/TP,15pF ON SEMICONDUCTOR	
6	VA211	Diode,TVS	EDTY0010501	RCLAMP1521P.TCT 15V 16.7 28V 4A 0W SLP1006P2 R/TP 2P 1SEMTECH CORPORATION	
6	L308	Inductor,Multilayer,Chip	ELCH0001403	LL1005-FHL1N0S 1NH 0.3NH 0V 500mA 0.1OHM 20GHZ 8 NON SHIELD 1 1.0X0.5X0.5MM R/TP TOKO, INC.	
6	L307,L321	Inductor,Multilayer,Chip	ELCH0003815	LQG15HS2N7S02D 2NH 0.3NH 0V 300mA 0.15OHM 6GHZ 8 NON SHIELD 1 1.0X0.5X0.5MM R/TP MURATA MANUFACTURING CO.,LTD.	
6	L305	Inductor,Multilayer,Chip	ELCH0003818	LQG15HS9N1J02D 9.1NH 5% 0V 300mA 0.26OHM 3.4GHZ 8 NON SHIELD 1 1.0X0.5X0.5MM R/TP MURATA MANUFACTURING CO.,LTD.	
6	L314	Inductor,Multilayer,Chip	ELCH0003825	LQG15HS56N02D 56NH 5% 0V 200mA 0.82OHM 800MHZ 8 NON SHIELD 1 1.0X0.5X0.5MM R/TP MURATA MANUFACTURING CO.,LTD.	
6	L301,L302,L303,L306	Inductor,Multilayer,Chip	ELCH0003826	LQG15HS3N3S02D 3.3NH 0.3NH 0V 300mA 0.17OHM 6GHZ 8 NON SHIELD 1 1.0X0.5X0.5MM R/TP MURATA MANUFACTURING CO.,LTD.	
6	L322	Inductor,Multilayer,Chip	ELCH0003838	LQG15HS8N2J02 8.2NH 5% - 300mA 0.24OHM 3.7KHZ 8 SHIELD 1 1.0X0.5X0.55MM R/TP MURATA MANUFACTURING CO.,LTD.	
6	L201,L205,L206	Inductor,Multilayer,Chip	ELCH0003842	LQG15HSR10J02 100NH 5% - 150mA 1.25OHM 600HZ 8 SHIELD 1 1.0X0.5X0.55MM R/TP MURATA MANUFACTURING CO.,LTD.	
6	L319,L320	Inductor,Multilayer,Chip	ELCH0003847	LQG15HS1N8S02 LQG15HS1N8S02,1.8 nH,S,1005,R/TP,chip coil MURATA MANUFACTURING CO.,LTD.	
6	L309	Inductor,Multilayer,Chip	ELCH0005001	HK10052N2S 2.2NH 0.3NH 0V 8A 10GOHM 70mHZ 300m NON SHIELD 1 1.0X0.5X0.5MM R/TP TAIYO YUDEN CO.,LTD	
6	L304	Inductor,Multilayer,Chip	ELCH0005004	HK100522NJ 22NH 5% 0V 8A 2.8GOHM 420mHZ 300m NON SHIELD 1 1.0X0.5X0.5MM R/TP TAIYO YUDEN CO.,LTD	
6	L312	Inductor,Multilayer,Chip	ELCH0005005	HK100527NJ 27NH 5% 0V 8A 2.3GOHM 470mHZ 300m NON SHIELD 1 1.0X0.5X0.5MM R/TP TAIYO YUDEN CO.,LTD	
6	L202,L203,L204,L207,L208,L209	Inductor,Multilayer,Chip	ELCH0005009	HK1005R10J 100NH 5% 0V 8A 1GOHM 940mHZ 150m NON SHIELD 1 1.0X0.5X0.5MM R/TP TAIYO YUDEN CO.,LTD	
6	L313	Inductor,Multilayer,Chip	ELCH0010402	LK1005R27-T LK1005R27-T,270 nH,M ,1005 ,R/TP ,CHIP TAIYO YUDEN CO.,LTD	
6	L101,L317	Inductor,Wire Wound,chip	ELCP0009410	LQM2HPN3R3MG0 LQM2HPN3R3MG0,3.3 uH,N,2x2.5x1.0,R/TP,chip power MURATA MANUFACTURING CO.,LTD.	

13. EXPLODED VIEW & REPLACEMENT PART LIST

Level	Location No.	Description	Part Number	Spec	Remark
6	J201	Jack,Phone	ENJE0008001	JAM3333-F32-7F 1P 4P ANGLE R/TP 4mm BLACK 6P -HON HAI PRECISION INDUSTRY CO.,LTD.	
6	CN403	Connector,FFC/FPC/PIC	ENQY0014201	04-6293-627-005-829+ 27P 0.30MM FPC STRAIGHT BOTH SMD R/TP LOCKING -KYOCERA ELCO	
6	CN203	Connector,I/O	ENRY0010801	04-5151-005-100-883 5P 0.65MM ANGLE RECEPTACLE DIP R/TP -KYOCERA ELCO	
6	S201	Card Socket	ENSY0020902	DM3AT-SF-PEJM5(21) 8,ETC,1.1 mm,13.85x15.95x1.68t,Metal shall change HIROSE ELECTRIC CO., LTD.	
6	J401	Card Socket	ENSY0022101	GCA26C-6S-H15-E1500 GCA26C-6S-H15-E1500,6,ETC2.54 mm,H=1.5 LS Mtron Ltd.	
6	CN402	Card Socket	ENSY0023701	SD-105076-001 Camera 24P STRAIGHT SMD R/TP -MOLEX INC.	
6	SW301	Connector,RF	ENWY0008701	MS-156C NONE STRAIGHT SOCKET SMD T/REEL AU 50OHM 400mDBHIROSE ELECTRIC CO., LTD.	
6	CN201	Terminal Block	ENZY0020402	HSBC-3PT25-17N HSBC-3PT25-17N,3,2.5 mm,BOTTOM HAN SHIN TERMINAL CO., LTD.	
6	Q301	TR,Bipolar	EQBN0019201	KTC3770V VSM,0.1 W,R/TP,1.2*1.2*0.5 Vcbo=20,Vceo=12,Vebo=2V,Ic=100mA KEC CORP.	
6	Q101,Q401	TR,Bipolar	EQBN0020501	KTC4075E NPN 5V 60V 50V 150mA 100NA 700 100mW ESM R/TP 3PKEC CORP.	
6	Q201	FET	EQFP0007601	KTJ6131E P-CHANNEL MOSFET -30V +-20 -0.05A 200HM 100mW ESM R/TP 3PKEC CORP.	
6	R411	Resistor,Chip	ERHY0000105	MCR01MZIP5F51R0 51OHM 1% 1/16W 1005 R/TP -ROHM CO.,LTD.	
6	R236	Resistor,Chip	ERHY0000140	MCR01MZIP5F3602 36KOHM 1% 1/16W 1005 R/TP -ROHM CO.,LTD.	
6	R233	Resistor,Chip	ERHY0000185	MCR01MZIP5F8200 820OHM 1% 1/16W 1005 R/TP -ROHM CO.,LTD.	
6	R137	Resistor,Chip	ERHY0000241	MCR01MZIP5J102 1KOHM 5% 1/16W 1005 R/TP -ROHM CO.,LTD.	
6	R125	Resistor,Chip	ERHY0000254	MCR01MZIP5J472 4.7KOHM 5% 1/16W 1005 R/TP -ROHM CO.,LTD.	
6	R119	Resistor,Chip	ERHY0000272	MCR01MZIP5J433 43KOHM 5% 1/16W 1005 R/TP -ROHM CO.,LTD.	
6	R118,R237, R402,R404, R405,R406, R412,R413, R414,R415, R416,R421, R422,R423, R424,R425, R426,R428, R429,R445, R446	Resistor,Chip	ERHY0003301	MCR01MZIP5J101 100OHM 5% 1/16W 1005 R/TP -ROHM CO.,LTD.	
6	R107,R216	Resistor,Chip	ERHZ0000204	MCR01MZIP5F1003 100KOHM 1% 1/16W 1005 R/TP -ROHM CO.,LTD.	
6	R219,R327	Resistor,Chip	ERHZ0000206	MCR01MZIP5F10R0 10OHM 0.1% 1/16W 1005 R/TP -ROHM CO.,LTD.	

13. EXPLODED VIEW & REPLACEMENT PART LIST

Level	Location No.	Description	Part Number	Spec	Remark
6	R420	Resistor,Chip	ERHZ0000213	MCR01MZP5F1203 120KOHM 1% 1/16W 1005 R/TP -ROHM CO.,LTD.	
6	R201,R208	Resistor,Chip	ERHZ0000240	MCR01MZP5F20R0 20OHM 1% 1/16W 1005 R/TP -ROHM CO.,LTD.	
6	R234	Resistor,Chip	ERHZ0000278	MCR01MZP5F3901 3.9KOHM 1% 1/16W 1005 R/TP -ROHM CO.,LTD.	
6	R213	Resistor,Chip	ERHZ0000295	MCR01MZP5F5102 51KOHM 1% 1/16W 1005 R/TP -ROHM CO.,LTD.	
6	R401,R433, R435,R436, R437,R438, R439,R440, R441,R442	Resistor,Chip	ERHZ0000355	MCR01MZP5F2700 270 ohm,1/16W,F,1005,R/TP ROHM CO.,LTD.	
6	R122,R260, R450,R451, R452	Resistor,Chip	ERHZ0000402	MCR01MZP5J100 10OHM 5% 1/16W 1005 R/TP -ROHM CO.,LTD.	
6	R102,R443, R448	Resistor,Chip	ERHZ0000405	MCR01MZP5J103 10KOHM 5% 1/16W 1005 R/TP -ROHM CO.,LTD.	
6	R105,R108, R113,R114, R117,R121, R130,R131, R132,R133, R134,R148, R205,R217, R261,R314, R332,R409, R427,R444	Resistor,Chip	ERHZ0000406	MCR01MZP5J104 100KOHM 5% 1/16W 1005 R/TP -ROHM CO.,LTD.	
6	R227,R262	Resistor,Chip	ERHZ0000407	MCR01MZP5J105 1KOHM 5% 1/16W 1005 R/TP -ROHM CO.,LTD.	
6	R447	Resistor,Chip	ERHZ0000412	MCR01MZP5J122 1.2KOHM 5% 1/16W 1005 R/TP -ROHM CO.,LTD.	
6	R206,R207	Resistor,Chip	ERHZ0000434	MCR01MZP5J1R0 1OHM 5% 1/16W 1005 R/TP -ROHM CO.,LTD.	
6	R410	Resistor,Chip	ERHZ0000441	MCR01MZP5J220 22OHM 5% 1/16W 1005 R/TP -ROHM CO.,LTD.	
6	R215,R218, R232,R407, R408	Resistor,Chip	ERHZ0000443	MCR01MZP5J222 2.2KOHM 5% 1/16W 1005 R/TP -ROHM CO.,LTD.	
6	R226	Resistor,Chip	ERHZ0000445	MCR01MZP5J224 220KOHM 5% 1/16W 1005 R/TP -ROHM CO.,LTD.	
6	R303	Resistor,Chip	ERHZ0000449	MCR01MZP5J243 24KOHM 5% 1/16W 1005 R/TP -ROHM CO.,LTD.	
6	R222,R223	Resistor,Chip	ERHZ0000451	MCR01MZP5J270 270OHM 5% 1/16W 1005 R/TP -ROHM CO.,LTD.	
6	R403,R419	Resistor,Chip	ERHZ0000465	MCR01MZP5J332 3.3KOHM 5% 1/16W 1005 R/TP -ROHM CO.,LTD.	
6	R109	Resistor,Chip	ERHZ0000475	MCR01MZP5J392 3.9KOHM 5% 1/16W 1005 R/TP -ROHM CO.,LTD.	
6	R204,R228	Resistor,Chip	ERHZ0000483	MCR01MZP5J470 47OHM 5% 1/16W 1005 R/TP -ROHM CO.,LTD.	
6	R106	Resistor,Chip	ERHZ0000484	MCR01MZP5J471 470OHM 5% 1/16W 1005 R/TP -ROHM CO.,LTD.	

13. EXPLODED VIEW & REPLACEMENT PART LIST

Level	Location No.	Description	Part Number	Spec	Remark
6	R305,R417	Resistor,Chip	ERHZ0000485	MCR01MZIP5J472 4.7KOHM 5% 1/16W 1005 R/TP -ROHM CO.,LTD.	
6	R202,R203, R209,R210, R211	Resistor,Chip	ERHZ0000486	MCR01MZIP5J473 47KOHM 5% 1/16W 1005 R/TP -ROHM CO.,LTD.	
6	R110	Resistor,Chip	ERHZ0000499	MCR01MZIP5J562 5.6KOHM 5% 1/16W 1005 R/TP -ROHM CO.,LTD.	
6	R224	Resistor,Chip	ERHZ0000529	MCR01MZIP5J152 1.5KOHM 5% 1/16W 1005 R/TP -ROHM CO.,LTD.	
6	R304	Resistor,Chip	ERHZ0000531	MCR01MZIP5J271 270OHM 5% 1/16W 1005 R/TP -ROHM CO.,LTD.	
6	R306	Resistor,Chip	ERHZ0003801	MCR01MZIP5J5R1 5.1OHM 5% 1/16W 1005 R/TP -ROHM CO.,LTD.	
6	U103	IC,Analog Switch	EUSY0173801	AAT4290IJS AAT4290IJS,SC70JW ,8 PIN,R/TP ,5 Individual Load Switch ANALOGIC TECH	
6	U401	IC,Bus Controller	EUSY0300008	PP2106M3 1.8/2.6V 1mA - MLF R/TP 28P -G5 CORPORATION	
6	U402	IC,Charge Pump	EUSY0344403	RT9396GQW QFN,24,R/TP,4CH+2LDO,IC,Sub PMICIC,Sub PMIC RICHTEK TECHNOLOGY CORP.	
6	U303	IC,LDO Voltage Regulator	EUSY0355701	RP103K281D-TR-F 1.7V TO 5.25V 2.8V 400mW DFN R/TP 4P - RICOH COMPANY, LTD.	
6	U201	IC,Analog Multiplexer	EUSY0372001	TS5USBA33402YZPR TS5USBA33402,WCSP,20,R/TP,MUIC TEXAS INSTRUMENTS INCO.	
6	U202	IC,Audio Sub System	EUSY0403901	WM9093ECS/R 1.71~5.5V 0W WLCSP R/TP 20P -WOLFSON MICROELECTRONICS PLC	
6	U204	IC,TTL	EUSY0407701	LMV331 2.7~5.5V - COMPARATOR SC70 R/TP 5P -TEXAS INSTRUMENTS INCO.	
6	U203	IC,Voltage Reference	EUSY0410801	RT9524 DFN,10,R/TP,DFN Cal Test Mode Single Charger IC for Micro USB,IC,ChargerIC,Charger RICHTEK TECHNOLOGY CORP.	
6	U102	IC,MCP,NOR	EUSY0417801	PF38F6066M0Y3DE NOR/1GBIT + PSRAM/256MBIT 1.7VTO1.9V 11 8 1.2 TR 56P - -Numonyx Asia Pacific Pte Ltd.	
6	U101	IC,Digital Signal Processors	EUSY0421201	PMB8810 0 0 0 NONE NONE BGA R/TP 217P -INFINEON TECHNOLOGIES	
6	X301	Oscillator,TCXO	EXST0001901	TG-5010LH-87N 26MHZ 2.5PPM 2.8V 32.0x25.0x10.0MM - SMD R/TPPSON TOYOCOM CORP	
6	X101	Crystal	EXXY0018701	FC-135(12.5PF, +-20PPM) 32.768KHZ 20PPM 12.5PF 32*15 SMD R/TPSEIKO EPSON CORPORATION	
6	X102	Crystal	EXXY0027001	DSX321G-26M(8PF) 26MHZ 10PPM 0F NONE SMD R/TPDAISHINKU CORPORATION.	
6	L210,L211, R103,R111, R112,R212, R214,R251, R252,R267, R315,R316, R338	Wire Pad,Short	SAFP0000501	LG-VS760 VRZ	
6	PT101	Thermistor,NTC	SETY0006301	NCP15XH103J03RC 10KOHM 5% 0V 0A 3.35KK SMD P/TP 1005sizeMURATA MANUFACTURING CO.,LTD.	

13. EXPLODED VIEW & REPLACEMENT PART LIST

Level	Location No.	Description	Part Number	Spec	Remark
6	D401,VA201,VA202,VA207,VA208,VA401,VA402,VA404,VA405,VA406,VA407,VA408,VA409,VA410,VA411,VA412,VA413,VA414,VA415,VA416,VA417,VA418,VA419	Varistor	SEVY0004301	ICVL0518100Y500FR 18V 0% 10F 1.0*0.5*0.55 NONE SMD R/TPINNOCHIPS TECHNOLOGY	
6	VA205,VA206,VA209,VA210	Varistor	SEVY0005202	EVLC5S02100 5.5V 0% 100F 1.0*0.5*0.6 UL SMD R/TPAMOTECH CO., LTD.	
6	FB202	Filter,Bead	SFBH0000903	HB-1M1005-601JT 600 ohm 1.0*0.5*0.5 SMD R/TP 2PCERATECH CORPORATION	
6	FB203	Filter,Bead	SFBH0000912	HB-1M1005-102JT 1000 ohm 1.0*0.5*0.5 SMD R/TP 2PCERATECH CORPORATION	
6	FB101	Filter,Bead	SFBH0007103	BLM15BB750SN1J 75ohm 1.0x0.5x0.55 SMD R/TP 2PMURATA MANUFACTURING CO.,LTD.	
6	FB204,FB205,FB206,FB208,R238	Filter,Bead	SFBH0008105	BLM15BD182SN1D 1800ohm ;1.0x0.5x0.55 SMD R/TP 2PMURATA MANUFACTURING CO.,LTD.	
6	FL201	Filter,EMI/Power	SFEY0007101	ICVFP10181E301FR ESD/EMI 0HZ 300pF 0H SMD R/TPINNOCHIPS TECHNOLOGY	
6	FL403,FL404,FL405	Filter,EMI/Power	SFEY0012501	ICVE10054E250R201FR ESD/EMI 0HZ 25pF 0H SMD R/TPINNOCHIPS TECHNOLOGY	
6	FL401,FL402	Filter,EMI/Power	SFEY0015501	ICVE10184E050R101FR ESD/EMI 550HZ 10F 0H SMD R/TPINNOCHIPS TECHNOLOGY	
6	FL301	Filter,Saw,Dual	SFSB0001803	SAWEN881MBK0F00 881.5MHz,942.5MHz 1.8*1.4*0.5 SMD R/TP 10PMURATA MANUFACTURING CO.,LTD.	
6	FL302	Filter,Saw,Dual	SFSB0001903	SAWEN1G84BK0F00 1842.5MHz,1960MHz 1.8*1.4*0.5 SMD R/TP 10PMURATA MANUFACTURING CO.,LTD.	
6	U301	RF Module	SMRH0006301	RF7161 MHz,MHz,GPRS QUAD TX MODULE,SP6T,6.63*5.24*1.02,22pin, RF MICRO DEVICES INC	
6	BAT101	Capacitor Assembly	SMZY0023501	PAS311HR-VG1 3.8 Backup Capacitor 0.03F,Module Assembly, TAIYO YUDEN CO.,LTD	
6	U304	Module,WLAN	SMZY0028601	SWB-B28 2.3VTO5.5V LGA 62P 9.0x7.8x1.2MMSAMSUNG ELECTRO-MECHANICS CO., LTD.	
6	ANT304	Antenna,Helical	SNMF0059501	AMAN301512ST01 SINGLE -2DB 50OHM 3AMOTECH CO., LTD.	
5	SAFD00	PCB Assembly,Main,SMT Top	SAFD0150901 6	LG-C305 IDNWA MAIN,G	

13. EXPLODED VIEW & REPLACEMENT PART LIST

Level	Location No.	Description	Part Number	Spec	Remark
6	LD401,LD402,LD403,LD404,LD405,LD406,LD407,LD408,LD409,LD410,LD411,LD412,LD413,LD414	LED,Chip	EDLH0011901	SSC-TWH104-HL WHITE 2.7~3.1 20mA 100~220mcd X(0.24~0.34) Y(0.25~0.34) 66mW 1608 R/TP 2P -SEOUL SEMICONDUCTOR CO.,LTD	
6	D201	Diode,TVS	EDTY0008606	PRSB6.8C 4.7V 5.7 - - 10W - R/TP 2P 1PROTEK DEVICES INC.	
6	R430,R431,R432,R434	Resistor,Chip	ERHZ0000355	MCR01MZF5F2700 270 ohm,1/16W,F,1005,R/TP ROHM CO.,LTD.	
6	R235	Wire Pad,Short	SAFP0000501	LG-VS760 VRZ	
6	SPFY00	PCB,Main	SPFY0235401	SPFY0235401 FR-4 Build-Up BUILD-UP 6 1 EXTRA,MAIN,F,FR-4,1.0 mm,BUILD-UP 6UNITECH PRINTED CIRCUIT BOARD CORP.	
6	MIC201	Microphone,Condenser	SUMY0010609	SPU0410HR5H -PB SPU0410HR5H -PB,UNIT,42 dB,3.76*2.95*1.1,mems smd mic KNOWLES ACOUSTICS	

13. EXPLODED VIEW & REPLACEMENT PART LIST

13.3 Accessory

Note: This Chapter is used for reference, Part order is ordered by SBOM standard on GCSC

Level	Location No.	Description	Part Number	Spec	Remark
2	SBPL00	Mobile Phone Battery Li-Ion	SBPL0098201	LGIP-430N-WW-TO LGIP-430N-WW-SANYO,3.7 V,900 mAh,1 CELL,PRISMATIC ,463450,INNERPACK,WW TOCAD DONGHWA	
2	SBPL00	Mobile Phone Battery Li-Ion	*S*SBPL0098901	LGIP-430N-WW-LGC LGIP-430N-WW-LGC,3.7 V,900 mAh,1 CELL,PRISMATIC ,463450,innerpack, WW LG CHEM LTD.	
2	SSAD00	Adapters	SSAD0034501	STA-U35ER 90Vac~264Vac 4.8V 400mA 5060 CE NONE NONE - SUNLIN ELECTRONICS CO.,LTD	
2	SSAD00	Adapters	*S*SSAD0034502	90Vac~264Vac 4.8V 400mA 5060 CE NONE NONE -	
2	SSAD00	Adapters	*S*SSAD0034504	STA-U35ES 90Vac~264Vac 4.8V 400mA 5060 CE NONE NONE - SALCOMP OY	
2	SSAD00	Adapters	*S*SSAD0034503	STA-U35ED 90Vac~264Vac 4.8V 400mA 5060 CE NONE NONE - DONG DO ELECTRONICS CO., LTD	