



Service Manual

C570



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1. INTRODUCTION

1.1 Purpose

This manual provides the information necessary to repair, calibration, description and download the features of this model.

1.2 Regulatory Information

A. Security

Toll fraud, the unauthorized use of telecommunications system by an unauthorized part (for example, persons other than your company's employees, agents, subcontractors, or person working on your company's behalf) can result in substantial additional charges for your telecommunications services. System users are responsible for the security of own system. There are may be risks of toll fraud associated with your telecommunications system. System users are responsible for programming and configuring the equipment to prevent unauthorized use. The manufacturer does not warrant that this product is immune from the above case but will prevent unauthorized use of common-carrier telecommunication service of facilities accessed through or connected to it.

The manufacturer will not be responsible for any charges that result from such unauthorized use.

B. Incidence of Harm

If a telephone company determines that the equipment provided to customer is faulty and possibly causing harm or interruption in service to the telephone network, it should disconnect telephone service until repair can be done. A telephone company may temporarily disconnect service as long as repair is not done.

C. Changes in Service

A local telephone company may make changes in its communications facilities or procedure. If these changes could reasonably be expected to affect the use of the this phone or compatibility with the network, the telephone company is required to give advanced written notice to the user, allowing the user to take appropriate steps to maintain telephone service.

D. Maintenance Limitations

Maintenance limitations on this model must be performed only by the manufacturer or its authorized agent. The user may not make any changes and/or repairs except as specifically noted in this manual. Therefore, note that unauthorized alternations or repair may affect the regulatory status of the system and may void any remaining warranty.

1. INTRODUCTION

E. Notice of Radiated Emissions

This model complies with rules regarding radiation and radio frequency emission as defined by local regulatory agencies. In accordance with these agencies, you may be required to provide information such as the following to the end user.

F. Pictures

The pictures in this manual are for illustrative purposes only; your actual hardware may look slightly different.

G. Interference and Attenuation

Phone may interfere with sensitive laboratory equipment, medical equipment, etc. Interference from unsuppressed engines or electric motors may cause problems.

H. Electrostatic Sensitive Devices

ATTENTION

Boards, which contain Electrostatic Sensitive Device (ESD), are indicated by the sign. Following information is ESD handling:



- Service personnel should ground themselves by using a wrist strap when exchange system boards.
- When repairs are made to a system board, they should spread the floor with anti-static mat which is also grounded.
- Use a suitable, grounded soldering iron.
- Keep sensitive parts in these protective packages until these are used.
- When returning system boards or parts like EEPROM to the factory, use the protective package as described.

2. PERFORMANCE

2.1 H/W Features

Item	Feature	Comment
Standard Battery	Li-ion, 1500mAh Battery Size : 65.3 (W) × 44(H) × 5.2(T) [mm] Battery Weight : 31g	
Standby Current	WCDMA w/o BT: Under 3 mA (DRX=1.28) GSM w/o BT: Under 3mA (Paging= 5 period)	
Talk time	WCDMA: Over 300 min (TX = 12dBm low) GSM: Over 270min (TX= Lvl 5)	
Stand by time	WCDMA: Over 450 hours (DRX = 1.28) GSM: Over 450hours (Paging = 5 Period)	
Charging time	Under 240 min	
RX Sensitivity	WCDMA: -106.7dBm/3.84MHz GSM: -105dBm(2.439%)	
TX maximum output power	WCDMA:+24dBm+1/-3 db (Power class3)/ 3.84MHz GSM: +33dBm ± 3dB, DCS/PCS: +30dBm ± 3dB	
GPRS compatibility	Class 12	
SIM card type	3V & 1.8V	
Display	2.4" 320 x 240 TFT LCD	
Key	Full Qwerty keypad	
ANT	Internal	
EAR Phone Jack	Yes (stereo)	
PC Synchronization	Yes	
Speech coding	EFR/FR/HR	
Data and Fax		
Vibrator	Yes	
Loud Speaker	Yes	
Voice Recoding	Yes	
Microphone	Yes	

2. PERFORMANCE

Item	Feature	Comment
Speaker/Receiver	Single speaker with Speaker/Receiver two mode	
Travel Adapter	Yes	
MIDI	64 poly	
MP3/AAC	Yes	
Options	Data Cable	

2. PERFORMANCE

2.2 Technical Specification

Item	Description	Specification			
1	Frequency Band	GSM850: 824~849MHz/869~894MHz GSM900: 880~915MHz/925~960MHz DCS: 1710~1785MHz/1805~1880MHz PCS: 1850~1910MHz/1930~1990MHz WCDMA850:824 MHz ~ 849 MHz/869~894MHz WCDMA900 :880 MHz ~ 915 MHz/925~960MHz WCDMA1900:1850 ~1910 MHz/1930~1990MHz WCDMA2100:1920 MHz~1980 MHz/2110~2170MHz			
2	Phase Error	GSM: RMS : 5°, Peak : 20 °			
3	Frequency Error	GSM : 0.1 ppm WCDMA: $\pm(0.1 \text{ p p m} + 10\text{Hz})$			
4	Power Level	GSM850			
		Power level	Power	Low Limit	Up Limit
		5	32	31	33
		6	31	30	32
		7	29	28	30
		8	27	25	29
		9	25	23	27
		10	23	21	25
		11	21	19	23
		12	19	17	21
		13	17	15	19
		14	15	13	17
		15	13	11	15
		16	11	8	14
		17	9	6	12
		18	7	4	10
		19	5	2	8

2. PERFORMANCE

Item	Description	Specification			
4	Power Level	DCS1800/PCS 1900			
		Power level	Power	Low Limit	Up Limit
		0	29	28	30
		1	28	27	29
		2	26	25	27
		3	24	22	26
		4	22	20	24
		5	20	18	22
		6	18	16	20
		7	16	14	18
		8	14	12	16
		9	12	9	15
		10	10	7	13
		11	8	5	11
		12	6	3	9
		13	4	1	7
		14	2	-1	5
		15	0	-3	3
		WCDMA850			
		Power level	Power	Low Limit	Up Limit
		Max	22.5	21	25
		WCDMA900			
		Power level	Power	Low Limit	Up Limit
		Max	22.2	21	25
		WCDMA1900			
		Power level	Power	Low Limit	Up Limit
		Max	22.2	21	25
		WCDMA2100			
		Power level	Power	Low Limit	Up Limit
		Max	22.2	21	25

2. PERFORMANCE

Item	Description	Specification	
5	Output RF Spectrum (due to modulation)	GSM850 & 900	
		Offset from Carrier (kHz).	Max. dBc
		100	+0.5
		200	-30
		250	-33
		400	-60
		600~ <1,200	-60
		1,200~ <1,800	-60
		1,800~ <3,000	-63
		3,000~ <6,000	-65
		6,000	-71
		DCS & PCS	
		Offset from Carrier (kHz).	Max. dBc
		100	+0.5
		200	-30
		250	-33
		400	-60
		600~ <1,200	-60
		1,200~ <1,800	-60
		1,800~ <3,000	-65
		3,000~ <6,000	-65
		6,000	-73
6	Output RF Spectrum (due to switching transient)	GSM 900/GSM 850	
		Offset from Carrier (kHz).	Max. dBm
		400	-19
		600	-21
		1,200	-21
		1,800	-24

2. PERFORMANCE

Item	Description	Specification		
6	Output RF Spectrum (due to switching transient)	DCS & PCS		
		Offset from Carrier (kHz).		Max. dBm
		400		-22
		600		-24
		1,200		-24
		1,800		-27
7	Spurious Emissions	Conduction, Emission Status		
8	Bit Error Ratio	GSM850 & 900 BER (Class II) < 2.439% @-102 dBm DCS & PCS BER (Class II) < 2.439% @-102 dBm WCDMA BER < 0.1% @-106.7 dBm < R E F l o r >		
9	RX Level Report Accuracy	±3 dB		
10	SLR	14±3 dB		
11	Sending Response	Frequency (Hz)	Max.(dB)	Min.(dB)
		100	-12	-
		200	0	-
		300	0	-12
		1,000	0	-6
		2,000	4	-6
		3,000	4	-6
		3,400	4	-9
		4,000	0	-
12	RLR	3±3 dB		

2. PERFORMANCE

Item	Description	Specification		
13	Receiving Response	Frequency (Hz)	Max.(dB)	Min.(dB)
		100	-12	-
		200	0	-
		300	2	-7
		500	*	-5
		1,000	0	-5
		3,000	2	-5
		3,400	2	-10
		4,000	2	
		* Mean that Adopt a straight line in between 300 Hz and 1,000 Hz to be Max. level in the range.		
14	STM R	>17 dB		
15	System frequency (13MHz tolerance)	≤ 2.5 ppm		
16	32.768KHz tolerance	≤ 30 ppm		
17	Ringer Volume	At least 58 dB under below conditions: 1. Ringer set as ringer. 2. Test distance set as 100 cm		

2. PERFORMANCE

Item	Description	Specification		
21	Charge Current	normal Charge : 600 mA pre Charge : 80 mA		
22	Antenna Display	BAR	WCDMA	GSM
		BAR 4 --> 3	-82 ± 3dBm	-91 ± 2dBm
		BAR 3 --> 2	-92 ± 3dBm	-96 ± 2dBm
		BAR 2 --> 1	-102 ± 3dBm	-101 ± 2dBm
		BAR 1 --> 0	-112 ± 3dBm	-106 ± 2dBm
23	Battery Indicator	Battery Bar		Specification
		BAR 4 --> 3		100%
		BAR 3 --> 2		50%
		BAR 2 --> 1		20%
		BAR 1 --> 0		8%
		Low Battery Alarm		20%
		Critical Low Battery Alarm		8%
		POWER OFF		0%
24	Low Voltage Warning	Battery Capacity < 8%		
25	Forced shut down Voltage	3.5 ± 0.03V		
26	Battery Type	1 Li-ion Battery Standard Voltage = 3.7 V Battery full charge voltage = 4.2 V Capacity: 830mAh		
27	Travel Charger	Switching-mode charger Input: 100 ~ 240 V, 50/60 Hz Output: 5.1 V, 700 mA		

3. TECHNICAL BRIEF

3.1 Transceiver (RTR 6285, FU1)

The RF parts consist of a transmitter part, a receiver part, a frequency synthesizer part, a voltage supply part, and a VCTCXO part.

The RTR6285 transceiver is the integrated GSM/UMTS multi-band and multi-mode digital cellular handsets and wireless data modems. The integrated solution also includes the GPS demodulator and the low noise amplifier (LNAs) for UMTS and GSM RX path. The GPS LNA, RF voltage controlled oscillator (VCO) modules, and other discrete components found in conventional designs.

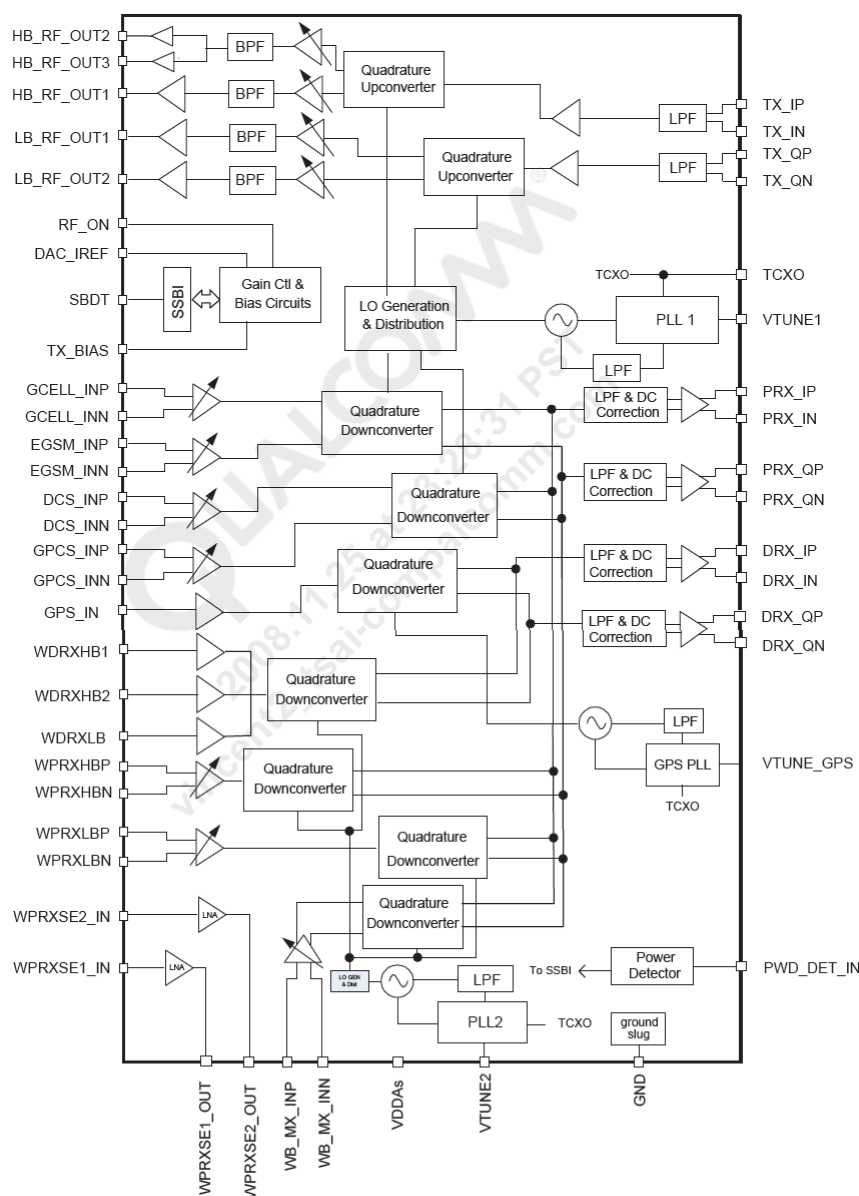


Figure 3-1 RTR6285 block diagram

3. TECHNICAL BRIEF

(1) Receiver Part

The RTR6285/RTR6280 receive paths include four GSM/EDGE Rx signal paths that support GSM 850, GSM 900, GSM 1800, and GSM 1900 bands and four WCDMA Rx signal paths (two single-ended and two differential) for one UMTS low band and three UMTS high bands.

A. RF front end – Antenna Switch Module(ASM, FS1)

The quad-band GSM/EDGE Rx paths start from the handset front-end circuits (GSM Rx filters and antenna switch module) FS1. The ASM (FS1) is used to control the Rx and Tx paths. And, the input signals VC1, VC2, VC3 and VC4 of a FS1 are directly connected to baseband controller to switch either Tx or Rx path on. The control logic is given below Table 3-1.

CONTROL LOGIC

Mode	Vc1	Vc2	Vc3	Vc4	Vdd
GSM850/900 Tx	1.8-3.0V	1.8-3.0V	0-0.2V	0-0.2V	2.5-3.0V
GSM1800/GSM1900 Tx	1.8-3.0V	0-0.2V	0-0.2V	0-0.2V	2.5-3.0V
GSM850 Rx	0-0.2V	1.8-3.0V	1.8-3.0V	0-0.2V	2.5-3.0V
GSM900 Rx	0-0.2V	1.8-3.0V	0-0.2V	0-0.2V	2.5-3.0V
GSM1800 Rx	0-0.2V	0-0.2V	1.8-3.0V	0-0.2V	2.5-3.0V
GSM1900 Rx	0-0.2V	0-0.2V	0-0.2V	0-0.2V	2.5-3.0V
UMTS1	1.8-3.0V	0-0.2V	1.8-3.0V	0-0.2V	2.5-3.0V
UMTS2	1.8-3.0V	0-0.2V	1.8-3.0V	1.8-3.0V	2.5-3.0V
UMTS3	1.8-3.0V	1.8-3.0V	1.8-3.0V	0-0.2V	2.5-3.0V
All-Off (no current)	0-0.2V	0-0.2V	0-0.2V	0-0.2V	0-0.2V

Table 3-1 THE ASM control logic

The four differential inputs are amplified with gain-stepped LNA circuits. Gain control is provided through software and serial interface. The LNA outputs drive the RF ports of quadrature RF-to-baseband downconverters. The downconverted baseband outputs are multiplexed and routed to lowpass filters (one I and one Q) whose passband and stopband characteristics supplement MSM device processing. These filter circuits allow DC offset corrections, and their differential outputs are buffered to interface with the MSM IC. Figure 3-2 is GSM RX path from ASM to RTR6285.

3. TECHNICAL BRIEF

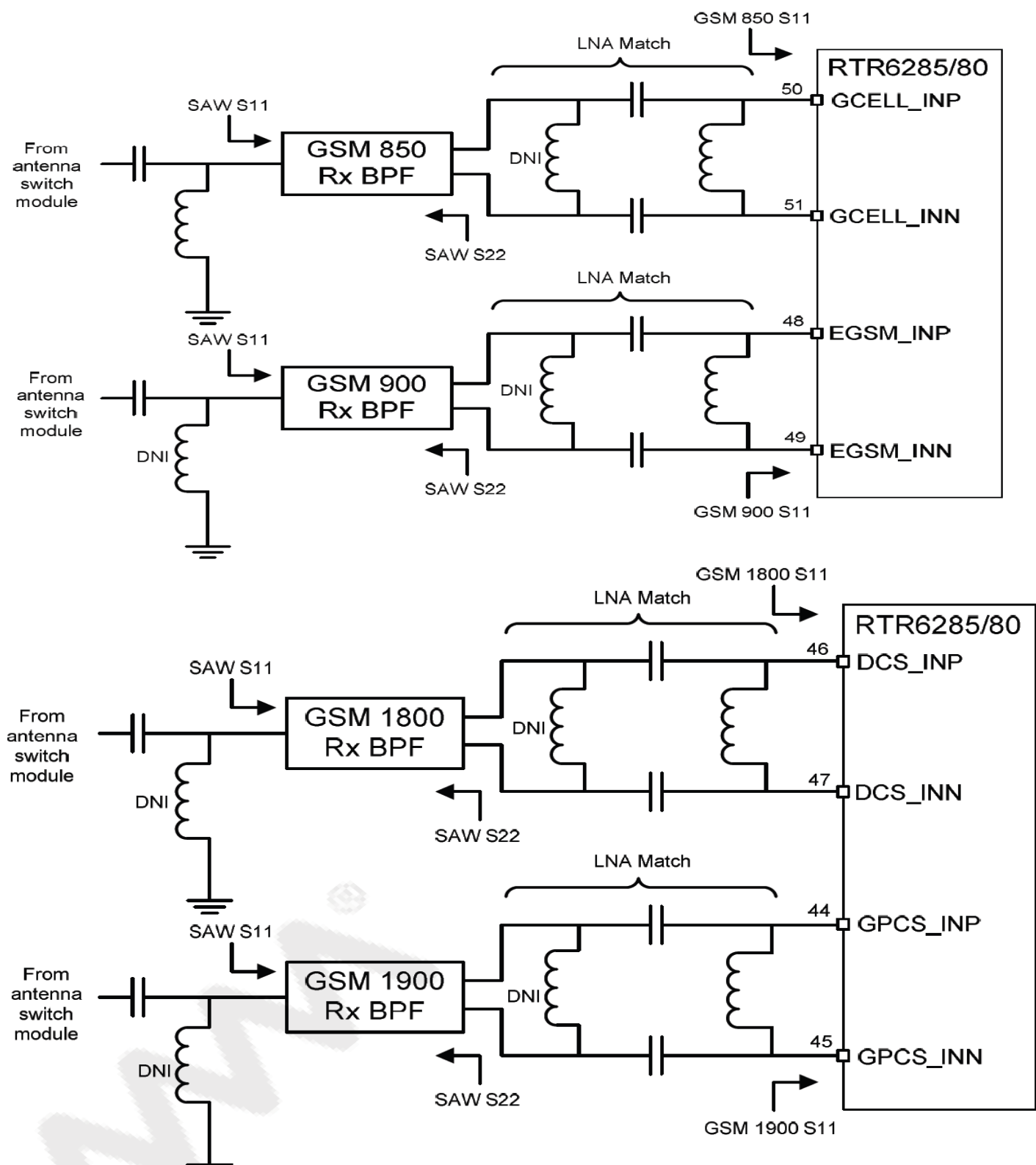


Figure 3-2 THE GSM RX path

3. TECHNICAL BRIEF

The two RTR6285/RTR6280 UMTS single-ended inputs accept UMTS 2100/1900/1800/1700 input signals from the handset RF front-end filters. The UMTS Rx inputs are provided with on-chip LNAs that amplify the signal before second-stage filters that provide differential signals to a shared downconverter. This second-stage input is configured differentially to optimize second-order intermodulation and common mode rejection performance. The gain of the UMTS front-end amplifier and the UMTS second-stage differential amplifier is adjustable, under MSM system chip control, to extend the dynamic range of the receivers. Figure 3-3 is UMTS RX path from ASM to RTR6285.

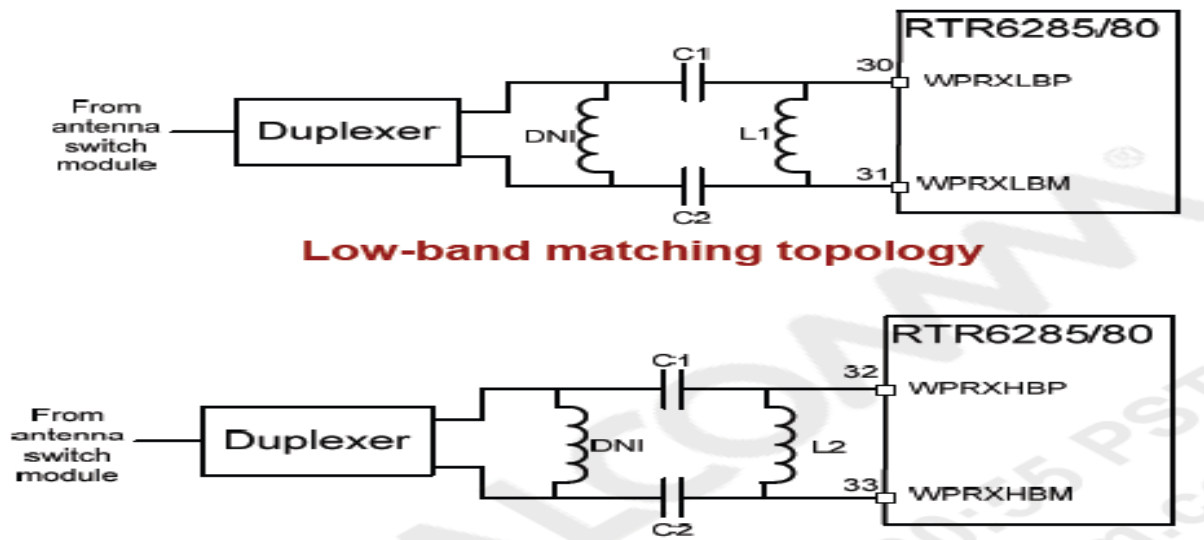


Figure 3-3 THE UMTS RX path

B. GPS

The GPS input path is followed by a dedicated downconverter. The GPS downconverter and secondary WCDMA downconverter outputs are multiplexed to drive a single set of baseband filter and buffer circuits. The secondary baseband output (in-phase and quadrature differential signals) is routed through the DRX_I/Q pins to the MSM device for further processing. This baseband interface supports either the WCDMA or GPS mode, whichever is active on the secondary path.

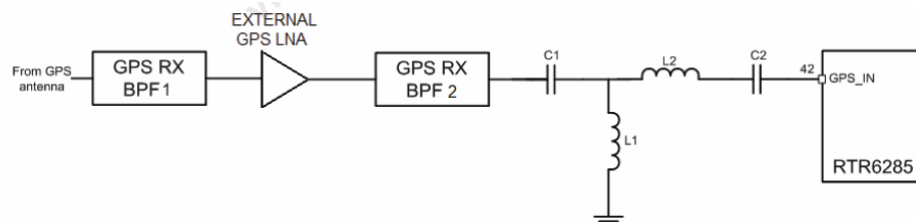


Figure 3-4 THE GPS RX path

3. TECHNICAL BRIEF

(2) Transmitter Part

The transmit path begins with differential baseband signals (I and Q) from the MSM device. These analog input signals are buffered, filtered by low-pass filter, corrected for DC offsets, amplified, and then applied to the quadrature upconverter mixers.

The upconverter outputs are amplified by multiple variable gain stages that provide transmit AGC control. SSBI is used to do the gain control. The specified driver amplifier output level is achieved while supporting the GSM/EDGE and UMTS transmit standard's requirements for GSM ORFS, carrier and image suppression, WCDMA ACLR, spurious emissions, Rx-band noise, etc. These upconverters translate the polar GMSK-modulated or 8-PSK modulated baseband PM signals and/or WCDMA baseband signals directly to the RF signals, which are filtered and feed into the GSM/EDGE polar PA and/or WCDMA PA.

The WCDMA Tx power is coupled back to the RTR6285/RTR6280 internal power detector input pin, PDET_IN, using a coupler for power measurement.

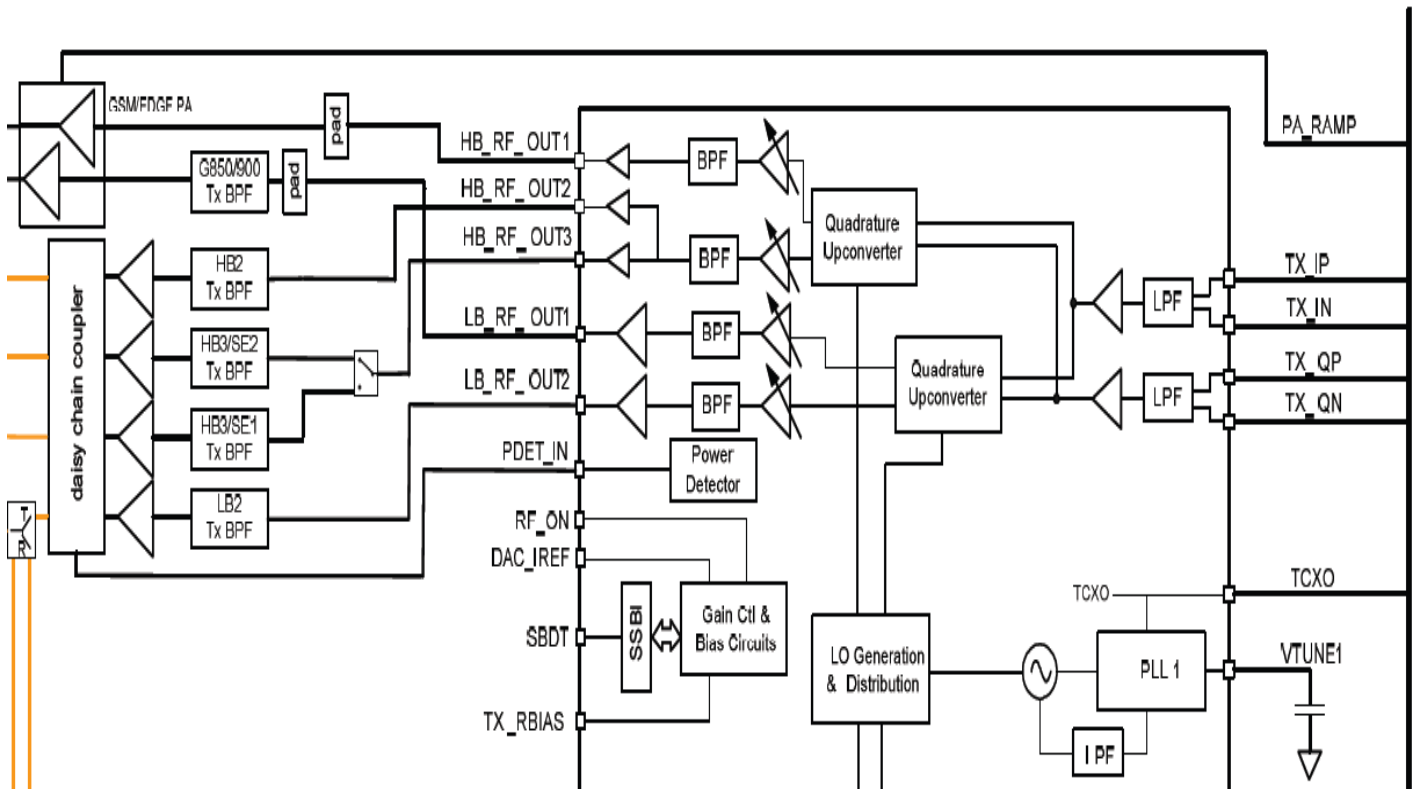


Figure. 3-5 RTR6285 TRANSMITTER PART

(3) PLLs

Three fully functional fractional-N synthesizers, including VCOs and loop filters, are integrated within the RTR6285 IC, while the RTR6280 IC has two fractional-N synthesizers. The first synthesizer (PLL1) creates the transceiver LOs that support the UMTS transmitter, and all four GSM band receivers and transmitters including: GSM 850, GSM 900, GSM 1800, and GSM 1900.

The second synthesizer (PLL2) provides the LO for the UMTS primary and secondary receivers (RTR6285 only). The third synthesizer (PLL3) provides the LO for the GPS receiver



The RTR6285 IC provides the I/Q path to connect MSM system chip for UMTS/GSM TX and RX signals.

The RF IQ signals are demodulated in MSM system chip to data stream then processed by baseband system.

Most control and status commands are communicated through the RTR6285 MSM device-compatible SSBI, enabling efficient initialization, WCDMA transmit gain control, control of device operating modes and parameters, verification of programmed parameters, and frequency lock status reports. The MSM device SSBI controller is the master while the RTR6285 IC is a slave.

The RTR6285 IC also provides a digital I/O pin for time-critical control signal.



Figure. 3-7 RTR6285 Baseband Interface

3. TECHNICAL BRIEF

3.2 Power Amplifier Module

(1) GSM PA (TQM7M5012H, FAR4)

The TQM7M5012H is a ultra-small (5x5mm), GSM/EDGE Polar PAM for handset applications. This module has been optimized for excellent EDGE efficiency, Rx band noise performance, ACPR and EVM in an open loop polar modulation environment at EDGE class E2+ operation while maintaining high GSM/GPRS efficiency.

High reliability is assured by utilizing TriQuint's 3rd generation InGaP HBT technology and by TriQuint's proven module design techniques.

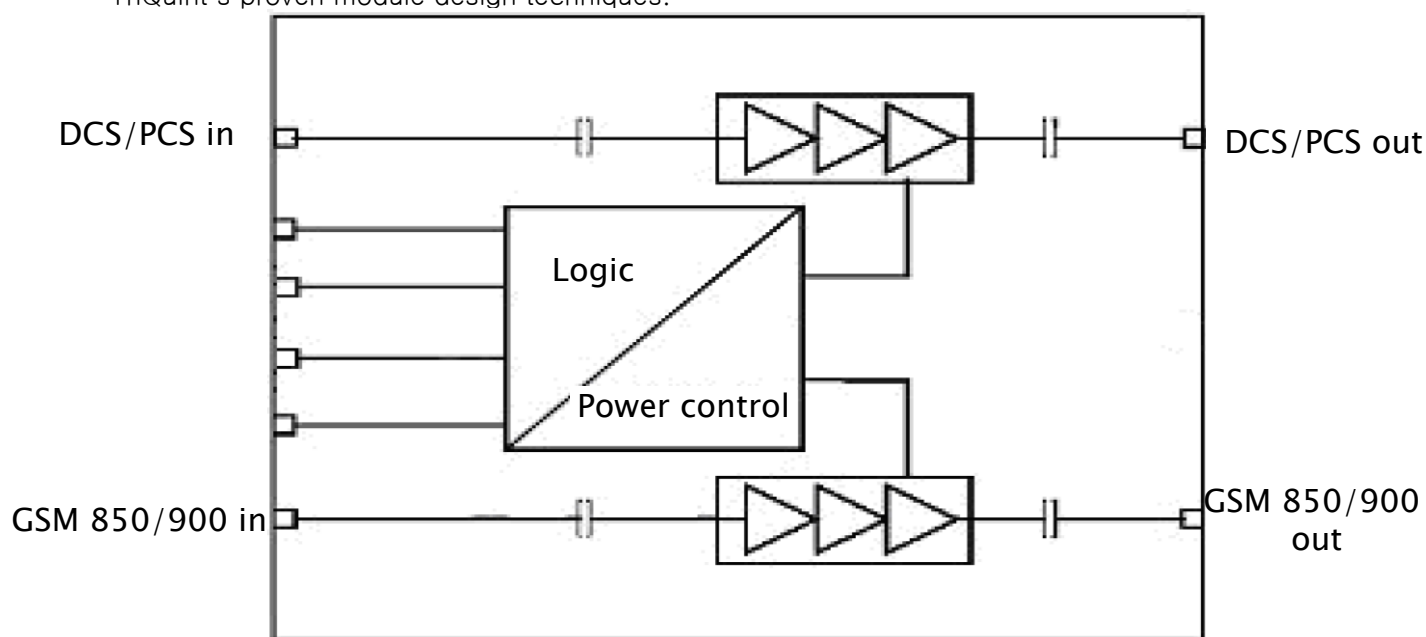


Figure 3-8 GSM PA Functional Block Diagram

(2) UMTS PA (FAR3 / SKY17787, FAR2 / SKY77188, FAR1)

A. Band I -- SKY77186, FAR3

The SKY77186 Power Amplifier Module (PAM) is a fully matched 10-pad surface mount module developed for Wideband Code Division Multiple Access (WCDMA) applications. This small and efficient module packs full 1920–1980 MHz bandwidth coverage into a single compact package. Because of high efficiencies attained throughout the entire power range, the SKY77186 delivers unsurpassed talk-time advantages. The SKY77186 meets the stringent spectral linearity requirements of High Speed Downlink Packet Access (HSDPA) data transmission with high power added efficiency. A directional coupler is integrated into the module thus eliminating the need for any external coupler.

3. TECHNICAL BRIEF

B. Band II -- SKY77187, FAR2

The SKY77187 Power Amplifier Module (PAM) is a fully matched 10-pad surface mount module developed for Wideband Code Division Multiple Access (WCDMA) applications. This small and efficient module packs full 1850–1910 MHz bandwidth coverage into a single compact package. Because of high efficiencies attained throughout the entire power range, the SKY77187 delivers unsurpassed talk-time advantages. The SKY77187 meets the stringent spectral linearity requirements of High Speed Downlink Packet Access (HSDPA) data transmission with high power added efficiency. A directional coupler is integrated into the module thus eliminating the need for any external coupler.

C. Band V -- SKY77188, FAR1

The SKY77188 Power Amplifier Module (PAM) is a fully matched 10-pad surface mount module developed for Wideband Code Division Multiple Access (WCDMA) applications. This small and efficient module packs full 824–849 MHz bandwidth coverage into a single compact package. Because of high efficiencies attained throughout the entire power range, the SKY77188 delivers unsurpassed talk-time advantages. The SKY77188 meets the stringent spectral linearity requirements of High Speed Downlink Packet Access (HSDPA) data transmission with high power added efficiency. A directional coupler is integrated into the module thus eliminating the need for any external coupler.

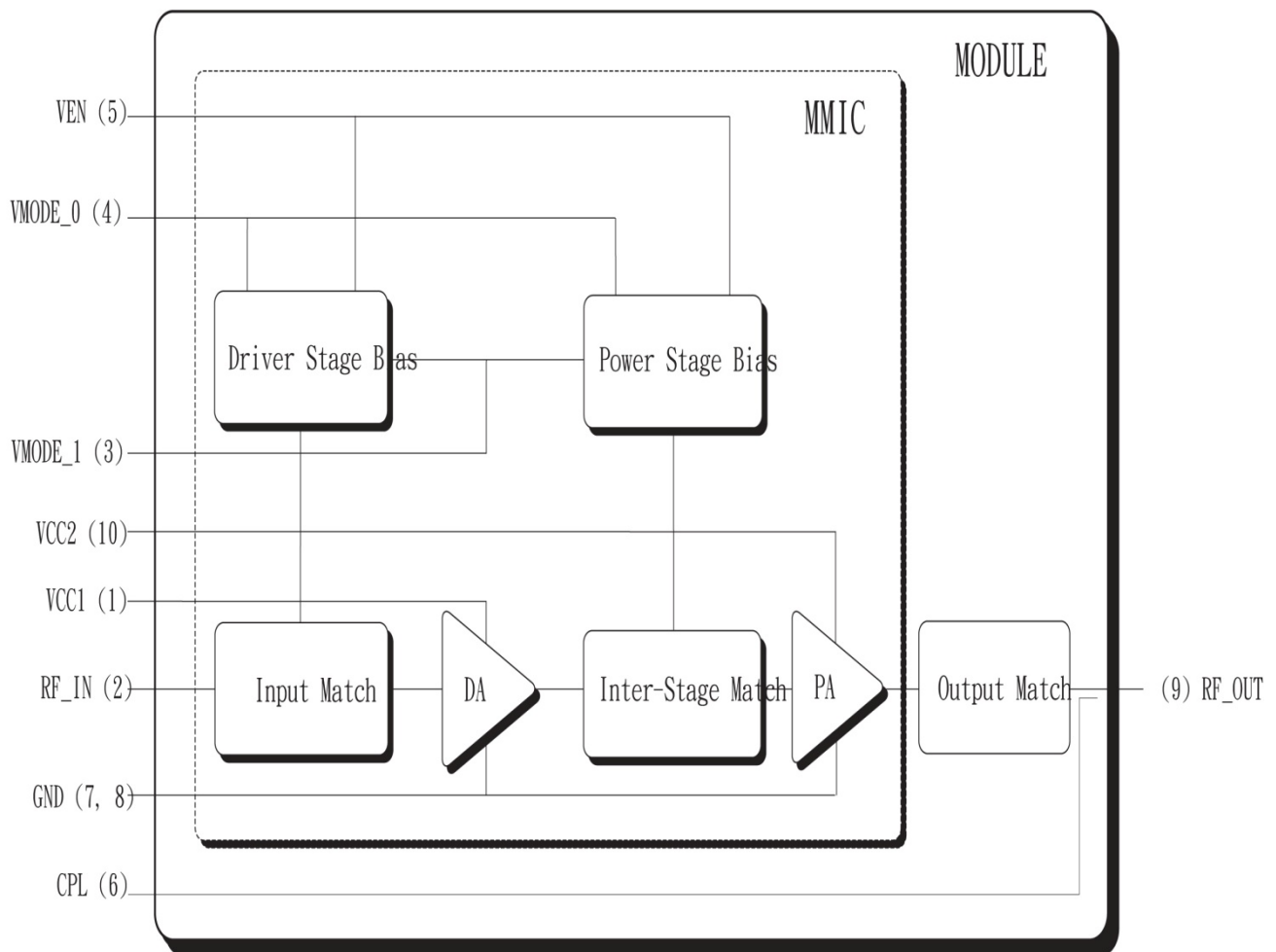


Figure 3–9 UMTS PA Block Diagram

3. TECHNICAL BRIEF

3.3 BT/WiFi/FM (BCM4329, FU1 on Sub board)

The BCM4329 family of single chip devices provides for the highest level of integration for a mobile or handheld wireless system, with integrated IEEE 802.11 a/b/g, Bluetooth 2.1 + Enhanced Data Rate (EDR), and FM radio receiver. It provides a compact ultra-small form-factor solution with minimal external components to drive the costs for mass volumes and allows for flexibility in size, form, and function of handheld devices. BCM4329 is designed to address the needs of highly mobile devices that require minimal power consumption and reliable operation.

The BCM4329's integrated CMOS WLAN 2.4 GHz and 5 GHz power amplifier provide sufficient output power to meet the needs of most WLAN devices. Furthermore, the BCM4329's integrated buck-boost regulator allows its internal power amplifiers to operate at optimal performance, even at low Vbat supply voltages.

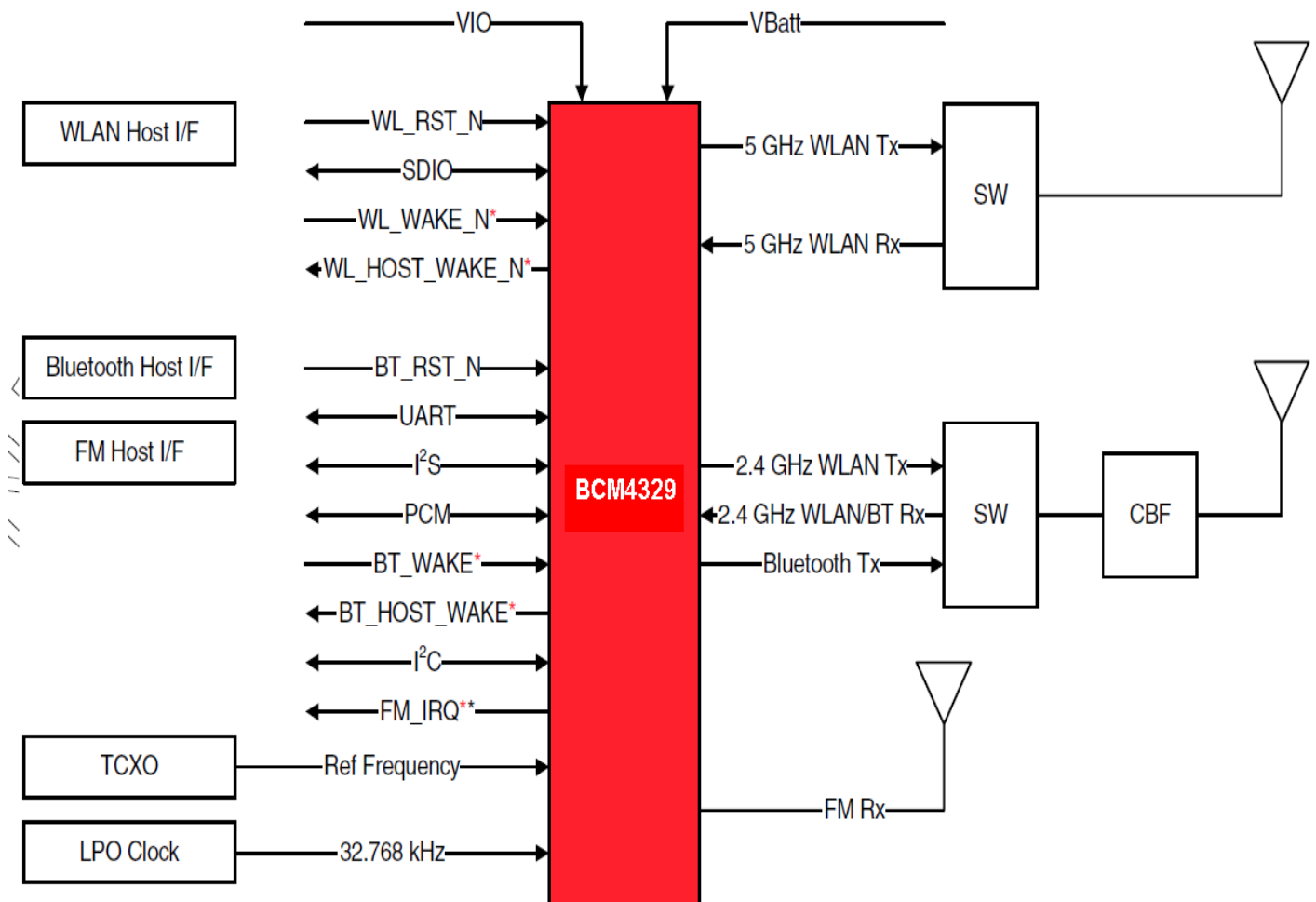


Figure 3-10 BCM4329 System Diagram

3.4 PMIC (PM7540, U7)

- Complete power management, housekeeping, and user interface functions for wireless devices.

1. Input power management.

- Valid external supply attachment and removal detection
- Supports unregulated external charger supplies and USB supplies as input power source.
- Supports Lithium-ion main batteries.
- Trickle, constant current, constant voltage, and pulsed charging of the main battery.
- Support coin cell backup battery (including charging)
- Battery voltage detectors with programmable thresholds.
- VDD collapse protection.
- Charger current regulation and real-time monitoring for over current protection.
- Charger transistor protection by power limit control.
- Control drivers for two external pass transistors and one external battery MOSFET.
- Voltages, current and power control loop.
- Automated recovery for sudden momentary power loss.

2. Output voltage regulation

- One boost switch-mode power supply for driving white LED and hosting USB-OTG.
- Four buck, switch-mode power supplies for efficiently generating MSMC1, MSMC2, MSME and PA supply voltages.
- Supports dynamic voltage scaling (DVS) for MSMC1, MSMC2 and PA outputs.
- 18 low dropout regulator circuits with programmable output voltages, implemented using three different current ratings: 300mA(four), 150mA(ten) and 50mA(four).
- One MIC bias regulator circuit.
- All regulators can be individually enable /disable for power savings.
- Low-power mode available on most regulators.
- All regulated outputs are derived from a common bandgap reference.

3. Integrated handset-level housekeeping functions reduces external parts count, size and cost.

- Analog multiplexer selects from five internal and up to 28 external inputs.
- Multiplexer output's offset and gain are adjusted, increasing the effective ADC resolution.
- Adjusted multiplexer output is buffered and routed to an MSM device ADC.
- Dual oscillators: a 32.768 kHz off-chip crystal and on-chip RC assure MSM device sleep clock.
- Crystal oscillator detector and automated switch-over upon lost oscillation.
- Real-time clock tracking time and generating associated alarms.
- ON-chip adjustments minimize crystal oscillator frequency errors.
- Control TCXO warm-up and synchronize, deglitch and buffer the TCXO signal.
- TCXO buffer control for optimal QPH/catnap timing.
- Multistage over temperature protection.

3. TECHNICAL BRIEF

4. Integrated handset-level user interfaces

- Four programmable current sinks recommended as keypad backlight, LCD backlight, camera flash, and general-purpose drivers.
- Vibration motor driver programmable from 1.2 to 3.1 in 100mV increments.
- Two-channel speaker driver with programmable gain, turn-on time, and muting; configurable inputs and outputs capable of stereo or mono operation.
- Video (TV) amplifier allows use as a camcorder or for slide presentations.

5. IC-level interfaces

- Configurable SBI for efficient initialization, status, and control
- Supports MSM interrupt processing with an internal manager.
- Many functions monitored and reported through real-time and interrupt status signals.
- Dedicated circuits for controlled power-on sequencing, including the MSM device's reset signal.
- Several events continuously monitored for triggering power-on/power-off sequences.
- Supports and orchestrates soft resets.
- USB-OTG transceiver for full-speed and low-speed interfacing of the MSM device to computers as a USB peripheral, or connecting the MSM device to other peripherals.
- Two sets of RUIM level translators enable MSM device interfacing with external modules.

6. 22 multipurpose pins that can be configured as digital or analog I/Os, bidirectional I/Os, or current sinks; default functions support the two sets of RUIM level translators, power-on circuit, analog multiplexer inputs, an LED driver, and a selectable reference voltage output.

7. Highly integrated functionality in a small package– 137pin CSP with a several center ground pins for electrical ground, mechanical stability, and thermal relief.

3. TECHNICAL BRIEF

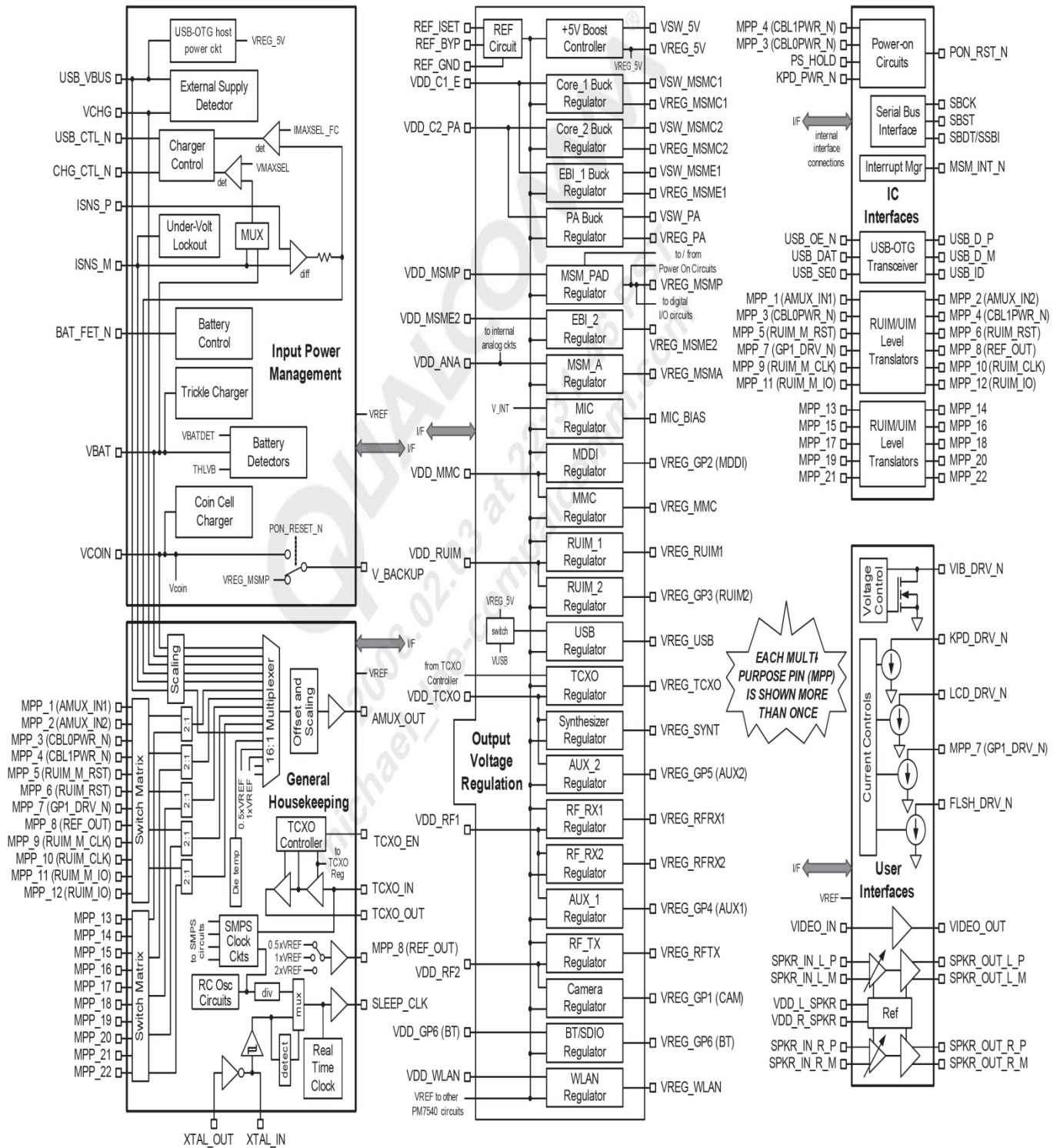


Figure 3-12 PM7540 function block Diagram

3. TECHNICAL BRIEF

3.5.1 Input power management.

VCHG	A valid analog voltage at this pin is recognized by the PM7540 IC to be an external supply, and factors into the IC's power management operating mode.
CHG_CTL_N	Control signal for the external pass transistor - a low voltage turns on the pass transistor.
USB_VBUS	This pin is configured as an analog input or an analog out depending upon the type of peripheral device connected. (Don't use in the C570)
USB_CTL_N	Control signal for the external USB pass transistor - a low voltage turns on the pass transistor. (Don't use in the C570)
ISNS_P	The positive current sensor input - connect to the pass transistor side of the sensor resistor.
ISNS_M	The negative current sensor input - connect to the VDD side of the sensor resistor.
BAT_FET_N	Control signal to the external battery MOSFET; connect directly to its gate.
VBAT	Monitors the battery voltage; connect directly to the battery plus terminal
VCOIN	Connection to the optional coin cell. Provides backup power to the crystal oscillator and real time clock circuits to maintain time and alarm functions if a valid external supply or main battery is not connected.
V_BACKUP	Connect this pin to the SRAM supply pin. (Don't use in the C570)

Table 3–1 Input Power Management Pin Description

3. TECHNICAL BRIEF

A. Input circuit schematic diagram

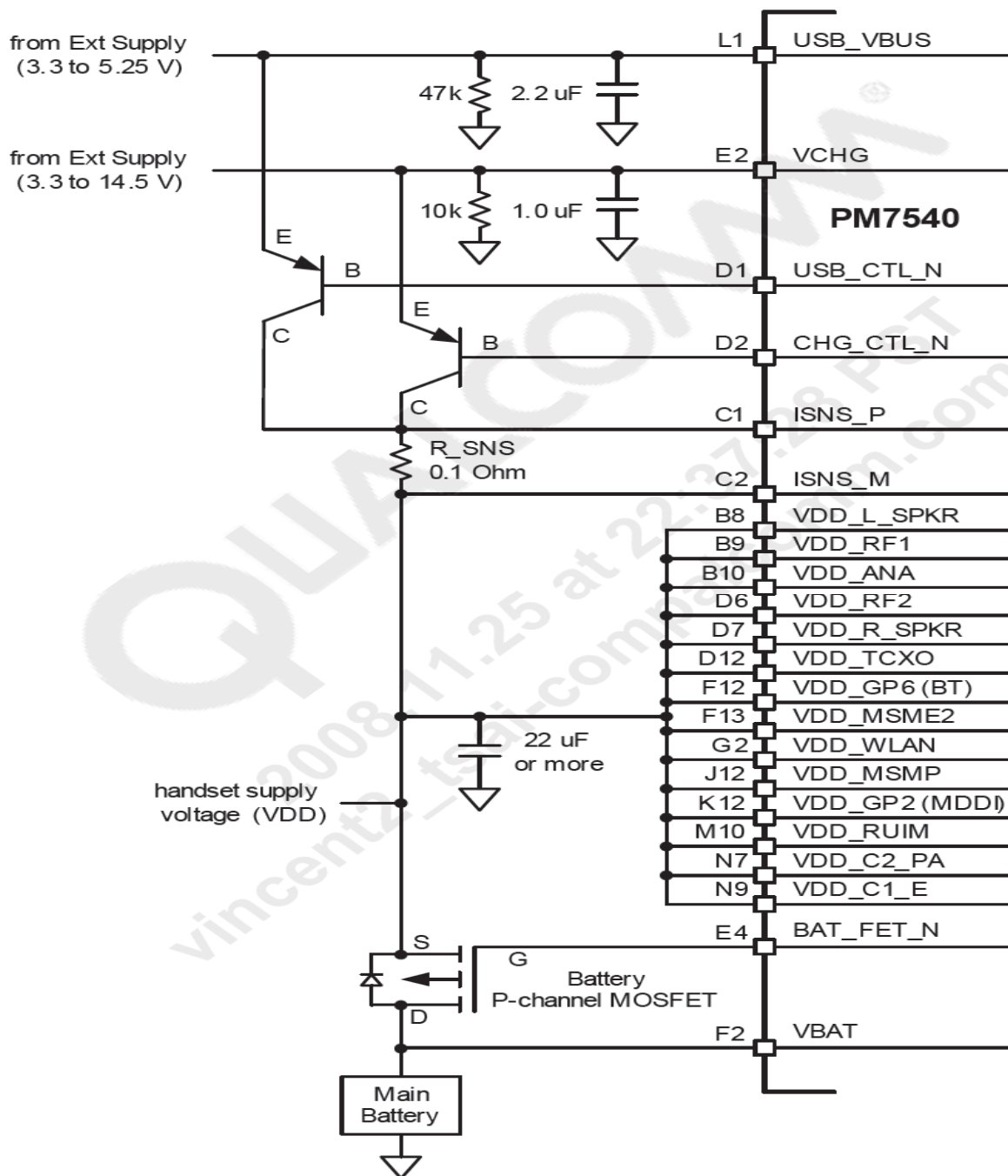


Figure 3-13 Input circuit schematic diagram

3. TECHNICAL BRIEF

B. External supply detection.

The PM7540 continually monitors external supply voltages (VCHG and VUSB) and the handset supply voltage (VDD). Internal detector circuit measure these voltages to recognize when supplies are connected or removed, and verify they are within their valid ranges when connected.

The PMIC detects when the external supply is removed by monitoring the voltage across the external PNP pass transistor. The detection circuit begins to close the pass transistor when the VCHG voltage drops to about 30mV, the detection circuitry cuts the bias to the pass transistor so that the removal can be detected.

C. Transistor drivers

Control drivers for the charger pass transistor and the battery MOSFET are included within the PM7540 device. The driver outputs are applied to the external devices via the PMIC's CHG_CTL_N, USB_CTL_N, and BAT_FET_N pins.

D. Voltage regulator

The PM7540 device provides closed-loop control of the pass transistor (via CHG_CTL_N) to regulate either the handset supply voltage (VDD) when not charging, or the main battery final voltage (VBAT) when charging. When fast charging is disabled, the battery MOSFET is opened and the voltage regulation point is the ISNS_M pin (VDD). When fast charging is enabled, the VBAT pin is the voltage regulation point.

E. Current regulator

An external sensor resistor is required and must be connected across the ISNS_P and ISNS_M pins to allow the PM7540 IC to continuously monitor the total handset electronics plus charger current. If the programmed current threshold is exceeded, the active pass transistor is forced to a high resistor, disrupting VDD or VBAT regulation but protecting against excess current.

The same circuits are used to regulate the total handset electronics plus charging current during the main battery's constant current charging mode. Either pass transistor (charger) can be active while the current is regulated-----only the appropriate control pin (CHG_CTL_N) is active.

3. TECHNICAL BRIEF

F. Main battery charging

The PM7540 device provides support circuitry for charging a lithium-ion battery, cycling through as many as four charging techniques: Trickle, constant current, constant voltage and pulsed.

Charging of a severely depleted battery begins with trickle charging, a mode that limits the current and avoids pulling VDD down. Once a minimum battery voltage is established using trickle charging, constant current charging is enabled via software to charge the battery quickly—this mode is sometimes called fast charging. Once the lithium-ion battery approaches its target voltage, the charge is completed using constant voltage.

G. Backup battery charging

Backup battery charging is enabled through software control and powered from VBAT. The on-chip charger is implemented using a programmable voltage regulator and a programmable series resistor. The MSM device reads the backup battery voltage through the PMIC's analog multiplexer to monitor charging.

3. TECHNICAL BRIEF

H. Trickle charging

Trickle charging of main battery, enable through MSM control and powered from VDD, is provide by PM7540 IC. This mode is used to raise a severely depleted battery's voltage to a level sufficient to begin fast charging.

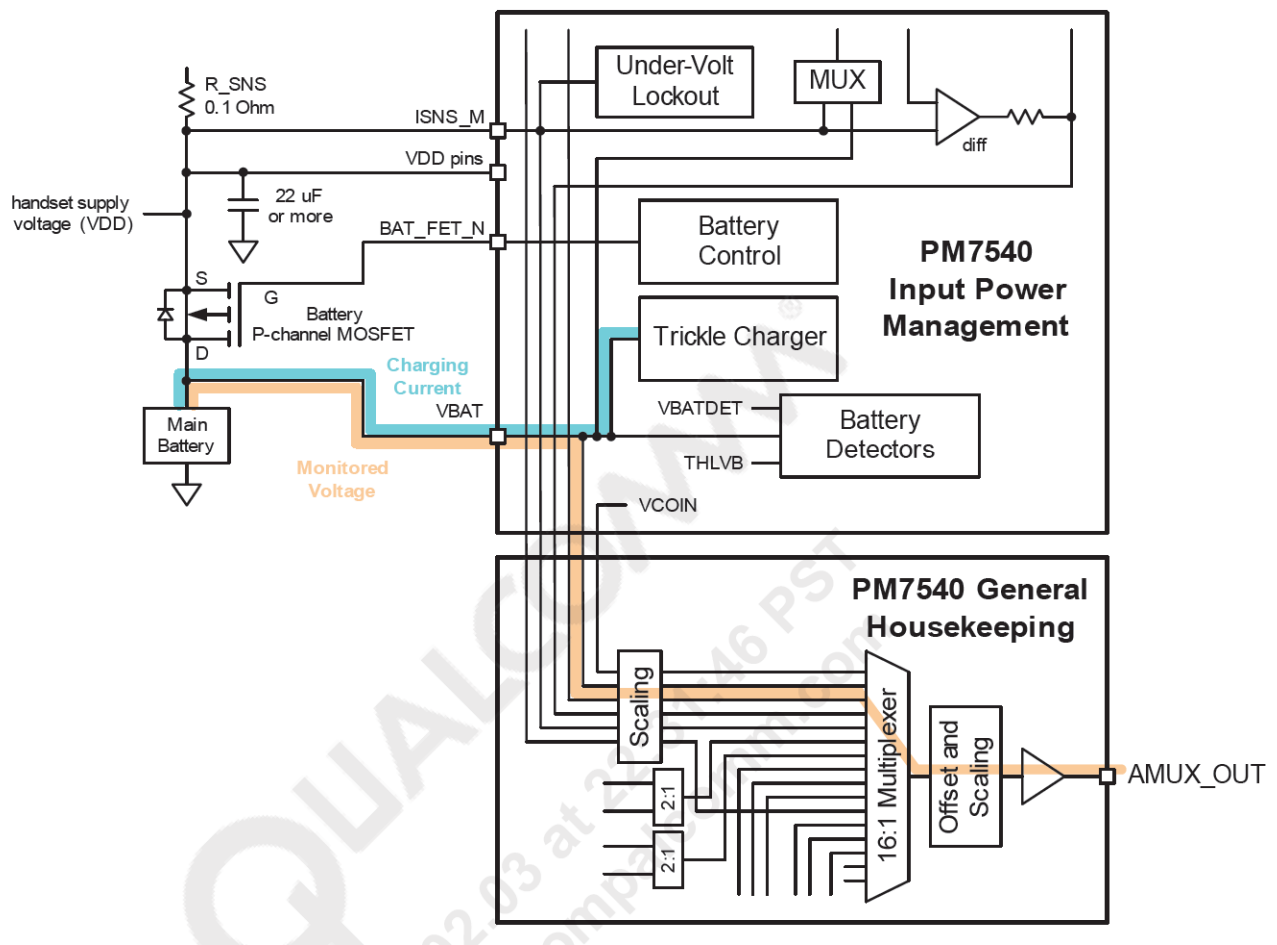


Figure 3-14 Trickle charging

3. TECHNICAL BRIEF

I. Constant current charging

The PM7540 IC supports constant current charging of the main battery by closing the battery MOSFET, and closed-loop controlling the active pass transistor (charger or USB). The closed-loop control regulates the total current to match the programmed value (IMAXSEL)

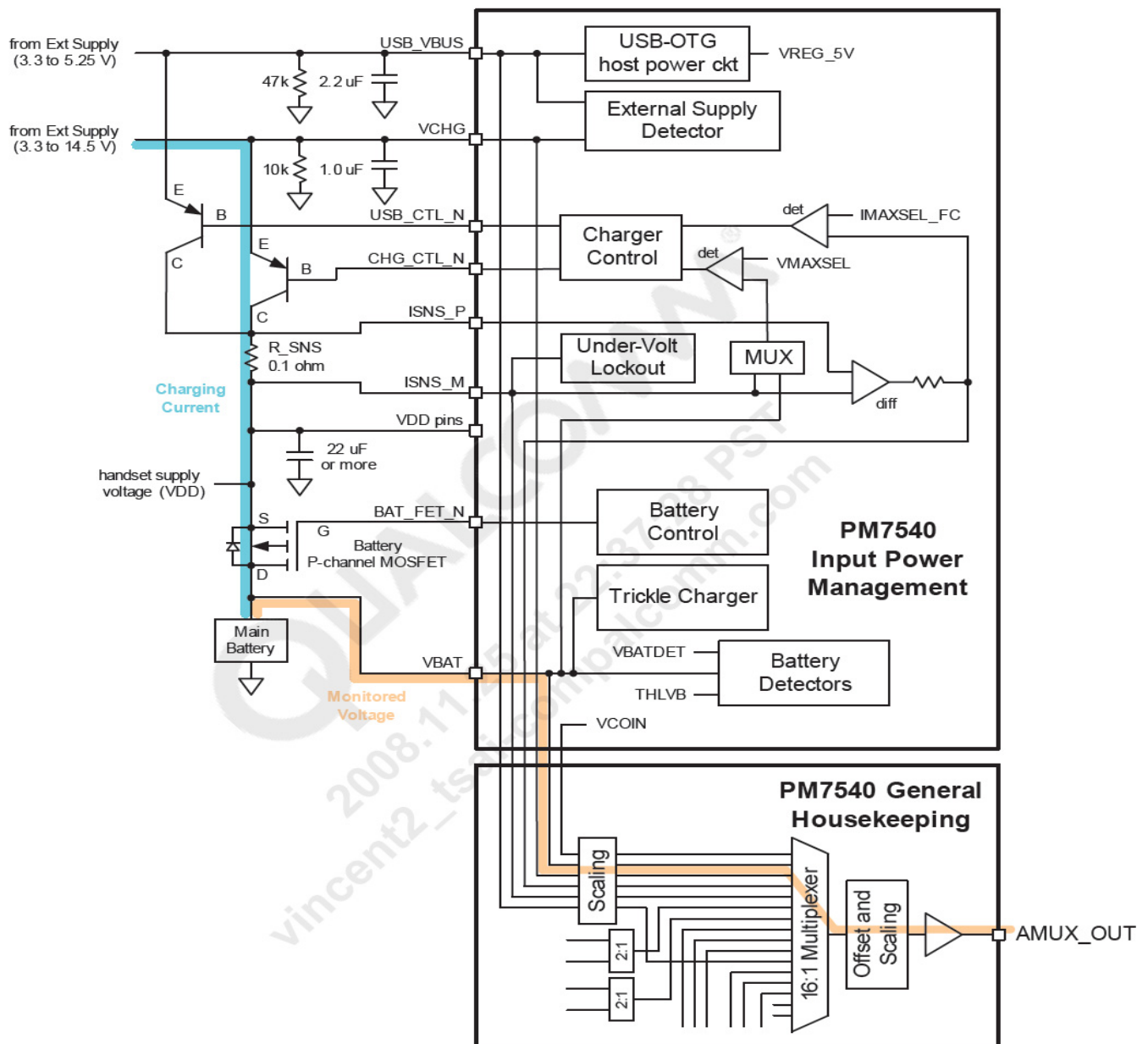


Figure 3-15 Constant current charging

3. TECHNICAL BRIEF

J. Constant voltage charging

Once constant current charging of a lithium-ion battery is finished, the charging continues using either constant voltage or pulse techniques.

The MSM device and its software determines if and when it is appropriate to begin the constant voltage mode with the charging process. Usually the decision to stop the constant current mode is based upon the battery voltage reaching a programmed threshold slightly above the intended final voltage.

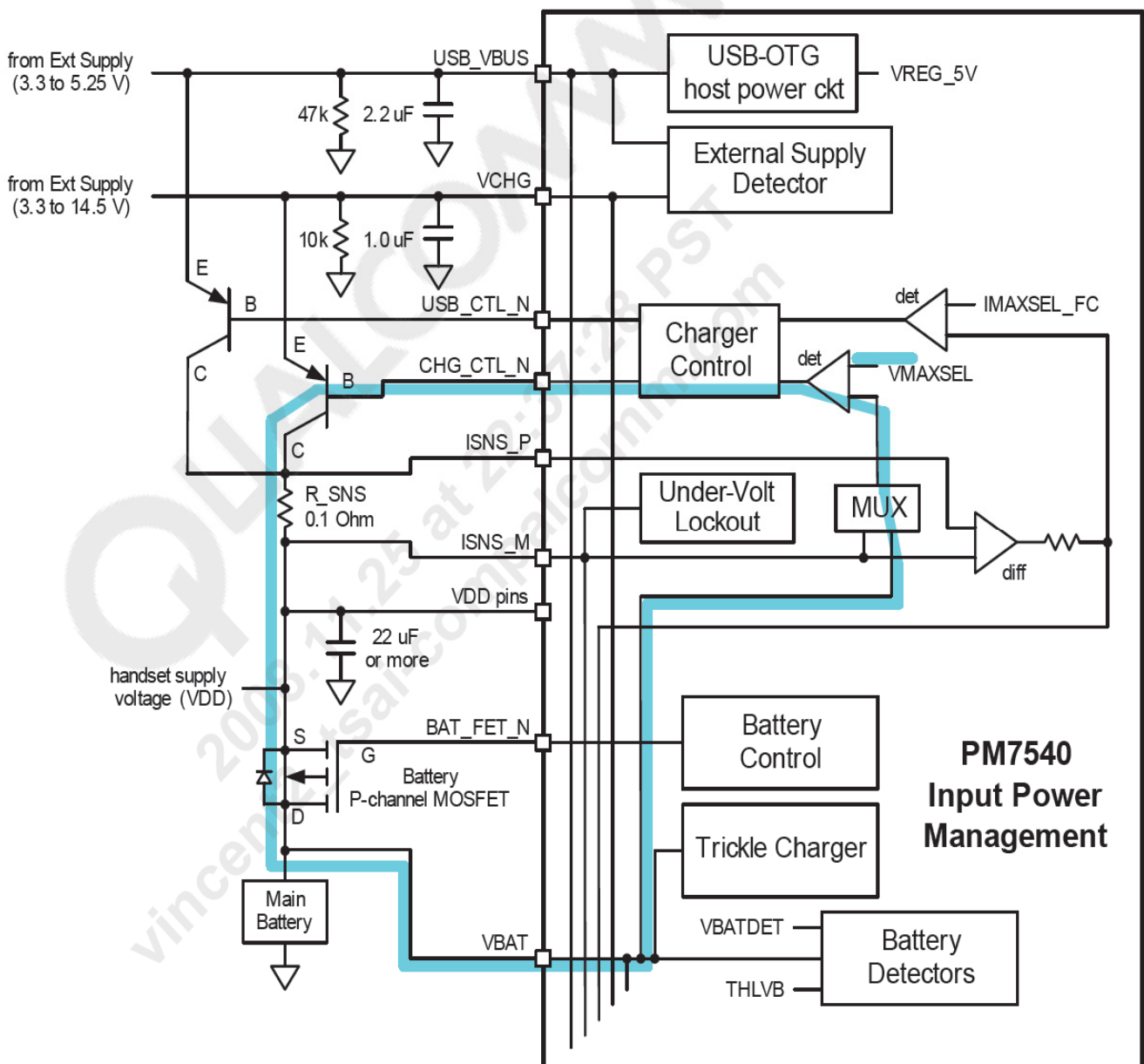


Figure 3-16 Constant voltage charging

3. TECHNICAL BRIEF

K. Coin cell charging

Coin cell charging is enable through MSM control; its supply current is sourced from the main battery through the VBAT pin.

All coin cell charging activity is controlled through software, allowing continuous or periodic charging of the coin cell and management of the main battery current.

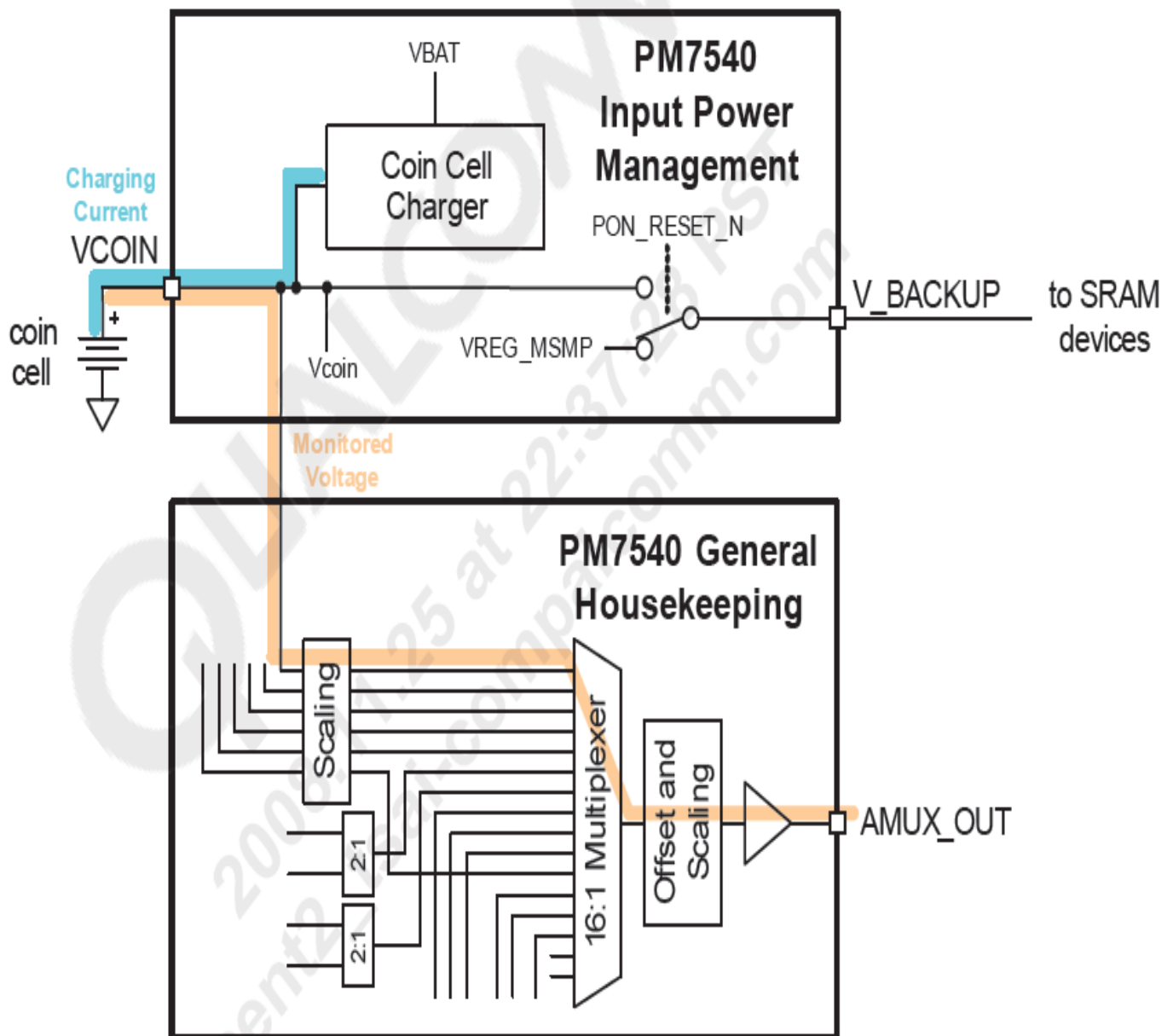


Figure 3–17 Coin cell charging

3. TECHNICAL BRIEF

3.5.2 Output voltage regulation

Twenty-four voltage regulators are provided— all programmable, all derived from a common bandgap reference circuit.

Two major types of voltage regulator circuits are on-chip: switched-mode power supplies (SMPS) and linear regulators. There are three types of SMPS supplies: the boost circuit step up its output voltage relative to the input voltage and is rated for 500mA; the buck circuits step down their output voltages and are rated for either 300 or 500mA each. There are four different linear regulator circuit, three categorized by their output current ratings (300, 150, and 50mA) and the fourth intended for biasing microphone.

VSW_5V	switching output of the +5V boost SMPS circuit.
VREG_5V	Senses the regulated output of the +5V boost SMPS
VSW_MSMC1	Switching output of the MSM core_1 buck SMPS circuit.
VREG_MSMC1	Senses the regulated output of the core_1 buck SMPS
VSW_MSMC2	Switching output of the MSM core_2 buck SMPS circuit.
VREG_MSMC2	Senses the regulated output of the core_2 buck SMPS
VSW_MSME	Switching output of the EBI_1 buck SMPS circuit.
VREG_MSME	Senses the regulated output of EBI_1 buck SMPS circuit.
VSW_PA	Switching output of the PA buck SMPS circuit.
VREG_PA	Senses the regulated output of the PA buck SMPS circuit.

Table 3–2 PM7540 Output Voltage Regulation Pin Description

3. TECHNICAL BRIEF

VREG_GP1	General-purpose linear regulator output #1
VREG_GP2	General-purpose linear regulator output #2
VREG_GP3	General-purpose linear regulator output #3
VREG_GP4	General-purpose linear regulator output #4
VREG_GP5	General-purpose linear regulator output #5
VREG_GP6	General-purpose linear regulator output #6
VREG_MMC	Linear regulator output intended to power MMC circuit.
VREG_MSMA	Linear regulator output intended to power MSM device analog function.
VREG_MSME2	Linear regulator output intended to power EBI_2 circuit.
VREG_MSMP	Linear regulator output intended to power MSM peripheral functions.
VREG_RFRX1	Linear regulator output intended to power primary receiver circuits.
VREG_RFRX2	Linear regulator output intended to power diversity receiver circuits.
VREG_RFTX	Linear regulator output intended to power transmitter circuits.
VREG_RUIM1	Linear regulator output intended to power RUIM_1 circuits.
VREG_SYNT	Linear regulator output intended to power frequency synthesizer circuits.
VREG_TCXO	Linear regulator output intended to power VCTCXO circuits.
VREG_USB	Linear regulator output intended to power the internal USB transceiver.
VREG_WLAN	Linear regulator output intended to power WLAN circuits.
VREG_BIAS	Linear regulator output intended to bias MIC circuits.

Table 3–2 PM7540 Output Voltage Regulation Pin Description

3. TECHNICAL BRIEF

B. PM7540 voltage regulator circuits

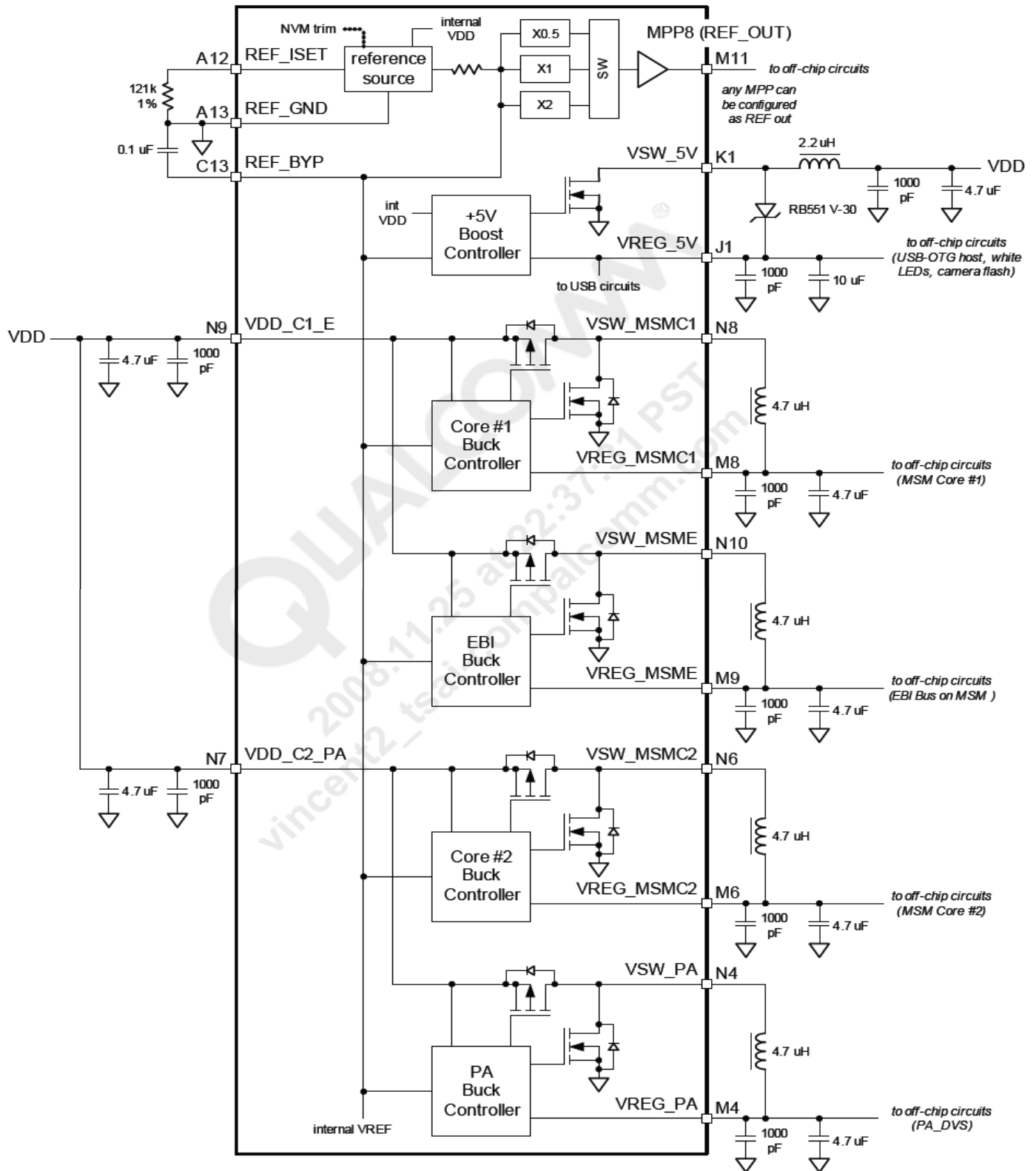


Figure 3-18 Voltage regulator circuit

3. TECHNICAL BRIEF

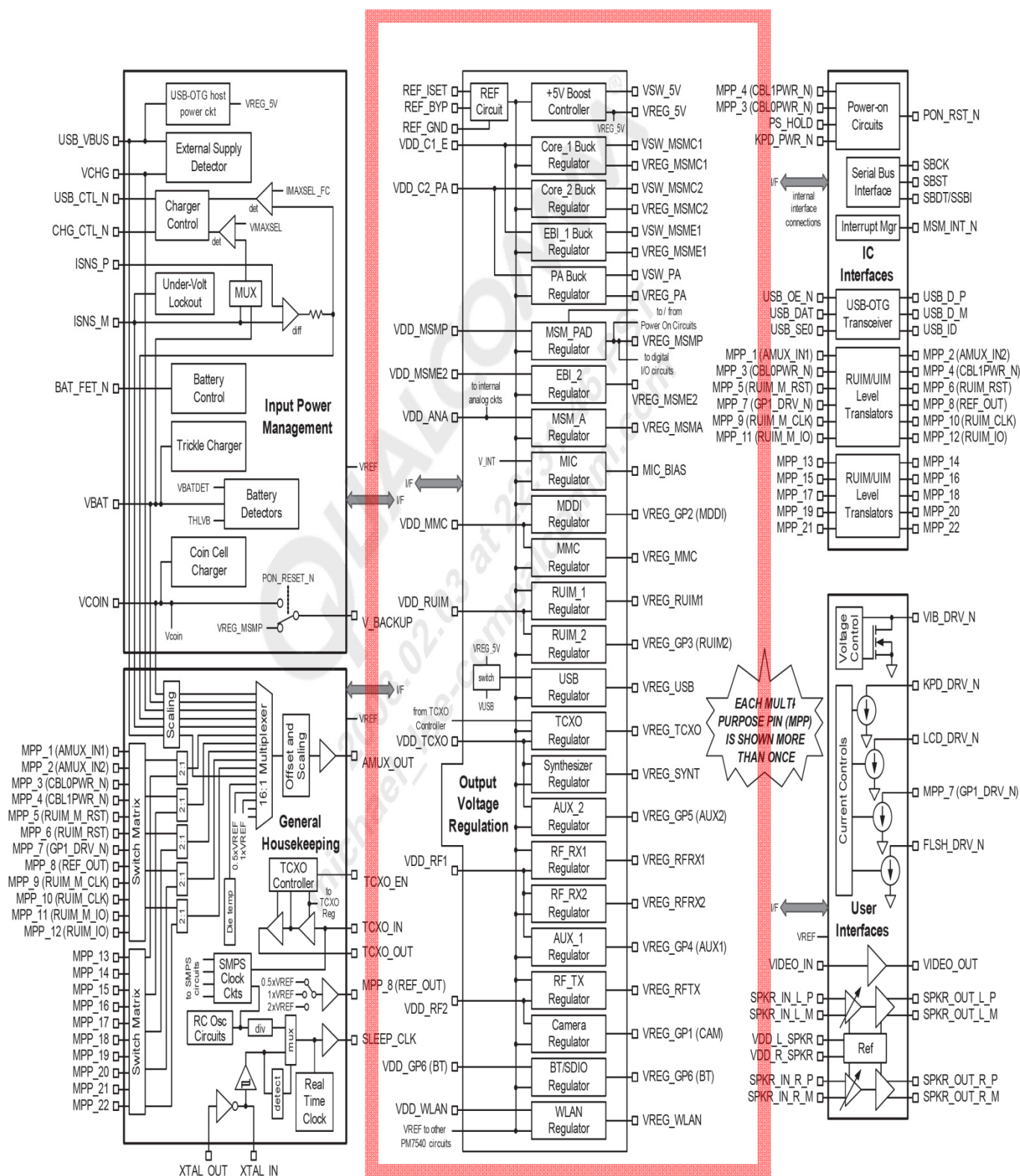


Figure 3-19 Voltage regulator circuit

3. TECHNICAL BRIEF

C. Voltage regulator summary

Type/name ^{1 2}	Default conditions ³	Voltage range	Intended use
SMPS - Boost +5 V (500 mA)	Off, 5.000 V	3.000 to 6.100 V	USB-OTG host, white LEDs, camera flash
SMPS - Buck MSMC1 (500 mA) MSMC2 (500 mA) MSME (500 mA) PA (300 mA)	On, 1.200 V On, 1.200 V On, 1.800 V Off, 1.800 V	0.750 to 3.050 V 0.750 to 3.050 V 0.750 to 3.050 V 0.750 to 3.050 V	MSM core #1; DVS available MSM core #2; DVS available Devices on EBI #1 bus Power amplifier(s); DVS available
Linear - 300 mA MSMA ⁴ MSMP ⁶ WLAN GP6 (BT)	On, 2.600 V On, 2.600 V Off, 2.850 V Off, 2.850 V	1.500 to 3.050 V 1.500 to 3.050 V 1.500 to 3.050 V 1.500 to 3.050 V	MSM analog circuits MSM pad voltage and other IC digital I/Os 802.11 wireless LAN Bluetooth
Linear - 150 mA MMC MSME2 RFRX1 RFRX2 RFTX RUIM1 GP1 (CAM) GP2 (MDDI) GP3 (RUIM2) GP5 (AUX2)	Off, 2.850 V On, 1.500 V Off, 2.850 V Off, 2.850 V Off, 2.850 V Off, 2.850 V Off, 2.850 V Off, 2.850 V Off, 2.850 V Off, 2.850 V	1.500 to 3.050 V 0.750 to 1.525 V 1.500 to 3.050 V 1.500 to 3.050 V 1.500 to 3.050 V 1.500 to 3.050 V 1.500 to 3.050 V 1.500 to 3.050 V 1.500 to 3.050 V 1.500 to 3.050 V	Multimedia or SD circuits Devices on EBI #2 bus First of two RF receiver circuit supplies Second of two RF receiver circuit supplies RF transmitter circuits RUIM module #1 Camera circuits MDDI circuits RUIM module #2 Auxiliary #2 analog circuits
Linear - 50 mA SYNT TCXO USB GP4 (AUX1)	Off, 2.850 V On, 2.850 V Off, 3.300 V Off, 2.850 V	1.500 to 3.050 V 1.500 to 3.050 V 3.000 V to 6.100 V 1.500 to 3.050 V	Tx VCO and PLL circuits VCTCXO and Rx VCO and PLL circuits Internal USB transceiver; not used off-chip Auxiliary #1 analog circuits
Linear - MIC bias	Off, 2.000 V	1.7380, 1.93, 2.00 V	Microphone bias

Table 3–3 Voltage regulator summary

3. TECHNICAL BRIEF

3.5.3 General Housekeeping

Housekeeping functions include an analog multiplexer with gain and offset adjustments; system clock circuits; real time clock for time and alarm functions; buffered reference voltage outputs; and over-temperature protection.

TCXO_IN	Input from the handset VCTCXO
TCXO_EN	Control signal from MSM device that enables TCXO controller tasks.
TCXO_OUT	Buffered and validated VCTCXO output clock signal
XTAL_IN	Connect the 32.768kHz crystal across these pins with capacitor from each pin to ground.
SLEEP_CLK	Buffered 32.768kHz sleep clock signal;
AMUX_OUT	Output of the analog multiplexer.
MPP_1	These are multipurpose pins whose intended functions are the first and second external inputs to the analog multiplexer.
MPP_2	
MPP_8	This is a multipurpose pin whose intended function is a selectable, buffered version of the internal reference voltages.

Table 3–4 PM7540 general housekeeping pin description

3. TECHNICAL BRIEF

A. Analog multiplexer

The PM functions include a 16 to 1 analog multiplexer to select a single analog signal for routing to the MSM device's housekeeping analog to digital converter.

The sixteen multiplexer inputs are derived from five internal connections, six hardwired external connections, and 22 MPPs that can be configured as multiplexer inputs.

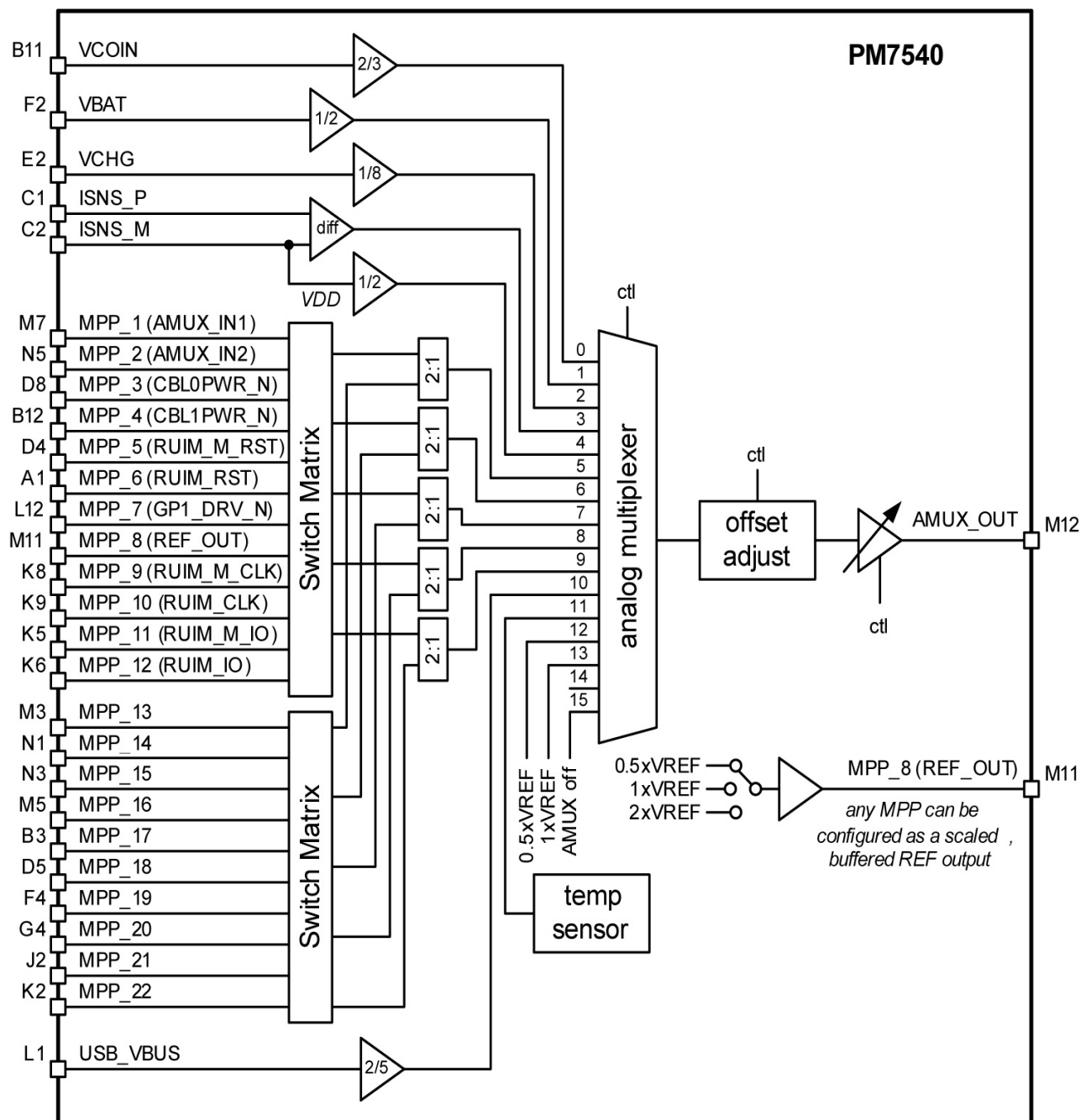


Figure 3–20 Analog multiplexer and associated circuits

3. TECHNICAL BRIEF

B. System clocks

The PMIC includes several clock circuits whose outputs are used for general housekeeping functions and elsewhere within the handset system. These circuits include the TCXO controller and buffers, RC oscillator, 32.768kHz crystal oscillator, SLEEP clock, and SMP S clocks.

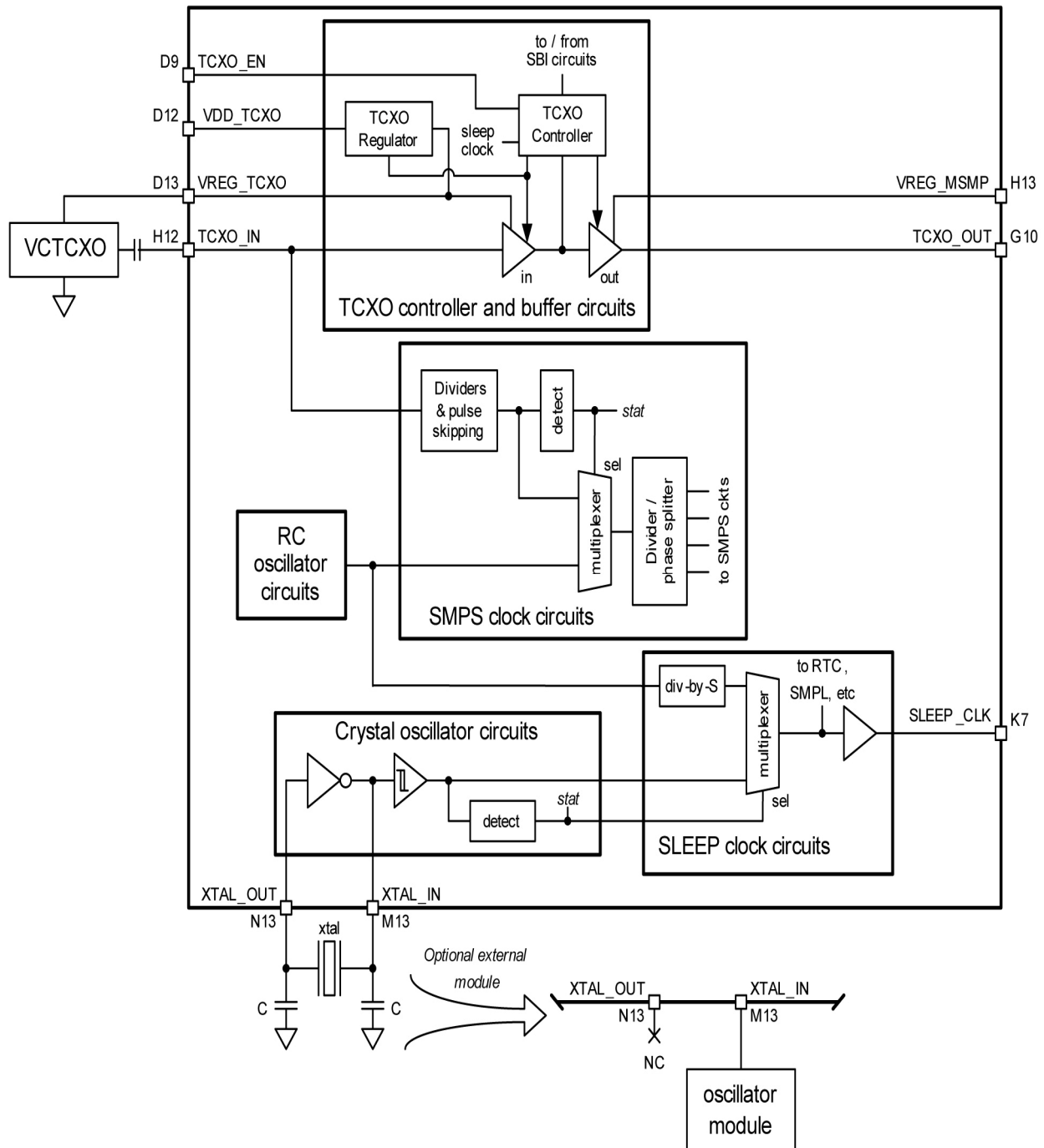


Figure 3-21 System clocks – functional block diagram

3. TECHNICAL BRIEF

3.5.4 User interface

The PM7540 IC supports common handset-level user interfaces. Three dedicated current sinks are intended for driving the keypad backlight, the LCD backlight, and a camera flash.

Alerting the handset user of incoming calls is supported with vibration and audio driver circuits. A vibration motor driver, supports silent alarm. A two-channel speaker driver is available for audible alarms.

KPD_DRV_N is intended to drive the keypad backlight

LCD_DRV_N is intended to drive the LCD backlight

FLSH_DRV_N is intended to drive high-voltage, high-current white or blue LEDs often used as a camera flash.

SPKR_IN_L_M	Minus and plus inputs to the left speaker driver circuit.
SPKR_IN_L_P	
SPKR_OUT_L_M	Minus and plus outputs from the left speaker driver circuit.
SPKR_OUT_L_P	
SPKR_IN_R_P	Minus and plus inputs to the right speaker driver circuit.
SPKR_IN_R_M	
SPKR_OUT_R_M	Minus and plus outputs from the right speaker driver circuit.
SPKR_OUT_R_P	
VIDEO_IN	Video amplifier output
VIDEO_OUT	Video amplifier output.
VIB_DRV_N	Vibration motor driver output
KPD_DRV_N	Programmable current sink intended to support keypad backlights.
LCD_DRV_N	Programmable current sink intended to support keypad backlights.
FLSH_DRV_N	Programmable current sink intended to support a camera flash strobe.
MPP_7	This is a multipurpose pin whose intended function is the programmable current sink intended to support general-purpose LED or backlight devices.

Table 3–5 PM7540 user interface pin description

3. TECHNICAL BRIEF

A. Current driver

The four backlight or LED driver are independently programmable. Three drivers are intended for specific applications and are named accordingly:

KPD_DRV_N is intended to drive the keypad backlight

LCD_DRV_N is intended to drive the LCD backlight

FLSH_DRV_N is intended to drive high-voltage, high-current white or blue LEDs often used as a camera flash.

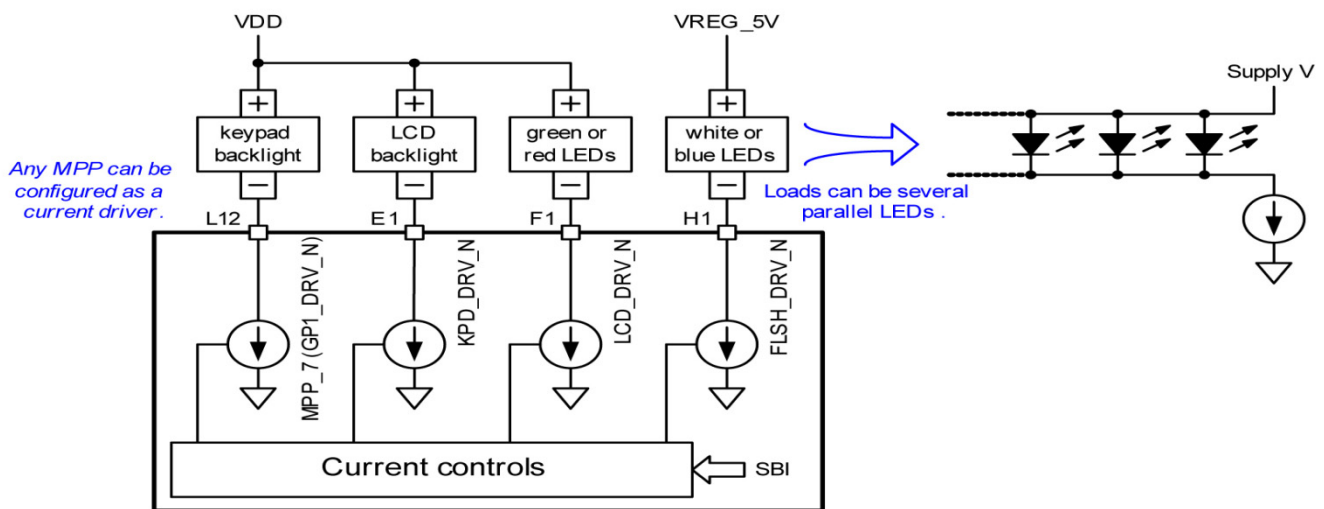


Figure 3-22 Current driver

B. Vibration motor driver

The PM7540 IC supports silent incoming call with its vibrator motor driver. The vibrator driver is a programmable voltage output that is referenced to VDD; when off, its output voltage is VDD. The motor is connected between VDD and pin N2; the voltage across the motor is $V_m = VDD - V_{out}$ where V_{out} is the PM7540 IC voltage at pin N2.

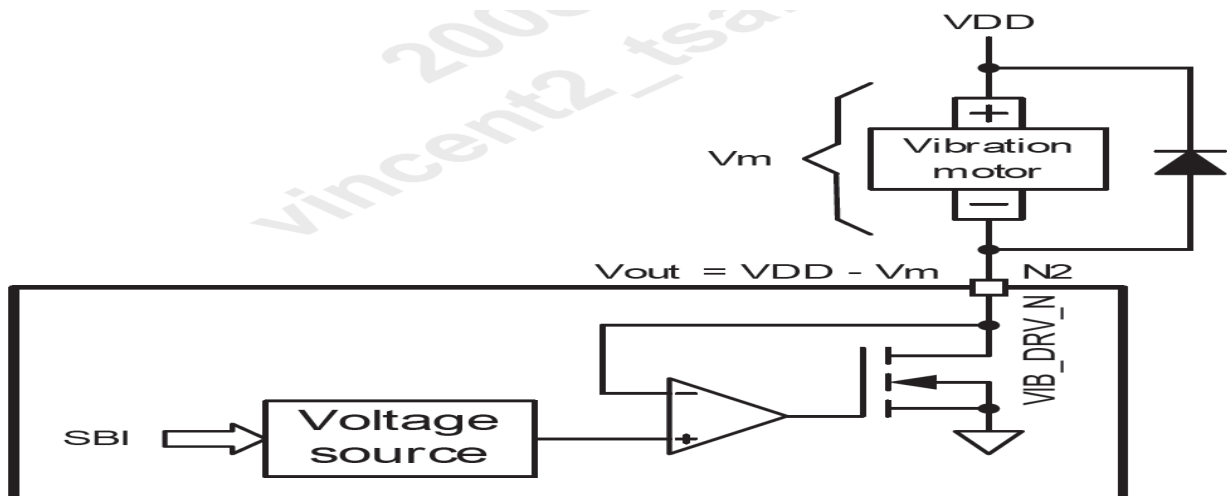


Figure 3-23 Vibrator motor driver

3. TECHNICAL BRIEF

C. Speaker driver

The PM7540 IC includes a stereo speaker driver with variable gain. The input can be configured for mono differential or stereo single-ended operation. Each channel's output is configured differentially, delivering 500mW to each 8-ohm speaker.

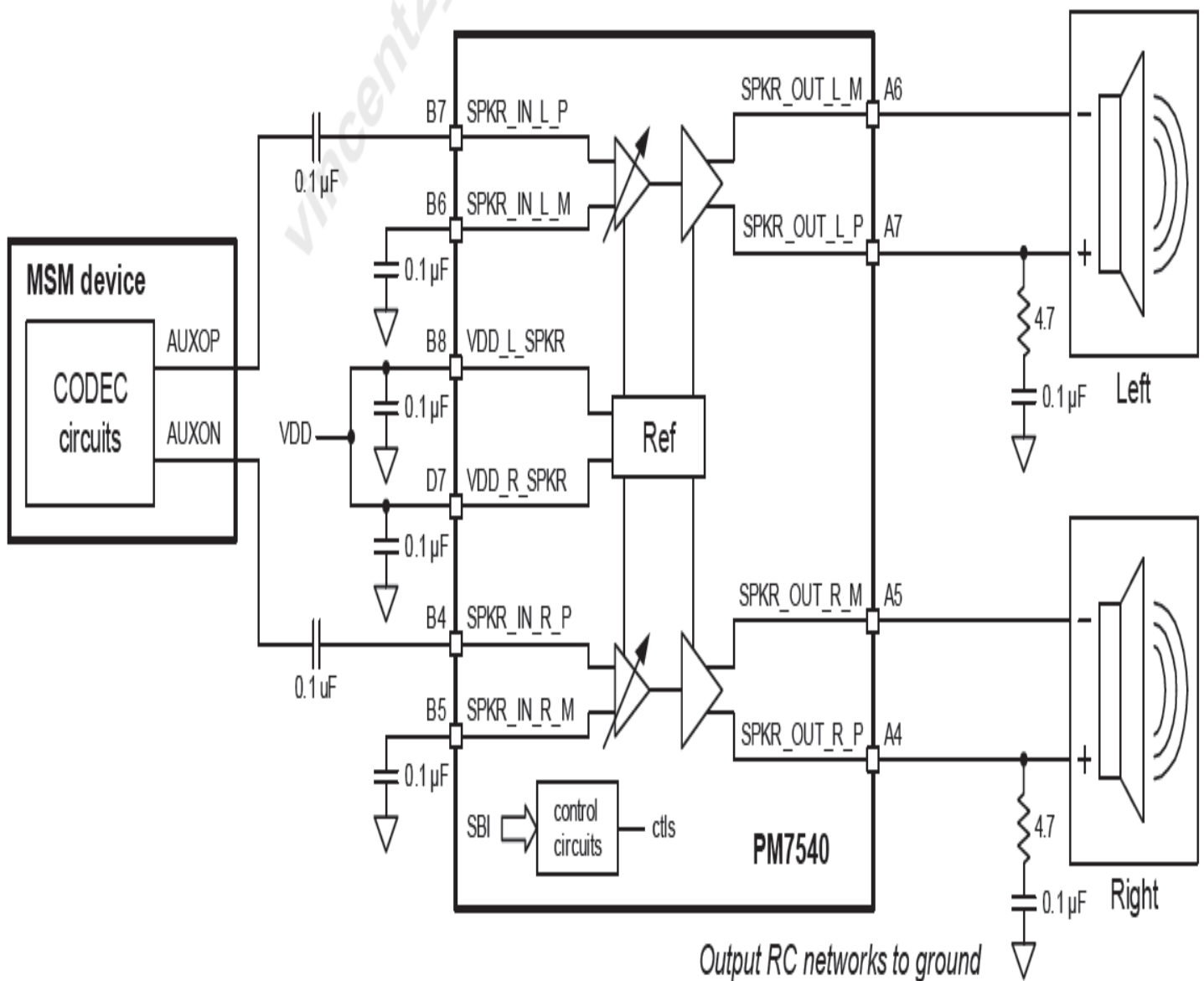


Figure 3–24 Speaker driver

3. TECHNICAL BRIEF

3.5.5 IC-level interface

The PM7540 IC-level interface circuits include power-on circuits, the SBI, the interrupt manager, a USB-OTG transceiver, and RUIM level translators.

KPD_PWR_N	Connect to the keypad power button.
PON_RESET_N	Connect this pin to MSM device's RESIN_N pin. During a PMIC power-on sequence, this signal is driven low to initial as MSM power-on reset.
PS_HOLD	Connect this pin to the MSM device's PS_HOLD output pin.
MPP_3	These two pins are multipurpose pins with the intended function of recognizing a serial cable insertion and initializing the power-on sequence.
MPP_4	
SBST	3-line SBI-- data , clock and strobe signals. For later MSM device: Single-wire SBI.
SBCK	
SBDT/SSBI	
MSM_INT_N	PMIC interrupt status is reported to MSM device using this signal. Logic low signals that an interrupt event has occurred.
USB_ID	Analog input used to sense whether a peripheral device is connected and if connected, to determine the peripheral type. (Don't use in the C570)
USB_D_P	Plus line of the differential, bidirectional USB signal to/from the peripheral device. (Don't use in the C570)
USB_D_M	Minus line of the differential, bidirectional USB signal to/from the peripheral device. (Don't use in the C570)
USB_OE_N	USB output enable signal .(Don't use in the C570)
USB_DAT	Plus line of the digital differential, bidirectional USB signal to/from the MSM device. (Don't use in the C570)
USB_SE0	Minus line of the digital differential, bidirectional USB signal to/from the MSM device. (Don't use in the C570)

Table 3-4 PM7540 IC-level pin description

3. TECHNICAL BRIEF

MPP_11 (RUIM_M_IO)	This pair's intended configuration is the bidirectional RUIM I/O level translator.
MPP_12 (RUIM_IO)	
MPP_9 (RUIM_M_CLK)	This pair's intended configuration is the RUIM clock level translator.
MPP_10 (RUIM_CLK)	
MPP_5 (RUIM_M_RST)	This pair's intended configuration is the RUIM reset level translator.
MPP_6 (RUIM_RST)	
MPP_1 to MPP_22	These multipurpose pins are software configurable with the following options: ● Digital input ● Digital output. ● Digital level translator ● Analog input ● Analog output ● Current sink
VDD_ANA	Input supply voltage for the MSMA linear regulator circuits.
VDD_C1_E	Input supply voltage for core_1 and EBI_1 buck converter circuits.
VDD_C2_PA	Input supply voltage for core_2 and PA buck converter circuits.
VDD_GP2	Input supply voltage for the MMC and GP2 linear regulator circuits.
VDD_GP6	Input supply voltage for the BT linear regulator circuit.
VDD_MSME2	Input supply voltage for the EBI_2 linear regulator circuit.
VDD_MSMP	Input supply voltage for the MSMP linear regulator circuit.
VDD_RF1	Input supply voltage for the RF_RX1, RF_RX2, and AUX_1 linear regulator circuit.
VDD_RF2	Input supply voltage for the RF_TX and GP1 linear regulator circuit.
VDD_RUIM	Input supply voltage for the RUIM_1 and RUIM_2 linear regulator circuit.
VDD_L_SPKR	Power supply for left speaker driver circuit.
VDD_R_SPKR	Power supply for right speaker driver circuit.
VDD_TCXO	Input supply voltage for the TCXO, SYNT, and AUX_2 linear regulator circuit.
VDD_WLAN	Input supply voltage for the WLAN linear regulator circuit.

Table 3–4 PM7540 IC-level pin description

3. TECHNICAL BRIEF

A. Power-on circuits and the power sequences

Dedicated circuits continuously monitor five events that might trigger a power-on sequence. If any of the five events occur these circuits power on the PMIC, determine the handset's available power sources, enable the correct source, and take the MSM device out of reset.

The inputs to the power-on circuit (MPP3, MPP4, PS_HOLD, and KPDPWR_N) are basic digital control signals and the only external output is PON_RESET_N.

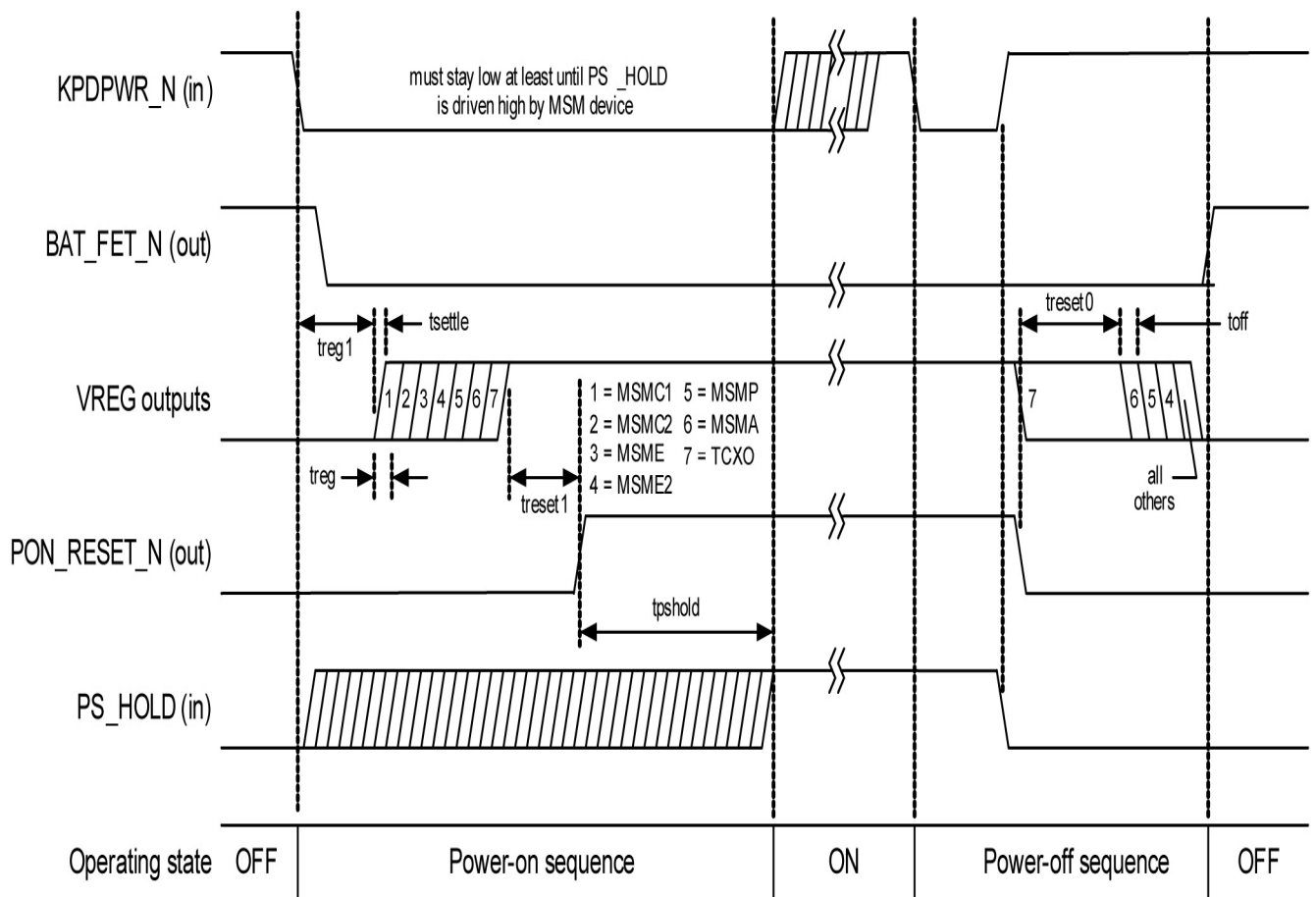


Figure 3–25 High-level power sequences timing diagram

3. TECHNICAL BRIEF

B. Serial bus interface (SBI)

The PM7540 IC allow two serial bus interface (SBI) implementations:

- A 3-wire SBI that support earlier MSM devices
- An SSBI that supports later MSM devices.

In both case, the SBI provides efficient initialization, status, and control communications. Configurable device parameters are set through SBI control registers, while many other registers are available to report parameter settings, device status, and interrupt events.

C. Interrupt manager

The PM7540 interrupt manager receives internal report on numerous functions and conveys real-time and latched status signals to the MSM device, thereby supporting the MSM device's interrupt processing.

The interrupt manager is an embedded function that does not require I/O specifications. All of its controls and output data accessed via the SBI.

D. Universal serial bus/on-the-go

The PM7540 includes an integrated universal serial bus/on-the-go (USB-OTG) transceiver on-chip. This transceiver operates at USB low speed (1.5Mbit/sec) and USB full-speed (12Mbit/sec). It is compliant with USB 2.0 specification, and the OTG Supplement.

E. RUIM level translators

All MPP pairs can be configured as RUIM level translators; three pairs are intended to be used as level translators that interface the handset's MSM device to an external RUIM module: MPP5/6, MPP9/10 and MPP11/12.

3. TECHNICAL BRIEF

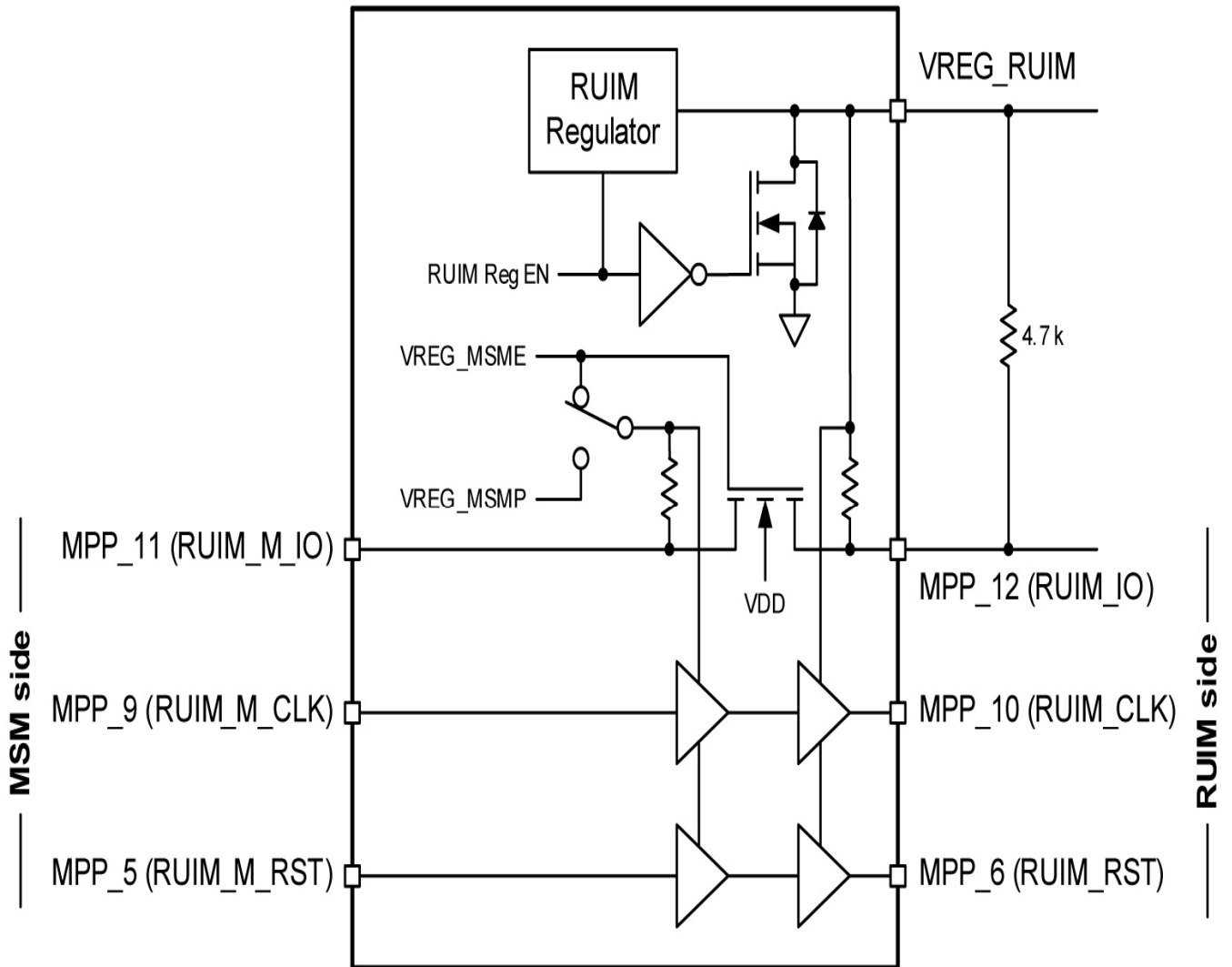


Figure 3-26 RUIM level translators

3. TECHNICAL BRIEF

3.6 MSM7227 (U1)

1. Four integrated processors
 - ARM1136JF-S for application functions.
 - ARM926EJ-S for modem functions.
 - The low-power, high-performance QDSP5000 application digital signal processor.
 - The QDSP4000 modem digital signal processor.
2. Memory support
 - 200MHz bus clock for DDR SDRAM.
 - Dual-memory buses separating the high-speed memory subsystem (EBI1) from low-speed peripherals (EBI2) such as LCD panels.
 - 1.8V or 2.6V memory interface support
 - NAND flash memory interface
 - Boot from NAND/OneNAND
3. Air interface
 - WCDMA: HSDPA, HSUPA, R99.
 - GSM/GPRS/EDGE
 - GPS position location: simultaneous-GPS and time-multiplexed GPS architectures.
 - Bluetooth 2.1 EDR device.
4. RF and PM interfaces
5. MDDI
6. Image processing
7. Video
8. Graphics
 - 2D and 3D rendering
 - 3.5M 3D-lighted triangles/sec
 - Resolution support: up to WVGA
 - Frame rate: (MPEG4/H.263 30fps@WVGA and H.264@15fps)
 - 3D pixel fill rate: 133MP/sec.
9. Audio
 - Vocoder support
 - Voice recognition, including speaker-independent digit dialing
 - Acoustic echo cancellation.
 - PureVoice Audio AGC.
 - Internal vocoder supporting 13Kbps Pure Voice.
 - Standard MIDI with 16 voices.
 - 72-tone CMX
10. Connectivity
 - High-speed on the go universal serial bus. (HS USB OTG)
 - Three universal asynchronous receiver transmitter (UART) serial ports.
 - Two data mover (DM) high speed UARTs (4Mbps)
 - USIM controller (via second or third UART)
 - USB-UICC
 - Four integrated 4-bit secure digital (SD) controller for SD/mini SD cards and SDIO
 - Transport stream interface (TSIF) for reception of digital mobile broadcast signals

3. TECHNICAL BRIEF

11. Internal functions

- Secure boot: protects against re-flashing attacks.
- Secure component framework
- Secure storage
- Unchangeable hardware ID unique to each MSM device.

12. GPIOs

- The MSM7227 IC includes 133 general-purpose I/O pins.

3. TECHNICAL BRIEF

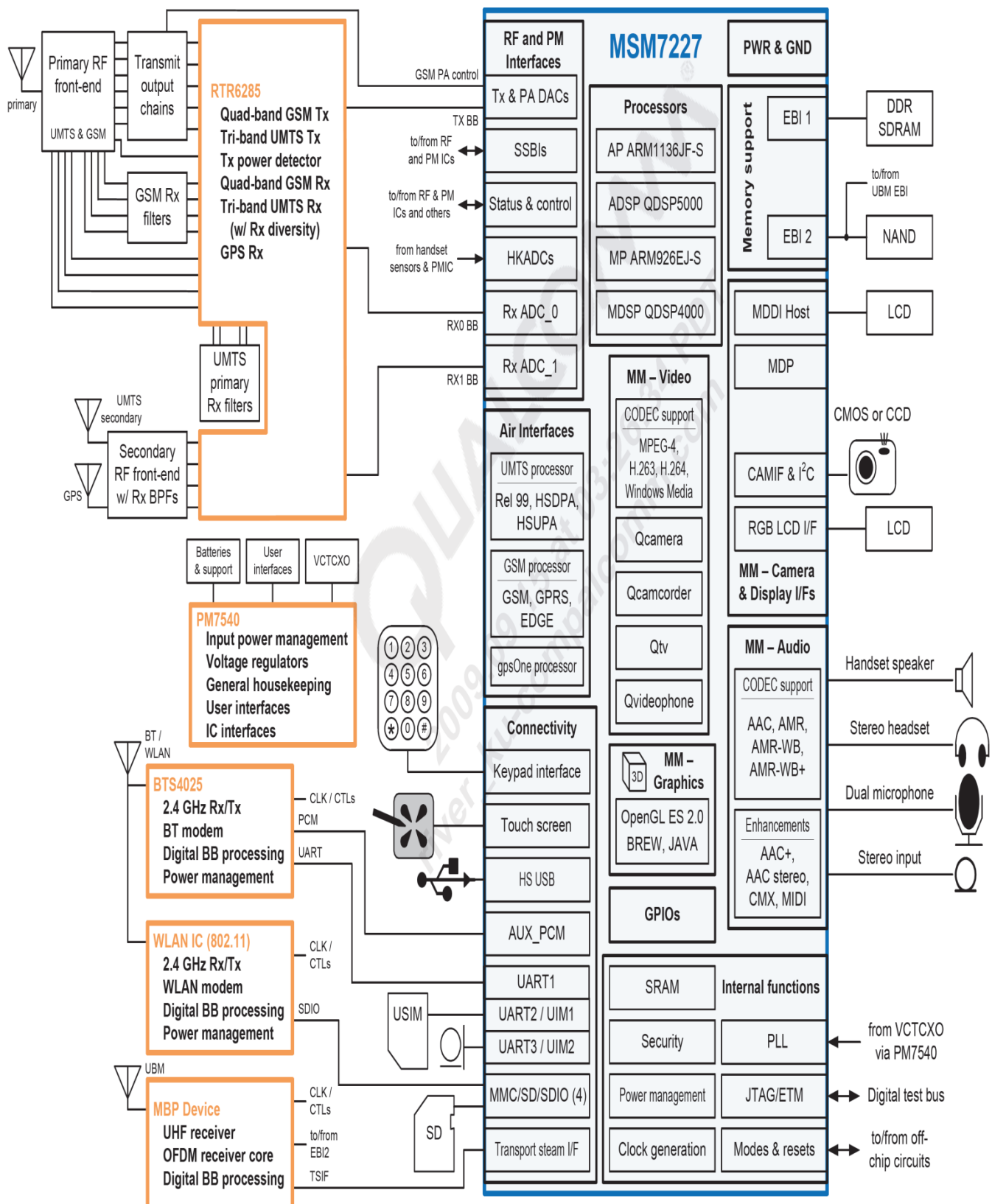


Figure 3-24 MSM7227 functional block diagram

3. TECHNICAL BRIEF

3.6.1 MSM7227 architecture

The MSM7227 integrates multiple microprocessors on chip: two ARM processors and two DSP processors.

- Modem subsystem
 - ARM926EJ-S microprocessor
 - QDSP4 (mDSP) processor
- Modem subsystem
 - ARM1136JF-S microprocessor
 - QDSP5 (aDSP) processor

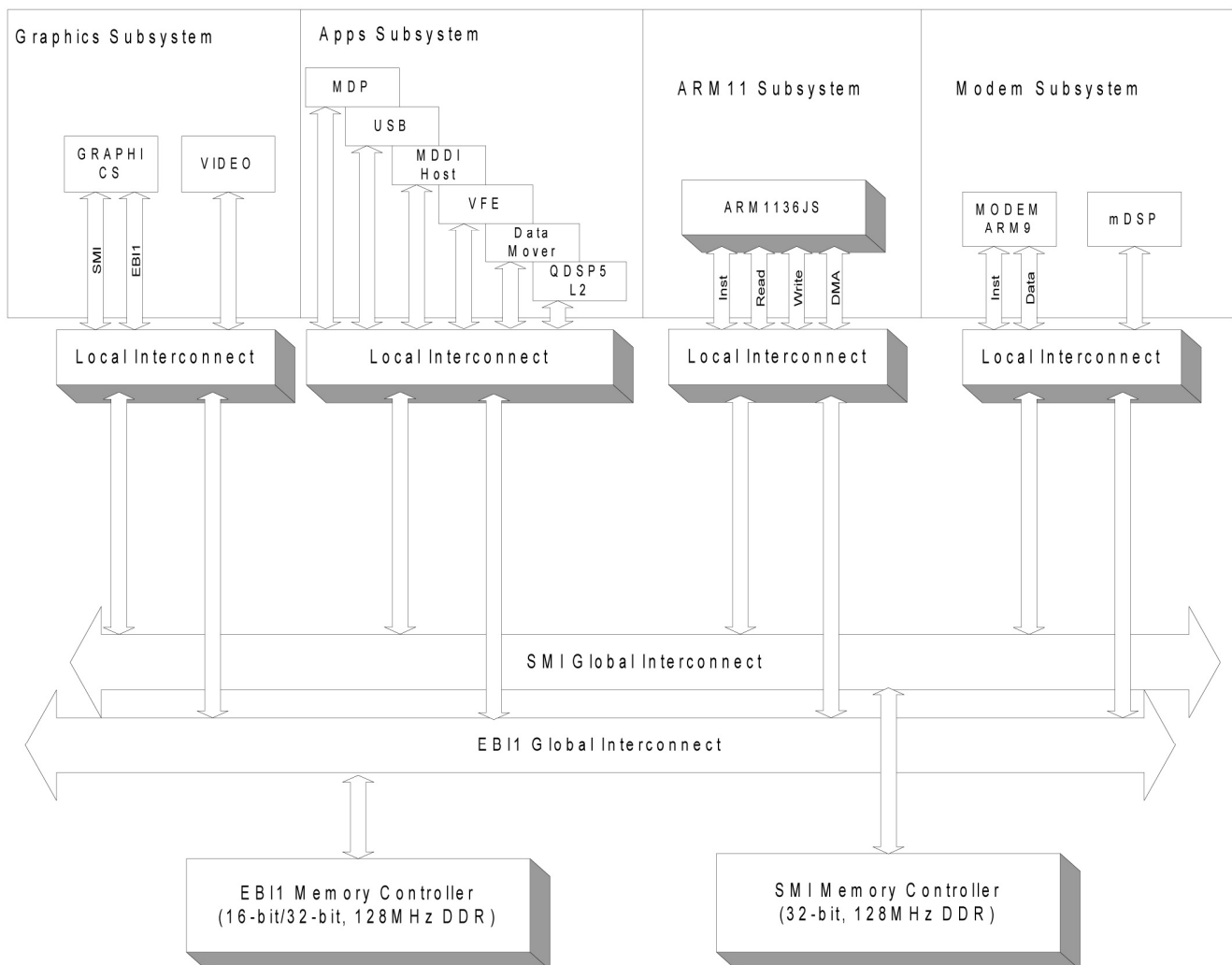


Figure 3-27 MSM7227 high-level architecture

3. TECHNICAL BRIEF

A. Modem subsystem

The modem subsystem is defined as everything under direct or indirect control of the mode m processor. It includes all blocks that provide modem functionality directly (such as WCD MA modulation and demodulation, searching, GPS, GSM modulation and demodulation, etc.) and all blocks that support primary modem functionality, such as that modem DSP, modem AHB bus, sleep controller, interrupt controller, etc.

The MSM7227 modem subsystem consists of the following components:

- An ARM926EJ-S as the main modem processor.
- A modem-to-applications bridge that connects the modem subsystem to the application subsystem
- A modem-to-peripheral bridge that connects the modem subsystem to the peripheral subsystem.
- A modem DSP that controls the operation of the concurrent modem hardware blocks and assists with symbol level processing of the physical layer traffic.
- A 64KB secure BOOT ROM containing the primary boot loader for the ARM926EJ-S processor.
- An internal RAM used by the modem processor for interprocessor communication with the applications.
- A security mode control (SMC) block containing, among other things, electrical fuses (Q fuses) that are used to disable specific functionality.
- An always-on modem power manager block in the always-on power domain to control power collapsing of the MSM7227 modem subsystem.

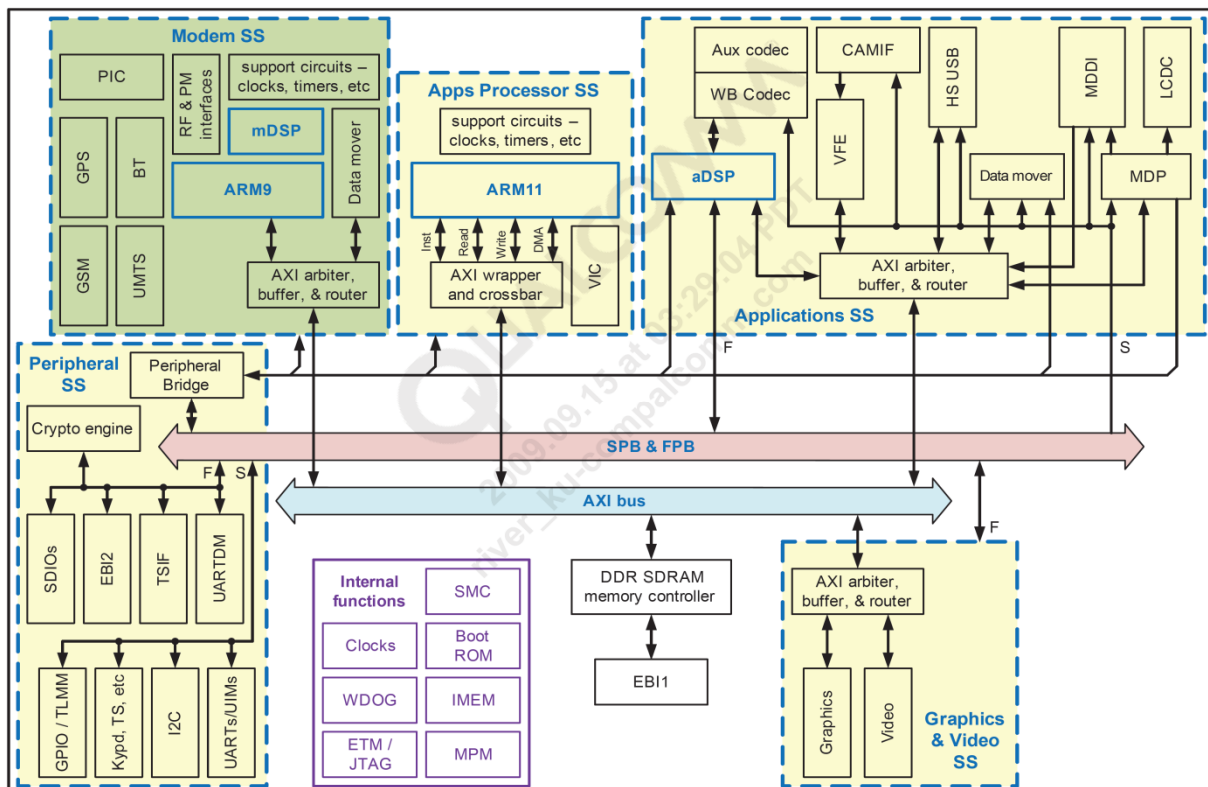


Figure 3-28 MSM7227 Modem subsystem function block diagram

3. TECHNICAL BRIEF

B. Peripheral Bus

The peripheral bus enables bus masters to connect with numerous peripheral device and lower bandwidth memories both within and external to the MSM7227 IC, thereby offloading the buses to the stacked memory interface (SMI) and external bus interface a (EBI1).

Five bus masters are supported: the modem processor, applications processor, applications data mover, applications DSP, and the mobile display processor (MDP). The peripheral bus slave devices exist within the bus subsystem, applications subsystem, and graphics subsystem.

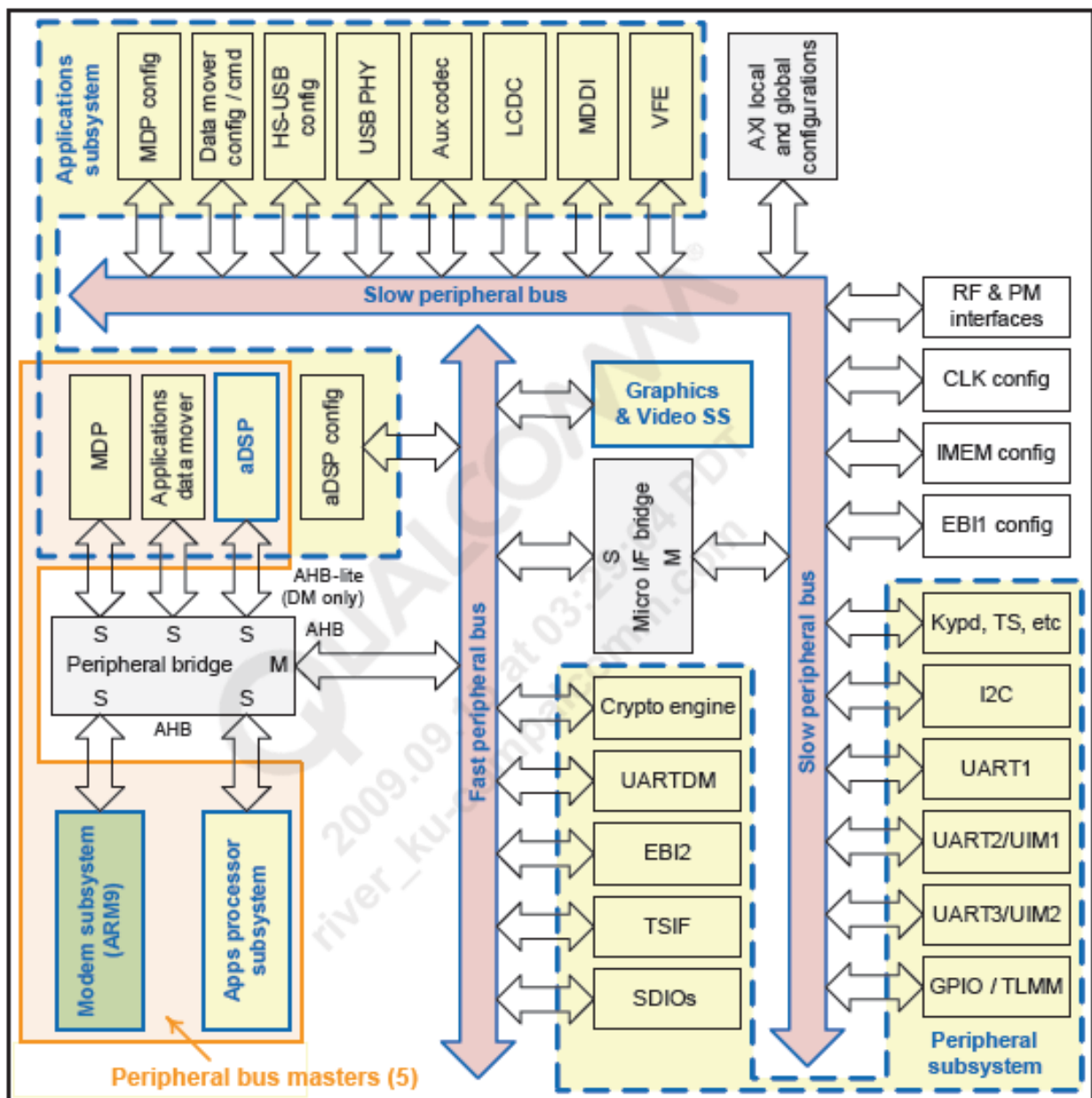


Figure 3-29 Peripheral bus connection diagram

3. TECHNICAL BRIEF

C. Application Subsystem

The MSM7227 application subsystem consists of the following components.

- An ARM1136 as the main application processor, with its supporting watchdog, clock and timers.
- An applications-to-modem bridge that connects the application subsystem to the modem subsystem.
- An application-to-peripheral bridge that connects the application subsystem to the peripheral subsystem.
- An application DSP, the QDSP5 with 128KB of memory that handles applications such as vocoder, video and graphics.
- A dedicated application data mover.
- Connectivity blocks that support various applications such as USB.
- Two MDDI host blocks and the MDP block that support various LCD display.
- Video blocks such as an MDDI client, video front-end and TV out to support camera and other video functions.

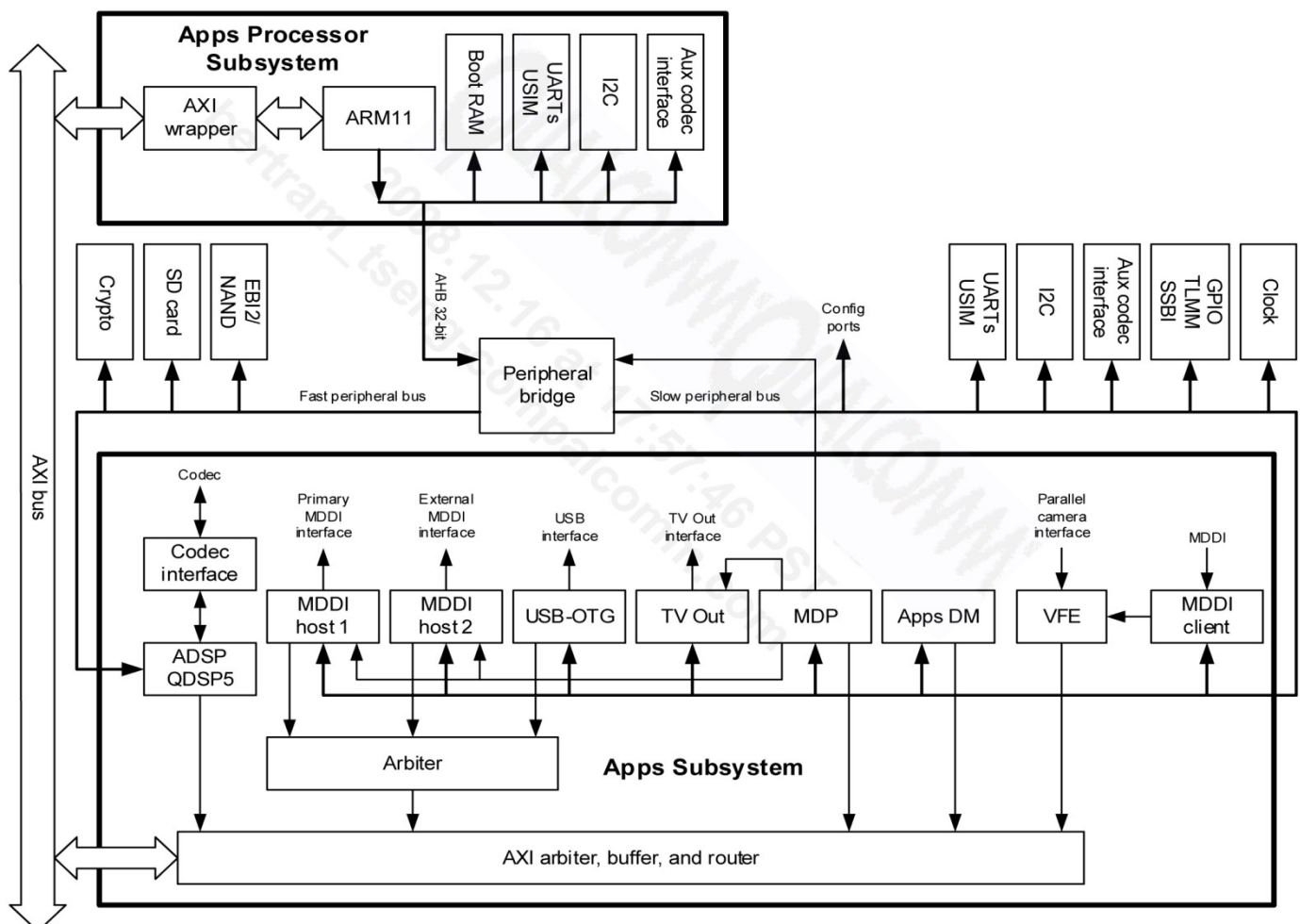


Figure 3-30 Application subsystem block diagram

3. TECHNICAL BRIEF

D. AXI buses: EBI1

To satisfy the requirement of high performance data transfer, a 64-bit advanced extensible interface (AXI) bus is used as a standard bus interface between the bus masters and slaves. The bus masters are connected to the external high-speed memory interfaces, EBI1. The various MSM7227 bus masters that can access the high speed memory interfaces via the AXI buses.

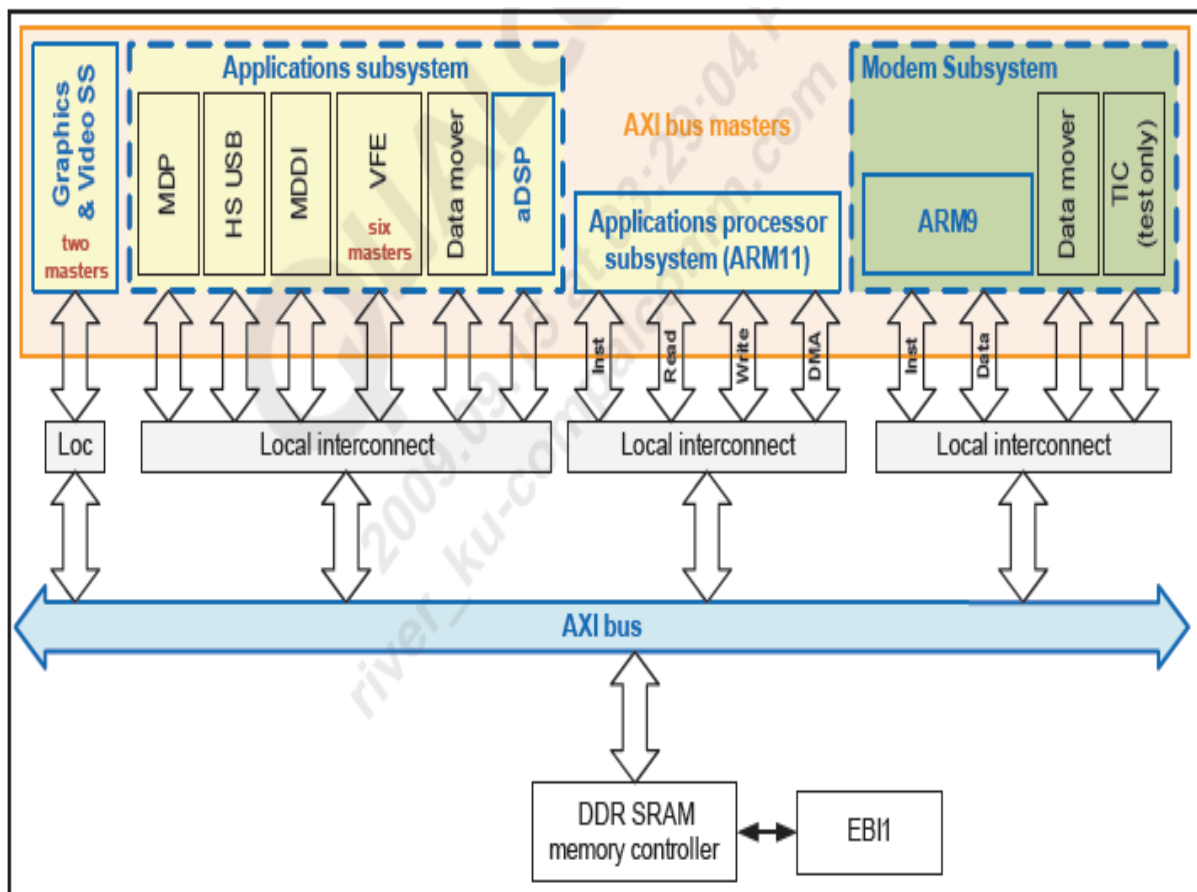


Figure 3-31 AXI bus connection diagram

3. TECHNICAL BRIEF

3.6.2 Memory Support

The MSM7227 IC provides two categories of memory interfaces: high-speed and low-speed. High-speed interfaces are needed for the multiple on-chip ARM processors, high-performance graphics, and video applications. The low-speed interface supports memory devices such as NAND flash and asynchronous SRAM, peripheral devices such as LCD, and the FLO receiver for multicast reception.

To support the high bandwidth, high density, and low latency requirements of the advanced on-chip application, the MSM7227 IC has a 64-bit high-speed, high-performance memory slave interfaces: the external bus interface 1 (EBI1).

The MSM7227 includes the low-speed EBI2 to support peripheral devices, more memory devices, and the FLO receiver for multicast reception.

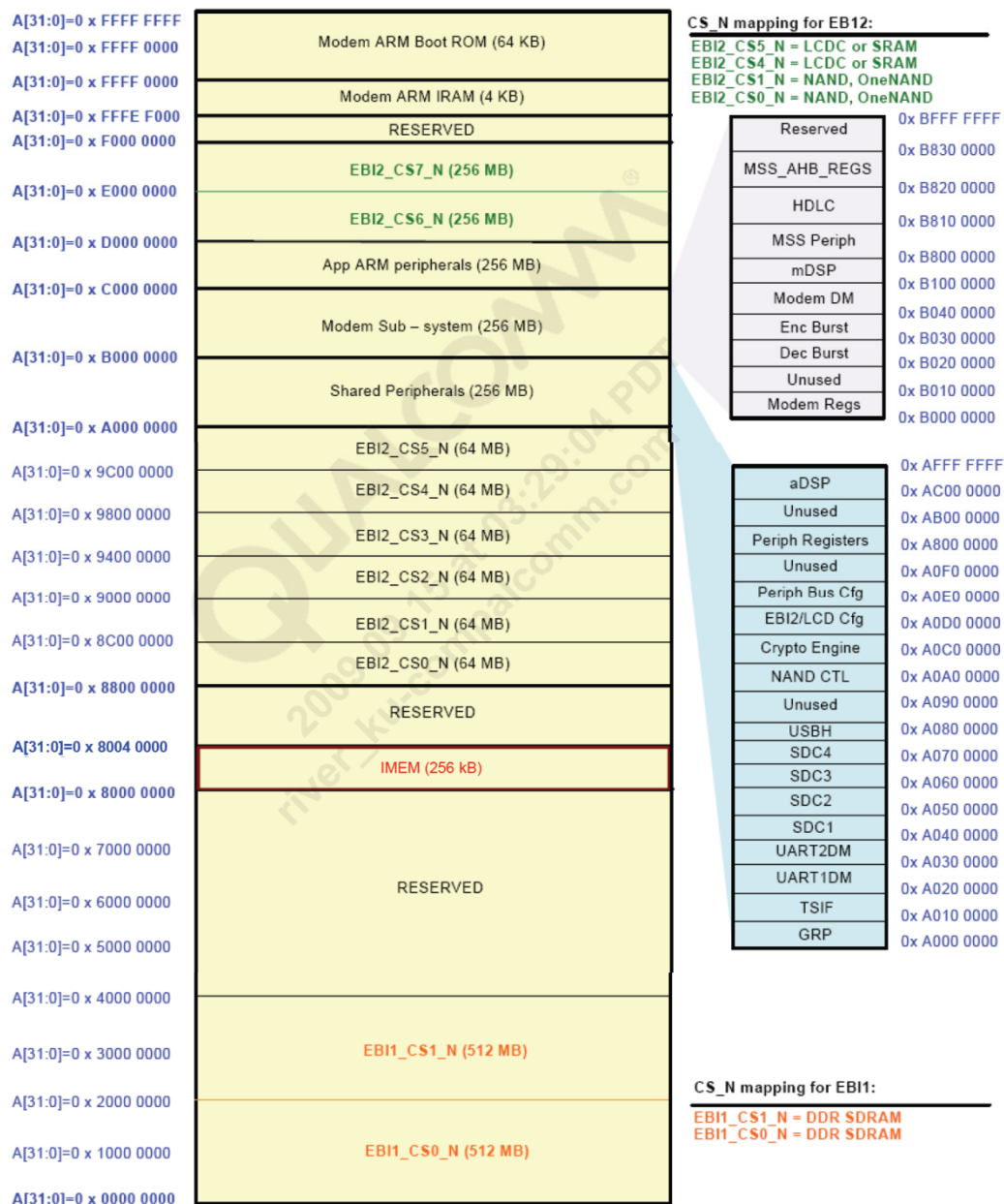


Figure 3–32 MSM7227 memory map

3. TECHNICAL BRIEF

A. High-speed memory interface (EBI1)

■ General EBI1 features include:

- Support for only low-power memories at 1.8V I/O power supply voltage
- AXI bus frequencies up to 200MHz
- DDR SDRAM clock rates from 9.6MHz to 200MHz
- A 16/32 bit static and dynamic memory interface

■ EBI1 connections include:

- Two-16 bit address bus
- One-32 bit bidirectional data bus
- Other bus signaling
- Data strobes, data masks, clocks, chip selects, enable, etc.

B. Pins Description.

[illegible]

3. TECHNICAL BRIEF

PIN	Symbol	Description
J26	EBI1_DQ31	32bit EBI1 DATA bus.
K20	EBI1_DQ30	
J20	EBI1_DQ29	
J23	EBI1_DQ28	
J22	EBI1_DQ27	
K19	EBI1_DQ26	
K26	EBI1_DQ25	
L22	EBI1_DQ24	
L19	EBI1_DQ23	
L23	EBI1_DQ22	
L20	EBI1_DQ21	
M19	EBI1_DQ20	
L26	EBI1_DQ19	
M26	EBI1_DQ18	
M22	EBI1_DQ17	
M23	EBI1_DQ16	
N26	EBI1_DQ15	
N19	EBI1_DQ14	
N20	EBI1_DQ13	
P26	EBI1_DQ12	
R26	EBI1_DQ11	
P19	EBI1_DQ10	
R25	EBI1_DQ9	
T26	EBI1_DQ8	
R22	EBI1_DQ7	
R23	EBI1_DQ6	
R20	EBI1_DQ5	
T23	EBI1_DQ4	
T22	EBI1_DQ3	
U25	EBI1_DQ2	
U23	EBI1_DQ1	
U22	EBI1_DQ0	

3. TECHNICAL BRIEF

PIN	Symbol	Description
H26	EBI1_DQS3	EBI1 data strobes
L25	EBI1_DQS2	
P20	EBI1_DQS1	
U26	EBI1_DQS0	
J25	EBI1_DM3	EBI1 data masks
M20	EBI1_DM2	
N25	EBI1_DM1	
V26	EBI1_DM0	
W26	EBI1_DCLK	Differential clock for DDR SDRAM
W25	EBI1_DCLKB	
V19	EBI1_BA0_N	DDR bank address
AC25	EBI1_BA1_N	DDR bank address
U19	EBI1_CS1_N	DDR SDRAM chip select
U20	EBI1_CS0_N	
R19	EBI1_CKE1	DDR clock enables
T19	EBI1_CKE0	
T20	EBI1_RAS_N	DDR Row select
N17	EBI1_CAS_N	DDR Column select
AB23	EBI1_WE_N	Write enable
AD26	EBI1_OE_N	Output enable

3. TECHNICAL BRIEF

3.6.3 Low-speed memory interface (EBI2)

The external bus interface 2 (EBI2) is the second of two MSM7227 external memory interfaces. EBI2 provides the interface for slow peripheral devices such as LCD, NAND flash memory, and the FLO receiver.

■ EBI2 features include:

The MSM7227 EBI2 interface supports asynchronous memory devices such as FLASH and SRAM (16bit and 8bit). Page mode is NOT supported.

- Programmable wait states for access, hold, and recovery on all chip selects.
- Bus sizing operations allow WORD, HWORD, and BYTE accesses to 16 and 8 bit memory.
- Insertion of recovery/turnover wait states (RECOV_CYCLES) to the beginning of the current chip select access when the previous access was a read to a different chip select, or a when the current access is a write and the previous access was a read to the same chip select.
- Addressing to chip select assertion setup wait states (ADDR_CS_SETUP) at the beginning of the access.
- RD_ACTIVE and WR_ACTIVE define the minimum assertion time for read and write respectively.
- Since the RECOV_CYCLES and ADDR_CS_SETUP wait states are applied at the beginning of the access, only the field with the greatest number of wait states take effect.
- Hold time between WE_N rising and the address/CS_N/data signals changing (WR_CS_HOLD wait states), as required by specific type of peripherals. The minimum value is RD_CS_HOLD=0.
- Supports byte-addressable 16 bit device (UB_N and LB_N signals).

The EBI2 interface not only supports memory devices, but can be used for parallel, port mapped LCD. The related features include:

- Support for both Motorola and Intel timing types (24bit, 18bit and 16bit)
- Bus sizing operations allow 18bit write accesses to an 18 bit LCD interface, WORD and HWORD accesses to parallel 16 bit data parallel interface, and WORD, HWORD, and BYTE access to parallel 8 bit data interface.
- System WORD, HWORD, and BYTE accesses to 16 bit and 8 bit wide devices on all chip selects.
- Support for 18 bit wide device is write mode only.
- Access times of up to 2000ns (at 66MHz AHB bus speed)
- Specific to Intel Interface mode
- EBI2 I/O are compatible with either 1.8V or 2.6V pad power supply voltage.
- The EBI2 supports any generic external peripheral whose interface timing is similar to asynchronous memories.

■ EBI2 connections

- 20 bit address bus
- 16 bit bidirectional data bus
- Chip selects, enables, etc.

3. TECHNICAL BRIEF

A. Pins Description.

PIN	Symbol	Description
B18	EBI2_ADR9	Reserved
B25	EBI2_ADR8	Reserved
F21	EBI2_ADR7	Reserved
B20	EBI2_ADR6	Reserved
F20	EBI2_ADR5	Reserved
H17	EBI2_ADR4	Reserved
E20	EBI2_ADR3	Reserved
C20	EBI2_ADR2	Reserved
C18	EBI2_ADR1	Reserved
F18	EBI2_ADR0	Reserved
B21	EBI2_DATA15	16 bit data bus
B22	EBI2_DATA14	
C21	EBI2_DATA13	
E21	EBI2_DATA12	
C22	EBI2_DATA11	
C24	EBI2_DATA10	
E26	EBI2_DATA9	
B24	EBI2_DATA8	
F25	EBI2_DATA7	
C26	EBI2_DATA6	
D26	EBI2_DATA5	
C23	EBI2_DATA4	
B23	EBI2_DATA3	
C25	EBI2_DATA2	
D25	EBI2_DATA1	
E23	EBI2_DATA1	

3. TECHNICAL BRIEF

PIN	Symbol	Description
L16	EBI2_LB_N	NAND flash address latch enable
C19	EBI2_UB_N	NAND flash Command latch enable
H19	EBI2_WE_N	NAND flash Write enable
B19	EBI2_OE_N	NAND flash Read enable
H20	EBI2_CS7_N	Chip select
J18	EBI2_CS6_N	Chip select 1st LCD
J17	EBI2_CS5_N	Chip select
H23	EBI2_CS4_N	Chip select
F22	EBI2_CS1_N	Chip select 2nd NAND
F23	EBI2_CS0_N	Chip select 1st NAND
G25	EBI2_BUSY0_N	Busy signal 1st NAND

3. TECHNICAL BRIEF

3.6.4 Housekeeping ADC

The MSM7227 device has an on-chip 12 bit analog to digital converter (ADC) that is available for digitizing analog signals representing parameter such as battery voltage, temperature, and RF power levels. These parameters support handset-level housekeeping functions—various tasks that must be performed to keep the “house”, or handset, in order. Thus the term housekeeping ADC (HKADC) is used. The ADC is also for touch screen purpose and hence is named the TSHKADC.

The MSM7227 TSHKADC is a 12 bit successive approximation circuit. The resolution of ADC is programmable and can operate in one of the following mode: 12 bit, 10 bit or 8 bit. The ADC will operate in 8 bit and 10 bit mode during housekeeping applications and will operate in 12 bit mode only during touch screen application.

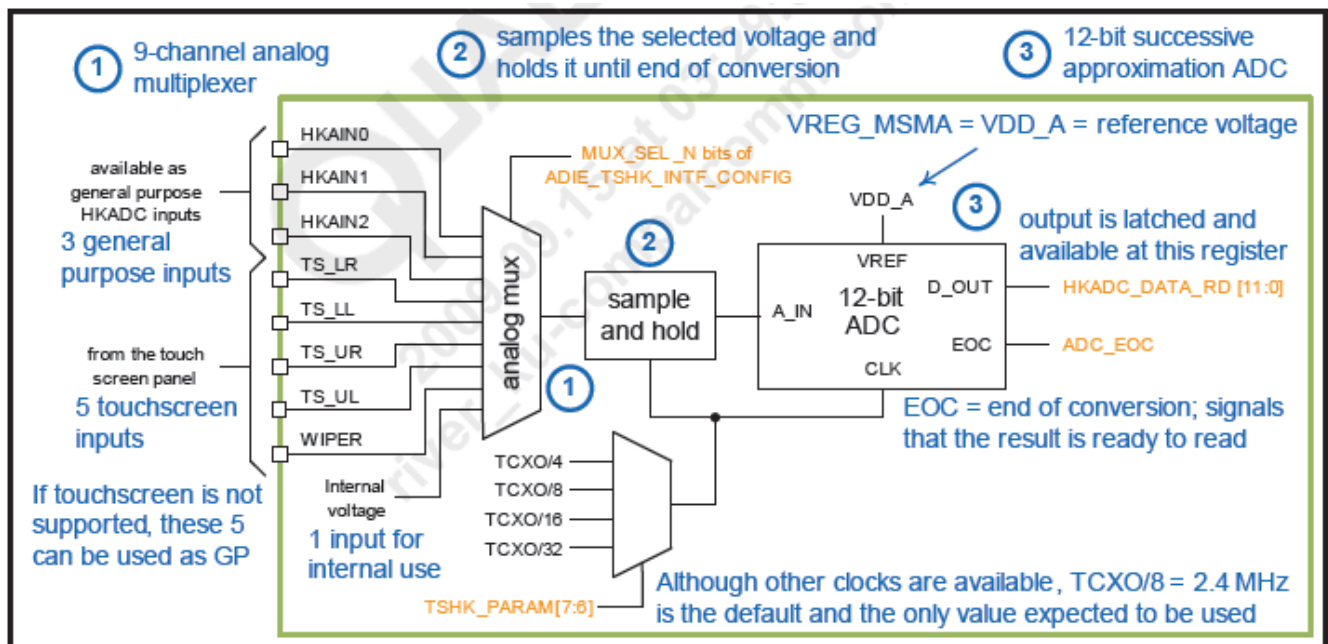


Figure 3-33 HKADC function block diagram

3. TECHNICAL BRIEF

3.6.5 MDDI and MDP

The mobile display digital interface (MDDI) is used for communications between the MSM7227 IC and display devices and/or a camera. A mobile display processor (MDP) is also provide a hardware accelerator that improves processing speeds and expands compatibility to include the EBI2 parallel interface.

A. MDDI

The MDDI is a cost effective, low power solution that enables high-speed short range communication between the MSM and either display devices and/or a camera using digital packet data links. MDDI simplifies the interconnection, reduces its cost, and improves reliability.

The devices connected by the MDDI link are called the host and client. Data going from the host to the client travels in the forward direction, and data from the client to the host travels in the reserve direction. The host always drives the strobe to the client, even when reserve data packets are sent. Data can flow in both the forward and reverse directions over the data pairs, although the host is always the master of the data link.

When interfacing to an LCD, the mobile device is the MDDI host and is the master of the communication link. When interfacing to a camera, the mobile device is the MDDI client and the camera is the host (and master of the link).

1. Pins Description.

PIN	Symbol	Description
AD13	MDDI_P_STB_N	LCD differential strobe pair
AE13	MDDI_P_STB_N	
AD14	MDDI_P_DATA_N	LCD differential data pair
AE14	MDDI_P_DATA_P	
AG15	MDDI_C_STB_N	Camera differential strobe pair
AH15	MDDI_C_STB_P	
AG14	MDDI_C_DATA0_N	Camera differential data pair 0
AH14	MDDI_C_DATA0_P	
AG13	MDDI_C_DATA1_N	Camera differential data pair 1
AH13	MDDI_C_DATA1_P	
AB14	MDDI_E_STB_N	Peripheral differential strobe pair
AA14	MDDI_E_STB_P	
AA15	MDDI_E_DATA_N	Peripheral differential data pair
AB15	MDDI_E_DATA_P	
AD15	VDD_MDDI	MDDI power supply
AE15	VSS_MDDI	MDDI ground

3. TECHNICAL BRIEF

3.6.6 Image Processing

There are two major functional blocks with the MSM7227 IC's image processing feature: the camera interface and TV out (or video out) interface.

A. Camera interface

The camera interface is intended for direct connection of a camera sensor to the MSM7227 device. It is used primarily in Qcamera, Qcamcorder, Qtv, and Qvideophone application. The MSM device will accept raw Bayer pattern data, execute the required image processing, and prepare the image for capture or transmission. The MSM device is also capable of supporting a YUV 4:2:2 input from the sensor.

A.1 CAMIF connections

Camera interface connections include:

- 12bit data bus for the pixel data information
- Horizontal and vertical synchronization signals
- Two-wire I2C bus as a control path between the MSM device and the camera module.
- dedicated master and pixel clock signals.
- two hardware-controlled synchronous control outputs (for shutter and flash)
- two pairs of hardware-controlled asynchronous control output (for auto-focus motors and zoom).

3. TECHNICAL BRIEF

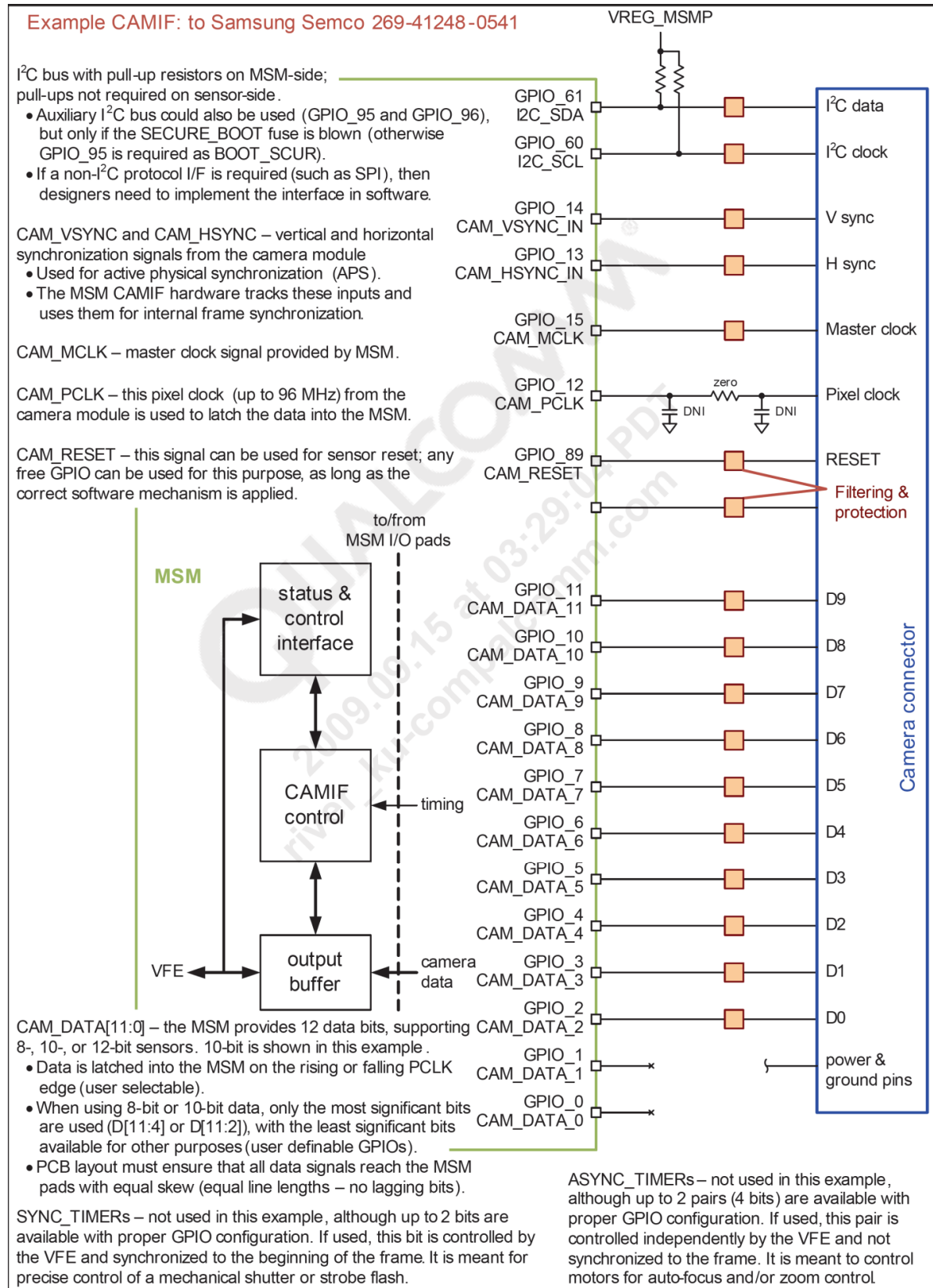


Figure 3–34 Parallel camera interface connections

3. TECHNICAL BRIEF

A.2 Pin Description

PIN	Symbol	Description
M8	CAM_DATA[11]	Parallel camera interface pixel data input
M7	CAM_DATA[10]	
L8	CAM_DATA[9]	
M1	CAM_DATA[8]	
N8	CAM_DATA[7]	
L5	CAM_DATA[6]	
N7	CAM_DATA[5]	
L7	CAM_DATA[4]	
M5	CAM_DATA[3]	
M4	CAM_DATA[2]	
L2	CAM_DATA[1]	
M2	CAM_DATA[0]	
P5	CAM_PCLK	Clock pixel input: data, vsync, and hsync signals
P11	CAM_HSYNC_IN	Parallel camera horizontal sync input
M11	CAM_VSYNC_IN	Parallel camera vertical sync input
N11	CAM_MCLK	Synchronization clock for sensors without their own
T11	AUX_I2C_SCL	Auxiliary I2C clock
N5	AUX_I2C_SDA	Auxiliary I2C data
I\$4	CAM_MRST	Software-controlled camera reset control signal
AD1	SYNC_TIMER1	Camera control, synchronous timer output 1
AB20	SYNC_TIMER2	Camera control, synchronous timer output 2
AD17	ASYNE_TIMER1A	Camera control, asynchronous timer output 1
AB17	ASYNC_TIMER1B	Camera control, asynchronous timer output 1
AE19	ASYNC_TIMER2A	Camera control, asynchronous timer output 2
AA19	ASYNC_TIMER2B	Camera control, asynchronous timer output 2

3. TECHNICAL BRIEF

3.6.7 Audio

The MSM7227 audio front comprises the stereo wideband codec, PCM interface, and additional DSP audio processing.

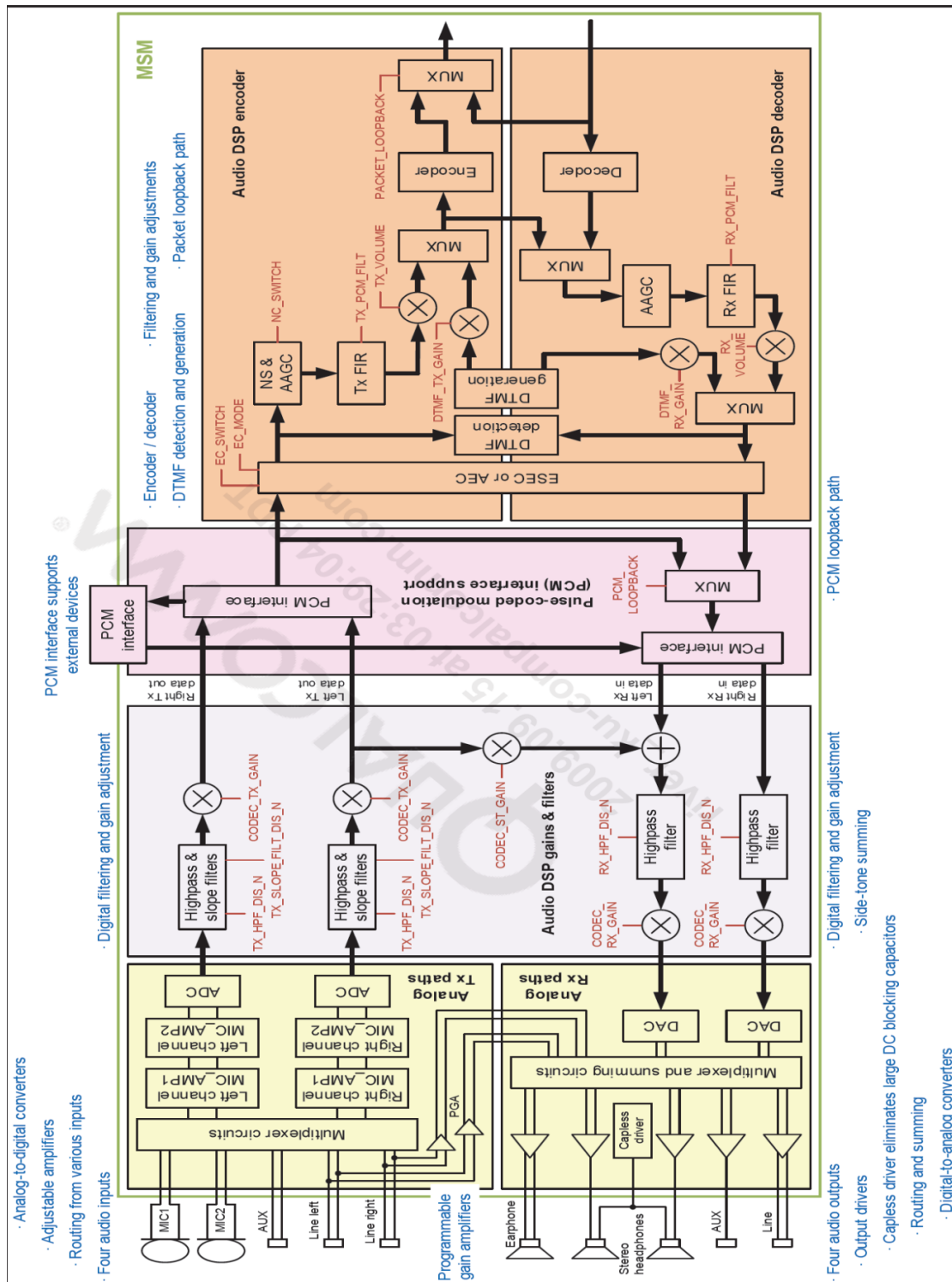


Figure 3–35 Codec, audio DSP, and PCM interface

3. TECHNICAL BRIEF

A. Audio connections

MSM7227 audio connections fall primarily into seven categories:

- Microphone inputs
- Auxiliary input
- Line inputs
- Earphone outputs
- Stereo headphone outputs
- Auxiliary output
- Line outputs

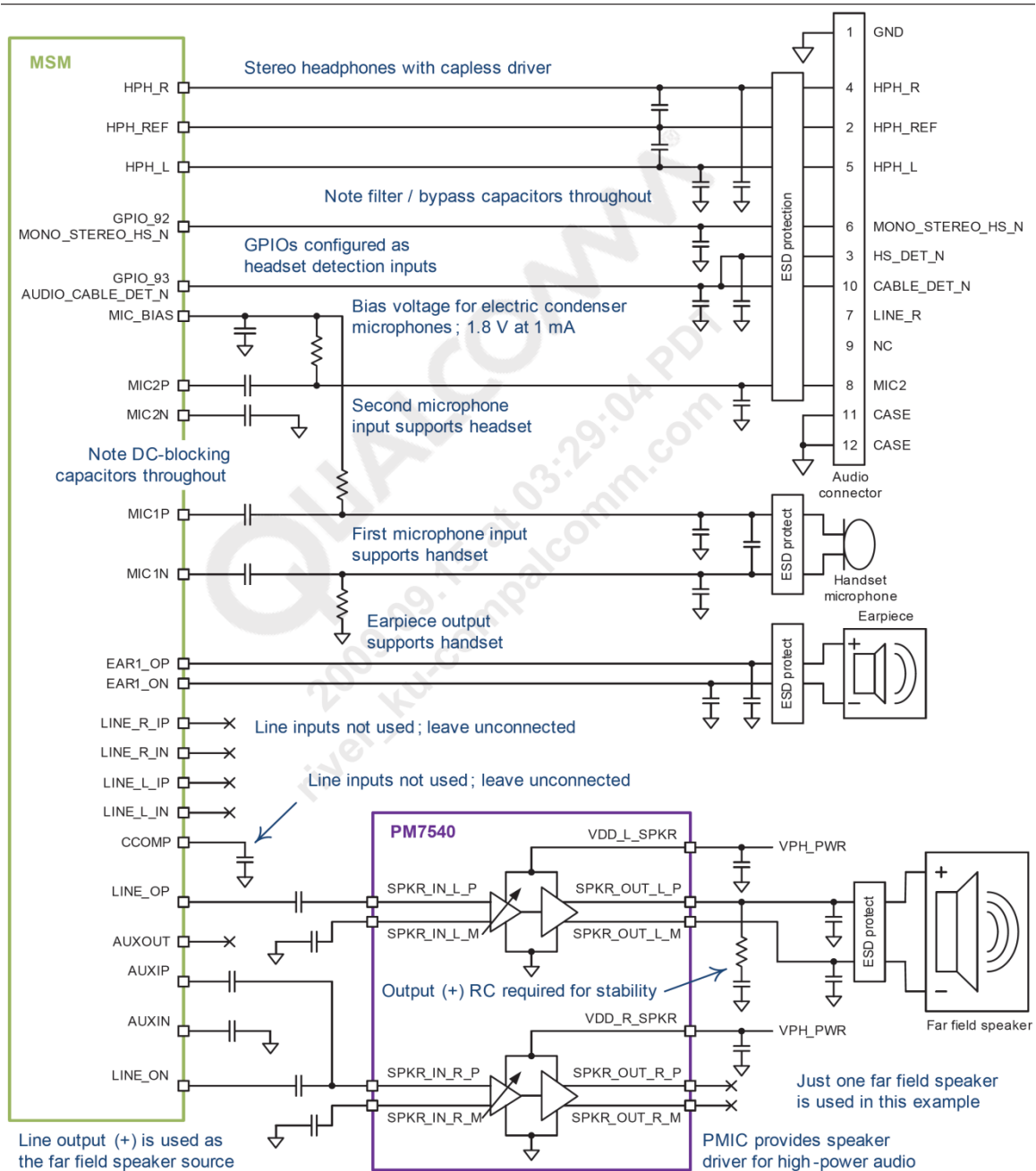


Figure 3-36 Analog codec front end with audio connections

3. TECHNICAL BRIEF

3.6.8 Connectivity

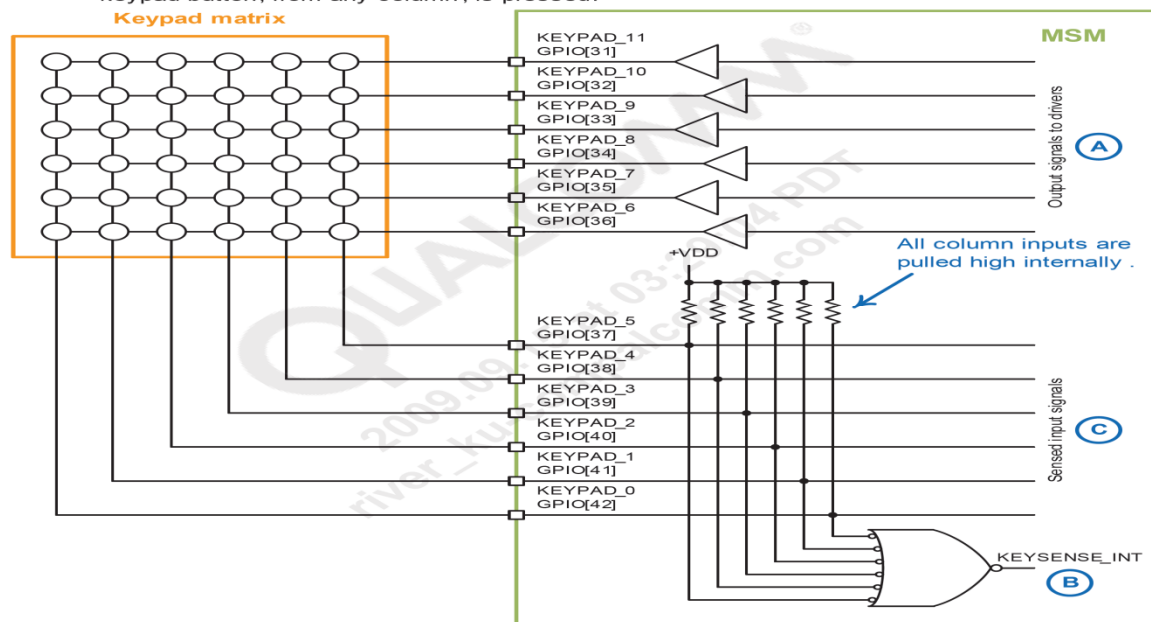
The MSM7227 supports many interfaces that provide handset users with connectivity to other people and data systems.

- Keypad interface
- MMC/SD/SDIO
- High-speed USB
- UARTs
- USIM
- USB-UICC
- transport stream interface for digital mobile broadcast
- Touchscreen
- I2C interface

A. Keypad interface

The MSM7227 provides a keypad interface that supports up to 6X6 or 7X5 keypad matrices. One set of MSM pins is connected to the keypad's columns and is used for sensing; another set of pins is connected to the keypad's row and is used for driving. The sensed columns reveal when any keypad button is pressed, and then the rows are driven to determine precisely which keypad button was pressed.

- ① Any keypad button press is detected by ORing all column signals together using a set of KEYPAD pins (such as KEYPAD[5:0] as shown below).
- Before a keypad button is pressed, all rows are driven low. (A)
 - When a keypad button is pressed, its corresponding column is pulled low (since all rows are low).
 - The KEYSENSE_INT signal is asserted whenever any keypad button, from any column, is pressed. (B)



- ② When the interrupt signal is received, the MSM begins scanning the keypad.
- During a scan, each row is sequentially driven low, one at a time. (A)
 - As each row is driven low, the columns are sensed. (C)
 - The precise keypad button being pressed is revealed when that button's column reads low while that button's row is driven low.

Figure 3-37 6 X 6 matrix

3. TECHNICAL BRIEF

B. Pin Description

PIN	Symbol	Description
AH20	Keypad[11]	Driven keypad line
AA20	Keypad[10]	Driven keypad line
AE20	Keypad[9]	Driven keypad line
AD20	Keypad[8]	Driven keypad line
AG22	Keypad[7]	Driven keypad line
AE26	Keypad[6]	Configurable keypad line; driven or sensed
AH22	Keypad[5]	Configurable keypad line; driven or sensed
AD21	Keypad[4]	Sensed keypad line
AE22	Keypad[3]	Sensed keypad line
AB21	Keypad[2]	Sensed keypad line
AG23	Keypad[1]	Sensed keypad line
AB22	Keypad[0]	Sensed keypad line

3. TECHNICAL BRIEF

C. MMC/SD/SDIO

A secure digital (SD) memory card is a flash-based memory card specifically designed to meet the security, capacity, performance, and environmental requirements inherent to newly emerging audio and video consumer electronic devices. The physical form factor, pin assignments, and data transfer protocol are forward-compatible with the multimedia card (MMC) while including some enhancements.

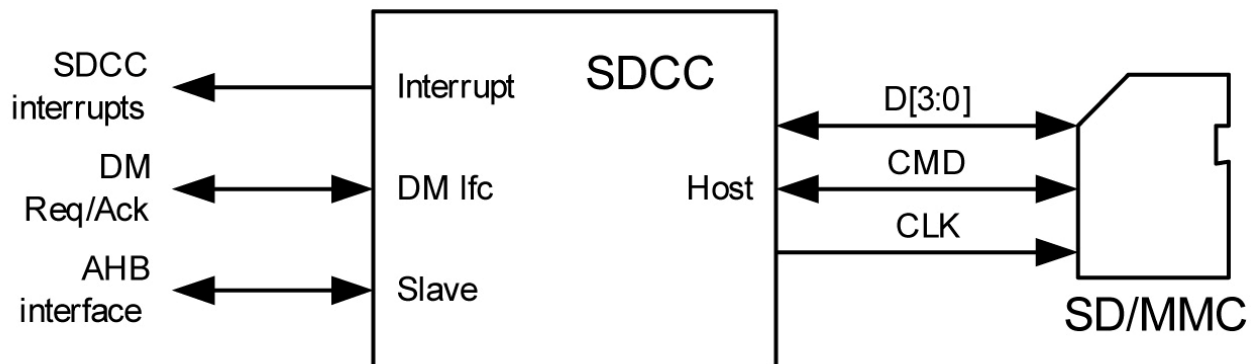


Figure 3–38 SDCC architecture

D. Pin Description

PIN	Symbol	Description
SDC1		
AA11	SDC1_DATA[3]	SDC1 data bit #3
AH8	SDC1_DATA[2]	SDC1 data bit #2
V13	SDC1_DATA[1]	SDC1 data bit #1
AD11	SDC1_DATA[0]	SDC1 data bit #0
AE10	SDC1_CMD	SDC1 command and response bit
AB11	SDC1_CLK	SDC1 clock

3. TECHNICAL BRIEF

■ Pin Description

PIN	Symbol	Description
SDC2		
AA13	SDC2_DATA[3]	SDC2 data bit #3
AE12	SDC2_DATA[2]	SDC2 data bit #2
V15	SDC2_DATA[1]	SDC2 data bit #1
V14	SDC2_DATA[0]	SDC2 data bit #0
AA12	SDC2_CMD	SDC2 command and response bit
AE11	SDC2_CLK	SDC2 clock
SDC3		
AB16	SDC3_DATA[3]	SDC3 data bit #3
AE16	SDC3_DATA[2]	SDC3 data bit #2
V16	SDC3_DATA[1]	SDC3 data bit #1
AD16	SDC3_DATA[0]	SDC3 data bit #0
AG16	SDC3_CMD	SDC3 command and response bit
AA16	SDC3_CLK	SDC3 clock
SDC4		
AE17	SDC4_DATA[3]	SDC4 data bit #3
AA18	SDC4_DATA[2]	SDC4 data bit #2
AG18	SDC4_DATA[1]	SDC4 data bit #1
V17	SDC4_DATA[0]	SDC4 data bit #0
AB24	SDC4_CMD	SDC4 command and response bit
AB25	SDC4_CLK	SDC4 clock

3. TECHNICAL BRIEF

E. USB

The universal serial bus (USB) is an interconnection standard widely supported by the electronic industry. The USB 2.0 spec defines data rates as low-speed (1.5 Mbps), full-speed (12 Mbps) and high-speed (480 Mbps).

The MSM7227 device contains a new USB high-speed function that is based on an embedded UTMI+core with a UTMI+ low pin interface (ULPI) compatible port. The MSM device's ULPI interface connects to an external ULPI PHY chip to complete the design. The ULPI core embedded in the MSM along with the PM7540 and a USB high-speed PHY IC provide support for the high-speed interface.

F. Pin Description

PIN	Symbol	Description
K1	USBH_CLK	Input clock from PHY
U7	USBH_DIR	Controls the direction of USBH_DATA. When high, data is driven into the MSM.
V12	USBH_NEXT	Used by the PHY to throttle data.
J8	USBH_STOP	Signals the end of a USB transmit packet or a register write operation, and optionally tops any receiver.
L14	USBH_DATA[7]	Bi-directional data pin
L13	USBH_DATA[6]	Bi-directional data pin
L12	USBH_DATA[5]	Bi-directional data pin
K8	USBH_DATA[4]	Bi-directional data pin
K7	USBH_DATA[3]	Bi-directional data pin
K5	USBH_DATA[2]	Bi-directional data pin
K4	USBH_DATA[1]	Bi-directional data pin
M12	USBH_DATA[0]	Bi-directional data pin

3. TECHNICAL BRIEF

G. Universal Asynchronous Receiver Transmitters

The MSM7227 is capable of providing up to four Universal Asynchronous Receiver Transmitter (UART) ports. Each MSM7227 UART communicates with serial data ports that conform to the RS-232 interface protocol.

Support for three UART interfaces in parallel with the following requirements:

- UART1: High speed, maximum of up to 4Mbps using the UART1DM data mover interface and up to 230 kbps for data services using the UART1 interface
- UART2DM: high speed maximum of up to 4Mbps using the data mover interface
- UART2: Maximum speed of 115 kbps
- UART3: Maximum speed of 115 kbps

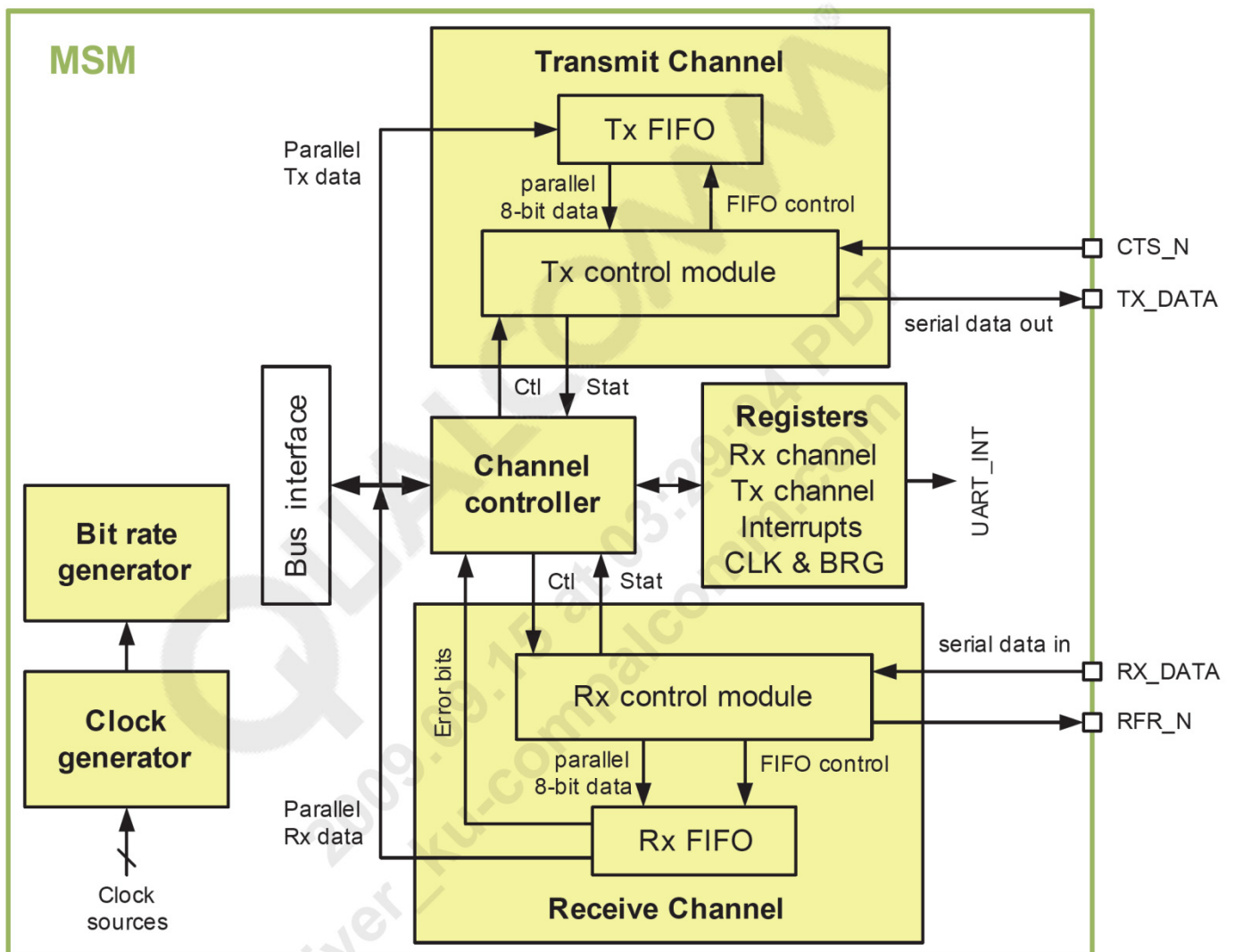


Figure 3-39 UART functional block diagram

3. TECHNICAL BRIEF

H. Pin Description

PIN	Symbol	Description
UART1 or UART1DM		
AA10	UART1_RFR_N	Ready for receiving
AG6	UART1_CTS_N	Clear to send
AB9	UART_RX_DATA	Receive serial data input
AA9	UART1_TX	Transmit serial data output
UART2DM		
AE17	UART1_RFR_N	Ready for receiving
AA18	UART1_CTS_N	Clear to send
AG18	UART_RX_DATA	Receive serial data input
V17	UART1_TX	Transmit serial data output
UART3		
AD8	UART1_RFR_N	Ready for receiving
AH6	UART1_CTS_N	Clear to send
AE8	UART_RX_DATA	Receive serial data input
AD9	UART1_TX	Transmit serial data output
UART4		
AC24	UART1_RFR_N	Ready for receiving
AE28	UART1_CTS_N	Clear to send
AC25	UART_RX_DATA	Receive serial data input
AD25	UART1_TX	Transmit serial data output

3. TECHNICAL BRIEF

I. USIM

The MSM7227 supports USIM interface. The PM7540 is recommended for implementing USIM interface. The PM7540 can support dual voltage cards (2.85V and 1.8V) and will perform all the necessary voltage translations to interface to the MSM7227 USIM slots.

J. Pin Description

PIN	Symbol	Description
UIM1		
AD8	UIM_CLK	Clock to the module
AH6	UIM_RESET	Reset to the module
AE8	UIM_PWR_EN	Power enable to the module
AD9	UIM_DATA	Data to/from the module
UIM2		
AC24	UIM2_CLK	Clock to the module
AE28	UIM2_RESET	Reset to the module
AC25	UIM2_PWR_EN	Power enable to the module
AD25	UIM2_DATA	Data to/from the module

3. TECHNICAL BRIEF

K. I2C interface

I2C is a two-wire bus for inter-IC communication that supports any IC fabrication process. Two wires, serial data (SDA) and serial clock (SCL), carry information between the connected devices. Each device is recognized by a unique address and can operate as either a transmitter or receiver, depending upon the device function.

■ Pin Description

PIN	Symbol	Description
Primary I2C bus		
V11	I2C_SCL	I2C serial clock (primary)
Y7	I2C_SDA	I2C serial data (primary)
Auxiliary I2C bus		
N5	AUX_I2C_SCL	I2C serial clock (auxiliary)
T11	AUX_I2C_SDA	I2C serial data (auxiliary)

3. TECHNICAL BRIEF

3.7 MCP memory

MCP memory: 4Gb NAND flash + 2Gb LP-DDR SDRAM

■ NAND Flash

I/O0– I/O7	Data input/output (X8 / X16)
I/O8– I/O15	Data input/output (X16)
AL	Address latch enable
CL	Command latch enable
CE	Chip enable
RE	Read enable
WE	Write enable
WP	Write protect
Vcc	Supply voltage
Vss	Ground

Table 3–3 Pins Description of NAND flash

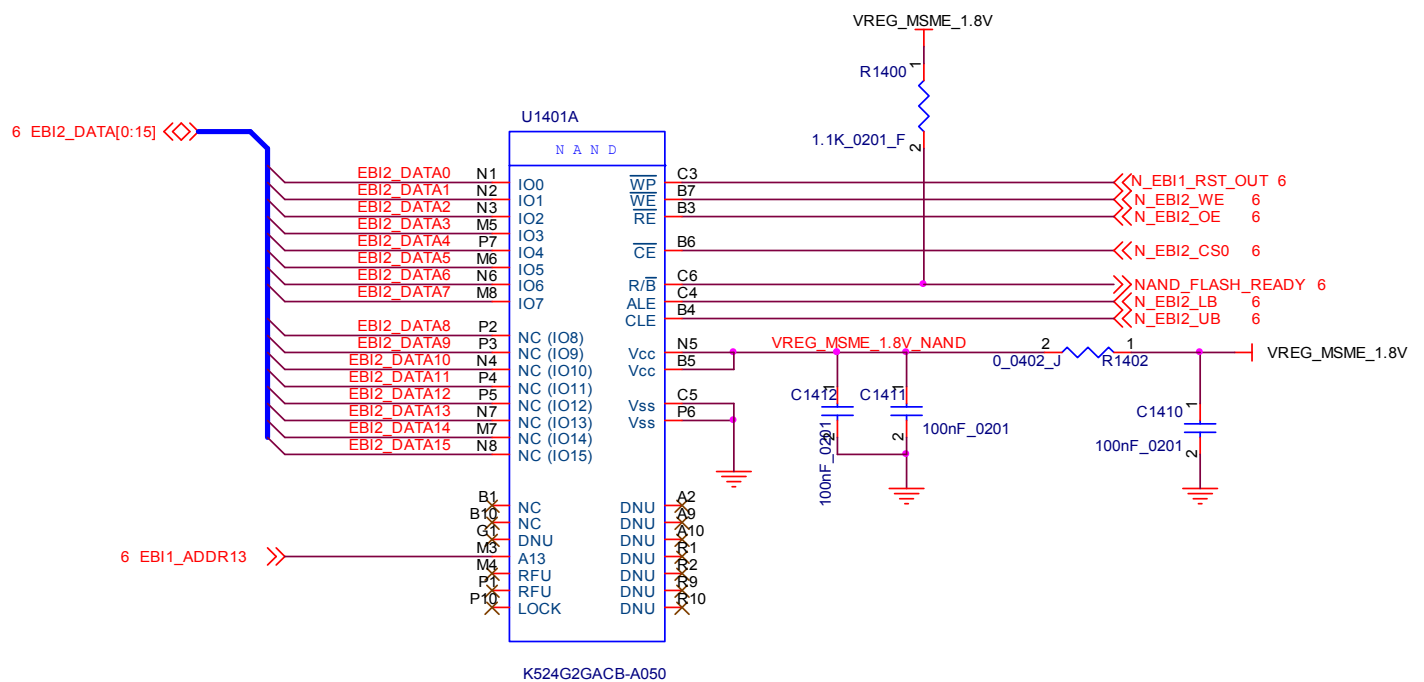


Figure 3–40 NAND flash circuit

3. TECHNICAL BRIEF

■ LP-DDR SDRAM

A0–Ax	Address input – A10 determines the precharge mode
BA0–BA1	Bank select inputs
DQ0–DQ15	Data input/outputs (X16/X32)
DQ16–DQ31	Data input/outputs (X32)
DQS0	Data read/write strobe for DQ0–DQ7
DQS1	Data read/write strobe for DQ8–DQ15
DQS2	Data read/write strobe for DQ16–DQ23
DQS3	Data read/write strobe for DQ24–DQ31
CK	Clock inputs
/CK	Clock inputs
CKE & CKE1	Clock enable input
/CS & /CS1	Chip select input
/RAS	Row address strobe input
/CAS	Column address strobe input
DQM0	DQ mask enable input controls DQ0–DQ7
DQM1	DQ mask enable input controls DQ8–DQ15
DQM2	DQ mask enable input controls DQ16–DQ23
DQM3	DQ mask enable input controls DQ24–DQ31
Vdd	Supply voltage
Vddq	Input/output supply voltage
Vss	Ground
Vssq	Input/output ground

Table 3–4 Pins Description of DDR SDRAM flash



3. TECHNICAL BRIEF

3.8 LG Display LCM

Parameter		Specification	Unit
Outline dimensions		54.3 (W) x 46.8 (H) x 1.7 (D)	mm
Main LCD Panel	Active area	48.96 (W) x 36.72 (H)	mm
	Viewing area	49.96 (W) x 37.72 (H)	mm
	Display format	320(W)xRGBx240(H)	
	Dot pitch	0.153 (W) x 0.153 (H)	mm

Table 3-5 LCM Mechanical Specification

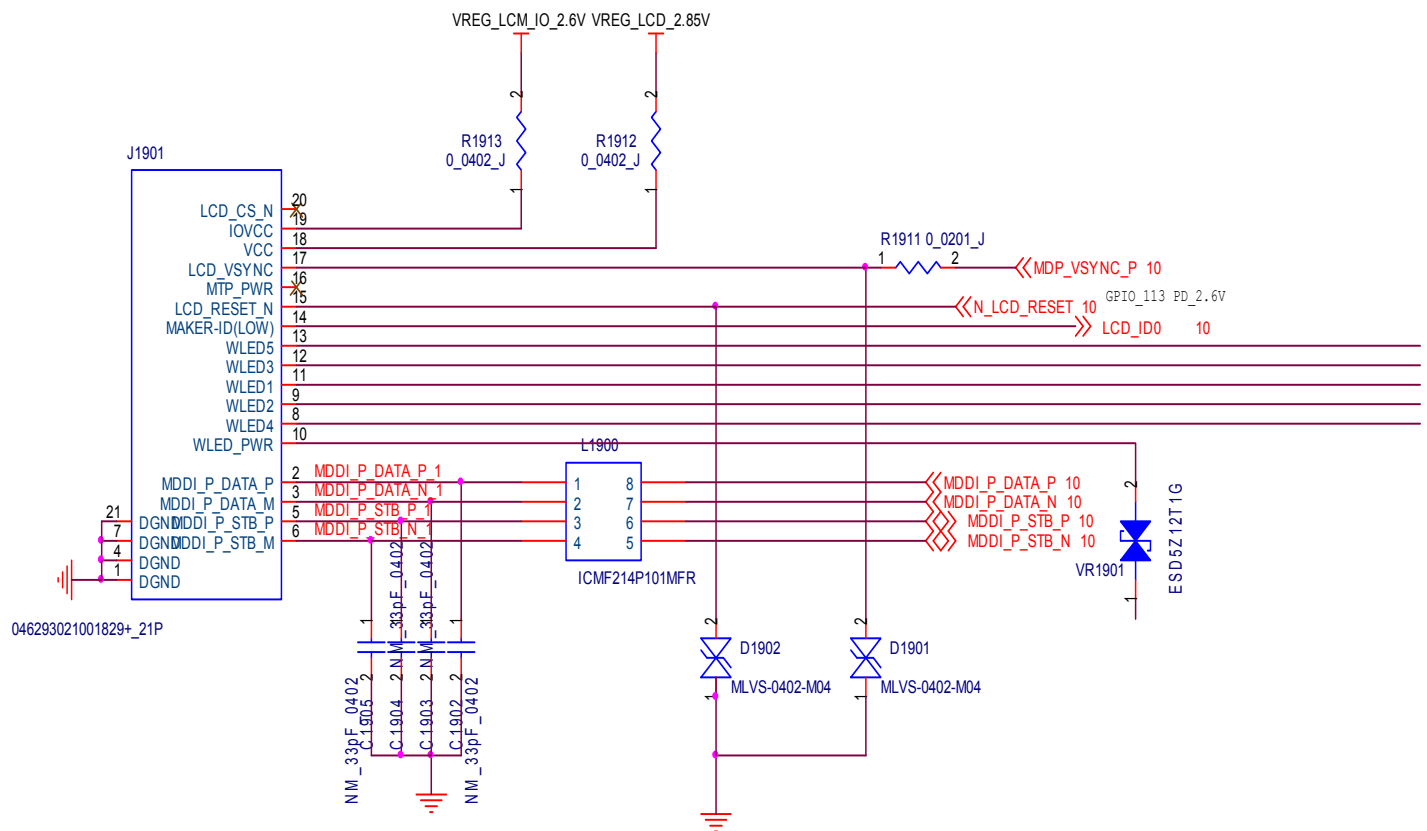


Figure 3-42 C570 LCM Circuit

3. TECHNICAL BRIEF

Symbol	Description
GND	Ground
MDDI_P_DATA_P	MDDI data signal line (+)
MDDI_P_DATA_M	MDDI data signal line (-)
GND	Ground
MDDI_P_STB_P	MDDI strobe signal line (+)
MDDI_P_STB_M	MDDI strobe signal line (-)
GND	Ground
WLED4	LED cathode
WLED2	LED cathode
WLED_PWR	LED anode
WLED1	LED cathode
WLED3	LED cathode
WLED5	LED cathode
MARK_ID	Ground
LCD_RESET_N	Hardware Reset
MTP_PWR	OPEN
LCD_VSYNC	Frame signal out
DVDD_2.8V	AMP power
DVDDIO_1.8V	Interface power
LCD_CS_N	LCD chip select
GND	Ground

Table 3-6 LCM Pins description

3. TECHNICAL BRIEF

3.9 VGA CCM

C570 supports VGA and 2M camera. VGA camera is for Video call and 2M camera is for picture.

■ VGA CCM

Module Specification	
Size (LWH/mm)	4±0.1 X 4±0.1 X 2.157±0.1
Image sensor	TOSHIBA 1/10" CMOS sensor
Full resolution	648 X 492 (VGA)
Output format (8bit)	YUV 422, RAW
Maximum image frame rate	30fps for VGA (640X480)
	60fps for QVGA (320X240)
scan mode	Progressive
Pixel size	2.2 um X 2.2 um

Table 3-7 VGA CCM mechanical specification

VGA camera Address: 7Ch

VGA Camera TOSHIBA

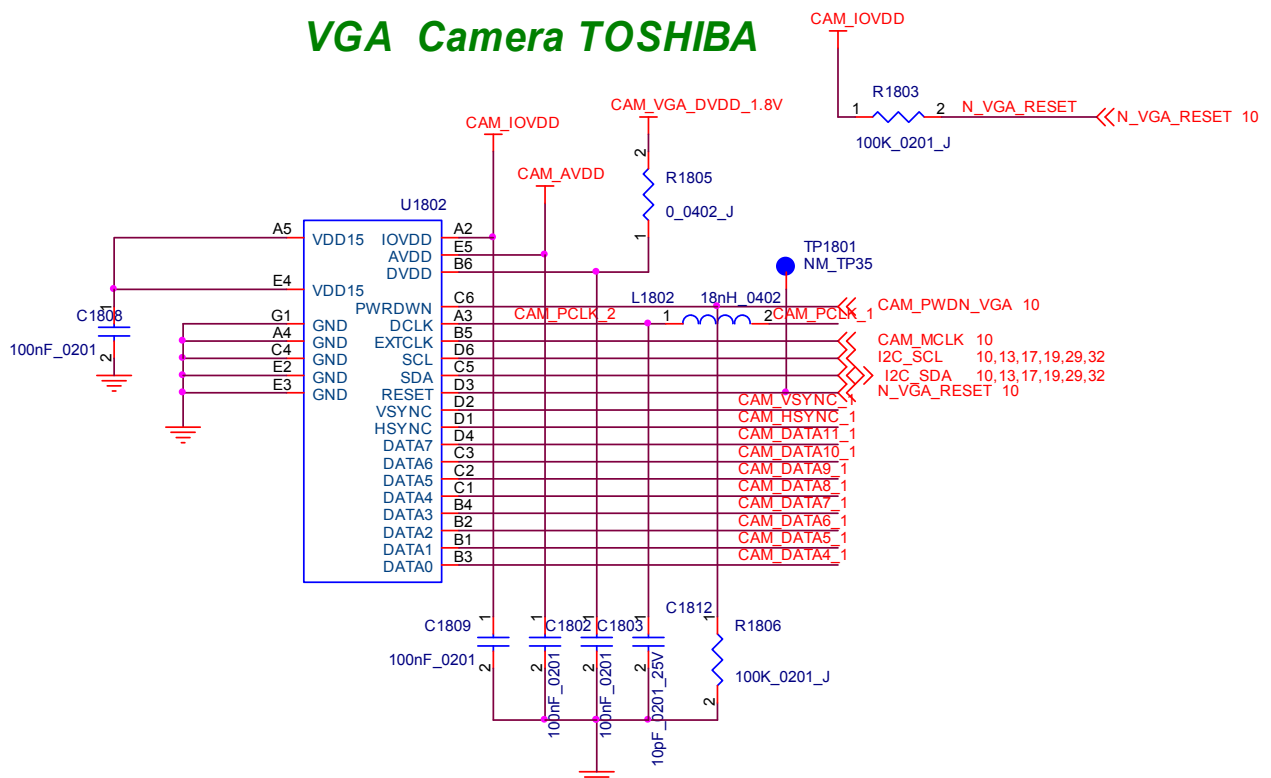
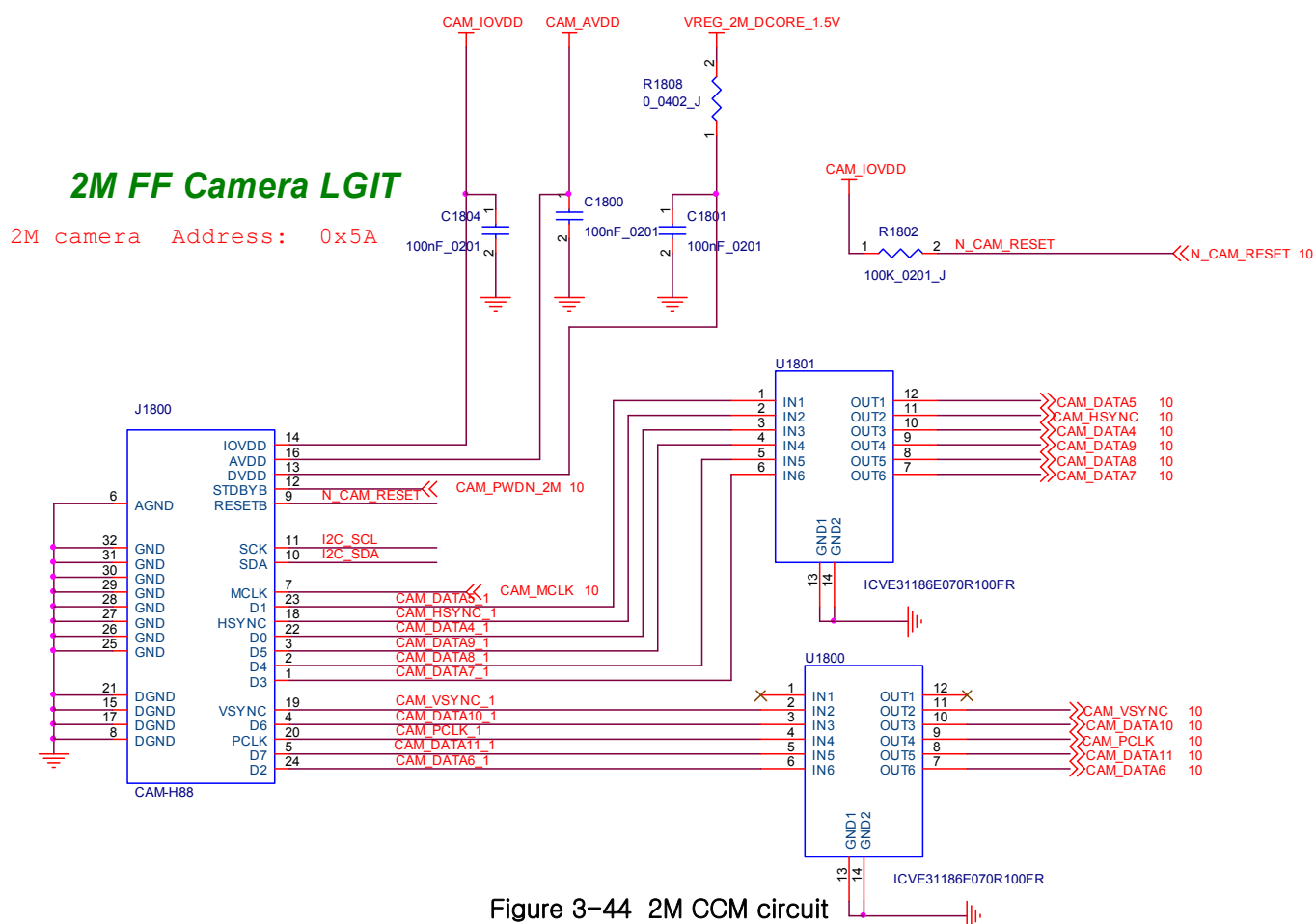


Figure 3-43 VGA CCM circuit

3. TECHNICAL BRIEF

Symbol	Description
SDA	Input/output data for I2C
SCL	input clock for I2C
PWRDWN	power down signal input
AVDD	Analog power
GND	System ground
IOVDD	I/O power
VDD15	Capacitor connector for internal regulator
DATA1	Image data output[1]
DATA5	Image data output[5]
DATA2	Image data output[2]
DATA3	Image data output[3]
D0VDD	Digital video port bit[0]
DVDD	Digital power
DATA4	Image data output[4]
EXTCLK	Data clock output
DATA6	Image data output[6]
DATA7	Image data output[7]
DCLK	Data clock output
VSYNC	Vertical reference output
HSYNC	Horizontal reference output

Table 3–8 VGA CCM Pins description



3. TECHNICAL BRIEF

Symbol	Description
IOVDD	Power for I/O circuit.
SCK	I2C clock
SDA	I2C data
STDBYB	power down active high
AGND	Analog ground
AVDD	Analog power
HSYNC	Horizontal reference output
D8	Digital video port bit[8]
D6	Digital video port bit[6]
D4	Digital video port bit[4]
D2	Digital video port bit[2]
D0	Digital video port bit[0]
DGND	Digital ground
DVDD	Power for digital core
PCLK	Pixel clock output
D1	Digital video port bit[1]
D3	Digital video port bit[3]
D5	Digital video port bit[5]
D7	Digital video port bit[7]
DGND	Digital ground
D9	Digital video port bit[9]
VSYNC	Vertical sync output
MCLK	Master input clock
RESETB	Reset (Active Low)

Table 3–10 2M CCM pins description



3. TECHNICAL BRIEF

3.12 Optical Joystick

To be a PDA phone, C570 also supports the directional device, which uses optical joystick. Optical joystick is specifically designed for wireless mobile application. It can control the clock & data via I2C interface.

Optic joystick B2B connector

OJ module Address: 0x33

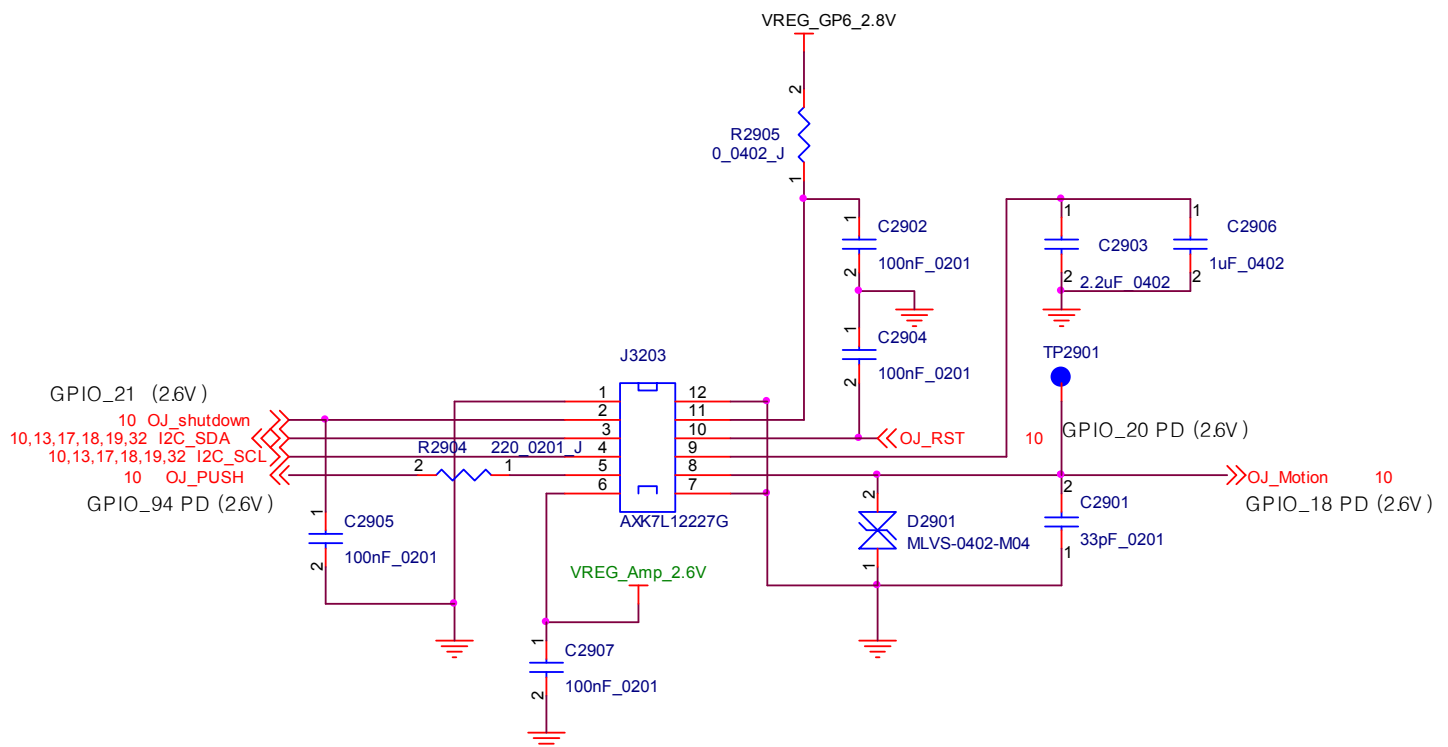


Figure 3-46 optical joystick circuit

3. TECHNICAL BRIEF

The following is block diagram of optical sensor. It connects PCB via B2B connector.

FLEXIBLE PCB include I2C sensor

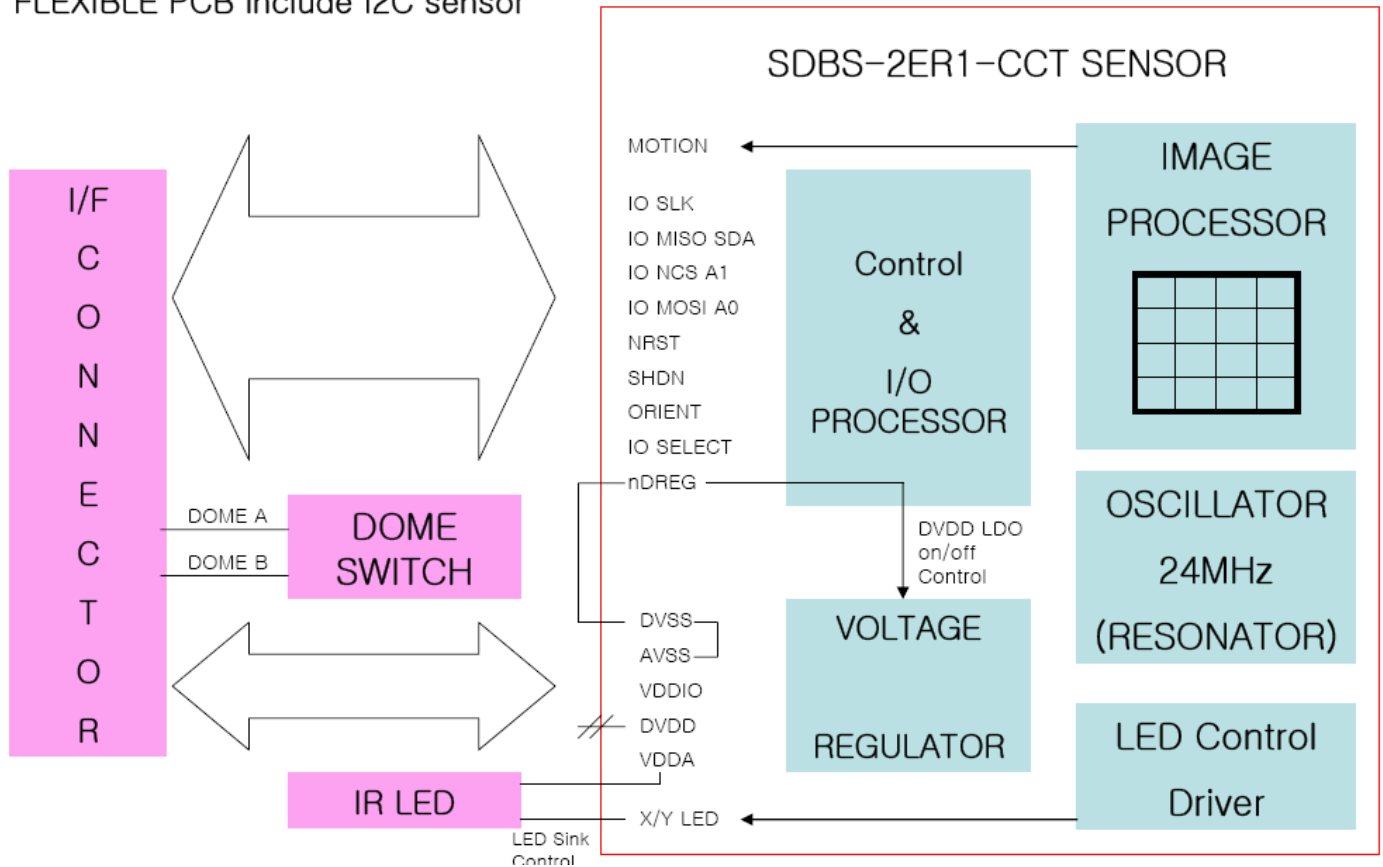


Figure 3-47 optical joystick block diagram

3.13 LCM backlight and keypad light

3. TECHNICAL BRIEF

Symbol	description
VOUT	Charge pump output
VIN	Input voltage 2.5v to 5.5v
SCL	I2C interface
SDA	I2C interface
nRST	HW reset (active low)
nINT	Comparator input for Phototransistor (not used)
DS1	Current sink inputs for LCM backlight
DS2	Current sink inputs for LCM backlight
D1	Current sink inputs for LCM backlight
D2	Current sink inputs for LCM backlight
D3	Current sink inputs for LCM backlight
D4	Current sink inputs for LCM backlight
D5	Current sink inputs for LCM backlight
D6	Current sink inputs for LCM backlight
GND	Ground
C1N	Connect to the flying capacitor C1
C2P	Connect to the flying capacitor C2
C2N	Connect to the flying capacitor C2
C1P	Connect to the flying capacitor C1

Table 3–11 ADP8860 pins description

3. TECHNICAL BRIEF

3.14 Side key and Qwerty key

C570 has four side keys and 43key Qwerty keypad. The four side keys are Function key, camera key, volume up and volume down key.

■ Side key

- Function key (N_Function_KEY) : Connect to PM7227 GPIO29
- Camera key (KEY_CAMERA) : Connect to MSM7227 LCD I/F
- Volume up (KEY_VOL_UP) : Connect to MSM7227 UART2
- Volume down (KEY_VOL_DOWN) : Connect to MSM7227 GPIO114

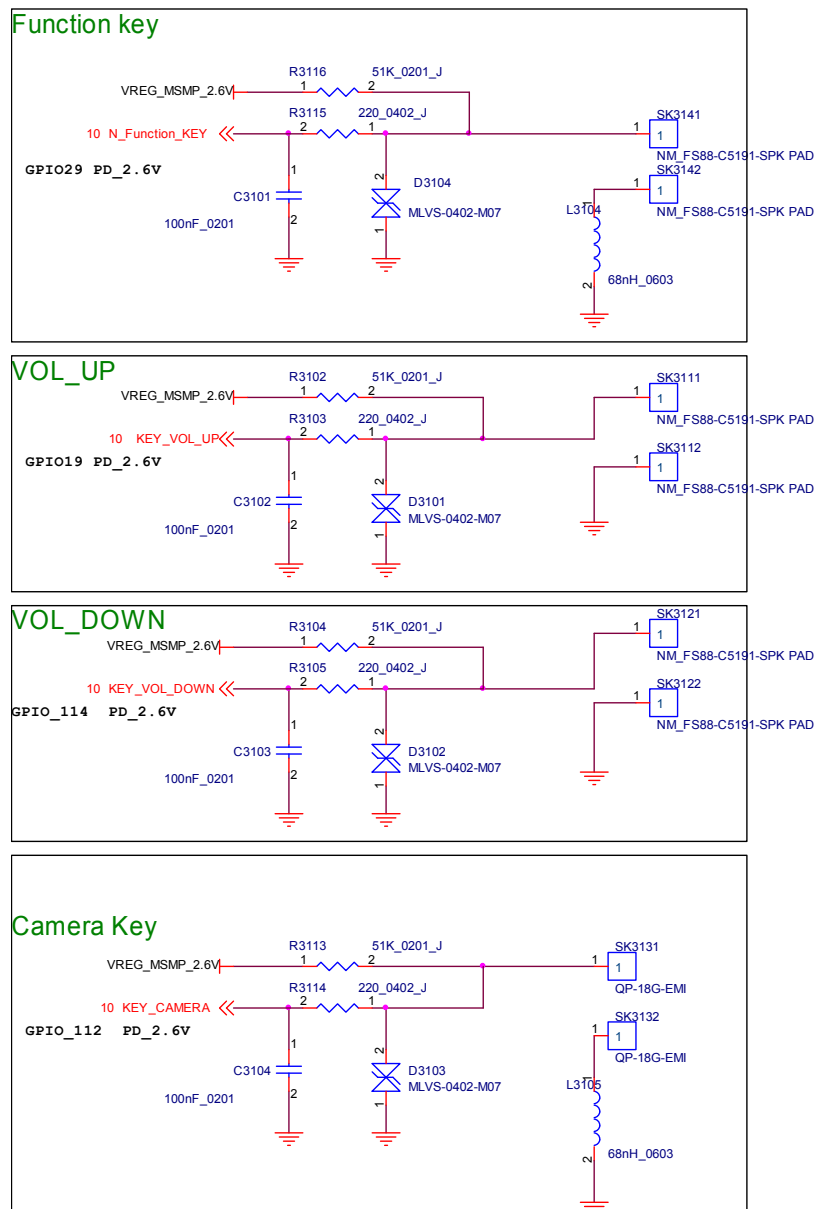


Figure 3-49 Side key circuit

3. TECHNICAL BRIEF

■ QWERTY key

Use 7X7 key matrix as shown below.

	COL1	COL2	COL3	COL4	COL5	COL6	COL7
ROW1	LSK		RSK	P	<==	Enter	
ROW2	Home				Back	O	L
ROW3	Send			I	K	M	■
ROW4	Fn	W	E	R	T	Y	U
ROW5		S	D	F	G	H	J
ROW6	Sym	Z	X	C	V	B	N
ROW7		A		Space	Q	,	

Send		LSK		OJ Up				RSK		End/ Power on
		OJ Left		OJ Push		OJ Right				
		Home		OJ Down				Back		
Q ~	W !	E \$	R 1	T 2	Y 3	U *	I /	O -	P +	
A ^	S (	D)	F 4	G 5	H 6	J #	K =	L "	<== DEL	
Z &	X :	C ;	V 7	B 8	N 9	M 0	, ?	. '	Enter	
CAPS 	Fn	Sym @	Space							

Table 3-12 7X7 key matrix

3. TECHNICAL BRIEF

3.15 USB PHY

C570 need to support high speed USB, but because PM7540 just only support up to full speed USB, so we use the integrated high speed USB transceiver for supporting high speed USB.

The high-speed USB module contains an embedded UTMI+ core with a built-in transceiver eliminating the need for an external PHY. Two additional pins are required for PHY operations which includes an external reference resistor pin (USBPHY_REXT) and a USB system clock pin (SYS_CLK). This interface and architecture is Shown below.

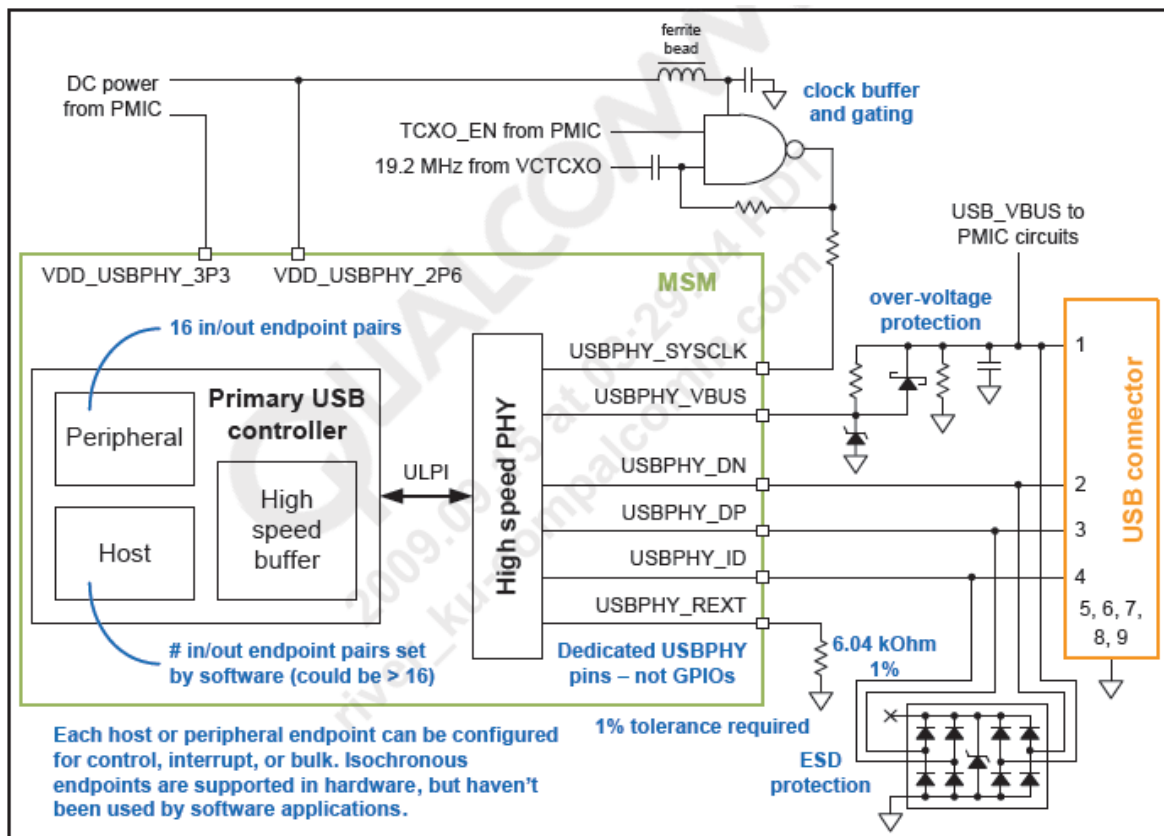


Table 3-13 MSM7227 integrated USB PHY connection & architecture

3. TECHNICAL BRIEF

3.16 T-Flash

C570 supports T-Flash memory card. The T-Flash's power source is from VREG_TFLASH_H_3V (PM7540. VREG_MMC). The card detection is N_SDC1_CD signal (MSM7227. GPIO92).

N_SDC1_CD signal	T-Flash status
High	Normal status. (T-Flash un-plug in)
Low	T-flash plug in

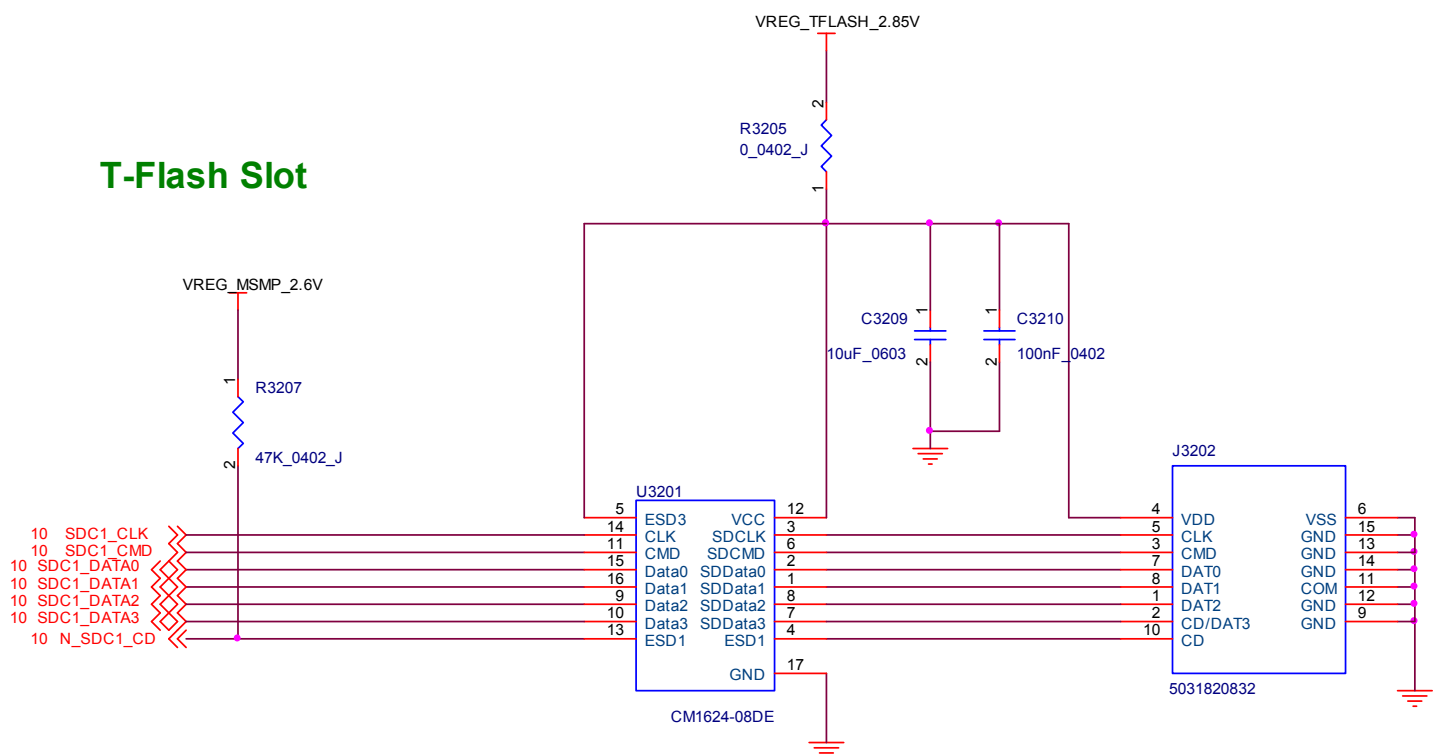


Figure 3-50 T-Flash circuit

3. TECHNICAL BRIEF

3.17 USIM

Symbol		Description
PM7540. VREG_RUIM	VREG_RUIM	USIM power
PM7540. MPP6	RUIM_P_RST	USIM reset pin, connect to USIM slot
PM7540. MPP10	RUIM_P_CLK	USIM clock pin, connect to USIM slot
PM7540. MPP12	RUIM_IO	USIM data pin, connect to USIM slot
PM7540. MPP5	RUIM_M_RST	USIM reset pin, connect to MSM7227 USIM1 interface
PM7540. MPP9	RUIM_M_CLK	USIM clock pin, connect to MSM7227 USIM1 interface
PM7540. MPP11	RUIM_M_IO	USIM data pin, connect to MSM7227 USIM1 interface

Table 3–15 USIM pins description

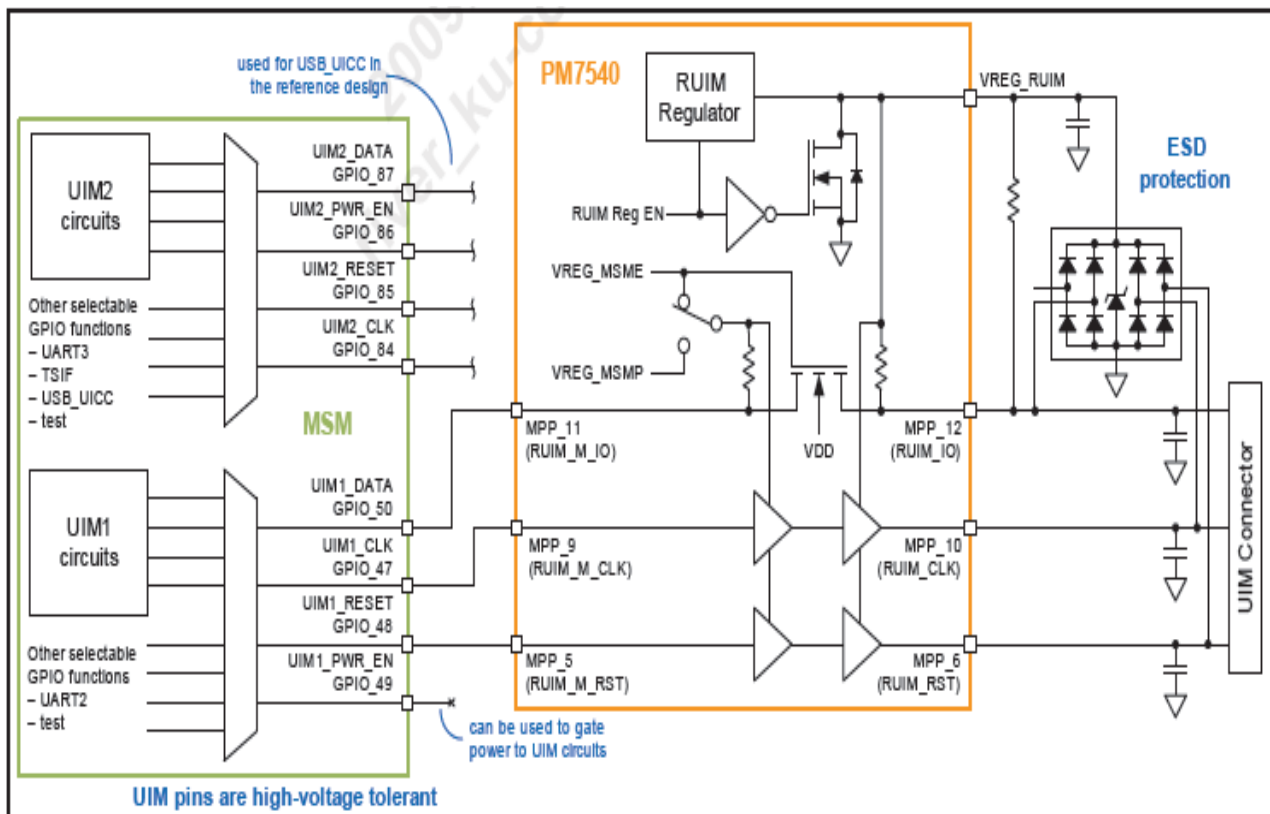
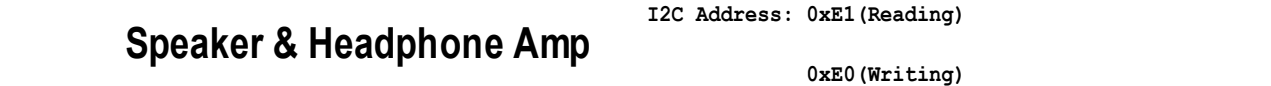


Figure 3–51 USIM connector with PM7540 level translations



3. TECHNICAL BRIEF

3.19 Internal Micphone

C570 has build in micphone, which is SMT type. The micphone signals (MIC1_P and MIC1_M) are directly from MSM7227 internal codec interface to micphone set.

MICROPHONE

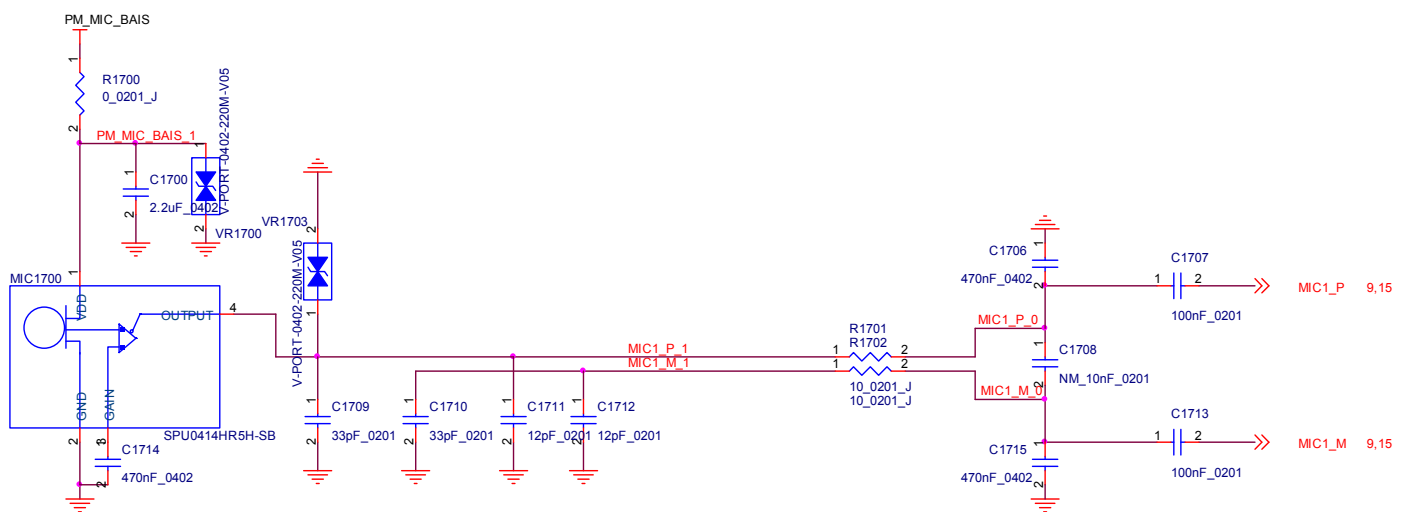


Figure 3-53 Micphone circuit

3. TECHNICAL BRIEF

3.21 3.5mm Ear-Mic with send/end key

C570 supports 3.5mm ear-mic with send/end key. We can utility MICBIAS to detect send/end key function. While headset is plug-in, STEREO_EN is short to GND. Then STEREO_EN pulls low. Instead, STEREO_EN pulls high while the headset is unplugged .

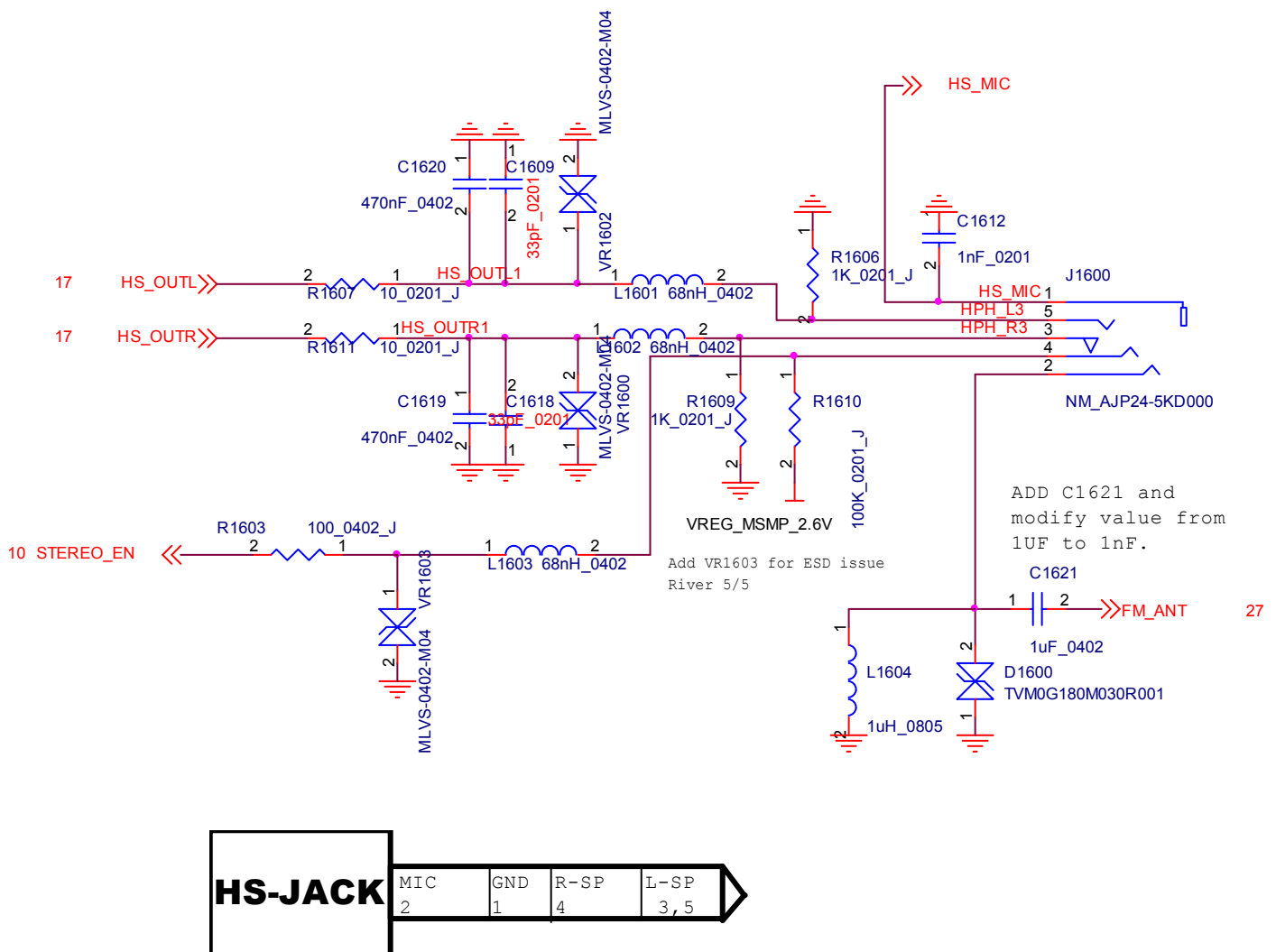


Figure 3–55 microphone circuit of 3.5mm ear-mic

3. TECHNICAL BRIEF

3.22 Main battery

C570 main battery is smart battery, which includes gas gauge IC.

Battery Gauging Address 0X6C

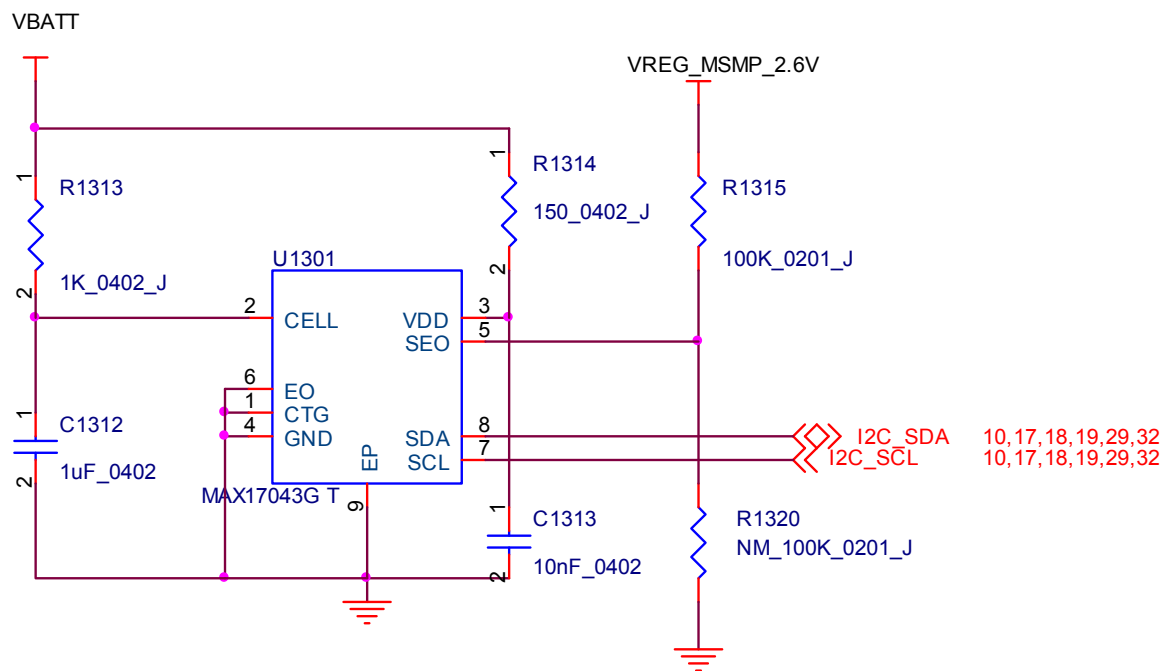


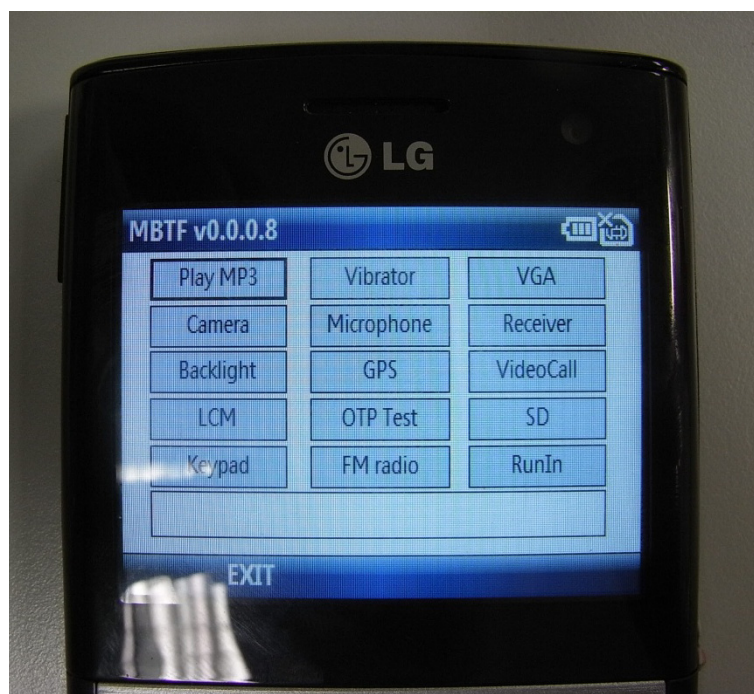
Figure 3–56 C570 gas gauge circuit

4 HW Trouble Shooting

C570 HW Trouble Shooting Guide

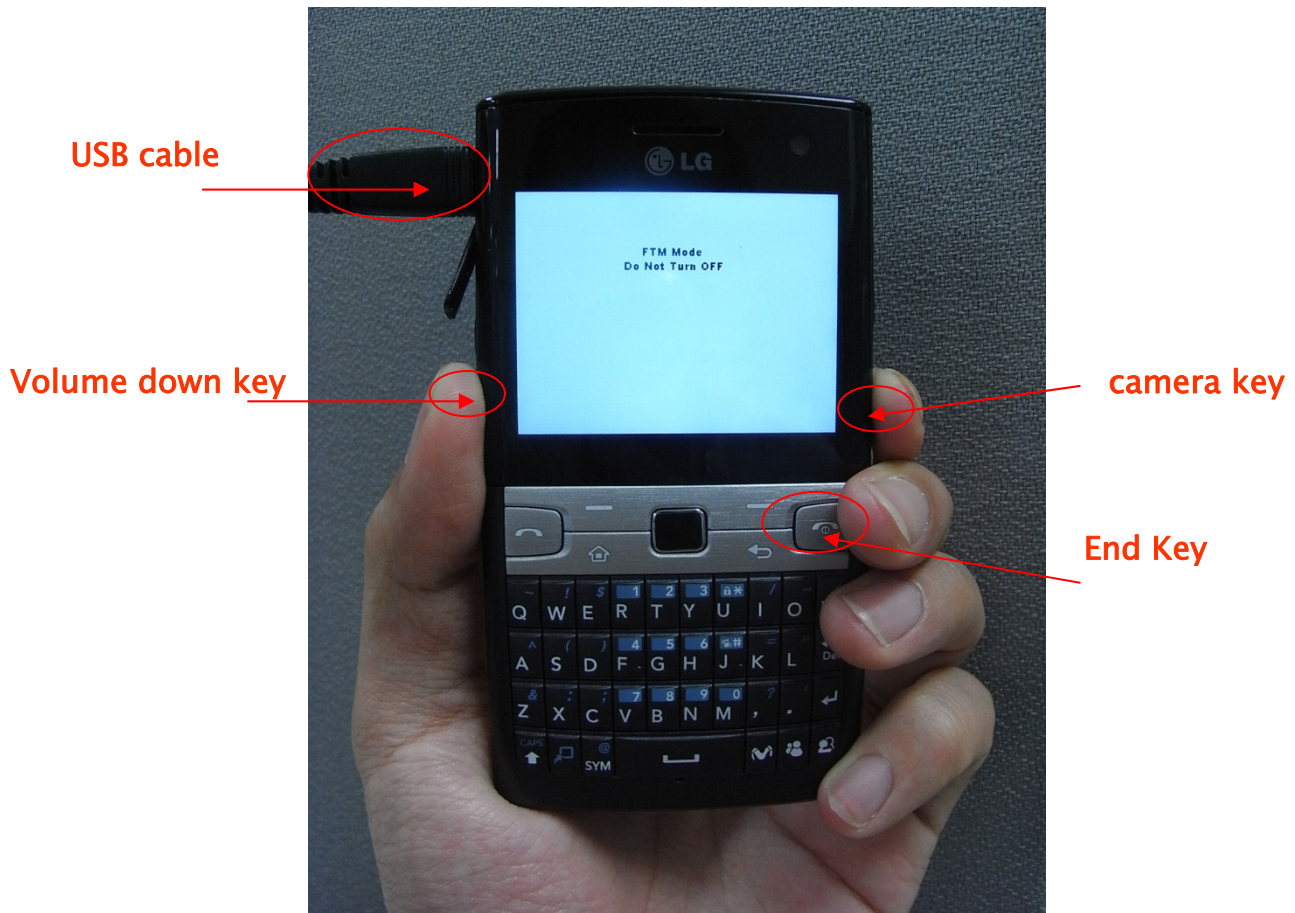
4.1 HW Function Check

Type #77763# then press "Send key"



RUN in : Auto execute the function test.

4.2 FTM Mode in Board Level



FTM mode in board level:

1. Provide power source.
2. Press camera key, volume down key.
3. Press End key
3. Entry the FTM mode.
4. Then insert the USB cable.

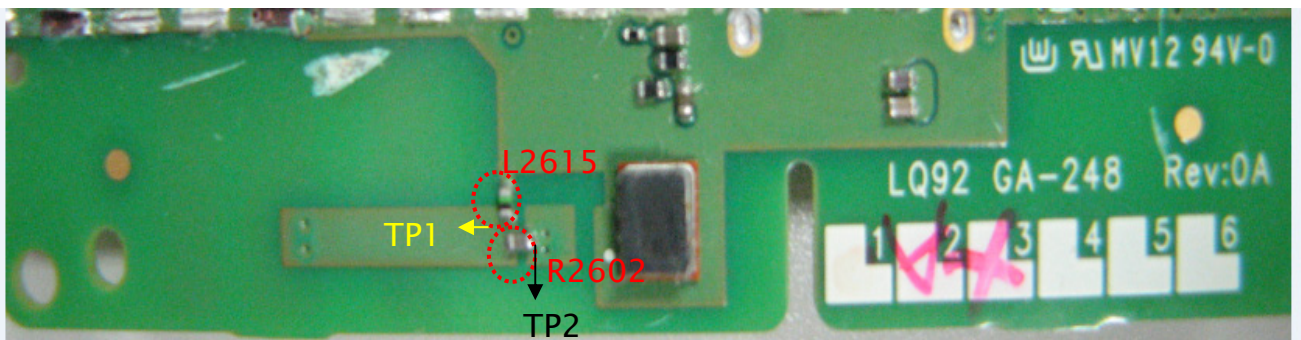
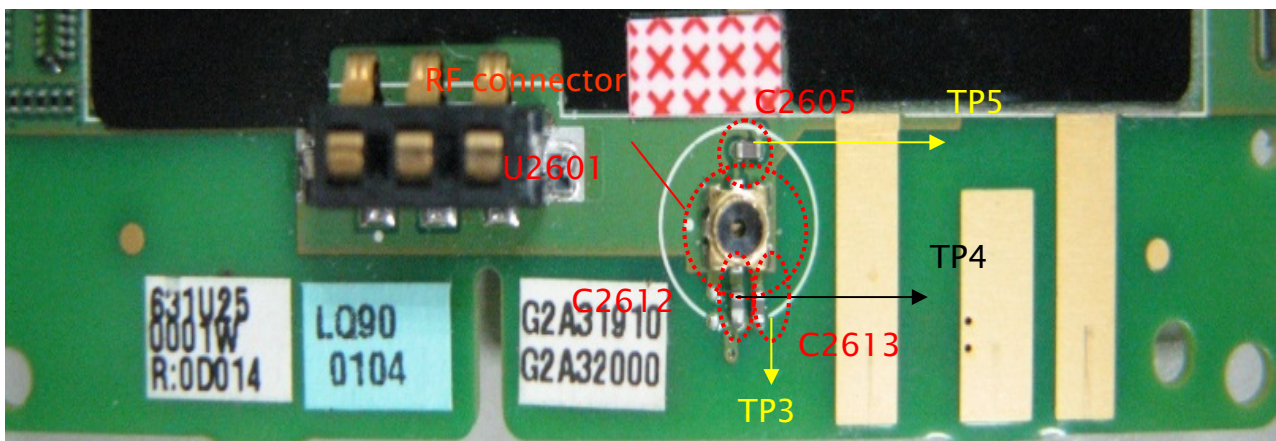
HW TROUBLE SHOOTING

4.3 Wireless Trouble

Antenna and antenna matching affect WCDMA and GSM wireless performance.

Picture Data

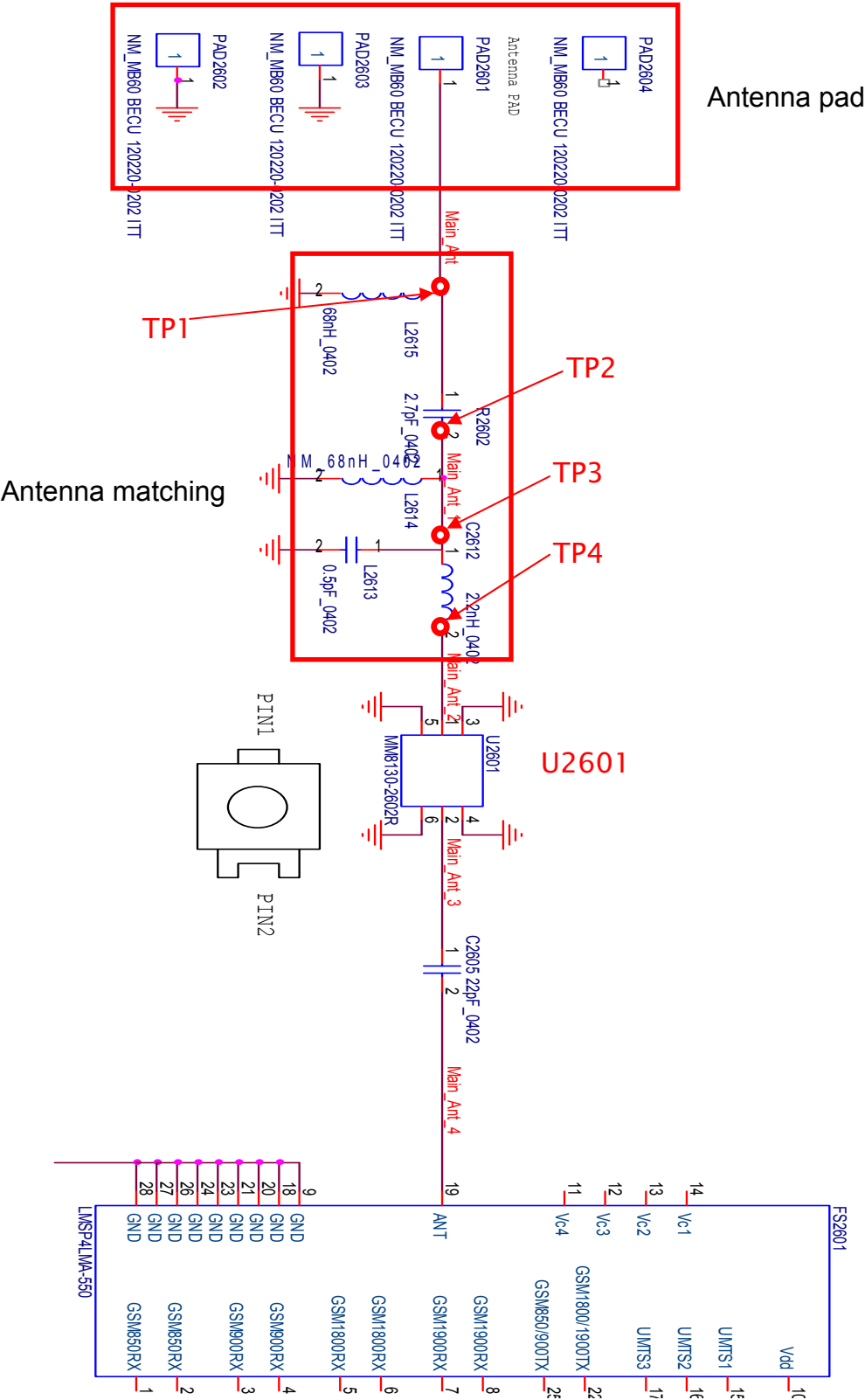
Main board top



Wireless Trouble

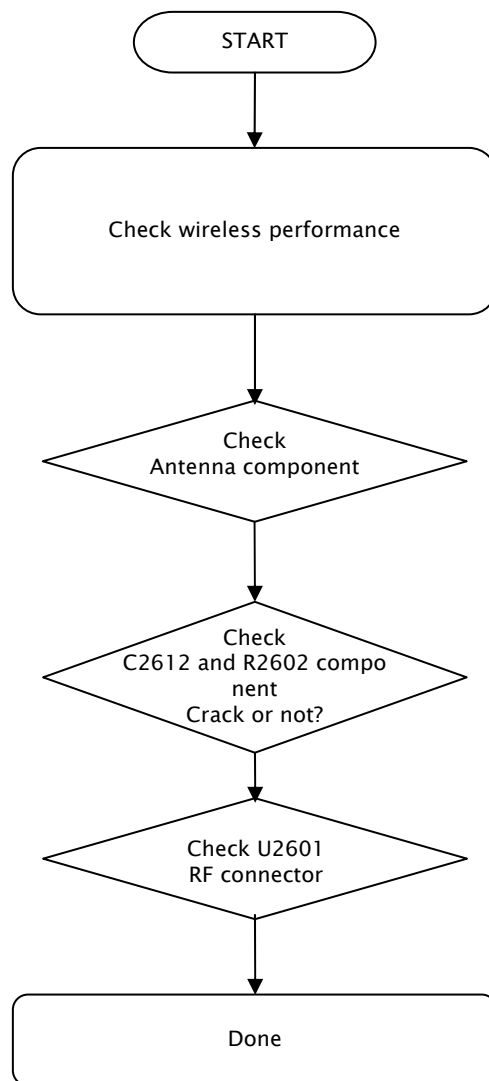
Circuit Diagram

Main Board



Wireless Trouble

Checking Flow



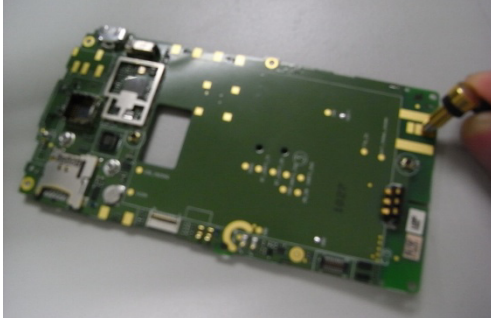
RF TROUBLE SHOOTING

Wireless Trouble

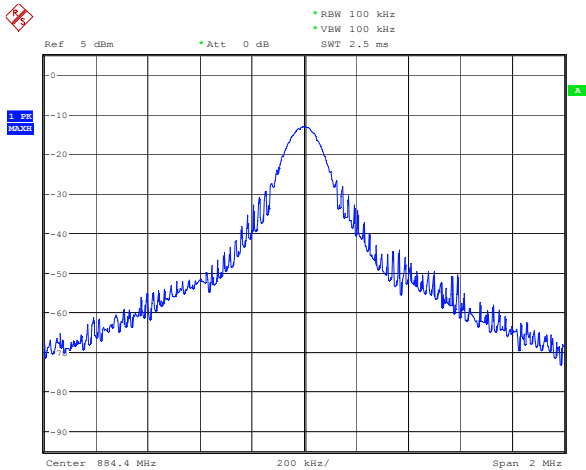
Waveform

Feed CW waveform to TP1 and measure Antenna's trace waveform.

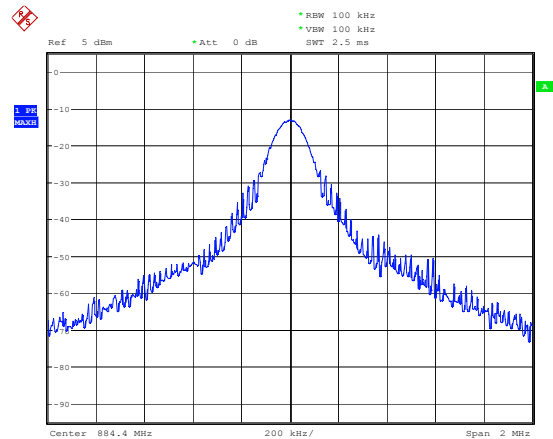
TP1



TP2: check FC8



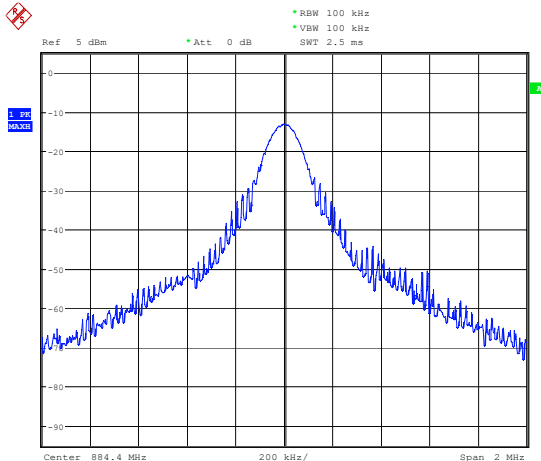
TP3: check FC7



Date: 17.NOV.2009 04:02:53

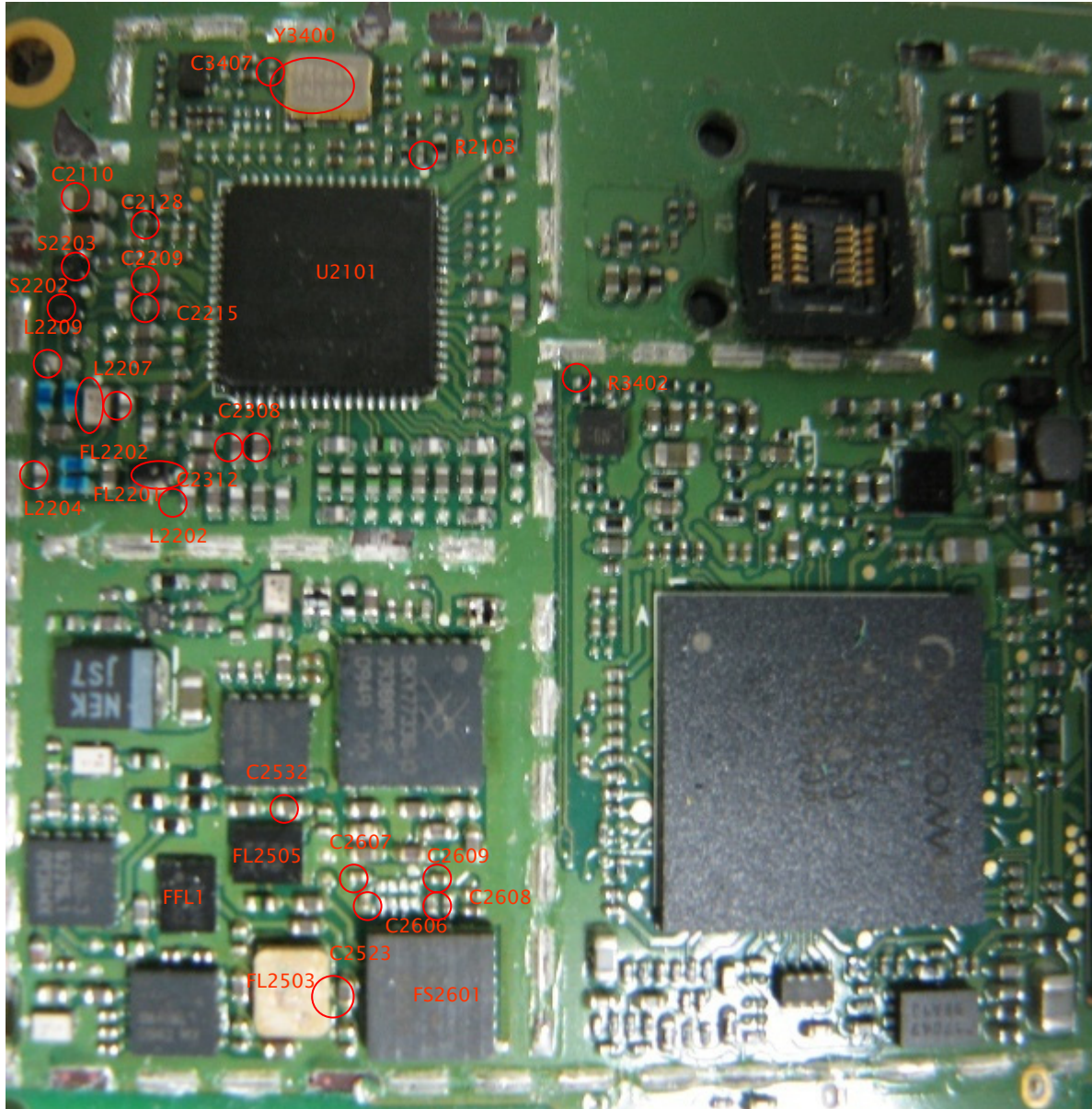
Date: 17.NOV.2009 04:02:53

TP4 : check FJP2



FJP2 also can be checked from DC resistance between TP3 and TP4 and it should be smaller than 1 ohm.

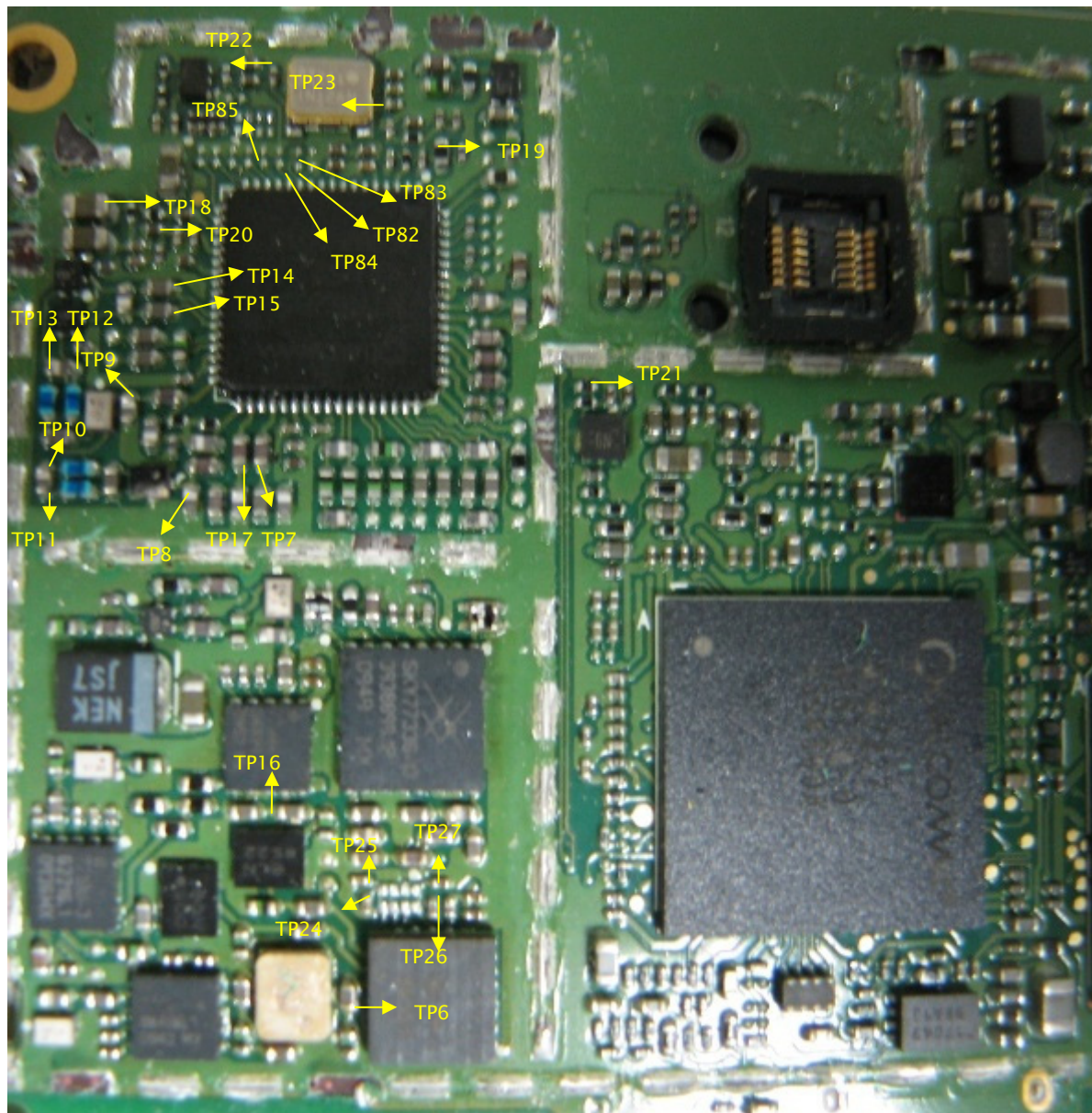
Date: 17.NOV.2009 04:02:53



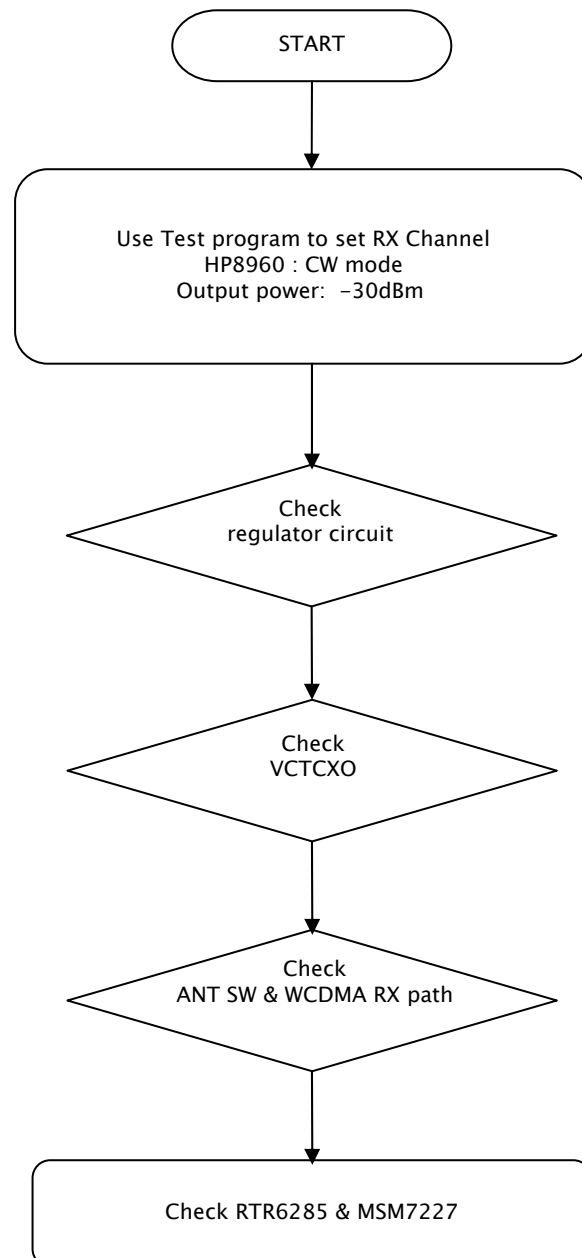
WCDMA1900/WCDMA2100 RX Trouble

Picture Data

Main board top

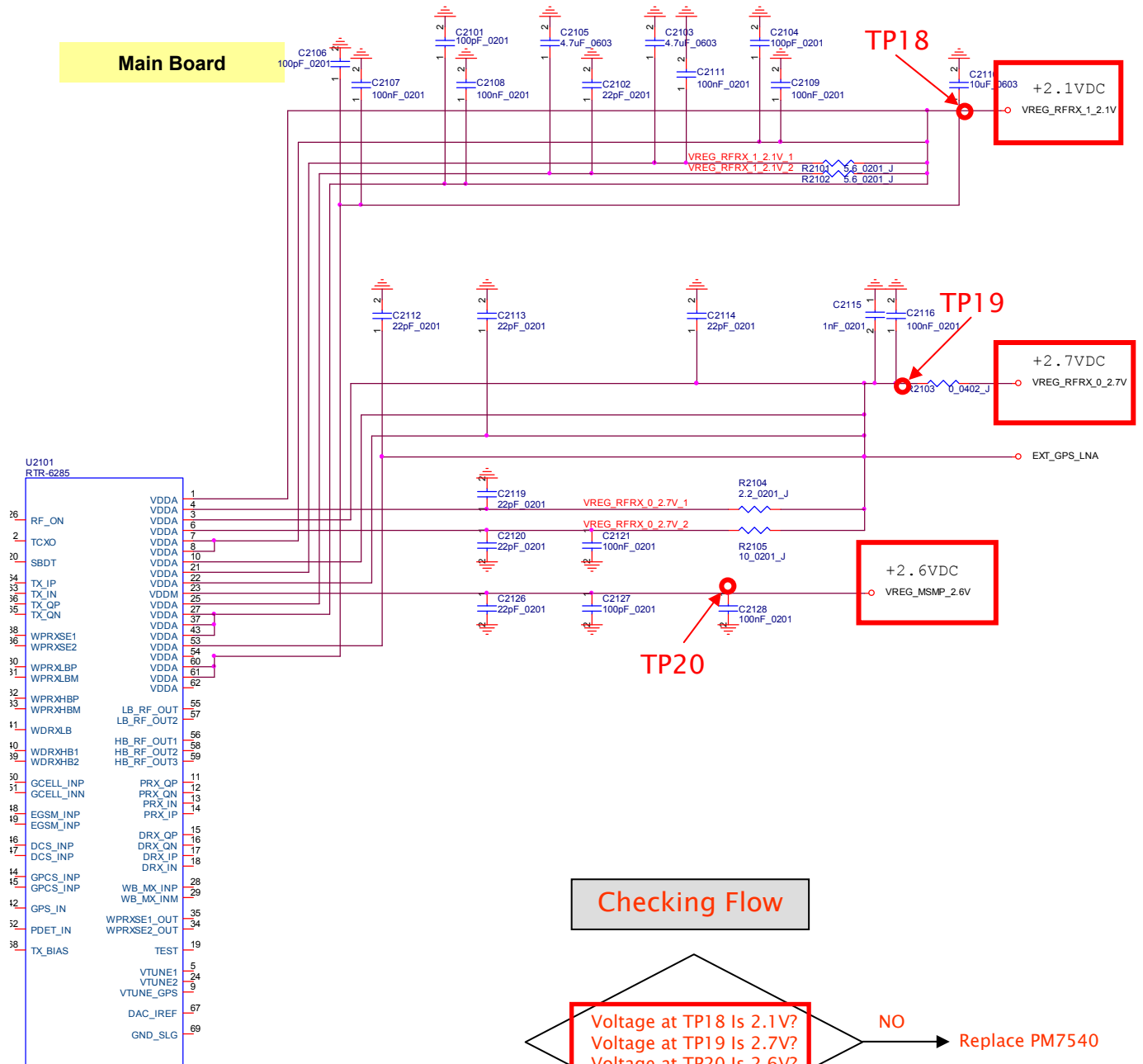


Checking Flow



(1) Checking Regulator Circuit

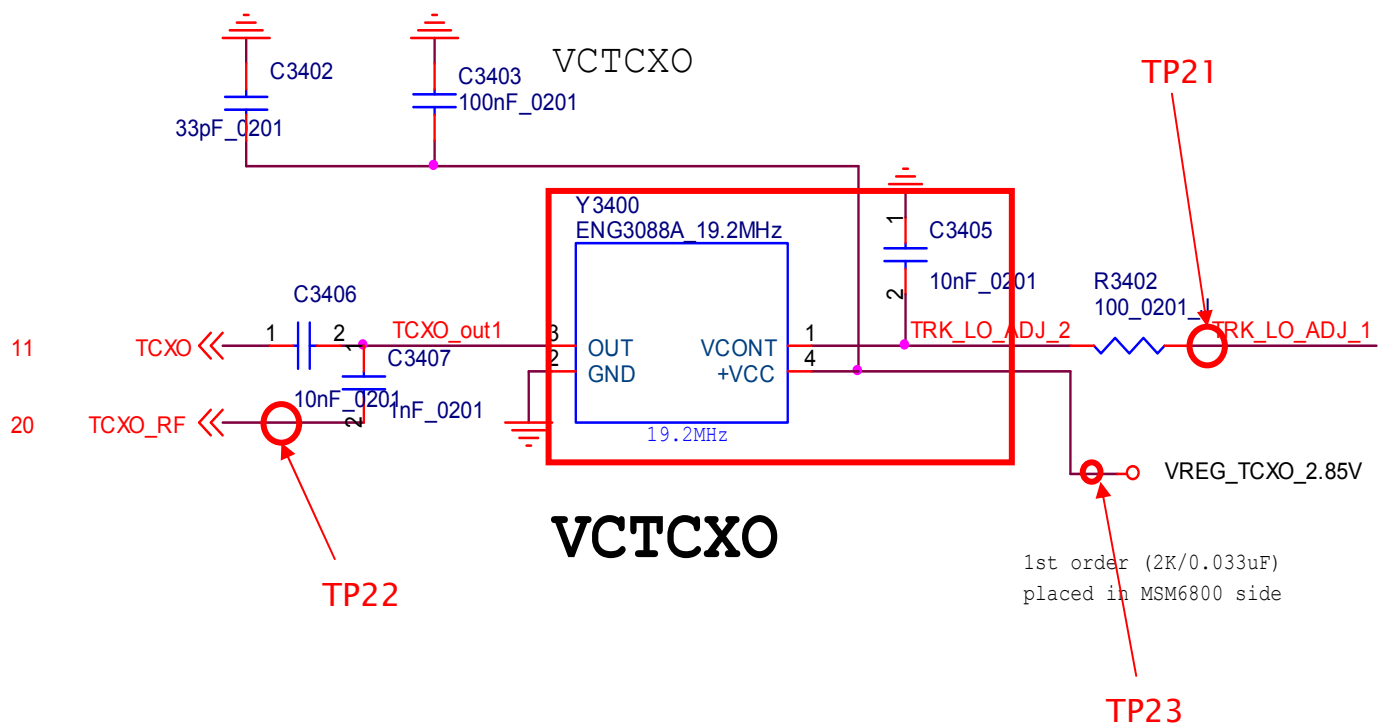
Circuit Diagram



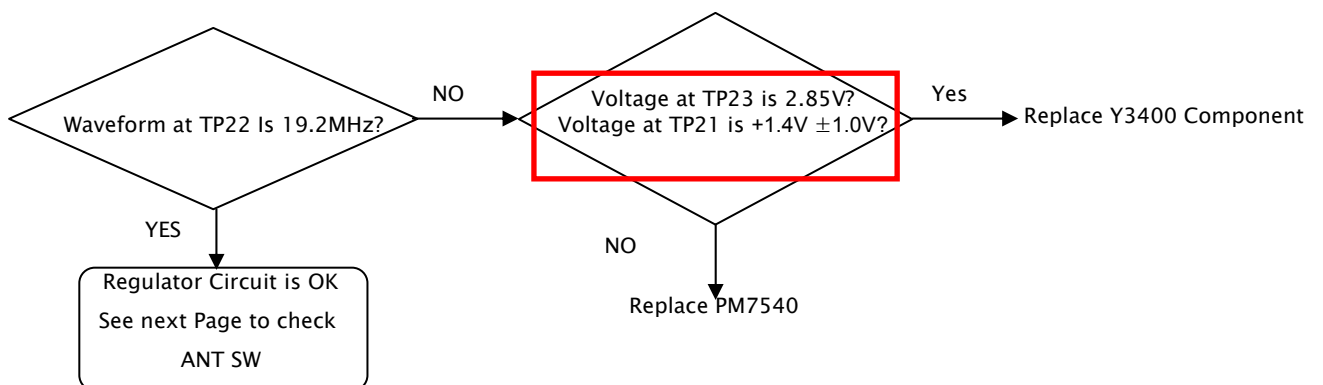
(2) Check VCTCXO

Circuit Diagram

Main Board



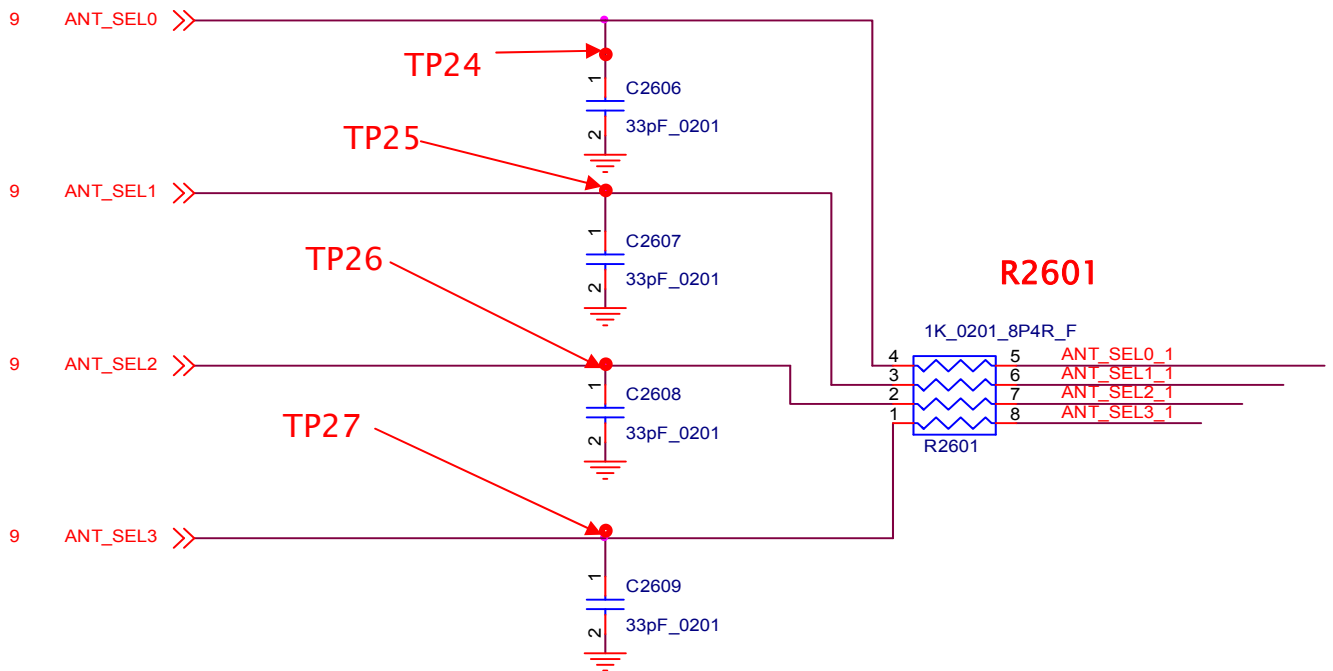
Checking Flow



(3) Checking Ant SW & RX path

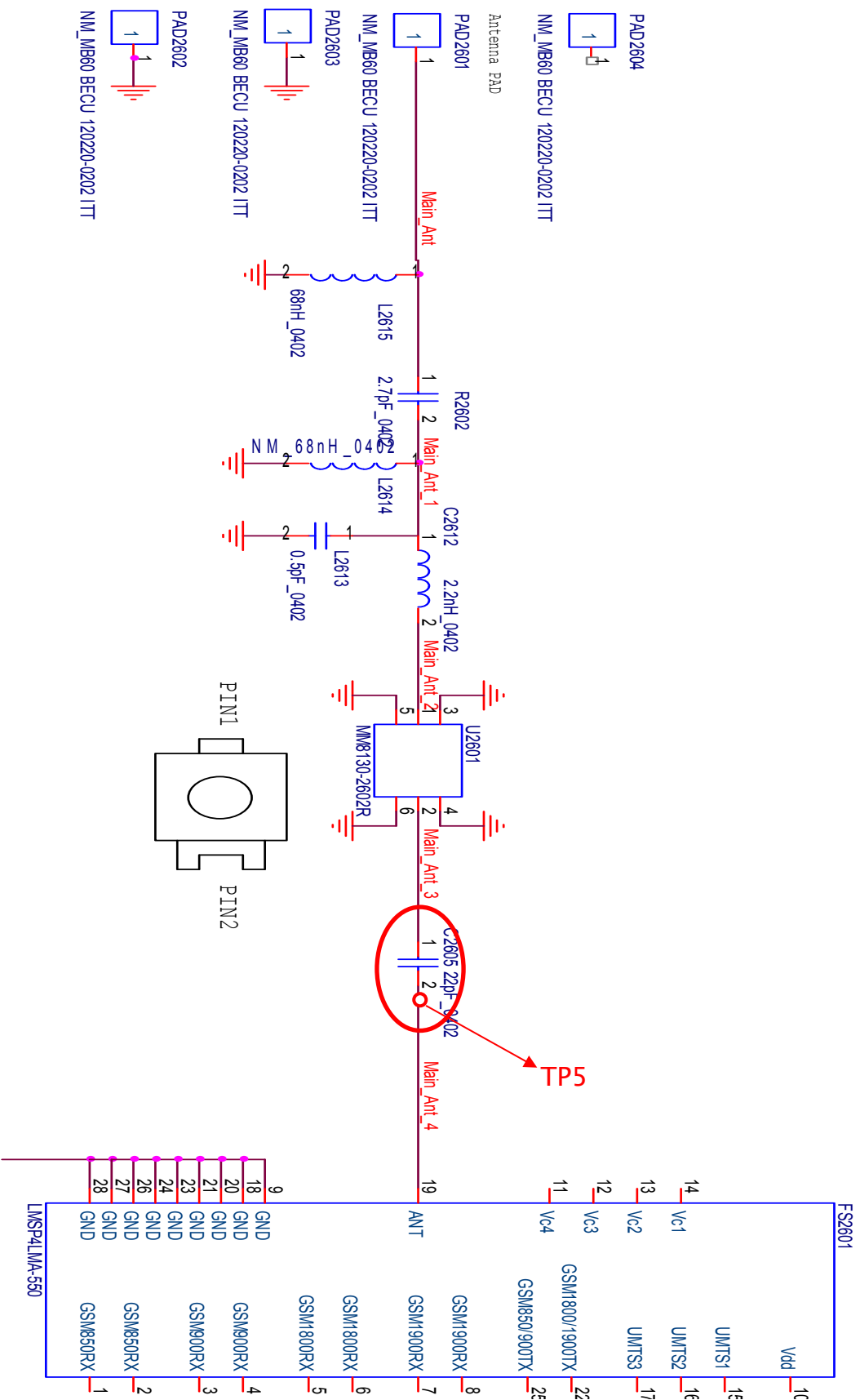
Circuit Diagram

Main Board



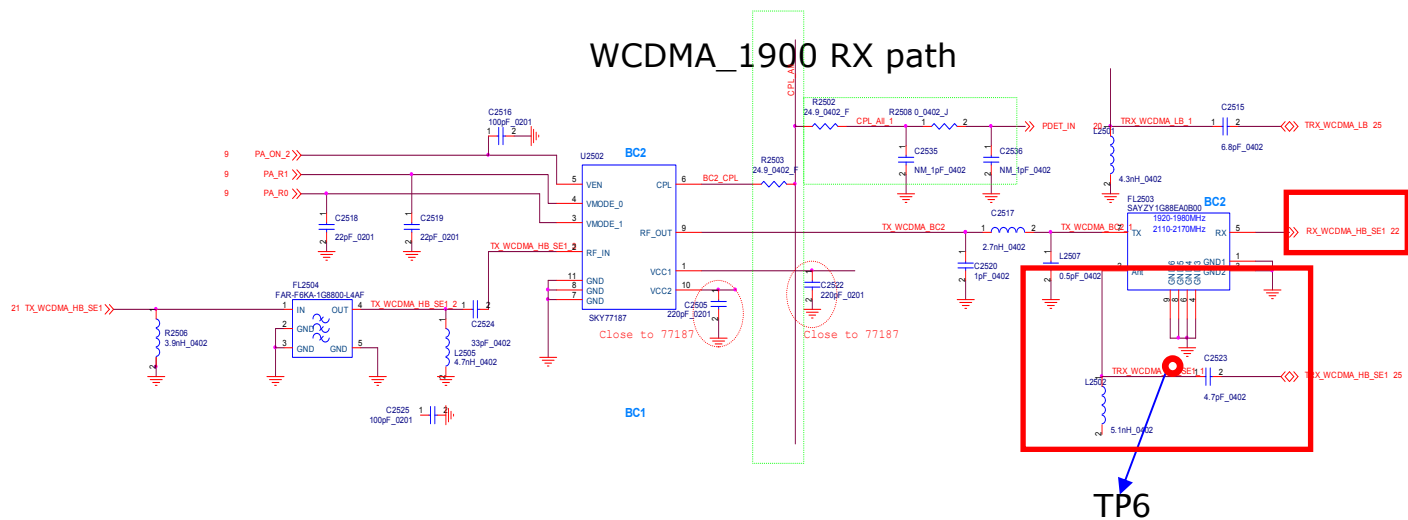
ANT SW Control Table 4-1

MODE	TP24 ANT_SEL0	TP25 ANT_SEL1	TP26 ANT_SEL2	TP27 ANT_SEL3
GSM850/EGSM900 TX	H	H	L	L
DCS1800/PCS1900 TX	H	L	L	L
GSM850 RX	L	H	H	L
EGSM900 RX	L	H	L	L
DCS1800 RX	L	L	H	L
PCS1900 RX	L	L	L	L
WCDMA_2100_Band 1 (UMTS1)	H	L	H	L
WCDMA_1900_Band 2 (UMTS3)	H	H	H	L
WCDMA_850_Band 5 (UMTS2)	H	L	H	H

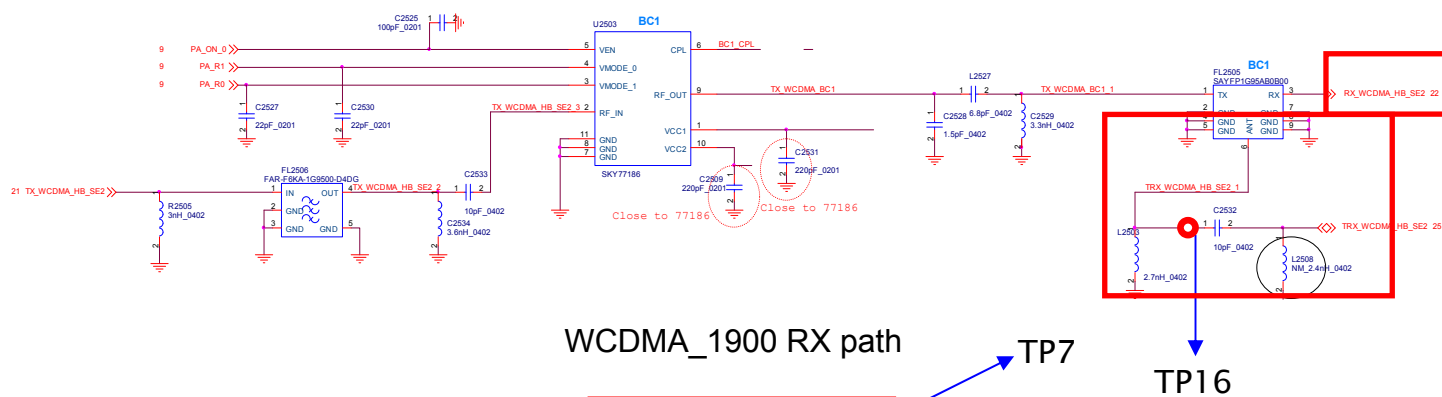


Circuit Diagram

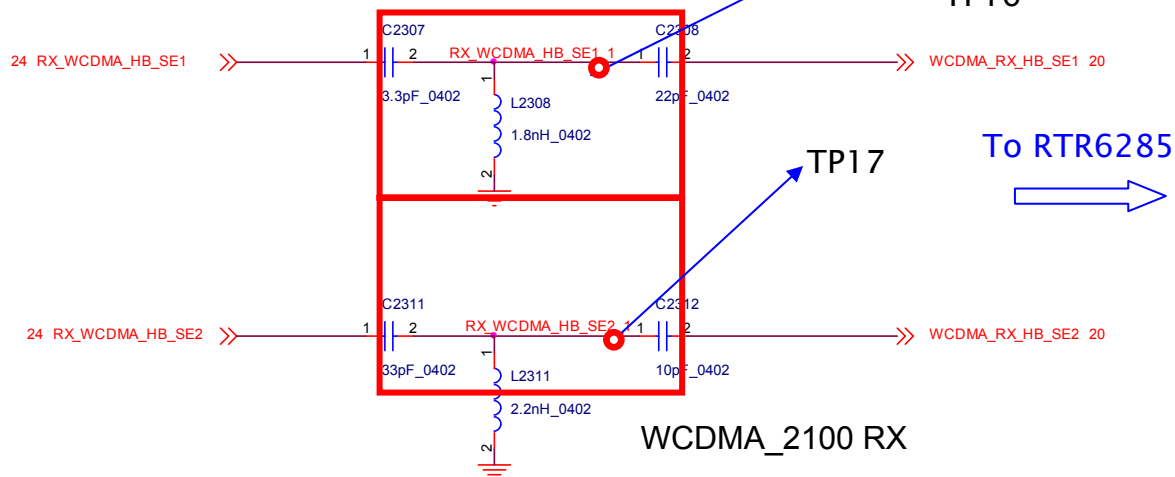
Main Board



WCDMA_2100 RX path

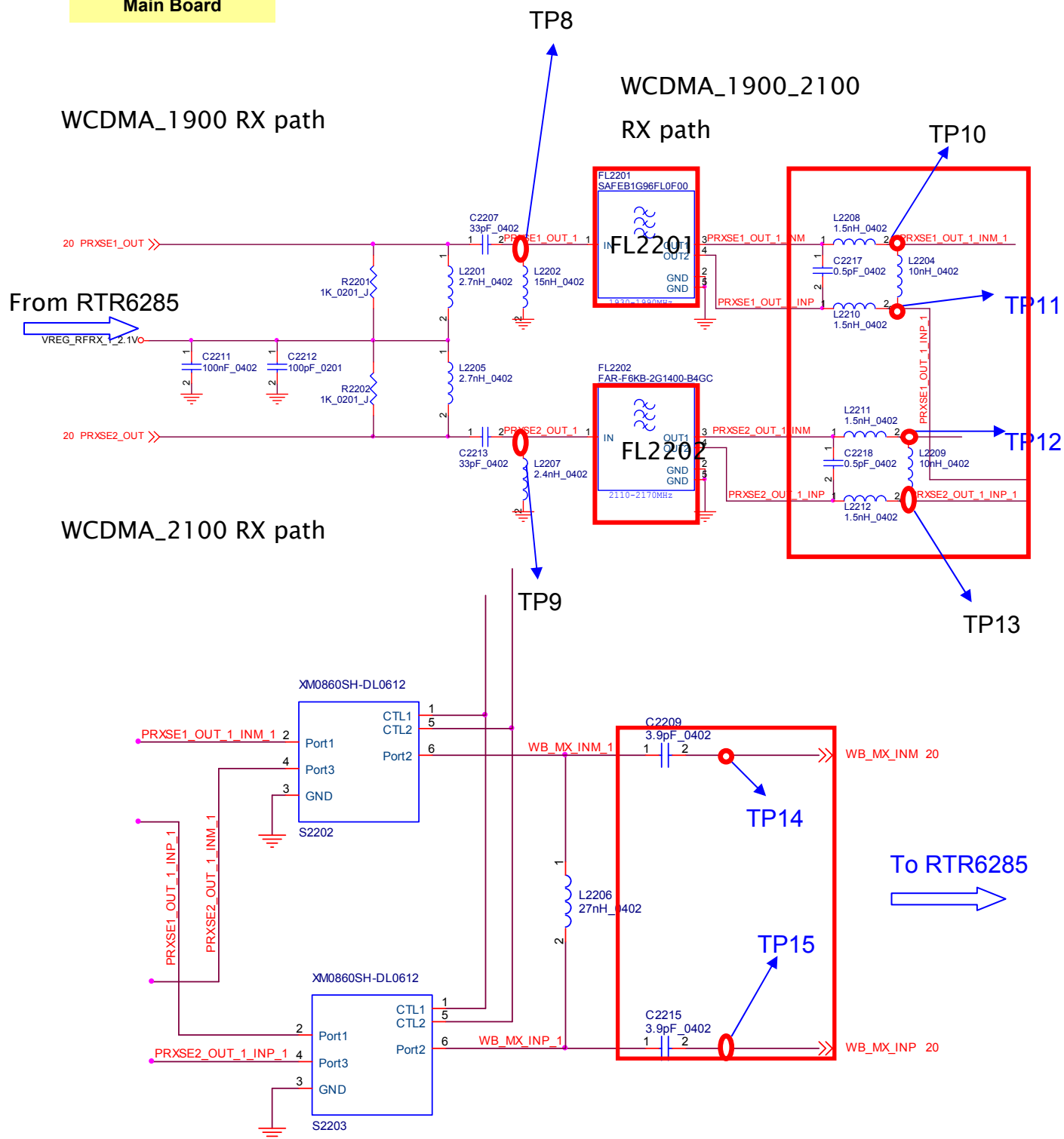


WCDMA_1900 RX path



Circuit Diagram

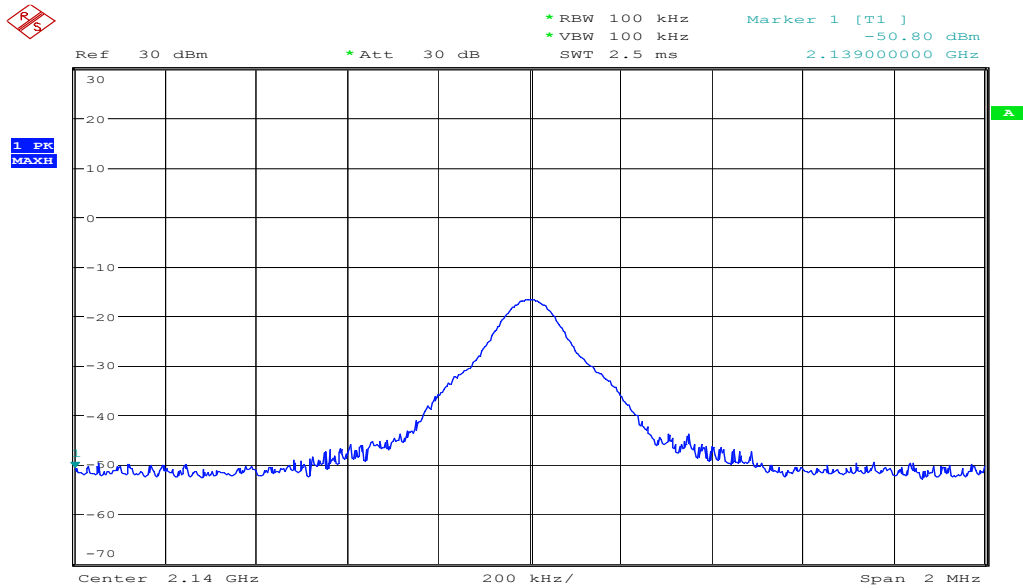
Main Board



Waveform

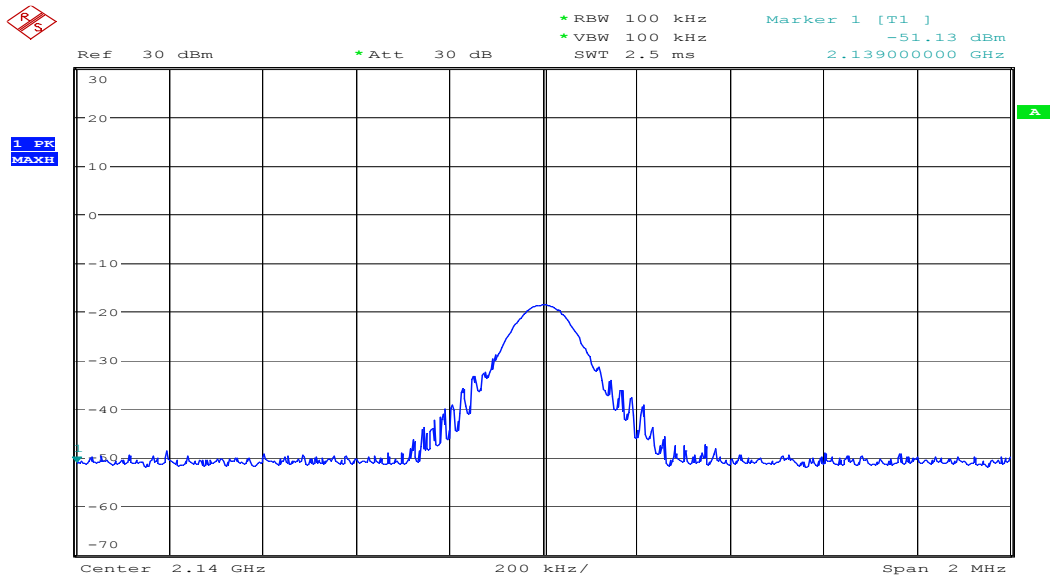
Feed CW waveform to RF connector. (If test WCDMA1900, please set WCDMA1900 RX frequency.) (If test WCDMA2100, please set WCDMA2100 RX frequency.)

TP5



Date: 17.NOV.2009 07:10:09

TP6 / TP16

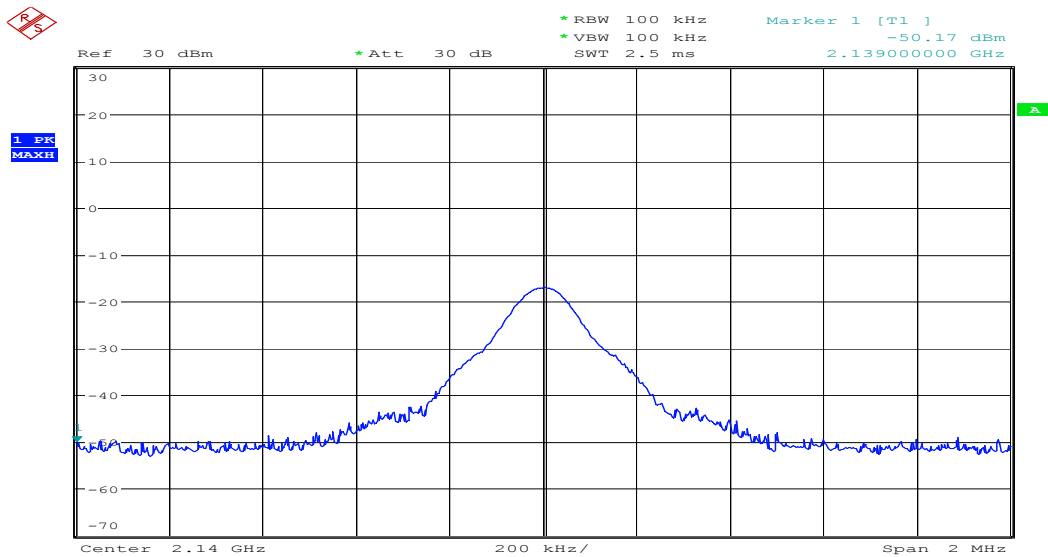


Date: 17.NOV.2009 07:12:37

Waveform

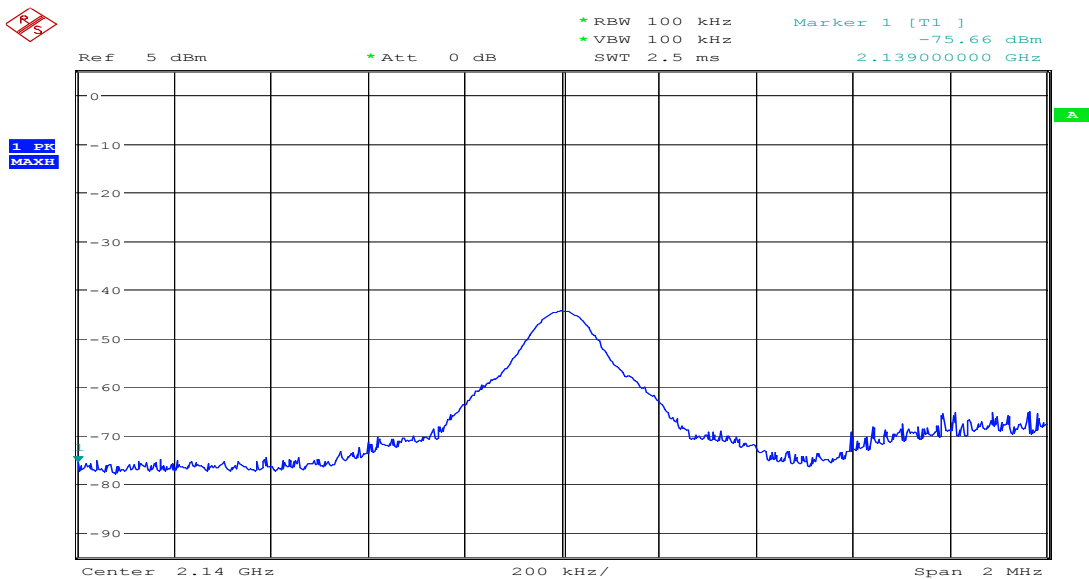
Feed CW waveform to RF connector. (If test WCDMA1900, please set WCDMA1900 RX frequency.) (If test WCDMA2100, please set WCDMA2100 RX frequency.)

TP7 / TP17



Date: 17.NOV.2009 07:14:35

TP8 / TP9

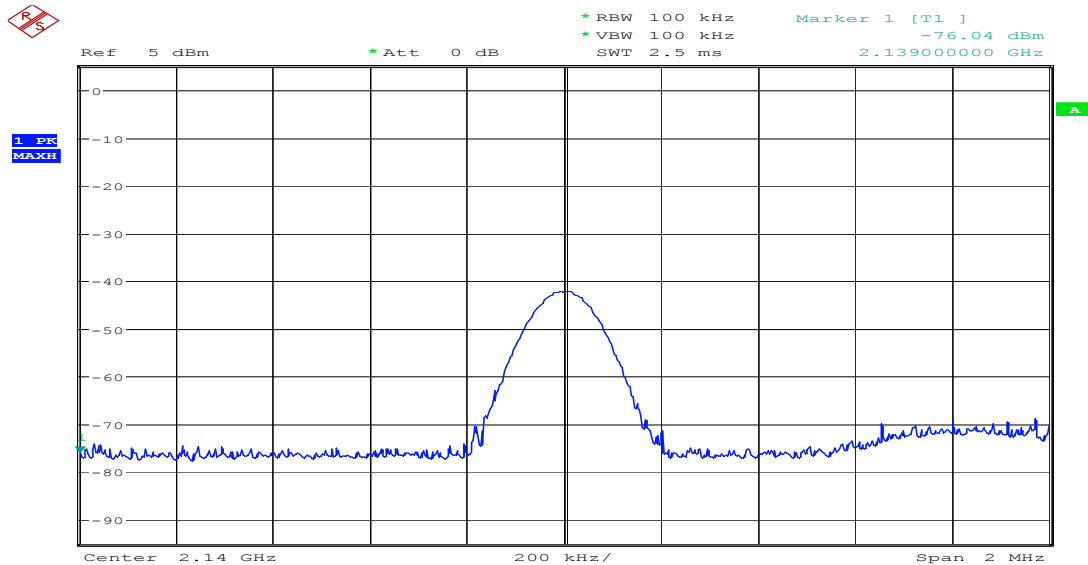


Date: 17.NOV.2009 07:20:19

Waveform

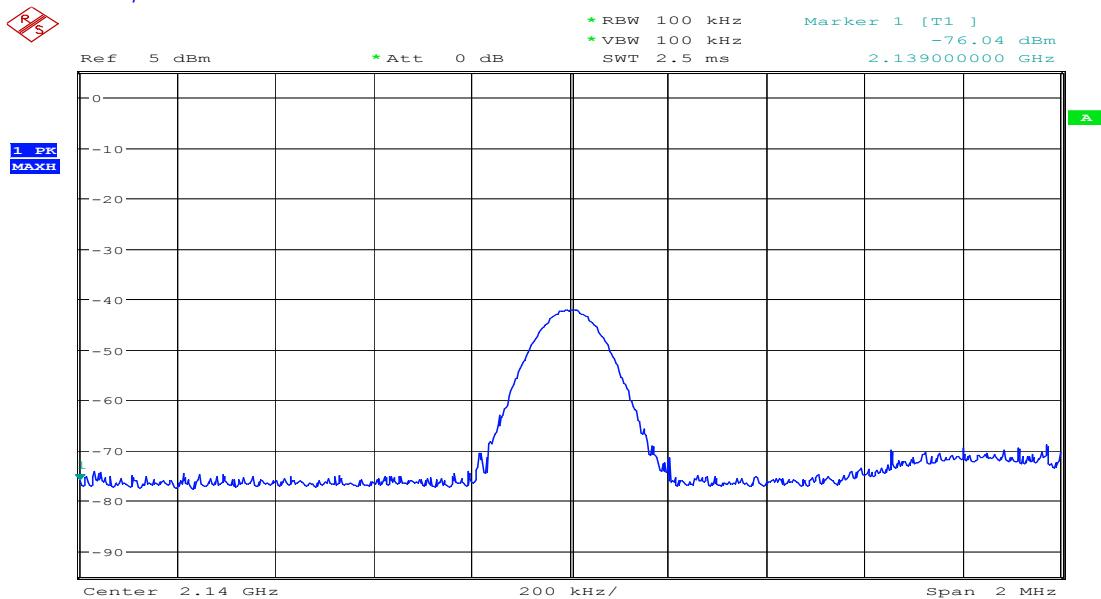
Feed CW waveform to RF connector. (If test WCDMA1900, please set WCDMA1900 RX frequency.) (If test WCDMA2100, please set WCDMA2100 RX frequency.)

TP10 / TP11



Date: 17.NOV.2009 07:22:42

TP12 / TP13

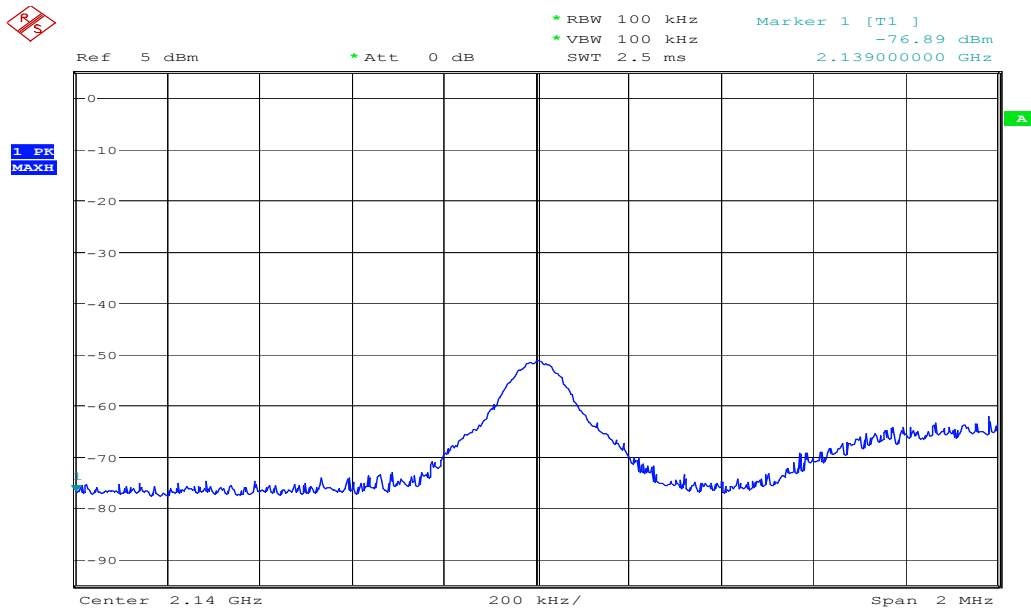


Date: 17.NOV.2009 07:22:42

Waveform

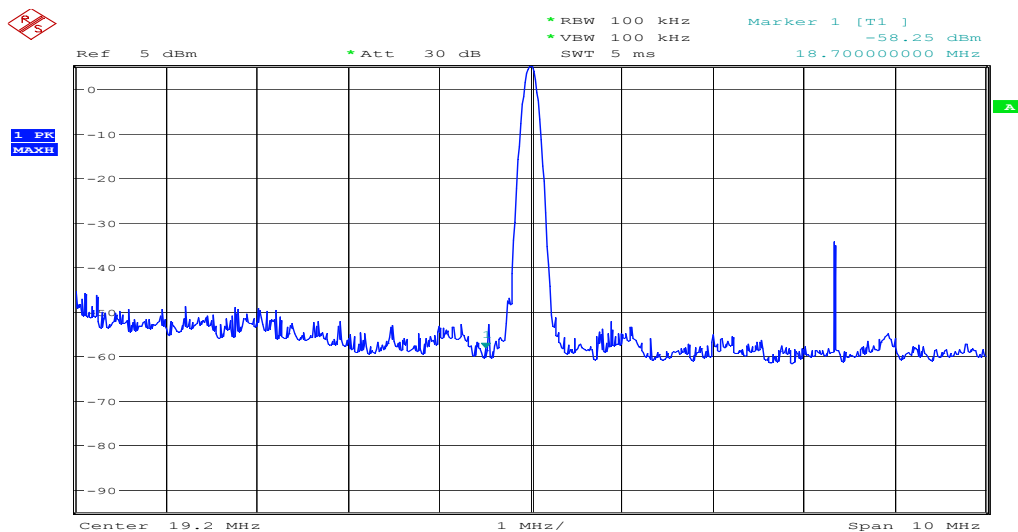
Feed CW waveform to RF connector. (If test WCDMA1900, please set WCDMA1900 RX frequency.) (If test WCDMA2100, please set WCDMA2100 RX frequency.)

TP14 / TP15



Date: 17.NOV.2009 07:23:44

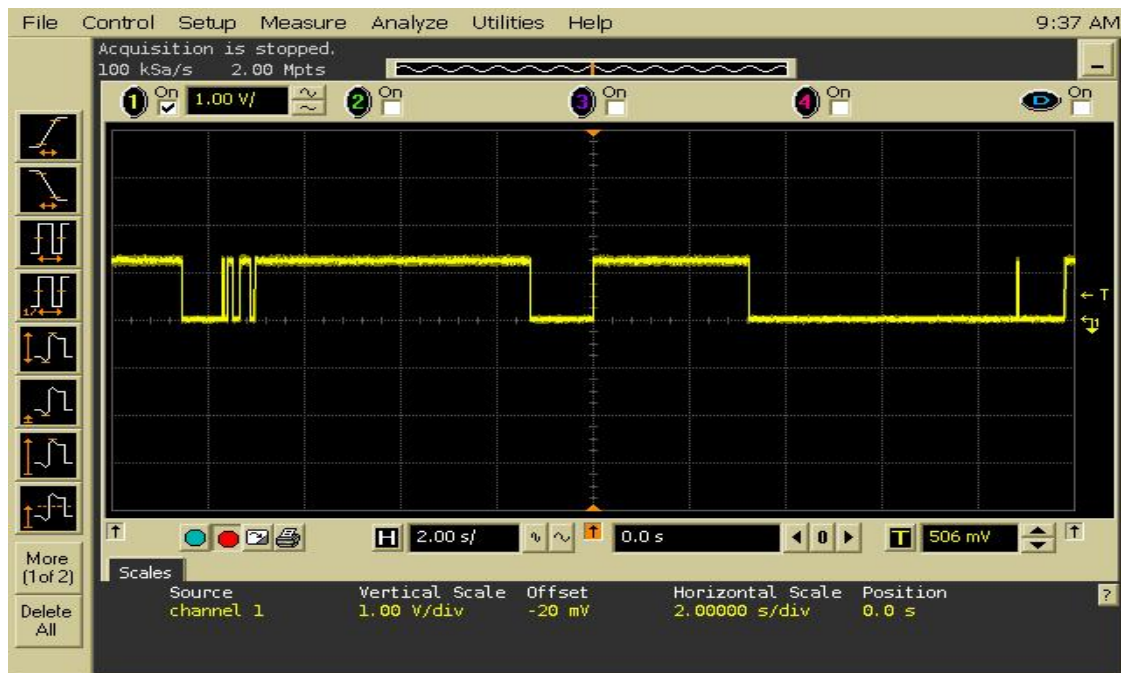
TP22



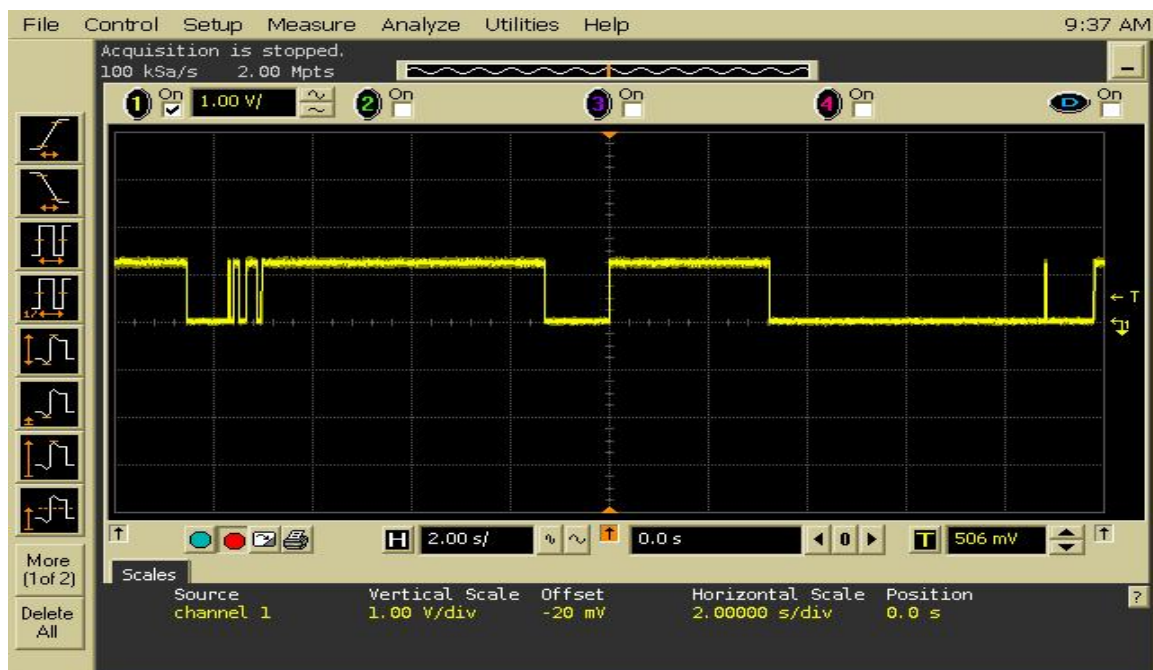
Date: 19.NOV.2009 06:30:48

Waveform

TP82 / TP83



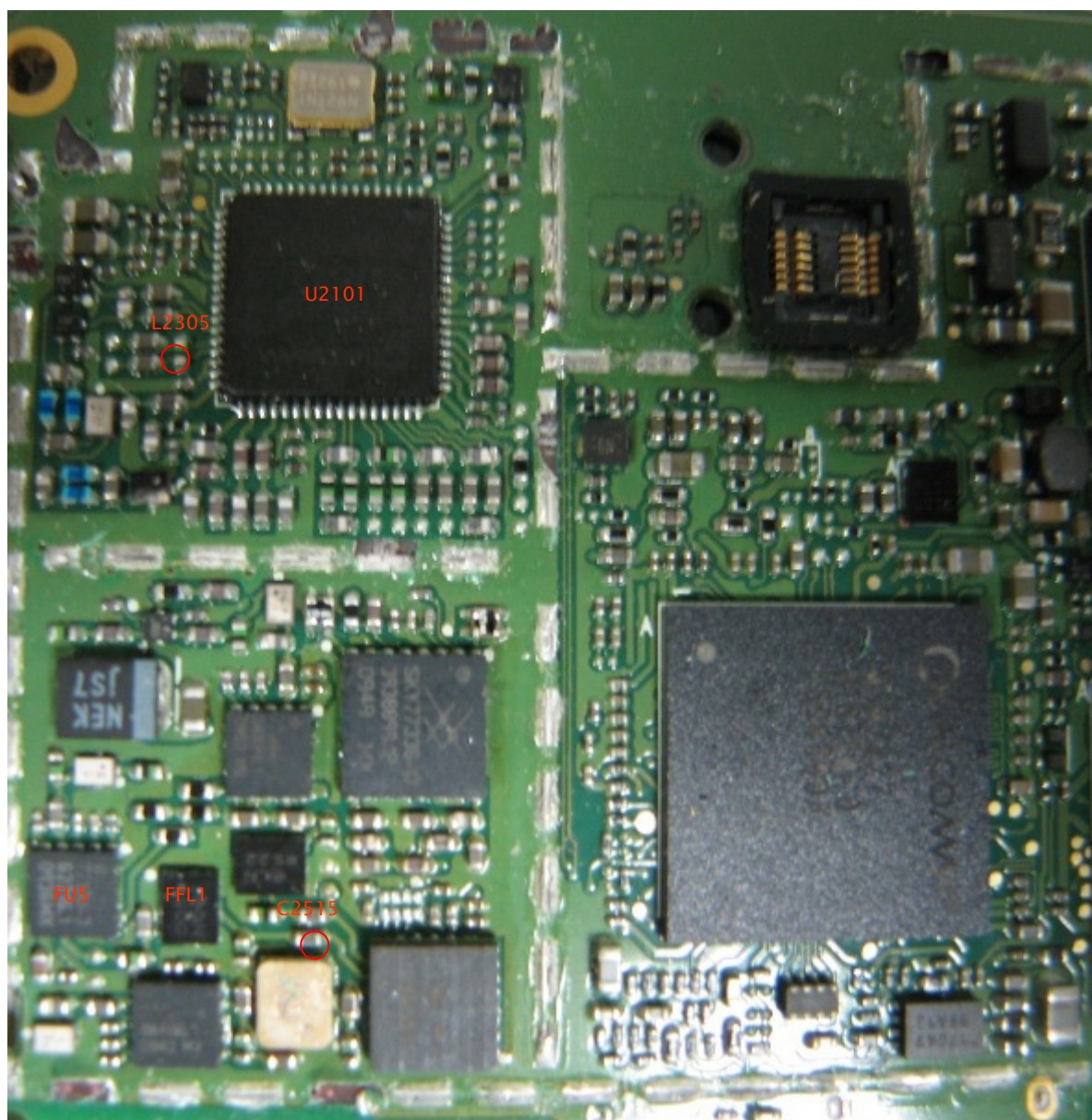
TP84 / TP85



WCDMA850 RX Trouble

Picture Data

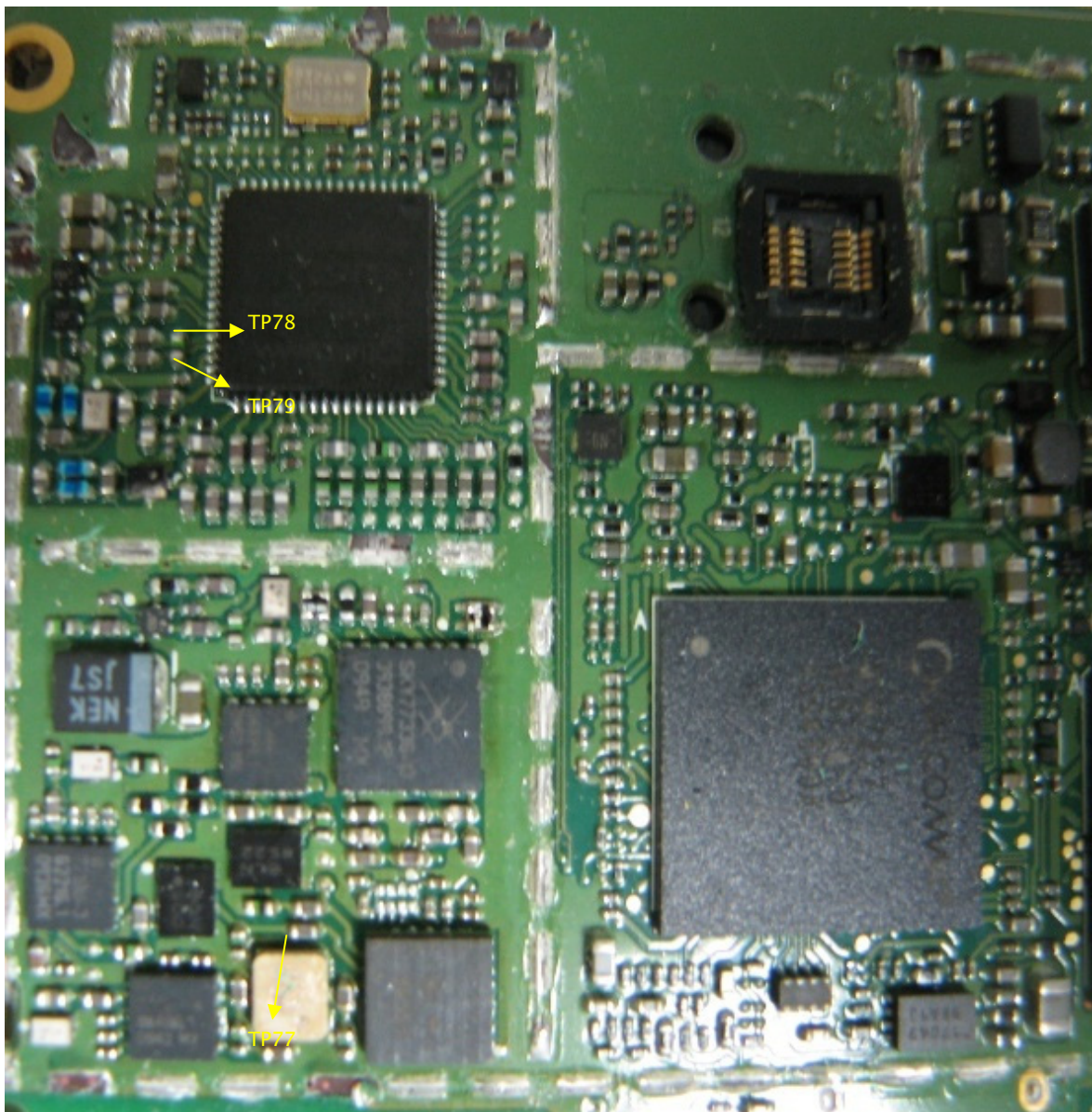
Main board top



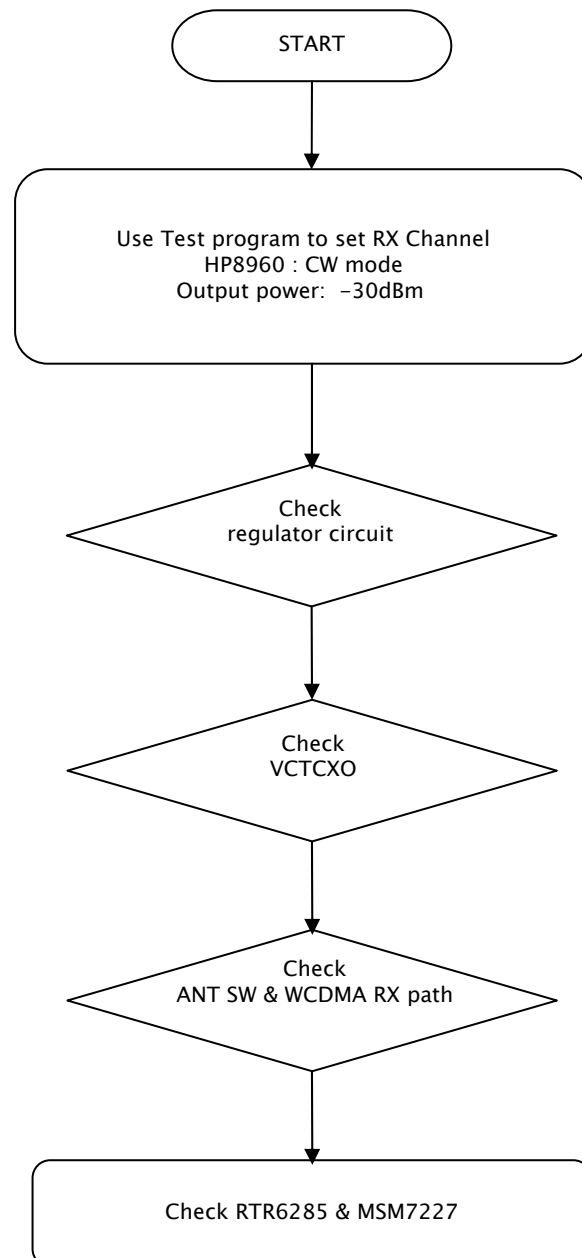
WCDMA850 RX Trouble

Picture Data

Main board top



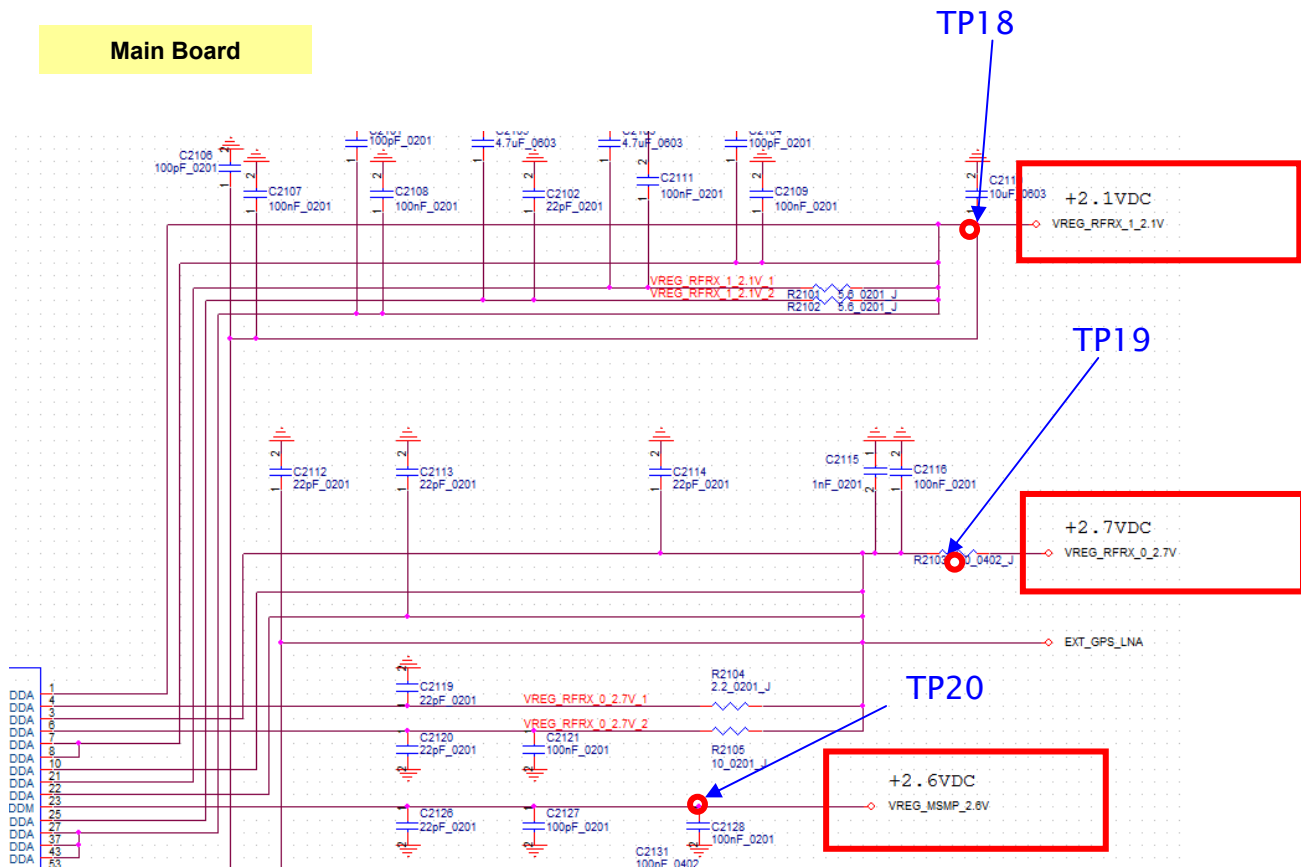
Checking Flow



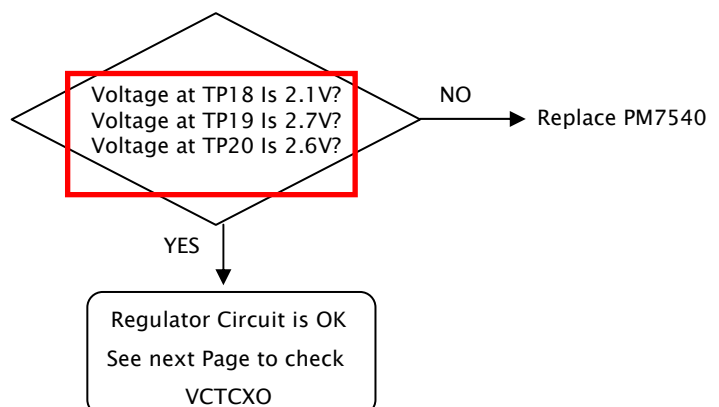
(1) Checking Regulator Circuit

Circuit Diagram

Main Board



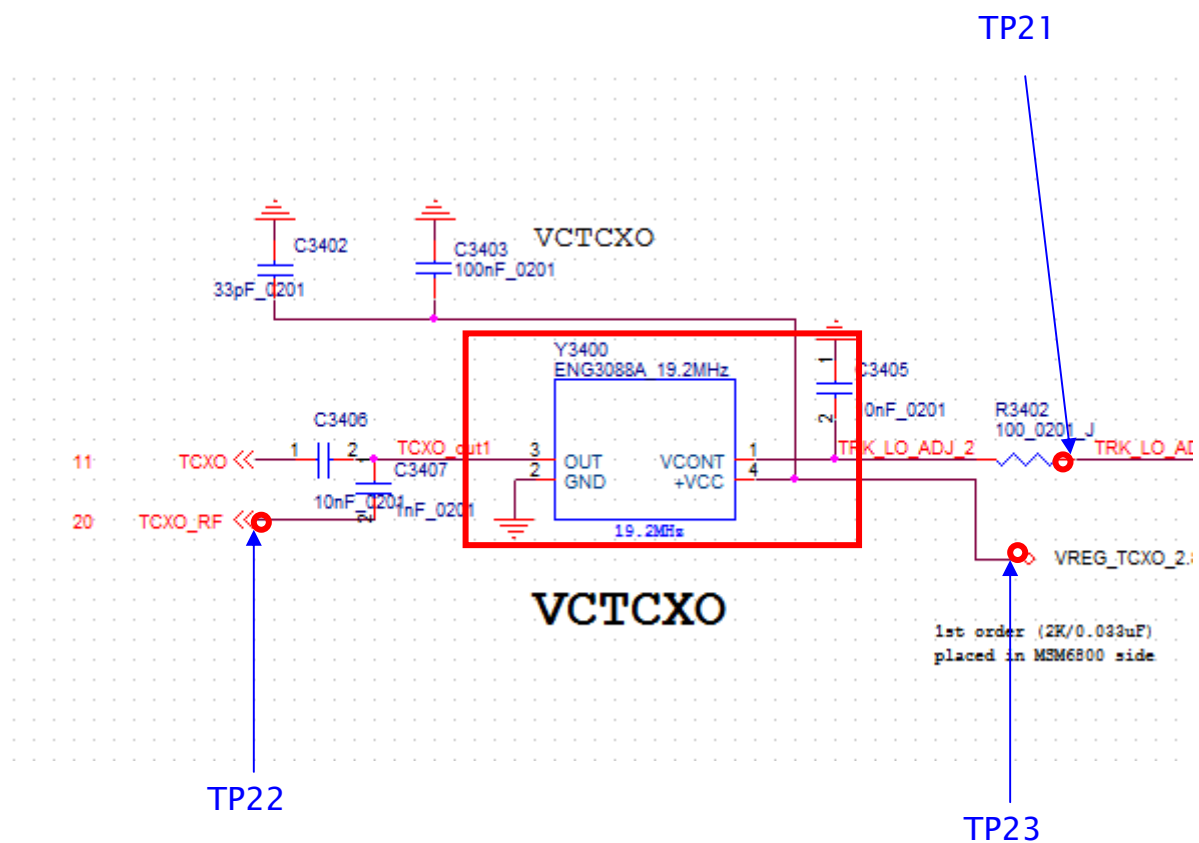
Checking Flow



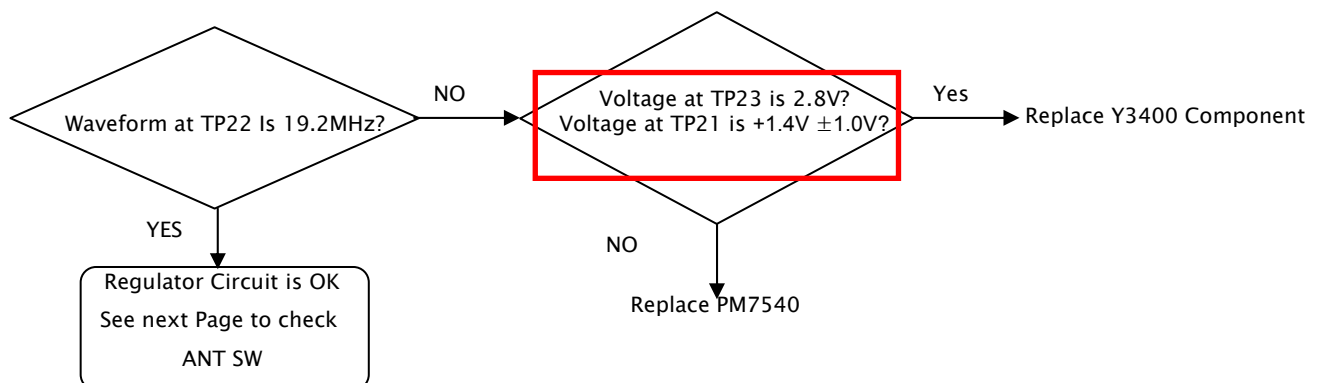
(2) Check VCTCXO

Circuit Diagram

Main Board



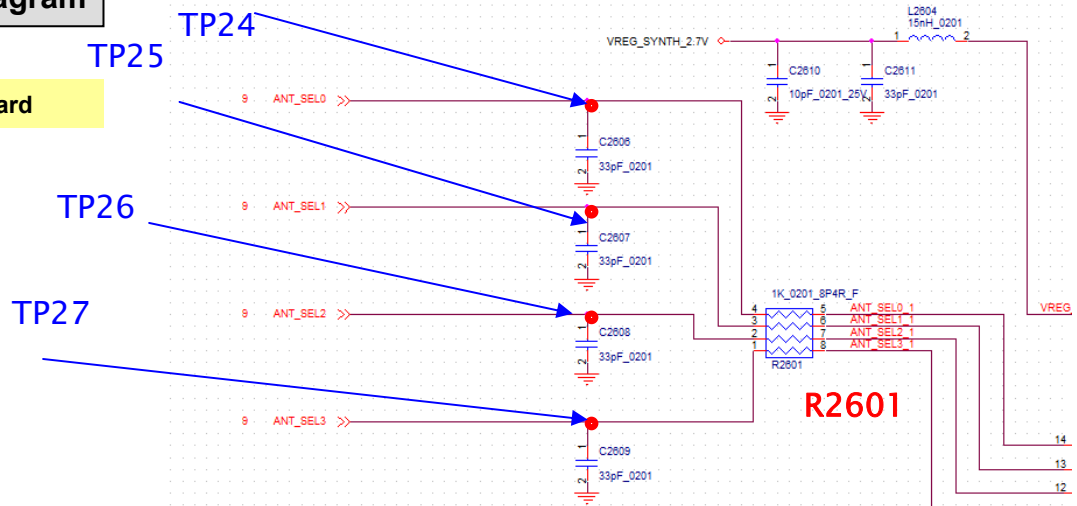
Checking Flow



(3) Checking Ant SW & RX path

Circuit Diagram

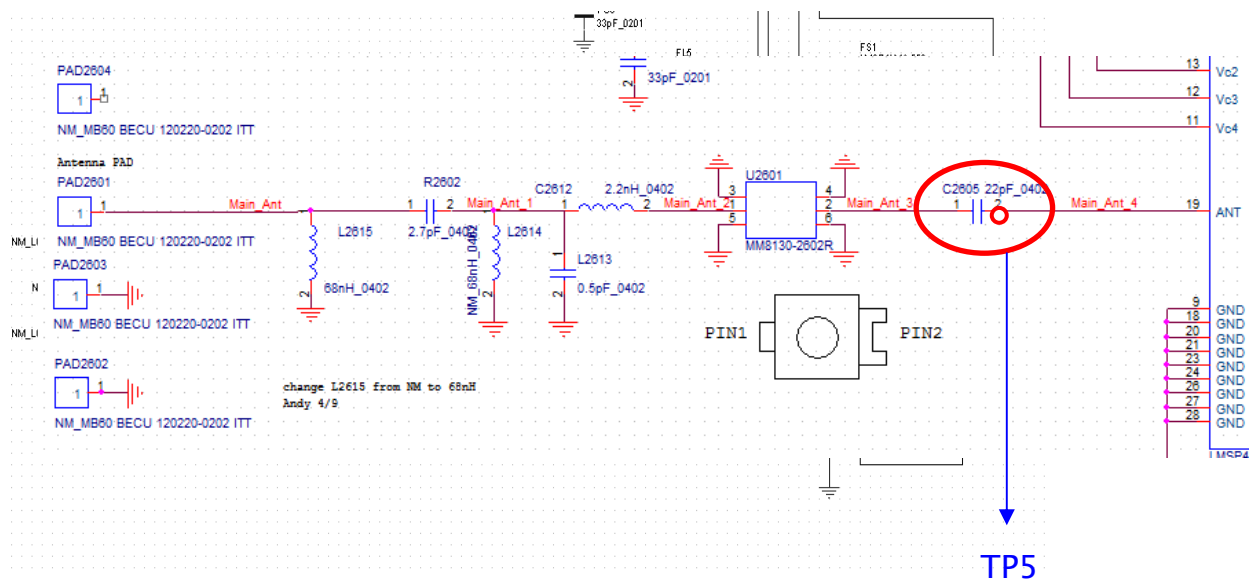
Main Board



TP24 TP25 TP26 TP27

MODE	ANT_SEL0	ANT_SEL1	ANT_SEL2	ANT_SEL3
GSM850/EGSM900 TX	H	H	L	L
DCS1800/PCS1900 TX	H	L	L	L
GSM850 RX	L	H	H	L
EGSM900 RX	L	H	L	L
DCS1800 RX	L	L	H	L
PCS1900 RX	L	L	L	L
WCDMA_2100_Band 1 (UMTS1)	H	L	H	L
WCDMA_1900_Band 2 (UMTS3)	H	H	H	L
WCDMA_850_Band 5 (UMTS2)	H	L	H	H

-1

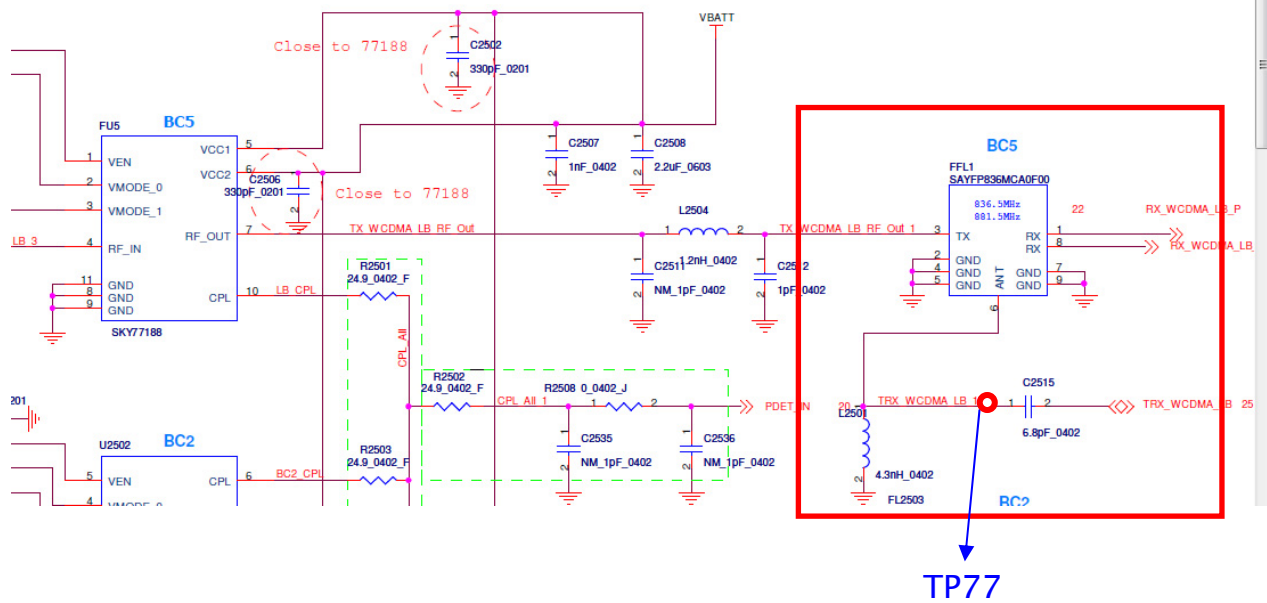


TP5

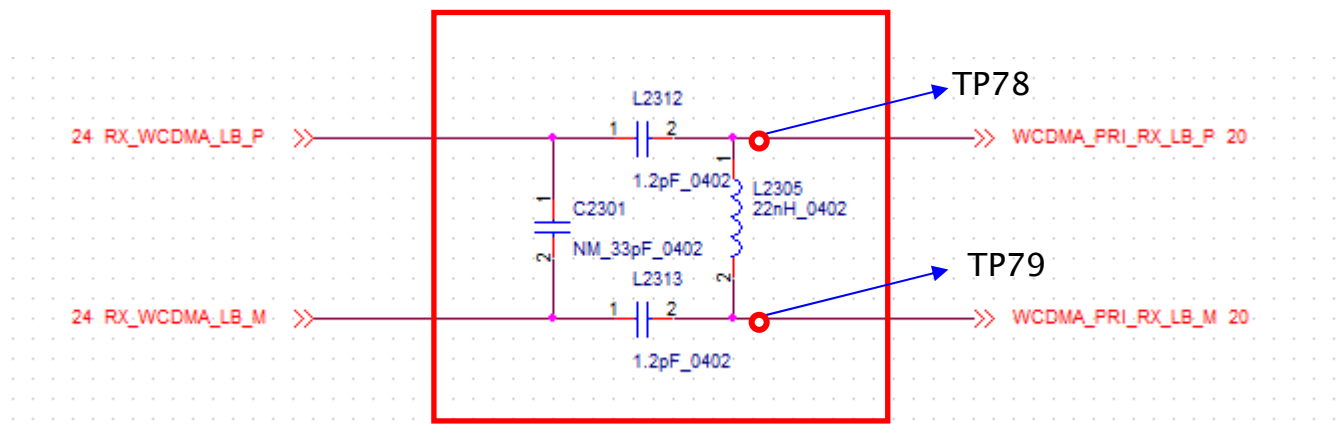
Circuit Diagram

Main Board

WCDMA_850 RX path

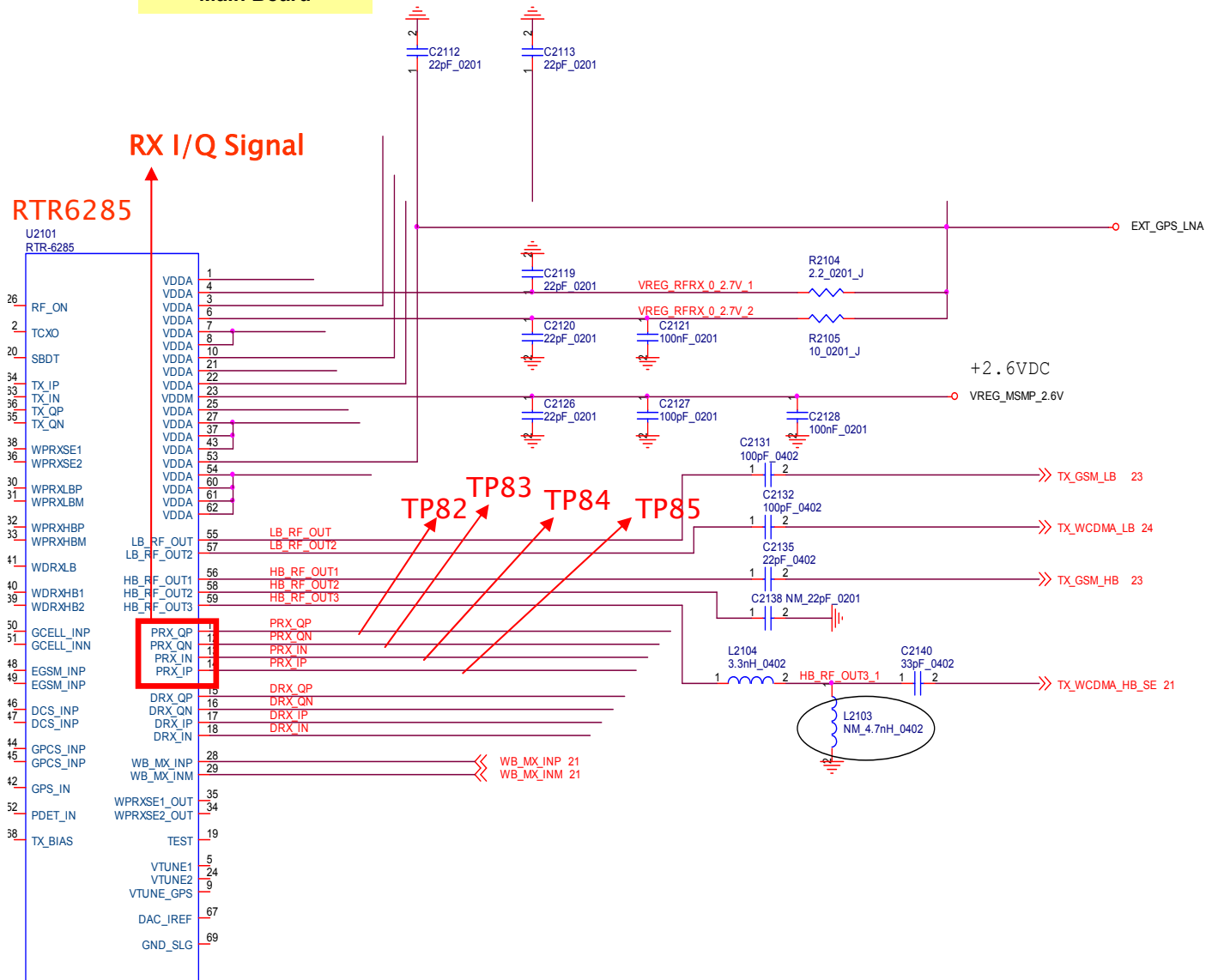


WCDMA_850 RX path



Circuit Diagram

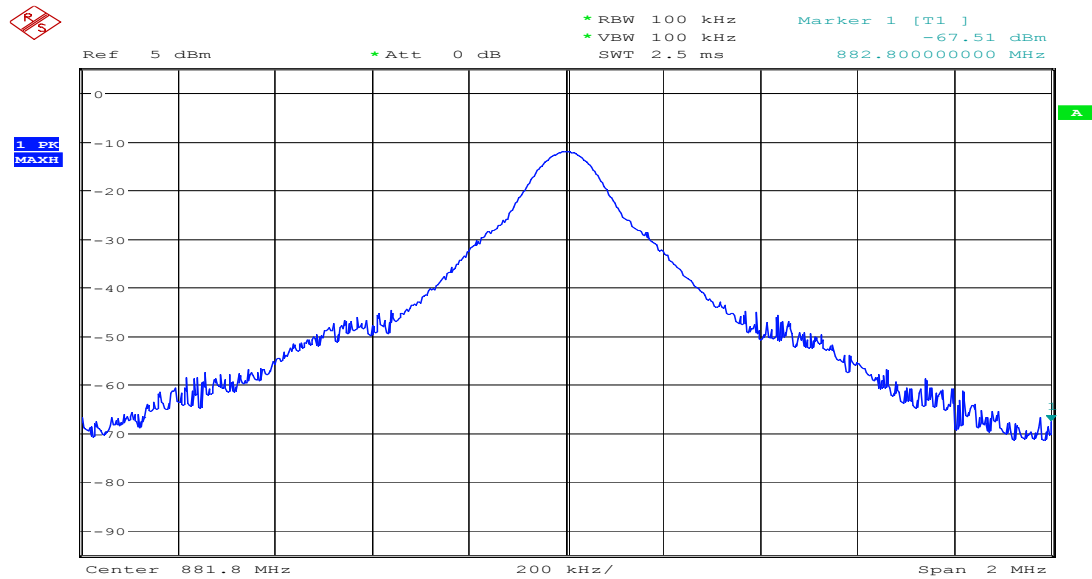
Main Board



Waveform

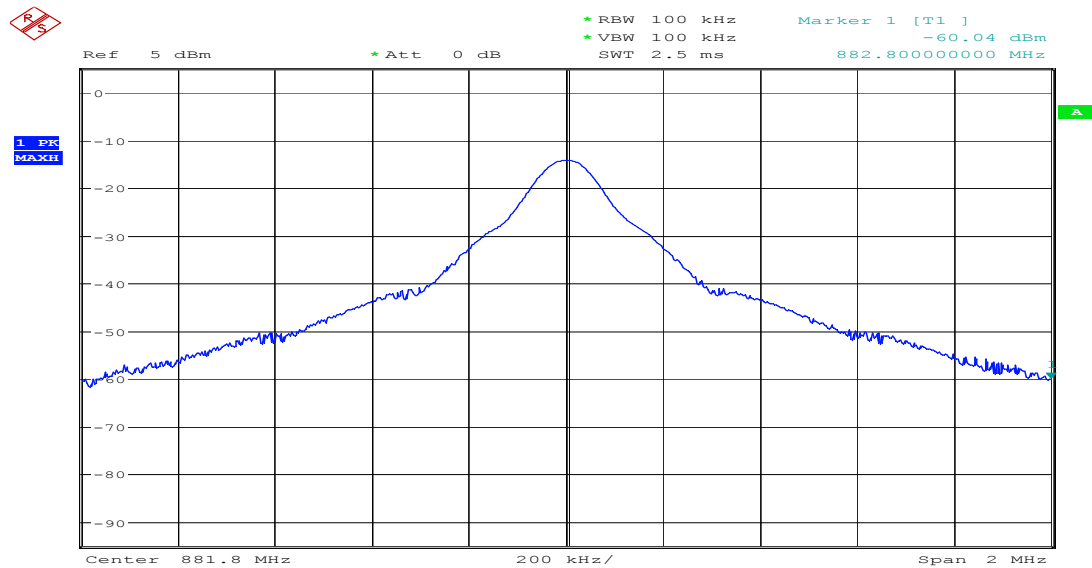
Feed CW waveform to RF connector. (Please set WCDMA850 RX frequency.)

TP5



Date: 17.NOV.2009 07:25:24

TP77

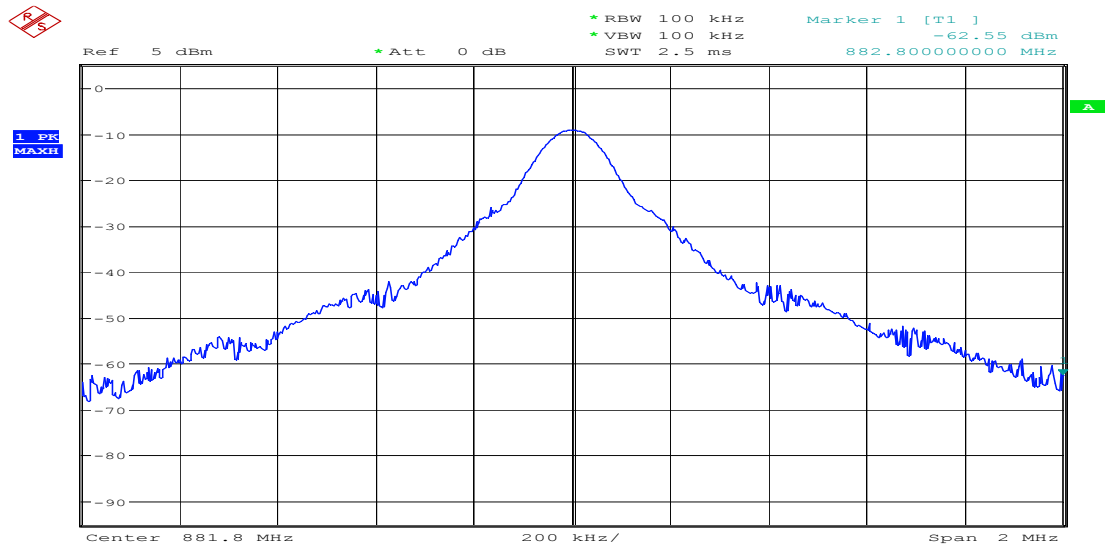


Date: 17.NOV.2009 07:27:57

Waveform

Feed CW waveform to RF connector. (Please set WCDMA850 RX frequency.)

TP78 / TP79



Waveform

TP82 / TP83



TP84 / TP85

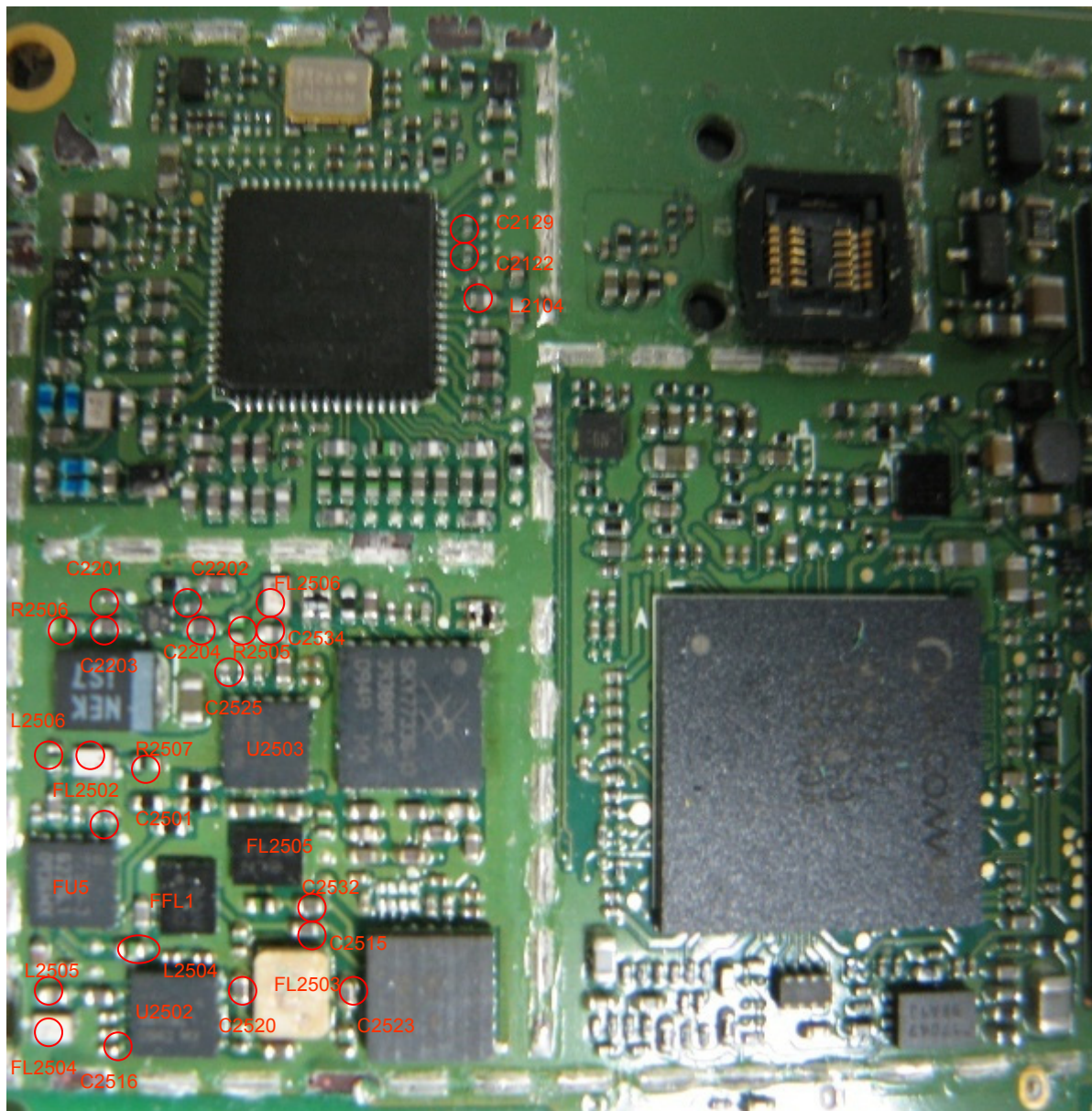


4.5 WCDMA TX Trouble

WCDMA2100/1900/850 TX Trouble

Picture Data

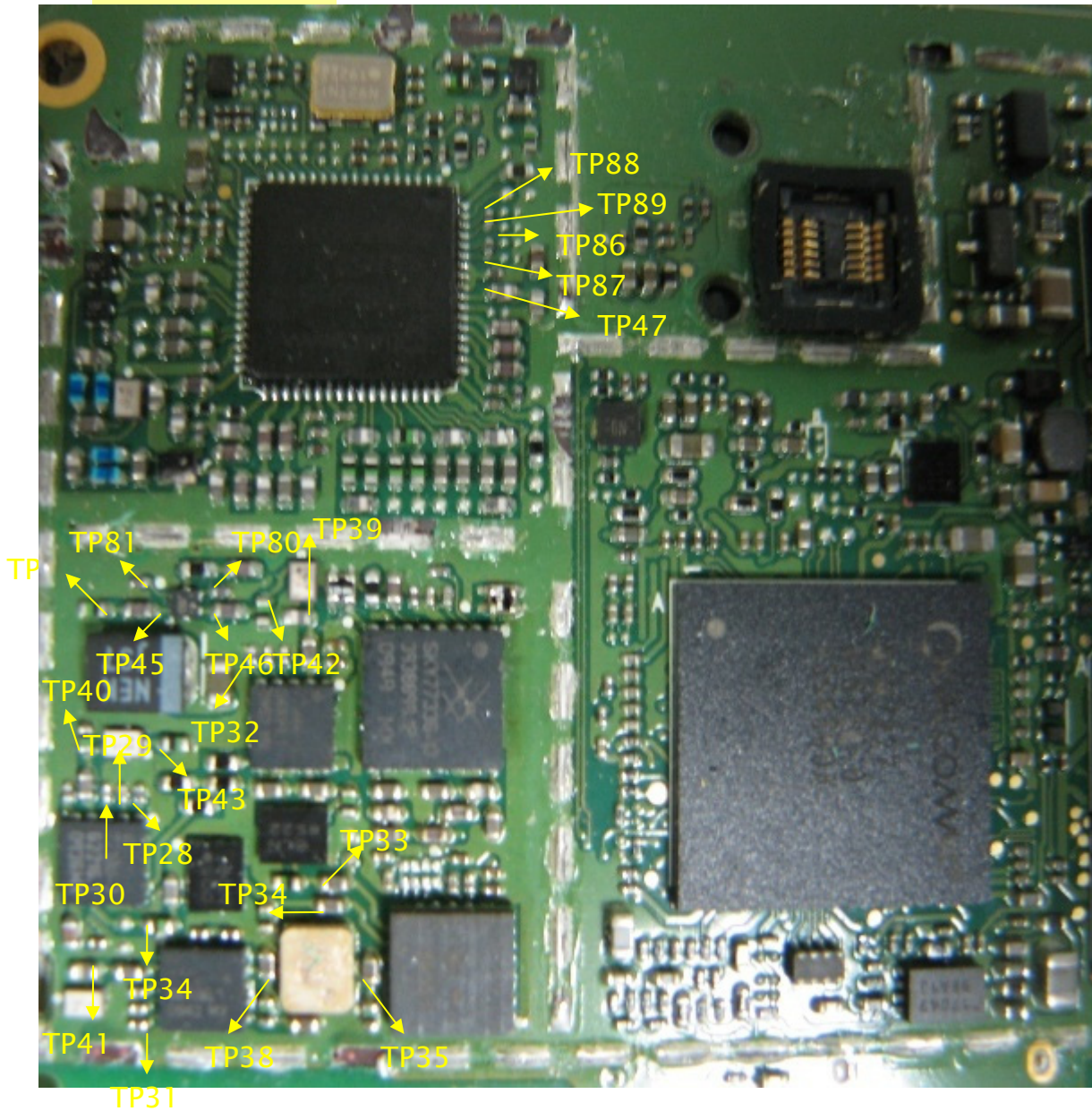
Main board top



WCDMA2100/1900/850 TX Trouble

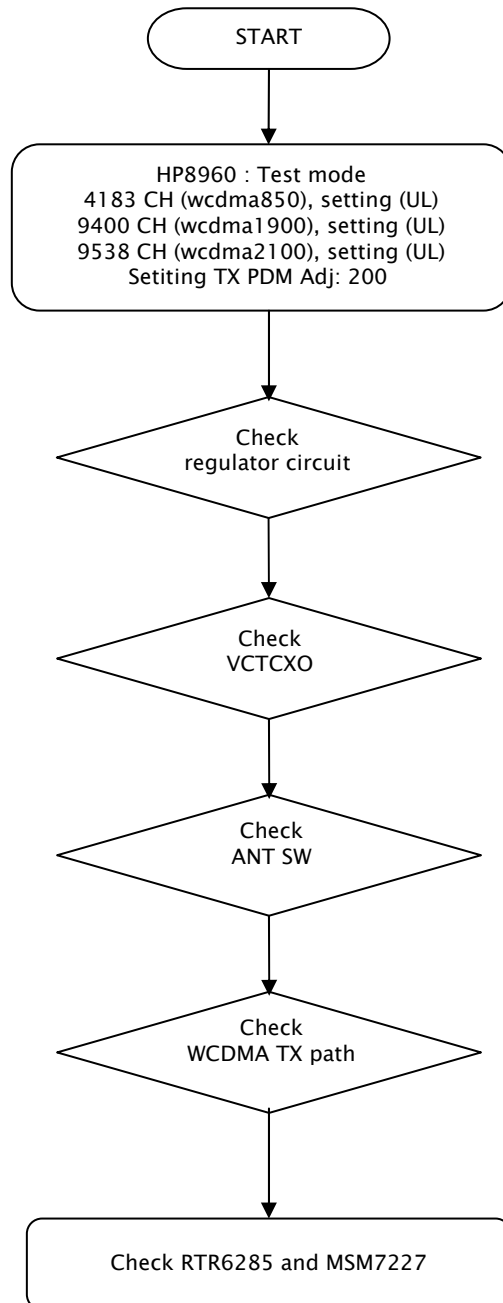
Picture Data

Main board top



WCDMA TX Trouble

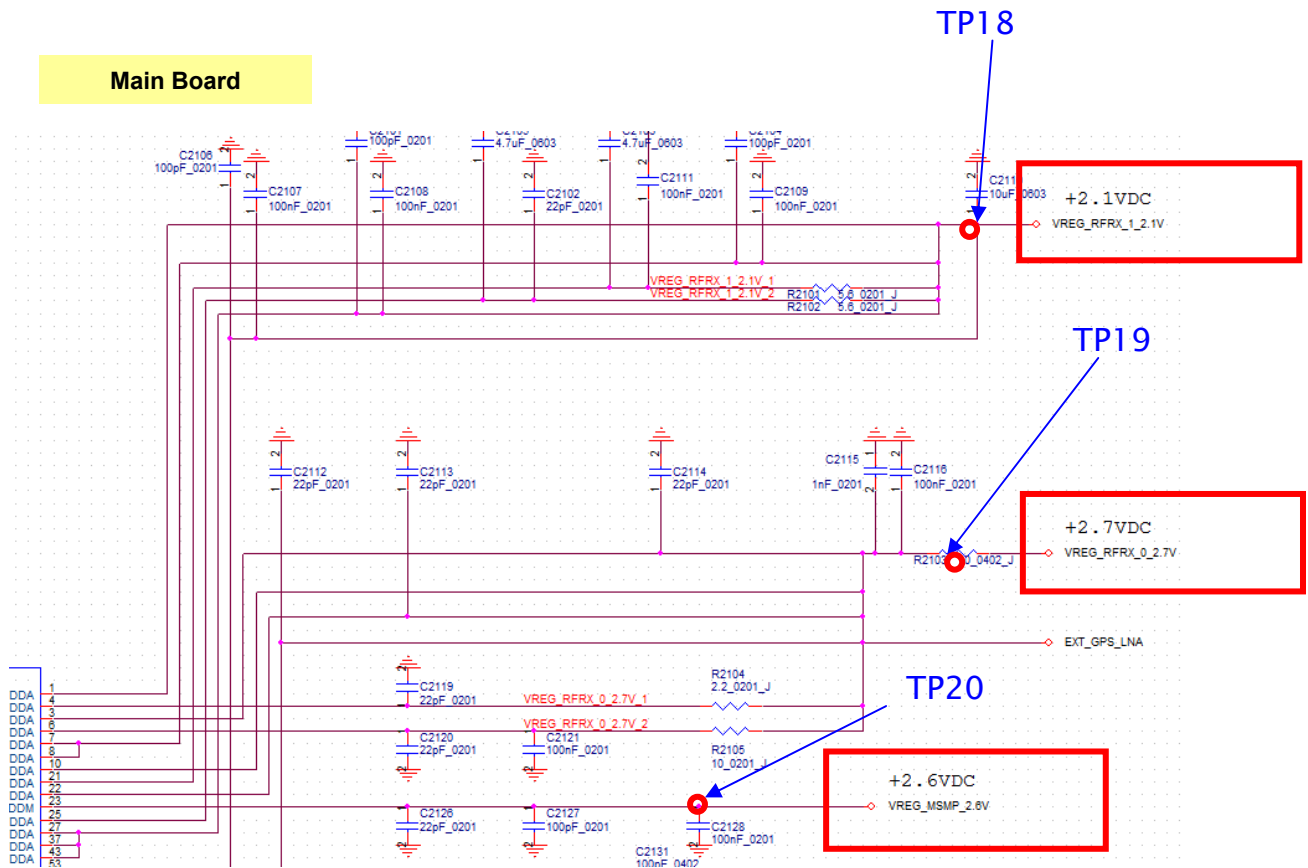
Checking Flow



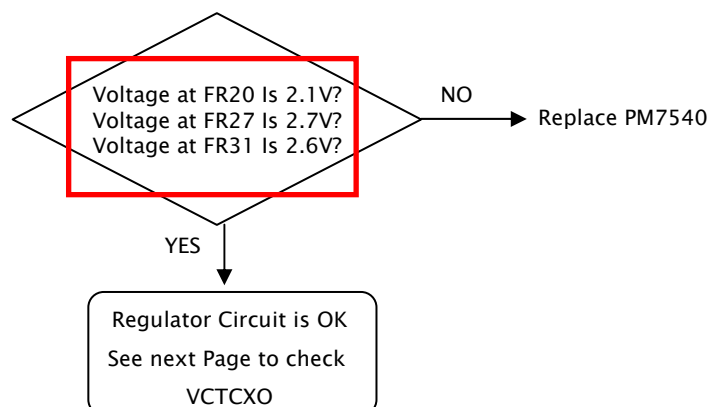
Checking Regulator Circuit

Circuit Diagram

Main Board



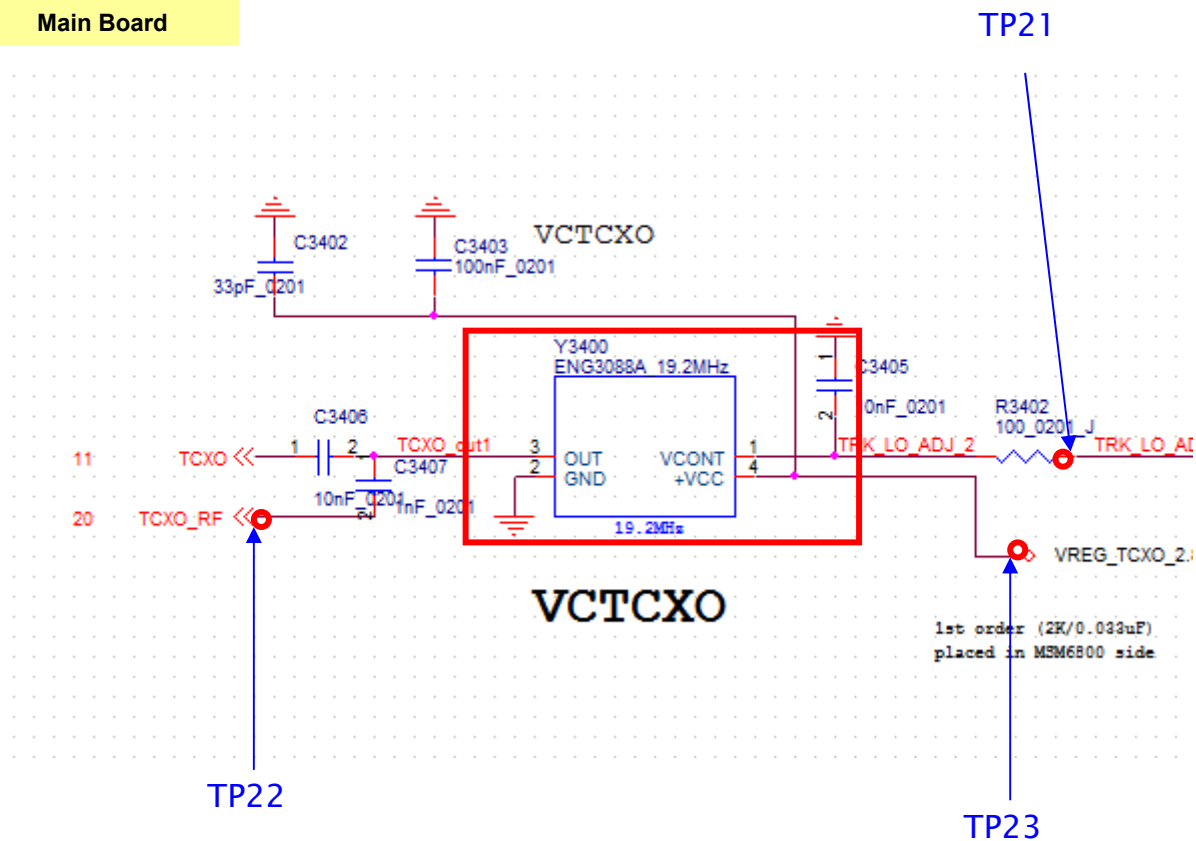
Checking Flow



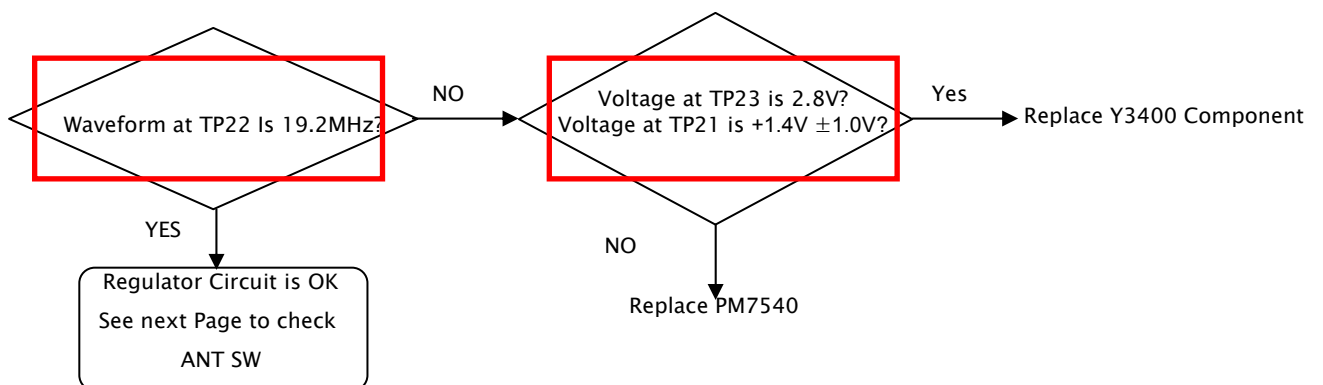
(2) Check VCTCXO

Circuit Diagram

Main Board



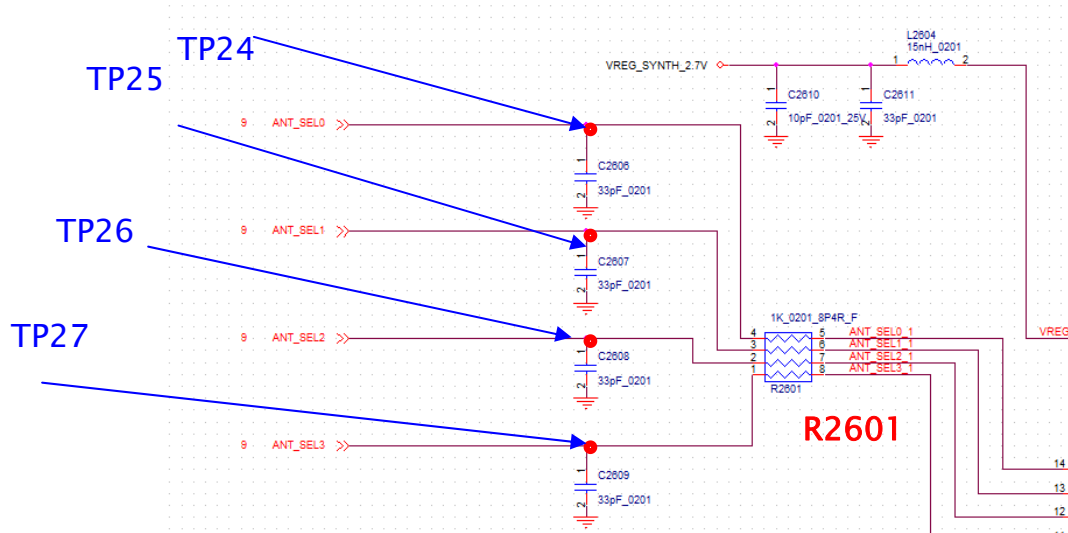
Checking Flow



(3) Checking Ant SW

Circuit Diagram

Main Board



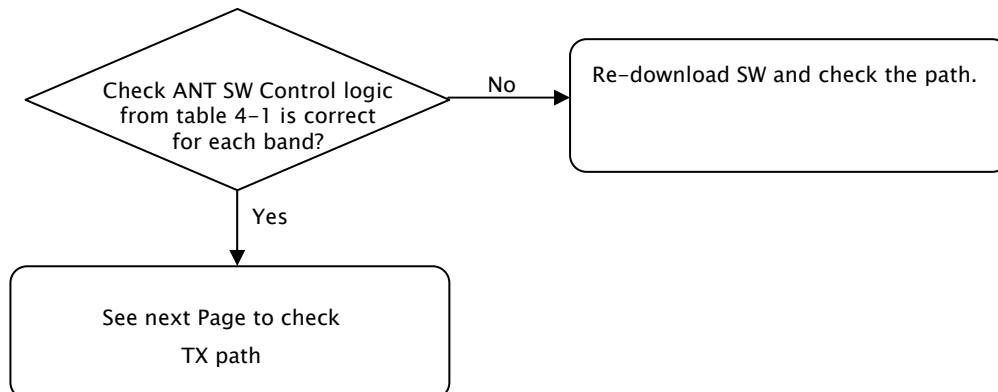
TP24 TP25 TP26 TP27

MODE	ANT_SEL0	ANT_SEL1	ANT_SEL2	ANT_SEL3
GSM850/EGSM900 TX	H	H	L	L
DCS1800/PCS1900 TX	H	L	L	L
GSM850 RX	L	H	H	L
EGSM900 RX	L	H	L	L
DCS1800 RX	L	L	H	L
PCS1900 RX	L	L	L	L
WCDMA 2100 Band 1 (UMTS1)	H	L	H	L
WCDMA 1900 Band 2 (UMTS3)	H	H	H	L
WCDMA 850 Band 5 (UMTS2)	H	L	H	H

-1

Checking Flow

Table 4.1



Circuit Diagram

Main Board



RF TROUBLE SHOOTING

	TP32	TP28	TP31
WCDMA PA STATE	PA_ON_0	PA_ON_1	PA_ON_2
OFF	L	L	L
WCDMA850 ON	L	H	L
WCDMA1900 ON	L	L	H
WCDMA2100 ON	H	L	L

TP30			TP29	
POWER MODE	ENABLE	PA_R0 (Vmod1)	PA_R1 (Vmod0)	VCC
POWER DOWN MODE	L	L	L	ON
Standby mode	L	don't care	don't care	ON
LOW POWER	H	H	H	ON
MEDIUM POWER	H	L	H	ON
HIGH POWER	H	L	L	ON
Optional Lower Vcc Mode	H	L	L	1.5V

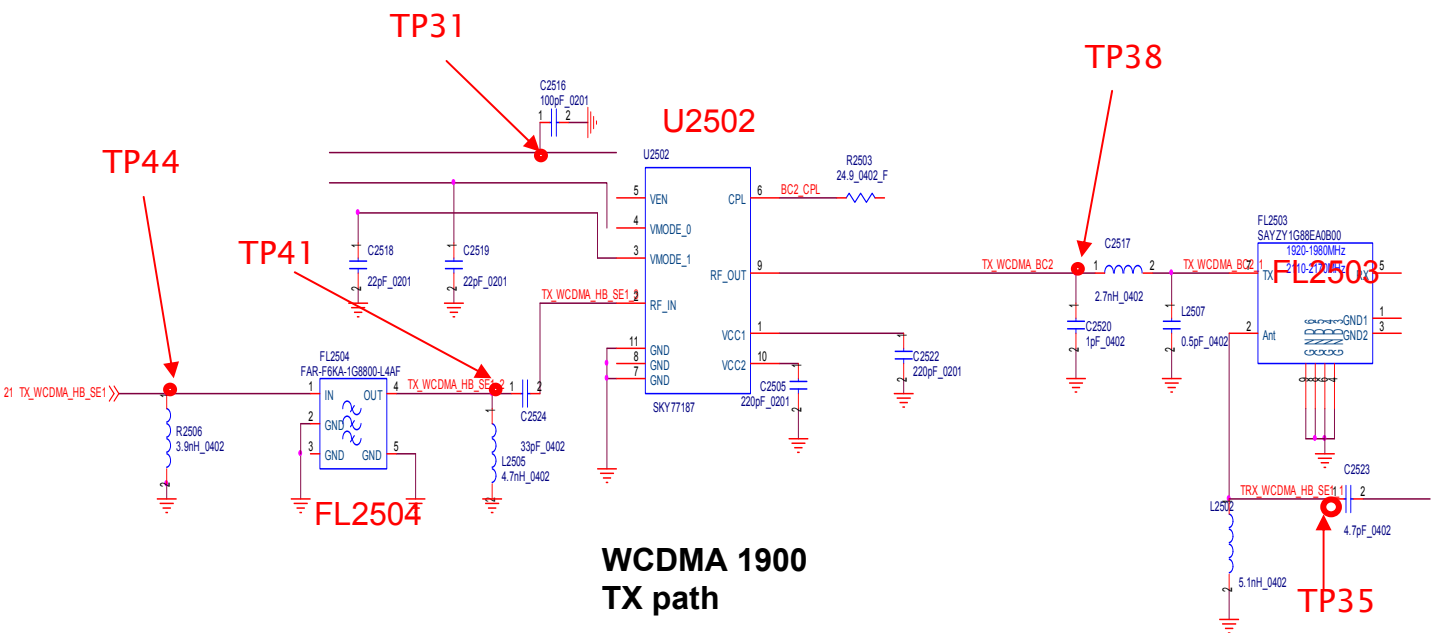
WCDMA PA STATE	PA_ON_0	PA_ON_1	PA_ON_2	INTER_TX_SW_SEL_1 GPIO93	INTER_TX_SW_SEL_1 GPIO93
OFF	L	L	L	L	L
WCDMA850 ON	L	H	L	L	L
WCDMA1900 ON	L	L	H	L	H
WCDMA2100 ON	H	L	L	H	L

WCDMA PA True Table 4-2

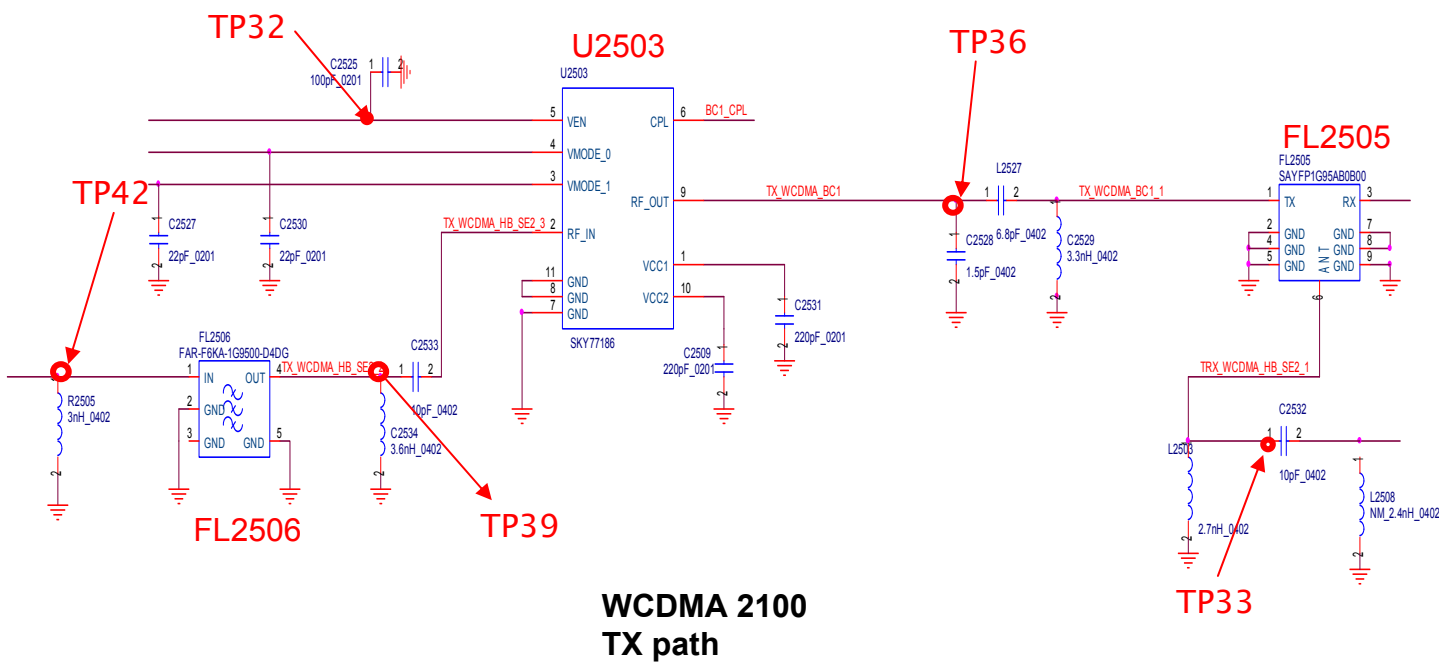
RF TROUBLE SHOOTING

Circuit Diagram

Main Board



WCDMA 1900
TX path

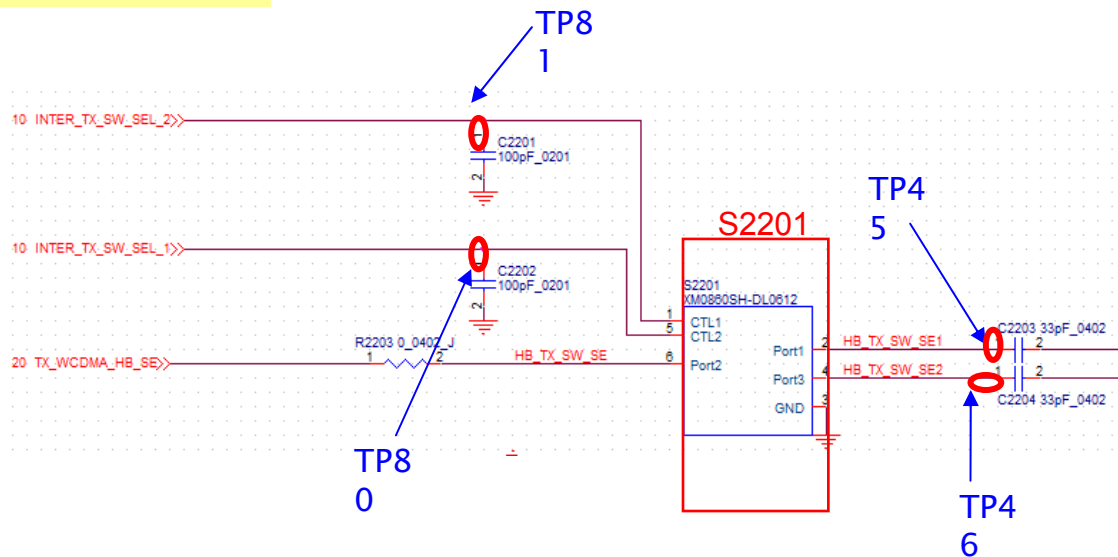


WCDMA 2100
TX path

RF TROUBLE SHOOTING

Circuit Diagram

Main Board



WCDMA PA STATE	TP3 PA_ON_0	TP2 PA_ON_1	TP3 PA_ON_2
OFF	L	L	L
WCDMA850 ON	L	H	L
WCDMA1900 ON	L	L	H
WCDMA2100 ON	H	L	L

WCDMA PA True Table 4-2

POWER MODE	ENABLE	TP3 PA_R0(Vmod1)	TP2 PA_R1(Vmod0)	VCC
Power Down Mode	L	L	L	ON
Standby Mode	L	don't care	don't care	ON
LOW POWER	H	H	H	ON
MEDIUM POWER	H	L	H	ON
HIGH POWER	H	L	L	ON
Optional Lower Vcc Mode	H	L	L	1.5V

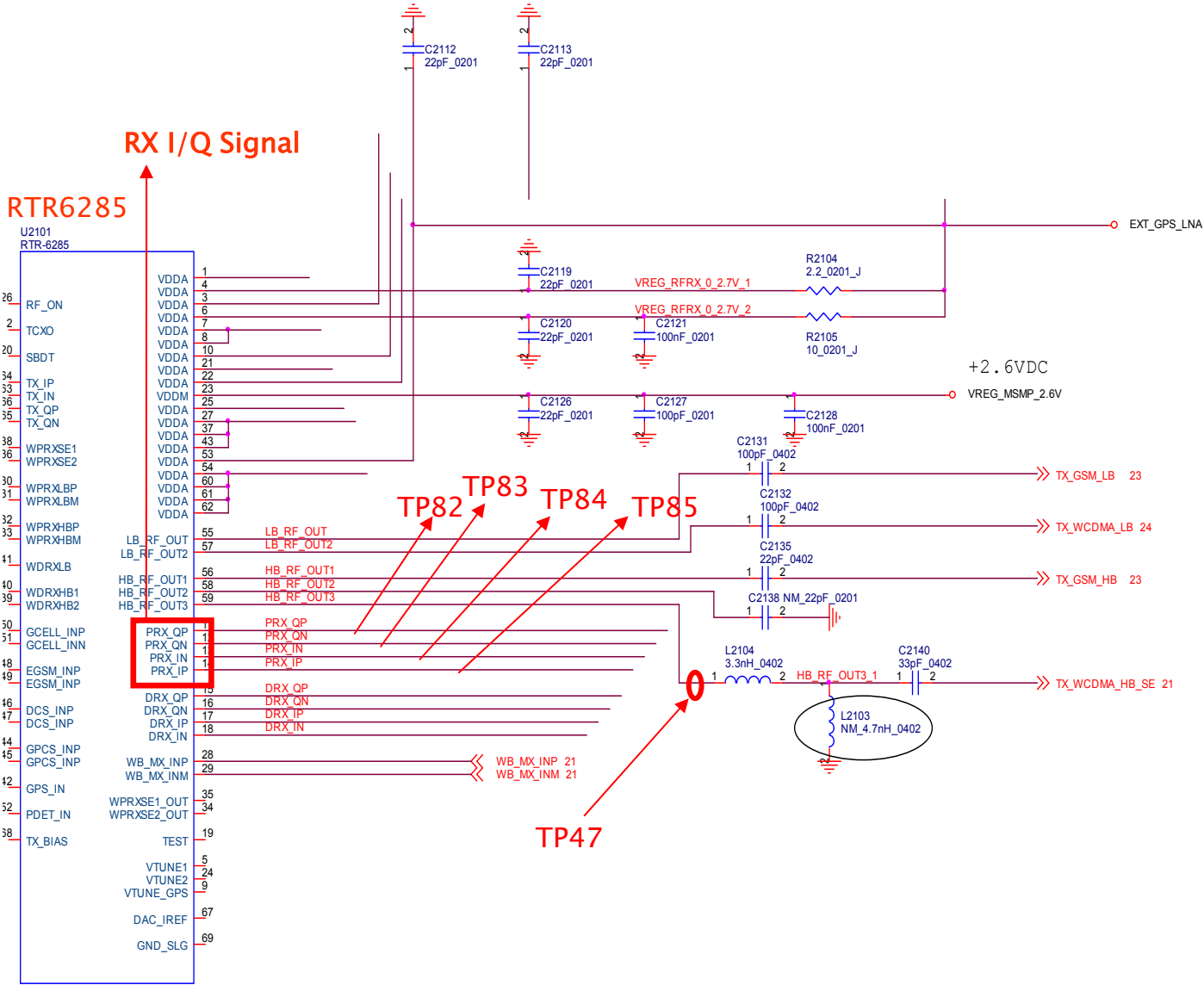
WCDMA PA True Table 4-3

WCDMA PA STATE	PA_ON_0	PA_ON_1	PA_ON_2	TP8 INTER_TX_SW_SEL_1 GPIO93	TP8 INTER_TX_SW_SEL_2 GPIO26
OFF	L	L	L	L	L
WCDMA850 ON	L	H	L	L	L
WCDMA1900 ON	L	L	H	L	H
WCDMA2100 ON	H	L	L	H	L

RF TROUBLE SHOOTING

Circuit Diagram

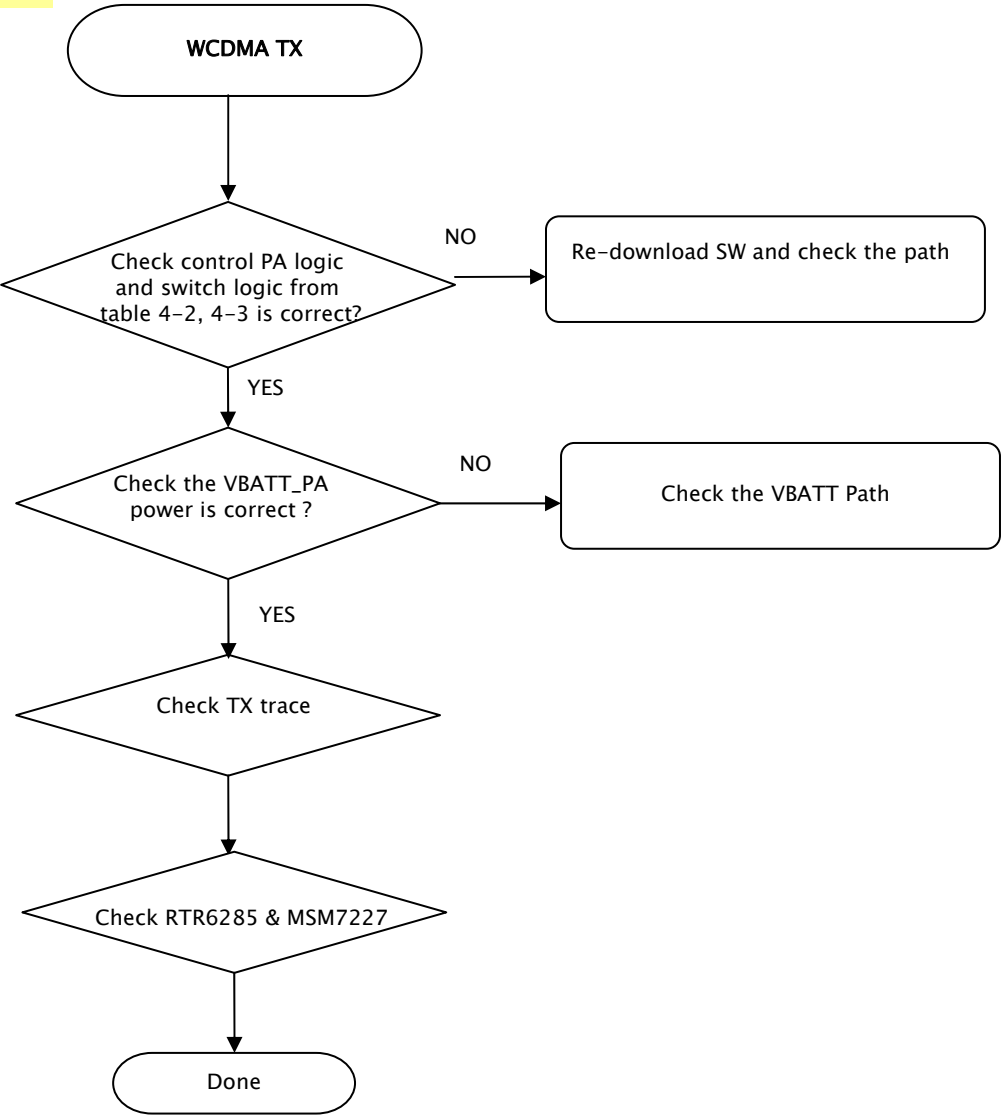
Main Board



RF TROUBLE SHOOTING

Checking Flow

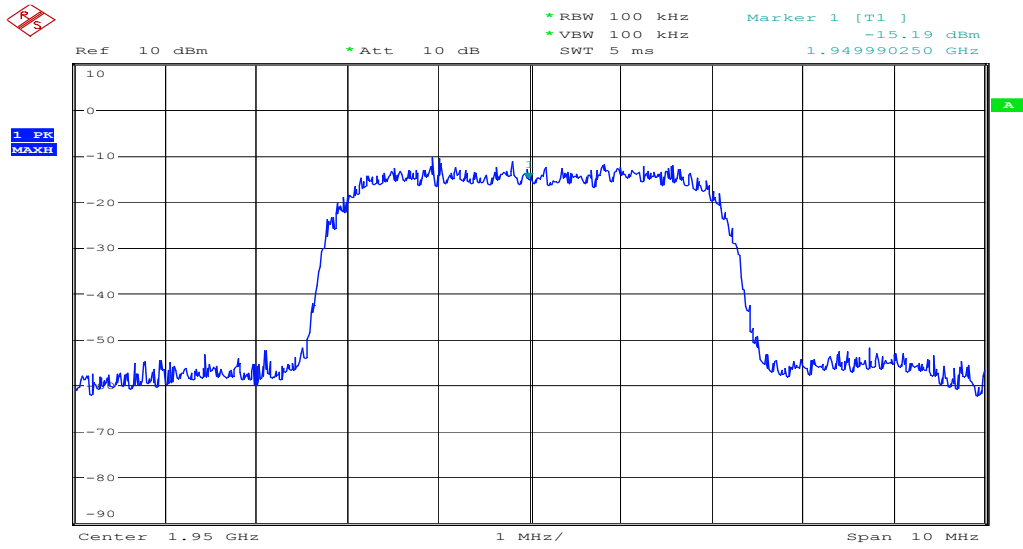
Main Board



Waveform

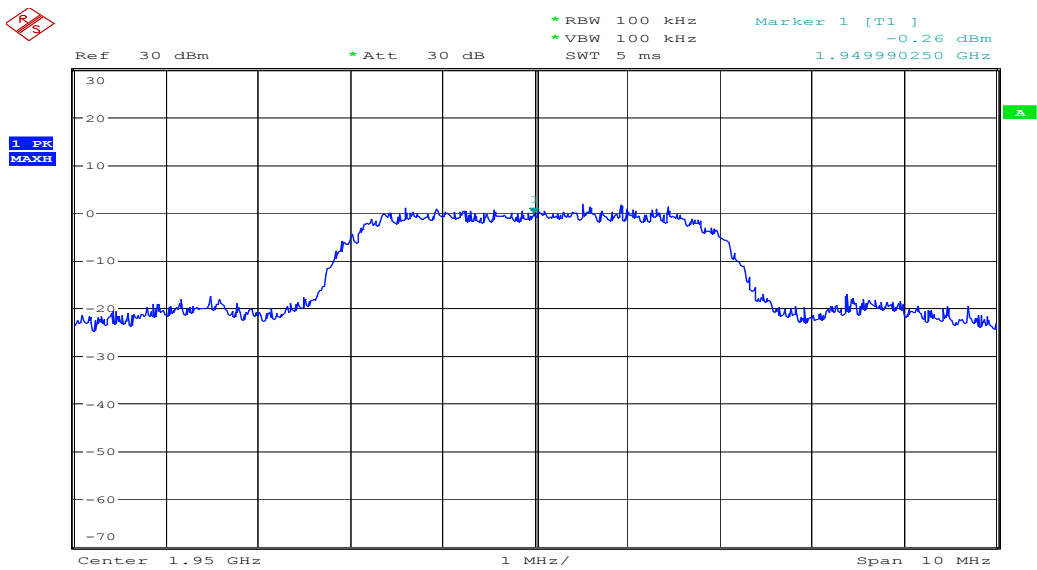
Use Test program to set TX on and measure picture as below.

TP5



Date: 17.NOV.2009 06:15:28

TP33 /TP34/ TP35

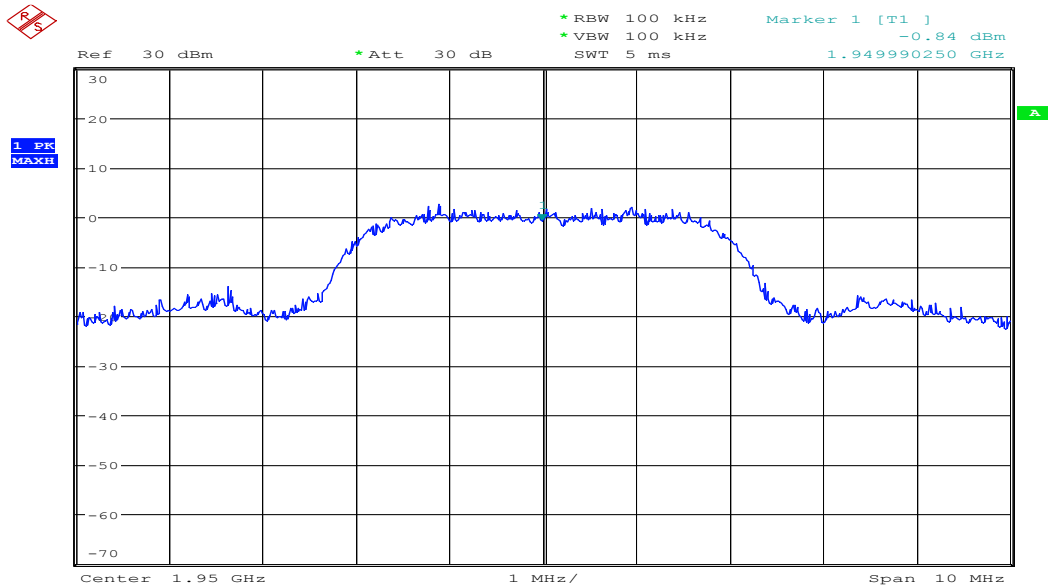


Date: 17.NOV.2009 06:18:09

Waveform

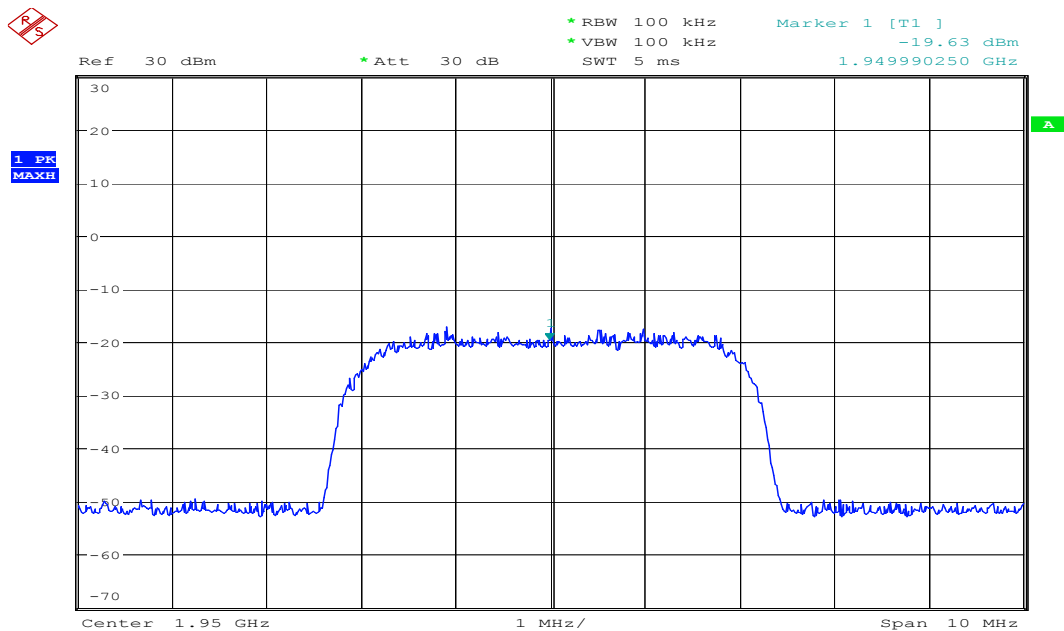
Use Test program to set TX on and measure picture as below.

TP36 /TP37 /TP38



Date: 17.NOV.2009 06:19:59

TP39 /TP40/ TP41

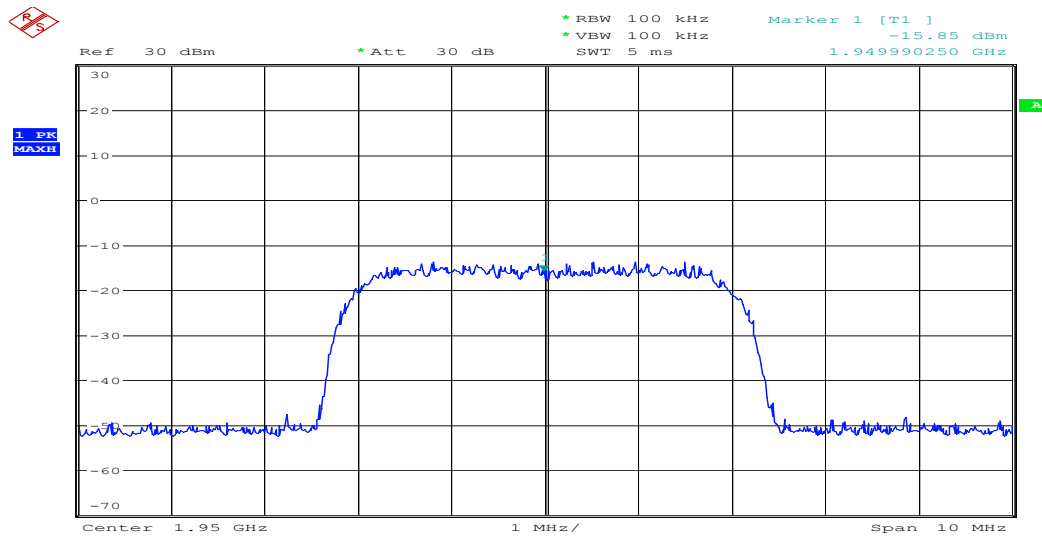


Date: 17.NOV.2009 06:21:19

Waveform

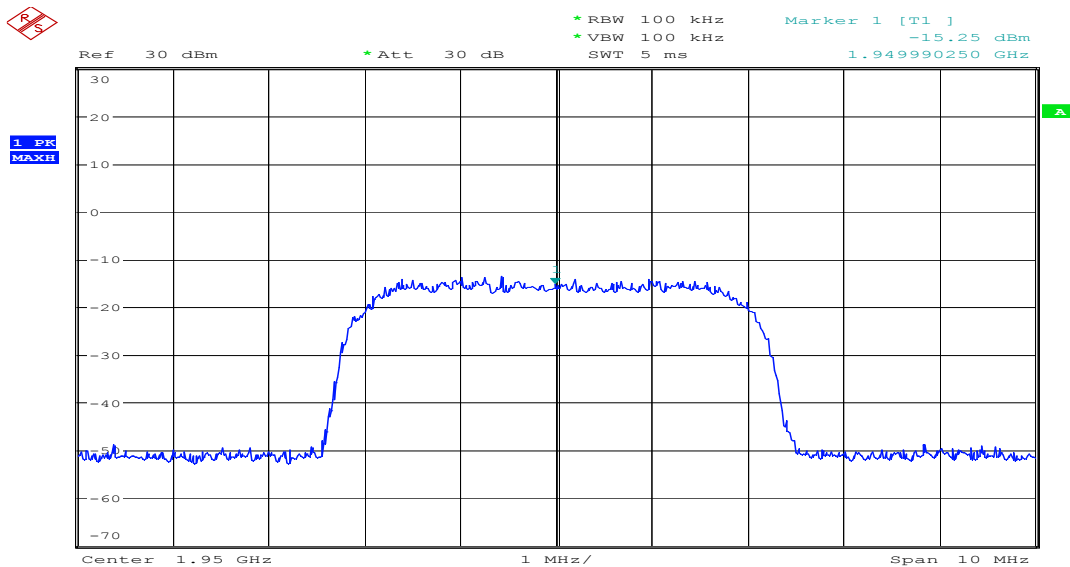
Use Test program to set TX on and measure picture as below.

TP42 /TP43 /TP44



Date: 17.NOV.2009 06:22:28

TP45 /TP46

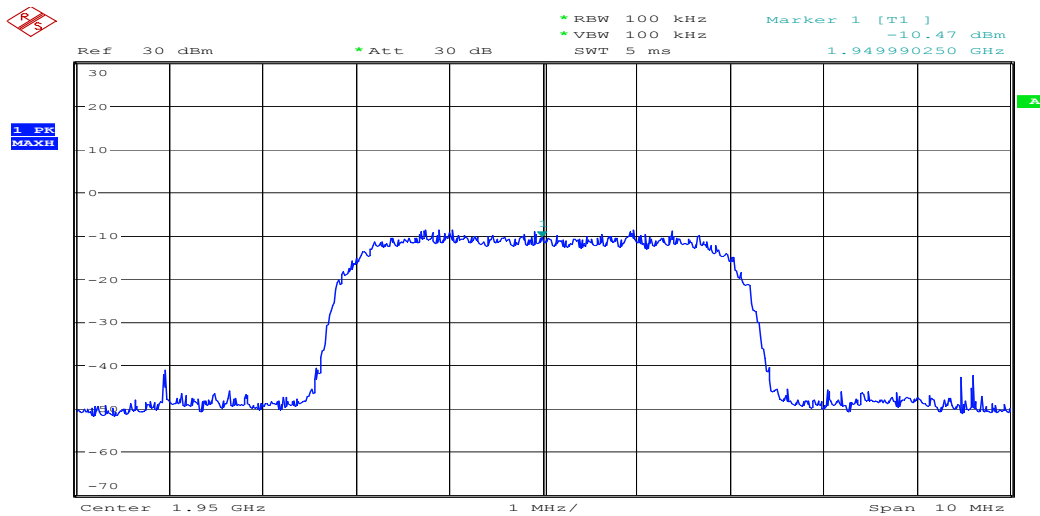


Date: 17.NOV.2009 06:25:18

Waveform

Use Test program to set TX on and measure picture as below.

TP47



Date: 17.NOV.2009 06:27:14

Waveform

TP86 / TP87



TP88 / TP89

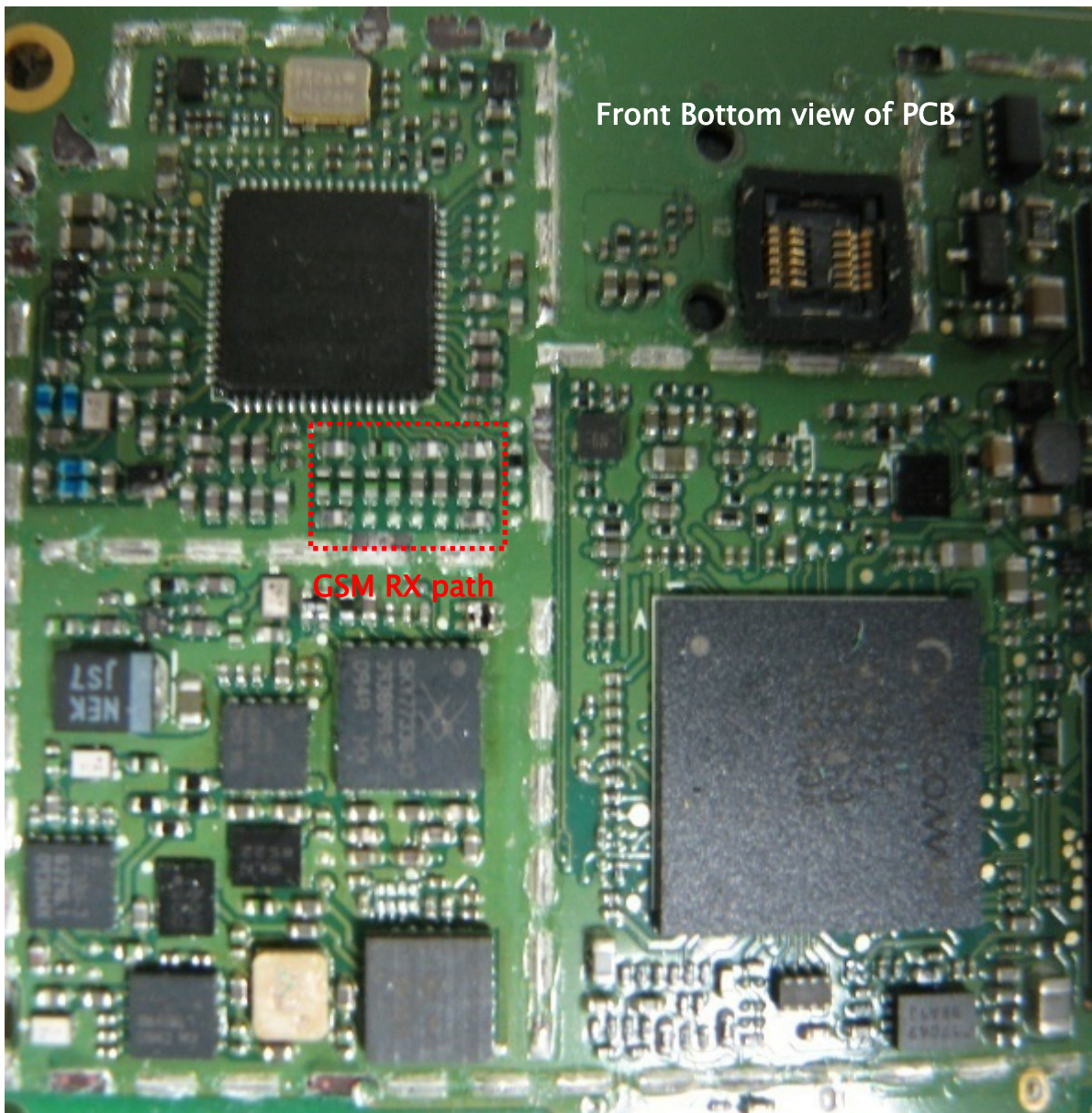


4.6 GSM RX Trouble

GSM RX Trouble

Picture Data

Main board top

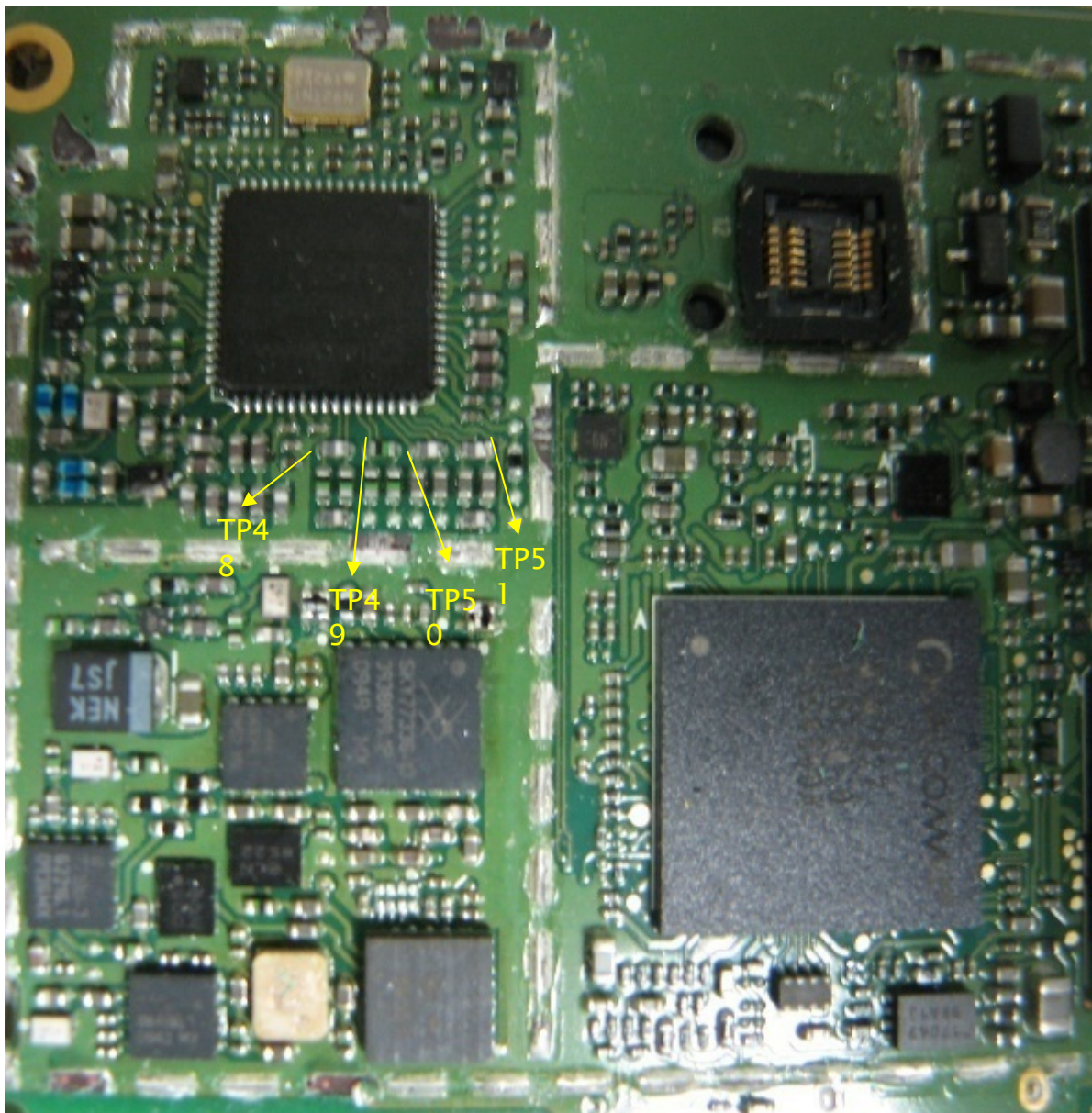


RF TROUBLE SHOOTING

GSM RX Trouble

Picture Data

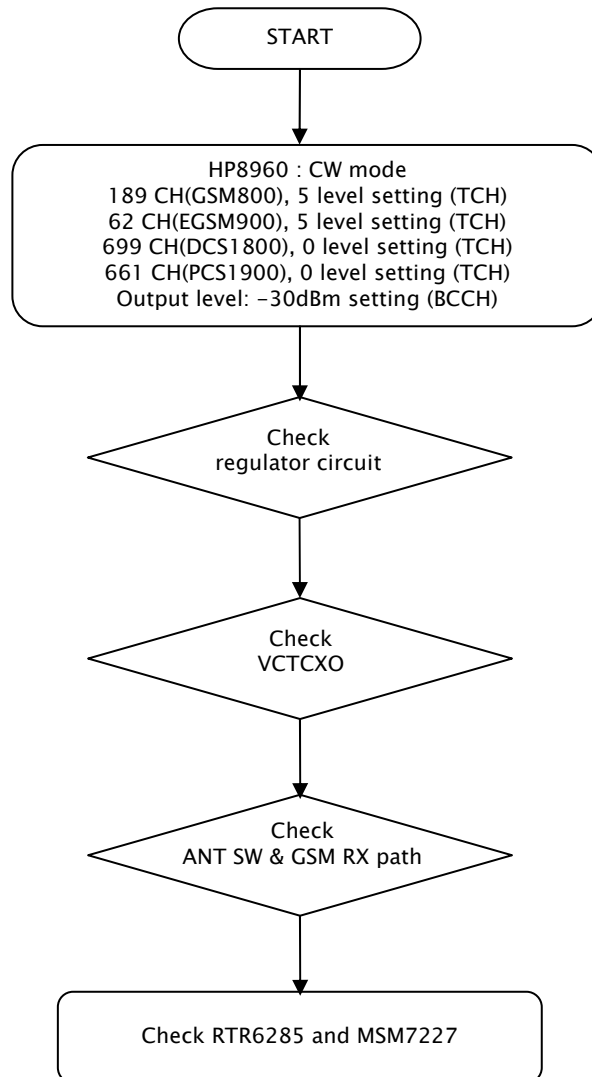
Main board top



RF TROUBLE SHOOTING

GSM RX Trouble

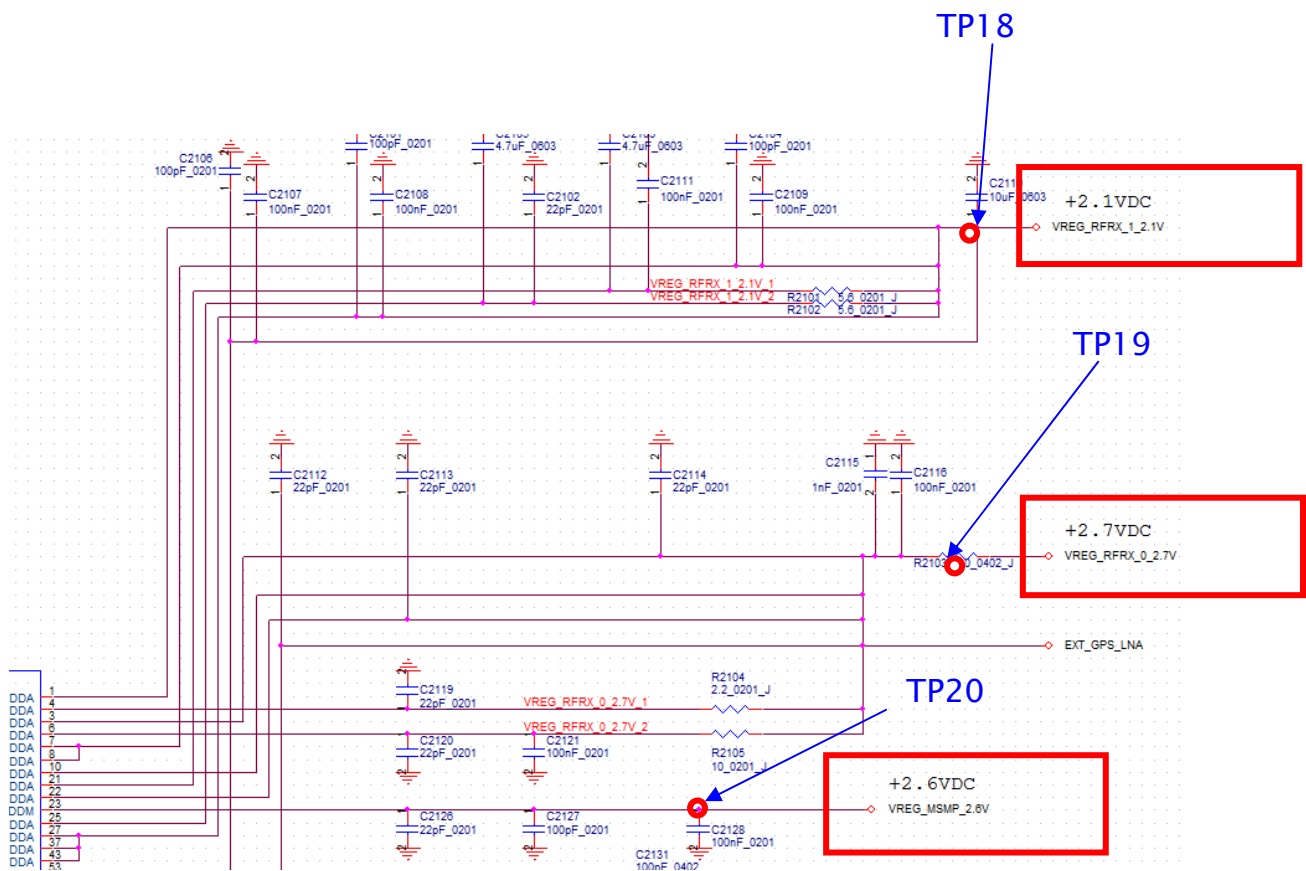
Checking Flow



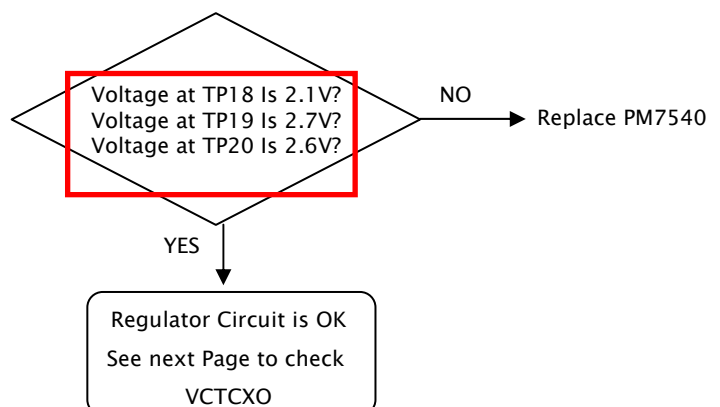
(1) Checking Regulator Circuit

Circuit Diagram

Main Board



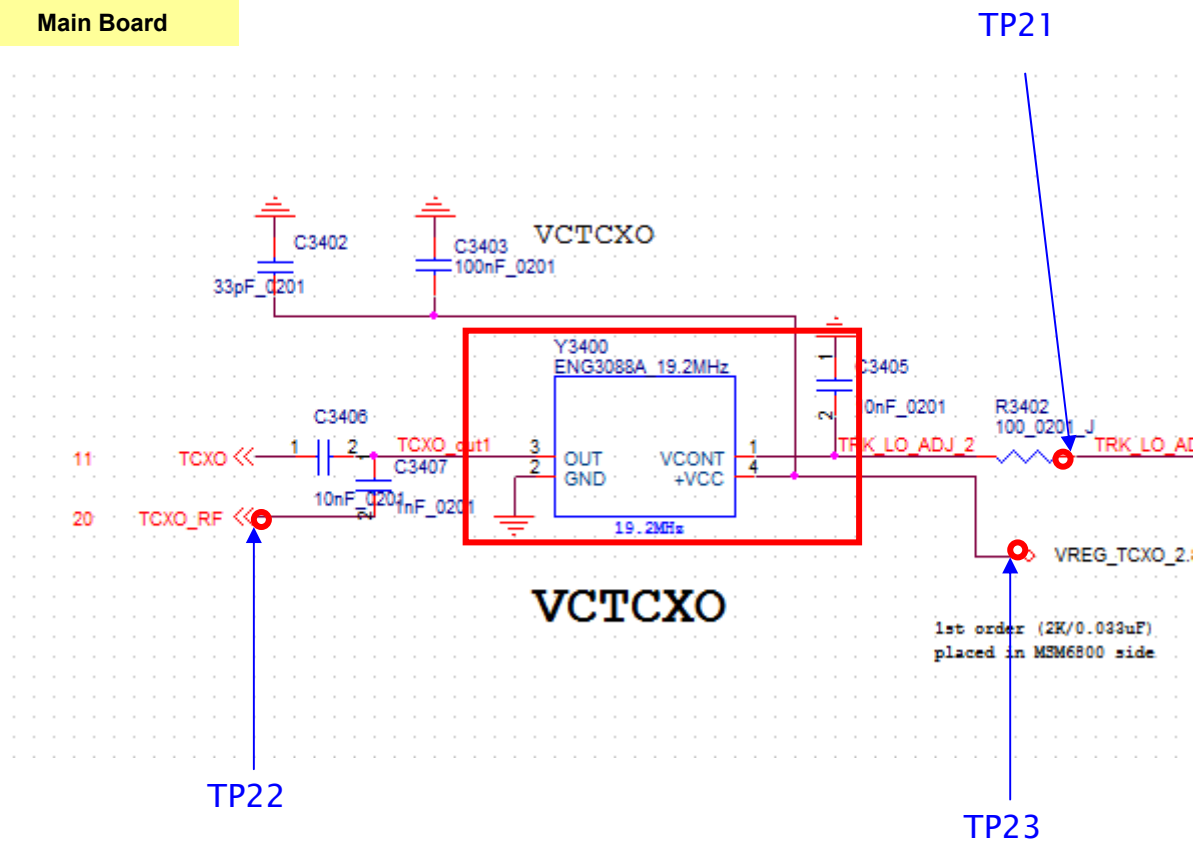
Checking Flow



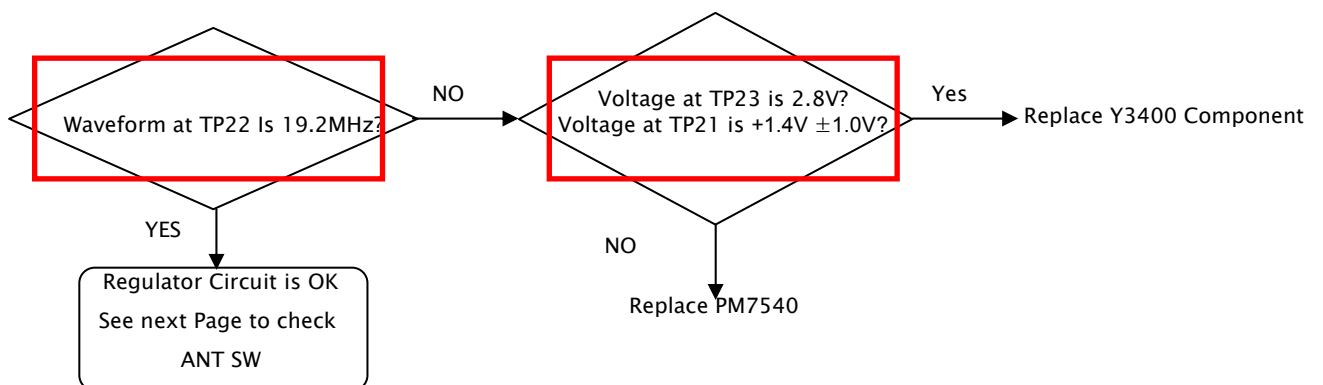
(2) Check VCTCXO

Circuit Diagram

Main Board



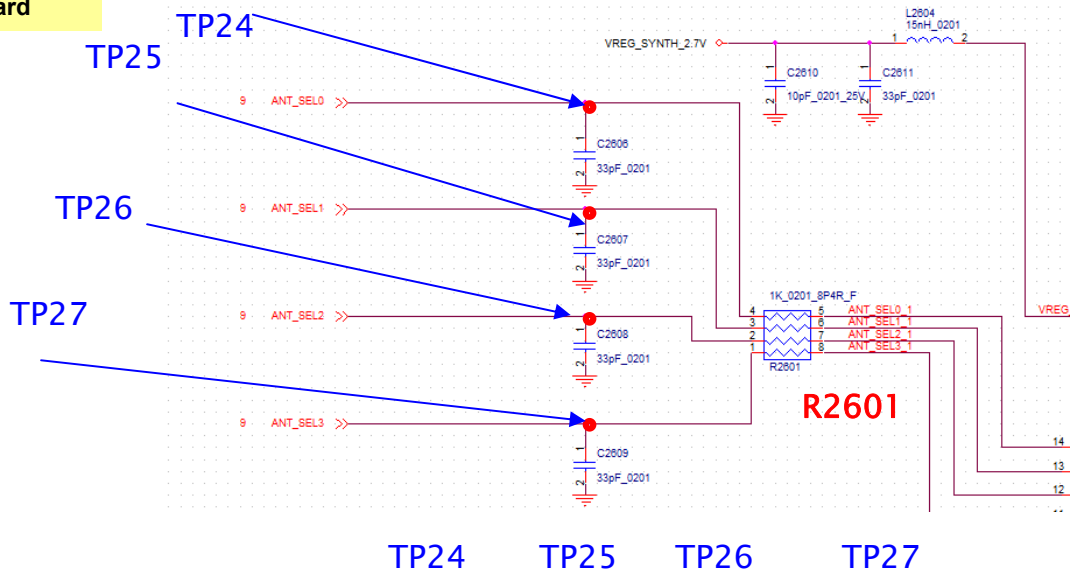
Checking Flow



(3) Checking Ant SW & RX path

Circuit Diagram

Main Board

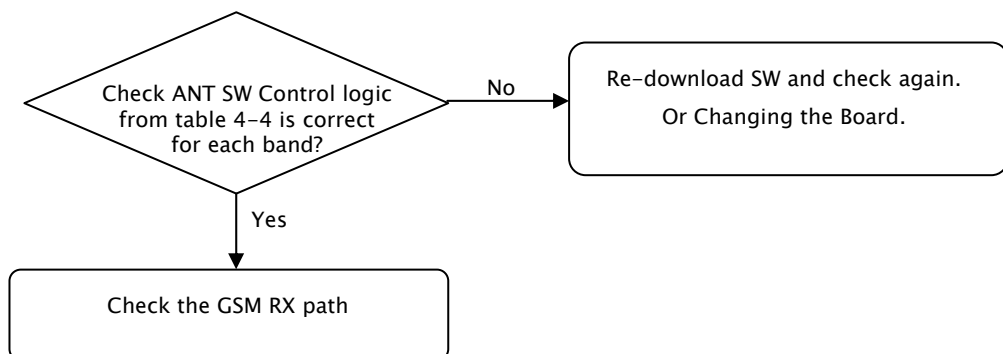


MODE	ANT_SEL0	ANT_SEL1	ANT_SEL2	ANT_SEL3
GSM850/EGSM900 TX	H	H	L	L
DCS1800/PCS1900 TX	H	L	L	L
GSM850 RX	L	H	H	L
EGSM900 RX	L	H	L	L
DCS1800 RX	L	L	H	L
PCS1900 RX	L	L	L	L
WCDMA_2100_Band 1 (UMTS1)	H	L	H	L
WCDMA_1900_Band 2 (UMTS3)	H	H	H	L
WCDMA_850_Band 5 (UMTS2)	H	L	H	H

-1

Checking Flow

ANT SW Control Table 4-4

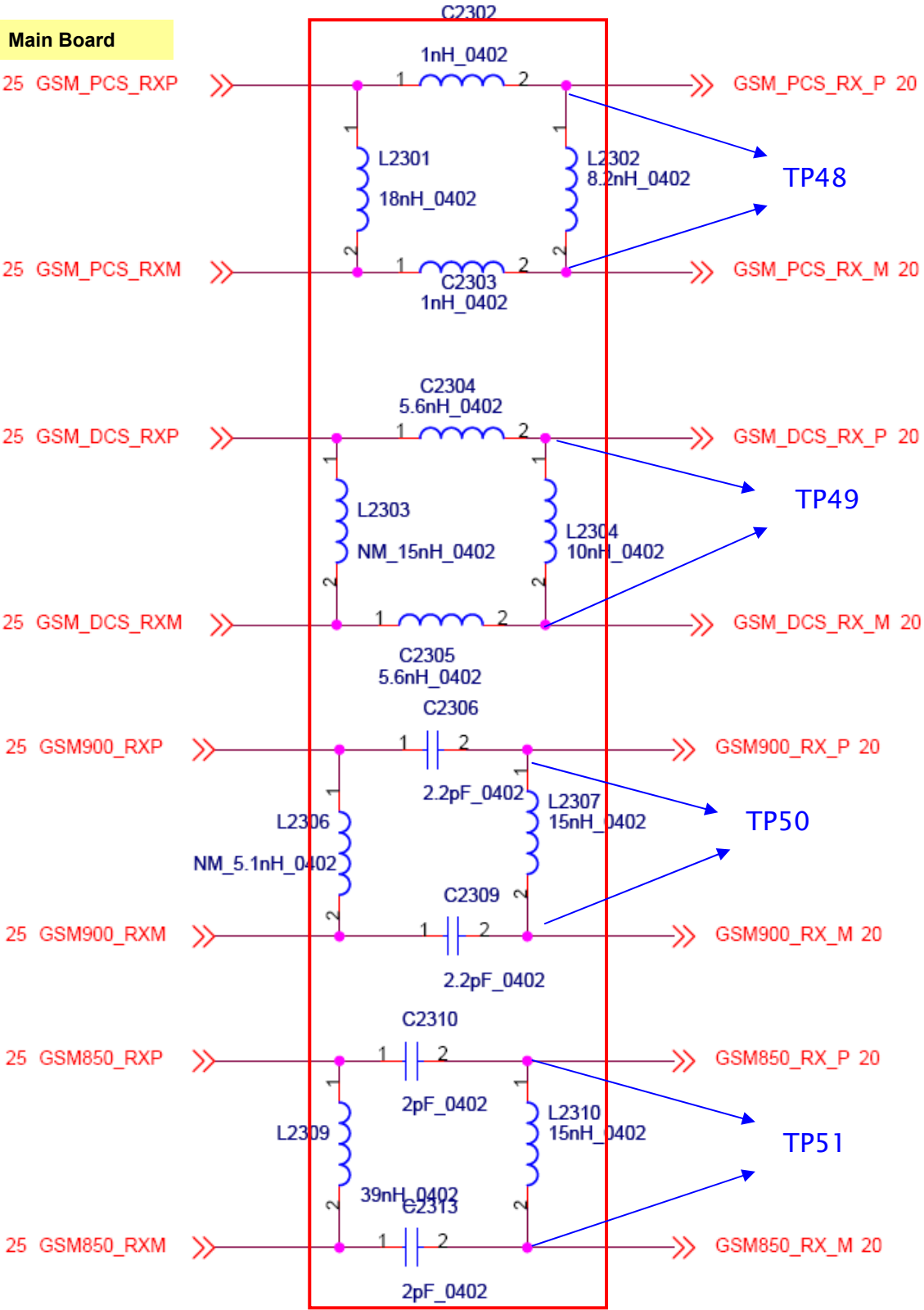


RF TROUBLE SHOOTING

Circuit Diagram

GSM RX path

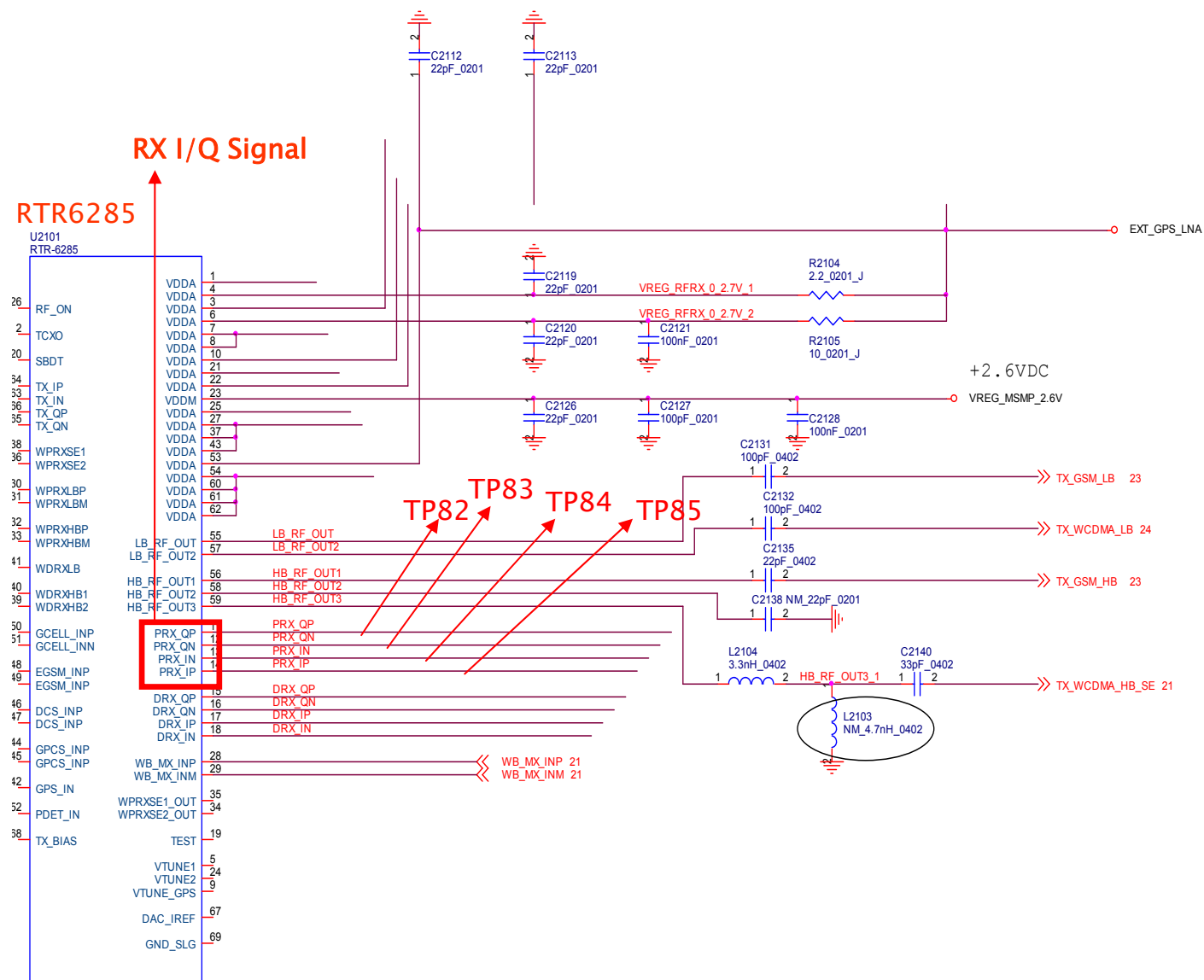
Main Board



RF TROUBLE SHOOTING

Circuit Diagram

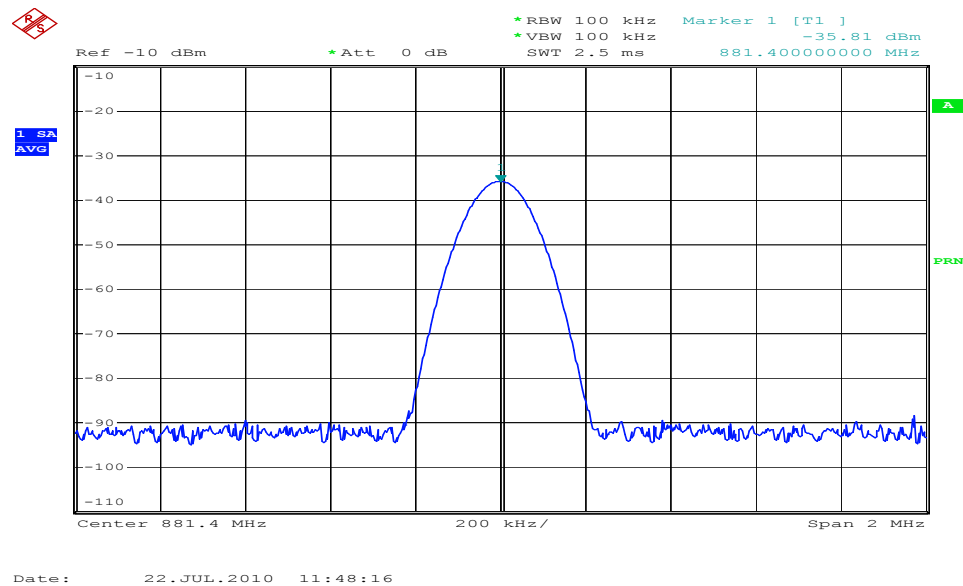
Main Board



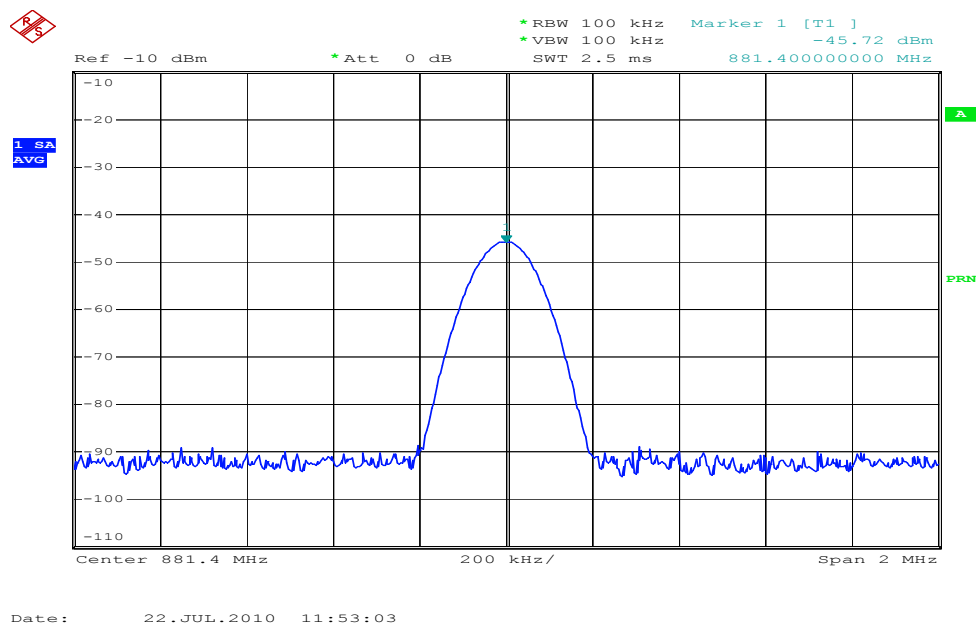
Waveform

Feed CW to RF connector and check waveform of RX path as below.

TP5

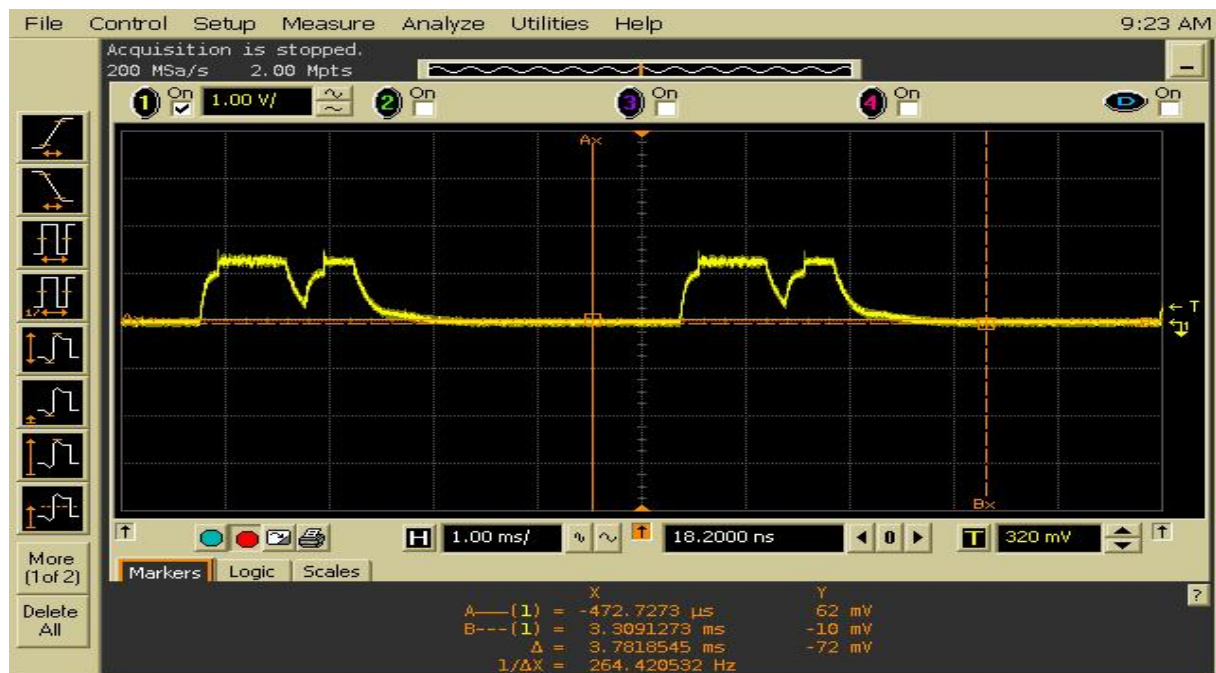


TP48 /TP49 /TP50 /TP51



Waveform

TP82 / TP83



TP84 / TP85

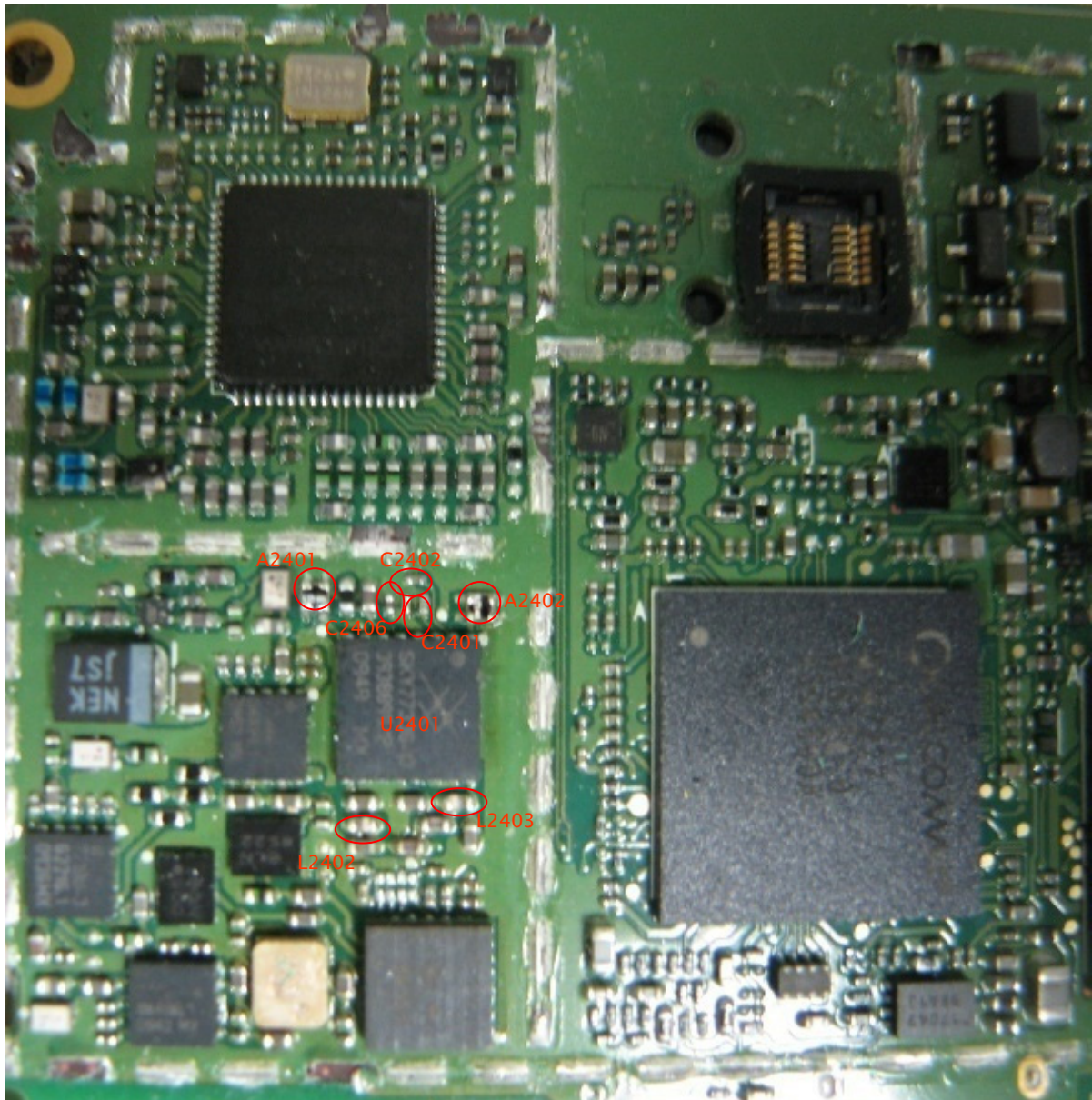


4.7 GSM TX Trouble

GSM TX Trouble

Picture Data

Main board top

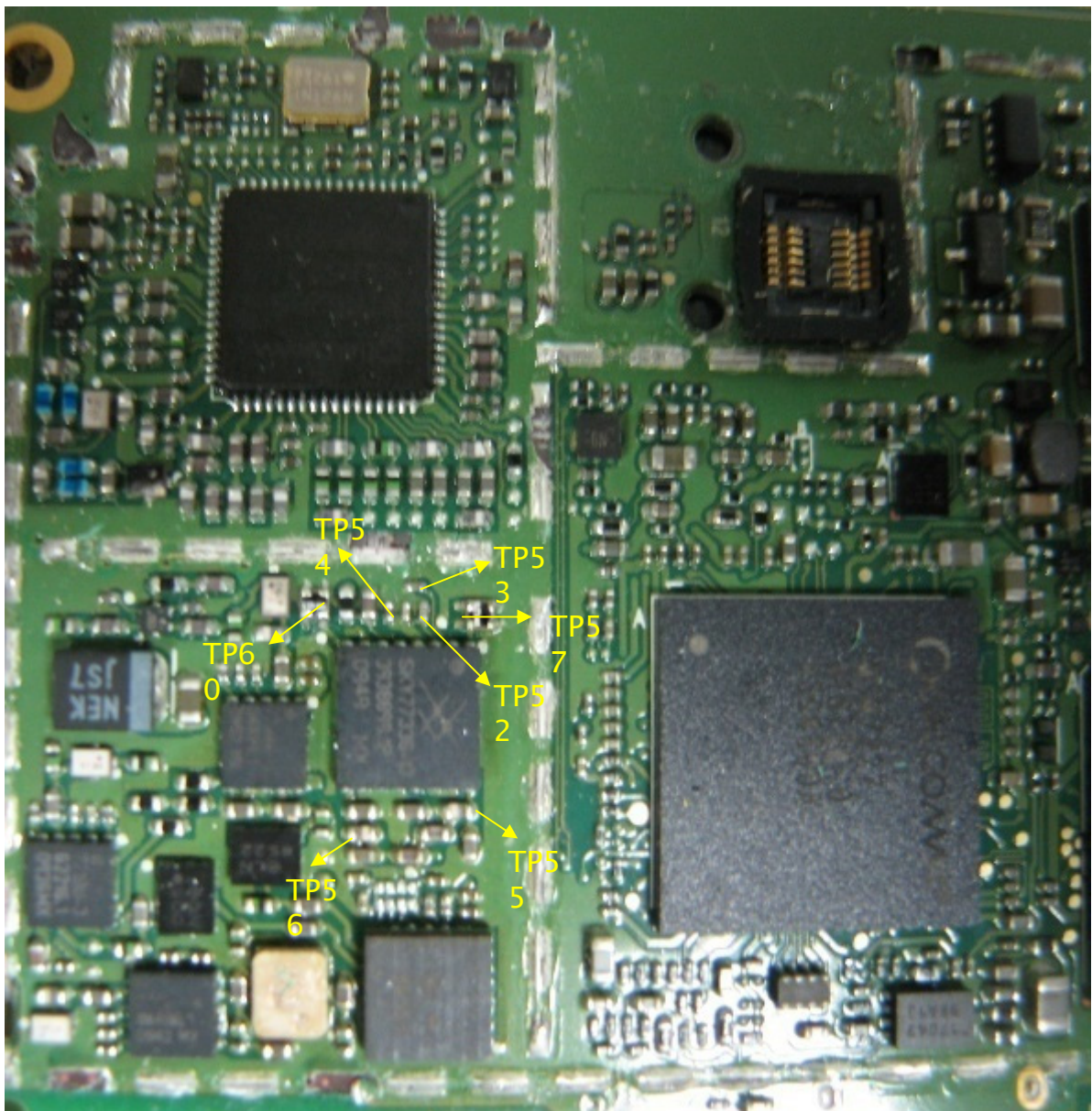


RF TROUBLE SHOOTING

GSM TX Trouble

Picture Data

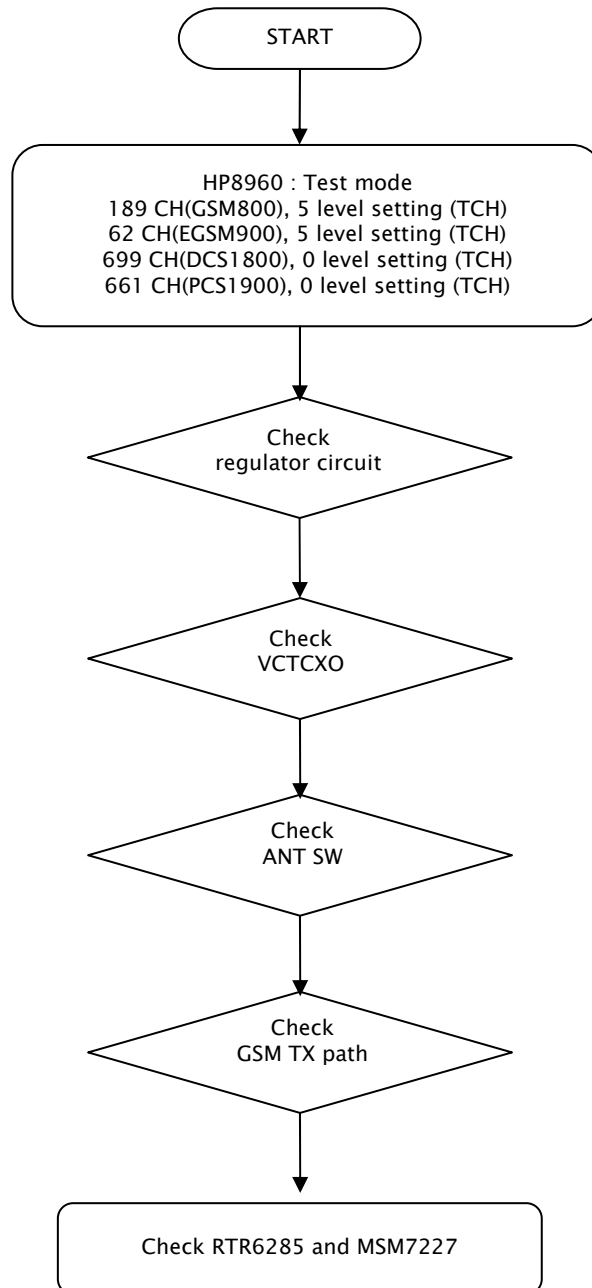
Main board top



RF TROUBLE SHOOTING

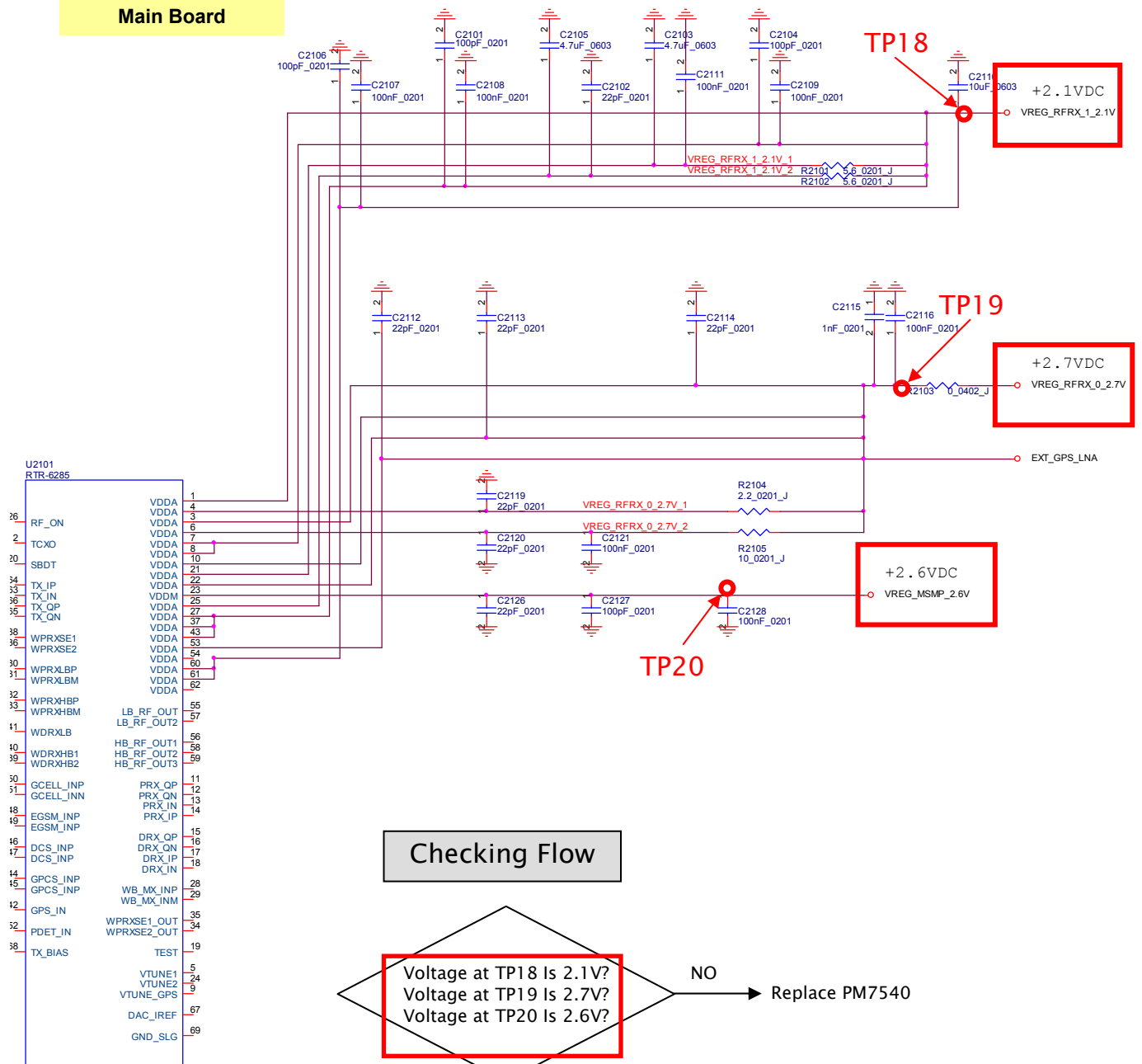
GSM TX Trouble

Checking Flow



Circuit Diagram

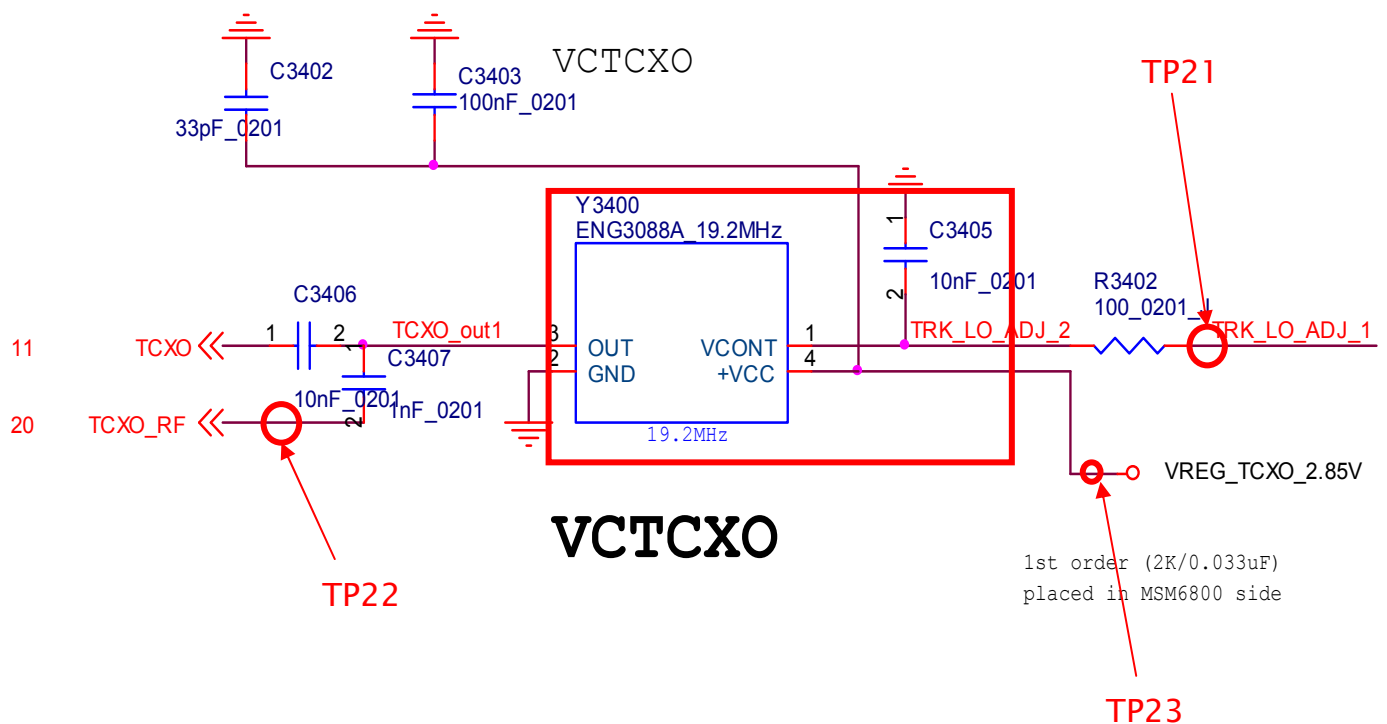
Main Board



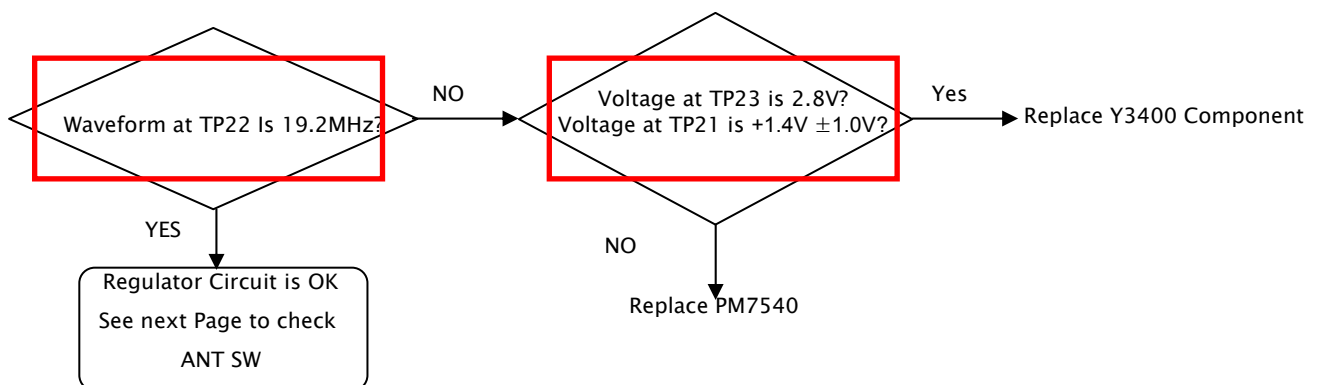
(2) Check VCTCXO

Circuit Diagram

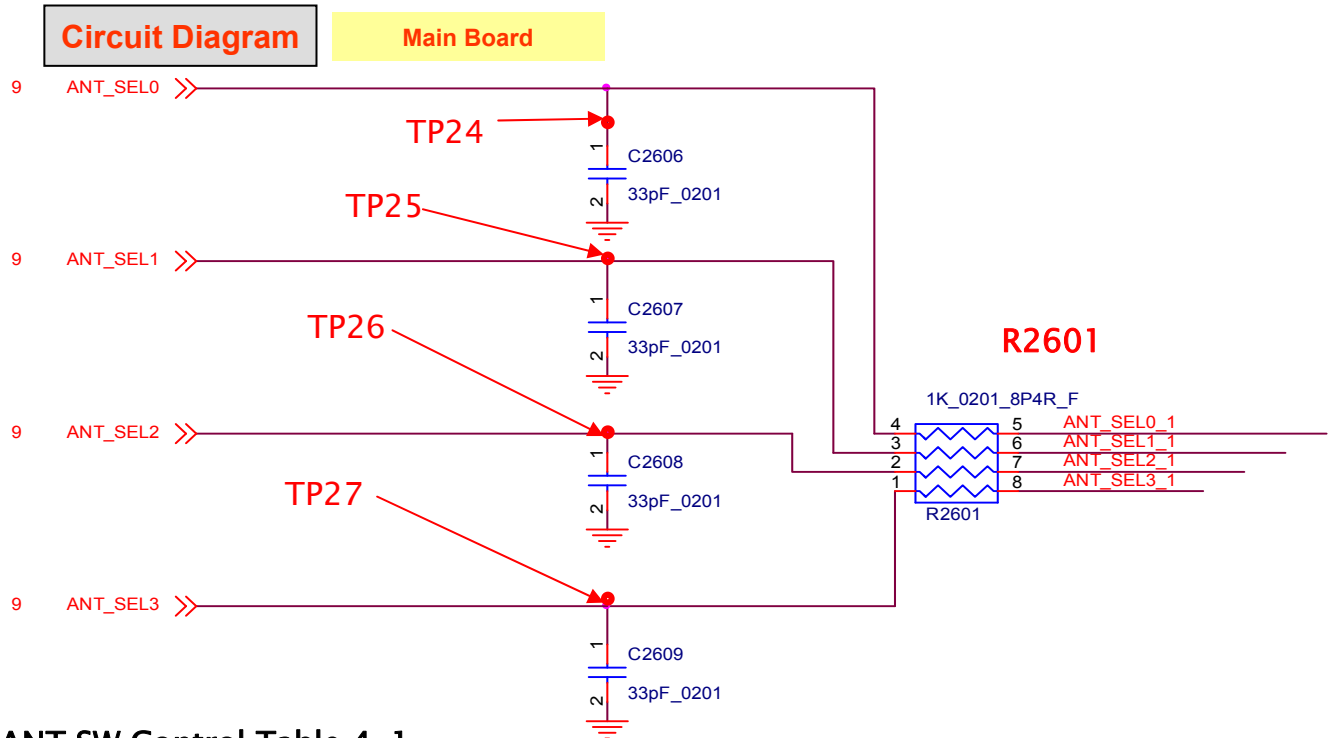
Main Board



Checking Flow



(3) Checking Ant SW & RX path

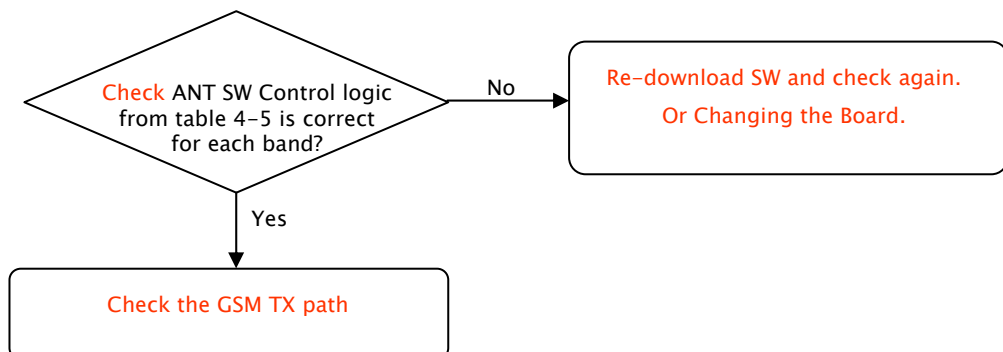


ANT SW Control Table 4-1

MODE	TP24 ANT_SEL0	TP25 ANT_SEL1	TP26 ANT_SEL2	TP27 ANT_SEL3
GSM850/EGSM900 TX	H	H	L	L
DCS1800/PCS1900 TX	H	L	L	L
GSM850 RX	L	H	H	L
EGSM900 RX	L	H	L	L
DCS1800 RX	L	L	H	L
PCS1900 RX	L	L	L	L
WCDMA_2100_Band 1 (UMTS1)	H	L	H	L
WCDMA_1900_Band 2 (UMTS3)	H	H	H	L
WCDMA_850_Band 5 (UMTS2)	H	L	H	H

Checking Flow

ANT SW Control Table 4-5

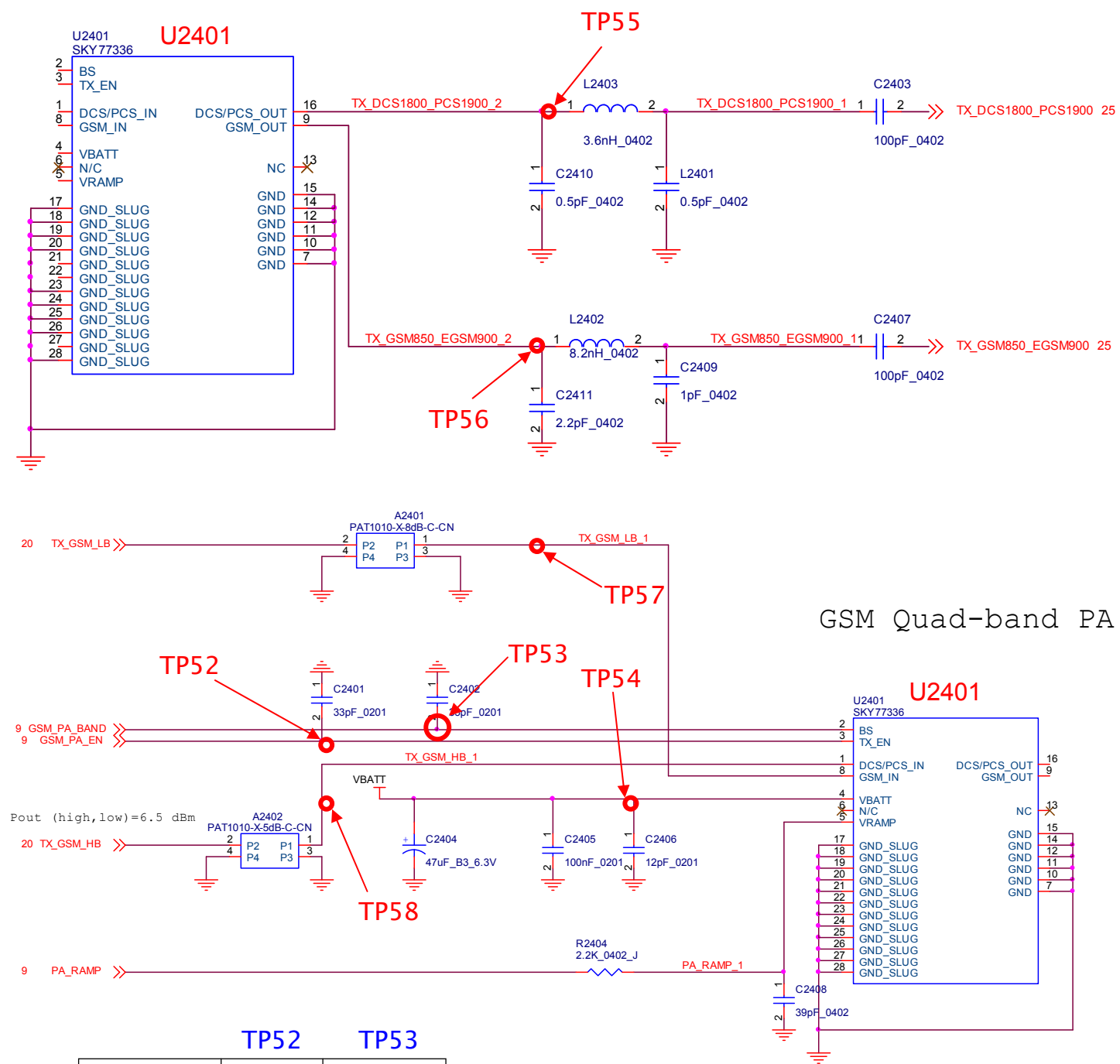


RF TROUBLE SHOOTING

(4) Checking GSM TX path

Circuit Diagram

Main Board



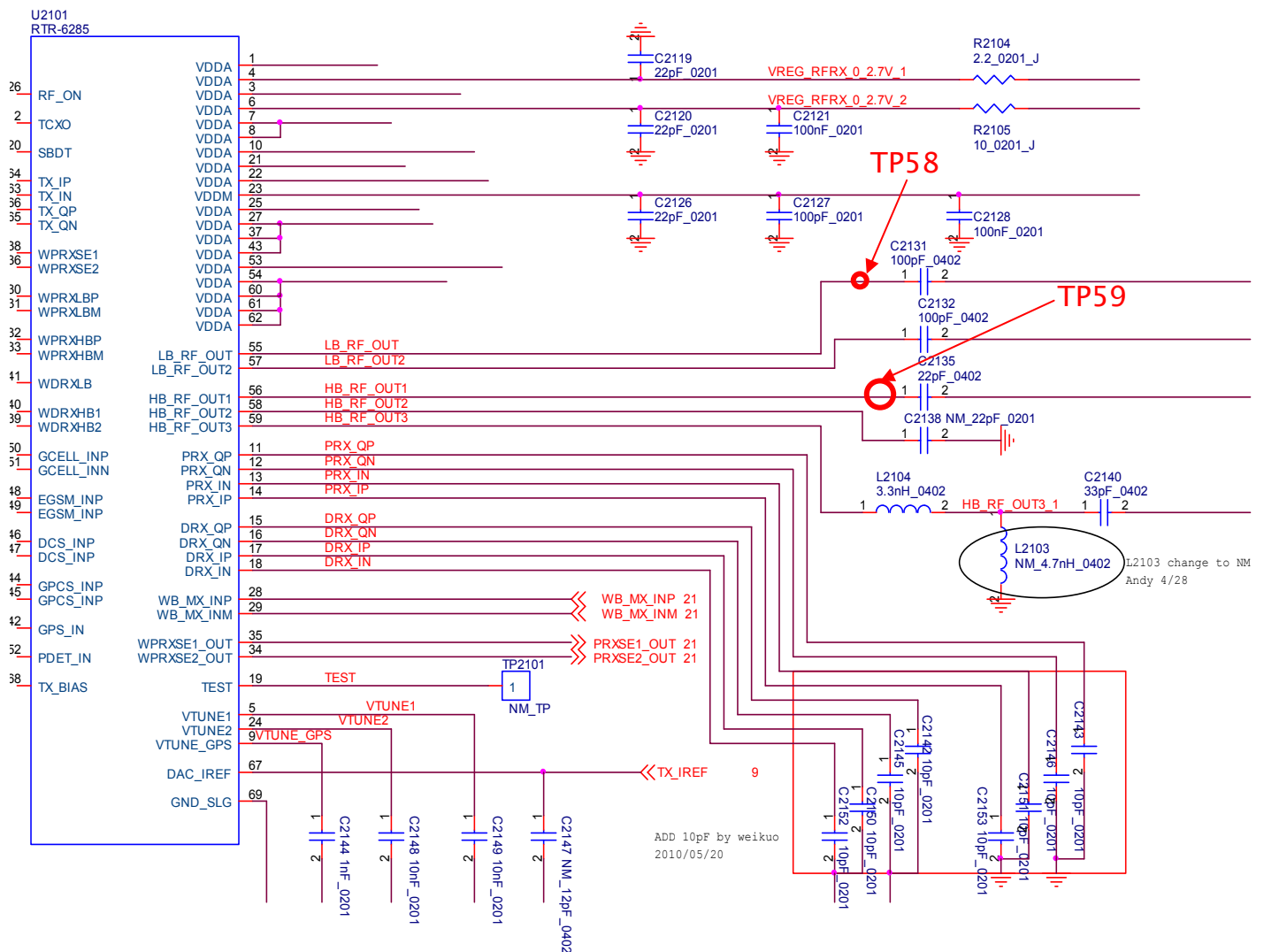
PA STATE	GSM_PA_EN	GSM_PA_BAND
Standby	L	L
TX GSM850/EGSM	H	L
TX DCS/PCS	H	H

GSM PA control true Table 4-6

Circuit Diagram

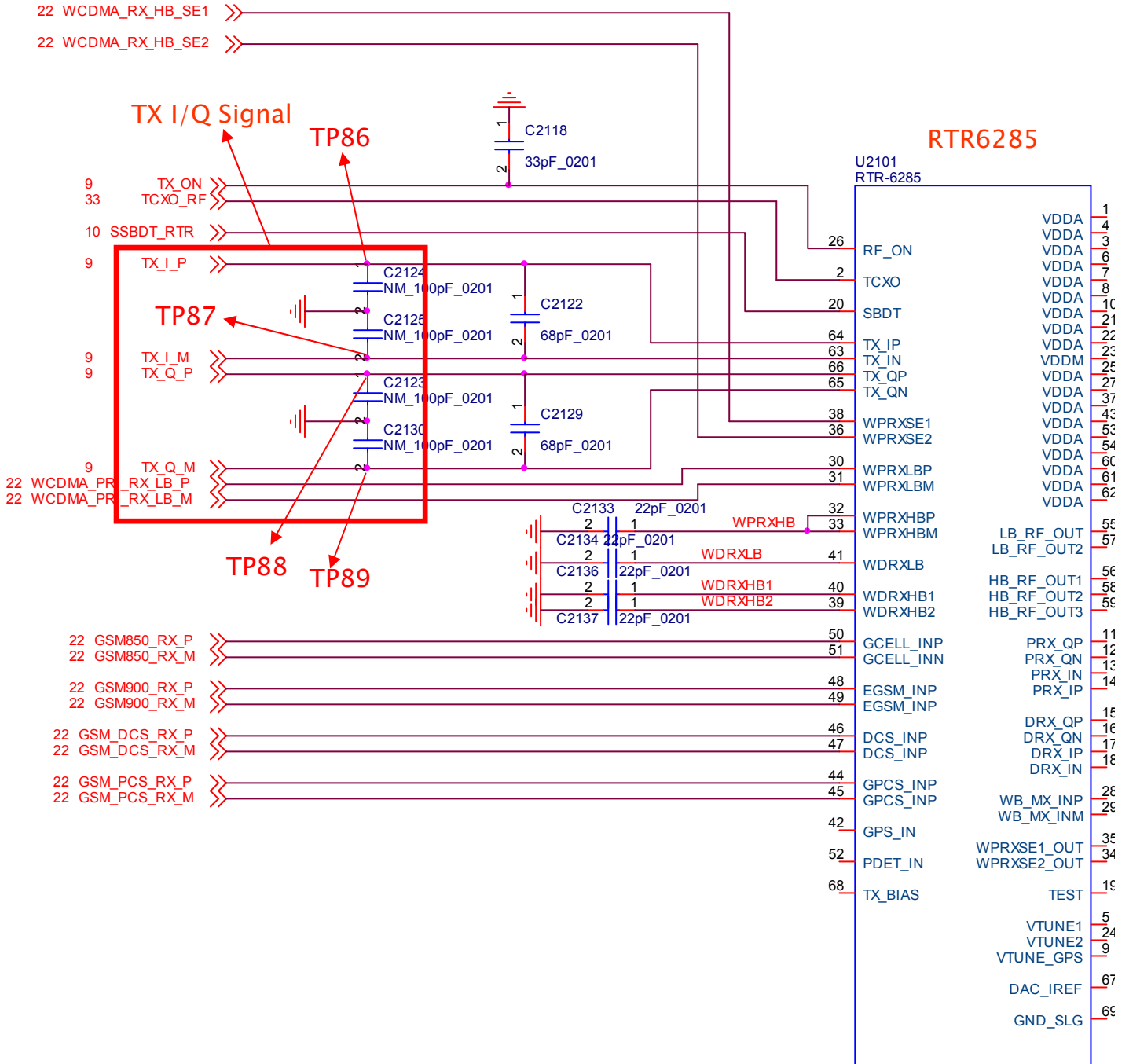
Main Board

RTR6285



Circuit Diagram

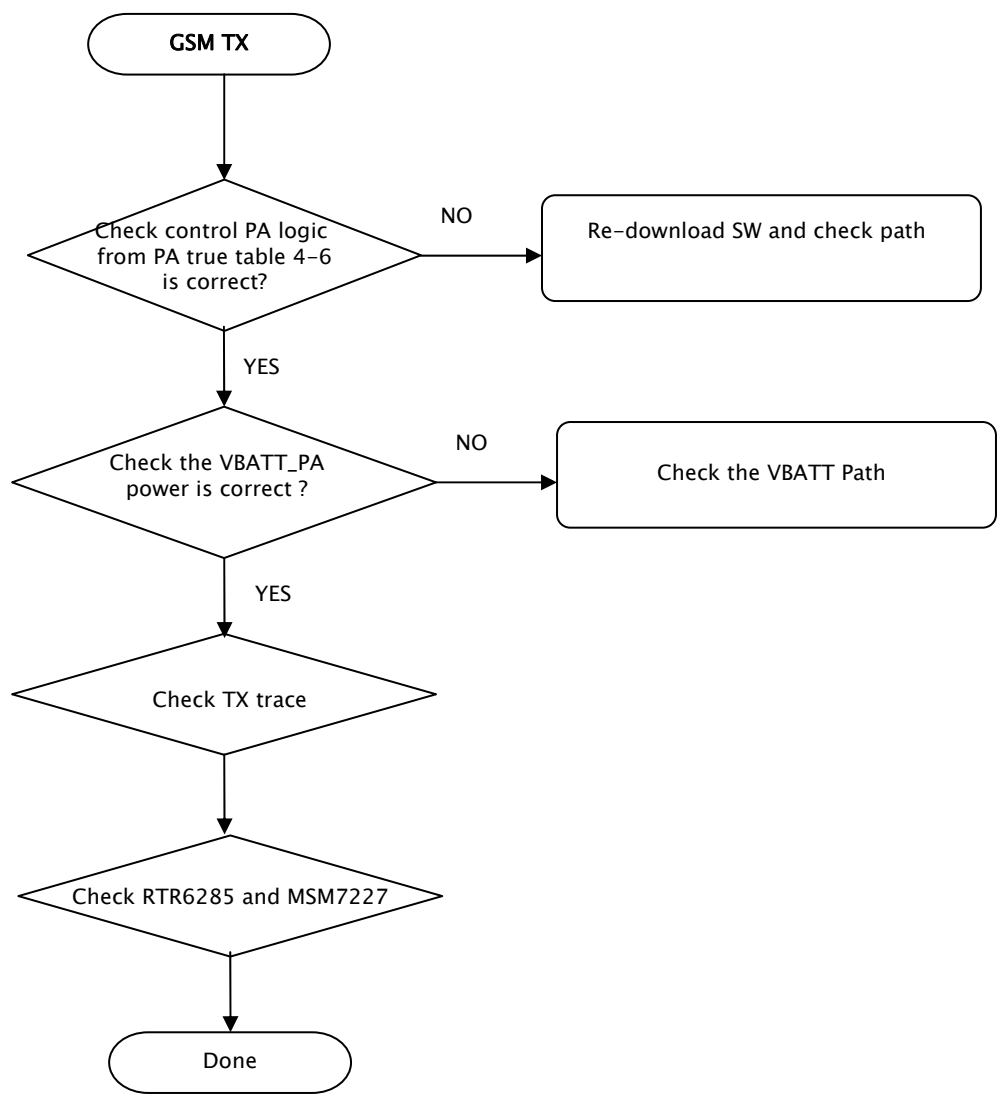
Main Board



RF TROUBLE SHOOTING

Checking Flow

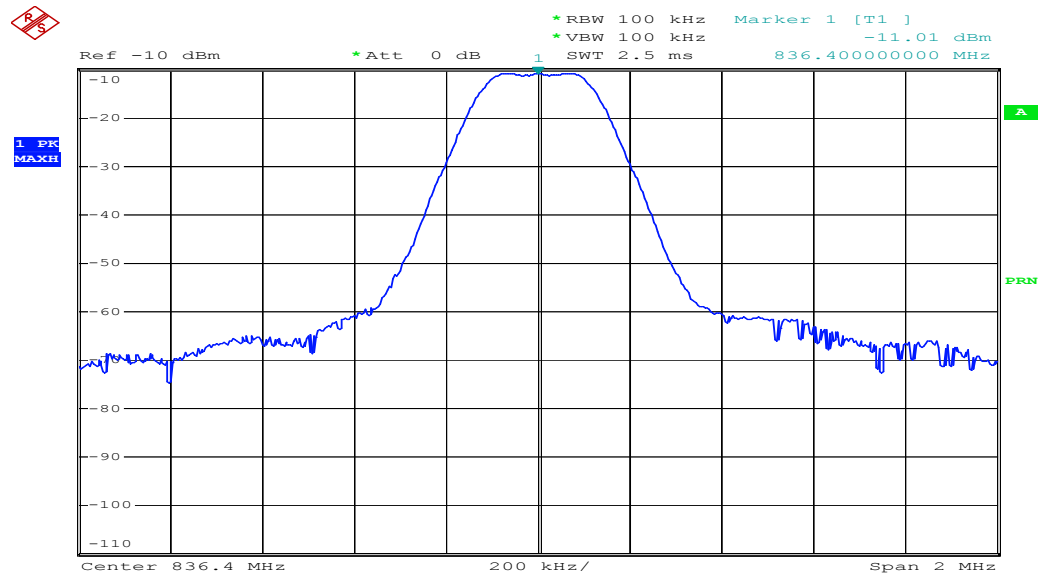
Main Board



Waveform

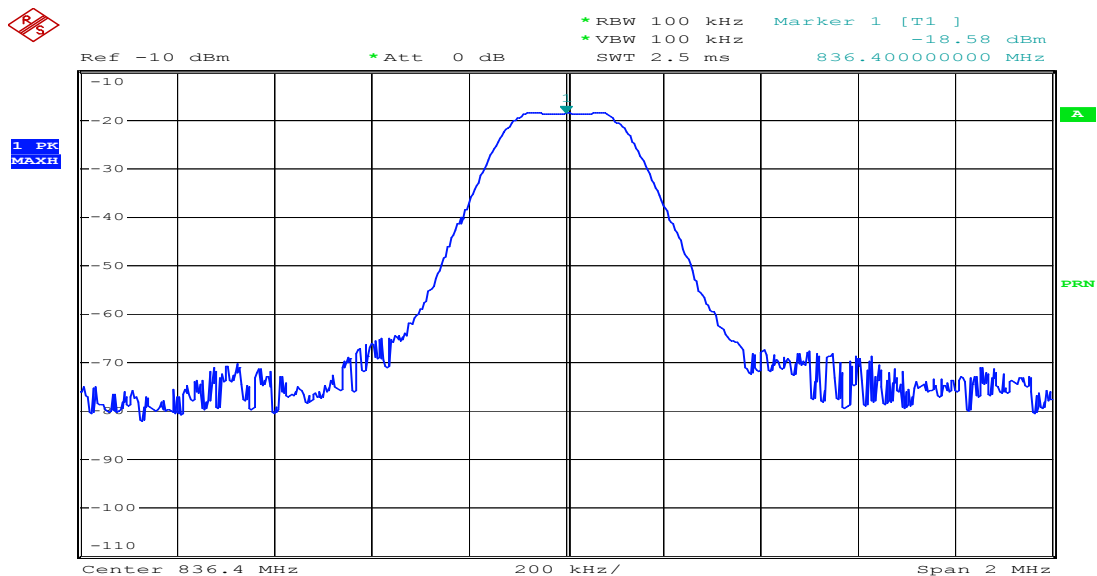
Use test program to set GSM TX power.

TP5



Date: 22.JUL.2010 12:02:35

TP55 / TP56

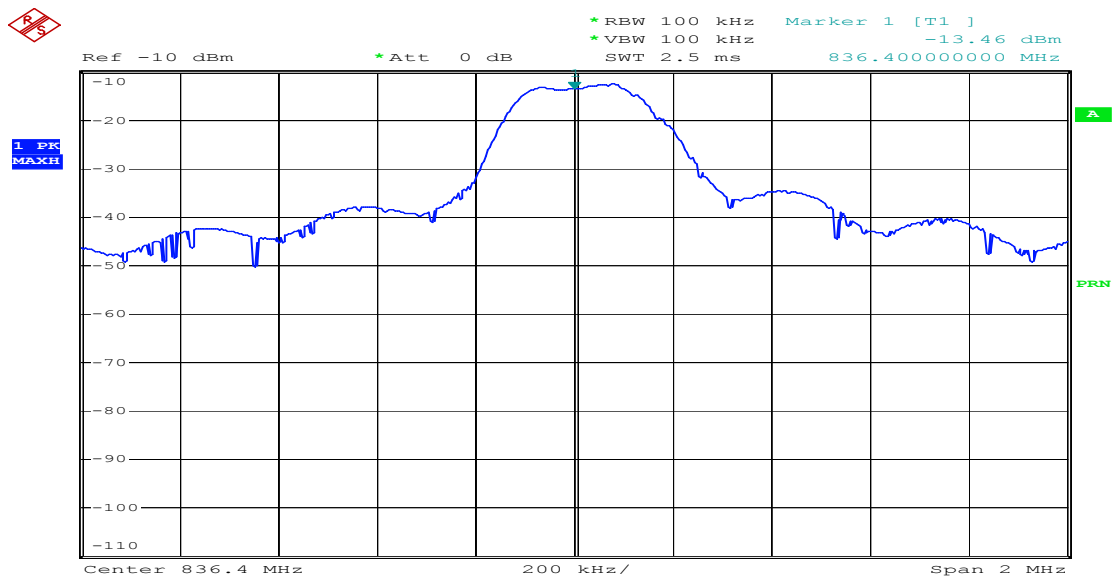


Date: 22.JUL.2010 12:07:36

Waveform

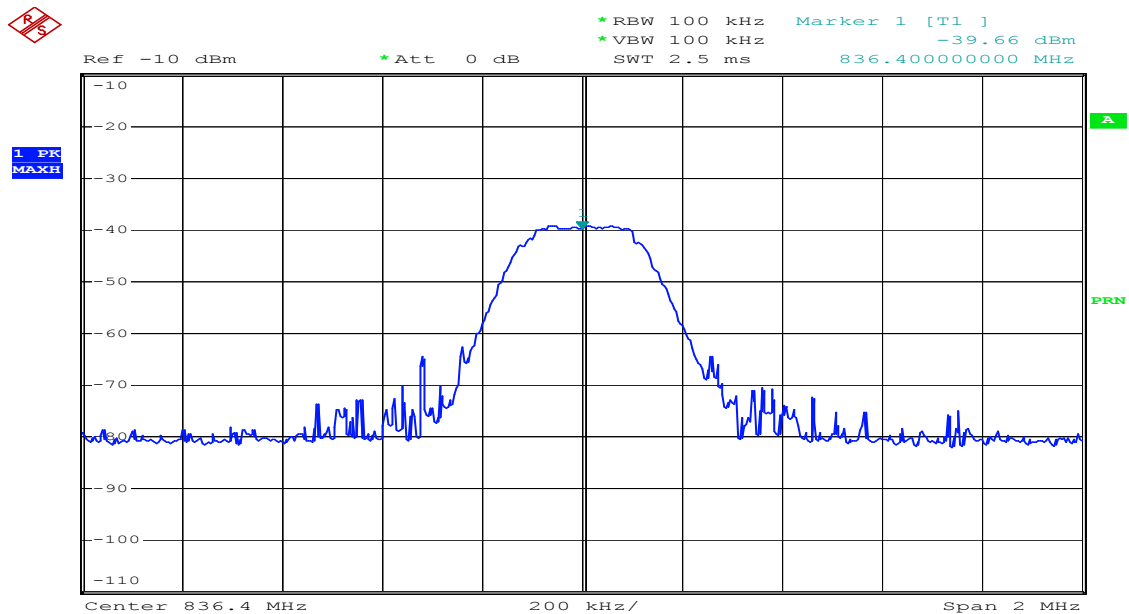
Use test program to set GSM TX power.

TP57



Date: 22.JUL.2010 12:09:33

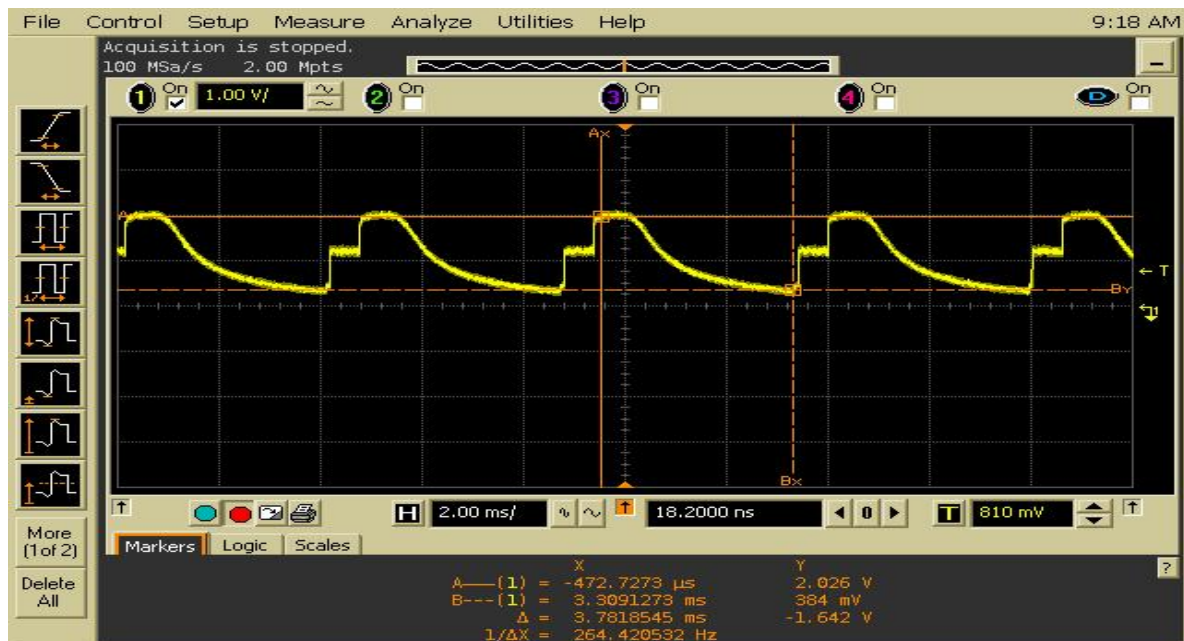
TP58 /TP59



Date: 22.JUL.2010 12:16:36

Waveform

TP86 / TP87



TP88 / TP89

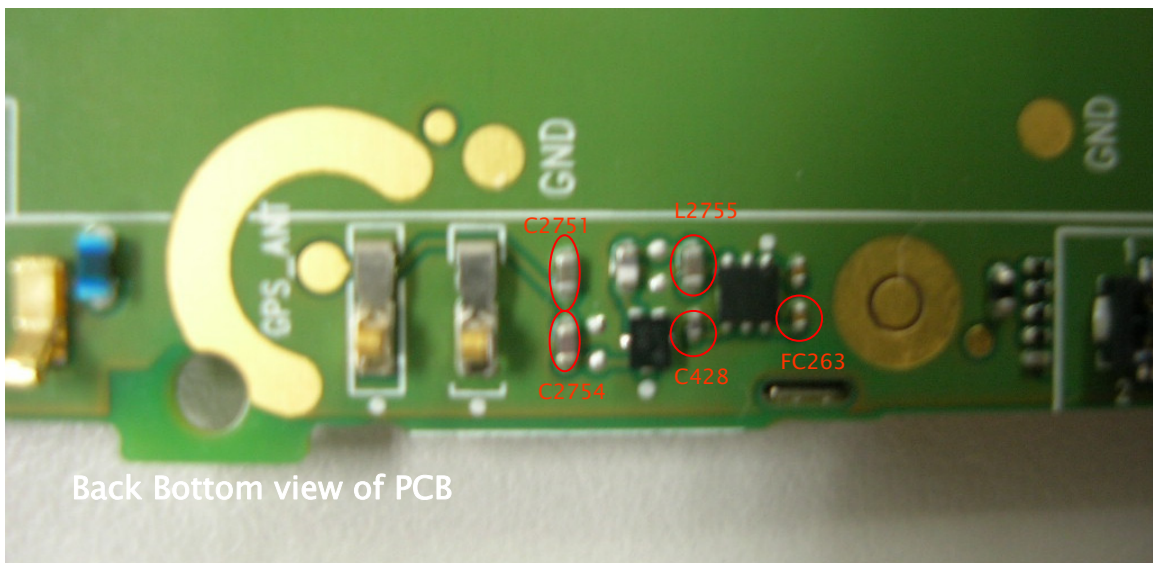
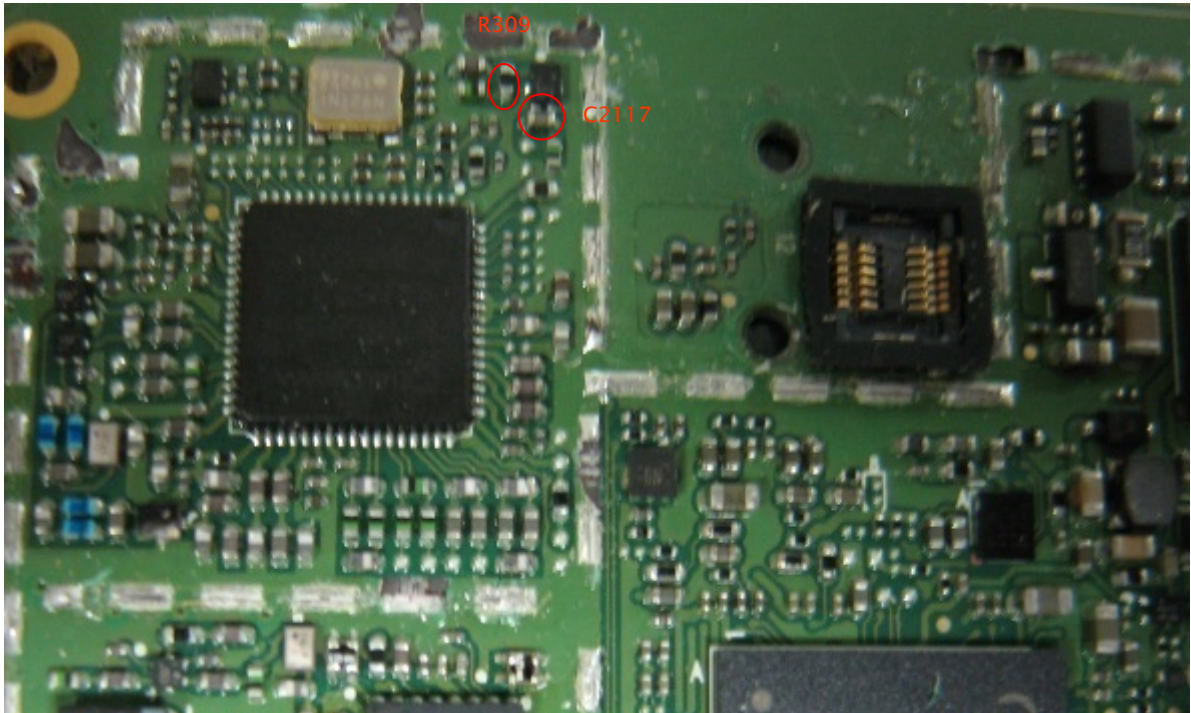


4.8 GPS Trouble

GPS Trouble

Picture Data

Main board top

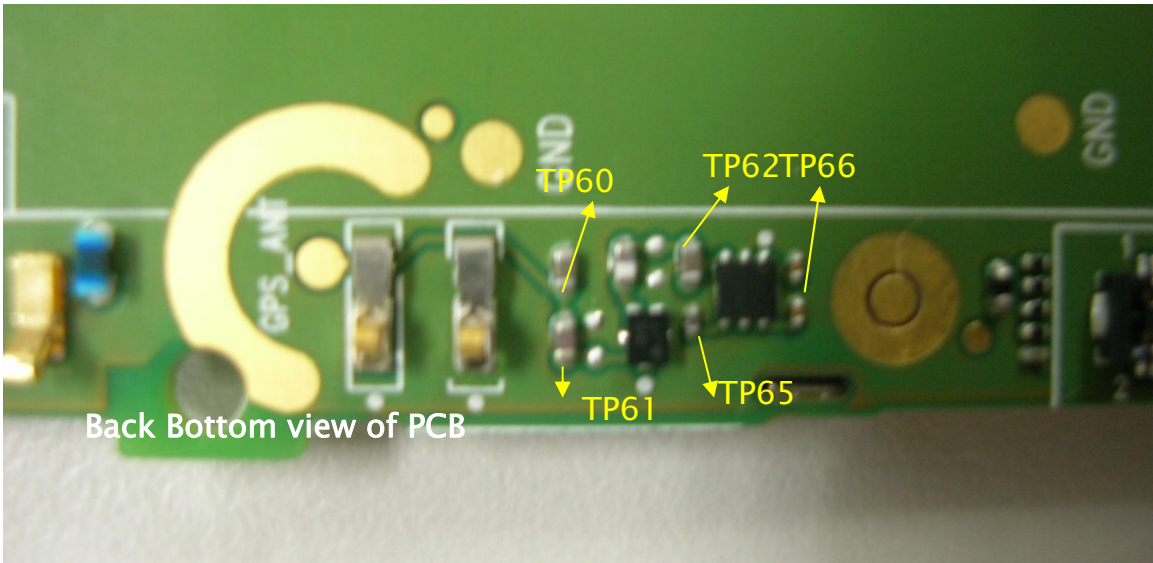
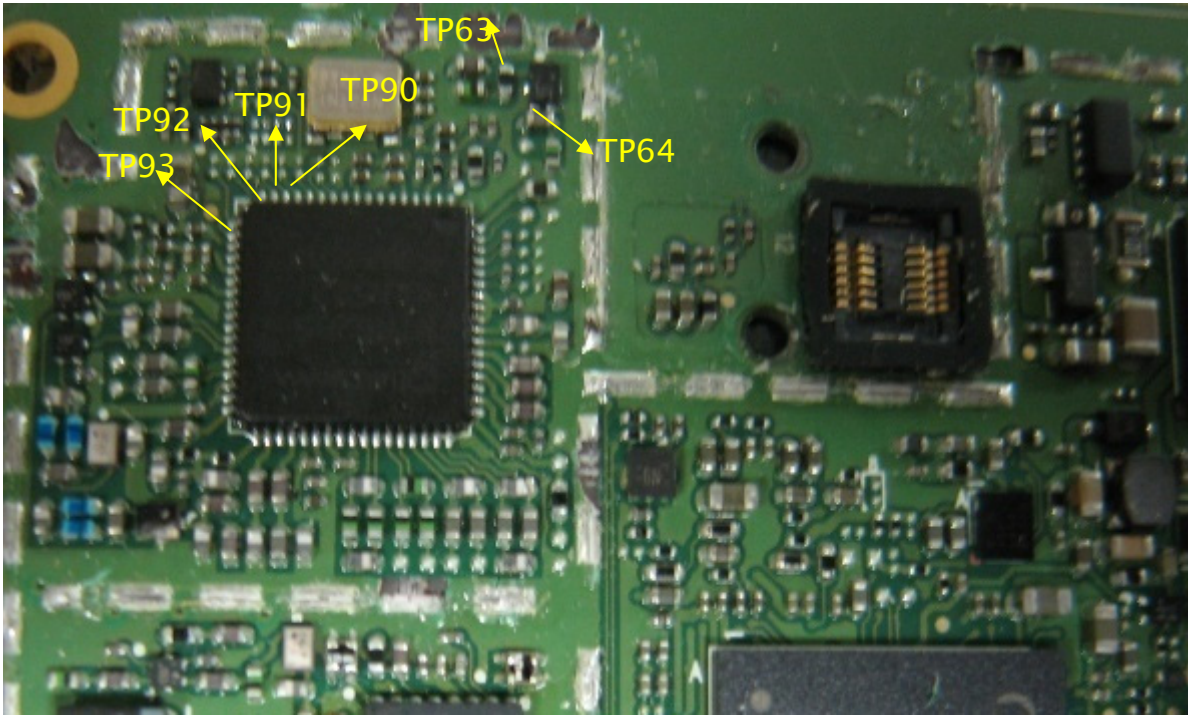


RF TROUBLE SHOOTING

GPS Trouble

Picture Data

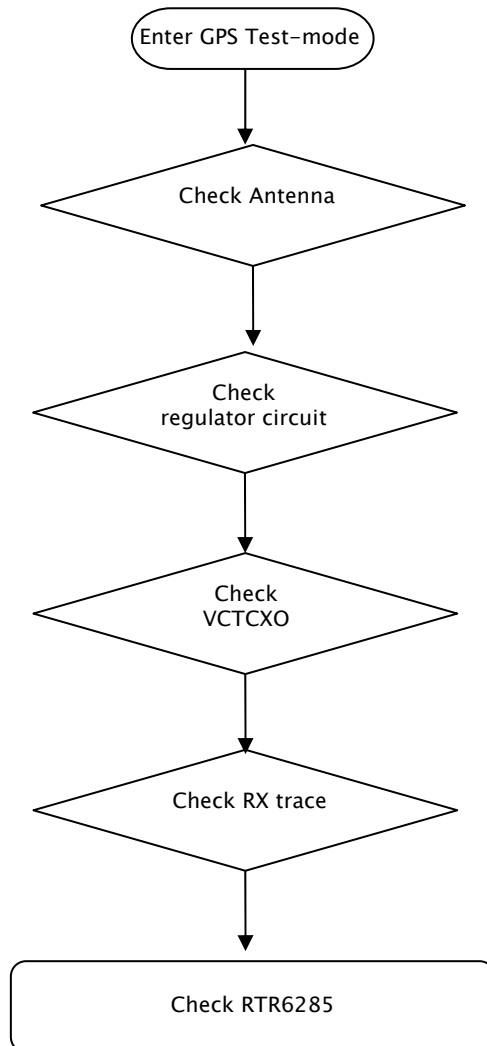
Main board top



RF TROUBLE SHOOTING

GPS Trouble

Checking Flow



Circuit Diagram

[illegible]

Checking Flow

Voltage at TP18 Is 2.1V?
Voltage at TP19 Is 2.7V?
~~Voltage at TP20 Is 2.6V?~~

Net EXT_GPS_LNA voltage is 2.7 V?

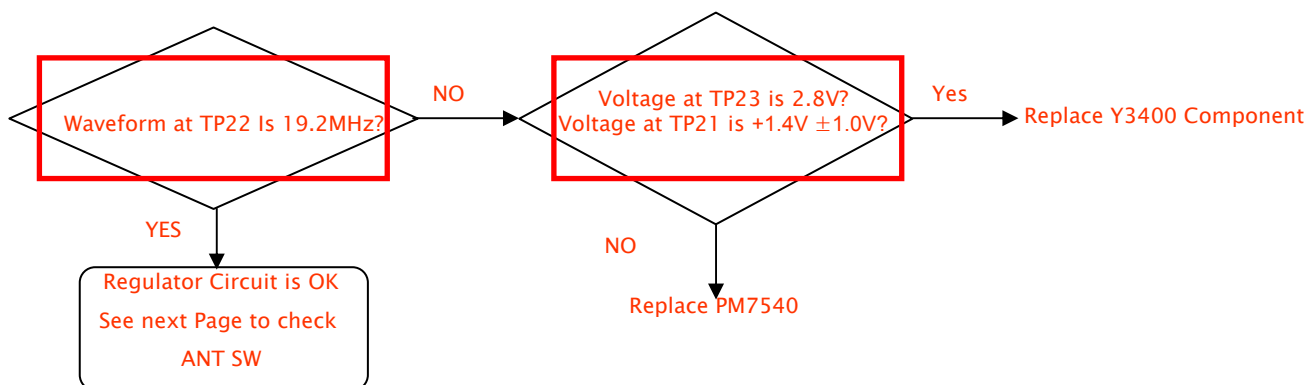
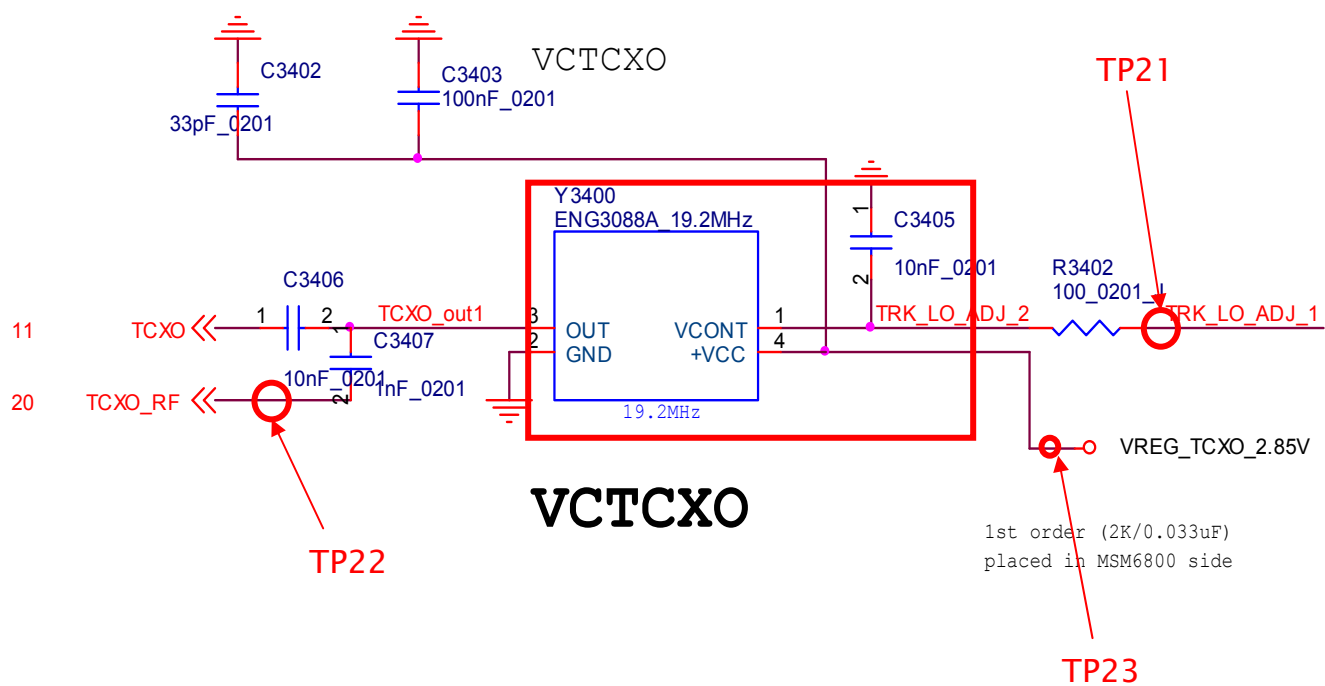
NO

Replace PM7540

YES

Regulator Circuit is OK
See next Page to check
VCTCXO

Circuit Diagram

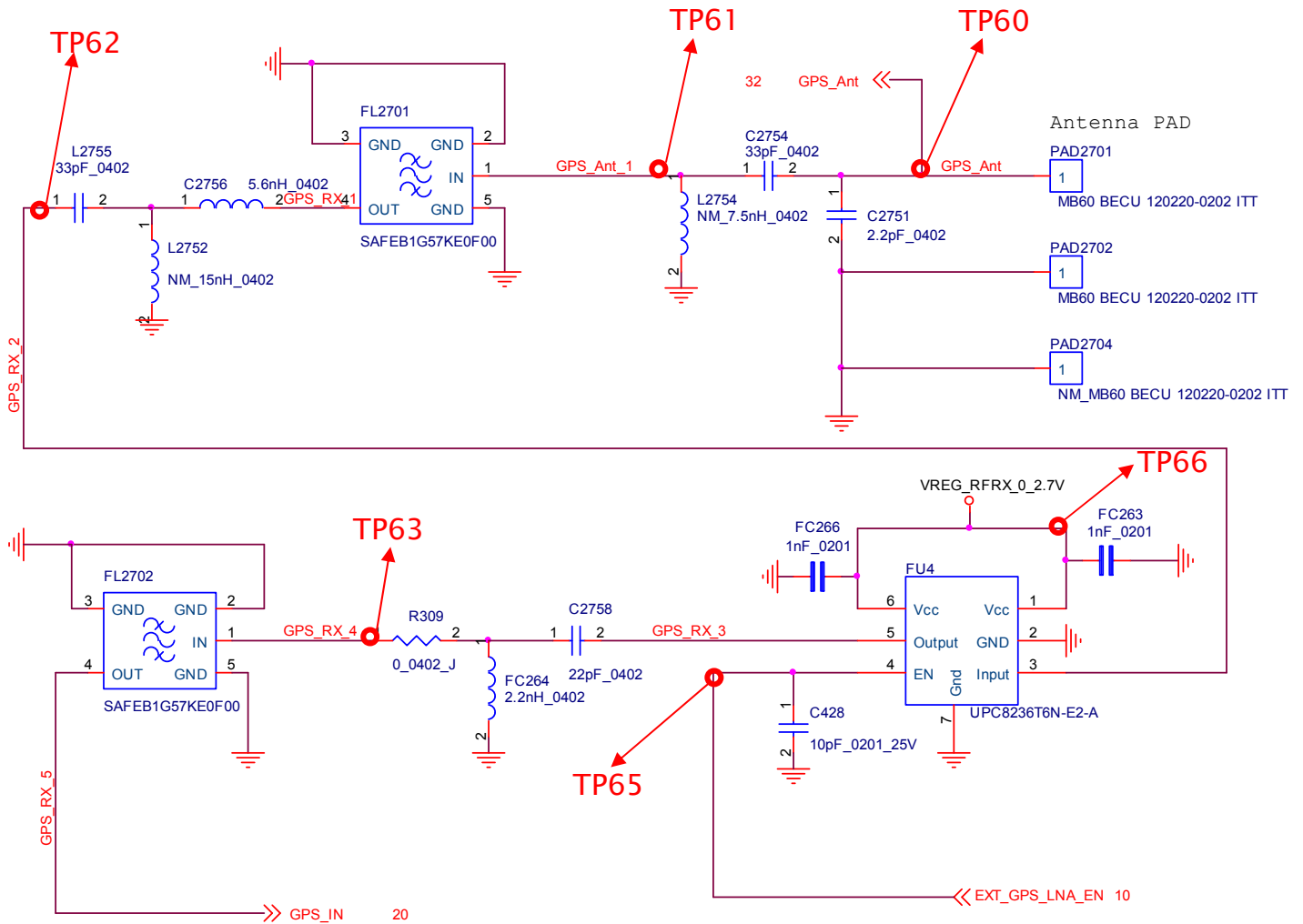


RF TROUBLE SHOOTING

(3) Checking LNA GPS Trace

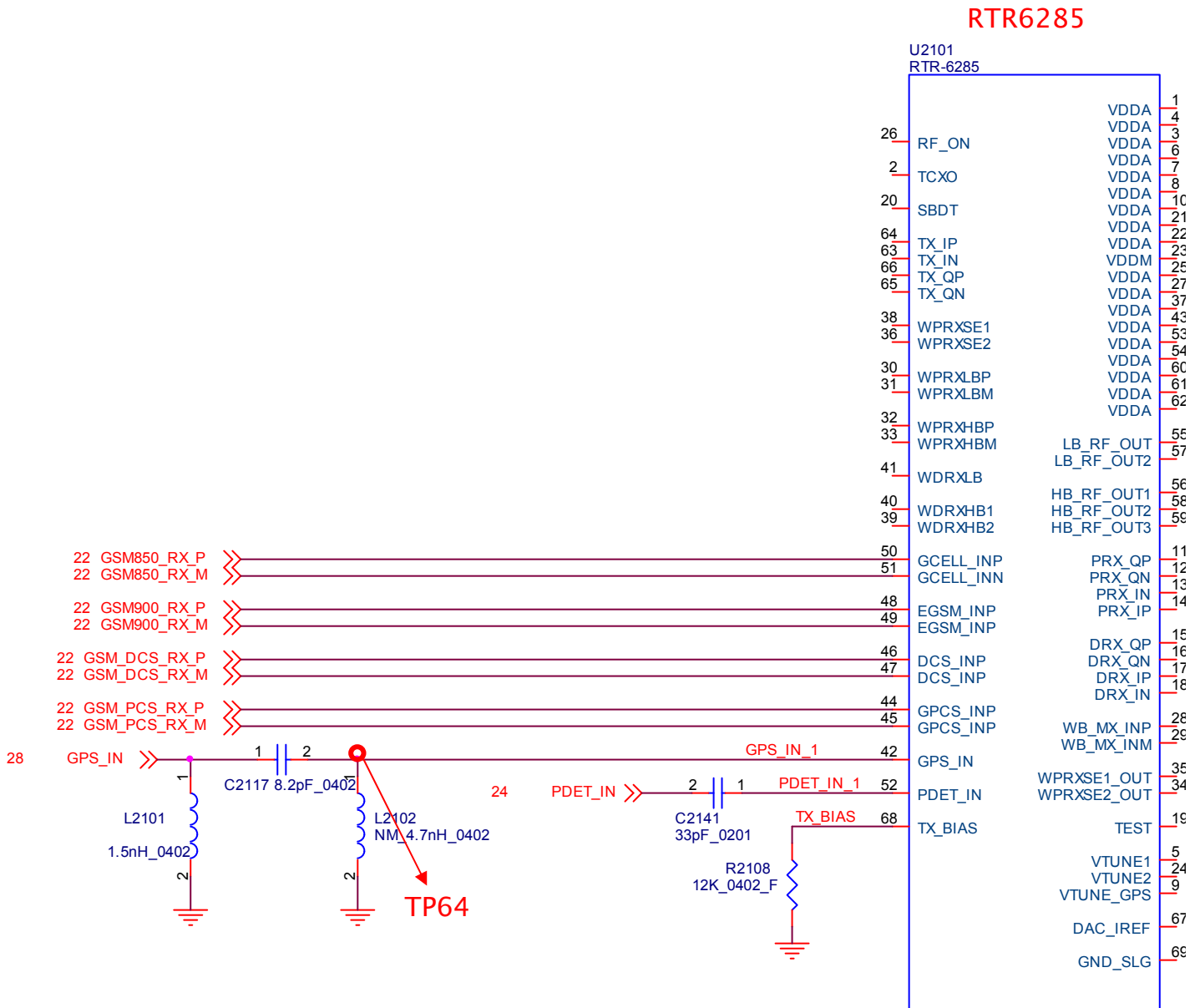
Circuit Diagram

Main Board



Circuit Diagram

Main Board



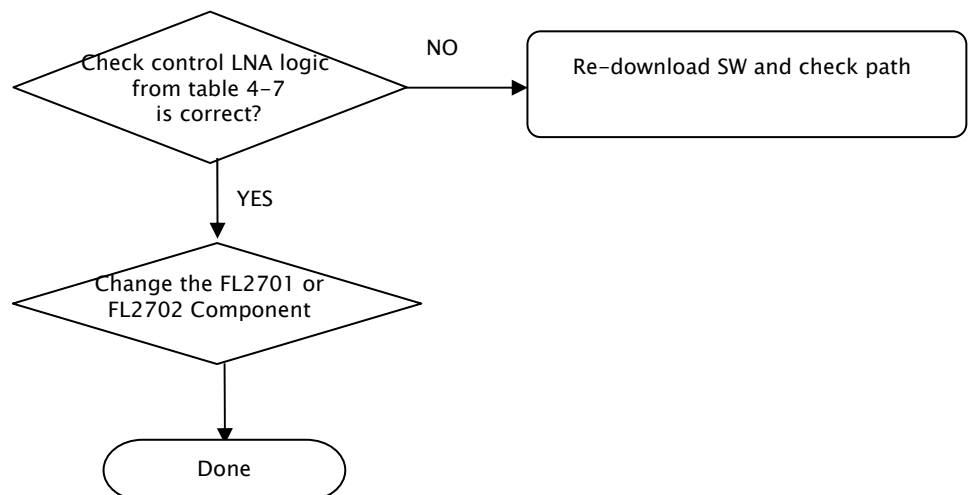
RF TROUBLE SHOOTING

(3) Checking LNA GPS Trace

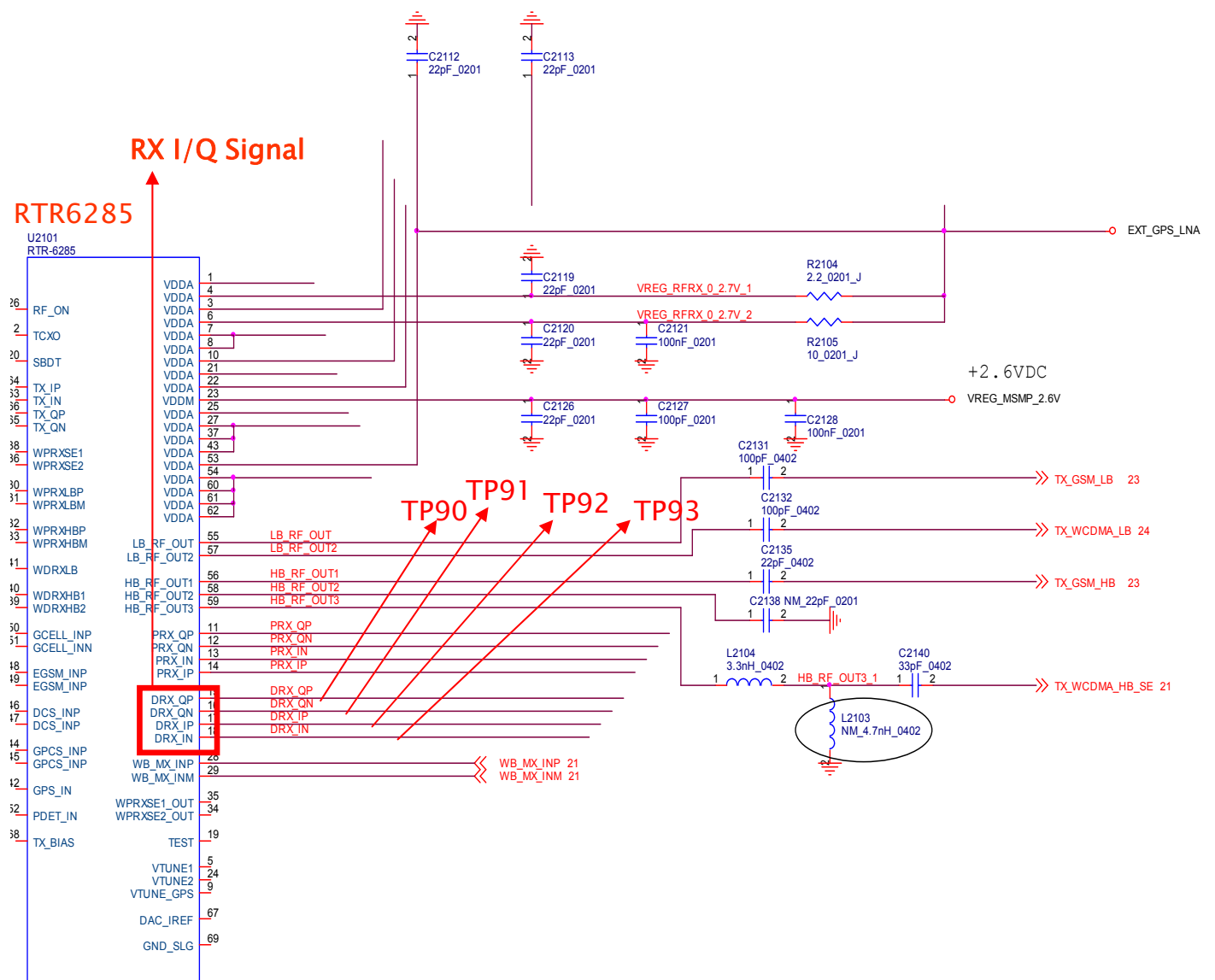
GPS mode	EXT_GPS_LNA_EN
ON	H
OFF	L

GPS LNA control Table 4-7

Checking Flow



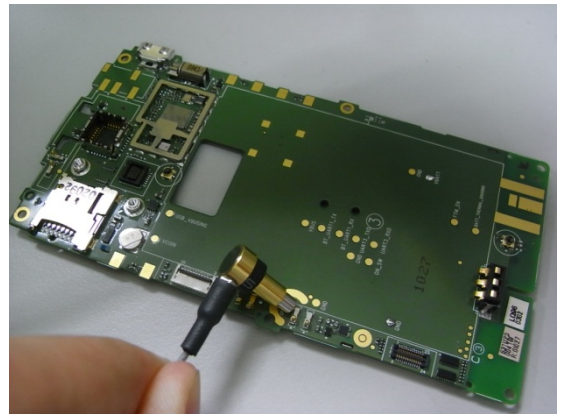
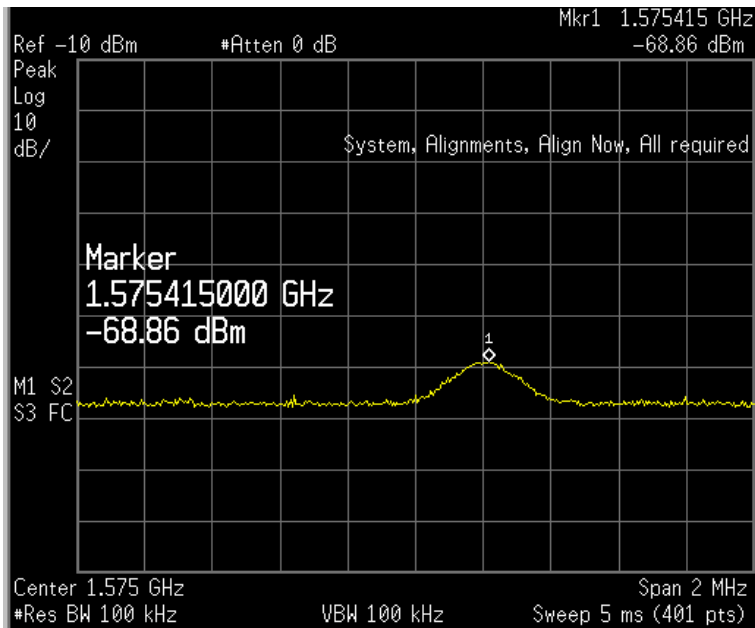
Main Board



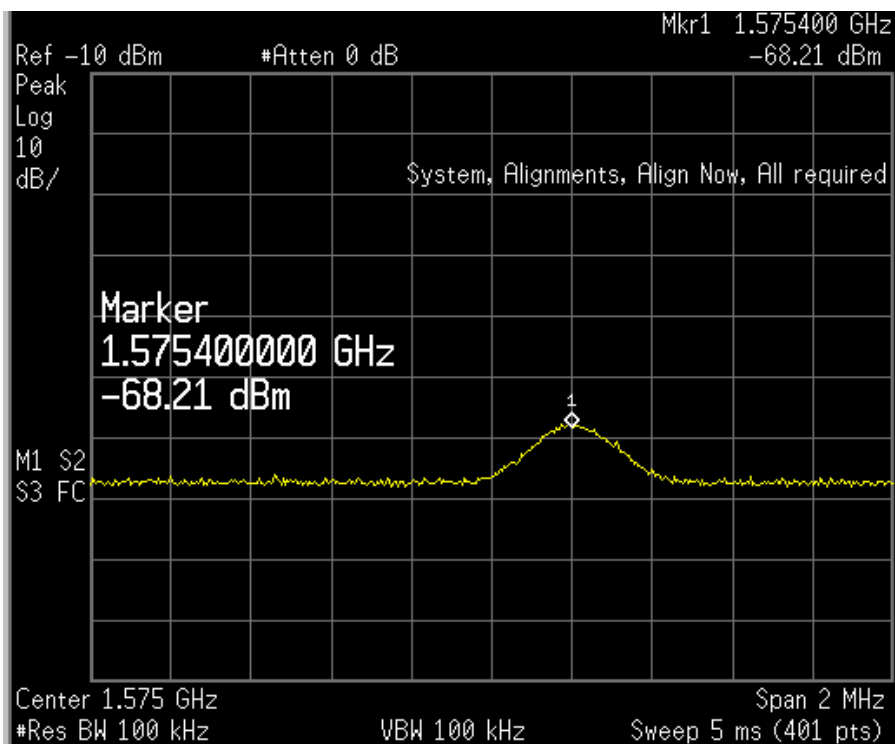
Waveform

Enter GPS Test-Mode and feed CW(1.5752MHz) to GPS antenna's pad.

TP60



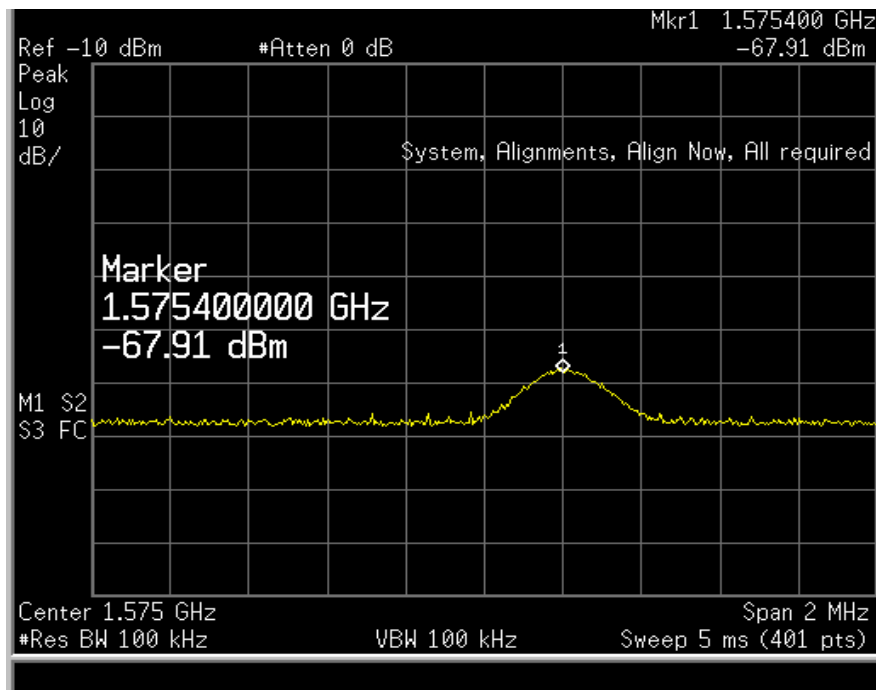
TP61



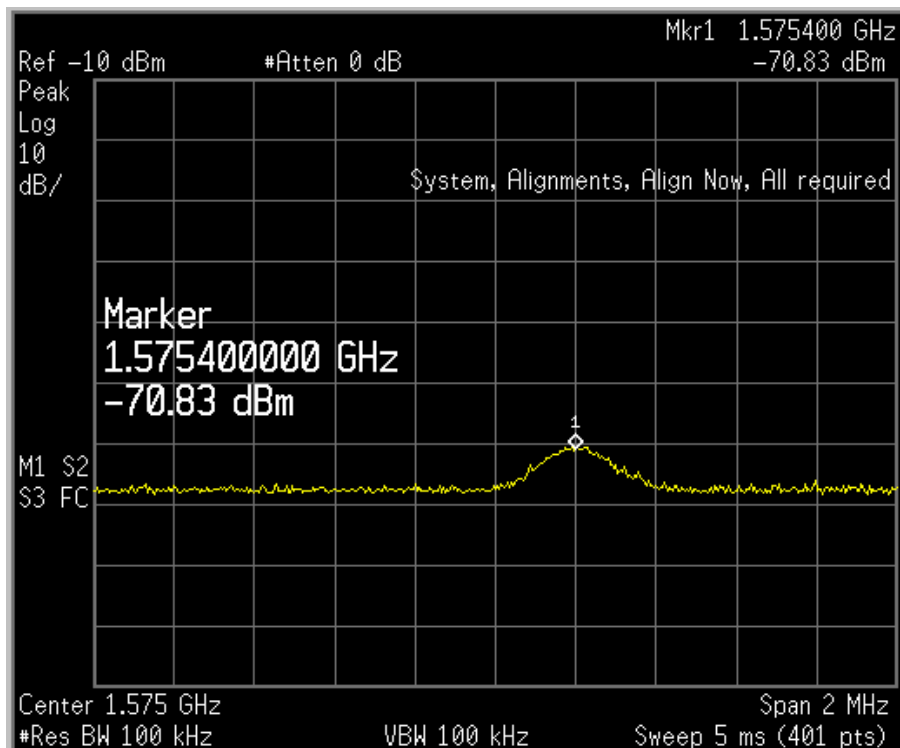
Waveform

Enter GPS Test-Mode and feed CW(1.5752MHz) to GPS antenna's pad.

TP62



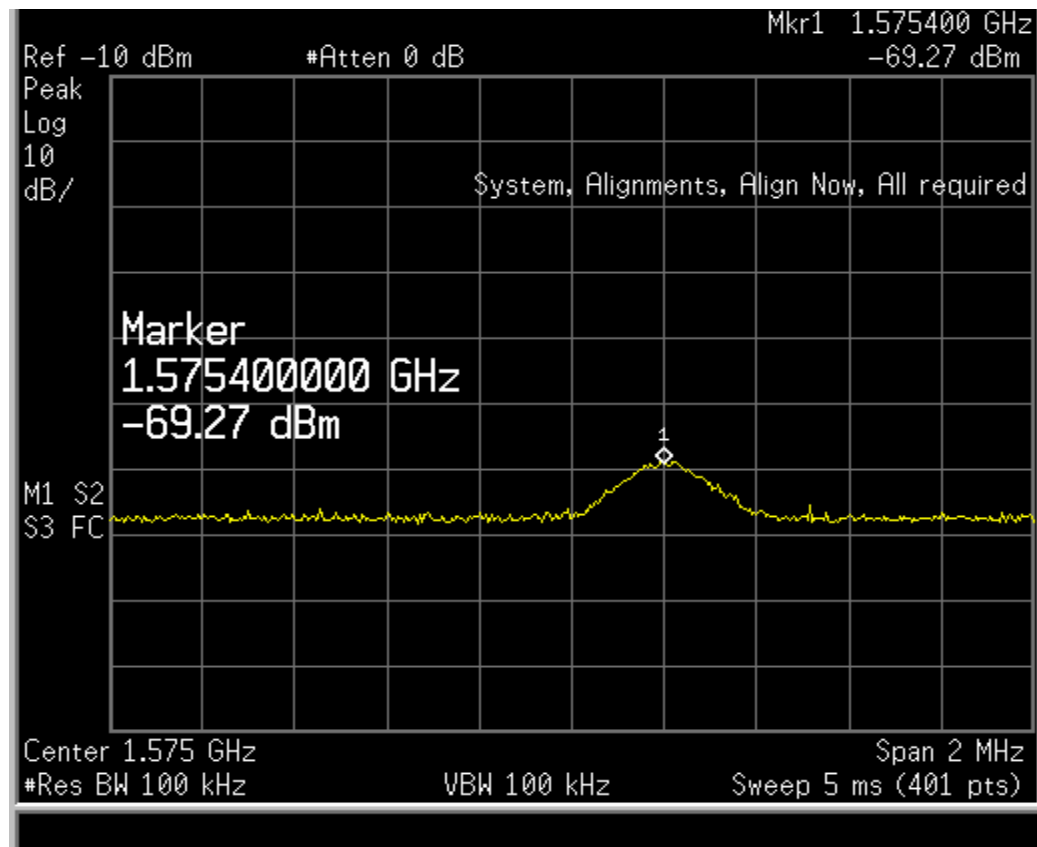
TP63



Waveform

Enter GPS Test-Mode and feed CW(1.5752MHz) to GPS antenna's pad.

TP64

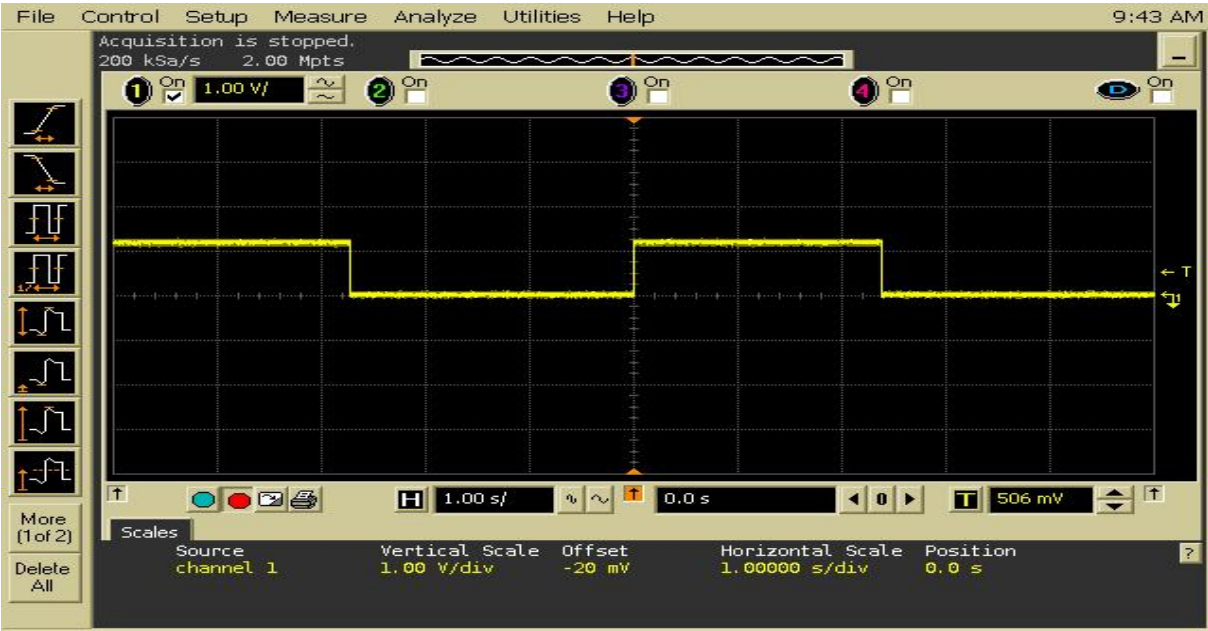


Waveform

TP90 / TP91



TP92 /TP93

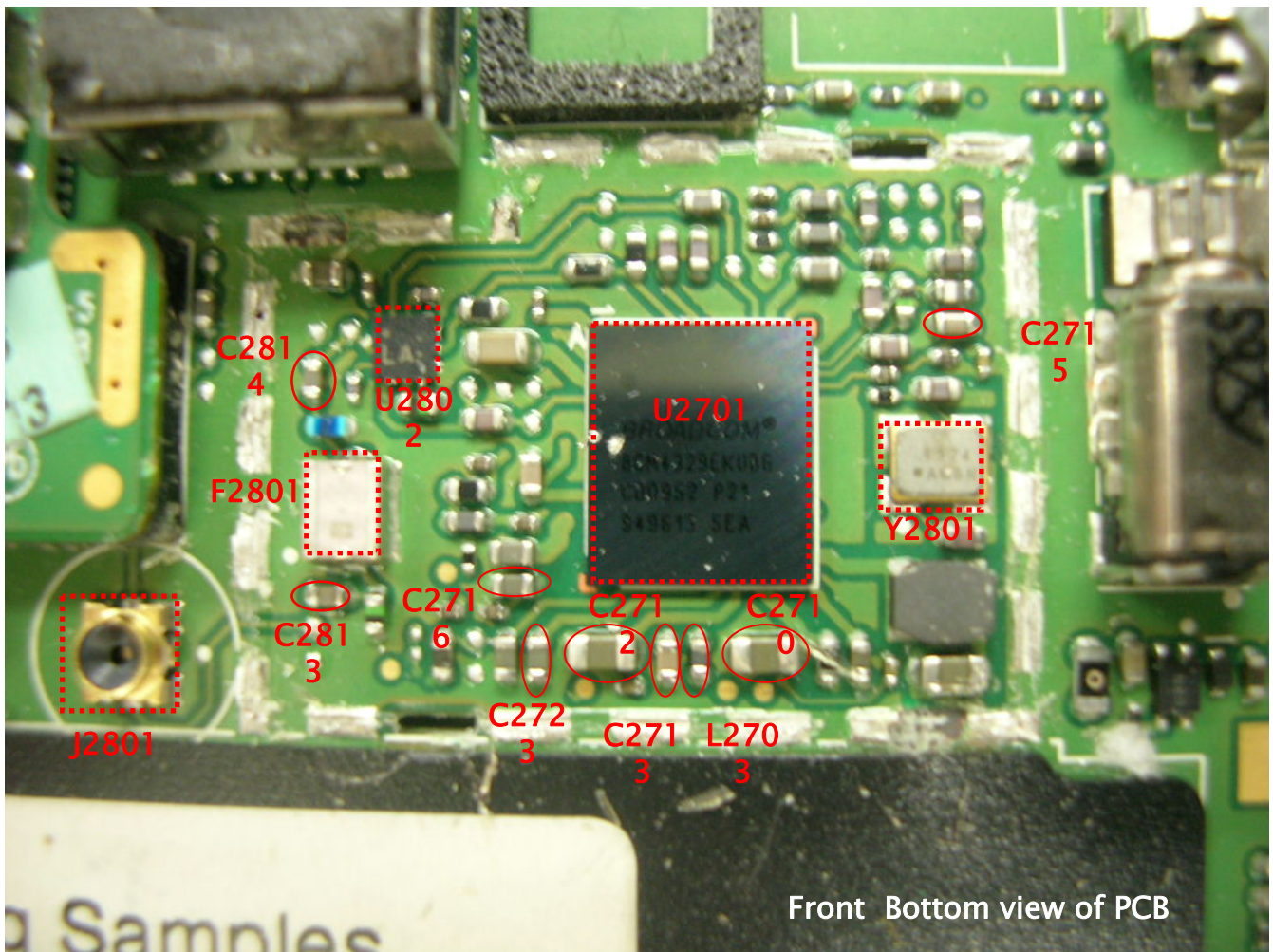


4.9 WLAN\BT\FM Trouble

WLAN\BT\FM Trouble

Picture Data

Main Board

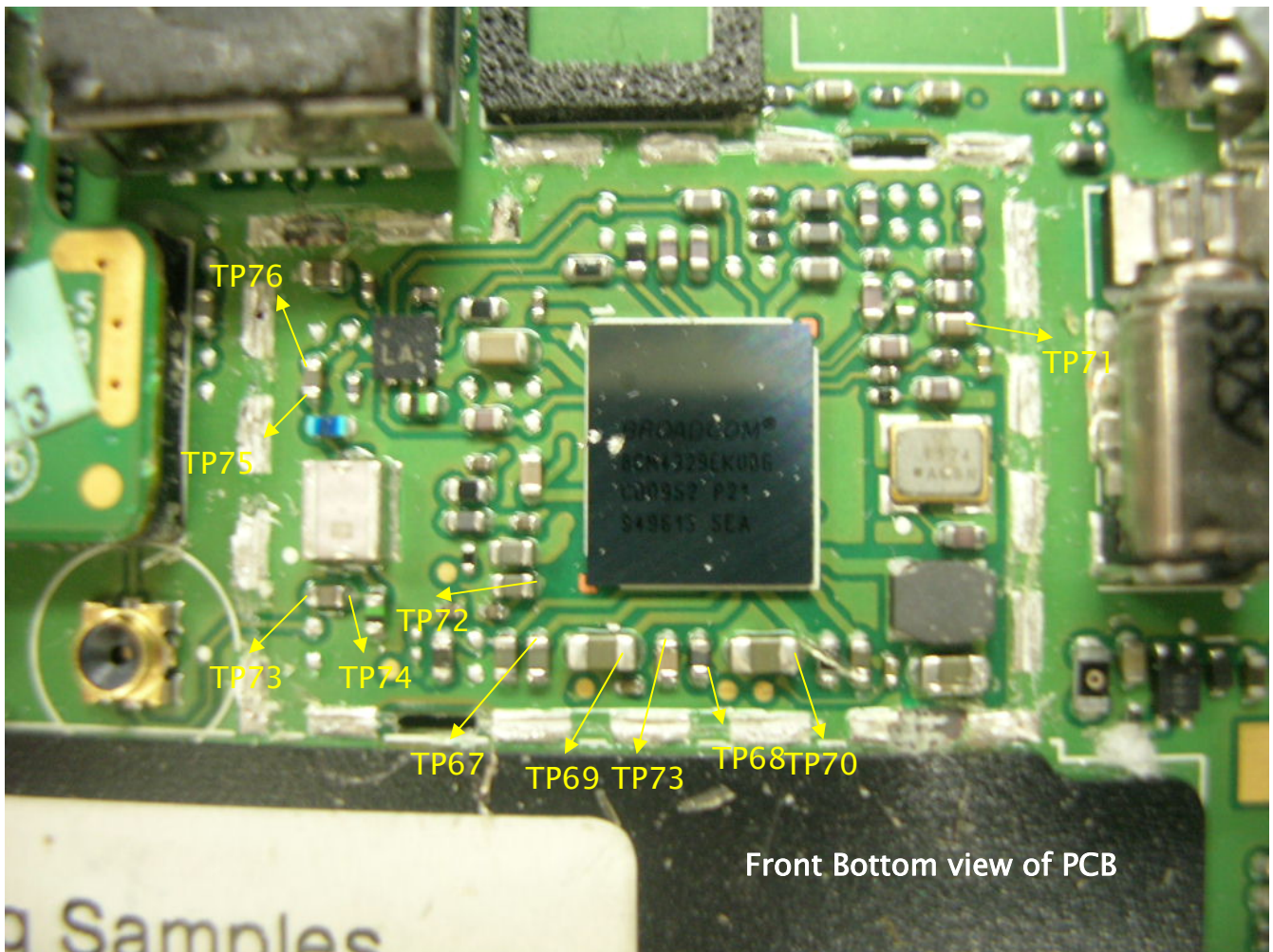


RF TROUBLE SHOOTING

WLAN\BT\FM Trouble

Picture Data

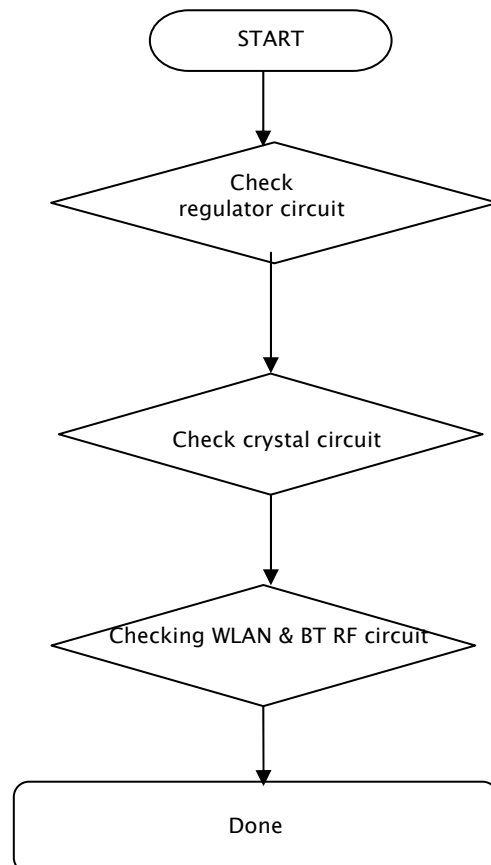
Main Board

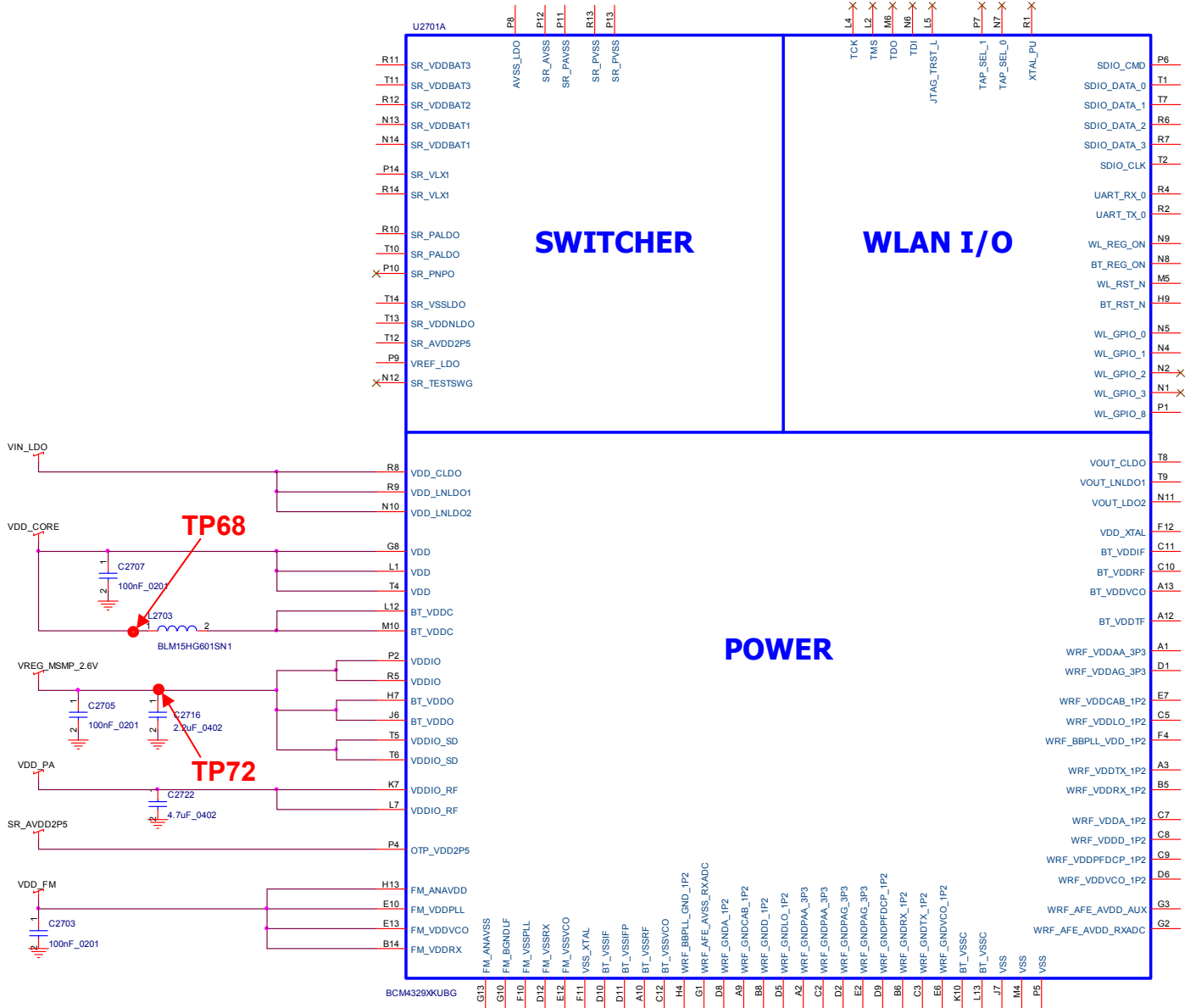


RF TROUBLE SHOOTING

WLAN\BT\FM Trouble

Checking Flow





BCM4329

RF TROUBLE SHOOTING

(1) Checking Regulator Circuit

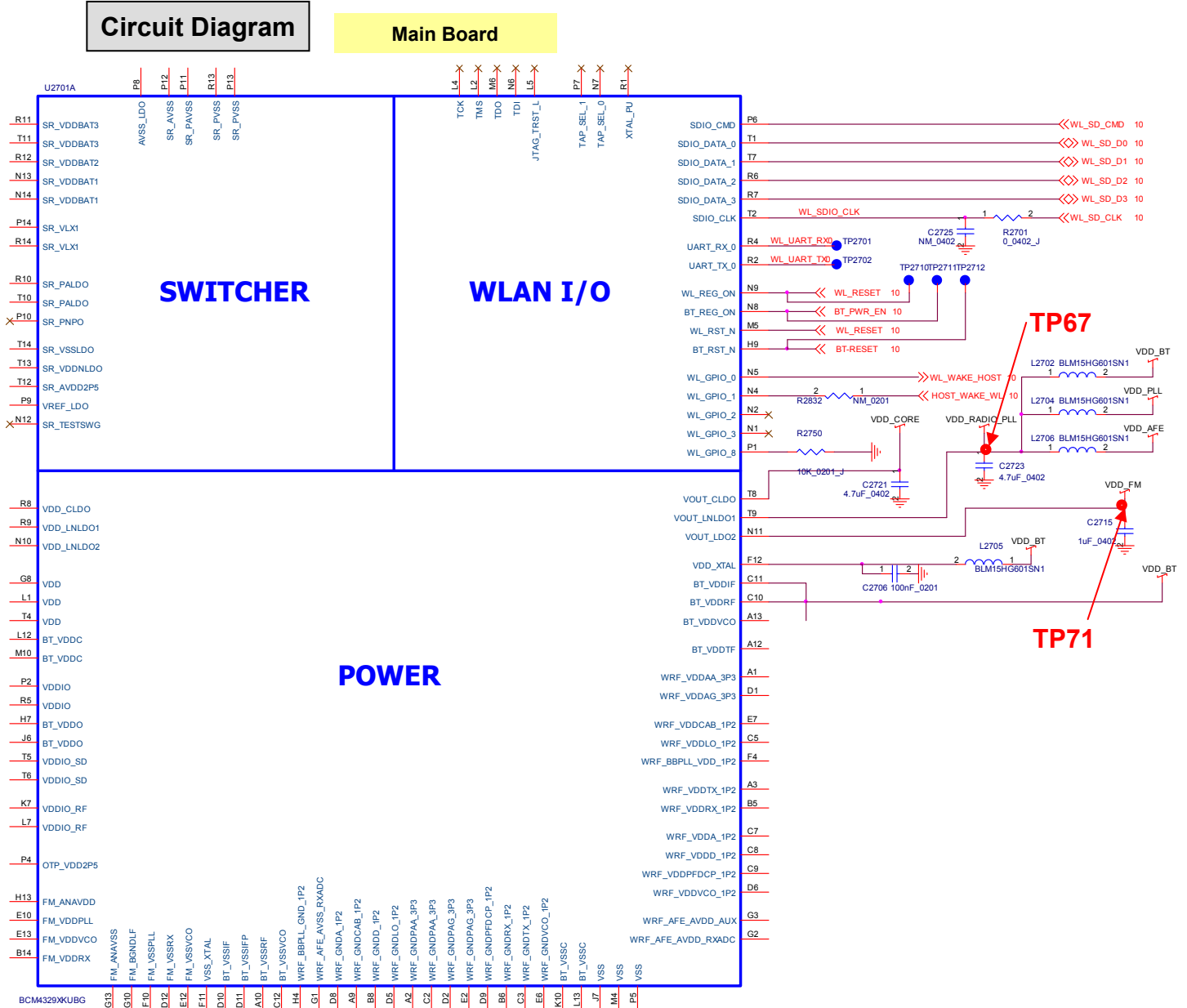
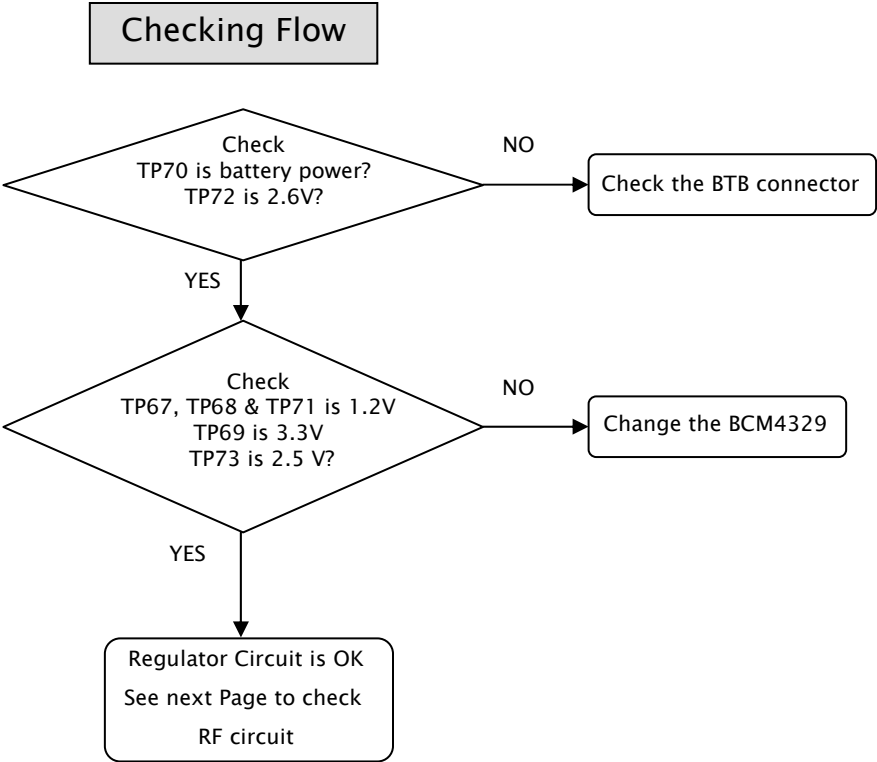


Table 20: Recommended Operating Conditions and DC Characteristics

Element	Symbol	Value			Unit
		Minimum	Typical	Maximum	
DC supply voltage for VBATT	VBATT	2.3	—	5.5	V
T9	VOUT_LNLDO1	O	1.2V output for low noise LDO1, 150 mA		
T12	SR AVDD2P5	O	2.5V LDO output		
T8	VOUT_CLDO	O	1.2V output for core LDO, 200 mA		
R10	SR_PALDO	O	internal PALDO output 3.3 V		
P2	VDDIO	I	Digital I/O supply (1.8V to 3.3V) 2.6 V		
N11	VOUT_LDO2	O	1.2V/2.5V–3.1V programmable output for low noise LDO2,		

RF TROUBLE SHOOTING

Circuit Diagram

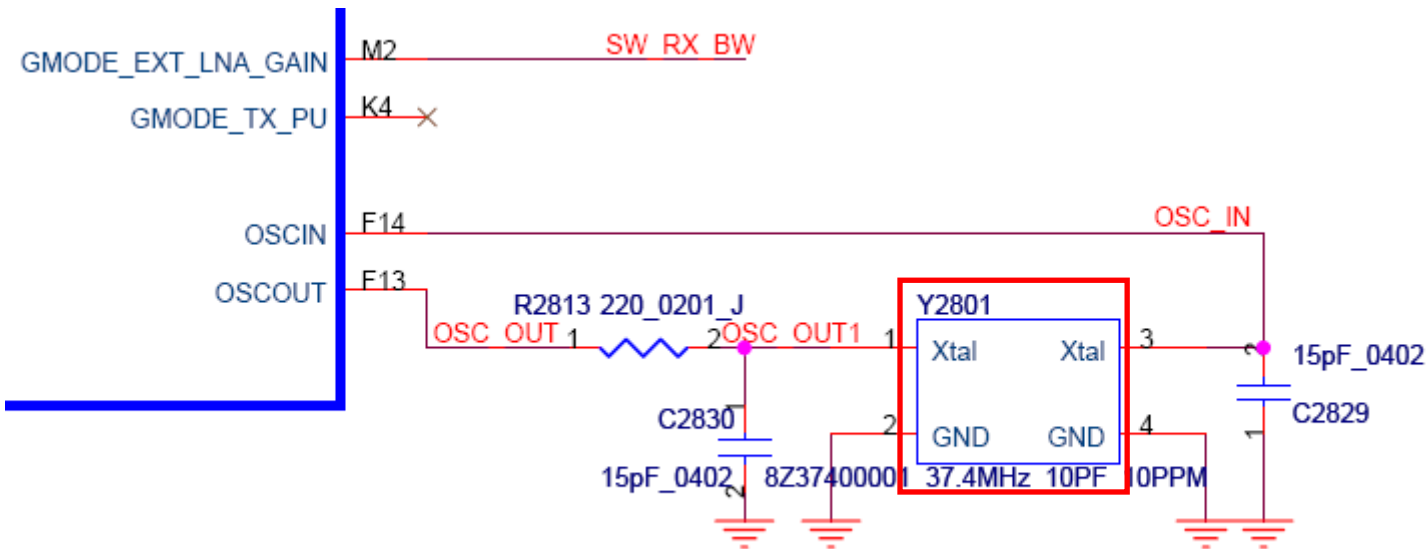


RF TROUBLE SHOOTING

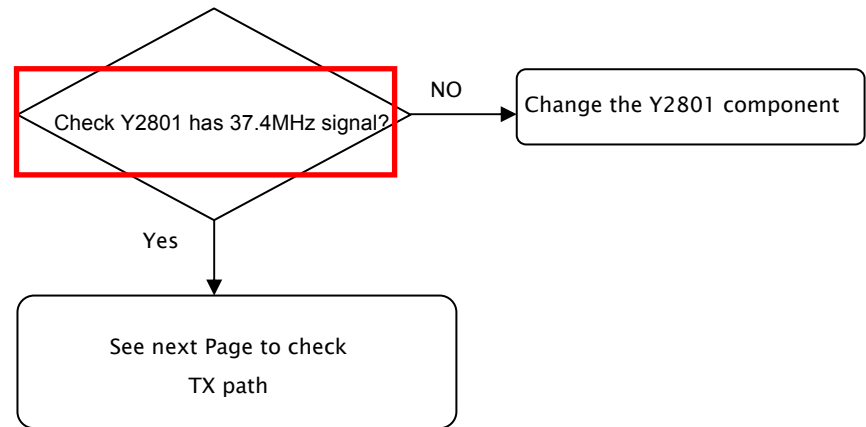
(2) Checking crystal circuit

Circuit Diagram

Main Board



Checking Flow

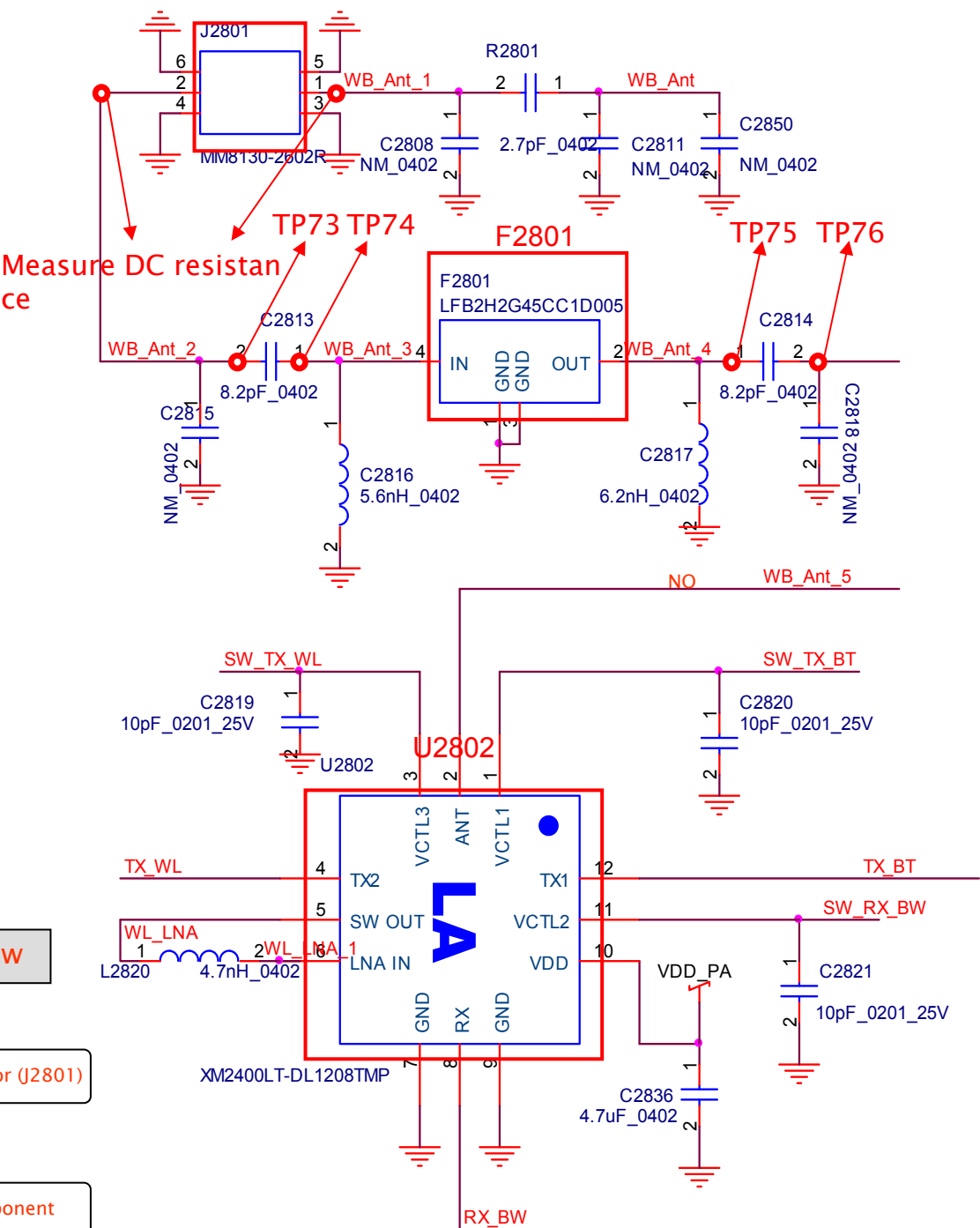


RF TROUBLE SHOOTING

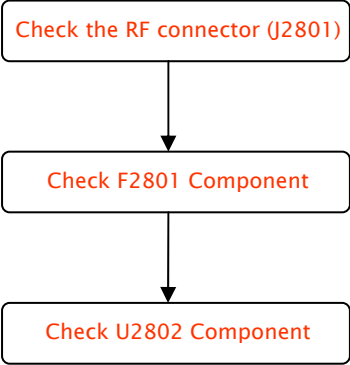
(3) Checking WLAN & BT RF circuit

Circuit Diagram

Main Board



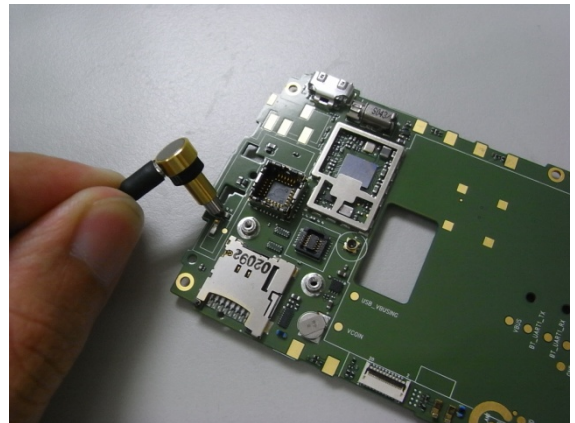
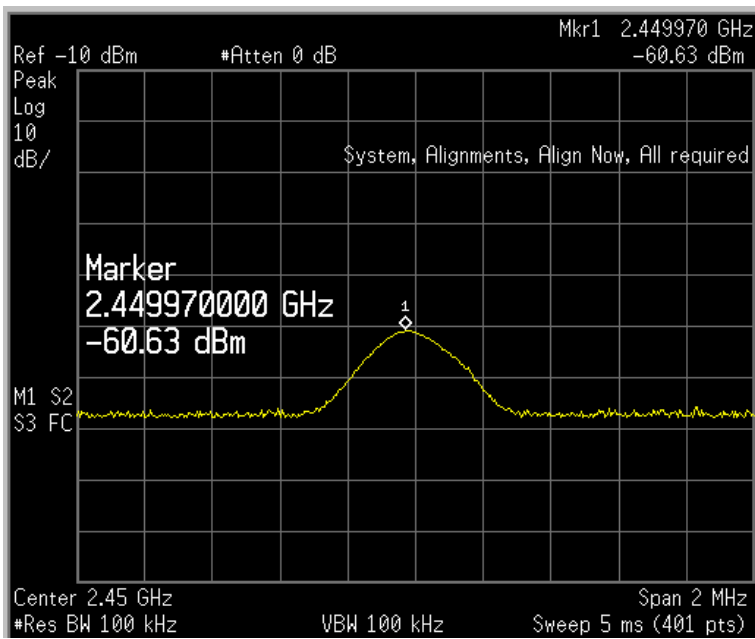
Checking Flow



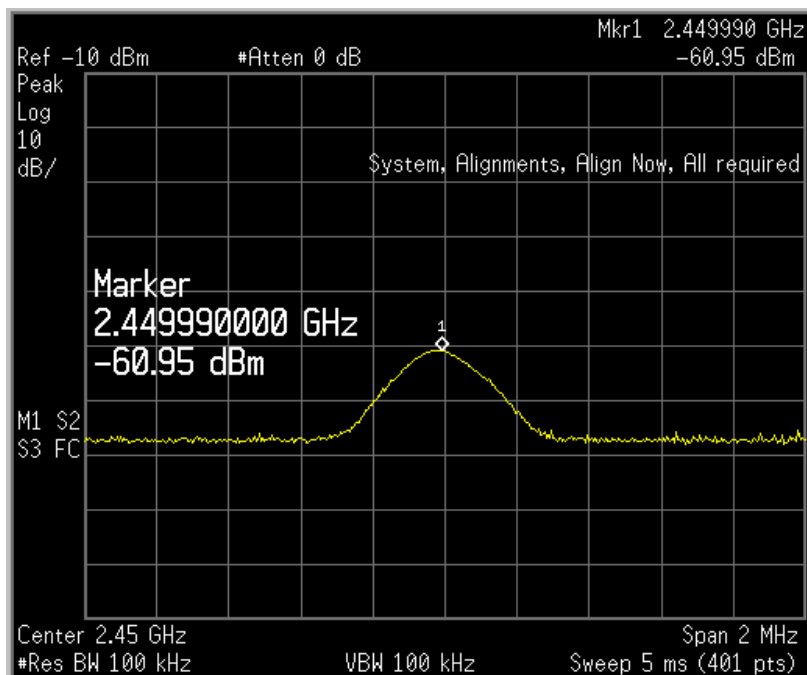
Waveform

Feed CW (2.45GHz) to WiFi/BT antenna's pad and measure waveform.

TP73



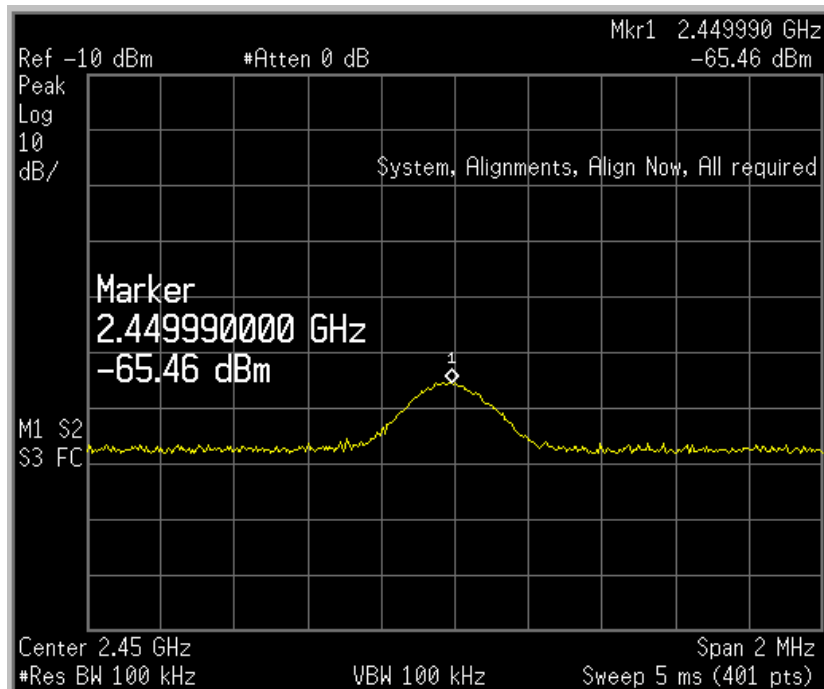
TP74



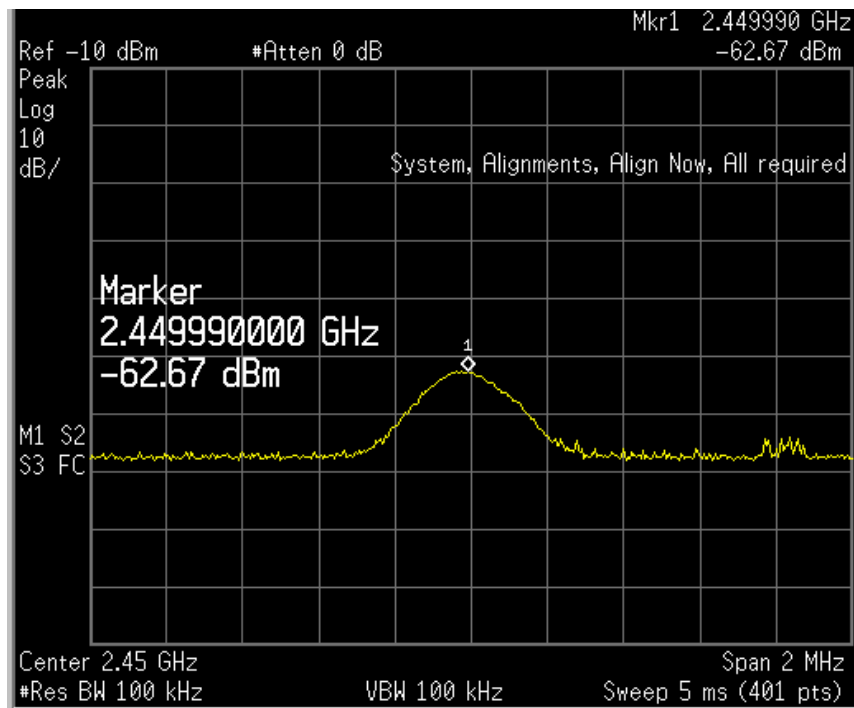
Waveform

Feed CW (2.45GHz) to Wi-Fi/BT antenna's pad and measure waveform.

TP75



TP76

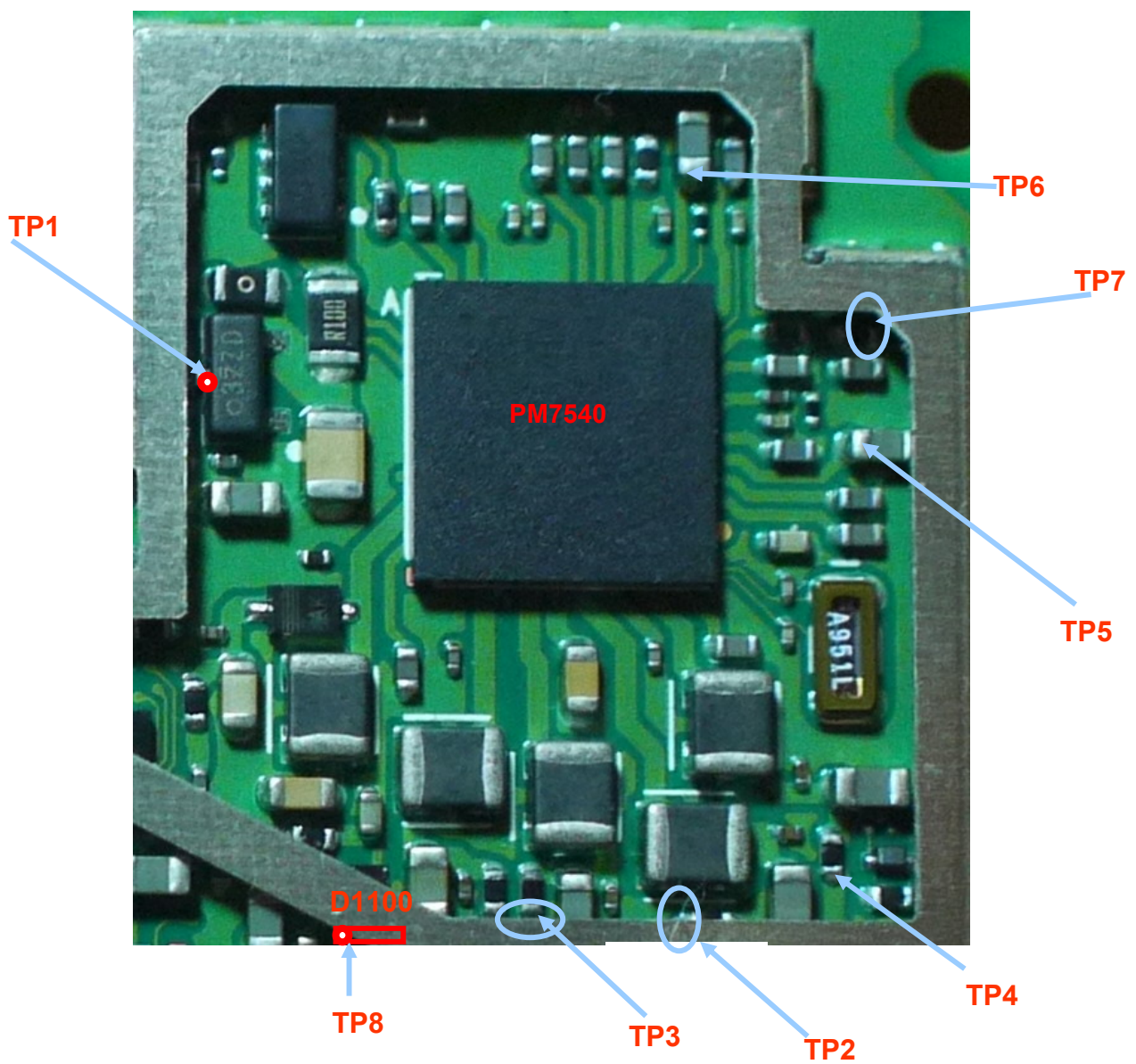


Baseband TROUBLE SHOOTING

4.10 Power On Trouble

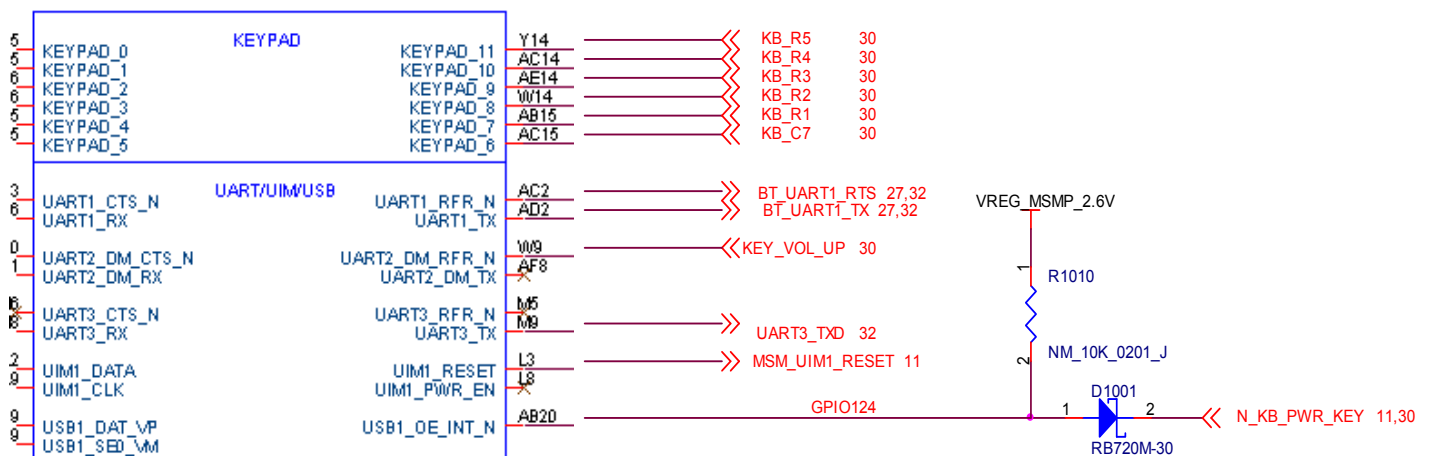
Picture Data

Main board top



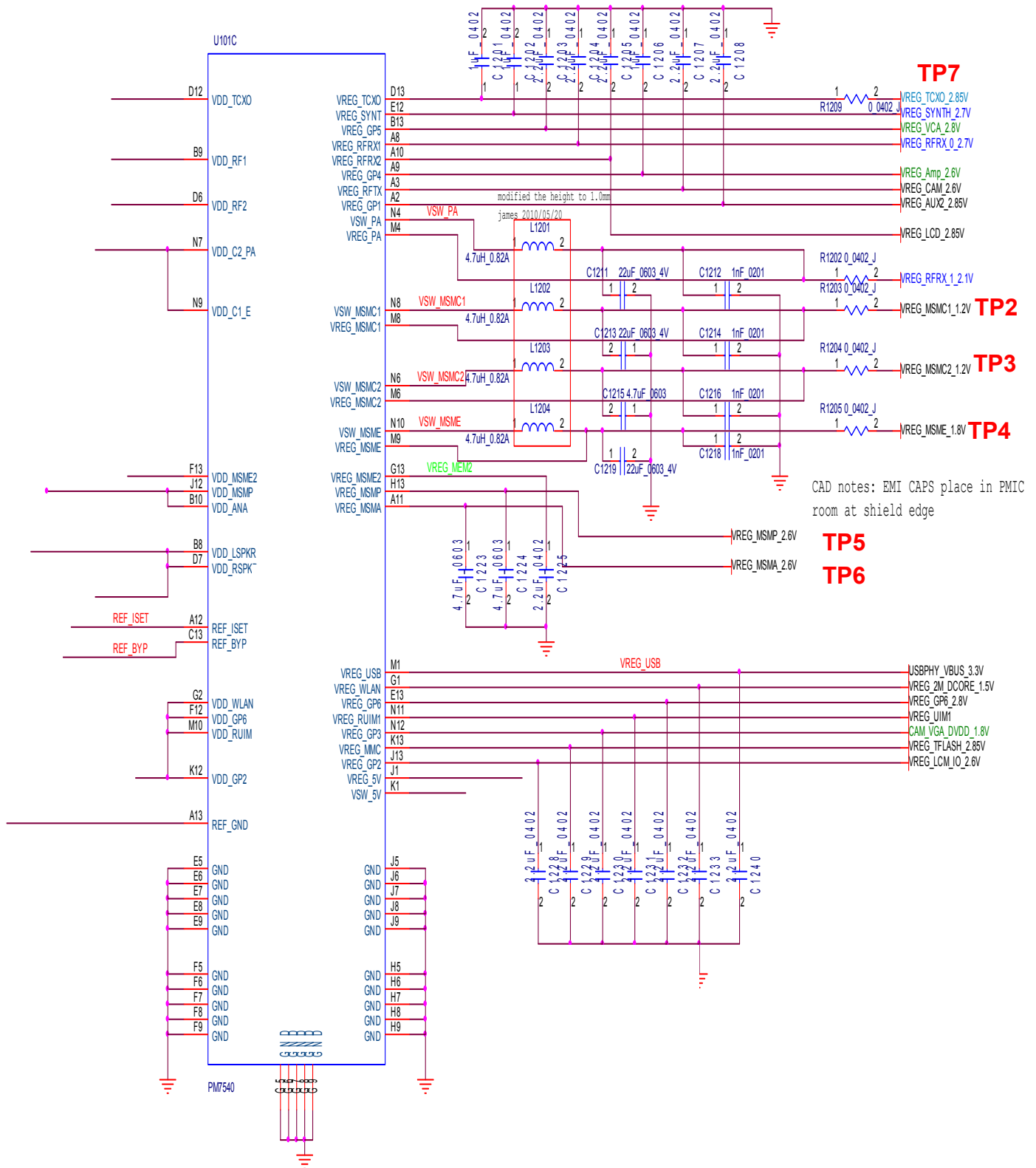
Circuit Diagram

TP8



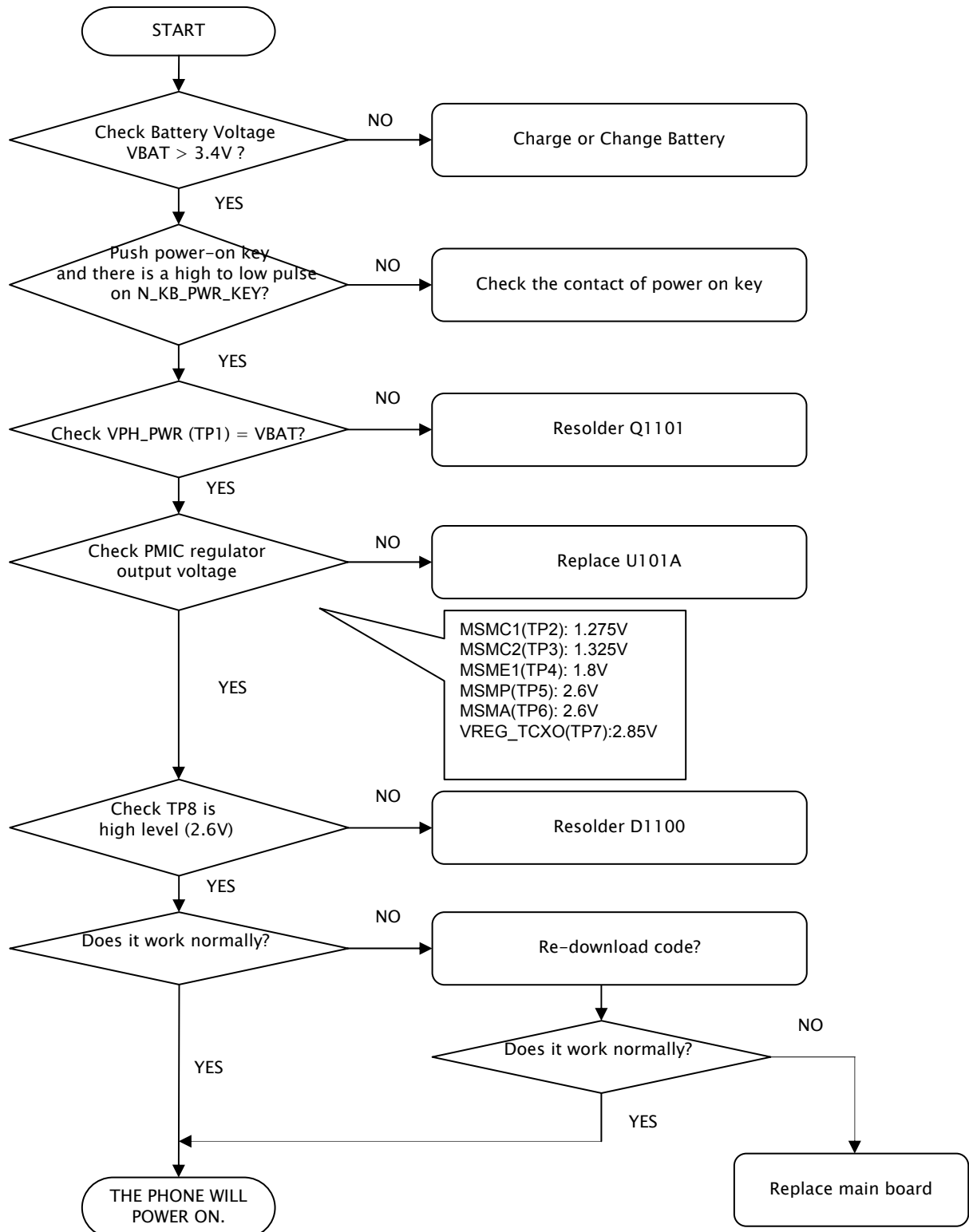
TROUBLE SHOOTING

Main Board



TROUBLE SHOOTING

Checking Flow

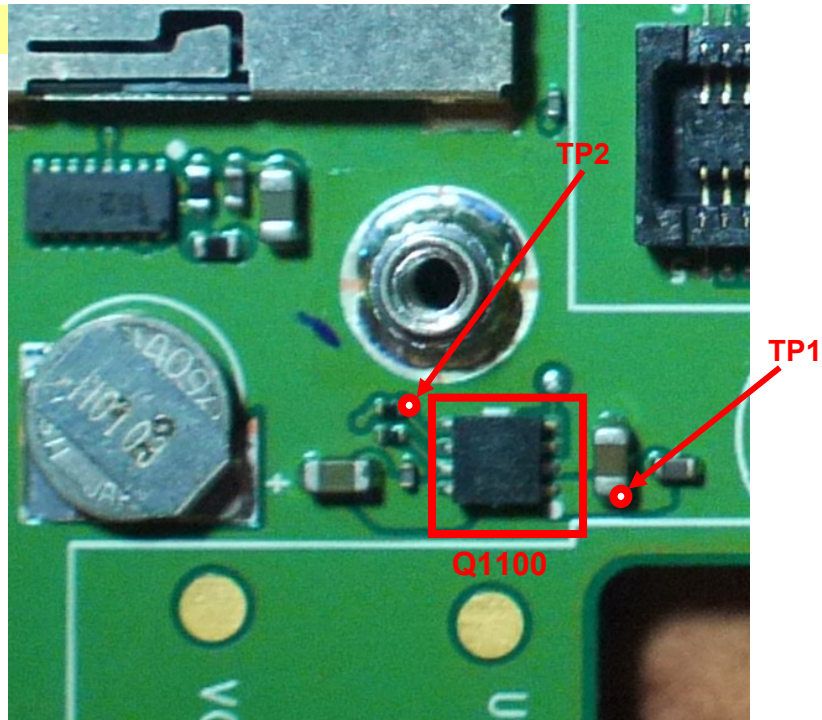


TROUBLE SHOOTING

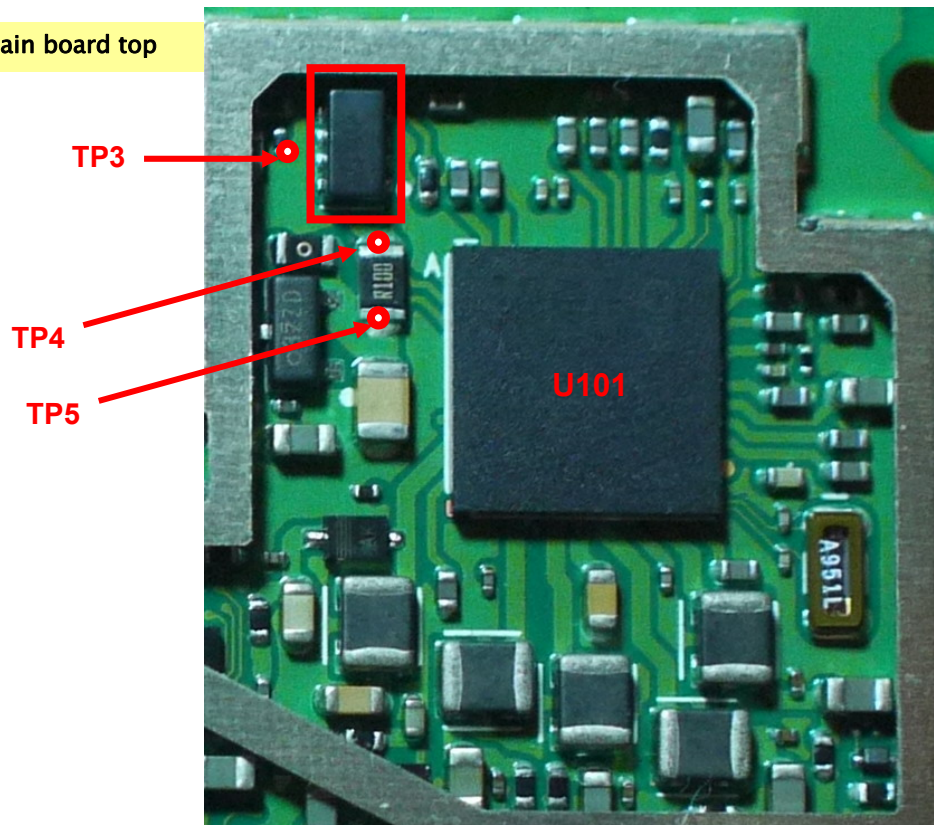
4.11 Charging Trouble

Picture Data

Main board bottom



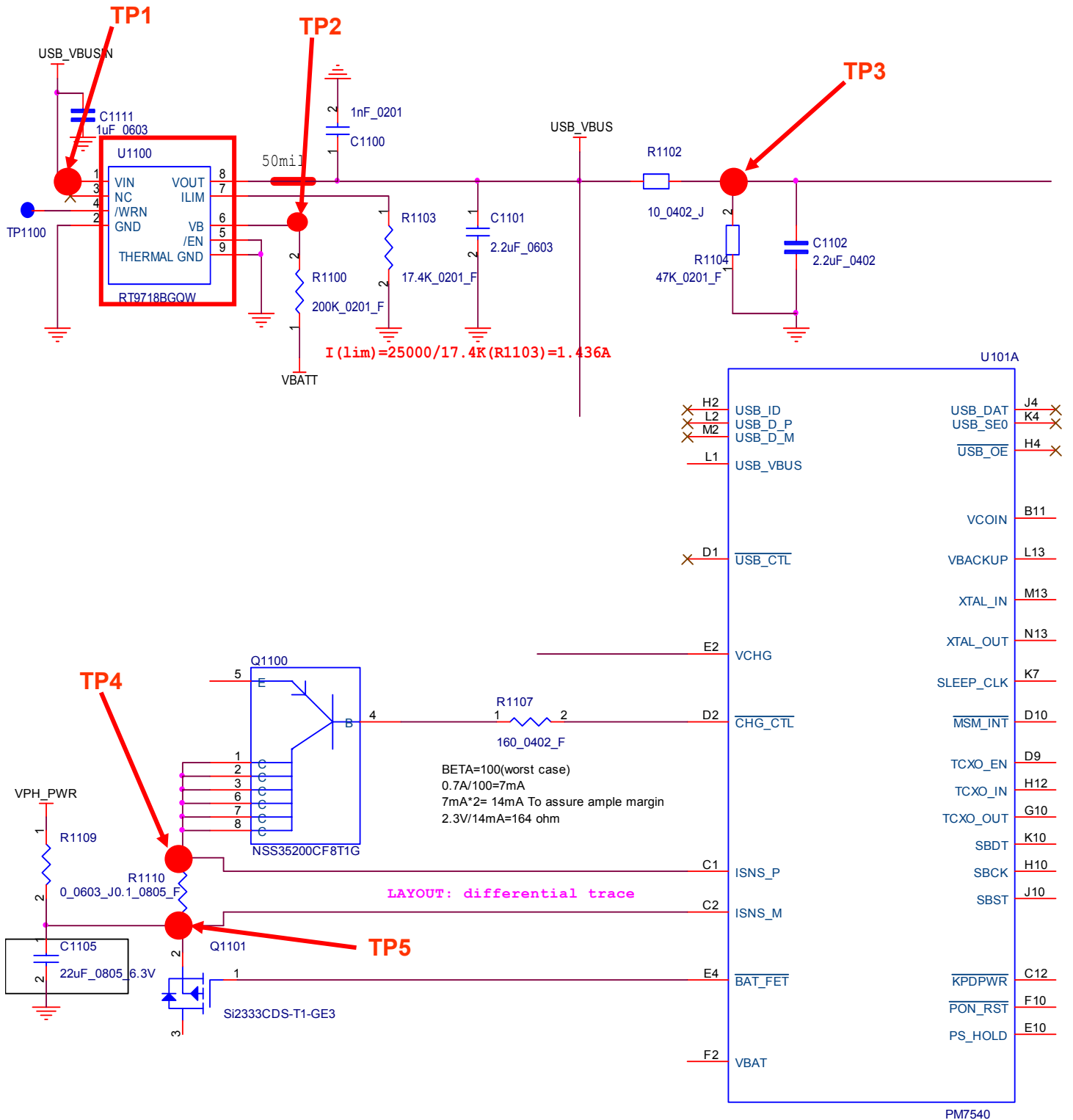
Main board top



TROUBLE SHOOTING

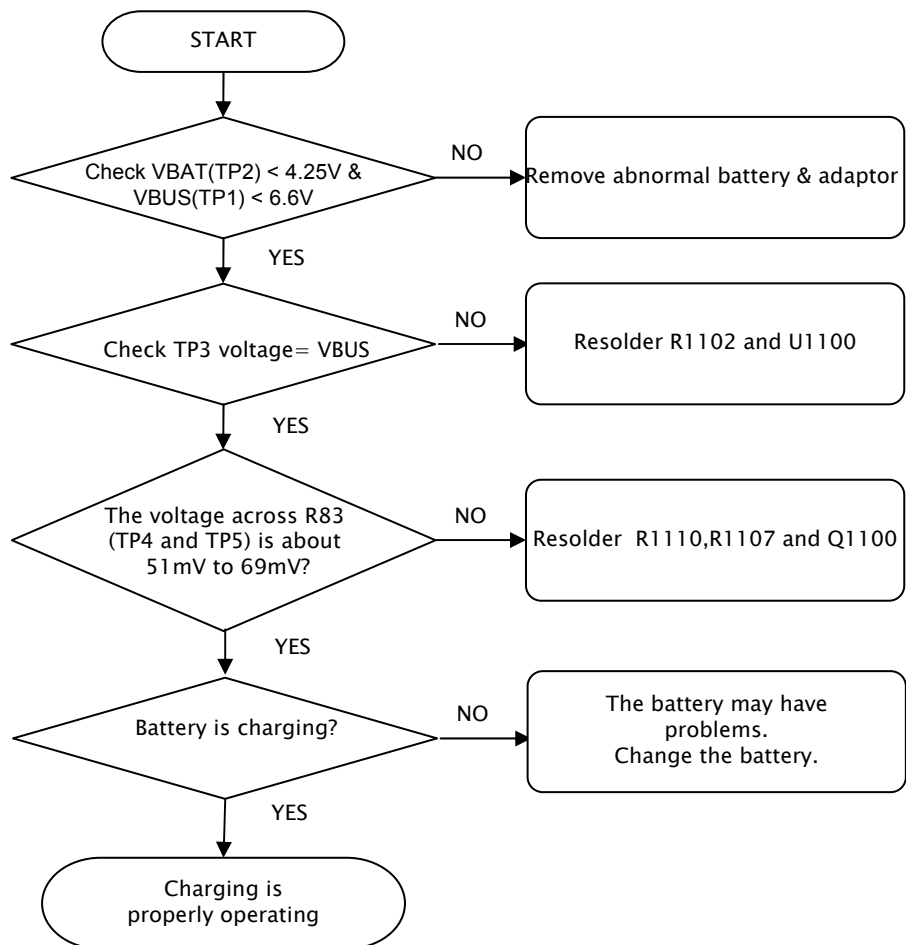
Circuit Diagram

Main Board



TROUBLE SHOOTING

Checking Flow

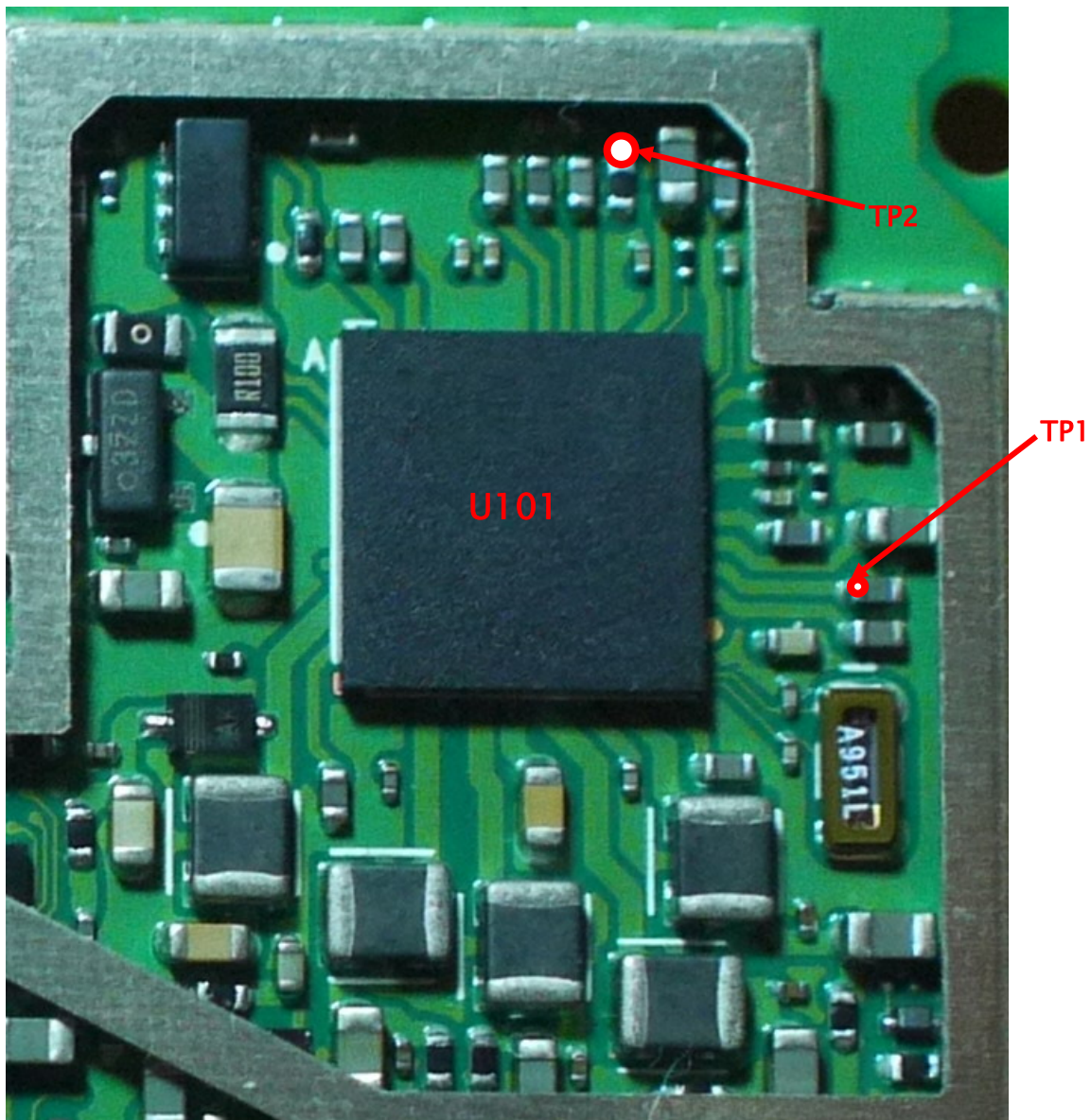


TROUBLE SHOOTING

4.12 LCD Trouble

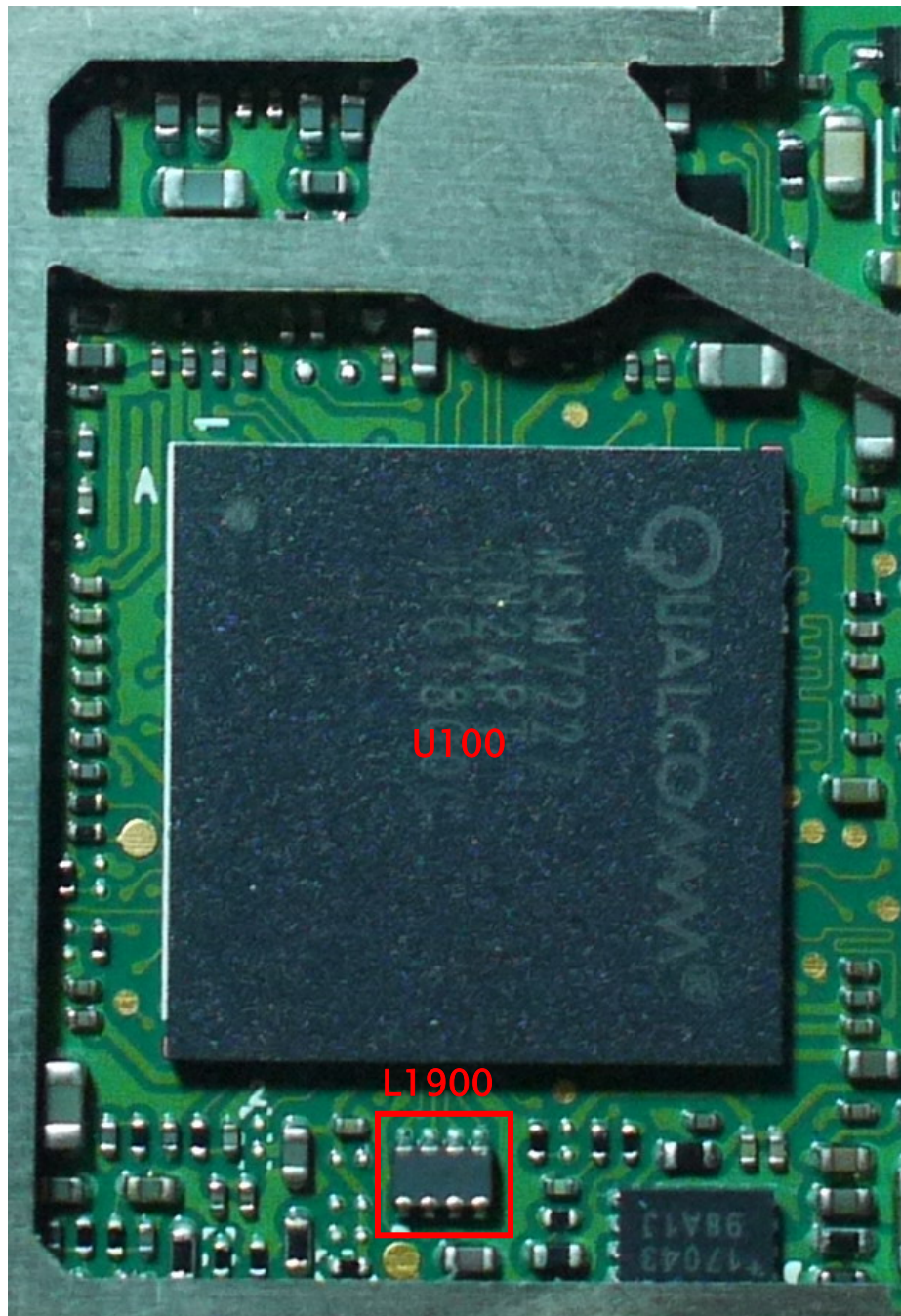
Picture Data

Main board top



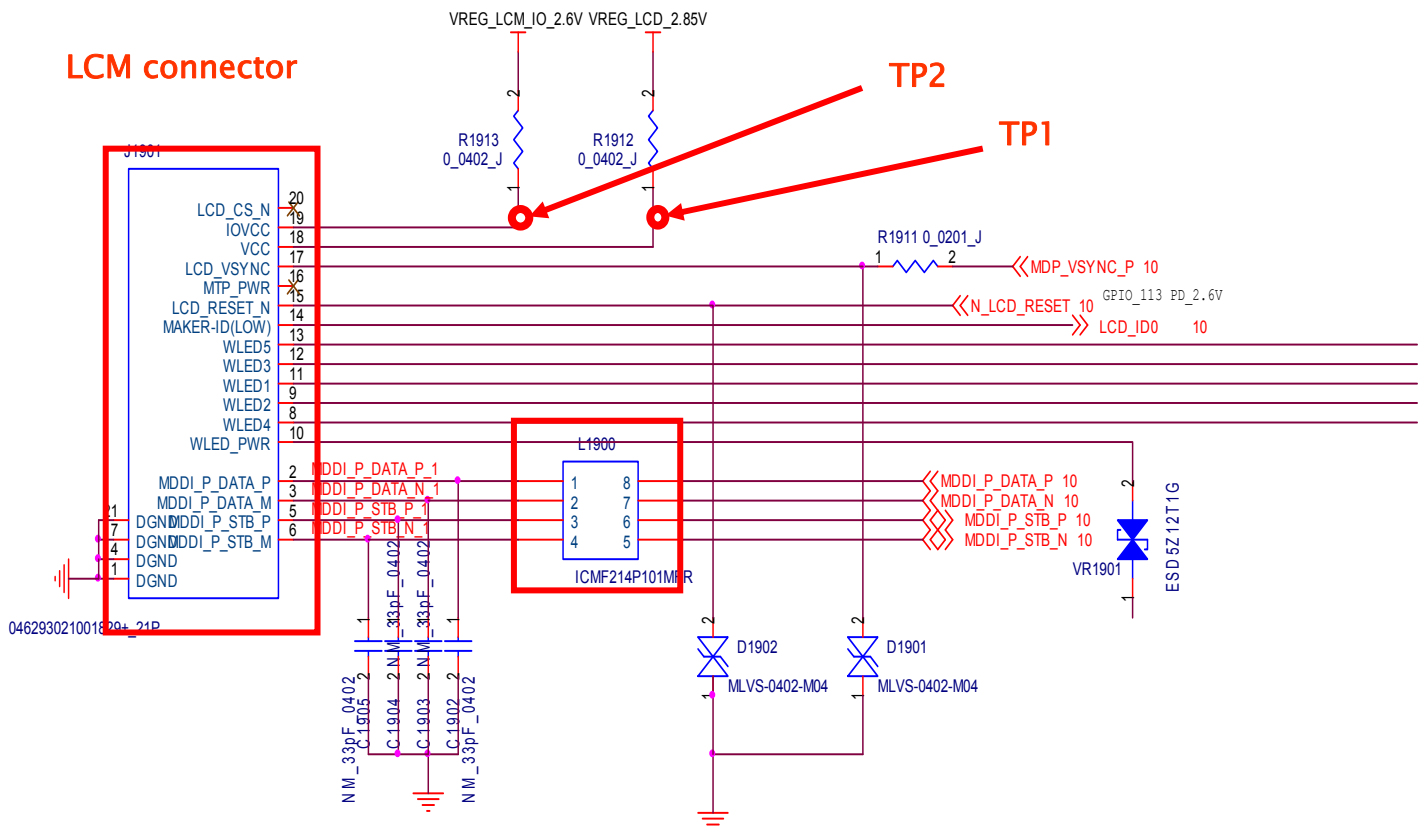
TROUBLE SHOOTING

Main board top



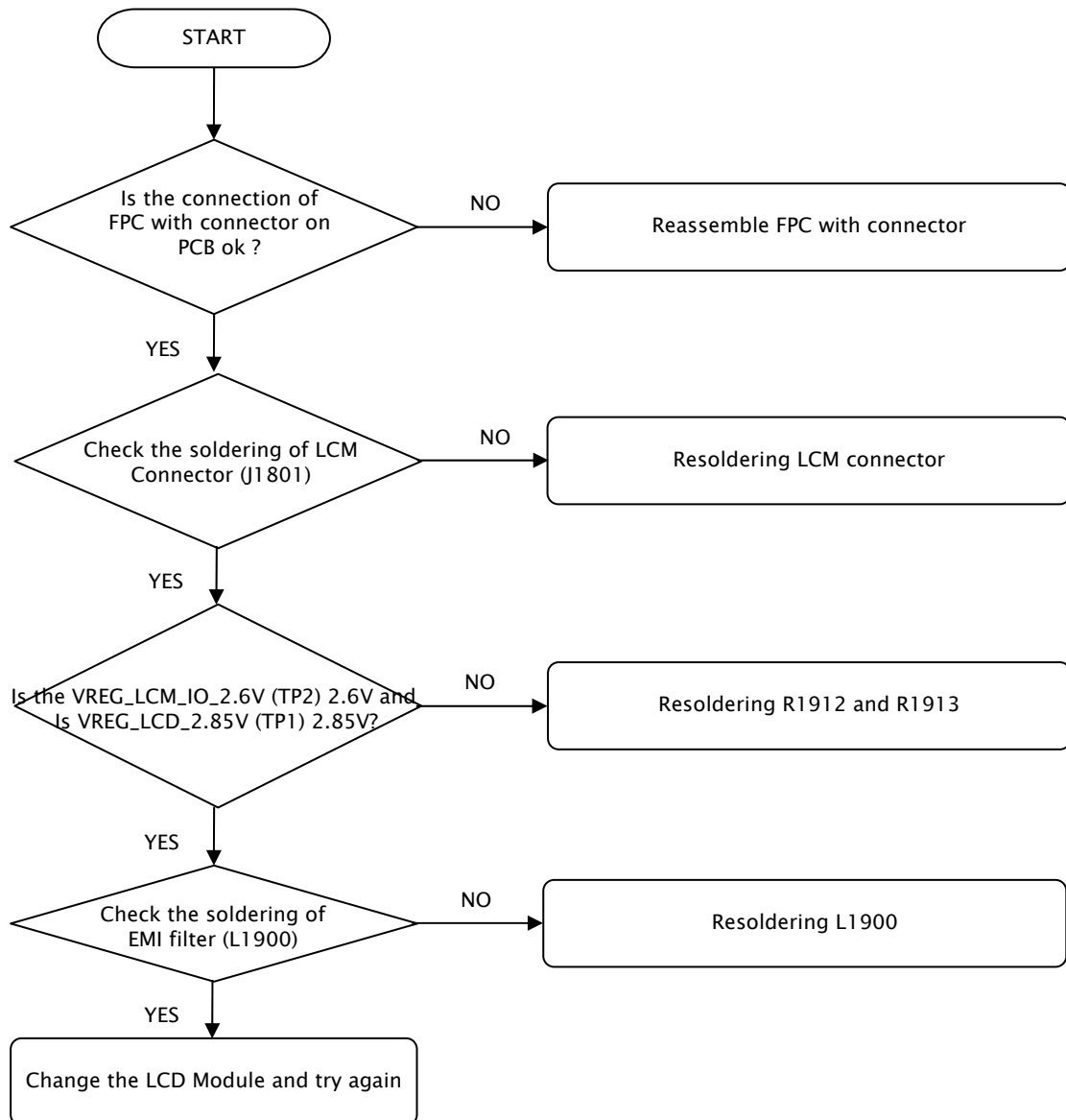
Circuit Diagram

Main Board



TROUBLE SHOOTING

Checking Flow

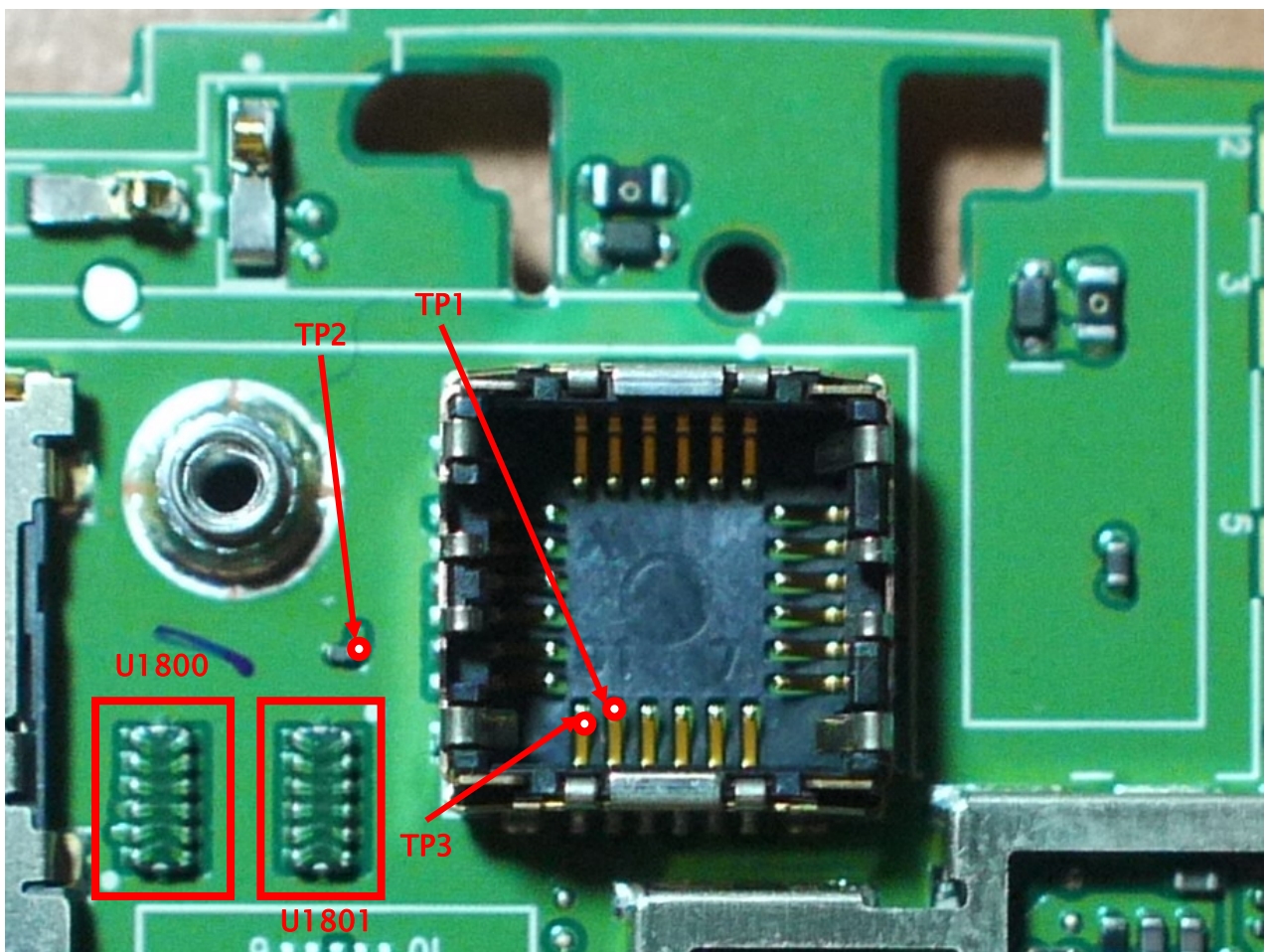


TROUBLE SHOOTING

4.13 2M Camera Trouble

Picture Data

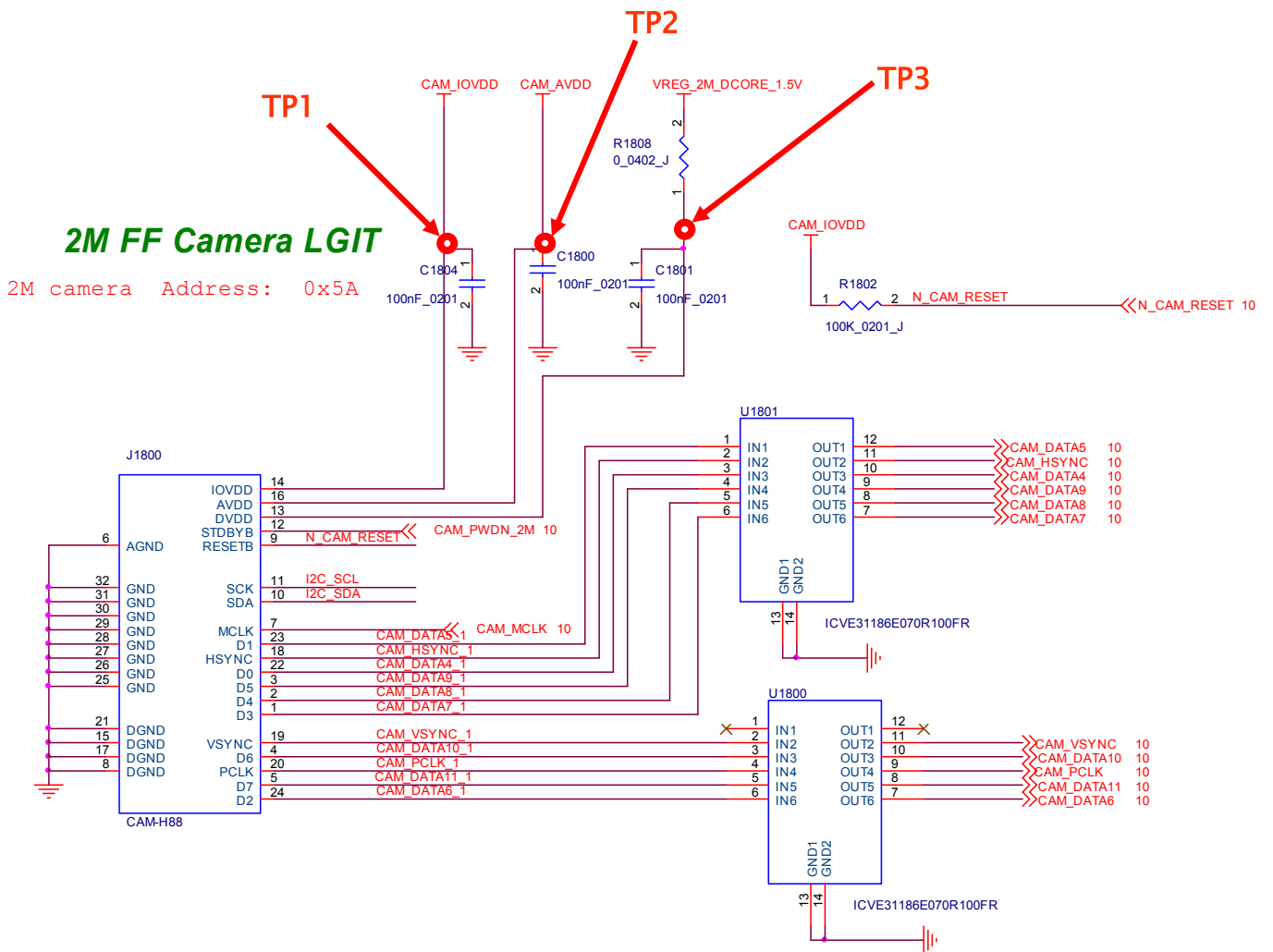
Main board top



TROUBLE SHOOTING

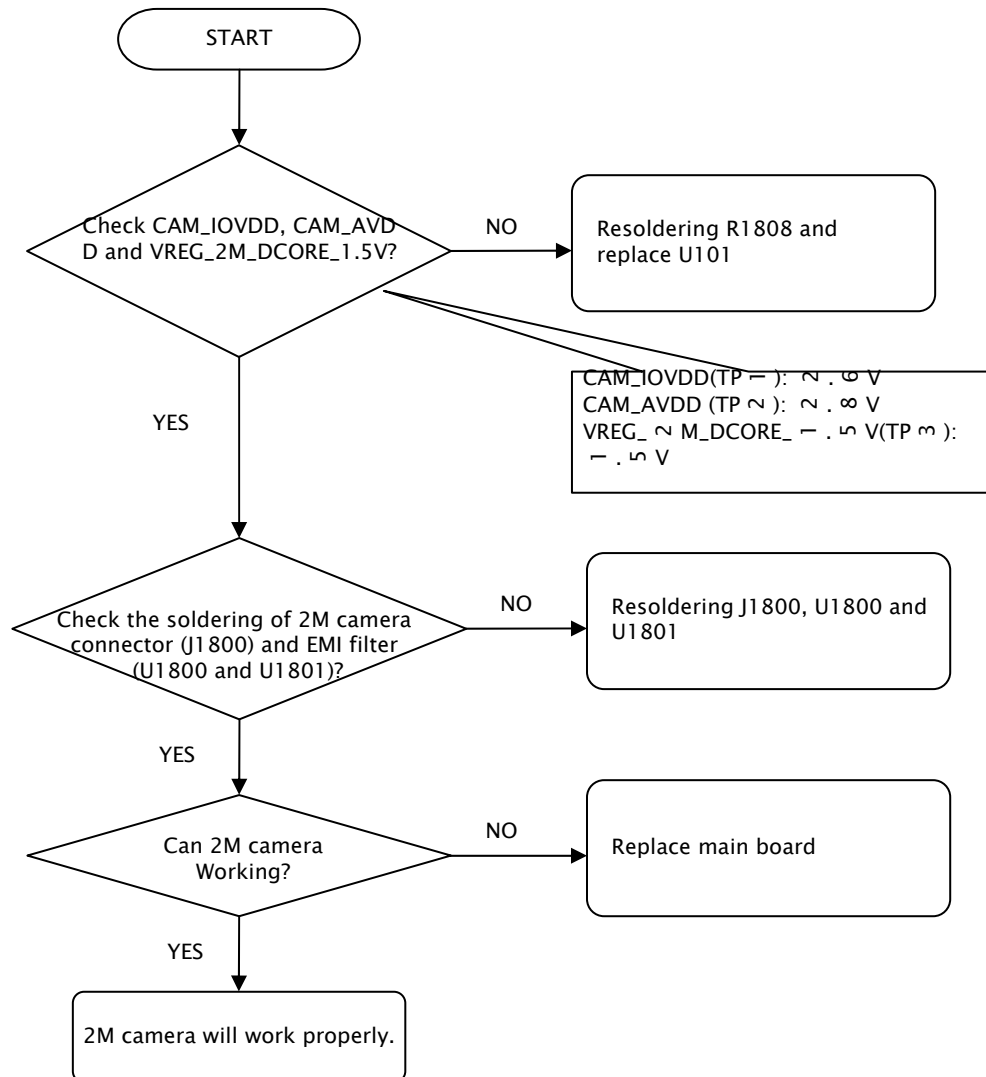
Circuit Diagram

Main board



TROUBLE SHOOTING

Checking Flow

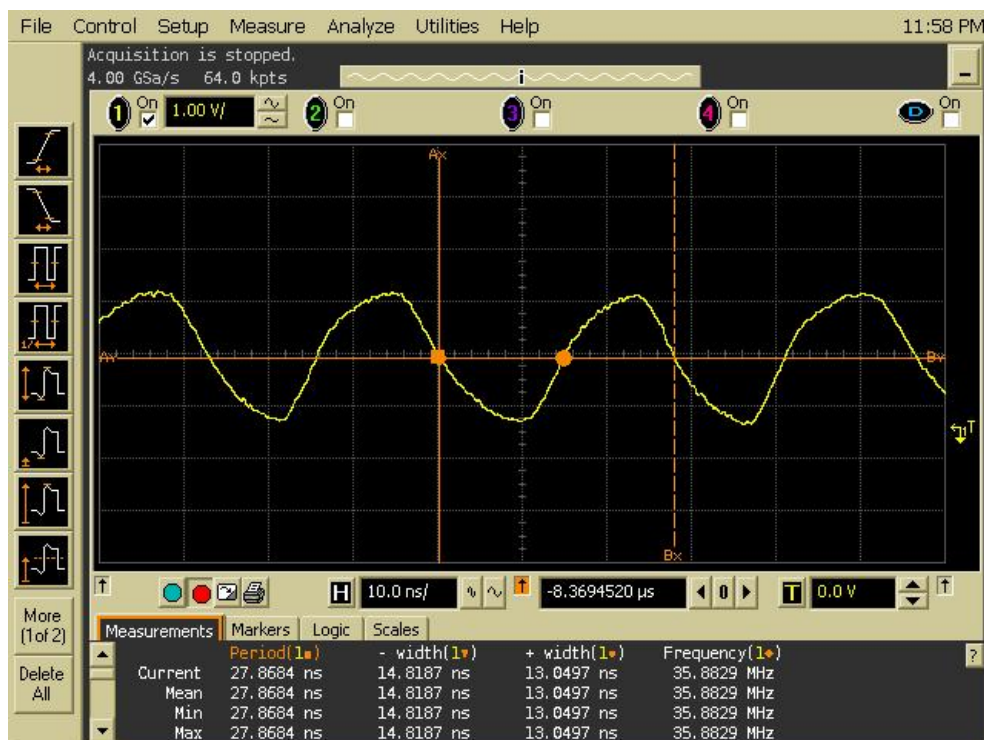


TROUBLE SHOOTING

Waveform



CAMIF_MCLK1



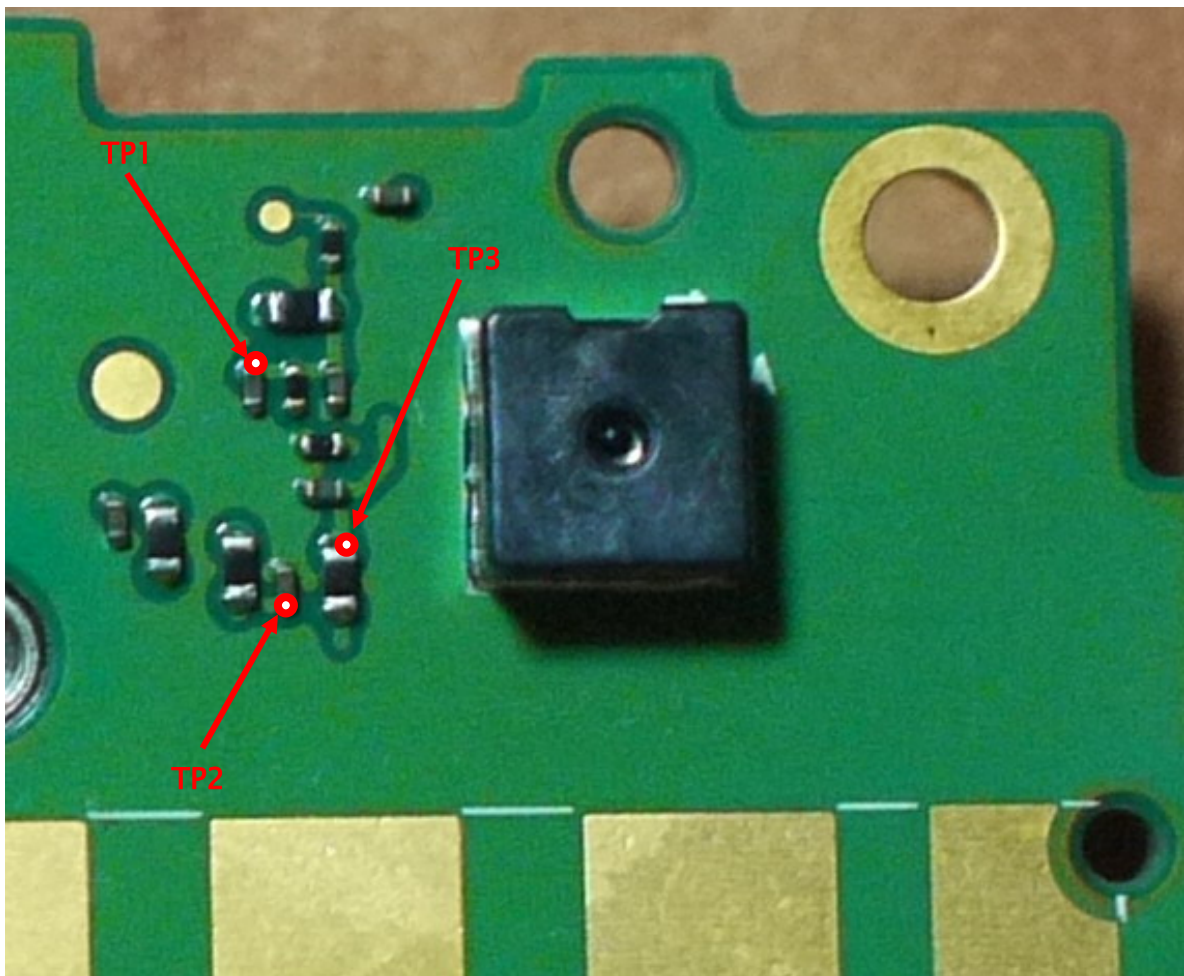
CAMIF_PCLK1

TROUBLE SHOOTING

4.14 VGA Camera Trouble

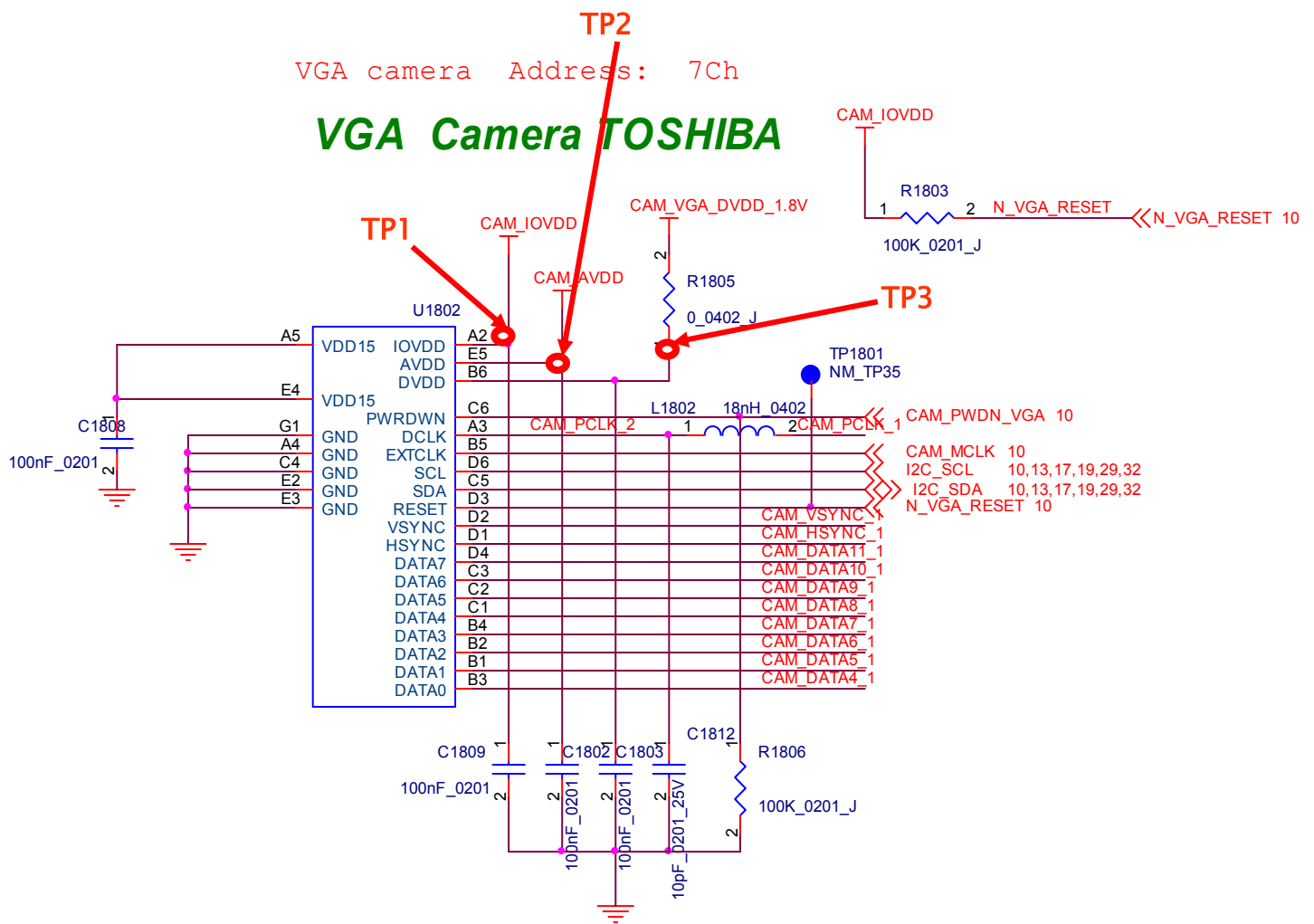
Picture Data

Main board top



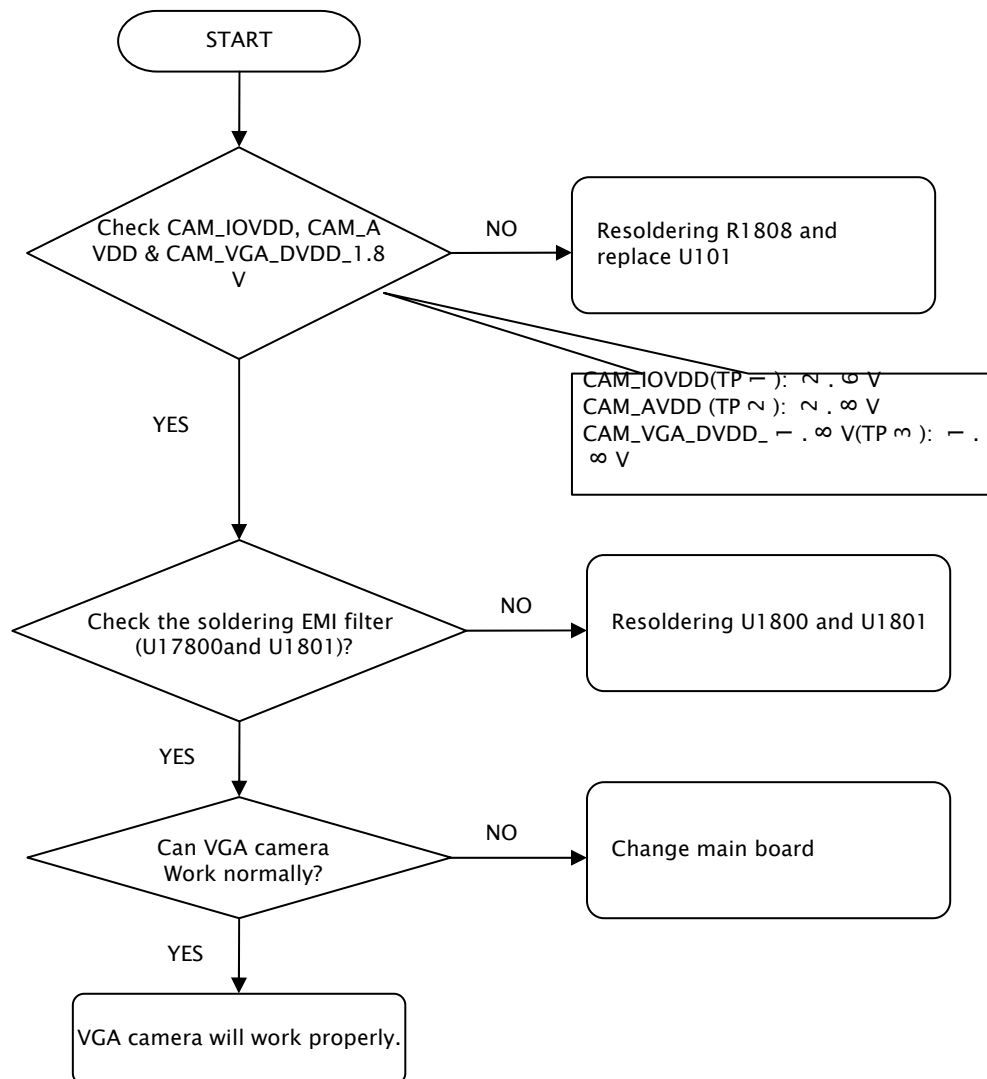
Circuit Diagram

Main board



TROUBLE SHOOTING

Checking Flow

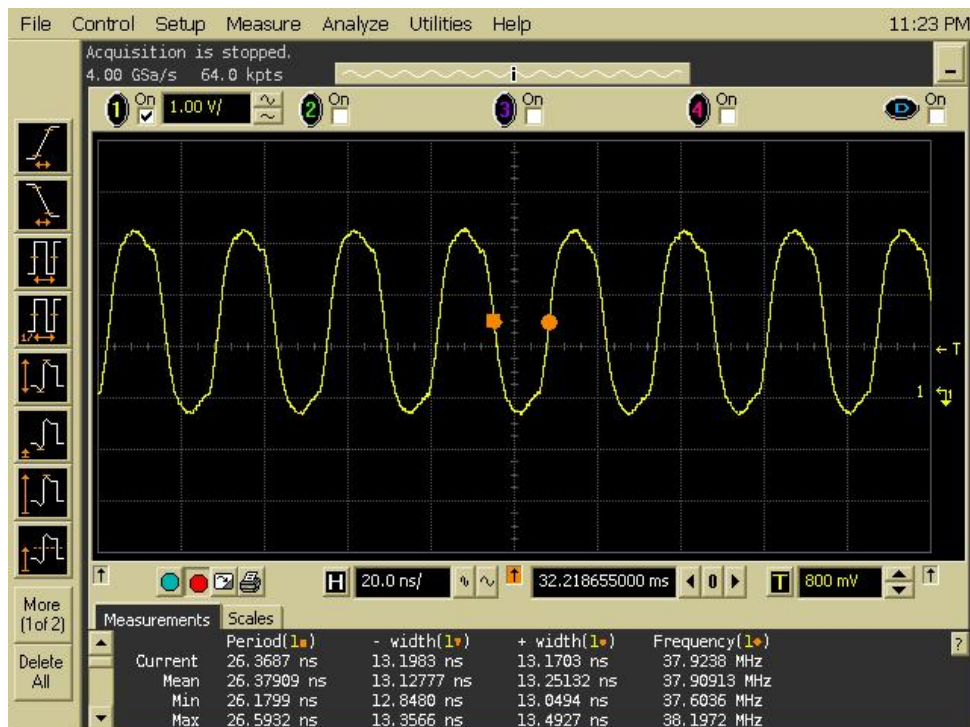


TROUBLE SHOOTING

Waveform



CAMIF_MCLK1



CAMIF_PCLK2

TROUBLE SHOOTING

4.1 5 LCD backlight Trouble

Picture Data

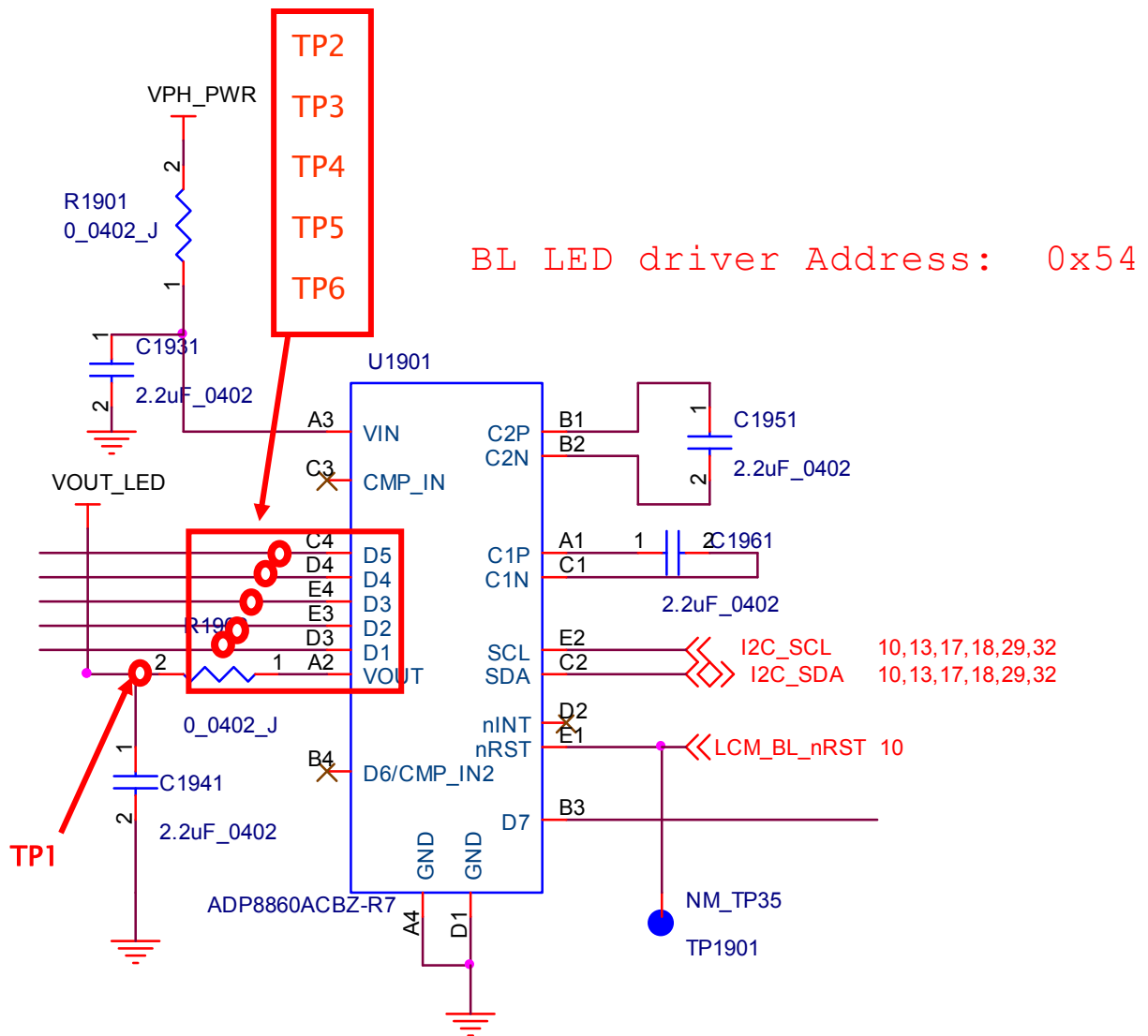
Main board Top



TROUBLE SHOOTING

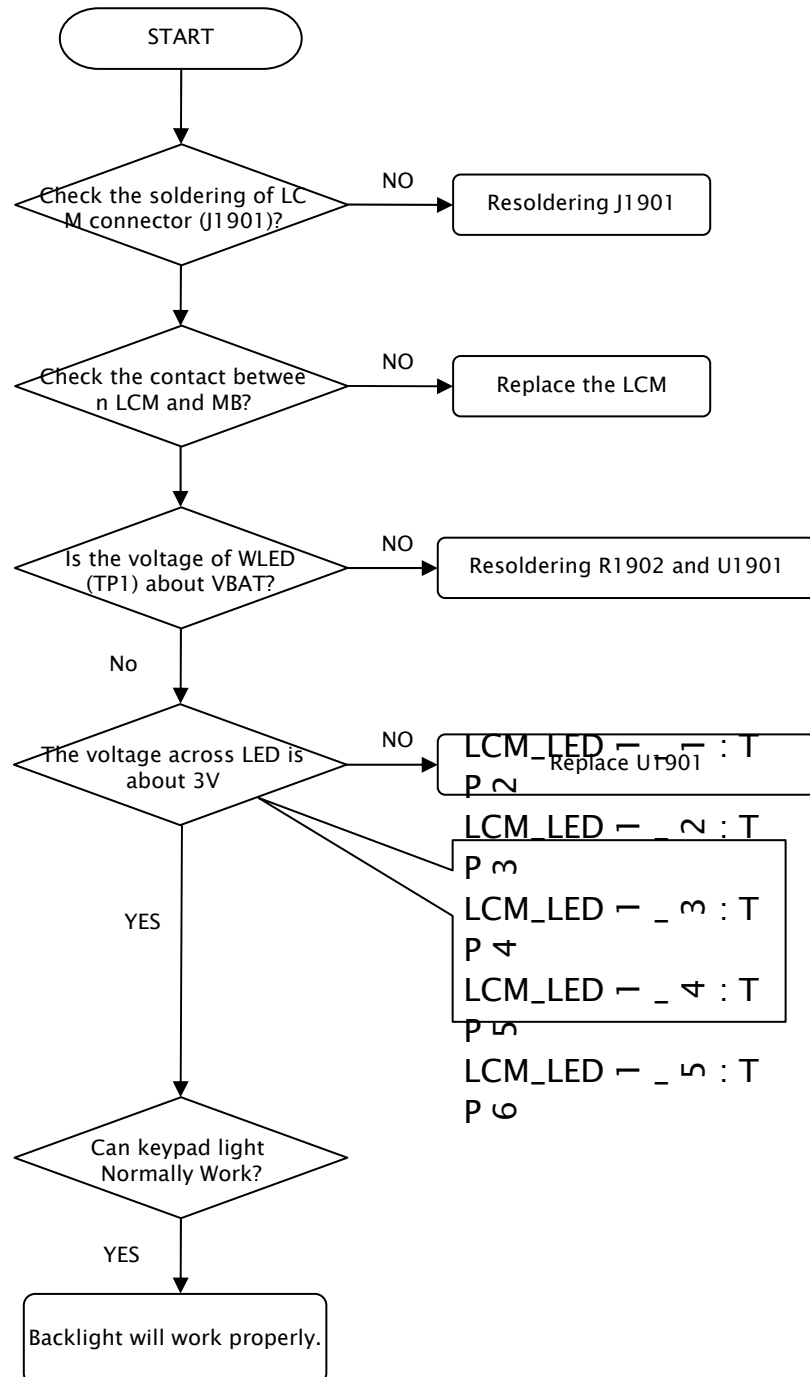
Circuit Diagram

Main board



TROUBLE SHOOTING

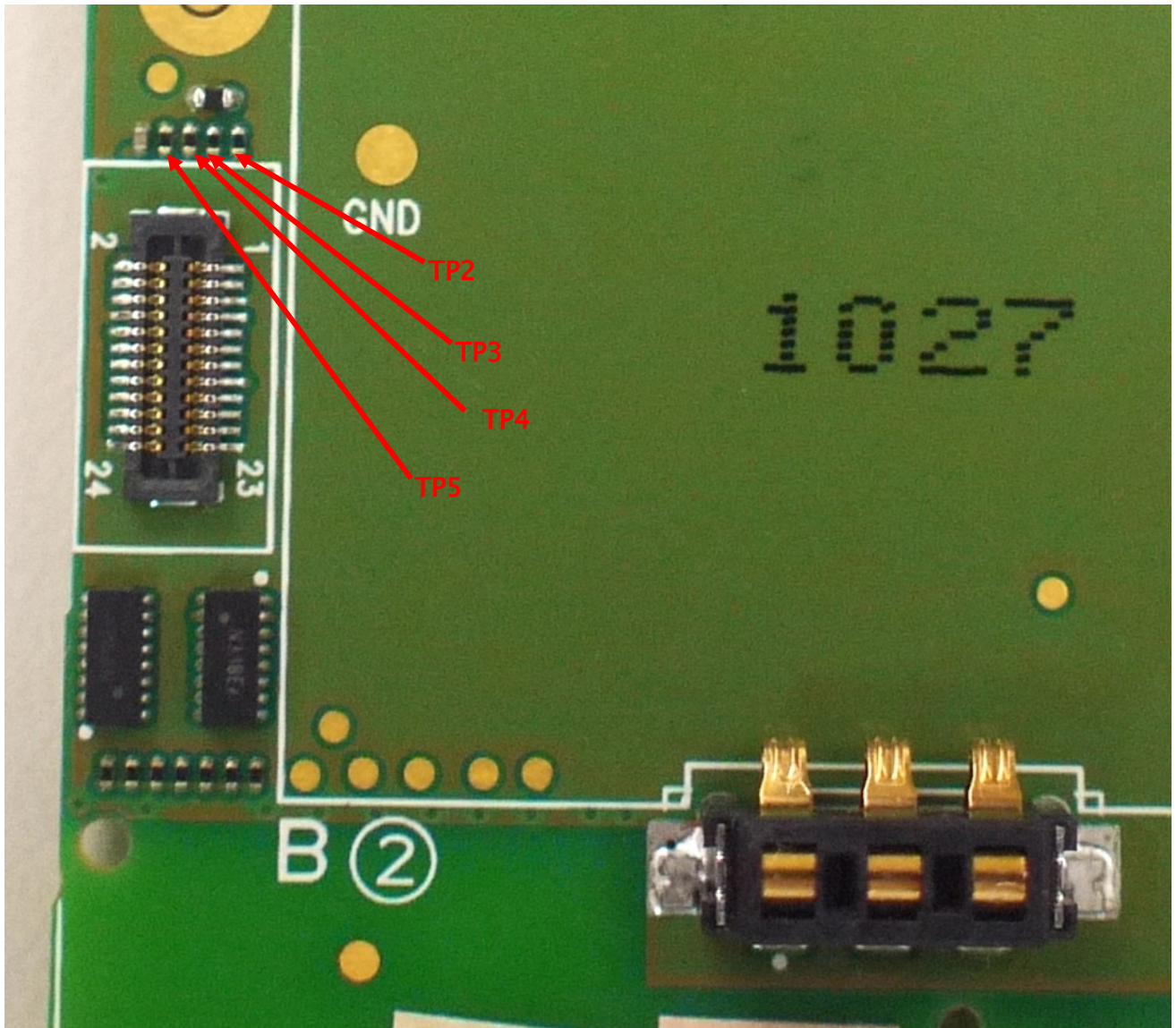
Checking Flow



4.16 KEYPAD Light Trouble

Picture Data

Main board bottom



Picture Data

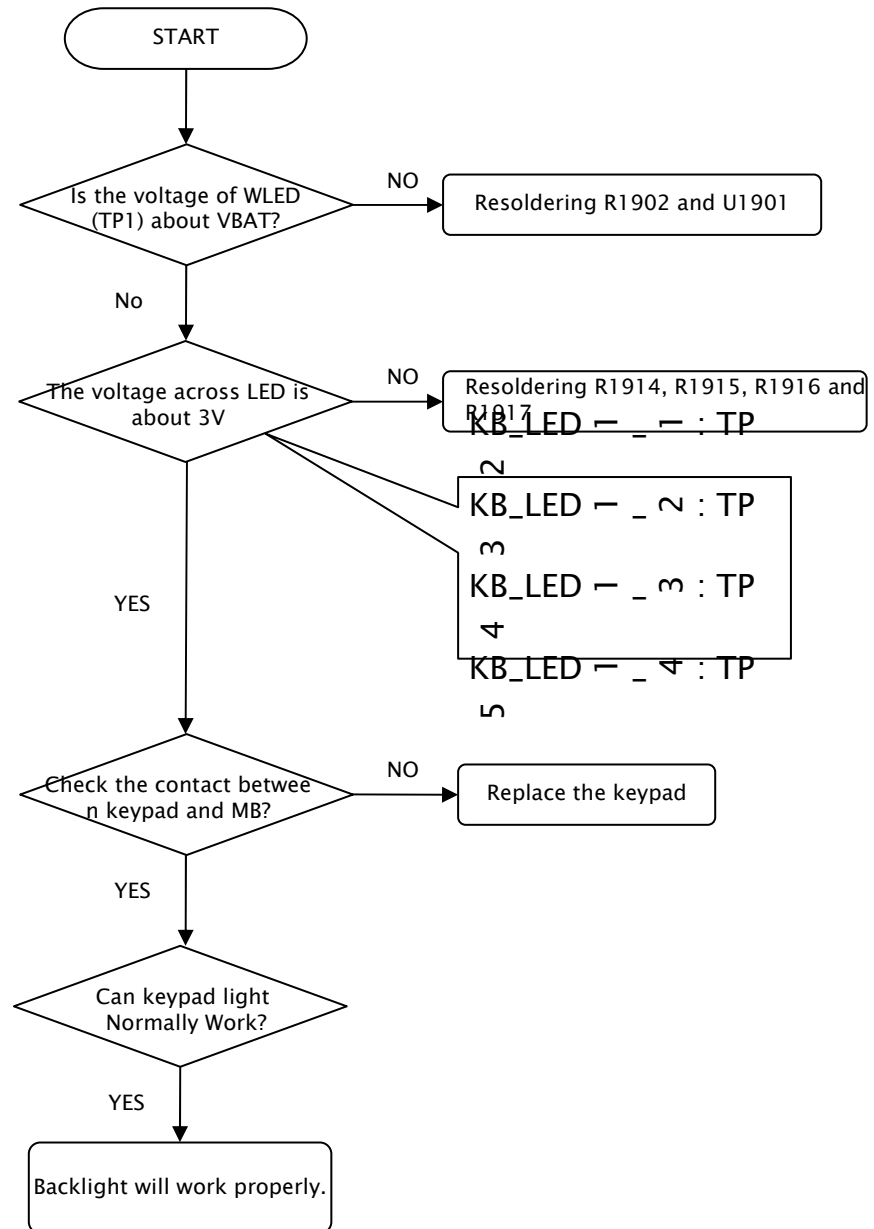
Main board Top



[illegible]

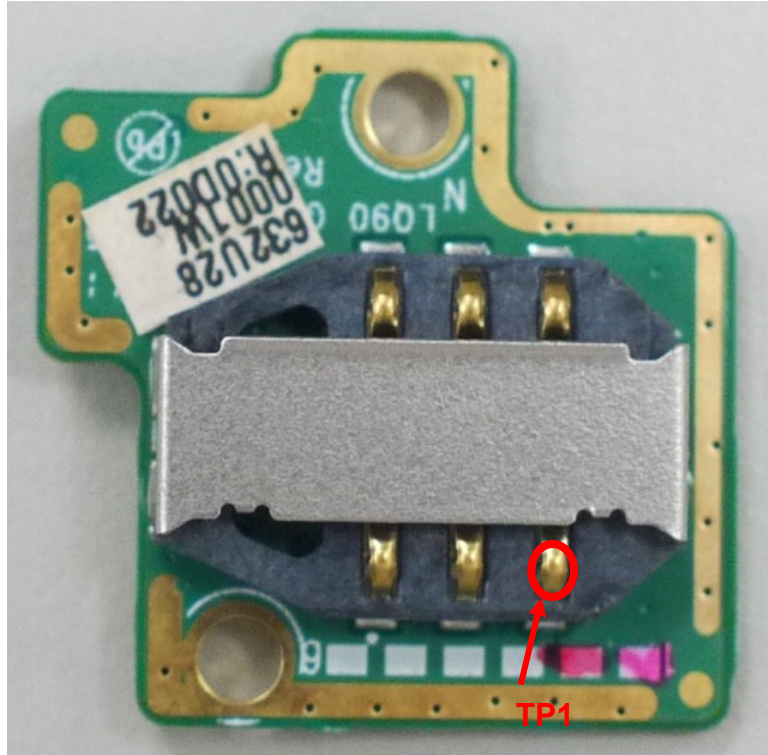
TROUBLE SHOOTING

Checking Flow

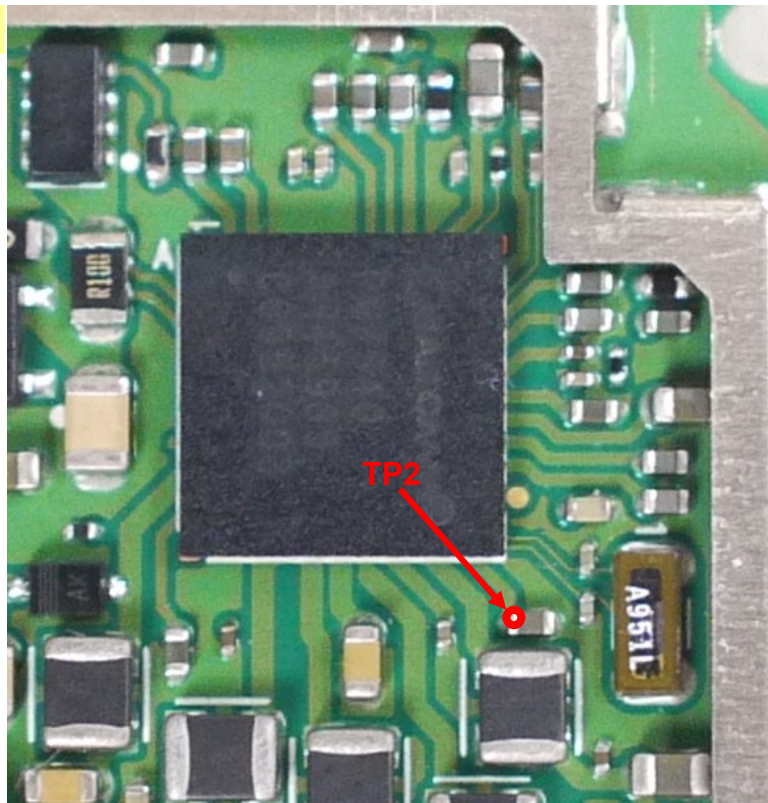


4.17 SIM Card Interface Trouble

Sub Board



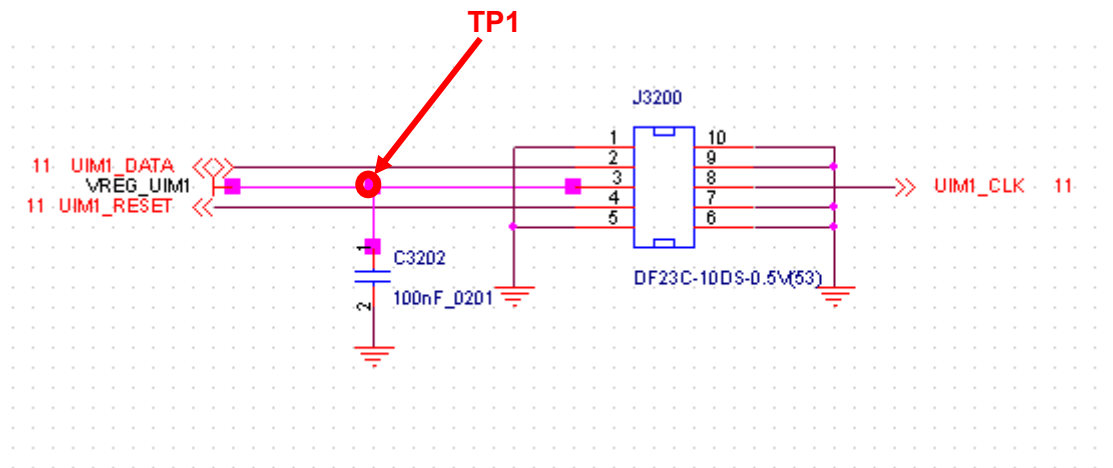
Main Board



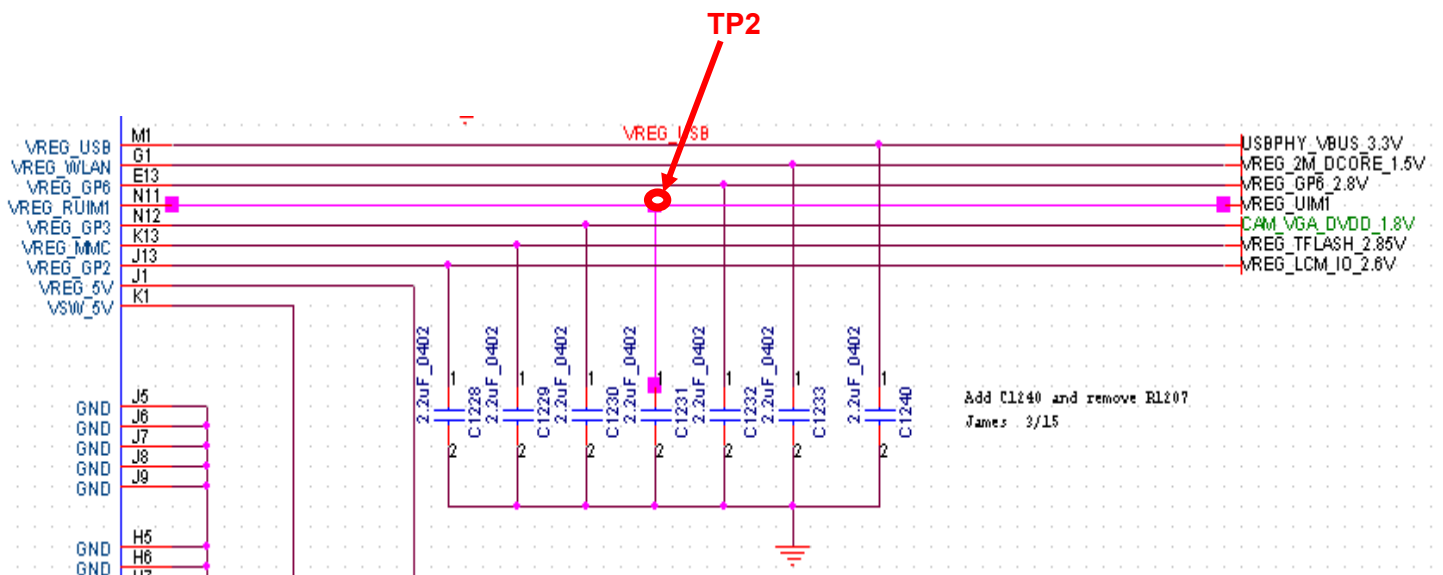
TROUBLE SHOOTING

Circuit Diagram

Sub Board

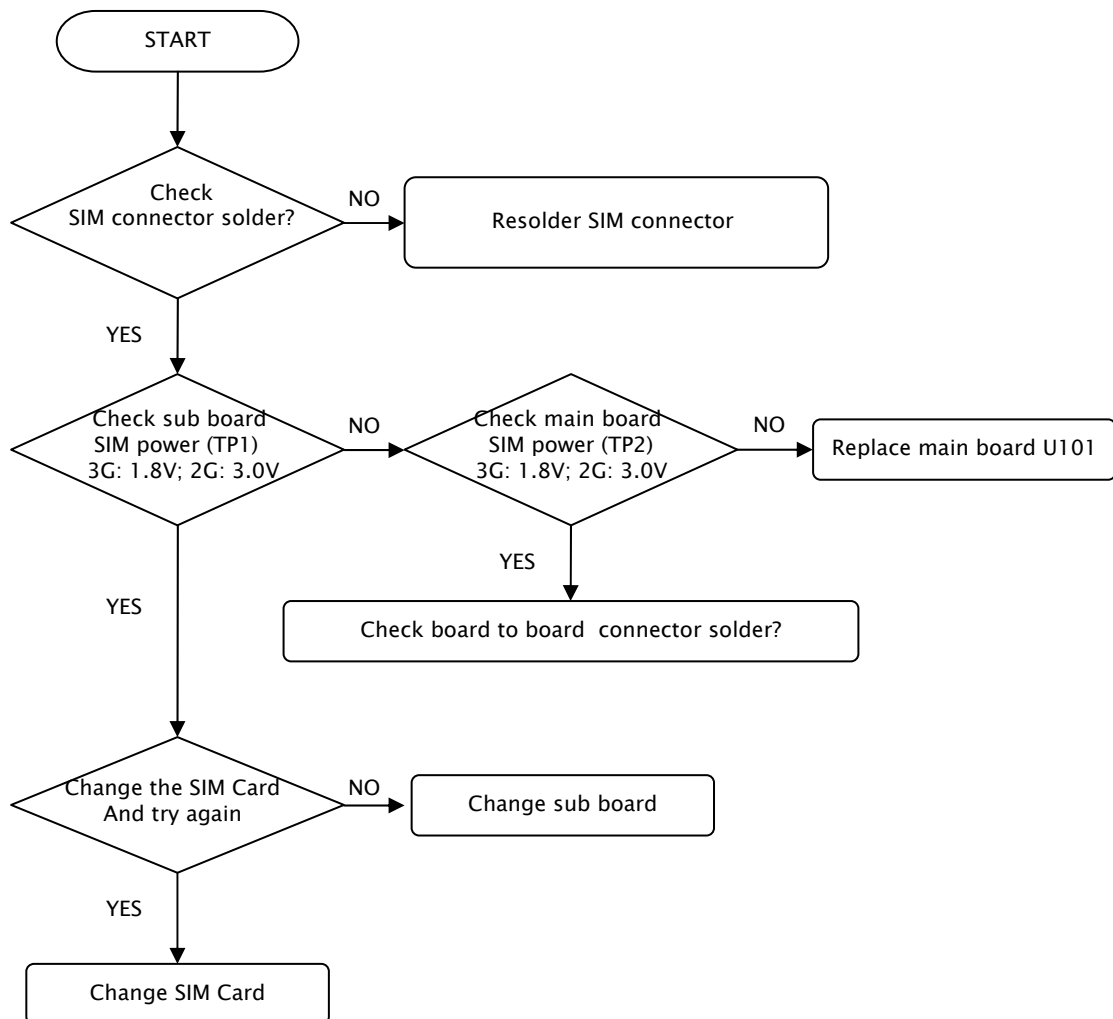


Main Board



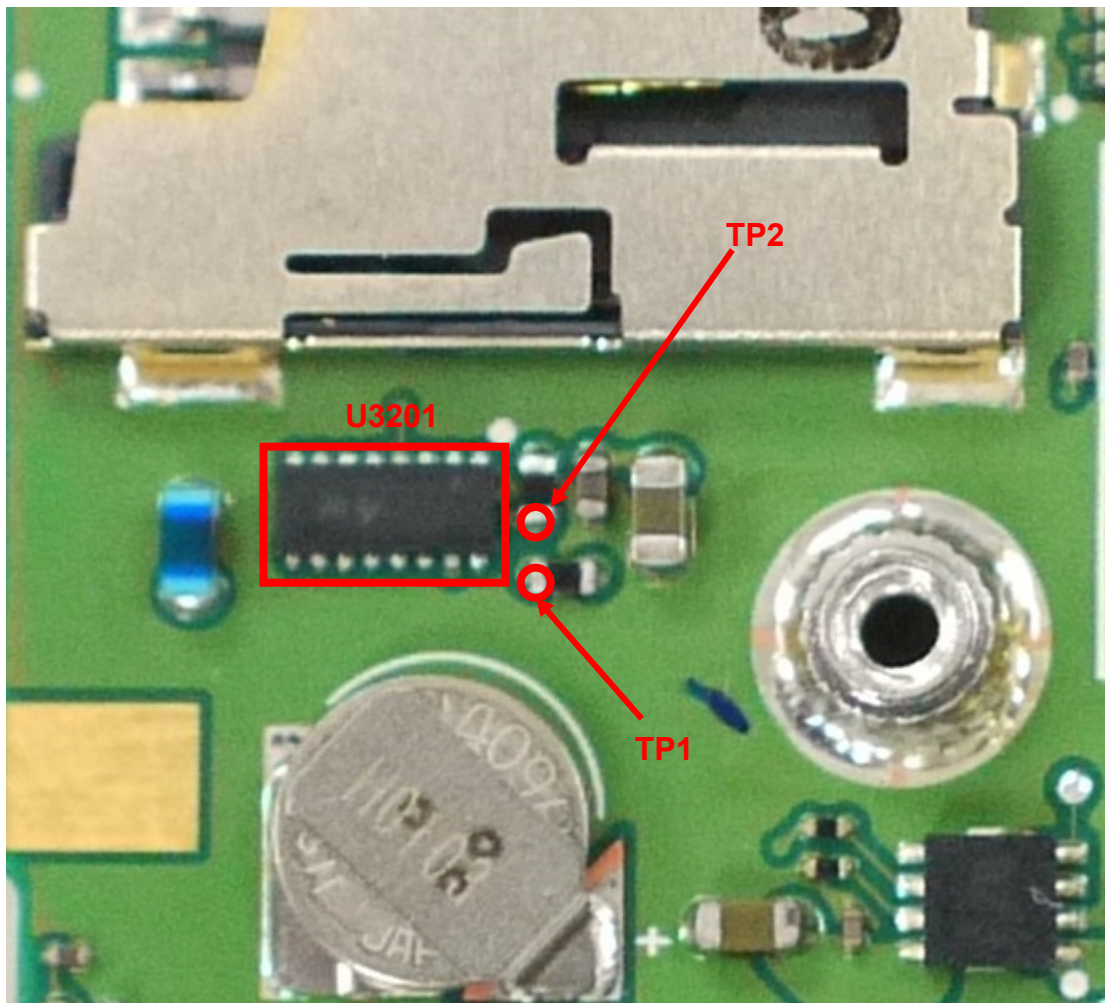
TROUBLE SHOOTING

Checking Flow



4.18 T-Flash Trouble

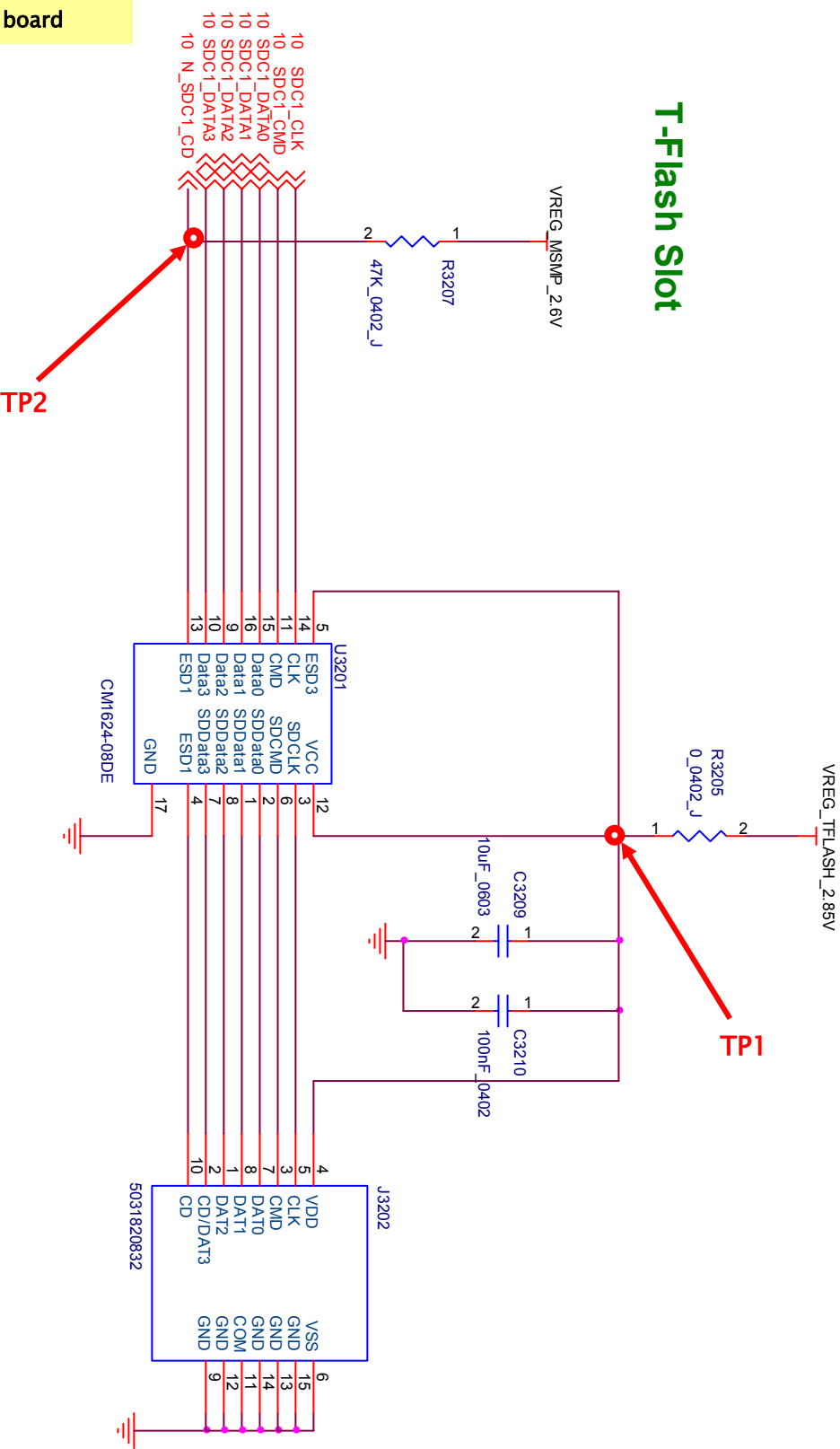
Main board Bottom



TROUBLE SHOOTING

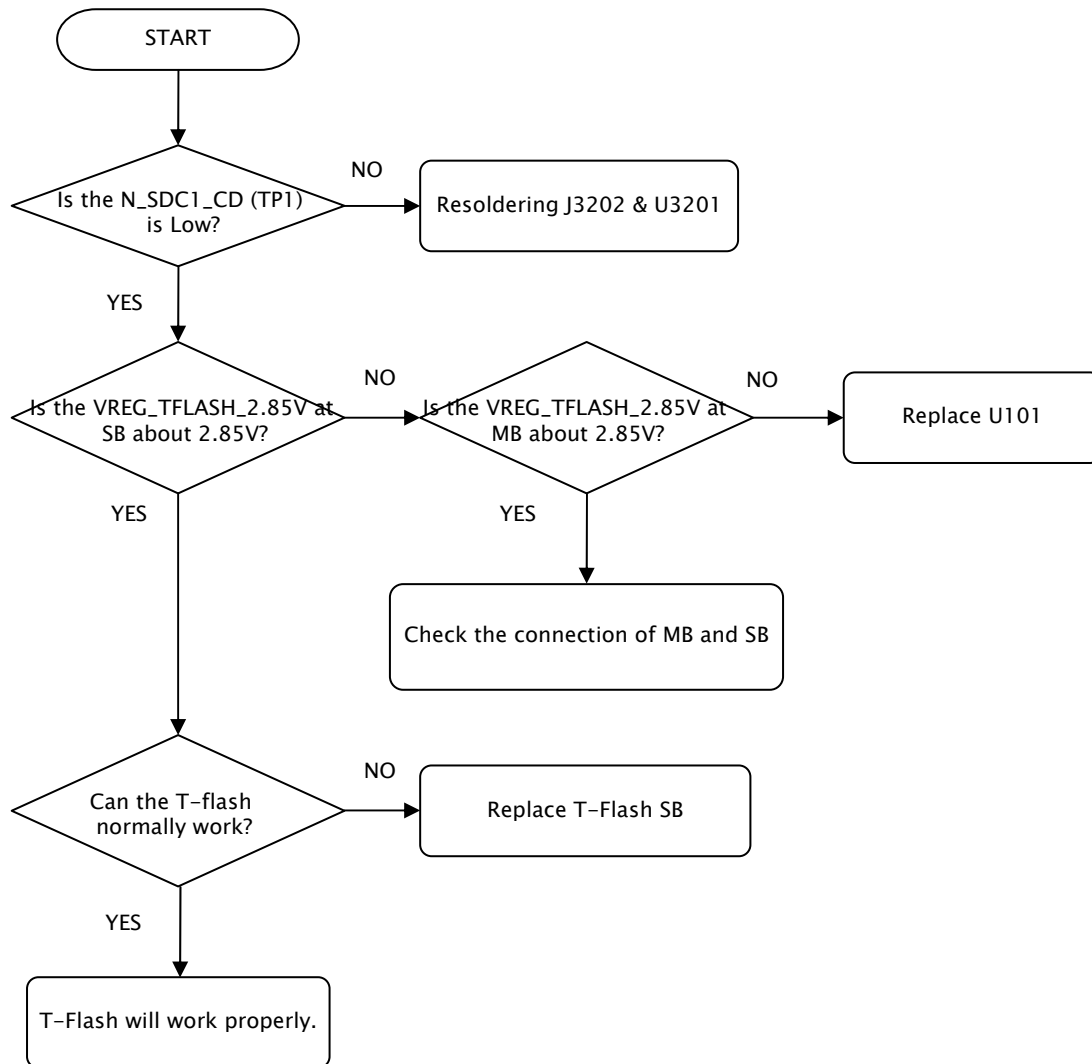
Circuit Diagram

Sub board



TROUBLE SHOOTING

Checking Flow

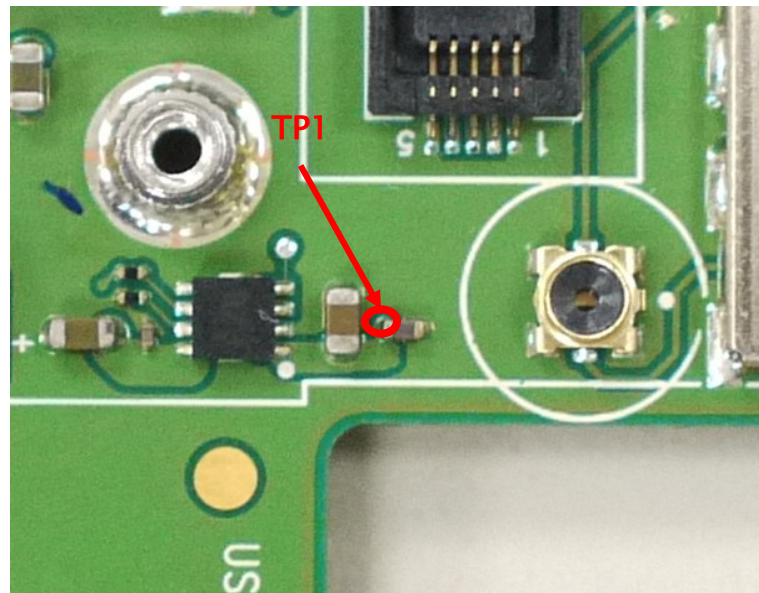


TROUBLE SHOOTING

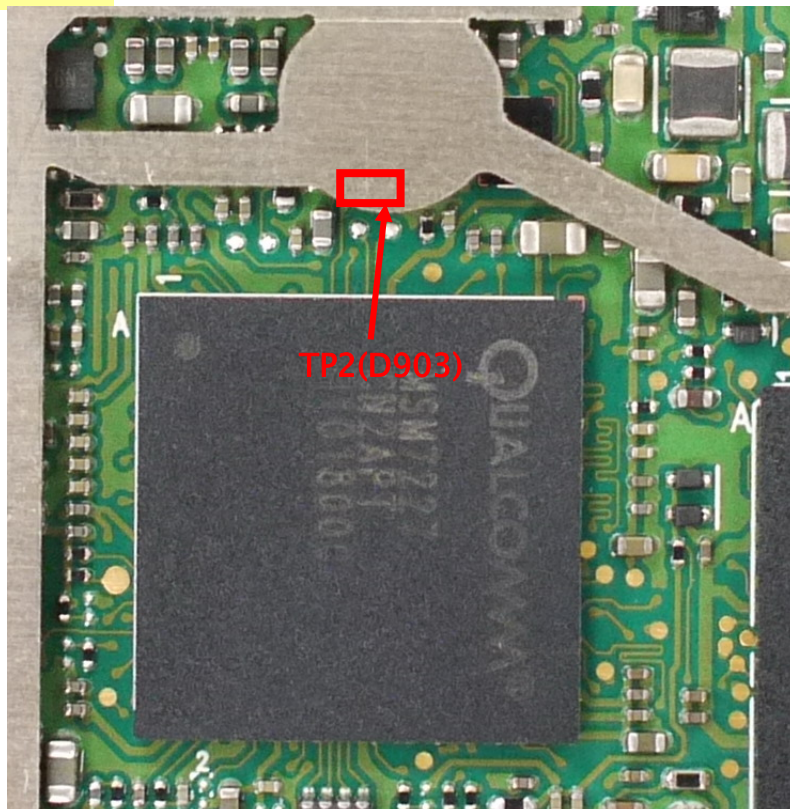
4.19 USB Trouble

Picture Data

Main board bottom



Main board top

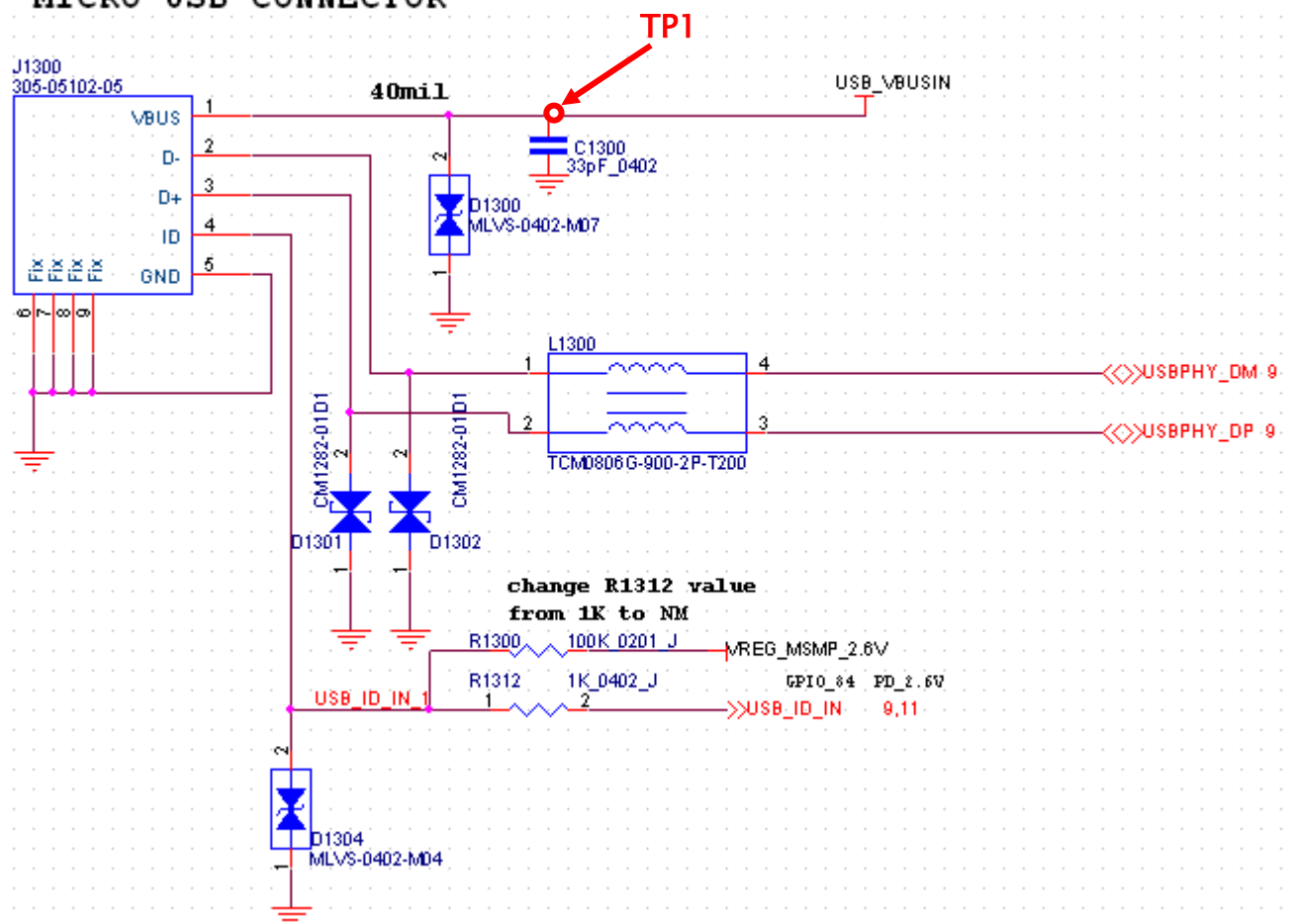


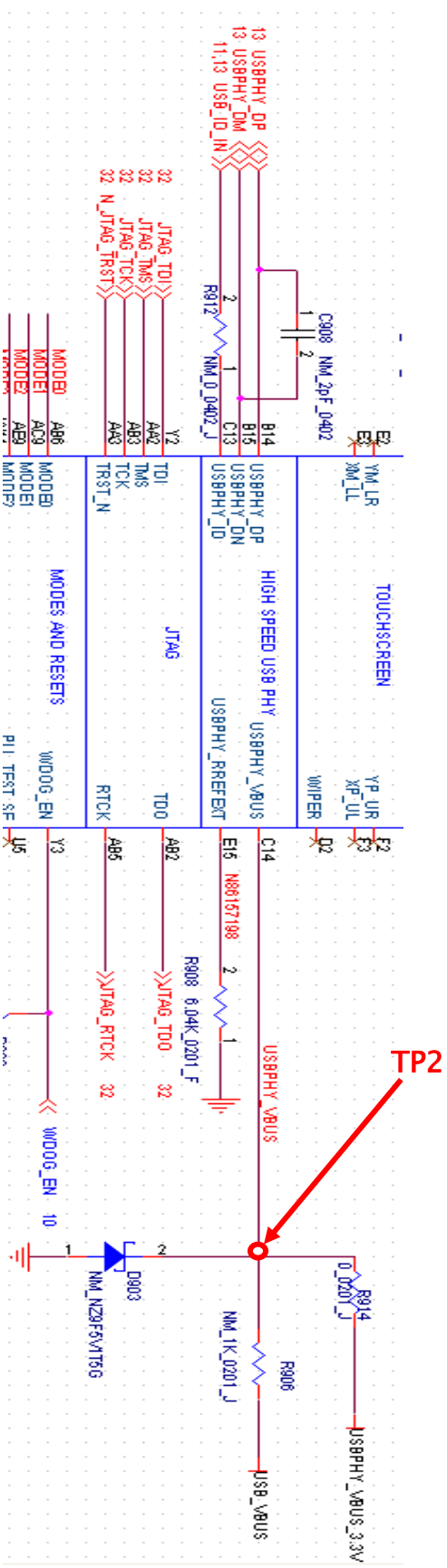
TROUBLE SHOOTING

Circuit Diagram

Main board

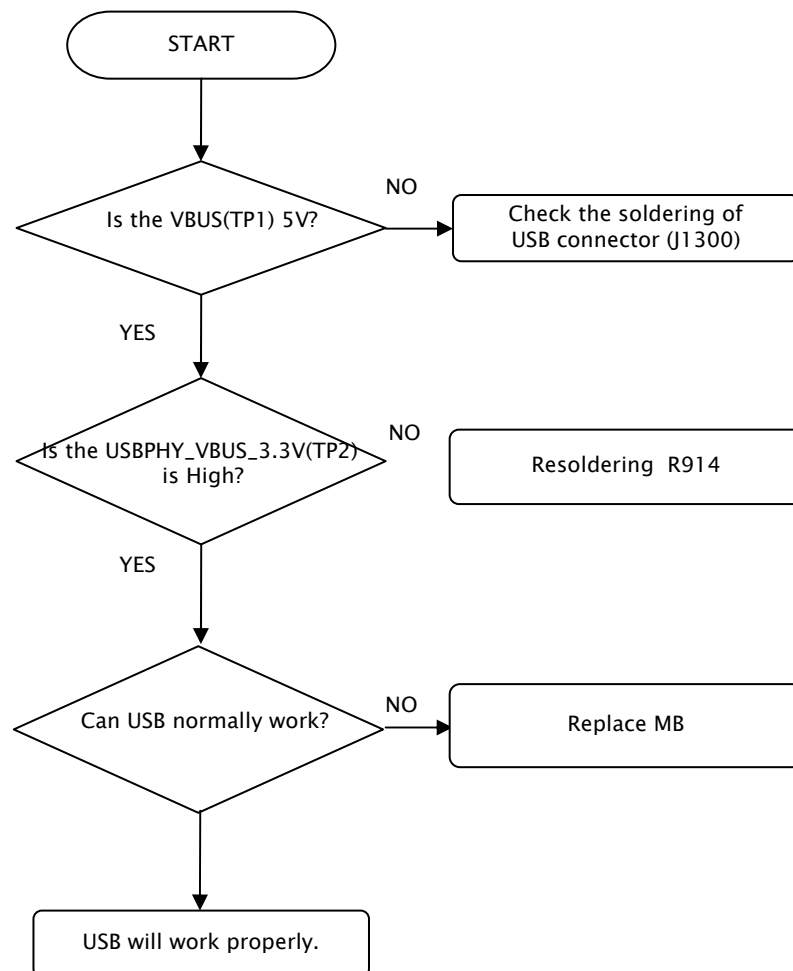
MICRO USB CONNECTOR





TROUBLE SHOOTING

Checking Flow

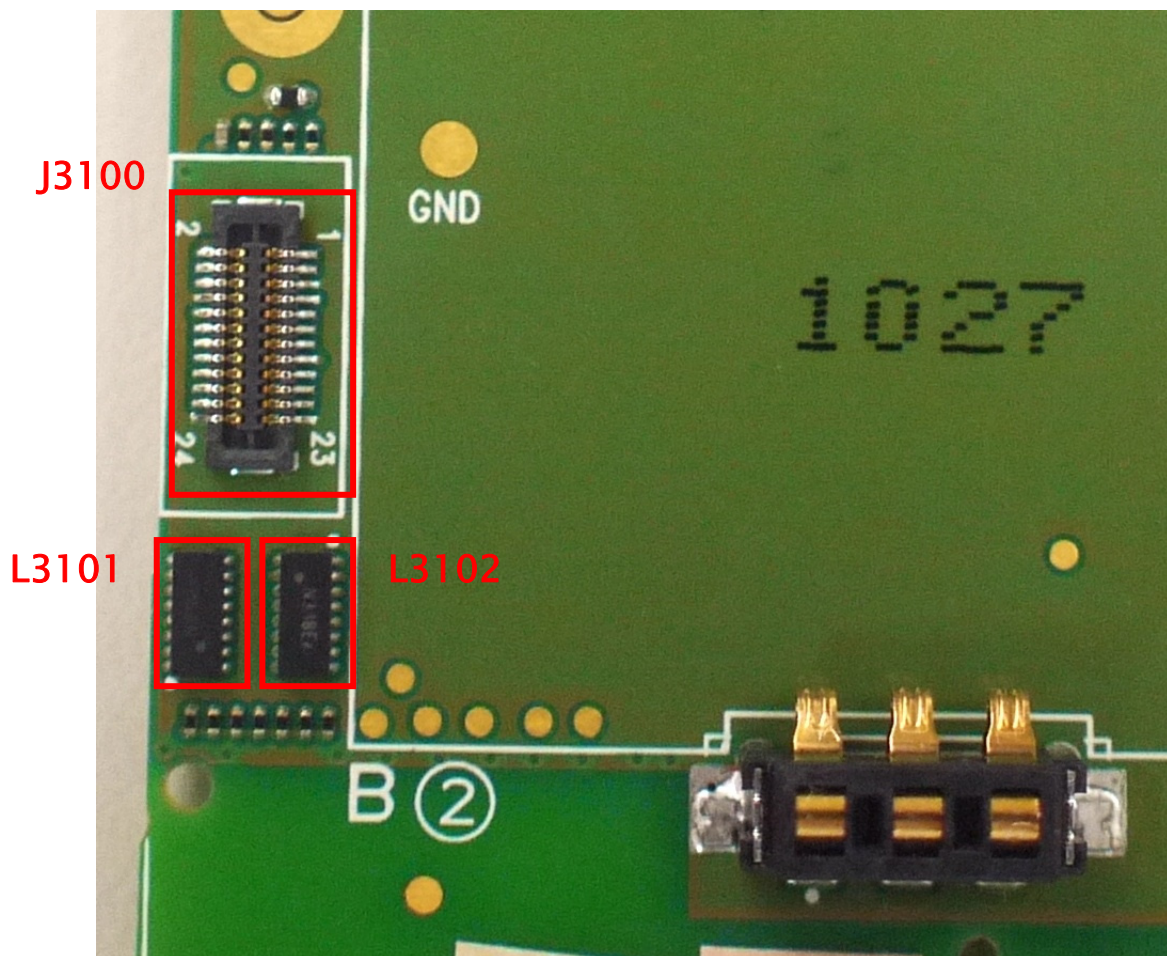


TROUBLE SHOOTING

4.20 Qwerty key Trouble

Picture Data

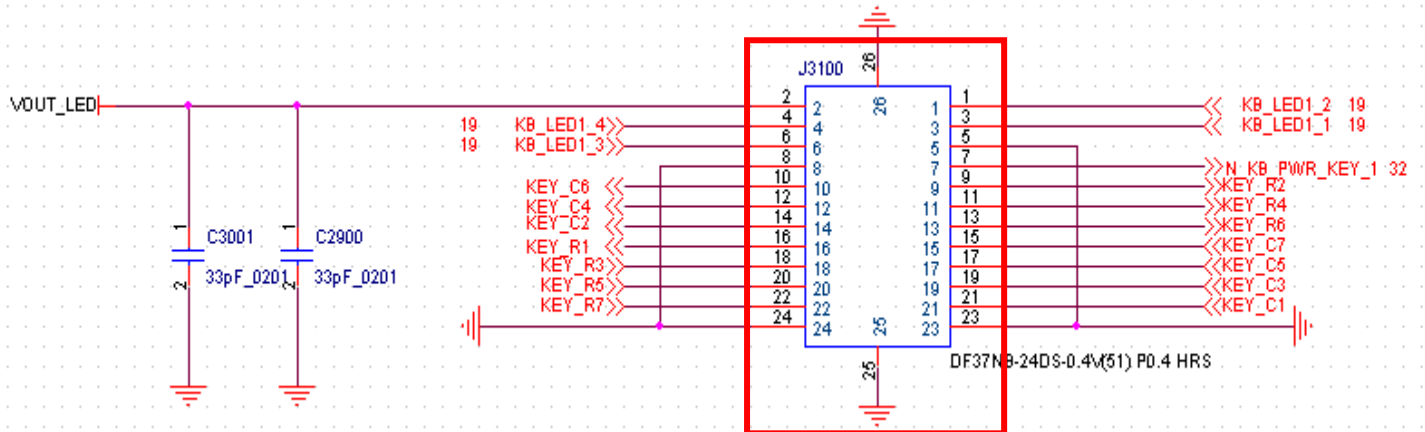
Main board top



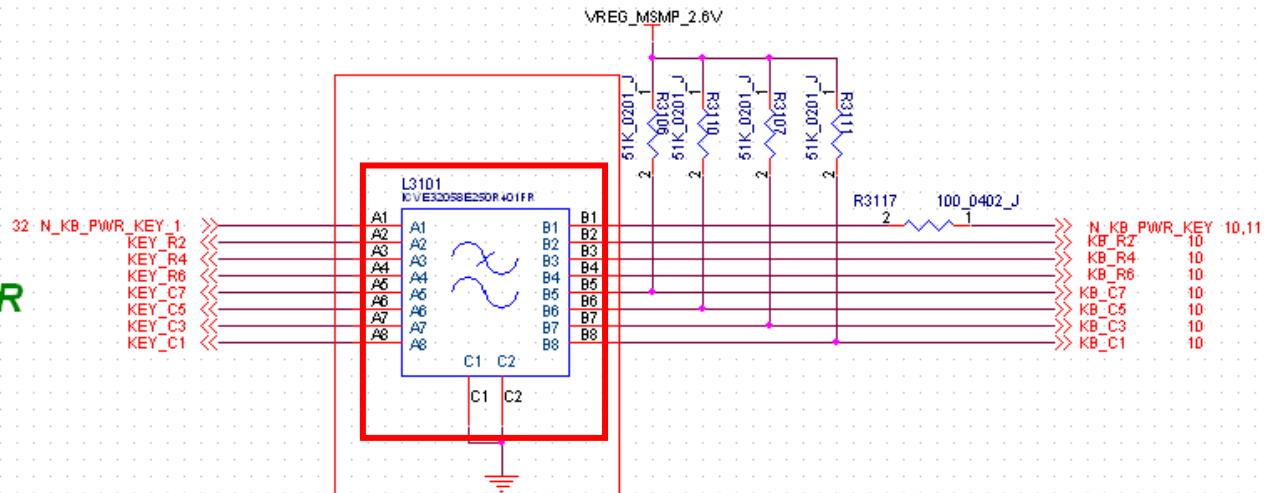
TROUBLE SHOOTING

Circuit Diagram

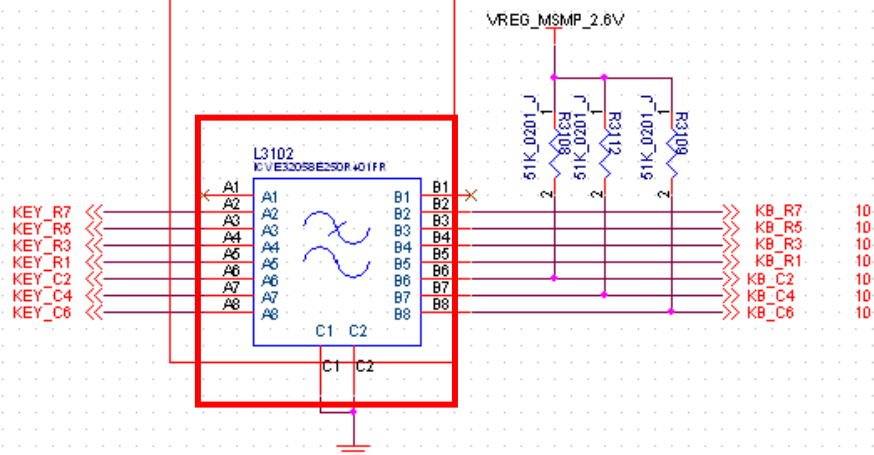
Main board



FILTER

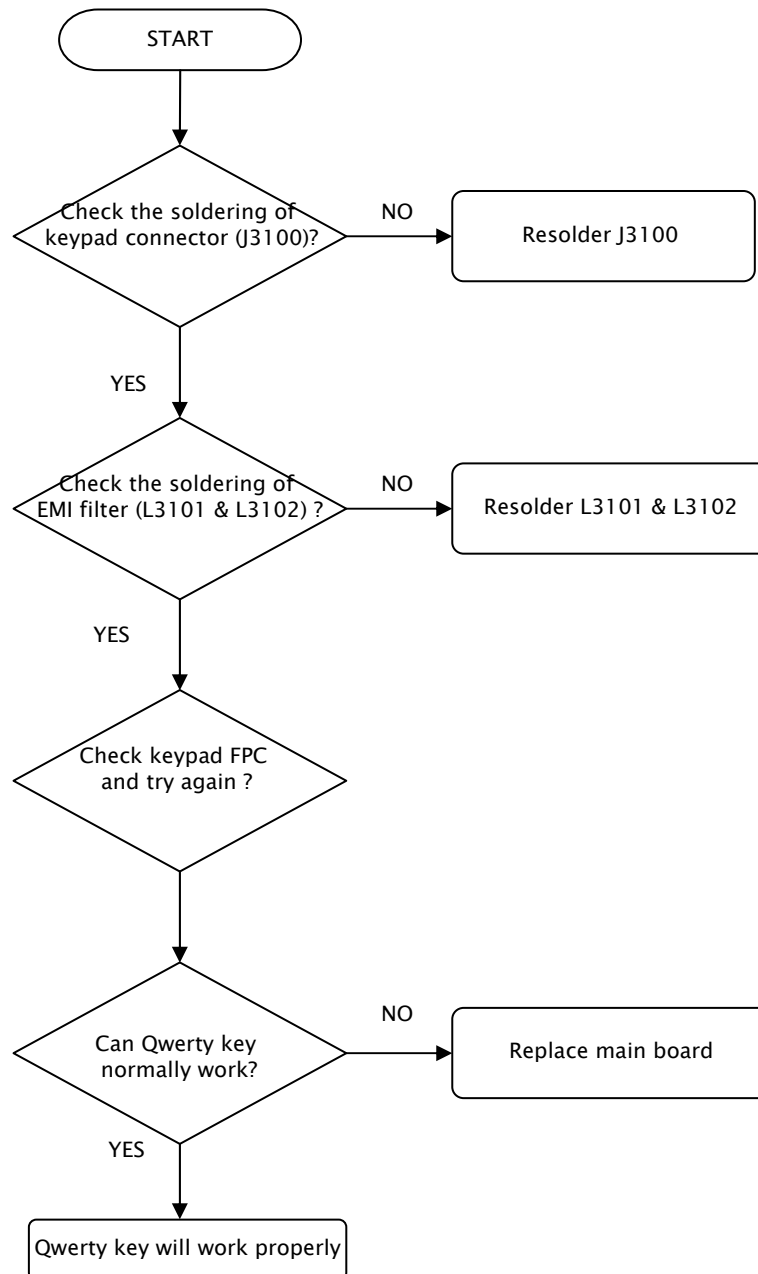


FILTER



TROUBLE SHOOTING

Checking Flow

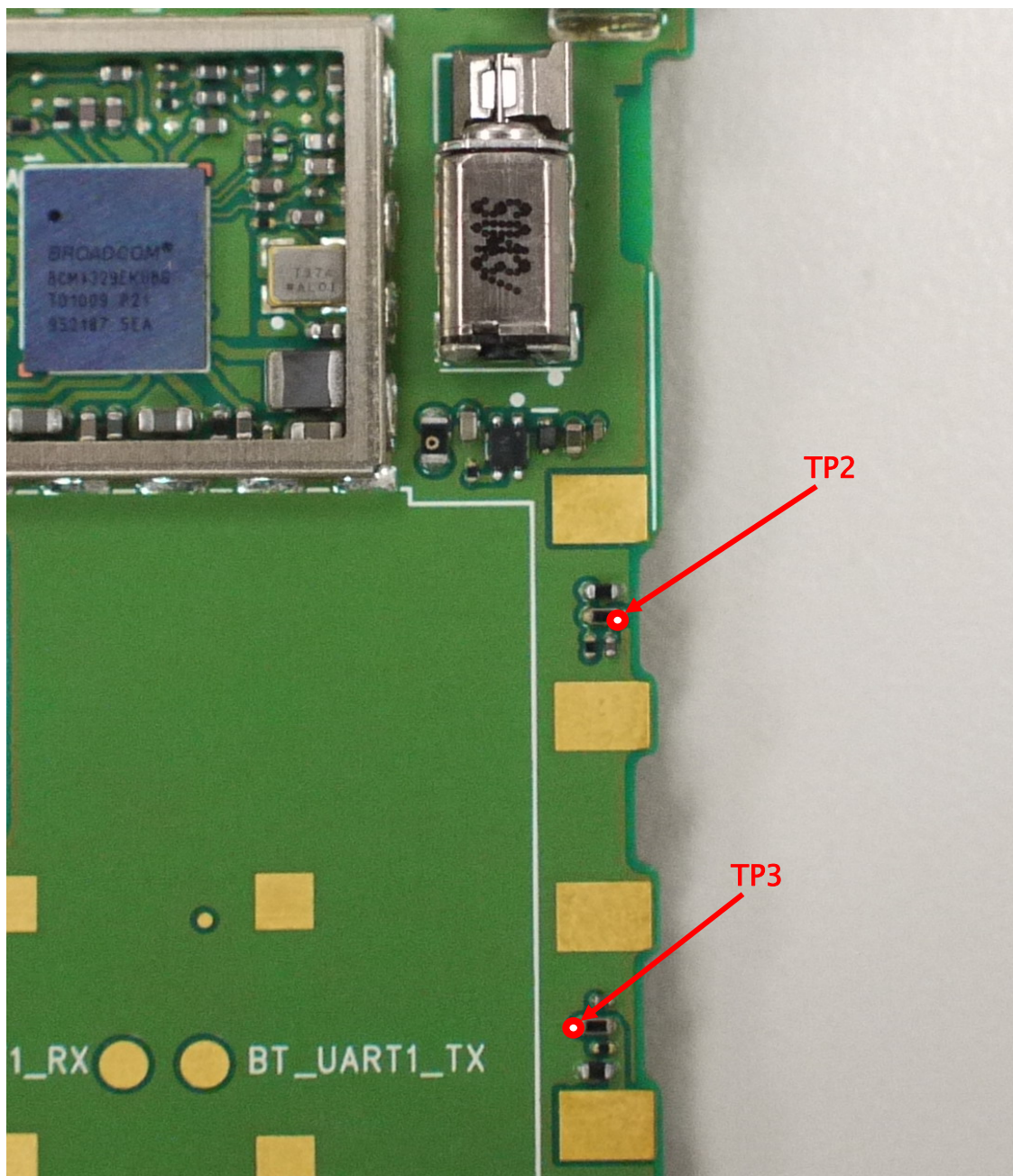


TROUBLE SHOOTING

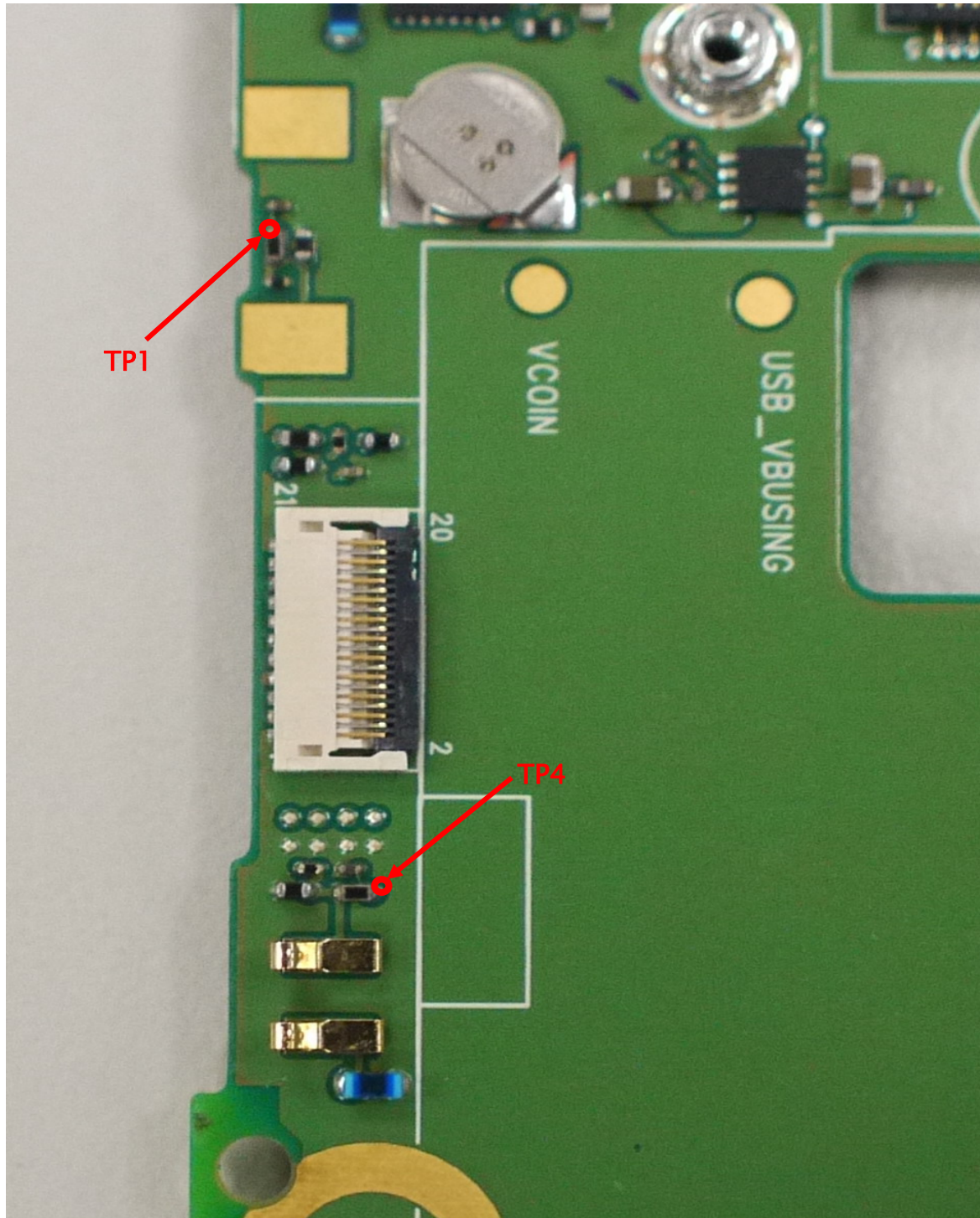
4.21 Side key Trouble

Picture Data

Main board Bottom



Main board Bottom

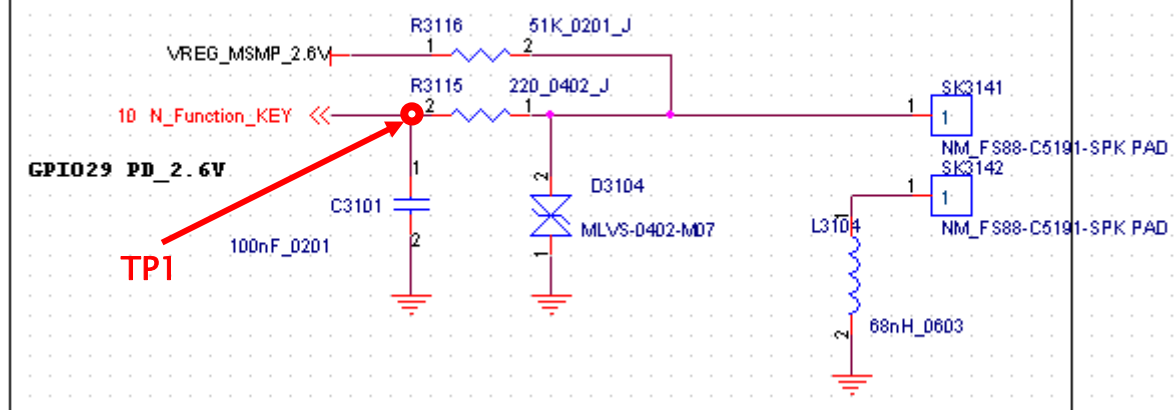


TROUBLE SHOOTING

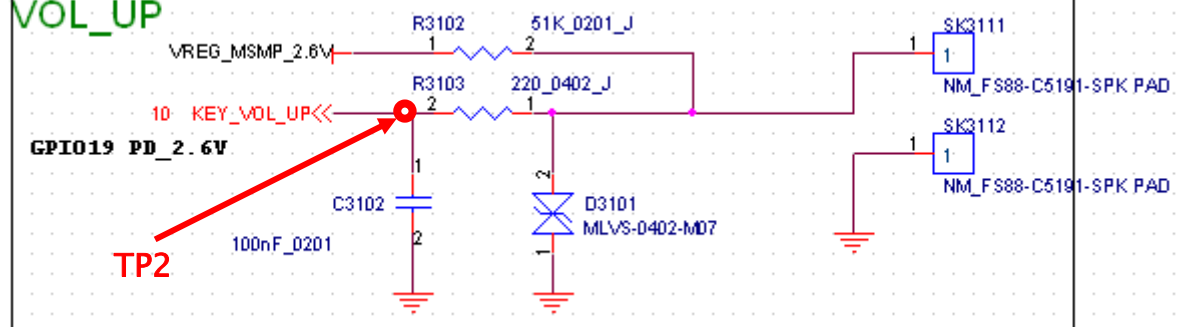
Circuit Diagram

Main board

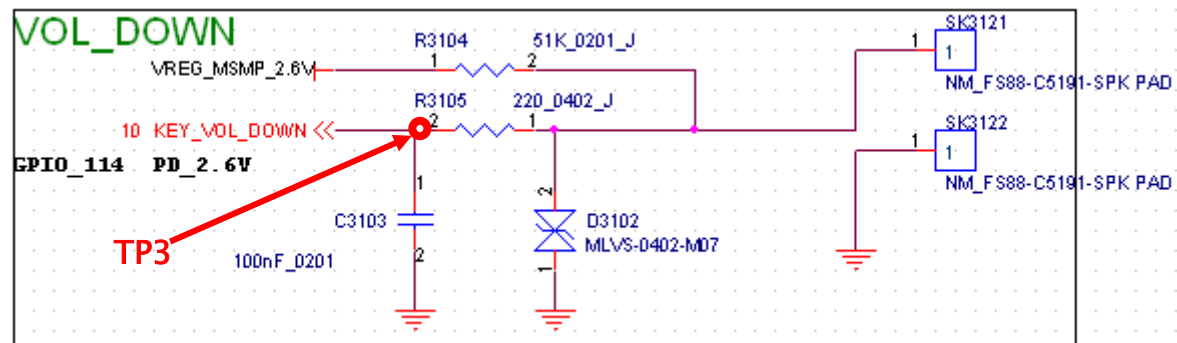
Function key



VOL_UP

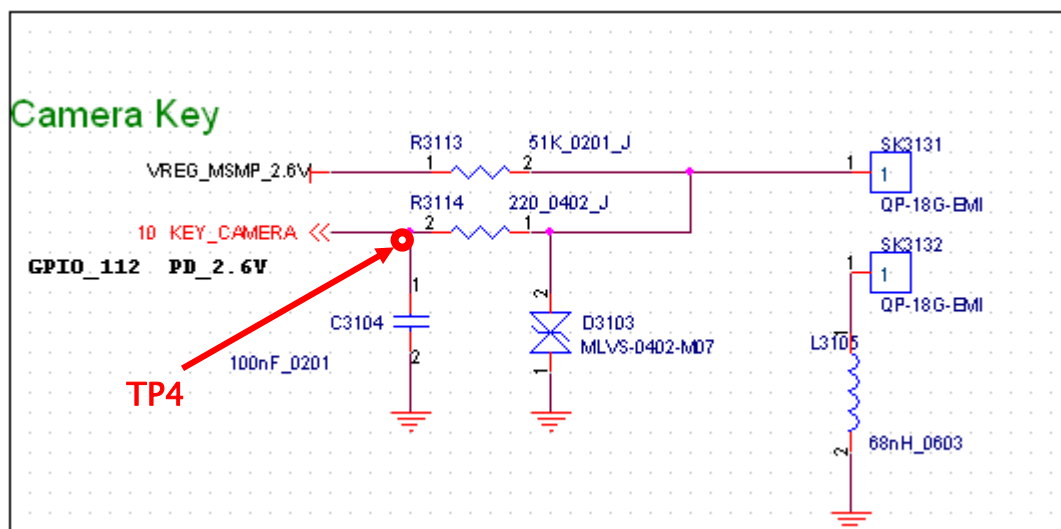


VOL_DOWN



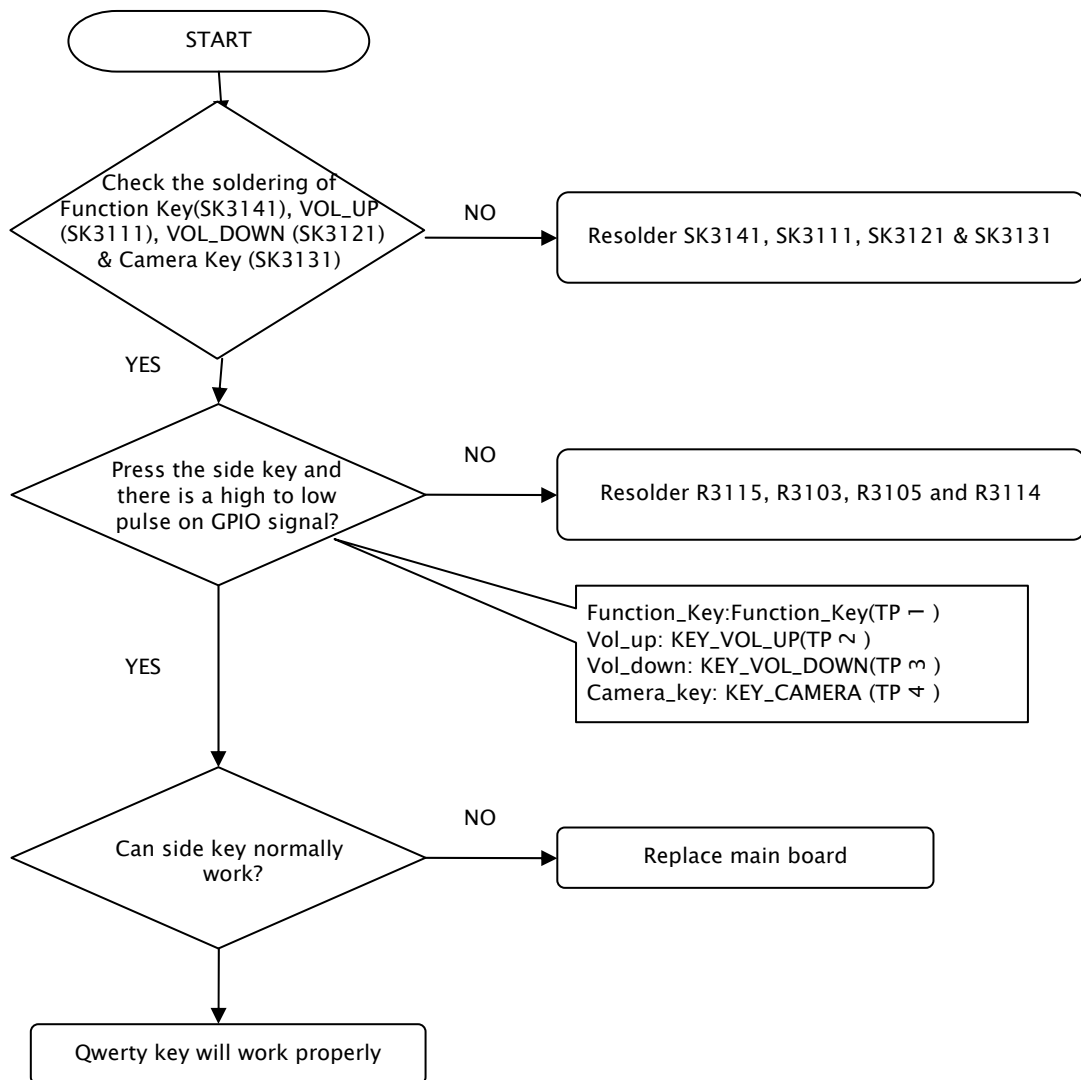
Circuit Diagram

Main board



TROUBLE SHOOTING

Checking Flow

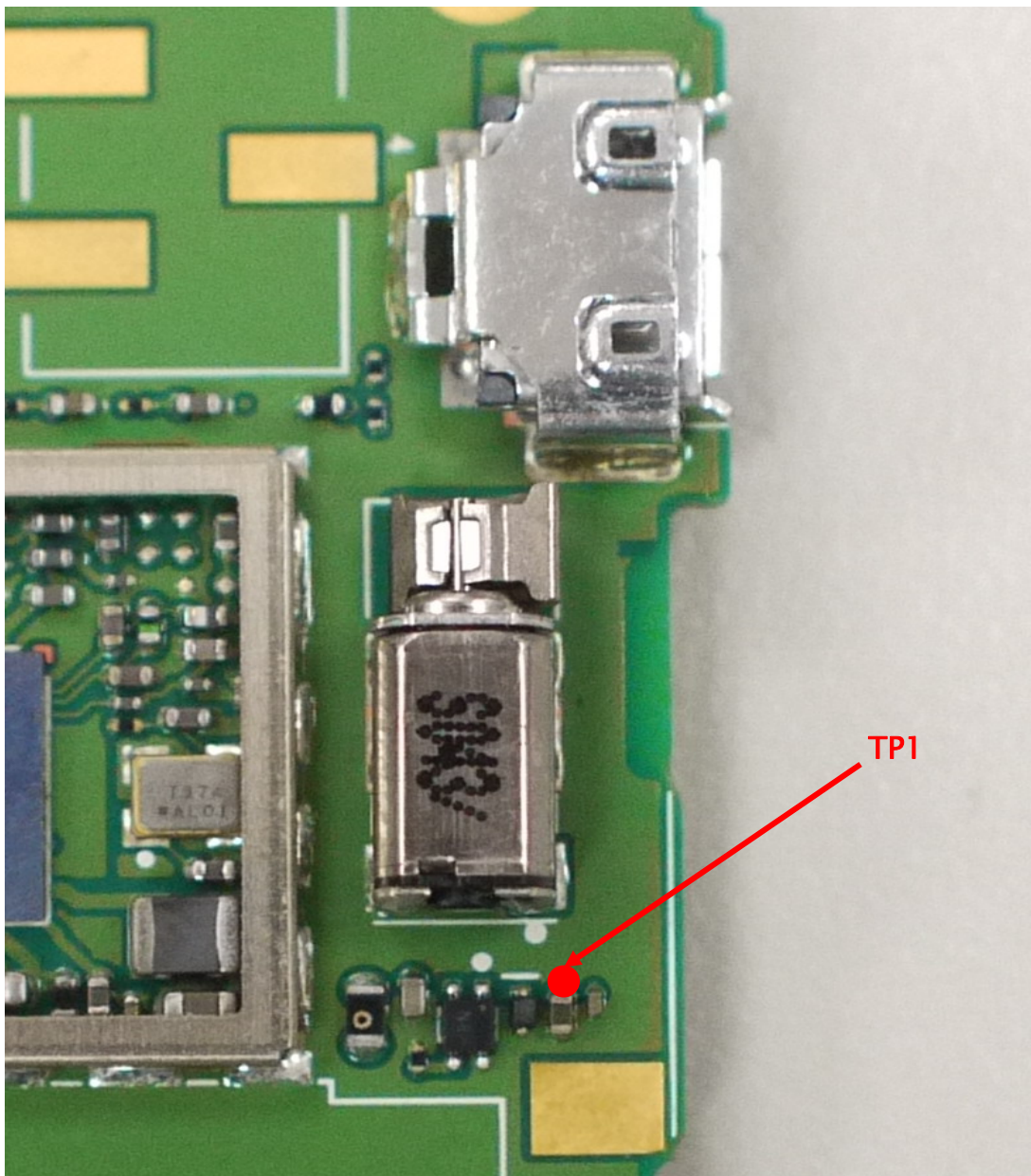


TROUBLE SHOOTING

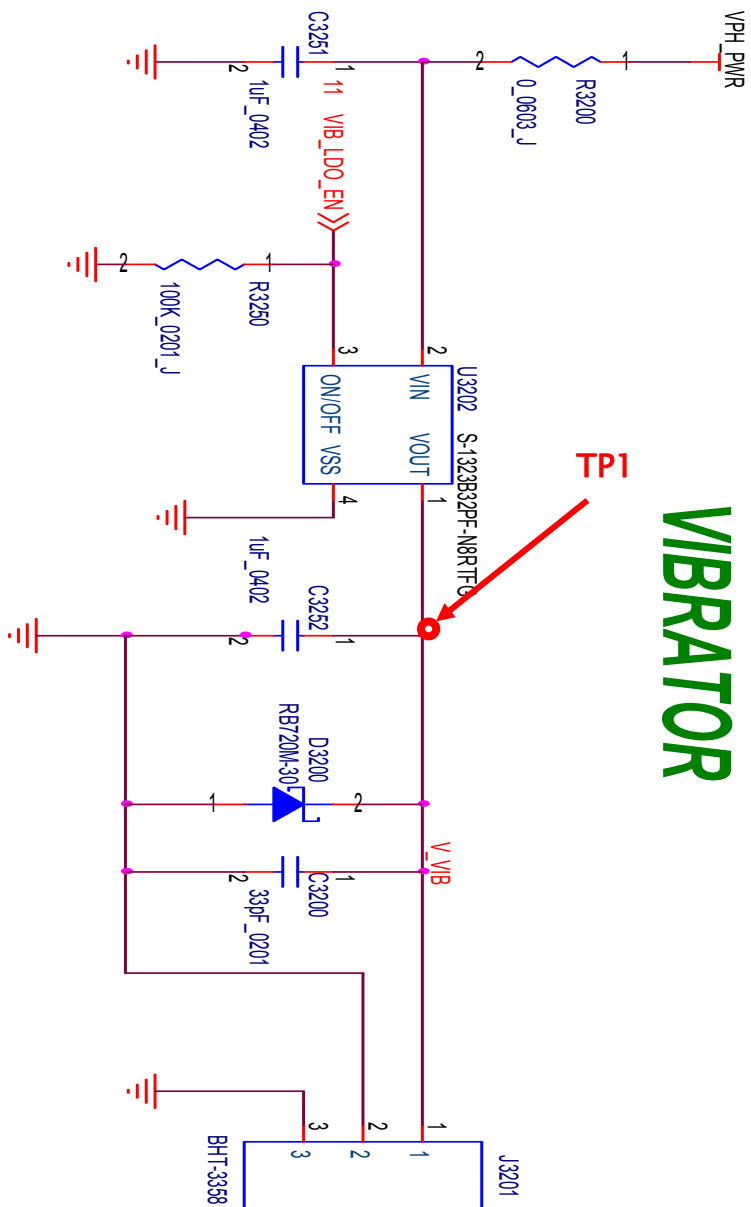
4.22 Vibrator Trouble

Picture Data

Main board bottom



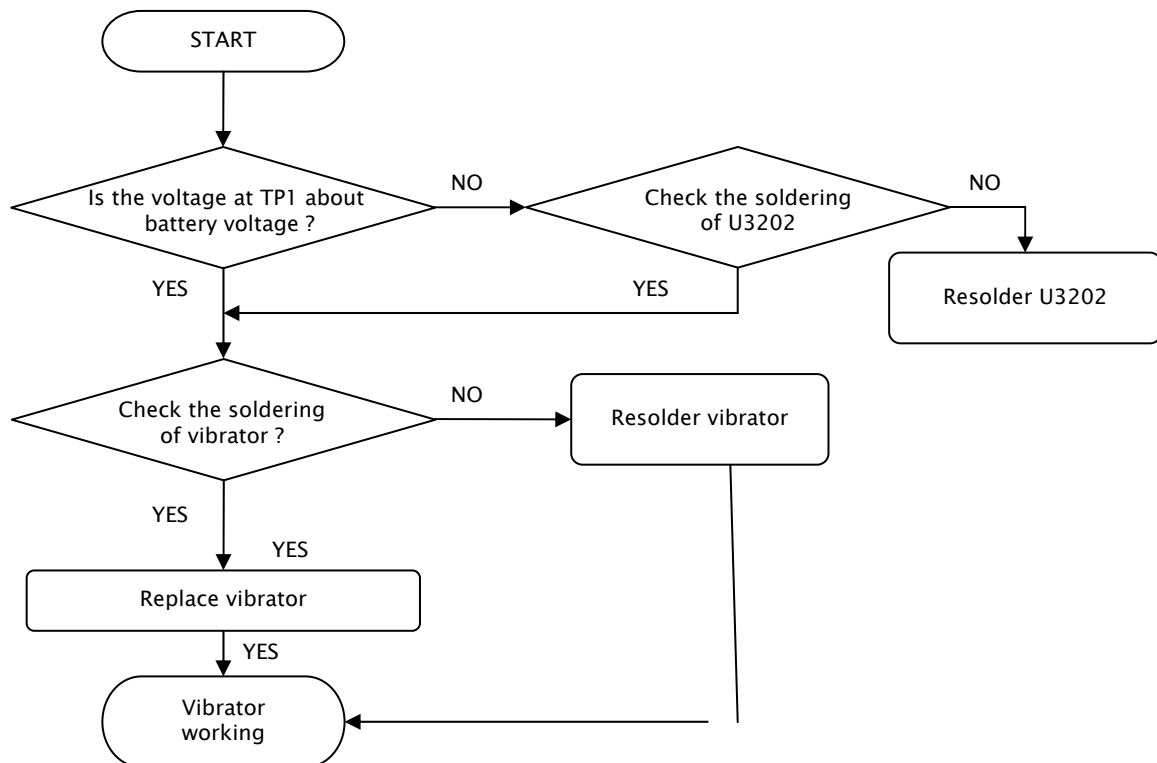
Circuit Diagram



TROUBLE SHOOTING

Checking Flow

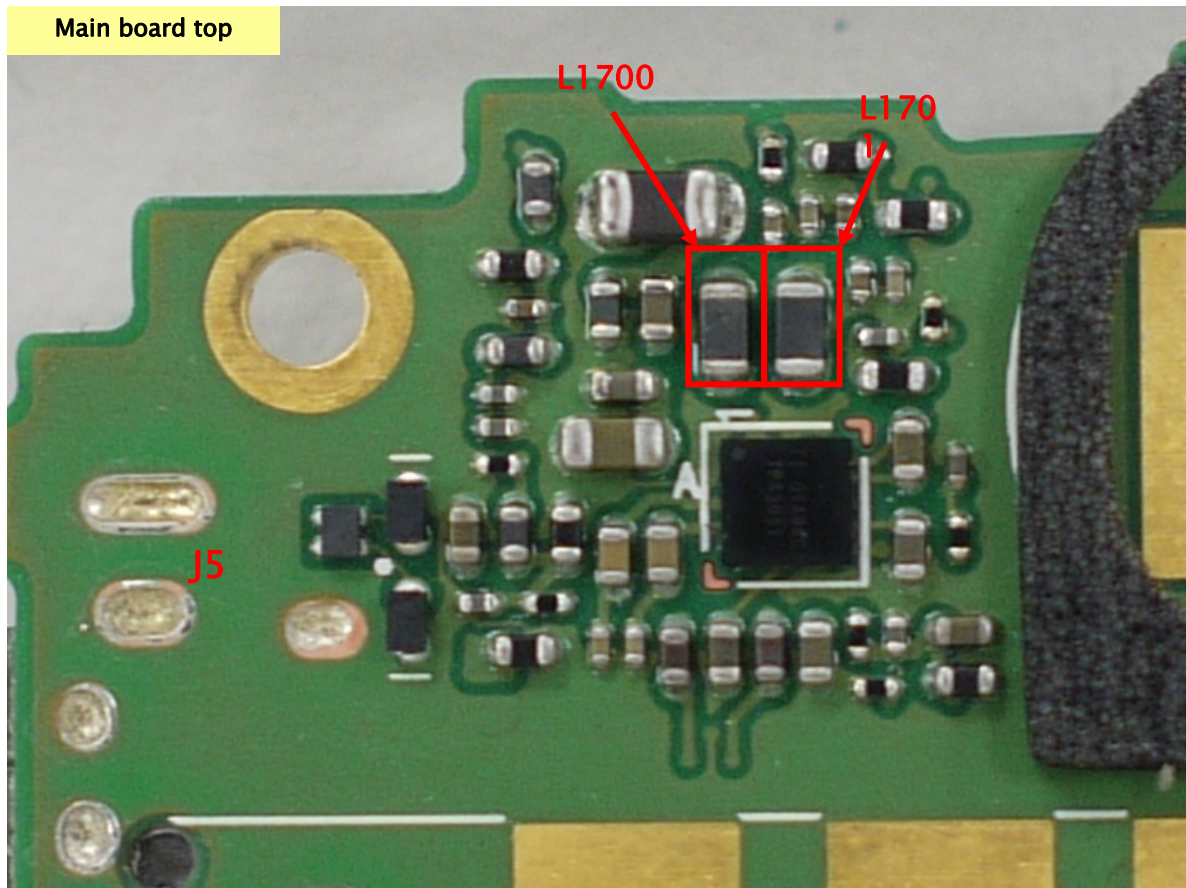
Setting : Enter the engineering mode, and set vibrator on at vibration of BB test menu



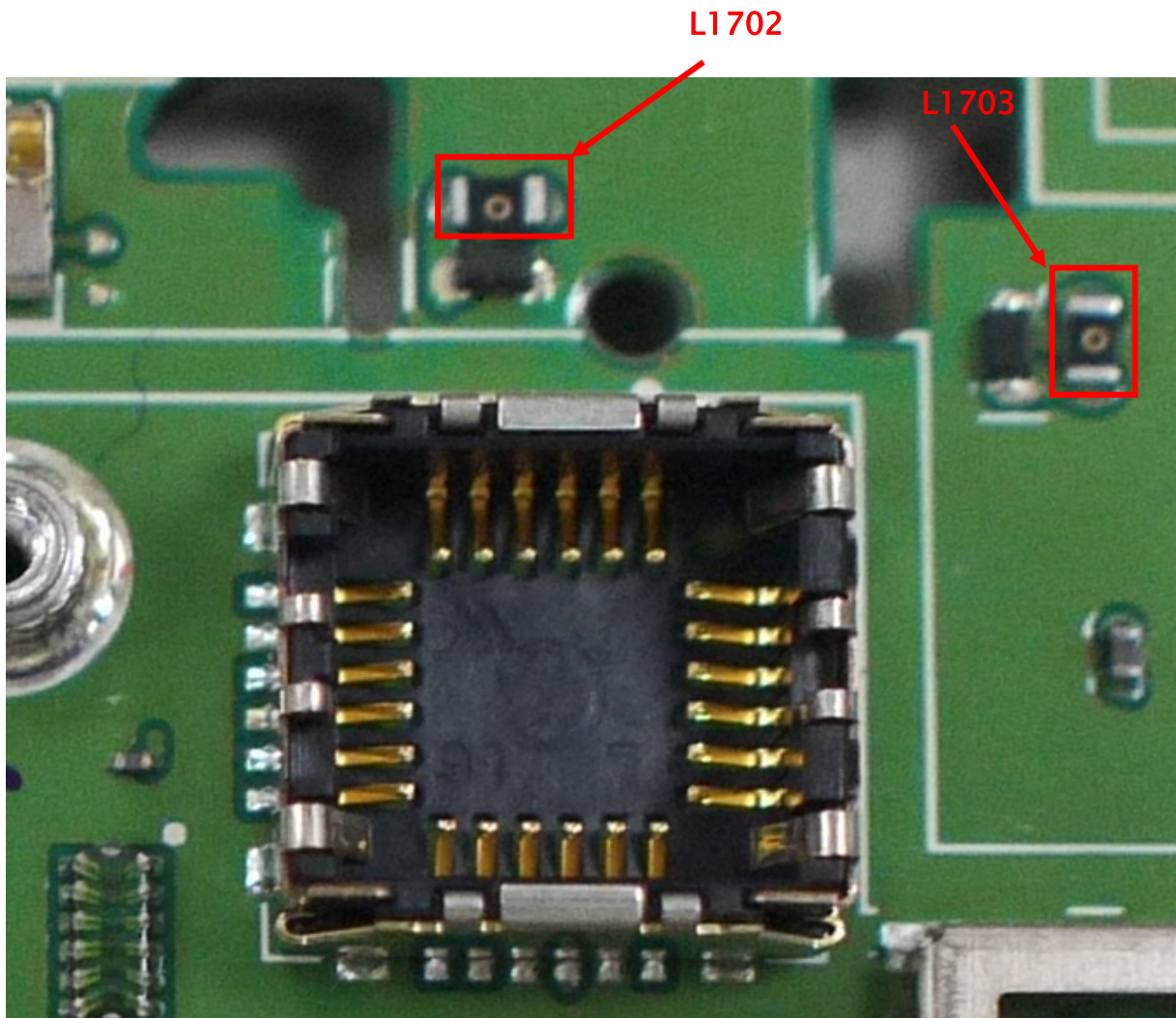
TROUBLE SHOOTING

4.23 Receiver Trouble

Picture Data



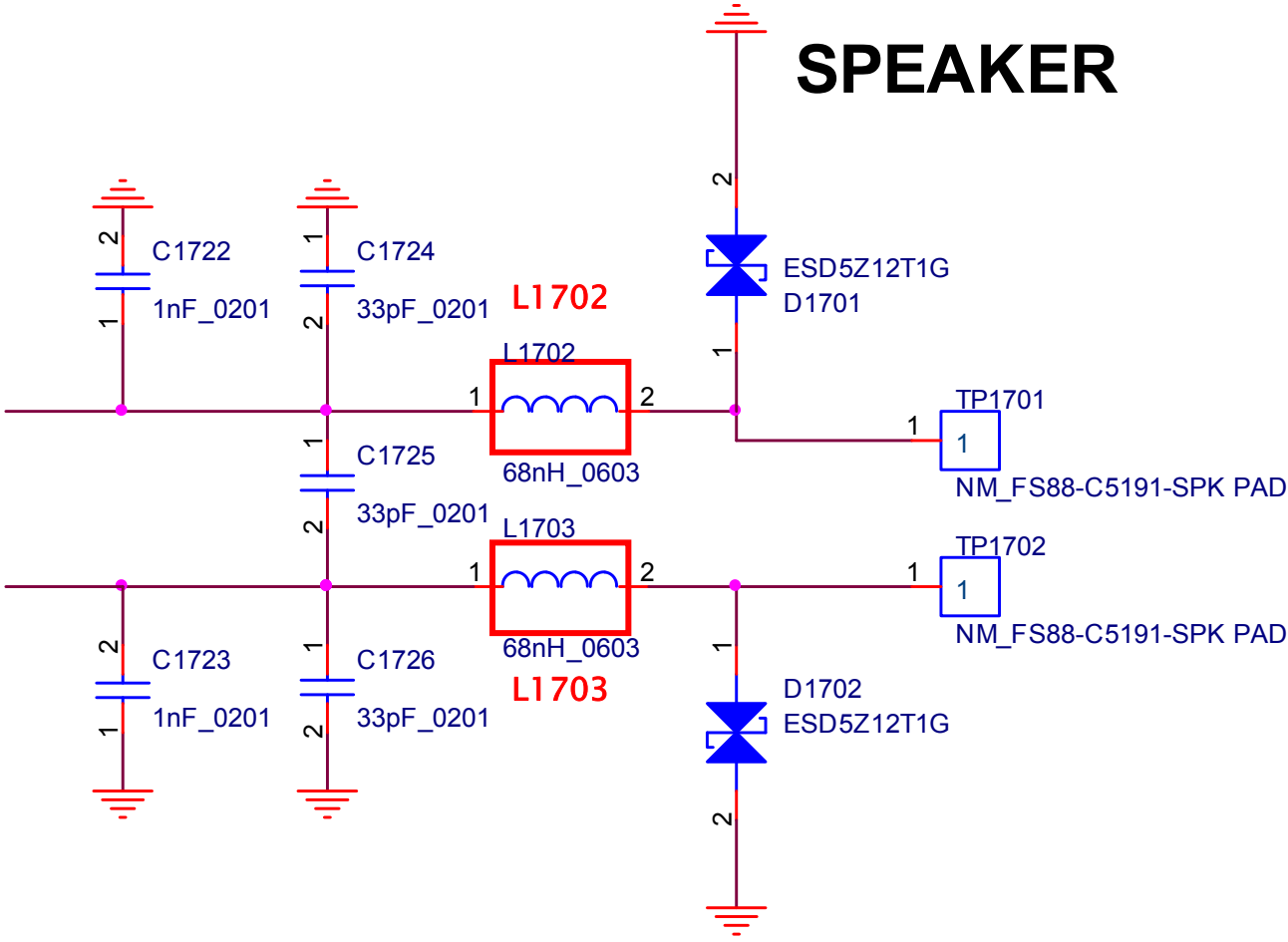
Main board bottom




```
I2C Address: 0xE1 (Reading)
0xE0 (Writing)
```



Main board

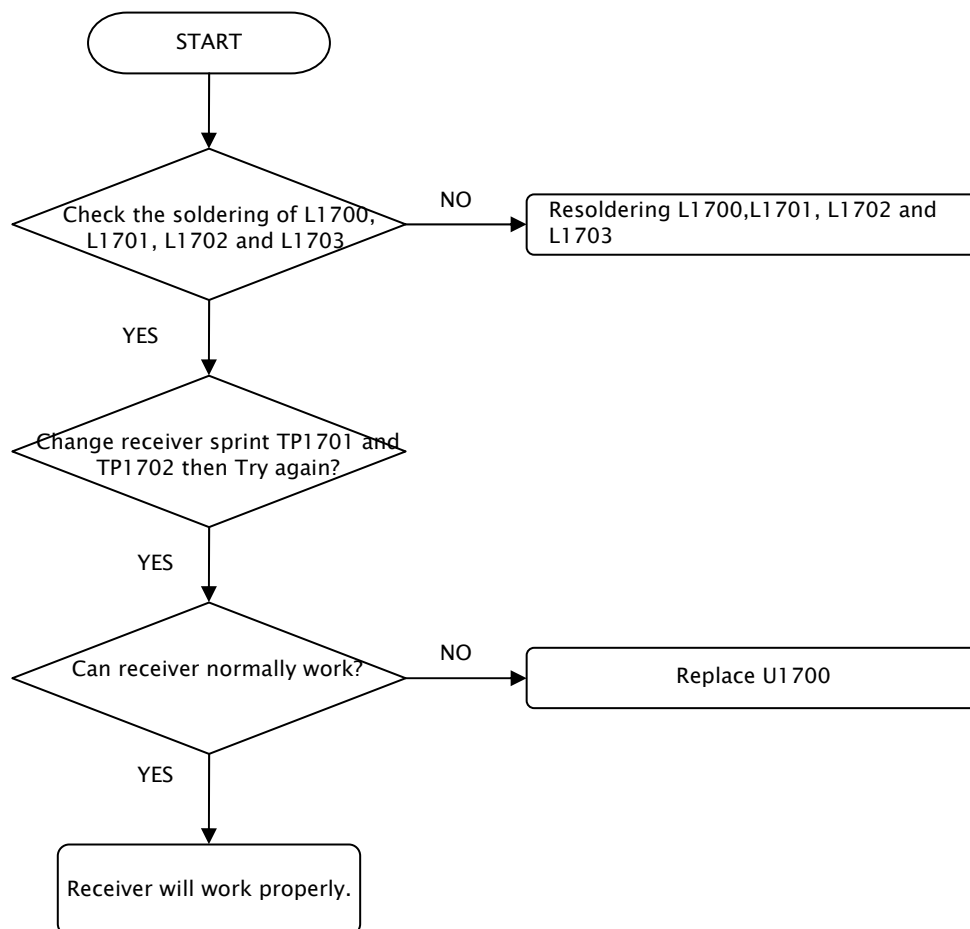


TROUBLE SHOOTING

Checking Flow

SETTING : After initialize Agilent 8960, Test EGSM, DCS mode

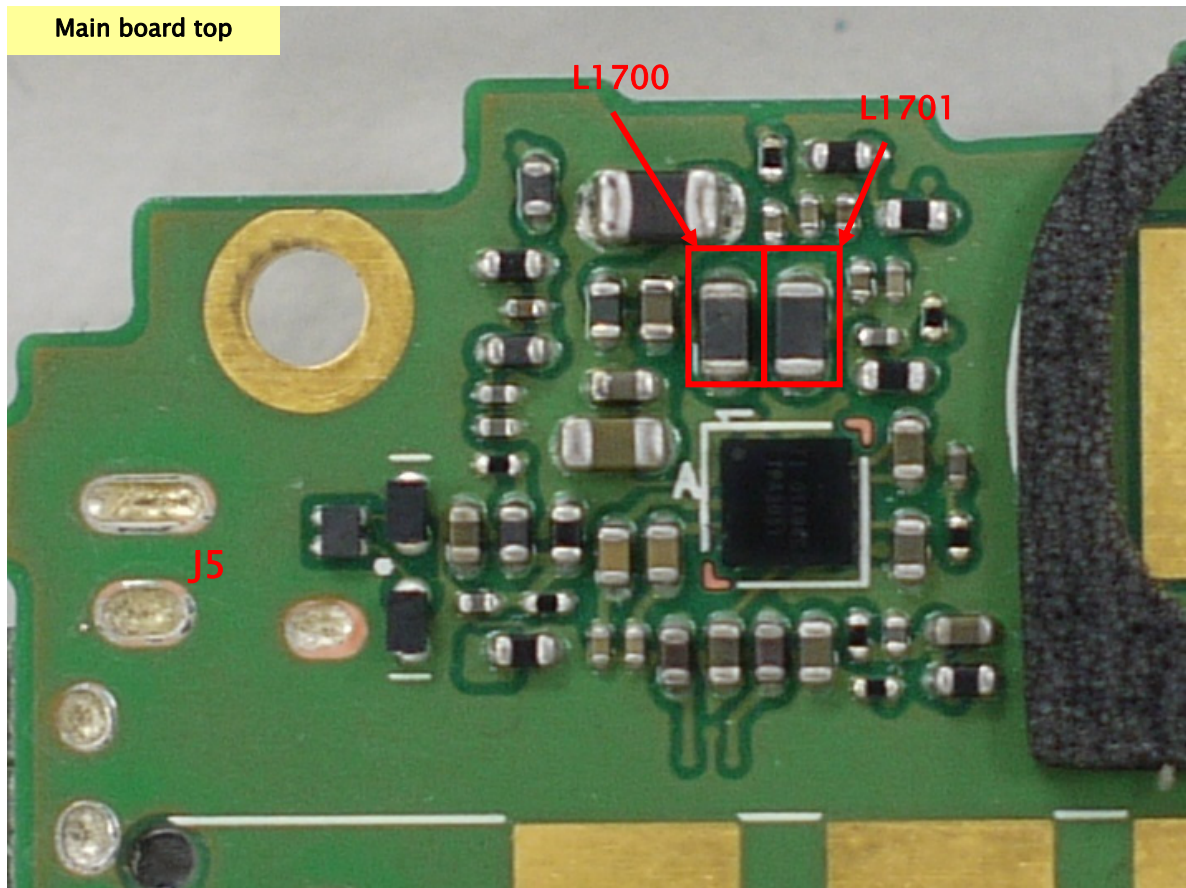
Set the property of audio as PRBS or continuous wave. Set the receiving volume of mobile as Max.



TROUBLE SHOOTING

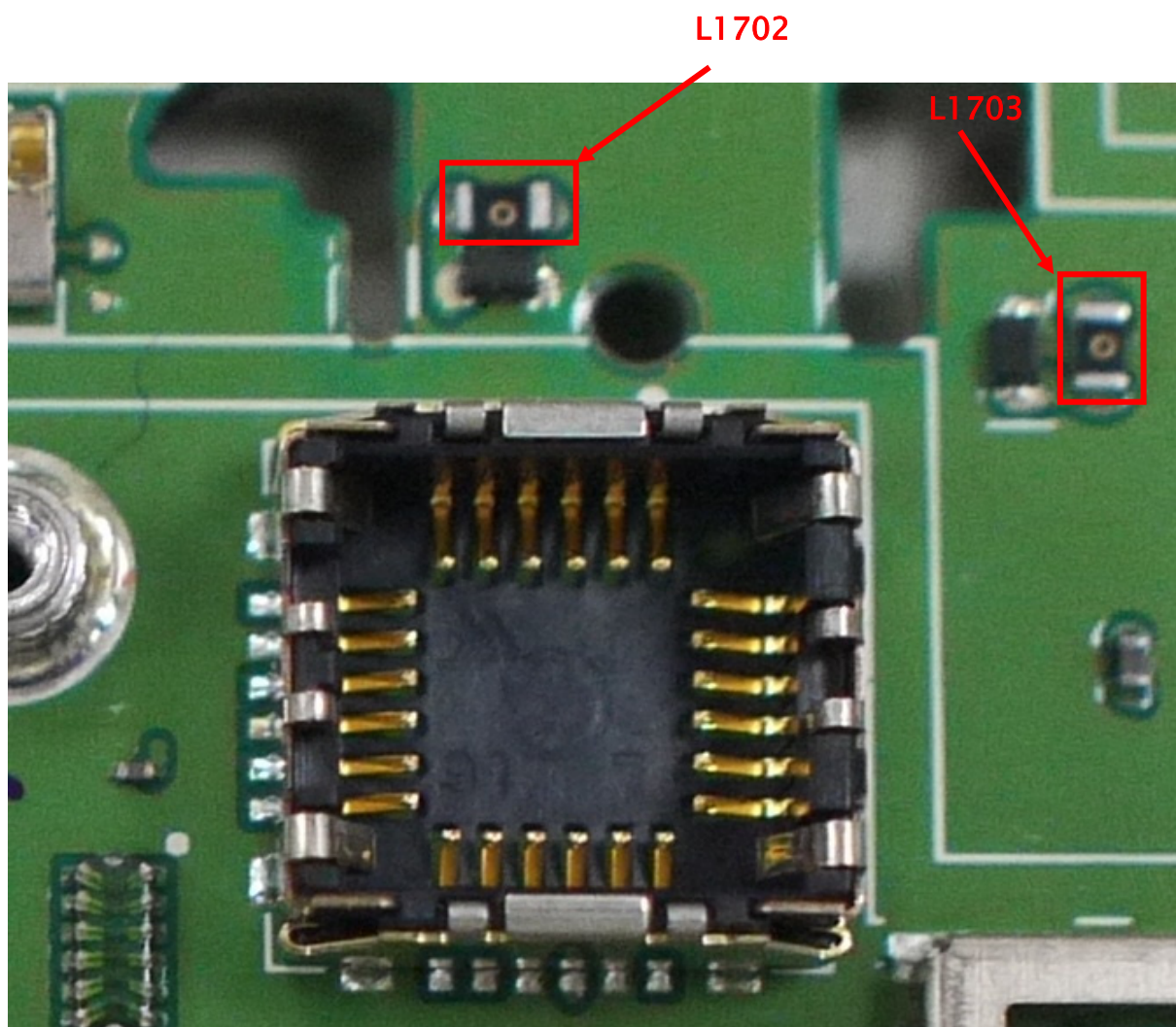
4.24 Speaker Trouble

Picture Data



TROUBLE SHOOTING

Main board bottom



TROUBLE SHOOTING

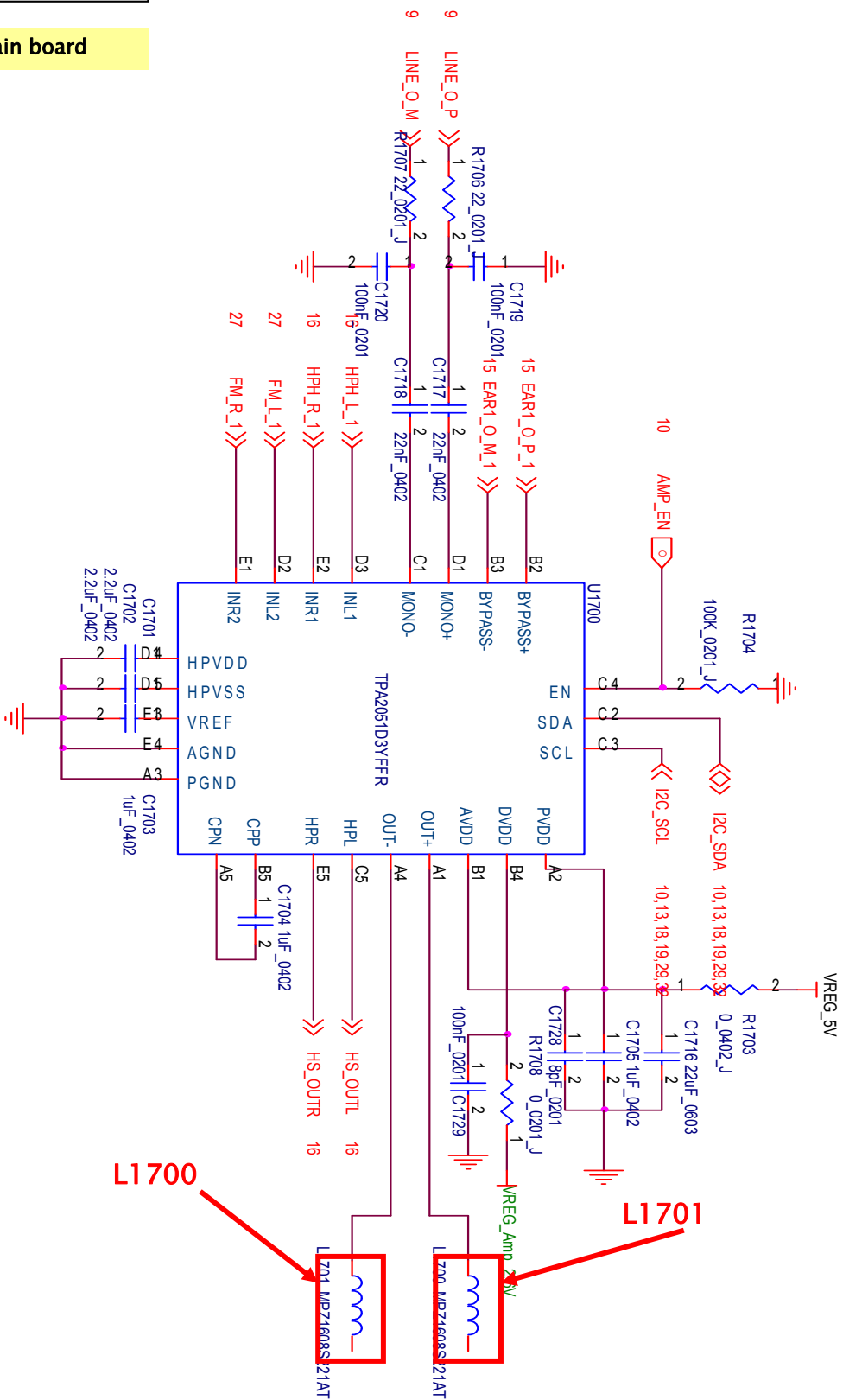
Circuit Diagram

Main board

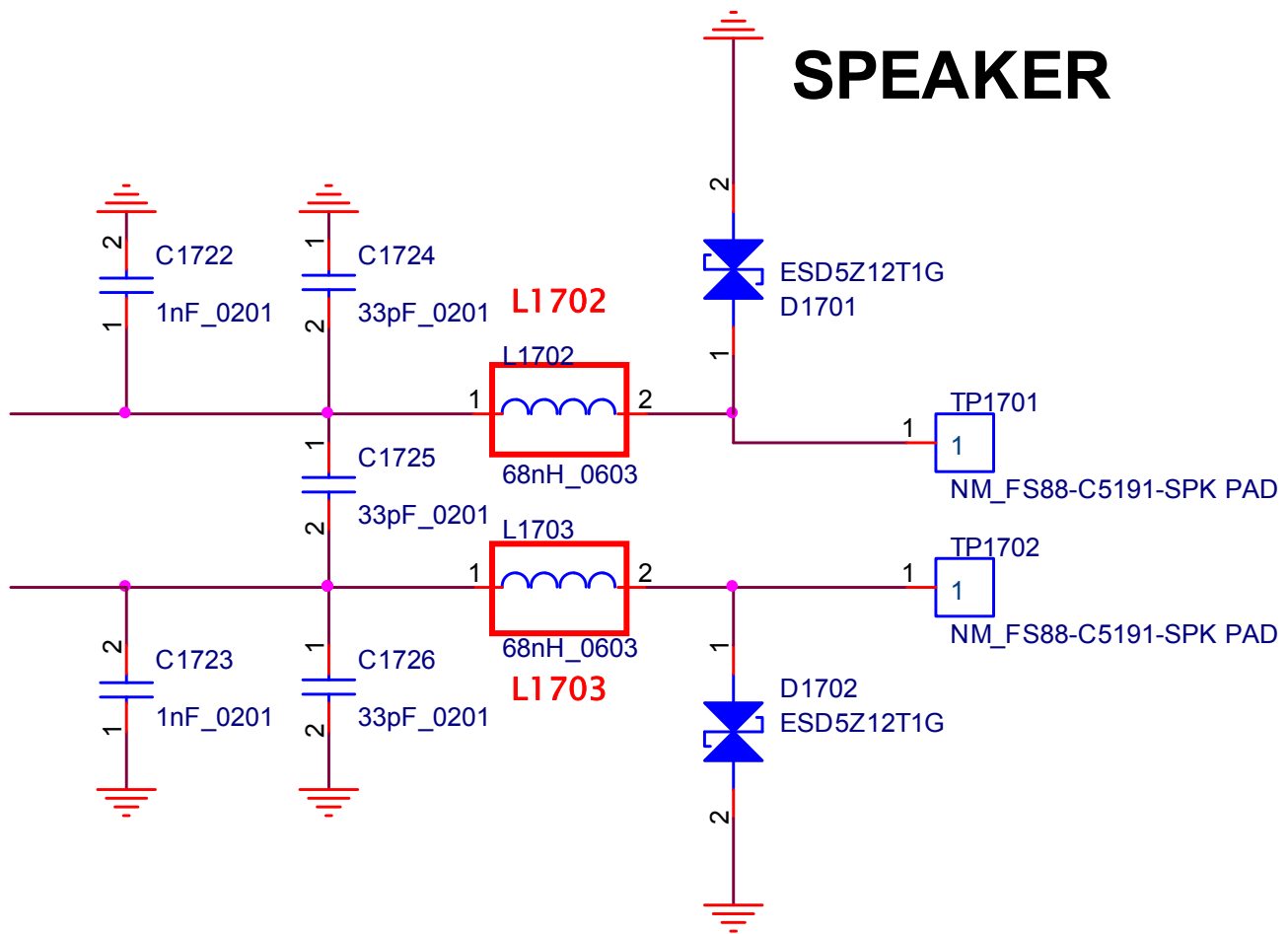
Speaker & Headphone Amp

I2C Address: 0xE1 (Reading)

0xE0 (Writing)

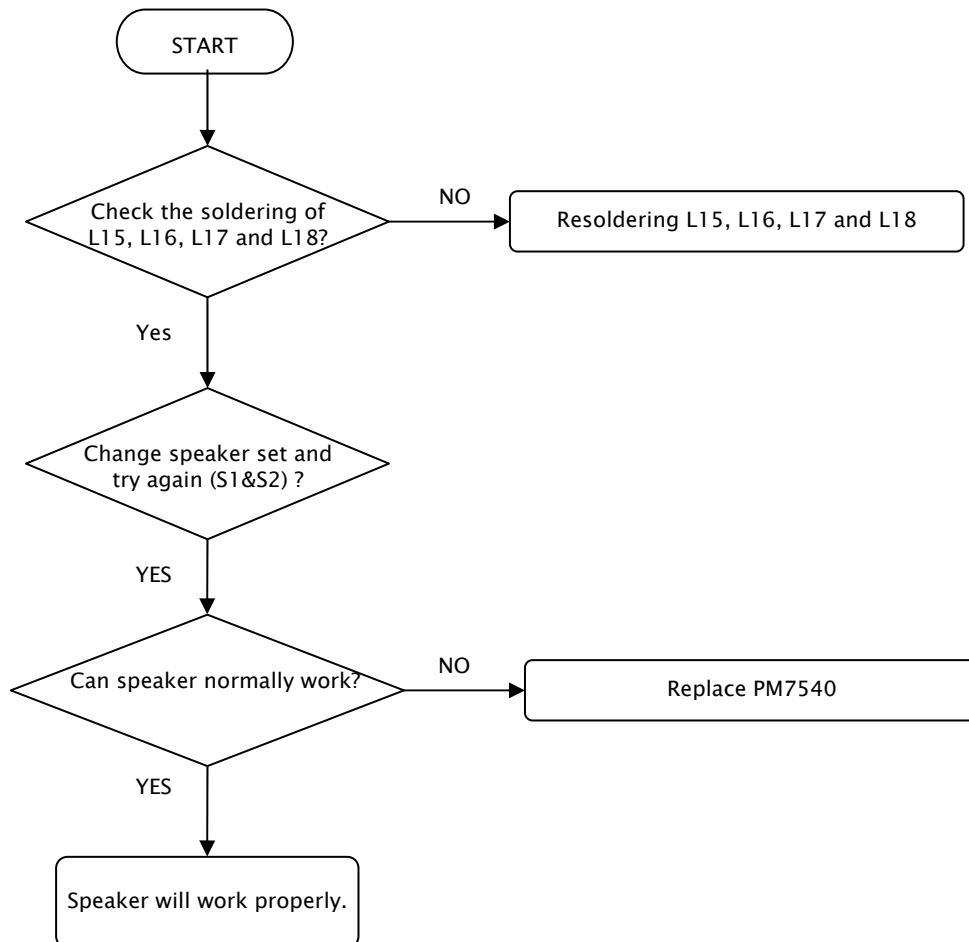


TROUBLE SHOOTING



TROUBLE SHOOTING

Checking Flow

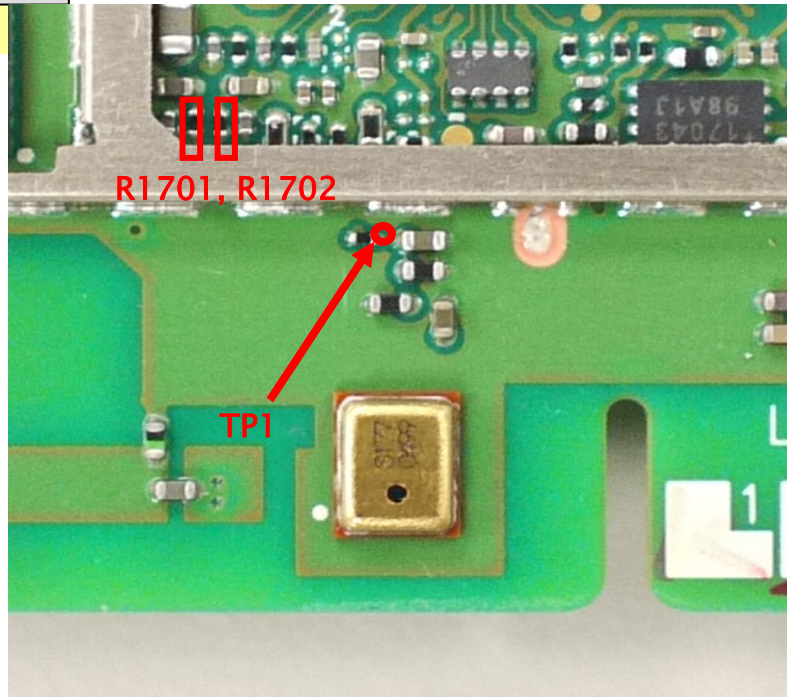


TROUBLE SHOOTING

4.25 Microphone Trouble

Picture Data

Main board top



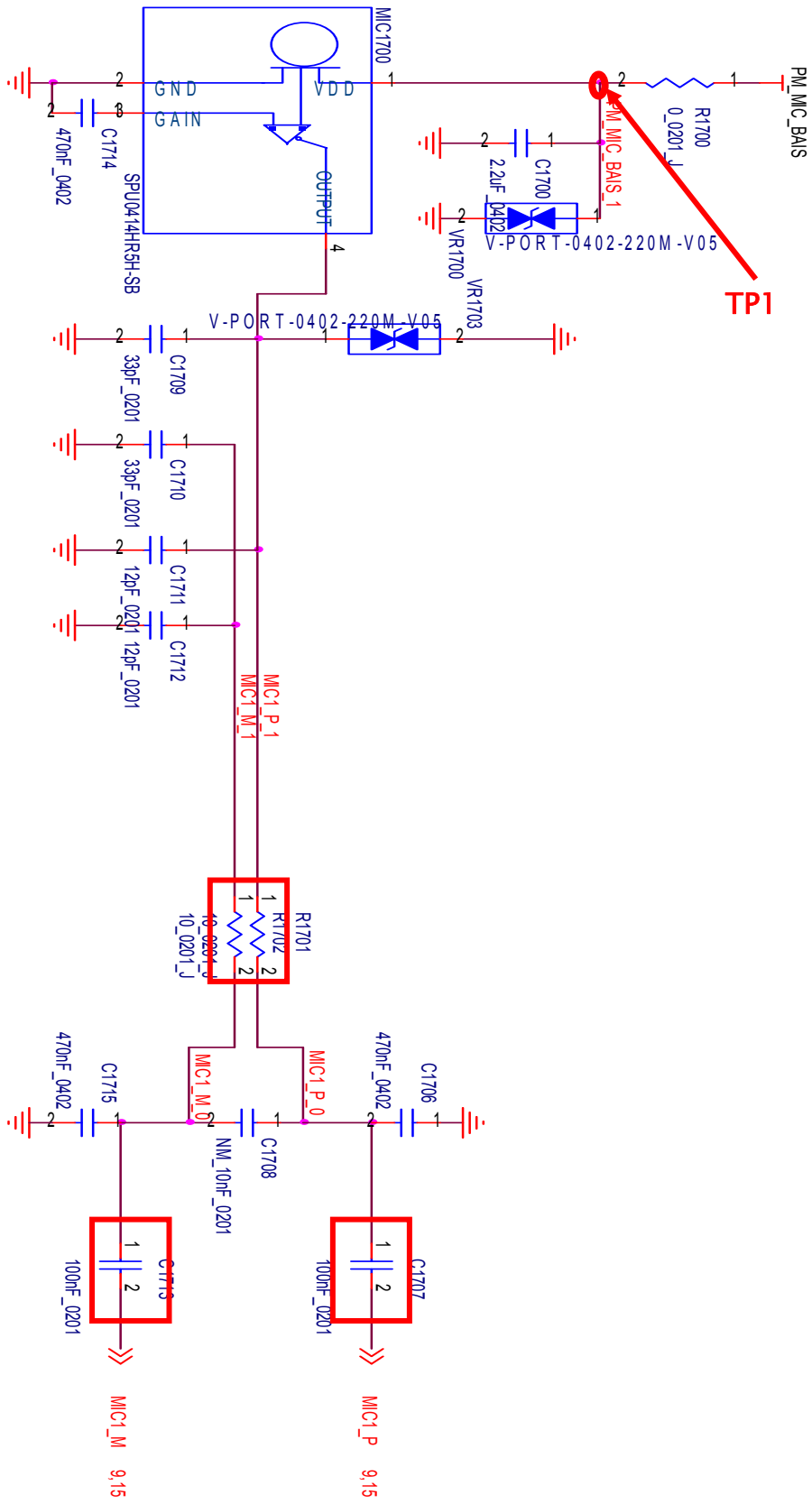
Main board top



TROUBLE SHOOTING

Main board bottom

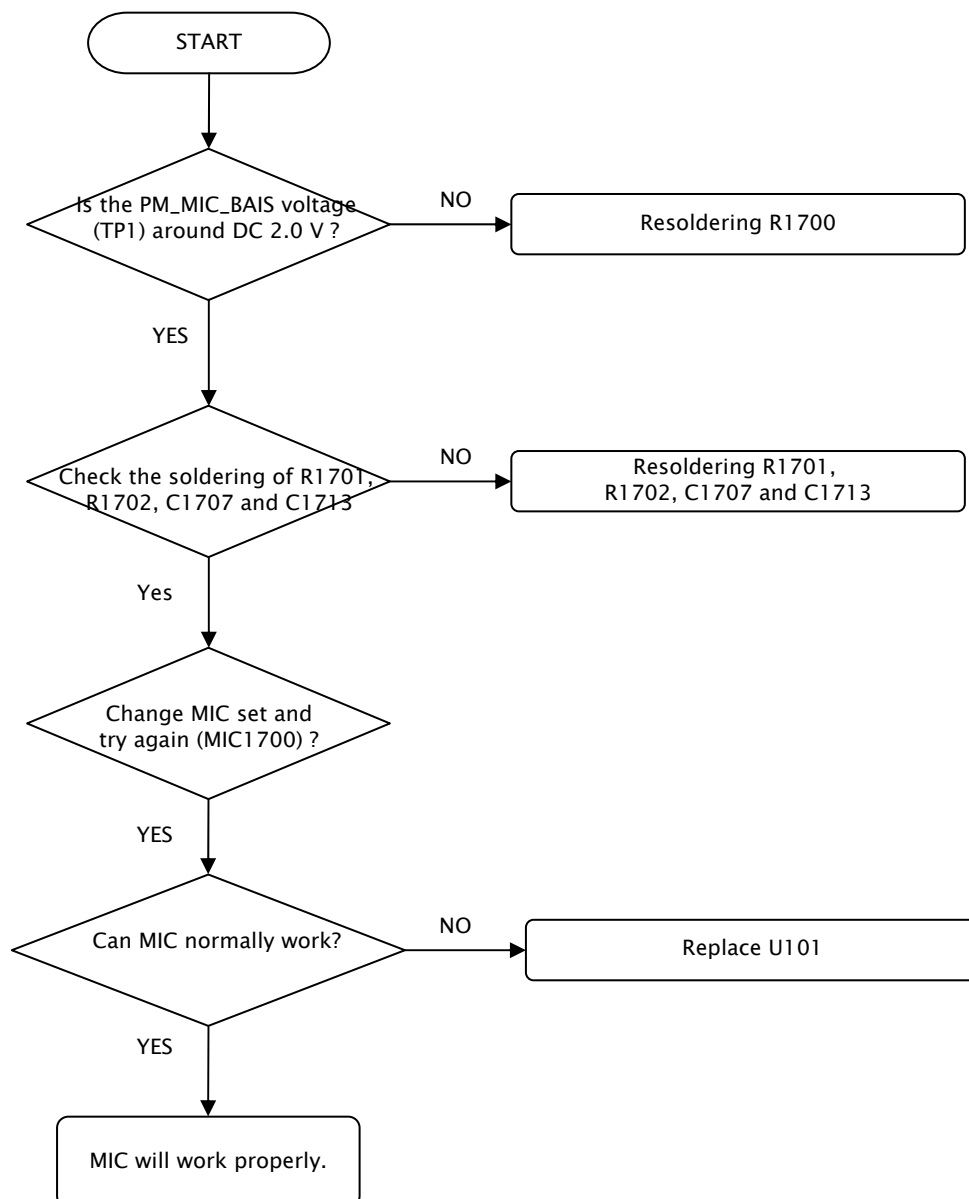
MICROPHONE



TROUBLE SHOOTING

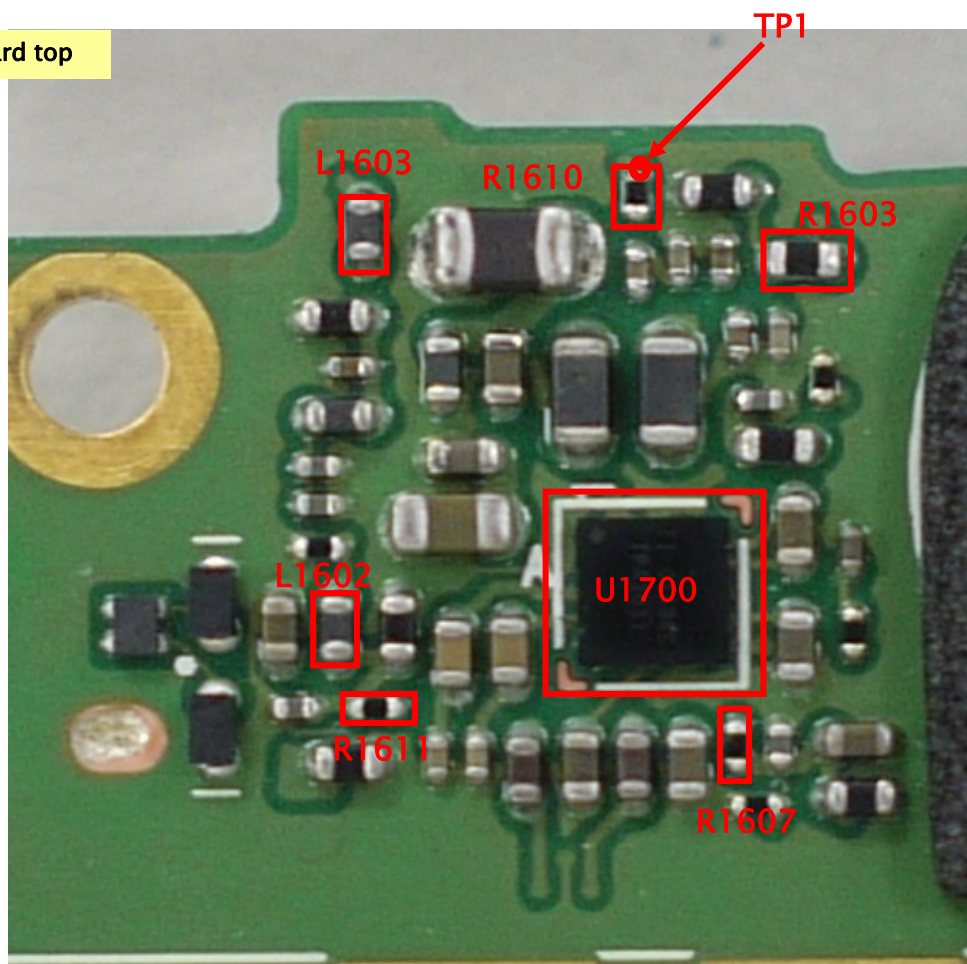
Checking Flow

SETTING : After initialize Agilent 8960, Test EGSM, DCS mode

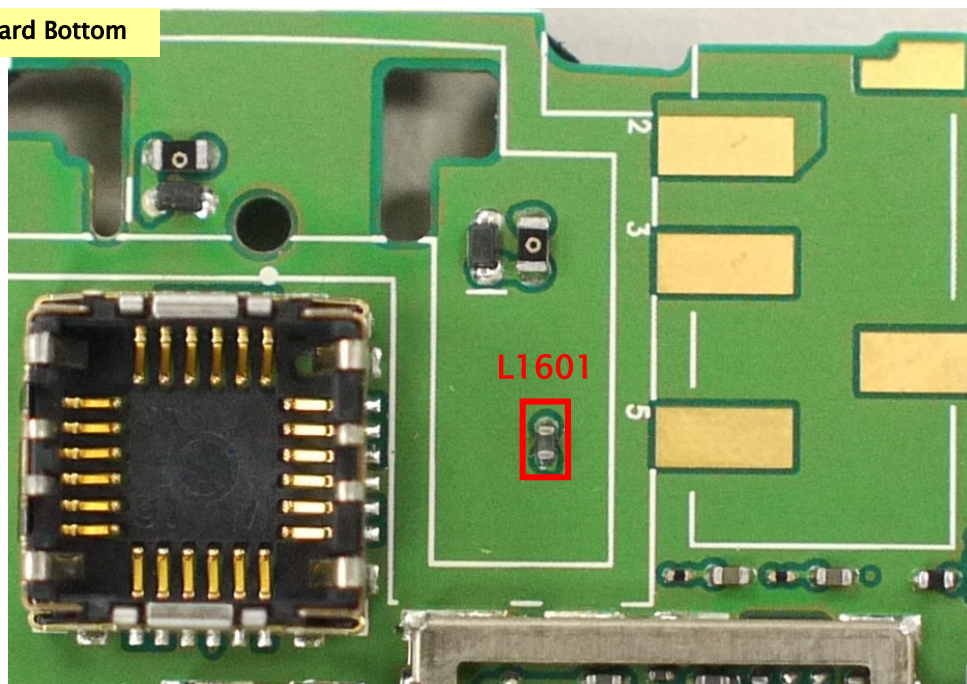


TROUBLE SHOOTING

Main board top

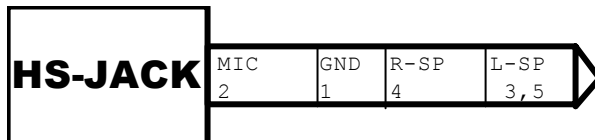
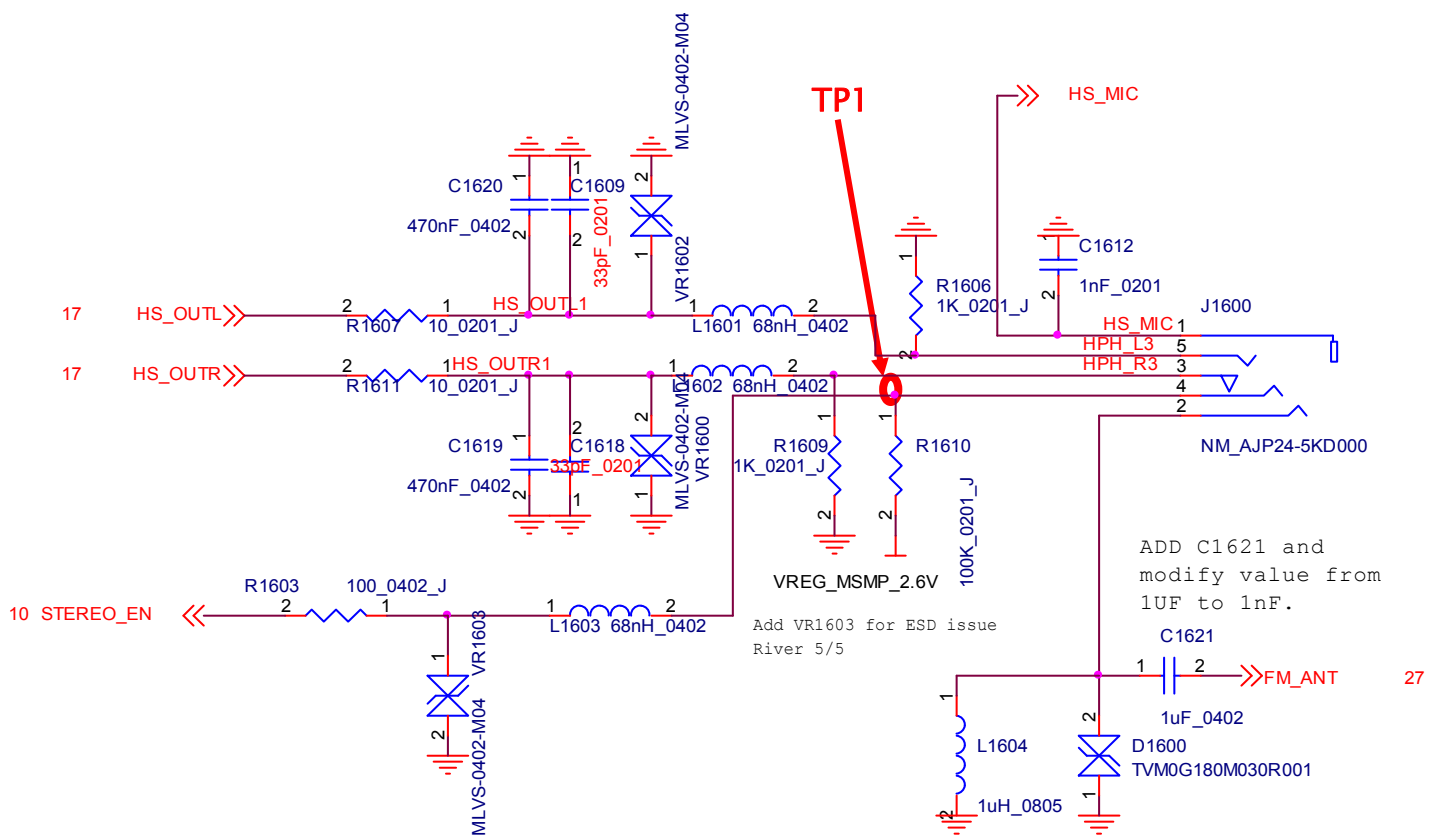


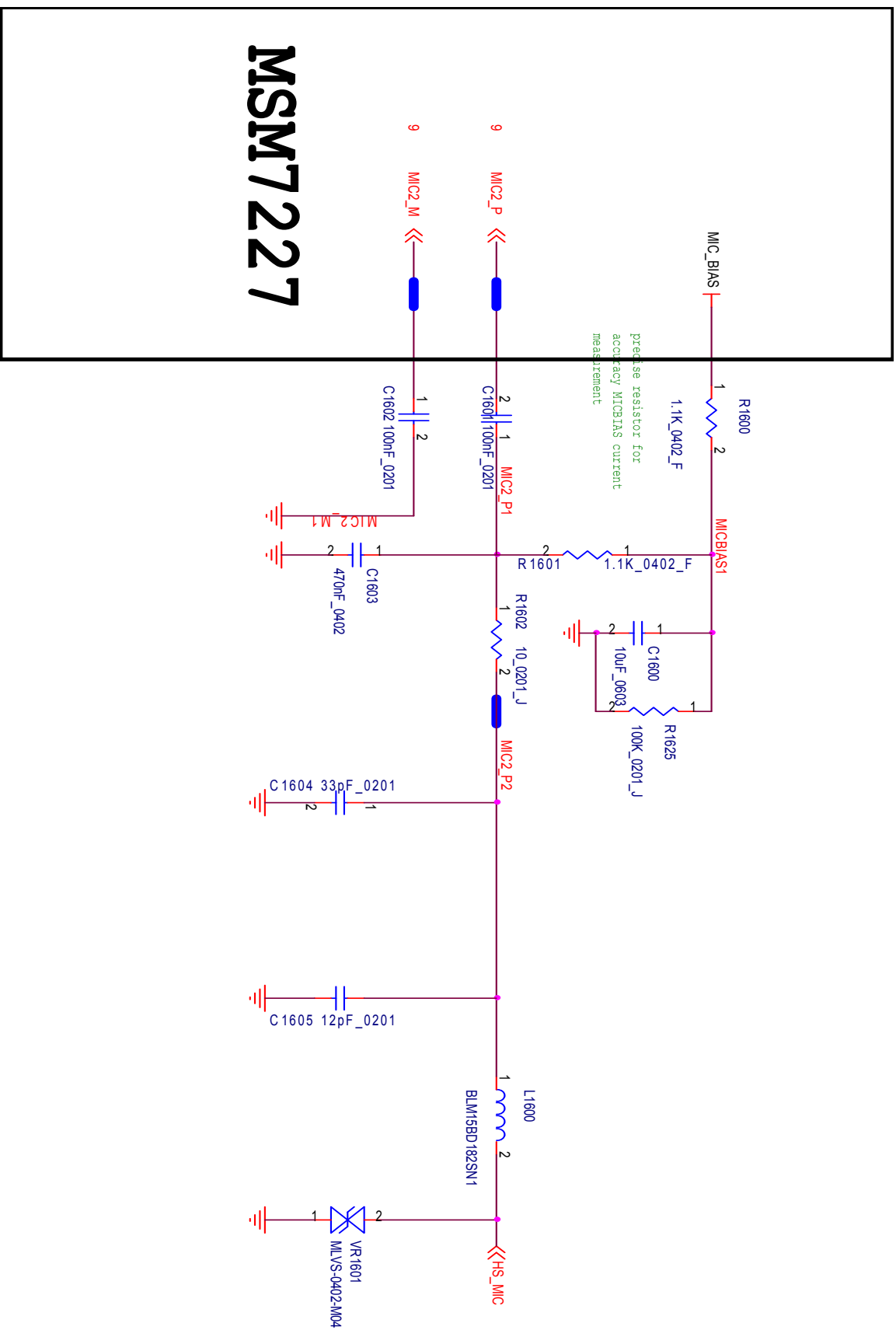
Main board Bottom



TROUBLE SHOOTING

Main board bottom

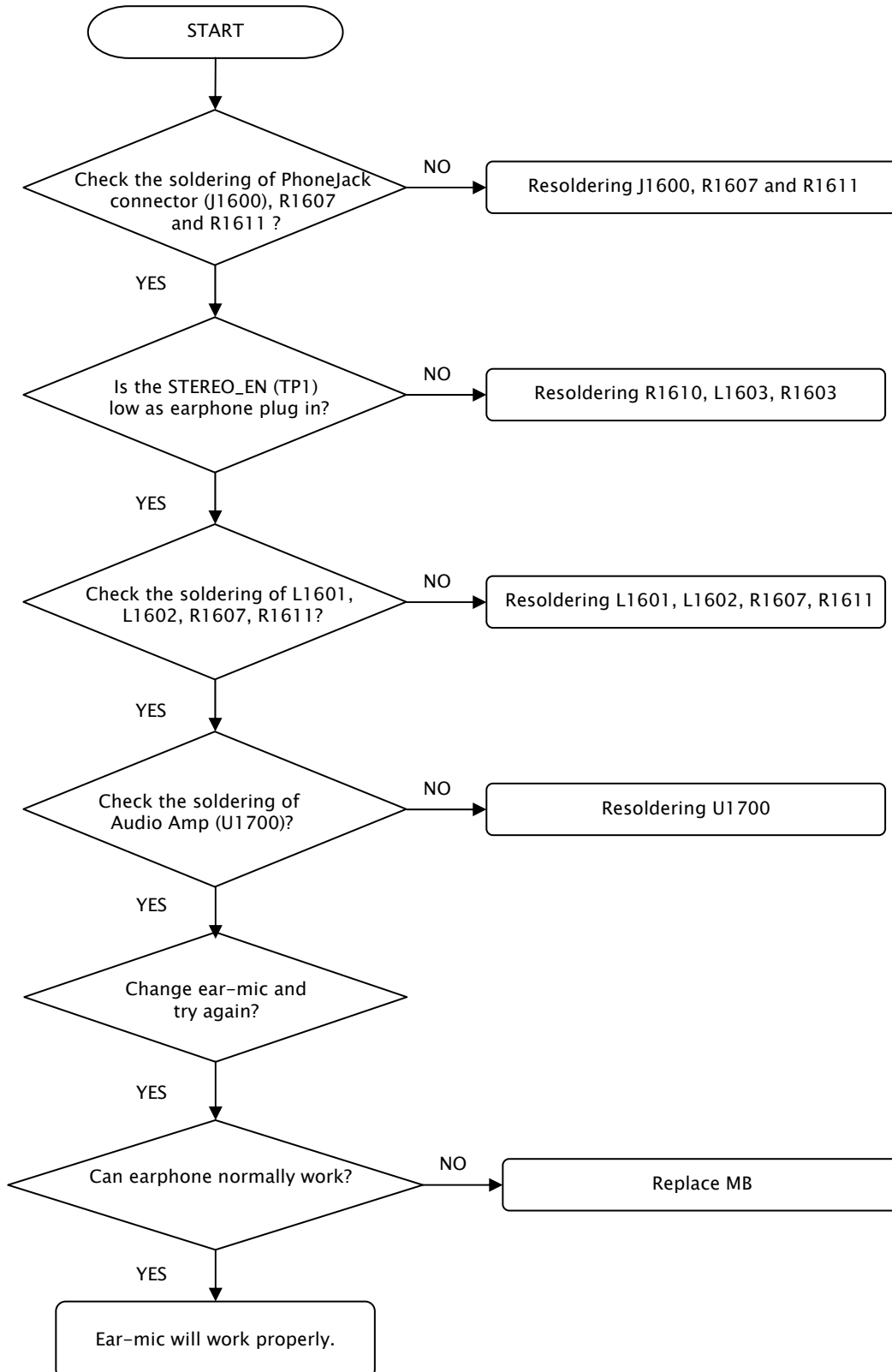




TROUBLE SHOOTING

Checking Flow

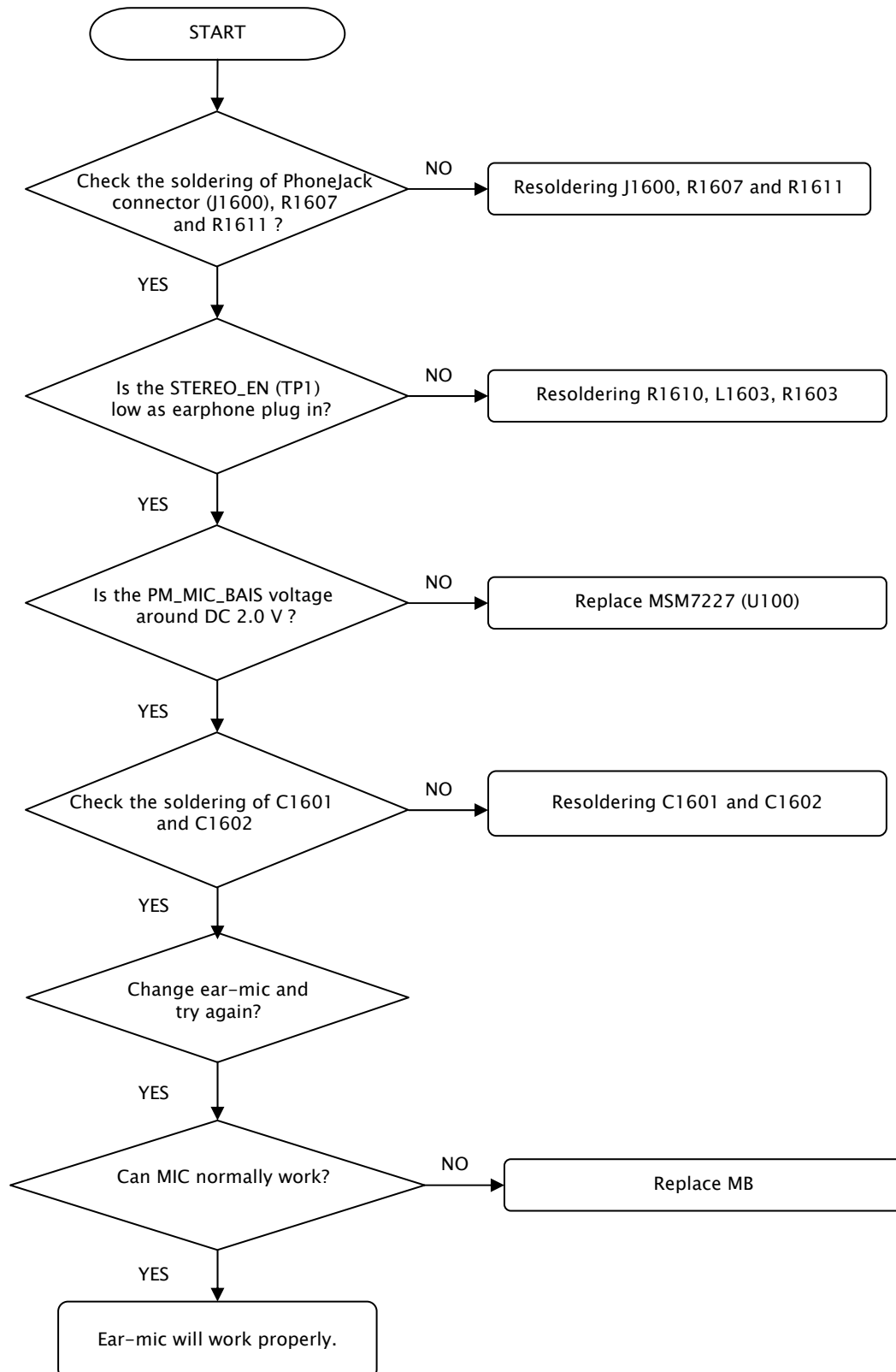
4.26 Earphone of ear-mic trouble



TROUBLE SHOOTING

Checking Flow

4.26 MIC of ear-mic trouble



5. DISASSEMBLY INSTRUCTION

5.1 Disassembly



Disassembly Tools — —
Screw Driver, Tweezers, PC
Sheet and Camera Jig
(PC Sheet — Thickness
0.5mm)



(Ensure the phone is turn
off)
Press the battery cover
hook and slide it away from
rear housing



Remove battery cover in the
direction show left



Remove battery in the
direction shown left



(Optional) Gently remove SIM card in the direction shown left



(Optional) Gently Gently push and pull out T-Flash card



Use Screw Driver to release Top Deco hook on disassembly hole position



Remove Top Deco



Separate Top Deco completely



Unfasten top side two screws shown as left



Unfasten back side four screws shown as left



Use PC Sheet to release the hooks around Main Lens



Release the hooks in the direction shown as left to pull off rear case



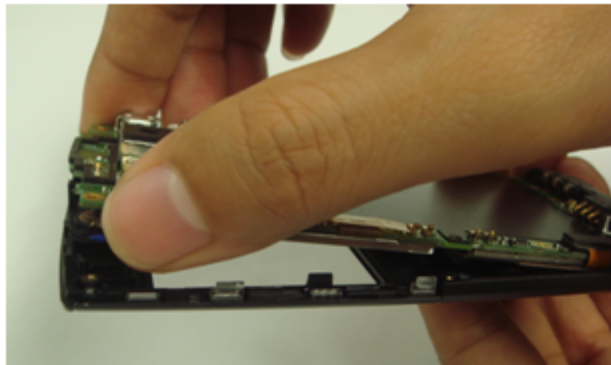
Pull open Rear Case in the direction shown as left



Separate Rear Case completely



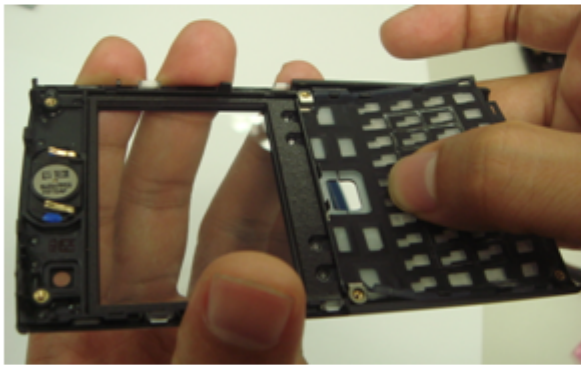
Unfasten two screws shown as left



Uplift PCBA from Front Case



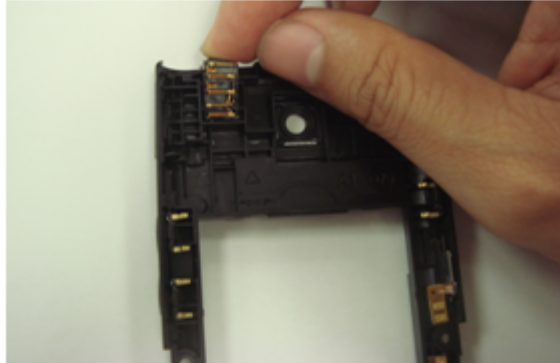
Separate Front Case and PCBA



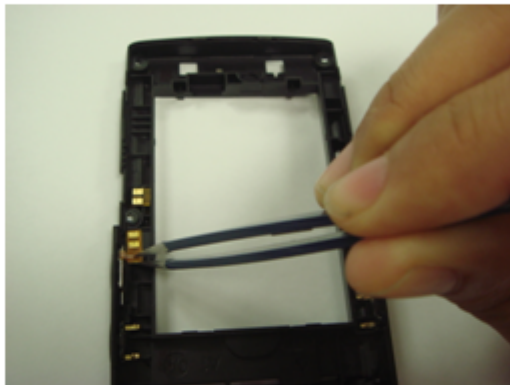
Detach Keypad from Front Case shown as left



Separate Front Case and Keypad



Remove Audio Jack



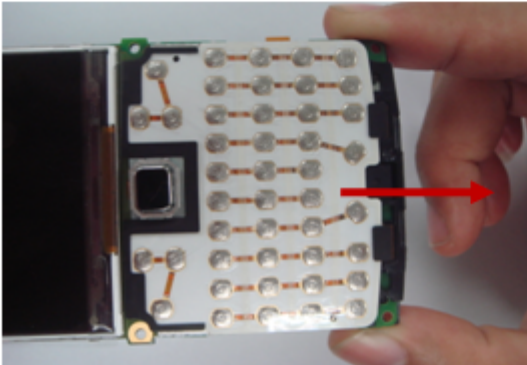
(Optional) Remove Camera
Key FPC



(Optional) Separate Camera
Key FPC



(Optional) Remove Switch

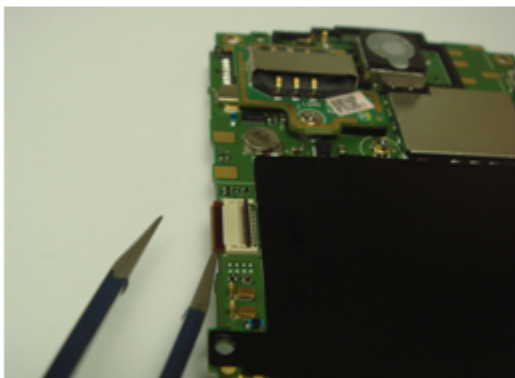
	(Optional) Separate Switch
	(Optional) Remove Camera Key Cap & Volume Key Cap
	(Optional) Separate Camera Key Cap & Volume Key Cap
	Remove Main Antenna Carrier in the direction shown left



(Optional) Pry off Mylar from FPC connector



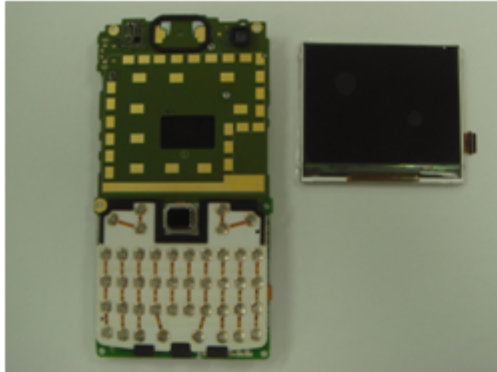
(Optional) Open the latch in the FPC connector



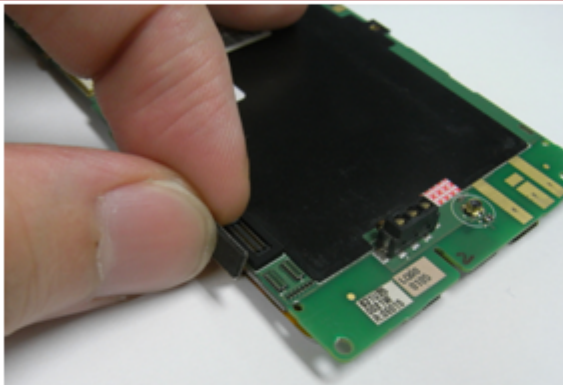
(Optional) Pull out the FPC carefully from the FPC connector



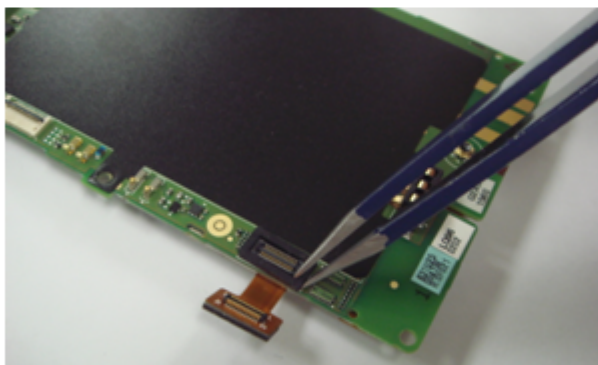
(Optional) Remove LCM Module



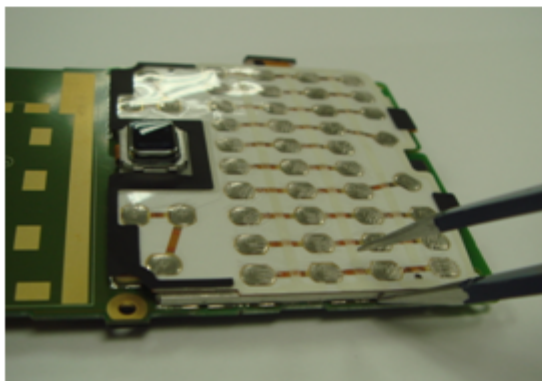
(Optional) Spereate LCM
and PCB board completely



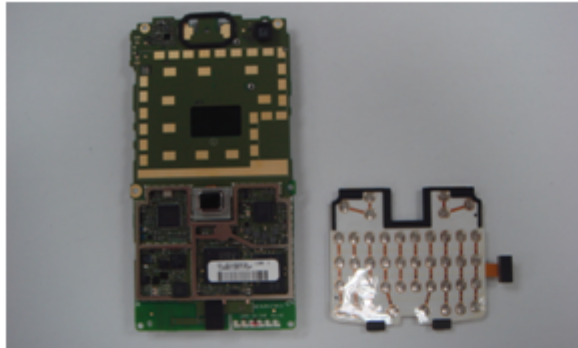
Pry off BTB connector to
remove FPC module



Remove rubber



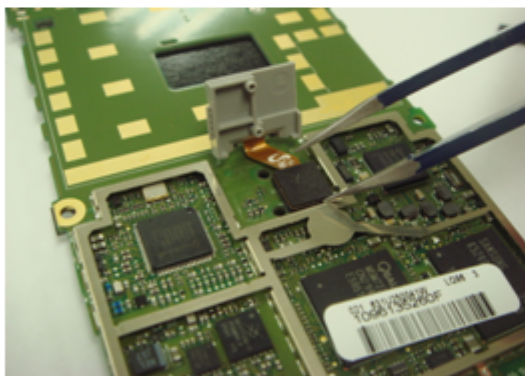
Detach FPC module gently



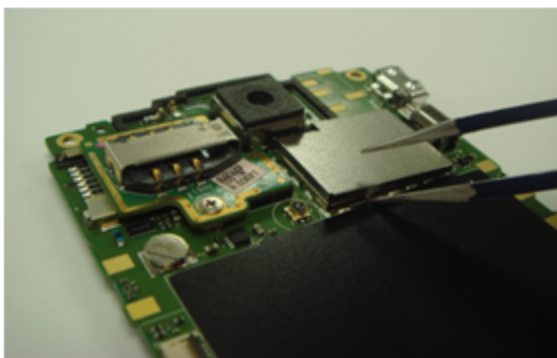
Separate FPC module and PCB board completely



Remove rubber



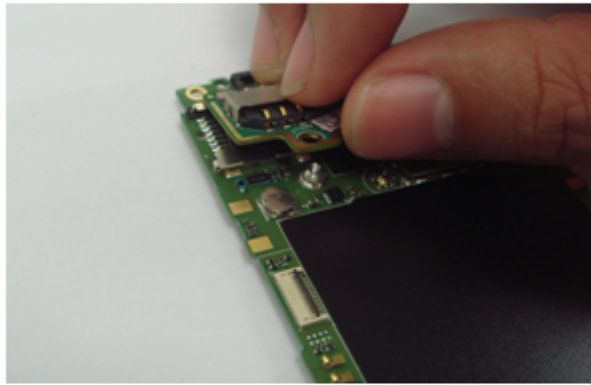
Pry off BTB connector to remove OJ module



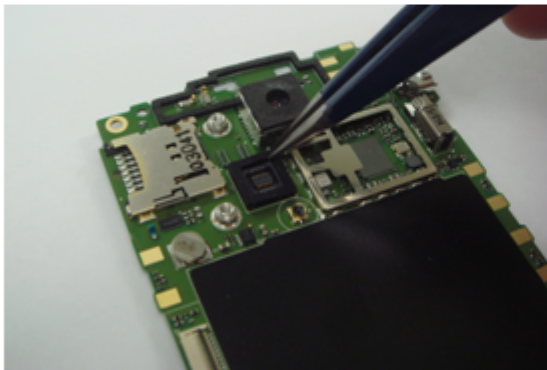
Remove Shielding Cover



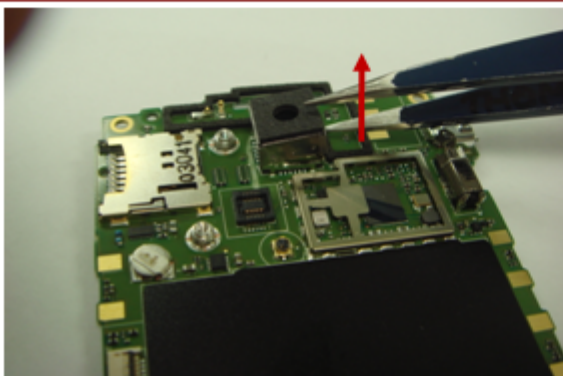
Unfasten two screws shown as left



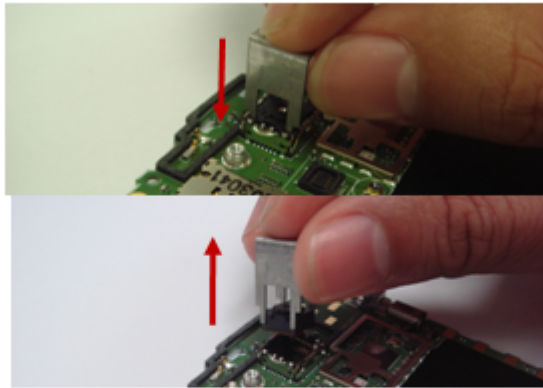
Remove Sub-board from Main board gently



Remove rubber



Disengage Camera Shielding Case along the four side to lift it up



Use Camera Jig to detach the Camera module in the direction shown left

1. Insert Jig tool into four corners completely
2. Grip and pull it out



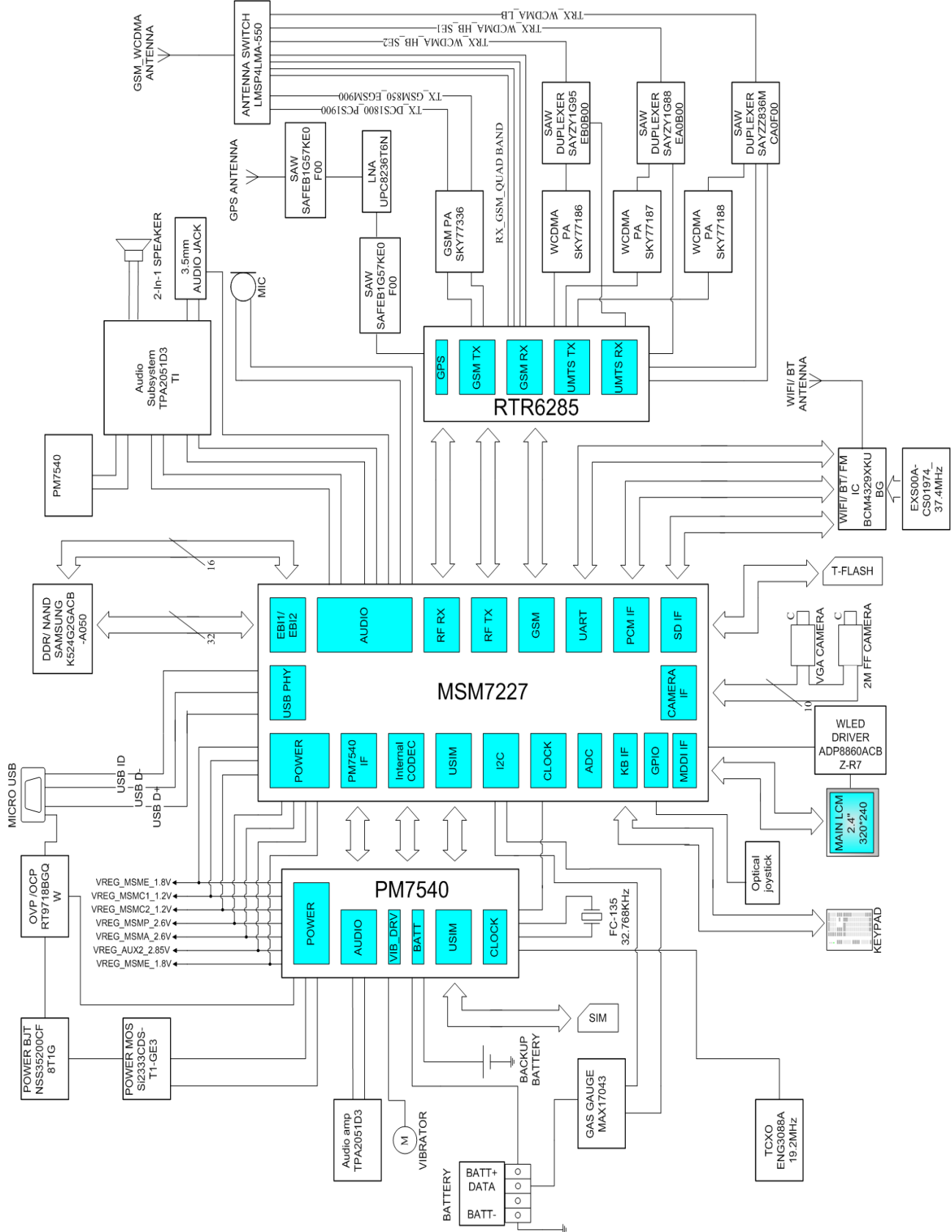
Separate Camera module completely



The disassembly is done!

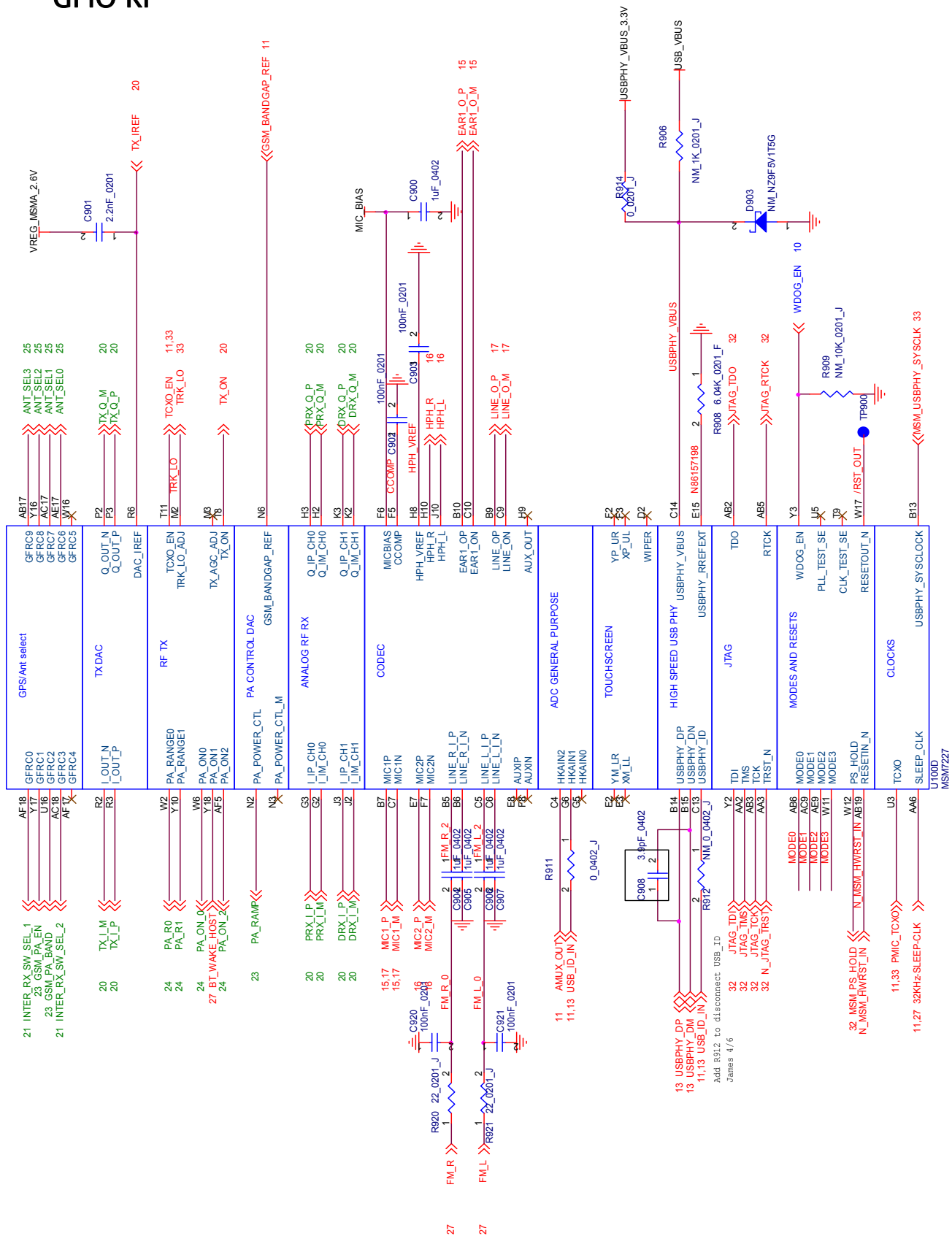
6. BLOCK DIAGRAM

6. BLOCK DIAGRAM

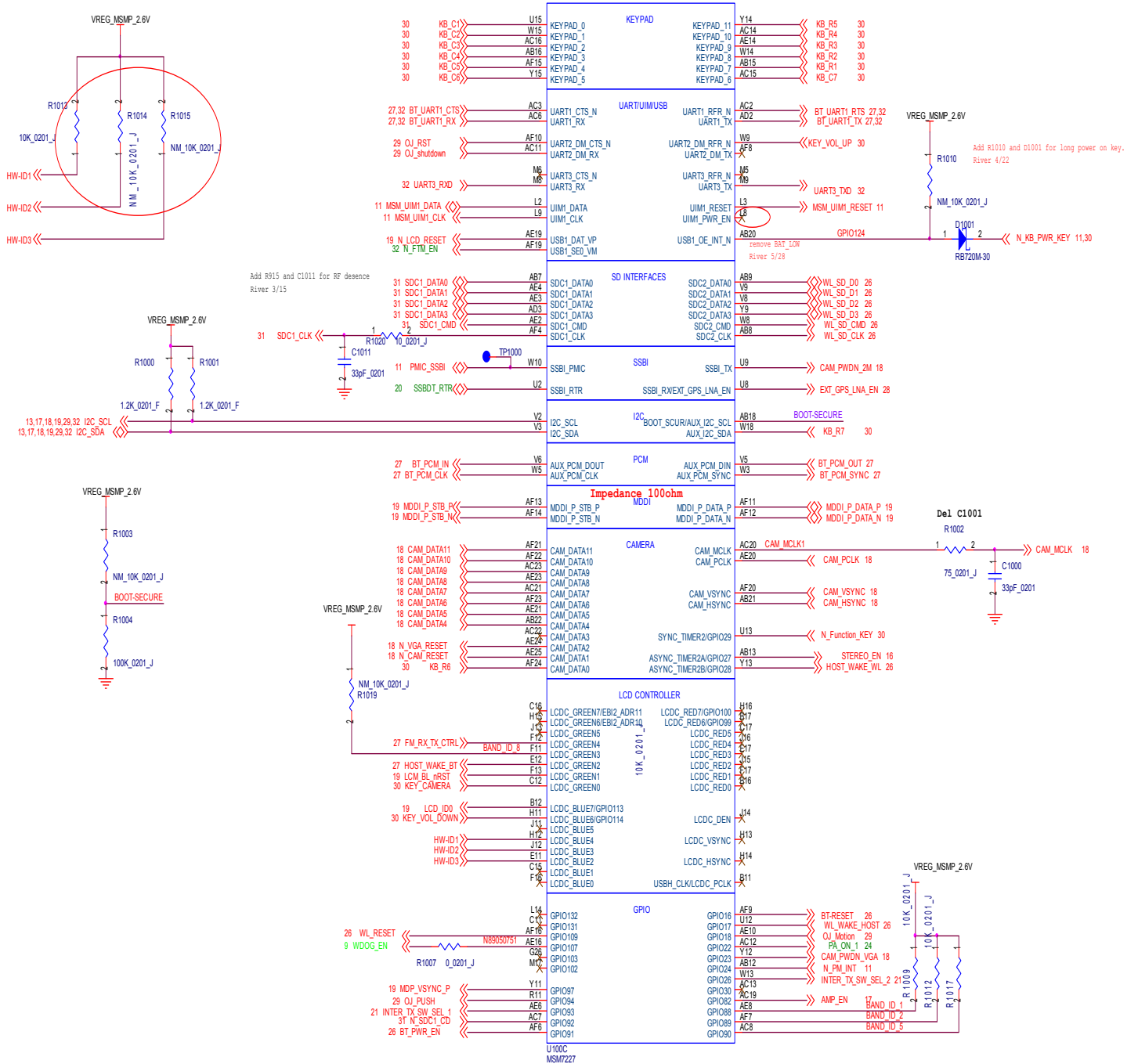


7. CIRCUIT DIAGRAM

GPIO RF

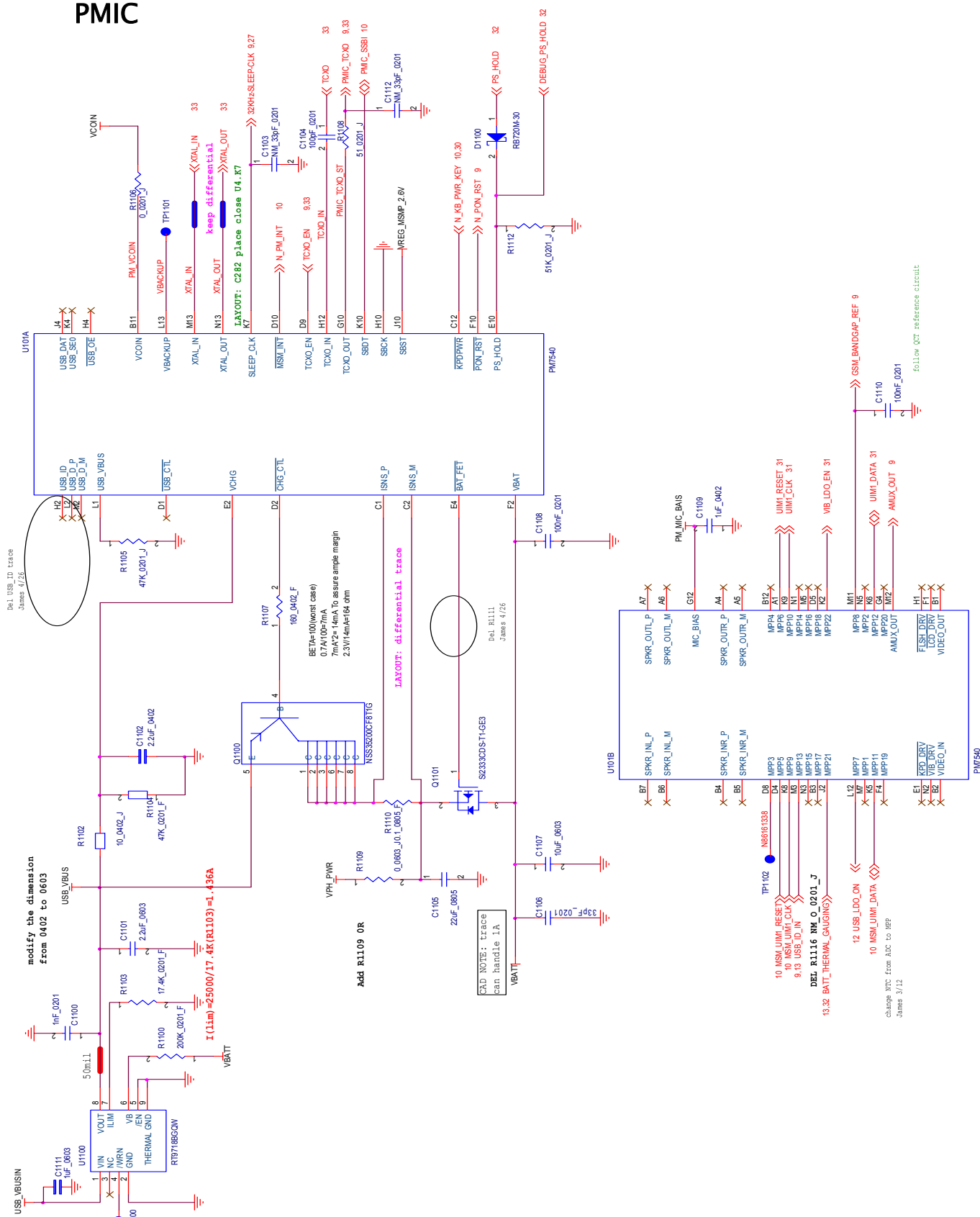


GPIO BB



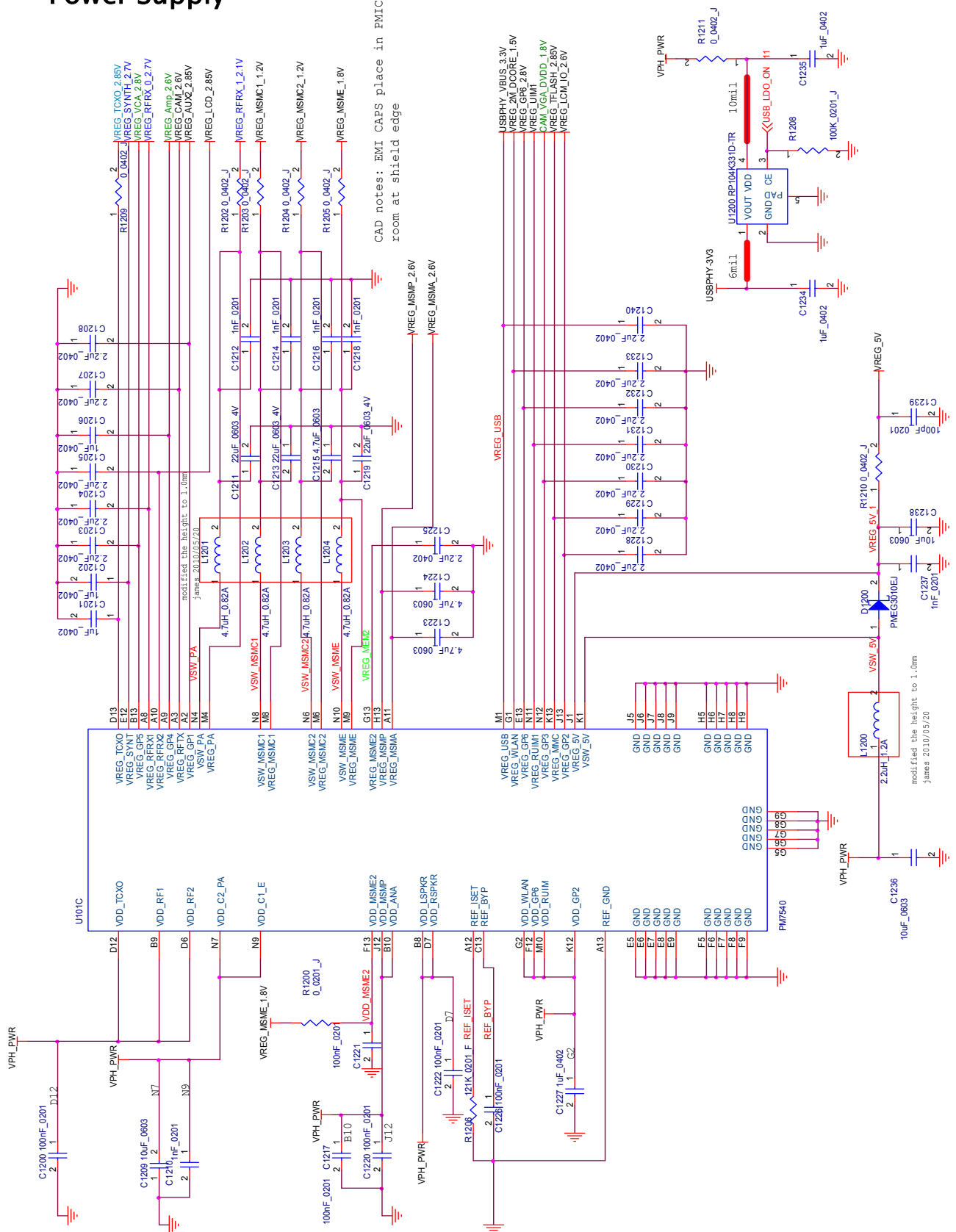
7. CIRCUIT DIAGRAM

PMIC



7. CIRCUIT DIAGRAM

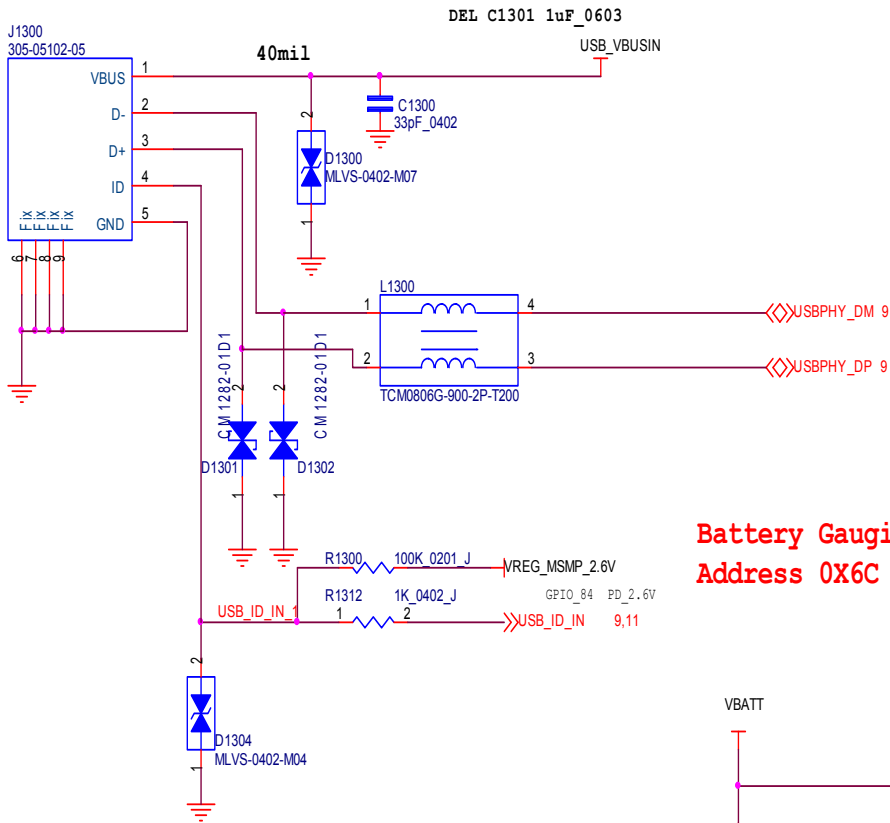
Power Supply



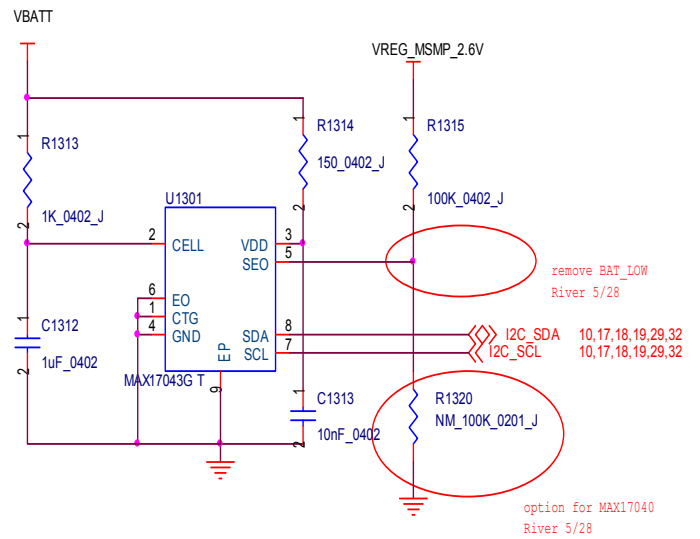
7. CIRCUIT DIAGRAM

USB/Charger

MICRO USB CONNECTOR

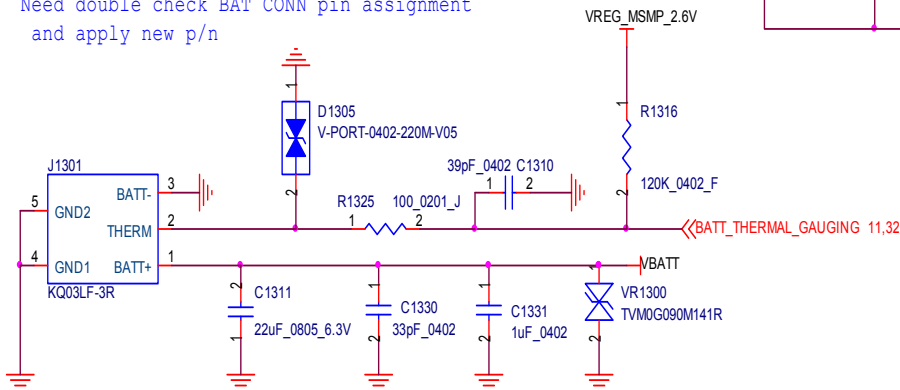


**Battery Gauging
Address 0X6C**



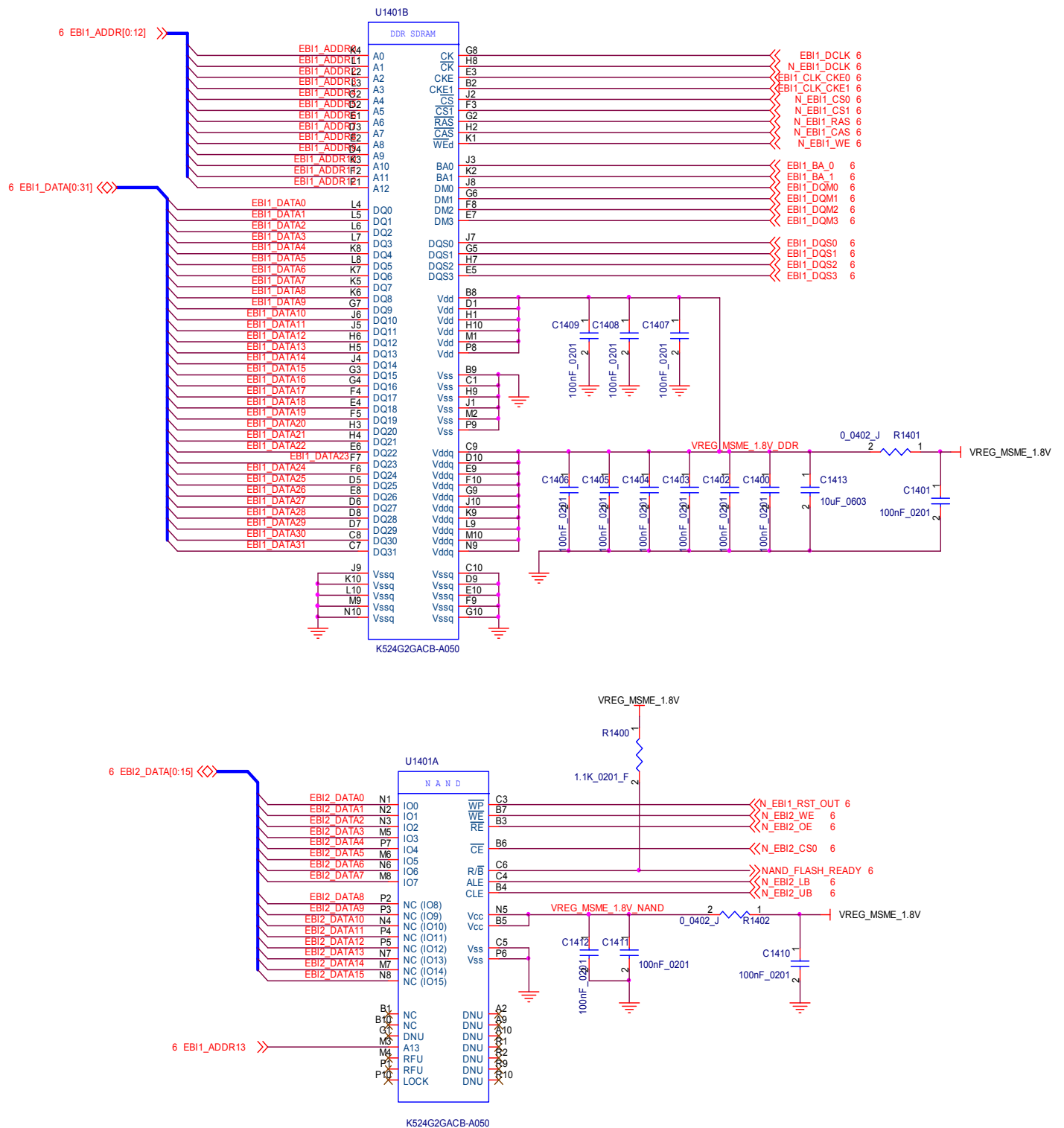
BAT CONN

Need double check BAT CONN pin assignment
and apply new p/n



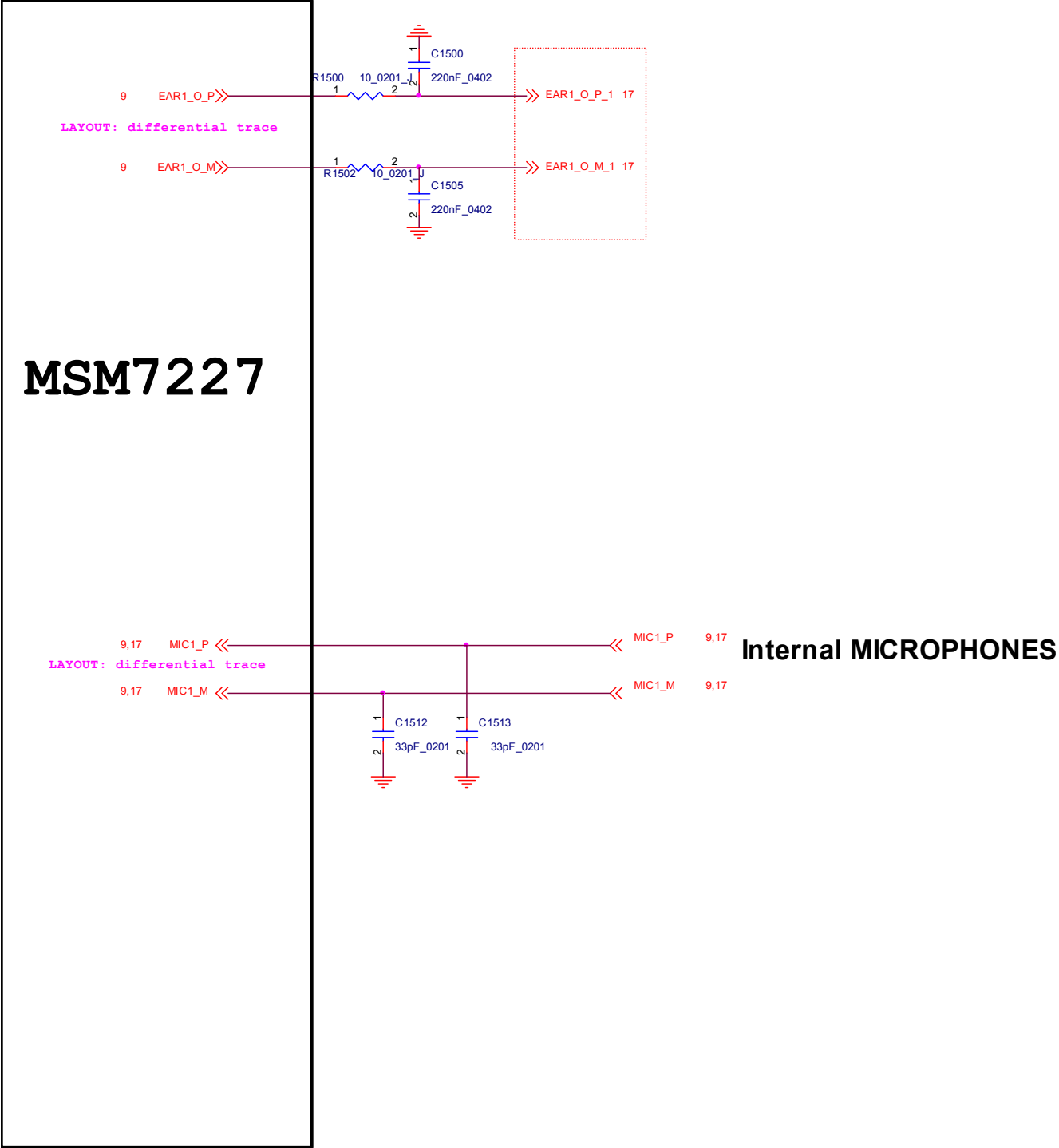
7. CIRCUIT DIAGRAM

Memory

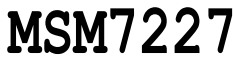


7. CIRCUIT DIAGRAM

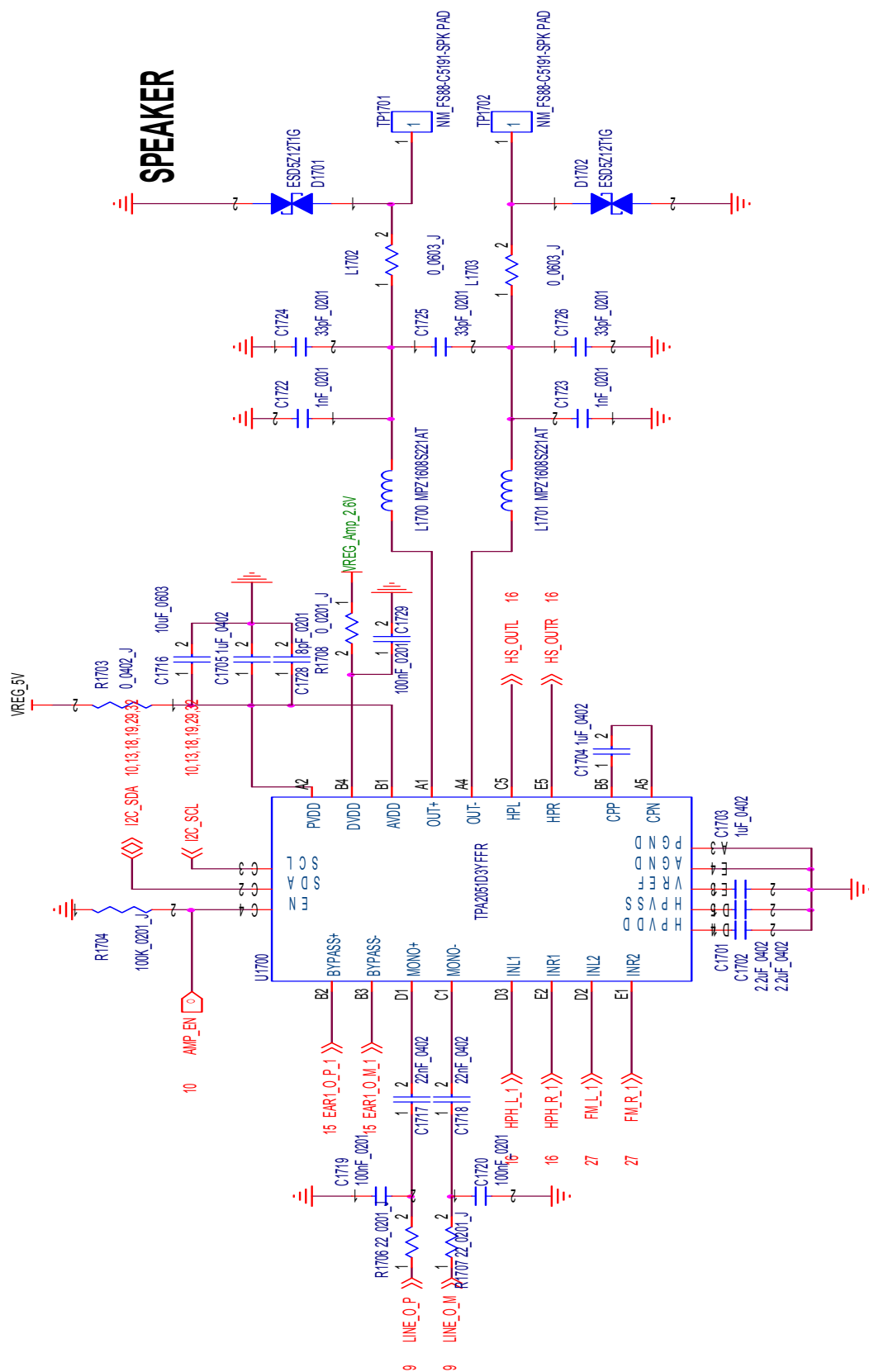
Audio1



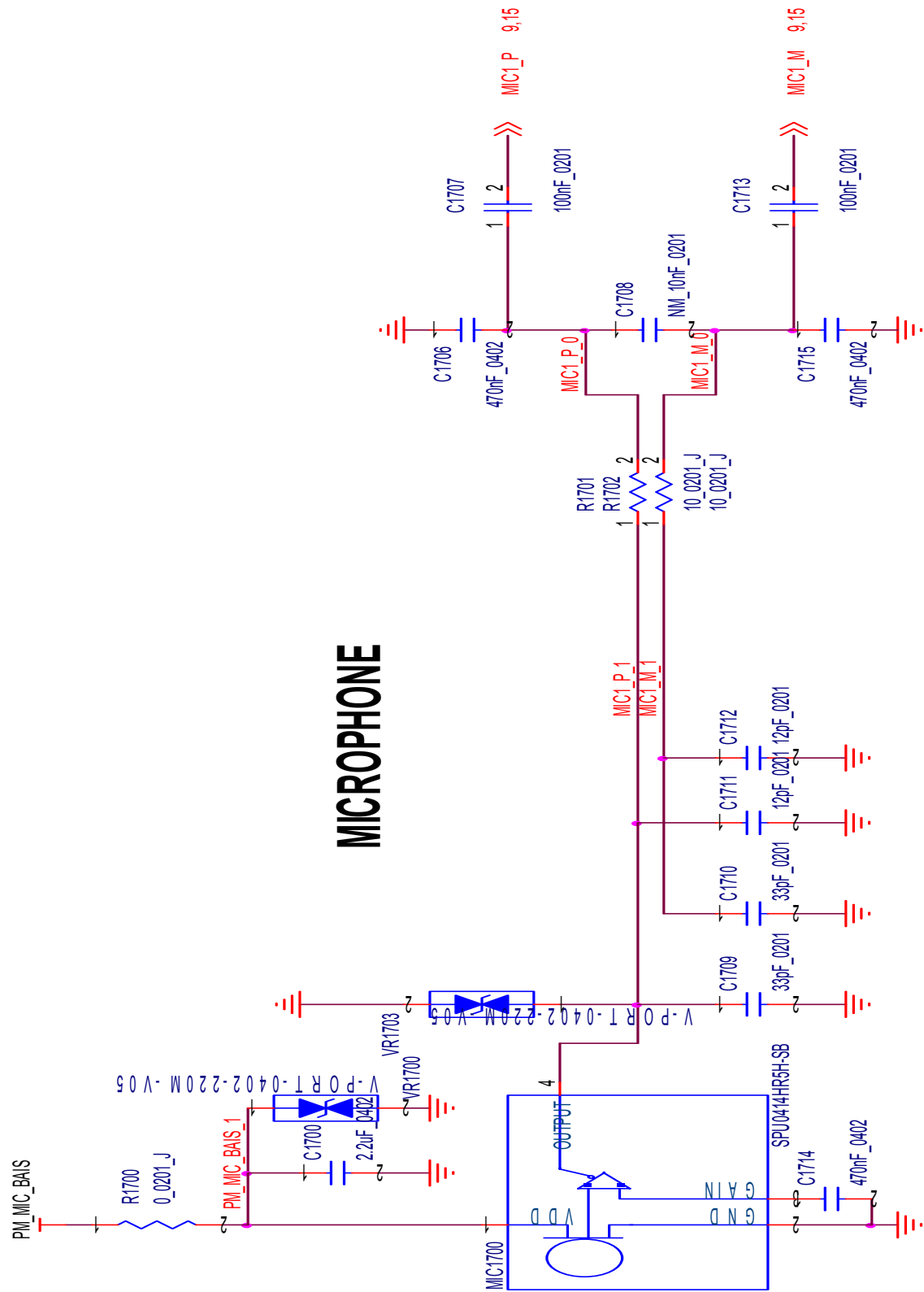
Audio2

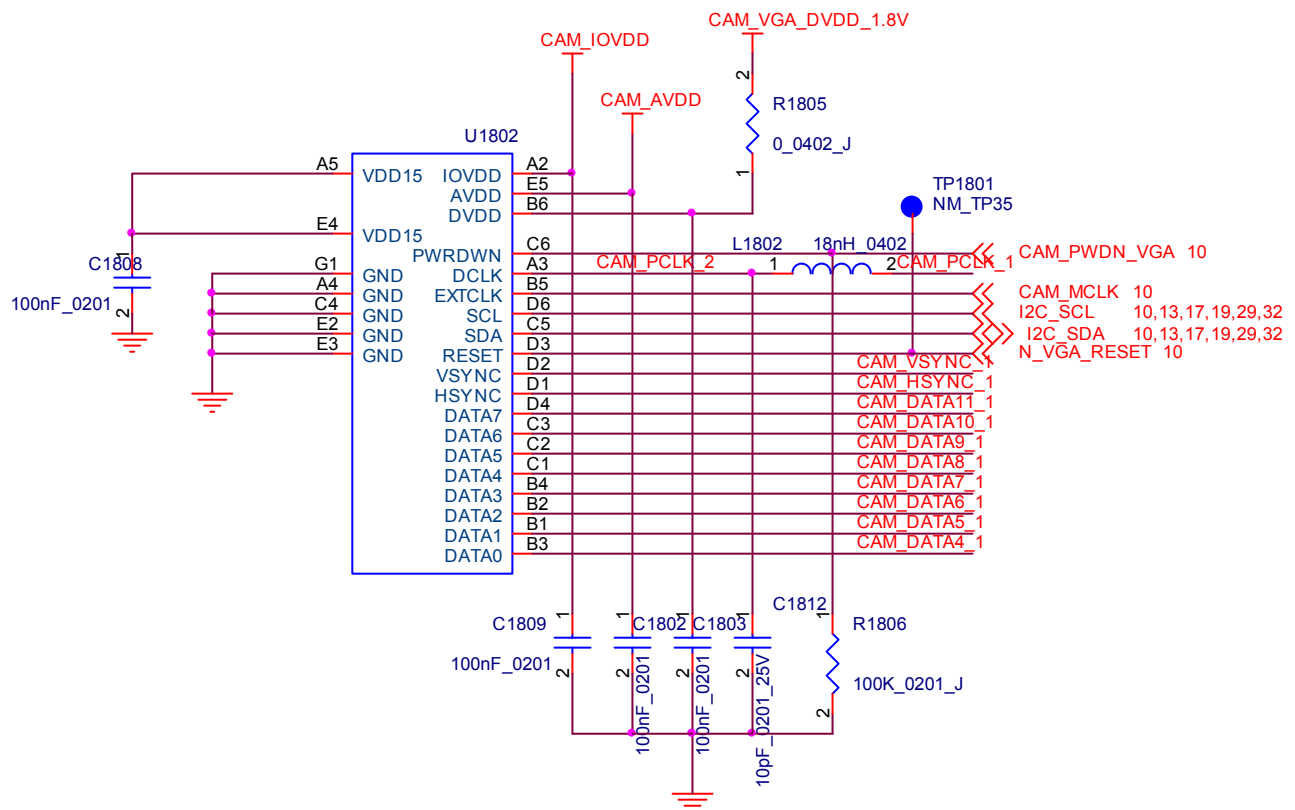


0xE0 (Writing)



Microphone



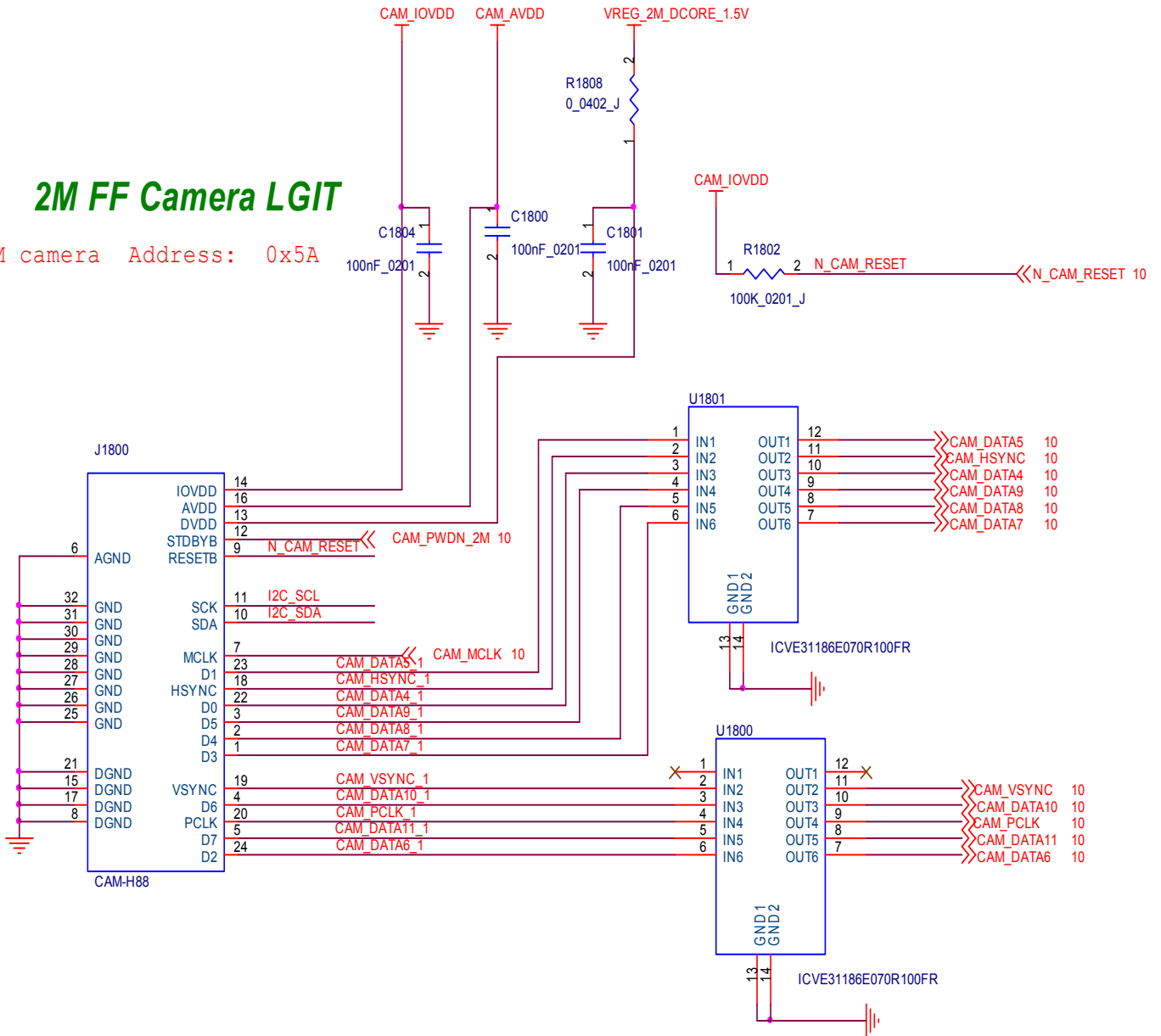


7. CIRCUIT DIAGRAM

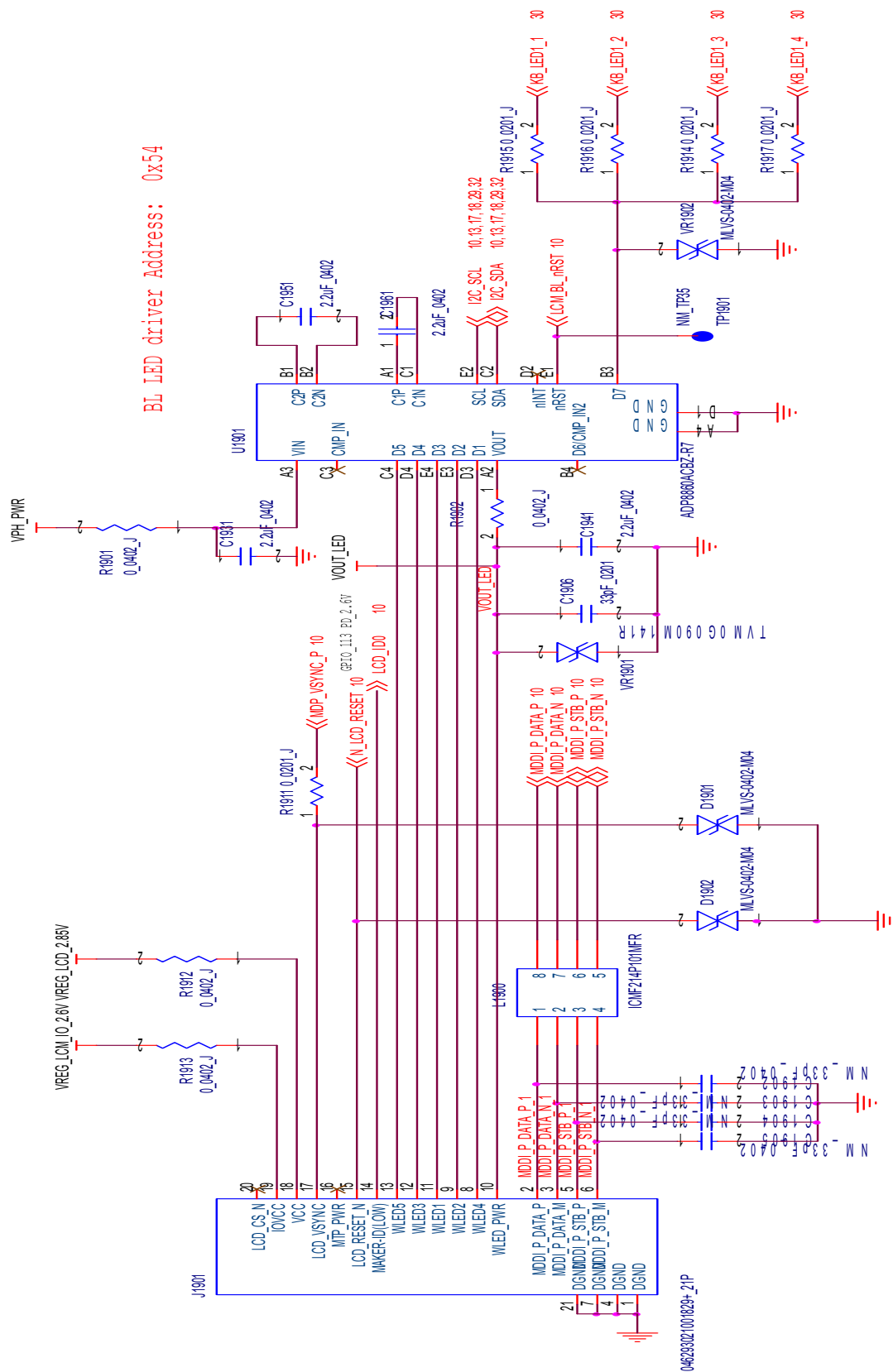
2M FF Camera

2M FF Camera LGIT

2M camera Address: 0x5A



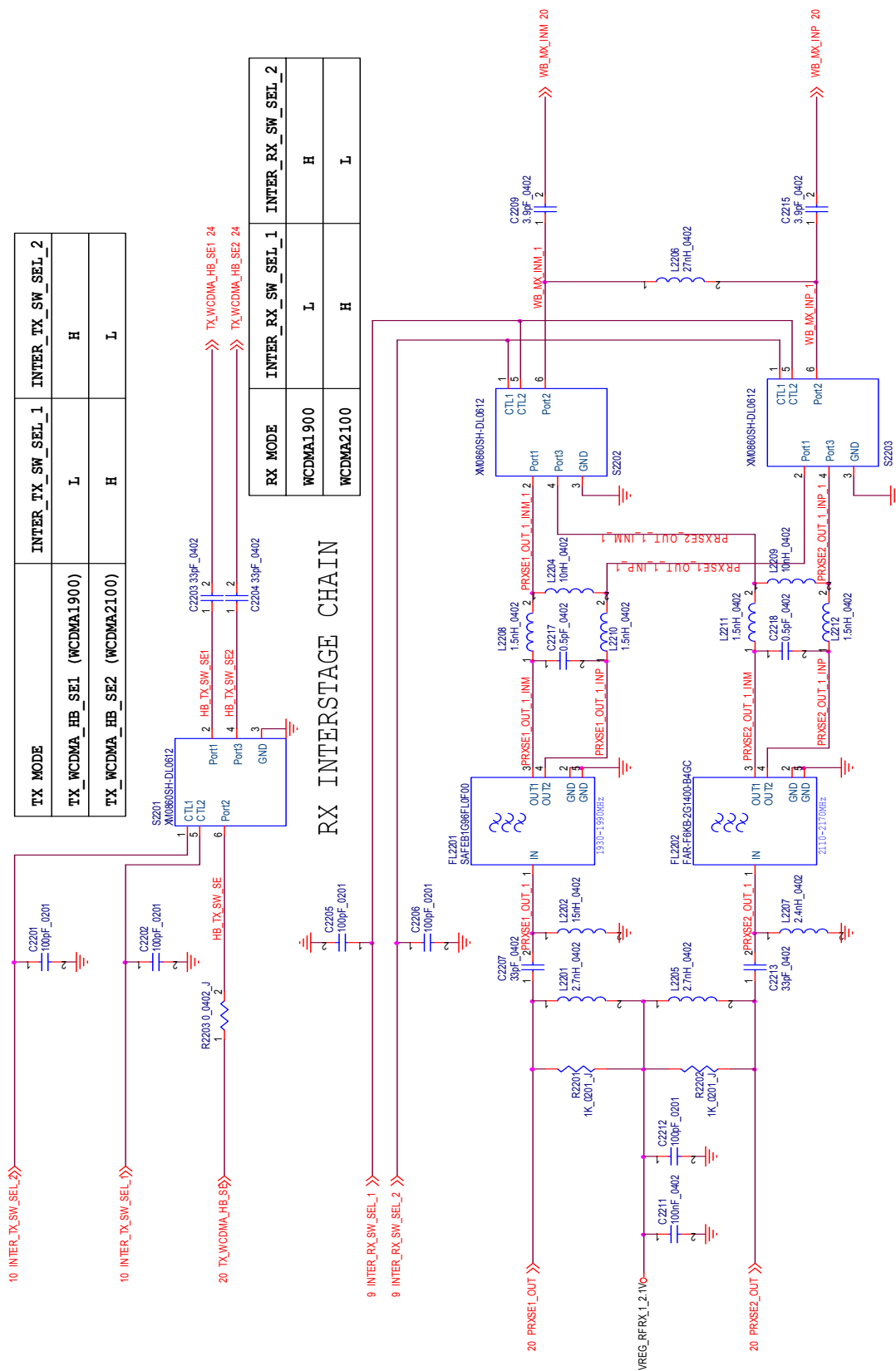
LCM



RF Transceiver1



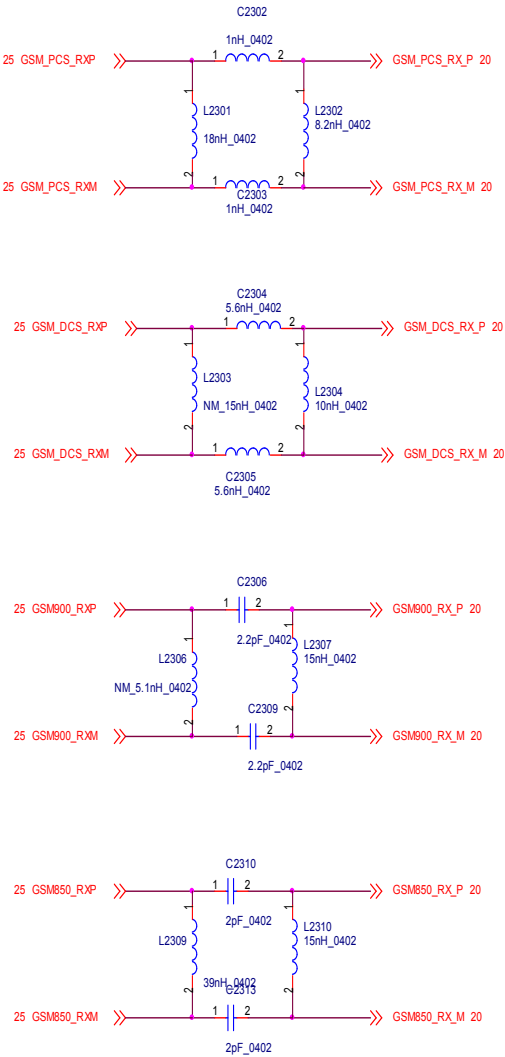
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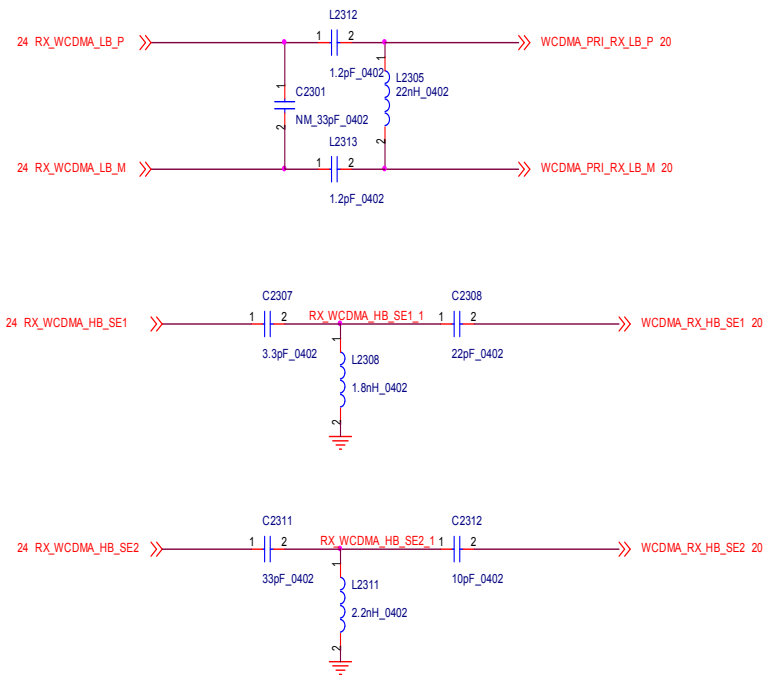
7. CIRCUIT DIAGRAM

RF Transceiver3

GSM RX CHAIN & MATCHING



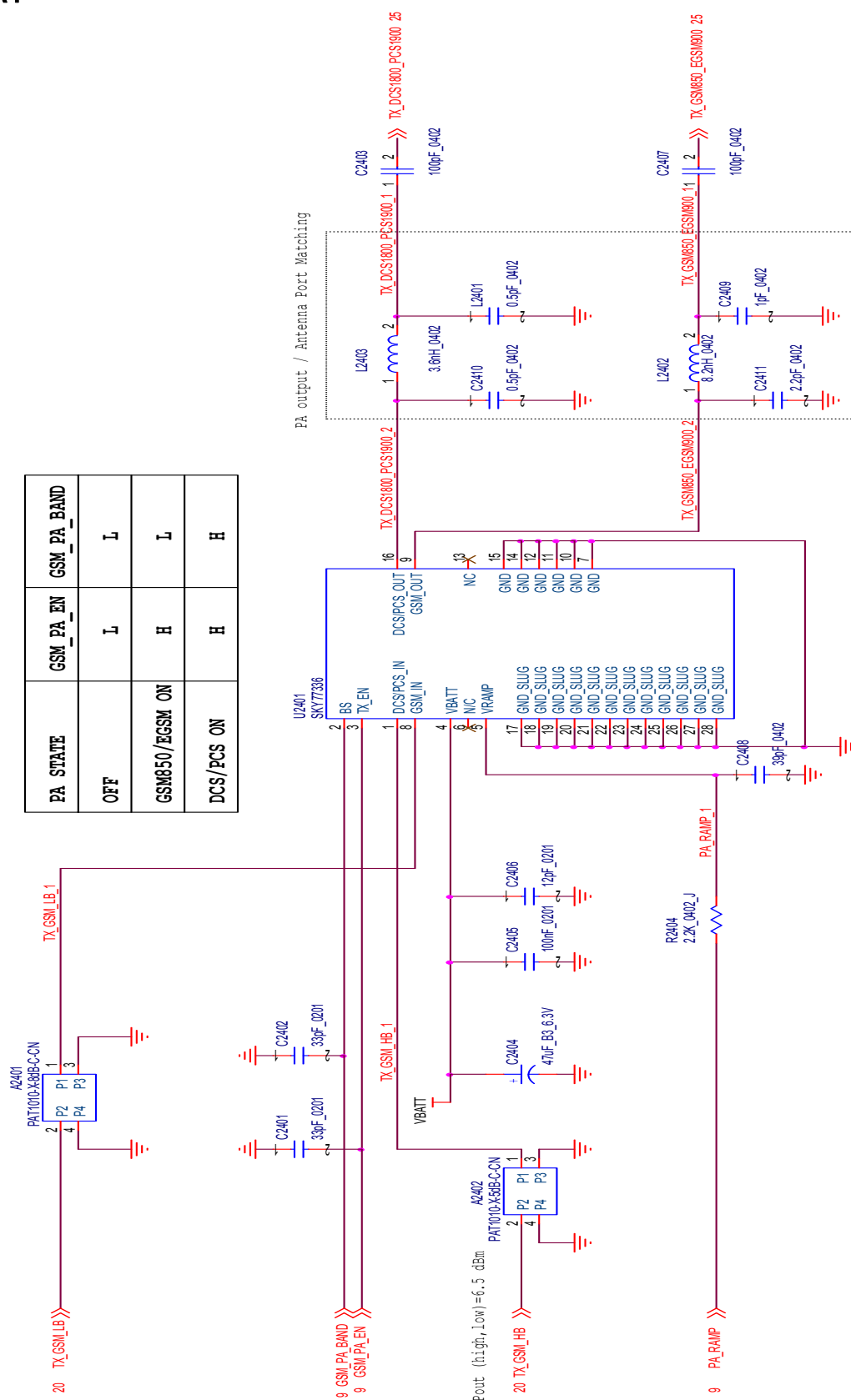
UMTS PRIMARY RX MATCHING



RF PA1

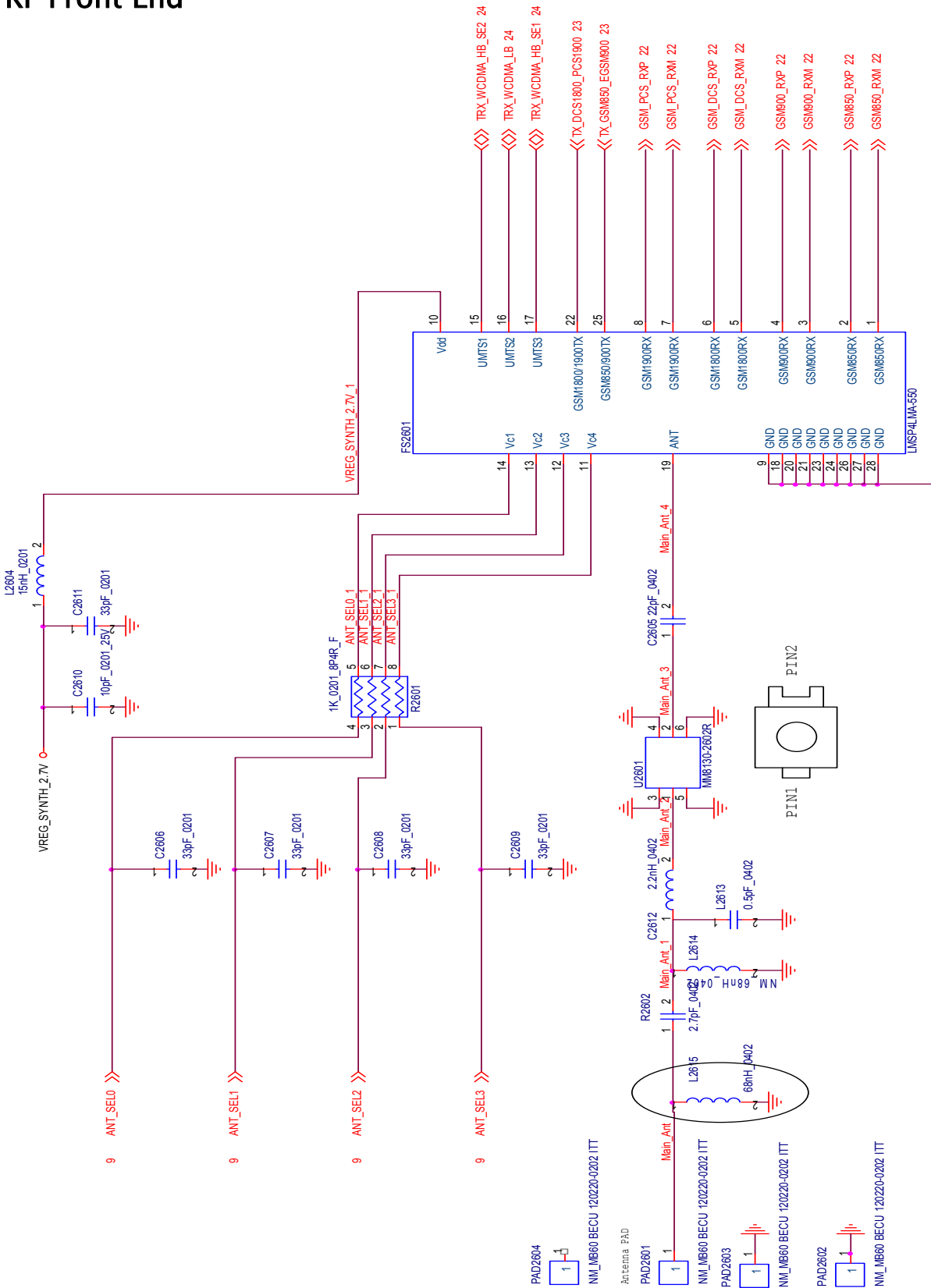
GSM Quad-band PA

PA STATE	GSM PA EN	GSM PA BAND
OFF	L	L
GSM850/EGSM ON	H	L
DCS/PCS ON	H	H

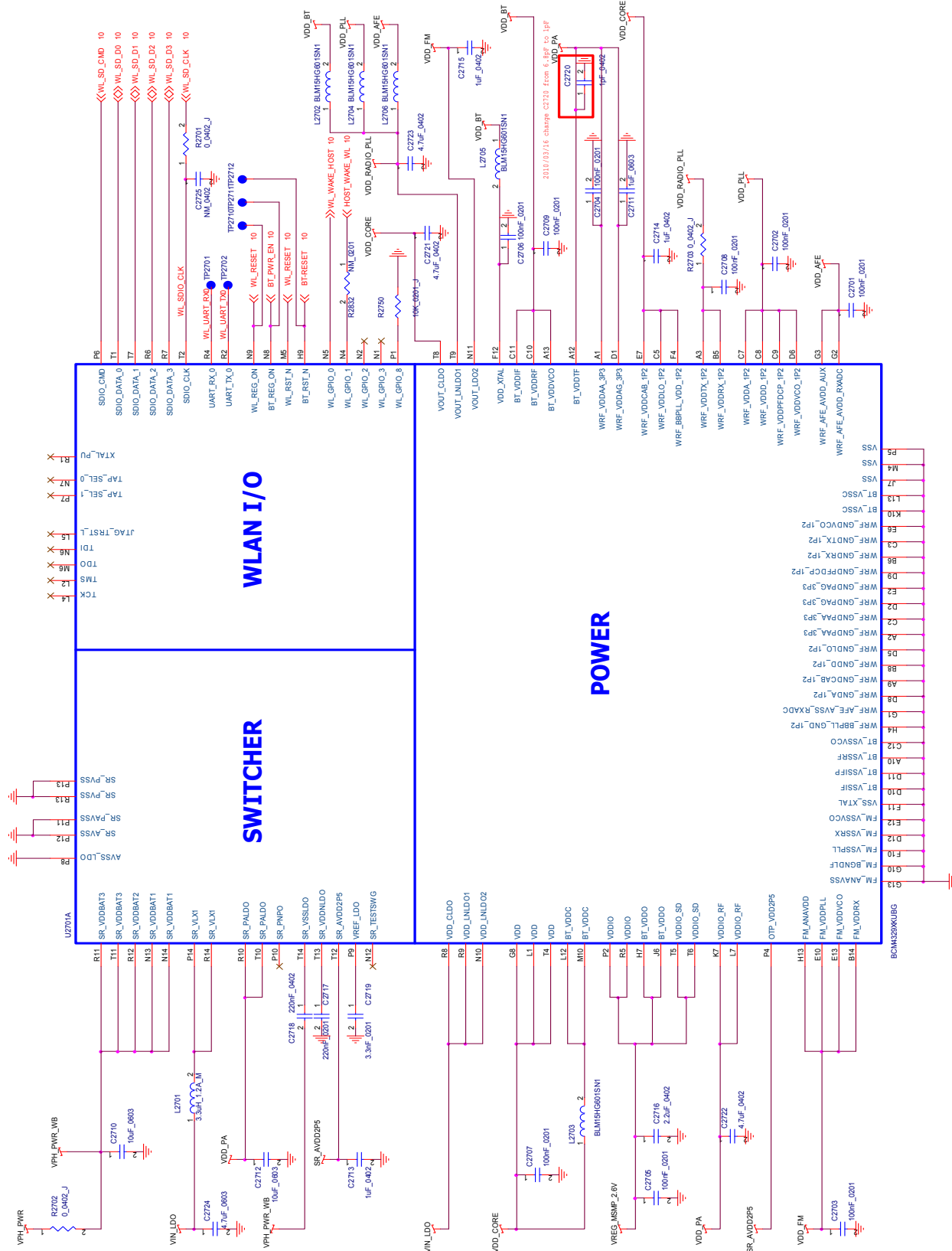


RF PA2

RF Front End

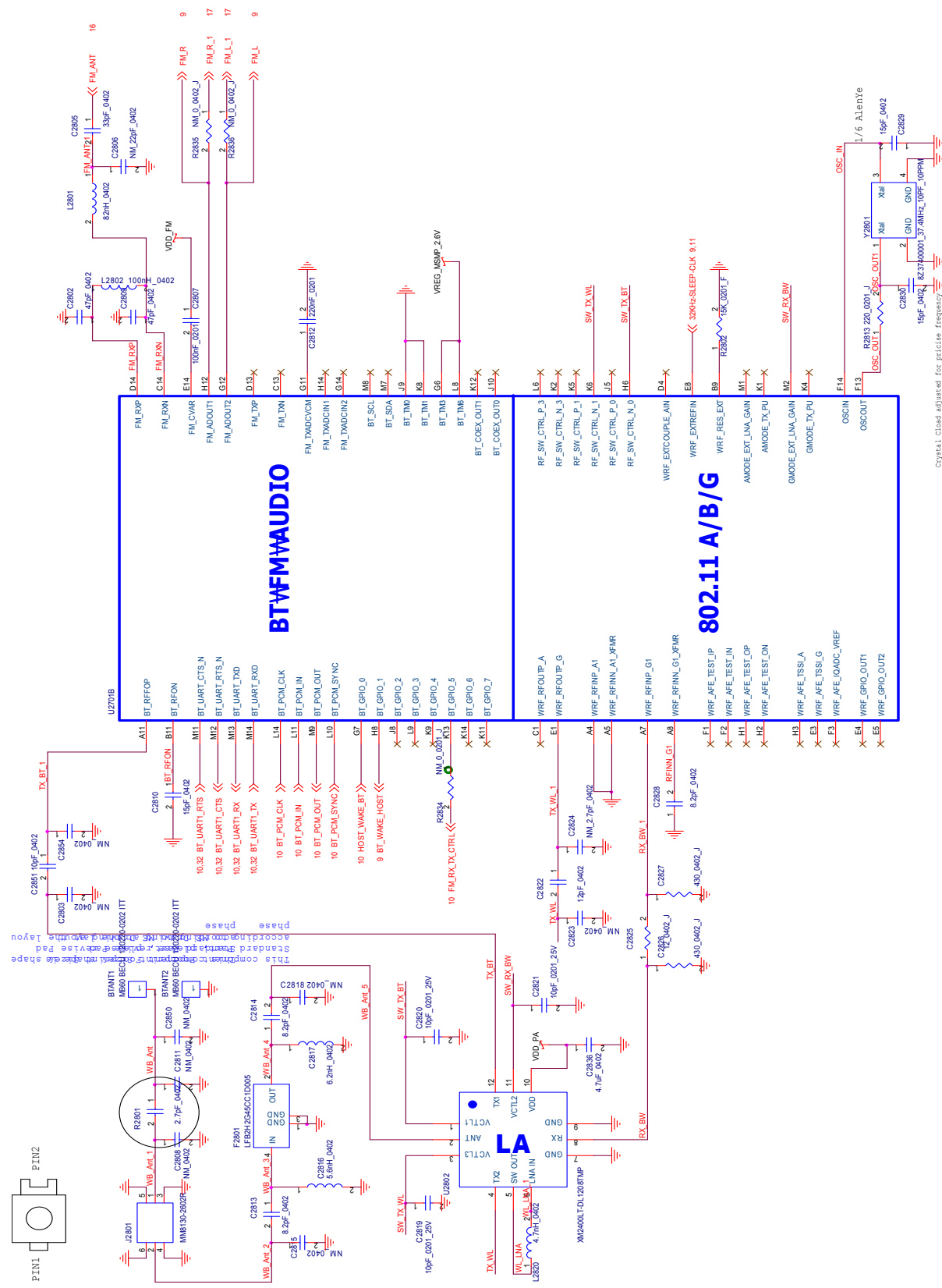


BT/WiFi/FM 1



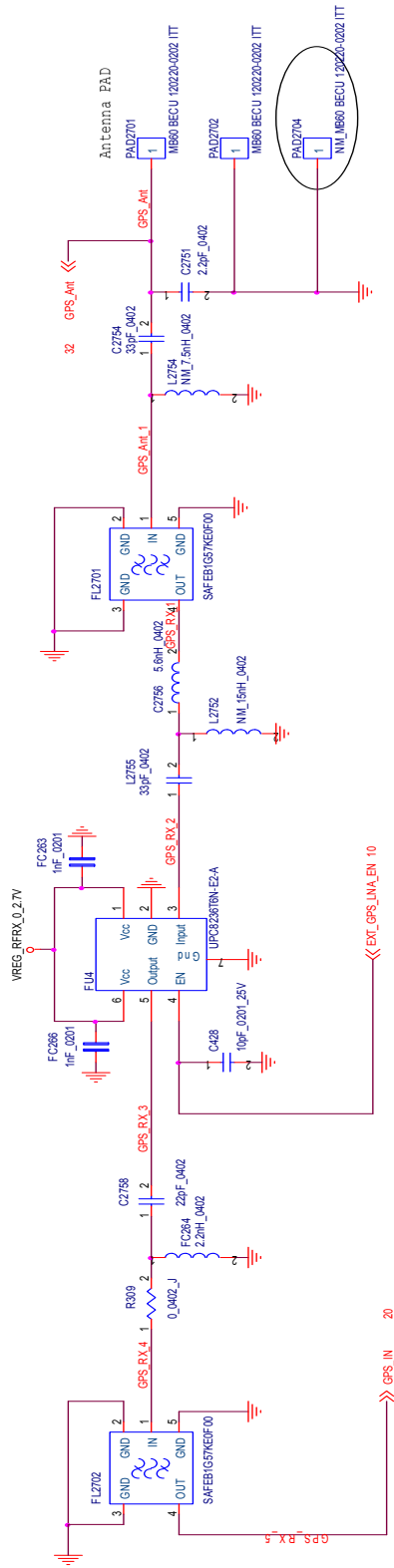
7. CIRCUIT DIAGRAM

BT/WiFi/FM 2



7. CIRCUIT DIAGRAM

GPS

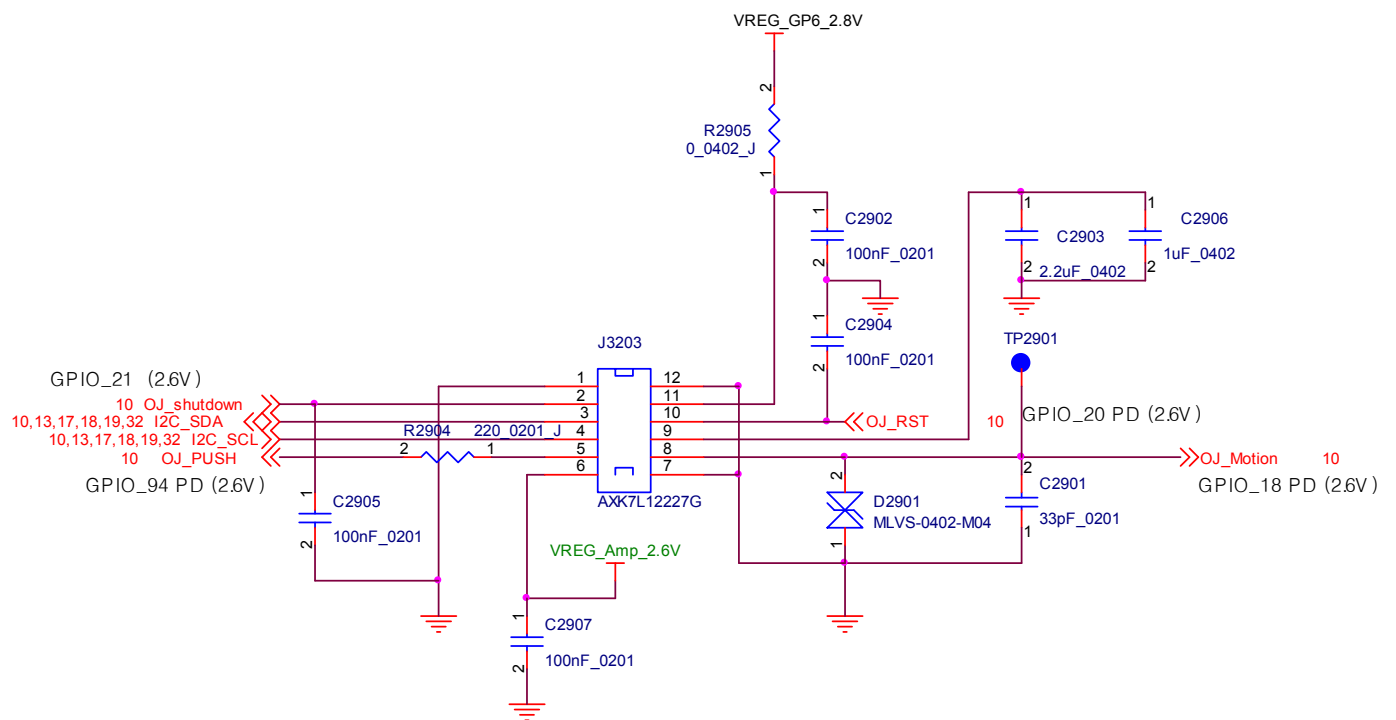


7. CIRCUIT DIAGRAM

Optical Sensor

Optic joystick B2B connector

OJ module Address: 0x33

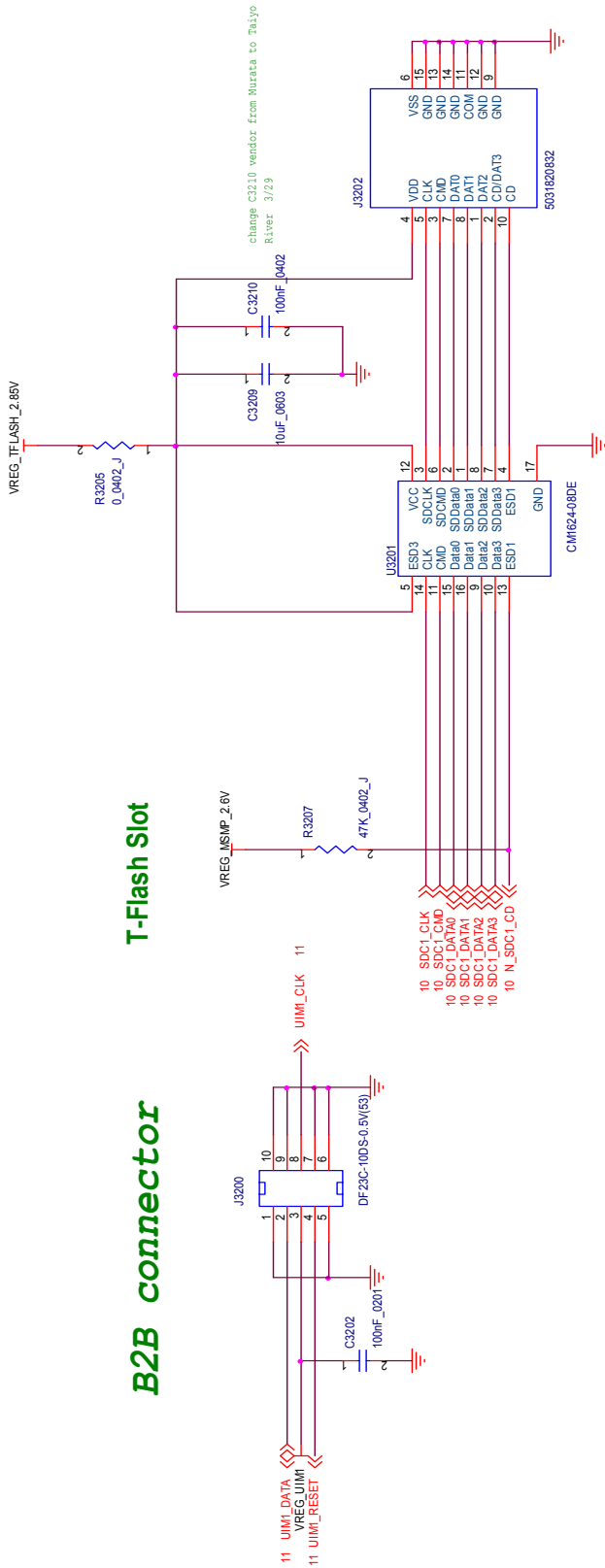


Keypad & Backlight



7. CIRCUIT DIAGRAM

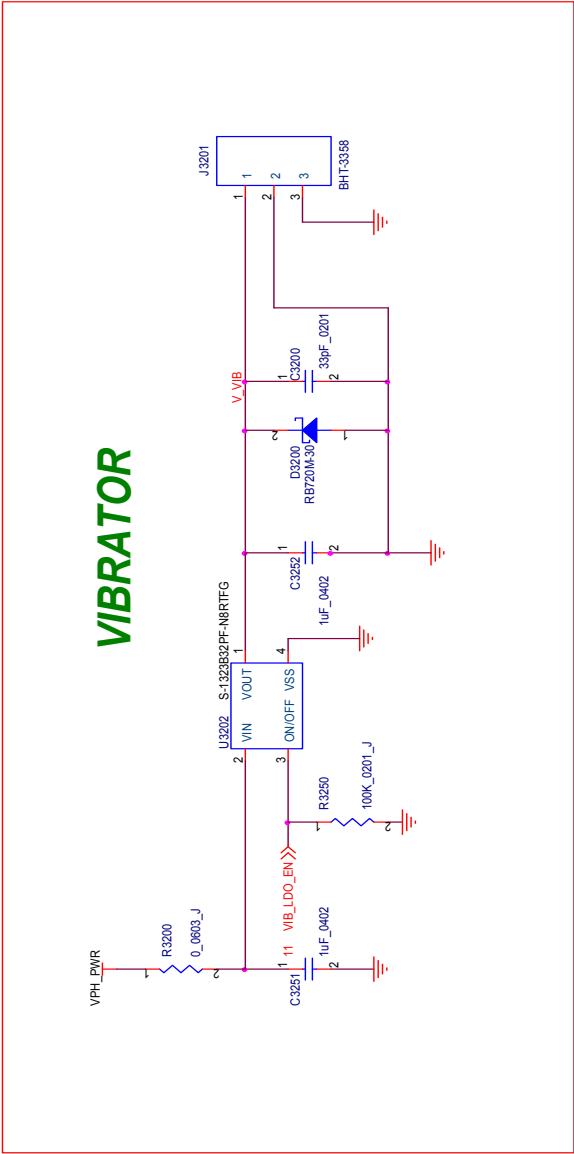
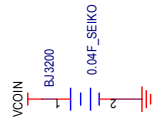
Vibrator & Connector



T-Flash Slot

B2B connector

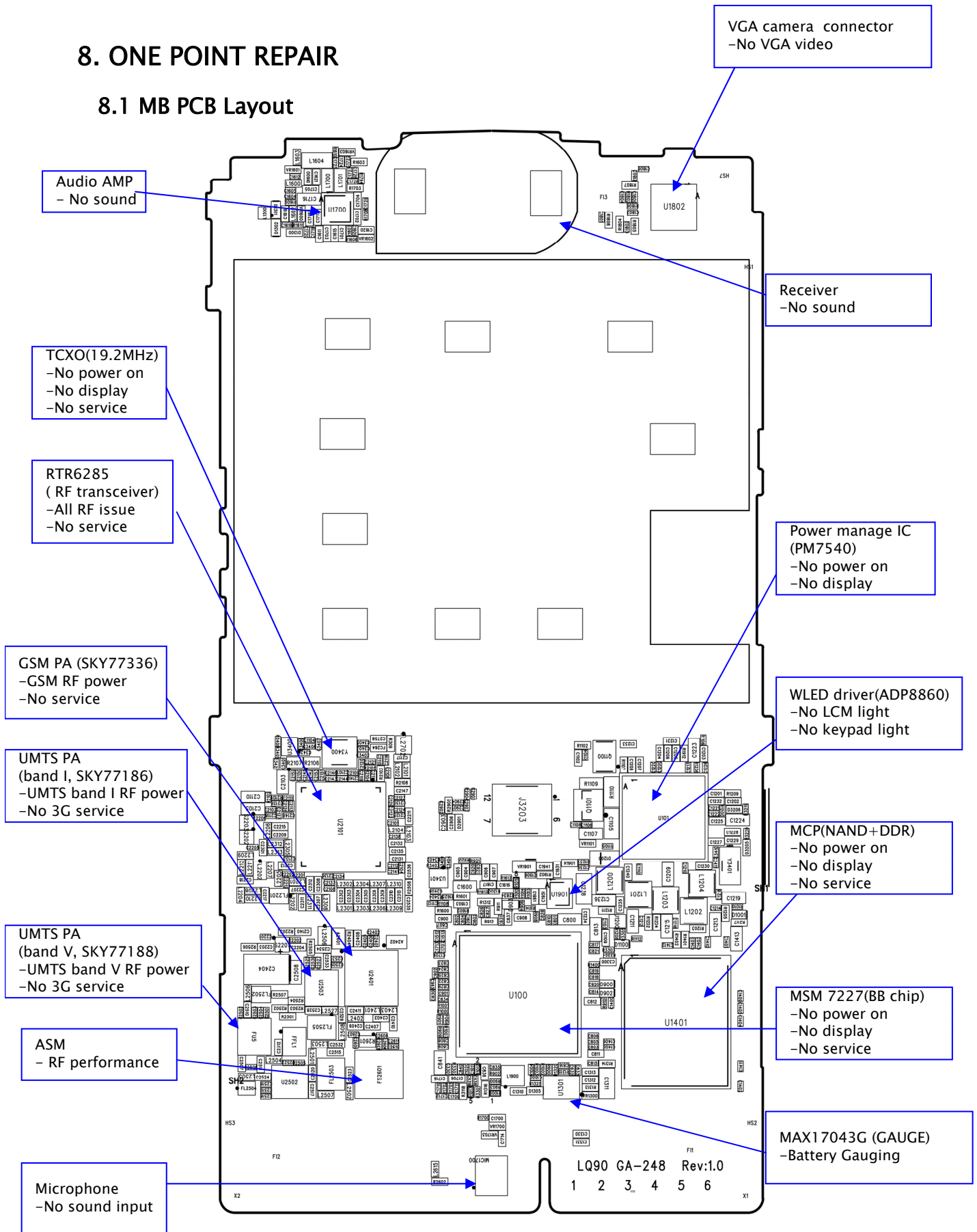
Back-up Battery



VIBRATOR

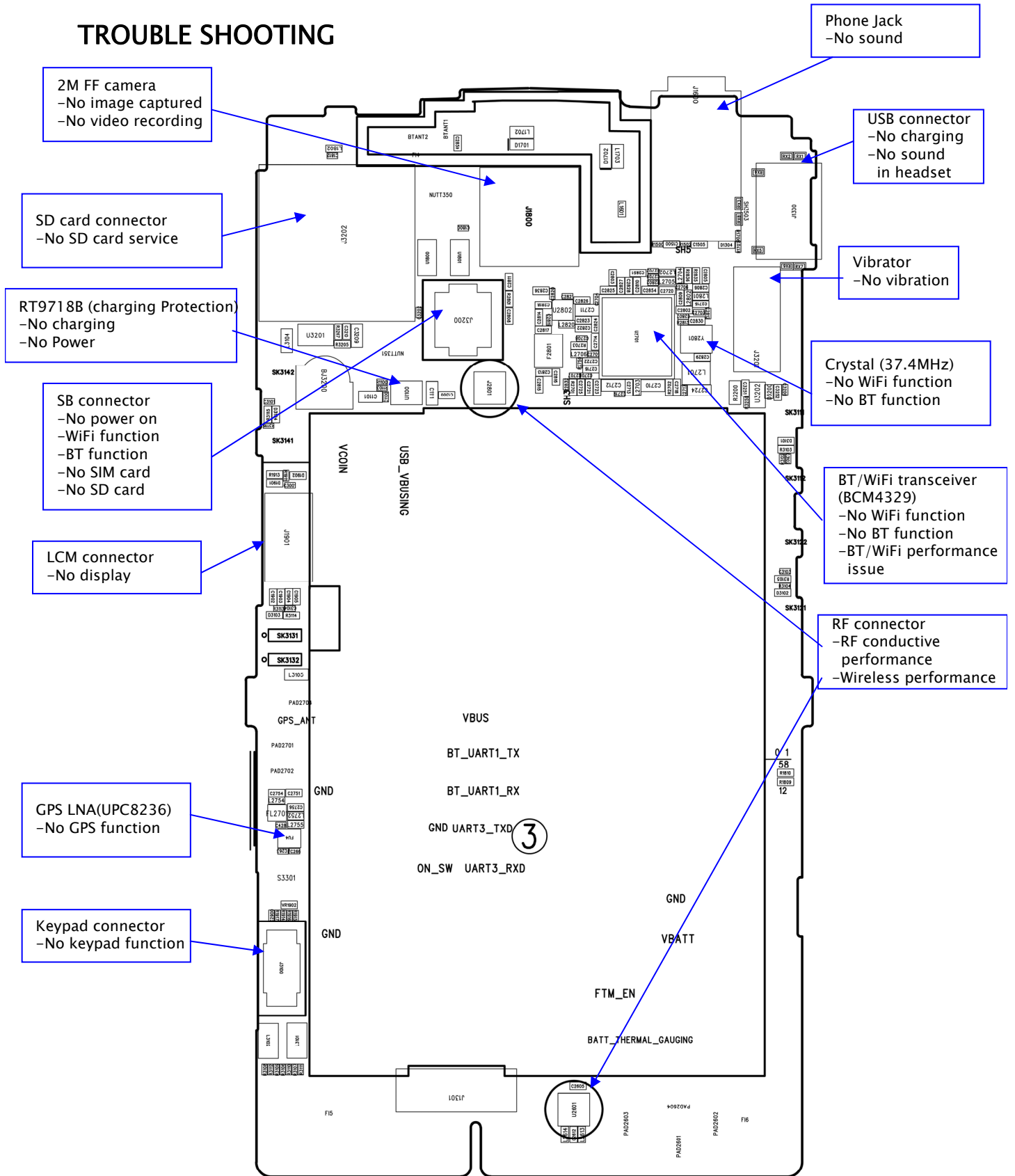
8. ONE POINT REPAIR

8.1 MB PCB Layout



C570 MB TOP SIDE PCB LAYOUT

TROUBLE SHOOTING

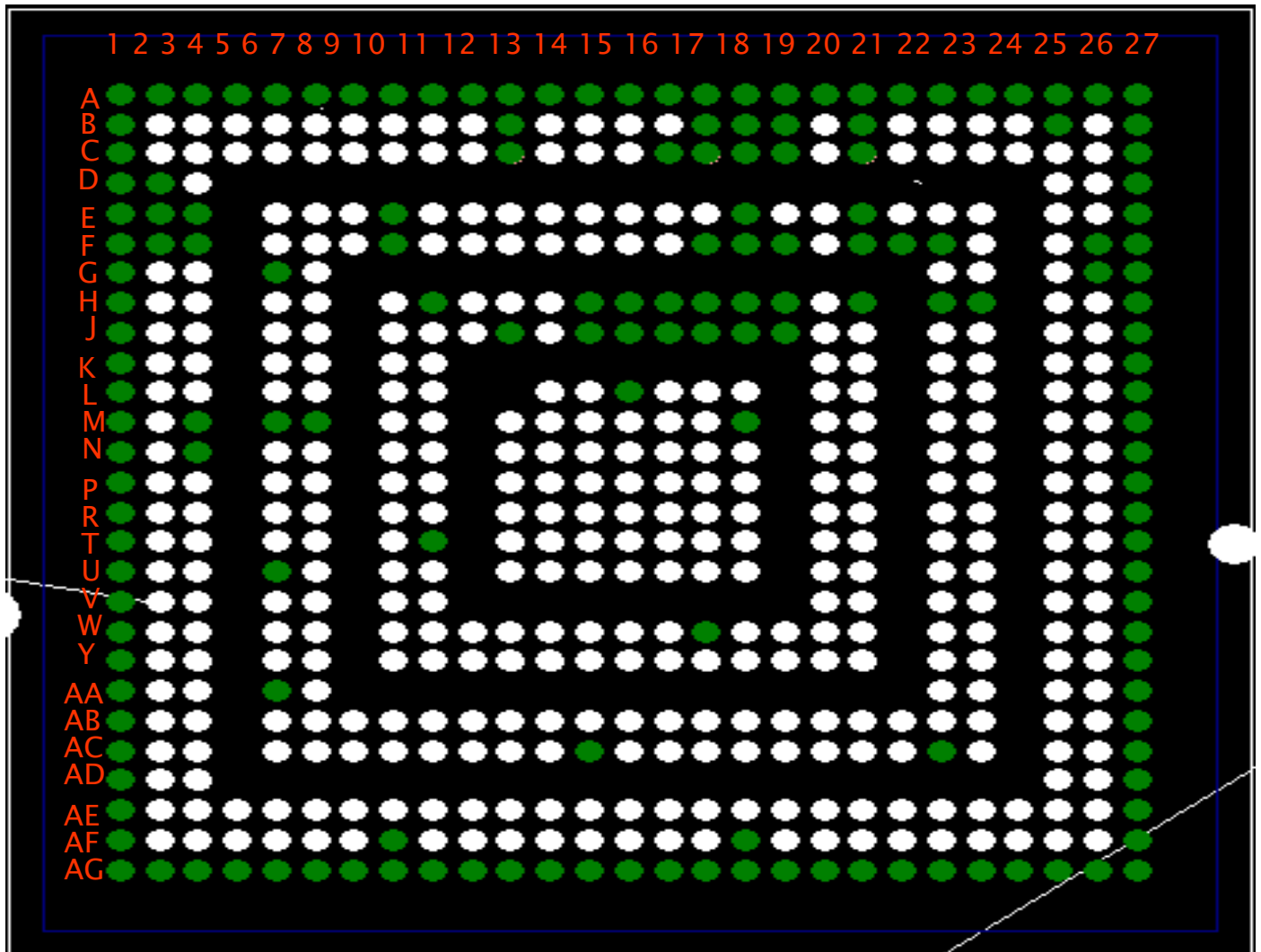


C570 MB BOTTOM SIDE PCB LAYOUT

U100 MSM 7227 pin assignment

[illegible]

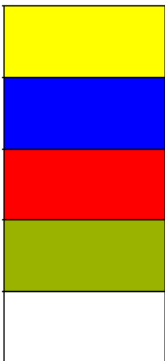
U100 MSM 7227 pin assignment



- unused pin
- used pin

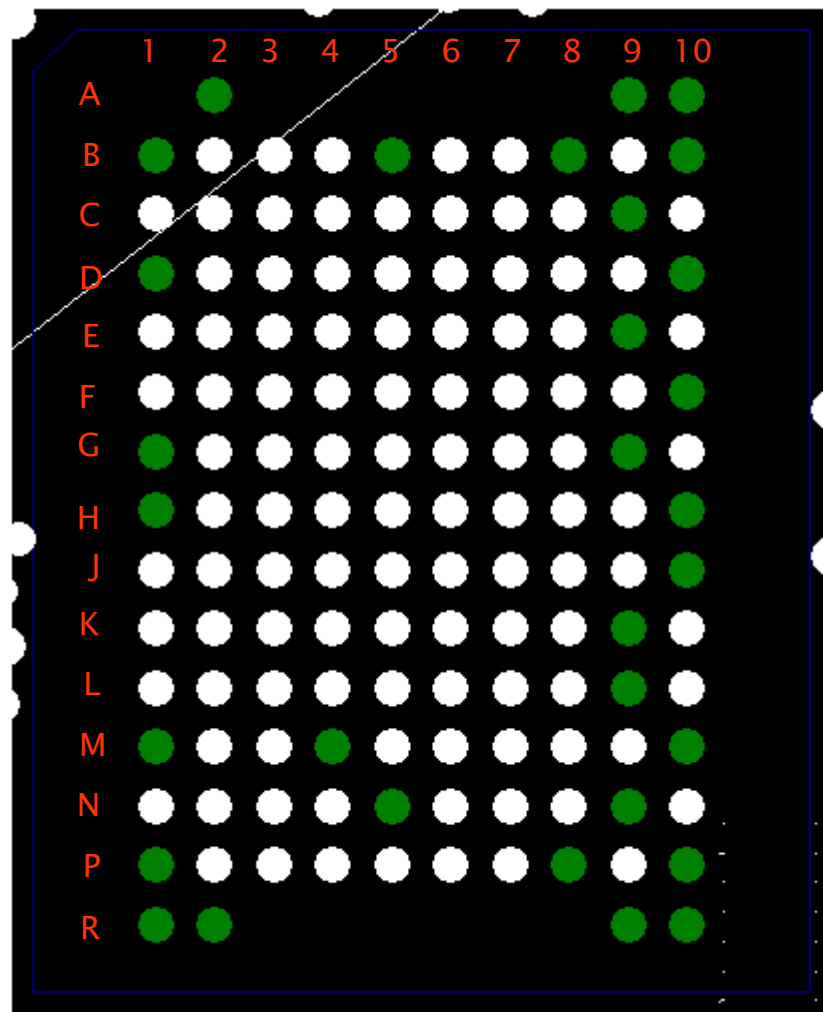
U1401 Memory pin assignment

	1	2	3	4	5	6	7	8	9	10
A	-	DNU	-	-	-	-	-	-	DNU	DNU
B	NC	NC	/REn	CLEn	VCCn	/CEn	/WEn	VDDd	VSSd	NC
C	VSSd	A4d	/WPn	ALEn	VSSn	R/Bn	DQ31d	DQ30d	VDDQd	VSSQd
D	VDDd	A5d	A7d	A9d	DQ25d	DQ27d	DQ29d	DQ28d	VSSQd	VDDQd
E	A6d	A8d	CKEd	DQ18d	DQS3d	DQ22d	DM3d	DQ26d	VDDQd	VSSQd
F	A12d	A11d	NC	DQ17d	DQ19d	DQ24d	DQ23d	DM2d	VSSQd	VDDQd
G	NC	/RASd	DQ15d	DQ16d	DQS1d	DM1d	DQ9d	CKd	VDDQd	VSSQd
H	VDDd	/CASd	DQ20d	DQ21d	DQ13d	DQ12d	DQS2d	/CKd	VSSd	VDDd
J	VSSd	/CSd	BA0d	DQ14d	DQ11d	DQ10d	DQS0d	DM0d	VSSQd	VDDQd
K	/WEd	BA1d	A10d	A0d	DQ7d	DQ8d	DQ6d	DQ4d	VDDQd	VSSQd
L	A1d	A2d	A3d	DQ0d	DQ1d	DQ2d	DQ3d	DQ5d	VDDQd	VSSQd
M	VDDd	VSSd	A13d	NC	IO3n	IO5n	IO14n	IO7n	VSSQd	VDDQd
N	IO0n	IO1n	IO2n	IO10n	VCCn	IO6n	IO13n	IO15n	VDDQd	VSSQd
P	NC	IO8n	IO9n	IO11n	IO12n	VSSn	IO4n	VDDd	VSSd	NC
R	DNU	DNU	-	-	-	-	-	-	DNU	DNU



- NAND
- M-DDR
- Power
- Ground
- NC/DNU

U1401 Memory pin assignment



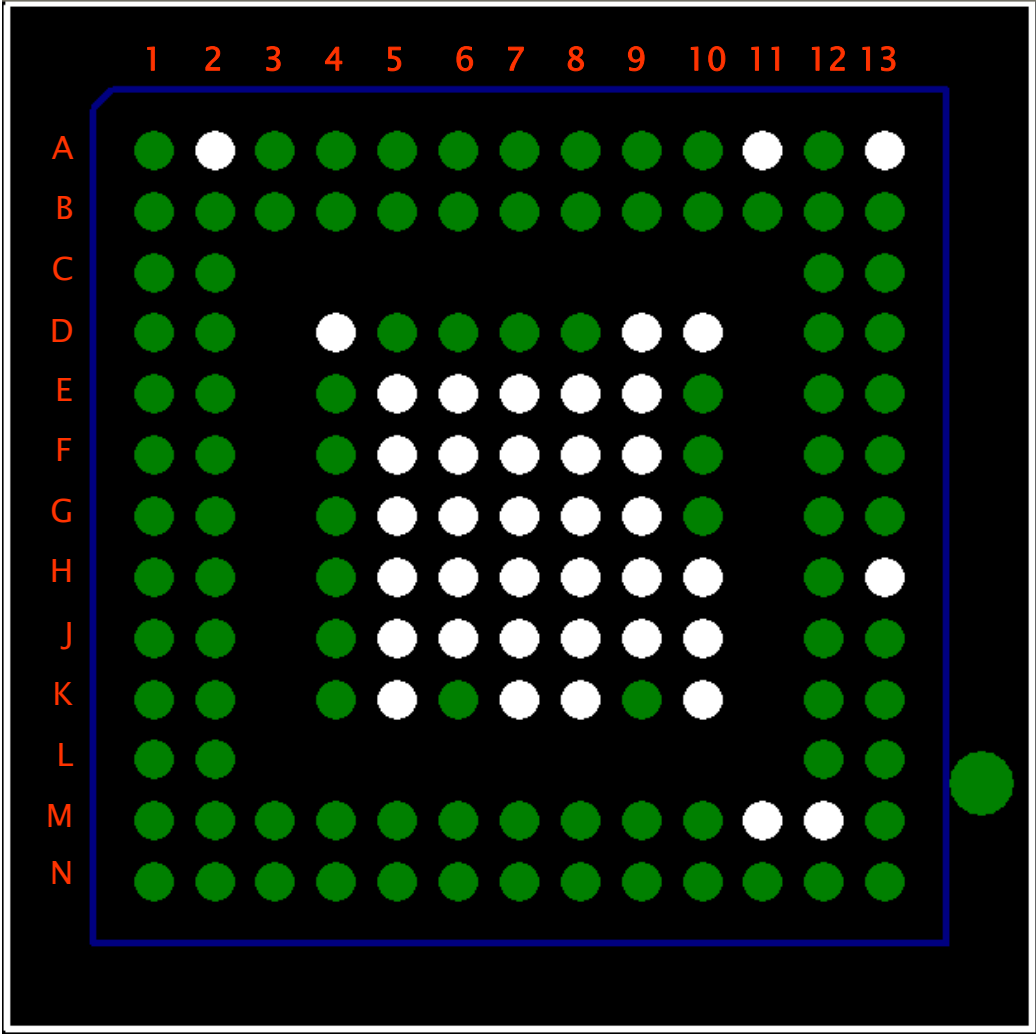
● unused pin

○ used pin

U101 PM7540 pin assignment

	1	2	3	4	5	6	7	8	9	10	11	12	13	
A	MPP_6	VREG_GP1	VREG_RFTX	SPKR_OUT_R_P	SPKR_OUT_R_M	SPKR_OUT_L_M	SPKR_OUT_L_P	VREG_RFRX1	VREG_GP4	VREG_RFRX2	VREG_MSMA	REF_ISET	REF_GND	A
B	VIDEO_OUT	VIDEO_IN	MPP_17	SPKR_IN_R_P	SPKR_IN_R_M	SPKR_IN_L_M	SPKR_IN_L_P	VDD_L_SPKR	VDD_RF1	VDD_ANA	VCOIN	MPP_4	VREG_GP5	B
C	ISNS_P	ISNS_M										KPD_PWR_N	REF_BYN	C
D	USB_CTL_N	CHG_CTL_N		MPP_5	MPP_18	VDD_RF2	VDD_R_SPKR	MPP_3	TCXO_EN	MSM_INT_N		VDD_TCXO	VREG_TCXO	D
E	KPD_DRV_N	VCHG		BAT_FET_N	GND	GND	GND	GND	GND	PS_HOLD		VREG_SYNT	VREG_GP6	E
F	LCD_DRV_N	VBAT		MPP_19	GND	GND	GND	GND	GND	PON_RESET_N		VDD_GP6	VDD_MSME2	F
G	VREG_WLAN	VDD_WLAN		MPP_20	GND	GND	GND	GND	GND	TCXO_OUT		MIC_BIAS	VREG_MSME2	G
H	FLSH_DRV_N	USB_ID		USB_OE_N	GND	GND	GND	GND	GND	SBCK		TCXO_IN	VREG_MSMP	H
J	VREG_5V	MPP_21		USB_DAT	GND	GND	GND	GND	GND	SBST		VDD_MSMP	VREG_GP2	J
K	VSW_5V	MPP_22		USB_SE0	MPP_11	MPP_12	SLEEP_CLK	MPP_9	MPP_10	SBDT/SSBI		VDD_GP2	VREG_MMC	K
L	USB_VBUS	USB_D_P										MPP_7	V_BACKUP	L
M	VREG_USB	USB_D_M	MPP_13	VREG_PA	MPP_16	VREG_MSME2	MPP_1	VREG_MSME1	VREG_MSME	VDD_RUIM	MPP_8	AMUX_OUT	XTAL_IN	M
N	MPP_14	VIB_DRV_N	MPP_15	VSW_PA	MPP_2	VSW_MSME2	VDD_C2_PA	VSW_MSME1	VDD_C1_E	VSW_MSME	VREG_RUIM1	VREG_GP3	XTAL_OUT	N
	1	2	3	4	5	6	7	8	9	10	11	12	13	
		INPUT PWR MGT			GEN HK			IC I/F			Power			
		OUTPUT V REG			USER I/F			MPP			Ground			

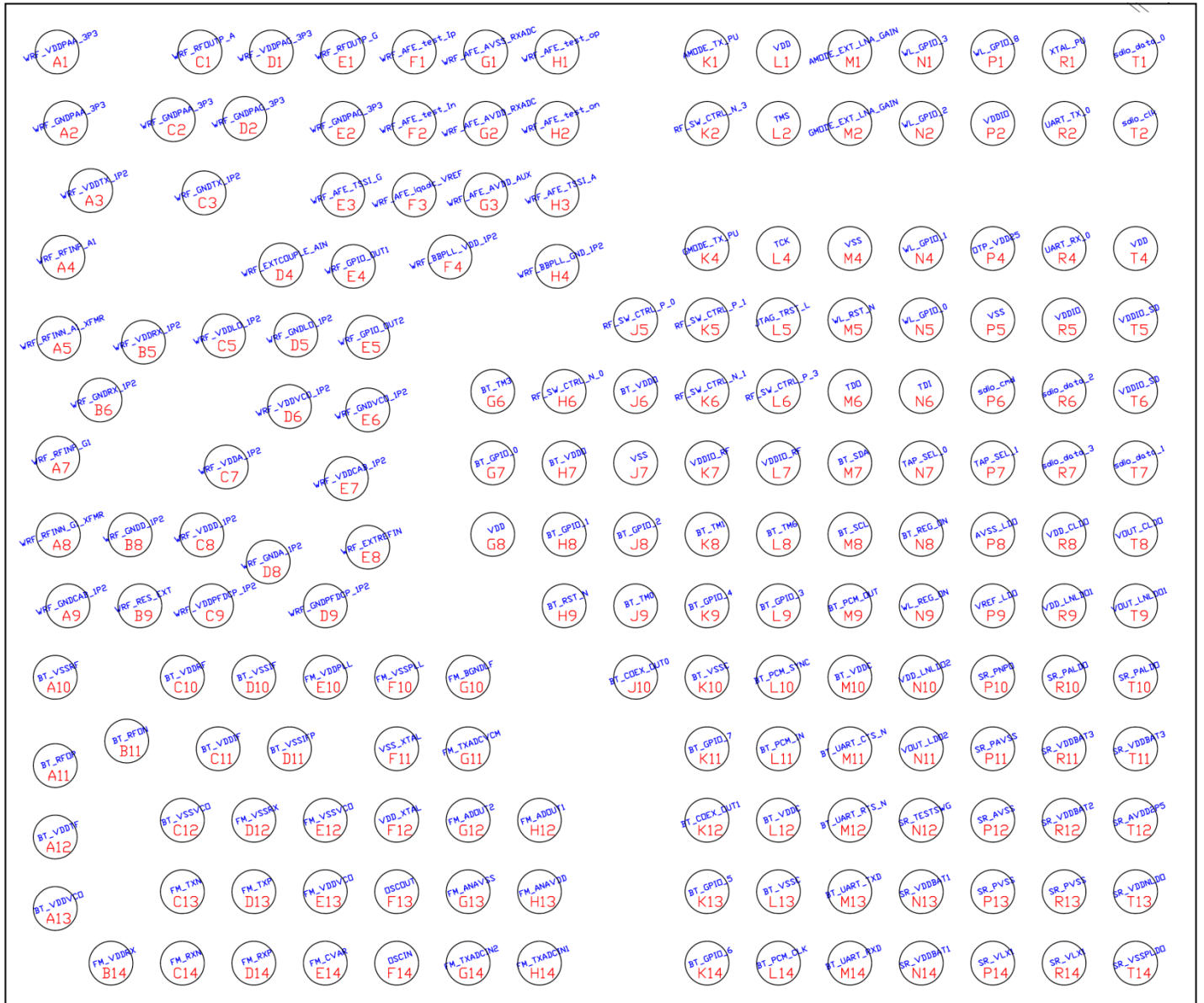
U101 PM7540 pin assignment



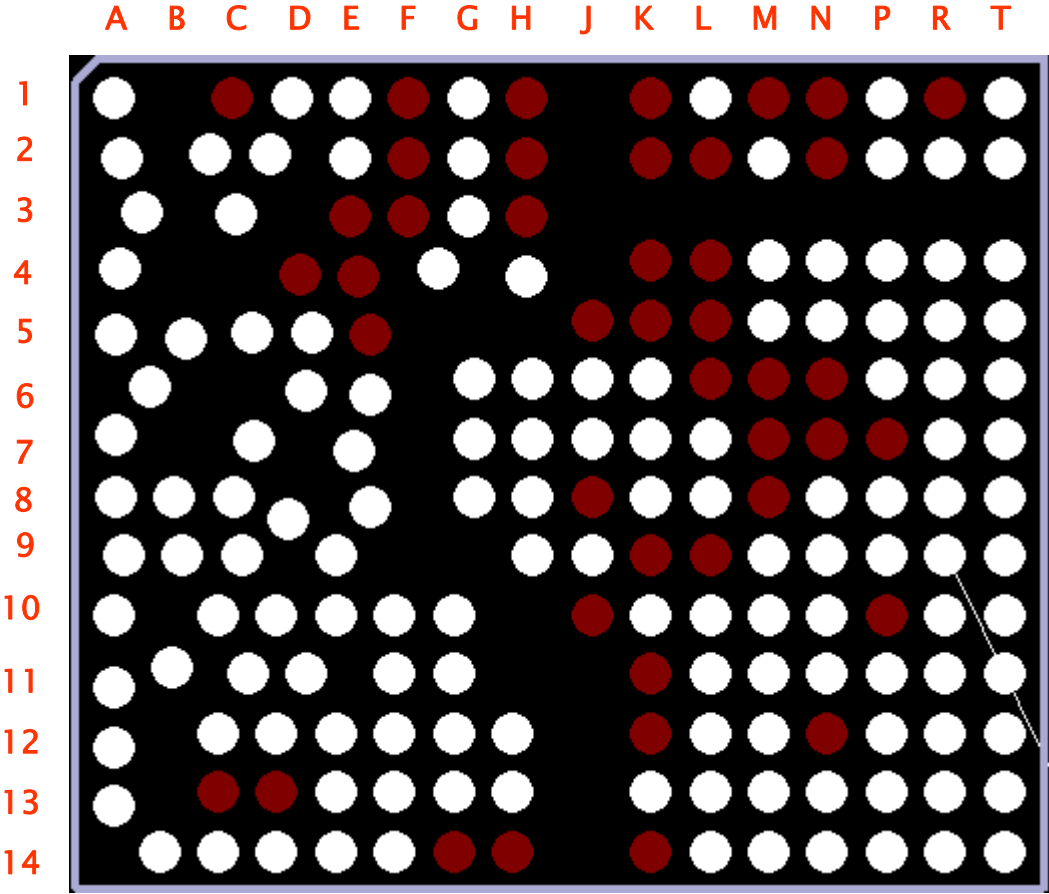
 unused pin

 used pin

U2701 BCM4329 pin assignment



U2701 BCM4329 pin assignment

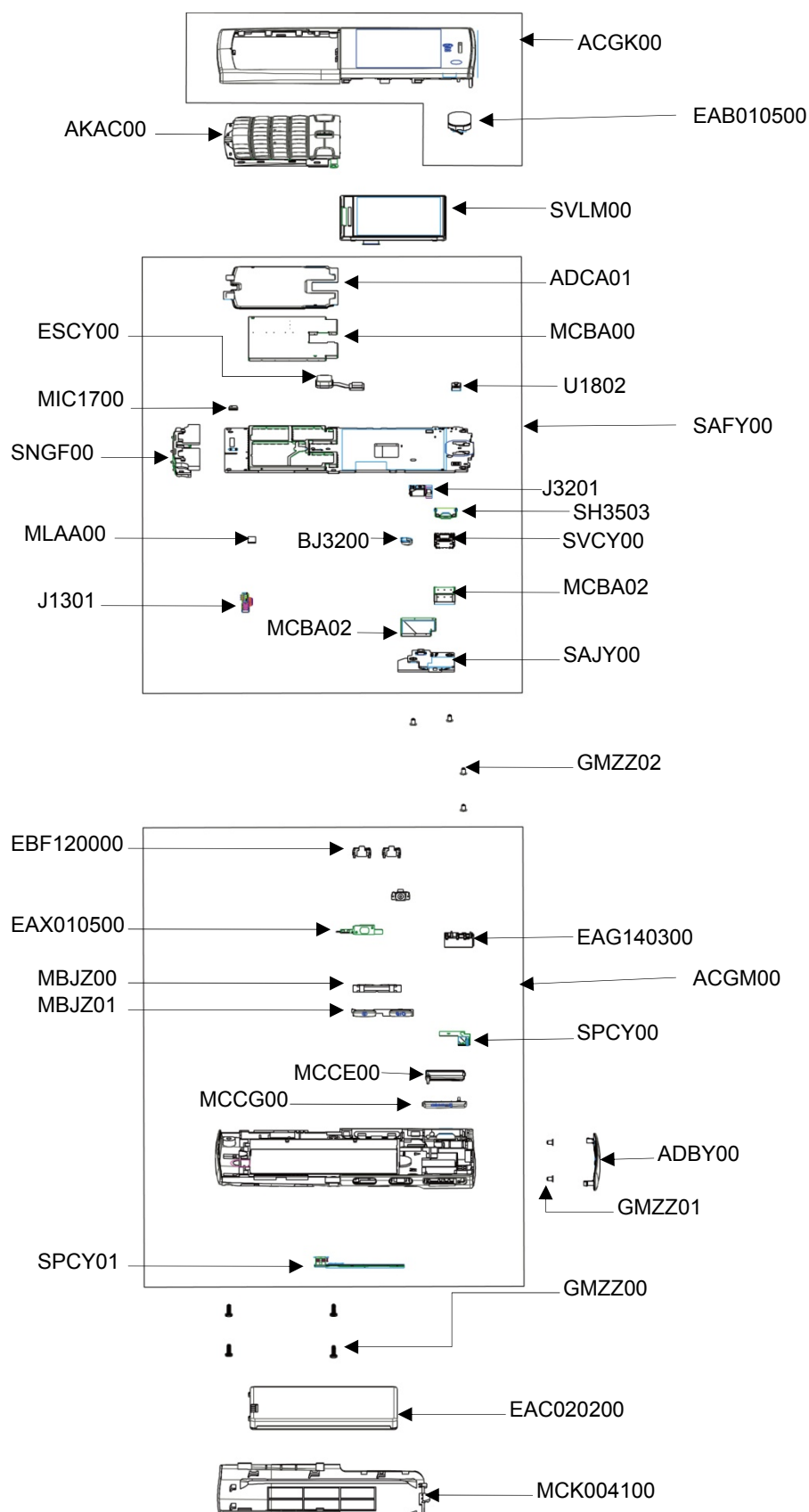


● unused pin
○ used pin

9. EXPLODEDVIEW & REPLACEMENT PART LIST

9.1 Exploded View

LOCATION NO.	DESCRIPTION
EAB010500	SPEAKER, TWO WAY MODE
AKAC00	KEYPAD ASSEMBLY, MAIN
SVLM00	LCD MODULE
ADCA01	DOME ASSEMBLY, METAL
MCBA00	CAN, SHIELD
U1802	CAMERA MODULE
ESCY00	SWITCH TACT (OPTICAL JOSTIC MODULE)
MIC1700	MICROPHONE, CONDENSE
SNGF00	ANTENNA, HELICAL
J3201	MOTOR, DC
SH3503	CAN, SHIELD
SVCY00	CAMERA MODULE
BJ3200	RECHARGEABLE BATTERY, LITHIUM ION (PCB BACKUP BATTERY)
MCBA02	CAN, SHIELD
MCBA01	CAN, SHIELD
MLAA00	LABEL APPROVAL (IMEI)
J1301	CONNECTOR, WAFER (BATTERY I/O CONNECTOR)
SAJY00	PCB ASSEMBLY, SUB (DIM CARD SMT)
GMZZ02	MACHINE SCREW
EBF120000	SWITCH TACT (SIDE BUTTON TACT)
EAG140300	JACK, PHONE
EAX010500	PCB, SIDEKEY (CAMERA SIDE KEY)
MBJZ00	BUTTON
MBJZ01	BUTTON
SPCY00	PCB, FLEXIBLE
MCCE00	CAP, RECEPTACLE
MCCG00	CAP, MULTIMEDIA CARD
ADBY00	DÉCOR ASSEMBLY
GMZZ01	MACHINE SCREW
SPCY01	PCB, FLEXIBLE
GMZZ00	MACHINE SCREW
EAC020200	RECHARGEABLE BATTERY, LITHIUM POLYMER
MCK004100	COVER BATTERY
ACGK00	COVER ASSEMBLY, FRONT
SAFY00	PCB ASSEMBLY, MAIN
ACGM00	COVER ASSEMBLY, REAR



9.2 Replacement parts

L V	LOC#	DESCRIPTION	LG P/N	SPEC
2		Manual Assembly, Oper ation	AMBA0184701	LG-C570g TFBTN ZZ:Without Color LG-C570g manual assy for TFB
2	MCK004100	Cover,Battery	MCJA0124601	COMPLEX LG-C570g TFBTN TN:TITANIUM MOLD, PC LUPOY SC-1004A, , , , ,
2	EAC020200	Rechargeable Battery,Lithium Polymer	SBPP0027401	LGIP-400N-WW-WP 3.7 V,1500 mAh,1 CELL,PRISMATIC,454261 WW LABEL,PRISMATIC,BLACK, WISE POWER
2		Accessory,Data Cable	SGDY0016701	KCA-ET-8-0020 KCA-ET-8-0020 Micro USB, 1.2M KSD CO., LTD
2		Earphone,Stere o	SGEY0003744	EMB-LGE004MSKB 3mW 16OHM 115DB 85HZTO126HZ 1M BLACK 3.5 L TYPE STEREO 4POLE PLUG - CRESYN CO.,LTD
2		Adapters	SSAD0032101	STA-U12MR STA-U12MR,100-240V,5060 Hz,5.0 V,0.7 A,NOM,STA-U12MR,Cableless SUNLIN ELECTRONICS CO.,LTD
2		Adapters	SSAD0032102	STA-U12MS 90Vac~264Vac 5.1V 700mA 5060 NOM NONE NONE - SALCOMP OY
2		Bag,Vinyl	MBAD0005204	COMPLEX LG-LX260 SPRAG ZZ:Without Color -
2		Box,Unit	MBEF0149401	COMPLEX LG-C570g TFOTN ZZ:Without Color BOXTW,LG-C570 STD Unit Box(TR1-1HW)
2		Label	MLAZ0050901	COMPLEX KU990 GBRBK ZZ:Without Color -
2	ACGK00	Cover Assembly,Front	ACGK0170101	LG-C570g TFBTN TN:TITANIUM -
2	ACGM00	Cover Assembly,Rear	ACGM0169101	LG-C570g TFBTN TN:TITANIUM -
3	MCCE00	Cap,Receptacle	MCCE0062601	COMPLEX LG-C570g TFBTN BK:Black MOLD, PC LUPOY SC-1004A, , , , ,
3	MCCG00	Cap,Multimedia Card	MCCG0026001	COMPLEX LG-C570g TFBTN BK:Black MOLD, PC LUPOY SC-1004A, , , , ,

LV	LOC#	DESCRIPTION	LG P/N	SPEC
3	MTAK00	Tape,Camera	MTAK0042601	COMPLEX LG-C570g TFBTN ZZ:Without Color CUTTING, STS, , , , ,
3	MWAE00	Window,Camera	MWAE0066801	COMPLEX LG-C570g TFBTN TR:Transparent CUTTING, PMMA MR 200, , , , ,
3	SPCY00	PCB,Flexible	SPCY0257001	21LQ90A001W LG-C570g TFBTN,FLEXIBLE,1.0,POLYI,.1229 mm,SINGLE Compal Communications Inc.
3	SPCY01	PCB,Flexible	SPCY0257201	P/N: 21LQ90A002W LG-C570g TFBTN,FLEXIBLE,1.0,POLYI,.2 mm,SINGLE Compal Communications Inc.
2	AKAC00	Keypad Assembly,Main	AKAC0020901	LG-C570g TFBTN TN:TITANIUM -
2	EAG140300	Jack,Phone	ENJE0008401	2311000241W ,10, Compal Communications Inc.
2	EBF120000	Switch,Tact	ESCY0008601	2322003081W V,A,HORIZONTAL,G,10C2P, Compal Communications Inc.
2	GMZZ00	Machine Screw	GMZZ0031001	1.6 mm,4.5 mm,MSWR3(BK) ,N ,+ , - , , , ,BH ,+ ,1.6 ,4.5 ,[empty] ,BLACK ,[empty] ,[empty] BH ,+ ,1.6 ,4.5 ,[empty] ,BLACK ,[empty] ,[empty]
2	GMZZ01	Machine Screw	GMZZ0031101	1.6 mm,2.6 mm,MSWR3(FN) ,N ,+ , - , , , ,BH ,+ ,1.6 ,2.6 ,[empty] ,SILVER ,[empty] ,[empty] BH ,+ ,1.6 ,2.6 ,[empty] ,SILVER ,[empty] ,[empty]
2	SAFY00	PCB Assembly,Main	SAFY0387701	LG-C570g TFBTN MAIN 1.0
4	ADCA01	Dome Assembly,Metal	ADCA0121701	LG-C570g TFBTN ZZ:Without Color Metaldome+LGF+PCB KEYPAD ASS'Y
5	MCBA00	Can,Shield	MCBA0090501	COMPLEX LG-C570g TFBTN ZZ:Without Color PRESS, STS, 0.15T, 39.7, 1.25, 54.1,
4	GMZZ01	Machine Screw	GMZZ0031101	1.6 mm,2.6 mm,MSWR3(FN) ,N ,+ , - , , , ,BH ,+ ,1.6 ,2.6 ,[empty] ,SILVER ,[empty] ,[empty] BH ,+ ,1.6 ,2.6 ,[empty] ,SILVER ,[empty] ,[empty]
4	MCBA01	Can,Shield	MCBA0090601	COMPLEX LG-C570g TFBTN ZZ:Without Color PRESS, STS, 0.15, , , ,

LV	LOC#	DESCRIPTION	LG P/N	SPEC
4	MCBA02	Can,Shield	MCBA0097401	COMPLEX LG-C570g TFBTN ZZ:Without Color PRESS, STS, 0.2mm, , , ,
4		Damper	MCQ66466601	CUTTING STS LGC570G.ATFBTN BK:Black -
7		Capacitor,Ceramic,Chip	ECCH0020401	1310551102W pF,2KV,A,B,HD,ETC,ETC,mm,mm Compal Communications Inc.
7		Capacitor,Ceramic,Chip	ECCH0023501	1333044151W pF,100V,A,B,HD,ETC,ETC,mm,mm Compal Communications Inc.
7		Connector,BtoB	ENBY0059501	2308000234W 10,mm,ETC,0.13MM, Compal Communications Inc.
7		Connector,Wafer	ENDY0001101	2304217021W 1P 0.13MM 3R STRAIGHT SCREW BK 2463 A/T657 2304217021W Compal Communications Inc.
4	SNGF00	Antenna,Helical	SNGF0065901	23A1LQ9001W ,dBd,DUAL, Compal Communications Inc.
4	SVCY00	Camera Module	SVCY0028101	7651CB6002W CCD,VGA, Compal Communications Inc.
4	SVLM00	LCD Module	SVLM0041901	76300024E2W Main,ETC,ETC,ETC, Compal Communications Inc.
5		Diode,TVS	EAH61412901	2050402004W 0V 0 0V 0A 0W 1-1F1A BK 10P 1 Compal Communications Inc.
5		Diode,Switching	EDSY0019701	1720072001W ,V,A,ETC, Compal Communications Inc.
5		Diode,TVS	EDTY0011201	2012002331W ,V,W,ETC, Compal Communications Inc.
5		Diode,TVS	EDTY0011301	2012002931W ,V,W,ETC, Compal Communications Inc.
5		Diode,TVS	EDTY0012601	2050005002W ,V,W,ETC, Compal Communications Inc.

LV	LOC#	DESCRIPTION	LG P/N	SPEC
5		Diode,TVS	EDTY0012701	2091431001W ,V,W,ETC, Compal Communications Inc.
5		Connector,BtoB	ENBY0059401	2308000233W 10,mm,ETC,0.13MM, Compal Communications Inc.
5		Connector,BtoB	ENBY0059601	2308000373W 10,mm,ETC,0.13MM, Compal Communications Inc.
5		Connector,I/O	ENEY0004601	2334503182W 10,0.13MM, Compal Communications Inc.
5	J1301	Connector,Wafer	ENKY0003401	230300003DW 10,mm,ETC,0.13MM,1R,BEIGE, Compal Communications Inc.
5		Connector,I/O	ENRY0009901	2306062931W 10,mm,ETC,0.13MM, Compal Communications Inc.
5		Connector,I/O	ENRY0011701	2336003051W 10,mm,ETC,0.30MM, Compal Communications Inc.
5		Card Socket	ENSY0026201	2325000881W 10,ETC,mm, Compal Communications Inc.
5		Connector,RF	ENWY0009101	2302081301W ,CONN,dB,0.13MM,RF ADAPTER, Compal Communications Inc.
5		IC,RF Amplifier	EUSY0402701	04F0823601W ,10 ,ETC , , , ; IC,Inverter Compal Communications Inc.
5		IC,Digital Signal Processors	EUSY0426901	0104329001C 10 10 10 1.5KBYTE 1.5KBYTE 10-Lead Micro PAK R/TP 10P only used ODM model(Kellogg) Compal Communications Inc.
5		IC,TTL	EUSY0427701	0440132304W ,10 ,ETC , , , ; IC,TTL Compal Communications Inc.
5		IC,Actuator Driver	EUSY0428101	04F0240001W ,10 ,ETC , , , ; IC,Actuator Driver Compal Communications Inc.
5		IC,A/D Converter	EUSY0428201	04G0971801W ,10 ,ETC , , , ; IC,A/D Converter Compal Communications Inc.

LV	LOC#	DESCRIPTION	LG P/N	SPEC
5		Crystal	EXXY0027601	1620037A21W MHz,PPM,pF,ohm,ETC, Compal Communications Inc.
5	SH3503	Can,Shield	MCBA0097601	COMPLEX LG-C570g TFBTN ZZ:Without Color PRESS, STS, 0.45mm, , , ,
5		Contact	MCIZ0008801	COMPLEX LG-C570g TFBTN ZZ:Without Color PRESS, STS, 0.2mm, , , ,
5		Contact	MCIZ0008901	COMPLEX LG-C570g TFBTN ZZ:Without Color PRESS, STS, 0.2mm, , , ,
5		Filter,Bead	SFBH0011601	1115601202W ohm,ETC, Compal Communications Inc.
5		Filter,EMI/Power	SFEY0017201	2091624001W SMD,Filter,LCR Compal Communications Inc.
5		Filter,EMI/Power	SFEY0017301	2093118002W BOX,Filter,LCR Compal Communications Inc.
5		Filter,Saw	SFSY0039501	2021575026W ETC, Compal Communications Inc.
5		Filter,Saw	SFSY0040101	2022450017W MHz,ETC, Compal Communications Inc.
5	J3201	Motor,DC	SJMY0010701	3933358001W V,A,12V, Compal Communications Inc.
5		Diode,Switching	EDSY0019401	1720301002W ,V,A,ETC, Compal Communications Inc.
5		Diode,Switching	EDSY0019701	1720072001W ,V,A,ETC, Compal Communications Inc.
5		Diode,TVS	EDTY0011001	2010000432W ,V,W,ETC, Compal Communications Inc.
5		Diode,TVS	EDTY0011201	2012002331W ,V,W,ETC, Compal Communications Inc.

LV	LOC#	DESCRIPTION	LG P/N	SPEC
5		Diode,TVS	EDTY0011301	2012002931W ,V,W,ETC, Compal Communications Inc.
5		Diode,TVS	EDTY0012601	2050005002W ,V,W,ETC, Compal Communications Inc.
5		Connector,BtoB	ENBY0059701	2308122231W 10,mm,ETC,0.13MM, Compal Communications Inc.
5		TR,Bipolar	EQBP0011601	1813520003W ,W,ETC, Compal Communications Inc.
5		FET	EQFP0010901	1820233304W ,W,V,A,ETC,MOSFET, Compal Communications Inc.
5		Filter,EMI/Power	ERNC0000201	1910214211W ohm,ohm,pF,10,ETC,ETC, Compal Communications Inc.
5		Filter,EMI/Power	ERNC0000301	1910806102W ohm,ohm,pF,10,AXI,ETC, Compal Communications Inc.
5		IC,Clock Recovery	EUSY0401201	0307006002W ,10,ETC,IC,BufferIC,Buffer Compal Communications Inc.
5		IC,Transceiver	EUSY0401301	0410628506C ,10 ,ETC , , ,IC,Tx/Rx Compal Communications Inc.
5		IC,RF Amplifier	EUSY0401601	0427718701C ,10 ,ETC , , ,IC,TTL Compal Communications Inc.
5		IC,RF Amplifier	EUSY0401901	0427718801C ,10,ETC,IC,TTLIC,TTL Compal Communications Inc.
5		IC,PMIC	EUSY0402201	0480754006C ,10,ETC,IC,TTLIC,TTL Compal Communications Inc.
5		IC,Analog Switch	EUSY0402301	04B0455001W ,10,ETC,IC,Tx/RxIC,Tx/Rx Compal Communications Inc.
5		IC,Analog Switch	EUSY0402401	04D0086001W ,10,ETC,IC,Tx/RxIC,Tx/Rx Compal Communications Inc.

LV	LOC#	DESCRIPTION	LG P/N	SPEC
5		IC,CODEC	EUSY0427001	0107227005C 10VTO10V 10W 10-Lead Micro PAK R/TP 10P only used ODM model(Kellogg) Compal Communications Inc.
5		IC,Charger	EUSY0427101	0205242002C 10 10 10W 10-Lead Micro PAK R/TP 10P only used ODM model(Kellogg) Compal Communications Inc.
5		IC,Buffer	EUSY0427201	0307748002W ,10 ,ETC , , ,IC,Buffer Compal Communications Inc.
5		IC,Analog Switch	EUSY0427301	0308860002W ,10 ,ETC , , ,IC,Analog Switch Compal Communications Inc.
5		IC,DMB	EUSY0427501	0427733601C 10VTO10V 10W 10-Lead Micro PAK R/TP 10P only used ODM model(Kellogg) Compal Communications Inc.
5		IC,Tx/Rx	EUSY0427601	0440010403W ,10 ,ETC , , ,IC,Tx/Rx Compal Communications Inc.
5		IC,ASIC	EUSY0427801	0481704301W 10 10M 10 10-Lead Micro PAK P/TR 10P ODM part Compal Communications Inc.
5		IC,A/D Converter	EUSY0428001	0490205101W ,10 ,ETC , , ,IC,A/D Converter Compal Communications Inc.
5		Filter,Multiplexer	EXSV0001501	1613088001W GW550h VIVBK for ODM Model Compal Communications Inc.
5		Crystal	EXXY0026601	1623276339W MHz,PPM,pF,ohm,ETC, Compal Communications Inc.
5		Coupler,RF Directional	SCBY0000201	1000510423W dB,dB,dB,ETC, Compal Communications Inc.
5		Coupler,RF Directional	SCBY0000301	1000810422W dB,dB,dB,ETC, Compal Communications Inc.
5		Filter,Duplexer,PC S	SDPY0004901	2060188002W MHz,MHz,dB,dB,dB,dB,AXI, Compal Communications Inc.
5		Filter,Duplexer,PC S	SDPY0005301	2060836011W MHz,MHz,dB,dB,dB,dB,ETC, Compal Communications Inc.

LV	LOC#	DESCRIPTION	LG P/N	SPEC
5		Filter,Bead	SFBH0011401	1101608105W ohm,ETC, Compal Communications Inc.
5		Filter,Bead	SFBH0011501	1115182202W ohm,ETC, Compal Communications Inc.
5		Filter,EMI/Power	SFEY0017101	2091282001W LG-C570g TFBTN Compal Communications Inc.
5		Filter,Saw	SFSY0039401	2020836012W ETC, Compal Communications Inc.
5		Filter,Saw	SFSY0039501	2021575026W ETC, Compal Communications Inc.
5		Filter,Saw	SFSY0039601	2021880001W MHz,ETC, Compal Communications Inc.
5		Filter,Saw	SFSY0040001	2022140008W ETC, Compal Communications Inc.
5		Filter,Saw	SFSY0042301	2021960020W MHz,ETC, Compal Communications Inc.
5	MIC1700	Microphone,Condenser	SUMY0013101	2220414501W UNIT,dB, Compal Communications Inc.
5	U1802	Camera Module	SVCY0028201	7651LQ9001W 7651LQ9001W 7651LQ9001W Compal Communications Inc.
2	EAX010500	PCB,Sidekey	SPKY0097201	21LQ905101W FR-4 Single 2 0.2 - Compal Communications Inc.
2	EAB010500	Speaker,Two Way Mode	SUVT0006501	2250181001W ohm,ohm,dB,dB,mm, Compal Communications Inc.
	MLAA00	LABEL APPROVAL (IMEI)	MLAA0062301	LABEL APPROVAL (IMEI)
3	MBJZ00	Button	MBJZ0045301	MOLD PC LUPOY HP-5004 LG-C570g TFBTN BK:Black MOLD, PC LUPOY SC-1004A, , , , ,

LV	LOC#	DESCRIPTION	LG P/N	SPEC
3	MBJZ01	Button	MBJZ0045401	COMPLEX LG-C570g TFBTN BK:Black MOLD, PC LUPOY SC-1004A, , , , ,
2	ADBY00	Decor Assembly	ADBY0022001	LG-C570g TFBTN BK:Black Upper Case DECO+adhesive
	ESCY00	JOG SW	ESCY0008401	COJ-P6BL-LQ90 CRUCIALTEC
4	SAJY00	PCB Assembly,Sub	SAJY0052001	LG-C570g TFBTN SUB 1.0
5	BJ3200	Rechargeable Battery,Lithium Ion	SBAL0001701	15R0407001W V,mAh,CELL,1/2A,ALLTEL SILVER, Compal Communications Inc.

10. SERVICE ENGINEERING TOOL

10.1 Instruction

The CCI Service Engineering (CSE) is a PC based automated phase and test solution for the service community. It allows users to perform the listed routines:

1. Hardware diagnosis
2. Read/Write Handset Specific Settings
3. RF Phasing
4. Stand Alone Tool for Current Model

Abbreviations

UI	User Interface
CSE	CCI Service Engineering
SAT	Stand Alone Tool
FTM	Factory Test Mode
DL	Download (Flashing)
DM tool	Download Tool

10.2 CSE Installation

10.2.1 Software/Hardware Requirement

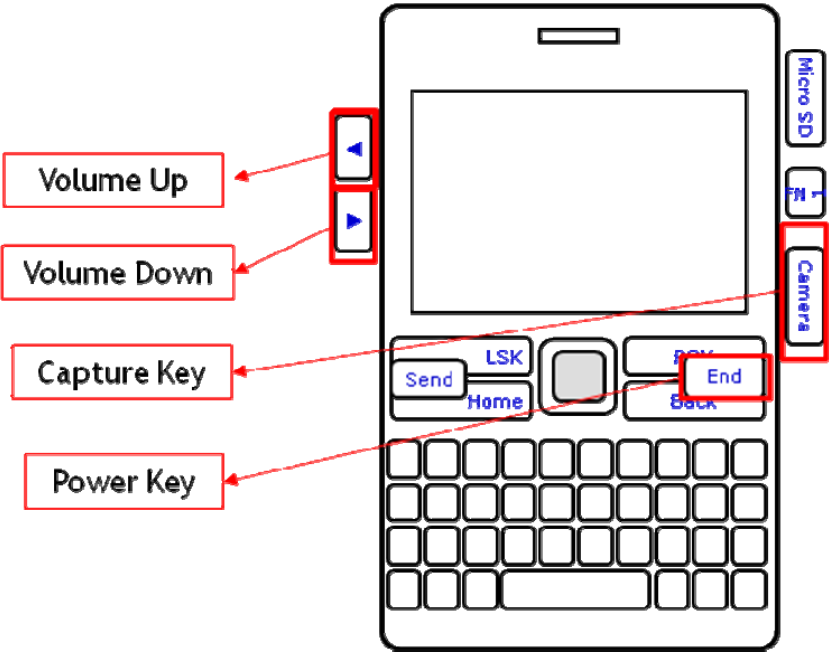
1. CSE installer (ex. CSE.msi).
2. PC installed with Microsoft Windows XP or Microsoft Windows SP2.
3. Microsoft .Net Framework 2.0.
4. MSXML 4.0 Service Pack 2.

10.2.2 Installation

1. Execute CSE.msi.
2. Follow Windows' instructions to complete the installation.

10.3 Phone Mode

The relevant phone keys to enter each phone mode are shown as the following:



	Phone Key 1	Phone Key 2
FTM mode	Capture	Volume Down
DL mode	Volume Up	Volume Down

Table 9-1. Phone Keys to enter each mode when power the phone on.

As the corresponding keys shown in Figure 19, to enter a mode please follow below steps:

- 1.Unplug USB Cable, Power off the phone and remove the battery.
- 2.Wait for more than 3 seconds, then put on battery.
- 3.Press and hold both *Phone Key 1* and *Phone Key 2* in **Table 4** for the dedicated mode to be entered.
- 4.Press “Power” key to power on phone.
- 5.After Phone is power on and enter the dedicated mode, release all pressed keys.
- 6.Plug in USB Cable.

10.4 Driver Installation

10.4.1 Software/Hardware Requirement

Before the installation, the following Software/Hardware should be prepared.

1. USB Driver installer (ex. USB Driver V2.0.4).
2. Note: USB Driver is not part of CSE package. Please contact responsible person to get the latest version of USB Driver.
3. The phone and the battery.
4. USB cable.
5. PC installed with Microsoft Windows XP SP2 or above.

10.4.2 Installation

The installation steps are as the following :

1. Set the phone to FTM/DL mode [9.3 Phone Mode] for the installation of FTM/DL driver.
2. Plug the USB cable into the phone and PC. In a few seconds, PC shows Qualcomm WinMoblie Diagnostics 3200 was found.



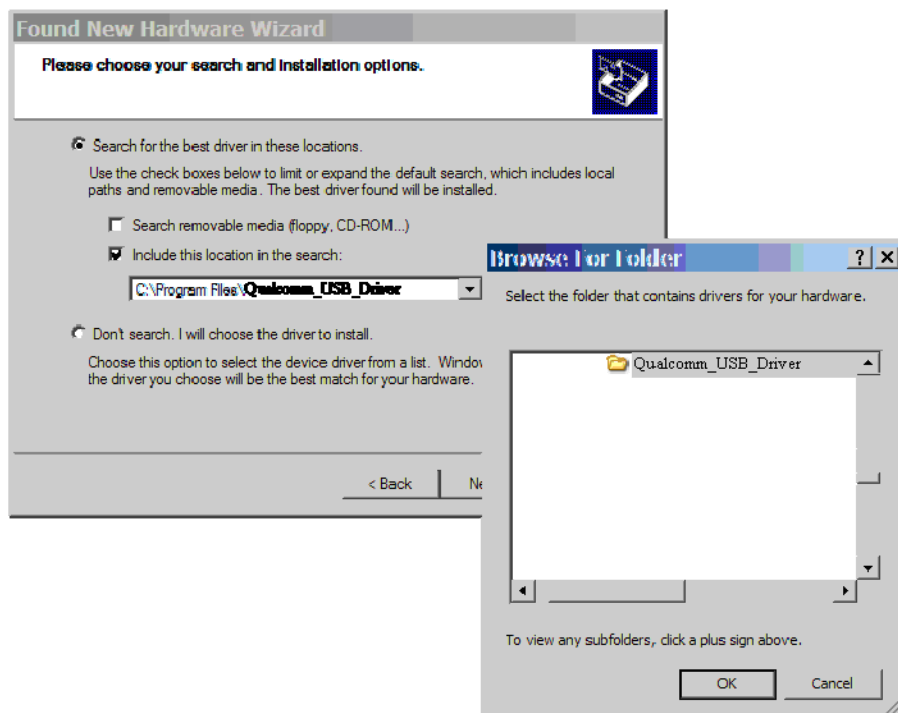
3. Click the message prompted by windows to install USB driver.
4. PC asked for drivers prompted. Select “No, not this time” & press Next.



5. Select “Install from a list or specific location (Advanced)” & press Next.



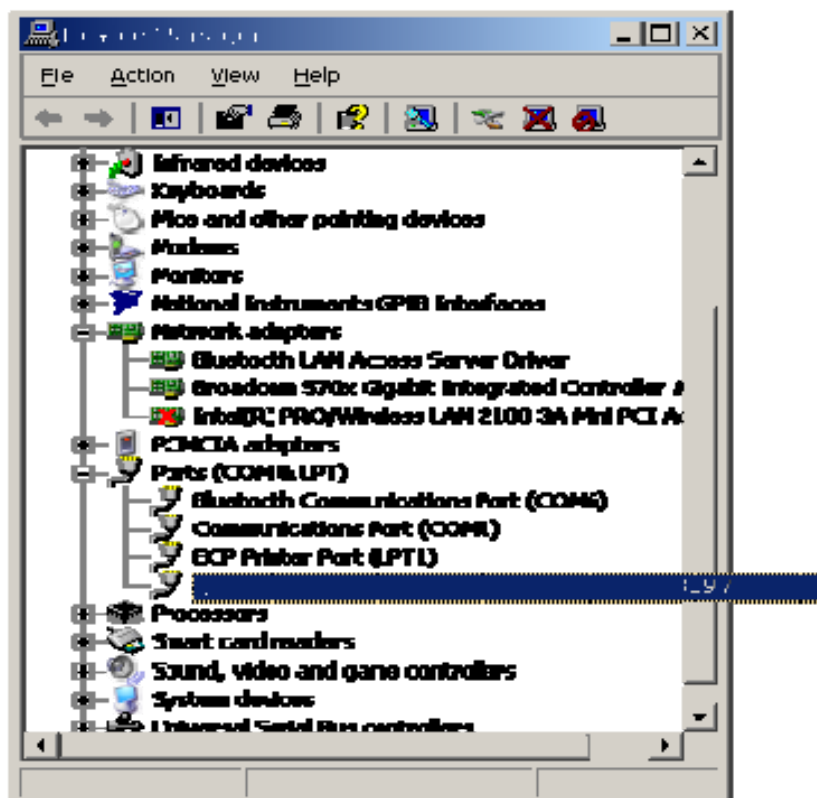
6. Select “Search for best drivers ...” & Browse to select the folder of Qualcomm USB Driver (ex. C:\Program Files\Qualcomm_USB_Driver_v2.0.50). & press Next.



7. The installation is finished & press “Finish” to close the Wizard.



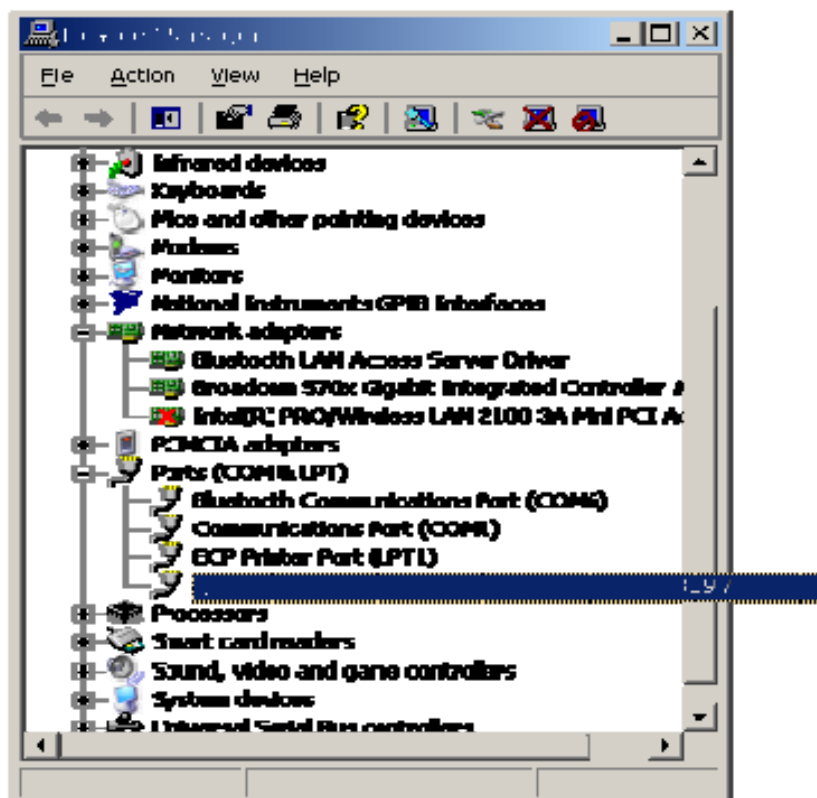
8. Open Device Manger and check whether Qualcomm Diagnostics Interface is installed successfully with the corresponding COM port.



7. The installation is finished & press “Finish” to close the Wizard.



8. Open Device Manger and check whether Qualcomm Diagnostics Interface is installed successfully with the corresponding COM port.



11. SERVICE ENGINEERING OPERATIONS

11.1 User Interface

The CSE(CCI Service Engineering) UI is as below:

- ◆Field 1 : Used for Model selection that you can choose the model you want to test.
- ◆Field 2 : Here the phone information is shown for the model selected. The IMEI field shows the IMEI number of the phone connected after the pressing of “Detect” button. Note that this operation could only be done for FTM mode phone.
- ◆Field 3 : Indicates current status for CSE
 - “Testing” means CSE is perform certain operations or in testing,
 - “PASS” means all tests are successful.
 - “Fail” stands for at least one of the test items is failed.
- ◆Field 4 : Function groups, it divides into
 - “HW Diagnostic” includes items related with hardware or peripherals.
 - “MEI Read/Writ” includes read & write IMEI number and Read SW Version
 - “SIM Unlock” includes read SIM Unlock status & Unlock SIM Lock password.
 - “Misc” includes Log setting and package information
- ◆Field 5 : Here is a list of the test items that are belonging to the selected function group. You can check the desired items for testing.
- ◆Field 6 : Execute the tests.
- ◆Field 7 : Here is a list of test results for all selected items.
- ◆Field 8 : Click it, it will connect the printer then print the ‘Test Result’
- ◆Field 9 : Clear the content of Field 7

11.2 Initial Operations

Before starting CSE tool, USB driver for FTM mode should be installed on your PC. Afterwards, connect the phone to PC by USB cable while the phone set in FTM mode [Appendix A. Set Phone Mode], and execute CSE tool.

For the execution of each function group, the model selection must be done in the group box “Select Model” with the current model of the phone. Only after these steps can we start to use each function group.

To check the connection, click “Detect” button in the group box “Phone information”, the IMEI number of the current connected phone will be gotten in the inline editor labeled “IMEI”.

11.2.1 Select Model and Detect IMEI

1. Set the phone to FTM mode].
2. Connect the phone to PC by USB cable.
3. Select the phone Model in the group box “Select Model” [Figure 2].

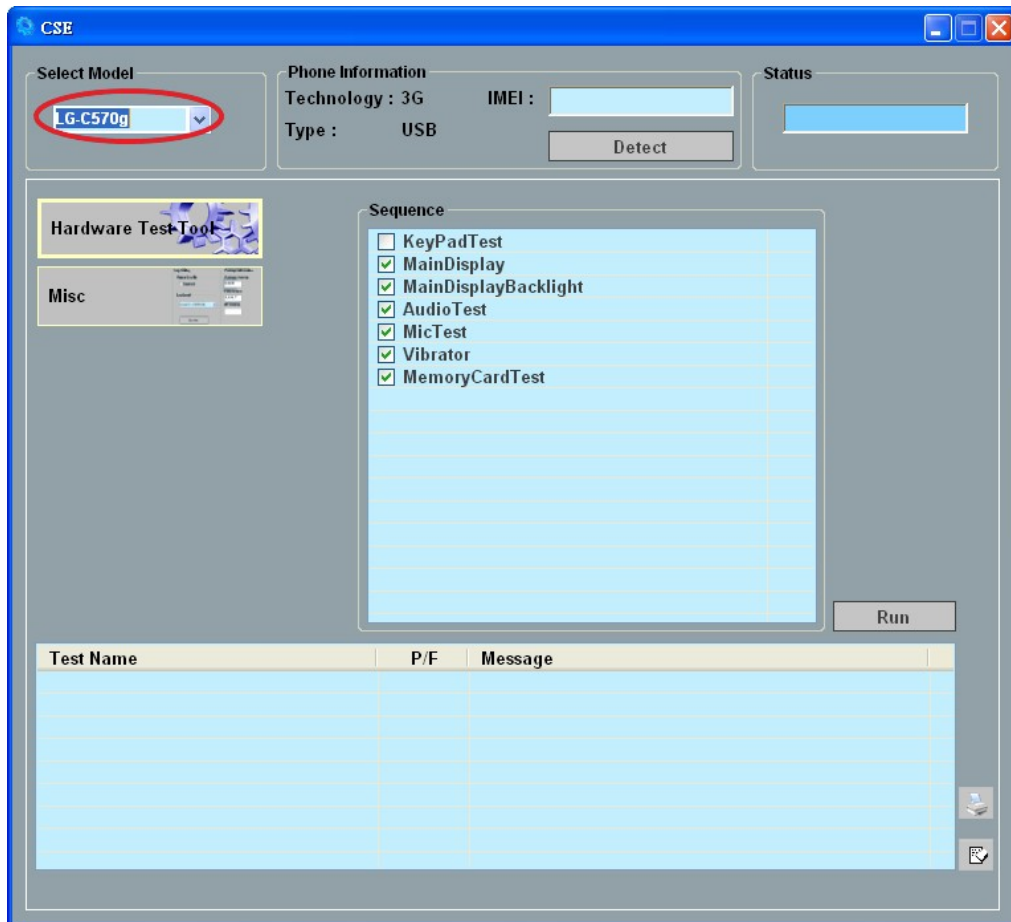
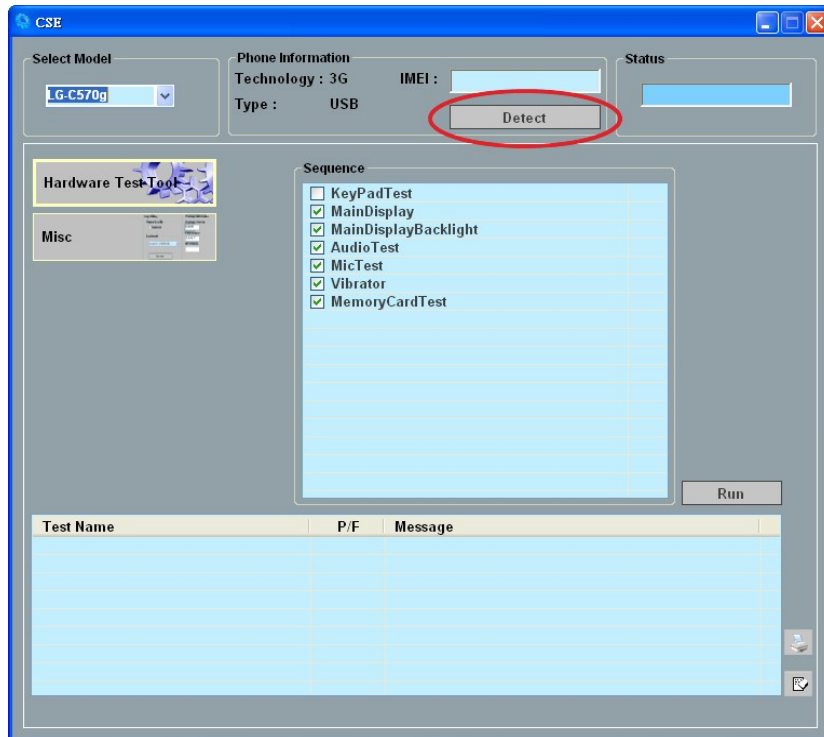


Figure 2 Model Selection

4. Click the “Detect” button [Figure 3].



5. The IMEI number will appear in the inline editor of the group box “Phone information” if there is a successful connection. Meanwhile, the editor in the group box “Status” will show “Pass” [Figure 4].

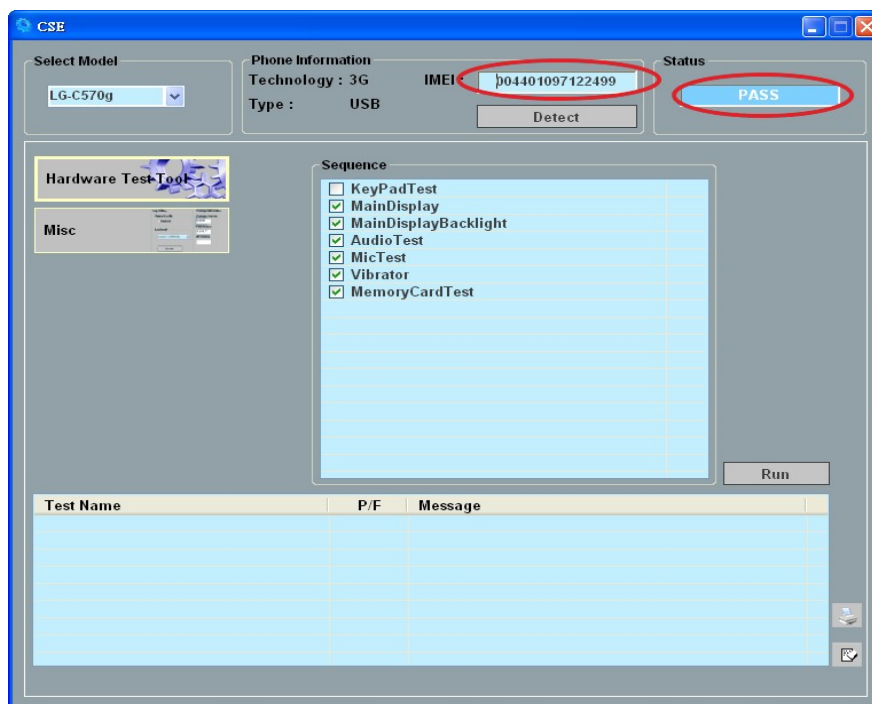


Figure 4 IMEI after a successful connection

11.3 Hardware Test

After model selection [9.3 Phone Mode], the test items can be shown in the group box “Sequence” by selecting the “HW Diagnostic” button in the function group [Figure 5].

Check the test items to be tested in the group box “Sequence” and press the button “Run” to execute the test sequence. Next, follow the instructions prompted on the screen until the end of the process. The test result will be shown in the window at the bottom of the screen.

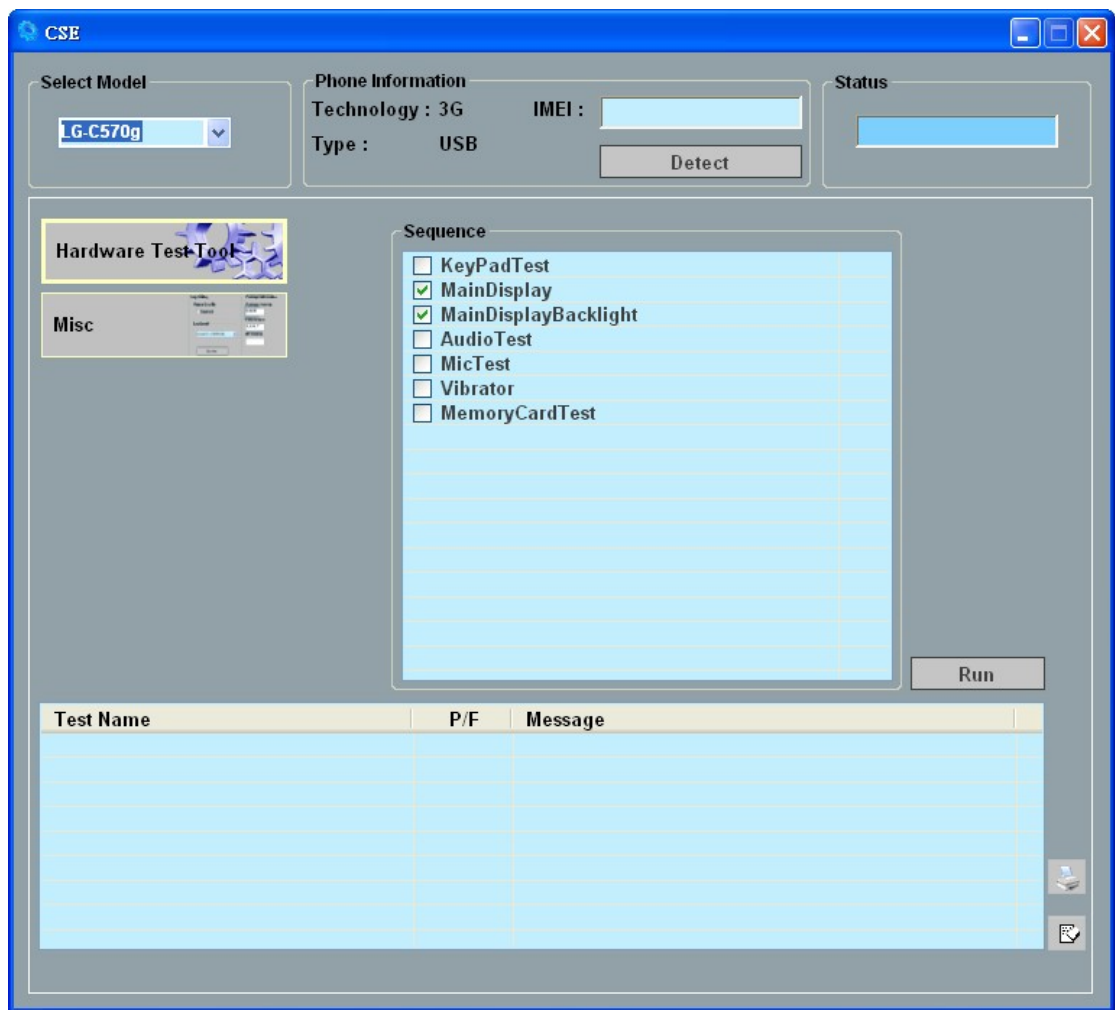


Figure 5. CSE HW Diagnostic UI.

The descriptions for each test item are listed as the following table.

Test Item	Description
KeyPadTest	Test all keys on the handset.
MainDisplay	Test handset LCM.
MainDisplayBacklight	Test backlight of handset's LCM.
AudioTest	Test speaker on the handset
MicTest	Test microphone on the handset
Vibrator	Test handset's vibrator.
Memory Card Test	Test the handset's memory read/write function.

Table 1 Test Item Description

11.3.1 Perform “MainDisplay” and “Vibrator” tests.

1. Check MainDisplay and Vibrator items in the group box “Sequence” [Figure 6].

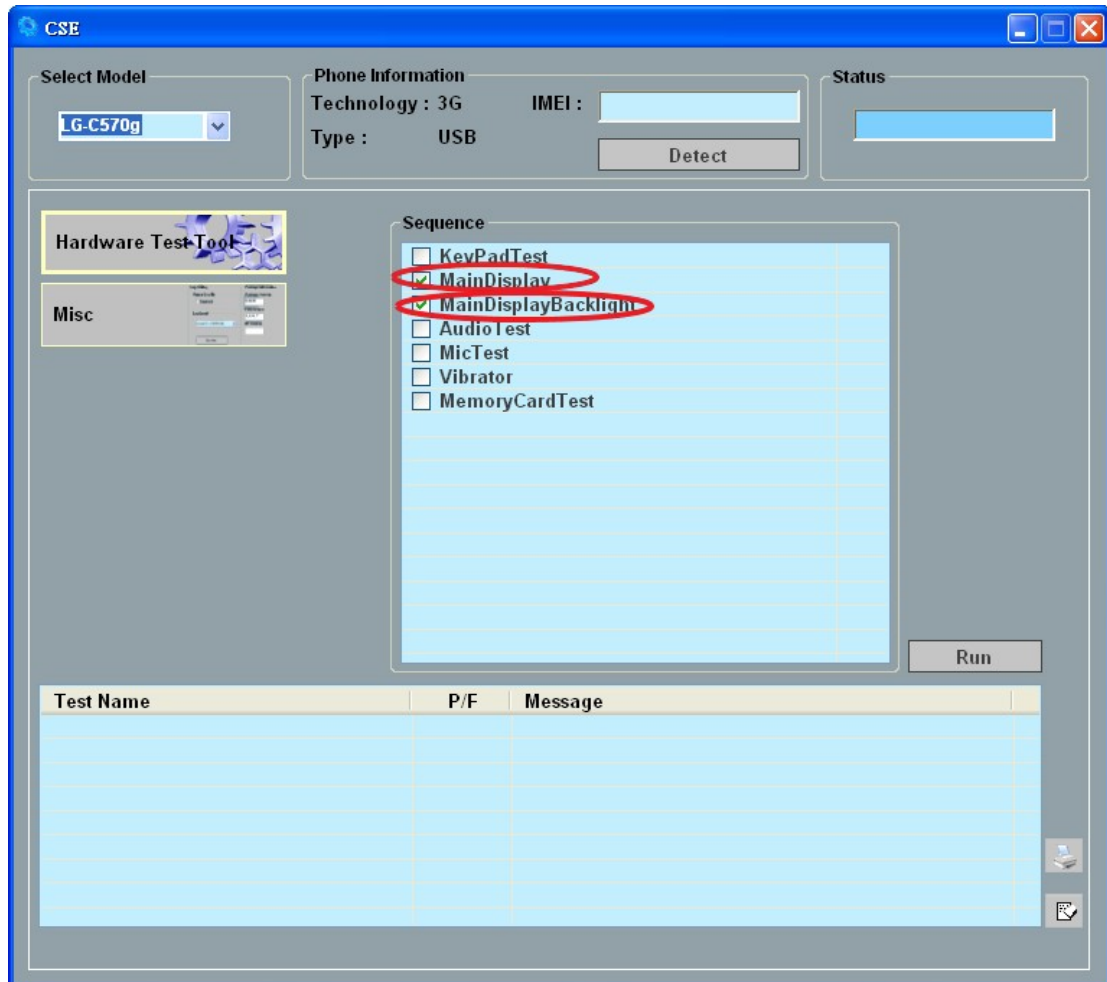


Figure 6 test selection in HW

2. Press the button “Run” to start the tests [Figure 7].

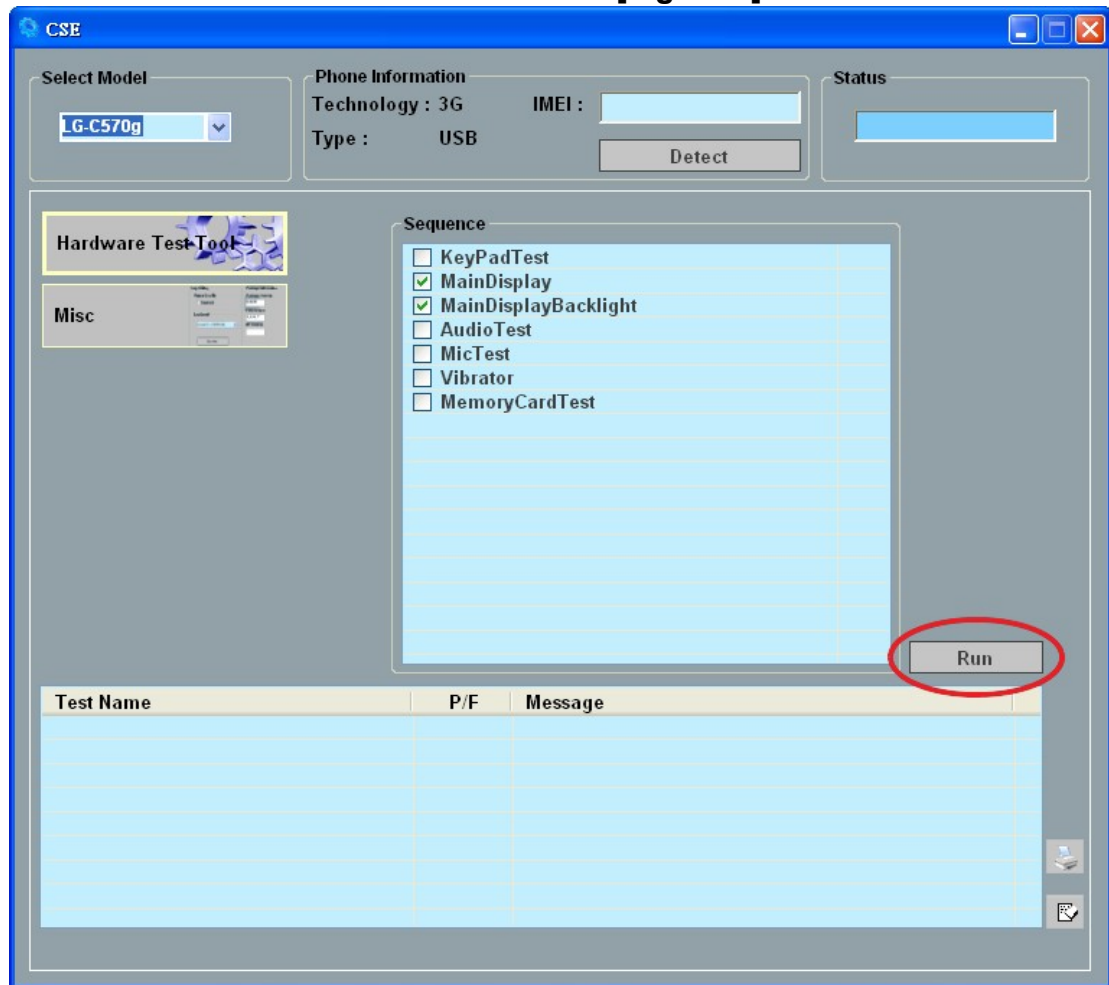


Figure 7. Click Run button to diagnose HW.

3. The corresponding messages [Figure 8] will be prompted in turn. According to the phone's response, click the button on the prompted window.

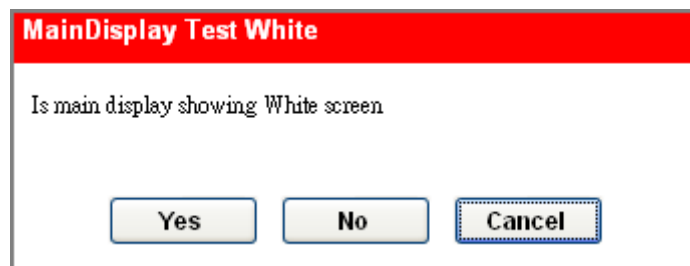


Figure 8. Prompted messages of HW tests

4. The result of each test will be shown in the bottom list. In the P/F column, “P” indicates the test of the name in the column “TestName” passes. Otherwise, “F” will be shown. The final result is represented by HardwareDiagnosticTest as its test name [Figure 9].

The screenshot shows the CSE Hardware Test Tool interface. At the top, there's a 'Select Model' dropdown set to 'LG-C570g'. To the right, 'Phone Information' shows 'Technology : 3G', 'IMEI : 004401097122499', and 'Type : USB'. A 'Detect' button is next to the IMEI field. On the far right, the 'Status' is 'PASS'. Below this, there's a 'Hardware Test Tool' section with a 'Misc' tab. The 'Sequence' section contains a list of tests with checkboxes: 'KeyPadTest' (unchecked), 'MainDisplay' (checked), 'MainDisplayBacklight' (checked), 'AudioTest' (unchecked), 'MicTest' (unchecked), 'Vibrator' (unchecked), and 'MemoryCardTest' (unchecked). A 'Run' button is at the bottom right of the sequence list. At the bottom, a table displays the test results.

Test Name	P/F	Message
MainDisplay Test-Red	P	
MainDisplay Test-Green	P	
MainDisplay Test-Blue	P	
MainDisplayBacklight Test-OFF	P	
MainDisplayBacklight Test-LOW	P	
MainDisplayBacklight Test-MEIDIUM	P	
MainDisplayBacklight Test-HIGH	P	
HardwareDiagnosticTest	P	

Figure 9 Results of HW tests.

The first column in the “Cable Loss Table” lists all the available bands, with each band’s channels (TxCH and RxCH) and cable losses (in dB) in its row. Each channel’s cable loss is shown right to it. For convenience, the checking/unchecking of all the band entries can be done by checking/unchecking of the first column entry “All”.

When there are some band entries selected, the button “Calibration” and “Call Test” will appear in the UI [Figure 17]. Therefore, RF test could only be processed with at least one band entries selected.

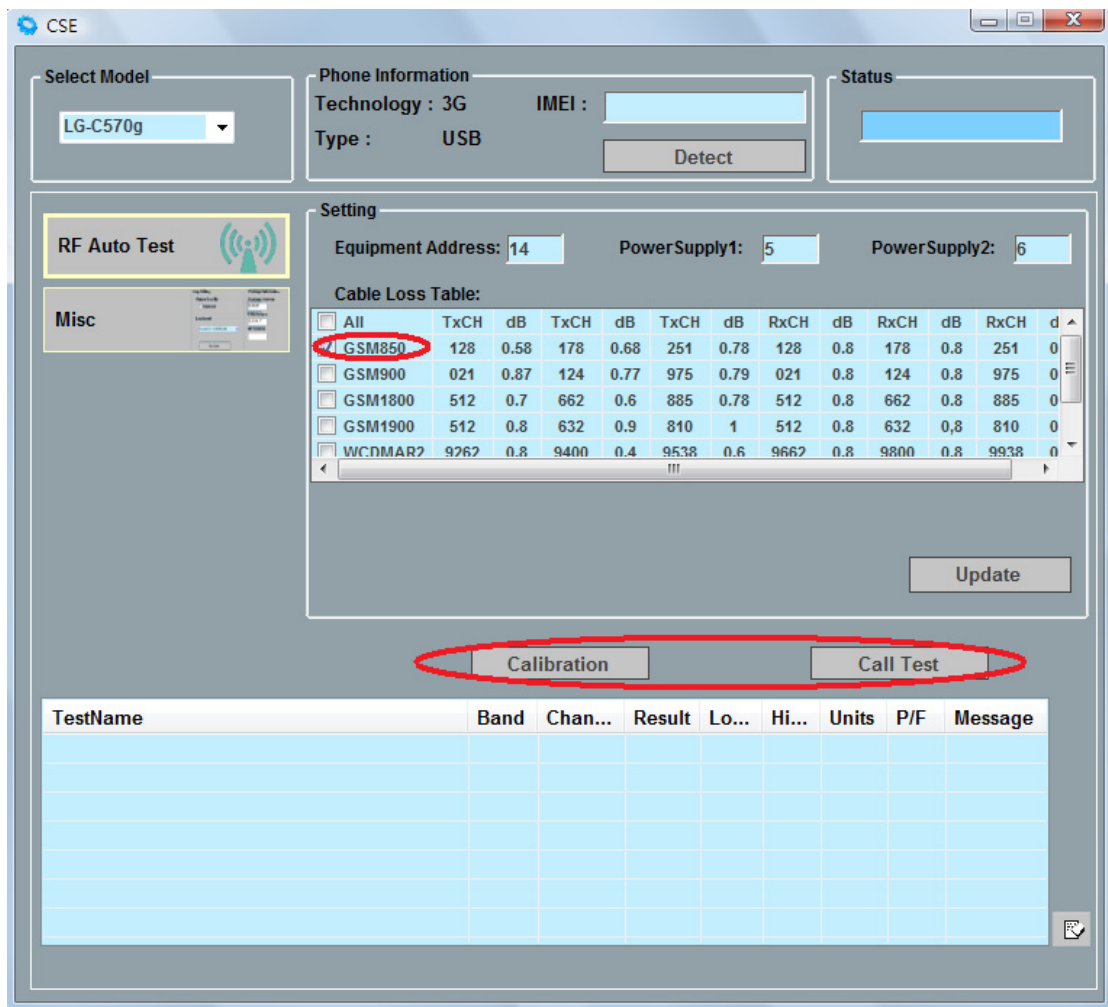


Figure 17. Calibration and Call Test buttons in RF UI.

To modify the cable loss, double click the value of the cable loss wanted to be modified and key its value [Figure 18]. Next, click the button “Update” at the bottom left of the group box “Setting” to activate the assigned value [Figure 19]. Note that the new cable loss value will be ineffective without the button “Update” clicked.

The screenshot shows the CSE software interface. At the top, there's a 'Select Model' dropdown set to 'LG-C570g'. Below it, 'Phone Information' shows 'Technology : 3G' and 'Type : USB'. A 'Detect' button is next to the 'IMEI' field. To the right is a 'Status' field. In the middle-left, there's a 'Setting' group box containing 'RF Auto Test' (with a signal icon), 'Misc', and a 'Cable Loss Table'. The 'Cable Loss Table' is a table with columns for technology, band, channel, and various loss values. The value '0.8' in the 'WCDMAR2' row is circled in red. Below the table is an 'Update' button. At the bottom, there's a large table with columns: TestName, Band, Chan..., Result, Lo..., Hi..., Units, P/F, and Message.

Technology	Band	Chan...	Result	Lo...	Hi...	Units	P/F	Message

Figure 18. Cable Loss Slot Modification.

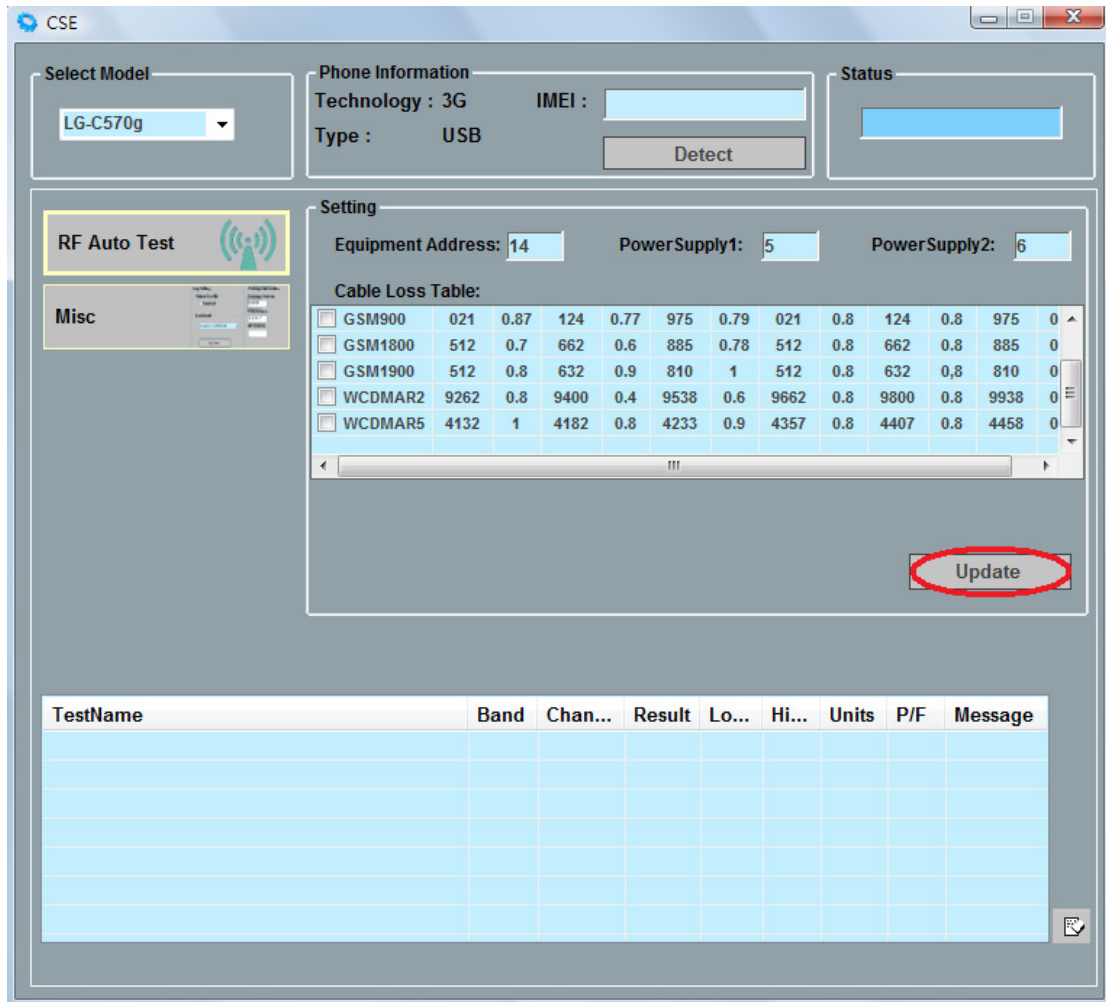


Figure 19. Activate new cable loss value by “Update” button.

11.5 CSE_LQ90_RF_Configuration

After model selection [Appendix A. Set Phone Mode], the feature items can be shown in a list by selecting the “RF Configuration” button in the function group [Figure 10].

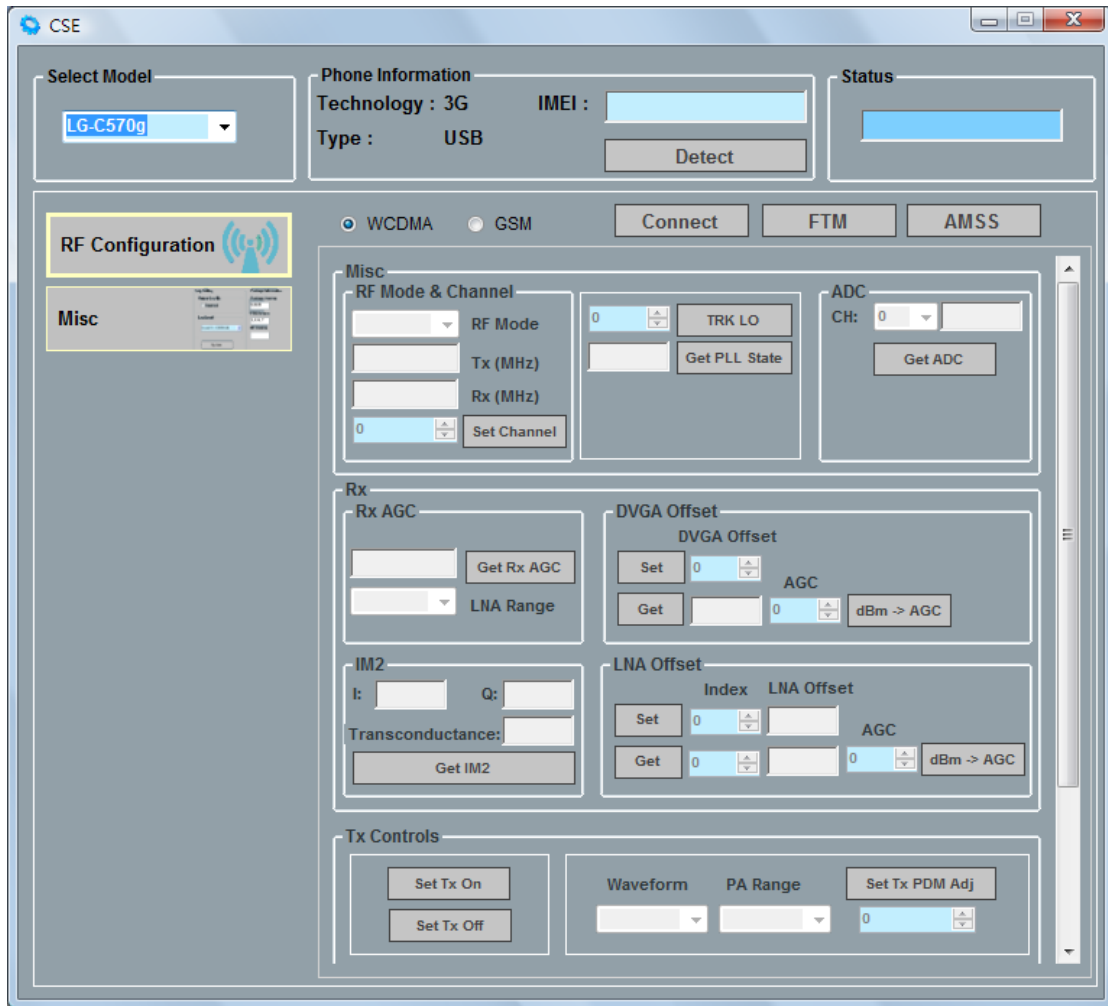


Figure 20. CSE RF Configuration UI.

11.5.1 Supporting network

CSE RF Configuration now supports GSM and WCDMA. It can configure Phone's network settings for trouble-shooting.

11.5.2 Environment

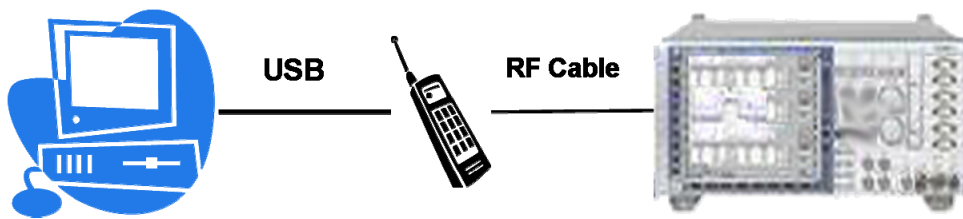


Figure 21. Test Environment.

CSE RF Configuration will setup phone through GPIB. After the setting is written to phone, we could use instrument to check the phone.

11.5.3 GSM in RF Configuration

The screenshot shows the RF Configuration interface for GSM mode. At the top, there are radio buttons for WCDMA and GSM (selected), and buttons for Disconnect, FTM, and AMSS. The interface is divided into several sections:

- RF Frequency:** Includes a dropdown for RF Mode, a numeric input for Set Channel (0), and two empty text boxes for Tx Freq (MHz) and Rx Freq (MHz).
- Power Control:** Includes three numeric inputs for PA DAC Input (0), PA Start Delta (0), and PA Stop Delta (0), and a dropdown for Set PCL.
- Rx Burst Command:** Includes a numeric input for Slot Number (0), a text box for Get RSSI, and four buttons: Burst Rx On, Cont Rx On, Burst Rx Off, and Cont Rx Off. There is also a dropdown for LIA Range.
- Tx Burst Command:** Includes two buttons: Set Tx On and Set Tx Off. Below them are three numeric inputs for DAC Start (0), DAC Stop (0), and DAC Step (0), with an Execute Sweep button. To the right, there are inputs for Slot Number (0), TSC Index (0), Data Source (Random Data), and Number of Burst (0), with an Infinite Burst checkbox and buttons for Set Tx Cont and Set Tx Burst.

◆ Misc

- **RF Mode:** This drop-down list lets you select from several RF modes: GSM 850, GSM 900, GSM 1800, and GSM 1900.
- **Set Channel:** You can change the Uplink channel by typing a number. A valid channel number per the applicable standard is available.
- **TRK LO:** Set the TRK LO value typing a number. TRK LO controls the voltage controlled temperature compensated crystal oscillator (VCTCXO) frequency. The maximum VCTCXO control voltage is 2047 and the minimum is -2048.

-
- **PA DAC Input:** Type a PA DAC(digital-to-analog convert) input value and click this button to specified dacInput value to generate a PA ramp profile.
 - **PA Start Delta:** Type PA start time value and then click the Set button to offset the PA ramp start time.
 - **PA Stop Delta:** Type PA stop time value and then click the Set button to offset the PA ramp stop time.
 - **Set PCL:** This drop-down list lets you select power level value to change PA power level.

◆ Rx Burst Command

- **Burst Rx On:** Type slot number and click Burst Rx On button to start burst Rx processing.
- **Burst Rx Off:** Type slot number and click Burst Rx Off button to stop burst Rx processing.
- **Cont Rx On:** Type slot number and click Cont Rx On button to start continuous Rx processing.
- **Cont Rx Off:** Type slot number and click Cont Rx Off button to stop continuous Rx processing.
- **Get RSSI:** Click the get RSSI button to get the RSSI value.
- **LNA Range:** This drop-down list lets you select LNA Range to sets the LNA gain state for the RF mode.

◆ Tx Burst Command

- **Set Tx On:** Click the Set Tx On button to start transmitter processing.
- **Set Tx Off:** Click the Set Tx Off button to stop transmitter processing.
- **Execute sweep:** This function takes 3 parameters, a DAC Start value, a DAC Stop value and a DAC Step value. It then turns the transmit burst on and varies the power from DAC Start to DAC Stop incrementing the power in steps of DAC Step. It uses the SET PA DAC input API to set the power for each burst. It has been introduced to make characterization of the GSM power amplifier easier and faster.
- **Set Tx Cont:** Set Tx Cont with three parameters: Slot Number, TSC Index and Data source. Note. Infinite Burst should be checked.
- **Set Tx Burst:** Set Tx Burst with four parameters: Slot Number, TSC Index, Data source and Number of Burst.

11.5.4 WCDMA in RF Configuration

☒ WCDMA ☐ GSM

Disconnect

FTM

AMSS

Misc

RF Mode & Channel

RF Mode

Tx (MHz)

Rx (MHz)

0

 Set Channel

0

 TRK LO

Get PLL State

ADC

CH:

0

 Get ADC

Rx

Rx AGC

Get Rx AGC

LNA Range

DVGA Offset

Set

0

 AGC

Get

0

 dBm -> AGC

IM2

I: Q:

Transconductance:

Get IM2

LNA Offset

Index LNA Offset

Set

0

 AGCGet

0

0

 dBm -> AGC

Tx Controls

Set Tx On

Set Tx Off

Waveform

 PA Range

Set Tx PDM Adj

0

Tx Sweep

Configure

0

 Tx Interval

0

 HDET Avg

Config Tx Sweep

Execute Sweep

HDET

0

 Step Index

HDET

Get HDET Value

◆ Misc

- **RF Mode:** This drop-down list lets you select from several RF modes: IMT, 1900A, 1900B, and 800.
- **Set Channel:** You can change the Uplink channel by typing a number. A valid channel number per the applicable standard is available.
- **TRK LO:** Set the TRK LO value typing a number. TRK LO controls the voltage controlled temperature compensated crystal oscillator (VCTXO) frequency. The maximum VCTXO control voltage is 4095 and the minimum is 0.
- **Get PLL State:** Click the Get PLL State button to get the PLL state.
- **Get ADC:** Use drop-down list to select the channel and click the Get ADC button to get the ADC value.

◆ Rx

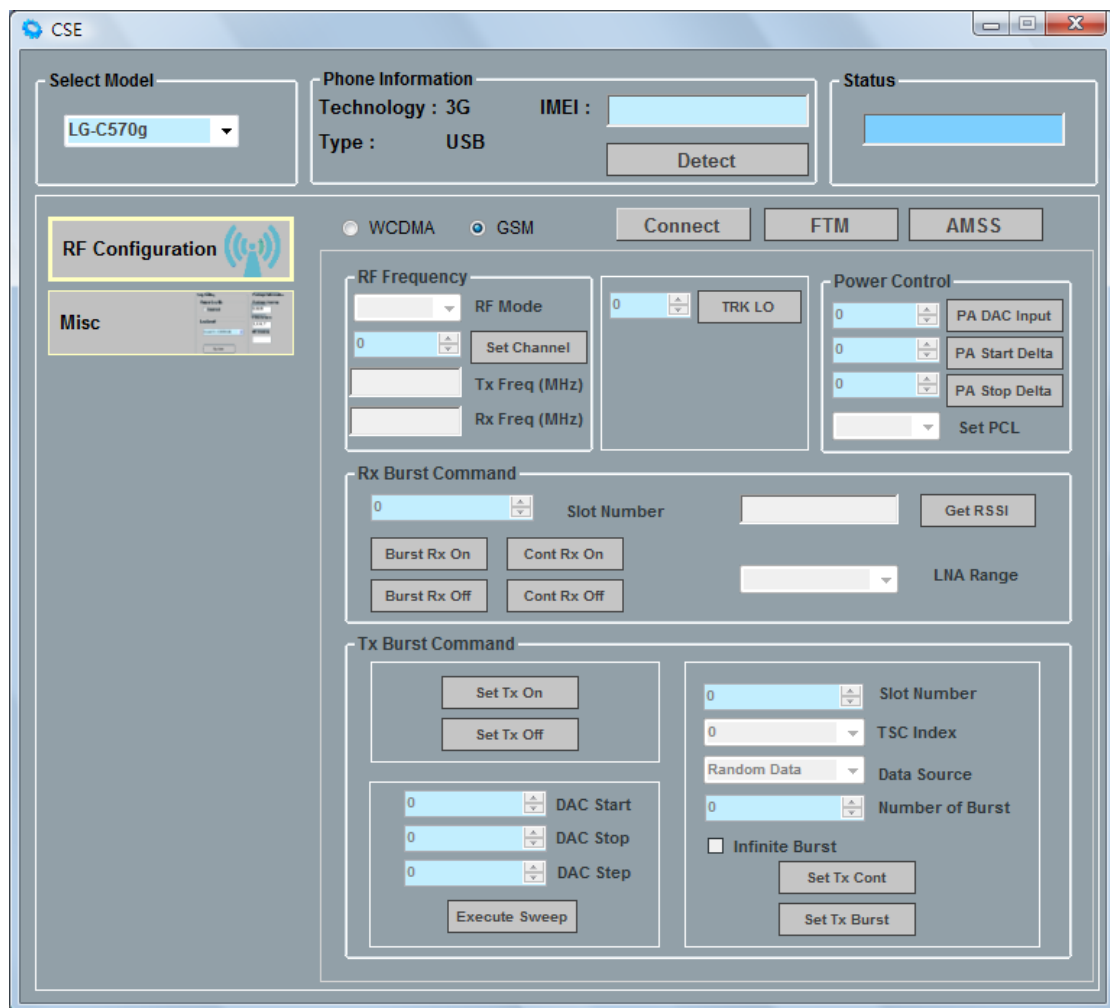
- **Get Rx AGC:** Click the Get Rx AGC button to get the Rx AGC.
- **LNA Range:** This drop-down list lets you select LNA Range to sets the LNA gain state for the RF mode.
- **Get IM2:** Click the Get IM2 button to retrieve the IM2 calibration register values and display them in the I, Q, and G (transconductance) boxes.
- **Get DVGA Offset:** Click the Get DVGA Offset button to retrieve the digital variable gain amplifier offset.
- **Set DVGA Offset:** Type a number in the Set DVGA (digital variable gain amplifier) Offset box and click the Set DVGA Offset button to set a value for DVGA offset.
- **Get LNA Offset:** Click the Get LNA Offset button to retrieve the LNA offset value for the given index.
- **Set LNA Offset:** Type numbers into the Index and Value boxes and click the Set LNA Offset button to set the LNA offset register for the given index value.

◆ Tx Controls

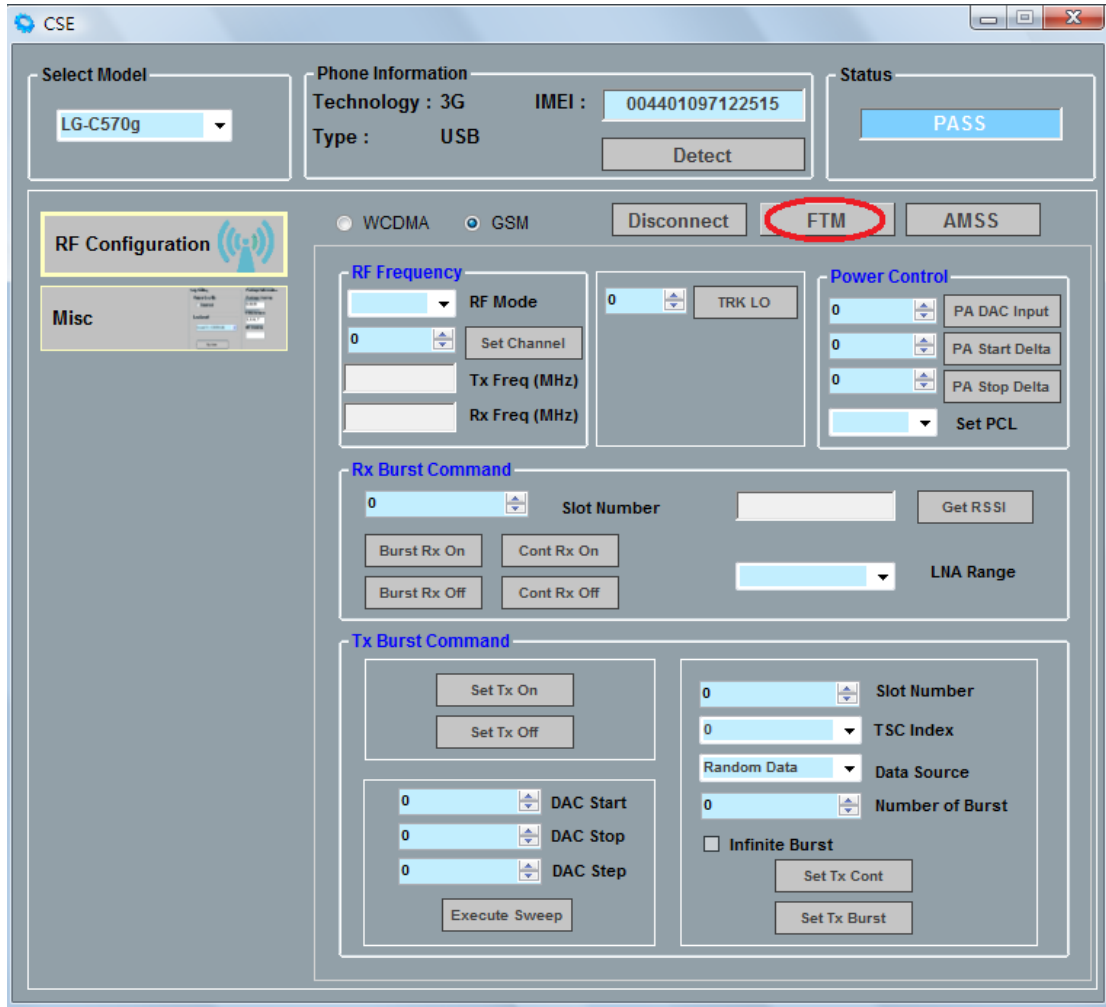
- **Set Tx On:** Click the Set Tx On button to turn on transmit chain.
- **Set Tx Off:** Click the Set Tx Off button to turn off transmit chain.
- **Waveform:** Click the appropriate check box to select WCDMA or continuous waveform (CW). The 'Modulated' option delivers a WCDMA waveform from the hardware platform under test and 'CW' delivers a continuous sinusoidal waveform, both centered at the selected Tx channel frequency.
- **PA Range:** Select power amplifier (PA) range by clicking the check box to select R0 on or off. R0 controls the PA Range 0 settings. ON sets the PA to high power mode and OFF sets it to low power mode.
- **Config Tx Sweep:** Click the Config Tx Sweep button to set the time interval of each step in the Tx calibration sweep and the number of HDET readings averaged per step.
- **Execute Sweep:** Click the Execute Sweep button to set up one or more complete TX sweeps from high power to low power with a predefined TX adjust PDM step size.
- **Get HDET Value:** You can change the index by clicking the down arrows. Click the 'Get HDET' button to retrieve HDET power data at the selected HDET index and display the value in the Value box.

11.5.5 Example: GSM “Tx On”

1. Select GSM and click “Connect” button

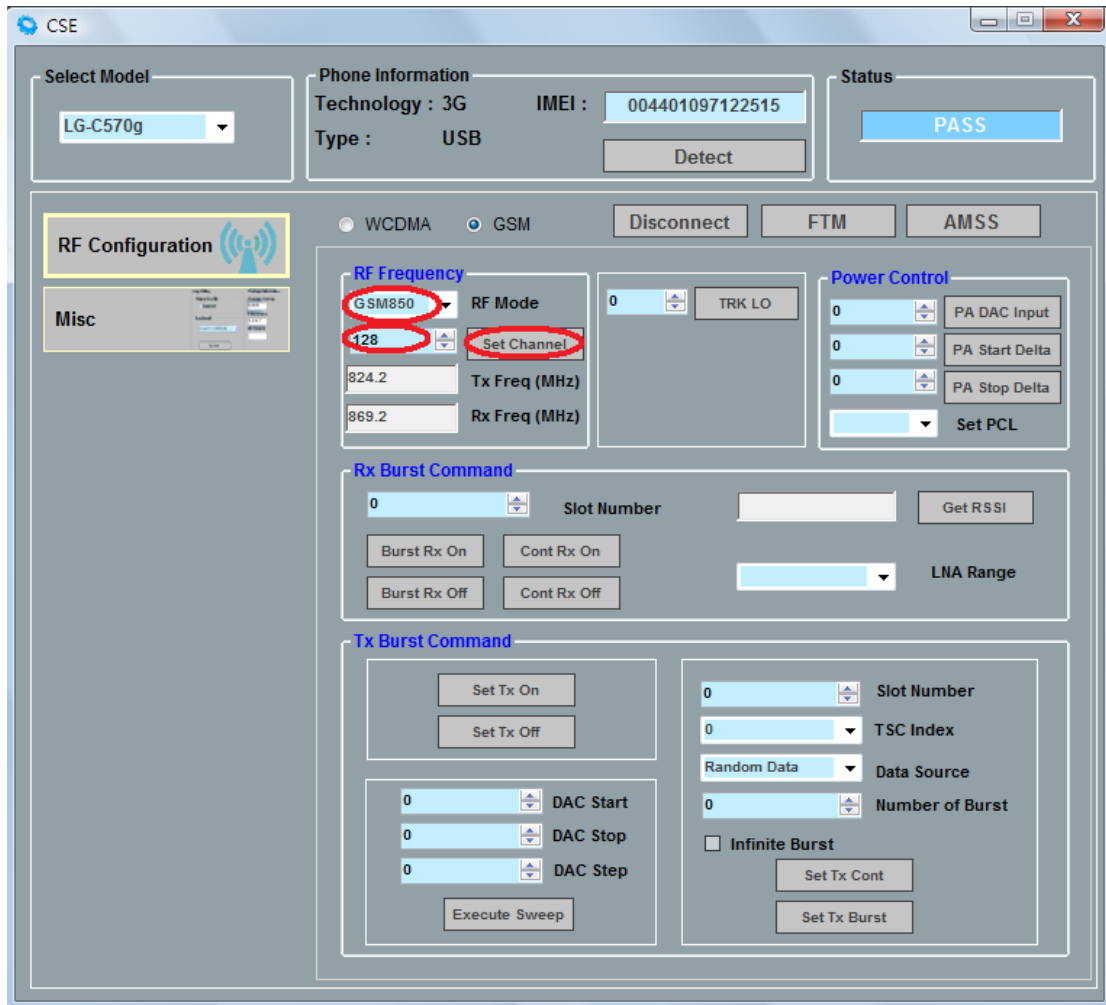


2. Click the FTM button to set the phone to FTM Mode.



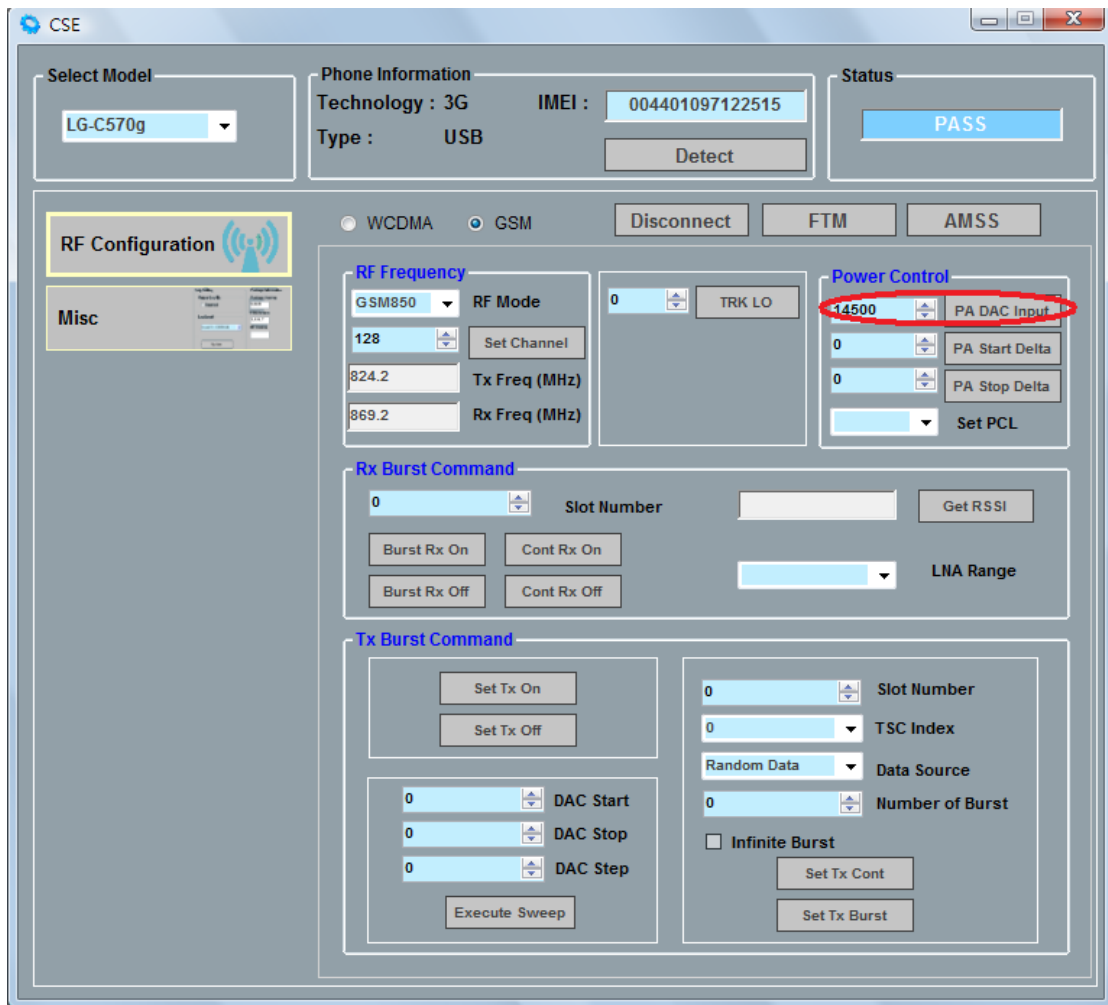
3. Setup "RF Frequency"

- 1) Select RF Mode
- 2) Input channel
- 3) Click "Set Channel" button.

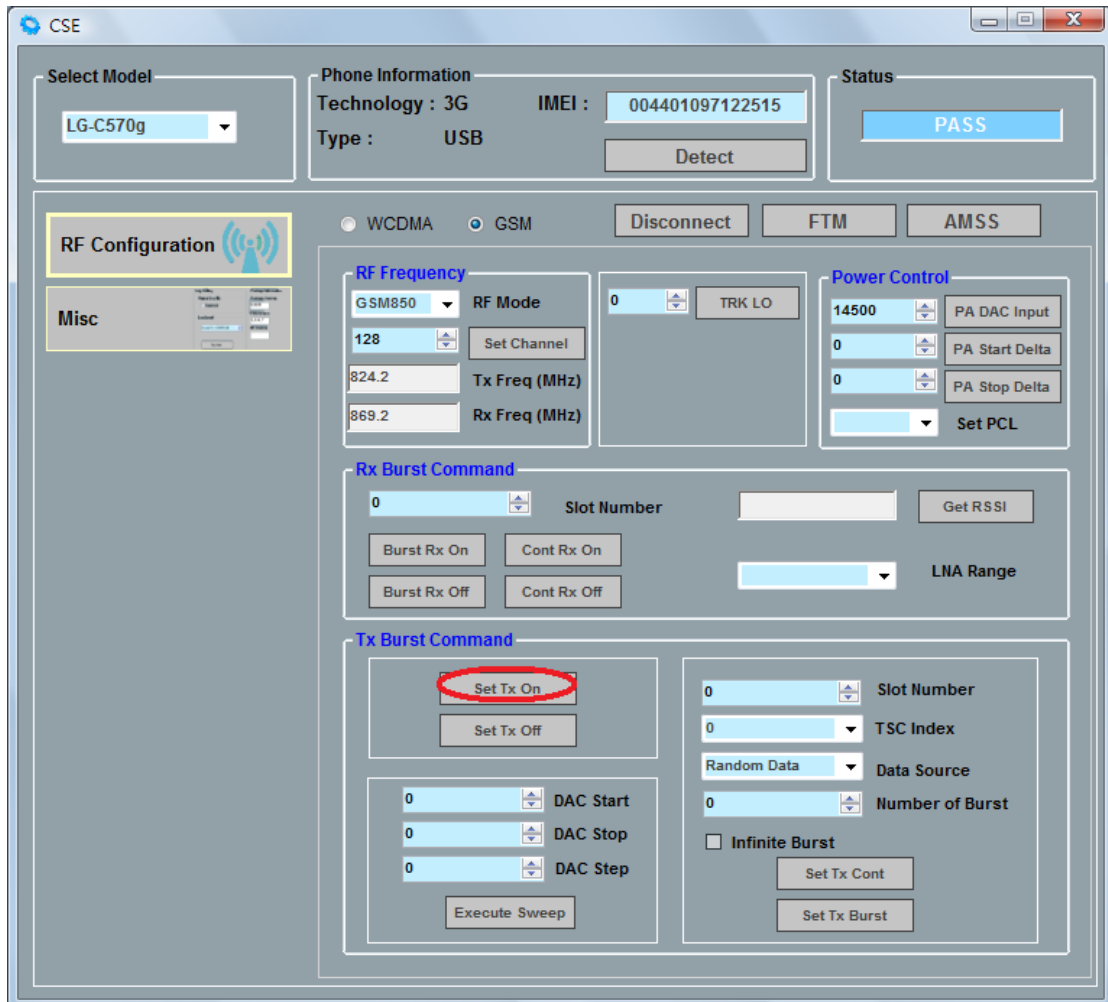


4. Setup "Power Control"

- 1) Set PA DAC value → 14500
- 2) Click "PA DAC Input" button

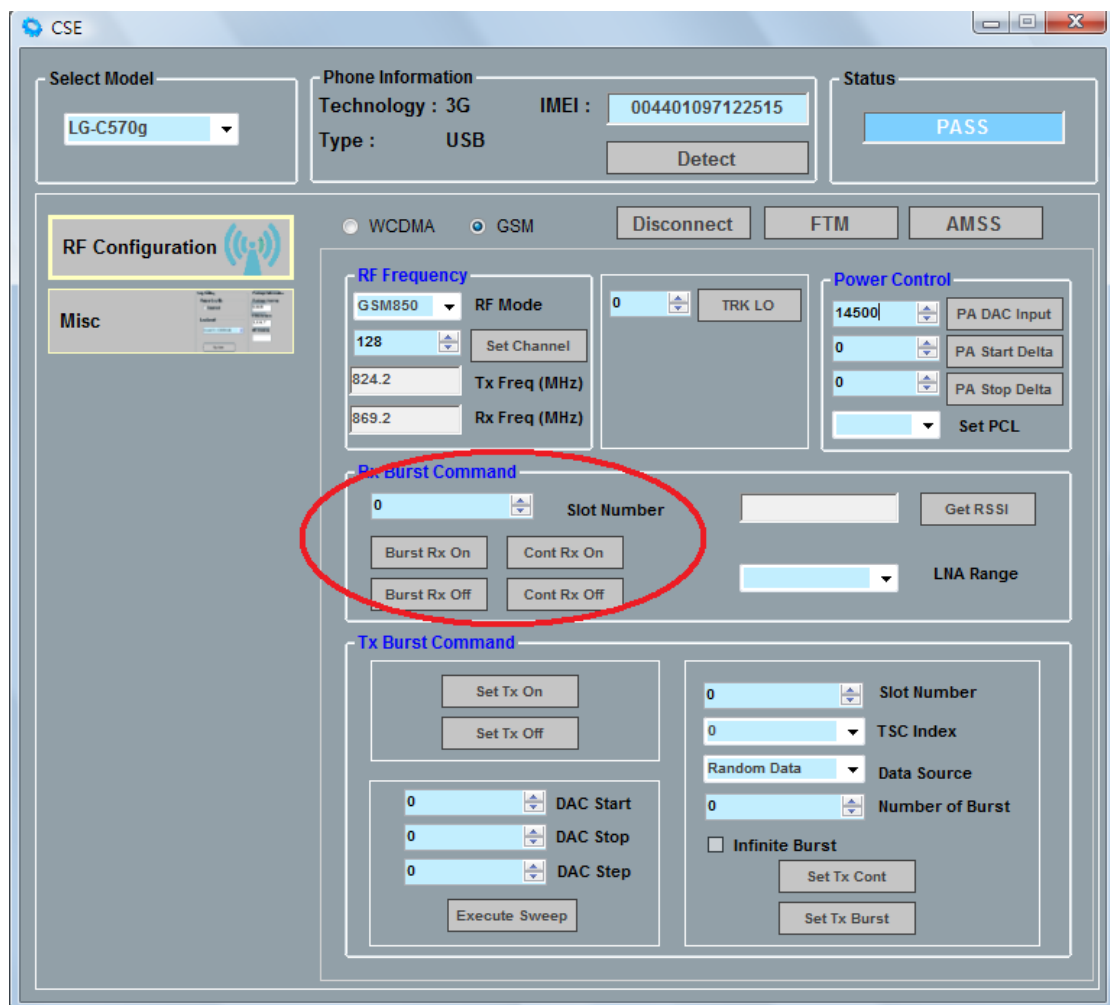


5. Click “Set Tx On” button.



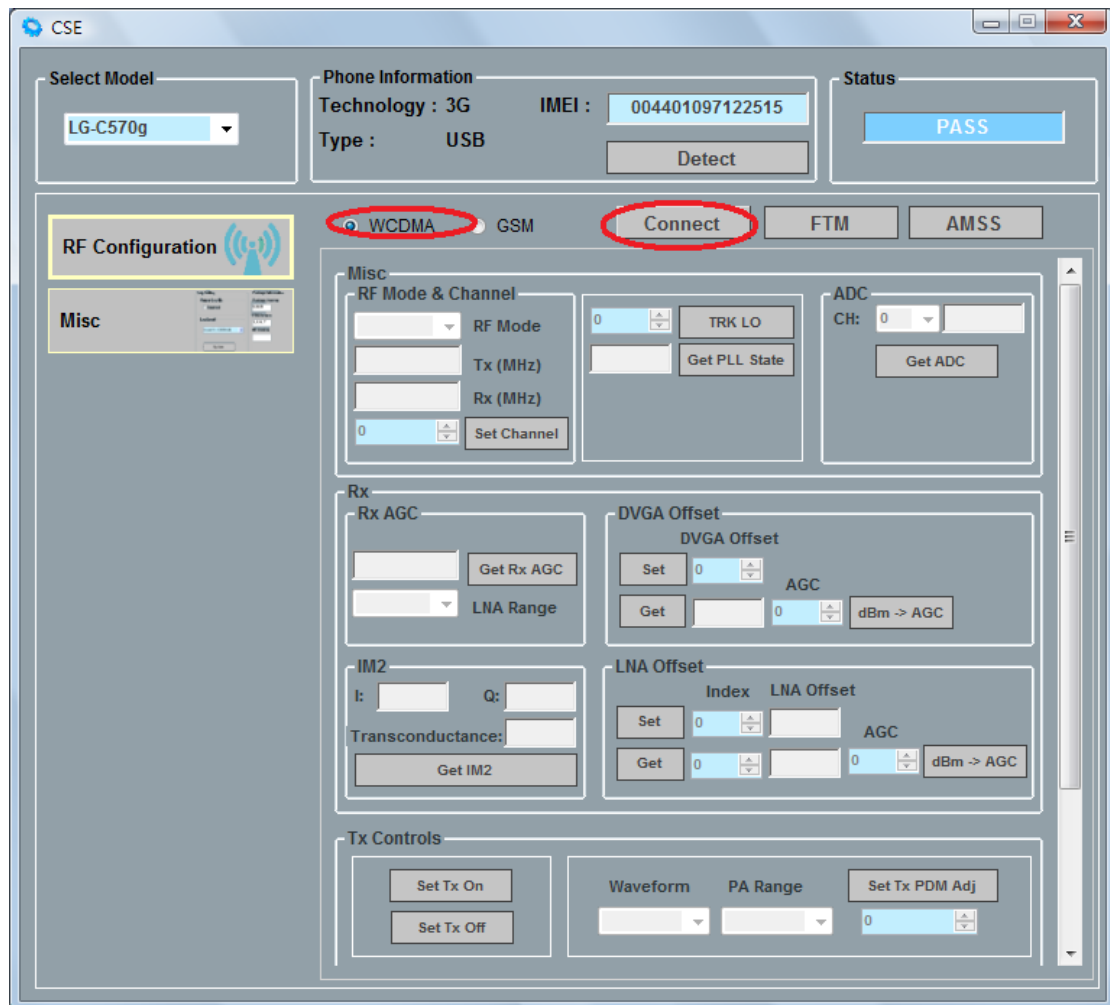
11.5.6 Example: GSM “Rx On”

1. Follow 3.7.5 to do step 1, 2, and 3.
2. Input “Slot Number” and click “Burst Rx On” button

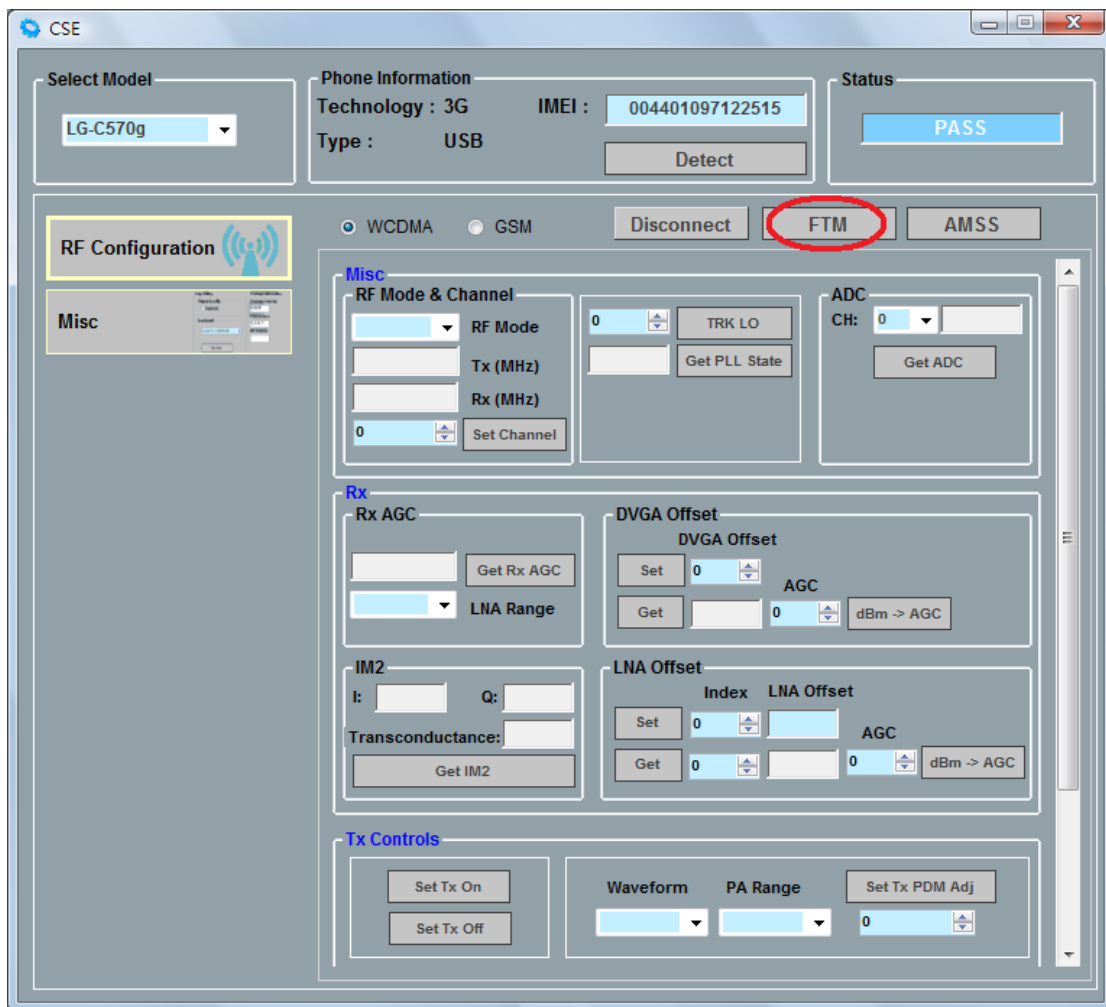


11.5.7 Example: WCDMA “Tx On”

1. Select GSM and click “Connect” button



2. Click the FTM button to set the phone to FTM Mode.



3. Setup "RF Mode & Channel"

- 1) Select RF Mode
- 2) Input channel
- 3) Click "Set Channel" button.

The screenshot displays the CSE (Cellular Setup Environment) software interface. The top section includes a 'Select Model' dropdown set to 'LG-C570g', 'Phone Information' showing 'Technology : 3G' and 'IMEI : 004401097122515', and a 'Status' indicator showing 'PASS'. Below this, the 'RF Configuration' section is active, with 'WCDMA' selected as the radio technology. The 'Misc' tab is chosen, and the 'RF Mode & Channel' sub-section is highlighted. In this sub-section, the 'RF Mode' dropdown is set to 'JMT', and the 'Channel' field is set to '9612'. The 'Set Channel' button is circled in red. Other fields in this section include 'Tx (MHz)' at 1922.4, 'Rx (MHz)' at 2112.4, and 'TRK LO' at 0. The 'ADC' section shows 'CH: 0' and a 'Get ADC' button. The 'Rx' section includes 'Rx AGC' and 'LNA Range' controls. The 'DVGA Offset' section shows 'Set' and 'Get' buttons for 'DVGA Offset' and 'AGC'. The 'LNA Offset' section shows 'Set' and 'Get' buttons for 'Index', 'LNA Offset', and 'AGC'. The 'Tx Controls' section includes 'Set Tx On', 'Set Tx Off', 'Waveform', 'PA Range', and 'Set Tx PDM Adj' controls.

CSE

Select Model: LG-C570g

Phone Information: Technology : 3G, IMEI : 004401097122515, Type : USB, Detect

Status: PASS

RF Configuration

Misc

WCDMA GSM Disconnect FTM AMSS

Misc

RF Mode & Channel

JMT RF Mode

1922.4 Tx (MHz)

2112.4 Rx (MHz)

9612 Set Channel

0 TRK LO

Get PLL State

ADC

CH: 0

Get ADC

Rx

Rx AGC

Get Rx AGC

LNA Range

DVGA Offset

DVGA Offset

Set 0

AGC

Get 0 dBm -> AGC

IM2

I: Q:

Transconductance:

Get IM2

LNA Offset

Index LNA Offset

Set 0

AGC

Get 0 dBm -> AGC

Tx Controls

Set Tx On

Set Tx Off

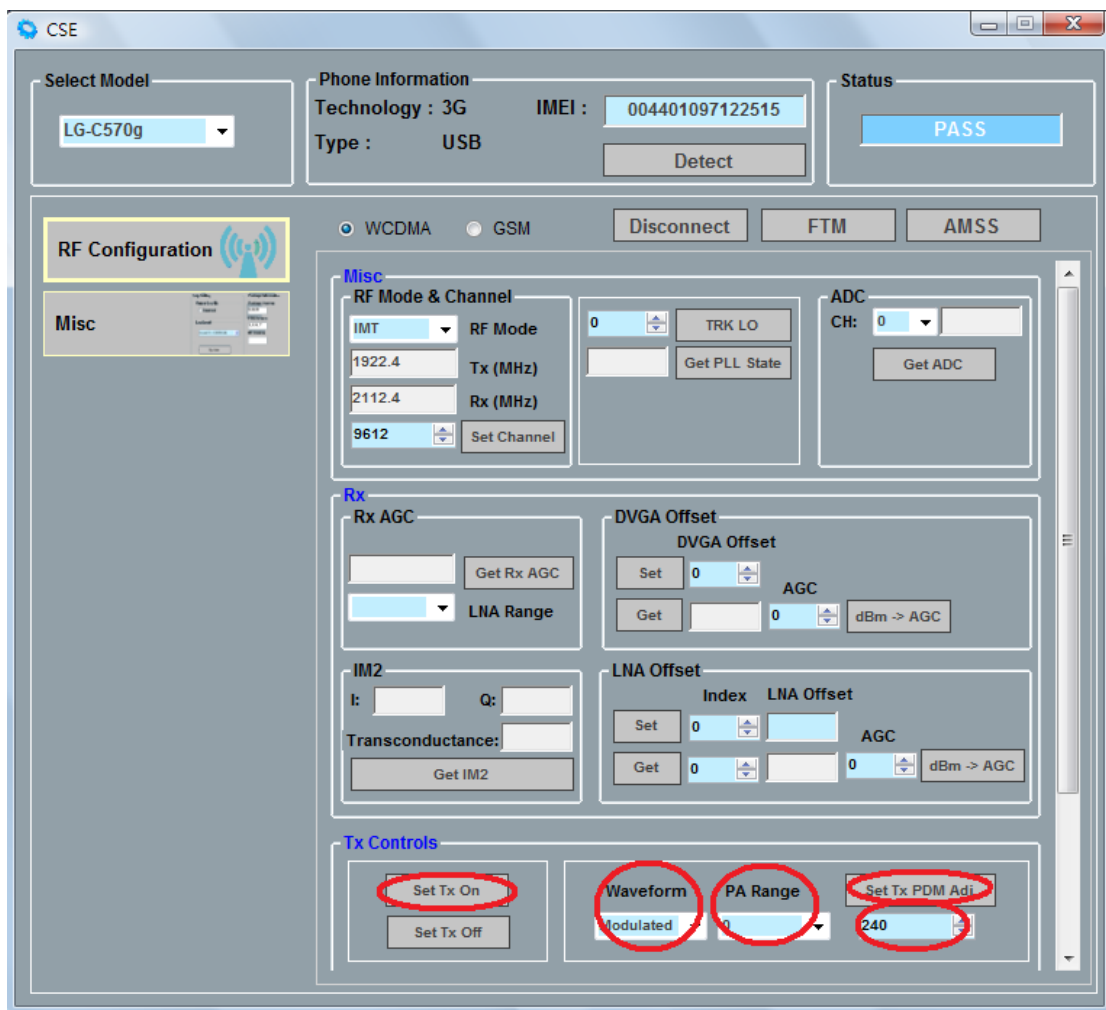
Waveform PA Range

Set Tx PDM Adj

0

4. Setup “Tx Controls”

- 1) Set “Waveform” → “Modulated”
- 2) Set “PA Range” → “0”
- 3) Set “Tx PDM” → “240”
- 4) Click the “Set Tx PDM Adj” button
- 5) Click the “Set Tx On” button
- 6) Set “PA Range” → “3”



10.7.8 Example: WCDMA “Rx On”

Follow 3.7.7 to do step 1, 2, and 3.

11.6 Miscellaneous Group

After model selection [Appendix A. Set Phone Mode], the relevant log settings are available by selecting the “Misc” button in the function group [Figure 22].

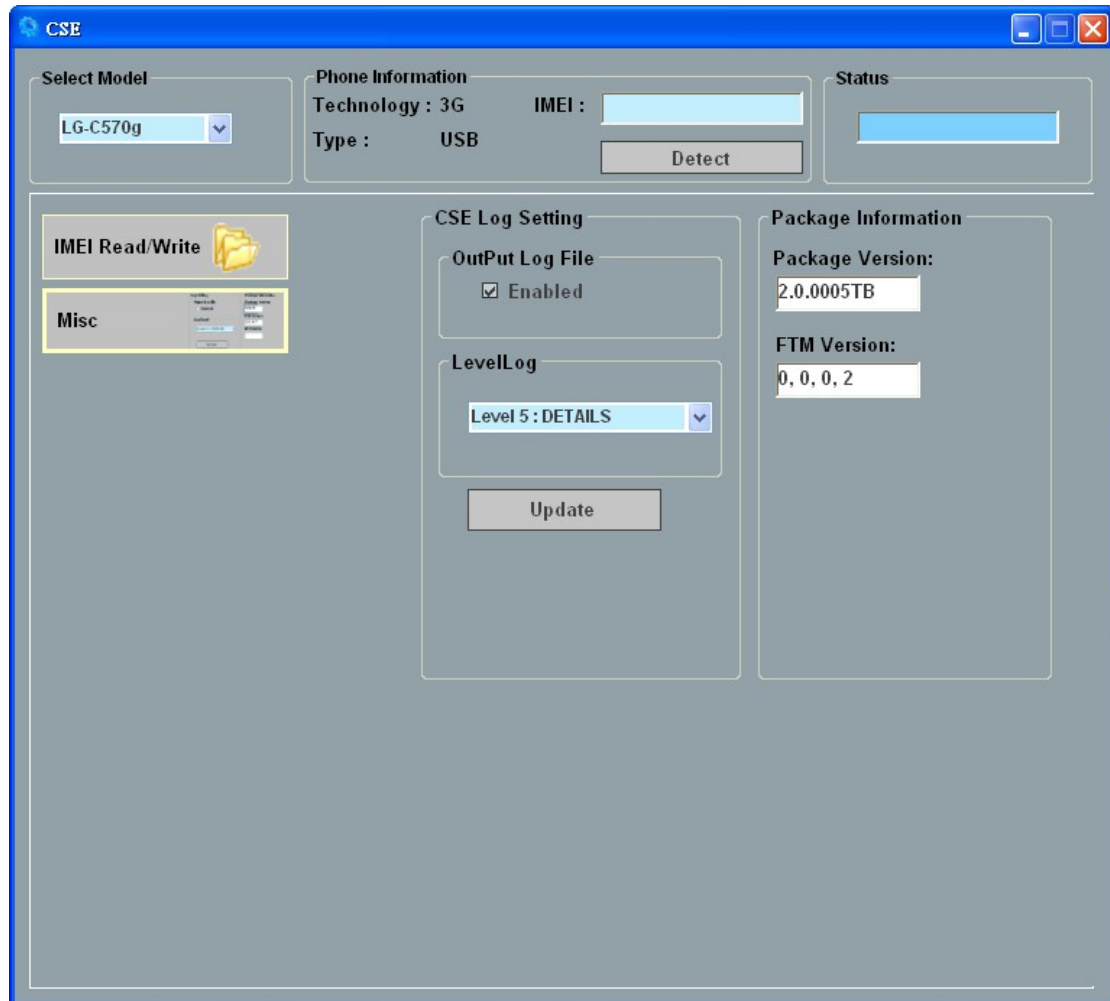


Figure 22. CSE miscellany UI.

There are mainly two group boxes for Misc function group, namely, “CSE Log Setting” and “Package Information”. The file “CSE Log Setting” logs the information of CSE tool. The default log path is “C:\ProgramFiles\CSE\CC\Testlogs”. To enable/disable log recording, check/uncheck the button “Enabled” checked box in the sub group box “Output log file”. The drop-down menu in the sub group box “CSE Log Setting” provides the selection of log level which decides the information to be recorded. A higher level will make the tool record more log information. Also, note that the handset information is not recorded here but the CSE software instead. It is mainly for debugging or problem analysis purpose regards to issues found when using CSE.

The following table specifies each of the log level.

Level	Level name	Description
Level 1	CRITICAL	All kinds of errors should be recorded.
Level 2	BASIC_PLUS	Record all possible warnings.
Level 3	BASIC	Record every function calls during the tool execution.
Level 4	BASIC_MINUS	Record all arguments of each function call.
Level 5	DETAILS	Record all information.

Table 3. Logging levels description.

The group box “Package Information” shows the version information of CSE package and its components.