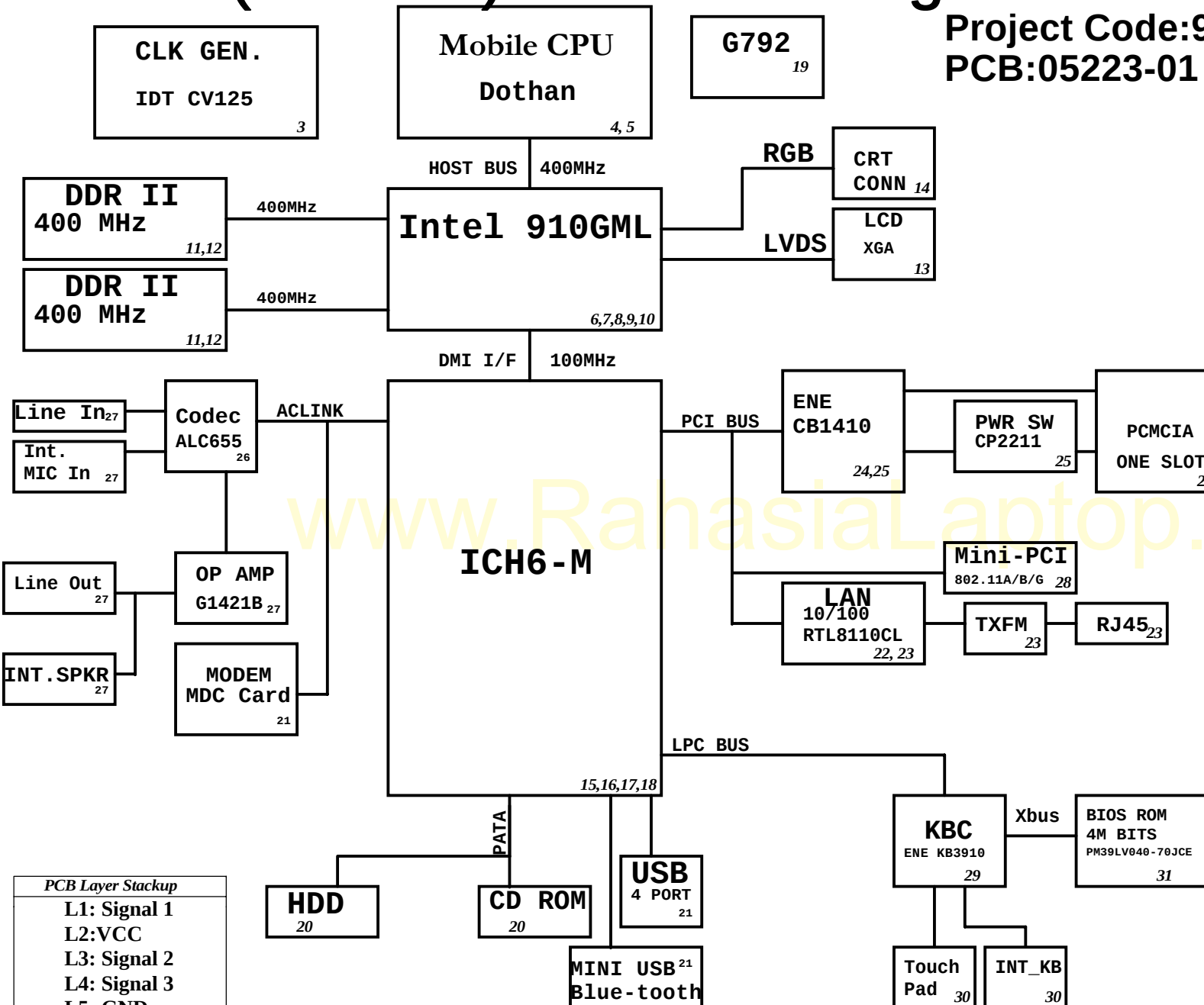


AG1(Alviso) Block Diagram 2005/11/01

Project Code:91.4G301.001
PCB:05223-01



CPU DC/DC ISL6218CV-T 34	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 27A

SYSTEM DC/DC TPS51120 35	
INPUTS	OUTPUTS
DCBATOUT	3D3V_S5 5V_S5
APL5912-LAC APL5308-25AC 36	
INPUTS	OUTPUTS
5V_S5 3D3V_S0	1D5V_S0 2D5V_S0
SYSTEM DC/DC ISL6227 37	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S3
TPS51100DGQ 37	
5V_S5	DDR_VREF DDR_VREF_S3

CHARGER ISL6255 38	
INPUTS	OUTPUTS
DCBATOUT	BT+ 16.8V 3A

PCB Layer Stackup

- L1: Signal 1
- L2: VCC
- L3: Signal 2
- L4: Signal 3
- L5: GND
- L6: Signal 4

<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title BLOCK DIAGRAM		
Size Custom	Document Number AG1(Alviso)	Rev 01
Date: Tuesday, November 01, 2005 Sheet 1 of 40		

Alviso Strapping Signals and Configuration

page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = Reserved 001 = FSB533 010 = FSB800 011-111 = Reversed
CFG[3:4]	Reversed	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	DDR I / DDR II	0 = DDR II 1 = DDR I
CFG7	CPU Strap	0 = Prescott 1 = Dothan (Default)
CFG[8:11]	Reversed	
CFG[12:13]	XOR/ALL Z test Straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[14:15]	Reversed	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG17	Reversed	
CFG18	CPU core VCC Select	0 = 1.05V (Default) 1 = 1.5V
CFG19	CPU VTT Select	0 = 1.05V (Default) 1 = 1.2V
CFG20	Reversed	
SDVOCRTL_DATA	SDVO Present	0 = No SDVO device present (Default) 1= SDVO device present

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORK In signal.

PCI Routing

	IDSEL	IRQ	REQ/GNT
1410	25	B.F.G	0
MiniPCI	21	F	1
LAN	23	E	2

ICH6-M Integrated Pull-up and Pull-down Resistors

ICH6-M EDS 14308 0.8V1

ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, GNT[5]/GPO[17], GNT[6]/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT, ACZ_BITCLK, DPRSLPVR, SPKR, EE_CS,	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDREQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

ICH6-M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------

<Core Design>

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Title

Memo

Size A3

Document Number

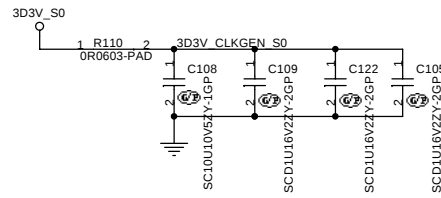
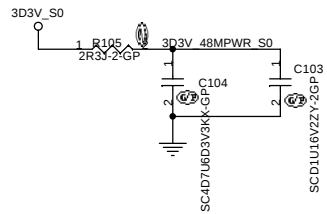
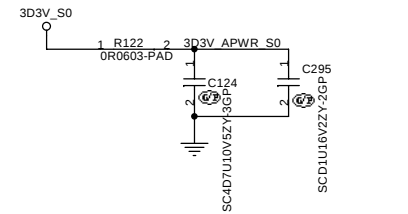
Rev

Date: Tuesday, November 01, 2005

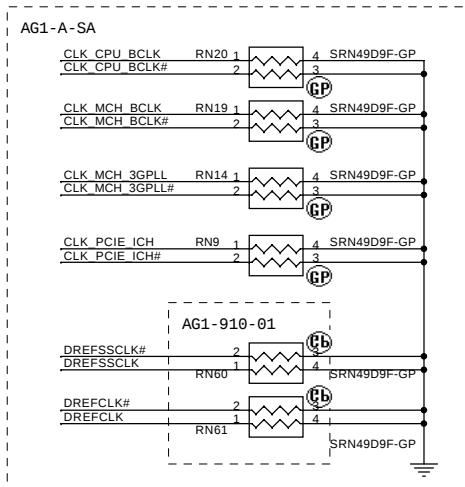
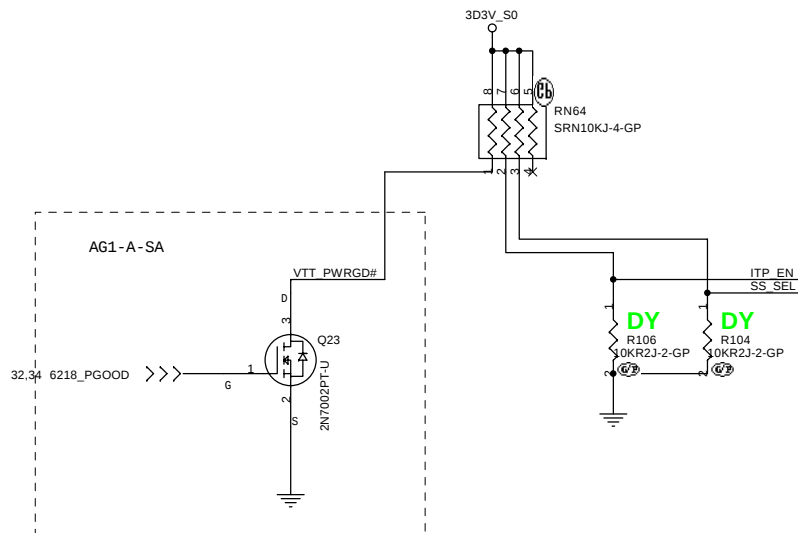
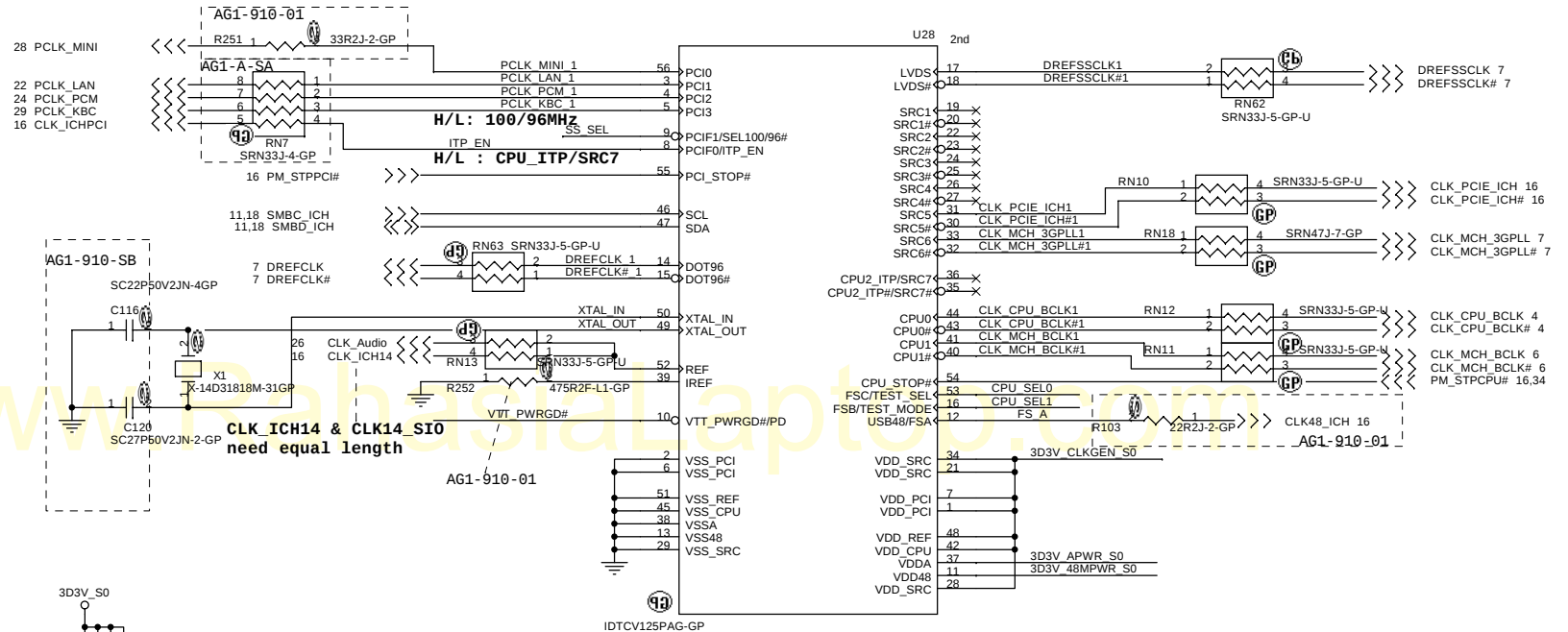
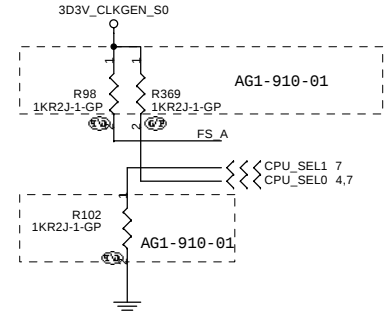
Sheet 2 of 40

AG1(Alviso)

01



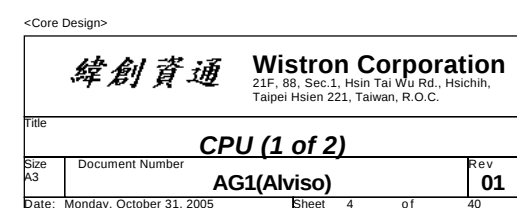
IN (3D3V_S0)	EN (6218_PG00D)	OUT (VTT_PWRGD#)
H	L	H
X	H	H1 - Z



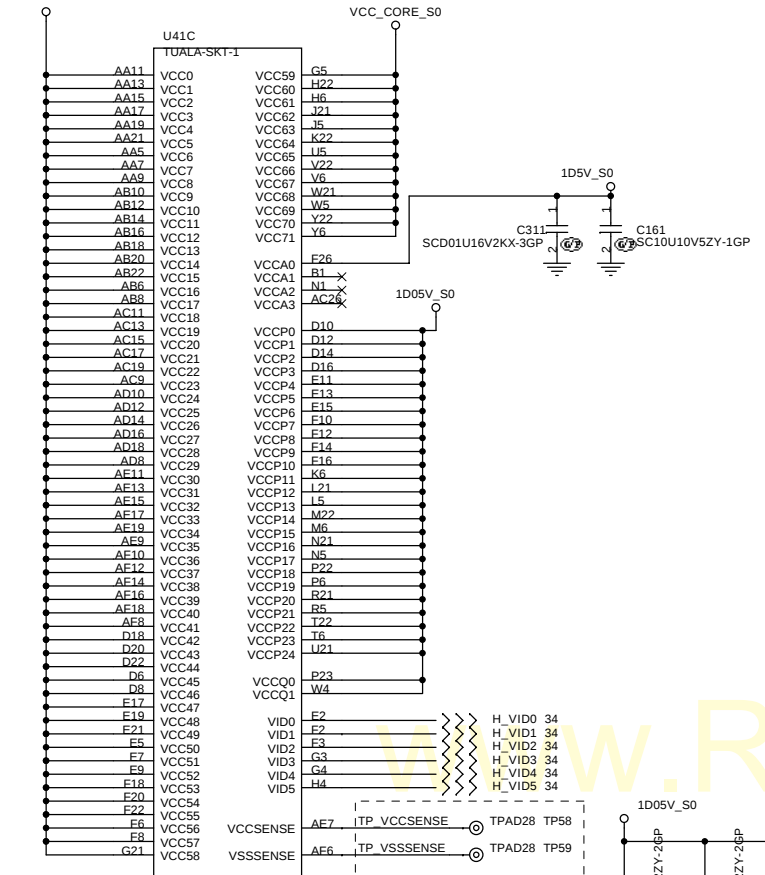
EMI capacitor			
CLK ICH14	EC45	1	SC10P50V2JN-4GP
PCLK PCM	EC41	1	SC10P50V2JN-4GP
PCLK MINI	EC70	1	SC10P50V2JN-4GP
PCLK KBC	EC42	1	SC10P50V2JN-4GP
CLK ICHPCI	EC43	1	SC10P50V2JN-4GP
CLK48 ICH	EC39	1	SC10P50V2JN-4GP

<Core Design>

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Title		
Clock Generator - IDT125		
Size	Document Number	Rev
A3	AG1(Alviso)	01
Date: Friday, October 28, 2005	Sheet 3 of 40	



VCC_CORE_S0

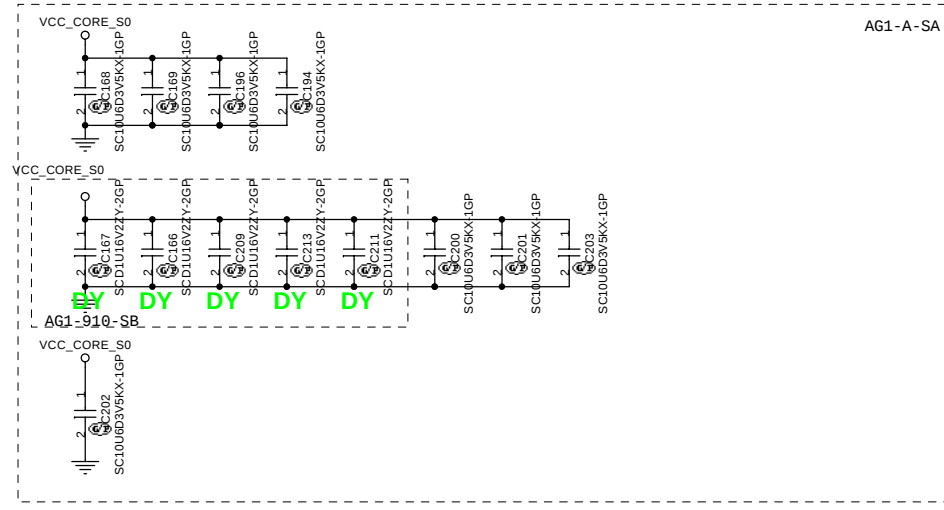


62.10053.061
CONNECTOR
Y

Layout Note:

VCCSENSE and VSSSENSE lines
should be of equal length.

Layout Note:
Provide a test point (with
no stub) to connect a
differential probe
between VCCSENSE and
VSSSENSE at the location
where the two 54.9ohm
resistors terminate the
55 ohm transmission line.



AG1-910-SB

VCC_CORE_S0

VCC_CORE_S0

VCC_CORE_S0

VCC_CORE_S0

VCC_CORE_S0

VCC_CORE_S0

U41D	TUALA-SKT-1	D13
A2	VSS0	VSS97
A5	VSS1	VSS98
A8	VSS2	VSS99
A11	VSS3	VSS100
A14	VSS4	VSS101
A17	VSS5	VSS102
A20	VSS6	VSS103
A23	VSS7	VSS104
A26	VSS8	VSS105
AA1	VSS9	VSS106
AA4	VSS10	VSS107
AA6	VSS11	VSS108
AA8	VSS12	VSS109
AA10	VSS13	VSS110
AA12	VSS14	VSS111
AA14	VSS15	VSS112
AA16	VSS16	VSS113
AA18	VSS17	VSS114
AA20	VSS18	VSS115
AA22	VSS19	VSS116
AA25	VSS20	VSS117
AB3	VSS21	VSS118
AB5	VSS22	VSS119
AB7	VSS23	VSS120
AB9	VSS24	VSS121
AB11	VSS25	VSS122
AB13	VSS26	VSS123
AB15	VSS27	VSS124
AB17	VSS28	VSS125
AB19	VSS29	VSS126
AB21	VSS30	VSS127
AB23	VSS31	VSS128
AB26	VSS32	VSS129
AC2	VSS33	VSS130
AC5	VSS34	VSS131
AC8	VSS35	VSS132
AC10	VSS36	VSS133
AC12	VSS37	VSS134
AC14	VSS38	VSS135
AC16	VSS39	VSS136
AC18	VSS40	VSS137
AC21	VSS41	VSS138
AC24	VSS42	VSS139
AD1	VSS43	VSS140
AD4	VSS44	VSS141
AD7	VSS45	VSS142
AD9	VSS46	VSS143
AD11	VSS47	VSS144
AD13	VSS48	VSS145
AD15	VSS49	VSS146
AD17	VSS50	VSS147
AD19	VSS51	VSS148
AD22	VSS52	VSS149
AD25	VSS53	VSS150
AE3	VSS54	VSS151
AE6	VSS55	VSS152
AE8	VSS56	VSS153
AE10	VSS57	VSS154
AE12	VSS58	VSS155
AE14	VSS59	VSS156
AE16	VSS60	VSS157
AE18	VSS61	VSS158
AE20	VSS62	VSS159
AE23	VSS63	VSS160
AE26	VSS64	VSS161
AE2	VSS65	VSS162
AE5	VSS66	VSS163
AE9	VSS67	VSS164
AF11	VSS68	VSS165
AF13	VSS69	VSS166
AF15	VSS70	VSS167
AF17	VSS71	VSS168
AF19	VSS72	VSS169
AF21	VSS73	VSS170
AF24	VSS74	VSS171
B3	VSS75	VSS172
B6	VSS76	VSS173
B9	VSS77	VSS174
B12	VSS78	VSS175
B16	VSS79	VSS176
B19	VSS80	VSS177
B22	VSS81	VSS178
B25	VSS82	VSS179
C1	VSS83	VSS180
C4	VSS84	VSS181
C7	VSS85	VSS182
C10	VSS86	VSS183
C13	VSS87	VSS184
C15	VSS88	VSS185
C18	VSS89	VSS186
C21	VSS90	VSS187
C24	VSS91	VSS188
D2	VSS92	VSS189
D5	VSS93	VSS190
D7	VSS94	VSS191
D9	VSS95	VSS192
D11	VSS96	VSS193

<Core Design>

CONNECTOR Y
62.10053.061

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU (2 of 2)

Size

A3

Document Number

AG1(Alviso)

Rev

01

Date:

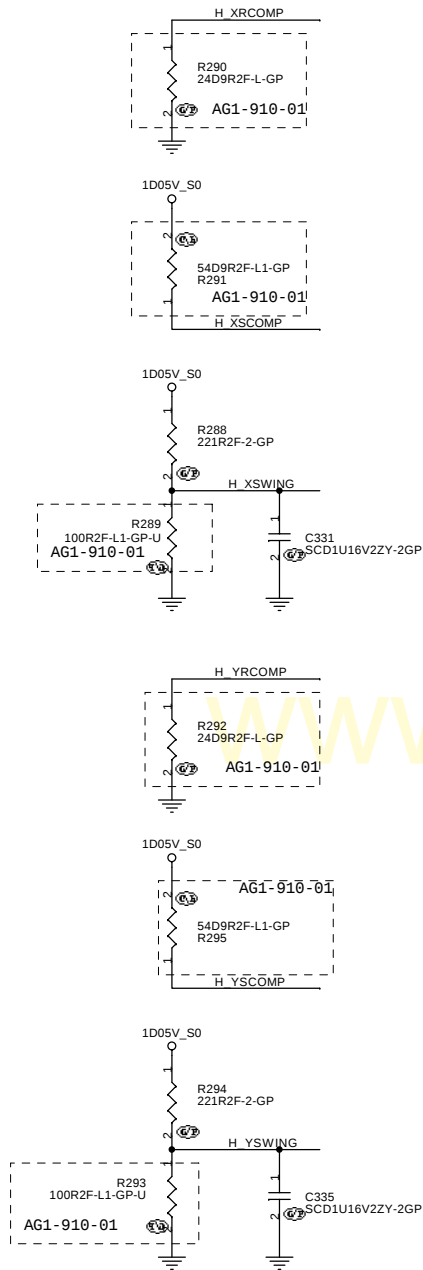
Monday, October 17, 2005

Sheet

5

of

40



Place them near to the chip

4 H_D#[63..0]

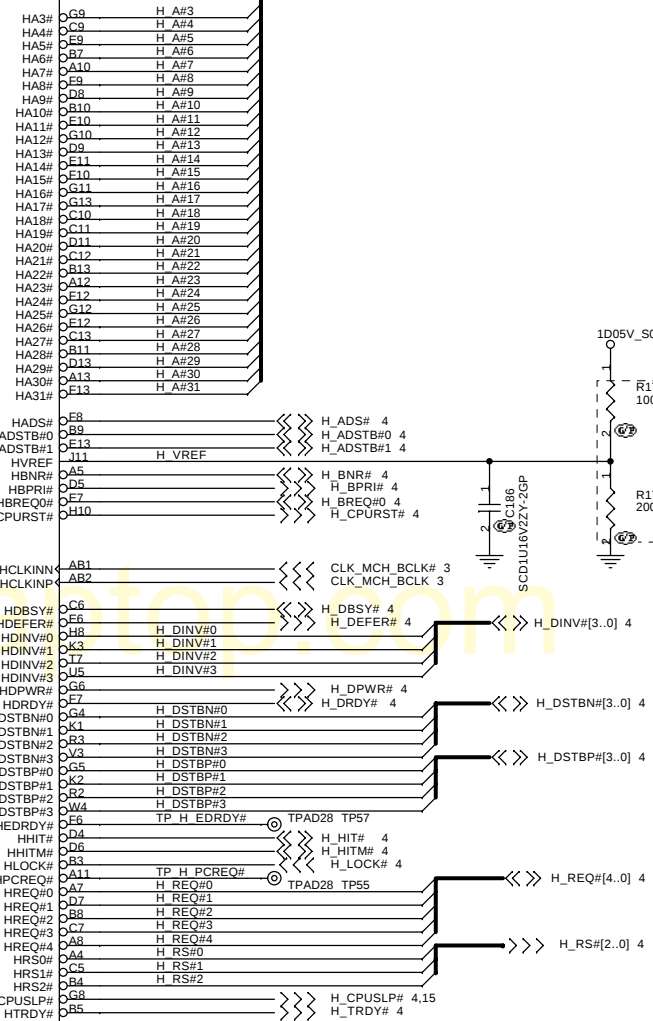


H_D#0	E40	HD0#
H_D#1	E41	HD1#
H_D#2	E42	HD2#
H_D#3	E43	HD3#
H_D#4	E44	HD4#
H_D#5	E45	HD5#
H_D#6	E46	HD6#
H_D#7	E47	HD7#
H_D#8	E48	HD8#
H_D#9	E49	HD9#
H_D#10	E50	HD10#
H_D#11	E51	HD11#
H_D#12	E52	HD12#
H_D#13	E53	HD13#
H_D#14	E54	HD14#
H_D#15	E55	HD15#
H_D#16	E56	HD16#
H_D#17	E57	HD17#
H_D#18	E58	HD18#
H_D#19	E59	HD19#
H_D#20	E60	HD20#
H_D#21	E61	HD21#
H_D#22	E62	HD22#
H_D#23	E63	HD23#
H_D#24	E64	HD24#
H_D#25	E65	HD25#
H_D#26	E66	HD26#
H_D#27	E67	HD27#
H_D#28	E68	HD28#
H_D#29	E69	HD29#
H_D#30	E70	HD30#
H_D#31	E71	HD31#
H_D#32	E72	HD32#
H_D#33	E73	HD33#
H_D#34	E74	HD34#
H_D#35	E75	HD35#
H_D#36	E76	HD36#
H_D#37	E77	HD37#
H_D#38	E78	HD38#
H_D#39	E79	HD39#
H_D#40	E80	HD40#
H_D#41	E81	HD41#
H_D#42	E82	HD42#
H_D#43	E83	HD43#
H_D#44	E84	HD44#
H_D#45	E85	HD45#
H_D#46	E86	HD46#
H_D#47	E87	HD47#
H_D#48	E88	HD48#
H_D#49	E89	HD49#
H_D#50	E90	HD50#
H_D#51	E91	HD51#
H_D#52	E92	HD52#
H_D#53	E93	HD53#
H_D#54	E94	HD54#
H_D#55	E95	HD55#
H_D#56	E96	HD56#
H_D#57	E97	HD57#
H_D#58	E98	HD58#
H_D#59	E99	HD59#
H_D#60	E100	HD60#
H_D#61	E101	HD61#
H_D#62	E102	HD62#
H_D#63	E103	HD63#
H_XRCOMP	C1	HXRCOMP
H_XSCOMP	C2	HXSCOMP
H_XSWING	D1	HXSWING
H_YRCOMP	I1	HYRCOMP
H_YSCOMP	I1	HYSCOMP
H_YSWING	P1	HYSWING

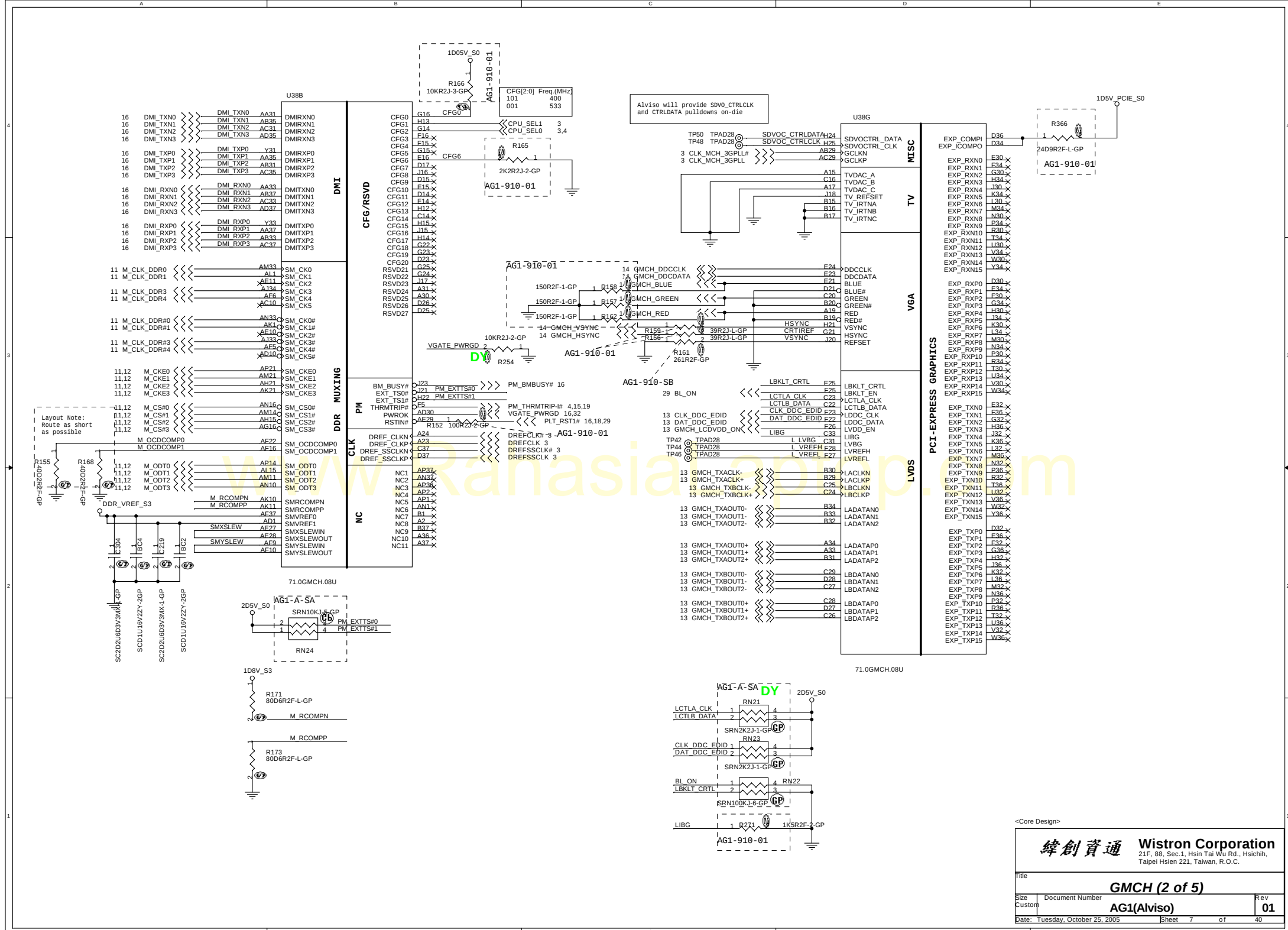
U38A

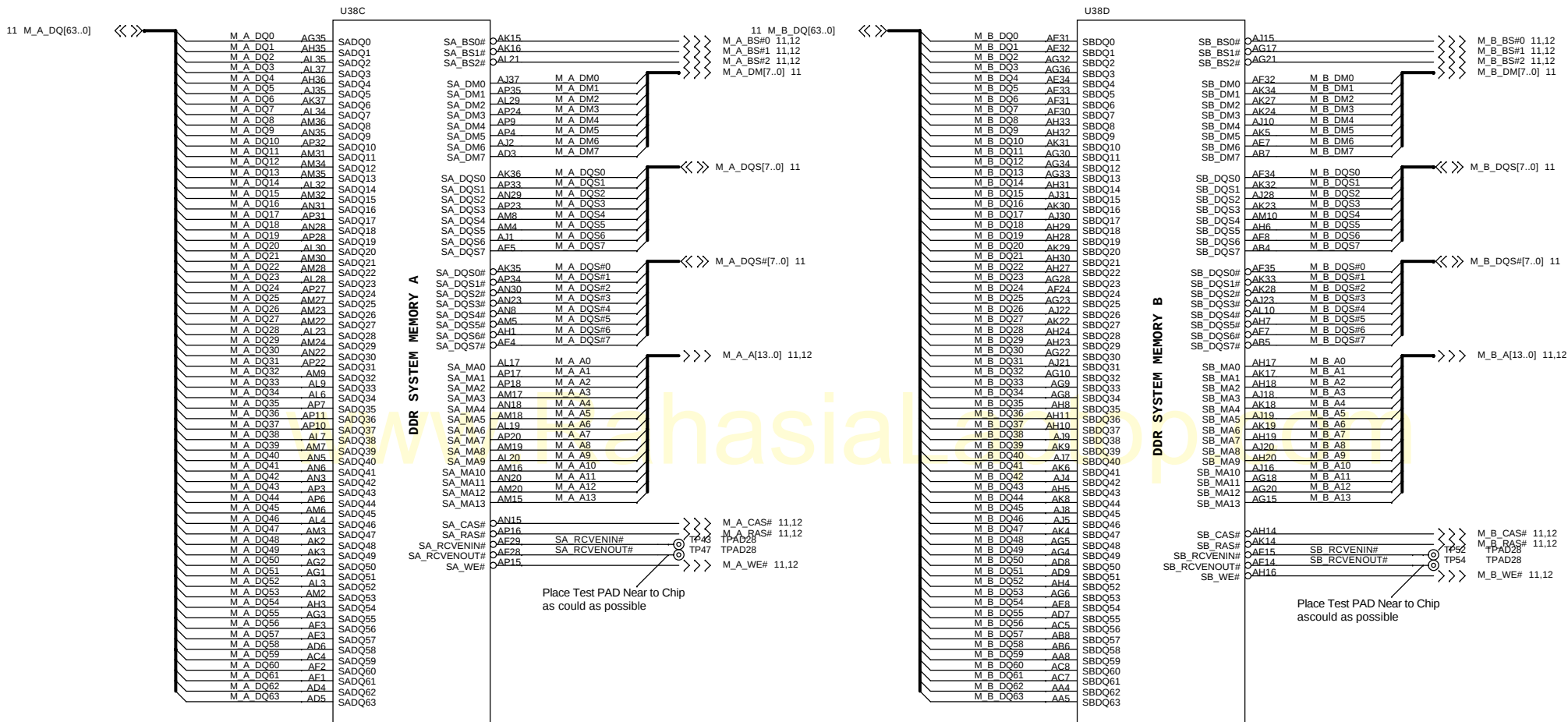
HOST

710GMCH.08U



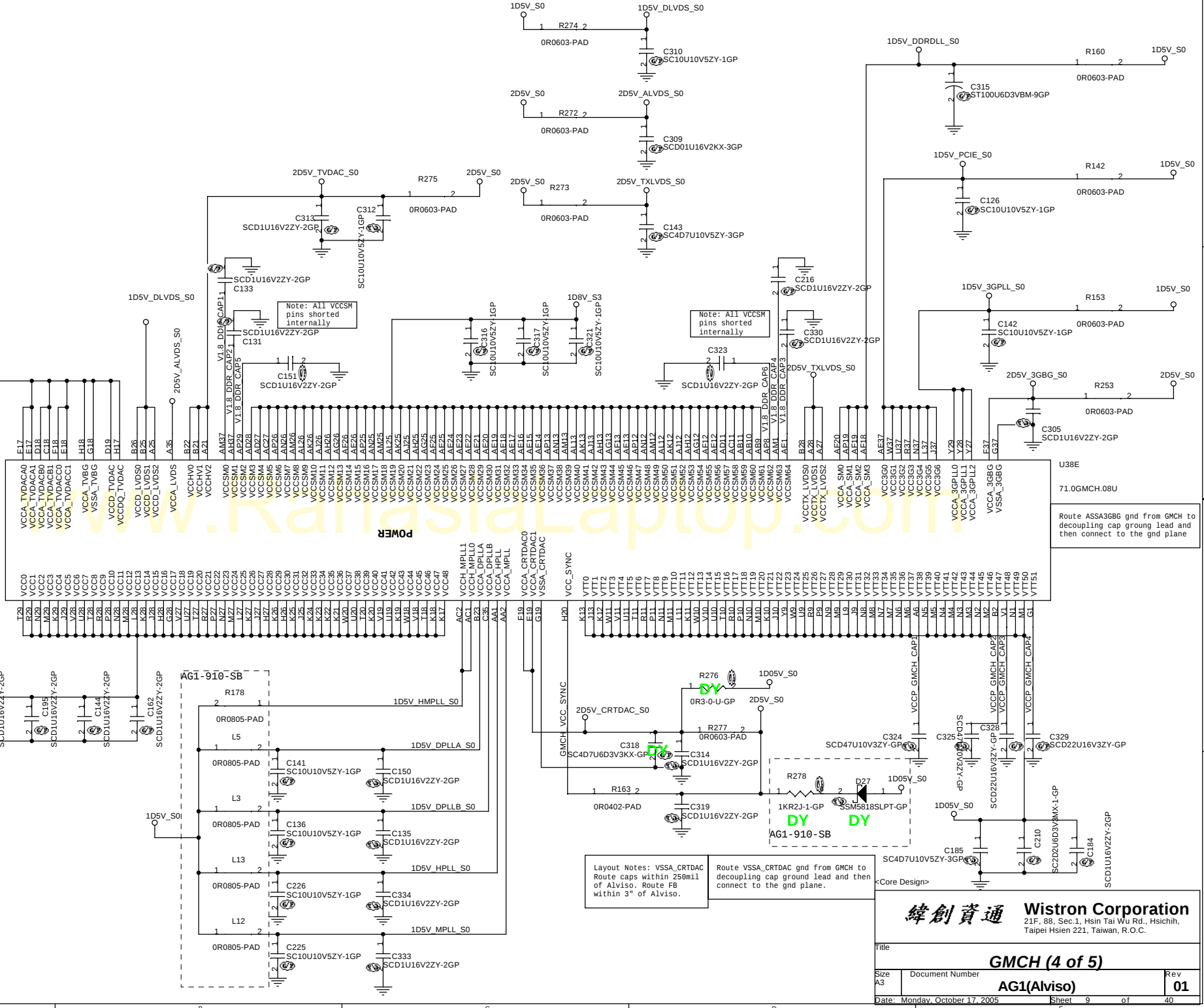
<Core Design>





Route ASSATVB6 gnd from GMCH to decoupling cap ground lead and then connect to the gnd plane

VCC 1D05_S0 for low speed graphic clock.1D5V_S0 for high speed clock.default use 1D05V_S0



POWER

POWER

POWER

POWER

POWER

POWER

POWER

POWER

POWER

POWER

POWER

POWER

POWER

POWER

POWER

POWER

POWER

POWER

POWER

POWER

POWER

POWER

POWER

POWER

Layout Notes: VSSA_CRTDAC
Route caps within 250mil of Alviso. Route FB within 3" of Alviso.

Route VSSA_CRTDAC gnd from GMCH to decoupling cap ground lead and then connect to the gnd plane.

<Core Design>

緯創資通

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Title

GMCH (4 of 5)

Size

A3

Document Number

AG1(Alviso)

Rev

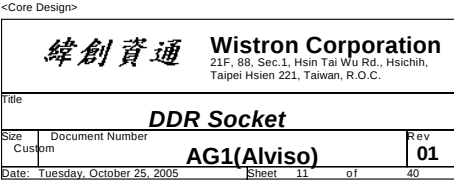
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Date

Monday, October 17, 2005

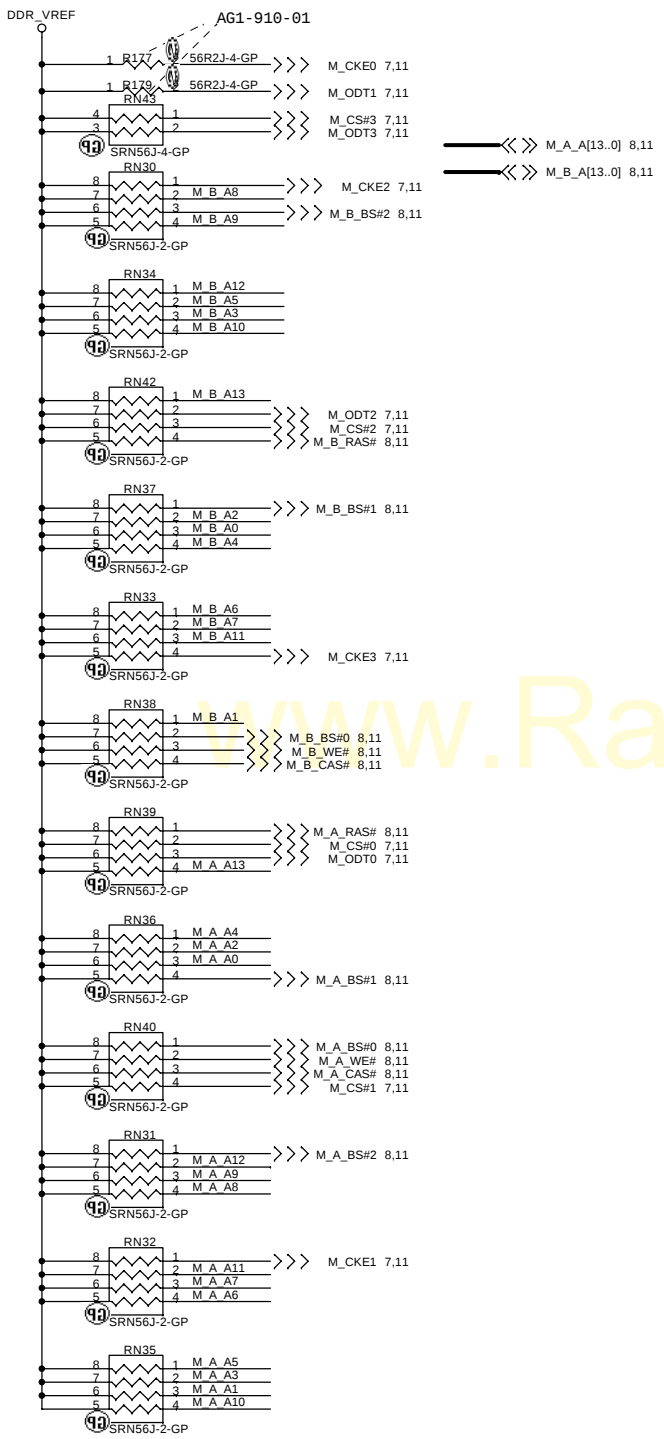
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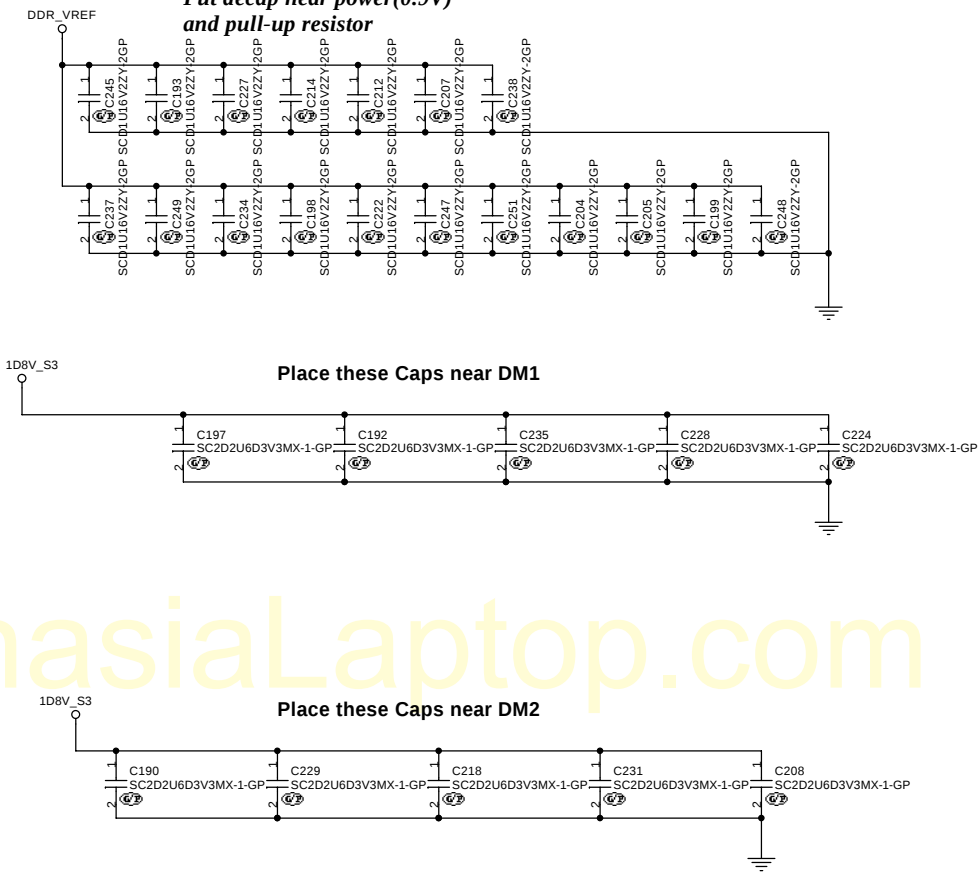
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

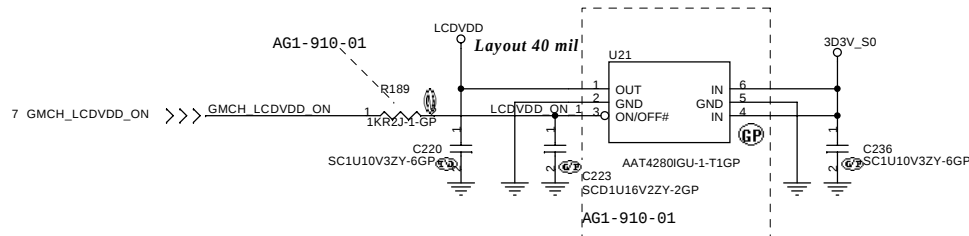


Decoupling Capacitor

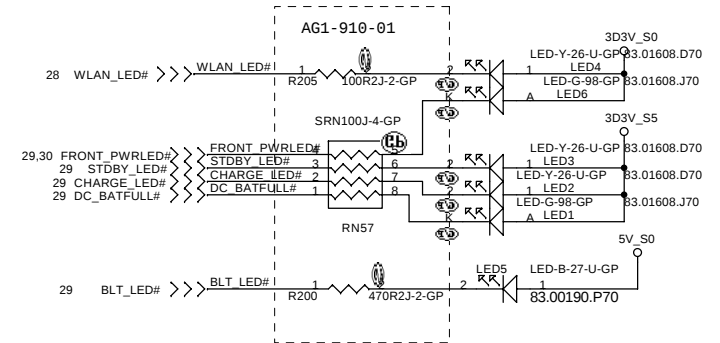
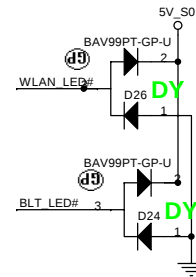
Put decap near power(0.9V) and pull-up resistor



LED



LCD/INVERTER/CCD CONN

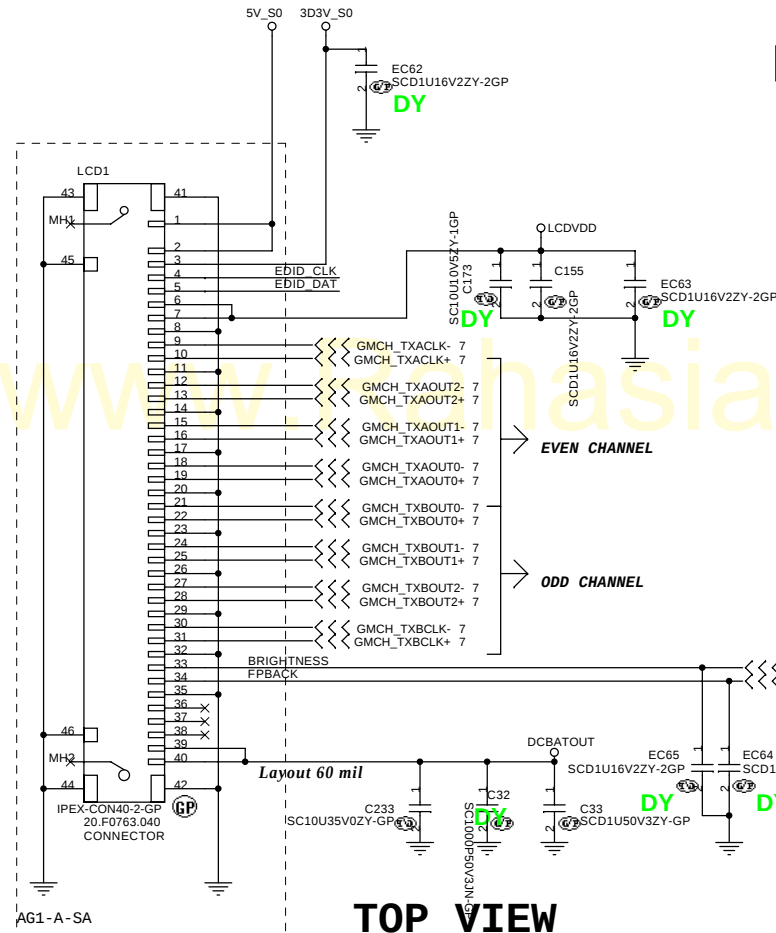


LED BD CONN

Pin	Symbol
1	5V
2	USB-
3	USB+
4	GND
5	GND

Pin	Symbol
1	Vin
2	Vin
3	PWM
4	BLON
5	GND
6	GND

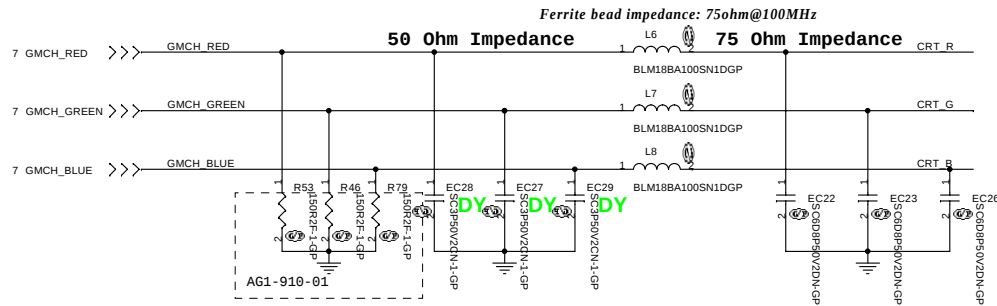
Pin	Symbol
1	5V_S0
2	PWRBTN#
3	PROGRAM#
4	EBUTTON#
5	INTERNET#
6	MAIL#
7	KCOL19
8	MAIL_LED#
9	STDBY_LED#
10	PWRLED#
11	GND
12	GND



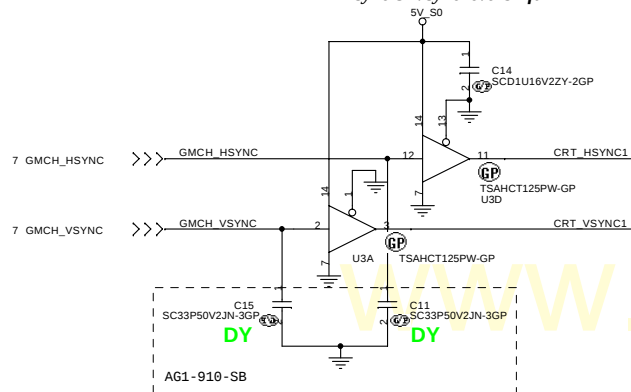
TOP VIEW

LCD

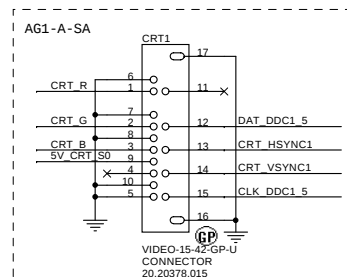
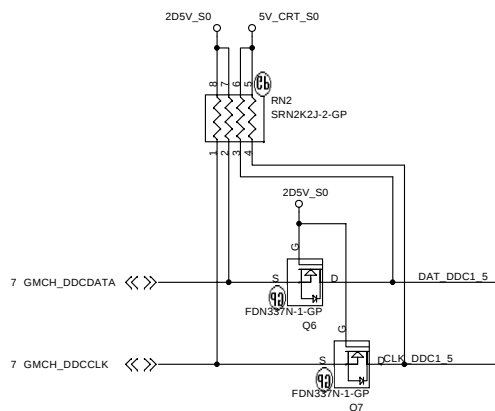
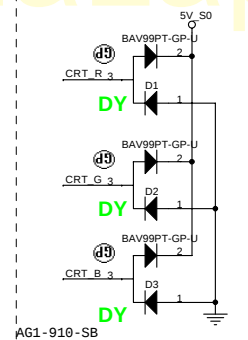
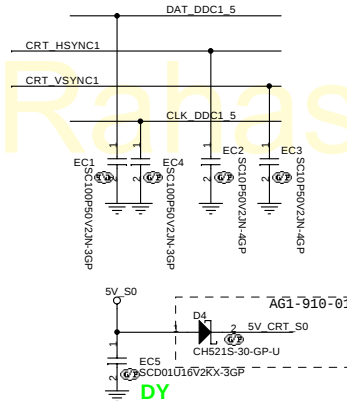
CRT CONNECTOR

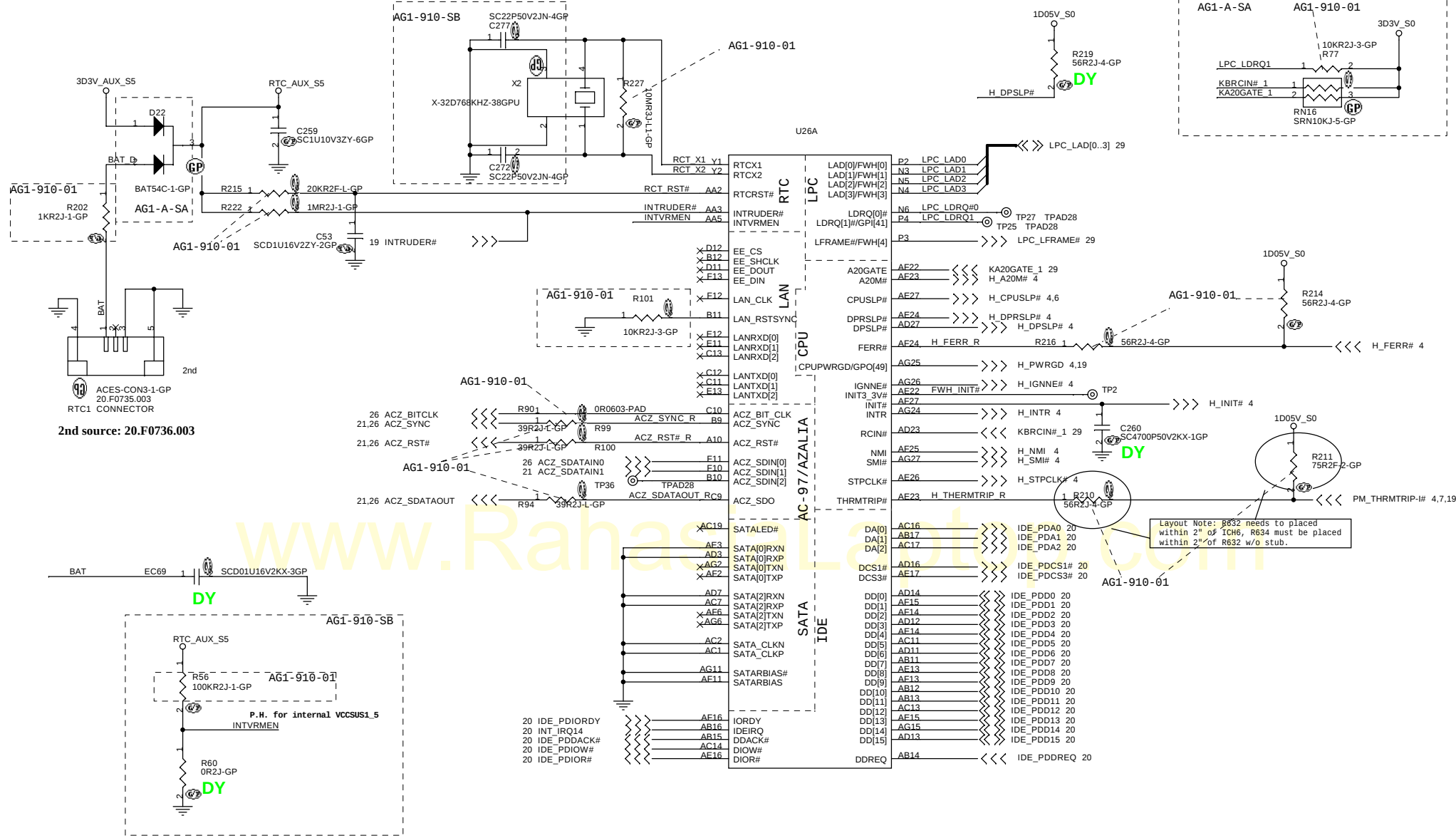


Hsync & Vsync level shift



DDC_CLK & DATA level shift







Layout Note:
Place above caps within
100 mils of ICH near F27, P27, AB27

Layout Note:
Place near pin AA19

Layout Note:
IDE decoupling

Layout Note:
PCI decoupling

Place within 100
mils of ICH
near pin AG5

Place within 100
mils of ICH
near pin AG9

Place within 100
mils of ICH
near E26, E27

Place within 100
mils of ICH
pin AG18

Place within 100
mils of ICH
pin A13

Place within 100
mils of ICH
pin V7

Place within 100
mils of ICH pin
AG13, AG16

Layout Note:
Distribute in PCI section
near pin A2-A6 near D1-H1

Place both
within 100 mils
of ICH near D27

Layout Note:
Place near AB18

Place within 100
mils of ICH

Layout Note:
Place near AG23

Place within 100
mils of ICH
pin A17

*Within a given well, 5VREF needs to be up before the
corresponding 3.3V rail

Layout Note:
Place near ICH6

Place within 100
mils of ICH

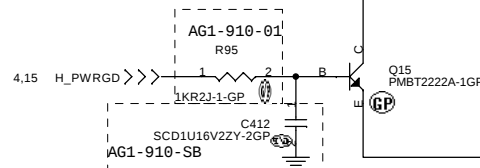
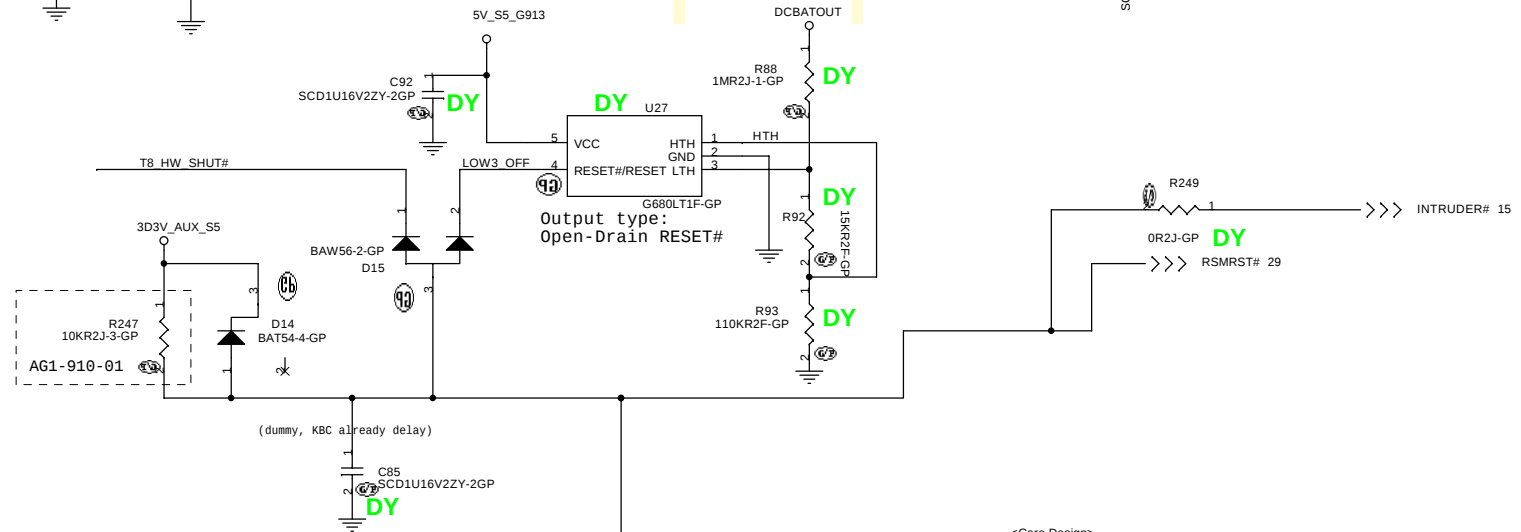
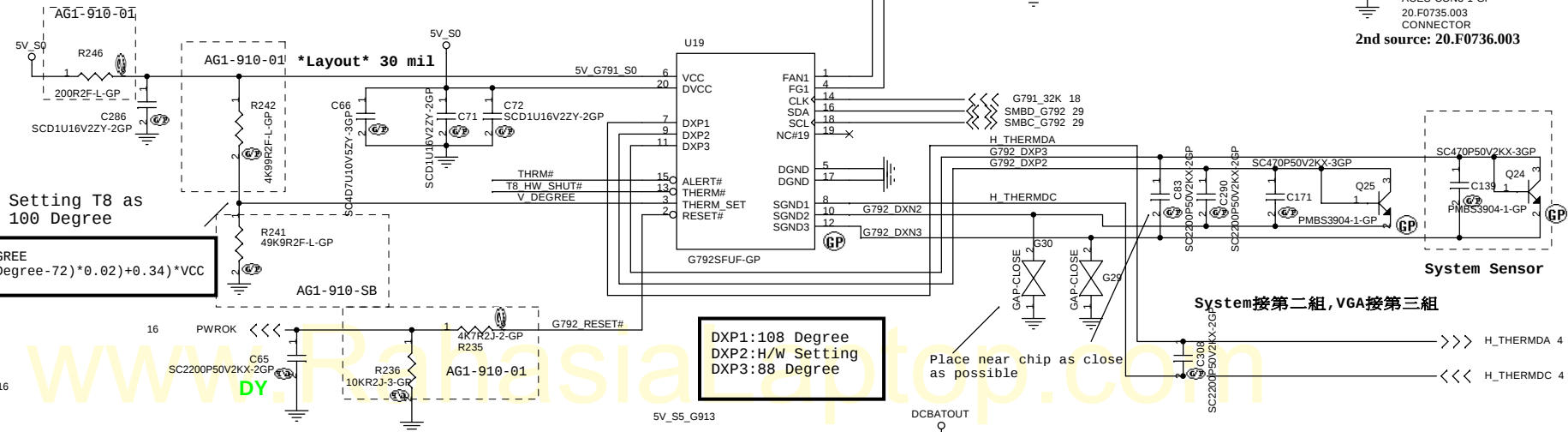
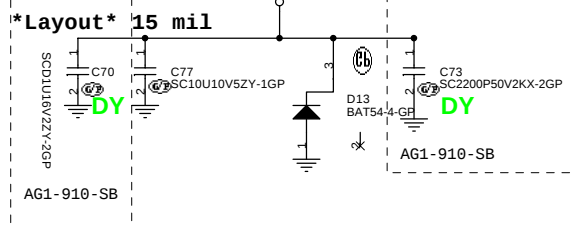
Layout Note:
Place near AB3

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title			
ICH6-M (3 of 4)			
Size	Document Number	Rev	
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Date:	Monday, October 31, 2005	Sheet	17 of 40



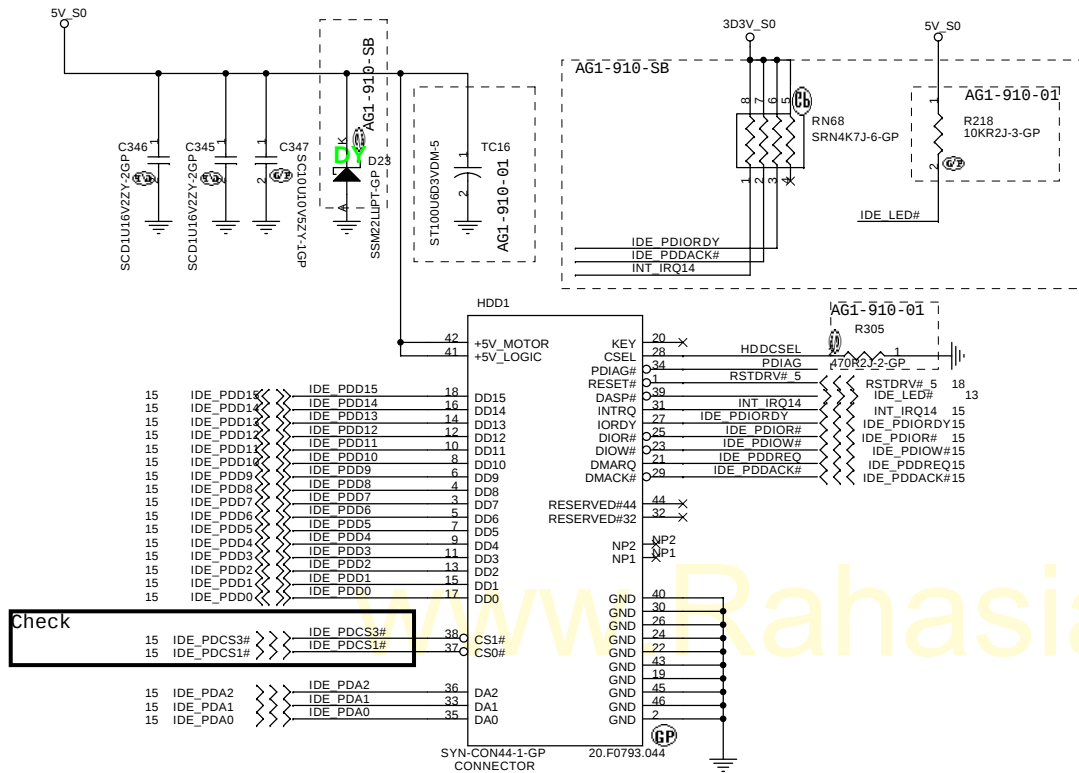


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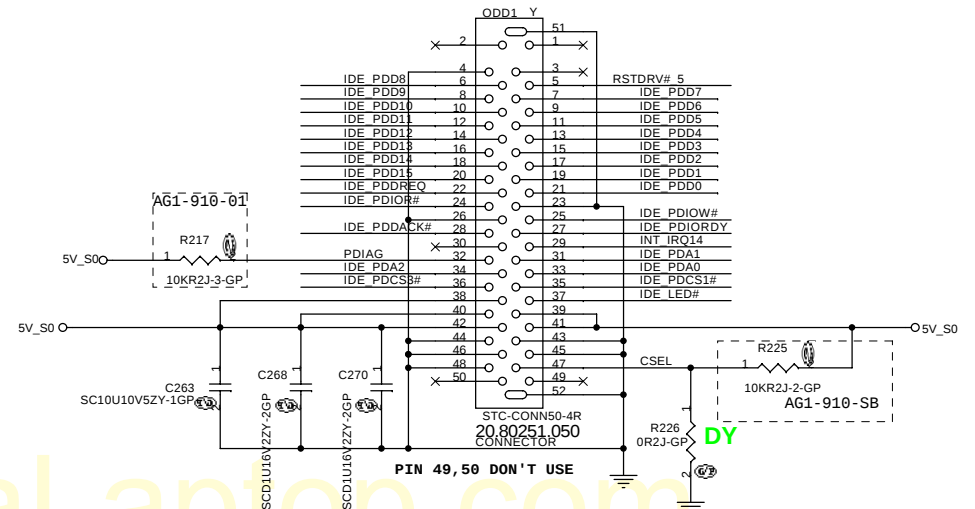
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title			Thermal/Fan Controller	
Size	Custom	Document Number	AG1(Alviso)	
Date	Thursday, October 27, 2005	Sheet	19	of 40
Rev	01			

HDD Connector



CD-ROM Connector

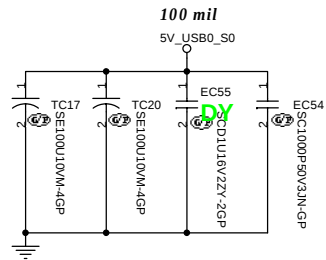
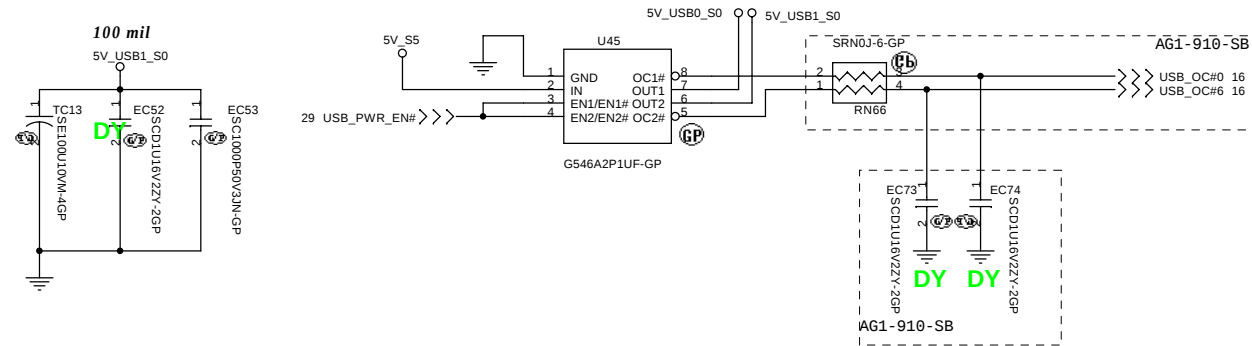


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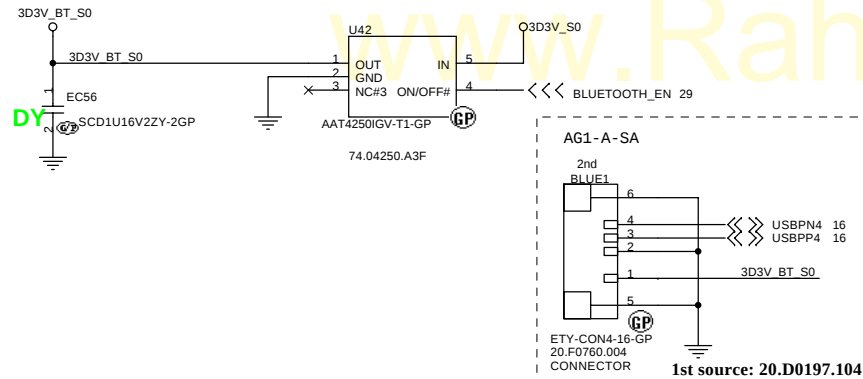
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
HDD and CDROM		
Size	Document Number	Rev
A3	AG1(Alviso)	01
Date:	Monday, October 31, 2005	Sheet 20 of 40

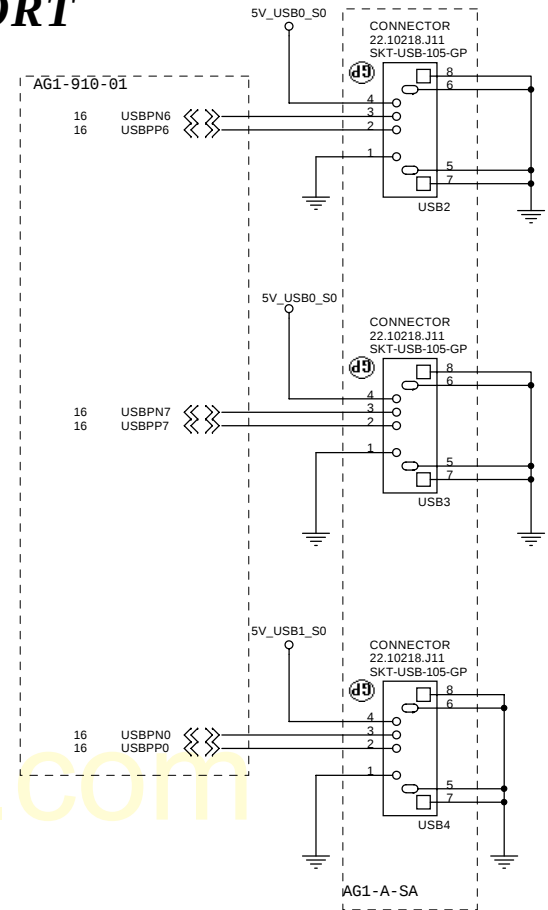
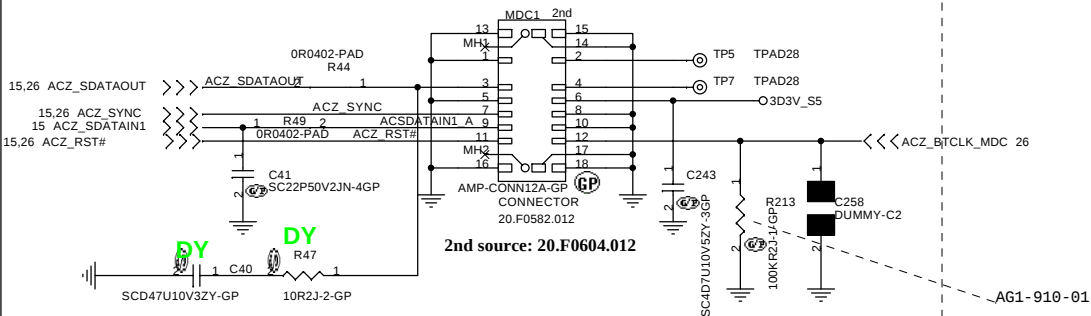
USB PORT

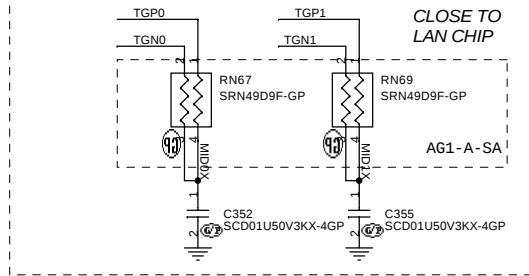


BLUETOOTH MODULE



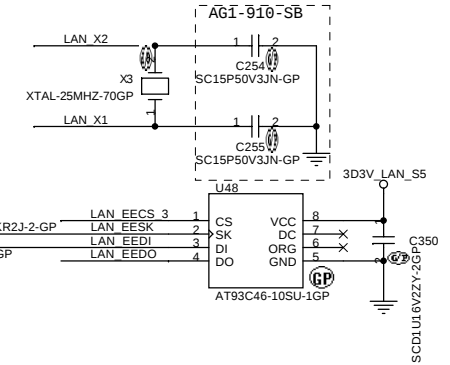
MDC 1.5 CONNECTOR



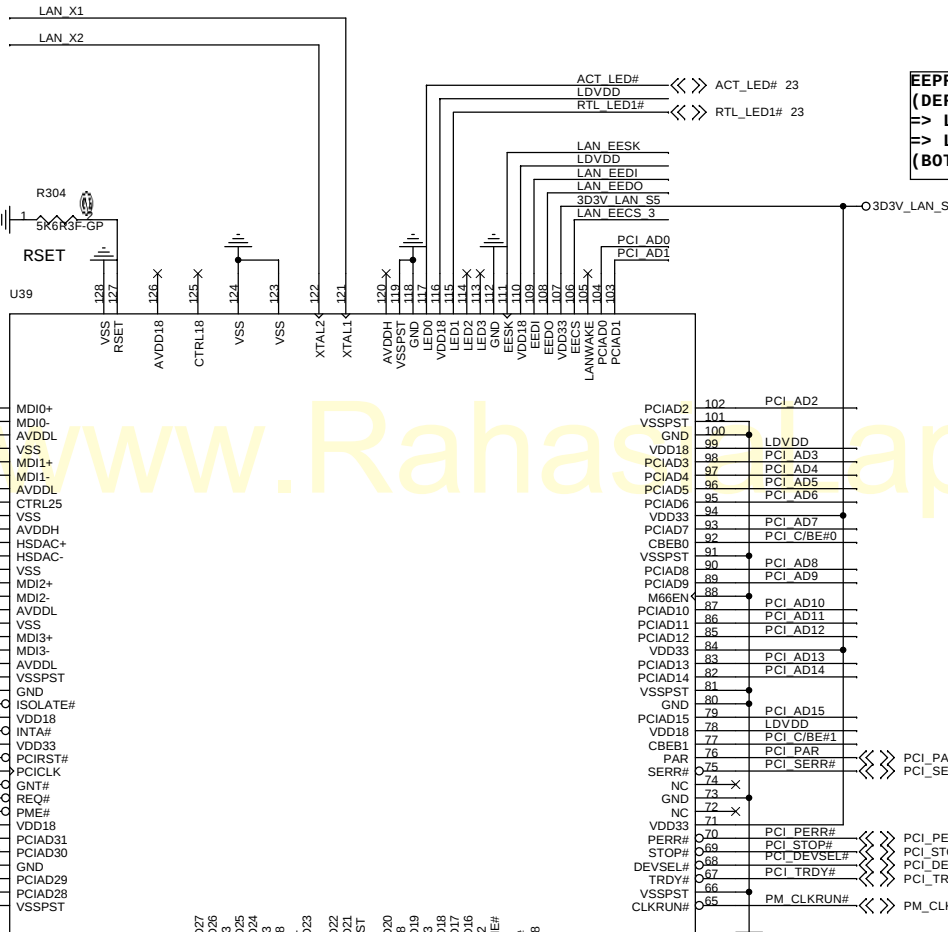


16,24,28 PCI_C/BE#[3..0] <<<

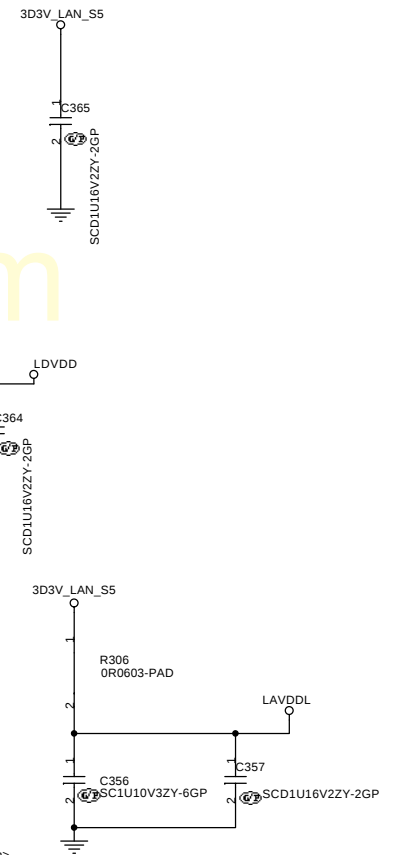
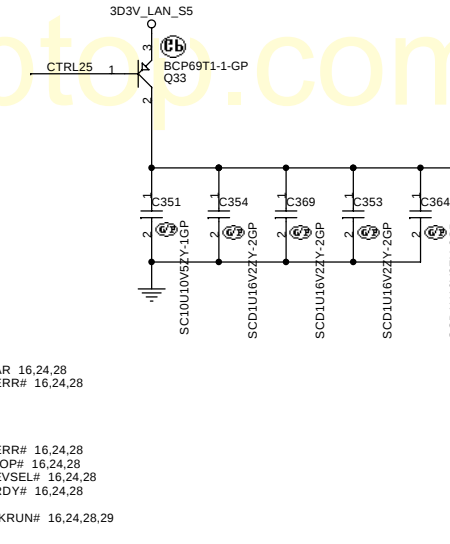
16,24,28 PCI_AD[31..0] <<<



EEPROM LED OPTION USE '01'
(DEFINED IN SPEC)
=> LED0 : ACT
=> LED1 : LINK
(BOTH 10/100 AND GIGA CHIP)



GIGALAN: RTL8110SBL
10/100 LAN: RTL8100C



<Core Design>

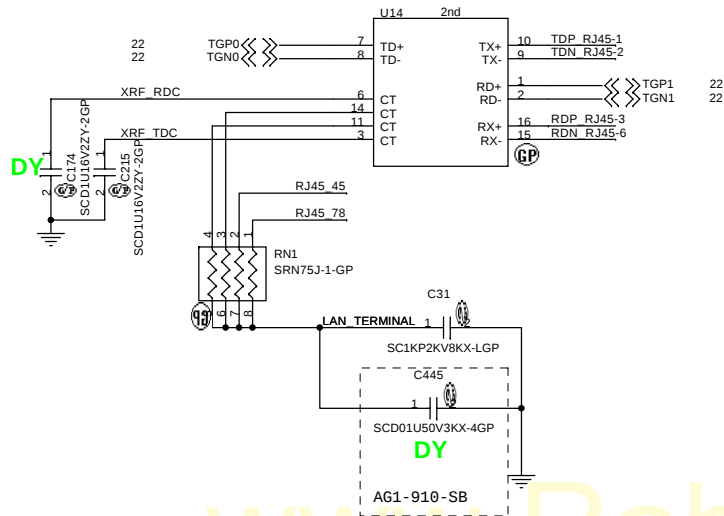
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **RTL8100CL**

Size: A3 Document Number: **AG1(Alviso)** Rev: **01**

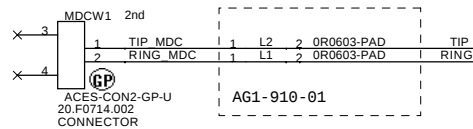
Date: Tuesday, October 25, 2005 Sheet: 22 of 40

10/100M Lan Transformer

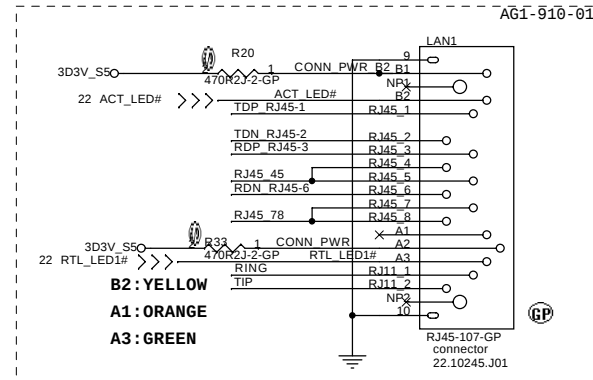


- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width,12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

LAN Connector



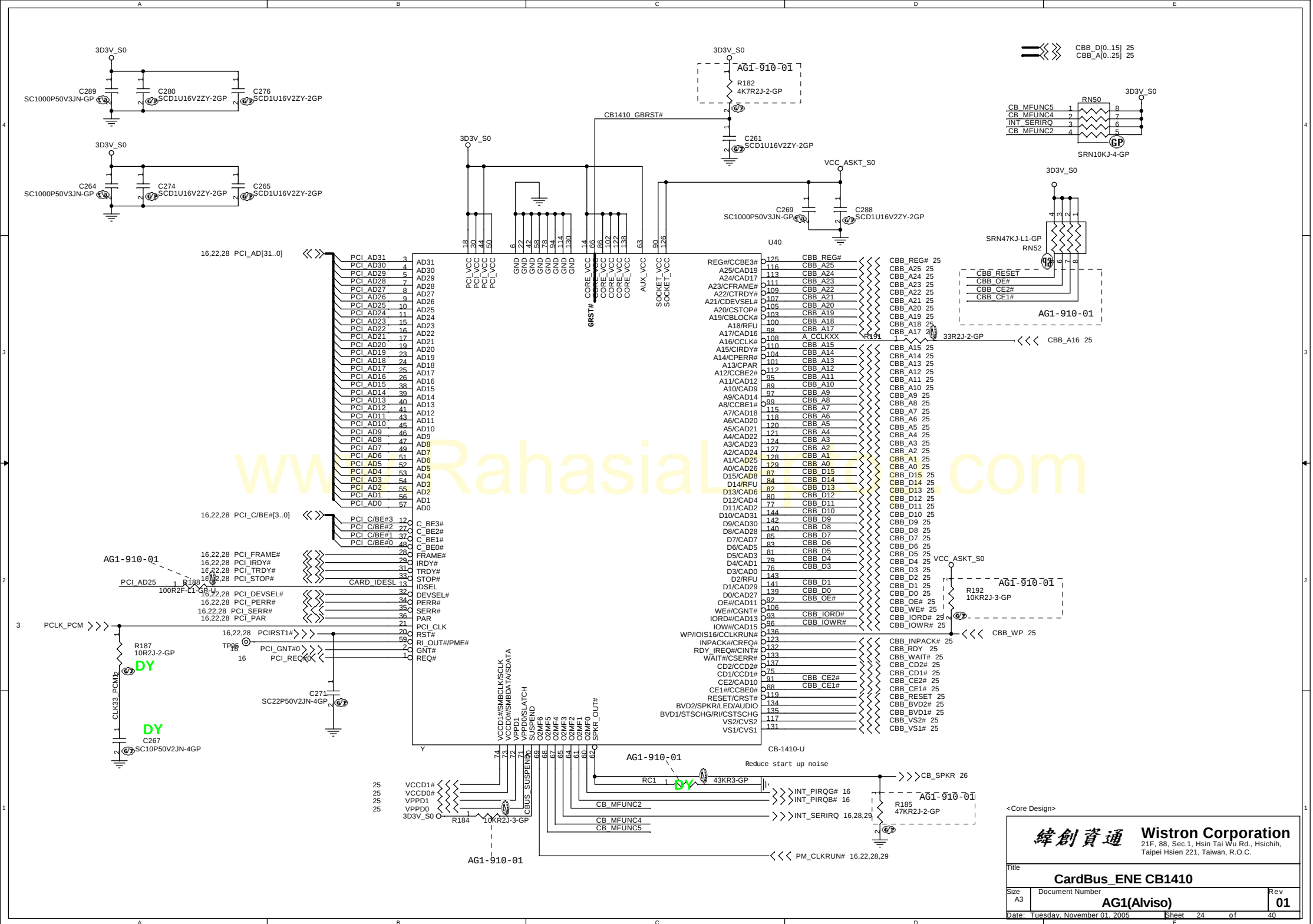
2nd source: 20.D0196.102



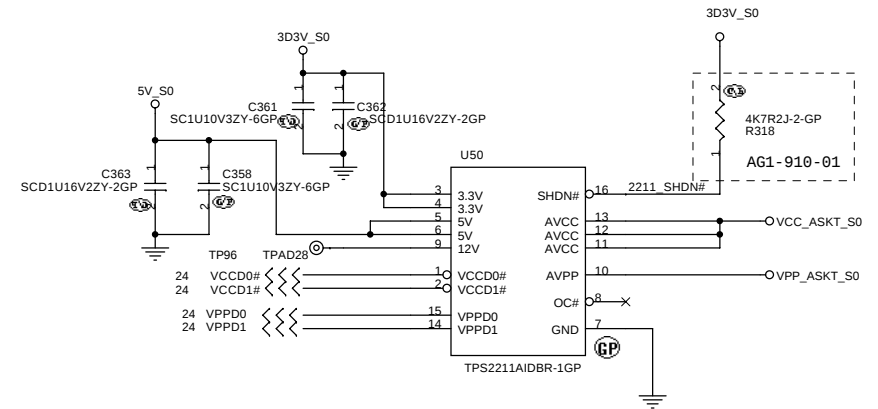
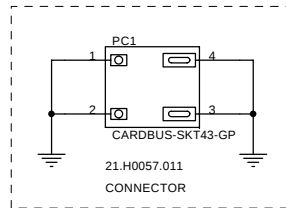
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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

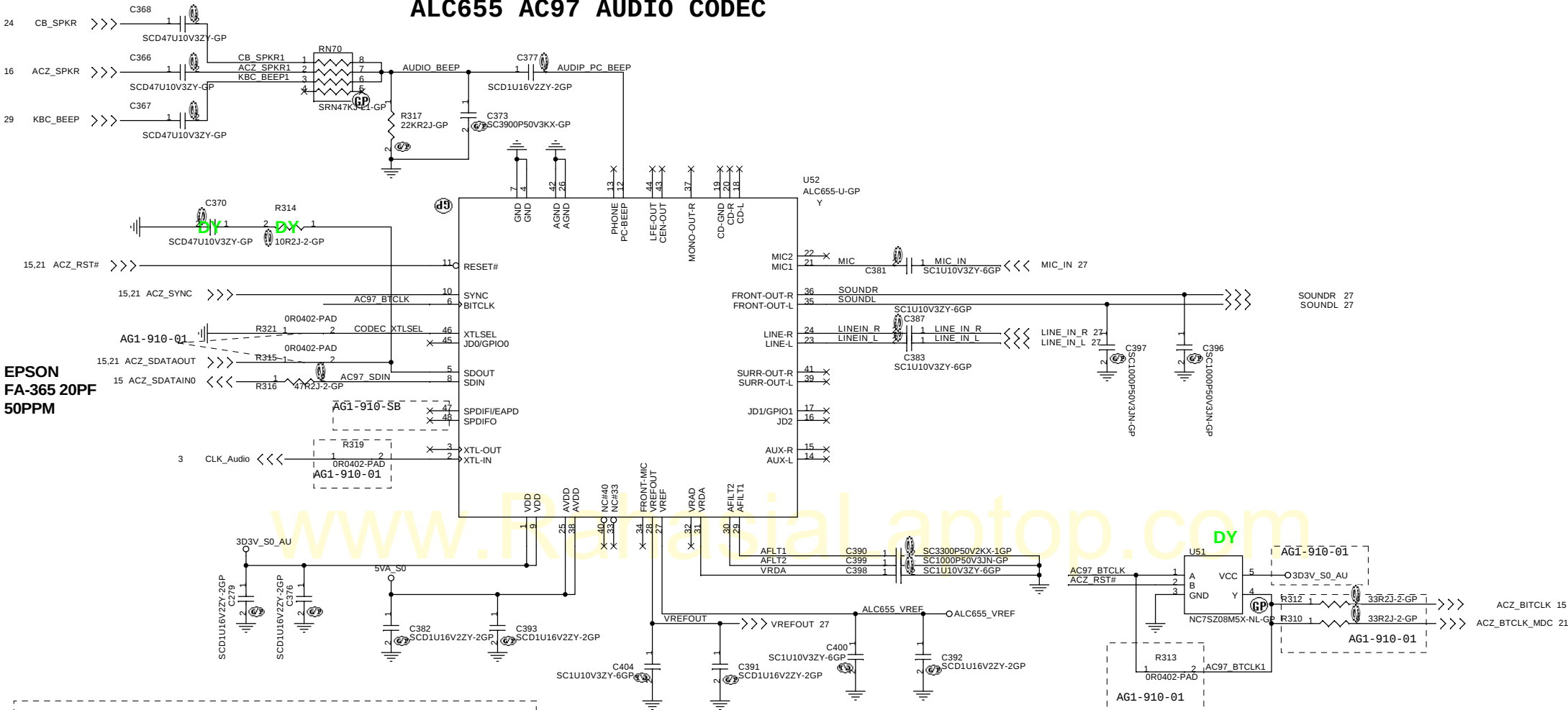
Title			LAN CONN	
Size	Document Number	AG1(Alviso)		Rev
A3				01
Date: Saturday, October 29, 2005			Sheet 23 of 40	



Power switch

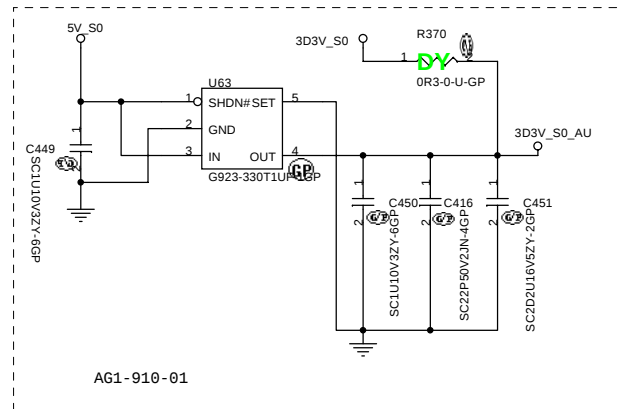
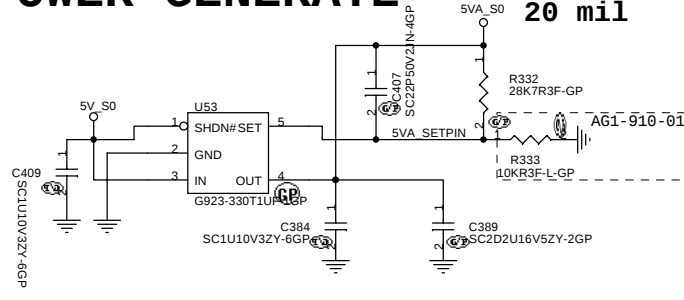


ALC655 AC97 AUDIO CODEC



POWER GENERATE

Layout
20 mil



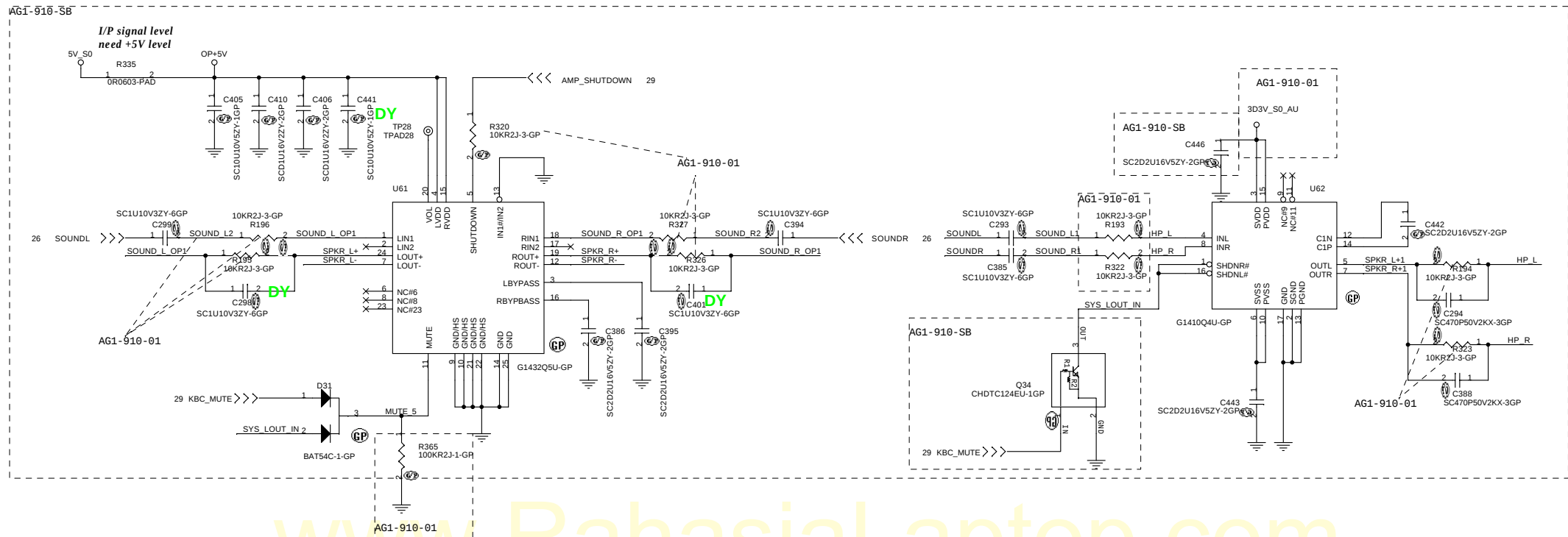
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緯創資通

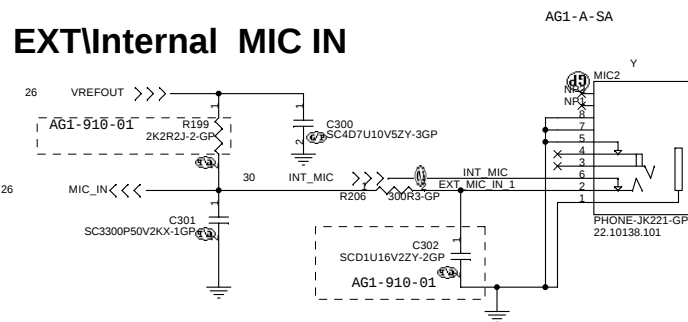
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
AC'97 CODEC - ALC655			
Size	Document Number		Rev
A3	AG1(Alviso)		01
Date: Tuesday, November 01, 2005		Sheet 26 of 40	

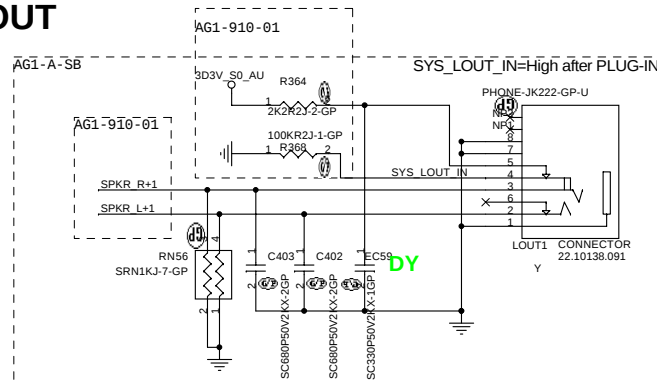
AUDIO OP AMPLIFIER



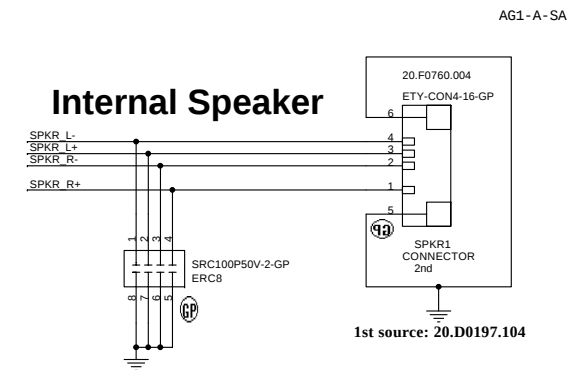
EXT/ Internal MIC IN



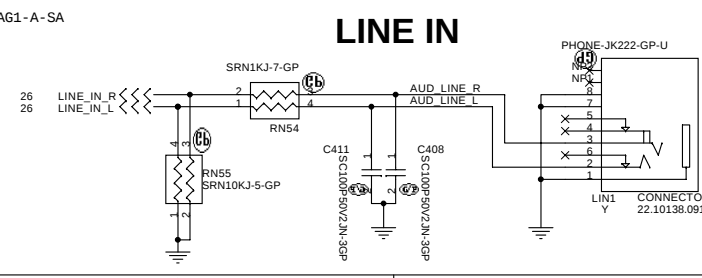
LINE OUT



Internal Speaker



LINE IN



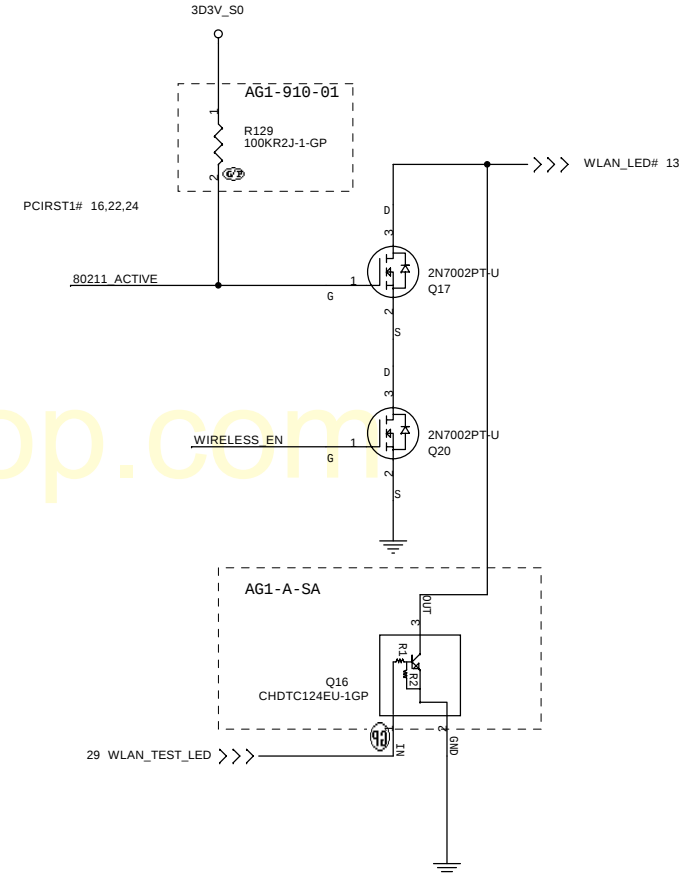
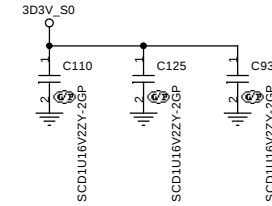
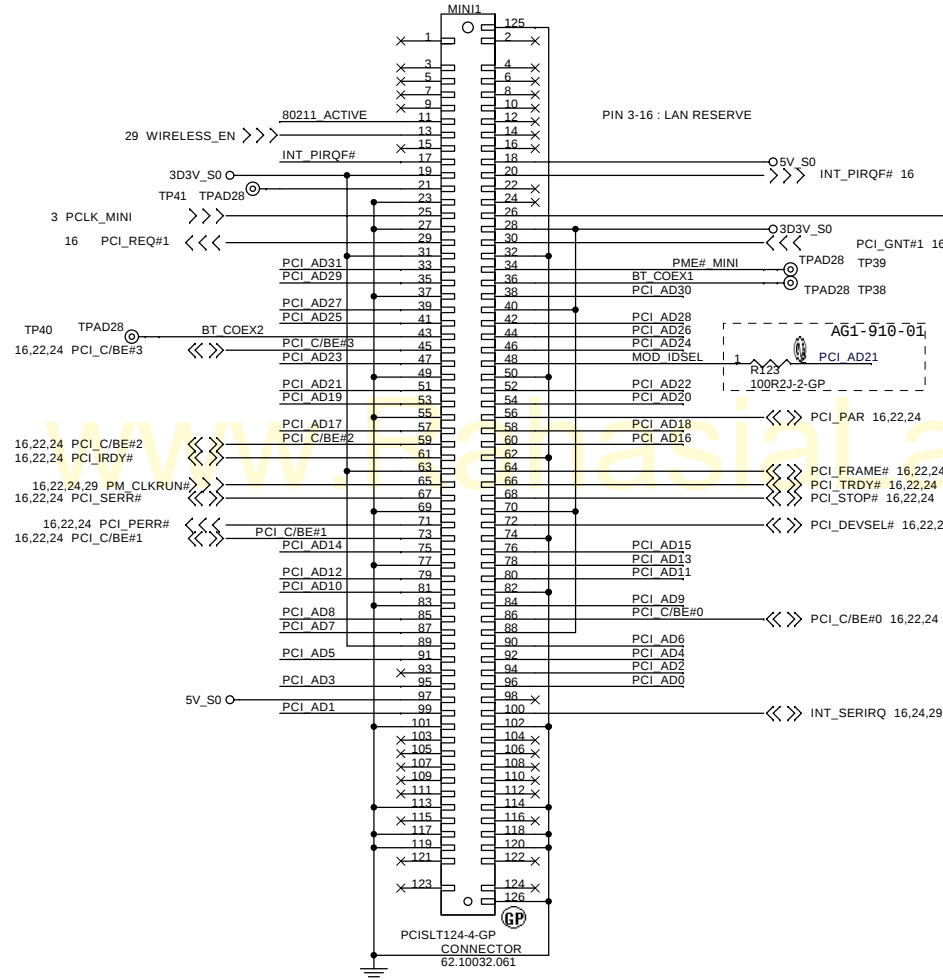
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緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title			Audio AMP and Jack
Size	Document Number	Rev	
AG1(Alviso)			01
Date: Monday, October 31, 2005	Sheet	27	of 40

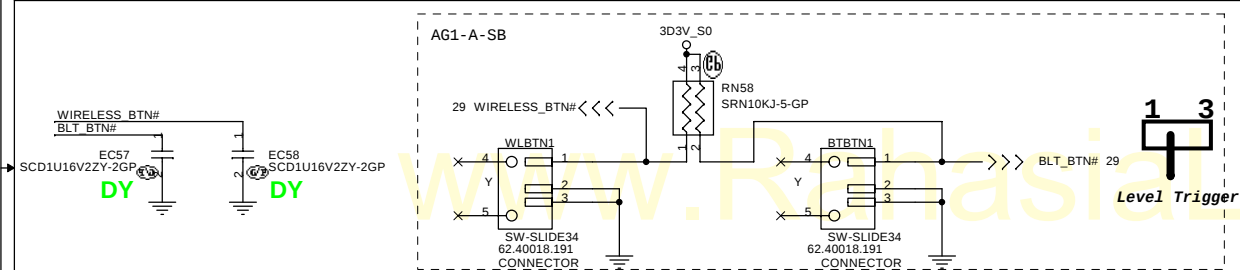
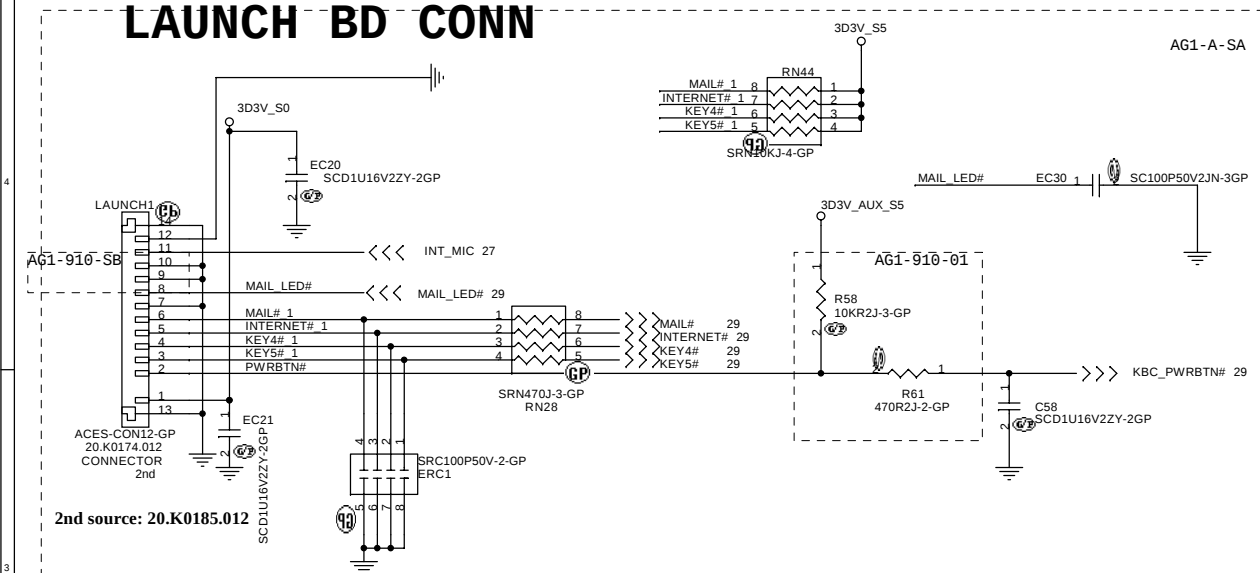
16,22,24 PCI_AD[31..0]

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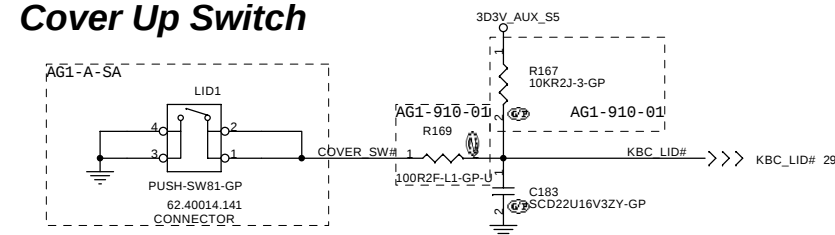


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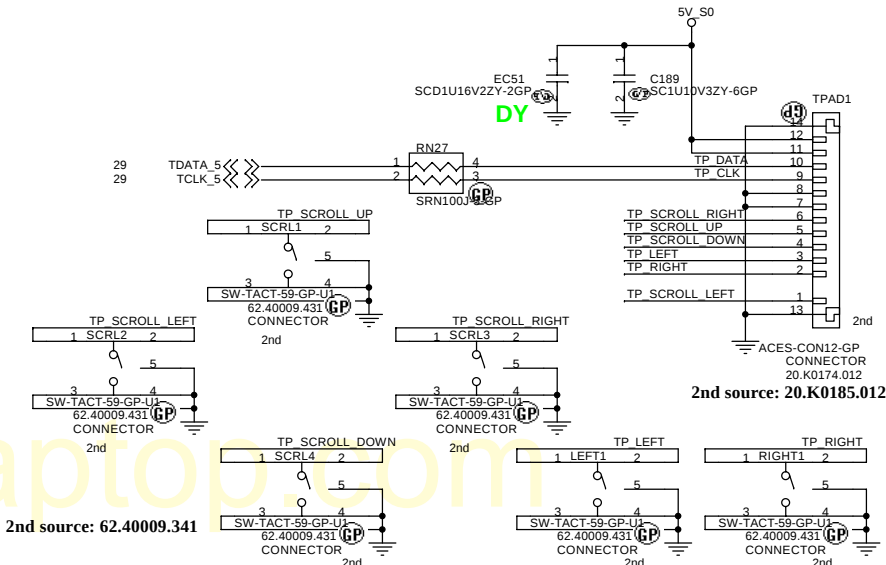
LAUNCH BD CONN



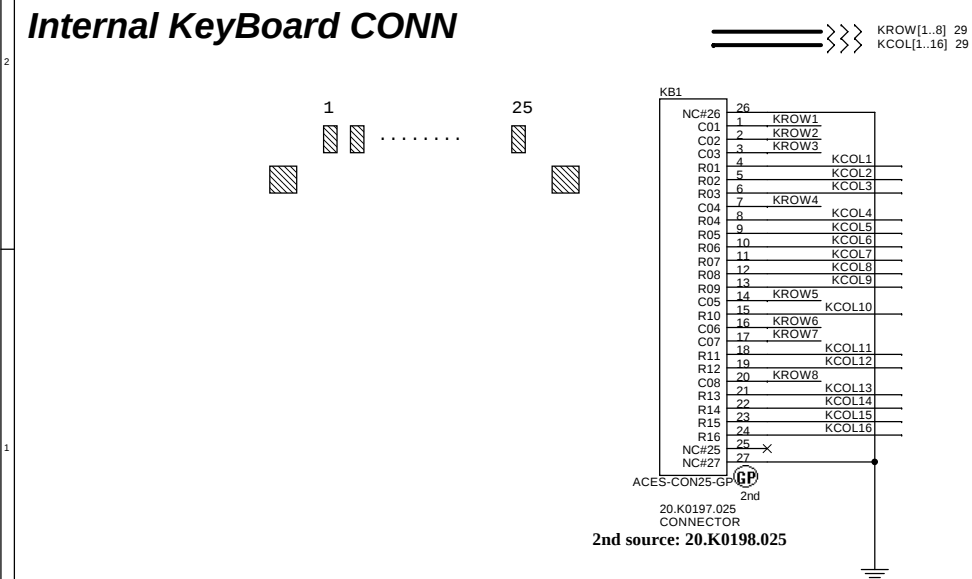
Cover Up Switch



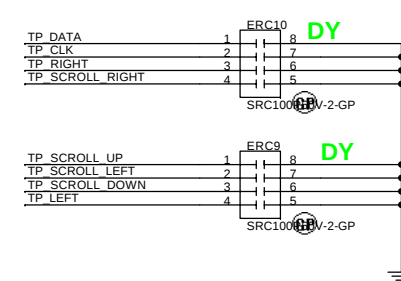
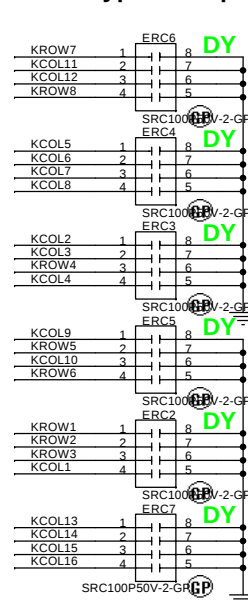
TOUCH PAD



Internal KeyBoard CONN



EMI Bypass cap.



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title	BUTTONs / KB / TOUCHPAD
-------	--------------------------------

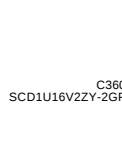
Size A3	Document Number AG1-910	Rev 01
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Date: Tuesday, November 01, 2005 Sheet 30 of 40

>>> KBC_D[0..7] 29

29 KBCBIOS_WE#
29 KBCBIOS_RD#
29 KBCBIOS_CS#

29 KBC_D0
29 KBC_D1
29 KBC_D2
29 KBC_D3
29 KBC_D4
29 KBC_D5
29 KBC_D6
29 KBC_D7



3D3V_AUX_S5

C360

SCD1U16V2ZY-2GP

U49

32

VDD

CE#

OE#

WE#

DQ0

DQ1

DQ2

DQ3

DQ4

DQ5

DQ6

DQ7

VSS

16

A0

A1

A2

A3

A4

A5

A6

A7

(SOCKET) 62.10002.032 - (IC)72.39040.H03 IN DIP,SMT

ROM SIZE MAX. 512KBYTE

PLCC32 Socket P/N:
SSKT3262.10002.032
SSKT32 62.10005.032

3D3V_S0

SRN10KJ-5-GP
RN8

9

AG1-910-01

Plz put G12 close SW1

PH at ICH6M

1

2

GAP-OPEN

G12

SW1

1

2

3

4

5

6

7

8

SW-DIP-4-2-U2-GP

CONNECTOR

DY

EC44
SC1000P50V33N-GP
DY

16 CHK_PW#
29 MATRIXID1#
29 MATRIXID2#

Keyboard matrix (from vendor)

		US	Jap	Eur	Other
Low Bit	MATRIXID1#	1	1	0	0
High Bit	MATRIXID2#	1	0	1	0

Board ID

3D3V_S0

R243
10KR2J-3-GP
DY

R221
10KR2J-3-GP
DY

R245
10KR2J-3-GP
DY

R220
10KR2J-3-GP
DY

16 PCB_VER0
16 PCB_VER1

PCB VER0
PCB VER1

Planar ID(2,1,0)

SA:

SB:

-1 :

<Core Design>

緯創資通

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

BIOS ROM

Size
A3

Document Number

AG1-910

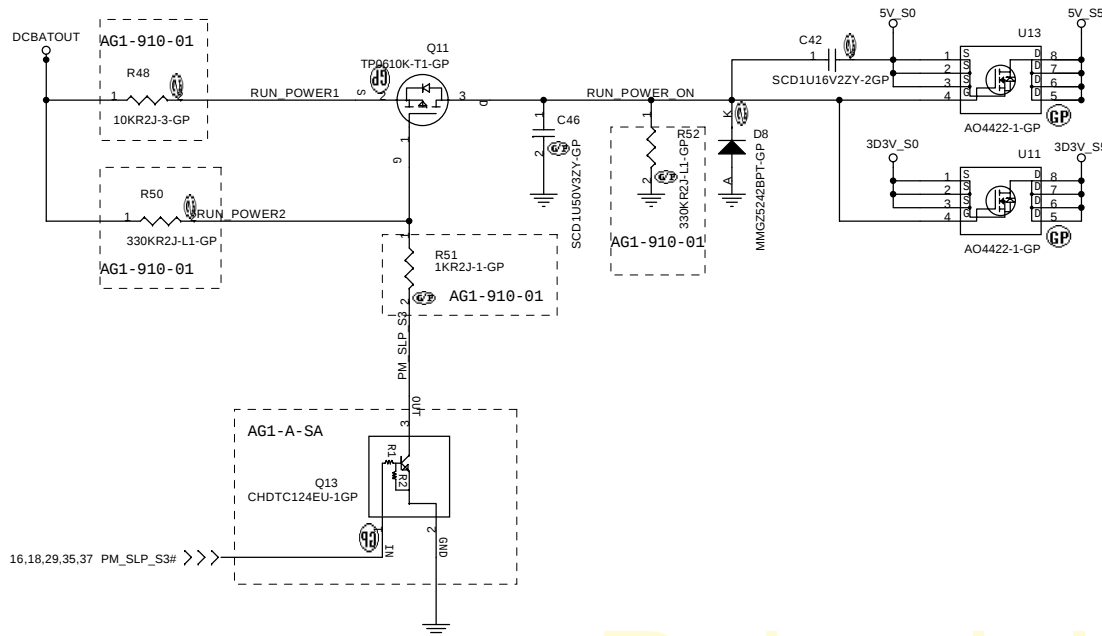
Rev

01

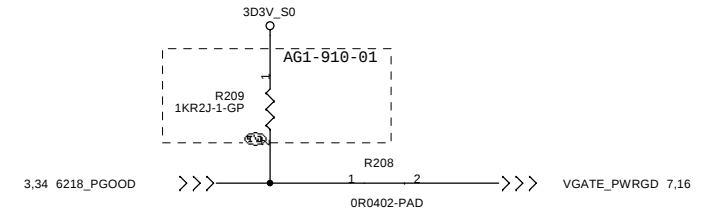
Date: Tuesday, November 01, 2005

Sheet 31 of 40

Run Power



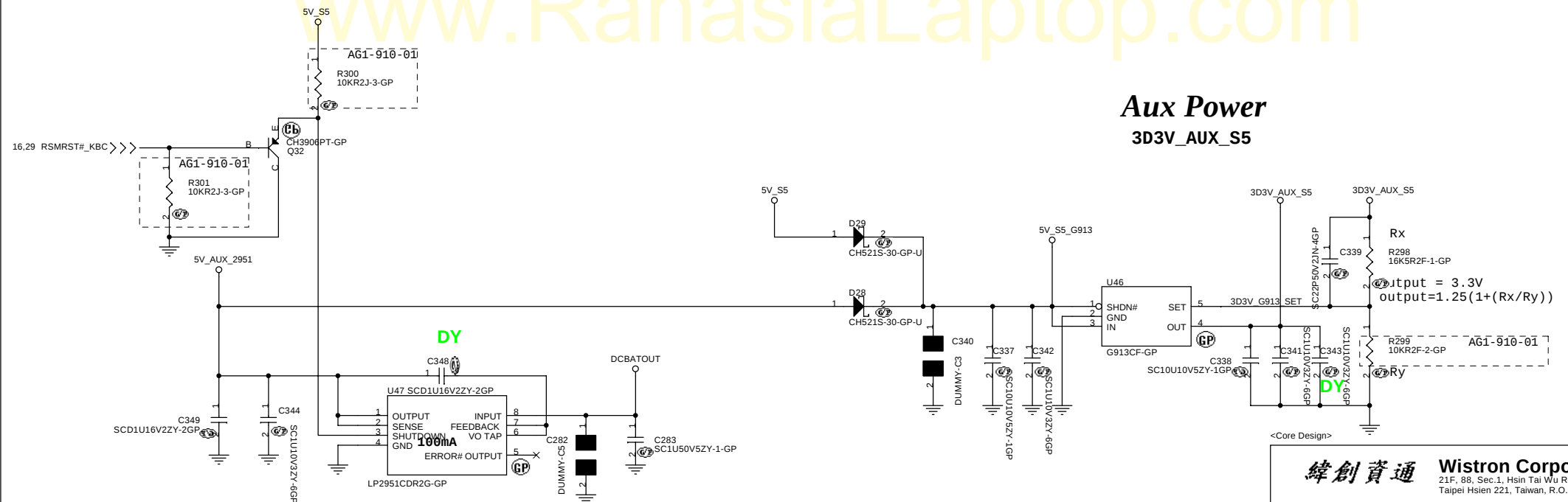
PWRGD for NB and SB



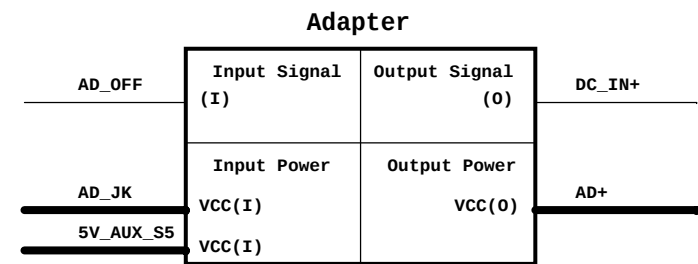
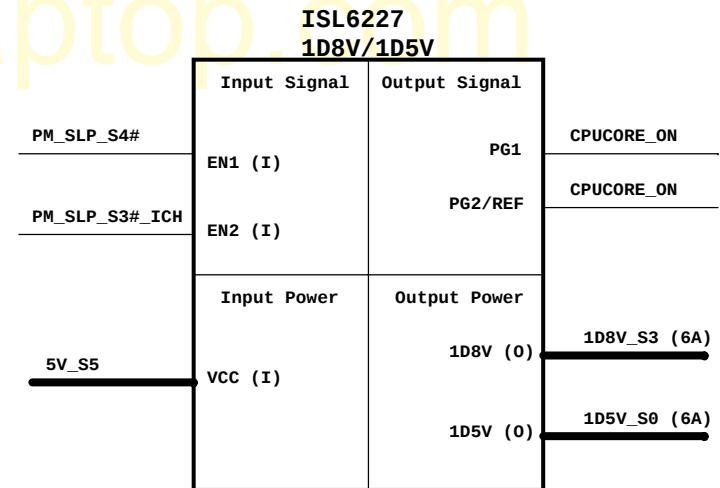
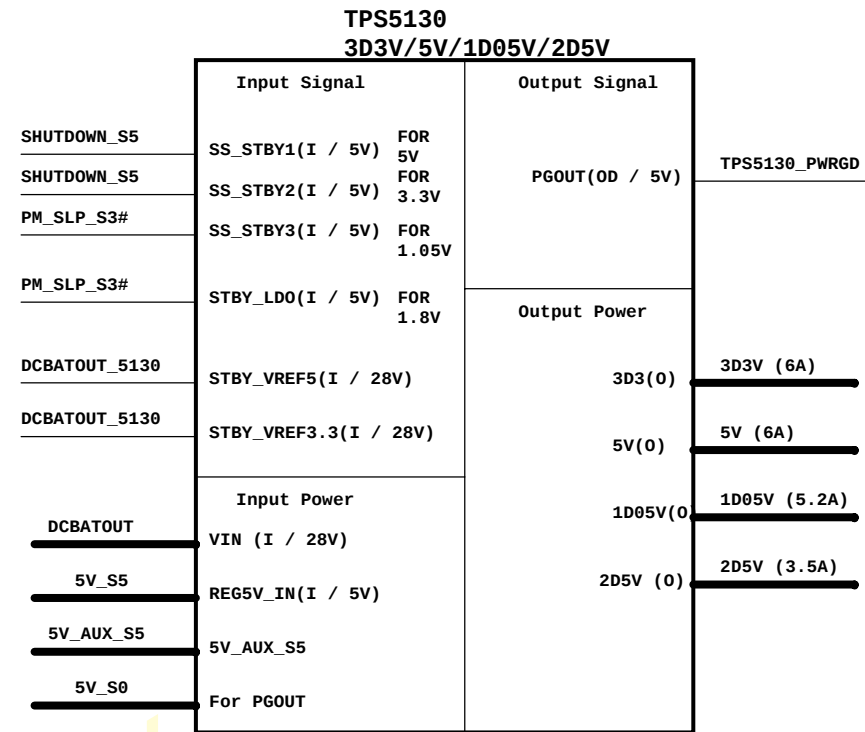
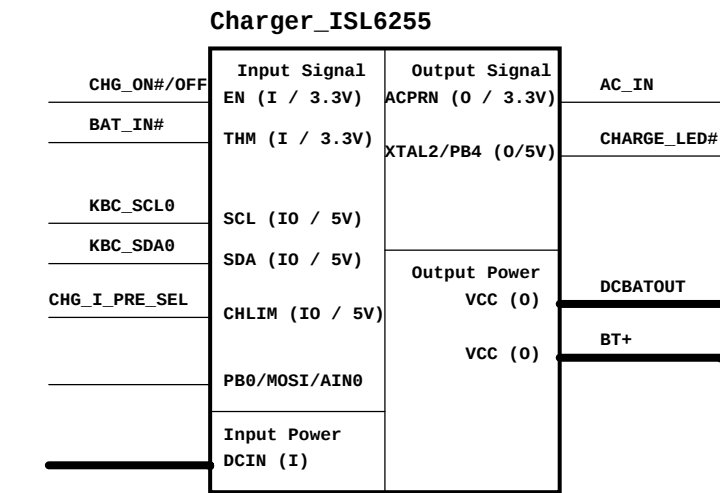
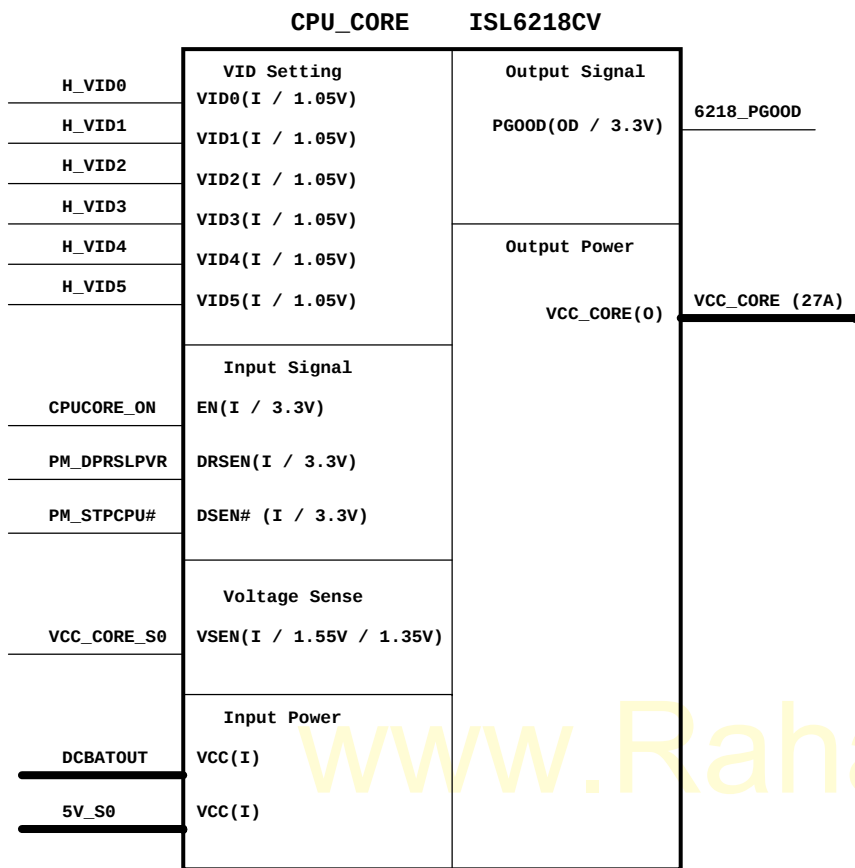
PWRGD to Turn on CPU_Core_Power

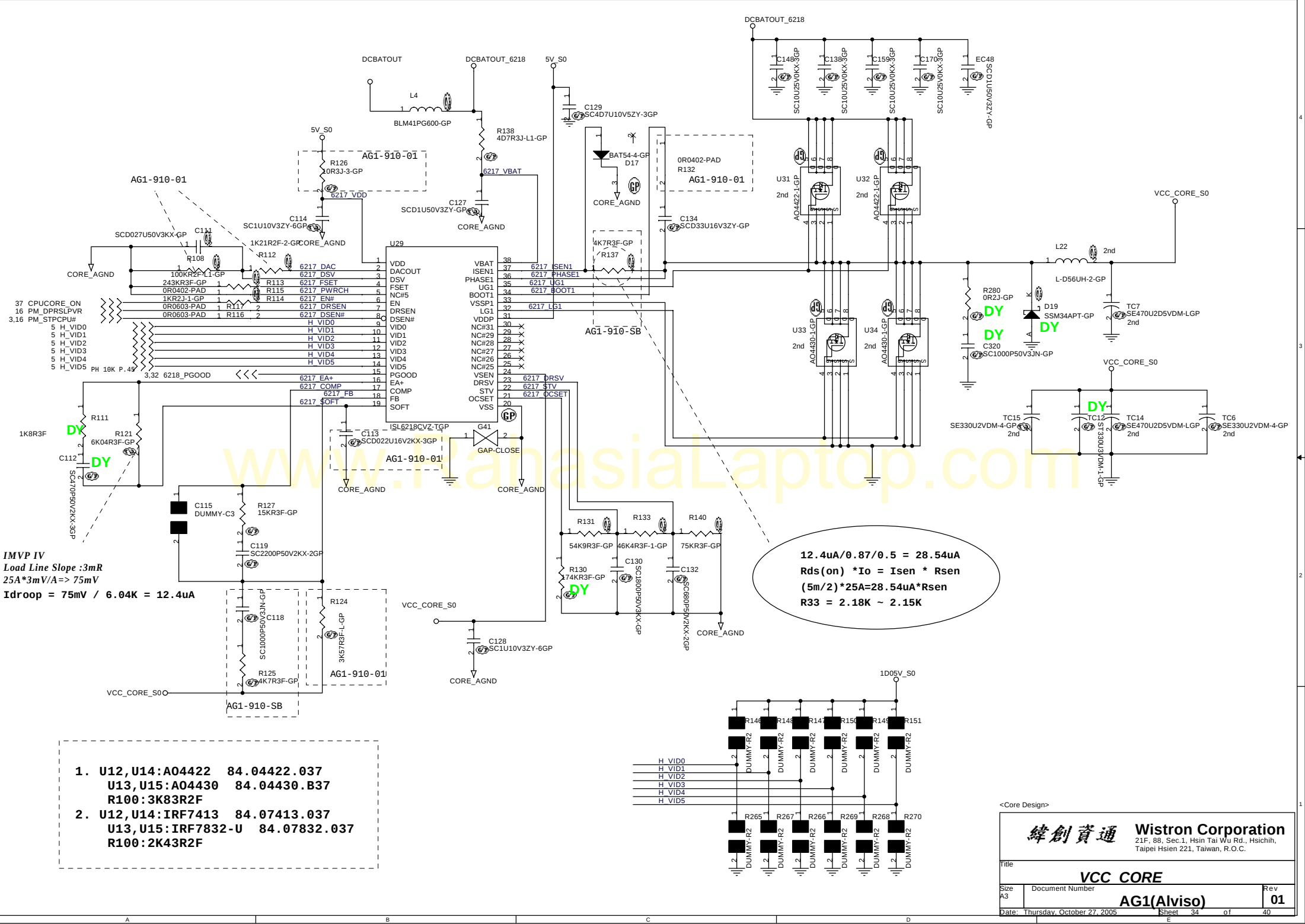
Aux Power

3D3V_AUX_S5



<Core Design>

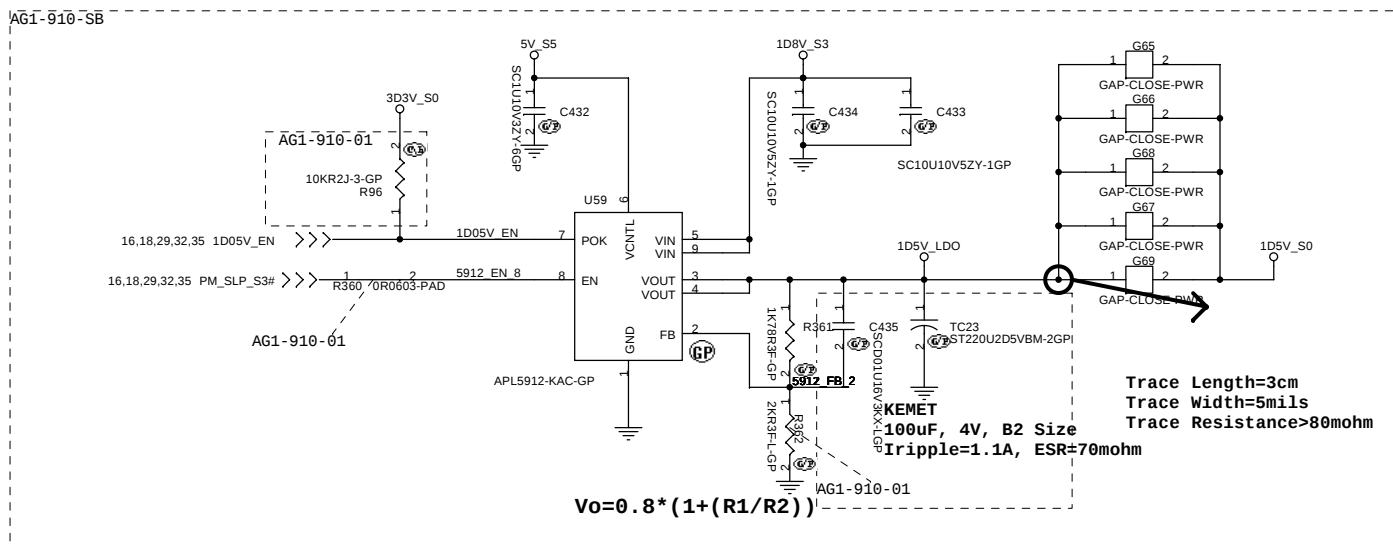




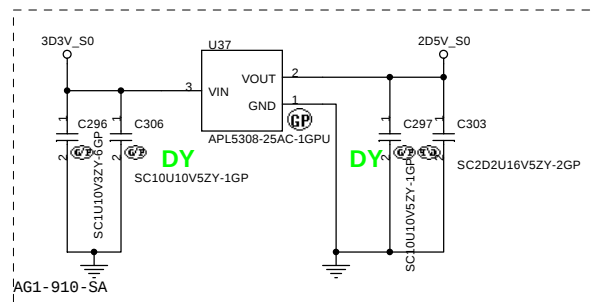
IMVP IV
Load Line Slope :3mR
25A*3mV/A=> 75mV
Idroop = 75mV / 6.04K = 12.4uA

$$12.4\mu A / 0.87 / 0.5 = 28.54\mu A$$
$$R_{ds(on)} * I_o = I_{sen} * R_{sen}$$
$$(5m/2) * 25A = 28.54\mu A * R_{sen}$$
$$R33 = 2.18K \sim 2.15K$$

- 1. U12,U14:A04422 84.04422.037
U13,U15:A04430 84.04430.B37
R100:3K83R2F
- 2. U12,U14:IRF7413 84.07413.037
U13,U15:IRF7832-U 84.07832.037
R100:2K43R2F



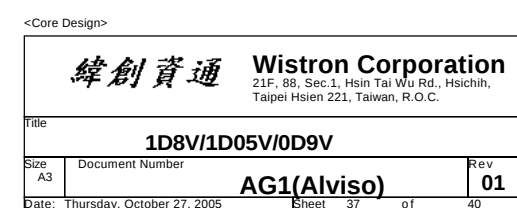
www.RahasiaLaptop.com

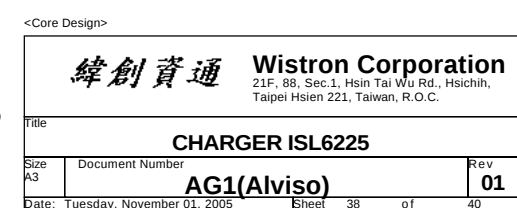


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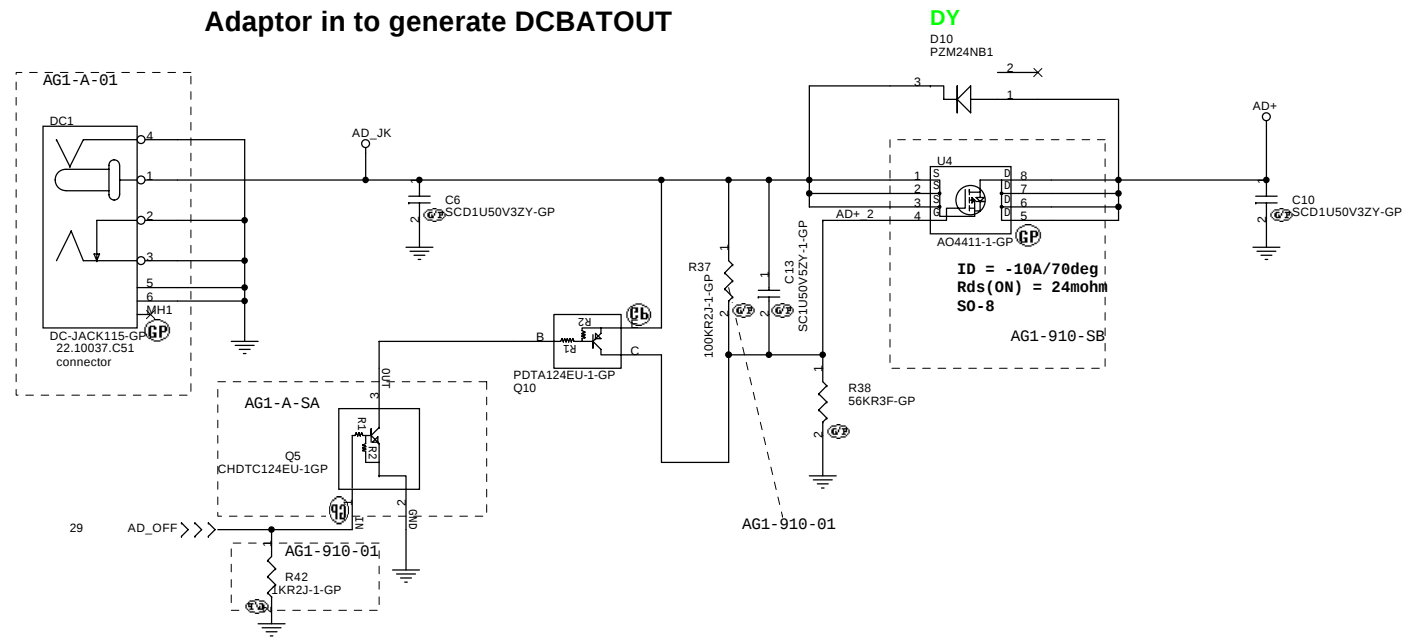
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
1D5V/2D5V(LDO)		
Size	Document Number	Rev
A3	AG1(Alviso)	01
Date: Monday, October 31, 2005		
Sheet 36 of 40		

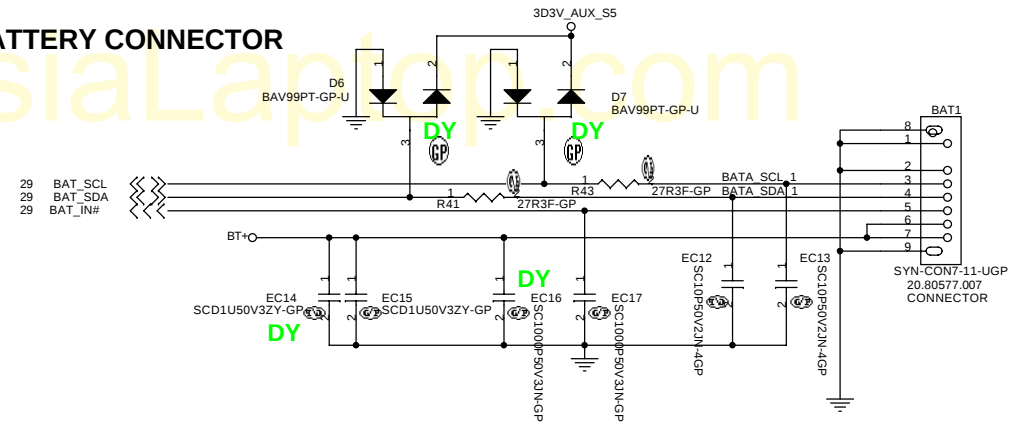




Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



<Core Design>

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title

AD/BATT CONN

Size
A3

Document Number

AG1(Alviso)

Rev
01

Date: Tuesday, November 01, 2005

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