Angel_CY
UMA Schematics Document
IVY Bridge
Intel PCH

DY :None Installed
DIS:DIS installed
DIS_Muxless :BOTH DIS or Muxless installed
DIS_PX:BOTH DIS or PX installed
DIS_PX_Muxless:DIS or PX or Muxless installed.
Muxless: Muxless installed.(PX4.0)
PX:MUX installed.(PX3.0)
PX_Muxless:BOTH PX or Muxless installed.
UMA:UMA installed
UMA_Muxless:BOTH UMA or Muxless installed
UMA_PX_Muxless:UMA or PX or Muxless installed

ANNIE: ONLY FOR ANNIE solution.
PSL: KBC795 PSL circuit for 10mW solution installed.
10mW: External circuit for 10mW solution installed.
65W: for 65W adaptor installed.
90W: for 90W adaptor installed.

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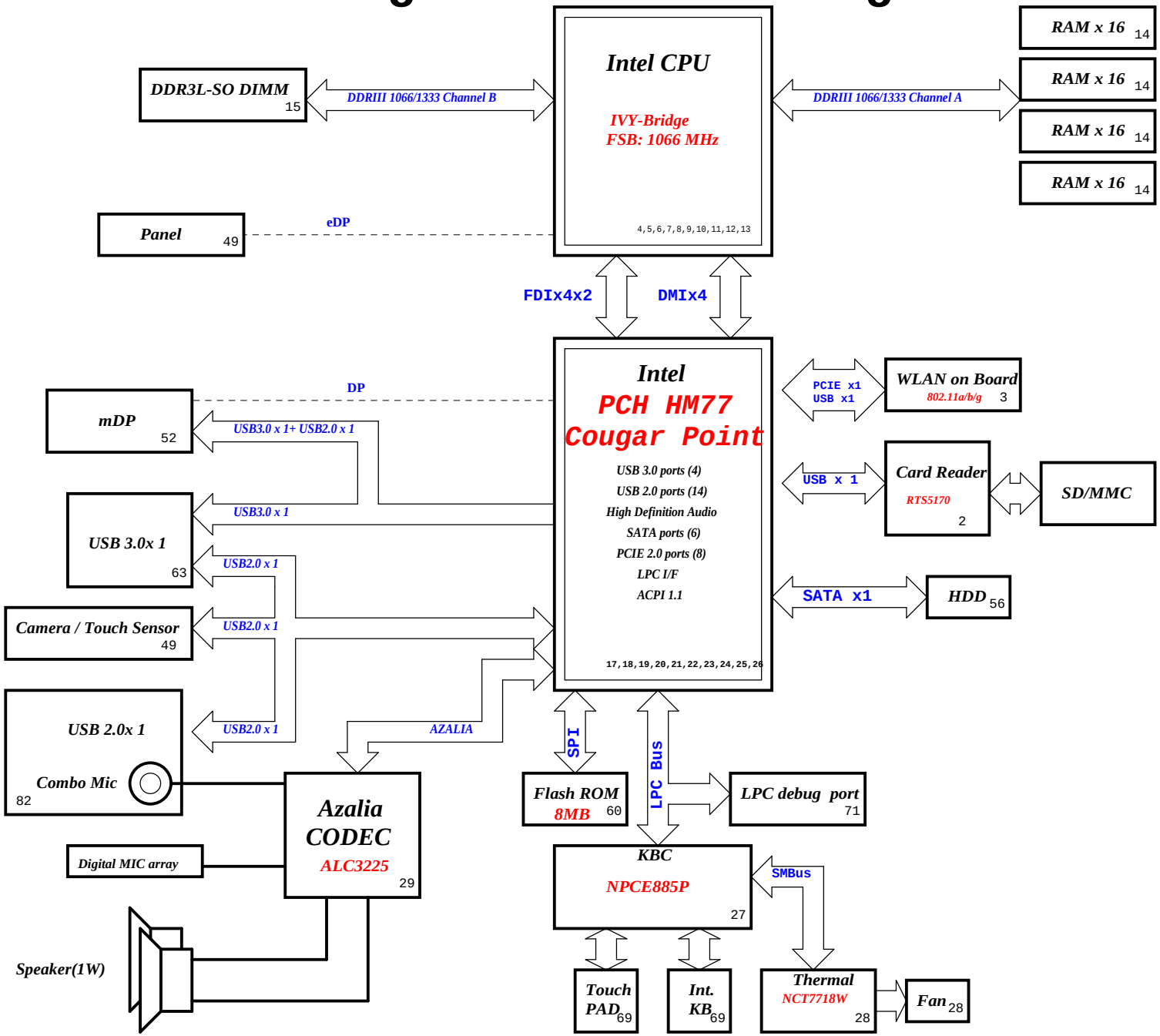
Project code : 91.4LJ01.001
PCB P/N :
Revision : 12313-1

Angel-CY Block Diagram



SYSTEM DC/DC BQ24727 40	
INPUTS	OUTPUTS
DCBATOUT	BT+

SYSTEM DC/DC TPS51225 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

CPU DC/DC TPS51640 42~44	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE VCC_GFXCORE

SYSTEM DC/DC TPS51363 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC RT8207 46	
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3 0D675V_S0 DDR_VREF_S3

SYSTEM DC/DC SYW232 47	
INPUTS	OUTPUTS
3D3V_S0	1D8V_S0

SYSTEM LOD S-1339D 47	
INPUTS	OUTPUTS
1D8V_S0	1D5V_S0

SYSTEM DC/DC SY8037 48	
INPUTS	OUTPUTS
5V_S5	0D85V_S0

PCB LAYER	
L1:Top	L5:Signal
L2:VCC	L6:Signal
L3:Signal	L7:GND
L4:GND	L8:Bottom

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Title: Block Diagram

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PCH Strapping

Huron River Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	1

POWER PLANE	VOLTAGE	Voltage Rails ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

PCIE Routing

LANE1	Mini Card2(WWAN)
LANE2	Mini Card1(WLAN)
LANE3	Card Reader
LANE4	Onboard LAN
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

SATA Table

SATA	
Pair	Device
0	HDD1
1	HDD2
2	N/A
3	N/A
4	ODD
5	ESATA

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

SMBus ADDRESSES

I² C / SMBus Addresses Device	Ref Des	HURON RIVER ORB Address Hex	Bus
EC SMBus 1 Battery CHARGER			BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP			SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI			PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

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Title: Table of Content

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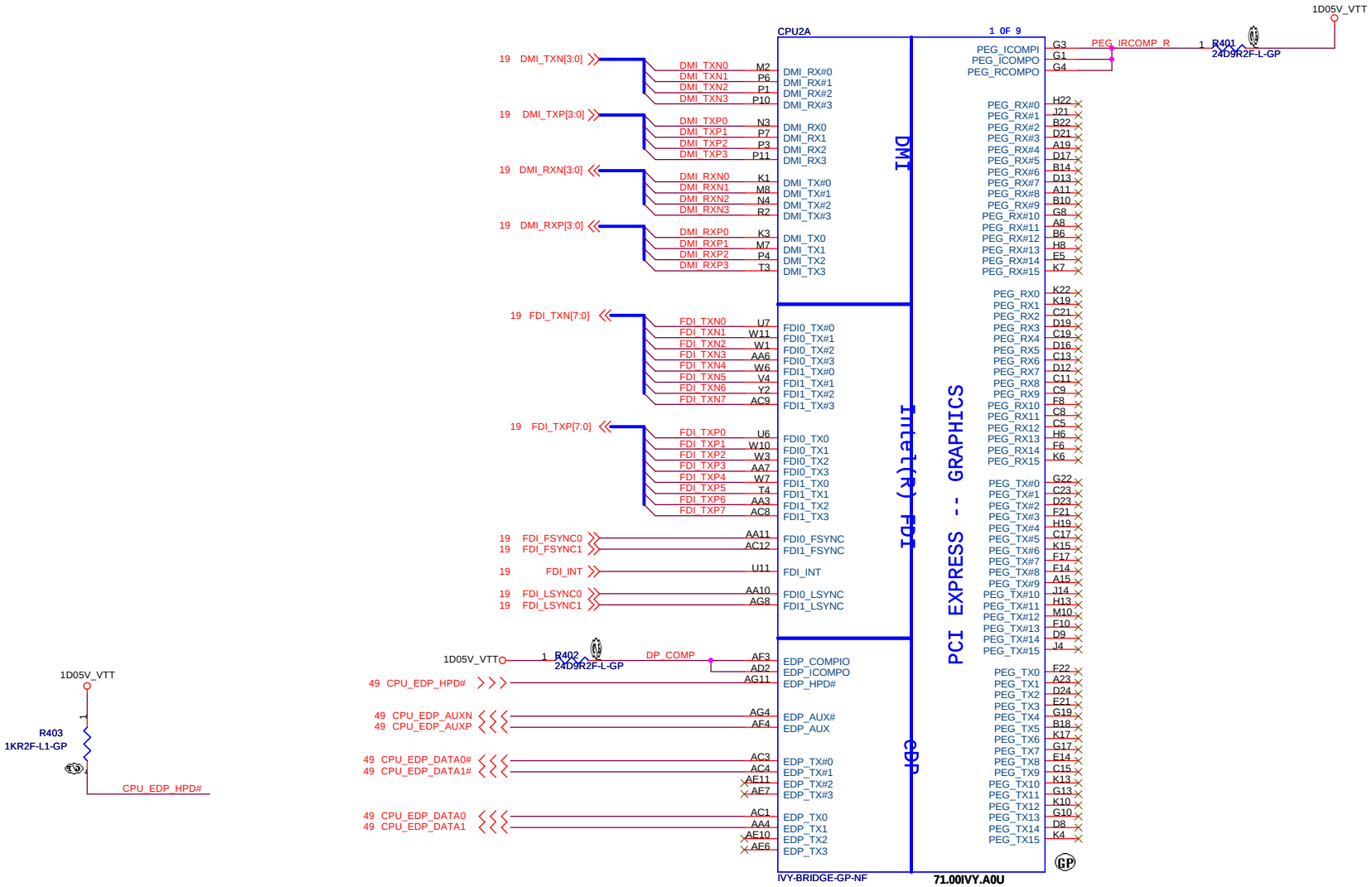
SSID = CPU



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Title: CPU (PCIE/DMI/FDI)

Size	Document Number	Rev
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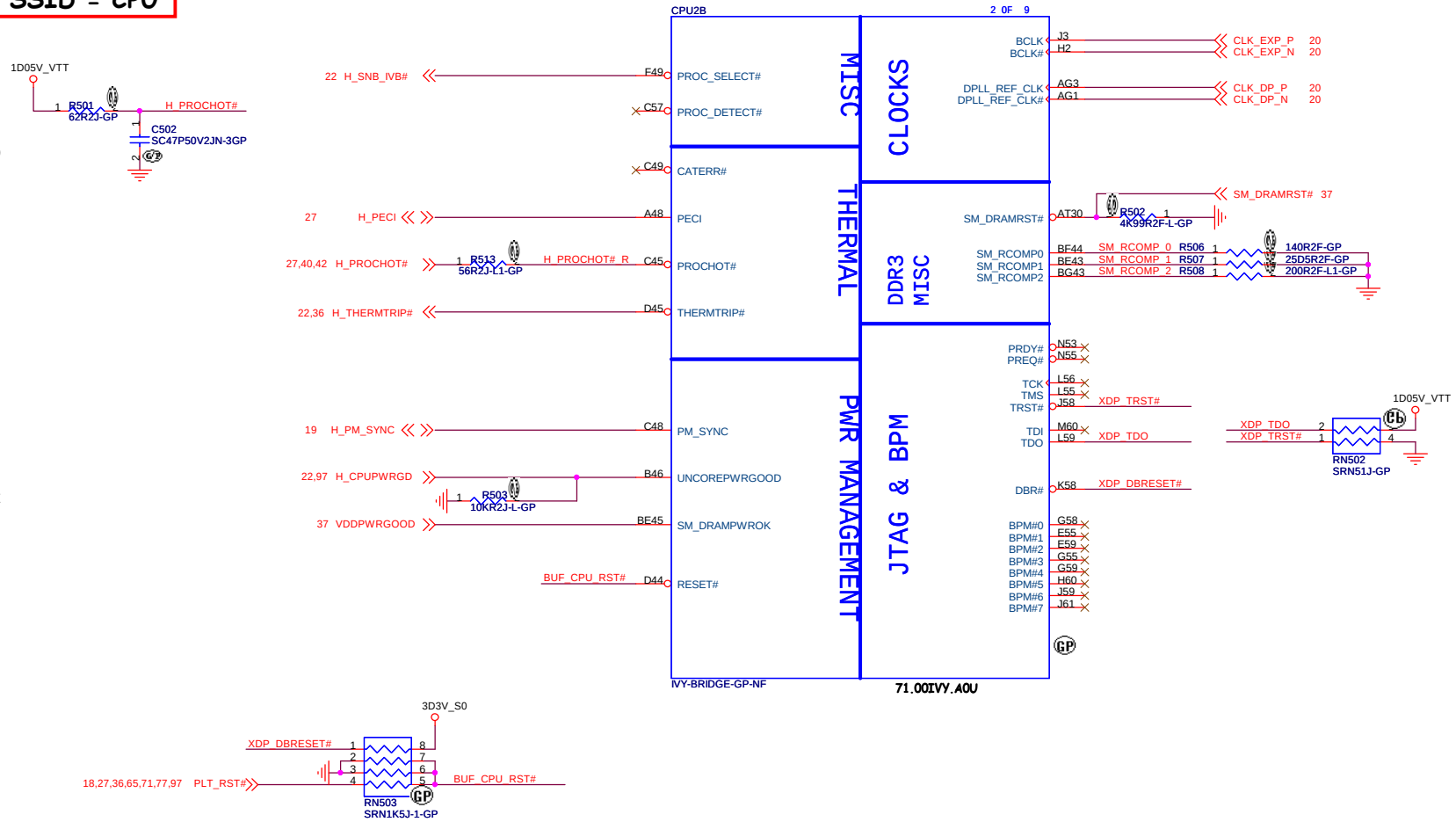
SSID = CPU



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Title: CPU (THERMAL/CLOCK/PM)

Size: A3 | Document Number: Angel-CY | Rev: 1

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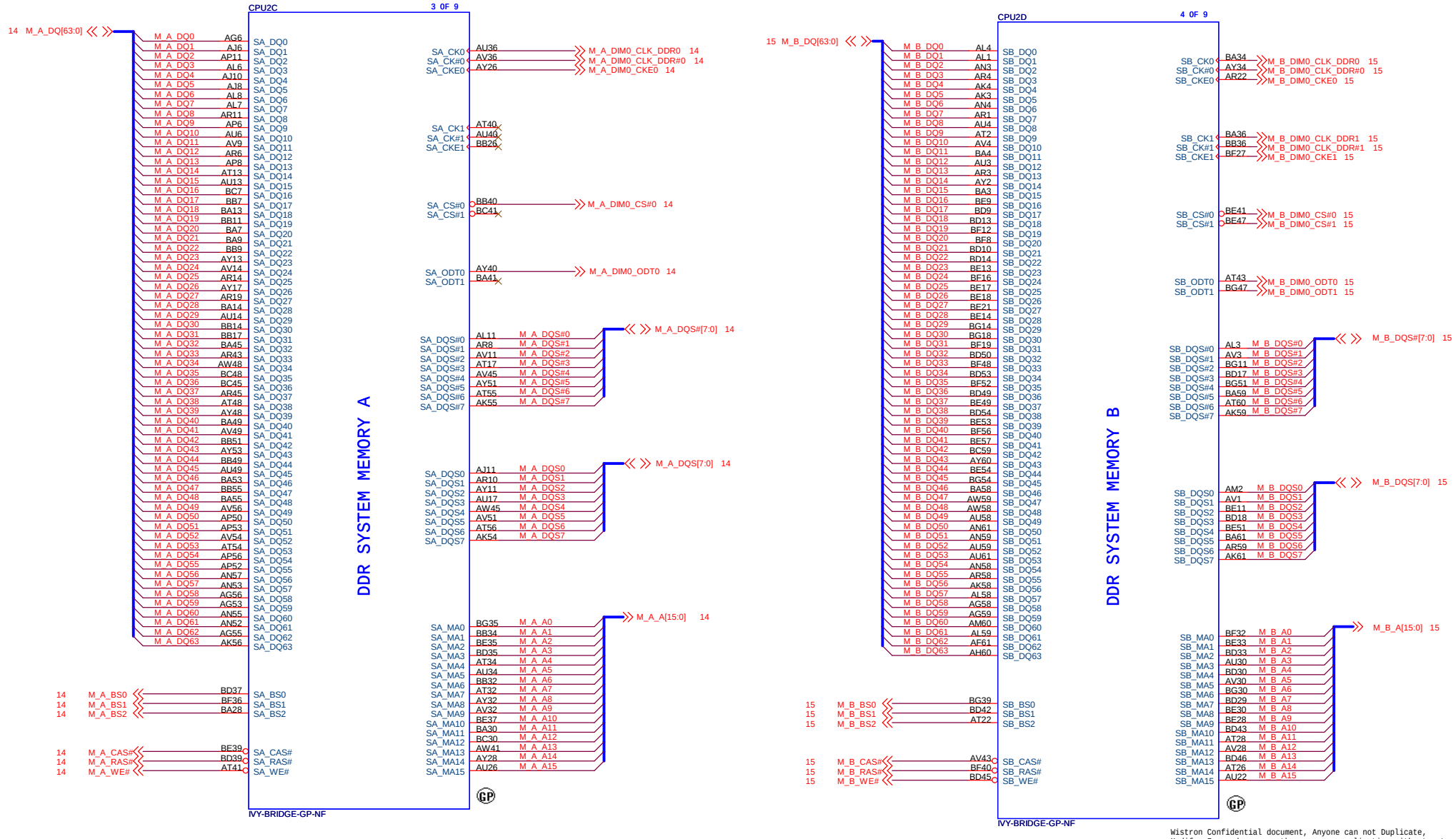
SSID = CPU



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Title	CPU (DDR)	
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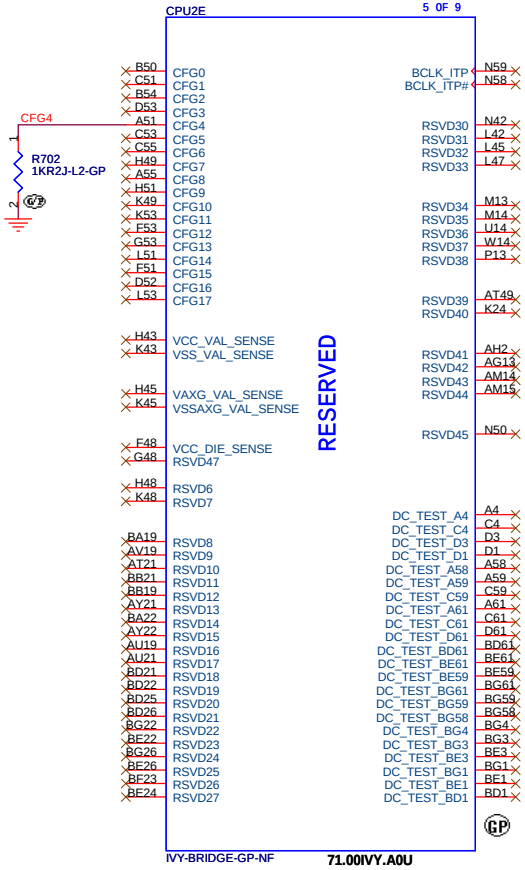
SSID = CPU



Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[0]		Connect a series 1 kOhms resistor on the critical CFG[0 trace in a manner which does not introduce any stubs to CFG[0] trace. Route as needed from the opposite side of this series isolation resistor to the debug port. ITP will drive the net to GND.	
CFG[2]	PCIe Static x16 Lane Numbering Reversal.	1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed	0
CFG[4]	Display Port Presence strap	1:Disabled - No Physical Display Port attached to Embedded DisplayPort No connect for disable 0:Enabled - An external Display Port device is connected to the Embedded Display Port Pull-down to GND through a 1KΩ ± 5% resistor to enable port	0
CFG[6:5]	PCI-Express Port Bifurcation Straps	00 = 1 x 8, 2 x 4 PCI Express 01 = reserved 10 = 2 x 8 PCI Express 11 = 1 x 16 PCI Express	00
CFG[17:7]	Reserved configuration lands. A test point may be placed on the board for these lands.		

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Title: CPU (RESERVED)

Size: A3 | Document Number: Angel-CY | Rev: 1

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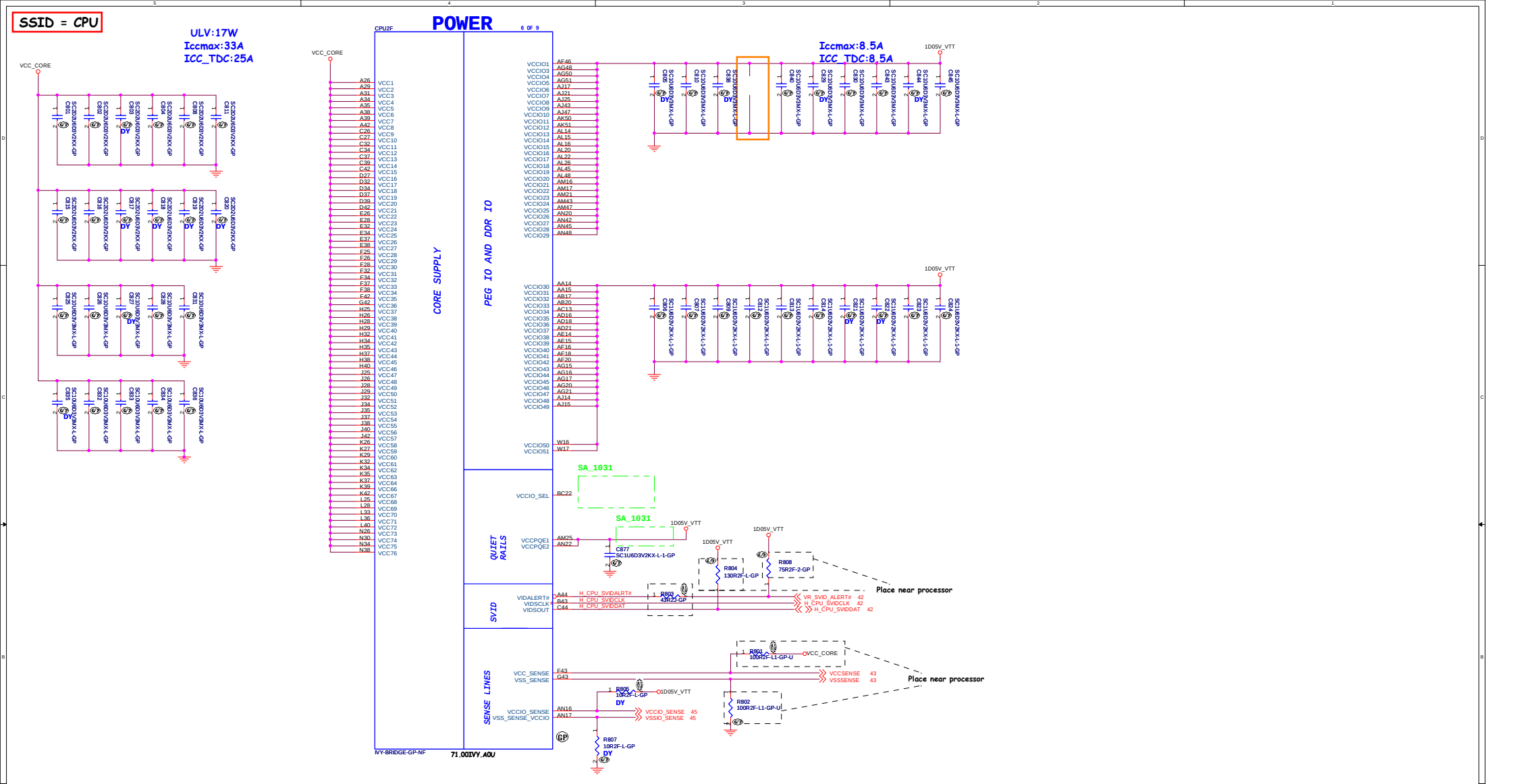

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Title	CPU (VCC_CORE)	
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SSID = CPU

Iccmax:18A(GT1)
ICC_TDC:12A(GT1)

POWER

CPU2G

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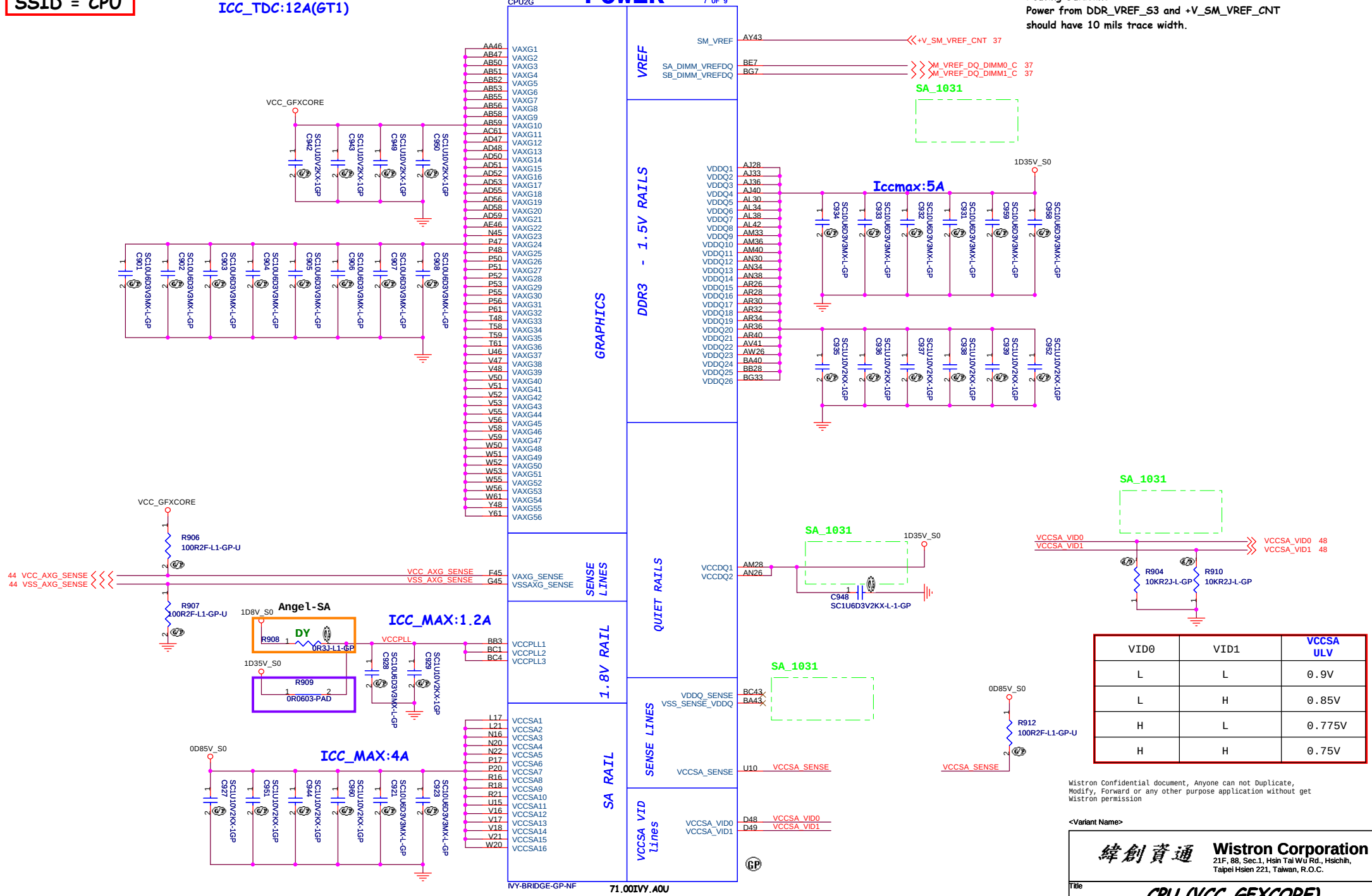
Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT should have 10 mils trace width.



VID0	VID1	VCCSA ULV
L	L	0.9V
L	H	0.85V
H	L	0.775V
H	H	0.75V

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Title: CPU (VCC_GFXCORE)

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SSID = CPU

CPU2H — 8 0F 9

VSS

A13	VSS1
A17	VSS2
A21	VSS3
A25	VSS4
A28	VSS5
A33	VSS6
A37	VSS7
A40	VSS8
A45	VSS9
A49	VSS10
A53	VSS11
A9	VSS12
AA1	VSS13
AA13	VSS14
AA50	VSS15
AA51	VSS16
AA52	VSS17
AA53	VSS18
AA55	VSS19
AA56	VSS20
AA8	VSS21
AB16	VSS22
AB18	VSS23
AB21	VSS24
AB48	VSS25
AB61	VSS26
AC10	VSS27
AC14	VSS28
AC46	VSS29
AC6	VSS30
AD17	VSS31
AD20	VSS32
AD4	VSS33
AD61	VSS34
AE13	VSS35
AE8	VSS36
AF1	VSS37
AF17	VSS38
AF21	VSS39
AF47	VSS40
AF48	VSS41
AF50	VSS42
AF51	VSS43
AF52	VSS44
AF53	VSS45
AF55	VSS46
AF56	VSS47
AF58	VSS48
AF59	VSS49
AG10	VSS50
AG14	VSS51
AG18	VSS52
AG47	VSS53
AG52	VSS54
AG61	VSS55
AG7	VSS56
AH4	VSS57
AH58	VSS58
AJ13	VSS59
AJ16	VSS60
AJ20	VSS61
AJ22	VSS62
AJ26	VSS63
AJ30	VSS64
AJ34	VSS65
AJ38	VSS66
AJ42	VSS67
AJ45	VSS68
AJ48	VSS69
AJ7	VSS70
AK1	VSS71
AK52	VSS72
AL10	VSS73
AL13	VSS74
AL17	VSS75
AL21	VSS76
AL25	VSS77
AL28	VSS78
AL33	VSS79
AL36	VSS80
AL40	VSS81
AL43	VSS82
AL47	VSS83
AL61	VSS84
AM13	VSS85
AM20	VSS86
AM22	VSS87
AM26	VSS88
AM30	VSS89
AM34	VSS90

VSS91	AM38
VSS92	AM4
VSS93	AM42
VSS94	AM45
VSS95	AM48
VSS96	AM58
VSS97	AN1
VSS98	AN21
VSS99	AN25
VSS100	AN28
VSS101	AN33
VSS102	AN36
VSS103	AN40
VSS104	AN43
VSS105	AN47
VSS106	AN50
VSS107	AN54
VSS108	AP10
VSS109	AP51
VSS110	AP55
VSS111	AP7
VSS112	AR13
VSS113	AR17
VSS114	AR21
VSS115	AR41
VSS116	AR48
VSS117	AR61
VSS118	AR7
VSS119	AT14
VSS120	AT19
VSS121	AT36
VSS122	AT4
VSS123	AT45
VSS124	AT52
VSS125	AT58
VSS126	AU1
VSS127	AU11
VSS128	AU28
VSS129	AU32
VSS130	AU51
VSS131	AU7
VSS132	AV17
VSS133	AV21
VSS134	AV22
VSS135	AV34
VSS136	AV40
VSS137	AV48
VSS138	AV55
VSS139	AW13
VSS140	AW43
VSS141	AW61
VSS142	AW7
VSS143	AY14
VSS144	AY19
VSS145	AY30
VSS146	AY36
VSS147	AY4
VSS148	AY41
VSS149	AY45
VSS150	AY49
VSS151	AY55
VSS152	AY58
VSS153	AY9
VSS154	BA1
VSS155	BA11
VSS156	BA17
VSS157	BA21
VSS158	BA26
VSS159	BA32
VSS160	BA48
VSS161	BA51
VSS162	BB53
VSS163	BC13
VSS164	BC5
VSS165	BC57
VSS166	BD12
VSS167	BD16
VSS168	BD19
VSS169	BD23
VSS170	BD27
VSS171	BD32
VSS172	BD36
VSS173	BD40
VSS174	BD44
VSS175	BD48
VSS176	BD52
VSS177	BD56
VSS178	BD8
VSS179	BE5
VSS180	BG13

IVY-BRIDGE-GP-NF

CPU2I — 9 0F 9

VSS

BG17	VSS181
BG21	VSS182
BG24	VSS183
BG28	VSS184
BG37	VSS185
BG41	VSS186
BG45	VSS187
BG49	VSS188
BG53	VSS189
BG9	VSS190
C29	VSS191
C35	VSS192
C40	VSS193
D10	VSS194
D14	VSS195
D18	VSS196
D22	VSS197
D26	VSS198
D29	VSS199
D35	VSS200
D4	VSS201
D40	VSS202
D43	VSS203
D46	VSS204
D50	VSS205
D54	VSS206
D58	VSS207
D6	VSS208
E25	VSS209
E29	VSS210
E3	VSS211
E35	VSS212
E40	VSS213
F13	VSS214
F15	VSS215
F19	VSS216
F29	VSS217
F35	VSS218
F40	VSS219
F55	VSS220
G51	VSS221
G6	VSS222
G61	VSS223
H10	VSS224
H14	VSS225
H17	VSS226
H21	VSS227
H4	VSS228
H53	VSS229
H58	VSS230
J1	VSS231
J49	VSS232
J55	VSS233
K11	VSS234
K21	VSS235
K51	VSS236
K8	VSS237
L16	VSS238
L20	VSS239
L22	VSS240
L26	VSS241
L30	VSS242
L34	VSS243
L38	VSS244
L43	VSS245
L48	VSS246
L61	VSS247
M11	VSS248
M15	VSS249

VSS250	M4
VSS251	M58
VSS252	M6
VSS253	N1
VSS254	N17
VSS255	N21
VSS256	N25
VSS257	N28
VSS258	N33
VSS259	N36
VSS260	N40
VSS261	N43
VSS262	N47
VSS263	N48
VSS264	N51
VSS265	N52
VSS266	N56
VSS267	N61
VSS268	P14
VSS269	P16
VSS270	P18
VSS271	P21
VSS272	P58
VSS273	P59
VSS274	P9
VSS275	R17
VSS276	R20
VSS277	R4
VSS278	R46
VSS279	T1
VSS280	T47
VSS281	T50
VSS282	T51
VSS283	T52
VSS284	T53
VSS285	T55
VSS286	T56
VSS287	U13
VSS288	U8
VSS289	V20
VSS290	V61
VSS291	W13
VSS292	W15
VSS293	W18
VSS294	W21
VSS295	W46
VSS296	W8
VSS297	Y4
VSS298	Y47
VSS299	Y58
VSS300	Y59

NCTF

NCTF TEST PIN : A5,A57,BC61,BG5 BG57,C3,E1,E61

VSS_NCTF_1#A5	A5
VSS_NCTF_2#A57	A57
VSS_NCTF_3#BC61	BC61
VSS_NCTF_8#BG5	BG5
VSS_NCTF_9#BG57	BG57
VSS_NCTF_10#C3	C3
VSS_NCTF_13#E1	E1
VSS_NCTF_14#E61	E61
VSS_NCTF_4	BD3
VSS_NCTF_5	BD59
VSS_NCTF_6	BE4
VSS_NCTF_7	BE58
VSS_NCTF_11	C58
VSS_NCTF_12	D59

IVY-BRIDGE-GP-NF

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Title	CPU (VSS)	
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Title	XDP	
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Date: Monday, April 22, 2013	Sheet 11 of 102	

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Title	***Reserved***	
Size A4	Document Number **Angel-CY**	Rev **1**
Date: Monday, April 22, 2013	Sheet 12 of 102	

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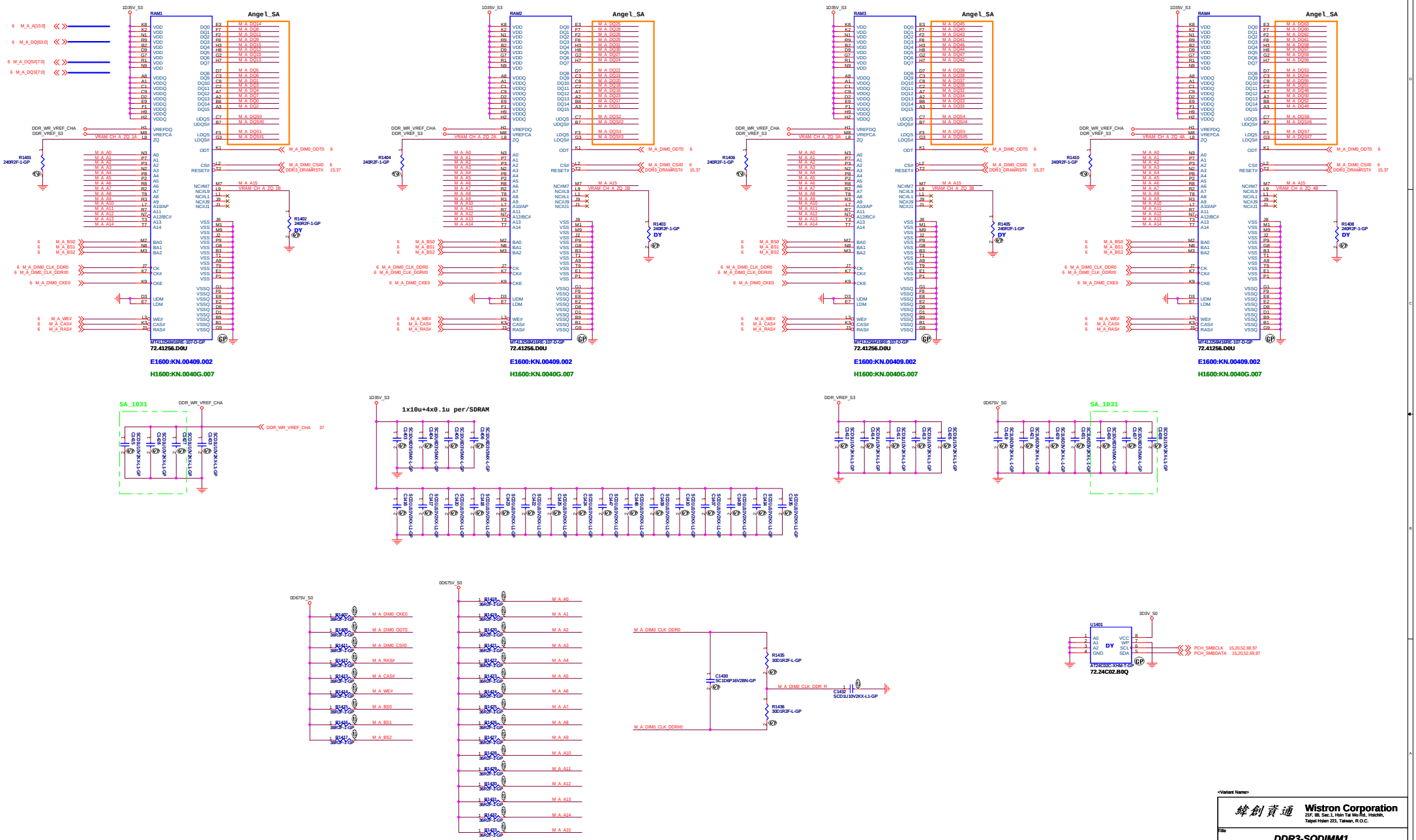
Title	***Reserved***	
Size A4	Document Number **Angel-CY**	Rev **1**
Date: Monday, April 22, 2013	Sheet 13 of 102	

SSID = MEMORY



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緯創資通	Wistron Corporation 2/F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	DDR3-SODIMM1	
Size: Custom	Document Number: Angel-CY	Rev: 1
Date: Monday, April 22, 2013	Sheet 14 of 102	

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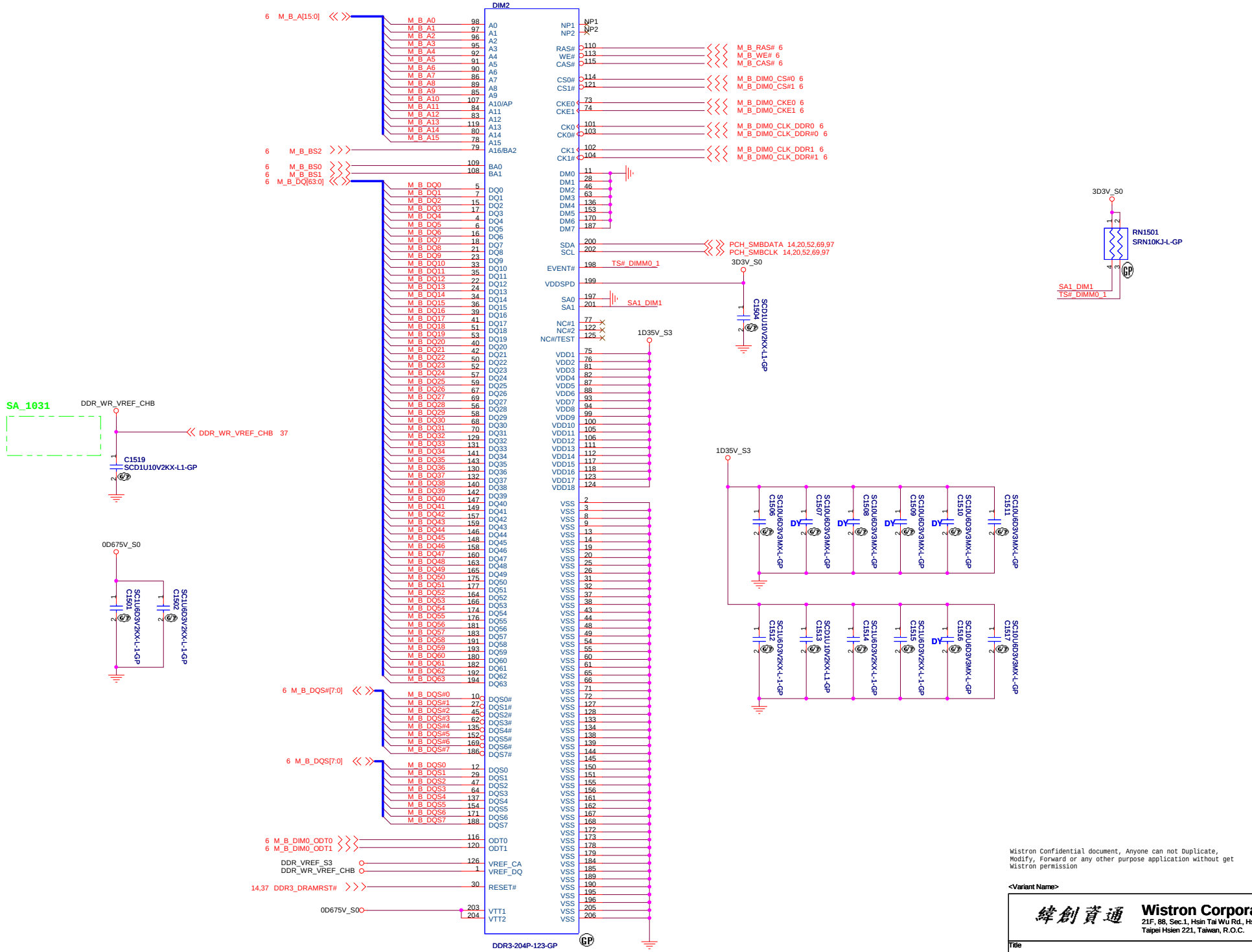

2ND = 62.10024.G11
3RD = 62.10024.S11
4th = 62.10017.X31

1st = 62.10024.M51

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Title: DDR3-SODIMM2

Size	Document Number	Rev
Custom	Angel-CY	1

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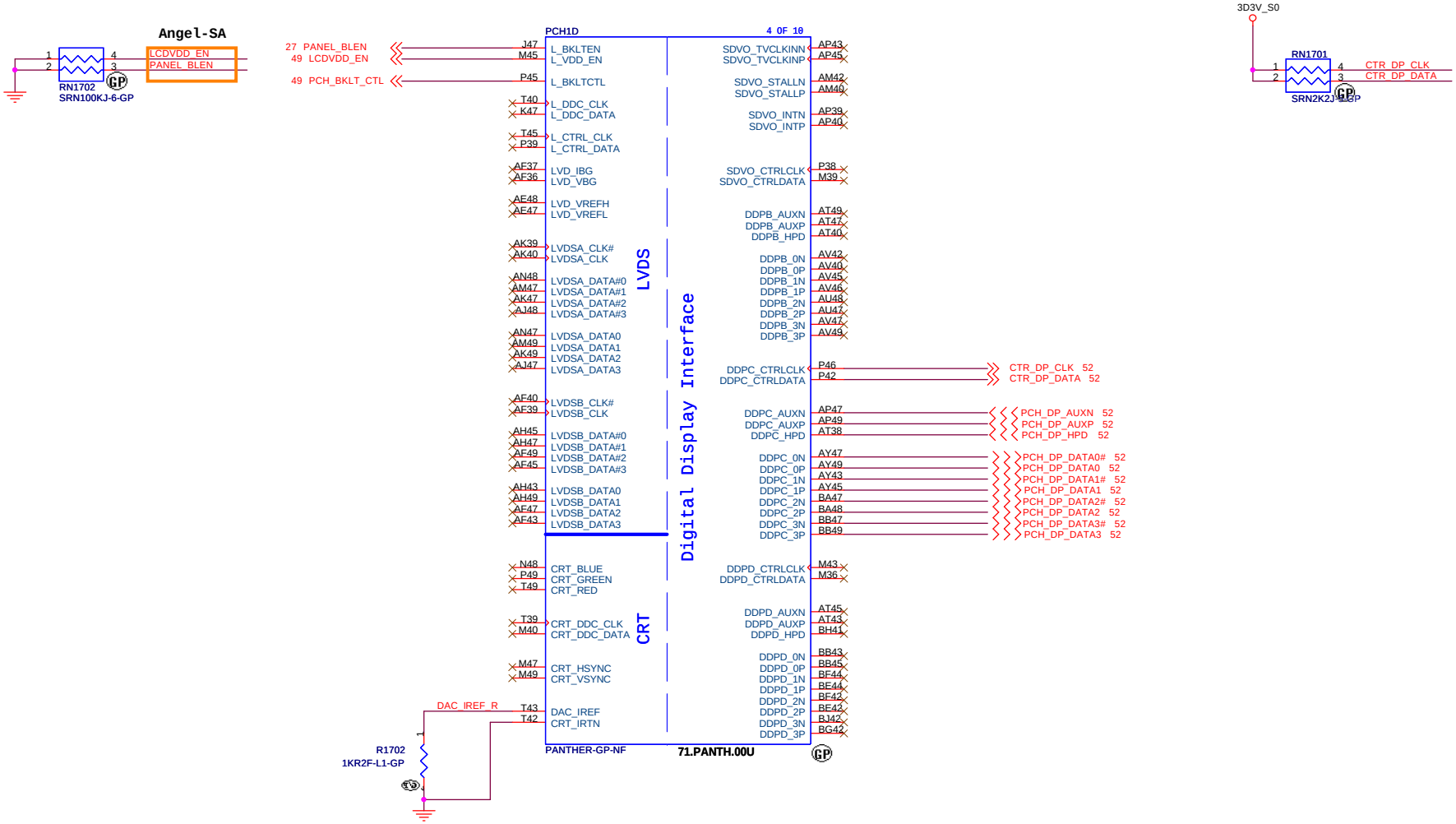
Title

DDR3-SODIMM2

Size	Document Number	Rev
A4	**Angel-CY**	**1**

Date: Monday, April 22, 2013 Sheet 16 of 102



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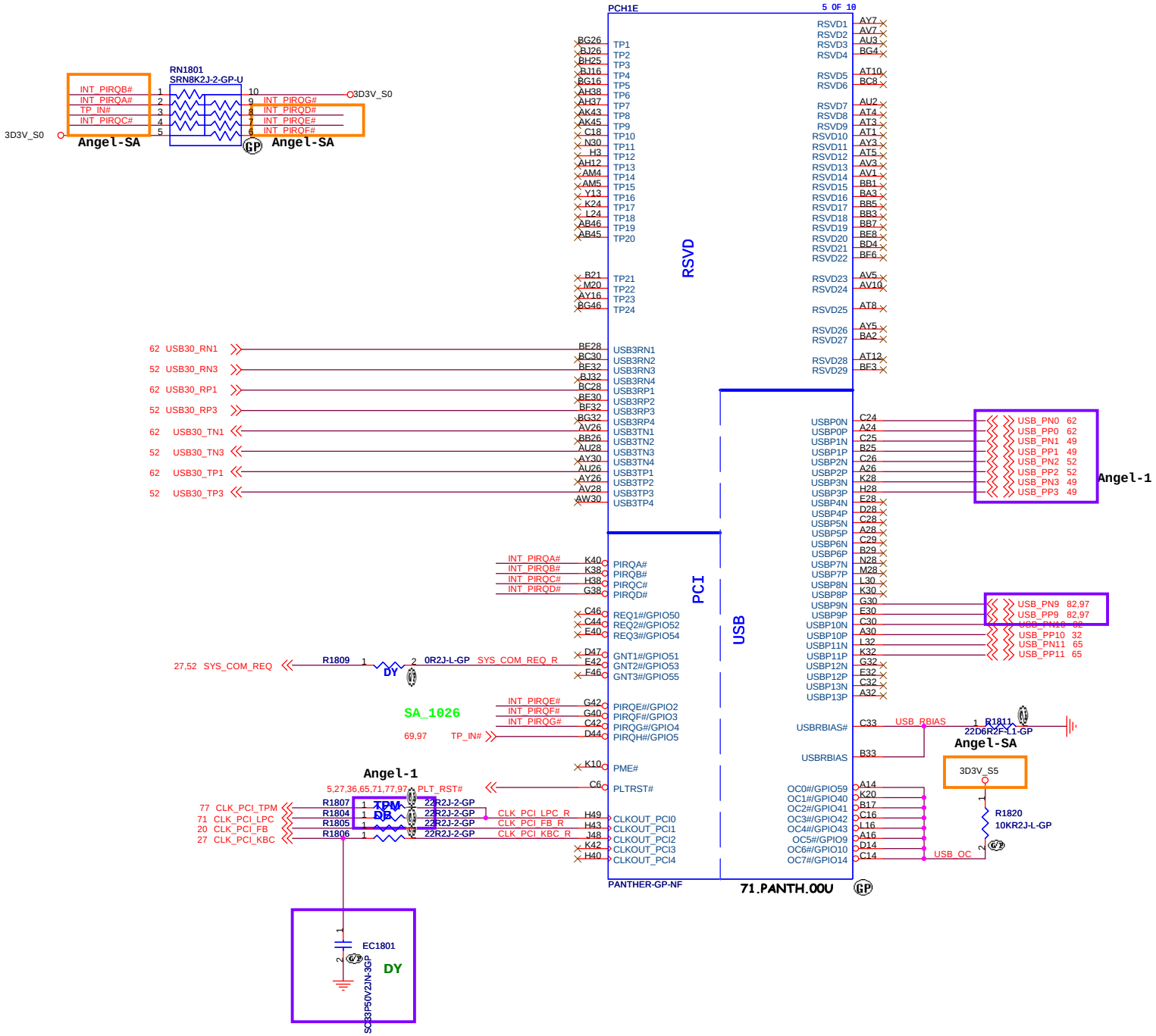
Title: PCH (LVDS/CRT/DDI)

Size	Document Number	Rev
A3	Angel-CY	1

Date: Monday, April 22, 2013 Sheet 17 of 102

SSID = PCH



USB Table

Pair	Device
0	USB3.0 Ext. port 1
1	TOUCH PANEL
2	mDP
3	CCD
4	NC
5	NC
6	X
7	X
8	NC
9	USB2.0 Ext. port 1
10	Card Reader
11	Mini Card1 (BT)
12	NC

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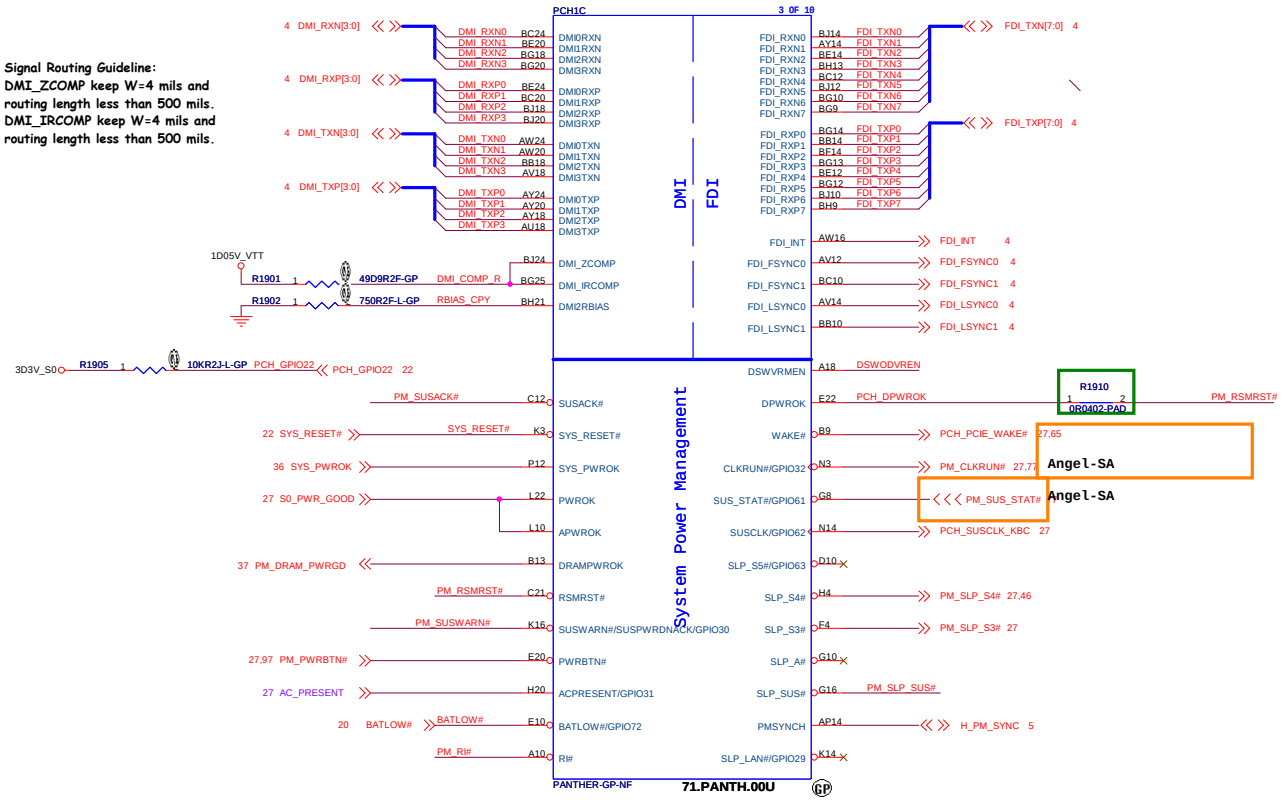
Title: PCH (PCI/USB/NVRAM)

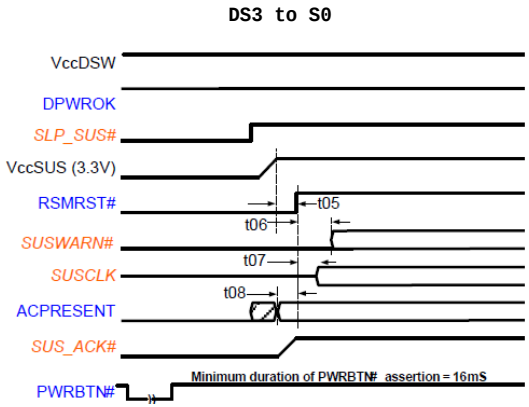
Size: A3 | Document Number: Angel-CY | Rev: 1

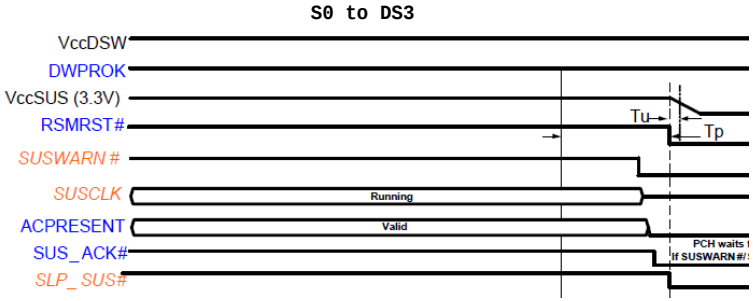
Date: Monday, April 22, 2013 | Sheet 18 of 102

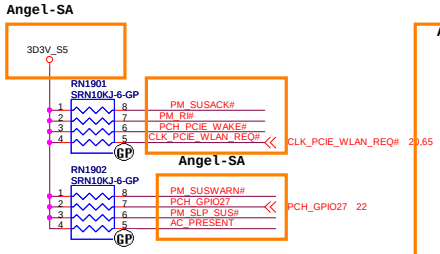
SSID = PCH

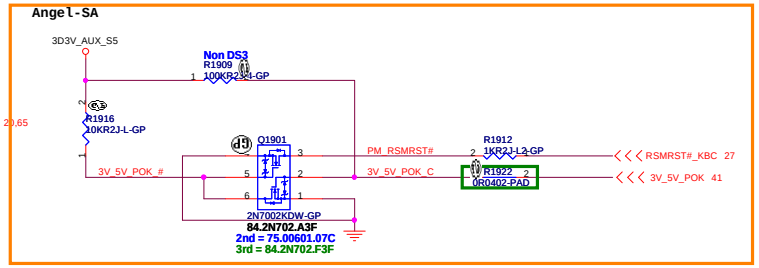
Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.

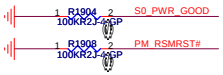






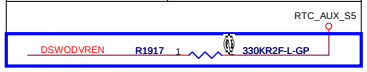






DSWODVREN - On Die DSW VR Enable

HIGH	Enabled (DEFAULT)
LOW	Disabled



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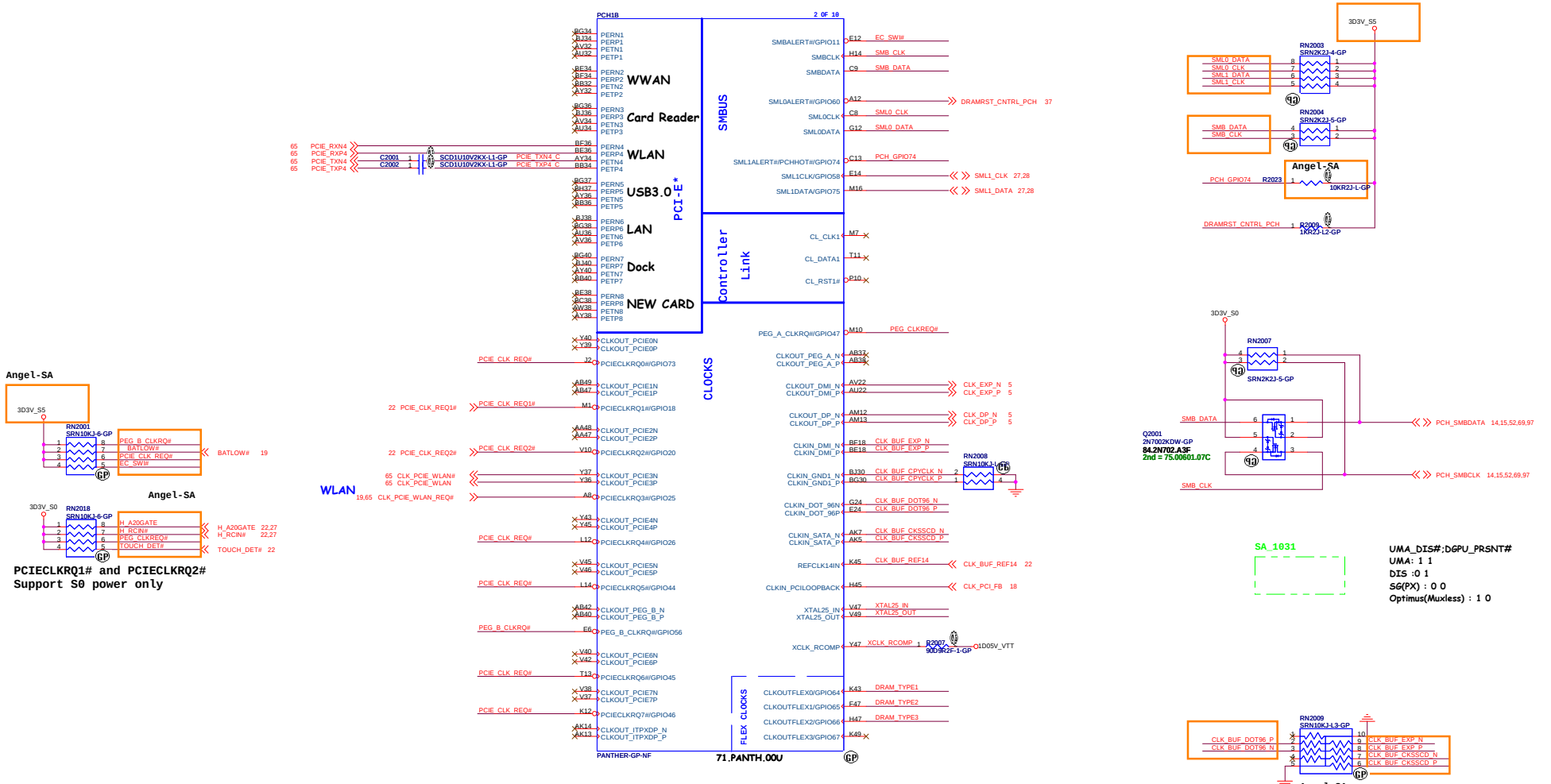
Title: PCH (DM I/FDI/PM)

Size: Custom | Document Number: Angel-CY | Rev: 1

Date: Monday, April 22, 2013 | Sheet 19 of 102

SSID = PCH



GPIO66 DRAM_Type3	GPIO65 DRAM_Type2	GPIO64 DRAM_Type1	Status
0	0	0	ELPIDA_KM.4GB09.003 ELPIDA DDR3L 1333 4GB EDJ4216EBBG-DJ-F
0	0	1	ELPIDA_KN.00409.002 ELPIDA DDR3L 1600 4Gb EDJ4216EFBG-GNL-F
0	1	0	Hynix_KN.0040G.007 HYNIX DDR3L 1600 4Gb H5TC4G63AFR-PBA LF+HF 256*16 29nm

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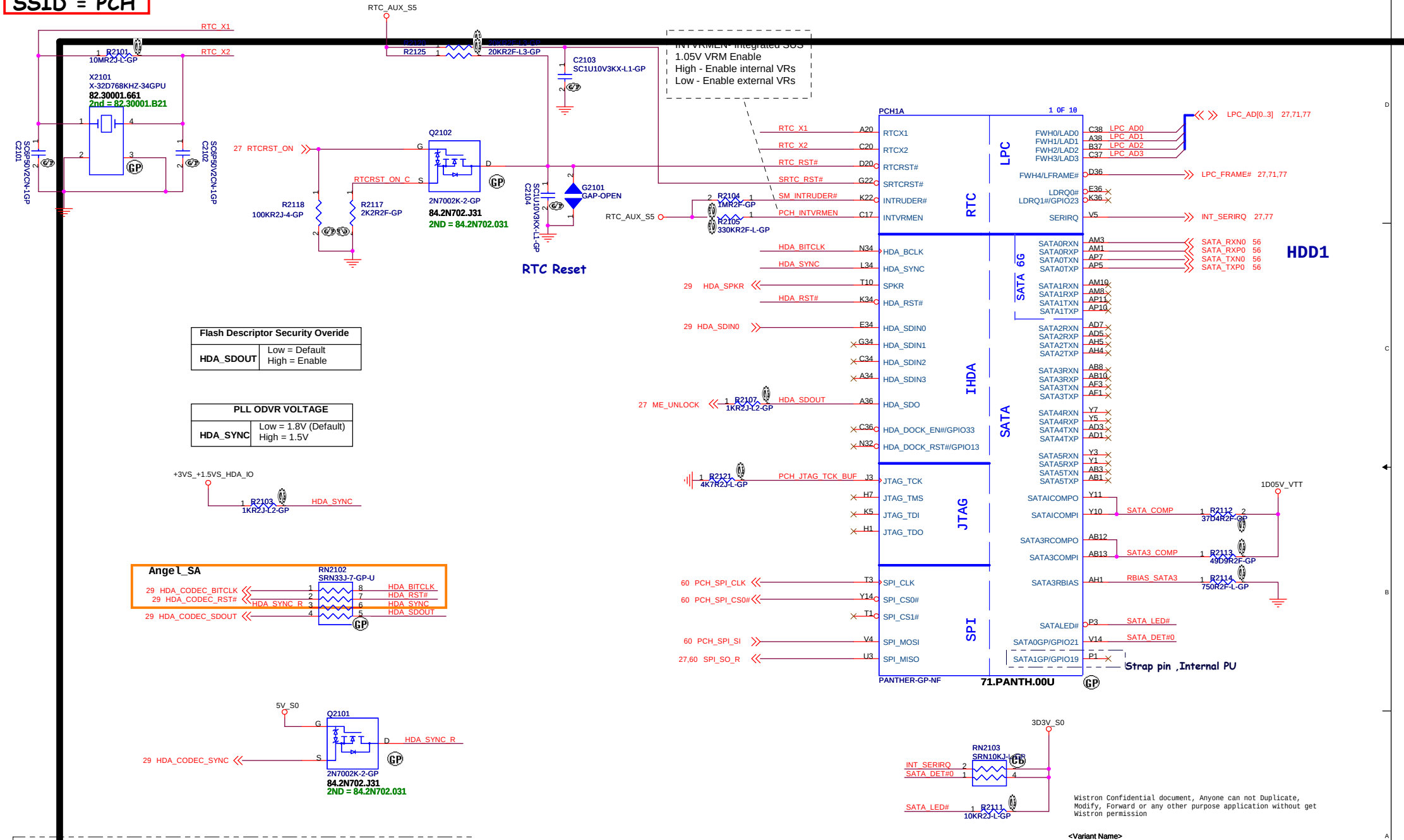
Title: PCH (PCI-E/SMBUS/CLOCK/CL)

Size: A2 | Document Number: Angel-CY | Rev: 1

Date: Monday, April 22, 2013 | Sheet 20 of 102

SSID = PCH



Flash Descriptor Security Overide	
HDA_SDOUT	Low = Default High = Enable

PLL ODVR VOLTAGE	
HDA_SYNC	Low = 1.8V (Default) High = 1.5V

HDA_SYNC:
This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode.
1K external pull-up resistor is required on this signal on the board.
Signal may have leakage paths via powered off devices(Audio Codec)
and hence contend with the external pull-up.
A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

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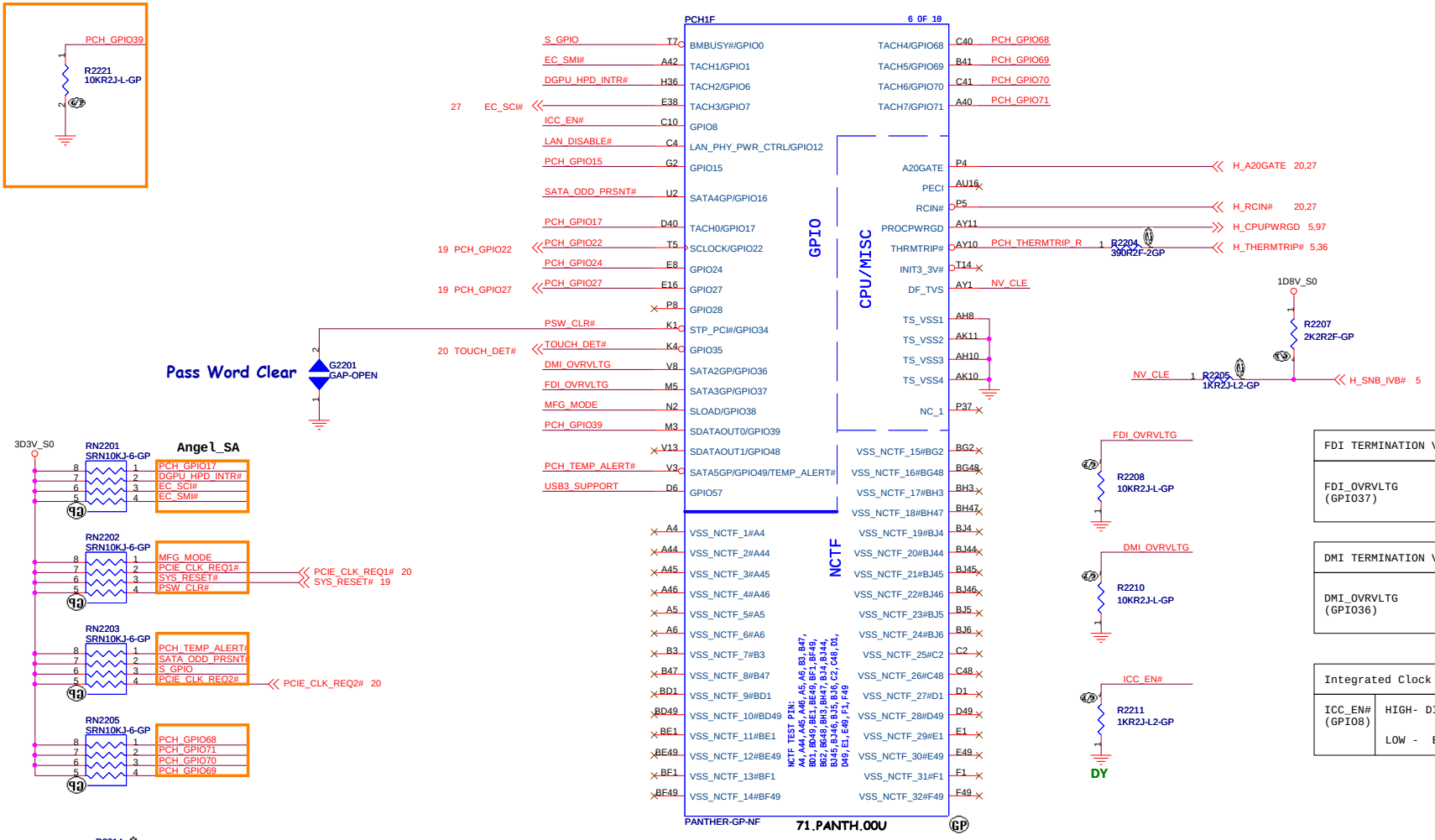
Title: PCH (SPI/RTC/LPC/SATA/IHDA)

Size	Document Number	Rev
A3	Angel-CY	1

Date: Monday, April 22, 2013 Sheet 21 of 102

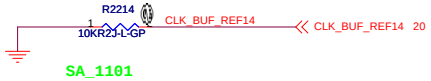
SSID = PCH

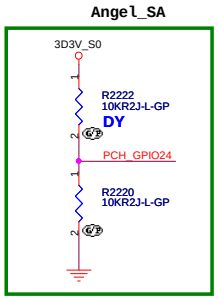


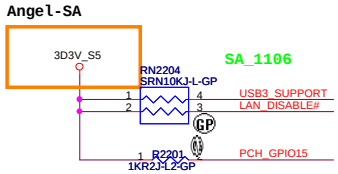
FDI TERMINATION VOLTAGE OVERRIDE(Reserved)	
FDI_OVRVLTG (GPIO37)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE(Reserved)	
DMI_OVRVLTG (GPIO36)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Chip Enable(Reserved)	
ICC_EN# (GPIO8)	HIGH- DISABLED [DEFAULT] LOW - ENABLED







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Title: PCH (GPIO/CPU)

Size: Custom | Document Number: Angel-CY | Rev: 1

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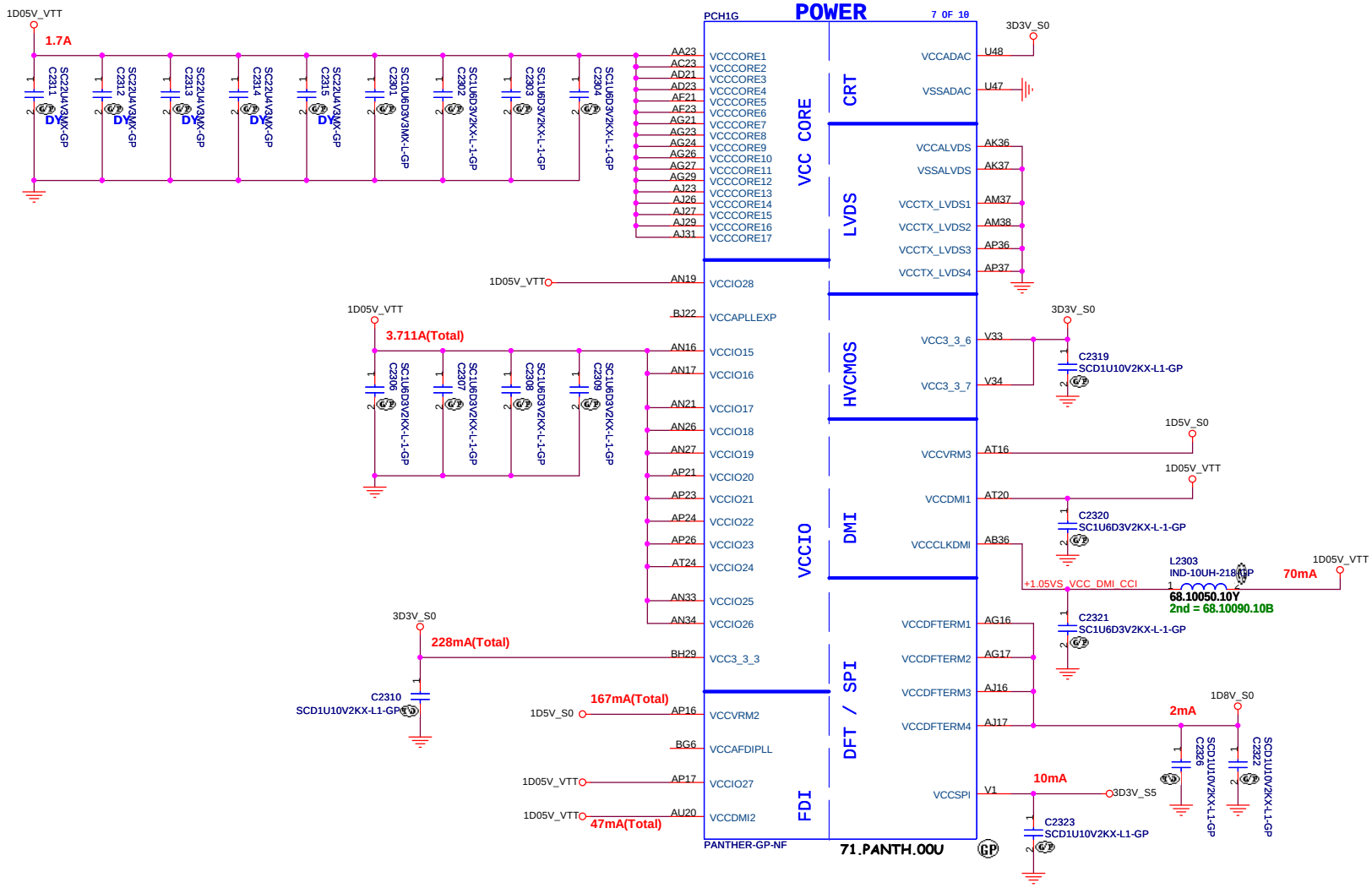

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Title: PCH (POWER1)

Size: A3 | Document Number: Angel-CY | Rev: 1

Date: Monday, April 22, 2013 | Sheet 23 of 102

SSID = PCH

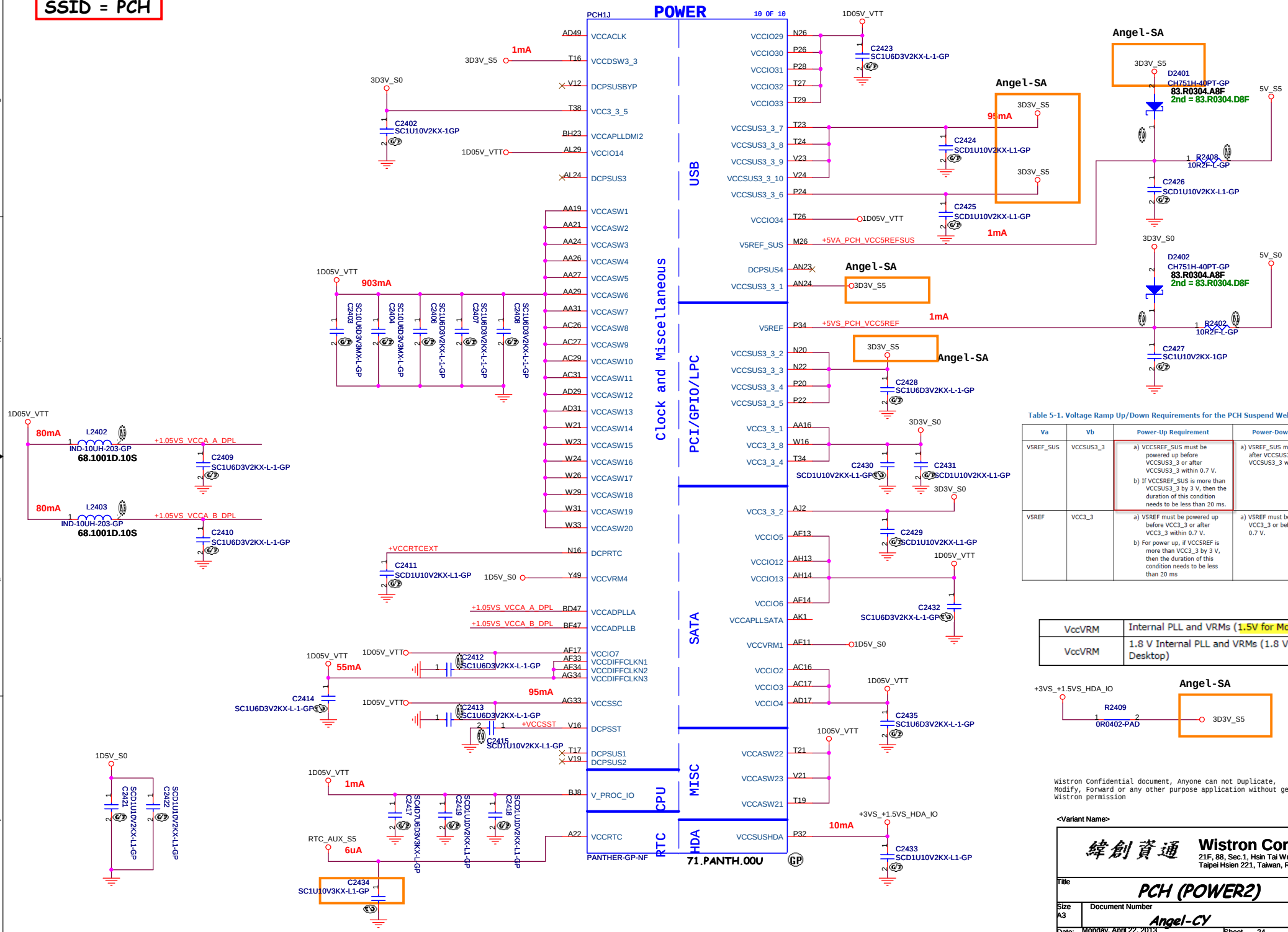

Table 5-1. Voltage Ramp Up/Down Requirements for the PCH Suspend Well Voltage Rails

Va	Vb	Power-Up Requirement	Power-Down Requirement
VSREF_SUS	VCCSUS3_3	a) VCCSREF_SUS must be powered up before VCCSUS3_3 or after VCCSUS3_3 within 0.7 V. b) If VCCSREF_SUS is more than VCCSUS3_3 by 3 V, then the duration of this condition needs to be less than 20 ms.	a) VSREF_SUS must be powered down after VCCSUS3_3 or before VCCSUS3_3 within 0.7 V.
VSREF	VCC3_3	a) VSREF must be powered up before VCC3_3 or after VCC3_3 within 0.7 V. b) For power up, if VCCSREF is more than VCC3_3 by 3 V, then the duration of this condition needs to be less than 20 ms	a) VSREF must be powered down after VCC3_3 or before VCC3_3 within 0.7 V.

VccVRM	Internal PLL and VRMs (1.5V for Mobile)
VccVRM	1.8 V Internal PLL and VRMs (1.8 V for Desktop)

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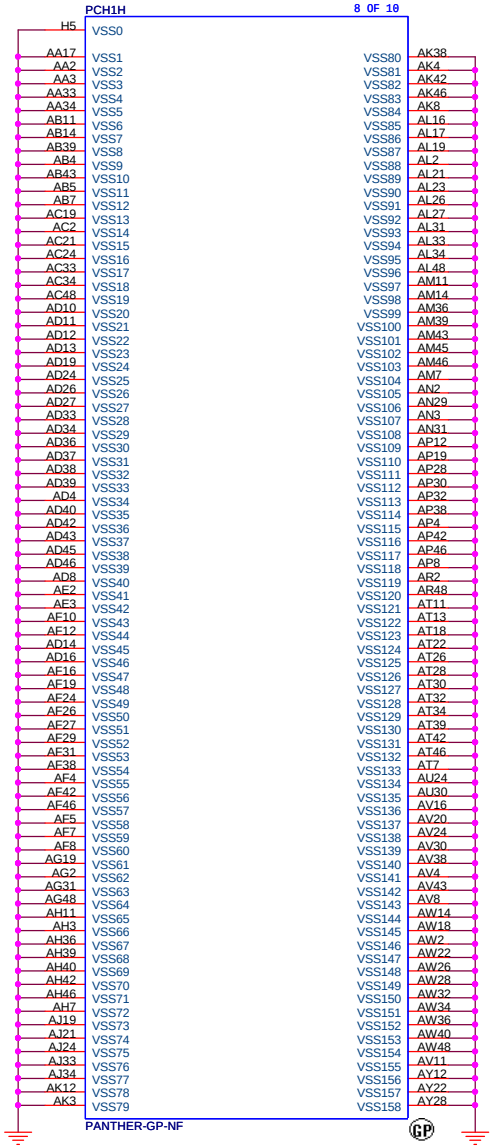
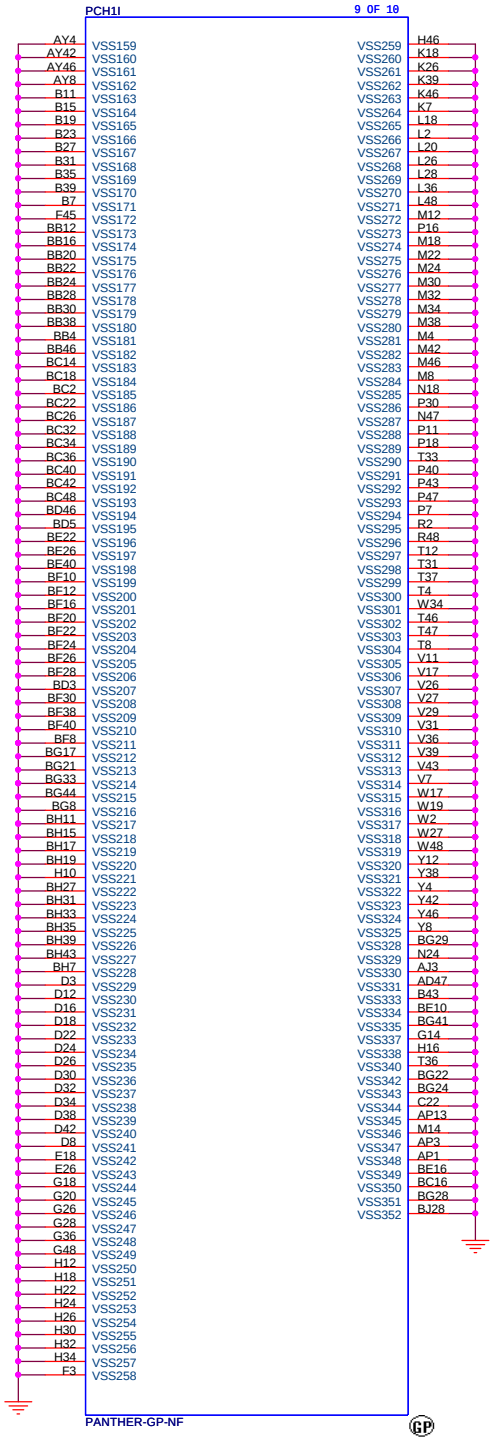
Title: PCH (POWER2)

Size: A3 | Document Number: Angel-CY | Rev: 1

Date: Monday, April 22, 2013 | Sheet 24 of 102

SSID = PCH





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Title	PCH (VSS)	
Size A3	Document Number Angel-CY	Rev 1
Date: Monday, April 22, 2013	Sheet 25 of 102	

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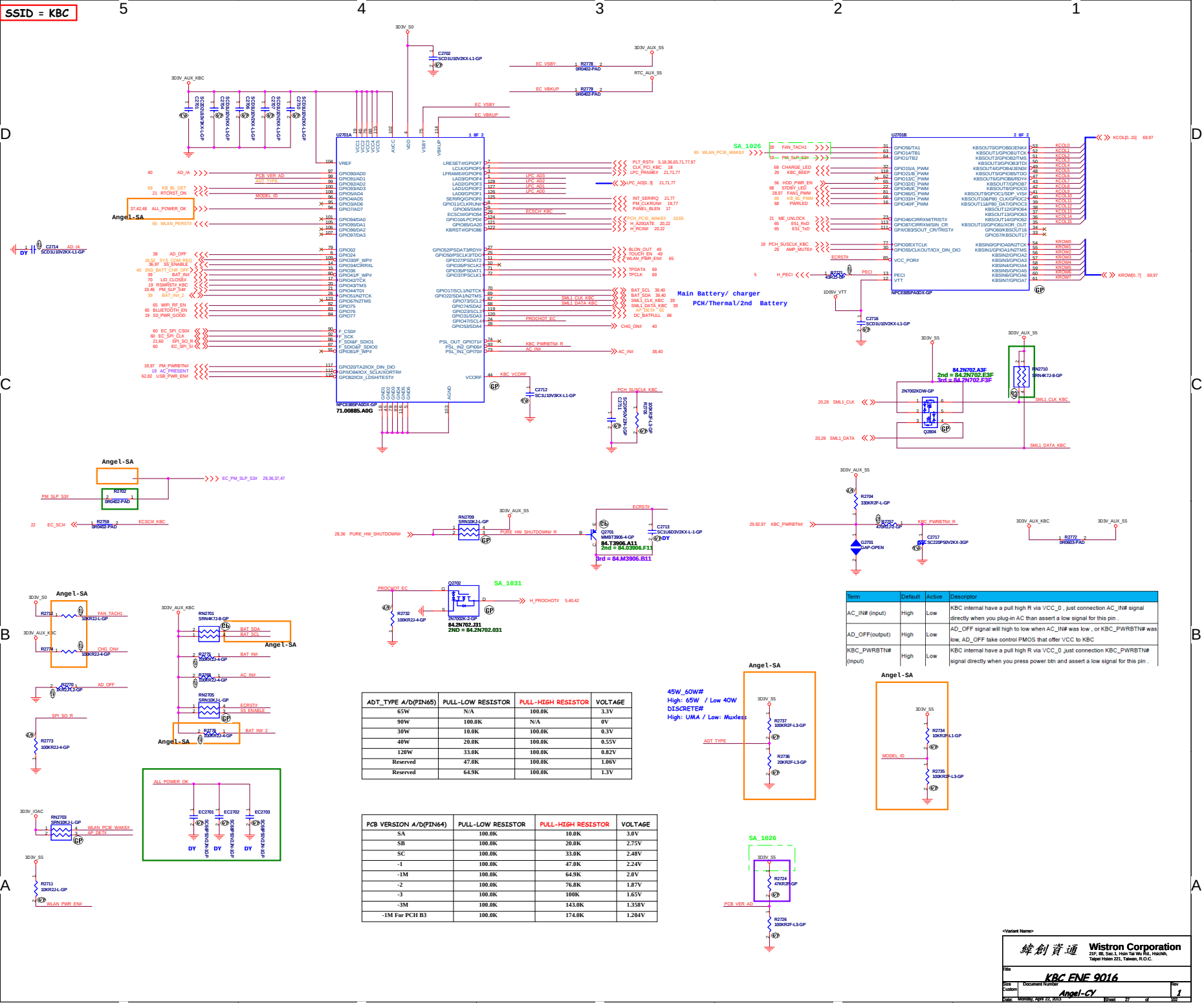
Title	*Clock(colay)*	
Size A4	Document Number **Angel-CY**	Rev **1**
Date: Monday, April 22, 2013	Sheet 26 of 102	

SSID = KBC



Term	Default	Active	Descriptor
AC_IN# (input)	High	Low	KBC internal have a pull high R via VCC_0 , just connection AC_IN# signal directly when you plug-in AC than assert a low signal for this pin .
AD_OFF(output)	High	Low	AD_OFF signal will high to low when AC_IN# was low , or KBC_PWRBTN# was low, AD_OFF take control PMOS that offer VCC to KBC
KBC_PWRBTN# (input)	High	Low	KBC internal have a pull high R via VCC_0 ,just connection KBC_PWRBTN# signal directly when you press power btn and assert a low signal for this pin .

ADT_TYPE A/D(PIN65)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
65W	N/A	100.0K	3.3V
90W	100.0K	N/A	0V
30W	10.0K	100.0K	0.3V
40W	20.0K	100.0K	0.55V
120W	33.0K	100.0K	0.82V
Reserved	47.0K	100.0K	1.06V
Reserved	64.9K	100.0K	1.3V

PCB VERSION A/D(PIN64)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
-1	100.0K	47.0K	2.24V
-1M	100.0K	64.9K	2.0V
-2	100.0K	76.8K	1.87V
-3	100.0K	100K	1.65V
-3M	100.0K	143.0K	1.358V
-1M For PCH B3	100.0K	174.0K	1.204V

<Variant Name>
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Title: KBC ENE 9016

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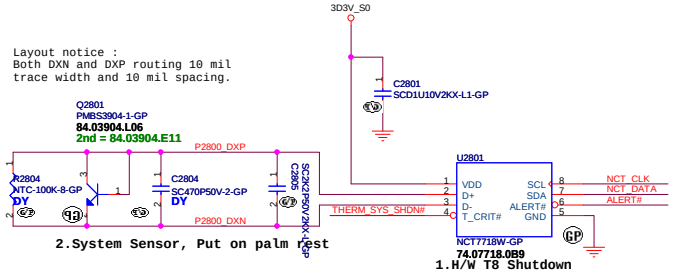
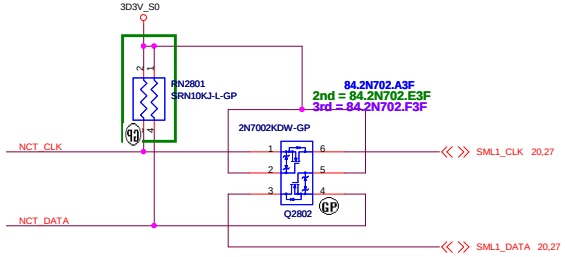
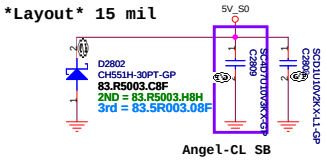
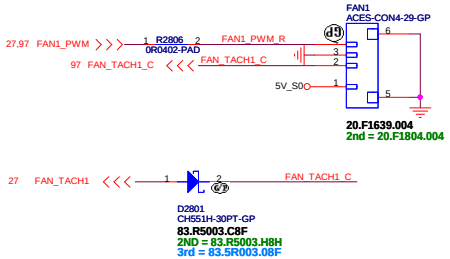
SSID = Thermal

Thermal sensor NCT 7718W





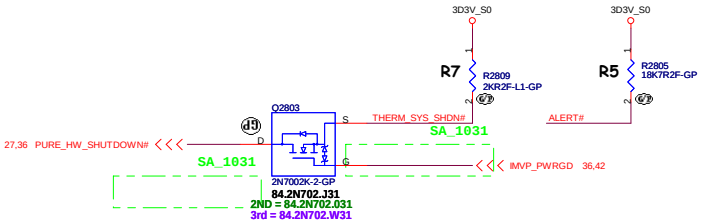




ALERT# /T_CRIT# Pull-up Resistor

R5 \ R7	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
2Kohm	77℃	87℃	97℃	107℃	117℃
7.5Kohm	79℃	89℃	99℃	109℃	119℃
10.5Kohm	81℃	91℃	101℃	111℃	121℃
14Kohm	83℃	93℃	103℃	113℃	123℃
18.7Kohm	85℃	95℃	105℃	115℃	125℃

T_CRIT temperature strapping point



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Title: Thermal Sensor NCT7718W

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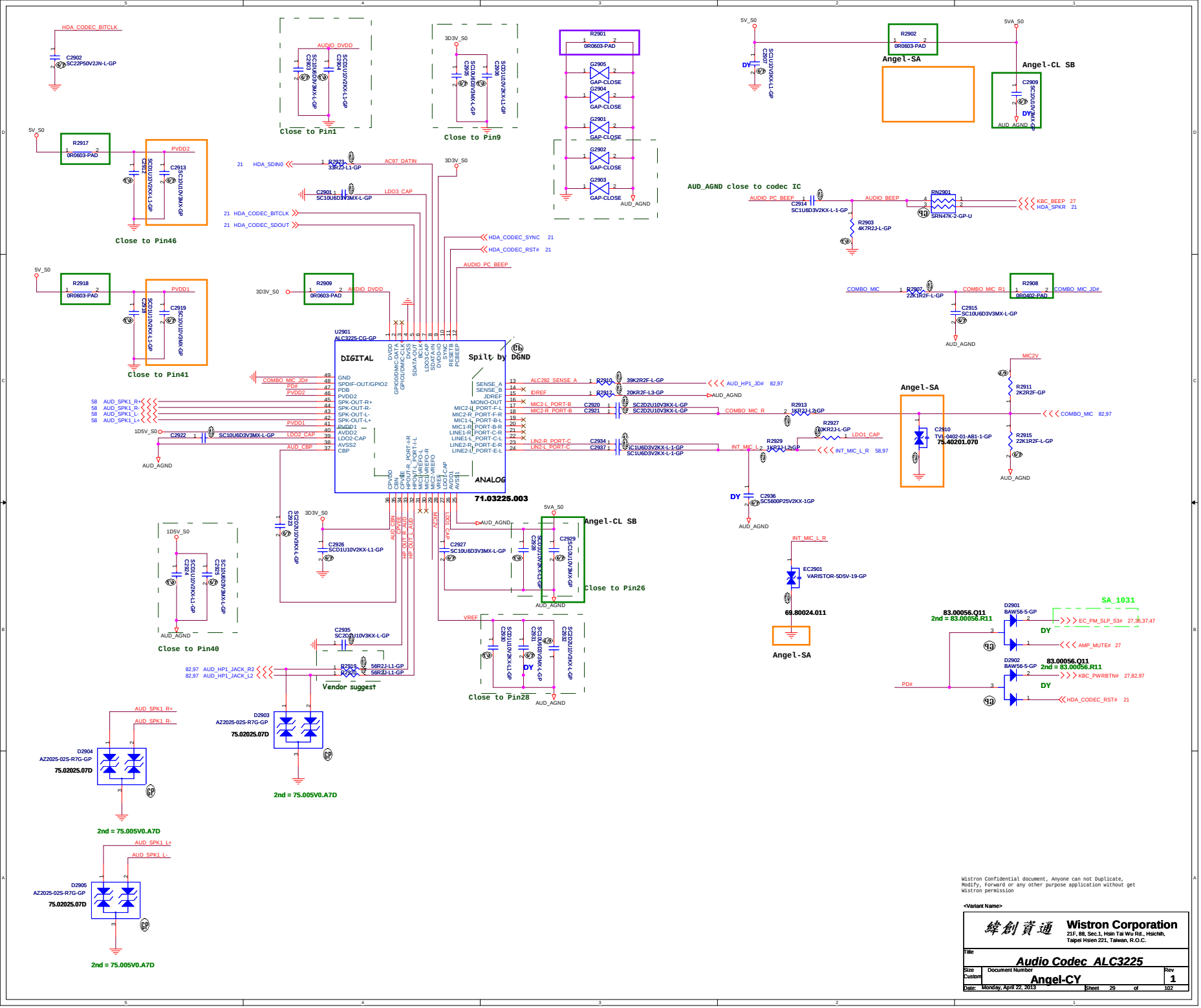

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Title: Audio Codec ALC3225

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AUDIO OP AMPLIFIER

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Title	Audio AMP	
Size A4	Document Number Angel-CY	Rev 1
Date: Monday, April 22, 2013	Sheet 30 of 102	

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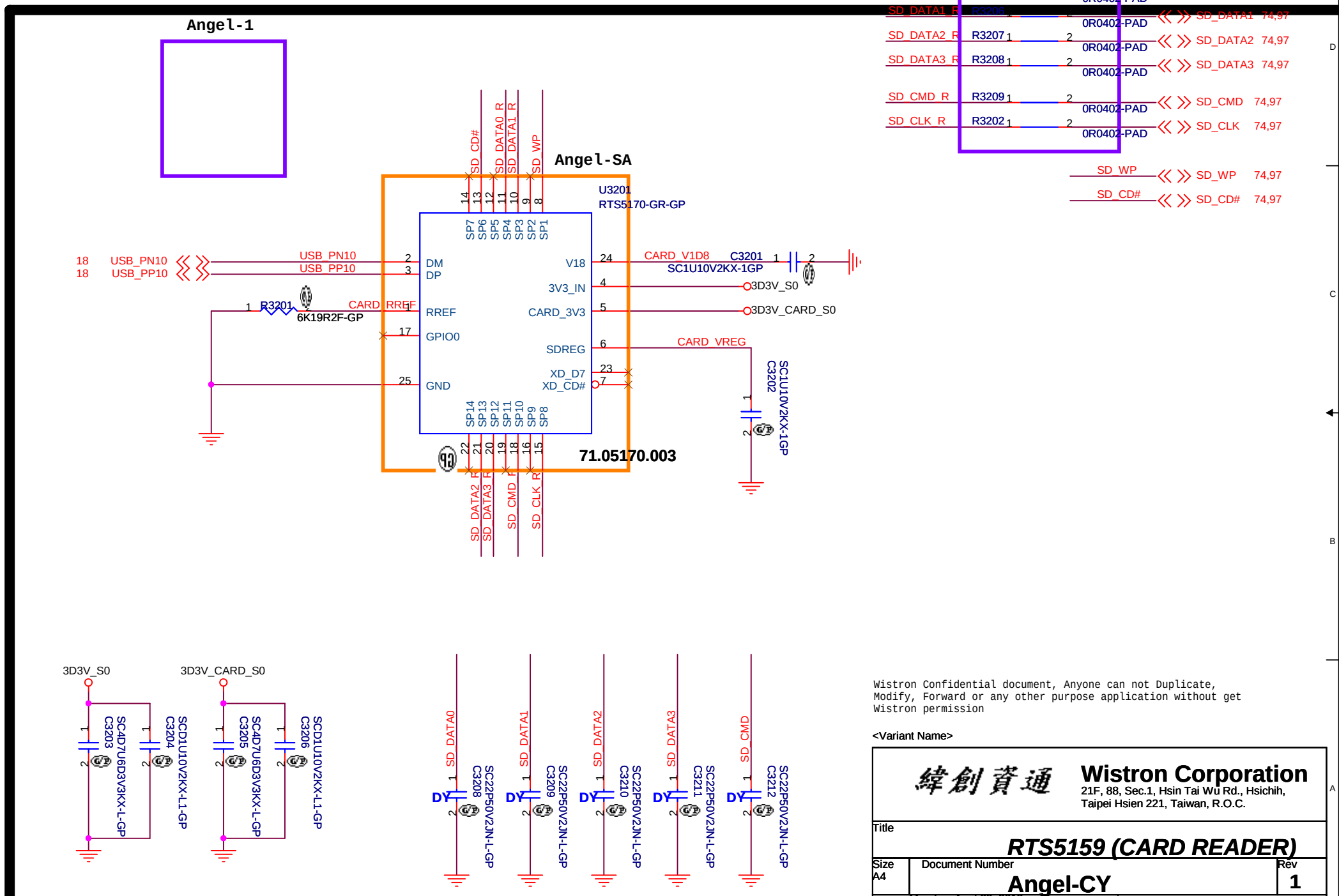
Taipei Hsien 221, Taiwan, R.O.C.

Title	AR8158	
Size A4	Document Number Angel-CY	Rev 1
Date: Monday, April 22, 2013	Sheet 31 of 102	



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Title: RTS5159 (CARD READER)

Size	Document Number	Rev
A4	Angel-CY	1

Date: Monday, April 22, 2013 Sheet 32 of 102

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Title	***Reserved***	
Size A4	Document Number **Angel-CY**	Rev **1**
Date: Monday, April 22, 2013	Sheet 33 of 102	

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Title	***Reserved***	
Size A4	Document Number **Angel-CY**	Rev **1**
Date: Monday, April 22, 2013	Sheet 34 of 102	

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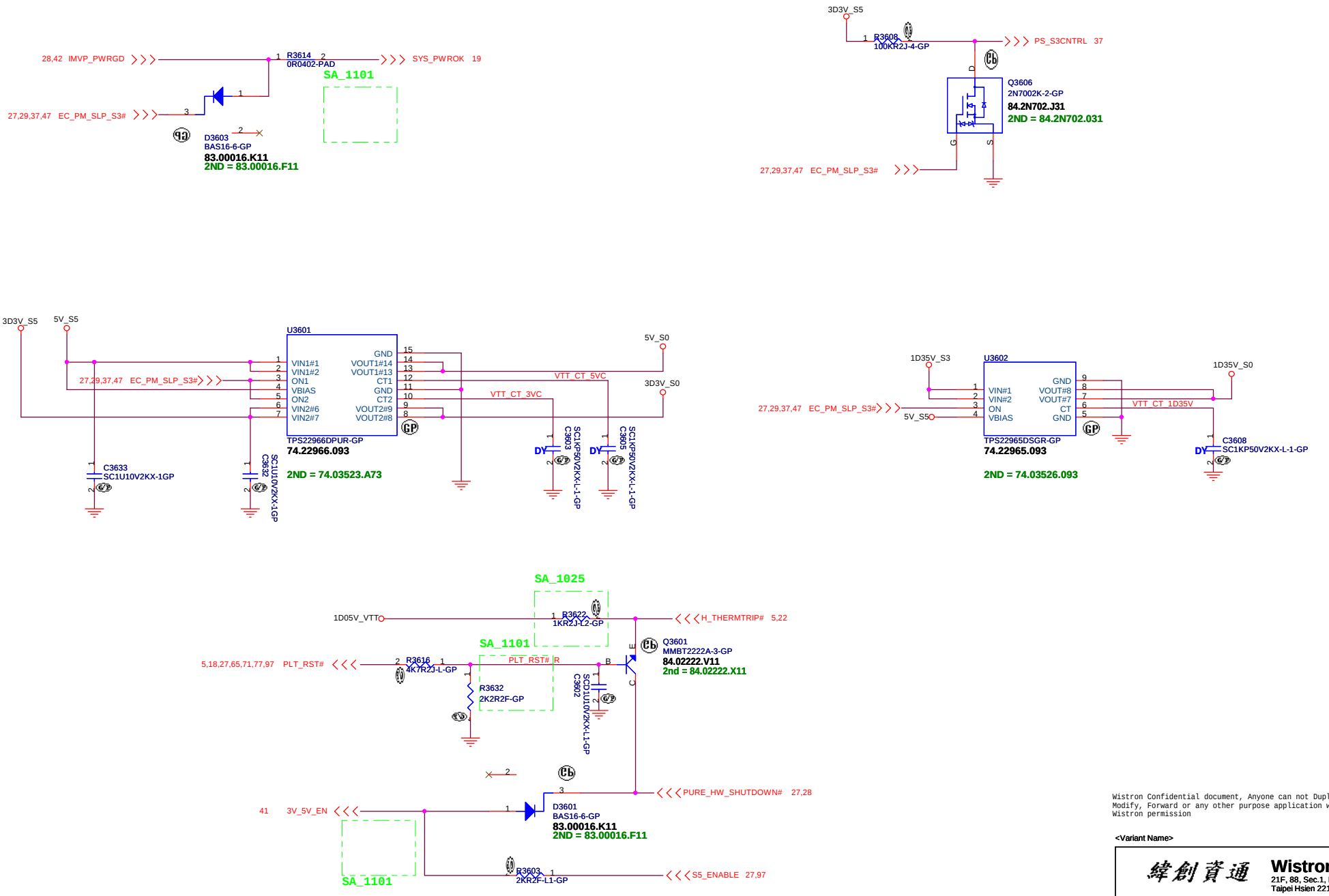
Title	***USB 3.0 Controller***	
Size A4	Document Number **Angel-CY**	Rev **1**
Date: Monday, April 22, 2013	Sheet 35 of 102	

Power Sequence



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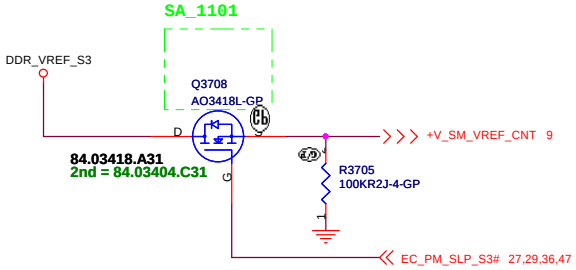
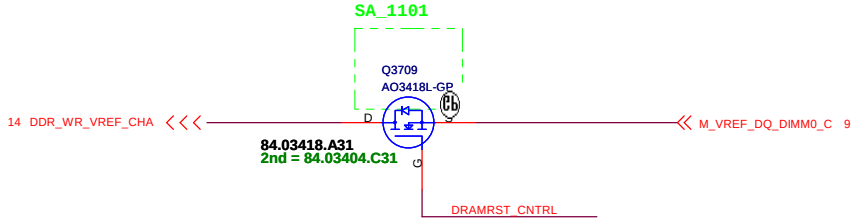
Title: **Power Plane Enable**

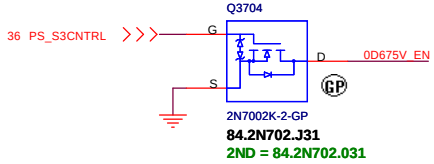
Size	Document Number	Rev
A3	Angel-CY	1

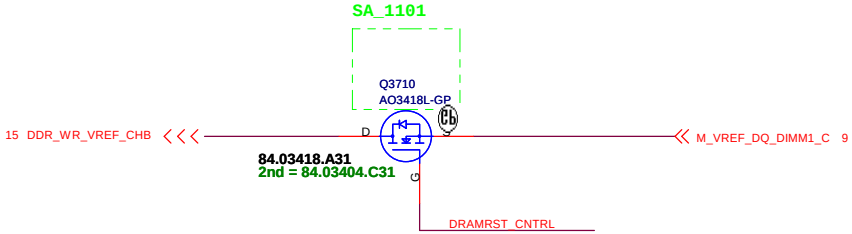
Date: Monday, April 22, 2013 Sheet 36 of 102

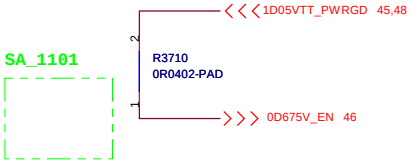
Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation



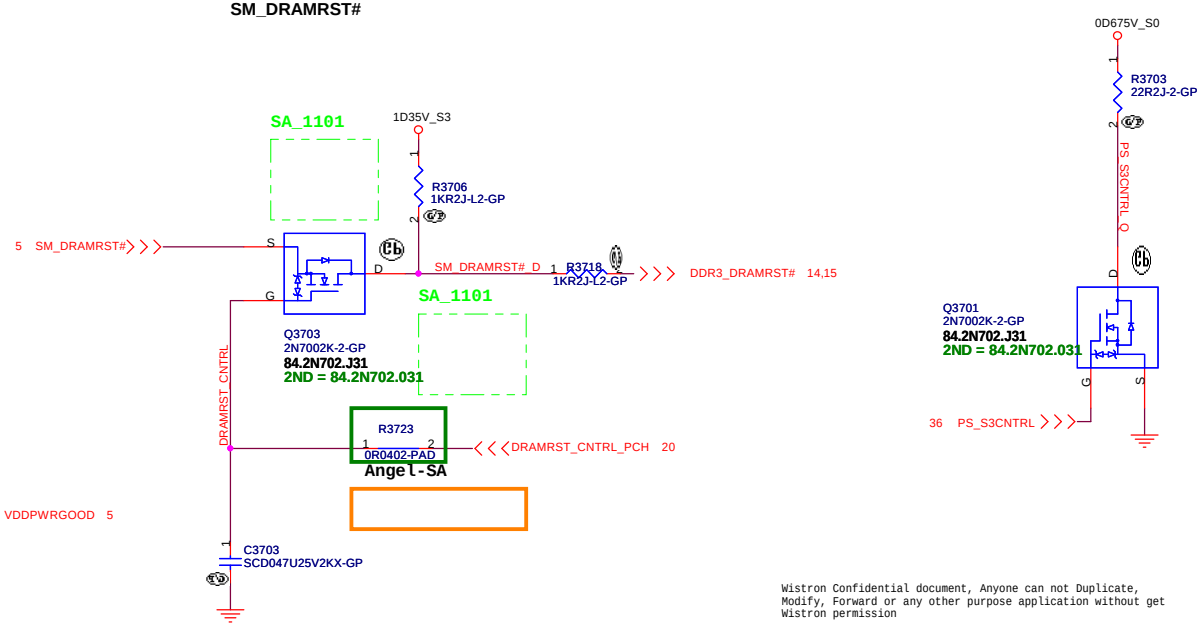




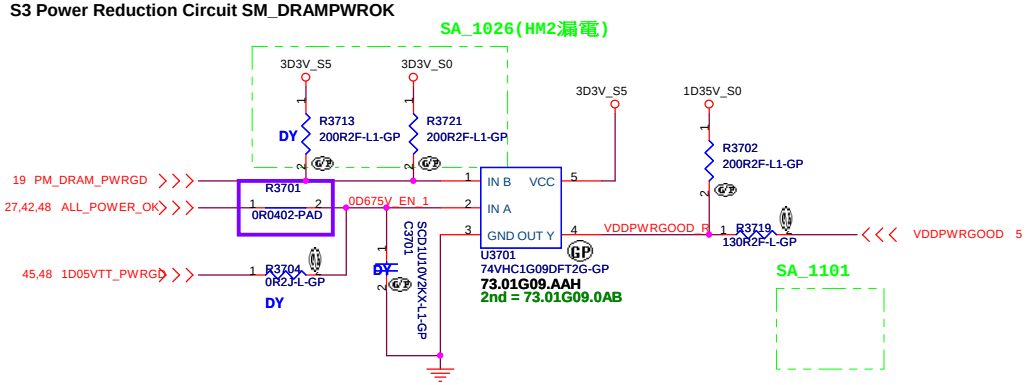




S3 Power Reduction Circuit
SM_DRAMRST#



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



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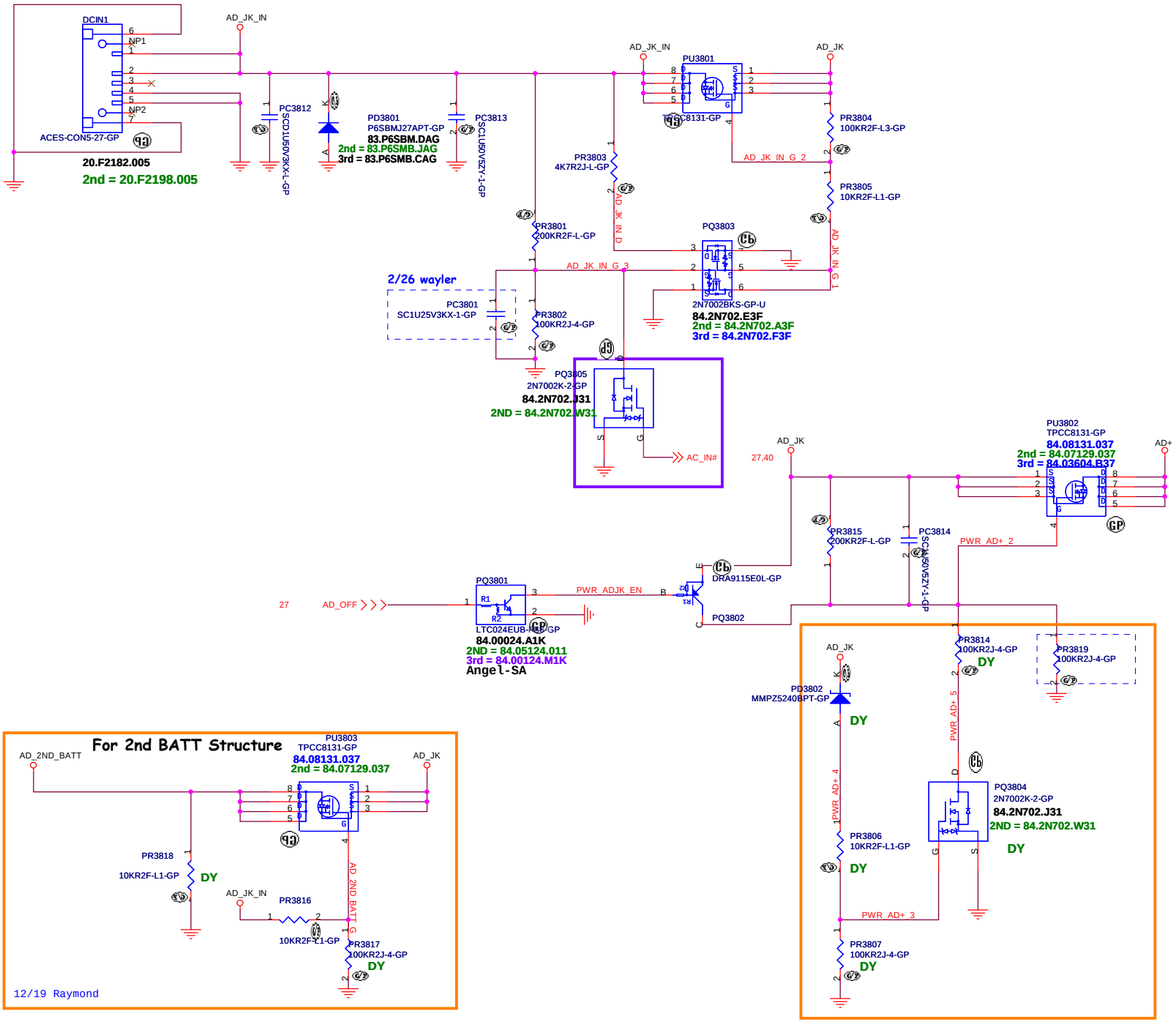
Title	ADAPTER	
Size A3	Document Number Angel-CY	Rev 1
Date: Monday, April 22, 2013	Sheet 37 of 102	

ANNIE solution

remember to check pin define

pitch = 2mm



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Title: DCIN JACK

Size: A3 | Document Number: Angel-CY | Rev: 1

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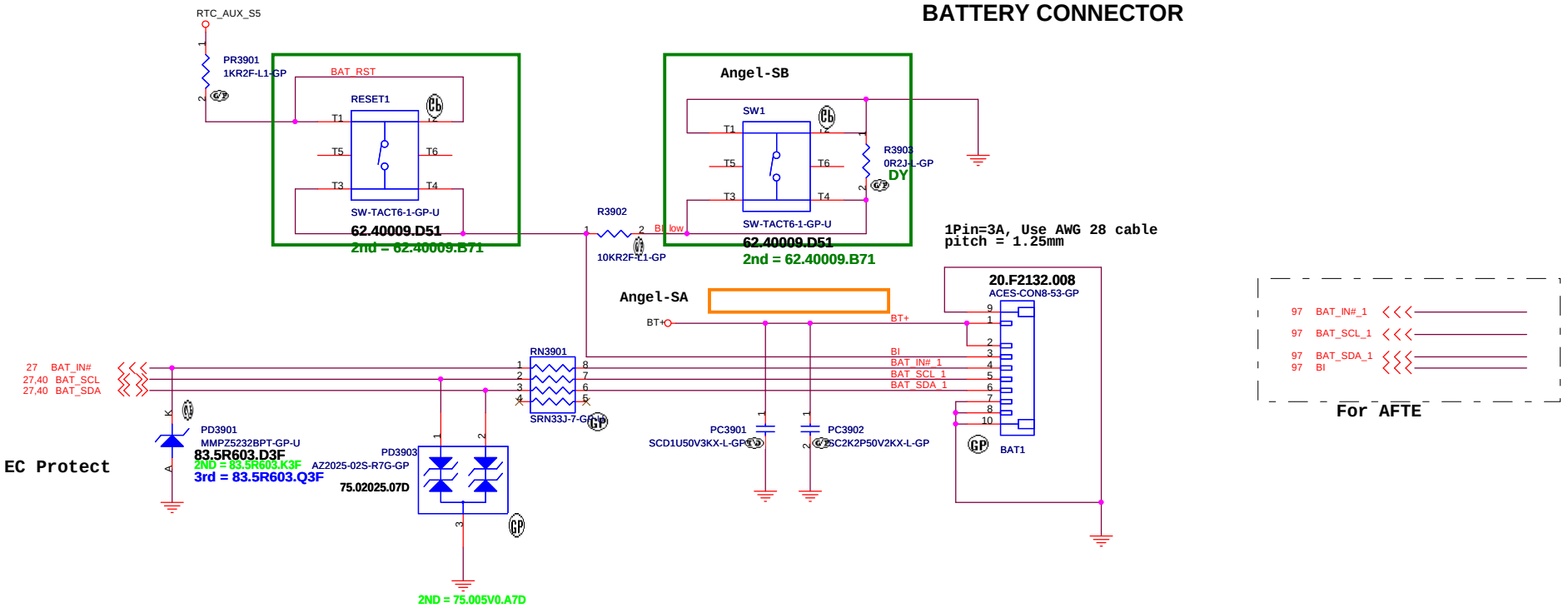
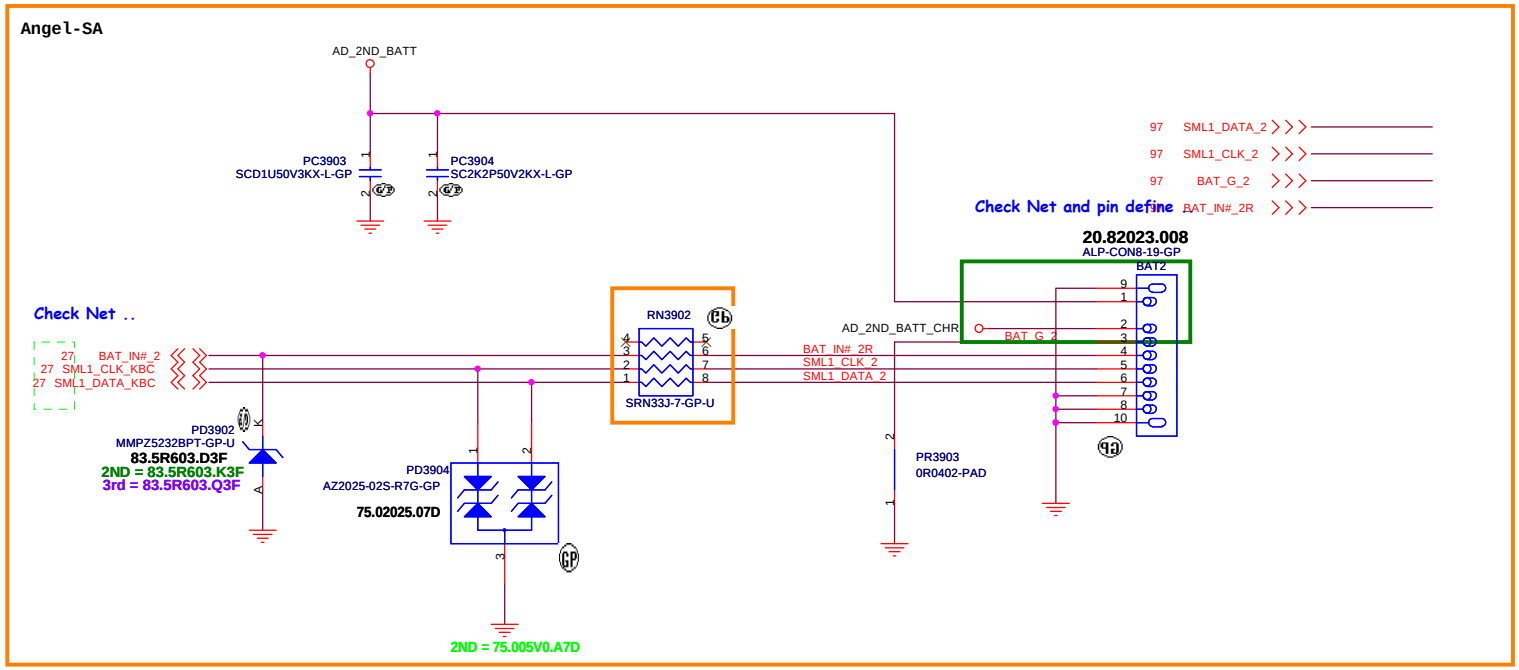
BATTERY CONNECTOR





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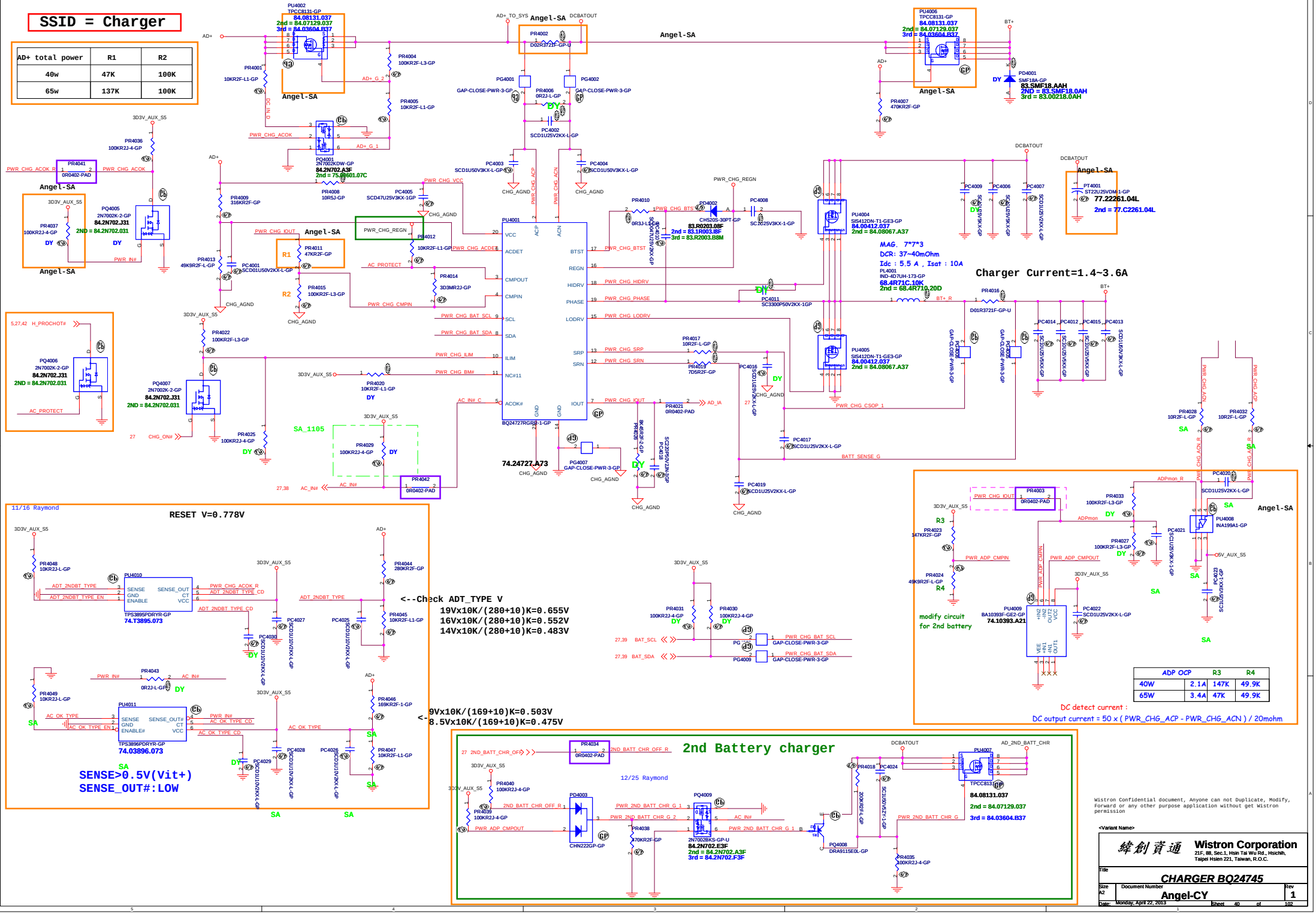
Title	BATT CONN	
Size A3	Document Number Angel-CY	Rev 1
Date: Monday, April 22, 2013	Sheet 39 of 102	

SSID = Charger

AD+ total power	R1	R2
40w	47K	100K
65w	137K	100K



ADP OCP	R3	R4
40W	2.1A	147K	49.9K
65W	3.4A	47K	49.9K

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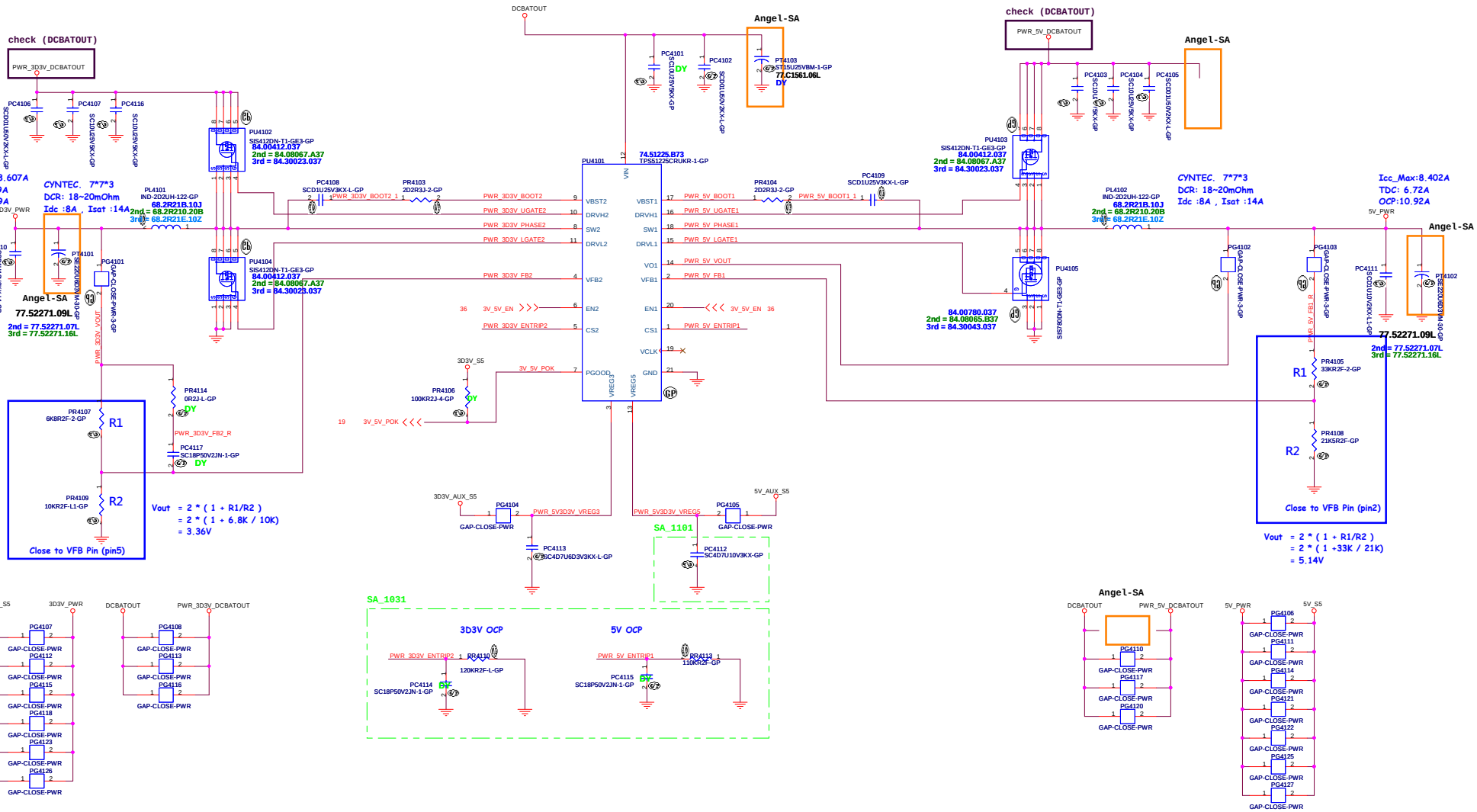
Title: **CHARGER BQ24745**

Size: A2 | Document Number: **Angel-CY** | Rev: 1

Date: Monday, April 22, 2013 | Sheet 40 of 102

SSID = PWR.Plane.Regulator_3p3v5v

check (UVP)



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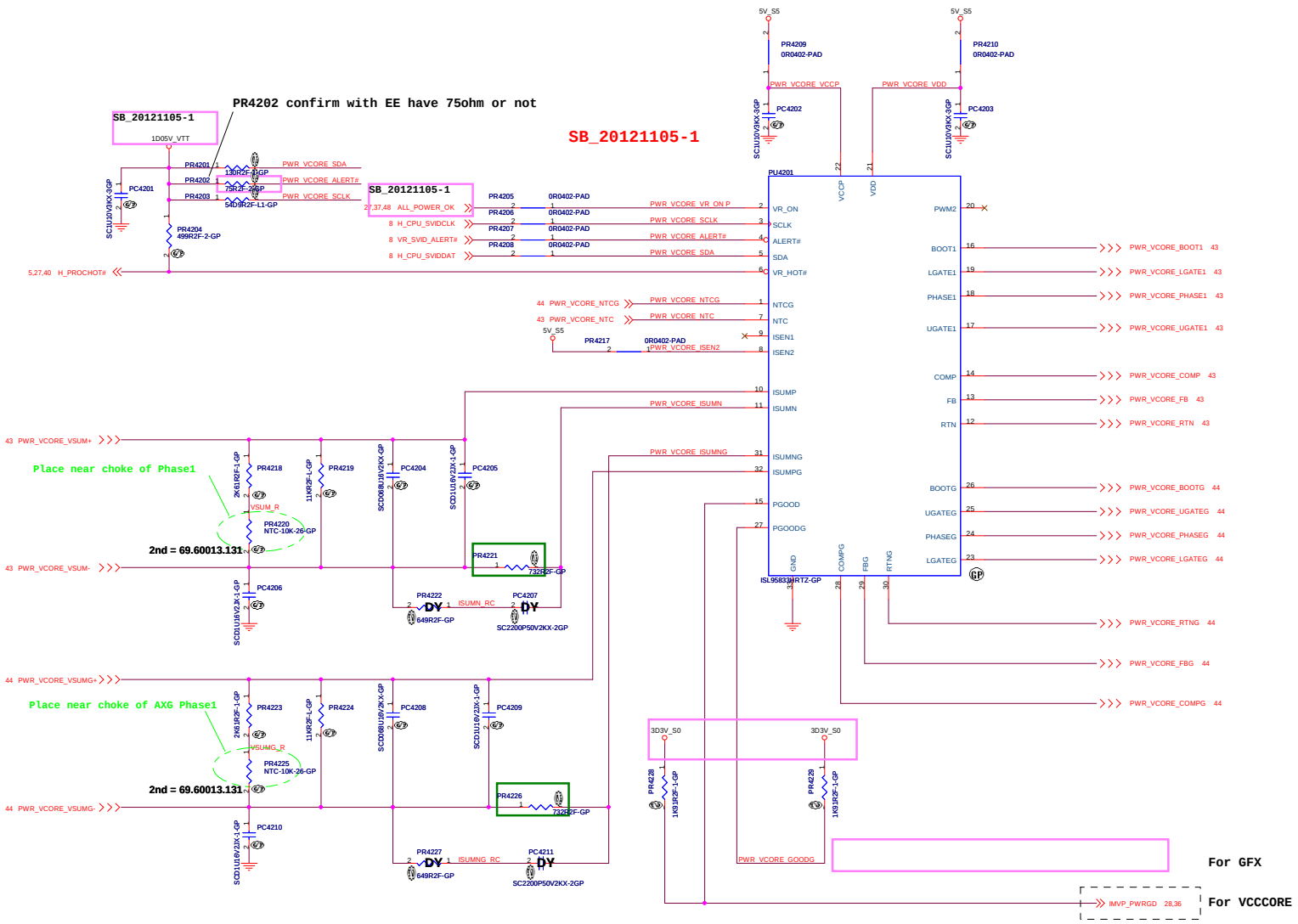
Title	TPS51125A 5V/3D3V	
Size: Custom	Document Number: Angel-CY	Rev: 1
Date: Monday, April 22, 2013	Sheet 41 of 102	

SSID = CPU.Regulator



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Title	ISL95833_CPU_CORE(1/3)	
Size: Custom	Document Number: Angel-CY	Rev: 1
Date: Monday, April 22, 2013	Sheet 42 of 103	

SB_20121105-1

BOM control

	Main source	2nd source
PU4301	84.03664.037 (FDMS3664S) Mount	
PU4302	84.03664.037 (FDMS3664S) DY	

BOM control

PU4301
FDMS3600-02-RJK0215-COLAY-GP
1st = 84.00920.037
2nd = 84.08107.B37
3rd = 84.00033.037

PWR_VCCCORE1_DCBATOUT
PC4303 SC10U25V5KX-GP
PC4304 SC10U25V5KX-GP
PC4305 SC10U25V5KX-GP

SA_20121019
DCBATOUT
PWR_VCCCORE1_DCBATOUT
PG4301 GAP-CLOSE-PWR
PG4304 GAP-CLOSE-PWR
PG4307 GAP-CLOSE-PWR
PG4308 GAP-CLOSE-PWR
PG4309 GAP-CLOSE-PWR
PG4310 GAP-CLOSE-PWR

42 PWR_VCORE_BOOT1
42 PWR_VCORE_UGATE1
42 PWR_VCORE_PHASE1
42 PWR_VCORE_LGATE1
PR4301 2D2R3-1-U-GP
BOOT1_RC
PC4301 SCD22U50V3ZY-1GP

Pana . 7 x 7 x 4
DCR 1.8~2.3 mOhm
Isat : 32A

VCC_CORE
PL4301 IND-D36UH-42-GP
68.R361A.10B
PG4319 GAP-CLOSE-PWR-3-GP
PG4323 GAP-CLOSE-PWR-3-GP
PT4305 ST470U2VDM-3GR-U1
PT4304 ST470U2VDM-3GR-U1
79.47719.2FL
2nd = 77.24771.01L
79.47719.2FL
2nd = 77.24771.01L

PR4314 3K83R2F-GP
NTC_RC
PR4315 16K9R2F-GP
PR4316 NTC-470K-8-GP
2nd = 69.60013.141
PWR_VCORE_NTC 42
NTC Place near high side MOSFET of Phase1

42 PWR_VCORE_VSUM+
PR4302 3K65R2F-1-GP
PWR_VCORE_VSUM+_GAP
42 PWR_VCORE_VSUM-
PR4303 1R2F-GP
PWR_VCORE_VSUM-_GAP
Parallel

42 PWR_VCORE_COMP
PR4304 42K2R2F-L-GP
42 PWR_VCORE_FB

PR4305 499R2F-2-GP
FB_RC
PC4306 SC470P50V2KX-3GP
PC4307 SC47P50V2JN-3GP
PR4306 1K62R2F-GP
PR4307 267KR2F-GP
COMP_RC
PC4308 SC150P50V2JN-3GP
PR4308 2KR2F-3-GP
COMP_R
PC4309 SC680P50V2KX-2GP

SA_20121019
PWR_VCCCORE1_DCBATOUT
DCBATOUT
PG4311 GAP-CLOSE-PWR
PG4312 GAP-CLOSE-PWR
PG4313 GAP-CLOSE-PWR
PG4314 GAP-CLOSE-PWR
PG4315 GAP-CLOSE-PWR
PG4316 GAP-CLOSE-PWR
PG4320 GAP-CLOSE-PWR
PG4321 GAP-CLOSE-PWR

PC4310 SC330P50V2JC-2-GP
DY
PC4311 SCD01U50V2KX-1GP
R4301 0R0402-PAD
42 PWR_VCORE_RTN
VCCSENSE 8
VSSSENSE 8
Parallel

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Title: ISL95833_CPU_CORE(2/3)
Size: Custom
Document Number: Angel-CY
Rev: 1
Date: Monday, April 22, 2013
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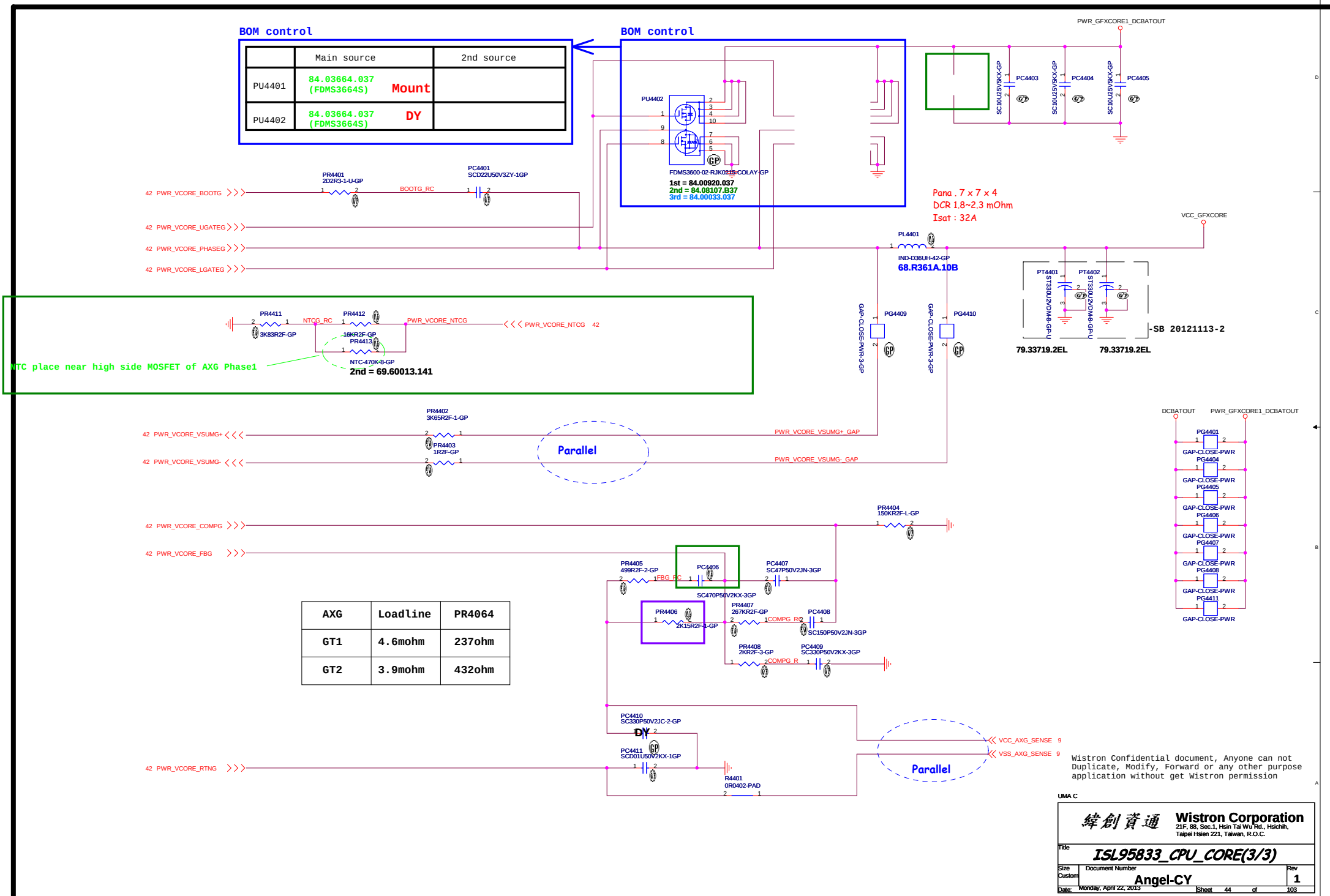
SB_20121105-1



AXG	Loadline	PR4064
GT1	4.6mohm	237ohm
GT2	3.9mohm	432ohm

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Title: ISL95833_CPU_CORE(3/3)

Size: Custom | Document Number: Angel-CY | Rev: 1

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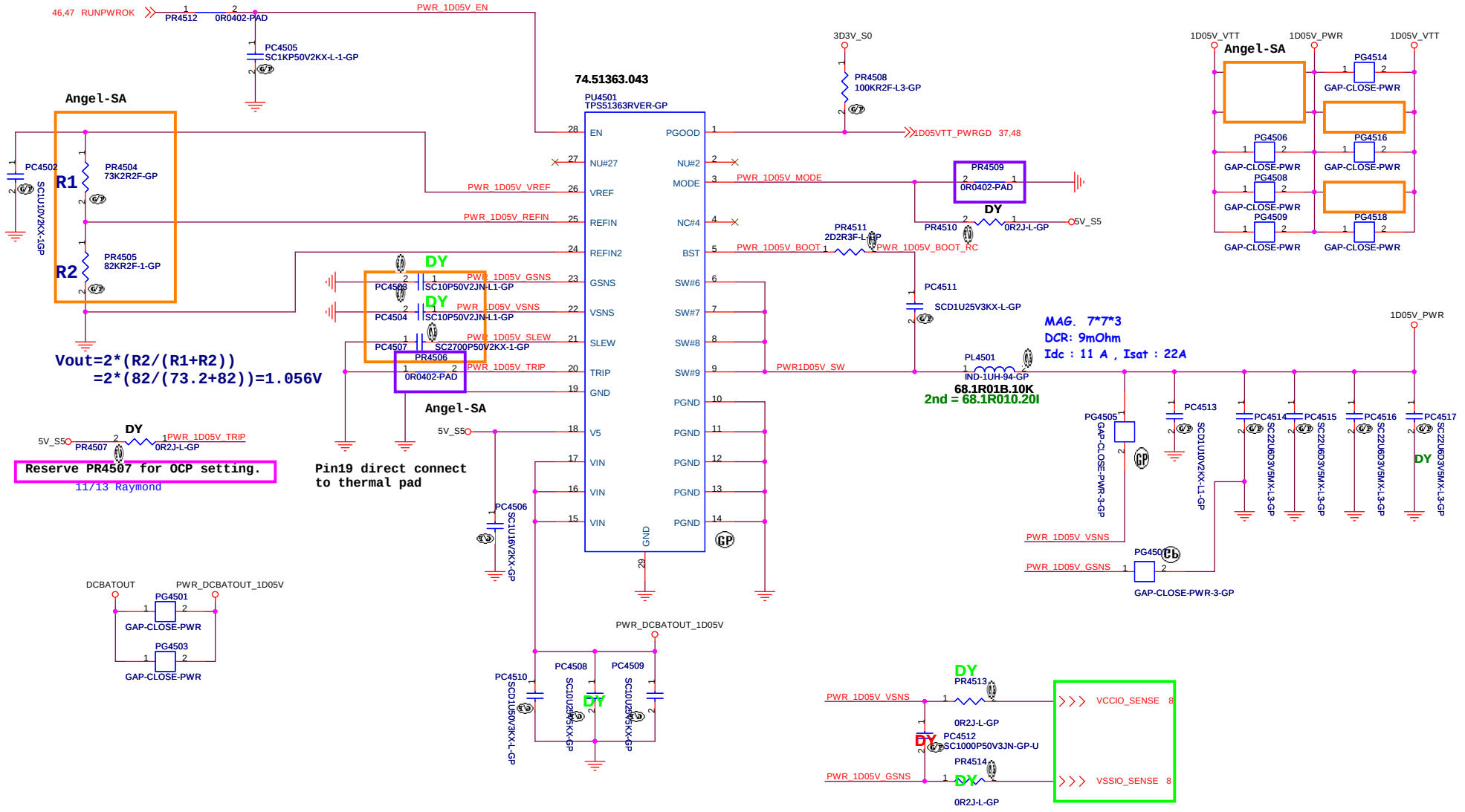
TPS51363 for 1D05V



HR PX

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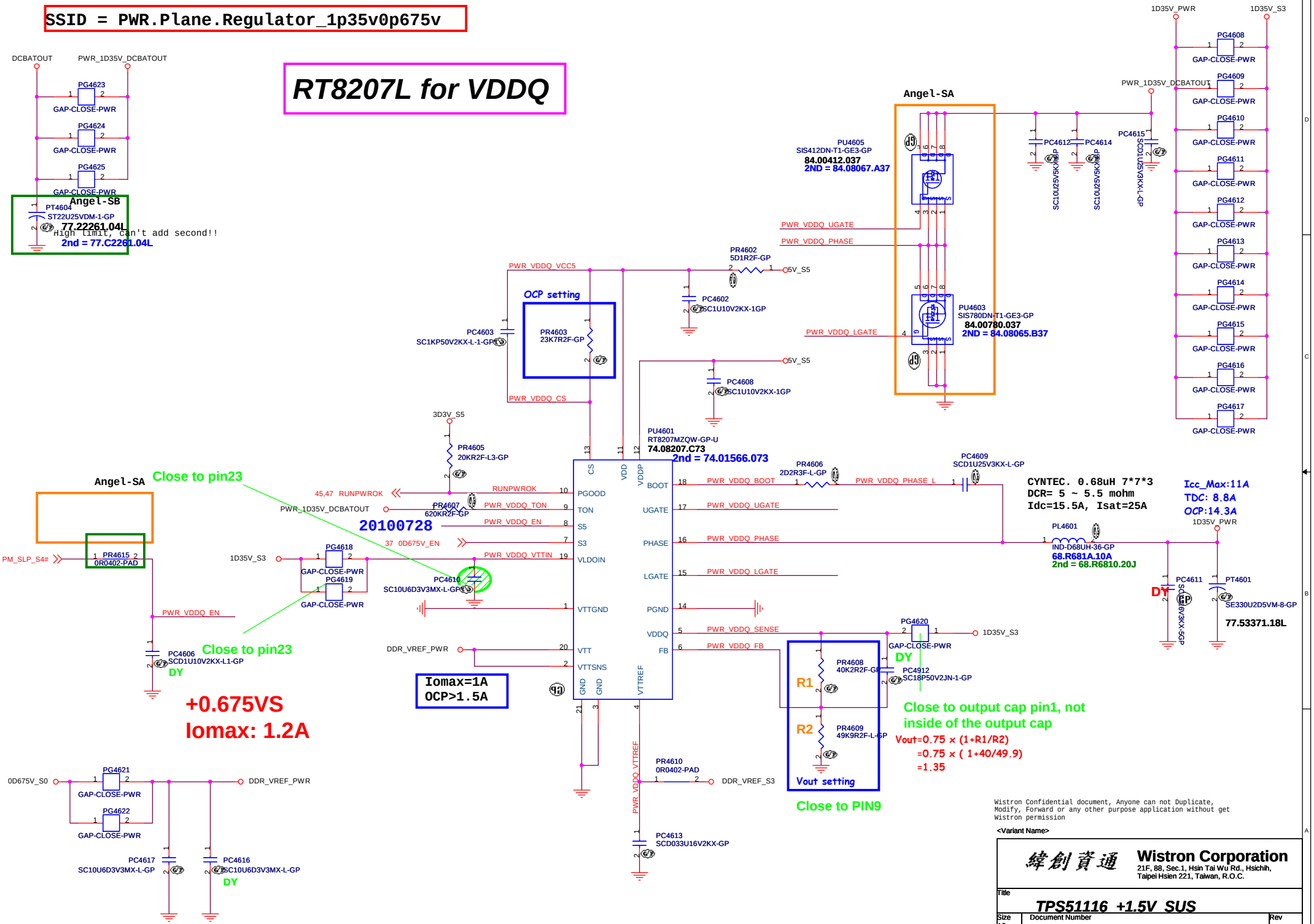
Title: *DC to DC 1D05V(TPS51218D)*

Size	Document Number	Rev
A3	Angel-CY	1

Date: Monday, April 22, 2013 Sheet 45 of 102

SSID = PWR.Plane.Regulator_1p35v0p675v

RT8207L for VDDQ



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<Variant Name>

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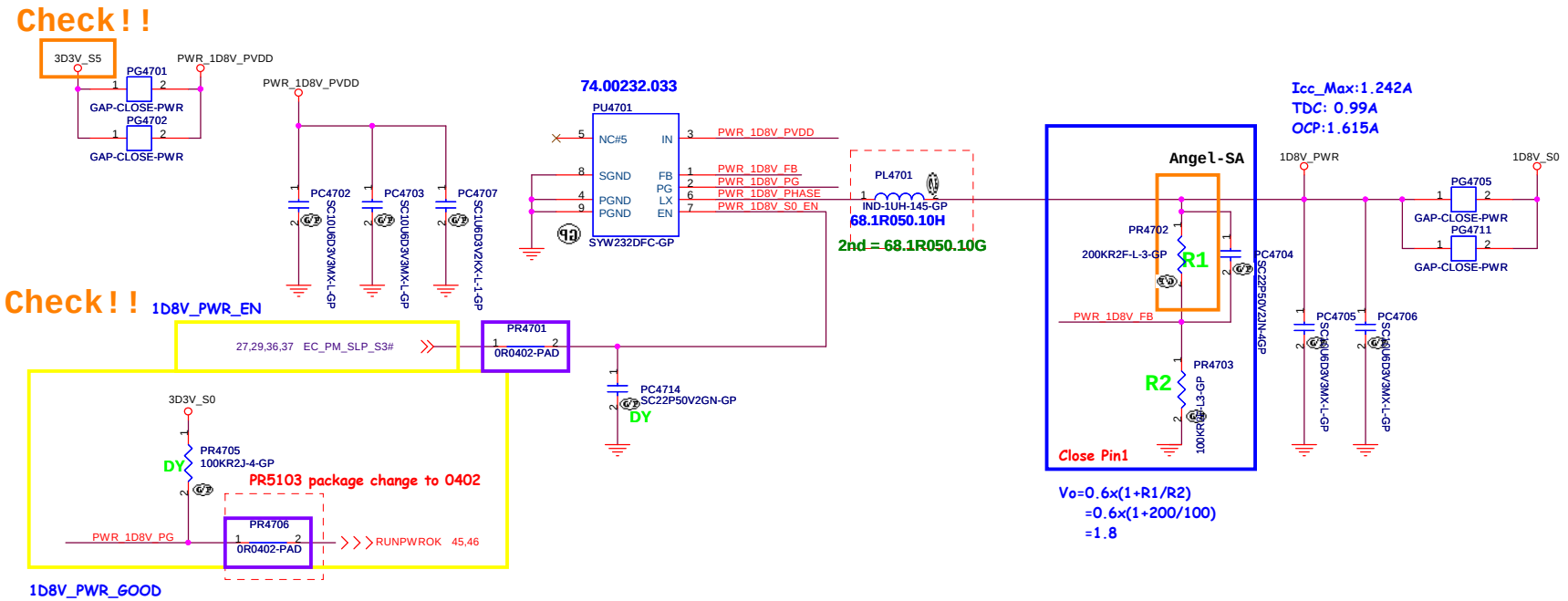
Title: TPS51116 +1.5V SUS

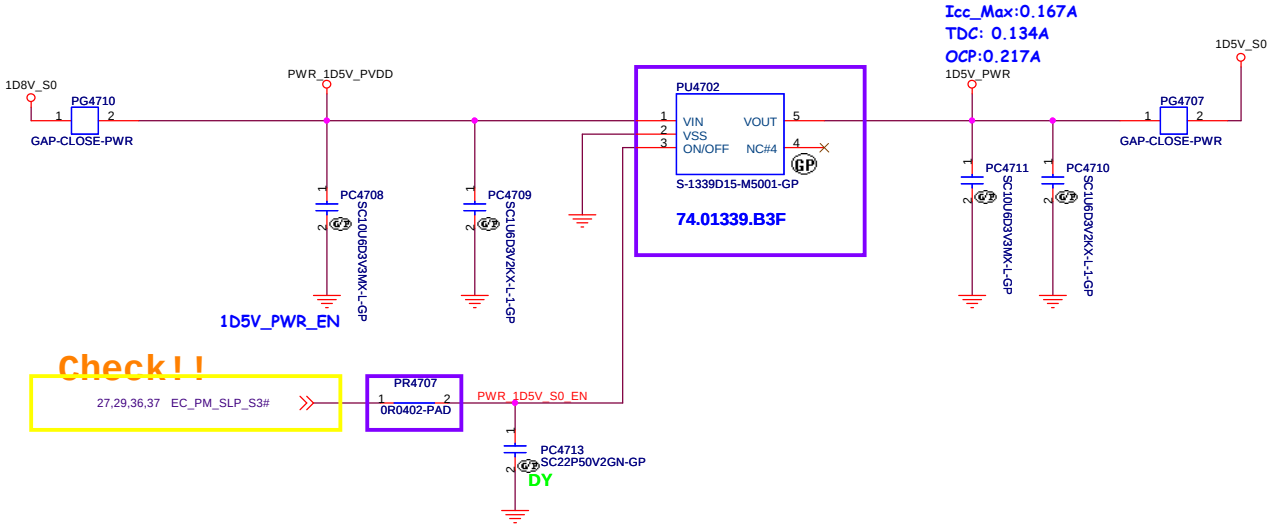
Size	Document Number	Rev
A3	Angel-CY	1

Date: Monday, April 22, 2013 Sheet 46 of 102

SSID = PWR.Plane.Regulator_1p8v



S-1339D15 for +1.5V



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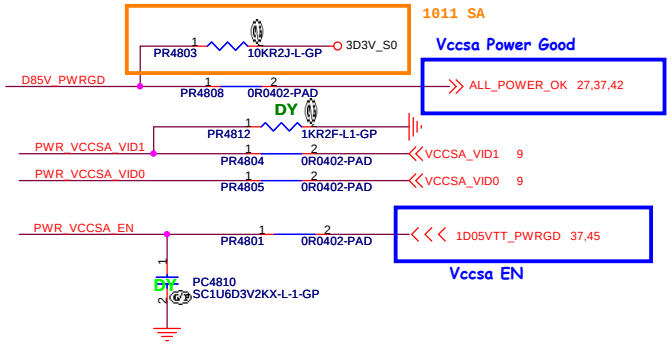
Title	DC CONVERTER_1D8V&1D5V	
Size A3	Document Number Angel-CY	Rev 1
Date: Monday, April 22, 2013	Sheet 47 of 102	

LDO G978 for VCCSA



D0, D1 V_O Selection Table

D0	D1	V_O, MODE=0	V_O, MODE=1
0	0	0.9V	0.9V
0	1	0.8V	0.85V
1	0	0.725V	0.775V
1	1	0.675V	0.75V

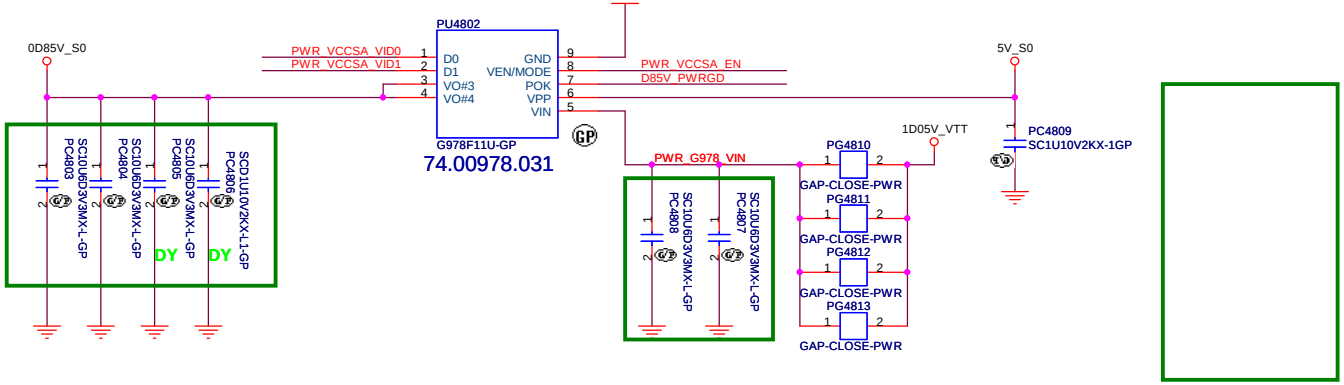
"x" means "don't care".

VEN/MODE Logic

VEN/MODE (VPP=5V)	EN logic
<0.6V	0
>1.0V	1

VEN/MODE (VPP=5V)	MODE logic
<2.0V	0
>2.6V	1

Design Current =4 A



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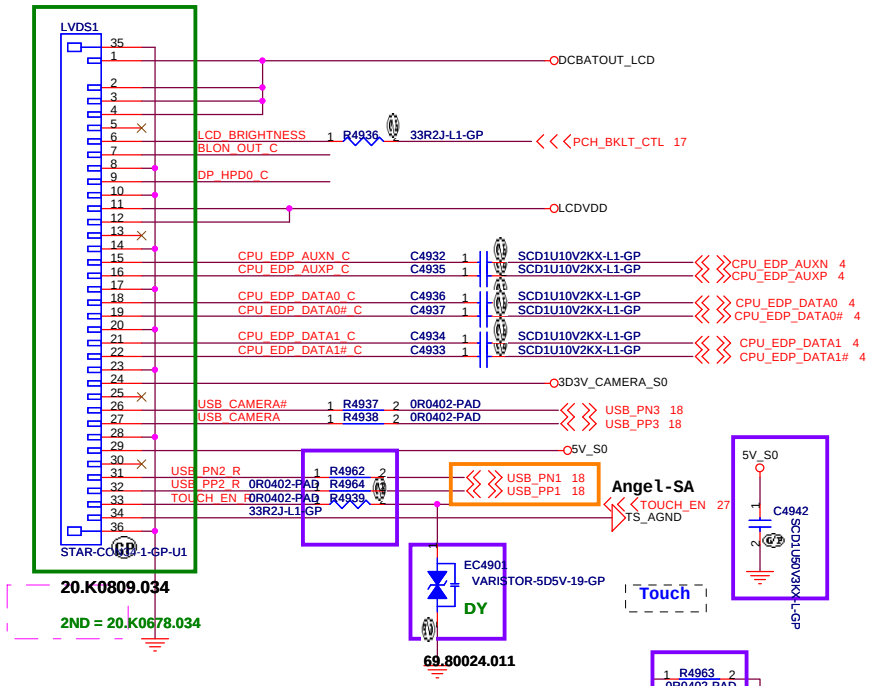
Title: *VCCSA LDO G978*

Size: A3 | Document Number: Angel-CY | Rev: 1

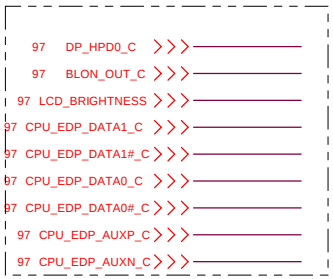
Date: Monday, April 22, 2013 | Sheet 48 of 103

SSID = VIDEO

Angel-SA

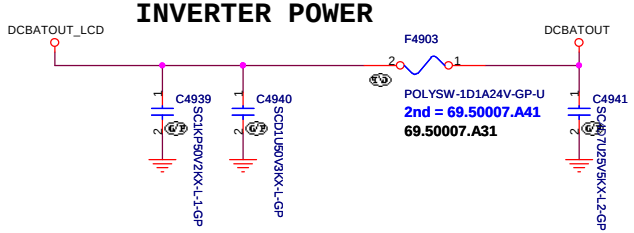


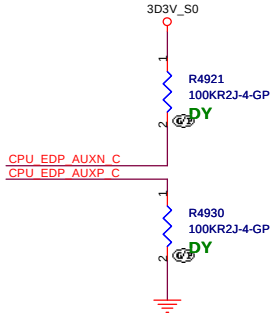
J1 Pin Assignment	
1	USB5V
2	D-
3	D+
4	GND
5	GND
6	INT



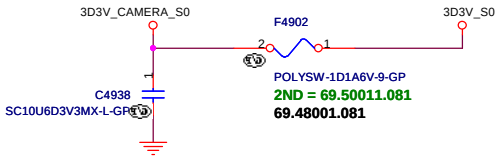
For AFTE

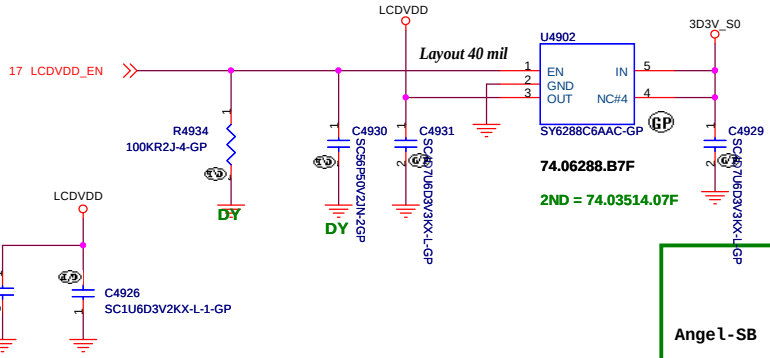
INVERTER POWER

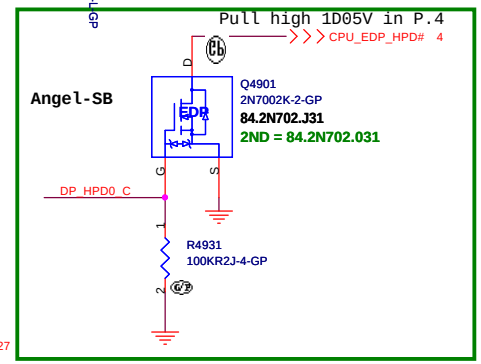


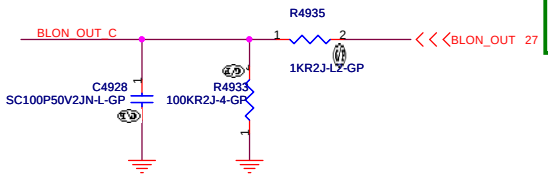


Camera Power









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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD Connector

Size: A3 | Document Number: Angel-CY | Rev: 1

Date: Monday, April 22, 2013 | Sheet 49 of 102

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Title	CRT Connector	
Size A4	Document Number Angel-CY	Rev 1
Date: Monday, April 22, 2013	Sheet 50 of 102	

HDMI Level Shifter & CONNECTOR

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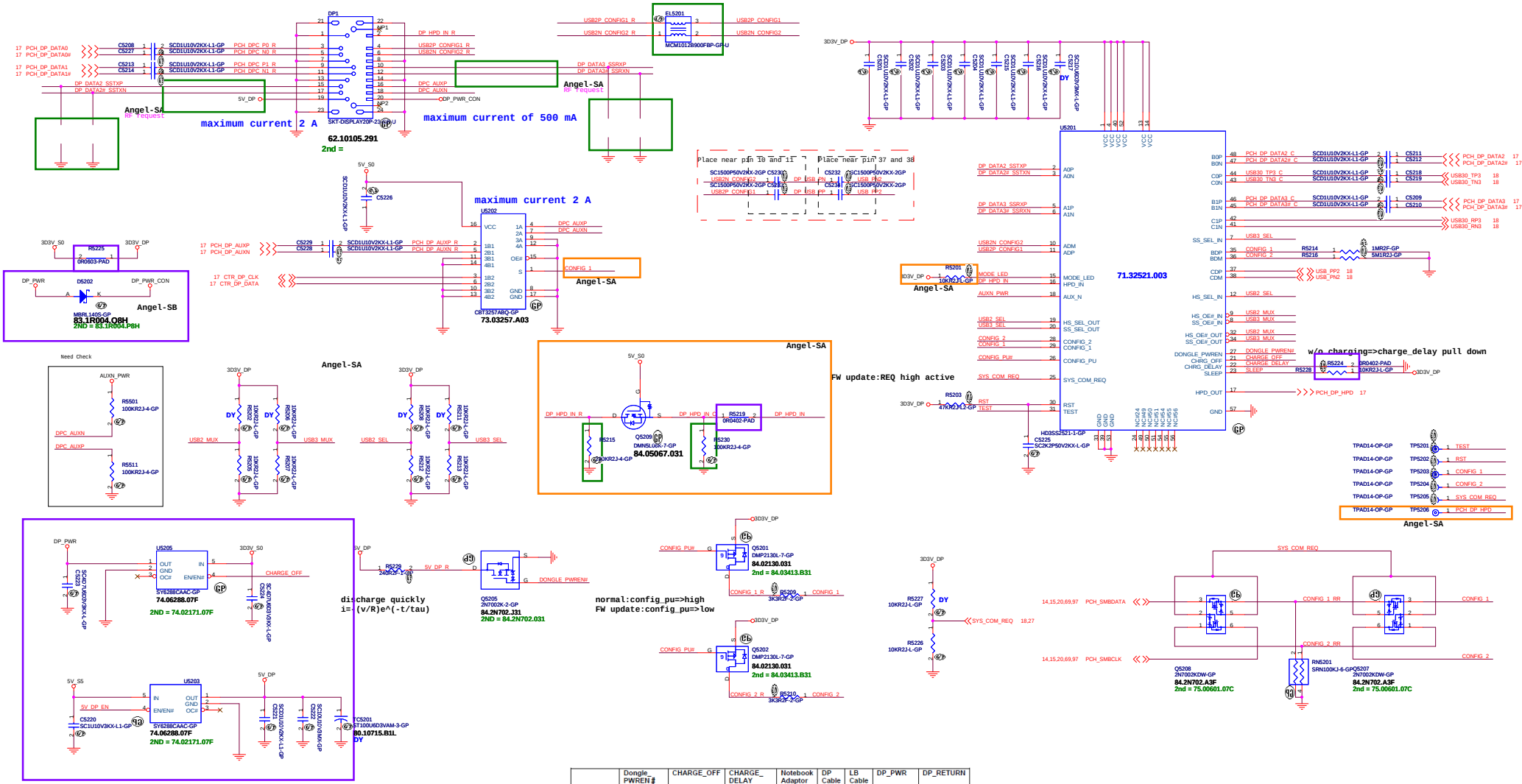
Title	HDMI Level Shifter/Connector	
Size A3	Document Number Angel-CY	Rev 1
Date: Monday, April 22, 2013	Sheet 51 of 102	



	Dongle_PWREN#	CHARGE_OFF	CHARGE_DELAY	Notebook Adaptor	DP Cable	LB Cable	DP_PWR	DP_RETURN
Display Mode – Cable connected	1	1	0	Don't care	x		3.3V OUT	GND
Display Mode – no cable connected	1	1	0	Don't care	NC	NC	3.3V OUT	GND
DOCKPORT no charging mode	0	0	0	x		x	Floating	Floating
DOCK PORT charging mode (valid only if LB cable is plugged in)	0	0	1			x	5V/12V/19V IN	5V/12V/19V IN
USB Charging/ Dongle mode	0	1	0	X		X	3.3V OUT	5VOUT

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Title: **Display Port**

Size: Custom | Document Number: **Angel-CY** | Rev: 1

Date: Monday, April 22, 2013 | Sheet 52 of 102

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Title	S-VIDEO	
Size A4	Document Number Angel-CY	Rev 1
Date: Monday, April 22, 2013	Sheet 53 of 102	

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Title	***Reserved***	
Size A4	Document Number **Angel-CY**	Rev **1**
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SSID = User.Interface

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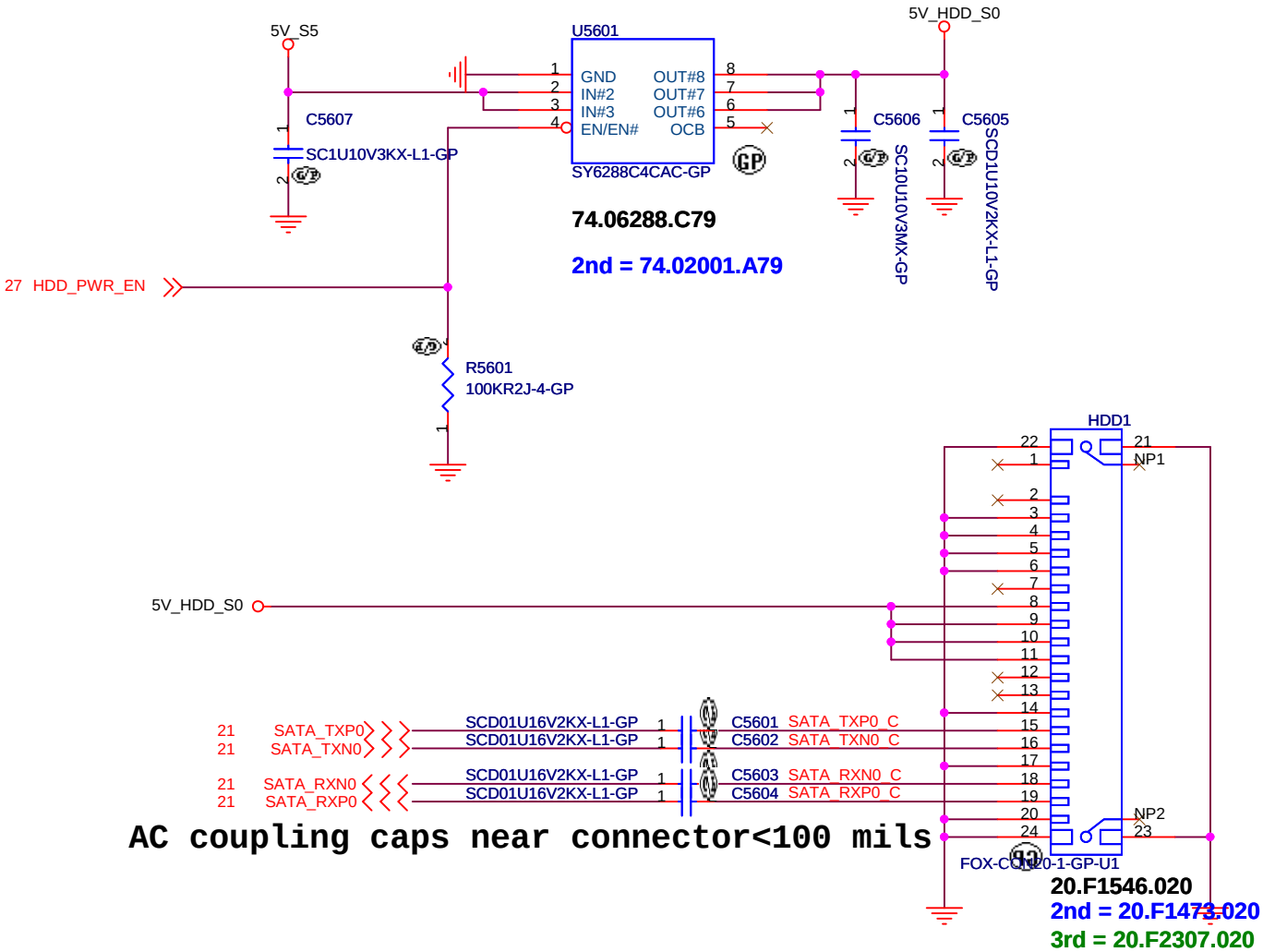
Title	ITP	
Size A4	Document Number Angel-CY	Rev 1
Date: Monday, April 22, 2013	Sheet 55 of 102	

SATA HDD Connector



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Title		
HDD		
Size A4	Document Number Angel-CY	Rev 1
Date: Monday, April 22, 2013	Sheet 56 of 102	

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<Variant Name>

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Title	E-SATA/USB CHARGER	
Size A4	Document Number Angel-CY	Rev 1
Date: Monday, April 22, 2013	Sheet 57 of 102	

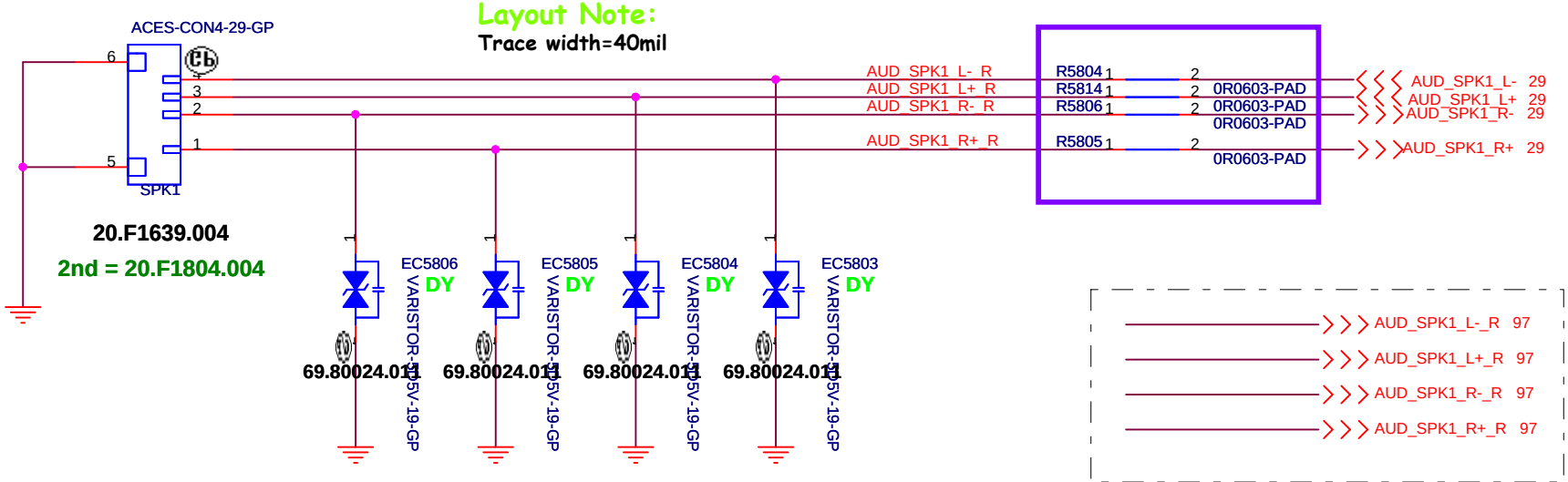
SSID = AUDIO

SSID = AUDIO

Speaker

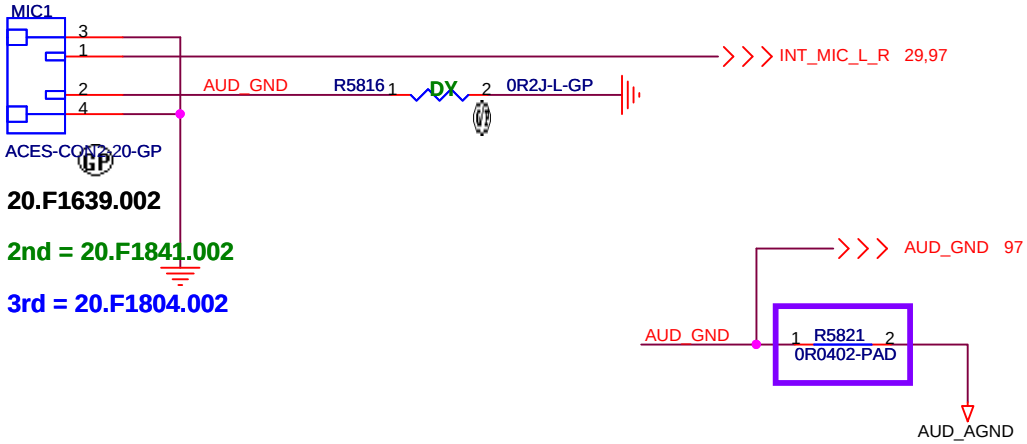
SA
10/22 change by Edwin
Pin Define SWAP

Layout Note:
Trace width=40mil



For AFTE

Combo Jack on Small Board



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Title	MIC/SPEAKER/JACK	
Size A4	Document Number Angel-CY	Rev 1
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1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

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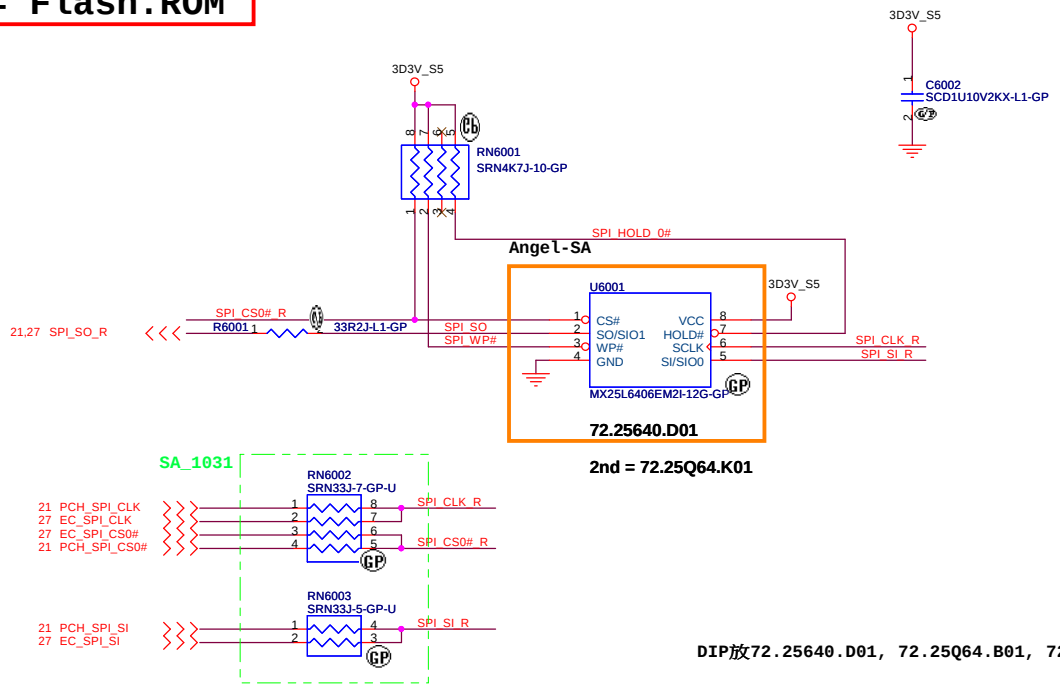
Title	LAN CONNECTOR	
Size A4	Document Number Angel-CY	Rev 1
Date: Monday, April 22, 2013	Sheet 59 of 102	

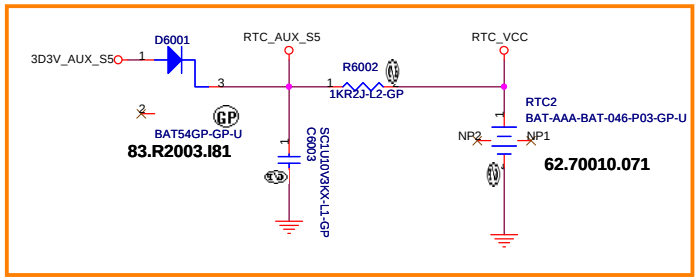
SSID = Flash.ROM



DIP放72.25640.D01, 72.25Q64.B01, 72.25Q64.A03

SSID = RBATT

Angel-SA



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Title	Flash/RTC	
Size Custom	Document Number Angel-CY	Rev 1
Date: Monday, April 22, 2013	Sheet 60 of 102	

SSID = USB

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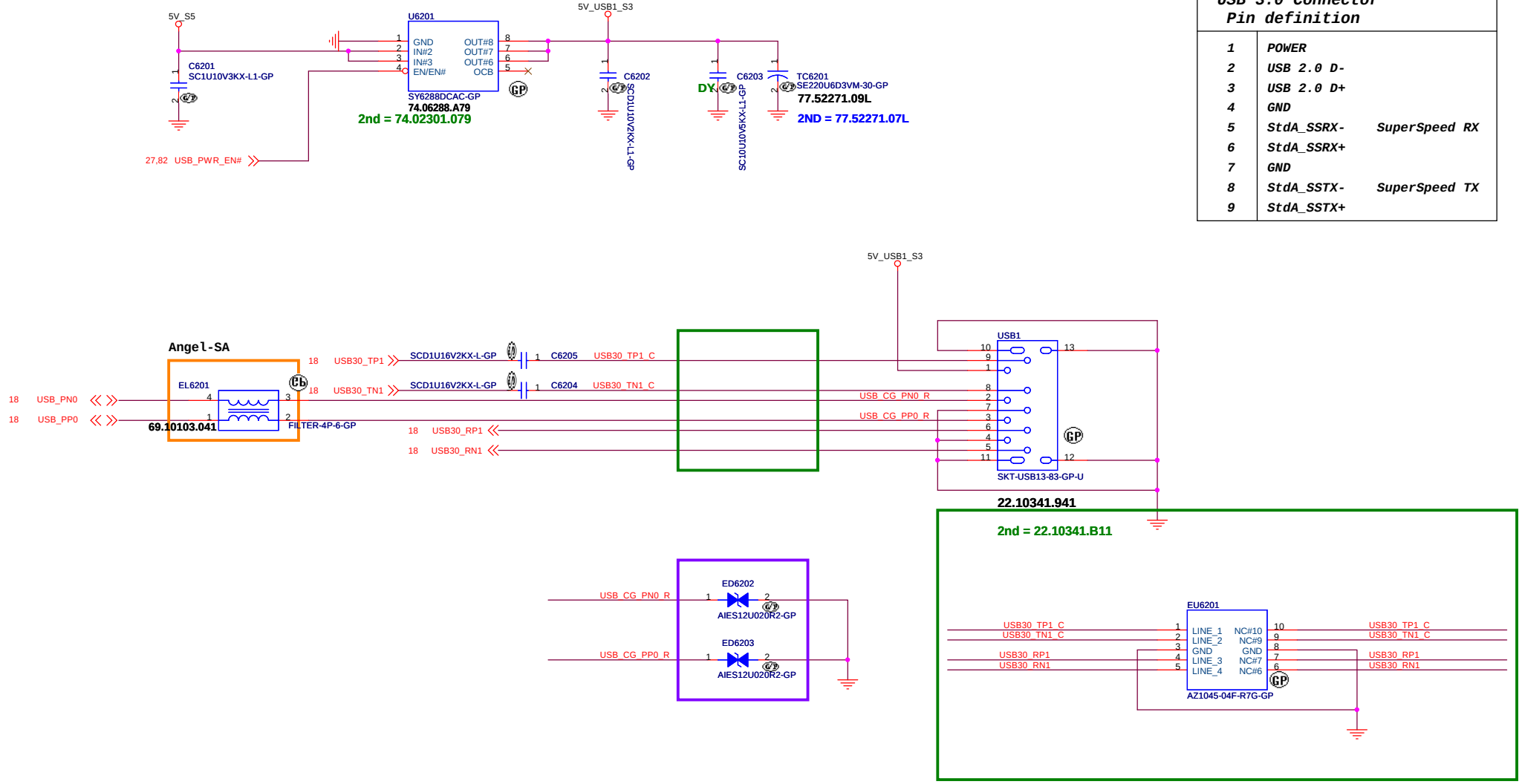
Title	***USB Power SW***	
Size A4	Document Number **Angel-CY**	Rev **1**
Date: Monday, April 22, 2013	Sheet 61 of 102	



USB 3.0 Connector Pin definition		
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

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Title: USB 3.0 Port

Size: A3 | Document Number: Angel-CY | Rev: 1

Date: Monday, April 22, 2013 | Sheet 62 of 102

SSID = User.Interface

Bluetooth Module conn.

Without BT

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Title	Bluetooth	
Size A4	Document Number Angel-CY	Rev 1
Date: Monday, April 22, 2013	Sheet 63 of 102	

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Title

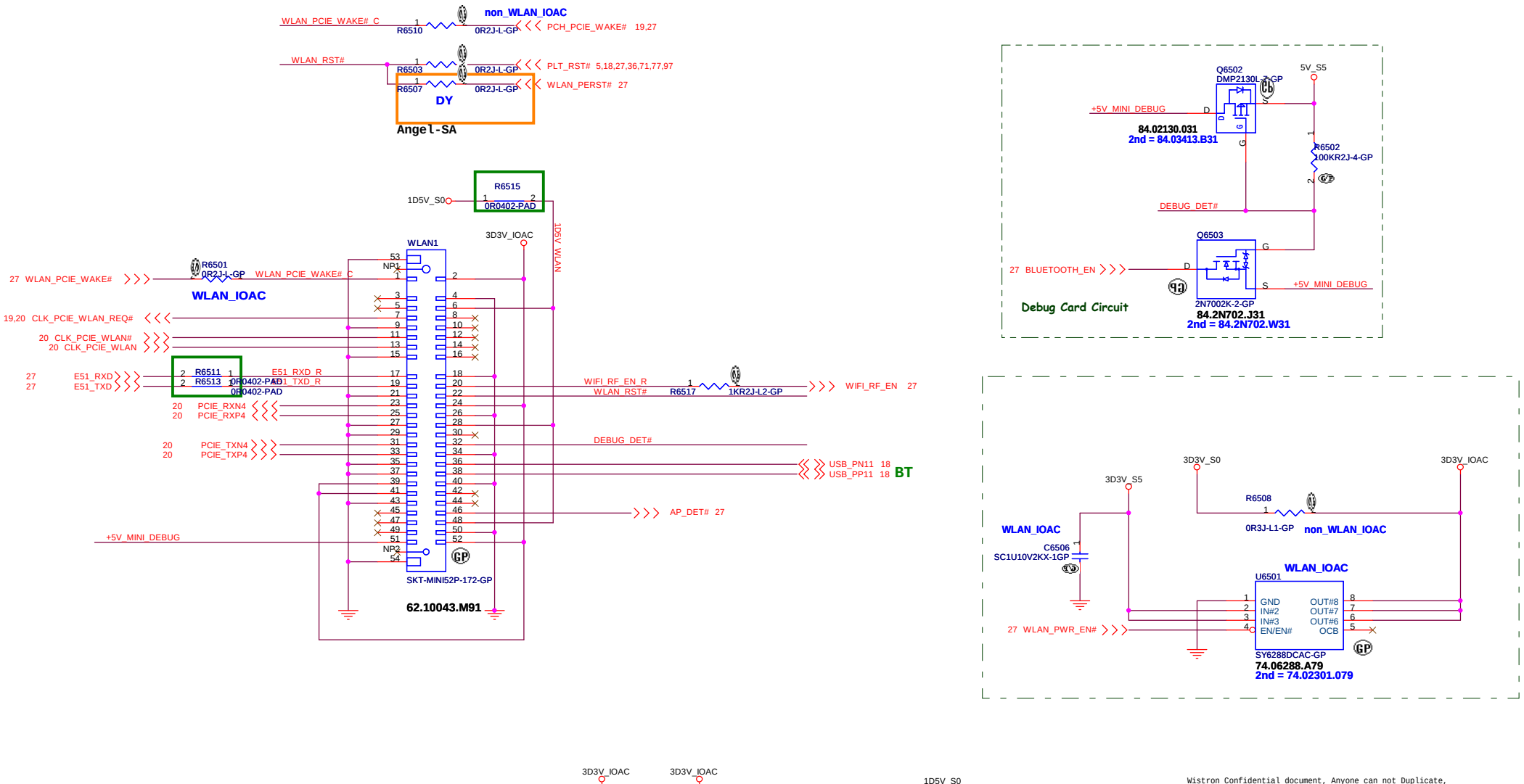
RESERVED

Size	Document Number	Rev
A4	**Angel-CY**	**1**

Date: Monday, April 22, 2013 Sheet 64 of 102

SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



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Title: MINICARD(WLAN)

Size: A3 | Document Number: Angel-CY | Rev: 1

Date: Monday, April 22, 2013 | Sheet 65 of 102

SSID = Wireless

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Title	WWAN Connector	
Size A4	Document Number Angel-CY	Rev 1
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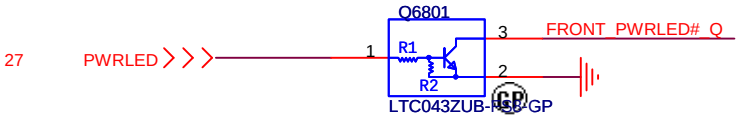
Title	***M-SATA***	
Size A4	Document Number **Angel-CY**	Rev **1**
Date: Monday, April 22, 2013	Sheet 67 of 102	

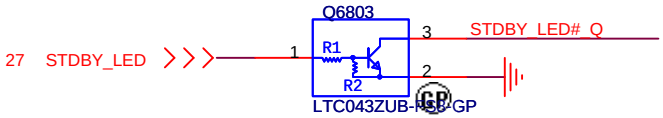
SSID = User.Interface

Power button LED



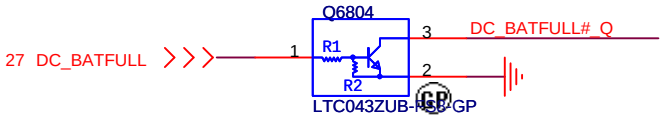
84.00043.011
2nd = 84.00143.D1K

Power STDBY_LED



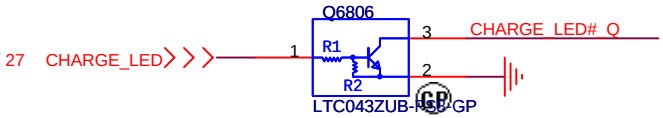
84.00043.011
2nd = 84.00143.D1K

Battery LED2(DC_BATFULL)

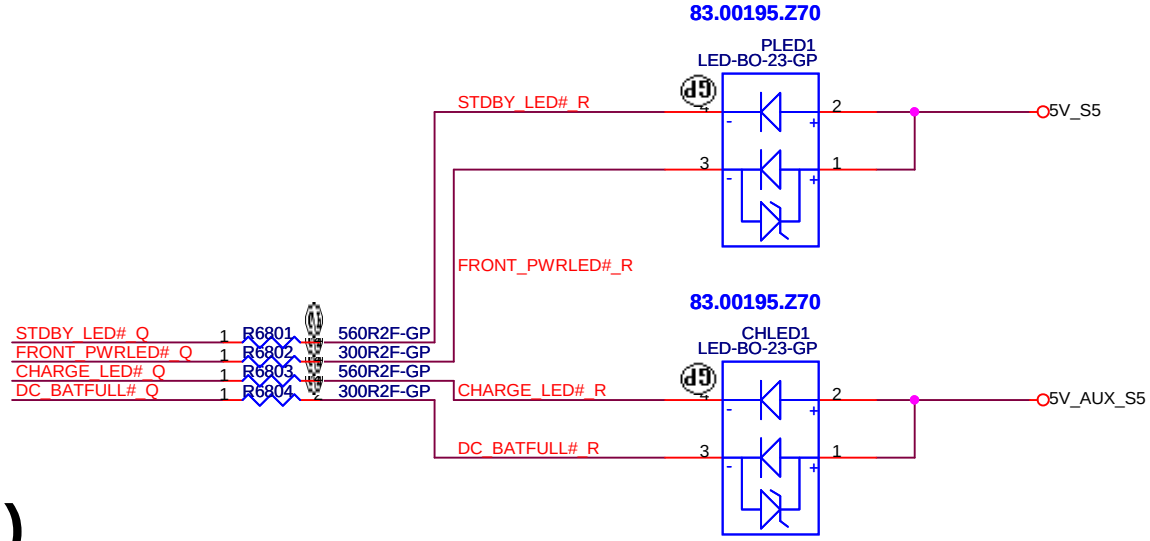


84.00043.011
2nd = 84.00143.D1K

Battery LED1(CHARGE)



84.00043.011
2nd = 84.00143.D1K



Devices

Part No.	Lens	Source Color	Pin Assignment
LTST-C195ZBKFKT	Water Clear	InGaN Blue	1,3
		AlInGaP Orange	2,4

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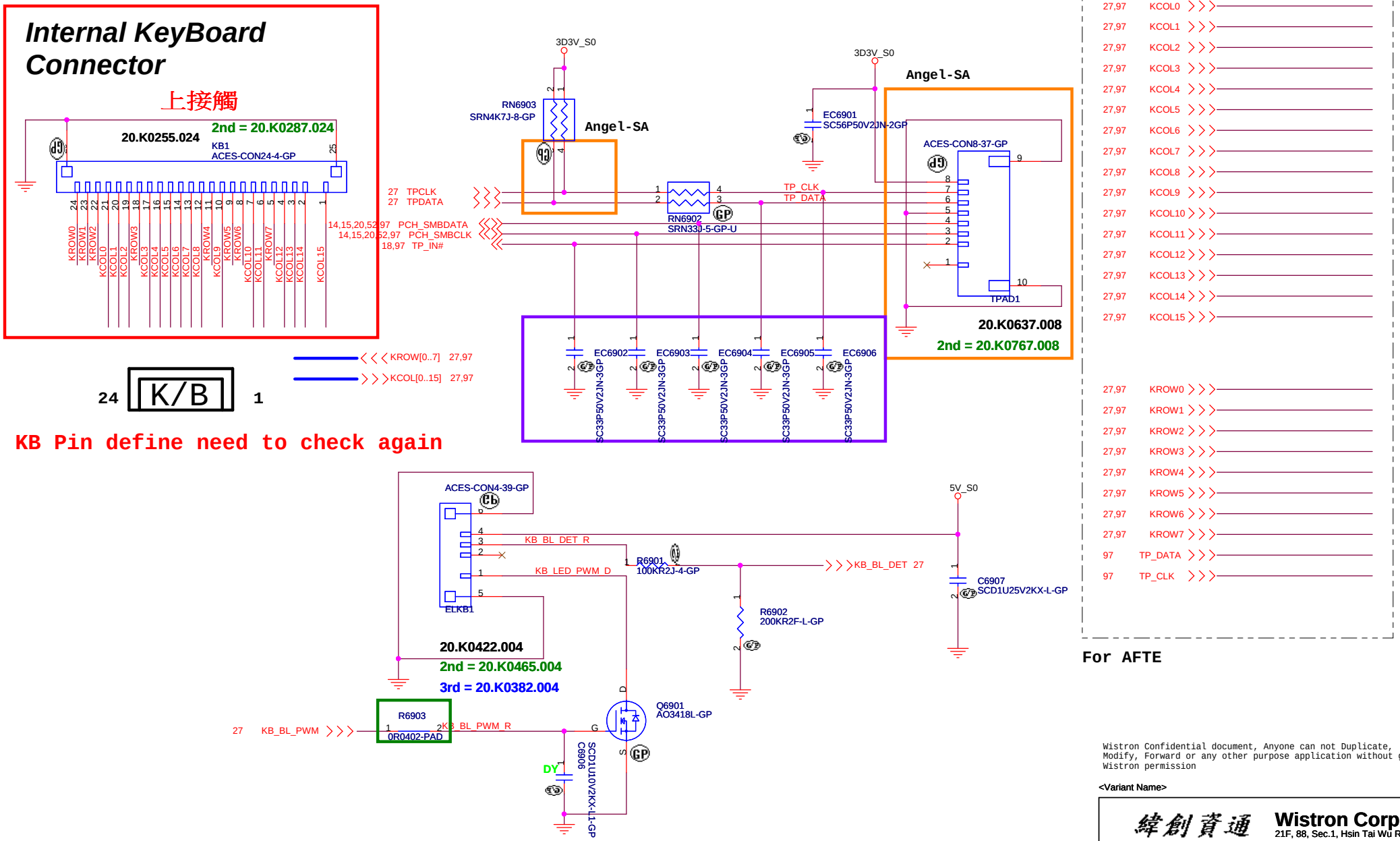
Title: *LED Bard/Power Button*

Size	Document Number	Rev
A4	Angel-CY	1

Date: Monday, April 22, 2013 Sheet 68 of 102

TOUCH PAD

D = KBC



For AFTE

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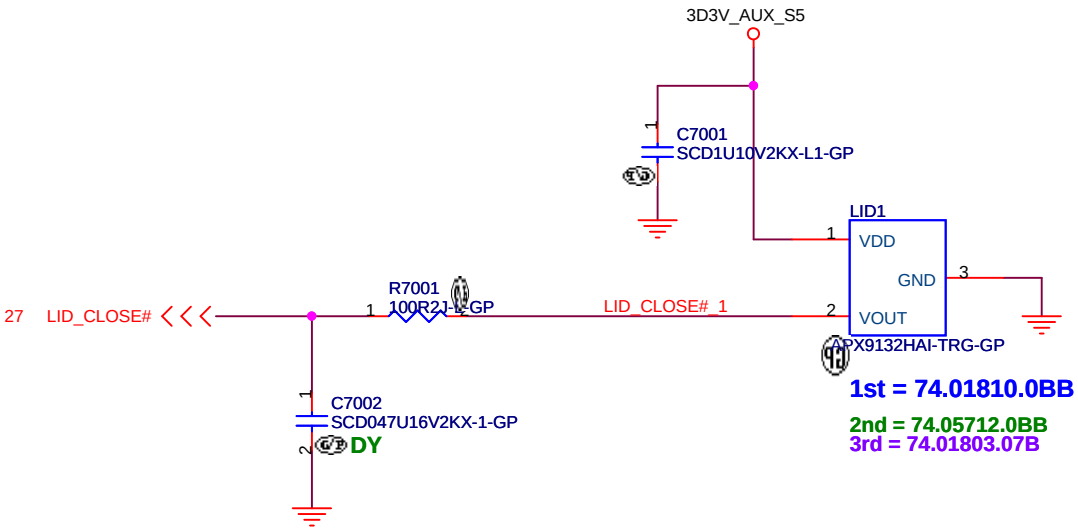
Title	Key Board/Touch Pad	
Size Custom	Document Number Angel-CY	Rev 1
Date: Monday, April 22, 2013	Sheet 69 of 102	



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<Variant Name>

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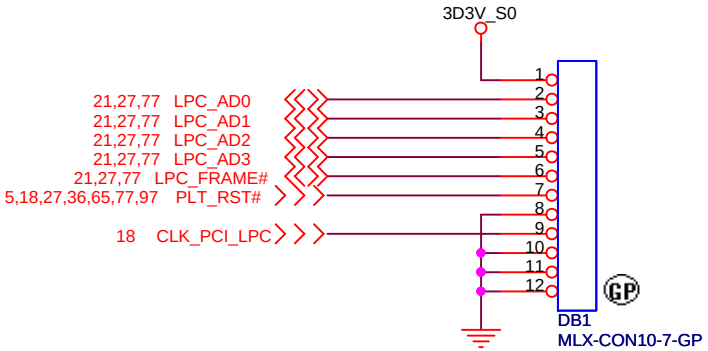
Title: **Hall Sensor**

Size	Document Number	Rev
A4	Angel-CY	1

Date: Monday, April 22, 2013 Sheet 70 of 102



DB

1st = 20.F0714.010

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Title	***Dubug connector***	
Size A4	Document Number **Angel-CY**	Rev **1**
Date: Monday, April 22, 2013	Sheet 71 of 102	

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Title	***Reserved***	
Size A4	Document Number **Angel-CY**	Rev **1**
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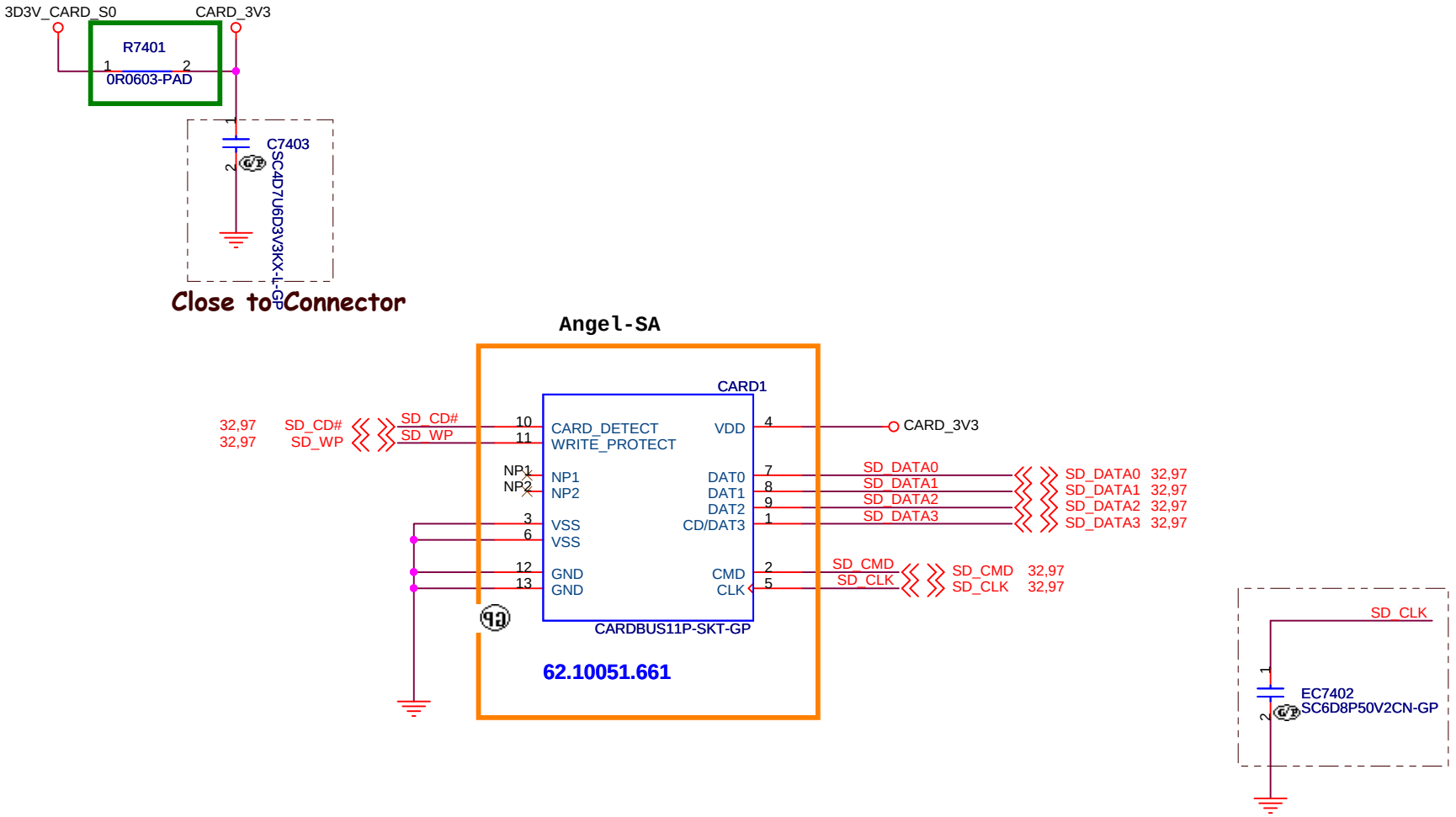
Title	***Reserved***	
Size A4	Document Number **Angel-CY**	Rev **1**
Date: Monday, April 22, 2013	Sheet 73 of 102	

SD/XD/MS Card Reader



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Title	CARD Reader CONN	
Size A4	Document Number Angel-CY	Rev 1
Date: Monday, April 22, 2013	Sheet 74 of 102	

SSID = ExpressCard

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Title	New Card	
Size A4	Document Number Angel-CY	Rev 1
Date: Monday, April 22, 2013	Sheet 75 of 102	

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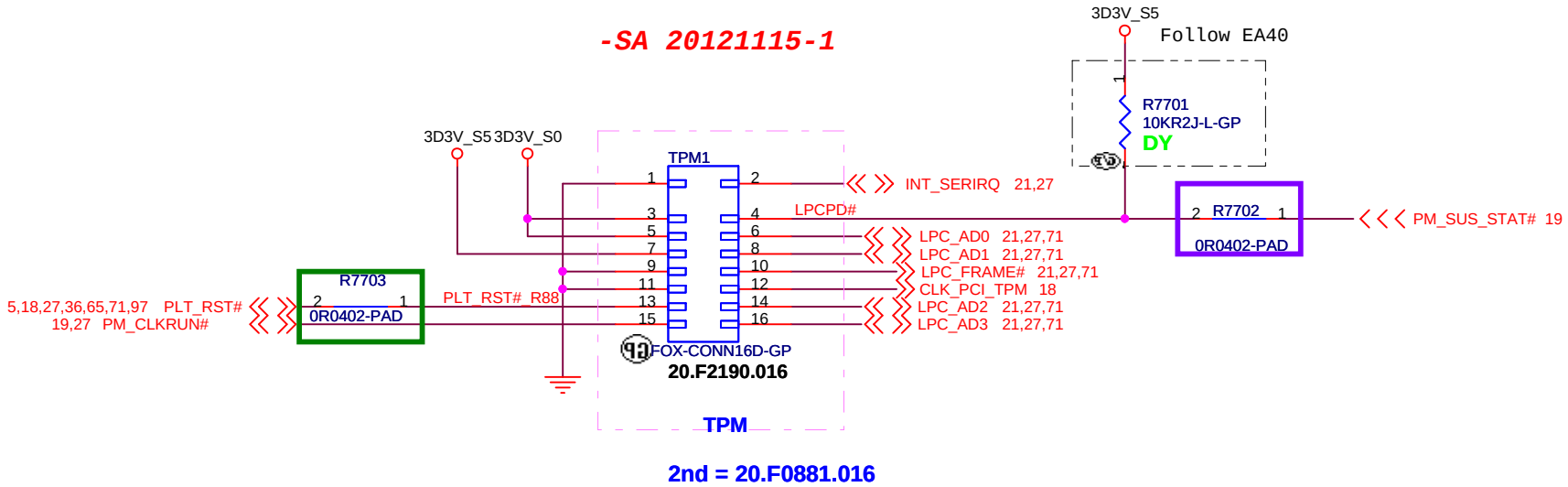
Title	***Reserved***	
Size A4	Document Number **Angel-CY**	Rev **1**
Date: Monday, April 22, 2013	Sheet 76 of 102	



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Title	Reserved	
Size A4	Document Number Angel-CY	Rev 1
Date: Monday, April 22, 2013	Sheet 77 of 102	

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Title	***Reserved***	
Size A4	Document Number **Angel-CY**	Rev **1**
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~~SSID - User Interface~~

Free Fall Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

Blanking

Note
1) Keep all signals are the same trace width. (included VDD, GND).
2) No VIA under IC bottom.

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<Variant Name>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title	Free Fall Sensor	
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Angel-SA

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Title

Reserved

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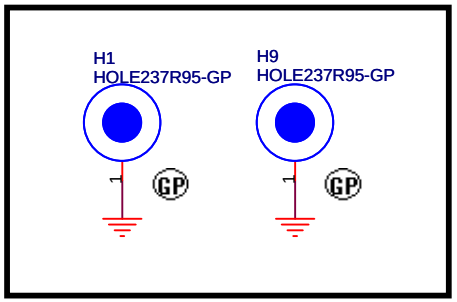

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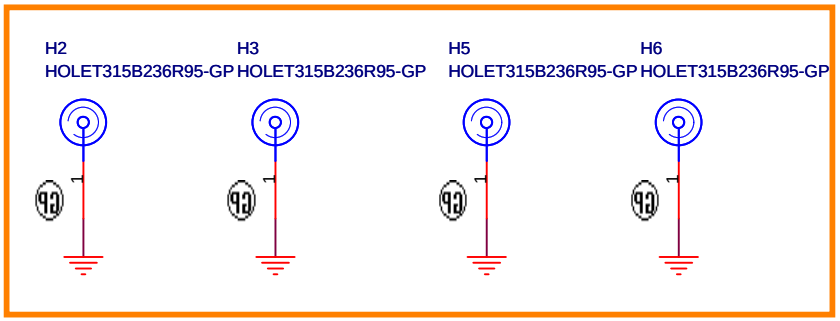

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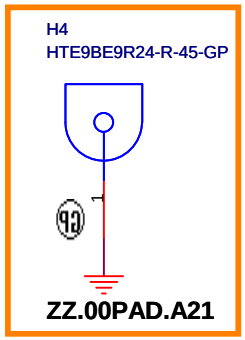

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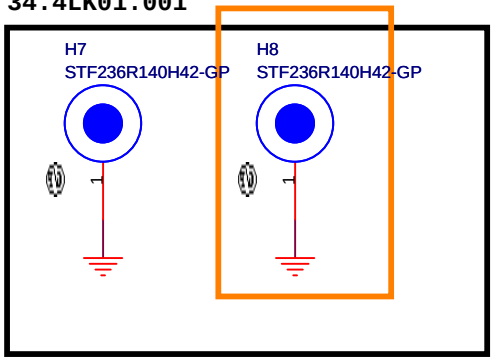

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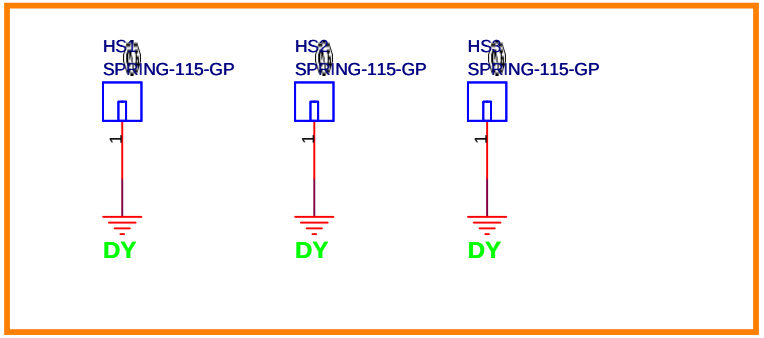

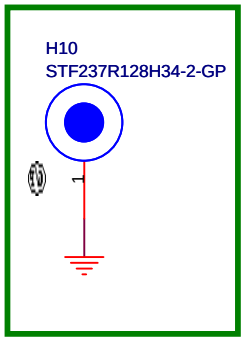

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Title: **Reserved**

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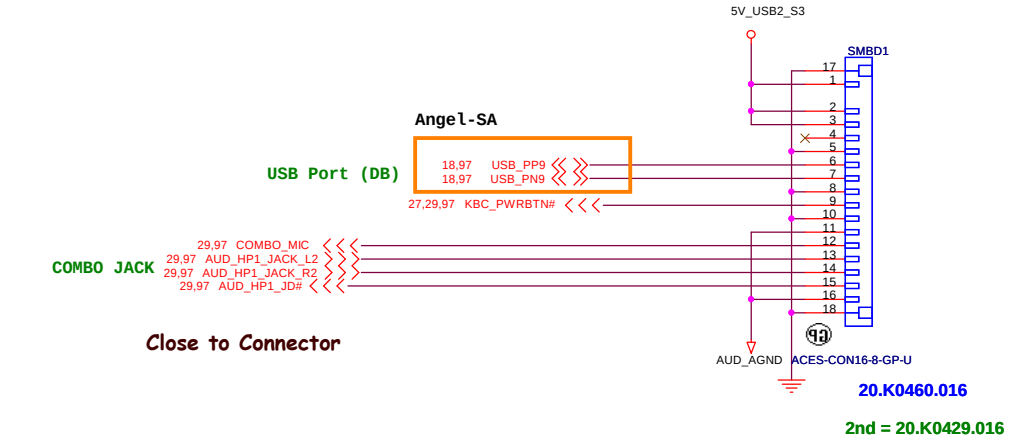

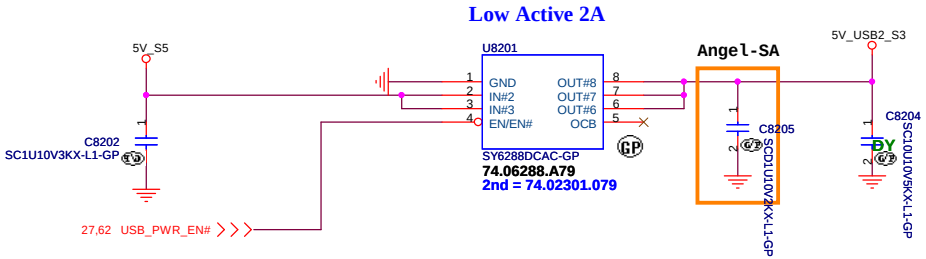

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Title: ***IO Board Connector***

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Title	GPU(PEG)	
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Title: GPU (DIGITALOUT)

Size	Document Number	Rev
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Title: ***GPU (VRAM I/F)***

Size	Document Number	Rev
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Title	GPU (GPIO/STRAP)	
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Title: ***GPU (POWER/GND)***

Size	Document Number	Rev
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Title
GPU-VRAM1,2 (1/4)

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Title
GPU-VRAM3,4 (2/4)

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Title

GPU-VRAM5,6 (3/4)

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Title	GPU-VRAM7,8 (4/4)	
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Title: RT8812A VGA CORE

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Title

DISCRETE VGA POWER

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Title	LVDS_Switch	
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Title	CRT_Switch	
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SSID = SDIO

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Title	TOUCH PANEL	
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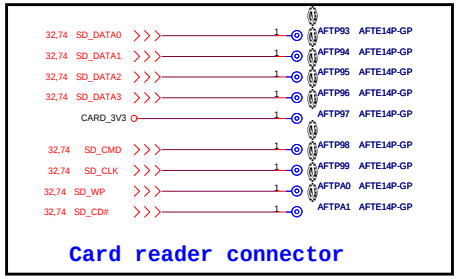

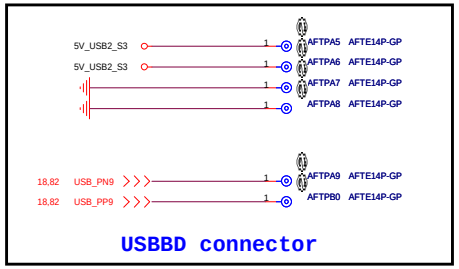

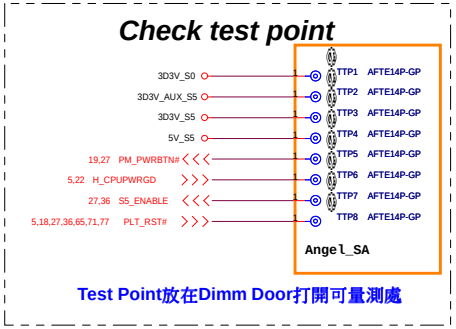

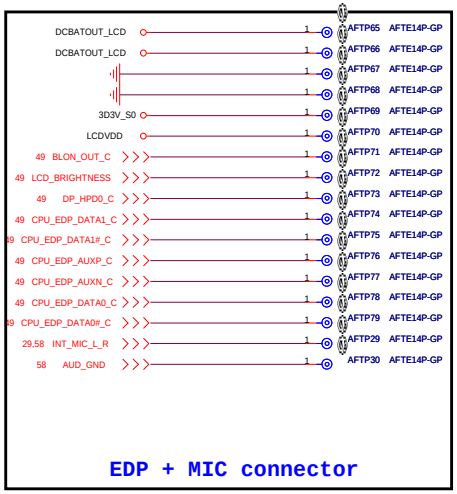

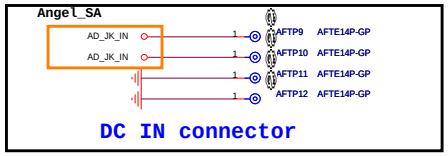

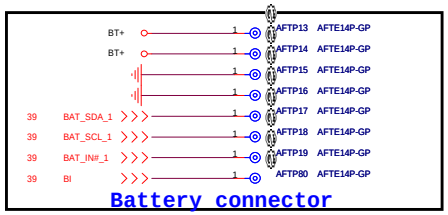

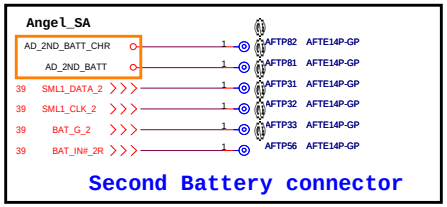

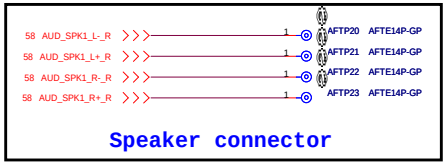

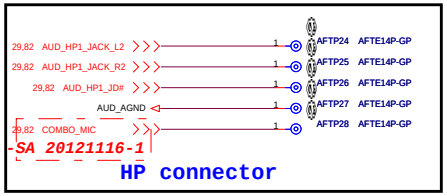

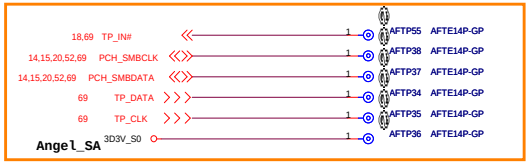

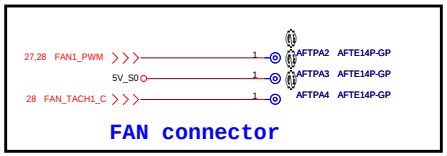

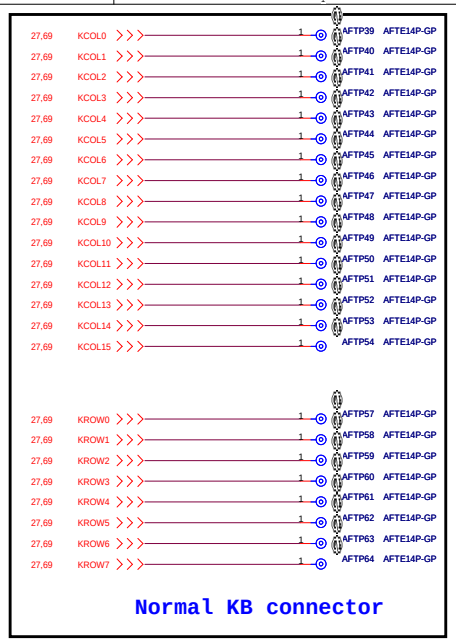

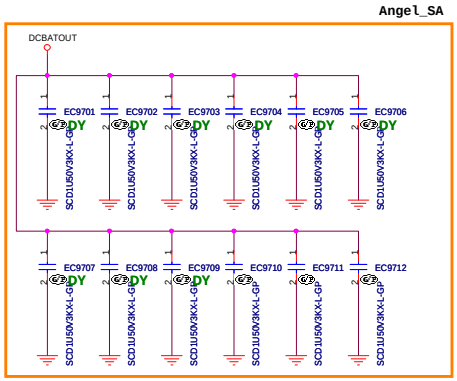

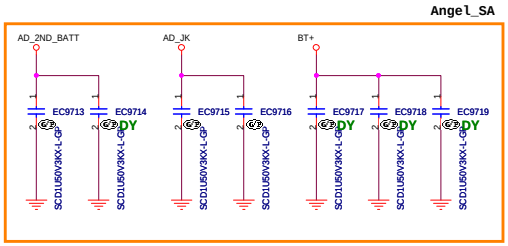

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Title: UNUSED PARTS/EMI Capacitors

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Title

Change History

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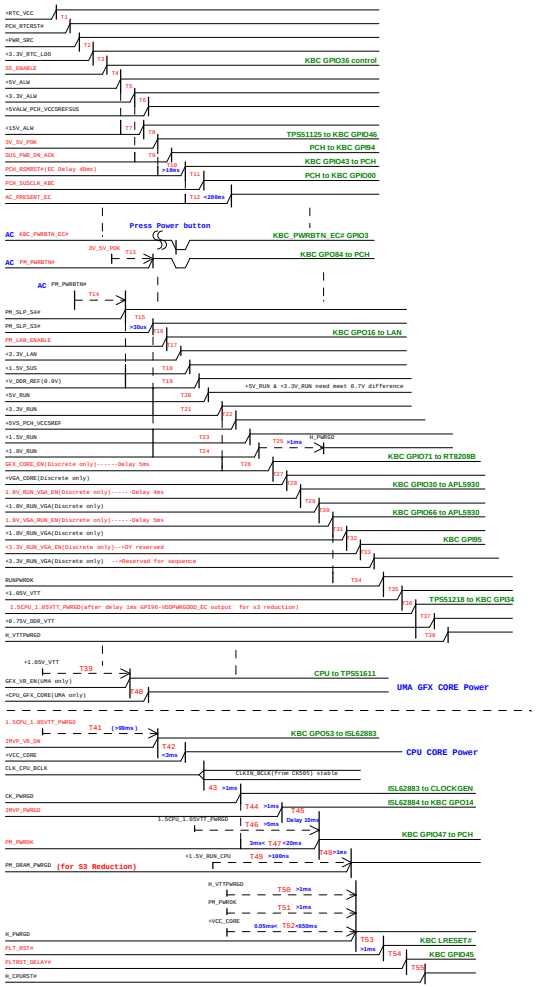
Intel-Power Up Sequence

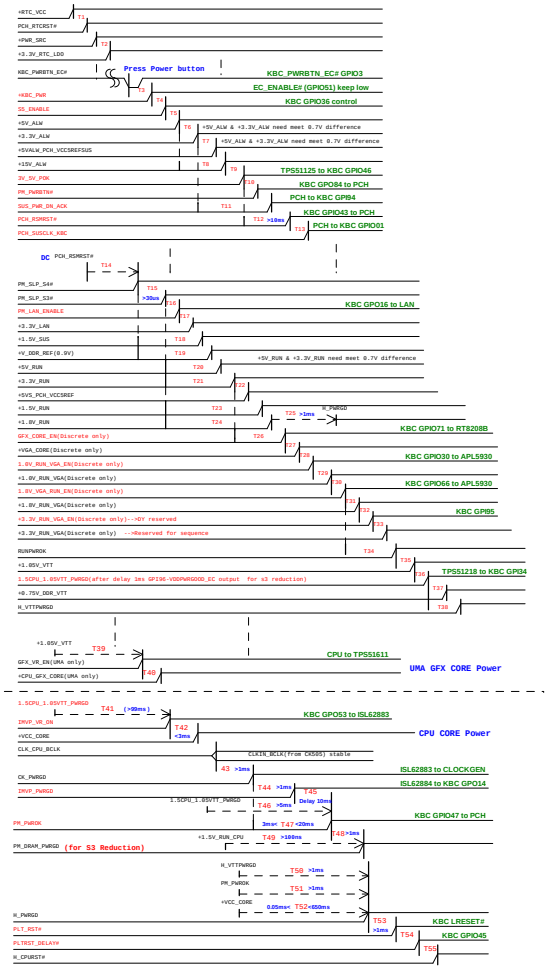
(AC mode)

red word: KBC GPIO

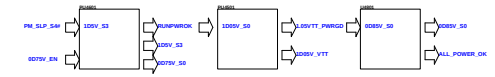


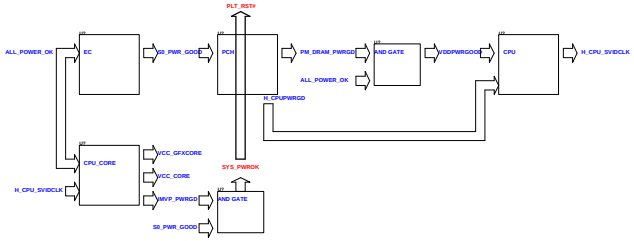
(DC mode)

red word: KBC GPIO



Power Sequence





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Power Sequence
Ansel-CY
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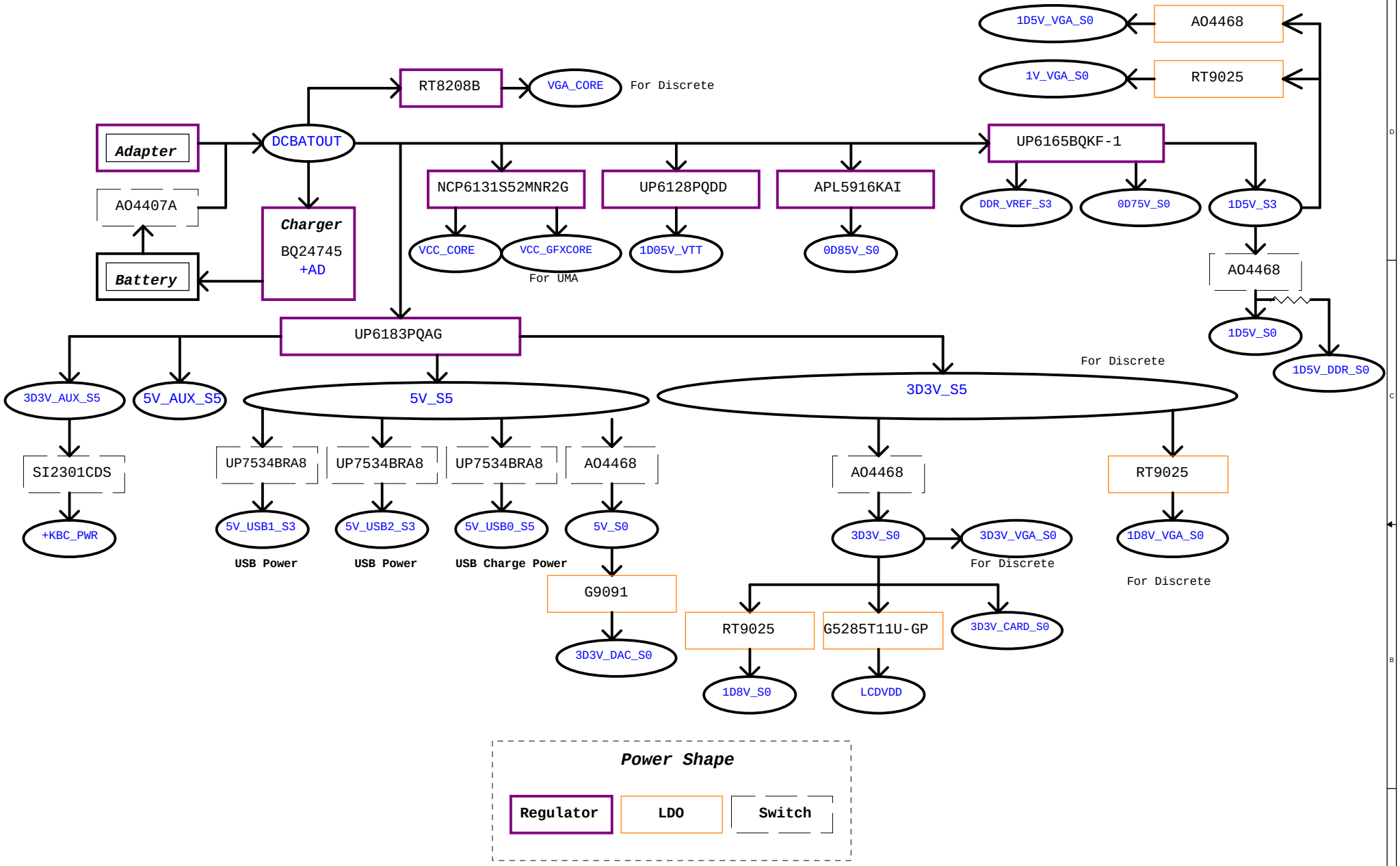

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Title: ***Power Block Diagram***

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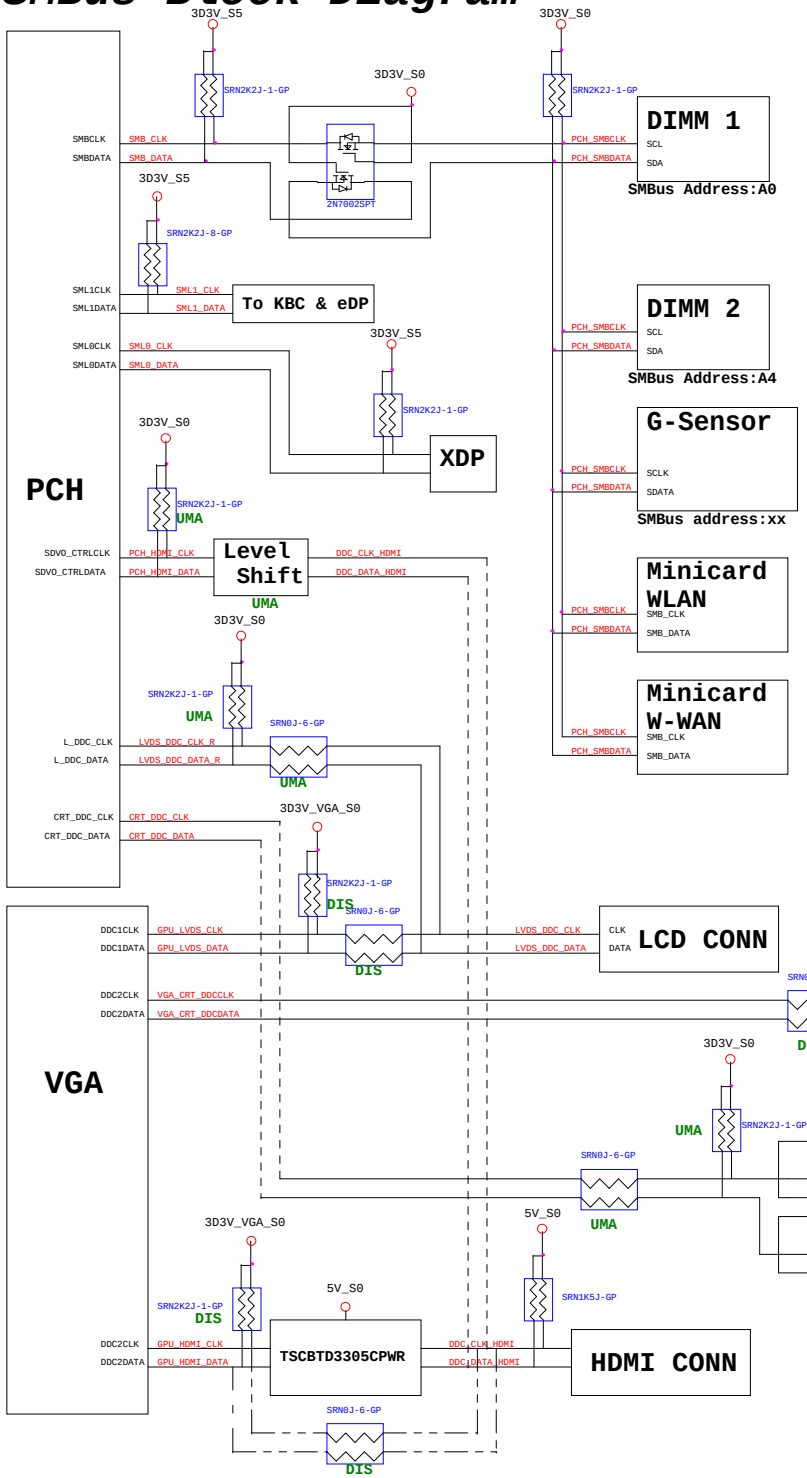
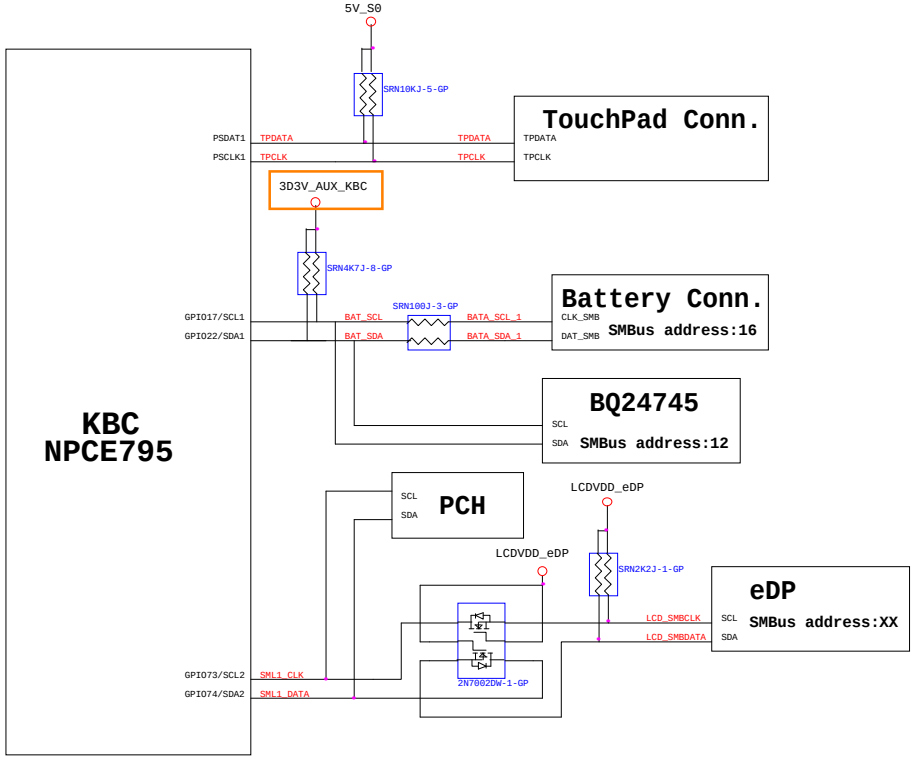
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS Block Diagram

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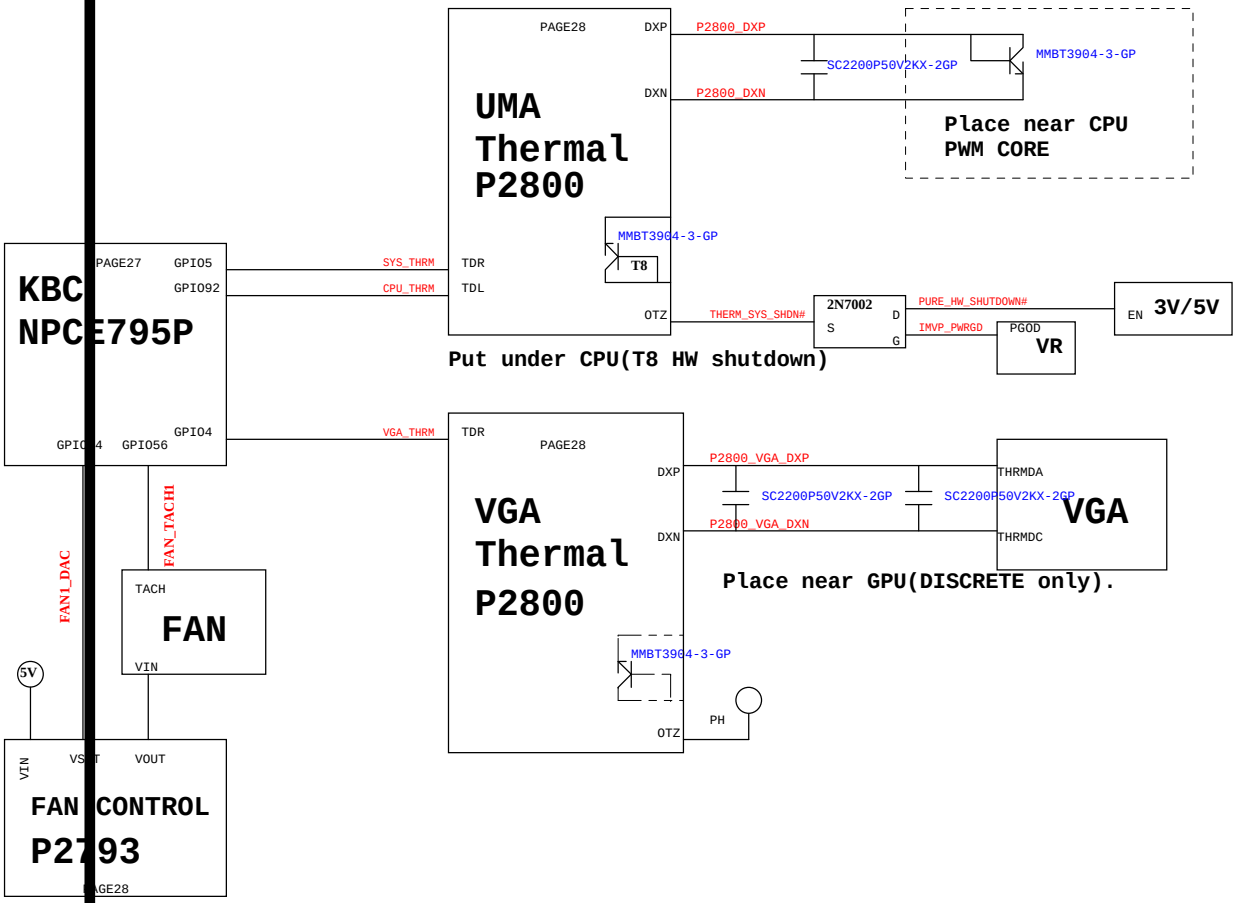
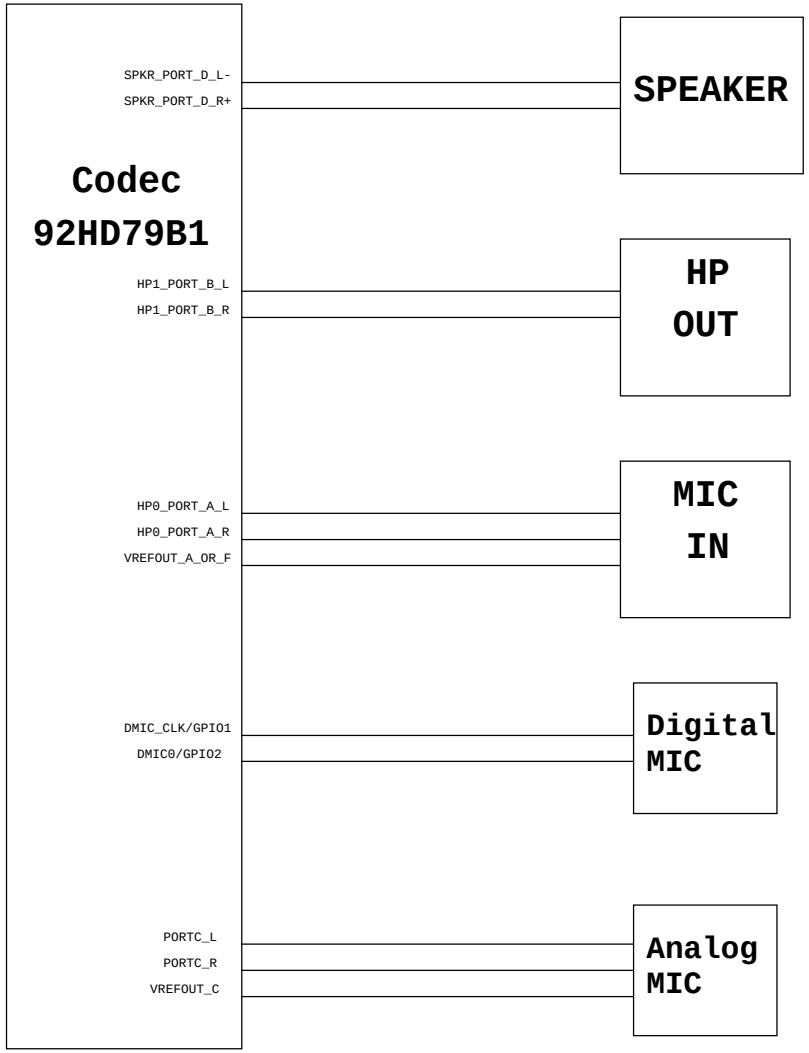
Thermal Block Diagram



Audio Block Diagram



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Title	Thermal/Audio Block Diagram	
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