

Arsenal DJ1 Discrete Schematics Document

Arrandale

Intel PCH

2010-05-03

REV : A01

DY : Nopop Component

PARK : Pop when schematic is PARK-LP Component

M92 : Pop when schematic is M92-LP Component

DISCRETE PARK



Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
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Title

Cover Page

Size
A3

Document Number

Arsenal DJ1 Discrete

Rev

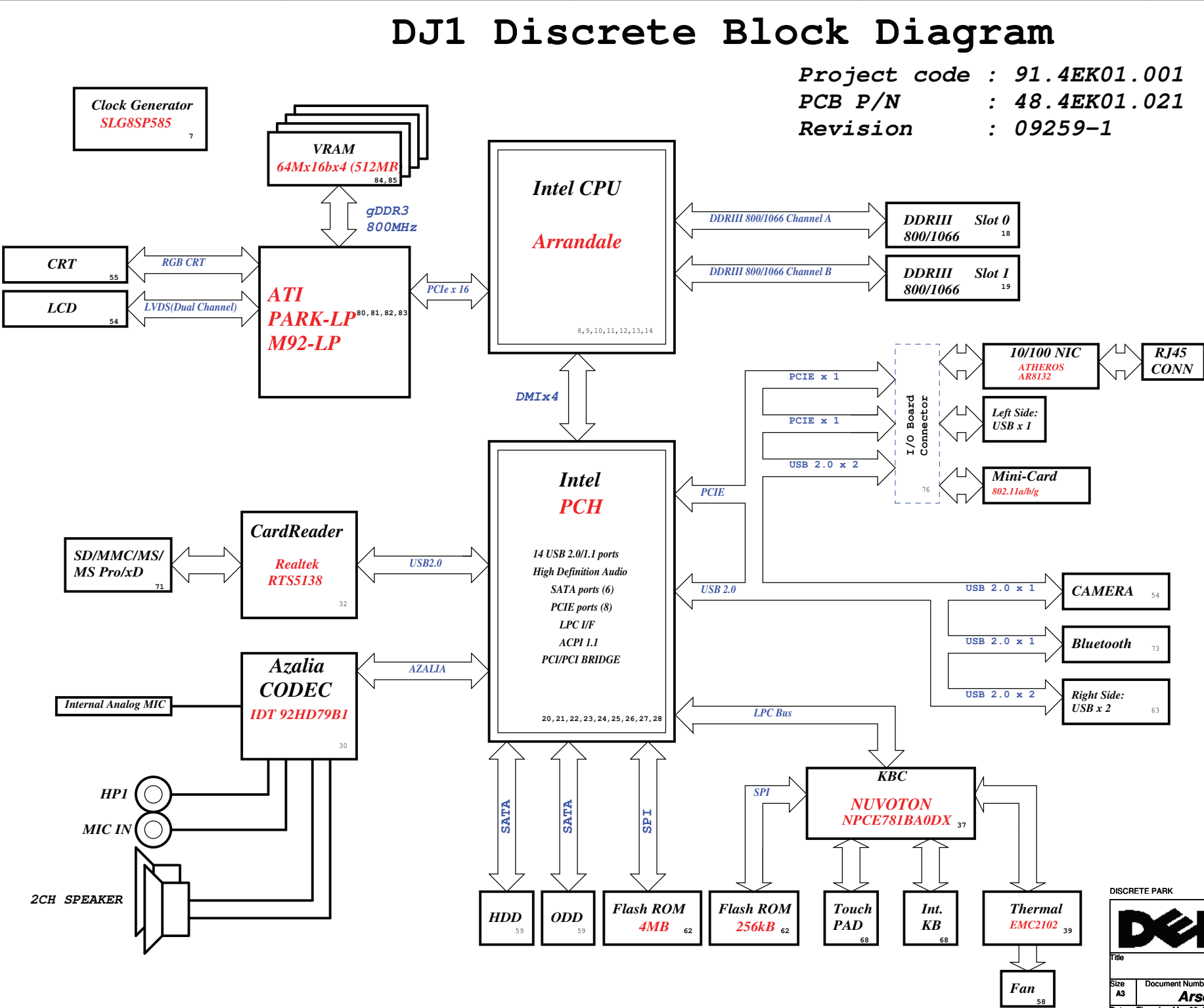
A01

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DJ1 Discrete Block Diagram

Project code : 91.4EK01.001
PCB P/N : 48.4EK01.021
Revision : 09259-1



CPU DC/DC	
ISL62882 47,48	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE
SYSTEM DC/DC	
TPS51218 49	
INPUTS	OUTPUTS
+PWR_SRC	+1.05V_VTT
SYSTEM DC/DC	
RT8205BGQW 46	
INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW2 +3.3V_RTC_LDO +5V_ALW +3.3V_ALW +15V_ALW
SYSTEM DC/DC	
RT8207GQW 50	
INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS +0.75V_DDR_VTT +V_DDR_REF
SYSTEM DC/DC	
APL5930KAI 88	
INPUTS	OUTPUTS
+1.5V_SUS	+1.1V_RUN
VGA	
RT8208BGQW 86	
INPUTS	OUTPUTS
+PWR_SRC	+VCC GFX_CORE
MAXIM CHARGER	
BQ24745	
INPUTS	OUTPUTS
+DC_IN +PBATT	+PWR_SRC
SYSTEM DC/DC	
APL5930 51	
INPUTS	OUTPUTS
+3.3V_ALW	+1.8V_RUN +1.8V_DELAY
SYSTEM DC/DC	
Switches 42	
INPUTS	OUTPUTS
+1.5V_SUS +5V_ALW +3.3V_ALW	+1.5V_RUN +5V_RUN +3.3V_RUN
PCB LAYER	
L1: Top	
L2: VCC	
L3: Signal	
L4: Signal	
L5: GND	
L6: Bottom	

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Block Diagram

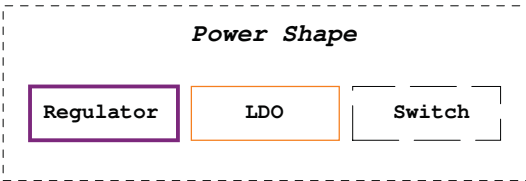
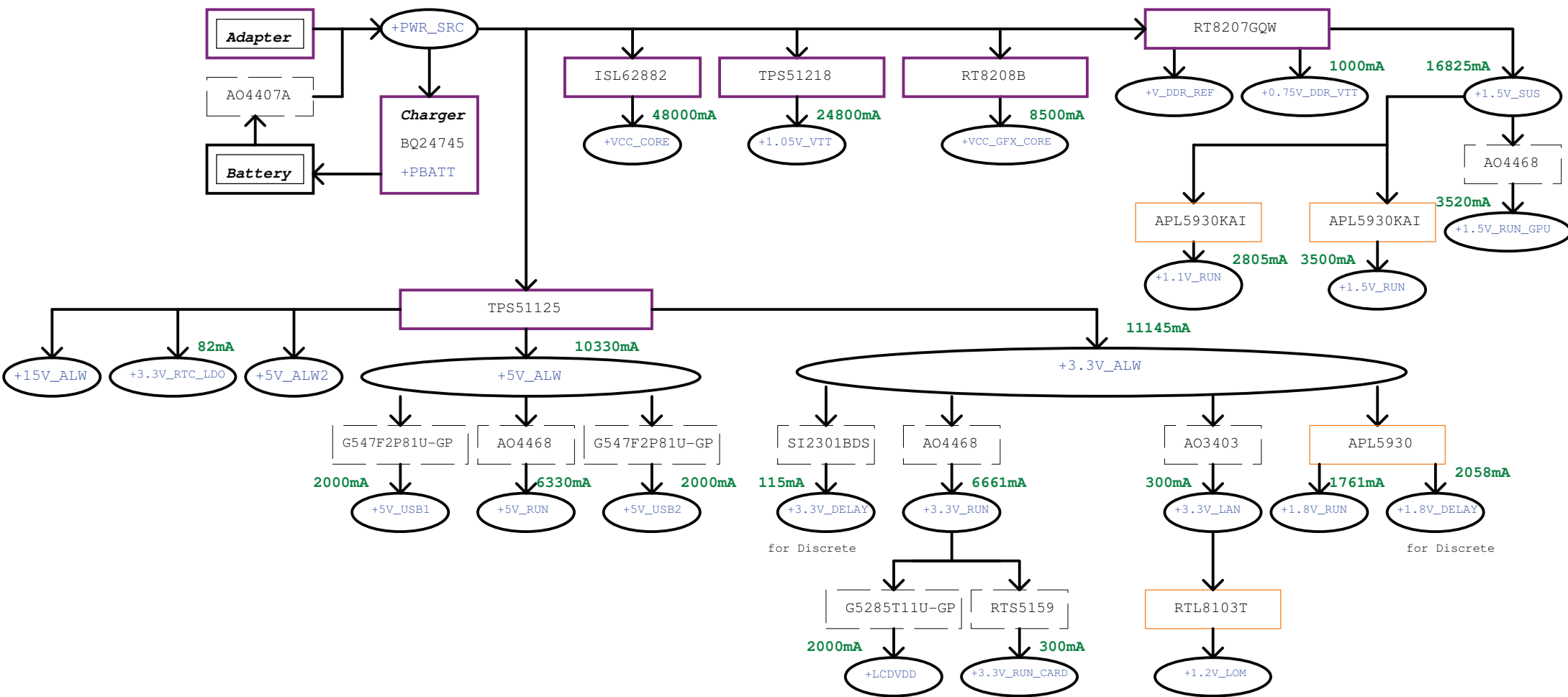
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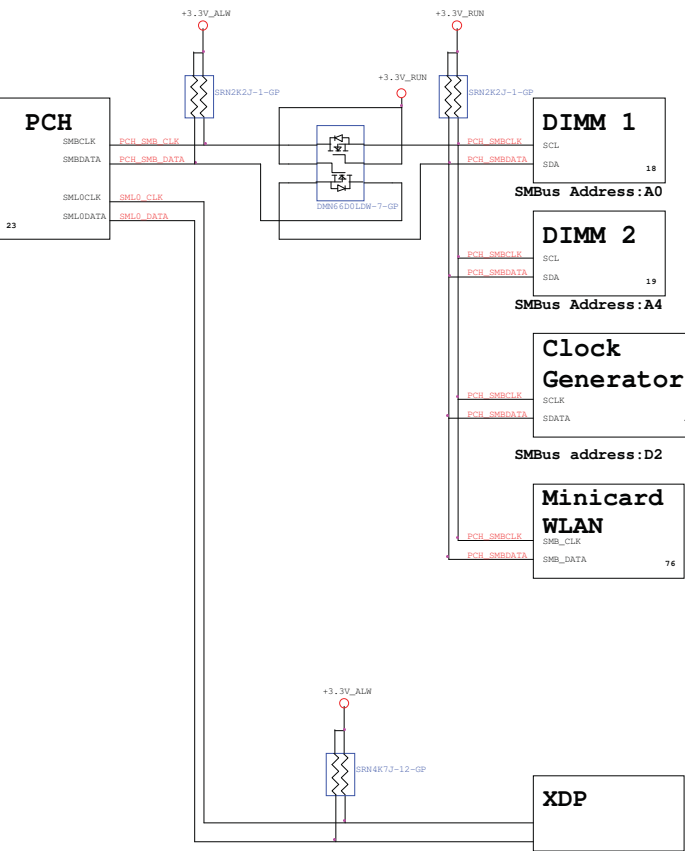
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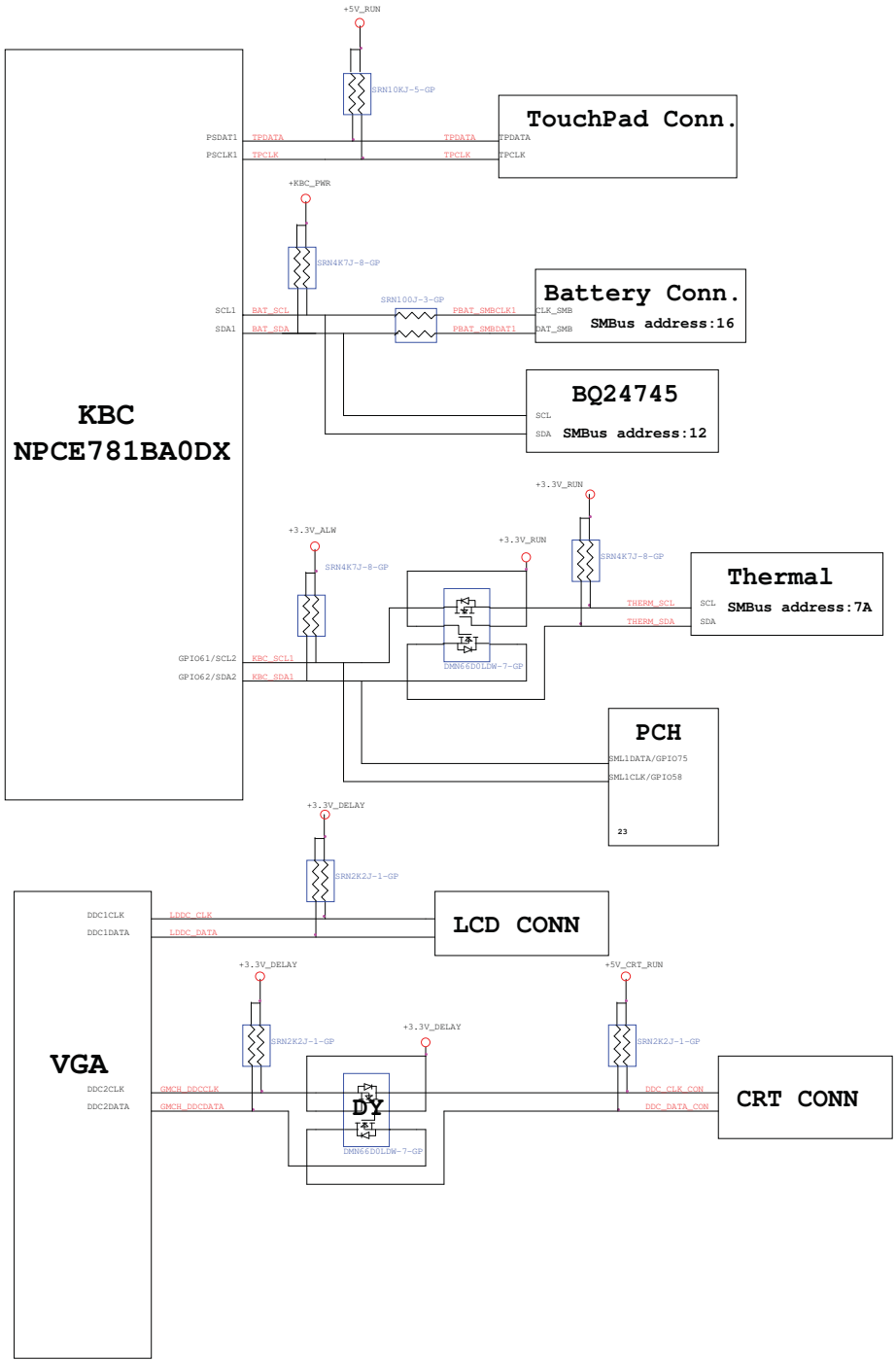
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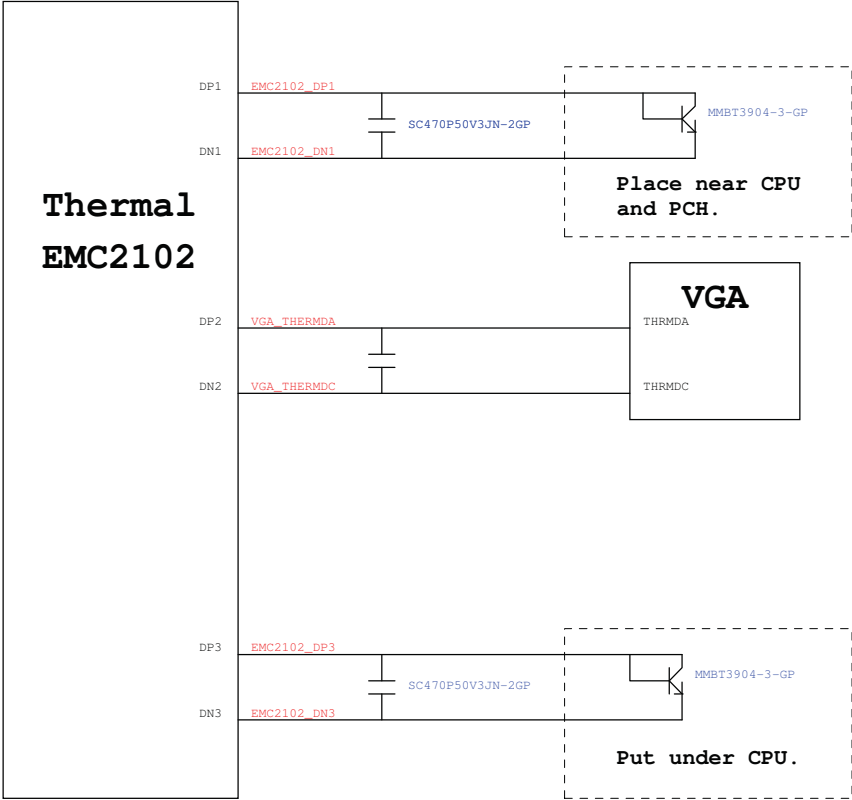
PCH SMBus Block Diagram



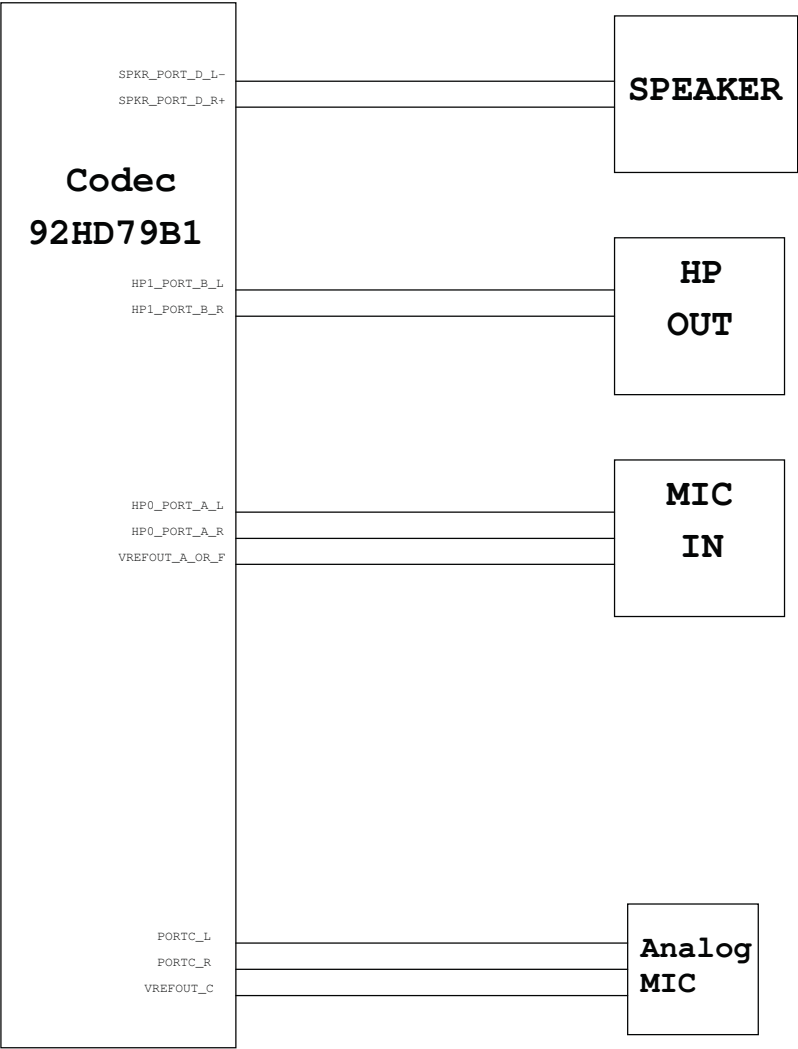
KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



PCH Strapping

Calpella Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/GPIO55	Default Mode: Internal pull-up. Low (0) = Top Block Swap Mode (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	High (1) = Integrated VRM is enabled Low (0) = Integrated VRM is disabled
GNT0#, GNT1#/GPIO51	Default (SPI): Left both GNT0# and GNT1# floating. No pull up required. Boot from PCI: Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/GPIO53	Default - Internal pull-up. Low (0)= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	Default: Do not pull low. Disable ME in Manufacturing Mode: Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable iTPM: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Danbury: Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN#/GPIO[33]	Low (0): Flash Descriptor Security will be overridden. High (1) : Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

PCIE Routing

LANE2	MiniCard WLAN
LANE3	LAN

USB Table

USB	
Pair	Device
0	USB0 (I/O Board)
1	X
2	USB2
3	USB3
4	X
5	WLAN (I/O Board)
6	X
7	X
8	X
9	BLUETOOTH
10	CARD READER
11	CAMERA
12	X
13	X

Processor Strapping

Calpella Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1
CFG[7]	Reserved - Temporarily used for early Clarksfield samples.	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor Note: Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

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Title

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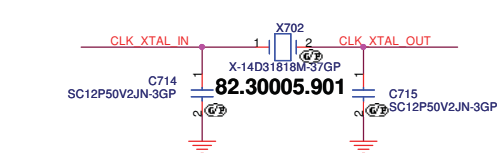
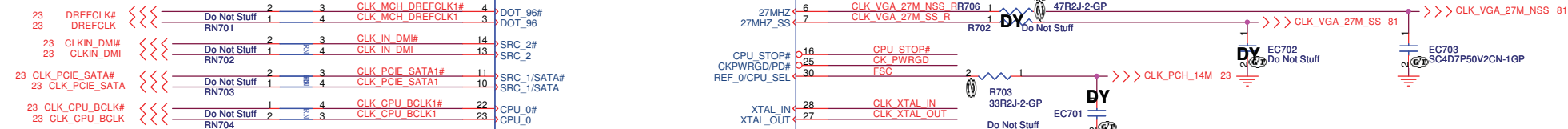
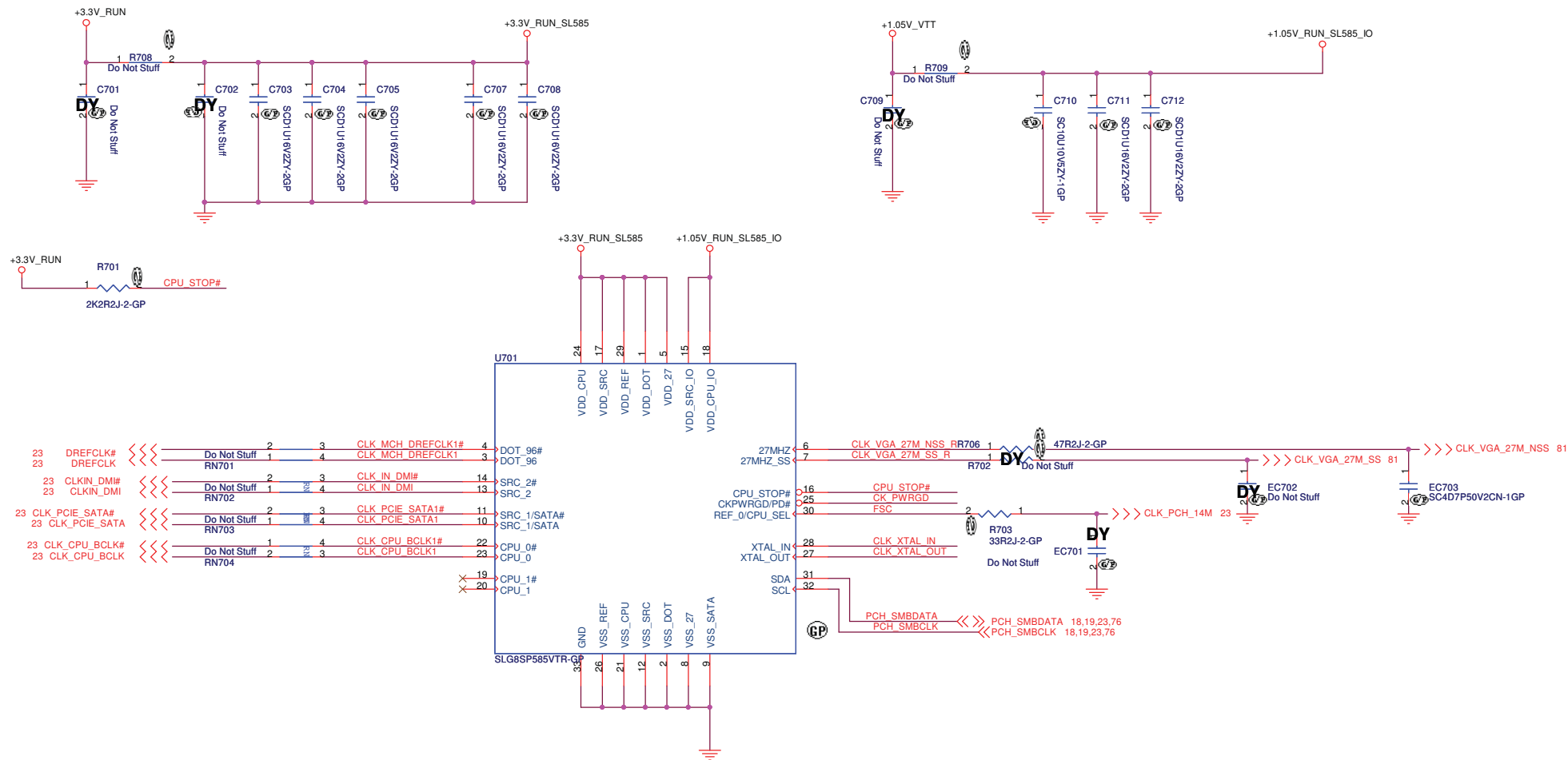
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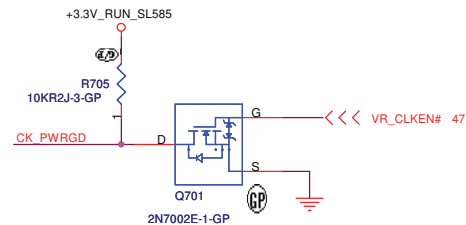
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SSID = CLOCK



FSC	0	1
SPEED	133MHz (Default)	100MHz



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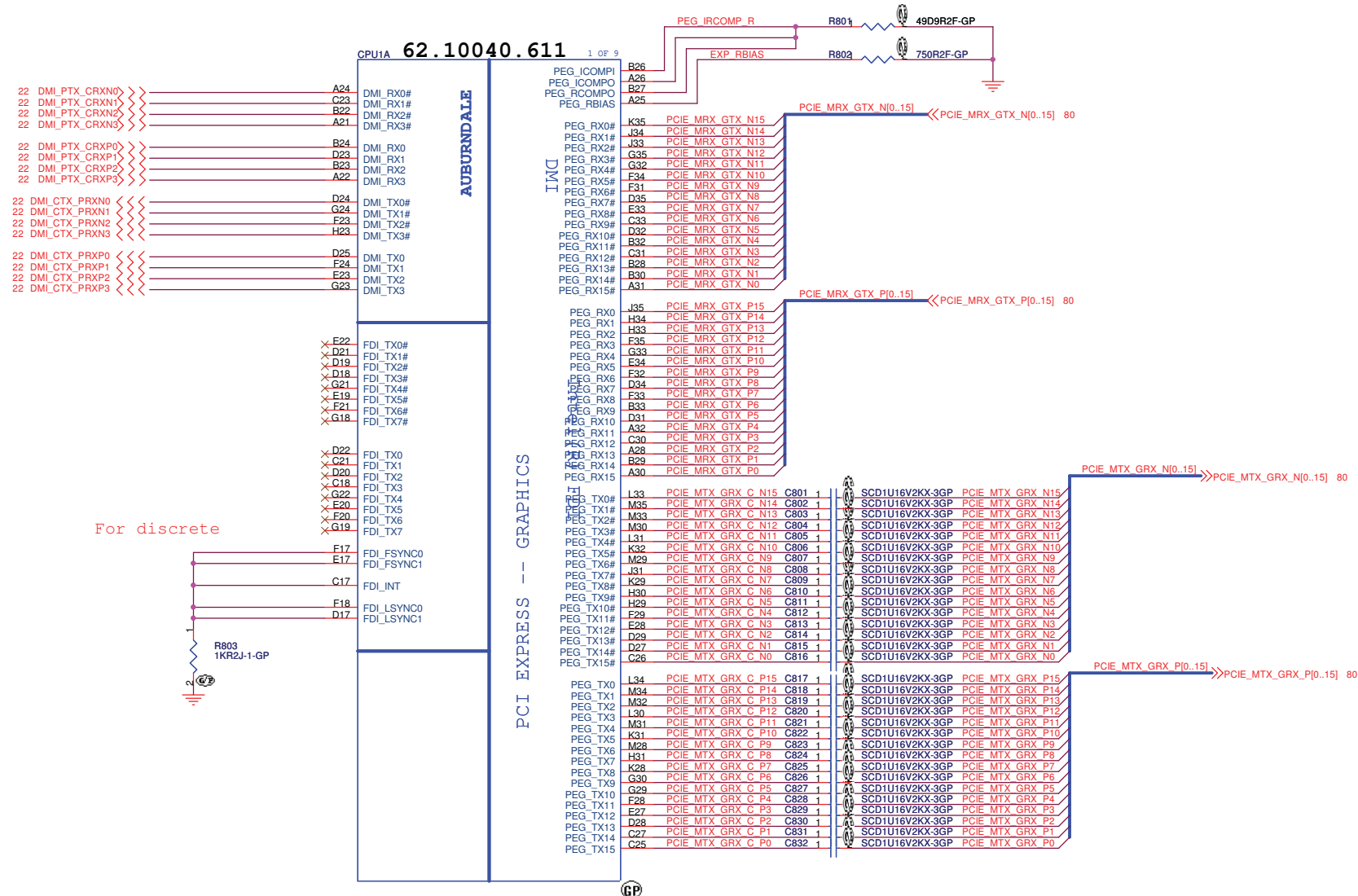
CPU (PCIe/DMI/FDI)

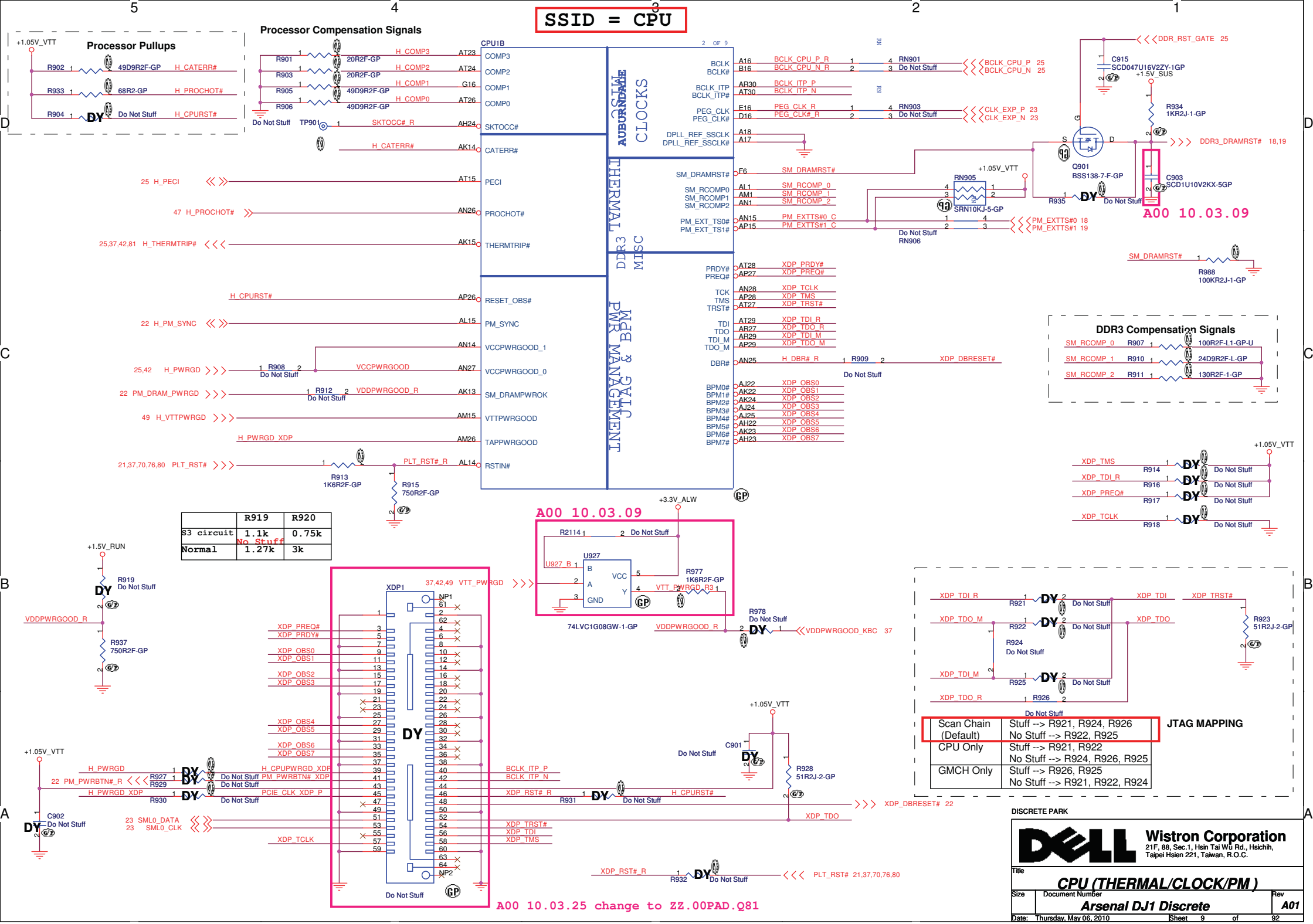
Arsenal DJ1 Discrete

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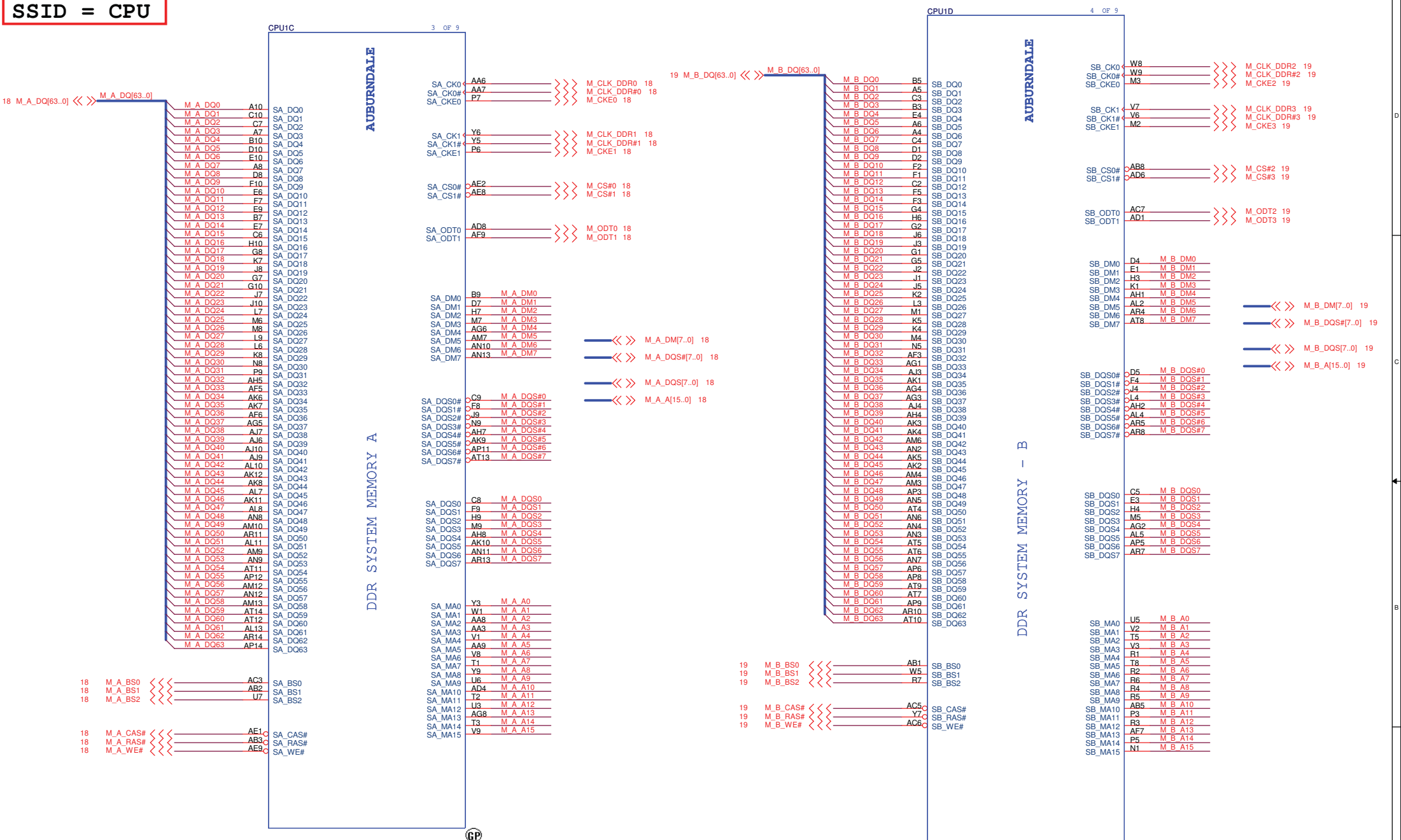
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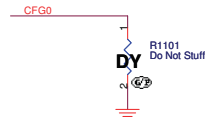




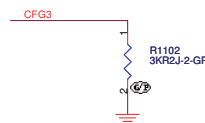
SSID = CPU



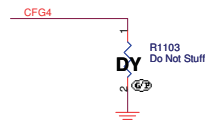
SSID = CPU



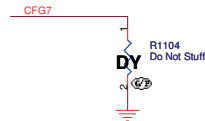
PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled



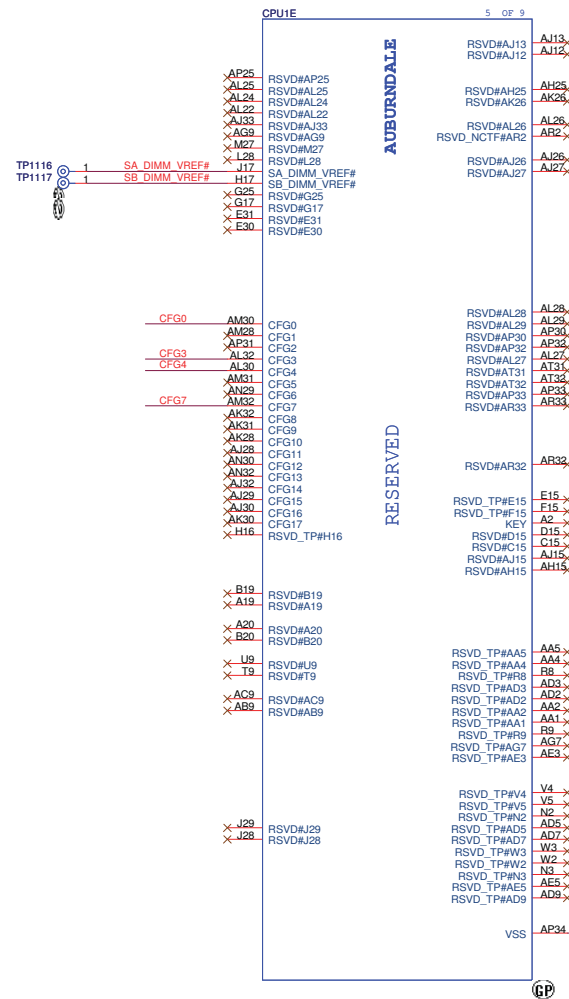
CFG3 - PCI-Express Static Lane Reversal	
CFG3	1:Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...



CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port



CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.



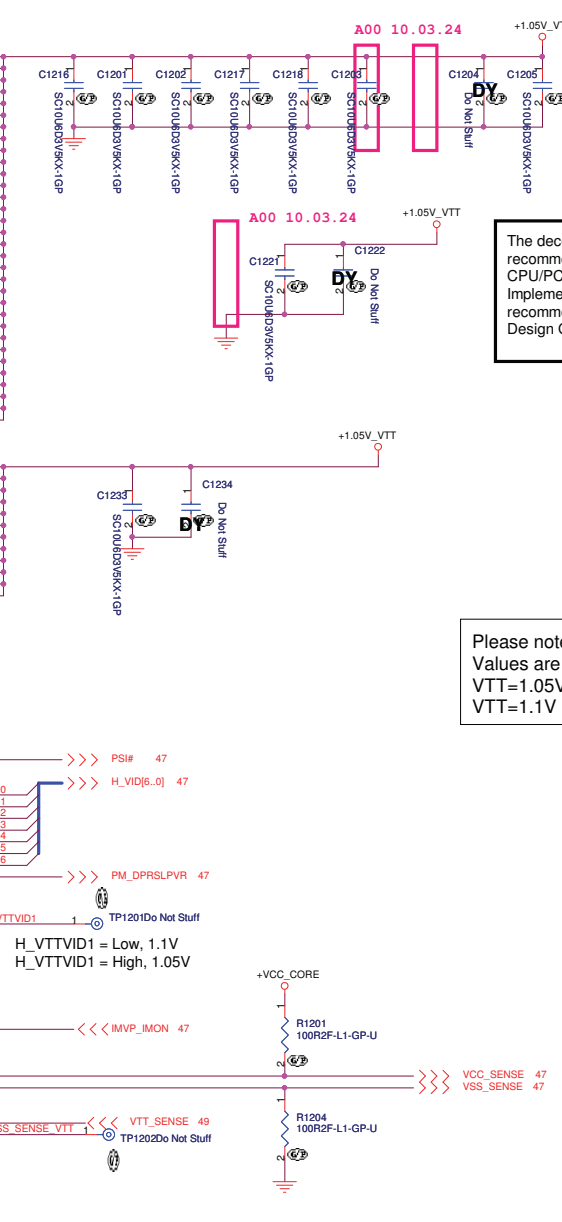
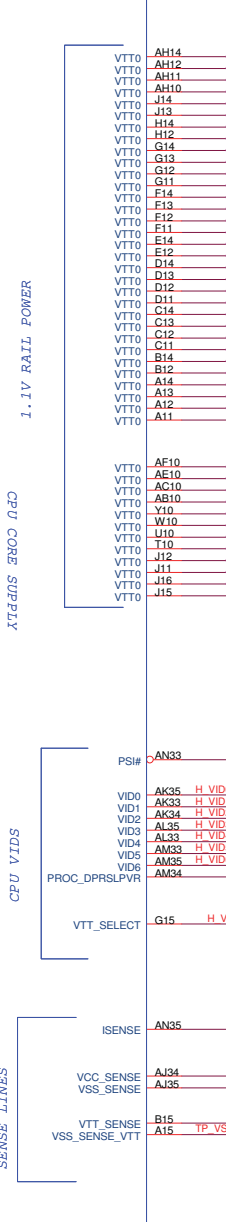
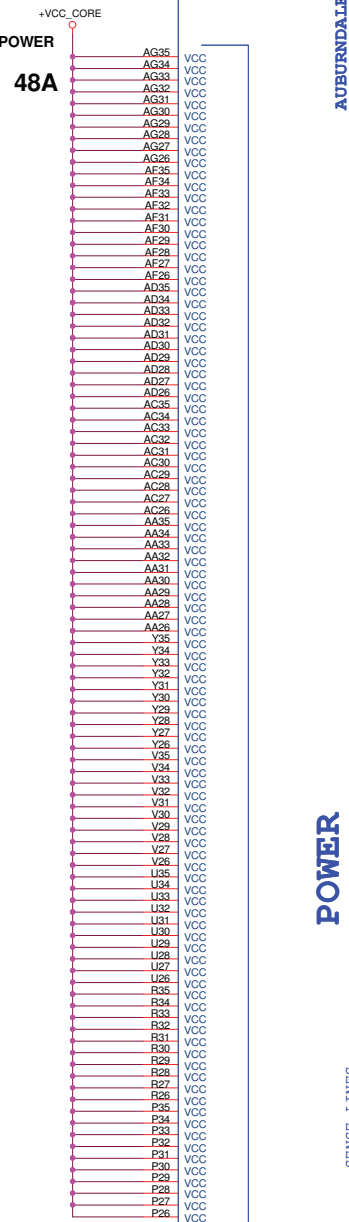
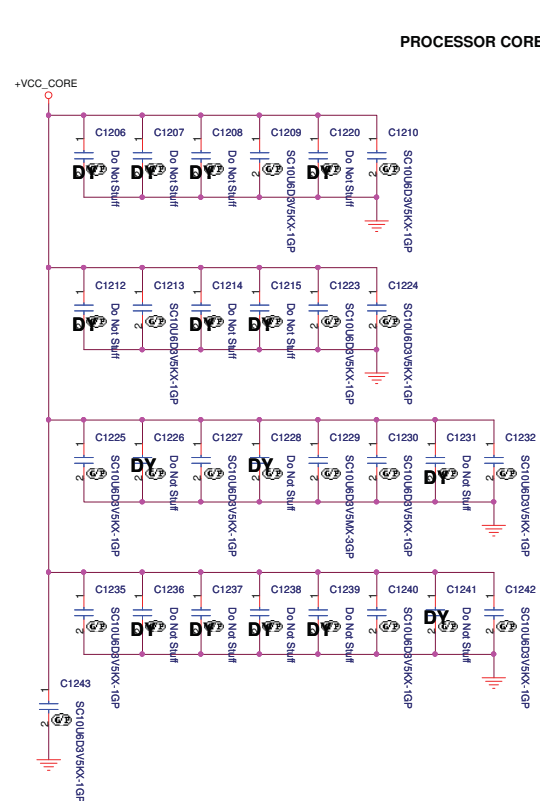
VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.

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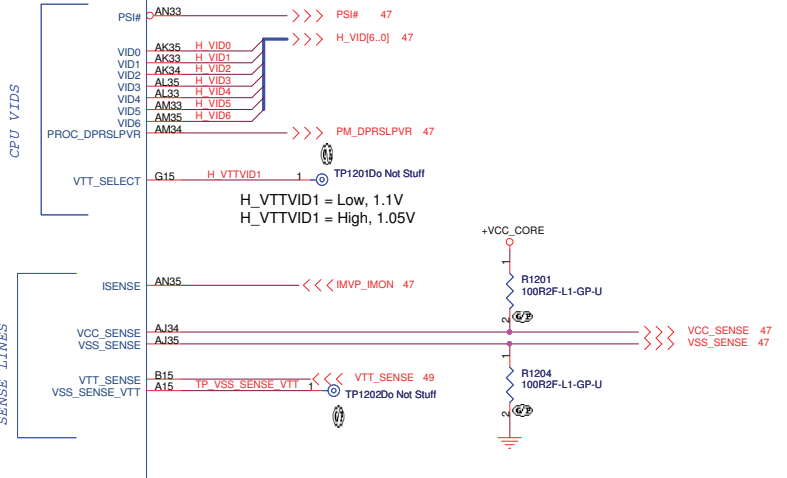
Title		
CPU (RESERVED)		
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SSID = CPU



The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that the VTT Rail Values are Auburndale
VTT=1.05V; Clarkfield
VTT=1.1V

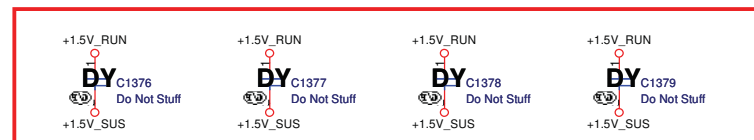
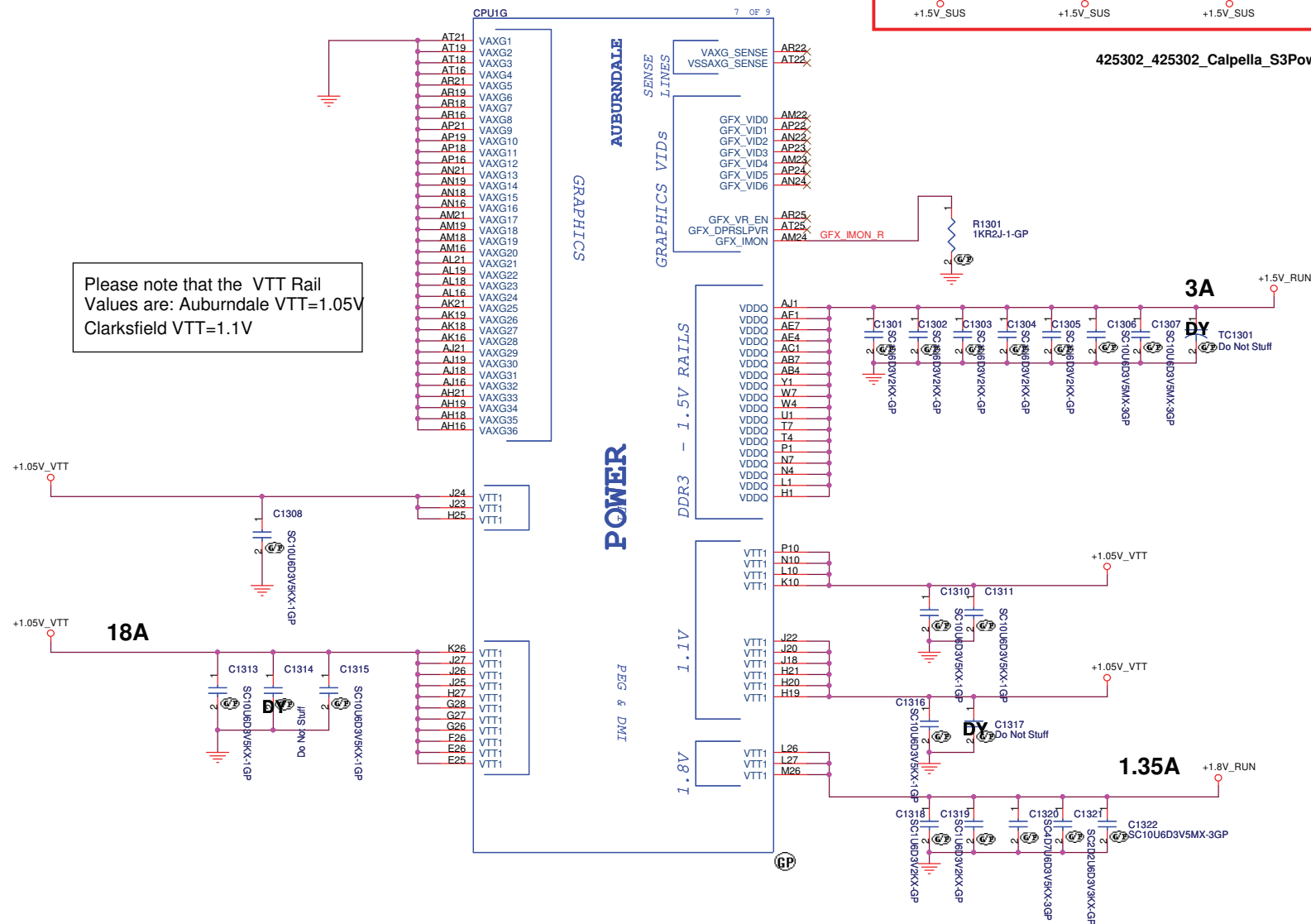


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Title		CPU (VCC_CORE)	
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SSID = CPU



425302_425302_Calpella_S3PowerReduction_WhitePape
Revision 0.7



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Title

CPU (VCC GFXCORE)

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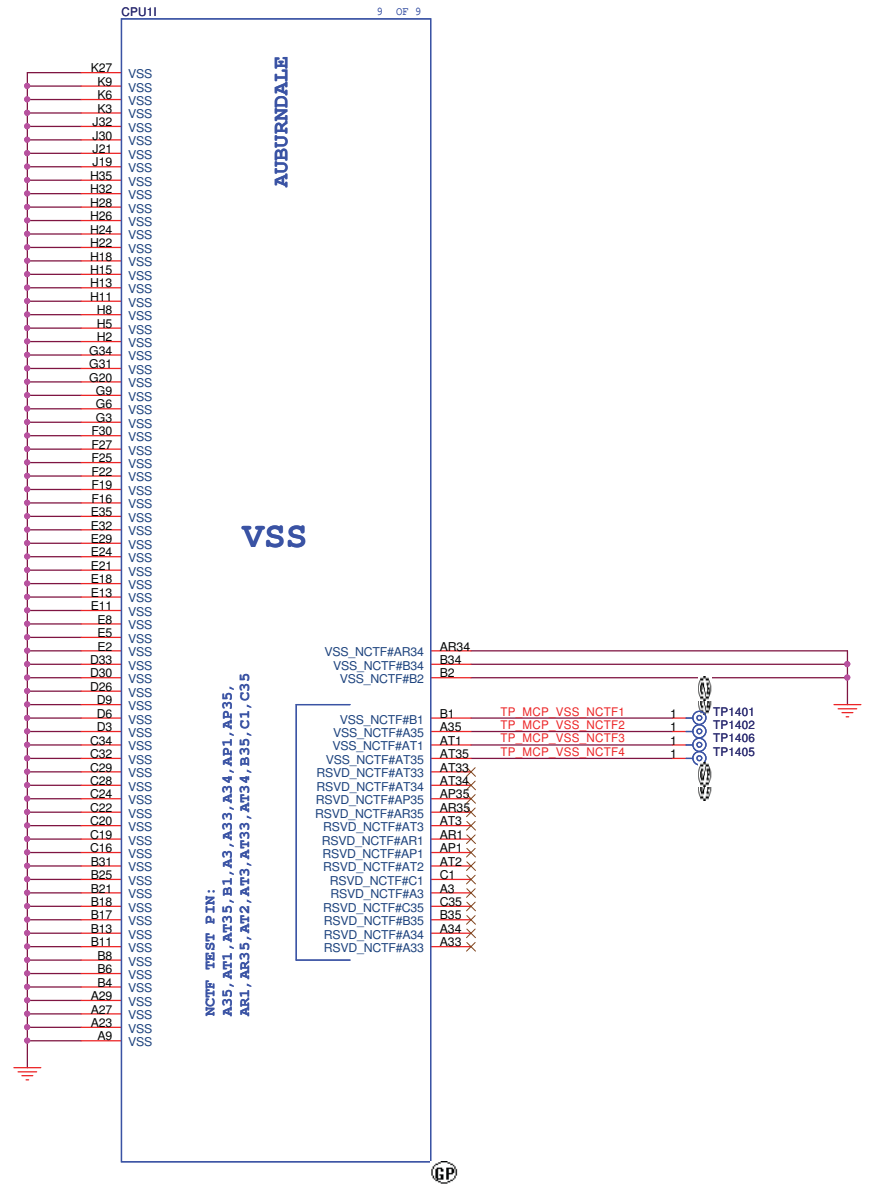
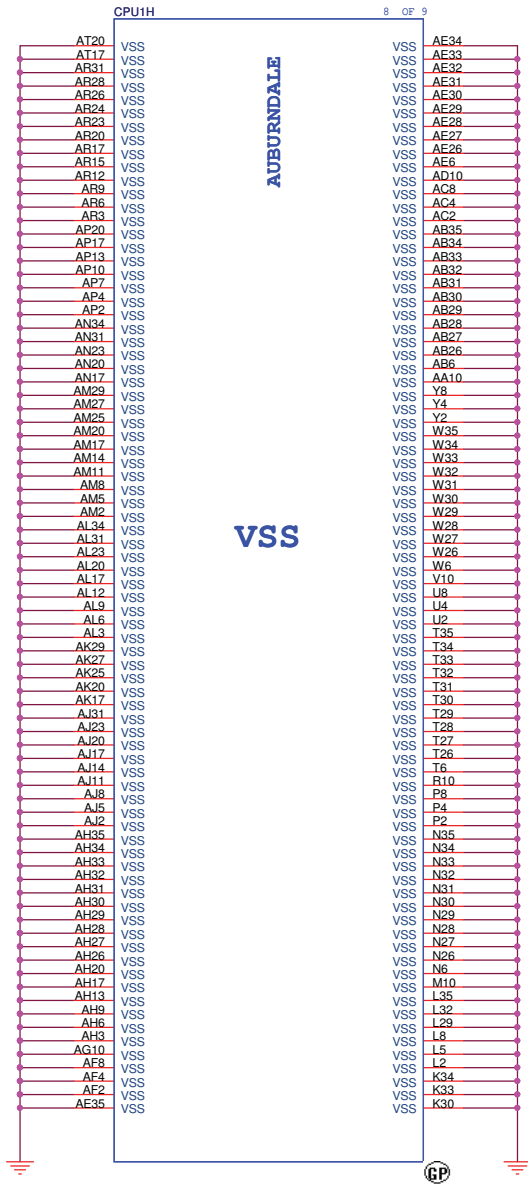
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SSID = CPU



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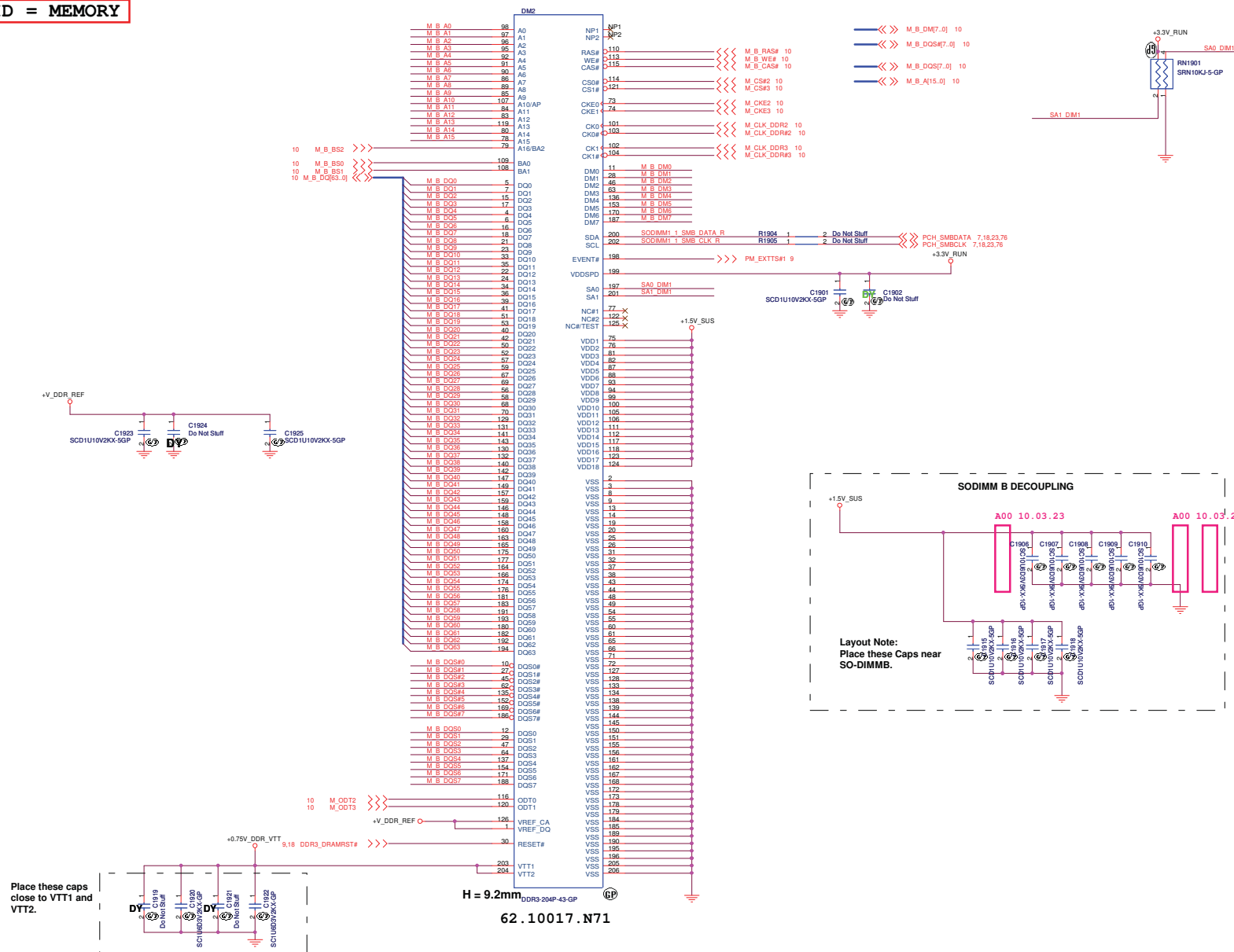
DELL Wistron Corporation
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Title
CPU (VSS)

Size Document Number Rev
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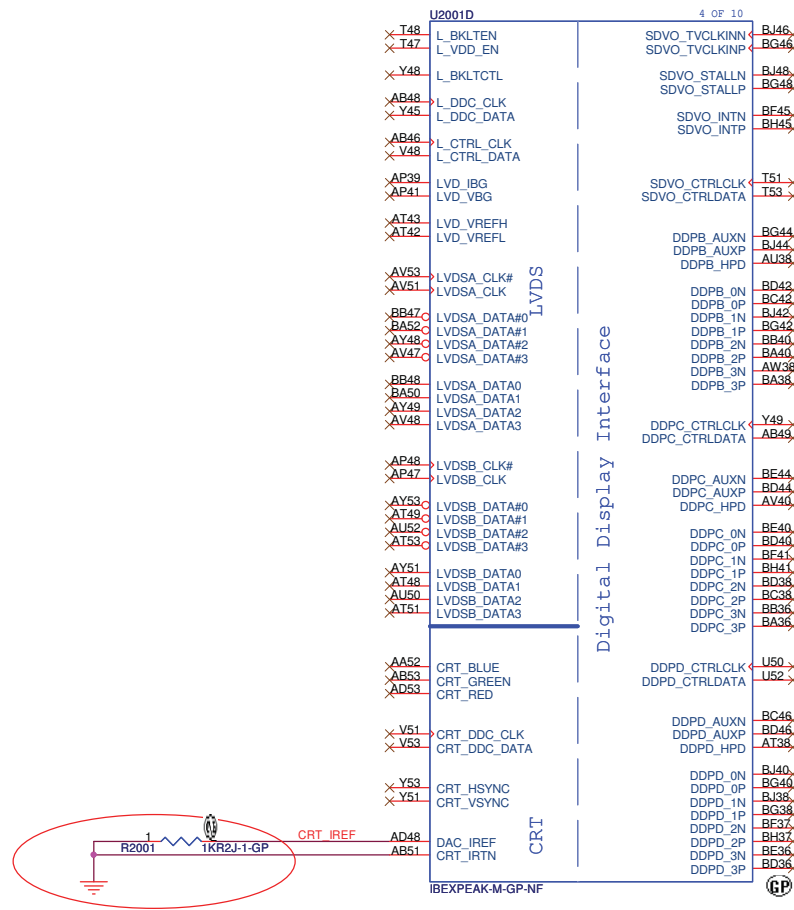
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SSID = MEMORY



Note: SO-DIMMB SPD Address is 0xA4 SO-DIMMB TS Address is 0x34	SO-DIMMB is placed farther from the Processor than SO-DIMMA
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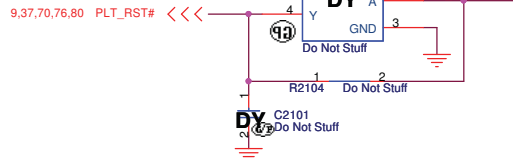
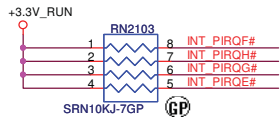
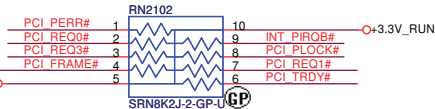
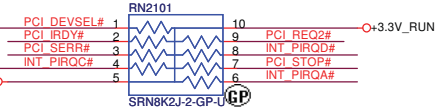
SSID = PCH



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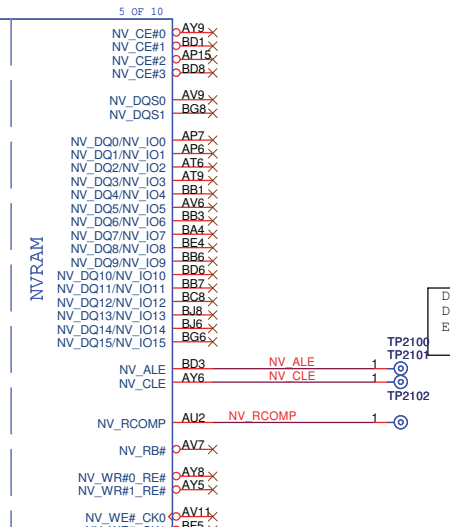
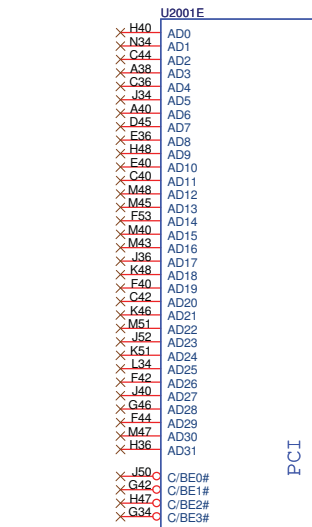
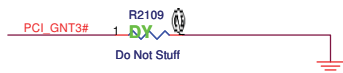
DELL			Wistron Corporation		
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SSID = PCH



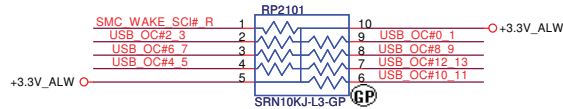
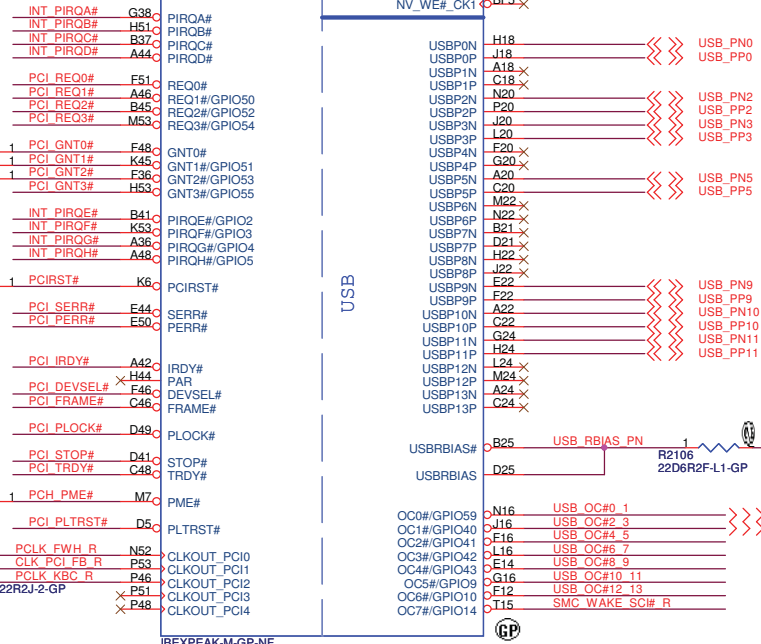
BOOT BIOS Strap		
PCI_GNT#1	PCI_GNT#0	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI (Default)

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default



Danbury Technology:
Disabled when Low.
Enable when High.

USB	
Pair	Device
0	USB0 (I/O Board)
1	X
2	USB2
3	USB3
4	X
5	WLAN (I/O Board)
6	X
7	X
8	X
9	BLUETOOTH
10	CARD READER
11	CAMERA
12	X
13	X

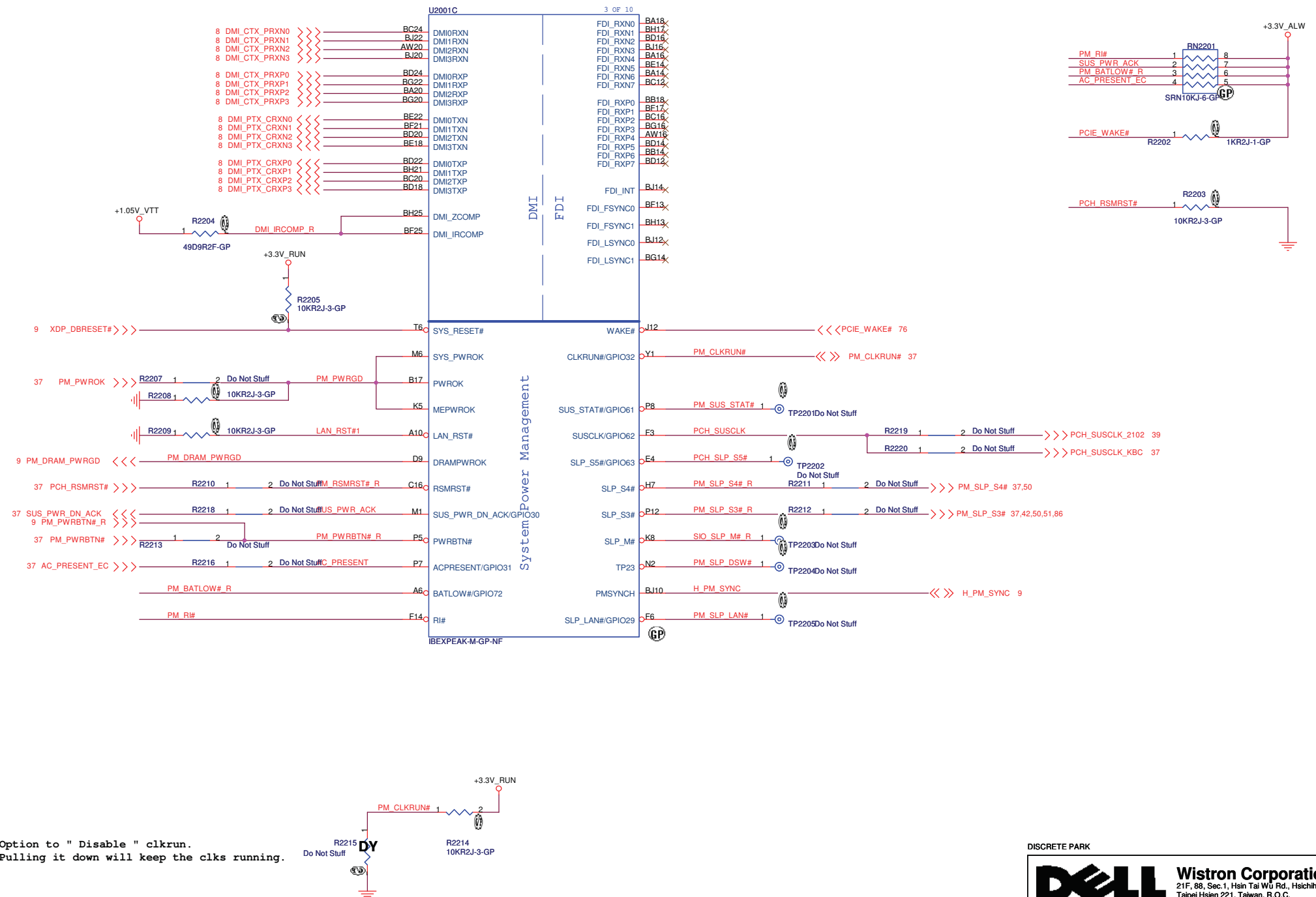


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Title		PCH (PCI/USB/NVRAM)	
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Title

PCH (DM I/FDI/PM)

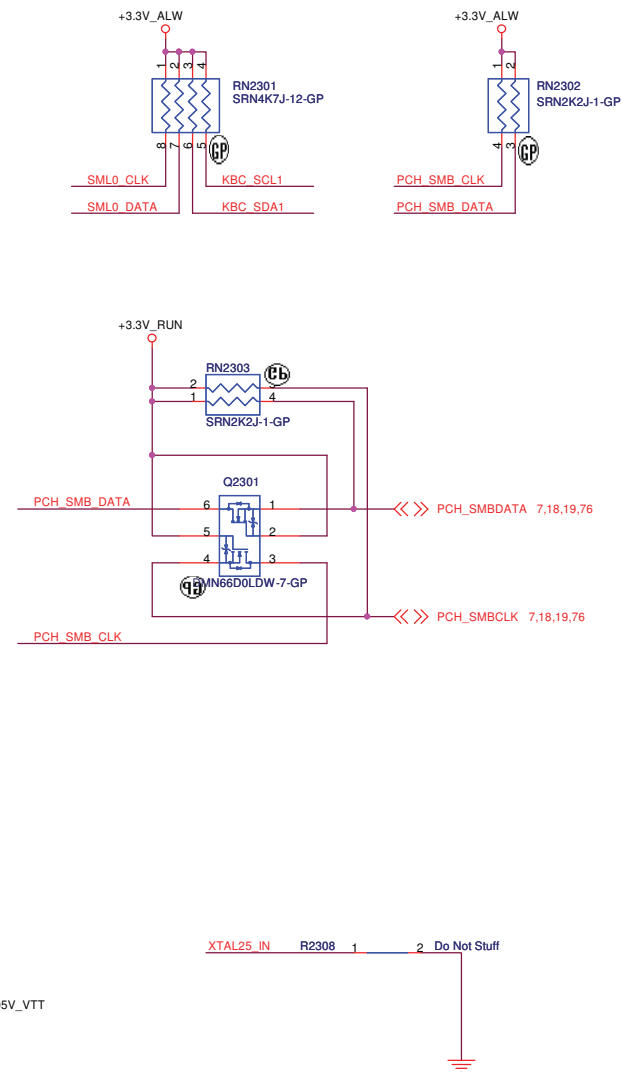
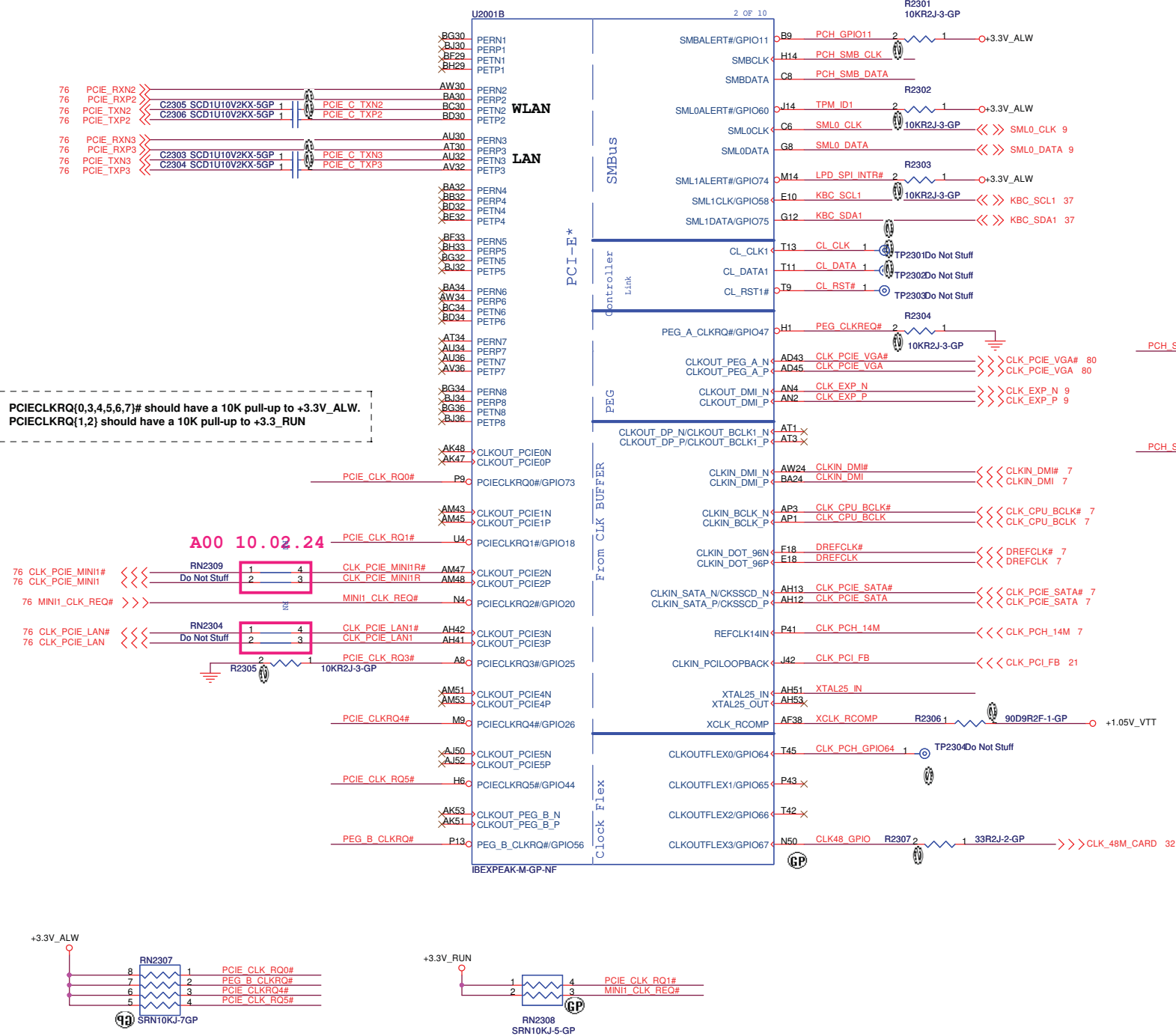
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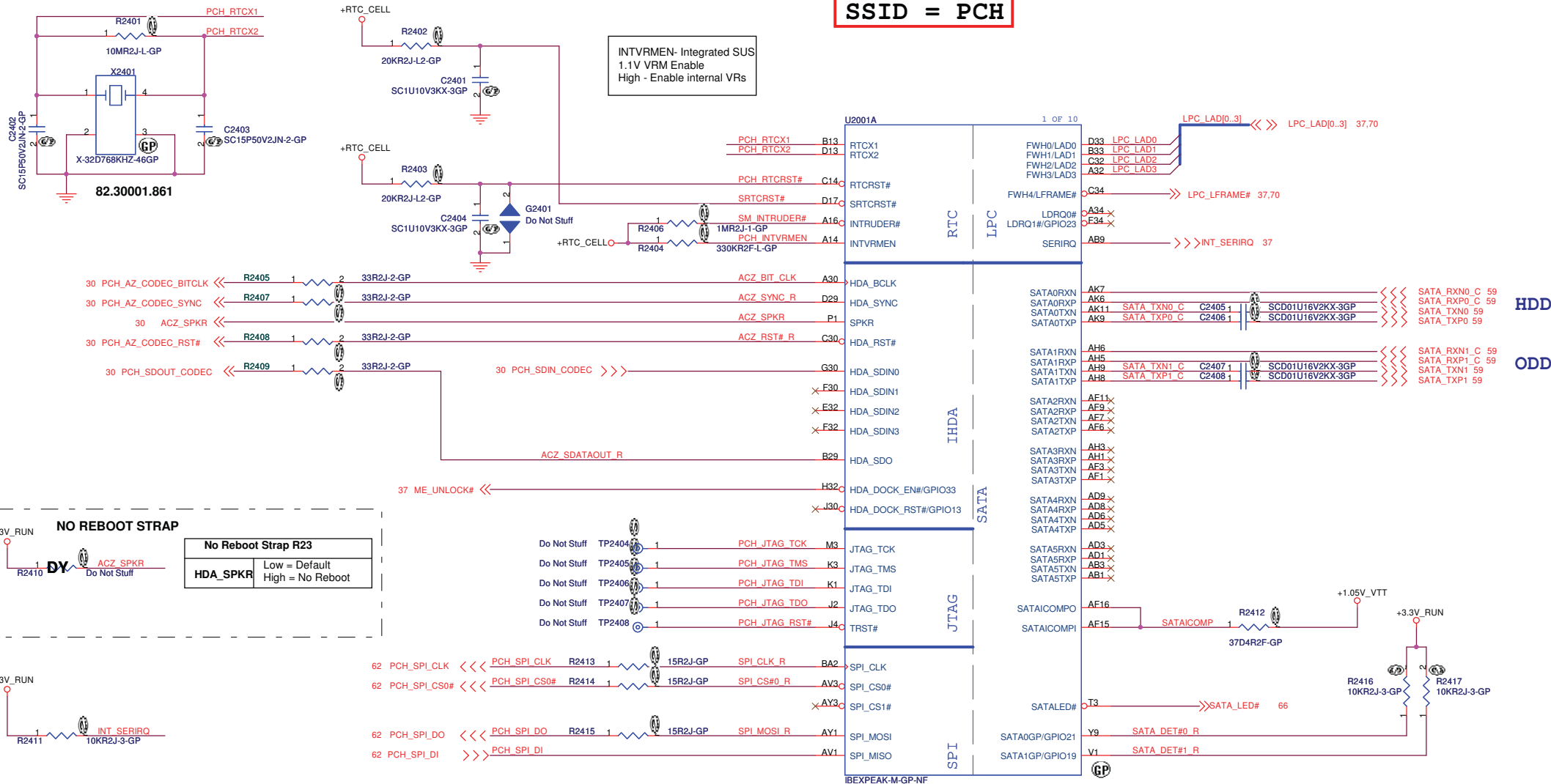
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SSID = PCH



SSID = PCH

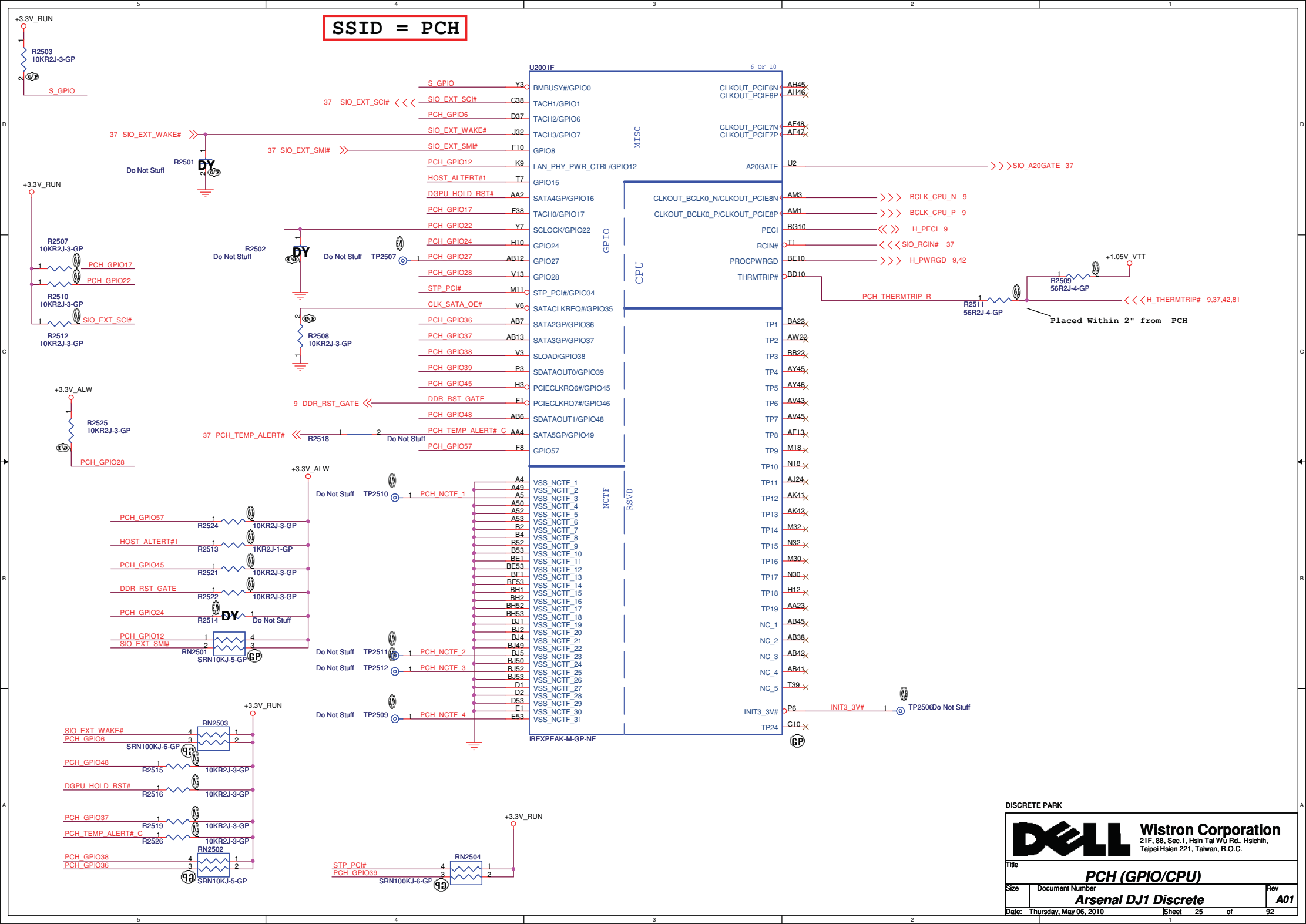


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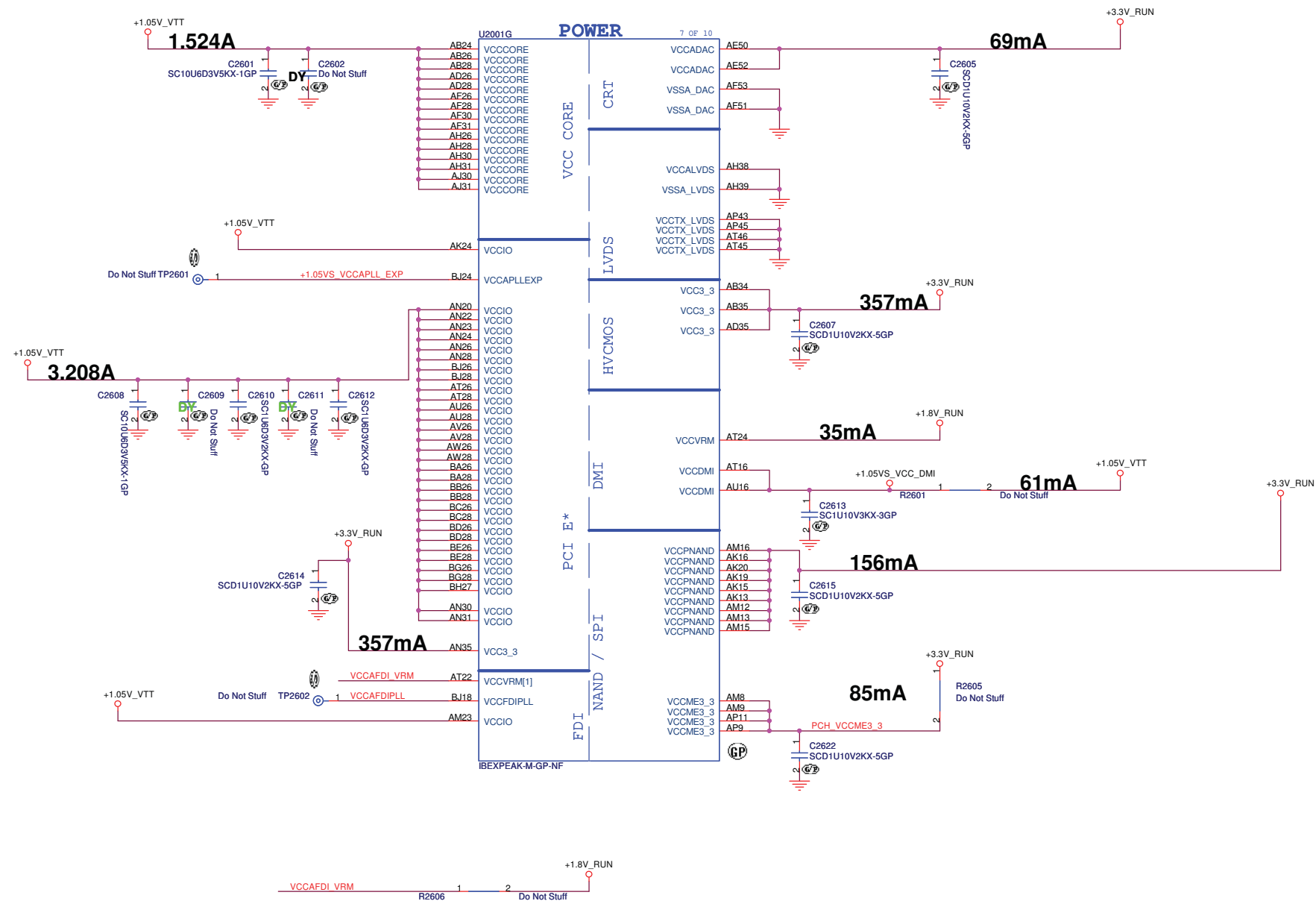
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Title: **PCH (SPI/RTC/LPC/SATA/IHDA)**
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Arsenal DJ1 Discrete

SSID = PCH



SSID = PCH



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	Title
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PCH (POWER1)

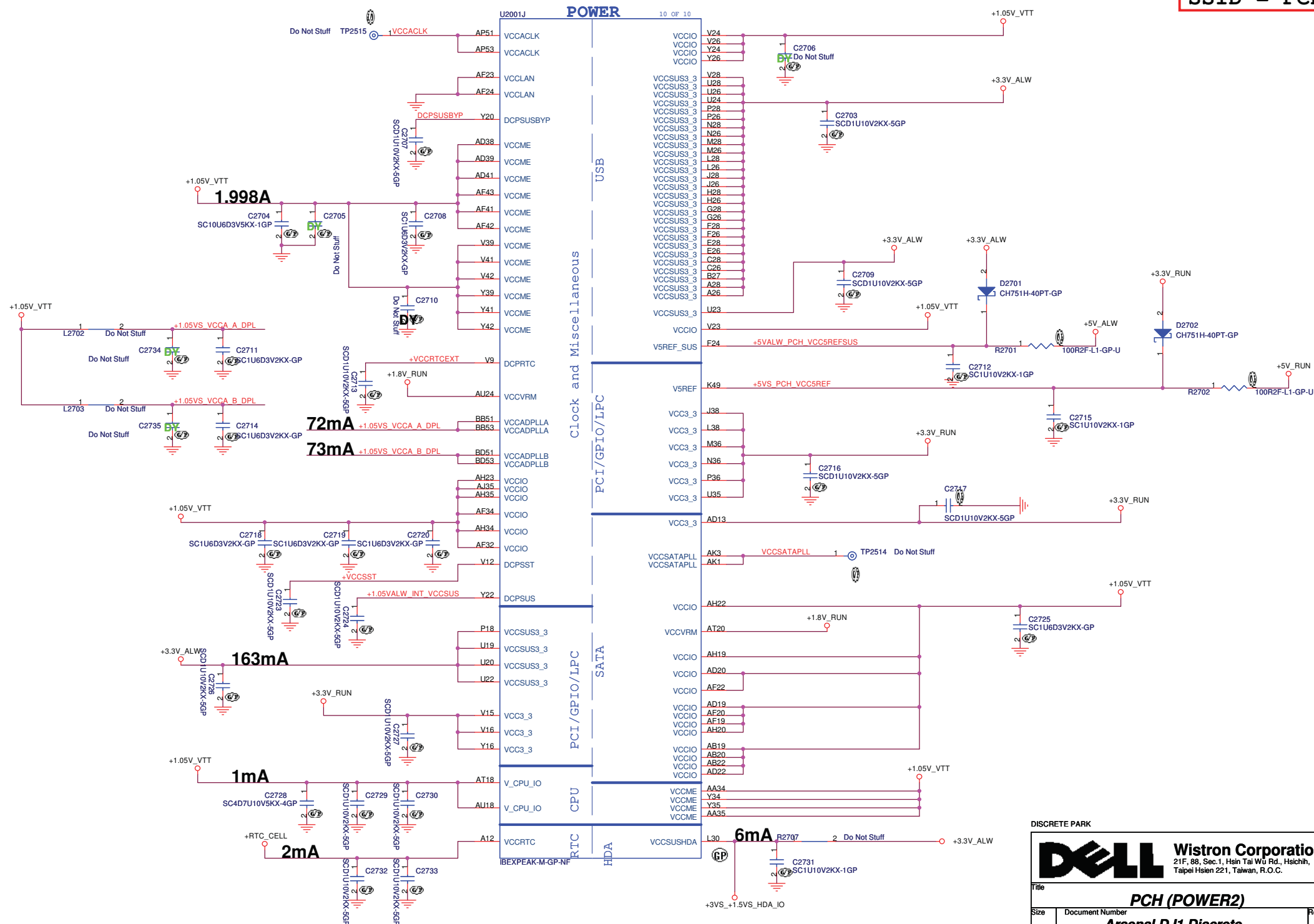
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Arsenal DJ1 Discrete

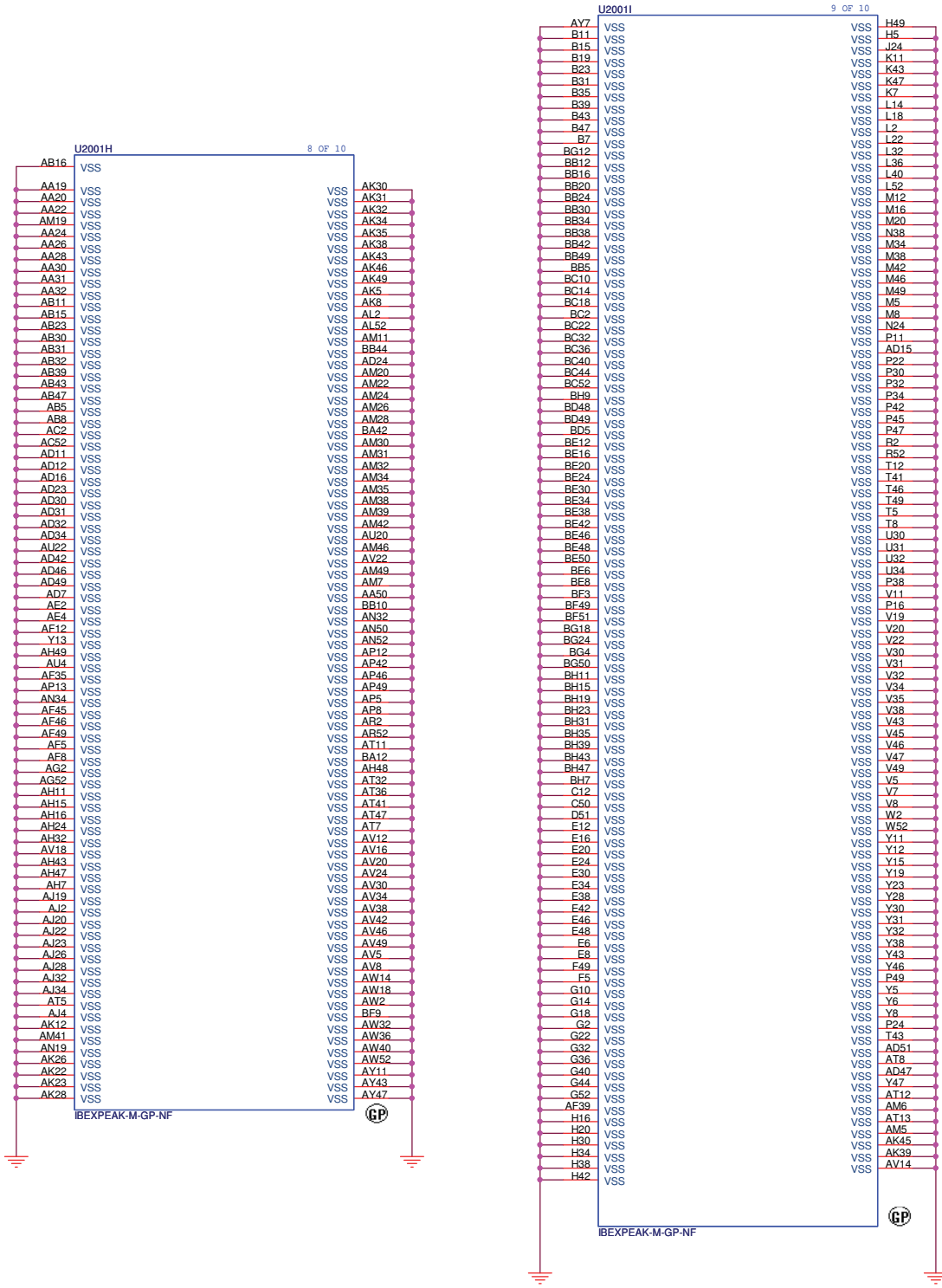
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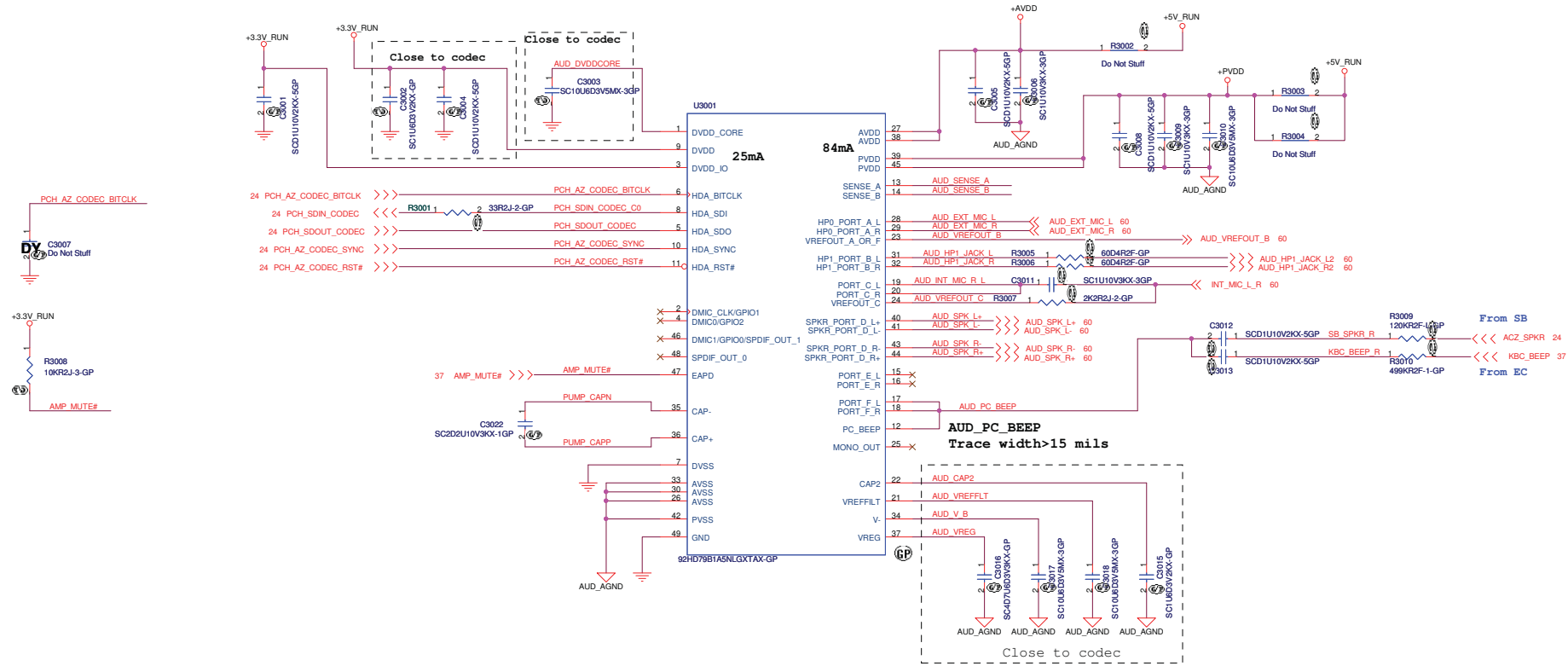
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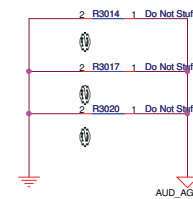
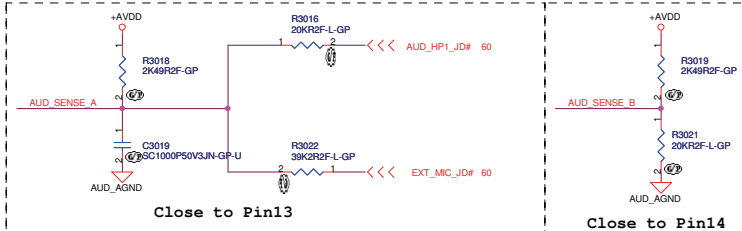
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SSID = AUDIO



Azalia I/F EMI

PCH_SDOUT_CODEC



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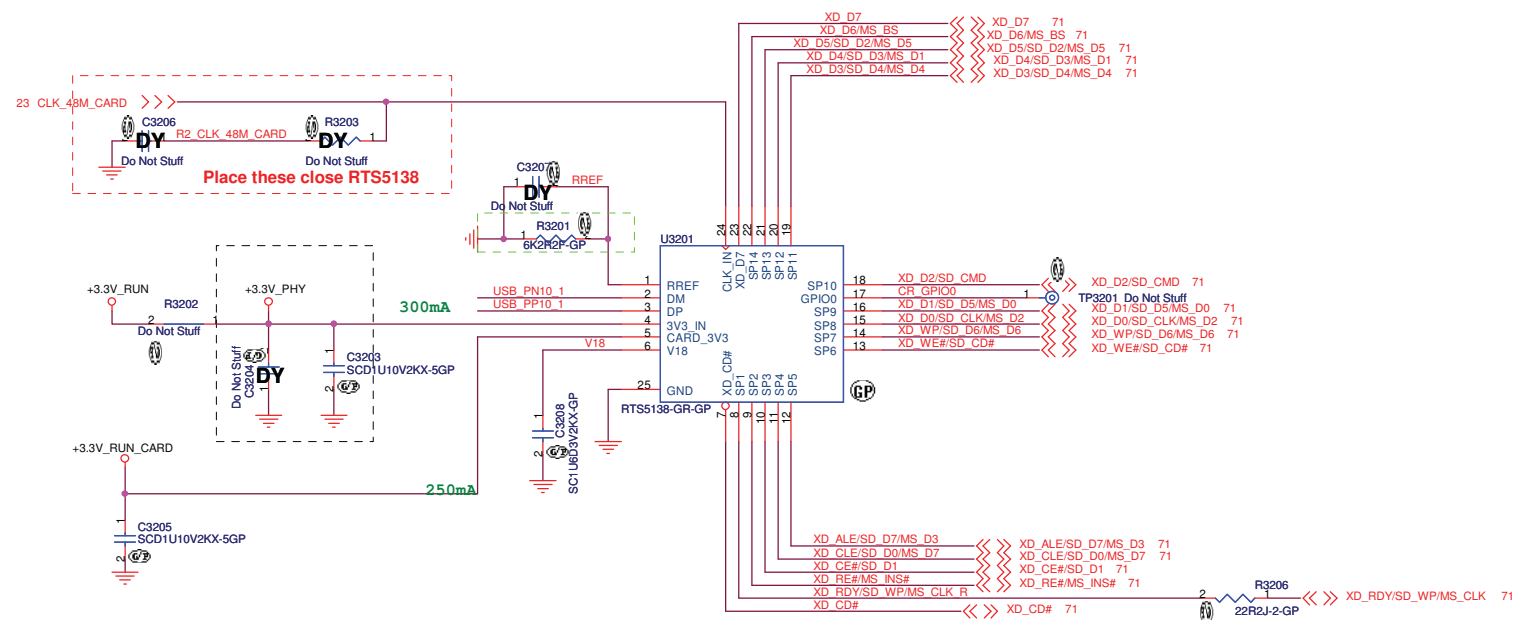
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Taippei Hsien 221, Taiwan, R.O.C.

Audio Codec 92HD79B1

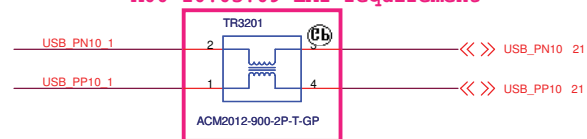
Size: Custom
Document Number: Arsenal D/J1 Discrete
Date: Thursday, May 06, 2010
Sheet: 30 of 92

Rev: A01

SSID = SDIO



A00 10.03.09 EMI requirement



DISCRETE PARK



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Card Reader-RTS5138

Size	1
Custom	

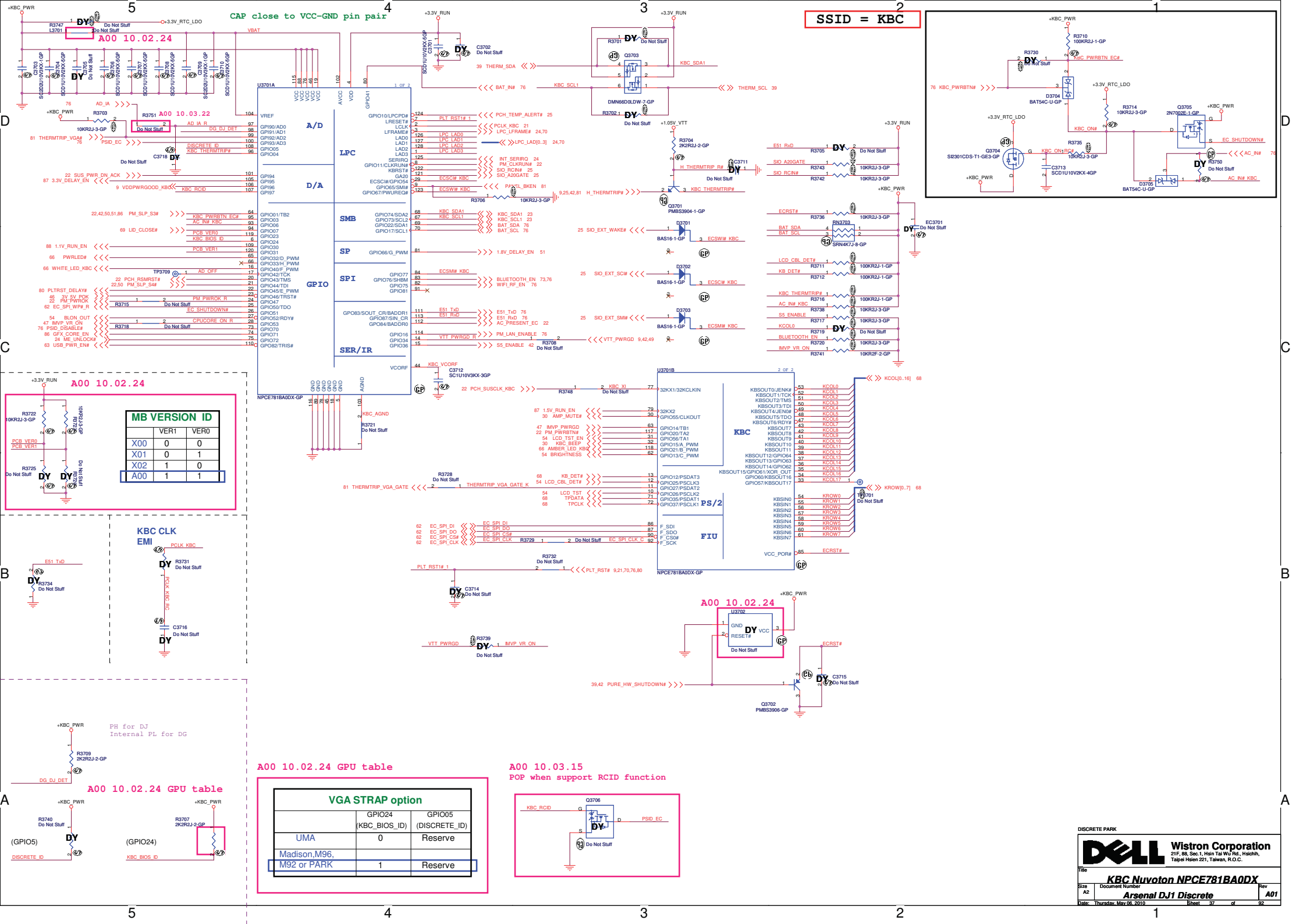
Document Number	Area
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Arsenal DJ1 Discrete

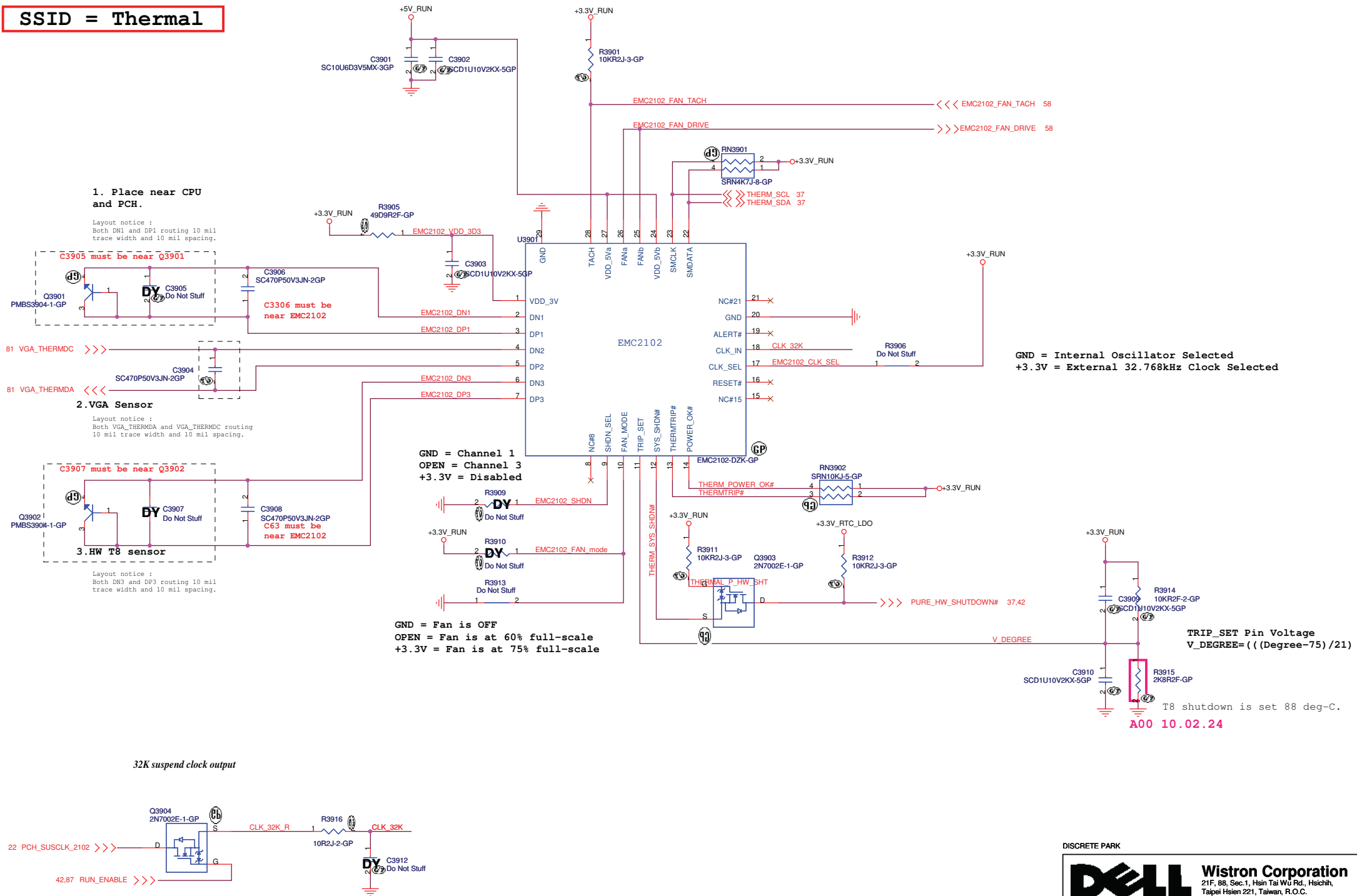
A01

Date: Thursday, May 06, 2010

Sheet	32	of	92
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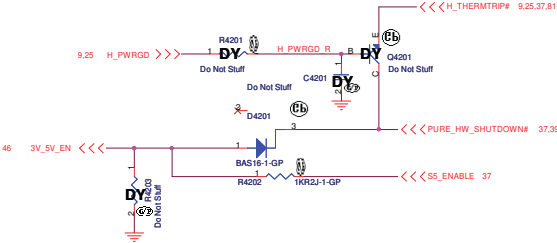
SSID = Thermal



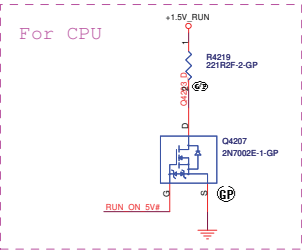
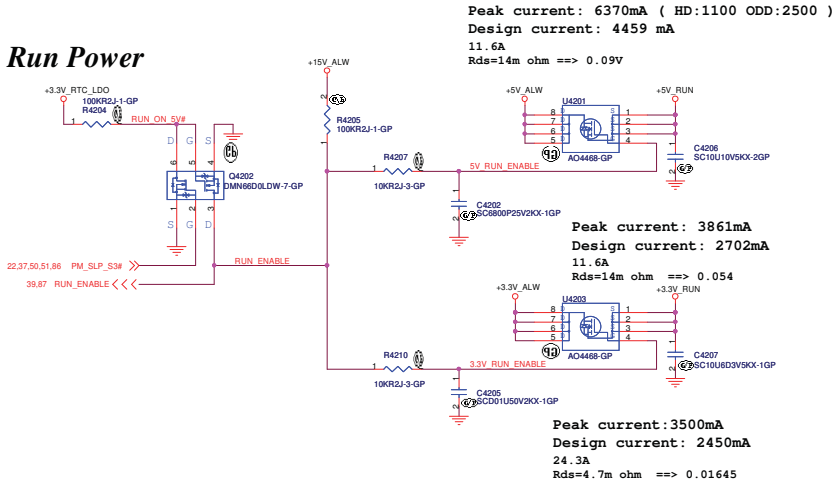
DISCRETE PARK



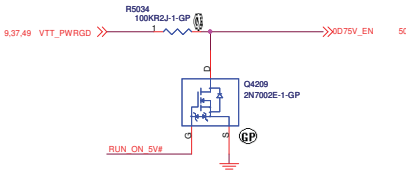
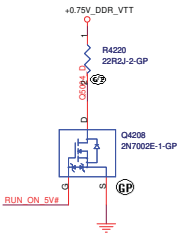
SSID = Reset.Suspend

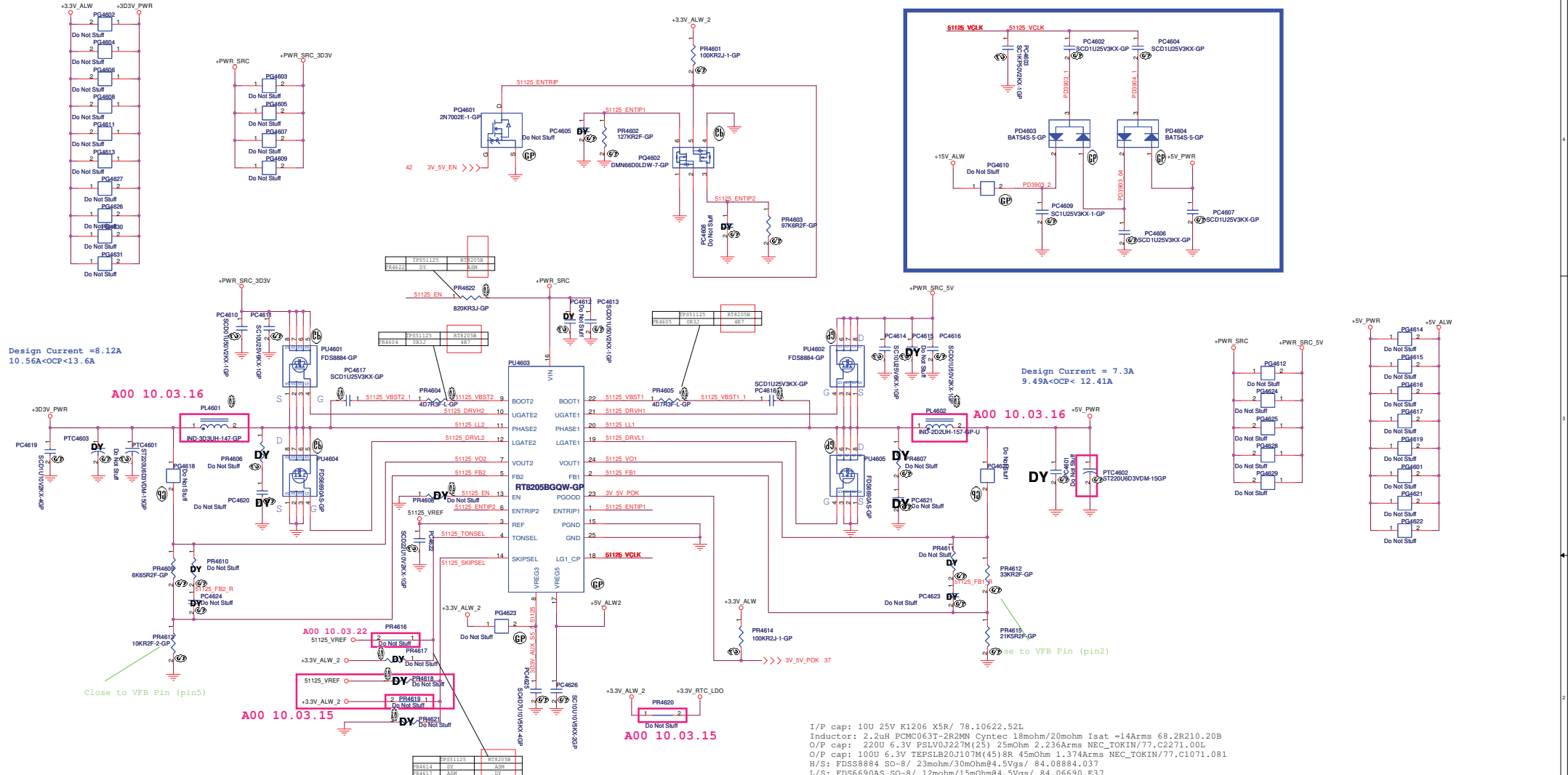


Run Power



425302_425302_Calpella_S3PowerReduction_WhitePape
Revision 0.7





I/P cap: 10u 25V K1206 X5R/ 78.10622.52L
Inductor: 3.3uH PCMB104T-3R3MS Cyntec 10.8mohm/11.8mohm Isat =16Arms 68.3R310.20C
O/P cap: 220u 6.3V PSLV0J227M(25) 25mohm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100u 6.3V TEP5LB20J107M(45)BR 45mohm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: FDS6690AS SO-8/ 23mohm/30mohm@4.5Vgs/ 84.08884.037
L/S: FDS6690AS SO-8/ 12mohm/15mohm@4.5Vgs/ 84.06690.E37

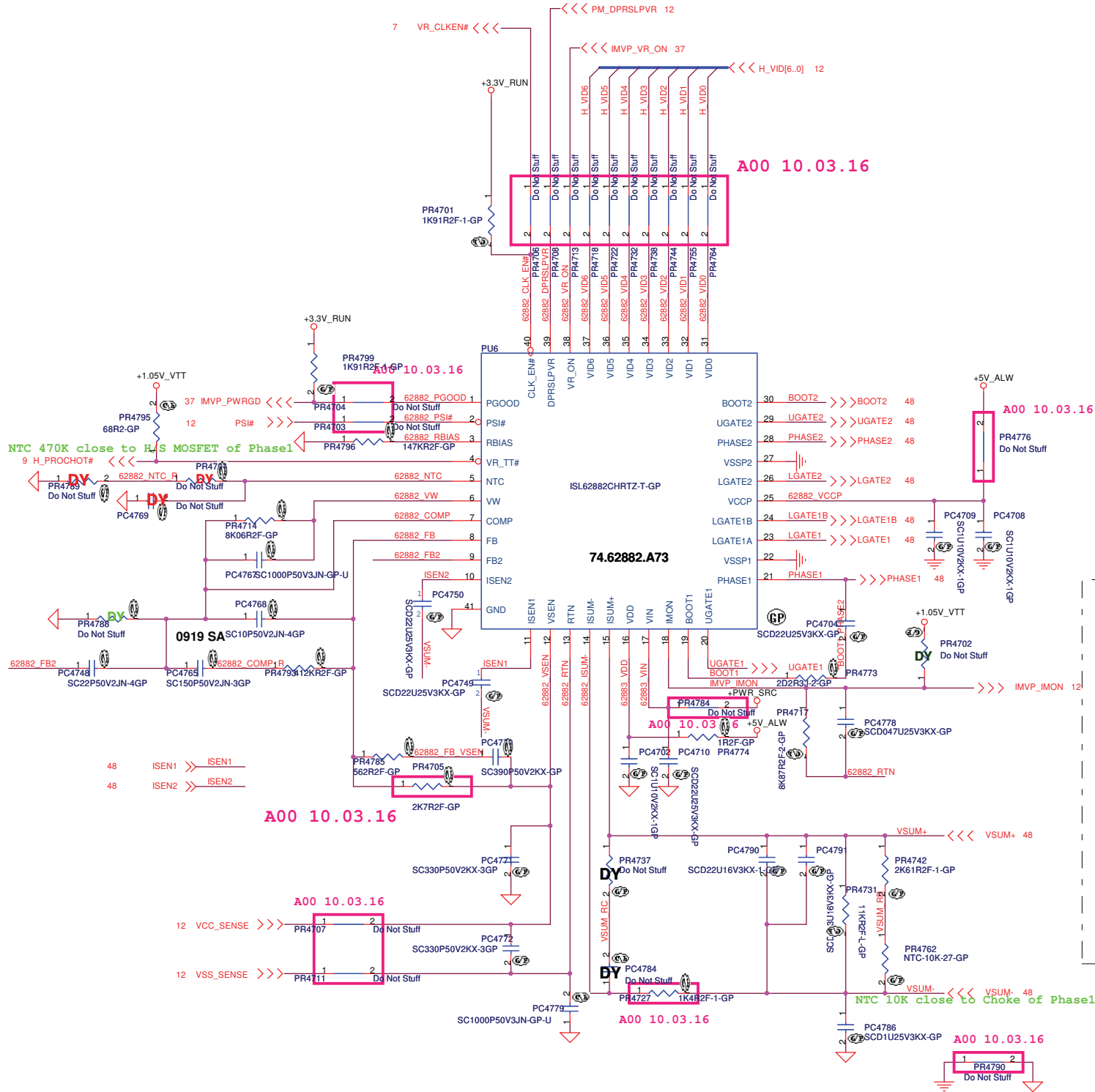
TPS51125:		
TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

RT8205B:		
TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3	365kHz	460kHz
VREG5	365kHz	460kHz

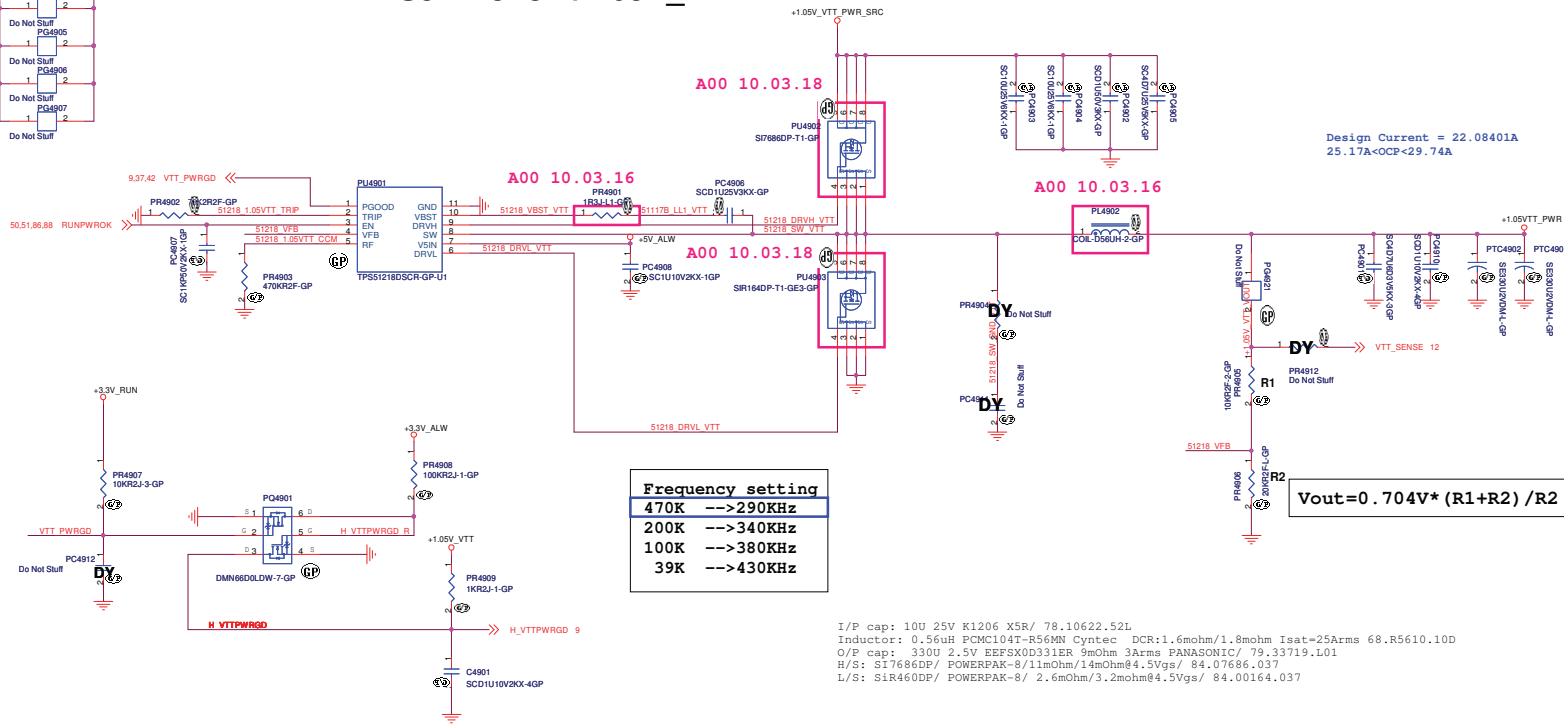
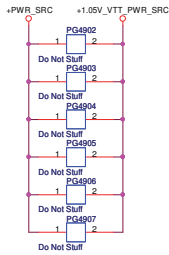
SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

EN0	Open	820kΩ to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

I/P cap: 10u 25V K1206 X5R/ 78.10622.52L
Inductor: 2.2uH PCMC063T-2R2MN Cyntec 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P cap: 220u 6.3V PSLV0J227M(25) 25mohm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100u 6.3V TEP5LB20J107M(45)BR 45mohm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: FDS6690AS SO-8/ 23mohm/30mohm@4.5Vgs/ 84.08884.037
L/S: FDS6690AS SO-8/ 12mohm/15mohm@4.5Vgs/ 84.06690.E37

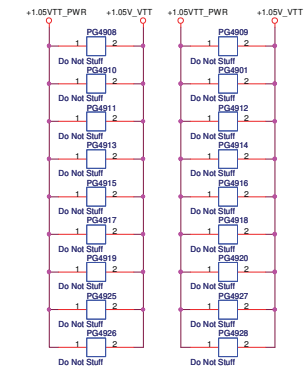


TPS51218 for +1.05V_VTT

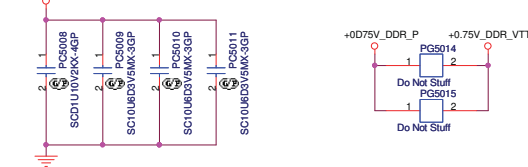
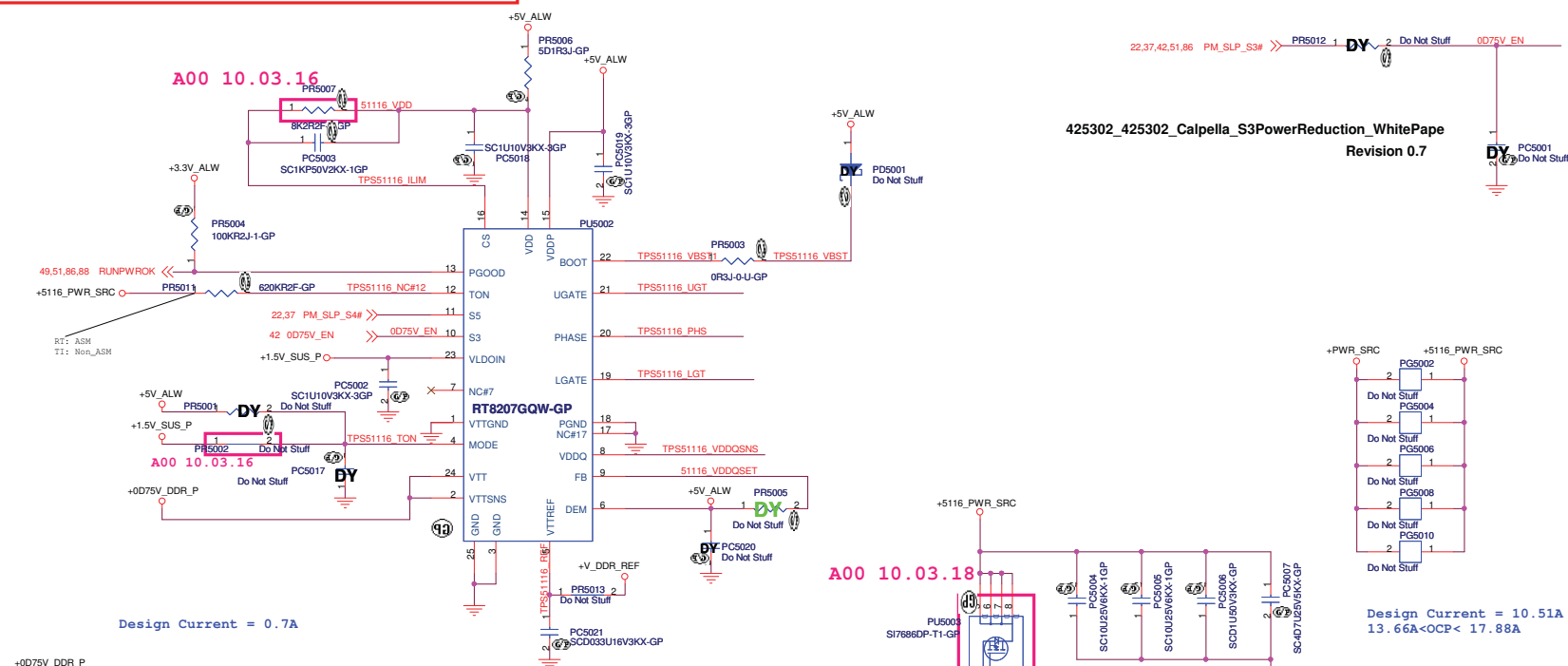


Design Current = 22.08401A
 25.17A<OCP<29.74A

$$V_{out} = 0.704V * (R1 + R2) / R2$$



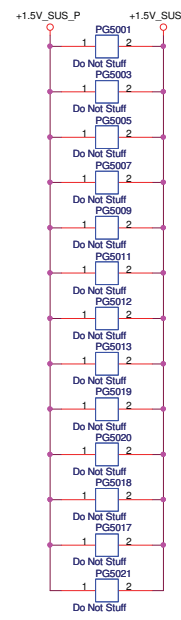
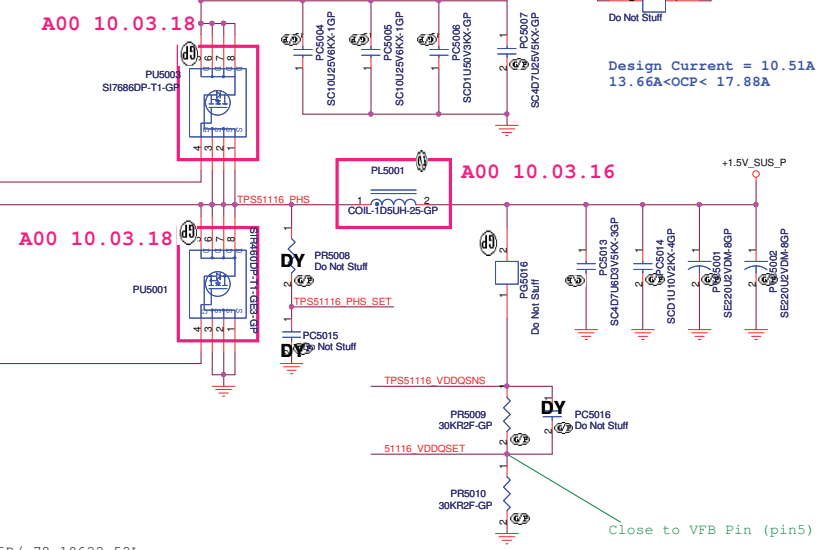
SSID = PWR.Plane.Regulator_1p5v0p75v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5uH PCMC104D-1R5 Cyntec DCR:3.8mohm Isat=33Arms 68.1R510.10J
O/P cap: 220U 2V EEFCT0D21ER 150mOhm 2.7Arms PANASONIC/ 79.22719.20L
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm4.5Vgs/ 84.00460.037
Switching freq-->400KHz



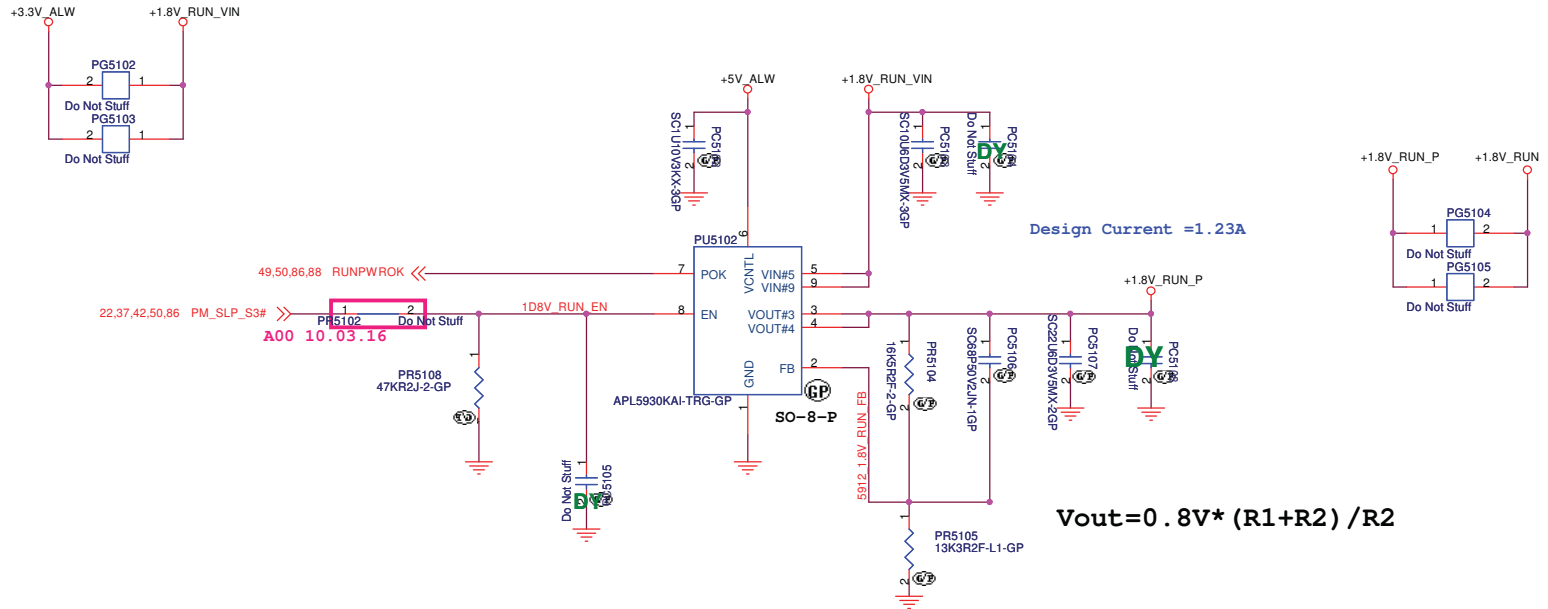
DISCRETE PARK



Title			
TPS51116 +1.5V <i>SUS</i>			
Size	Document Number	Rev	
Custom	Arsenal DJ1 Discrete	A01	
Date:	Thursday, May 06, 2010	Sheet 50	of 92

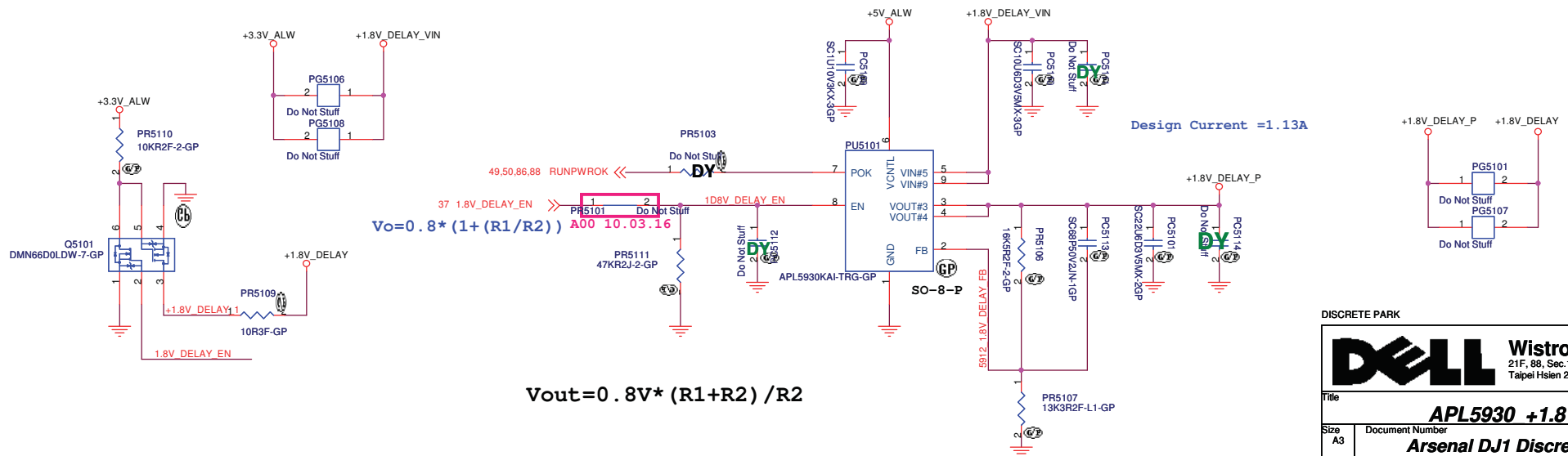
SSID = PWR.Plane.Regulator_1p8v

APL5930 for +1.8V_RUN



SSID = PWR.Plane.Regulator_1p8v

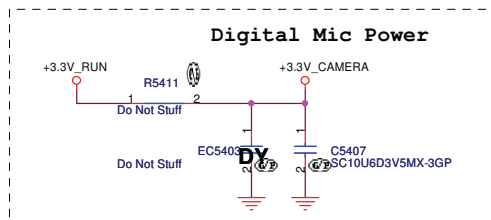
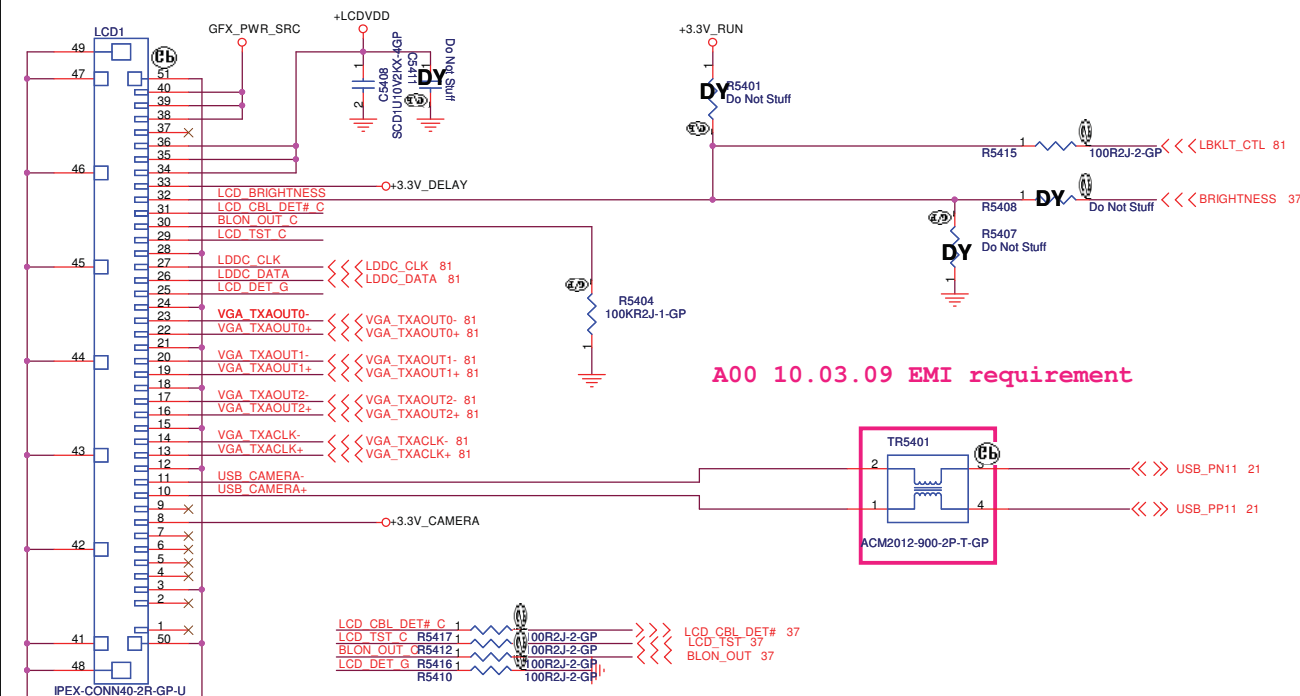
APL5930 for +1.8V_DELAY



DISCRETE PARK

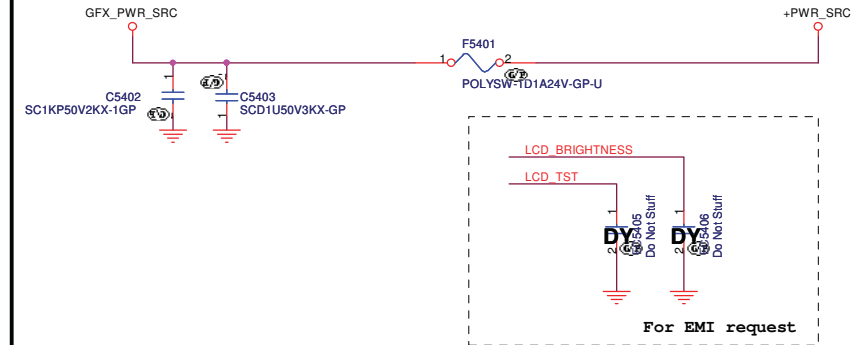
SSID = VIDEO

LVDS CONNECTOR



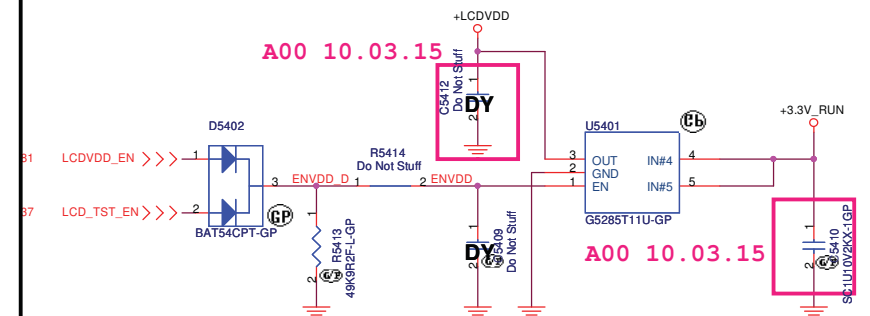
SSID = Inverter

INVERTER POWER



SSID = VIDEO

LCD POWER



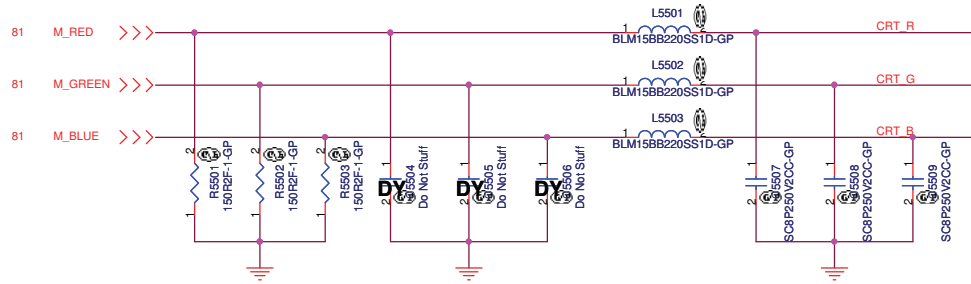
DISCRETE PARK

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<i>LCD/Inverter Connector</i>			
Size A3	Document Number		Rev <i>A01</i>
<i>Arsenal DJ1 Discrete</i>			
Date:	Thursday, May 06, 2010	Sheet 54	of 92

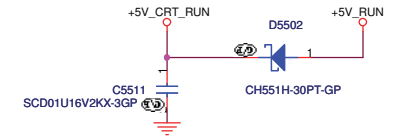
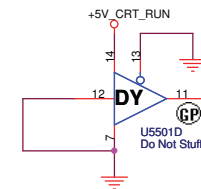
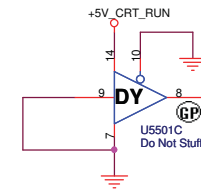
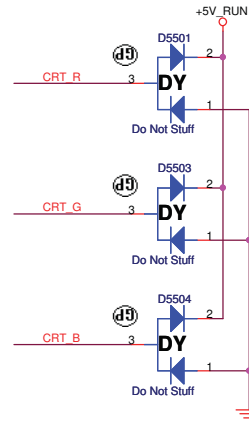
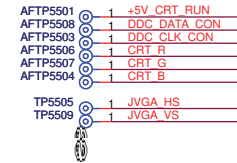
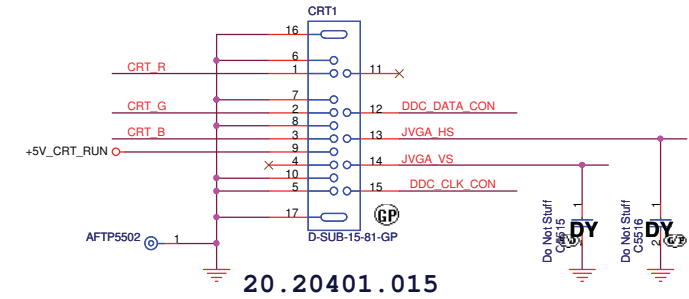
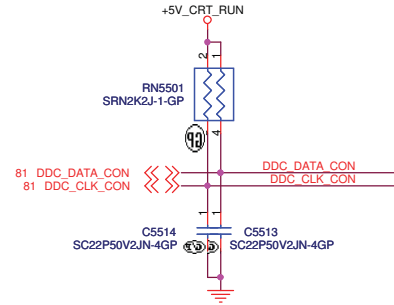
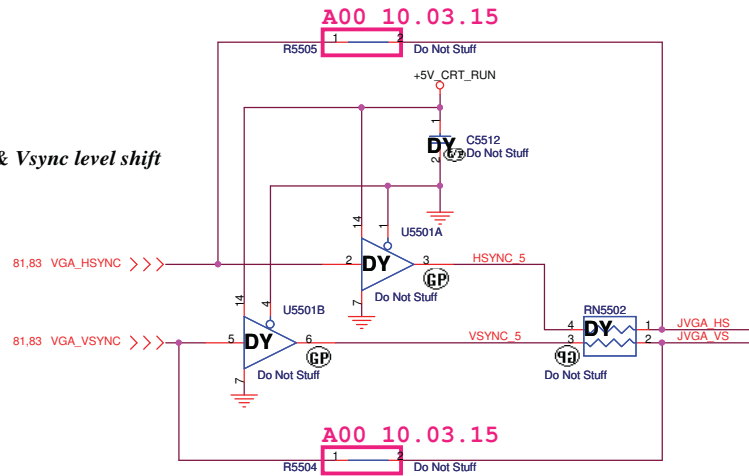
SSID = VIDEO

Layout Note:

- *Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
- * RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.



Hsync & Vsync level shift

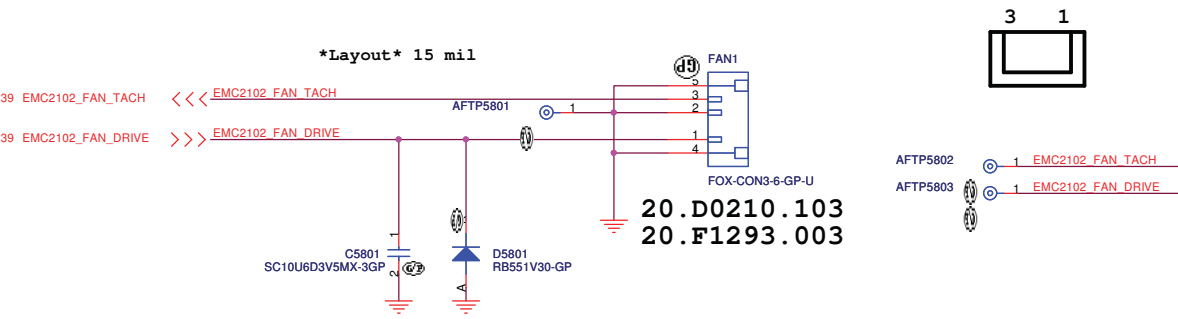


DISCRETE PARK

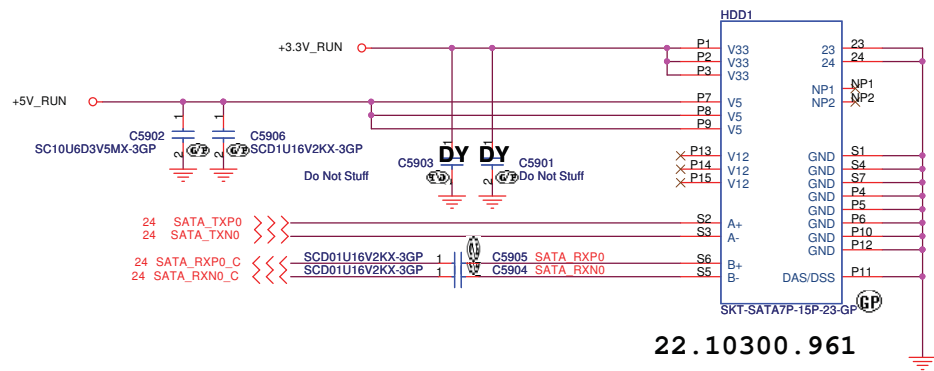
SSID = User.Interface

SSID = Thermal

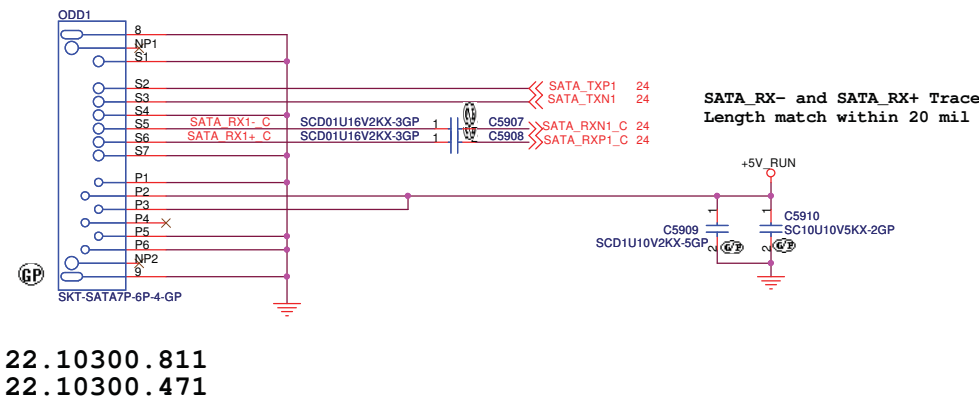
Fan Connector



SATA HDD Connector



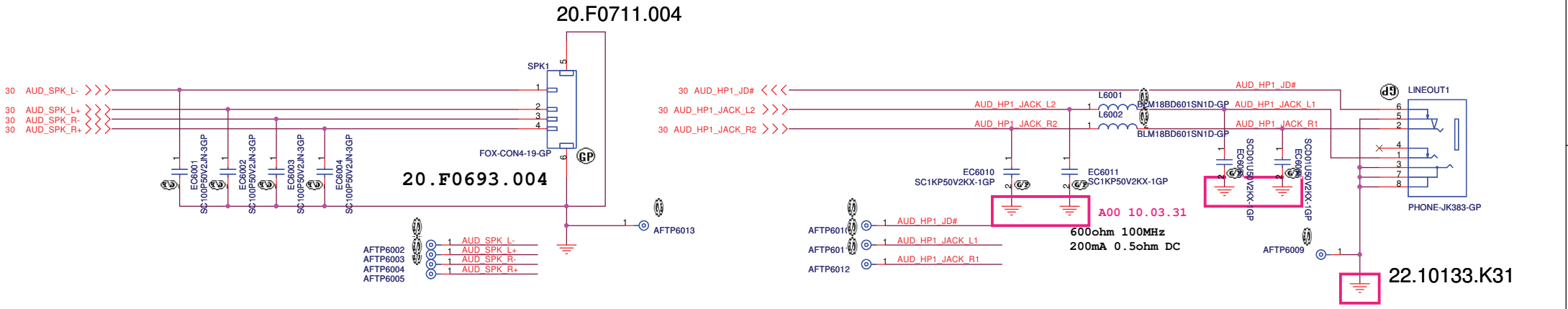
ODD Connector



SSID = AUDIO

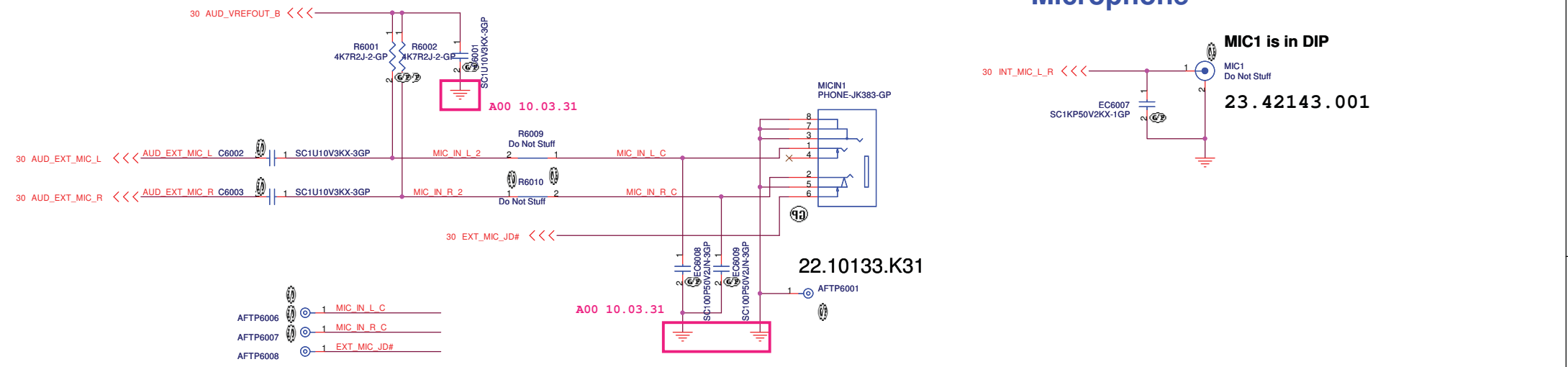
Speaker Connector

LINE1 OUT



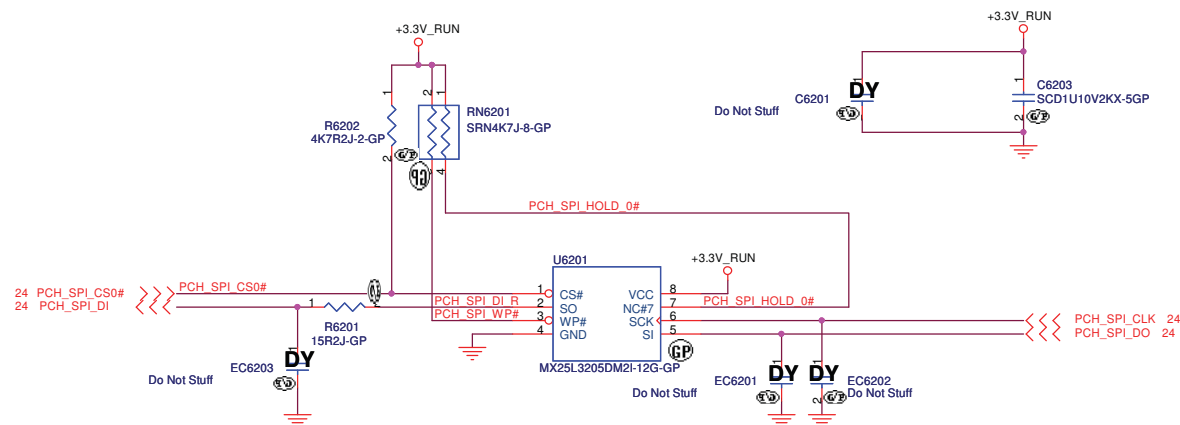
MIC IN

Internal Microphone

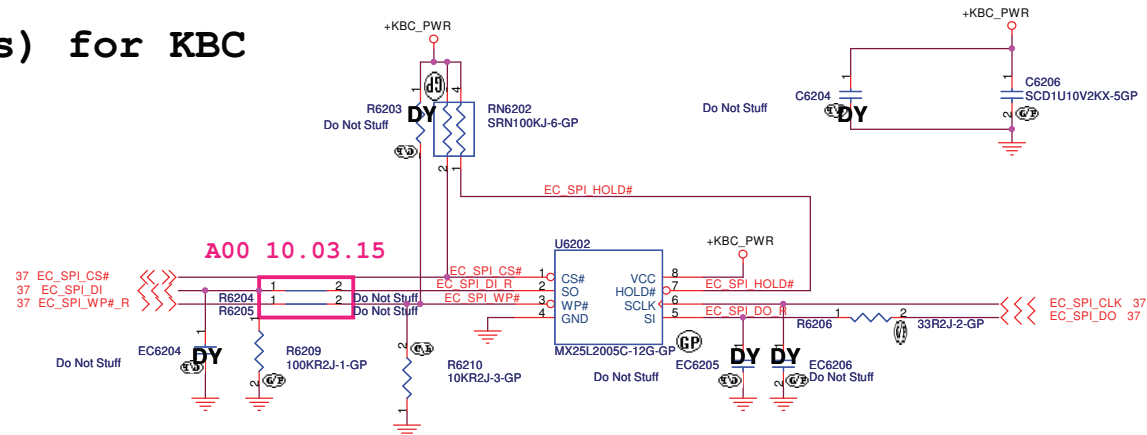


SSID = Flash.ROM

SPI FLASH ROM (32M bits) for PCH

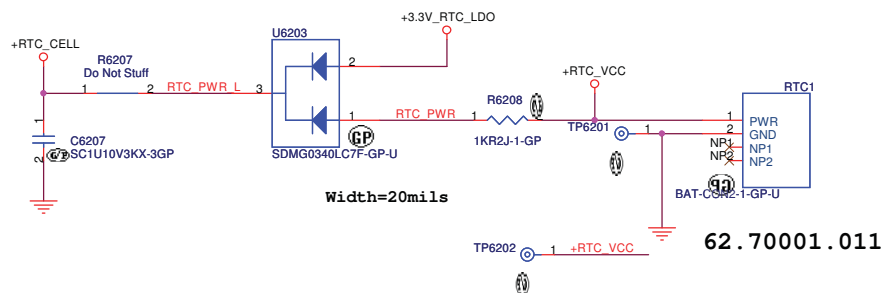


SPI FLASH ROM (2M bits) for KBC



SSID = RBATT

RTC Connector



DISCRETE PARK



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Flash/RTC

Size
A3

Document Number

Arsenal DJ1 Discrete

Rev

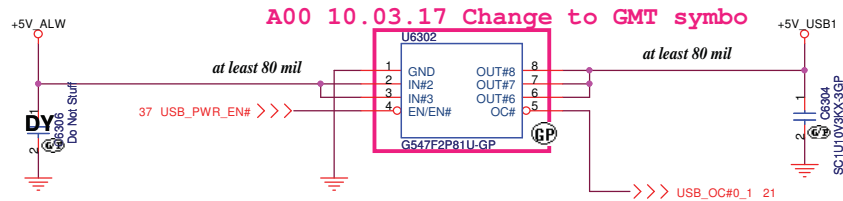
A01

Date: Thursday, May 06, 2010

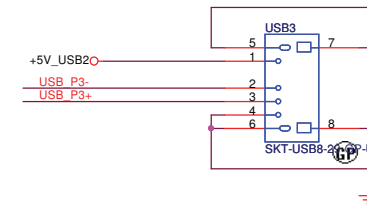
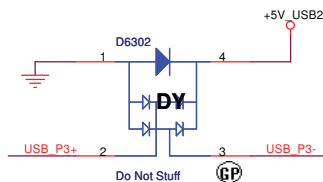
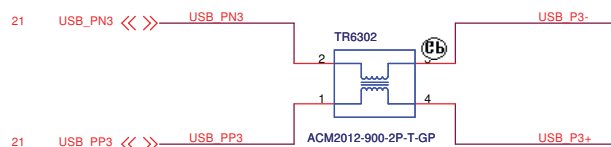
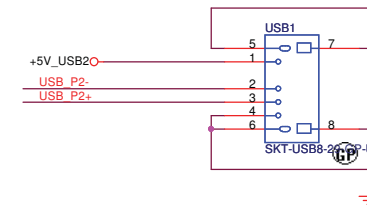
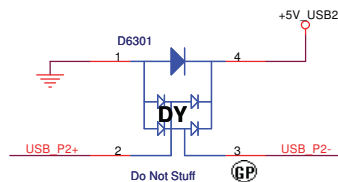
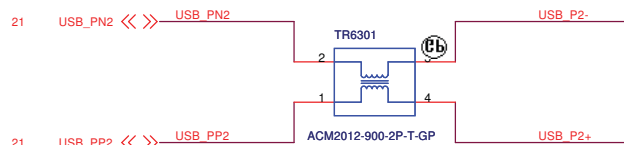
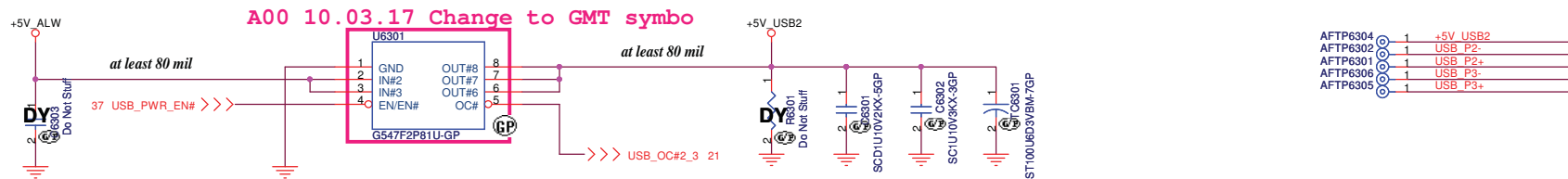
Sheet 62 of 92

SSID = USB

IO Board USB Power



Right USB Power



22.10254.451

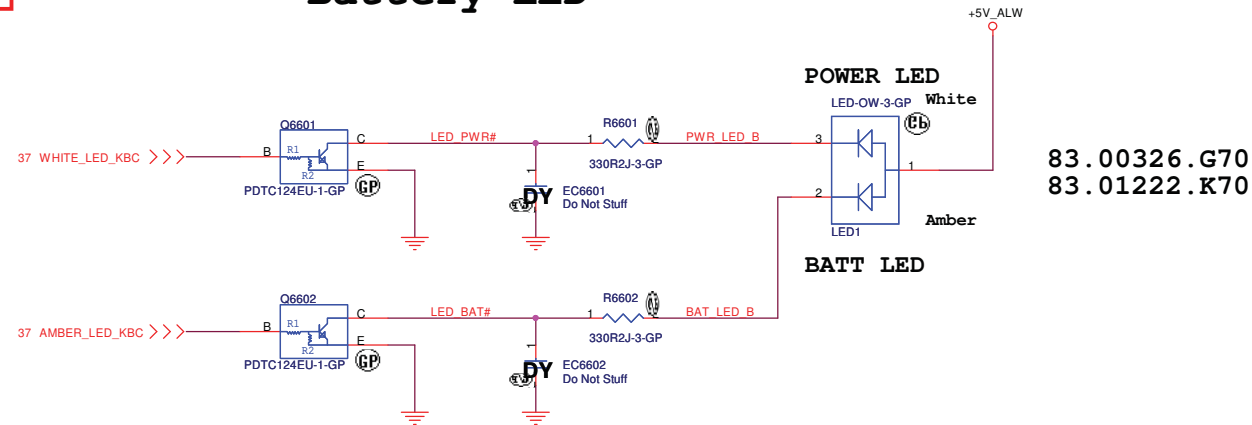
DISCRETE PARK

DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

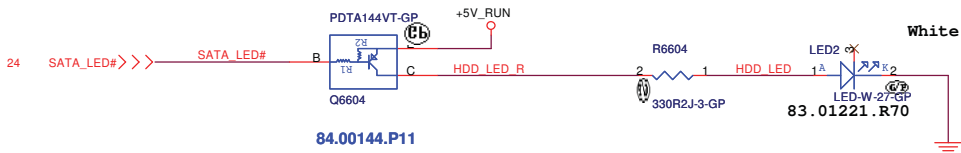
Title				
USB				
Size	Document Number			Rev
	Arsenal DJ1 Discrete			A01
Date:	Thursday, May 06, 2010	Sheet	63	of 92

SSID = User.Interface

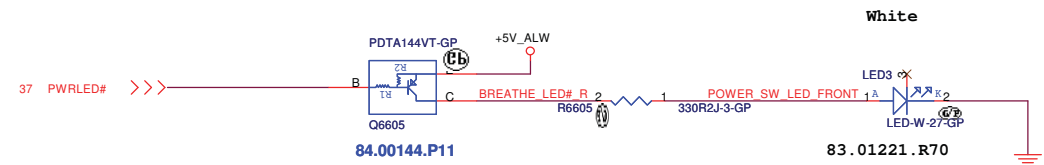
Battery LED



HDD LED



BREATHE PWR LED (Front)



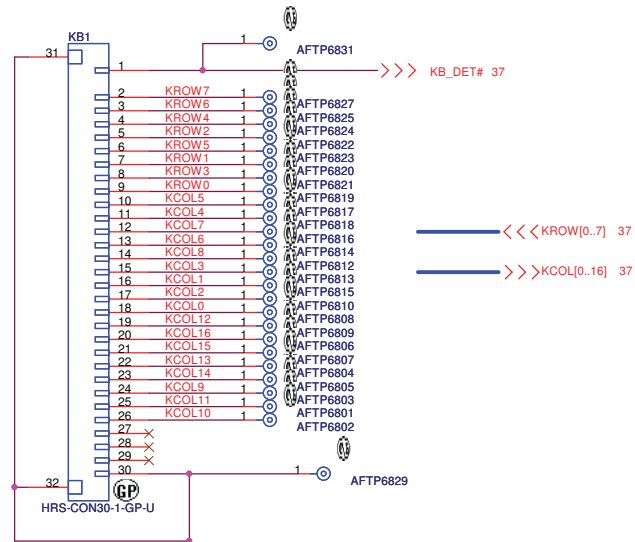
DISCRETE PARK

DELL Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **LED**
Size: A3 Document Number: **Arsenal DJ1 Discrete** Rev: **A01**
Date: Thursday, May 06, 2010 Sheet: 66 of 92

SSID = KBC

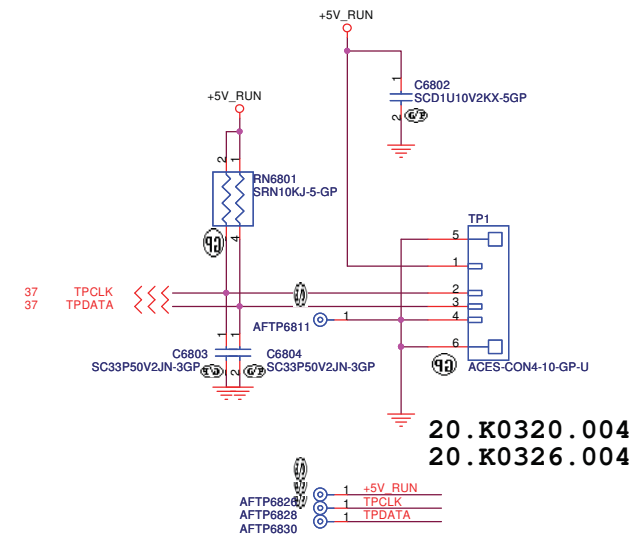
Internal KeyBoard Connector

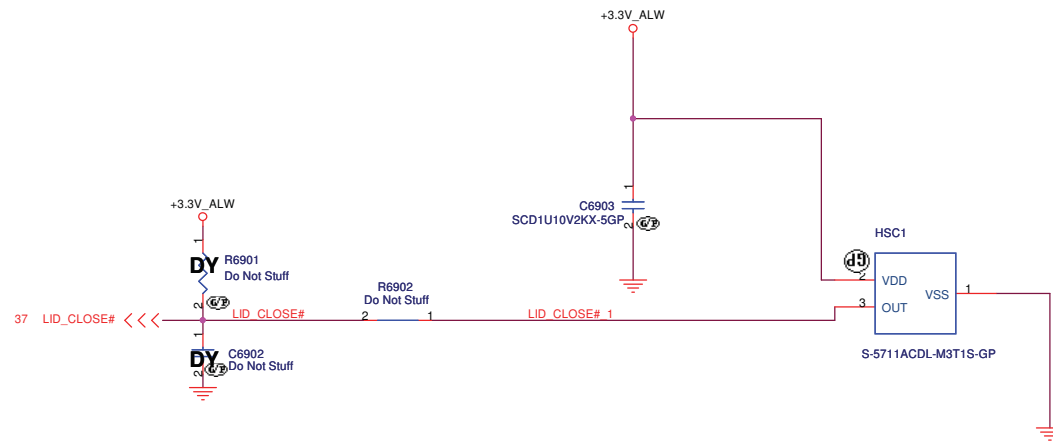


Main 20.K0421.030
20.K0259.030

```
SSID = Touch.Pad
```

TouchPad Connector





DISCRETE PARK



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Hall Sensor

Size
A3

Document Number

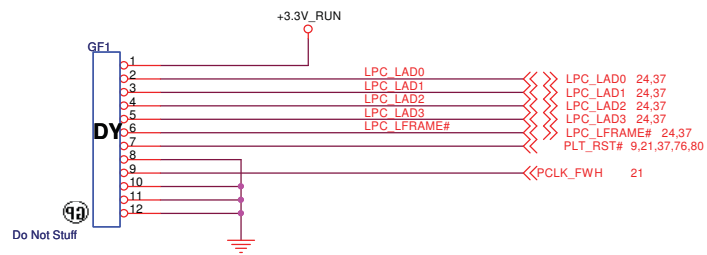
Arsenal DJ1 Discrete

Rev

A01

Date: Thursday, May 06, 2010

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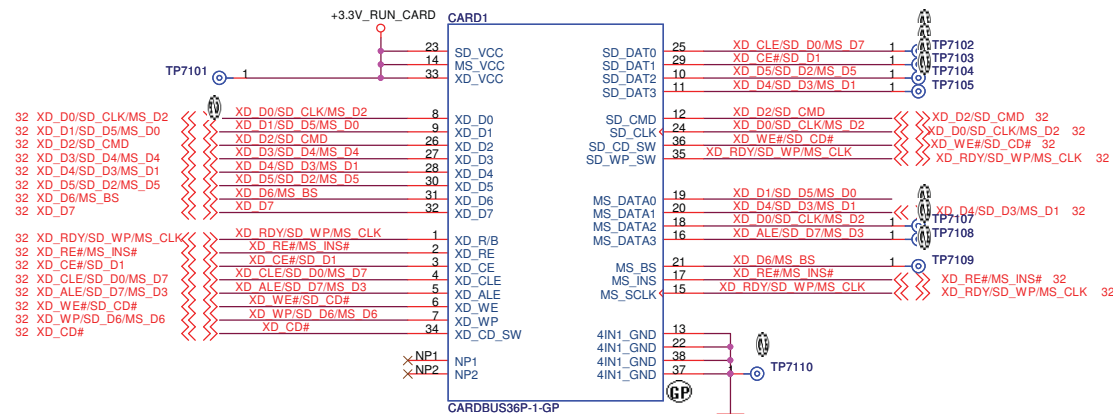
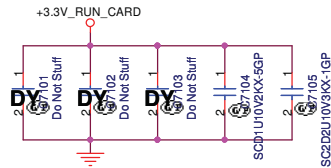


DISCRETE PARK

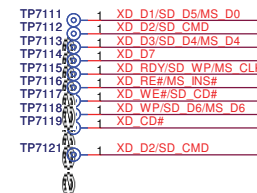
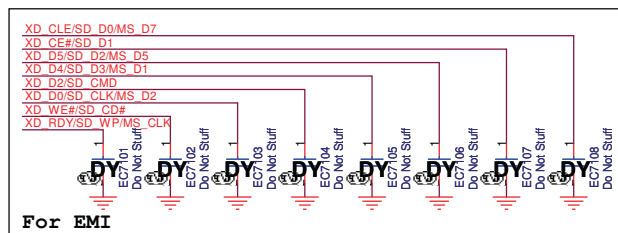
		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size A3	Document Number Arsenal DJ1 Discrete		Rev A01
Date: Thursday, May 06, 2010	Sheet 70	of 92	

SSID = SDIO

SD/XD/MS Card Reader



20.I0109.001
20.I0081.011



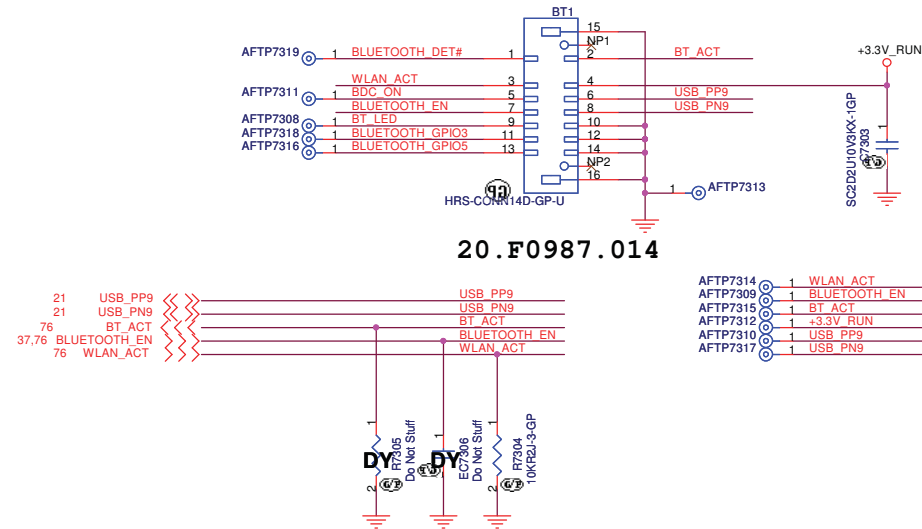
DISCRETE PARK



Title			CARD Reader CONN		
Size			Document Number		
A3			Arsenal DJ1 Discrete		
Date: Thursday, May 06, 2010			Sheet 71 of 92		
Rev			A01		

SSID = User.Interface

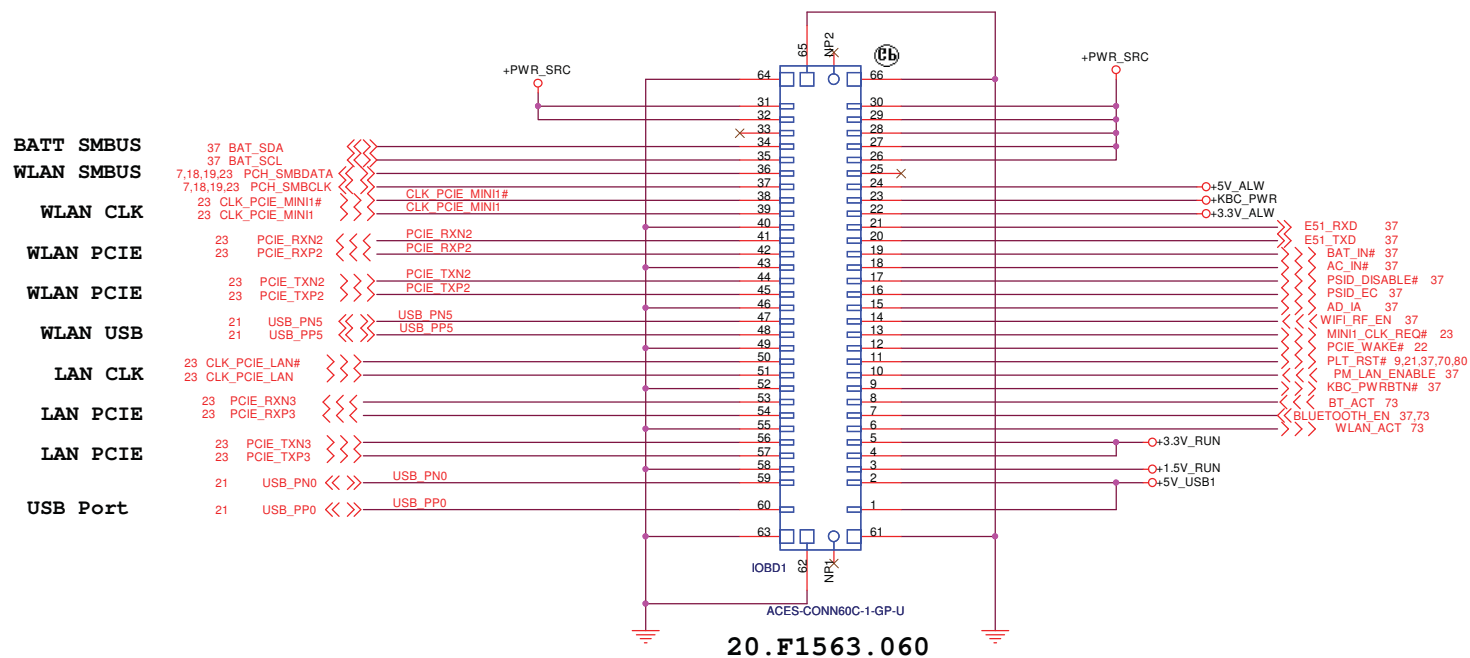
Bluetooth Module conn.



DISCRETE PARK

DELL			Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
Bluetooth					
Size A3	Document Number Arsenal DJ1 Discrete				Rev A01
Date: Thursday, May 06, 2010	Sheet 73		of 92		

SSID = PWR.Support



DISCRETE PARK



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21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

IO Board Connector

Size

A3

Document Number

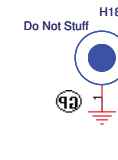
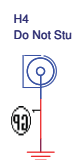
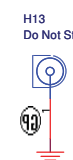
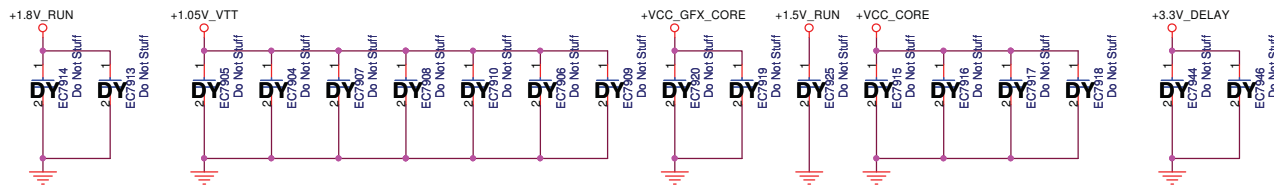
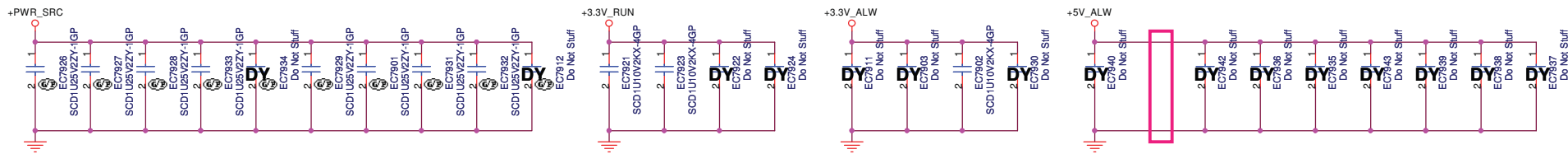
Arsenal DJ1 Discrete

Rev

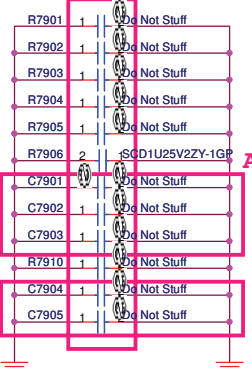
A01

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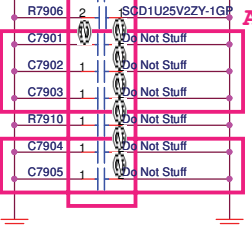
A01 10.05.03



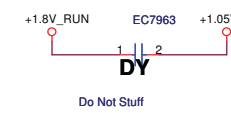
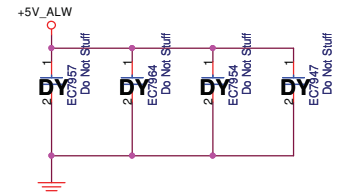
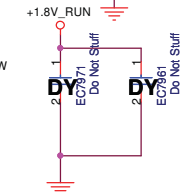
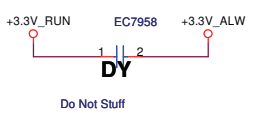
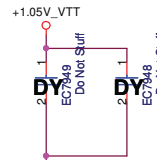
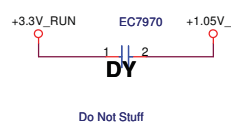
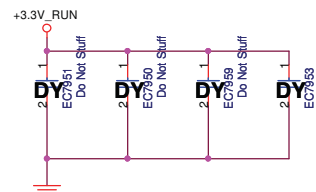
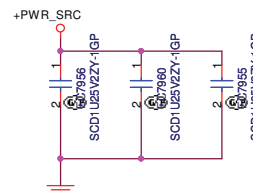
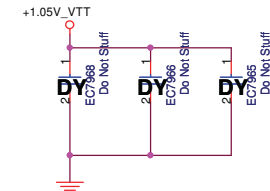
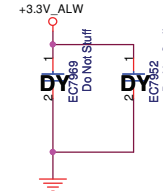
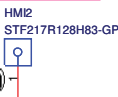
A00 10.03.09 Remove HBT1



A00 10.03.15



A00 10.04.01



DISCRETE PARK



Title				
UNUSED PARTS/EMI Capacitors				
Size	Document Number			Rev
A3	Arsenal DJ1 Discrete			A01
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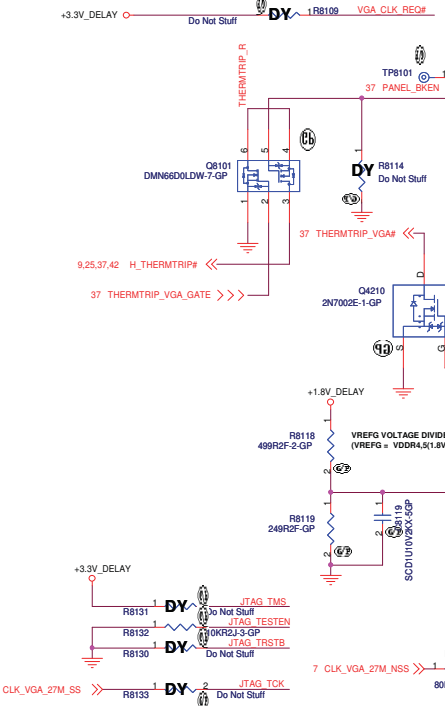
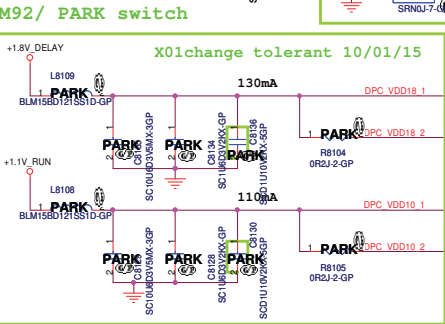
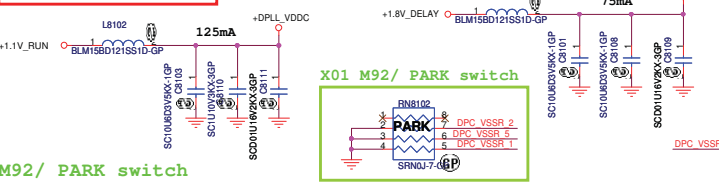
PCIE_MRX_GTX_N[0..15] >> PCIE_MRX_GTX_N[0..15] 8

**VGA PCIE(1/4)**

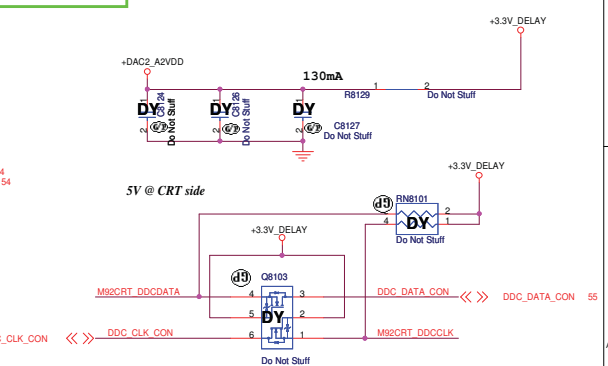
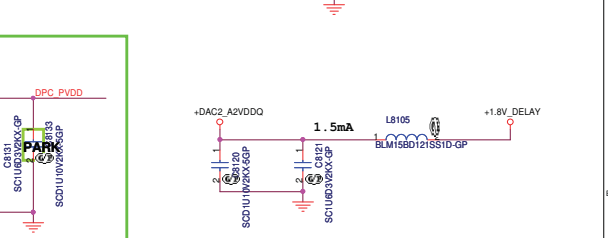
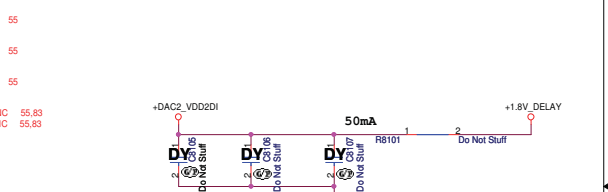
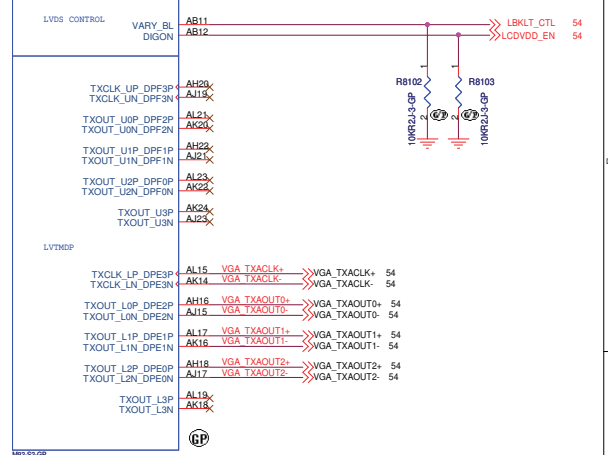
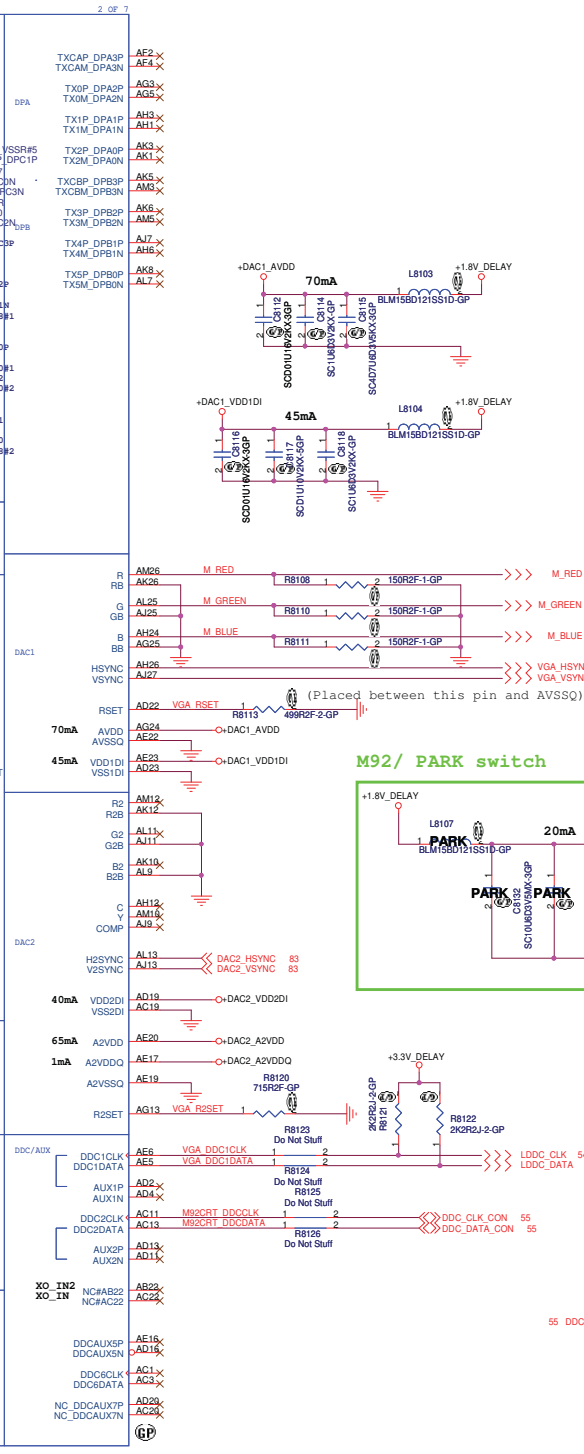
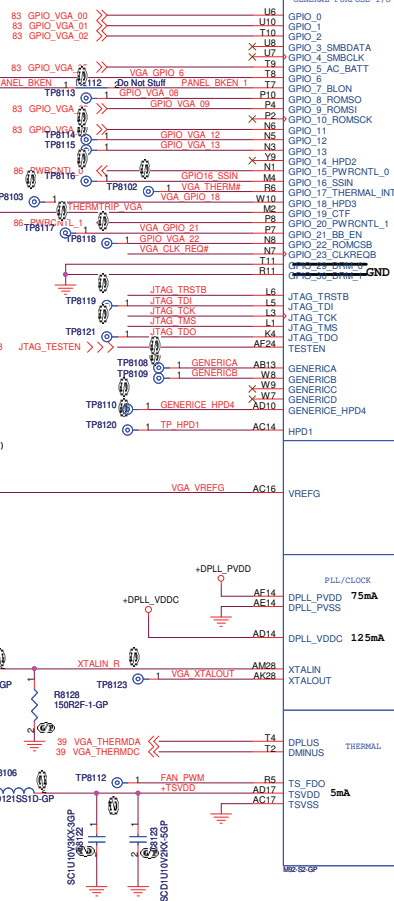
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SSID = VIDEO



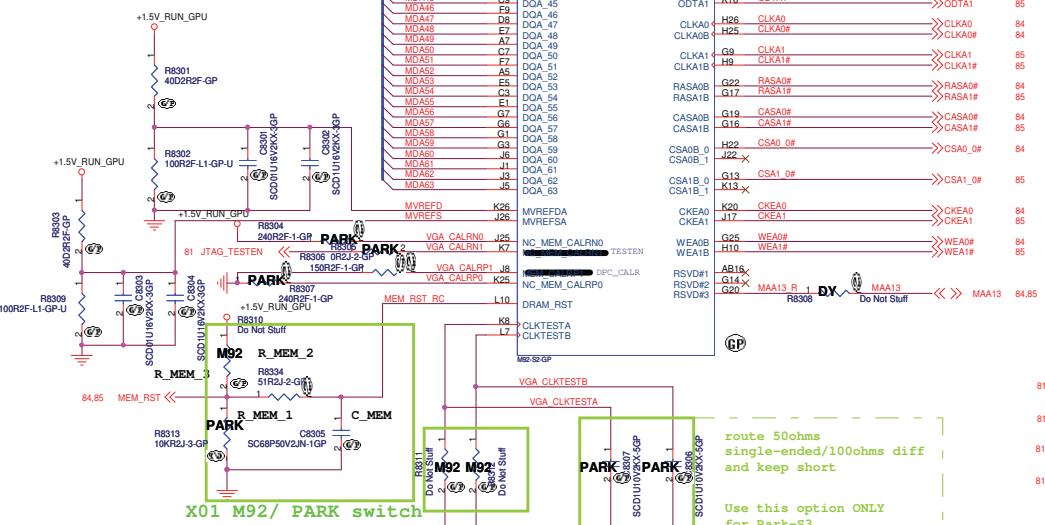
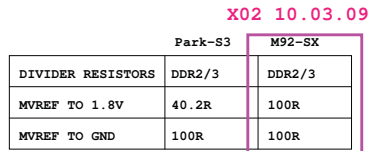
SIGNALS	Normal mode	Debug mode
JTAG_TESTEN	0	1
JTAG_TRSTB	0	1
JTAG_TCK	NC	1
JTAG_TMS	1	1



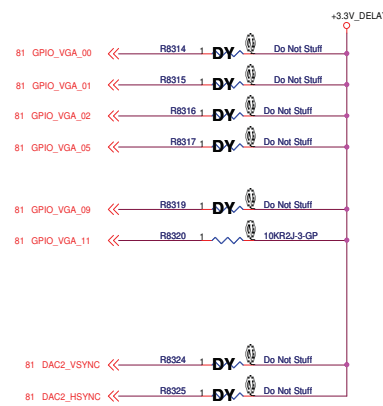
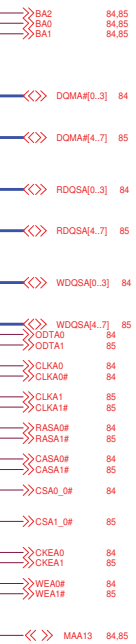
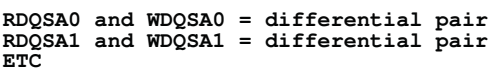


SSID = VIDEO

```
( 0.5 * VDDR1 ) ( for SSTL-1.8/SSTL-2/DDR2 )
( 0.7 * VDDR1 ) ( for GDDR3/GDDR4 )
```



Designator	For M9X-S2	For Park-S3
R_MEM_1	DNI	10K
R_MEM_2	OR/Short	51R
R_MEM_3	2.2K	DNI
C_MEM	2.2nF	68pF

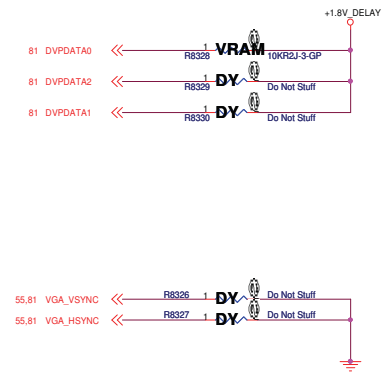


ATI RESERVED CONFIGURATION STRAPS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESE
GPI03 , H2SYNC , V2SYNC
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
128MB 256MB 64MB 32MB 512MB 1GB 2GB 4GB	x000	ST Microelectronics	M25P05A	0100
	x001		M25P10A	0101
	x010		M25P20	0101
	x		M25P40	0101
	x		M25P80	0101
	x	Chingis (formerly PMC)	Pm25LV512A	0100
	x		Pm25LV010A	0101
	x			

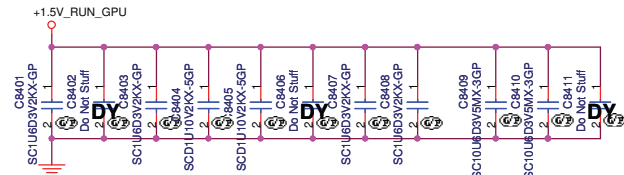
STRAPS	PIN	DESCRIPTION
TX_FWRS_ENB (Internal PD)	GPIO0	Transmitter Power Savings Enable V 0= 50% Tx output swing 1= Full Tx output swing
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable V 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled
BIF_GEN2_EN_A	GPIO2	V 0 = Advertises the PCI-E device as 2.5Gt/s 1 = Advertises the PCI-E device as 5Gt/s
BIF_CLK_PM_EN	GPIO8	V 0= Disable CLKREQ# power management capability 1= Enable CLKREQ# power management capability
ROMIDCFG[3:0] (Internal PD)	GPIO[13,12,11]	if BIOS_ROM_EN=1, then Config[3:0] defines the ROM type if BIOS_ROM_EN=0, then Config[3:0] defines the primary memory aperture size
BIOS_ROM_EN (Internal PD)	GPIO_22_ROMCSB	Enable external BIOS ROM device V 0= Disable external BIOS ROM device 1= Enable external BIOS ROM device
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] V 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI

STRAPS	PIN	DESCRIPTION
MEM_TYPE	DVPDATA(2,0) (Internal PD)	MEMORY_TYPE,MAKE AND SIZE INFO 00 - gDDR3 64Mx16 Hynix 01 - gDDR3 64Mx16 Samsung 10 - gDDR3 128Mx16 Hynix 11 - gDDR3 128Mx16 Samsung

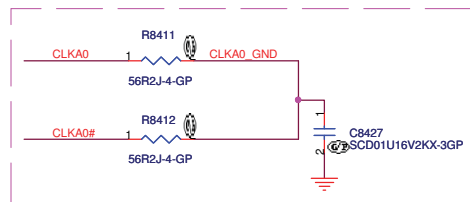
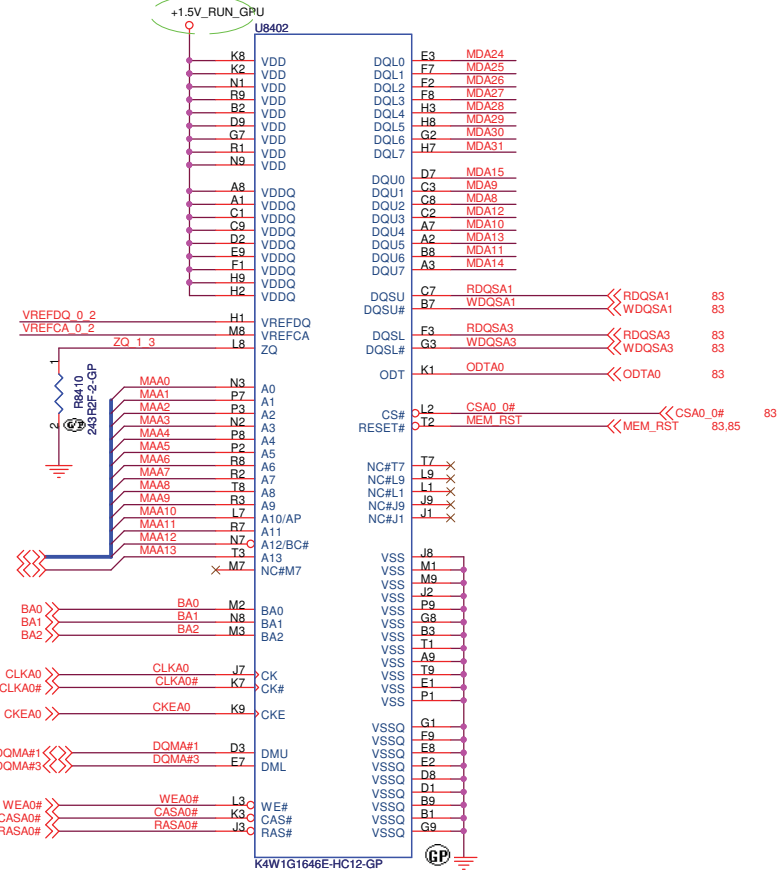
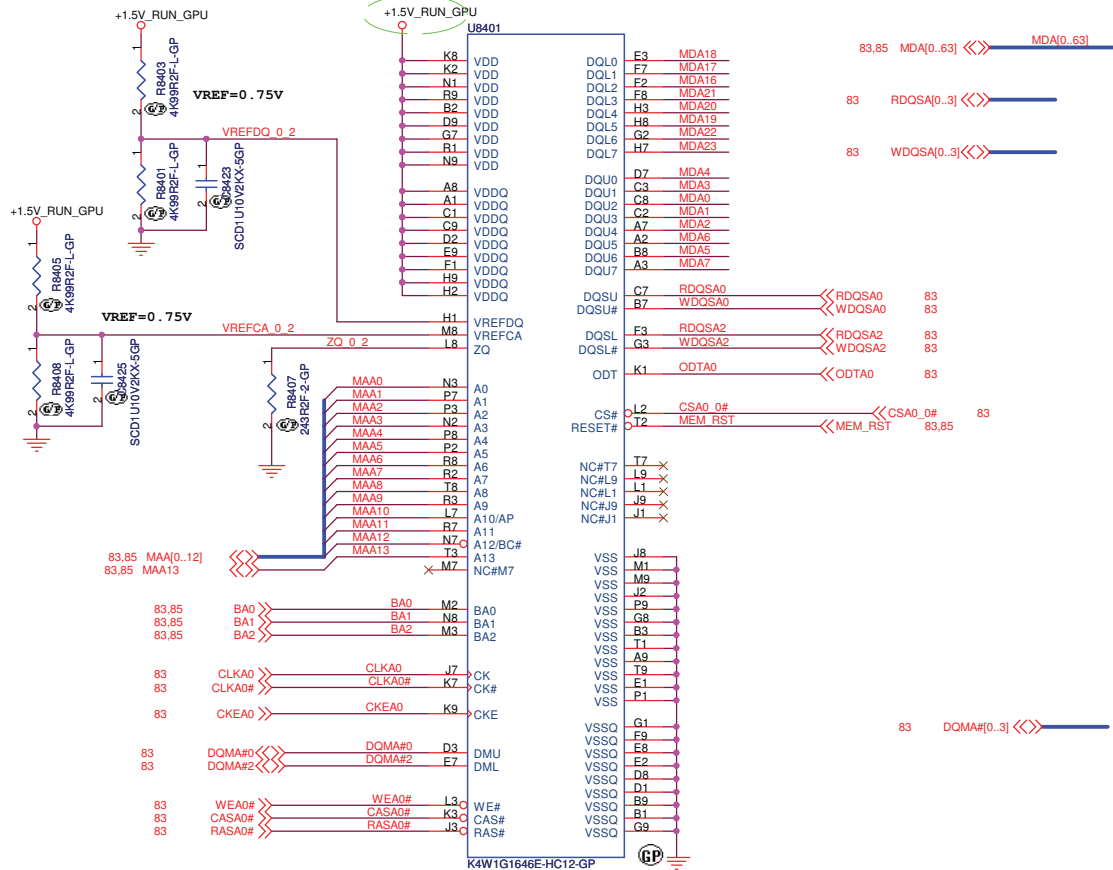
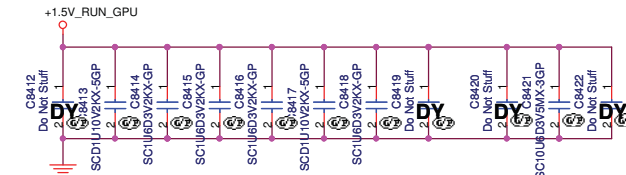


SSID = VIDEO

Place blow decoupling caps close VDD pin.



Place blow decoupling caps close VDD pin.



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Size Document Number

Custom Arsenal DJ1 Discrete

Date: Thursday, May 06, 2010

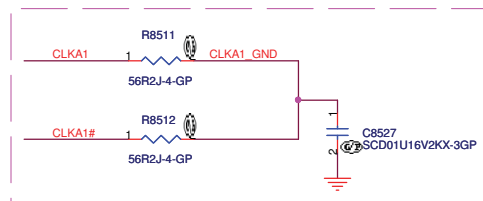
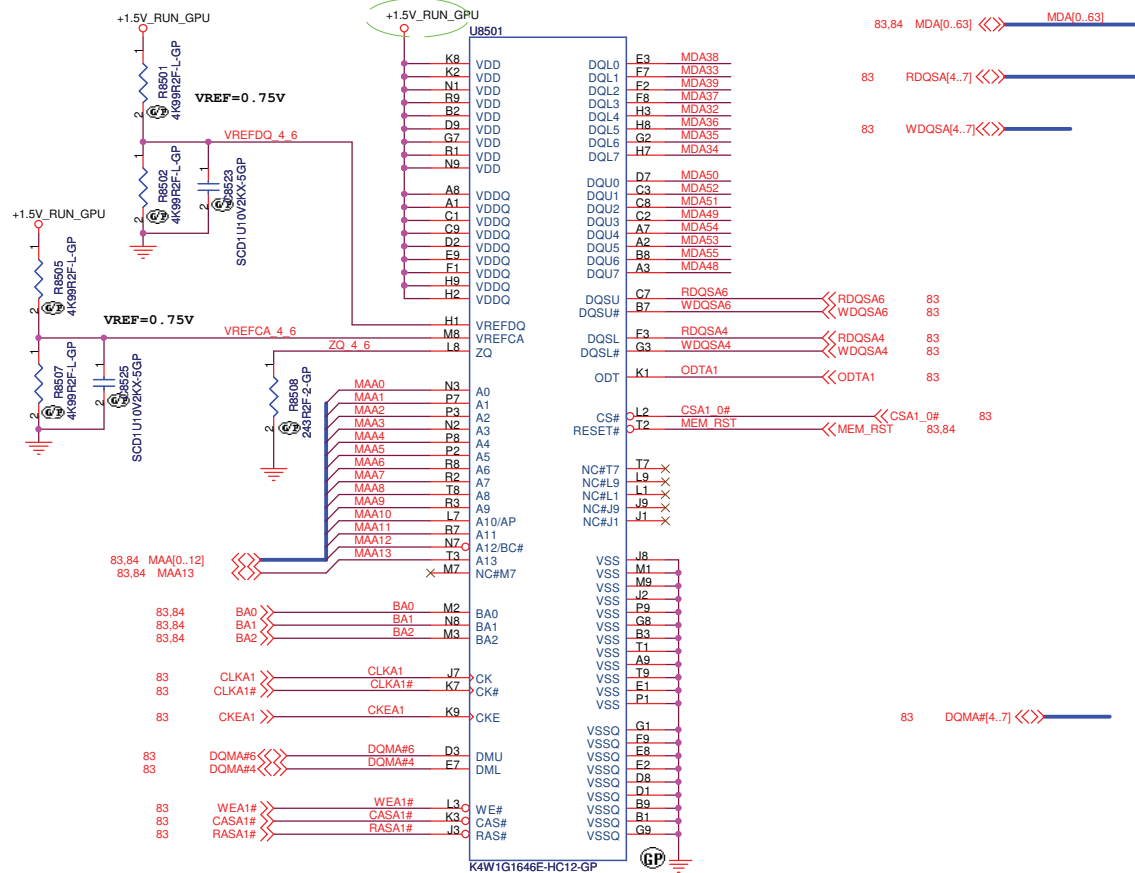
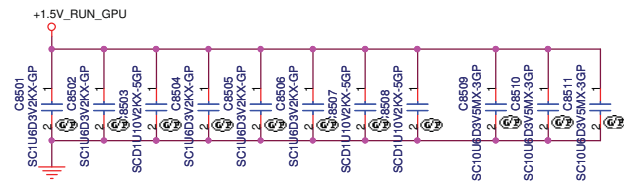
GPU-VRAM (1/2)

Rev A01

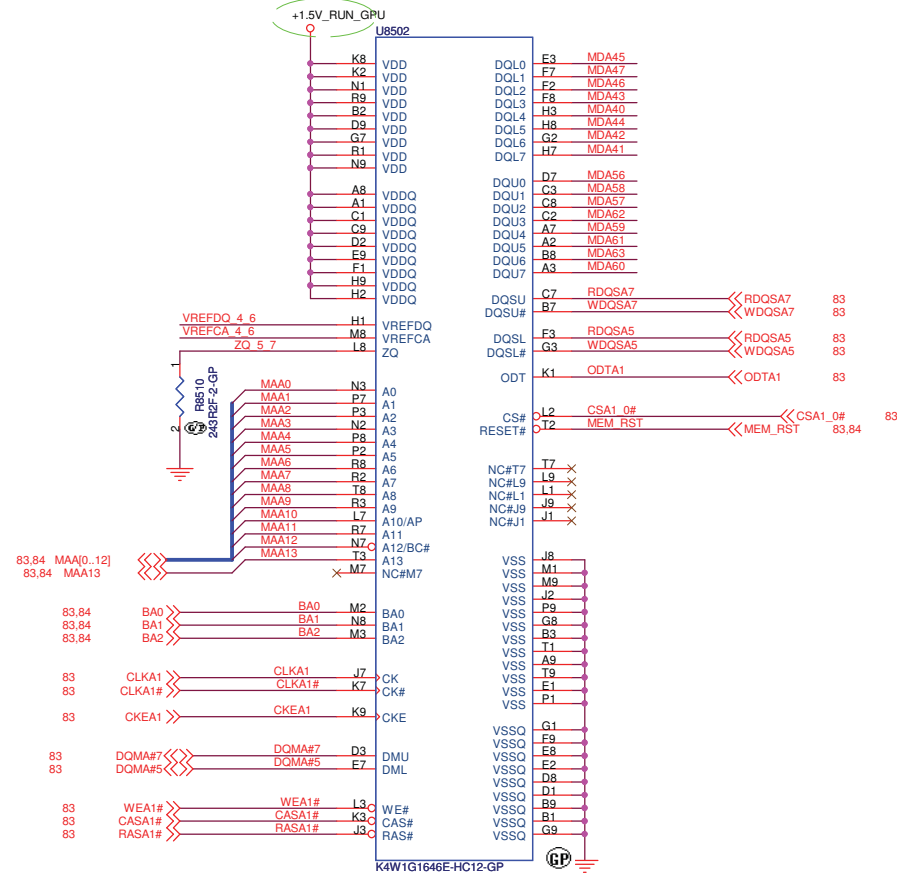
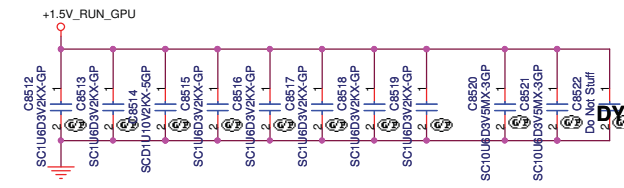
Sheet 84 of 92

SSID = VIDEO

Place blow decoupling caps close VDD pin.



Place blow decoupling caps close VDD pin.



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Title

GPU-VRAM (2/2)

Size	
Custom	

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RT8208BGQW for +VGA_CORE



PARK-LP Power-Play

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RT8208B +VGA_CORE

Arsenal DJ1 Discrete

A01

The diagram shows a circuit for providing 1.5V to an M92 module. A red line represents the 1.5V power supply, labeled "RUN ON 1.5V#" at the bottom left. This line connects to a terminal labeled "G" on the M92 module. Another terminal on the module, labeled "S", is connected to ground (indicated by a ground symbol). A third terminal, labeled "1", is connected to a power source labeled "+1.5V_RUN_GPU". A blue squiggly line, representing a resistor, connects the "1" terminal to the "G" terminal. The text "M92" and "Do Not Stuff" are printed on the module. A circular symbol with "EP" inside is also present.

Peak current: 3520mA
 Design current: 2464mA
 11.6A
 Rds=14m ohm ==> 0.04928

For Discrete +1.5V_RUN

1.5V_RUN

+1.5V_RUN_GPU

A00 10.03.29 change to 0805

R8701 1

R8702 2

U4202

M92

Do Not Stuff

C4203

C4204

Do Not Stuff

1.5V_RUN_ENABLE

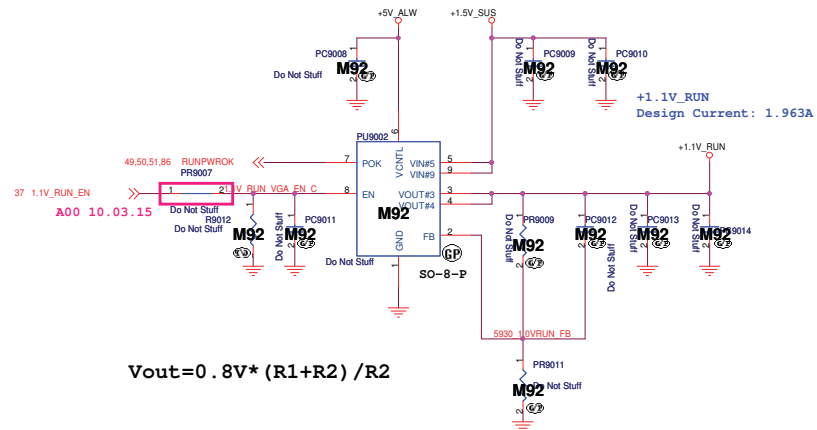
M92

Do Not Stuff

SC10U6D3V5KX-1GP

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
		Power Plane +1.05V GFX	
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APL5930KAI for +1.1V_RUN



$$V_{out} = 0.8V * (R1 + R2) / R2$$



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APL5930_+1.1V_RUN

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Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
1	47	2010/01/04	Wistron	CPU core power was two phase	Remove PC4766	
2	81 82 83	2010/01/04	Wistron	M92/ PARK switch	ADD RN8102,R8104,R8105,R8201,L8202,L8212,C8203 R8310,R8311,R8312 Connect Ball L17 to +1.5V_RUN_GPUand Ball L16 to GND	X01 X01
3	81	2010/01/04	ATI	Modify Park to Normal mode	PD R8132 to GND	X01
4	87	2010/01/04	Wistron	Derect connect +1.5V_RUN to +1.5V_RUN_GPU.	Change +1.5V_SUS power rail to +1.5V_RUN ADD R8701,R8702 NOPOP U4202,C4203,C4204,R4209,R4208 Q4203,R4215,Q4206	X01
5	80 81 82 83 84	2010/01/04	Wistron	BOM Control	PARK:POP R8003,RN8102,R8104,R8105,C8134,C8135,C8136 C8128,C8129,C8130,L8108,L8109,C8131,C8132,C8133 L8107,C82127,C82129,C82125,C82130,L8213,L8214 R8209,L8211,R8313,C8306,C8307,R8332,R8333,R8308 ,R8304,R8305,R8307,R4212 M92:POP R82011,C8203,L8202,L8212,R8310,R8311,R8312 R4211,R4213,Q4204,Q4205	X01
6	37 62	2010/01/05	Wistron	Improve BIOS data loss issue.	ADD U3702 circuit POP R6210 NOPOP R6203	X01
7	87 88	2010/01/05	Wistron	M92/Park Co-lay to use 1.1V_RUN LDO.	ADD PU9002 LDO circuit Remove U8703 MOSFET circuit	X01
8	59	2010/01/06	Wistron	Suyin ODD connect PT build SMT issue	Change to 22.10300.811	X01
9	7 46 60 79 86	2010/01/06	Wistron	EMI requirement	Pop EC7932,EC7960,EC7933,EC7928,EC7931,EC7929,EC7901 ,EC7926,PC8911,PC4610,EC7927,EC7962,EC7955,PC4616, EC7956,EC7923,EC7921,EC7902,PC4619,EC6001,EC6002, EC6003,EC6004,EC703	X01
10	62	2010/01/07	Wistron	Change RTC battery connect drawing from Coxoc to Foxconn by SMT issue	Change to 62.70001.011	X01
11	24	2010/01/07	Wistron	Schematic could not PD this pin	Packege ball name:AY3 NC	X01
12	39	2010/02/24	Wistron	T8 shutdown is set 88 deg-C.	Change R3915 to 64.28015.6DL	A00
13	37	2010/02/24	Wistron	Change MB VERSION ID and GPU table	POP R3723,R3722 NOPOP R3725 Remove R3724,R3727	A00
14	37	2010/02/24	Wistron	Power bottom delay issue	NOPOP Reset IC U3702	A00

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Title

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Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
15	32 54	2010/03/09	Wistron	EMI requirement	ADD TR3201,TR5401	A00
16	79	2010/03/09	Wistron	ME requirement	Remove HBT1	A00
17	09	2010/03/09	Wistron	S3 Power Reduction requirement	POP U927,R2114,R977 NOPOP R978	A00
18	09	2010/03/09	Wistron	DDR3_DRAMRST# drop issue	ADD C903	A00
19	79	2010/03/09	Wistron	Change page83 DIVIDER RESISTORS table		A00
20	37	2010/03/15	Wistron	Support RCID function schematic when pop Q3706	ADD Q3706	A00
21	46	2010/03/15	Wistron	Operation Mode Select to Diode Emulation Mode	POP PR4619 NOPOP PR4618	A00
22	79	2010/03/15 2010/05/03	Wistron	EMI requirement	Reserve Pad C7901,C7902,C7903	A00
23	54	2010/03/15	Wistron	LCD VDD power	ADD C5412 ,change C5410 from 0.1uf to 1uf	A00
24	46 47 50 88	2010/03/16	Wistron	Change 0 ohm to short pad	R2114,R4218,PR4620,PR4616,PR4619,PR4706, PR4708, PR4713, PR4718, PR4722,PR4732, PR4738, PR4744, PR4755, PR4764, PR4704,PR4703, PR4707, PR4711, PR4784,PR4790, PR4784,PR4776,PR5002,PR9007,R3751	A00
25	47 49 50 89	2010/03/16	Wistron	change to 2.7Kohm for CPU_CORE load/line setting. change to 1.4Kohm for CPU_CORE OCP setting. change to 1ohm for boost resister. change to 73.2Kohm for 1.05V OCP setting. change to 8.2Kohm for 1.5V OCP setting. change to 8.45Kohm for VGA_CORE OCP setting.	PR4705 change to 2.7Kohm PR4727 change to 1.4Kohm PR4901 change to 1ohm PR4902 change to 73.2Kohm PR5007 change to 8.2Kohm . PR8905 change to 8.45Kohm	A00
26	46 48 49 50 86	2010/03/16	Wistron	Power requirement	Change PL4814,PL4817 from 68.R3610.10M to 68.R3610.10T Change PL4602 from 68.2R21B.10A to 68.2R210.20Q Change PL8601 from 68.2R210.20B to 68.2R210.20Q Change PL4601 from 68.3R31A.10W to 68.3R310.20I Change PTC4602 from 77.23371.12L to 77.C2271.00L Change from 68.R5610.10D to 68.R5610.20I Change PL5001 from 68.1R510.10J to 68.1R510.20I	A00
27	63	2010/03/17	Wistron	USB Enable pin signal issue remove UPI vendor	Change U6302,U6301 to GMT symbo	A00
28	42	2010/03/17	Wistron	Change symbo from VISHAY to AOL	Modify U4204	A00
29	48 49 50	2010/03/18	Wistron	Power requirement	Change PQ4840 PQ4833 PU4902 PU5003 from 84.07686.A37 to 84.07686.037	A00
30	12 18 19	2010/03/24	Wistron	PSE issue,Layout routing	Remove C1219,C1211,C1803,C1804, C1809,C1905,C1911,C1912DISCRETE PARK	A00
31	09	2010/03/25	Wistron	XDP1 change to ZZ.00PAD.Q81	 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. Title Change History Size A3 Document Number Arsenal DJ1 Discrete Rev A01 Date: Thursday, May 06, 2010 Sheet 90 of 92	

Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
32	79	2010/05/03	Wistron	EMI requirement	POP C7901,C7902,C7903,C7904,C7905,R7901,R7902,R7903,R7904,R7905,R7906,R7910	A01

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Change History

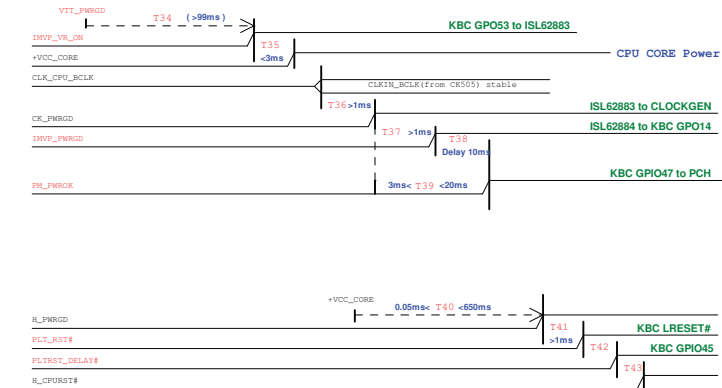
Arsenal DJ1 Discrete

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(AC mode)

red word: KBC GPIO



(DC mode)

red word: KBC GPIO

