

GM/PM45 Block Diagram

<http://hobi-elektronika.net>

Project code:

PCB P/N : 08124

REVISION : -1 2008/12/18

Database: XX.XXXXX.XXX

Database PCB:

Revision:

PCB STACKUP 8L

TOP _____
GND/PWR _____
L3-signal _____
PWR _____
GND/PWR _____
L6-signal _____
GND _____
BOTTOM _____

SYSTEM DC/DC
TPS51120 43

INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5
SYSTEM DC/DC TPS51124 44	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 1D05V_S0

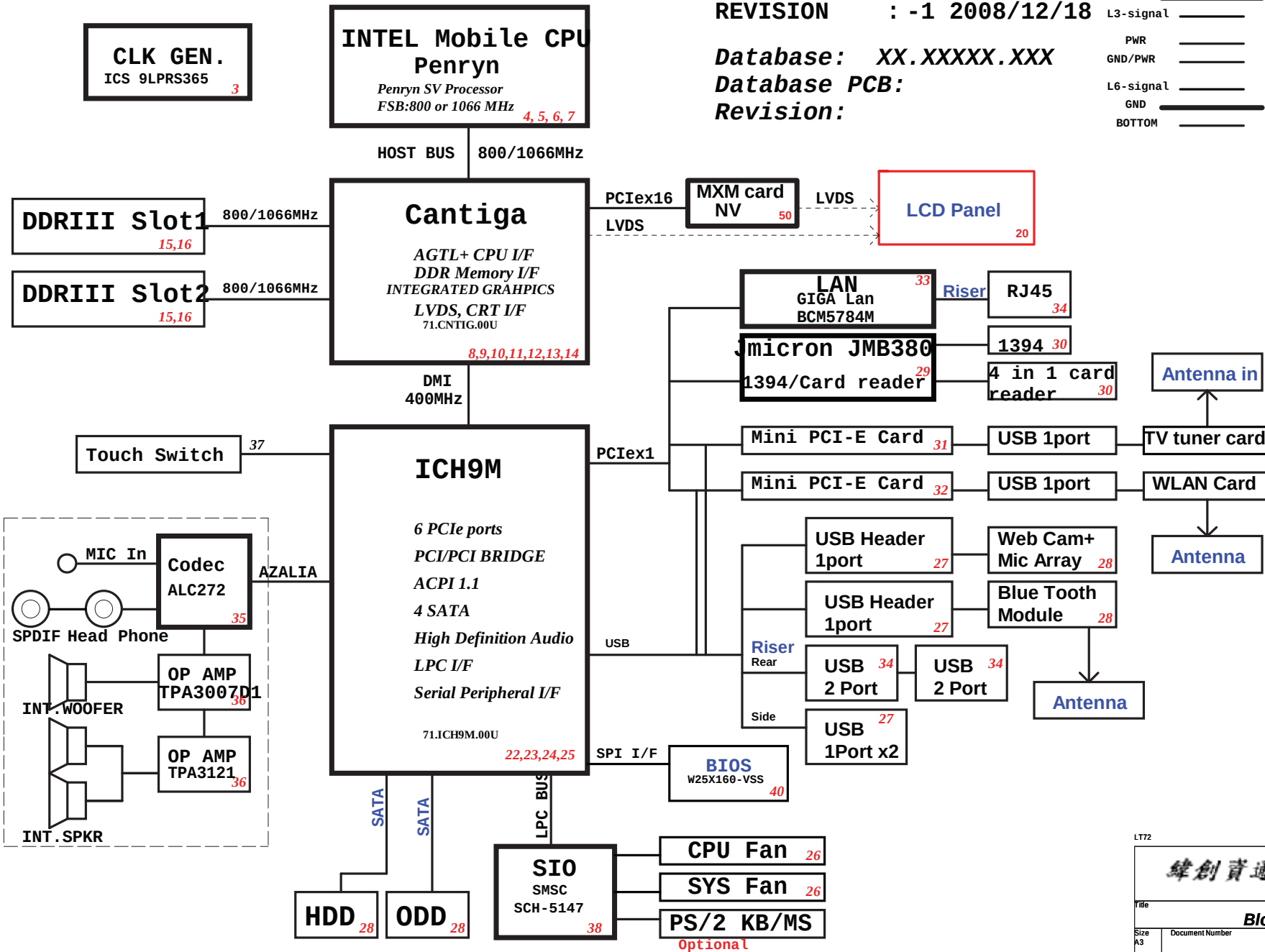
CPU DC/DC
ADP3208A 46

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

LT72

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Block Diagram		
Size A3	Document Number Bali	Rev -1
Date: Friday, February 13, 2009	Sheet 1 of 52	



A ICH9M

PIN NAME	POWER WELL	USAGE	AFTER PLTRST	Notes	PIH&PID	Default value
GP100	MAIN		GPI			High
GP101	MAIN	LPC_SM*	GPI	Input LPC DR Event Input (Low active)		High
GP102	MAIN	IRQE*	GPI			High
GP103	MAIN	IRQFI*	GPI			High
GP104	MAIN	IRQGI*	GPI			High
GP105	MAIN	IRQHI*	GPI			High
GP106	MAIN	Touch_INT_SB	GPI	H Normal, L Enable		High
GP107	MAIN	CDR_REFECT_SB	GPI	H Normal, L Enable	CDR_REFECT_TOUCH	High
GP108	RESUME		GPO			High
GP109	RESUME	NO	Native(WOL_EN)	check		High
GP110	RESUME	NO	GPI			High
GP111	RESUME	OCPI#	Native(SMBALERT#)			High
GP112	RESUME	NO	GPO			Low
GP113	RESUME	NO	GPI			High
GP114	RESUME	NO	GPI			High
GP115	---	---	---	---	---	---
GP116	MAIN	DPRSLP_VR	Native(DPRSLP_VR)	H Enable Internal PD 20k		Low
GP117	MAIN		GPI			High
GP118	MAIN		GPO	H Enable		High
GP119	MAIN	Wireless LAN_EN	GPO			High
GP120	MAIN		GPO	Internal PD 20k (CarrPU)		High
GP121	MAIN		GPO			High
GP122	MAIN	TV_EN	OD			High
GP123	MAIN	NO	Native(DRQ1#)	Internal PD 20k		High
GP124	RESUME		GPI			Low
GP125	---	---	---	---	---	---
GP126	RESUME					Low
GP127	RESUME		GPO			Low
GP128	RESUME		GPO			Low
GP129	RESUME	OC'45	Native(OC'45)			High
GP130	RESUME	OC'6	Native(OC'6)			High
GP131	RESUME	OC'7	Native(OC'7)			High
GP132	---	---	---	---	---	---
GP133	HDA_DOCK_EN#		GPO	Internal PU 20k		High
GP134	MAIN	NO	GPO			Low
GP135	MAIN		GPO			Low
GP136	MAIN	MMX_DET	GPI	H: no MMX, L: MMX on		High
GP137	MAIN	USB_CHR_EN	OD	CAMERA_EN L Enable		High
GP138	MAIN	PCB_VERR1	OD			High
GP139	MAIN	PCB_VERR1	OD			High
GP140	RESUME	OC'01	Native(OC'01)			High
GP141	RESUME	OC'23	Native(OC'23)			High
GP142	RESUME	OC'23	Native(OC'3#)			High
GP143	RESUME	OC'45	Native(OC'4#)			High
GP144	RESUME	OC'8	Native(OC'8#)			High
GP145	RESUME	OC'9	Native(OC'9#)			High
GP146	RESUME	OC'10	Native(OC'10#)			High
GP147	RESUME	OC'11	Native(OC'11#)			High
GP148	MAIN	PCB_VERR2	GPI			High
GP149	MAIN	SB_INVERTER_EN#	GPO	Teemahr NC Cantiga chipset Internal PU 20k		High
GP150	MAIN	(REQ1#)	Native(REQ1#)			High
GP151	MAIN	NO (GNT1#)	Native(GNT1#)	Internal PU 20k		High
GP152	MAIN	(REQ2#)	Native(REQ2#)			High
GP153	MAIN	NO (GNT2#)	Native(GNT2#)	Internal PU 20k		High
GP154	MAIN	(REQ3#)	Native(REQ3#)			High
GP155	MAIN	NO (GNT3#)	Native(GNT3#)	Internal PU 20k		High
GP156	RESUME	NO	GPI			Low
GP157	RESUME	CMOS_IN	GPI	-1A add		High
GP158	RESUME	NO	GPI	Internal PU 20k		High
GP159	RESUME	OC'01	Native(OC'0#)			High
GP160	RESUME	NO	Native(WOLALERT#)			Low
GP161						
GP162						
GP163						

B

SCH 5147

GPIO #	Usage	Power Well	IO Mode	IO Direction	IO Level	IO Pull-up	IO Pull-down	IO Tri-state	IO Open-drain	IO Schmitt	IO Hysteresis	IO Debounce
GP10	GPIO	MAIN	N/A	MAIN (VCC)								
GP11	GPIO	MAIN	N/A	AUX (VTR)								
GP12	GPIO	MAIN	N/A	AUX (VTR)								
GP13	GPIO	MAIN	N/A	AUX (VTR)								
GP14	GPIO	MAIN	N/A	AUX (VTR)								
GP15	Thermal Trip	MAIN	N/A	MAIN (VCC)								
GP16		MAIN	N/A	AUX (VTR)								
GP17		MAIN	N/A	AUX (VTR)								
GP20		MAIN	AUX (VTR)	MAIN (VCC)								
GP21	KB	MAIN	AUX (VTR)	MAIN (VCC)								
GP22	KB	MAIN	AUX (VTR)	MAIN (VCC)								
GP27	MS	MAIN	AUX (VTR)	AUX (VTR)								
GP32	MS	MAIN	AUX (VTR)	MAIN (VCC)								
GP33	MS	MAIN	AUX (VTR)	MAIN (VCC)								
GP36		MAIN	AUX (VTR)	MAIN (VCC)								
GP37		MAIN	AUX (VTR)	MAIN (VCC)								
GP40		MAIN	AUX (VTR)	AUX (VTR)								
GP41		MAIN	AUX (VTR)	AUX (VTR)								
GP42		MAIN	AUX (VTR)	AUX (VTR)								
GP43		MAIN	AUX (VTR)	MAIN (VCC)								
GP50		MAIN	AUX (VTR)	AUX (VTR)								
GP51		MAIN	AUX (VTR)	AUX (VTR)								
GP52	Dual Core/Qual Core	MAIN	AUX (VTR)	AUX (VTR)								
GP53		MAIN	AUX (VTR)	AUX (VTR)								
GP54		MAIN	AUX (VTR)	AUX (VTR)								
GP55		MAIN	AUX (VTR)	AUX (VTR)								
GP56		MAIN	AUX (VTR)	AUX (VTR)								
GP57		MAIN	AUX (VTR)	AUX (VTR)								
GP60		MAIN	AUX (VTR)	AUX (VTR)								
GP61		MAIN	AUX (VTR)	AUX (VTR)								

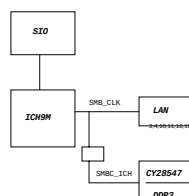
PCI Routing

no	IOSEL	INT	REQ	OUT
0	no	no	no	no

PCIe Routing

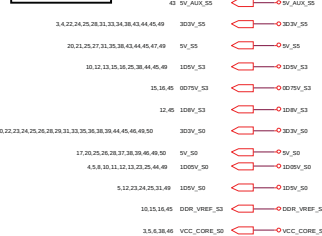
LANE1	Lan
LANE2	MINICRON380
LANE3	MiniCard TV
LANE4	MiniCard WLAN

SMBus



USB Table

Pair	Device
0	USB0
1	USB1
2	USB2
3	USB3
4	USB4
5	USB5
6	WIRELESS
7	BT
8	CAMERA
9	miniPCI-E
10	miniPCI-E
11	miniPCI-E



C

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D

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5

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Signal	Usage/When Sampled	Comment
HDA_SDOOT	XOR Chain Entrance PCI Port Config bit1, Rising Edge of PWOK	Allow entrance to XOR Chain testing when TP3 pulled low when TP3 not pulled low at rising edge of PWOK, sets bit1 of MPC_PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCI config bit10, Rising Edge of PWOK	This signal has a weak internal pull-down. Sets bit0 of MPC_PC(Config Registers: offset 224h)
GN2#/GP103	PCI config bit2, Rising Edge of PWOK	This signal has a weak internal pull-up. Sets bit2 of MPC_PC(Config Registers: offset 224h)
GP102	Reserved	This signal should not be pulled high.
GP17#/GP105	ES1 Strap (Server only) Rising Edge of PWOK	ES1 compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GN2#/GP105	Top-Block Swap override. Rising Edge of PWOK	Sampled low: Top-Block Swap mode (inverts A16 for all cycles targeting PMM BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GN2# being pulled down.
GN2#/SPT_C51#/SPT_C51#/SPT_C51#	Boot BIOS Destination Selection 0:1. Rising Edge of PWOK	Controlable via Boot BIOS Destination bit (Config Registers: offset 3410h: bit 11:10). GN2# is HIGH, SPT_C51# is LOW.
SPT_MOSI	Sample low: the integrated TPM will be disabled. Sample high: the HCN TPM enable strap is sampled low and the TPM disable bit is clear, the integrated TPM will be enable.	
GP1049	DMA Termination Voltage, Rising Edge of PWOK	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal, Rising Edge of PWOK	Signal has weak internal pull-up. Sets bit 27 of MPC_LR(device 28: Function 9: Offset 08)
SPKR	No Reboot. Rising Edge of PWOK	If sampled high, the system is strapped to the "No Reboot" mode (ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWOK	This signal should not be pulled low unless using XOR Chain testing.
GP103#/HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWOK	Sampled low: the Flash Descriptor Security will be overridden. If high, the security measures will be in effect. This should only be enabled in manufacturing environments using an external pull-up resistor.

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5

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Pin Name	Strap Description	Configuration
CF6[2:0]	FSB Frequency Select	000 = FSB667 011 = FSB667 010 = FSB800 Others = Reserved
ZF6[4:3] ZF5 ZF6[15:14] ZF6[18:17]	Reserved	
CF65	DMI x2 Select	0 = DMI x2 1 = DMI x4 (default)
CF66	ITPM Host Interface	0 = The ITPM Host Interface is enabled (note2) 1 = The ITPM Host Interface is disabled (default)
CF67	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher 1 = TLS cipher (default)
CF69	PCI Express Lane	0 = Reverse Lanes, 15-9, 14-5, etc... 1 = Normal operation (default); Lane Numbered in order
CF610	PCI Express Loopback enable	0 = Enable (note 3) 1 = Disabled (default)
CF6[13:12]	XOR/ALL	00 = Reserve 01 = XOR mode Enabled 10 = ALL2 mode Enabled (Note 3) 11 = Disabled (default)
CF616	FSB dynamic GDT	0 = Dynamic GDT Disabled 1 = Dynamic GDT Enabled (default)
CF619	DMI Lane Reversal	0 = Normal operation (default); Lane Numbered in order 1 = Reverse Lanes
CF620	Digital Display Port (SDVO/DP/HDMI) Concurrent with PCIe	0 = Only Digital Display Port 1 = SDVO/DP/HDMI (default); operating simultaneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 = SDVO Card Present (default) 1 = SDVO Card Present
check_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (default) 1 = LFP Card Present; PCIe disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (UPXN Power OR PWOK) signal.
2. ITPM can be disabled by a 'Soft-Strap' option in the Flash-Descriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling ITPM via CF66.
Only one of the CF618/CF612/CF613 straps can be enabled at any time.

E

ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 355845 Rev. 2.2

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SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST#	PULL-UP 15K
DPRSLPVR/GP1016	PULL-DOWN 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GP1033	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_S0IN[3:0]	PULL-DOWN 20K
HDA_SDOOT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]/GP10[50,53,51]	PULL-UP 20K
GP10[20]	PULL-DOWN 20K
GP10[49]	PULL-UP 20K
LDA[3:0]/FWM[3:0]	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GP1023	PULL-UP 20K
PMEN	PULL-UP 20K
PMWRTN	PULL-UP 20K
SATALED#	PULL-UP 15K
SPT_C51#/GP1038/CLP106	PULL-UP 20K
SPKR	PULL-DOWN 20K
SPT_MOSI	PULL-UP 20K
TACH [3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

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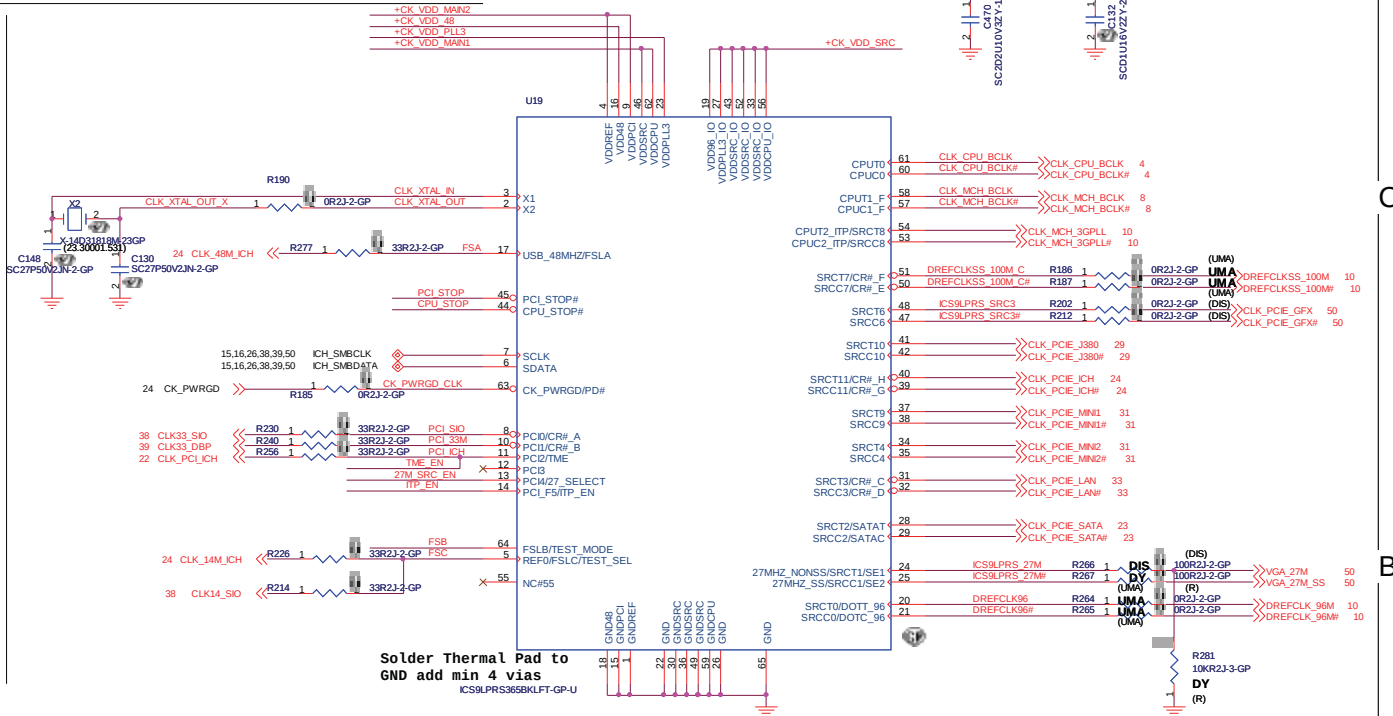
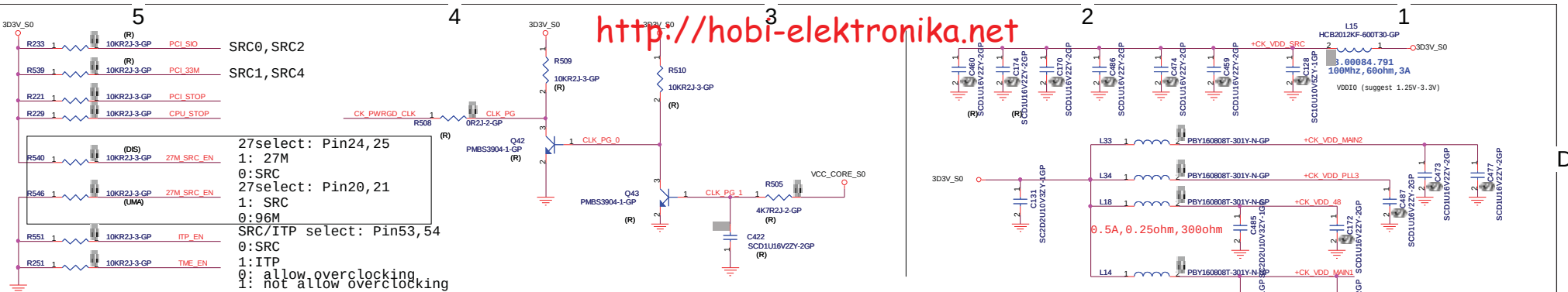
A

B

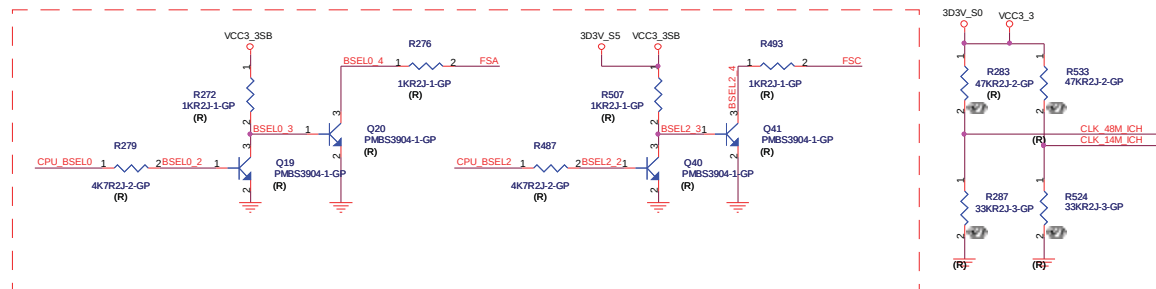
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D

E



For wireless performance



F _{3,5} C	F _{3,5} H	F _{3,5} A	CPH	50C	PCJ	COJ	50K	100K
RD	RD	RD	[M/s]	[M/s]	[M/s]	[M/s]	[M/s]	[M/s]
0	0	0	286.66	100.30	33.33	90.00	34.318	48.00
0	0	1	133.33	100.30	33.33	90.00	34.318	48.00
0	0	2	290.00	100.30	33.33	90.00	34.318	48.00
0	0	3	196.66	100.30	33.33	90.00	34.318	48.00
1	0	0	330.33	100.30	33.33	90.00	34.318	48.00
1	0	1	190.00	100.30	33.33	90.00	34.318	48.00
1	0	2	436.00	100.30	33.33	90.00	34.318	48.00
1	1	0	290.00	100.30	33.33	90.00	34.318	48.00

 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
<i>Clock generator ICS-9LPRS365</i>			
Size Custom	Document Number		Rev
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Date	First Rev	Sheet	of
2000/03/13	1	3	3

5

4

3

2

1

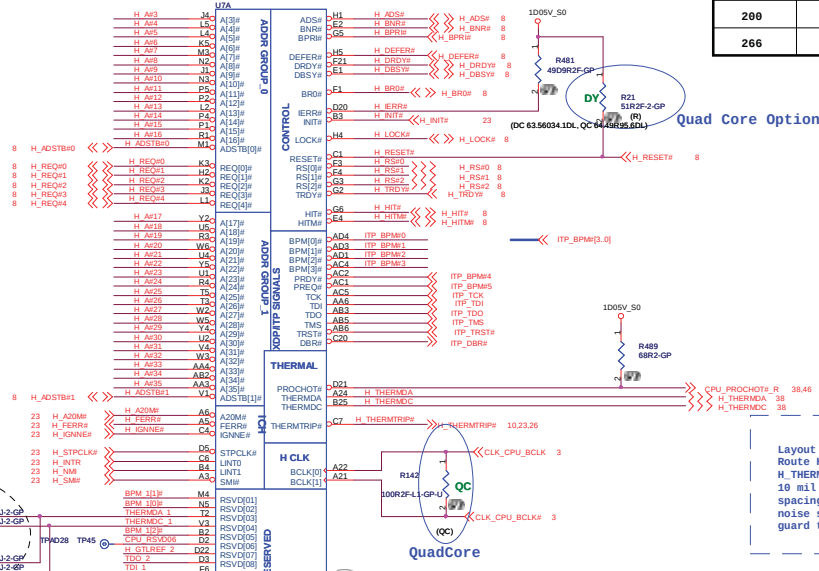
H_A0[3:5] <<<

SB 8/6 Layout Lib
62.10079.001=>
(Old) BGA479-SKT-9-U1H199
(New) BGA479-SKT-9-U2H293

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CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

H_D0[6:5] <<<



Layout Note:
Route H_THERMA and
H_THERMC on same layer w/
10 mil trace & 10 mil
spacing. Route away from
noise sources with ground
guard tracks on each side.

-1 CPU socket change to 62.10053.571

QuadCore

XDP FOR QUAD CORE CPU

Need check!!

R462: Use 1.91K
in Topology2,
1.74K for
Topology1.

QuadCore

CPU	F8
DC	GND
QC	Floating

Layout note:
Comp0,2 connect with Z0=27.4ohm, make
trace length shorter than 0.5".
Comp1,3 connect with Z0=55ohm, make
trace length shorter than 0.5".

CPU	Auto Detect
DC	3D3V_S5
QC	GND

Need check!!

1686D Truth Value Table		
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

CPU_CONT	KBC
1	RSRMRST# KEEP LOW AND POWER LED FLASH
0	RSRMRST# AND POWER LED NORMALLY

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu,
Taipei Hsinchu 301, Taiwan, R.O.C.

Penryn(I13)-AGTL+/XDP

Rev -1

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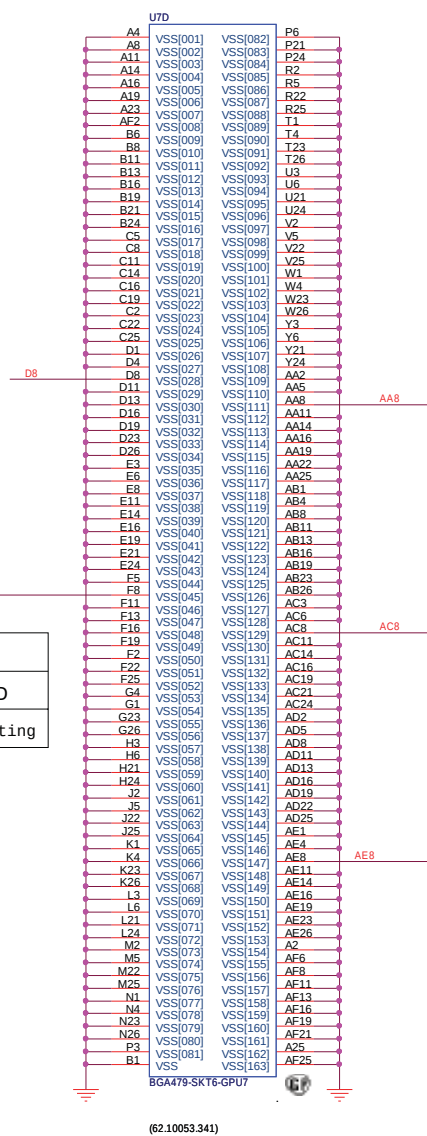
5

4

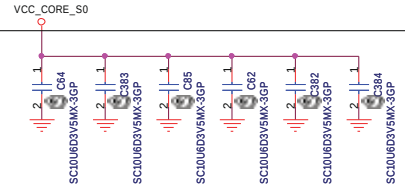
3

2

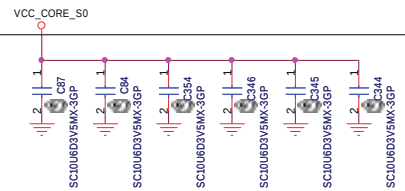
1



Place these capacitors on L1
(North side ,Secondary Layer)

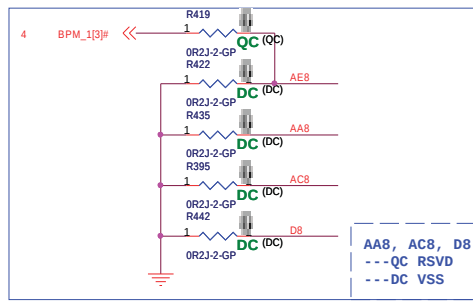
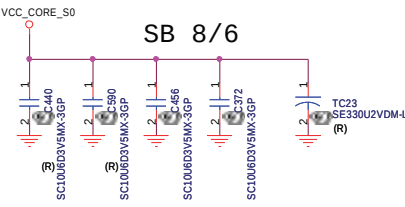
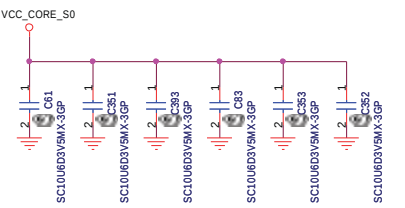
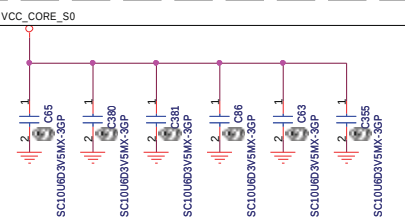


Place these capacitors on L1
(North side ,Secondary Layer)



Mid Freqenced
Decoupling

Place these capacitors on L1
(North side ,Secondary Layer)



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ITP Connector

Remove

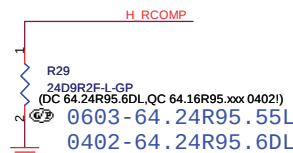
LT72

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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Penryn(3/3)-GND&Bypass			
Size	Document Number		Rev
B	Bali		SA
Date: Friday, February 13, 2009		Sheet 7	of 52



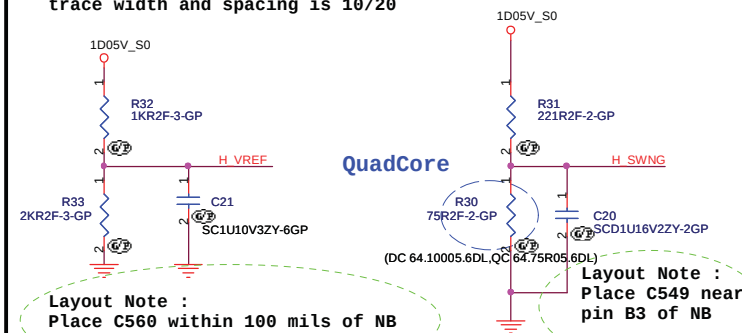
Layout note:
Trace should be 10-mil wide
with 20-mil spacing

QuadCore



check Quade core only or not?

Layout Note :
H_RCOMP / H_VREF / H_SWNG
trace width and spacing is 10/20



-check Quade core only or not?

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HOST

Signal	AD9288 Pin	AD9288 Pin Name
H SWNG	C5	H_SWING
H RCOMP	E3	H_RCOMP
H_RESET#	C12	H_CPURST#
H_CPUSLP#	E11	H_CPUSLP#
H VREF	A11	H_AVREF
	B11	H_DVREF

1 OF 2				
H_AH_3	A14	H_A#3		H_AH#3.3
H_AH_4	C15	H_A#4		
H_AH_5	F16	H_A#5		
H_AH_6	H13	H_A#6		
H_AH_7	C18	H_A#7		
H_AH_8	M16	H_A#8		
H_AH_9	J13	H_A#9		
H_AH_10	P16	H_A#10		
H_AH_11	R16	H_A#11		
H_AH_12	N17	H_A#12		
H_AH_13	M13	H_A#13		
H_AH_14	E17	H_A#14		
H_AH_15	P17	H_A#15		
H_AH_16	E17	H_A#16		
H_AH_17	G20	H_A#17		
H_AH_18	B19	H_A#18		
H_AH_19	J16	H_A#19		
H_AH_20	E20	H_A#20		
H_AH_21	H16	H_A#21		
H_AH_22	J20	H_A#22		
H_AH_23	L17	H_A#23		
H_AH_24	A17	H_A#24		
H_AH_25	B17	H_A#25		
H_AH_26	L16	H_A#26		
H_AH_27	C21	H_A#27		
H_AH_28	J17	H_A#28		
H_AH_29	H20	H_A#29		
H_AH_30	B18	H_A#30		
H_AH_31	K17	H_A#31		
H_AH_32	B20	H_A#32		
H_AH_33	F21	H_A#33		
H_AH_34	K21	H_A#34		
H_AH_35	L20	H_A#35		
H_ADS#	H12	H_ADS#		H_ADS# 4
H_ADSB#0	B16	H_ADSB#0		H_ADSB#0 4
H_ADSB#1	G17	H_ADSB#1		H_ADSB#1 4
H_BNR#	A9	H_BNR#		H_BNR# 4
H_BPRI#	F11	H_BPRI#		H_BPRI# 4
H_BRO#	G12	H_BRO#		H_BRO# 4
H_DEFER#	E9	H_DEFER#		H_DEFER# 4
H_DBSY#	AH7	CLK MCH BCLK		H_DBSY# 4
HPLL_CLK#	AHE	CLK MCH BCLK#		CLK MCH BCLK 3
HPLL_CLK#	J11	H_DPWR#		CLK MCH BCLK# 3
H_DPWR#	F9	H_DRDY#		H_DPWR# 4
H_DRDY#	H9	H_HIT#		H_DRDY# 4
H_HIT#	E12	H_HITM#		H_HIT# 4
H_HITM#	H11	H_LOCK#		H_HITM# 4
H_LOCK#	C9	H_LOCK#		H_LOCK# 4
H_TRDY#		H_TRDY#		H_TRDY# 4
H_DIN#V0	J8	H_DIN#V0		H_DIN#V0 4
H_DIN#V1	L3	H_DIN#V1		H_DIN#V1 4
H_DIN#V2	Y13	H_DIN#V2		H_DIN#V2 4
H_DIN#V3	Y1	H_DIN#V3		H_DIN#V3 4
H_DSTBN#0	L10	H_DSTBN#0		H_DSTBN#0 4
H_DSTBN#1	M7	H_DSTBN#1		H_DSTBN#1 4
H_DSTBN#2	AA5	H_DSTBN#2		H_DSTBN#2 4
H_DSTBN#3	AE6	H_DSTBN#3		H_DSTBN#3 4
H_DSTBP#0	L9	H_DSTBP#0		H_DSTBP#0 4
H_DSTBP#1	M8	H_DSTBP#1		H_DSTBP#1 4
H_DSTBP#2	AA6	H_DSTBP#2		H_DSTBP#2 4
H_DSTBP#3	AE5	H_DSTBP#3		H_DSTBP#3 4
H_REQ#0	B15	H_REQ#0		H_REQ#0 4
H_REQ#1	F13	H_REQ#1		H_REQ#1 4
H_REQ#2	B13	H_REQ#2		H_REQ#2 4
H_REQ#3	B14	H_REQ#3		H_REQ#3 4
H_REQ#4		H_REQ#4		H_REQ#4 4
H_RS#0	B6	H_RS#0		H_RS#0 4
H_RS#1	F12	H_RS#1		H_RS#1 4
H_RS#2	C8	H_RS#2		H_RS#2 4

CANTIGA-GM-GP-U-NF
(71.0GM47.00U)

緯創資通

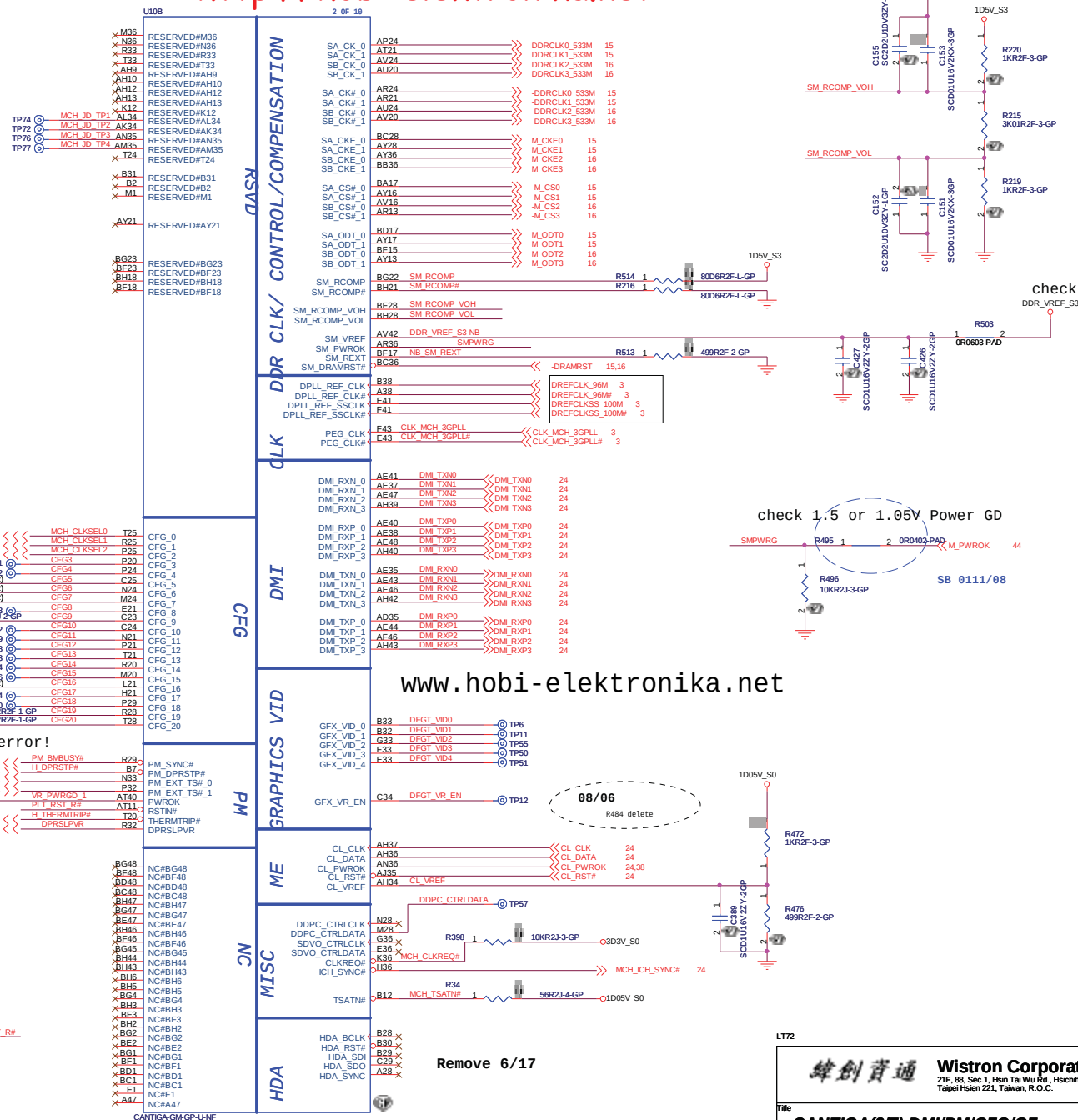
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

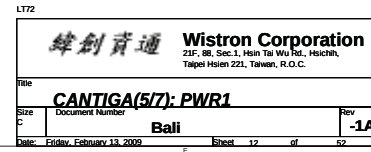
Title	CANTIGA(1/7): HOST I/F
-------	-------------------------------

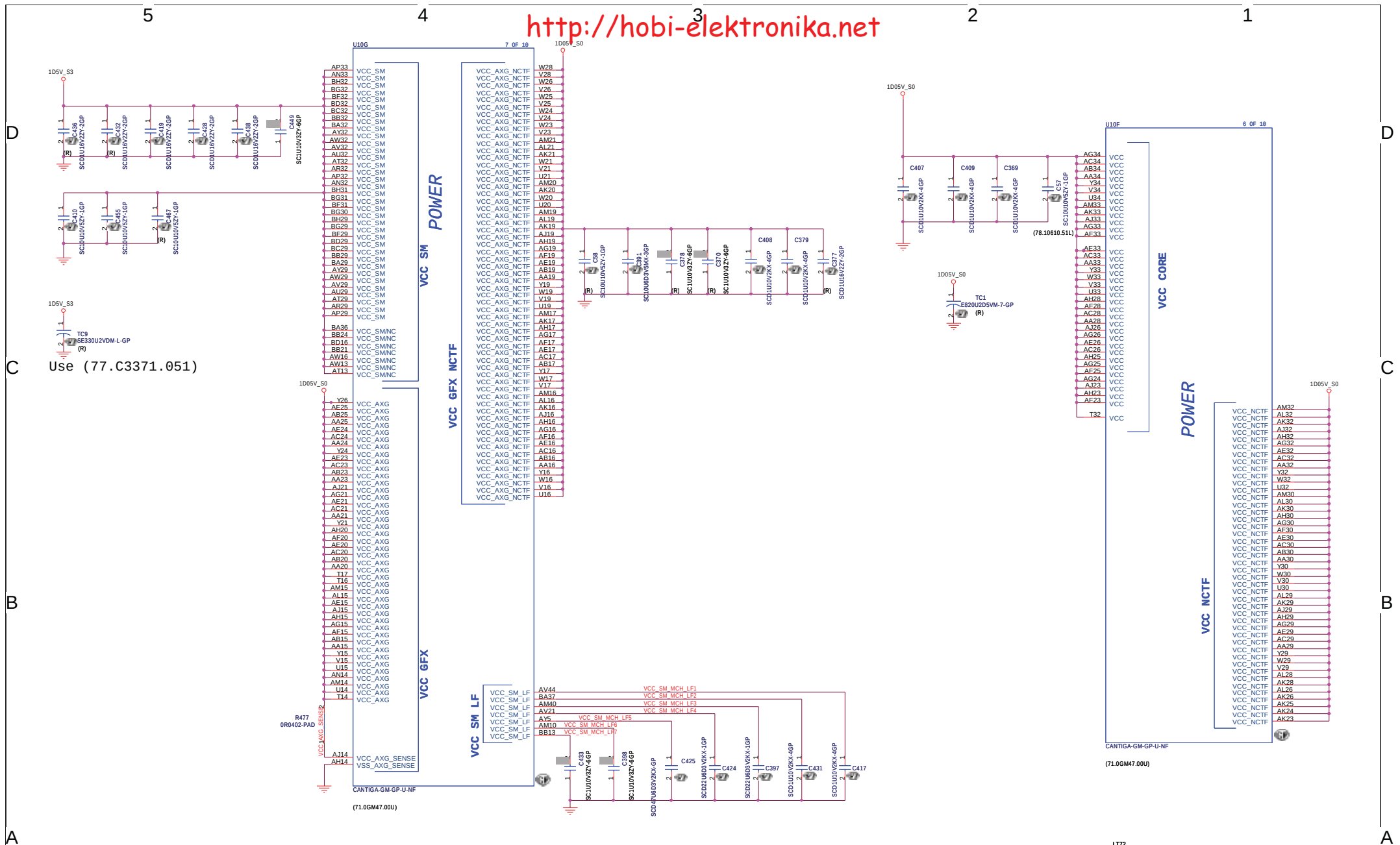
Size B	Document Number Bali	Rev -1
Date: Friday, February 13, 2009	Sheet 8 of	52



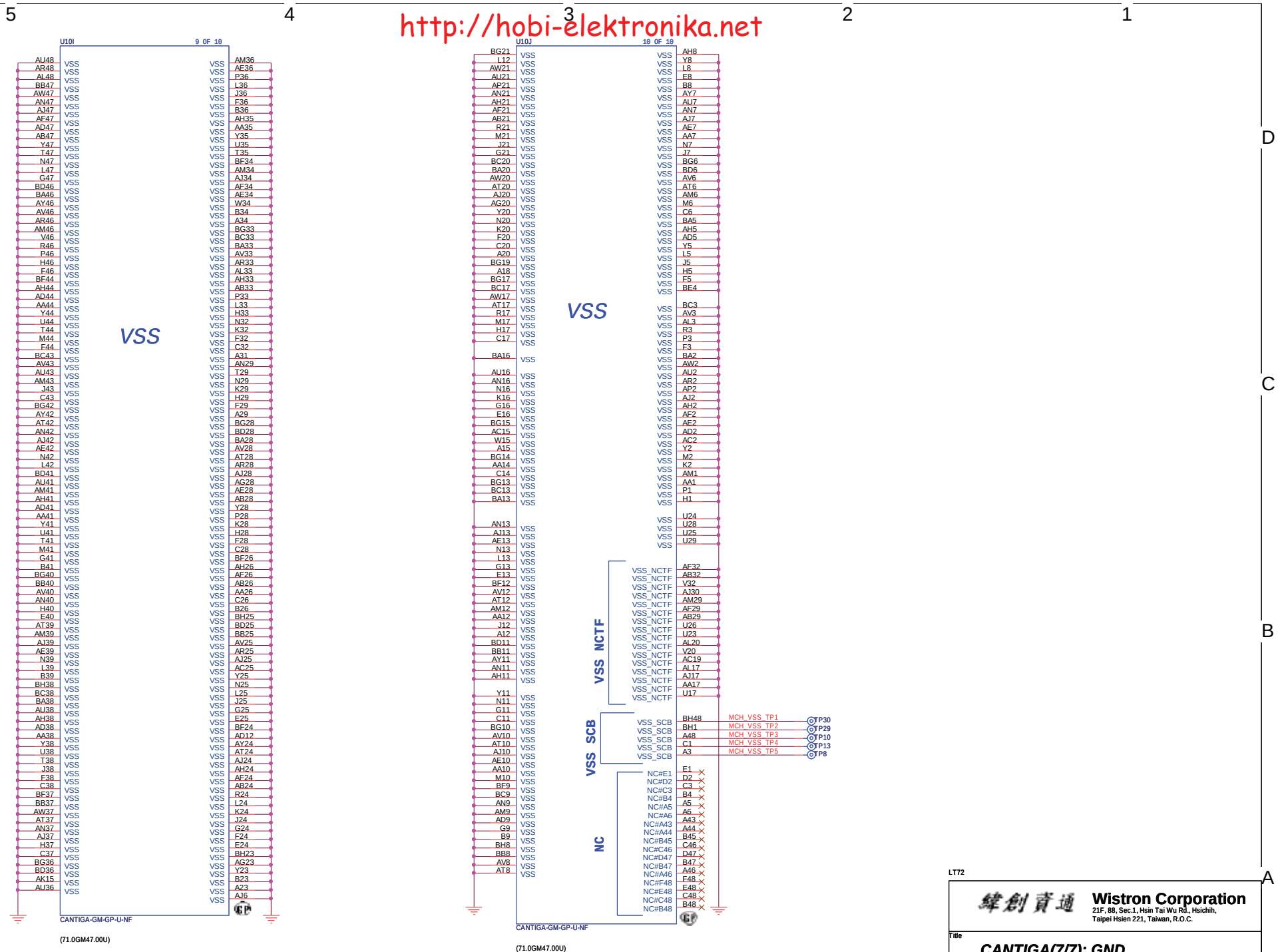
CFG5 : DMIx2
CFG6 : iTPM
CFG7 : ME Crypto
CFG9: PCIE STD& REV
CFG16 : FSB Dynamic ODT
CFG19 : DMI Lane reversal
CFG20 : DP concurrent
CFG[17:3]:internal pullup
CFG[20:18]:internal pulldown







LT72



<http://hobi-elektronika.net>

[www.hobi-elektronika.net](http://hobi-elektronika.net)

NORMAL TYPE

Place one cap to each power pin and as close as possible

Place caps close to pin1 as possible

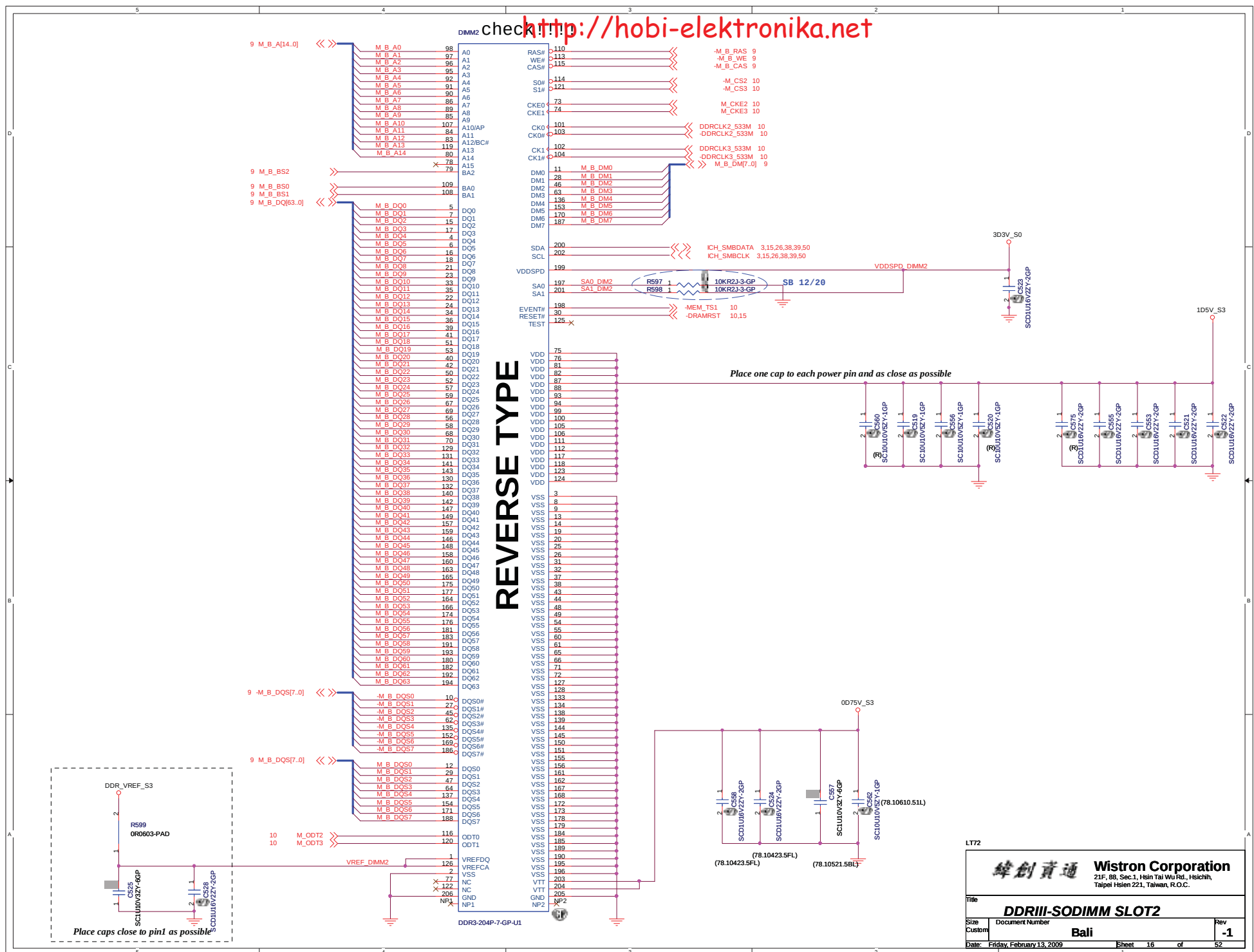
LT72

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Taipei Hsien 221, Taiwan, R.O.C.

File
DDRIII-SODIMM SLOT1

Size	Document Number	Rev
Custom	Bali	-1

Date: Friday, February 13, 2009 Sheet 15 of 52



LT72

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Title: **DDR3-SODIMM SLOT2**

Size: Custom

Document Number: **Bali**

Date: Friday, February 13, 2009

Sheet: 16 of 52

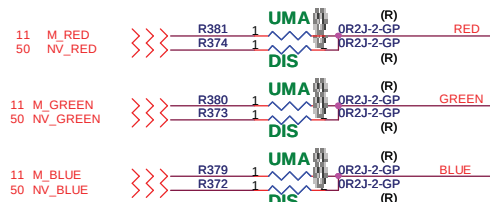
Rev: **-1**

CRT I/F & CONNECTOR

<http://hobi-elektronika.net>

20070615 Change VGA header for debug propose

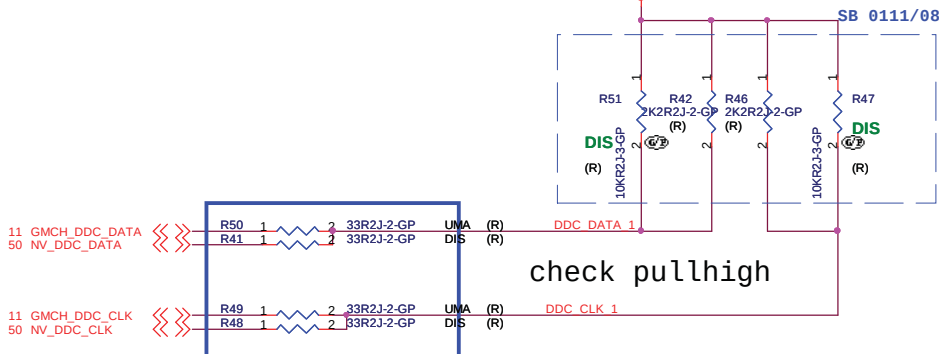
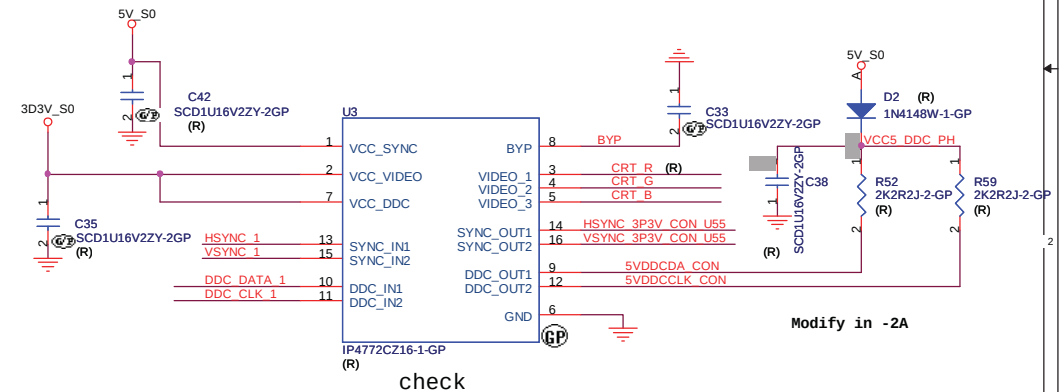
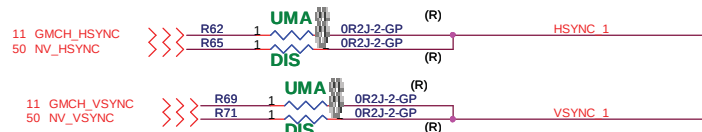
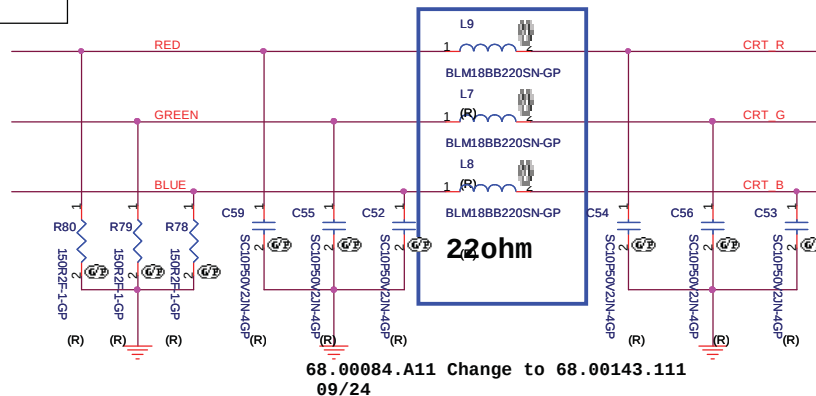
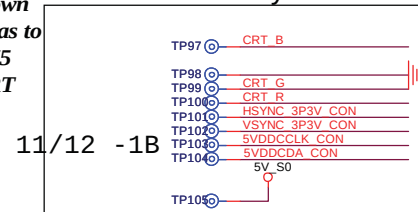
8/6 Modify. Mirror connection and Key 1



Layout Note:
Place these resistors
close to the CRT-out
connector

Layout Note:
Pi-filter & 150 Ohm pull-down
resistors should be as close as to
CRT CONN. RGB will hit 75
Ohm first, pi-filter, then CRT
CONN.

-1A Modify the connector



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Title

CRT Connector

Size

Document Number

Bali

Rev

-1

Date: Friday, February 13, 2009

Sheet 17

of

52

Naming convention -

Please confirm if Bali MB is "L-IGM45" -----It's true.

Paste location?-----

Place character string "L-IGM45" in silk-screen layer and Easy to observe position of PCB.
don't paste it with lable paper.

Location Box for P/N+Head Code+FRU Number -----

please follow lenovo SPEC about size,after the assembly,the Box is advantageous for the scanning the position.

Please provide this number rule information-----

Please follow lenovo SPEC.

Remove

Location Box for MAC Address -----

Please lay aside nearby P/N Box, does not affect to the P/N lable scanning position.

Please provide MAC information-----

Lenovo does not supply this information, after needing ODM supplier apply and assign it to use.

Label for LC ERP No.; (A label with 8 digits' Arabic number) -----

This Lable with 11s lable(P/N+HC+ FRU) the identical lable, now was also already unable to provide the information,
the interior needs to discuss.only reserve Box(itme 2).

Please provide this number rule information-----

the number need apply from lenovo system,needs the internal
discussion.

LT72

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
VGA IN(1/2)-RGB IN			
Size	Document Number		Rev
B	Bali		-1
Date:	Friday, February 13, 2009	Sheet	18 of 52

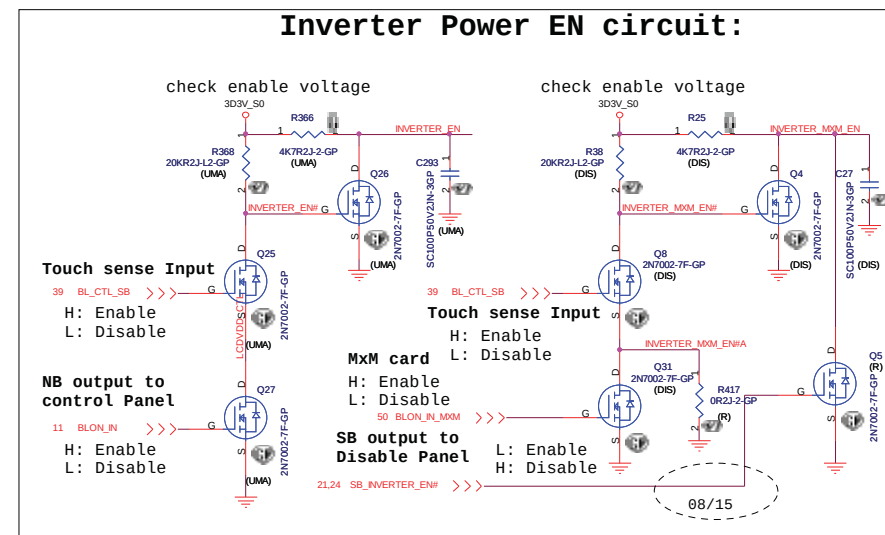
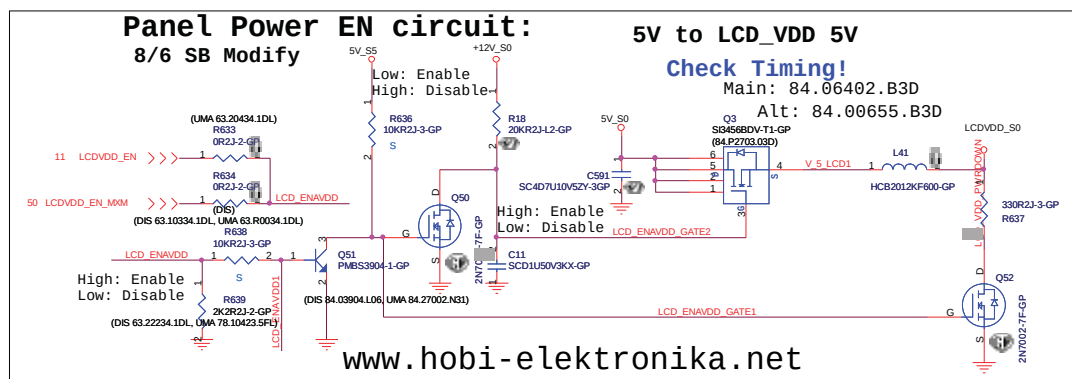
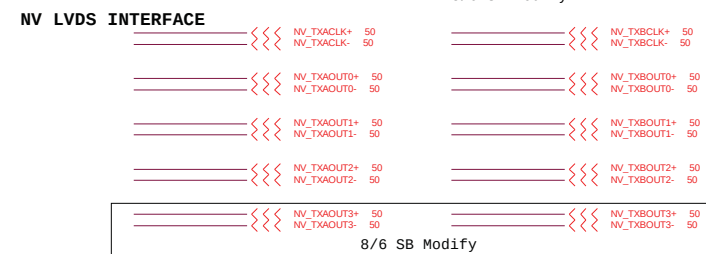
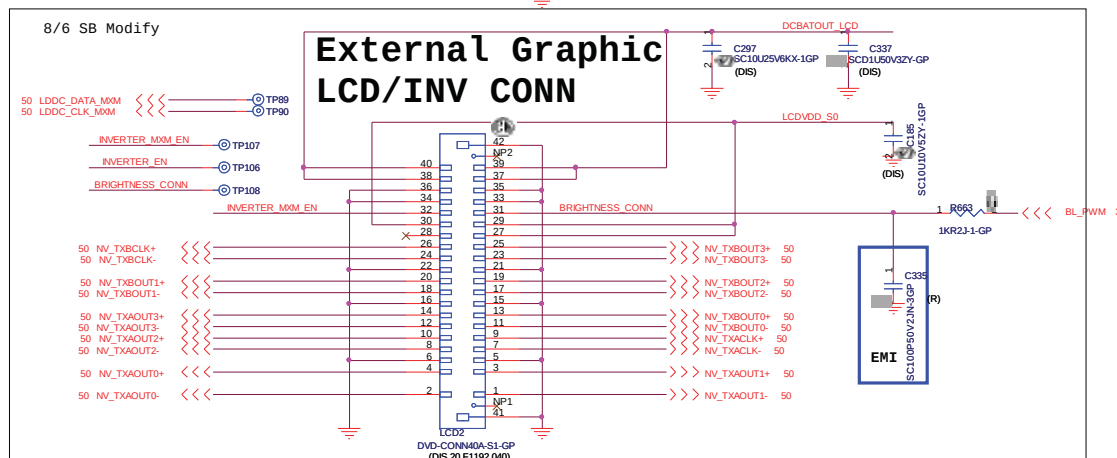
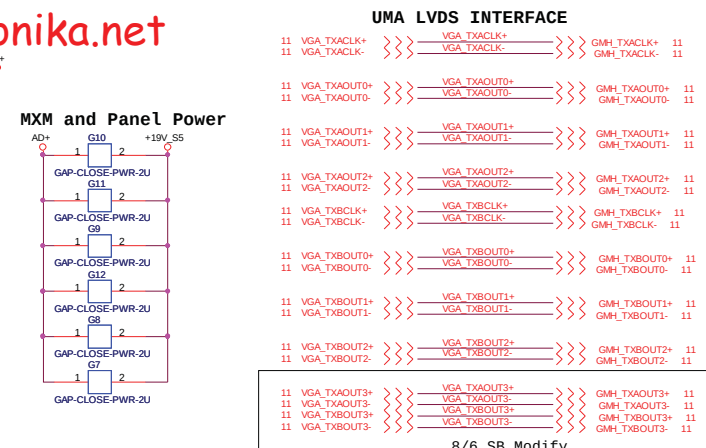
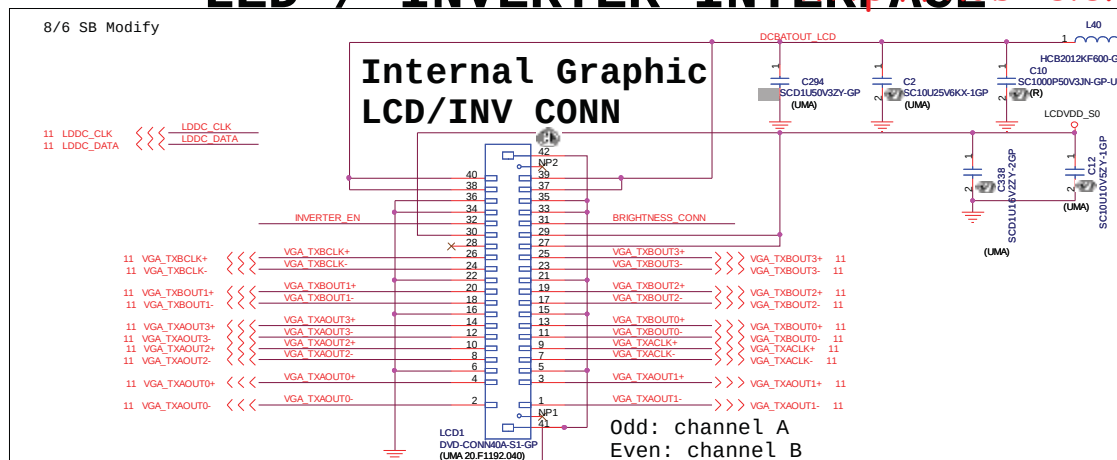
<http://hobi-elektronika.net>

Remove

LT72

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
VGA IN(2/2)-NT68665H			
Size B	Document Number	Bali	Rev
			-1
Date: Friday, February 13, 2009		Sheet 19	of 52

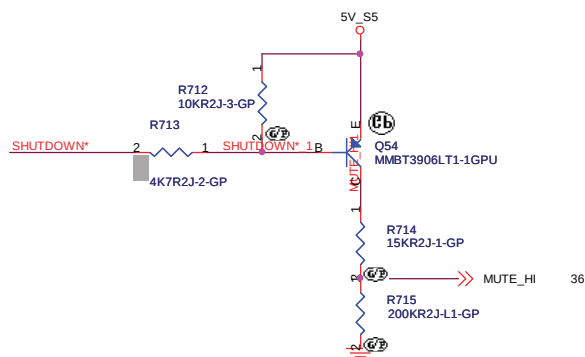
ERFACE <http://hobi-elektronika.net>



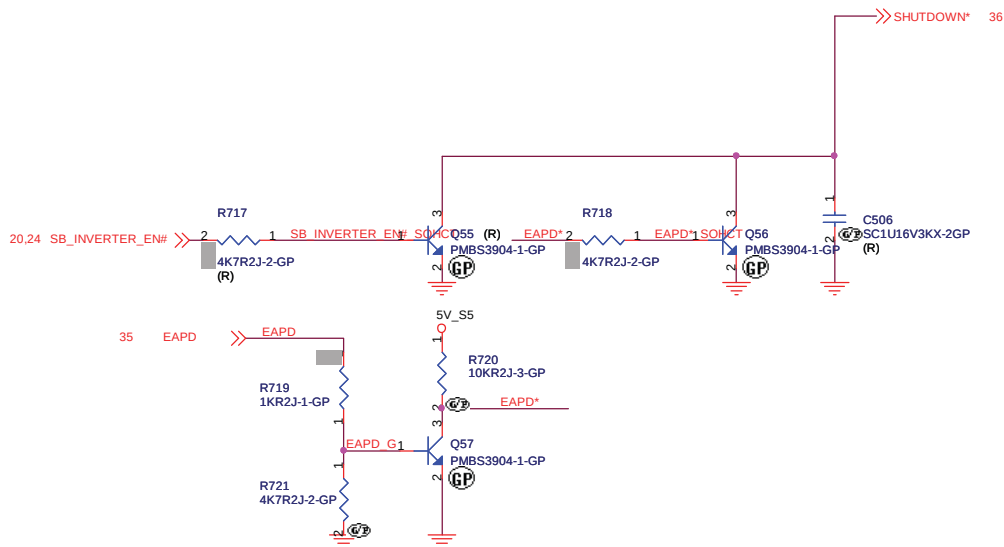
www.hobi-elektronika.net

10/2 -1A Unmount

10/16 -1A Modify



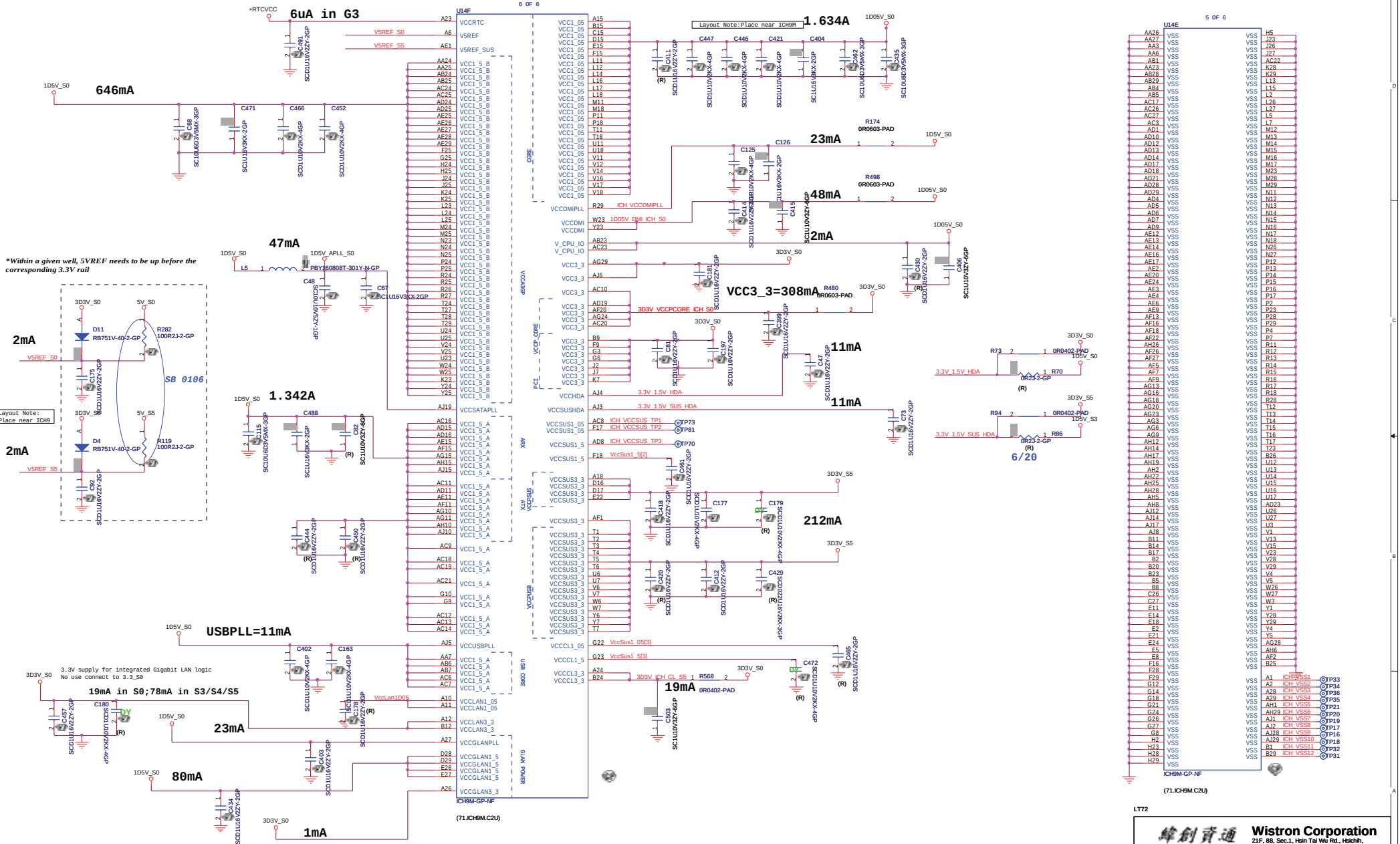
8/15 SB Modify



LT72

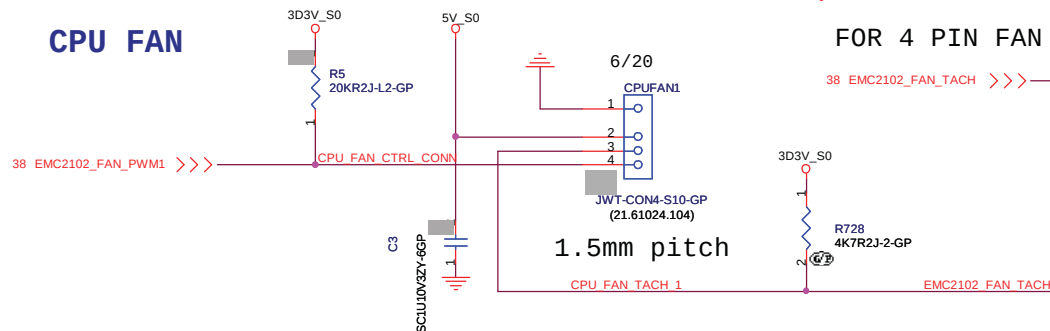
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
MUTE			
Size	Document Number		Rev
B	Bali		-1
Date:	Friday, February 13, 2009	Sheet	21 of 52





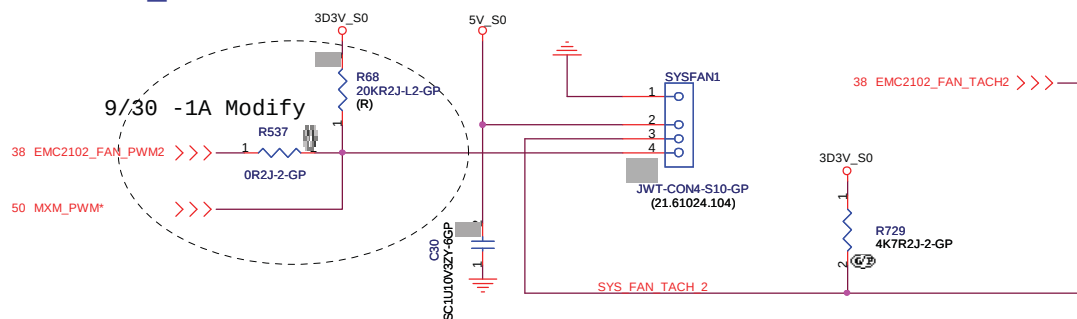
CPU FAN

FOR 4 PIN FAN



8/19 SB Modify

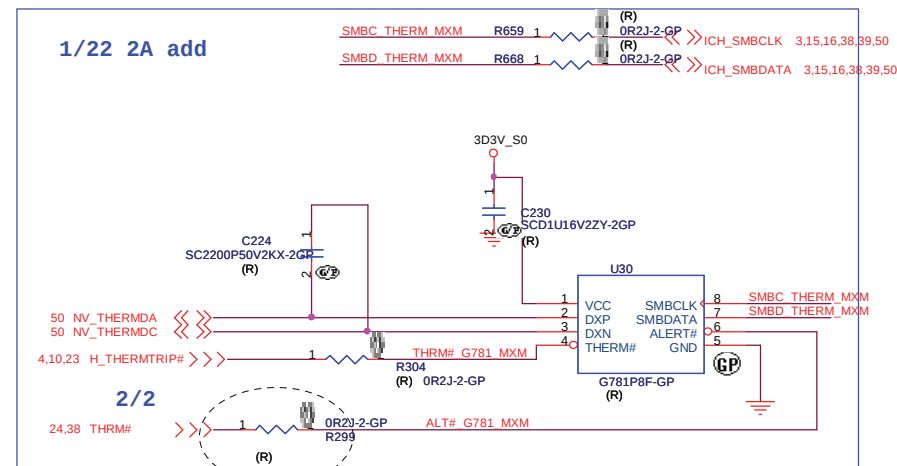
MXM_SYS FAN



8/19 SB Modify

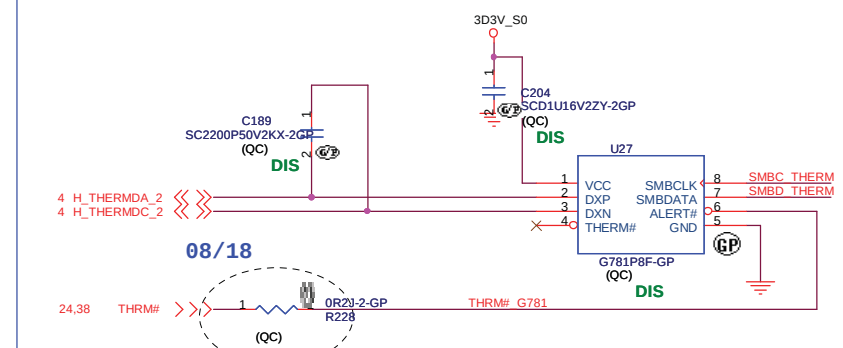
08/18

Remove MxM card thermal detect IC



SB 8/11 Modify

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LT71 DIS BOM

緯創資通

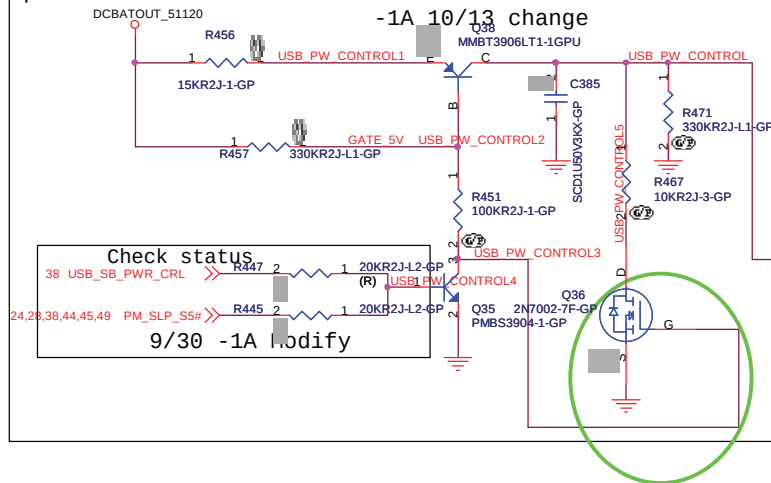
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title Thermal/Fan Controller EMC2102		
Size B	Document Number Bali	Rev SB
Date: Friday, February 13, 2009	Sheet 26 of	52

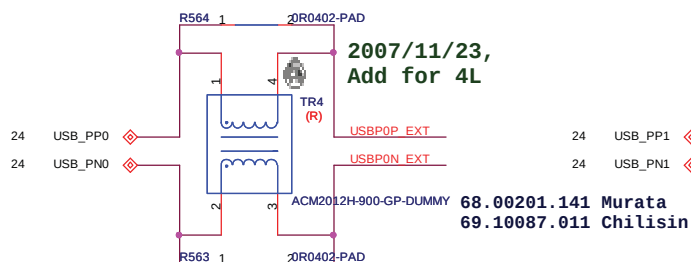
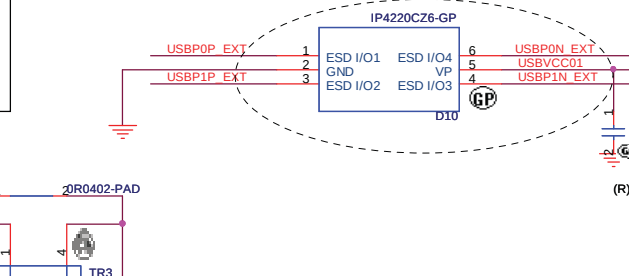
<http://hobi-elektronika.net>

USB PORT

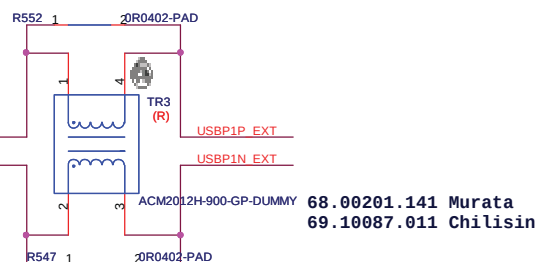
Check USB power switch Need check this block
power switch S5 OFF



Need check! Vgs=+/-20V

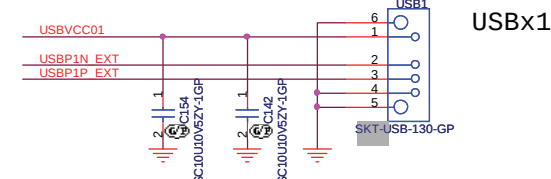
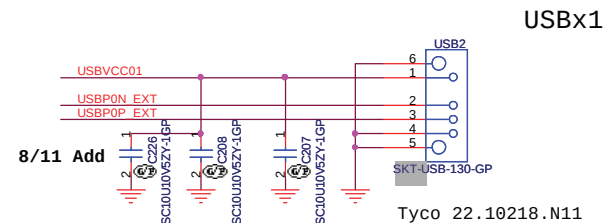
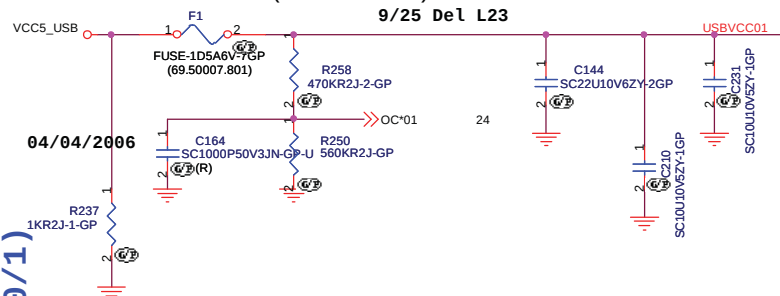


Remove 6/17



USB Power

Use 69.50007.801 (Littelfuse)



LT72

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Title

USB I/O

Size

Document Number

Bali

Rev

Date

Friday, February 13, 2009

Sheet

27

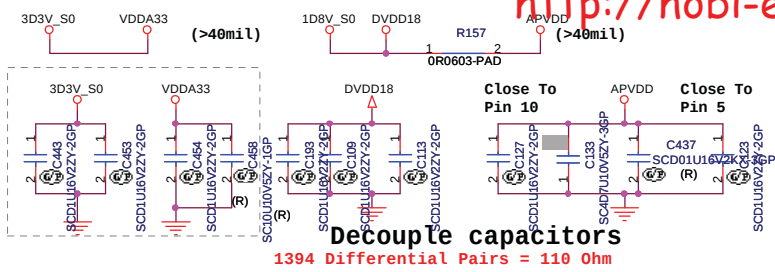
of

52

Rev

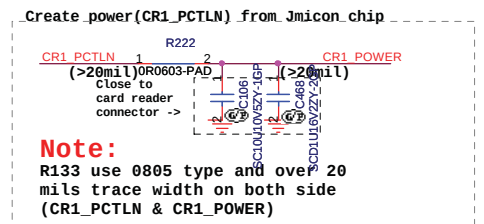
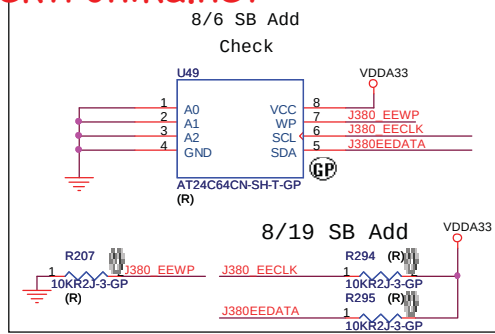
-1

**+3V3 and +1V8
Source power
must disable at
S3 mode**



Decouple capacitors
1394 Differential Pairs = 110 Ohm

**Power Circuit Trace Width: 40 mil (Min.)
Power plane or Power shape is more better**



Note:
R133 use 0805 type and over 20
mils trace width on both side
(CR1_PCTLN & CR1_POWER)

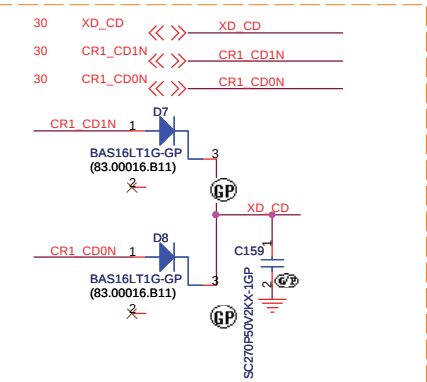
LED remove
For Debug circuit remove 2008.06.13

For D3E Mode remove
2008.06.13

D3E support (From Ver.B)

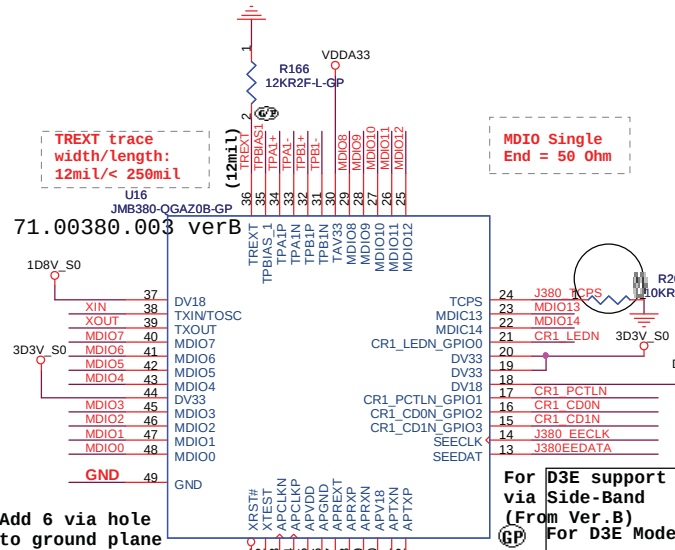
Note:
1. Add Q3 & Delete R135, if JMB38x
Power domain is different to SB chip
2. Delete Q3 & Add R135, if JMB38x
Power domain is same as SB chip

Card Reader power circuit



Card Reader Connector

BIOS Note:
Clock to JMB38x must
always turn on, no matter
any system power state

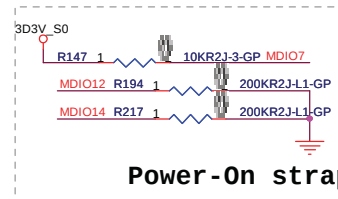


Add 6 via hole
to ground plane

**For D3E support
via Side-Band
(From Ver.B)
For D3E Mode remove
2008.06.13**

QFN-48

**Card Reader Pull
High/Low Resistors**



Power-On strapping setting

reserve 10Kohm pull-low to
GND?for MDIO7 (for EEPROM
use).
H:on-board, L:on Add-in card
H:CR1_PCTLN high active,L:CR1_PCTLN low active
(MDIO12 is no use in MP version Ic)
H:CR1_LEDN high active,L:CR1_LEDN low active

Check Pin13,14,15,16,17,20 function

緯創資通 Wistron Corporation
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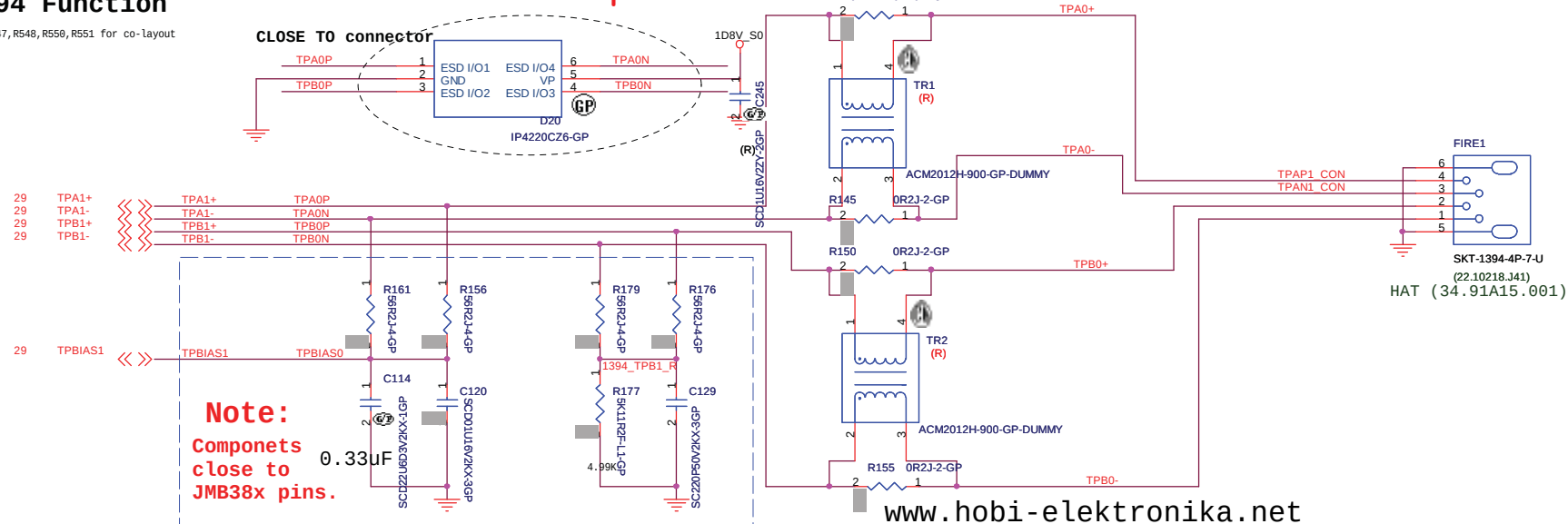
Title: **Jmicron380**

Size: **Bali** Rev: **SB**

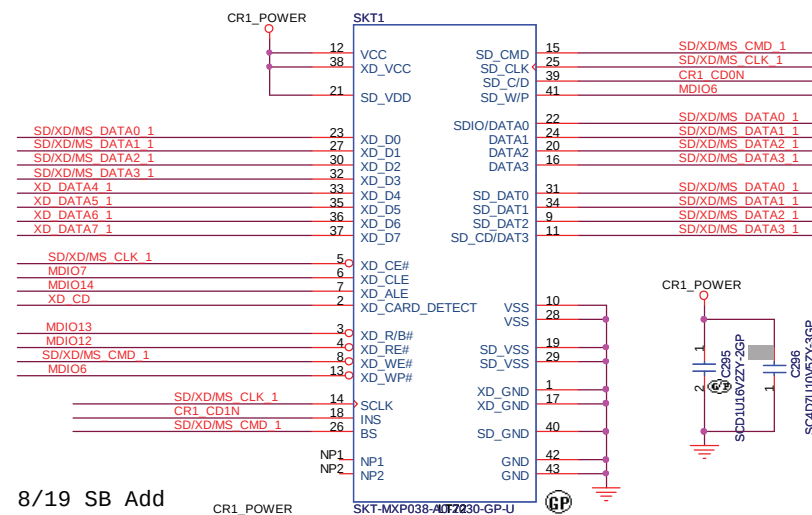
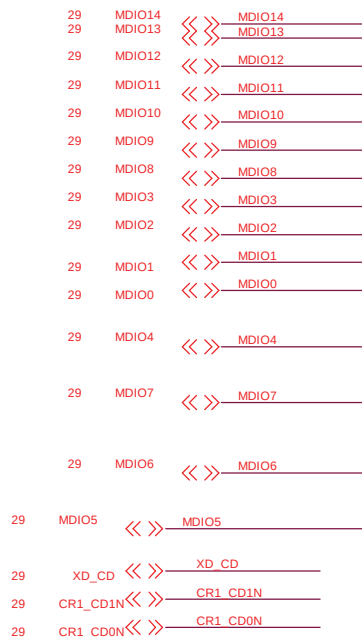
Date: Friday, February 13, 2009 Sheet 29 of 52

Reserve R547, R548, R550, R551 for co-layout

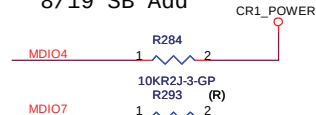
<http://hobi-elektronika.net>



4 in 1 Card reader



8/19 SB Add

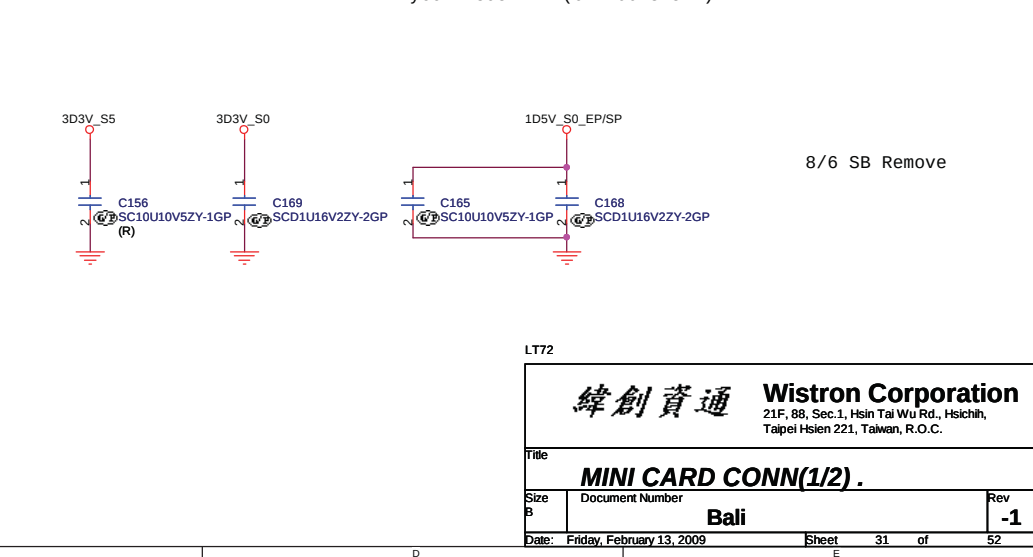
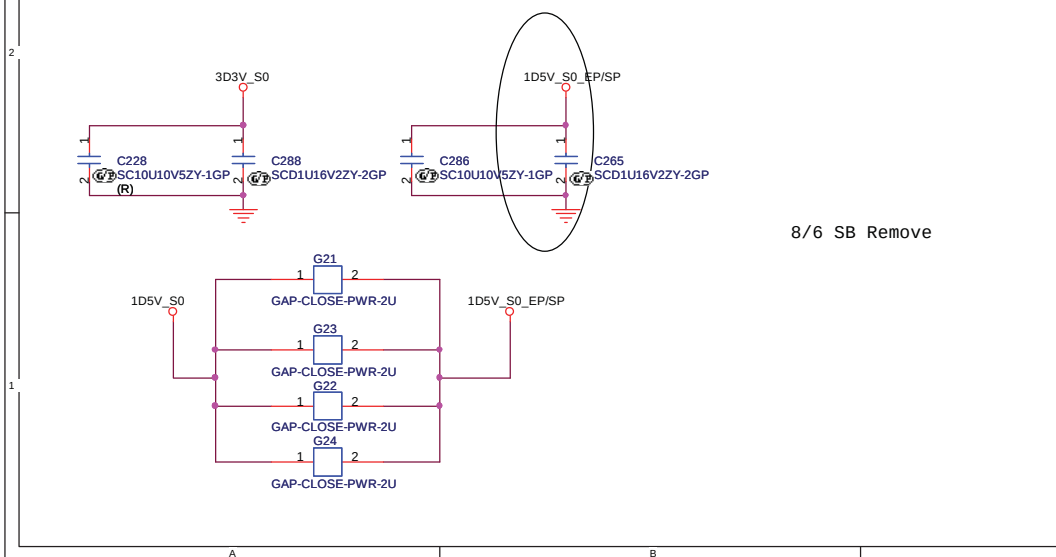
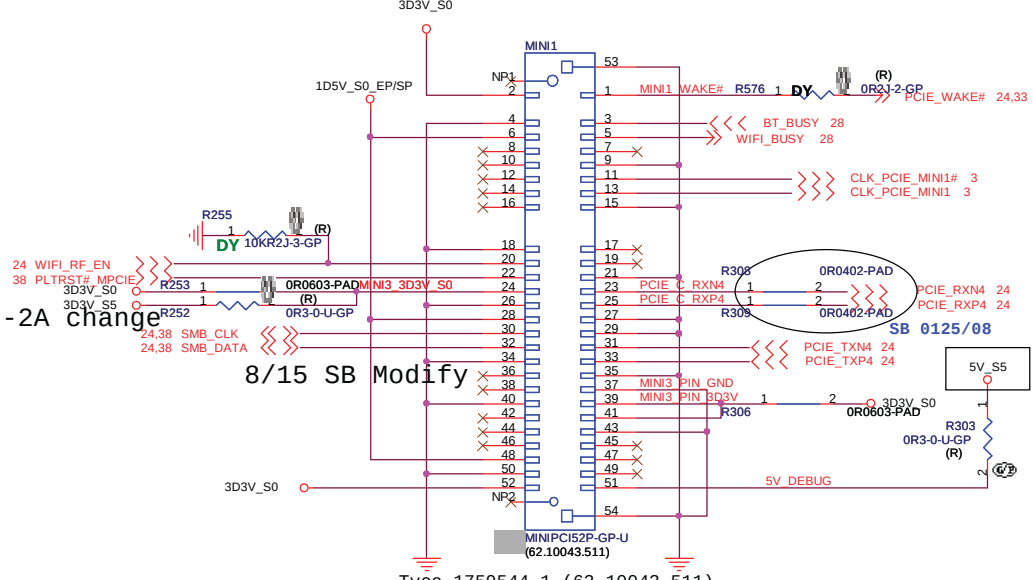
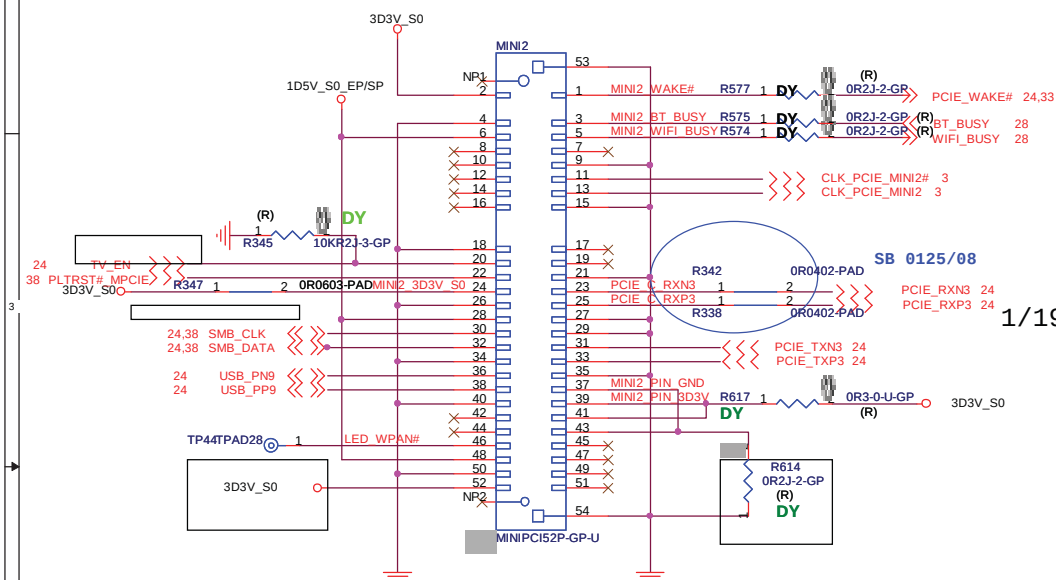


reserve 10Kohm pull-low to GND?for MDI07 (for EEPROM use).

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
R5C832/IEEE1394/SD/BT			
Size B	Document Number	Bali	Rev -1
Date:	Friday, February 13, 2009	Sheet 30 of 52	

WWAN/TV-TUNER

Wireless Card(Present support EP/SP)



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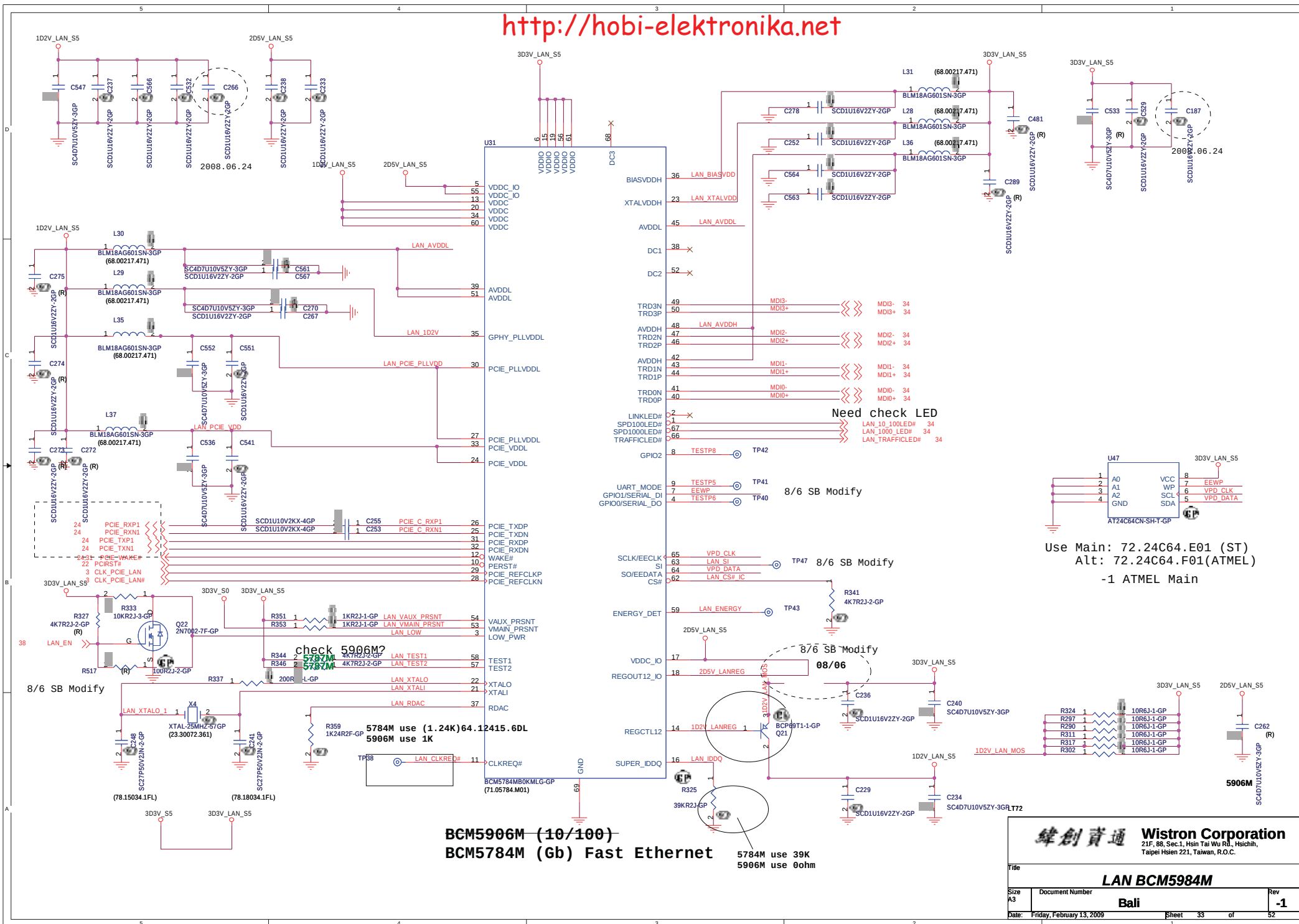
緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title MINI CARD CONN(1/2) .			
Size B	Document Number Bali	Rev -1	
Date: Friday, February 13, 2009	Sheet 31	of 52	

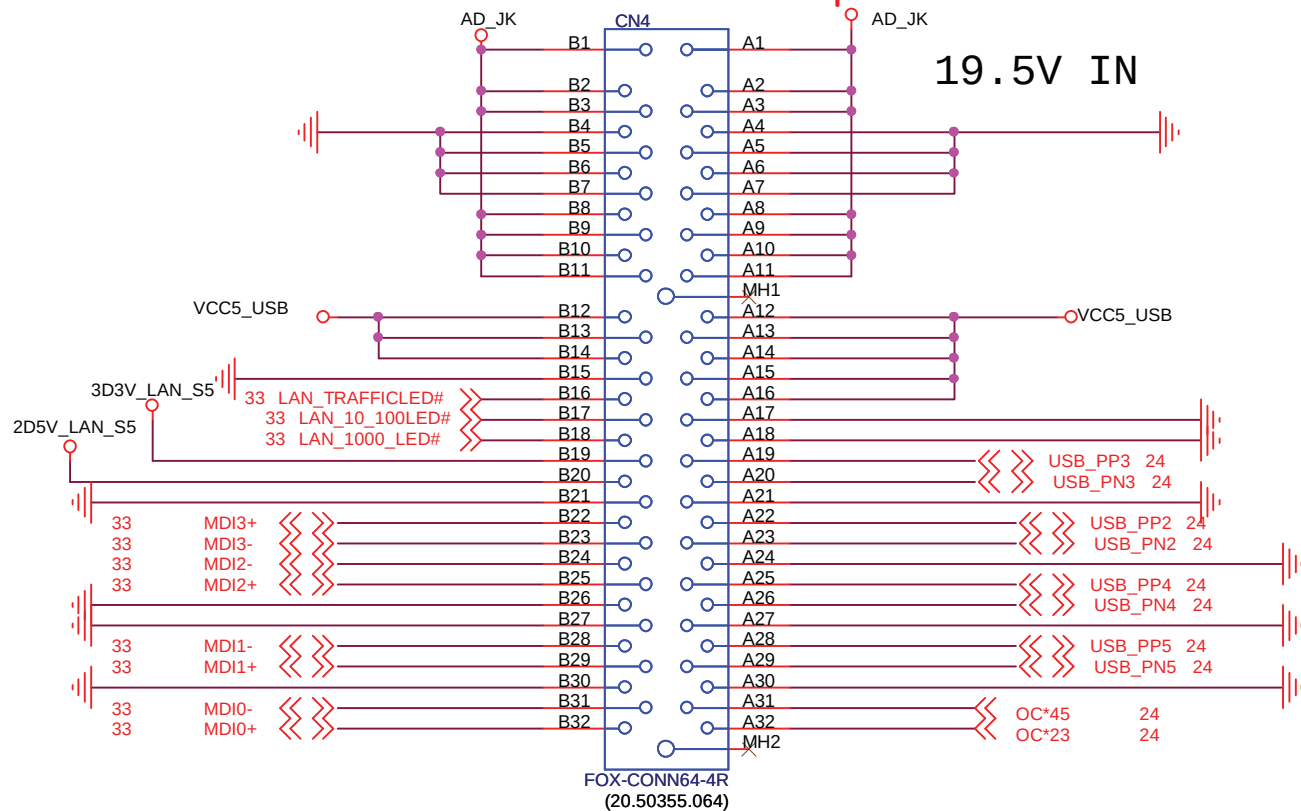
<http://hobi-elektronika.net>

Remove

LT72

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
MINIPCIE Robson			
Size B	Document Number Bali		Rev SB
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Lotes: 20.50355.064
Tyco: (20.50246.064)

10/100M Lan Transformer

RJ45+RJ11=>
cheange Riser
Card

New Card =>
cheange to
Page 32

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Title		
Riser		
Size A	Document Number	Rev
	Bali	-1
Date:	Friday, February 13, 2009	Sheet 34 of 52



Title			
AUDIO CODEC-ALC272			
Size A3	Document Number		Rev
	Bali		S
Date:	Friday, February 13, 2009	Sheet	35 of 52

AMP: for Main R/L Speaker <http://hobi-elektronika.net>

New solution ClassD: TI TPA3121D2

Put near U44 Change R/L, add R 2.2%

10/16 -1A Modify

www.hobi-elektronika.net

8/15 SB Modify

Put near U43

What function!? Diode type!?

Add more AGND VIA

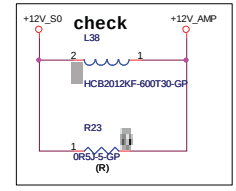
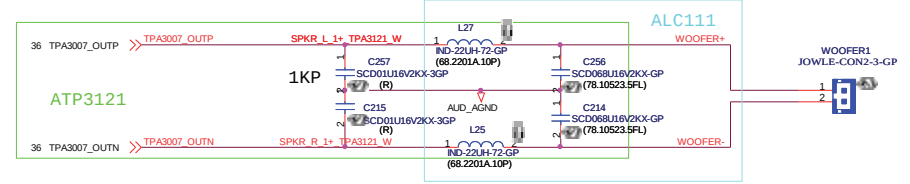
Speaker1_L FSOV 1.122V
Speaker1_R FSOV 1.107V
Woofer_MONO FSOV 1.089V

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緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title			AUDIO AMP/SPEAKER	
Size	Document Number	Rev		
Custom	BALI	SB		
Date:	Friday, February 13, 2009	Sheet	36	of 52

Sub Woofer
22uH for TPA3007
8.2uH for ALC111



10uH for ALC111
68.22010.20B Youth
68.2201A.10P Chilism
68.2201A.10N Tai-Tech

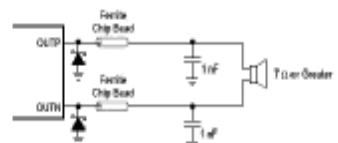


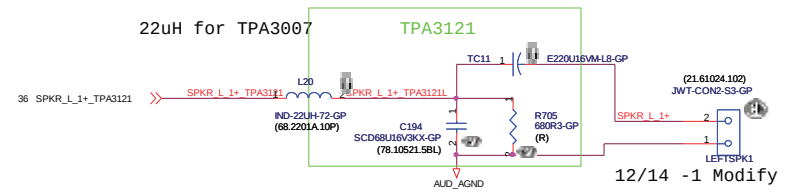
Figure 16. Typical Ferrite Chip Bead Filter [Chip bead example: Fair-Rite 251206100Y3]



Figure 17. Typical LC Output Filter for 8-Ω Speaker. Cutoff Frequency of 41 kHz

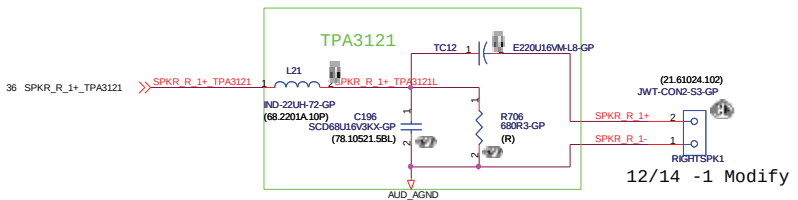
www.hobi-elektronika.net

22uH for TPA3007

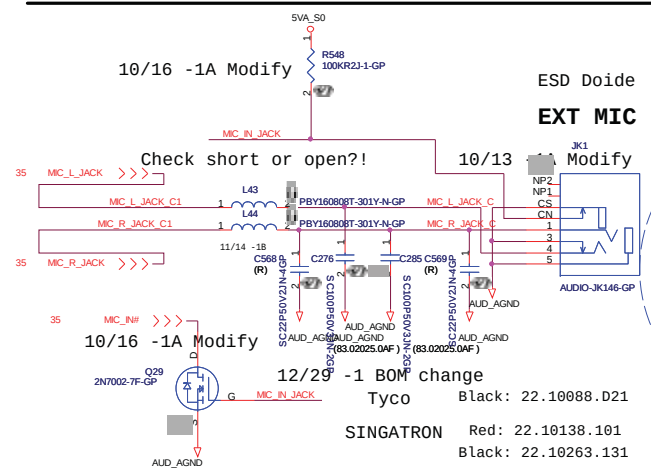


22uH
68.22010.20B YOUTH (remove)
68.2201A.10P Chilisin
68.2201A.10N TAI-TECH

220uF
CHEMICON 09.2271D.L16
SANYU 09.2271D.L13
Rubycon 09.2271D.J8L

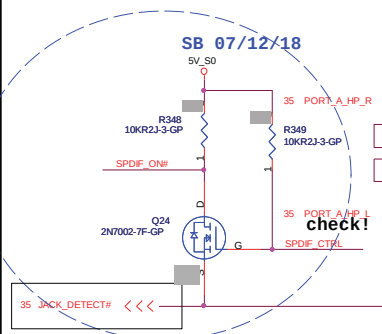


10/16 -1A Modify



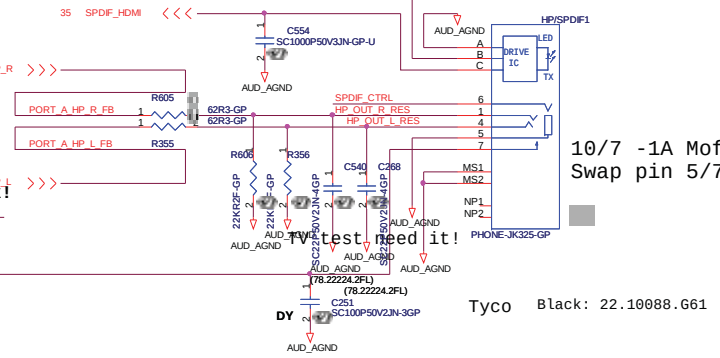
ESD Doide
EXT MIC

10/13 Modify



HP_OUT/ LINE_OUT

Power on S0



10/7 -1A Mofify Lib
Swap pin 5/7

Check!

Check PART

12/29 -1 BOM change

Wistron Corporation		
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Title		
AUDIO HP_JK/ MIC_JK/SUBWOF		
Size	Document Number	Rev
Custom	Bali	SB
Date:	Friday, February 13, 2009	Sheet 37 of 52



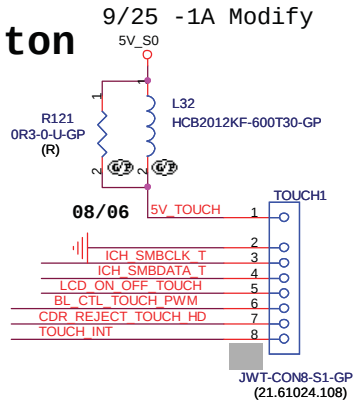
Touch button

LCD_ON_OFF_TOUCH
Power ON: High
Touch: Low/High/Low...

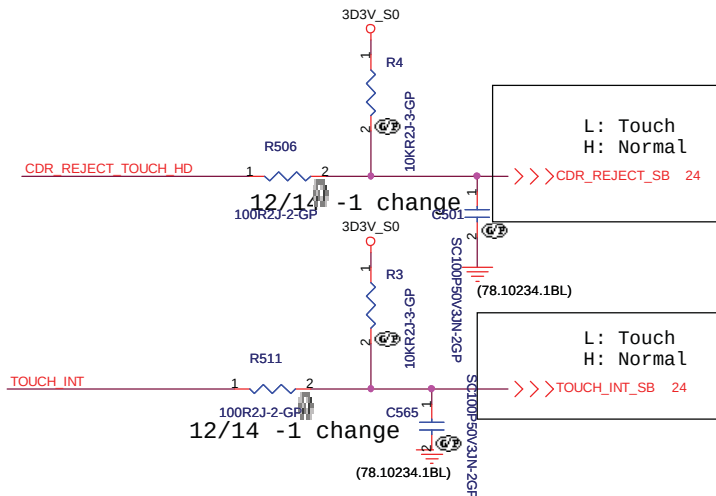
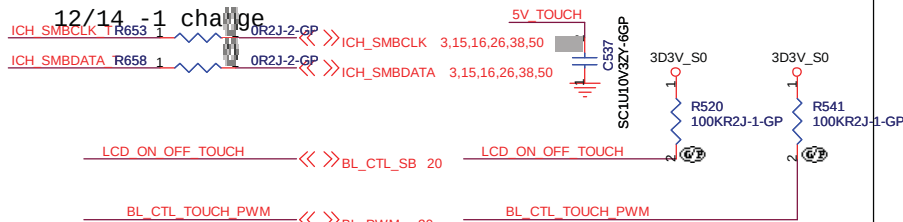
BL_CTL_TOUCH_PWM
PWM duty for Inverter Board

CDR_REJECT_TOUCH_HD
L: Touch
H: Normal

TOUCH_INT
L: Touch any key
H: Normal

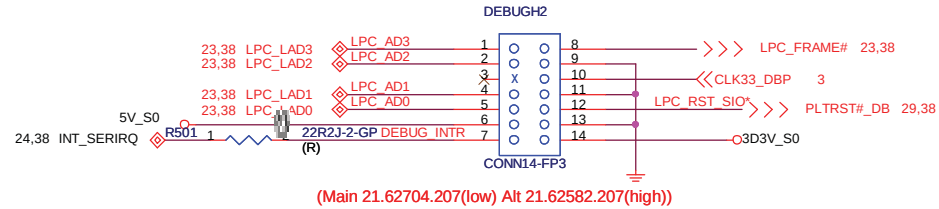


9/25 -1A Modify



<http://hobi-elektronika.net>

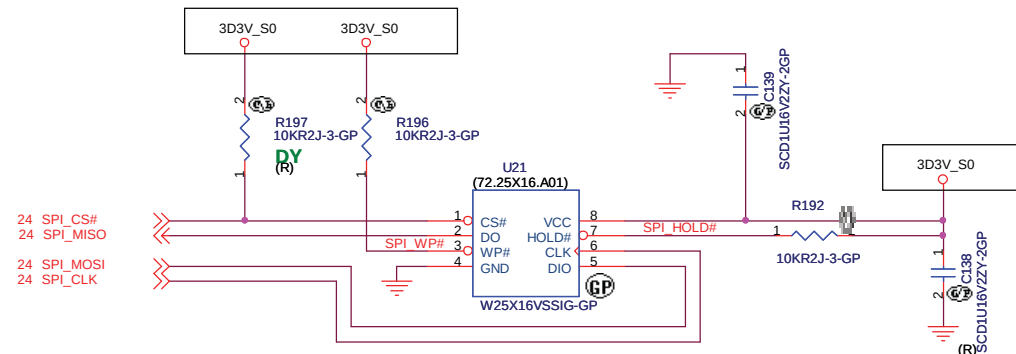
debug header



21.62704.207
David HEAD ML
2R14P(-1#6)ST
14452360
(high2.56+4mm)

SPI ROM for System & KBC

SPI Socket: 62.10089.011



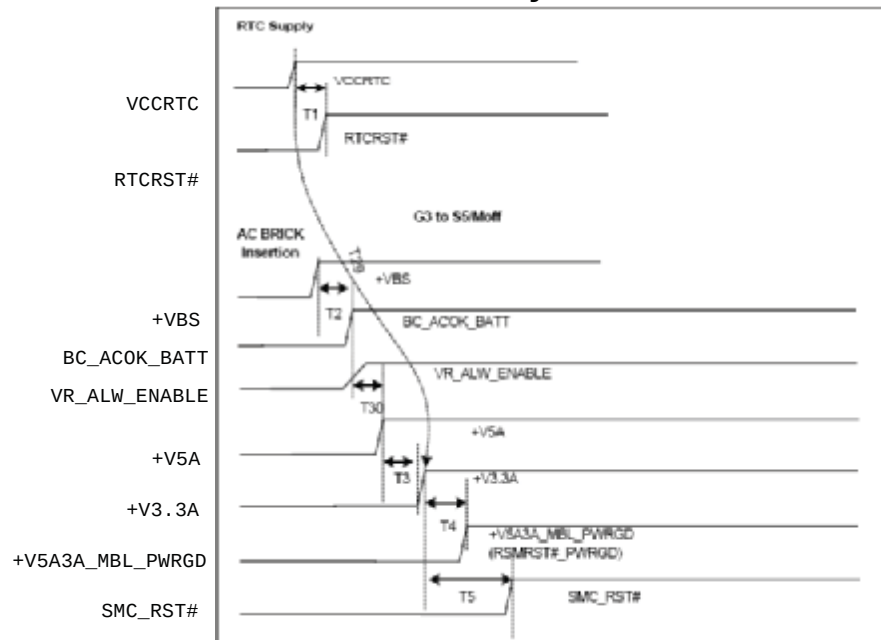
1. Main Source: 72.25X16.A01(Winbond 16Mb)
2. 2nd Source: 72.25165.A01 (MXIC 16Mb)
3. 3ns source: 72.25016.A01 (SST -50 16MB)
72.25016.D01 (SST-75 16Mb)

12/14 -1 Remove BIOS socket

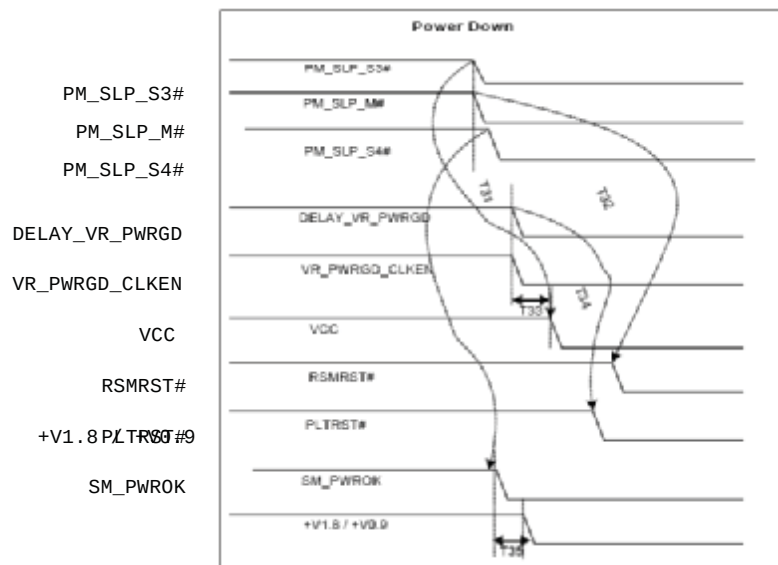
L72

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Keyboard /Touch Pad			
Size Custom	Document Number	Bali	Rev -1
Date:	Friday, February 13, 2009	Sheet 39 of 52	

Standby Power ON



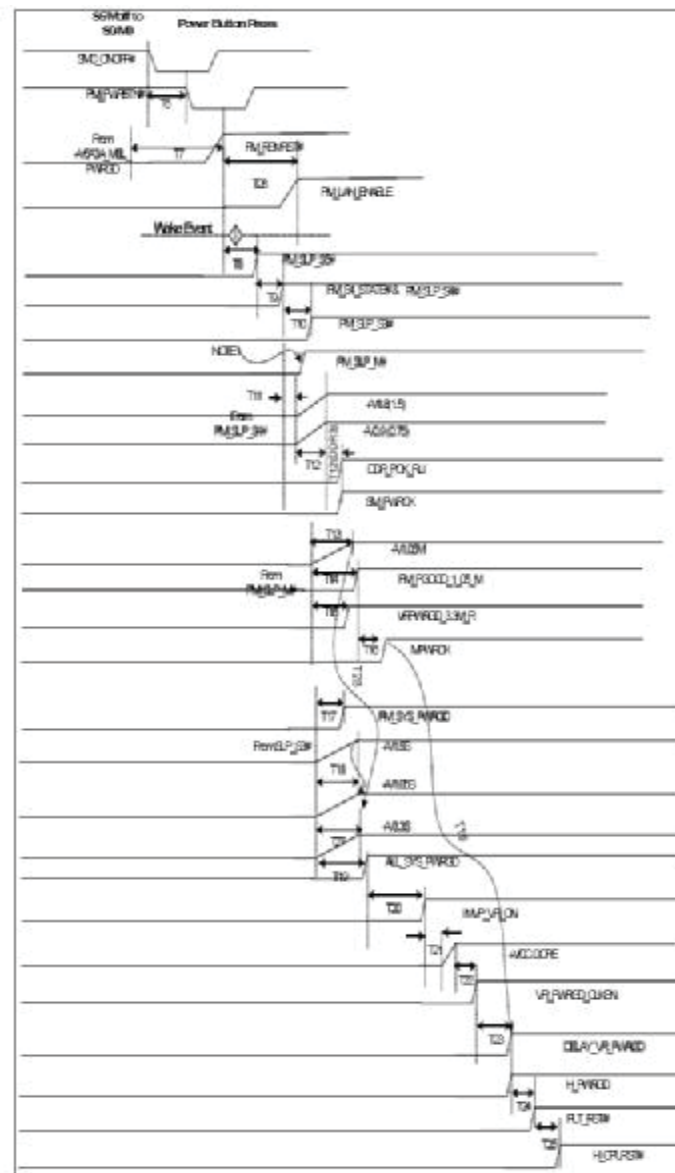
Power DOWN

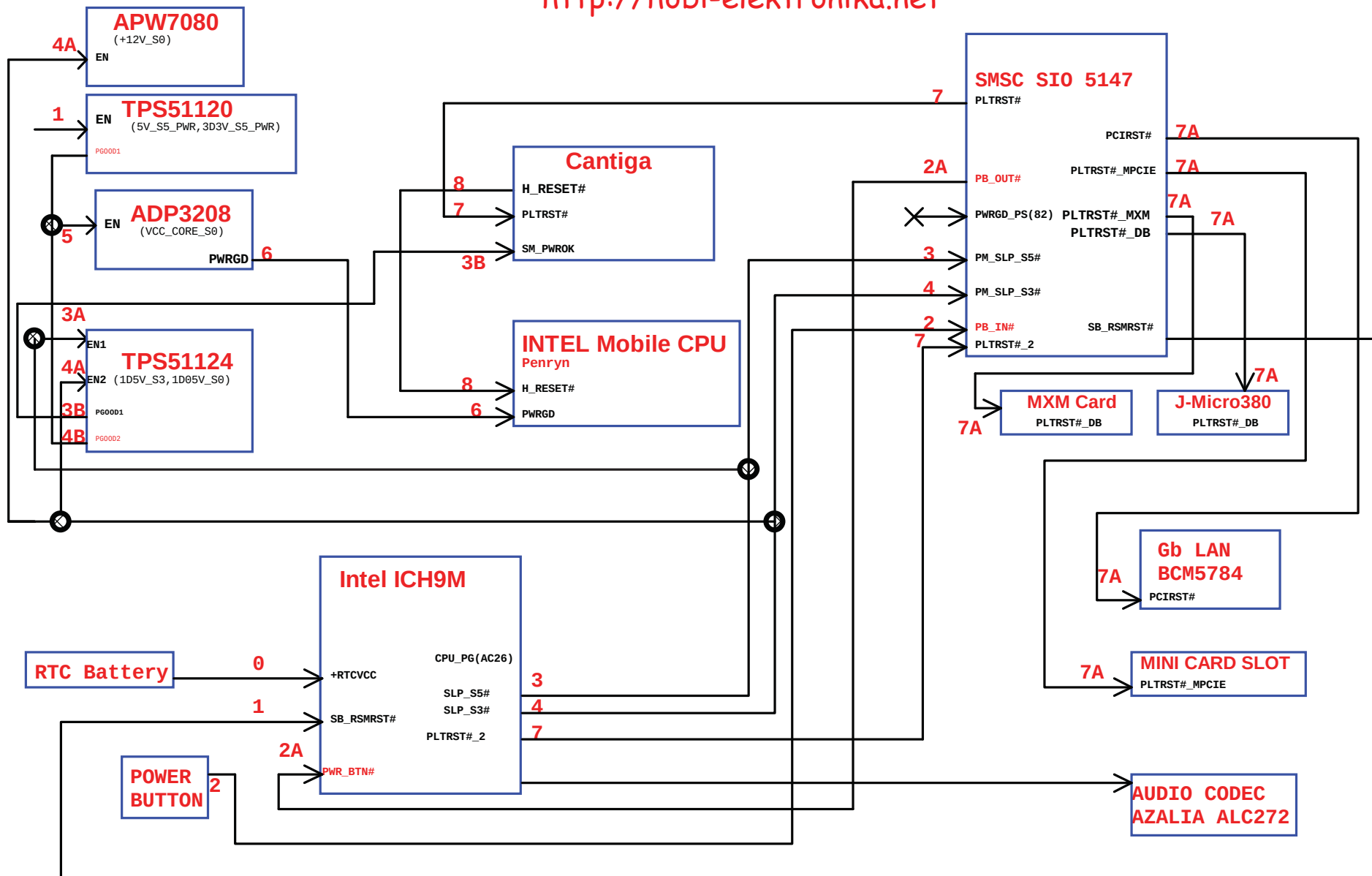


Power ON

SMC_ONOFF#
PM_PWRBTN#
PM_RSMRST#
PM_LAN_ENABLE
PM_SLP_S5#
PM_S4_STATE#&PM_SLP_S4#
PM_SLP_S3#
PM_SLP_M#
+V1.8(1.5)
+V0.9(0.75)
DDR_POK_RU
SM_PWROK
+V1.05M
PM_PG00D_1_05_M
VRPWRGD_3.3M_R
MPWROK

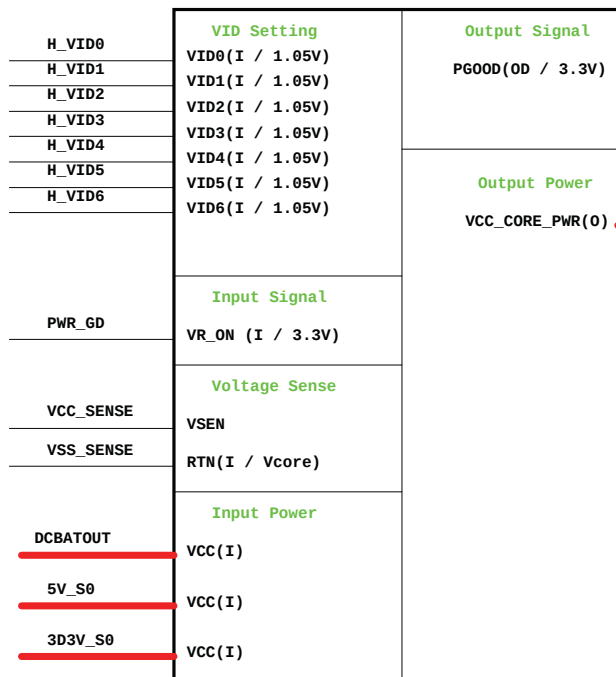
PM_SYS_PWRGD
+V1.5S
+V1.05S
+V3.3S
ALL_SYS_PWRGD
IMVP_VR_ON
VCC CORE
VR_PWRGD_CLKEN
DELAY_VR_PWRGD
H_PWRGD
PLT_RST#
H_CPURST#



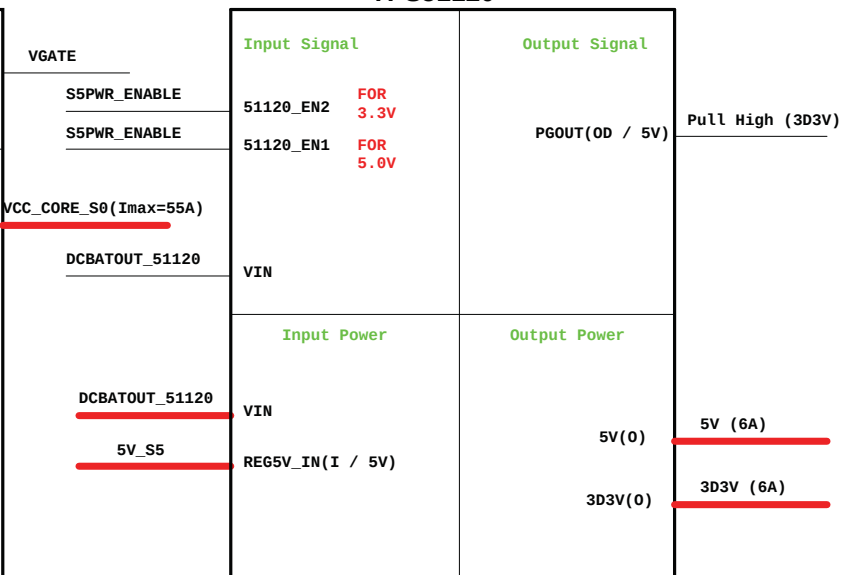


RESET/POWER GOOD MAP

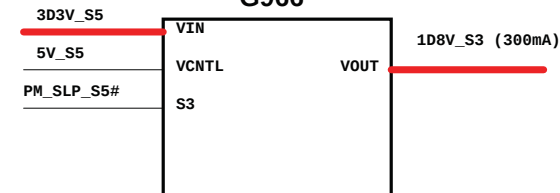
**CPU_CORE
ADP3207A**



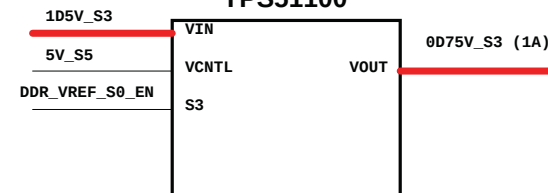
**3.3V/5V
TPS51120**



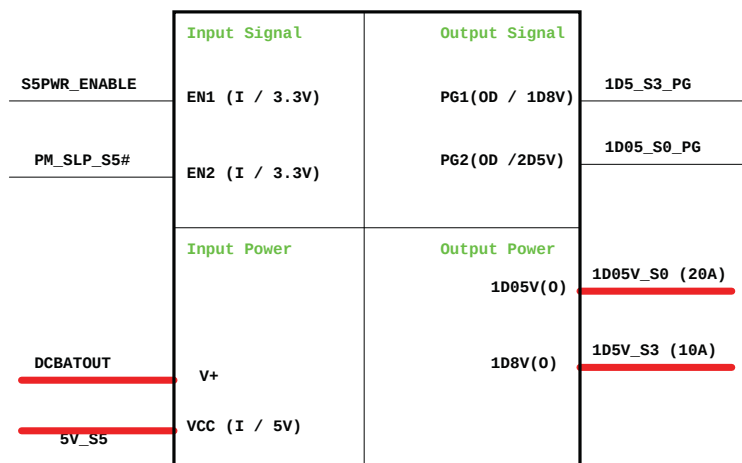
**1D8V_S3
G966**



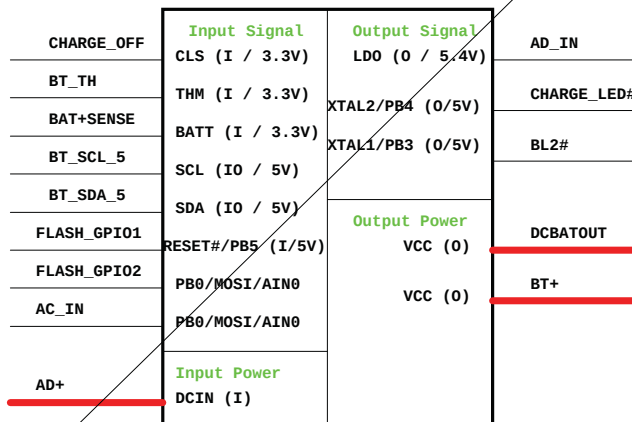
**DDR_0D75V_S3
TPS51100**



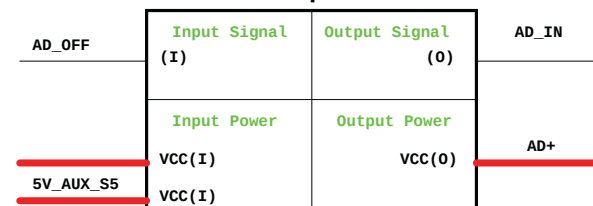
**1D5V/1D05V
TI TPS51124**



**Charger
MAX8725**



Adapter

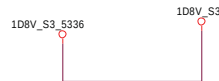


緯創資通 Wistron Corporation
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File			
POWER BLOCK DIAGRAM			
Size A3	Document Number	Bali	Rev Bali
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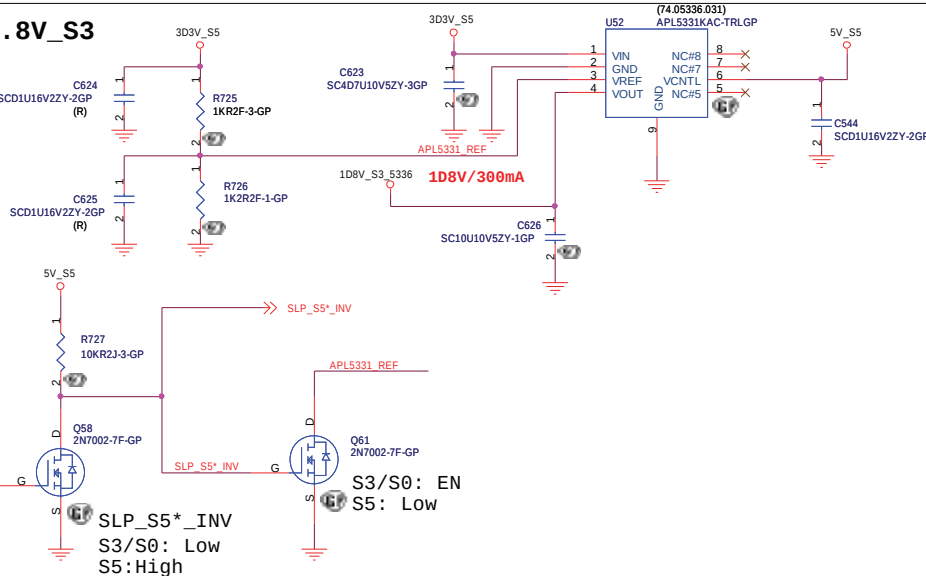
9/25 -1A Remove



3D3V_S5 -> 1.8V_S3

1D8V

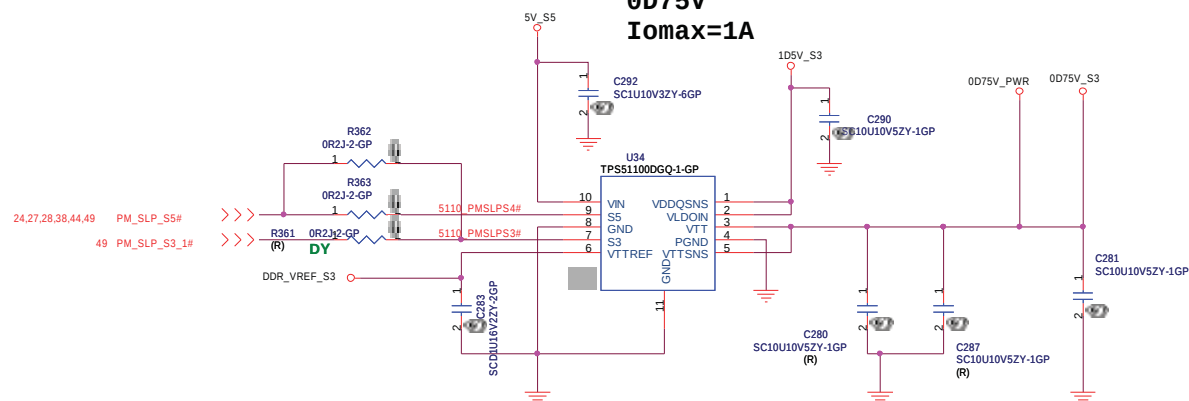
Iomax=300mA



24,27,28,38,44,49 PM_SLP_S5# >>>
PM_SLP_S5#
S3/S0: High
S5: Low

SLP_S5*_INV
S3/S0: Low
S5: High

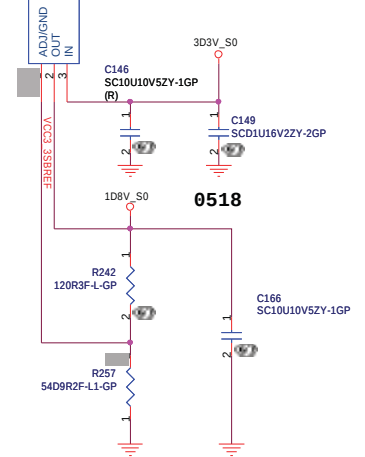
0D75V
Iomax=1A



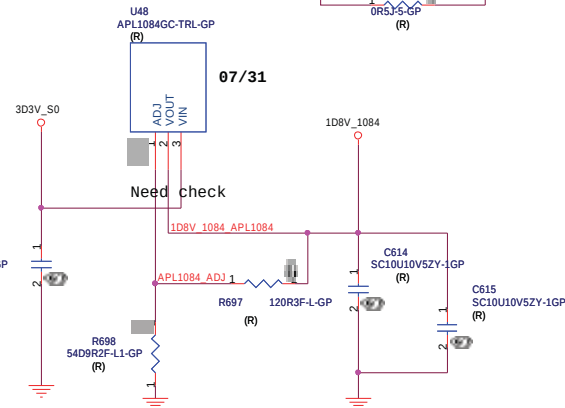
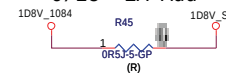
24,27,28,38,44,49 PM_SLP_S5# >>>
49 PM_SLP_S3_1# >>>

DDR_VREF_S3

0518
check current
3D3V -> 1.8V



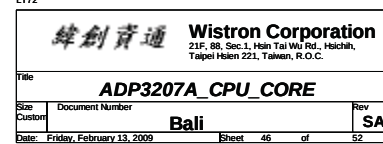
9/25 -1A Add



LT72

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

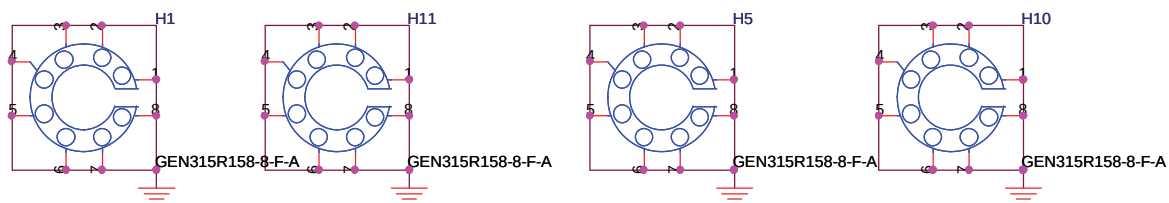
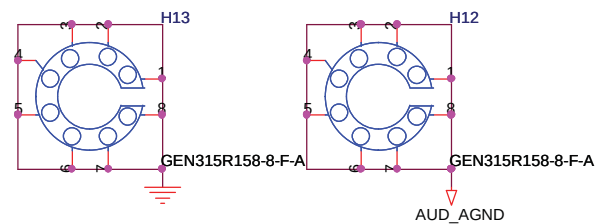
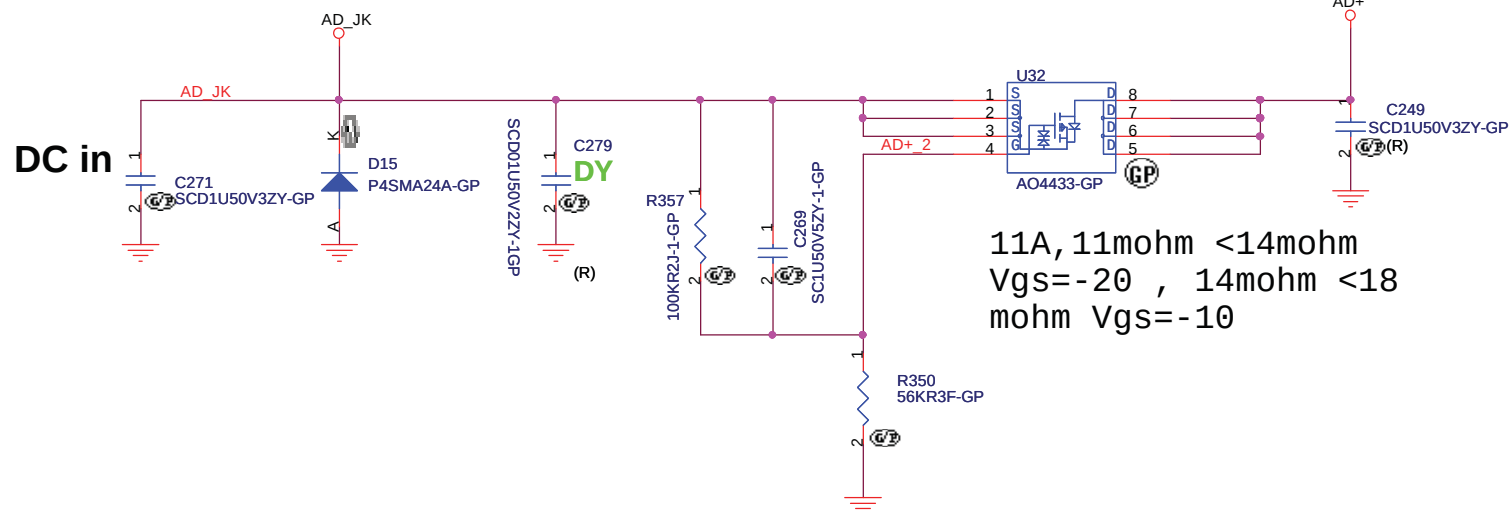
File			
LDO 1D8V / 0D75V			
Size	Document Number	Rev	
A3		Bali	
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Adaptor in to generate DCBATOUT

Add alternate 84.01403.A37

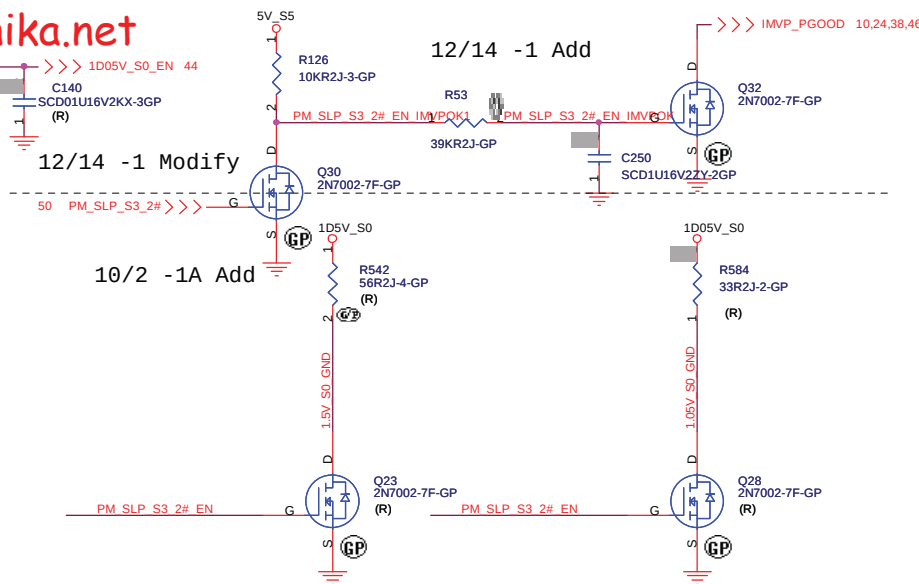
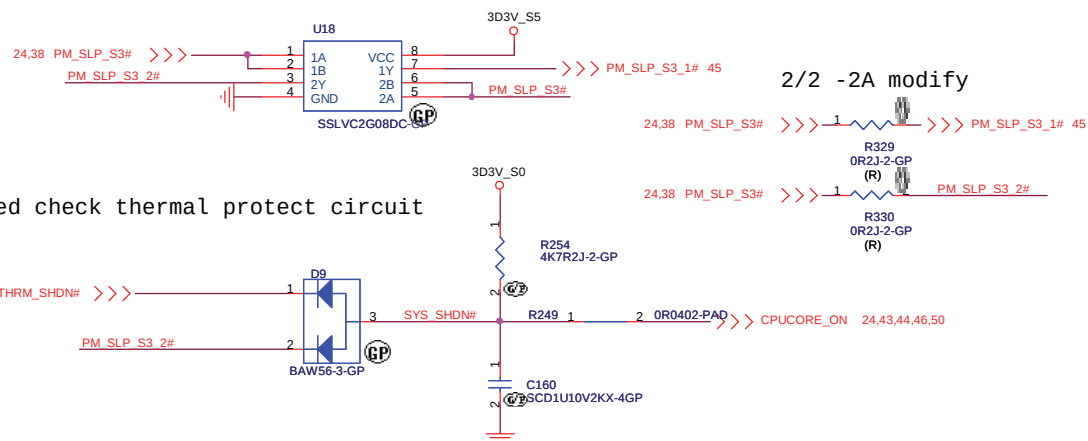


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Taipei Hsien 221, Taiwan, R.O.C.

Title		
ADT&BATT CONN		
Size A4	Document Number Bali	Rev SA
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Reset Logic

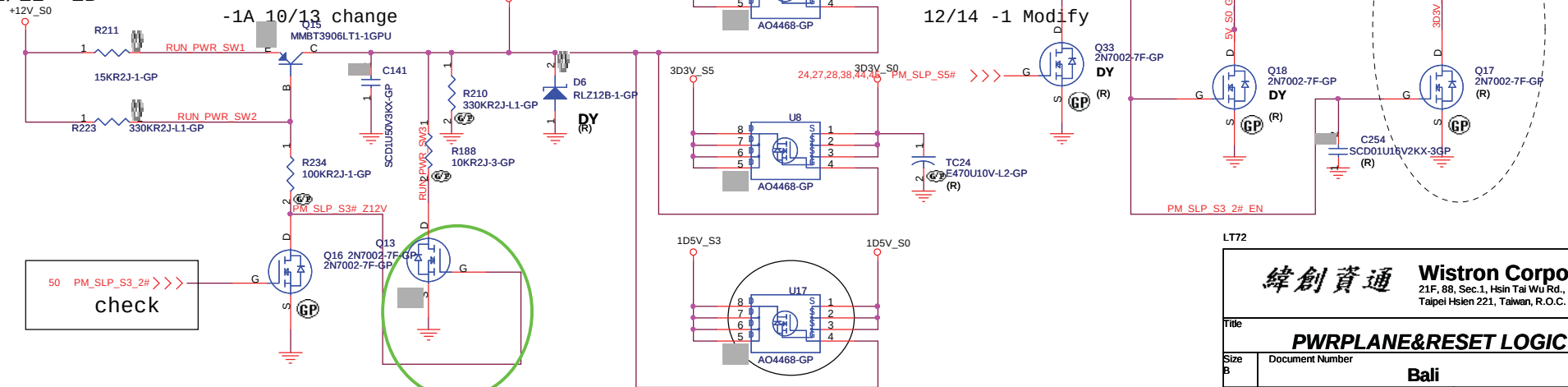
need modify for DT thermal protect



www.hobi-elektronika.net

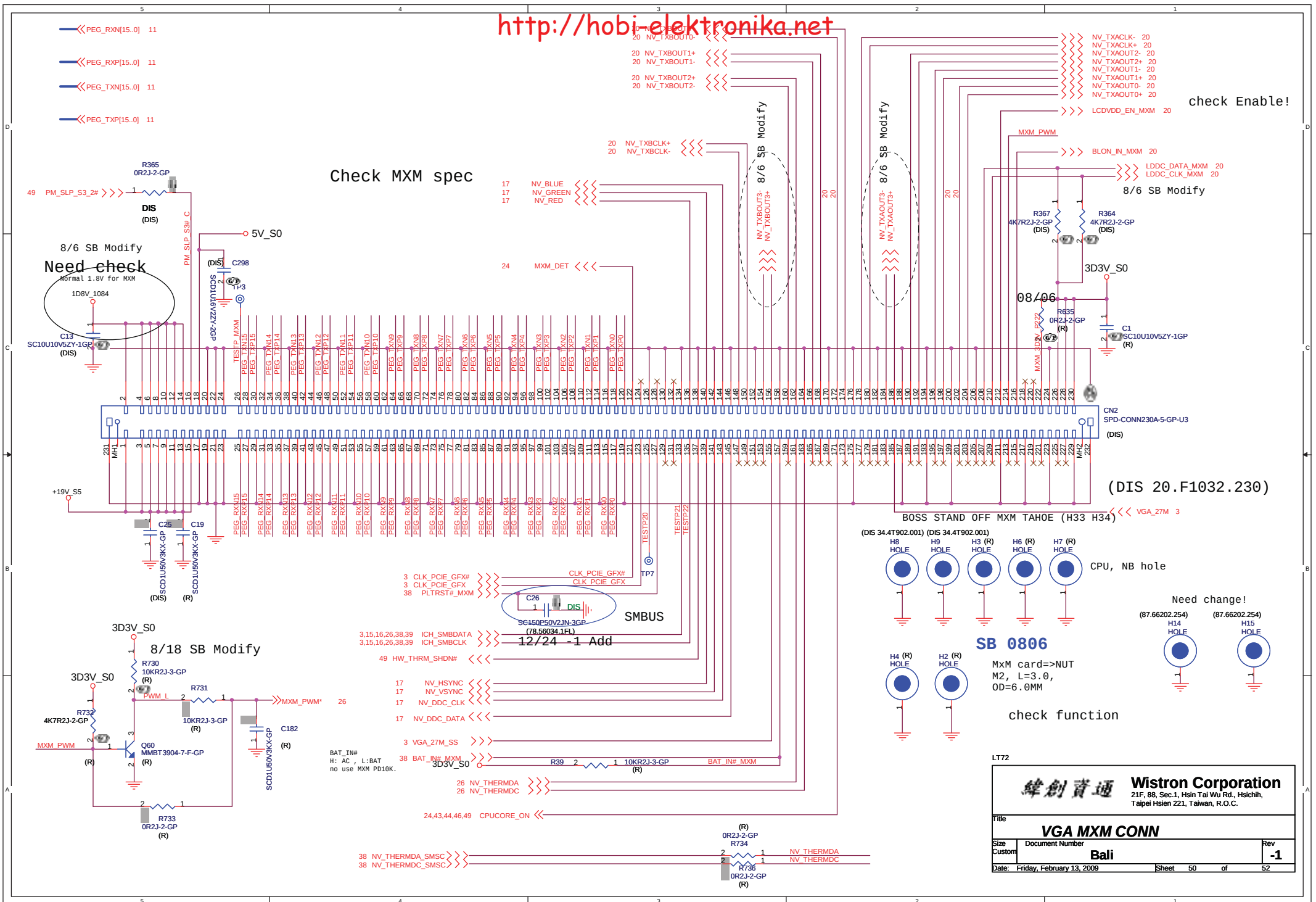
Run Power

11/12 -1B



LT72

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
PWRPLANE&RESET LOGIC			
Size B	Document Number Bali		Rev -1
Date:	Friday, February 13, 2009	Sheet 49 of 52	



Vendor check	Result	RD check	Source	Schmeatic	
			NB	0	01_BLOCK DIAGRAM
			NB	Δ	02_Table of Content
ICS ?	Modify ICS 6/25,26		New	0	03_Clock Gen CY28647->Realtek (need check solution)
			NB	0	04_Penryn(1/3)-AGTL+
			NB	0	05_Penryn(2/3)-PWR
Intel			NB	0	06_Penryn(3/3)-GND&Bypass
(1)First	Modify		NB	0	07_Penryn(4/4)-XDP PORT
FB 6/23	in 6/24		NB	0	08_Cantiga(1)-HOST I/F
			NB	0	09_Cantiga(2)-DDR3 A/B CH
			NB	0	10_Cantiga(3)-DMI/PM/CFG
			NB	0	11_Cantiga(4)-VGA/LVDS/TV
			NB	0	12_Cantiga(5)-PWR1
			NB	0	13_Cantiga(6)-PWR2
			NB	0	14_Cantiga(7)-GND
			NB	0	15_DDRIII-SODIMM SLOT1
			NB	0	16_DDRIII-SODIMM SLOT2
			YAMA	0	17_CRT CONN-> No need
			remove		18_VGA IN(1/2)-RGB IN->No need
			remove		19_VGA IN(2/2)-NT68665H->No nee
			NB/NEW	0	20_LCD CNN/ Lid SW
			remove		21_HDMI->no need
			NB	0	22_ICH9(1/4)-PCI /INT
			NB	0	23_ICH9(2/4) LAN/HD/IDE/LPC/RTC
	Modify in 6/20		NB	0	24_ICH9(3/4) PM,USB,GPIO
			NB	0	25_ICH9(4/4) POWER&GND
			New	0	26_THERMAL EMC2102-> Fan
			New	0	27_USB I/O / Modem
			New	0	28_HD/CDROM I/F+USB device
JM380	6/19 Modify 6/20		New	0	29_R5C833/PCI(1/2)-> Jmicon Solution
			New	0	30_R5C833/IEEE1394/SD/BT(2/2)
			NB	0	31_MINI CARD CONN(1,2)
			remove		32_New Card
Lan	6/26 Modify 6/26		New	Δ	33_LAN BCM5906M
			New	0	34_LAN/New Card->Riser Card
Realtek			New	0	35_AUDIO CODEC ALC888S-> ALC262
6/20,23	Modify 6/22,24		New	0	36_AUDIO AMP/Speaker
TI 6/18-24	Modify 6/25		New	0	37_AUDIO HP_JK/ MIC_JK/SUBWOF
SMSC 6/20	Modify 6/27		New	0	38_KBC WPCE8765C-> SIO
			New	0	39_KB /TP /Lanuch Board
			No		40_CIR / SPI ROM / LEDs-> Power Sequence
			No		41_SWITCHs / DEBUG-> Reset
			NB/New	No	42_Power Block Diagram
TI 6/17	Modify 6/18		NB	0	43_PW_5V_S5/3V_S5(TPS51120)
			NB	0	44_PW1D05V_S0/1D5V_S3(TPS51124)
			NB	0	45_LDO 1D8V/0D75V
ON 6/17	Modify 6/18		NB	Δ	46_PW_CPU_CORE(ADP3207A)
TI 6/25	Modify 6/24-25		New	0	47_CHARGER MAX8725-> +12V
			NB	V	48_AD / BATT CONN
					49_PWR PLANE & RESET LOGIC
					50_VGA MXM CONN
					51_SMALL BD CONN->check List
					52_LVDS SWITCH->Power Map

V finish

0 most
Δ half

X not yet

No no change

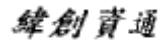
Check MxM spec: OK

NB Δ 49_PWR PLANE & RESET LOGIC
NB 0 50_VGA MXM CONN
New 0 51_SMALL BD CONN->check List
New V 52_LVDS SWITCH->Power Map

Need check Spec

Need check Amplify
Need check Amplify

LT72

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
SMALL BD CONN	
Size	Document Number
A3	Bali
Date:	Rev
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Sheet	of
51	52

Adaptor
+19.5VSB

Without MXM	11.1A	216.5W	140W	119W
With MXM	13.4A	261W	170W	144W

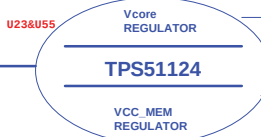
65% 55%

CPU: 2.45A

Memory, NB: 1.43A

+19.5V
2.45A

+19.5V
1.43A



U39

NB CPU	
VCORE	35A
VTT	4.5A

DDR3 V_1P5 (6A)

DDR III DIMM

1.5V VDD/VDDQ (S0, S1)	6A
0.9V VTT(S0)	1.2A

U38 NB GMCH

1.05V VTT	1.1A
1.05V VTT S0	2.2A
1.25/1.05V VCC3_3	1.2A
3.3V VCC3_3	0.12A
1.8V VCC3_3	0.01A
1.5V VTT S0	0.2A
1.8V VTT S0	0.4A

U36 SB ICH9M

1.05V VTT	1.2A
1.5V VTT	2.4A
3.3V VccCL3_3	0.4A
3.3V VccCL3_3	0.4A
3.3V VccSus3_3	0.2A

U40 ETHERNET

3.3V TBD	
2.5V TBD	
1.2V TBD	

U48

USB X4 FR	USB X4 RL	2XPS/2
VDD 5V Dual 2.0A	VDD 5V Dual 2.0A	5V Dual 1.0A

U8 SUPER I/O

VCC3_3	+3.3V DUAL 18mA
--------	-----------------

U51 HD AUDIO CODEC

+3.3V 40mA	
+5V 52mA	

Inverter: ?1.5A

MXM ?3A

HDD/ODD: 1A

V_1P5_MEM (S0, S1, S3) 2.6A

X16 PCIE

3.3V	3.0A
12V	5.5A

PCIE x1

3.3V	3.0A
12V	0.5A
3.3V DUAL	0.375A

IEEE1394/CARDBUS

3.3V 0.3A	
-----------	--

FAN: 0.2A
MB: 0.5A
HDD/ODD: 2A
Buzzer: 2A

NB/SB: 0.6A
LAN: 1A
MB: 1A
PCI-E: 2.8A

U35 Jmicron380

NB/SB: 0.6A
MB: 1A
PCI-E: 2.8A

NB/SB: 0.2+2.4A

VCC5_SB MOS 5V_S0 4.5A

VCC3_SB MOS 3D3V_S0 5.4A

U35 3.3V DUAL REGULATOR CEM2939A 1D8V_S0

1D5V_S3 MOS 1D5V_S0 4.4A

V_1P5_MEM (S0, S1, S3) MOS 1D5V_S0 2.6A

VCC_1P5_ICH (S0, S1) 1P5_S0 (S0, S1)

VCC_1P5_ICH (S0, S1) 1P5_S0 (S0, S1)

VCC_1P5_ICH (S0, S1) 1P5_S0 (S0, S1)

VCC_1P5_ICH (S0, S1) 1P5_S0 (S0, S1)

VCC_1P5_ICH (S0, S1) 1P5_S0 (S0, S1)

With MXM 6.05A
Without MXM 3.7A

With MXM 8.2A
Without MXM 5.1A
8.5A

MXM ?0A



VCC5_SB MOS VCC5_USB 4A
USB: 4A

U35 3D3V_S5 LDO 1D8V_S5