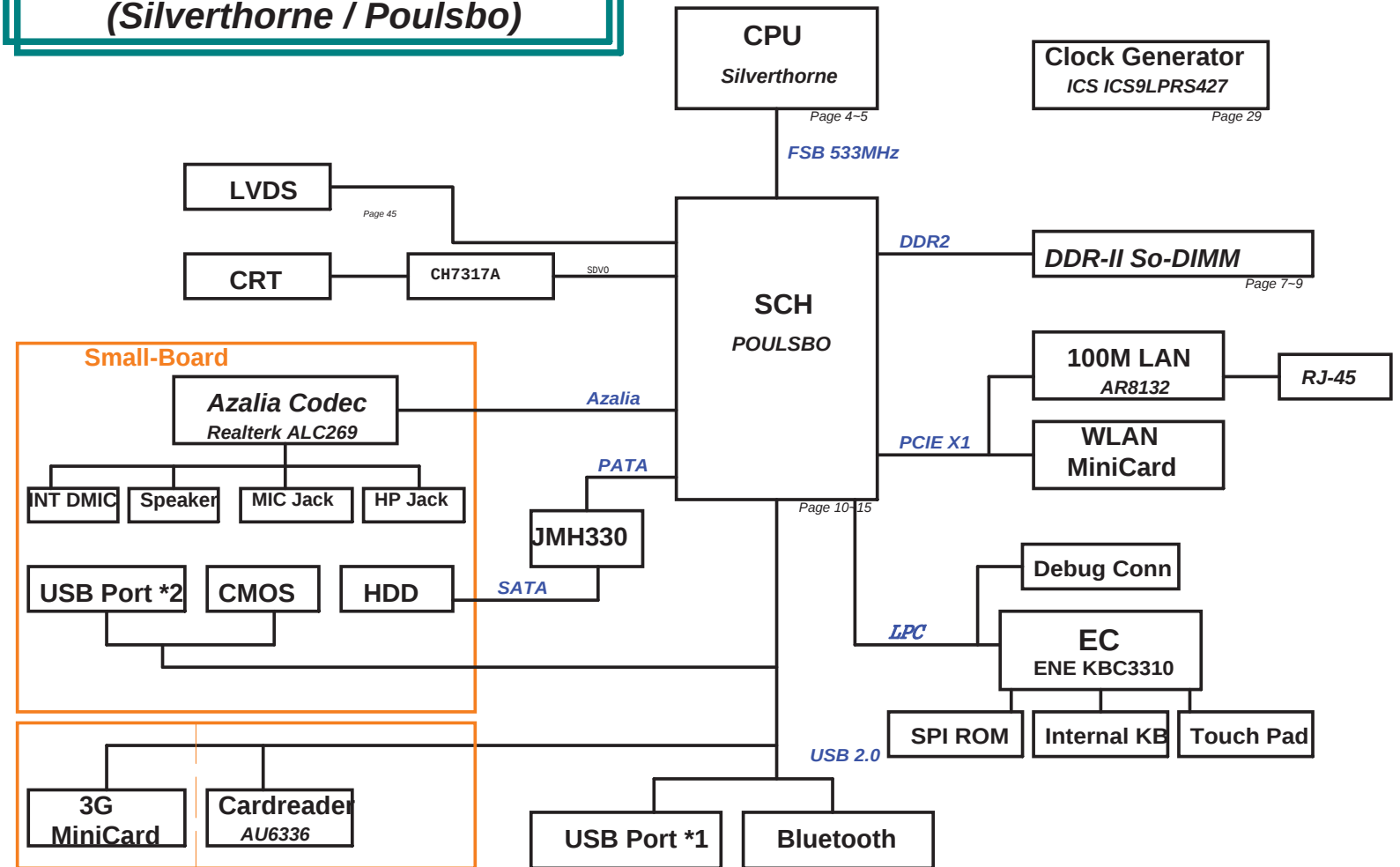


01_BLOCK DIAGRAM
02_SCH GPIO Setting
03_EC Pin Define
04_Power Sequense DC
05_Power Sequence AC
06_Power Sequence Description
07_Clock Gen_ICS9LPR427
08_CPU-SILVERTHORNE (1)
09_CPU-SILVERTHORNE (2)
10_CPU-SILVERTHORNE (3)
11_SCH_Poulsbo_HOST (1)
12_SCH_Poulsbo_DDR2 (2)
13_SCH_Poulsbo_LVDS/SDVO (3)
14_SCH_Poulsbo_PM/USB/IDE/AZ (4)
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17_SCH_Poulsbo_GND (7)
18_DDR2_SODIMM
19_DDR2_Termination
20_CH7317_SDVO_CRT
21_Onboard VGA
22_LCD Conn_LID
23_3.5G
24_Mini WIFI
25_Bluetooth_BT253
26_FAN_THERMAL SENSOR
27_LAN_Atheros AR8113/AR8132
28_RJ45
29_Small brd Conn
30_PATA TO SATA
31_USB Port
32_EC_ENE KB3310
33_SPI_ROM_Debug Conn
34_Reset Map
35_KB_Touch Pad
36_
37_Discharge
38_PWR Jack
39_Screw Hole
40_EMI
41_Power Flow
42_Vcore
43_Power System
44_Power_+1.8V & VTTDDR
45_Power_VCCP
46_Power_+1.5VS & +2.5VS
47_Charger
48_Power_Load Switch
49_Power Latch
50_HISTORY

1101HA Block Diagram (Silverthorne / Poulsbo)



SCH GPIO SETTING

Pin	Pin Name	Connect to	Type	Power Well	S3	S4/ S5	Input/Output Set
U41	GPIOUS0	PM_LEVELDOWN#	I/O CMOS3.3	Sus	VIX-unknown	OFF	Output
N43	GPIOUS1	CPU_LEVELDOWN	I/O CMOS3.3	Sus	VIX-unknown	OFF	Output
N45	GPIOUS2	PM_PWRBTN#	I/O CMOS3.3	Sus	VIX-unknown	OFF	Input
R41	GPIOUS3/ USBCC	+VCCP_OV0	I/O CMOS3.3	Sus	VIX-unknown	OFF	output
G29	GPIO0	Strap CMC/ BT_Disable	I/O CMOS3.3	Core	OFF	OFF	Input
K30	GPIO1	CARD_READER_EN#	I/O CMOS3.3	Core	OFF	OFF	Output
F34	GPIO2	SIMCARD_IN#	I/O CMOS3.3	Core	OFF	OFF	iutput
G33	GPIO3	Strap CMC	I/O CMOS3.3	Core	OFF	OFF	Input
K36	GPIO4	3GLAN_OFF	I/O CMOS3.3	Core	OFF	OFF	Output
H36	GPIO5	MINICARD_EN#	I/O CMOS3.3	Core	OFF	OFF	Output
F36	GPIO6	DDR_MEM_CONFIG	I/O CMOS3.3	Core	OFF	OFF	Input
J31	GPIO7/ SLPIOVR#	SLPIOVR#	I/O CMOS3.3	Core	OFF	OFF	Output
H34	GPIO8/ PROCHOT#	CAMERA_EN	I/O CMOS3.3/ OD	Core	OFF	OFF	Output
K28	GPIO9/ EXTTS1#	WLAN_LED	I/O CMOS3.3	Core	OFF	OFF	Output

<Variant Name>

		Title : SCH GPIO Setting	
ASUSTek Computer INC.		Engineer: N/A	
Size A3	Project Name 1101HA	Rev 1.2	
Date: Tuesday, July 21, 2009		Sheet 2 of 50	

EC KB3310 GPIO SETTING

Pin	Pin Name	Signal Name	Type	Note
1	GPIO00/GA20	A20GATE	O	
2	GPIO01/KBRST#	RC_IN#	O	
6	GPIO04	HOTKEY_SW0#	I	Internal pull high
13	GPIO05/PCIRST#	BUF_RST#	I	
14	GPIO07	HOTKEY_SW1#(no use)		
15	GPIO08	EXT_SMI#	OD	10K pull high to +3VSB
16	GPIO0A	LID_EC_R#	I	Internal pull high
17	GPIO0B/ESB_CLK	PCB_ID0	I	
18	GPIO0C/ESB_DAT	PCB_ID1	I	
19	GPIO0D	LID_EC_L#(no use)	I	Internal pull high
20	GPIO0E/SCI#	KBC_SCI#	O	10K pull high to +3VSB
21	GPIO0F/PWM0	BL_PWM_DA	O	
23	GPIO10/PWM1	BATSEL#	I	Battery critical capacity
25	GPIO11/PWM2	PM_PWRBTN#	OD	Internal pull high in ICH
26	GPIO12/FANPWM1	FAN0_PWM	O	CPU Fan
27	GPIO13/FANPWM2	FAN1_PWM	O	VGA Fan
28	GPIO14/FANFB1	FAN0_TACH	I	CPU FanTach
29	GPIO15/FANFB2	FAN1_TACH	I	VGA FanTach
30	GPIO16/E51_TX	E51_TX	O	RS232 debug port
31	GPIO17/E51_RX	E51_RX	I	RS232 debug port
32	GPIO18	PWR_SW#	I	Internal pull high
34	GPIO19/PWM3	PS-ON	O	latch power
36	GPIO1A/NUMLED	NUM_LED#	O	
38	GPIO1D/CLKRUN#	LPC_CLKRUN#	O	
39	GPIO20/KSO0/TP_TEST	KSO0	O	
40	GPIO21/KSO1/TP_PLL	KSO1	O	
41	GPIO22/KSO2	KSO2	O	
42	GPIO23/KSO3	KSO3	O	
43	GPIO24/KSO4	KSO4	O	
44	GPIO25/KSO5	KSO5	O	
45	GPIO26/KSO6	KSO6	O	
46	GPIO27/KSO7	KSO7	O	
47	GPIO28/KSO8	KSO8	O	
48	GPIO29/KSO9	KSO9	O	
49	GPIO2A/KSO10	KSO10	O	
50	GPIO2B/KSO11	KSO11	O	
51	GPIO2C/KSO12	KSO12	O	
52	GPIO2D/KSO13	KSO13	O	
53	GPIO2E/KSO14	KSO14	O	
54	GPIO2F/KSO15	KSO15	O	
55	GPIO30/KSI0	KSI0	I	Internal pull high
56	GPIO31/KSI1	KSI1	I	Internal pull high
57	GPIO32/KSI2	KSI2	I	Internal pull high
58	GPIO33/KSI3	KSI3	I	Internal pull high
59	GPIO34/KSI4	KSI4	I	Internal pull high
60	GPIO35/KSI5	KSI5	I	Internal pull high
61	GPIO36/KSI6	KSI6	I	Internal pull high
62	GPIO37/KSI7	KSI7	I	Internal pull high
63	GPI38/AD0	BAT_A	I	
64	GPI39/AD1	BAT_B	I	
65	GPIO3A/AD2	BAT_C	I	
66	GPIO3B/AD3	BAT_D	I	
68	GPO3C/DA0	CHG_EN#	O	battery charger enabled

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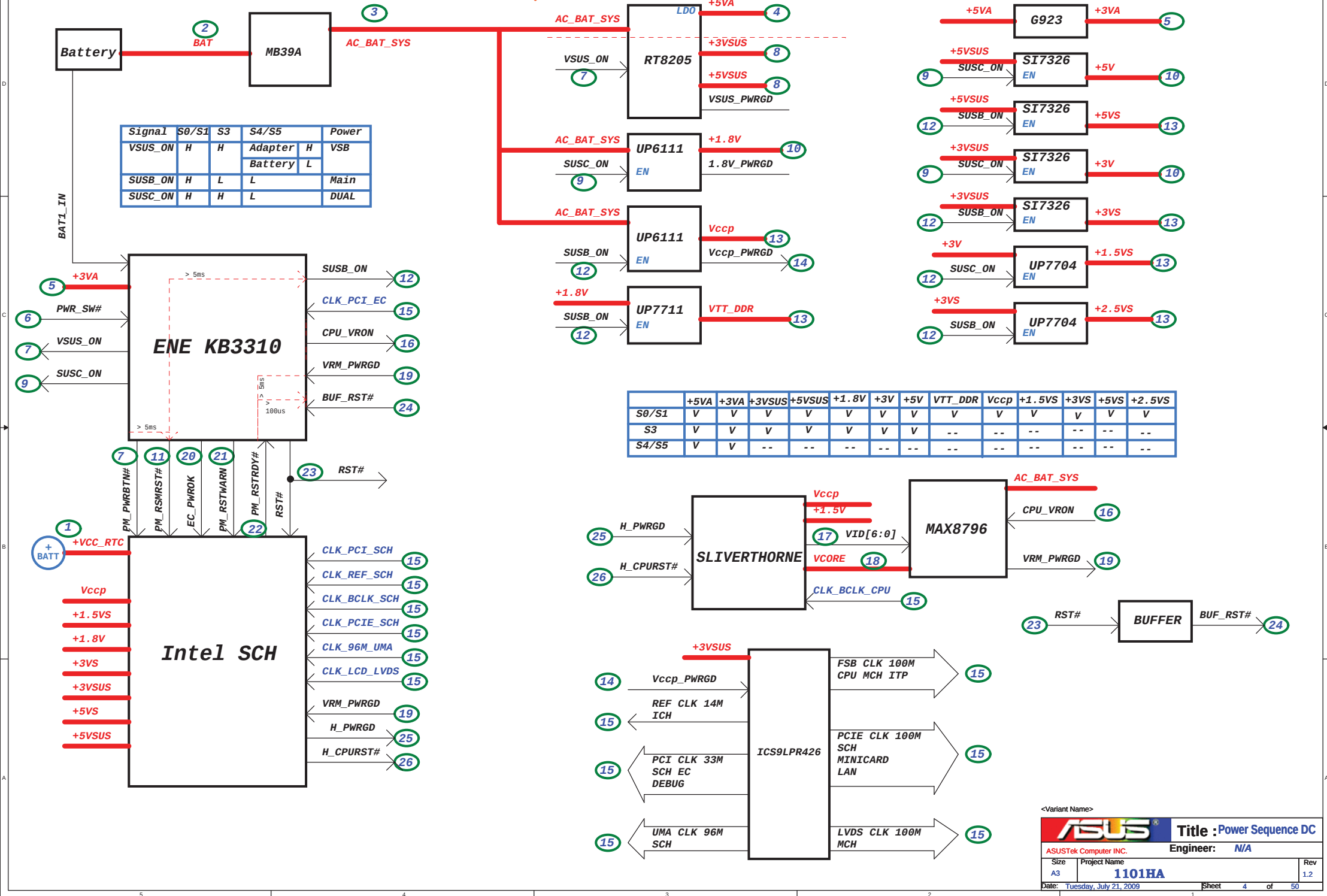
Pin	Pin Name	Signal Name	Type	Note
70	GPO3D/DA1	LCD_BACKOFF#	O	
71	GPO3E/DA2	THRO_CPU_VOLT#	O	
72	GPO3F/DA3	BAT_LL#	O	Battery Low Low
73	GPIO40	AC_OK	I	AC Adaptor Plug in
74	GPIO41	PM_RSMRST#	O	10K pull down to GND
75	GPI42	BAT_IN	I	Batt1 (Small/Internal): 1-present, 0-absent
76	GPI43	BAT2_IN	I	Batt2 (Small/Internal): 1-present, 0-absent
77	GPIO44/SC1	SMB0_CLK	I/OD	4.7K pull high to +3VA_EC
78	GPIO45/SDA1	SMB0_DAT	I/OD	4.7K pull high to +3VA_EC
79	GPIO46/SC2	SMB1_CLK	I/OD	10K pull high to +3V
80	GPIO47/SDA2	SMB1_DAT	I/OD	10K pull high to +3V
81	GPIO48/KSO16	KB_ID0	I	for KB type detection
82	GPIO49/KSO17	KB_ID1	I	for KB type detection
83	GPIO4A/PSCLK1	N.C.	O	
84	GPIO4B/PSDAT1	CRT_IN	I	
85	GPIO4C/PSCLK2	CRT_DACPWR_EN#	O	
86	GPIO4D/PSDAT2	CRTDAC_RST#	O	
87	GPIO4E/PSCLK3	TP_CLK	I/OD	10K pull high to +3V
88	GPIO4F/PSDAT3	TP_DAT	I/OD	10K pull high to +3V
89	GPIO50/SELIO#	CHG_LED_GREEN#	O	Green charger LED
90	GPIO52/E51_CS#	CHG_LED_UP#	O	Orange charger LED
91	GPIO53/CAPLED	CAP_LED#	O	
92	GPIO54	PWR_LED_UP	O	
93	GPIO55/SCRLLED	SCRL_LED#	O	
95	GPIO56	GS1_INT1(no use)	I	Internal pull high
97	GPIOA00/SDICS#	SPI_MODE#	O	4.7K pull down to GND
98	GPXOA01/SDICLK	SUSC_ON	O	
99	GPXOA02/SDIDO	VSUS_ON	O	
100	GPXOA03	CPU_VRON	O	
101	GPXOA04	SUSB_ON	O	
102	GPXOA05	CNT1_CHG#	O	batt1 (Big/External) charging enabled. Batt1 is discharging priority in AC mode.
103	GPXOA06	CNT1_DIS#	O	batt1 discharging enabled
104	GPXOA07	CNT2_CHG#	O	batt2 (Big/External) charging enabled. Batt2 is discharging priority in AC mode.
105	GPXOA08	CNT2_CHG#	O	batt2 discharging enabled
106	GPXOA09	SPI_WP#	O	
107	GPX0A10	OP_SD#	O	Audio OP
108	GPXOA11	BAT_LEARN	O	
109	GPXID0/SDIDI	PM_PWROK	O	Battery parallel, H:1P, L:2P~3P
110	GPXID1	RST#	O	
112	GPXID2	THRO_CPU	O	Active if CPU temperature over spec
114	GPXID3	PM_SLPRDY#	I	SLPRDY#,100K pull down to GND
115	GPXID4	SLPMODE	I	SUSC#,100K pull down to GND
116	GPXID5	VRM_PWRGD	I	Pull high to +3V
117	GPXID6	PM_RSTRDY#	I	
118	GPXID7	RSTWARN	O	
121	GPIO57	GS1_INT2(no use)	I	Internal pull high
126	GPIO58/SPICLK	SPI_CLK	O	
127	GPIO59/TEST_CLK	GS2_INT1(no use)	O	

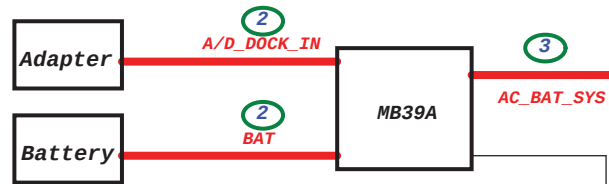
EC KB3310 Other Pin SETTING

Pin	Pin Name	Signal Name	Type	Note
3	SERIRQ	INT_SERIRQ	I/OD	10K pull high to +3V
4	LFRAME#	LPC_FRAME#	I	
5	LAD3	LPC_AD3	I/O	
7	LAD2	LPC_AD2	I/O	
8	LAD1	LPC_AD1	I/O	
9	VCC	+3VA	P	
10	LAD0	LPC_AD0	I/O	
11	GND	GND	P	
12	PCICLK	CLK_PCI_EC	I	
22	VCC	+3VA	P	
24	GND	GND	P	
33	VCC	+3VA	P	
35	GND	GND	P	
37	ECRST#	EC_RST#	I	100K pull high to +3VA_EC
67	AVCC	+3VA_AEC	P	
69	AGND	AGND	P	
94	GND	GND	P	
96	VCC	+3VA	P	
111	VCC	+3VA	P	
113	GND	GND	P	
119	RD#/SPIDI	SPI_SO	I	
120	WR#/SPIDO	SPI_SI	O	
122	XCLKI	K_XCLKI	I	
123	XCLKO	K_XCLKO	O	
124	V18R	V18R	P	Reserved 1uF to GND
125	VCC	+3VA	P	
128	SPICS#/SELMEM#	SPI_CS#	O	

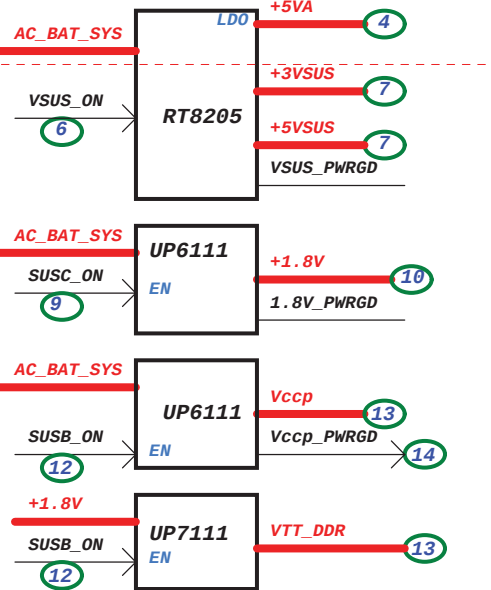
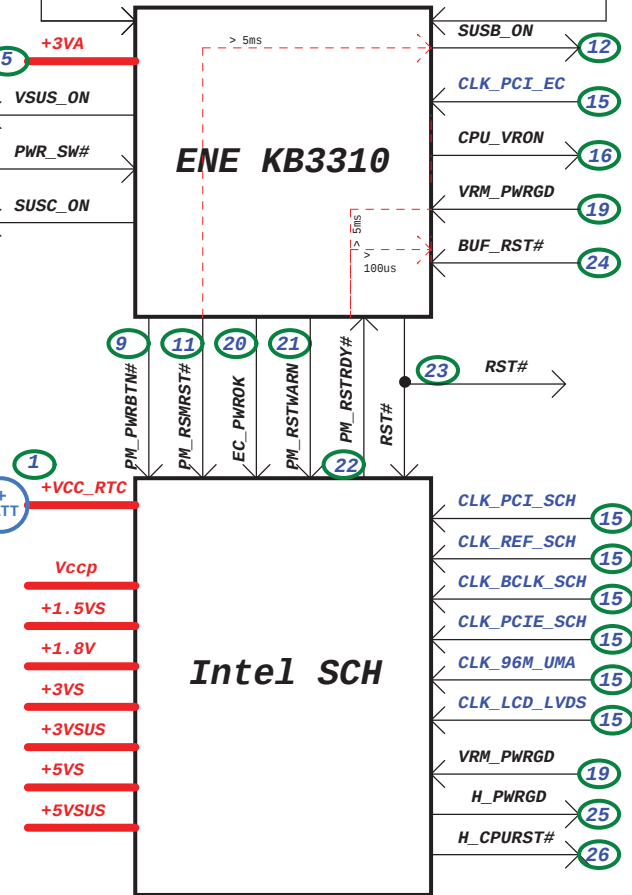
<Variant Name>

		Title : EC Pin Define	
ASUSTek Computer INC.		Engineer: N/A	
Size A3	Project Name 1101HA	Rev 1.2	
Date: Tuesday, July 21, 2009		Sheet	3 of 50

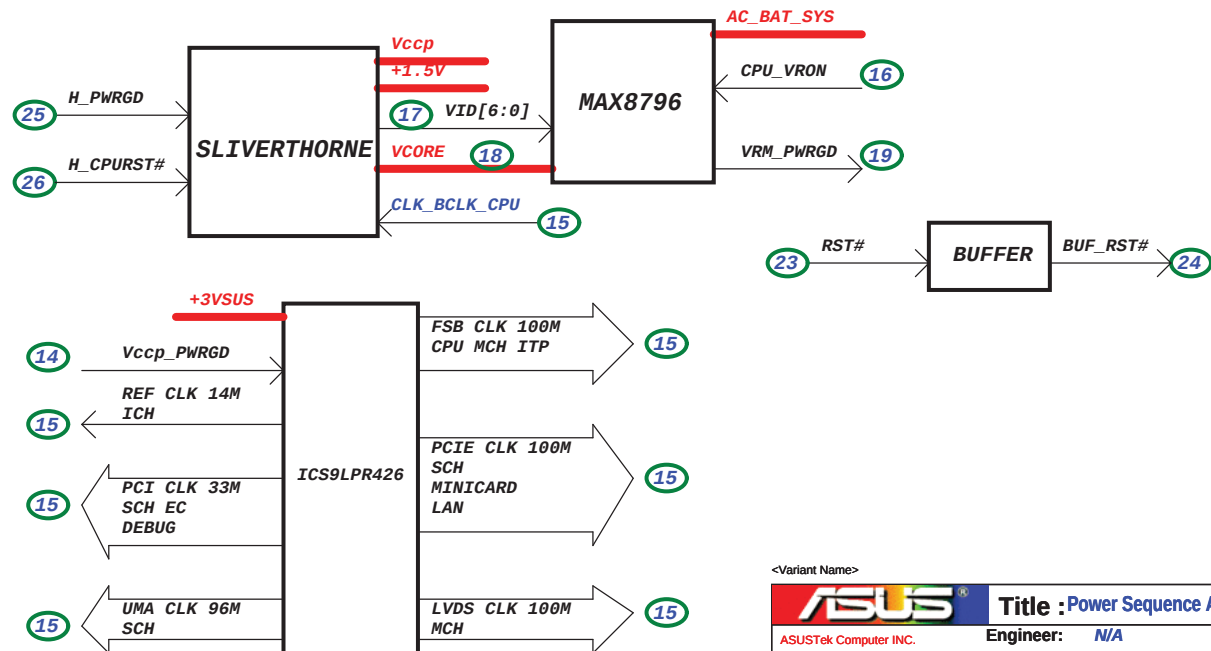
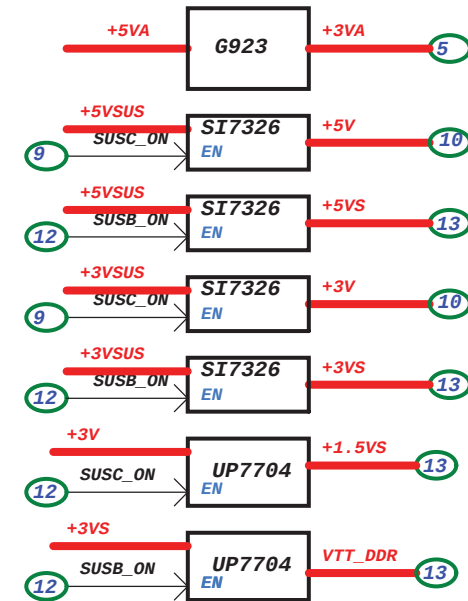




Signal	S0/S1	S3	S4/S5	Power
VSUS_ON	H	H	Adapter	VSB
			Battery	L
SUSB_ON	H	L	L	Main
SUSC_ON	H	H	L	DUAL



	+5VA	+3VA	+3VSUS	+5VSUS	+1.8V	+3V	+5V	VTT_DDR	Vccp	+1.5VS	+3VS	+5VS	+2.5VS
S0/S1	V	V	V	V	V	V	V	V	V	V	V	V	V
S3	V	V	V	V	V	V	V	--	--	--	--	--	--
S4/S5	V	V	V	V	--	--	--	--	--	--	--	--	--



S4/S5 to S0(Adapter Mode)

This sequence will occur whenever the system is in S4/S5 and the EC initiates a sleep exit sequence from S4/S5 to S0.

Initial EC state: VSUS_ON=0, SUSB_ON=0, SUSC_ON=0, A20GA=X, KBRST=X, CPU_VRON=0, ICH_PWROK=0, RSTWARN=0, and PM_RSMRST#=0, RESET#=0.

- 1.Waiting for AC_OK until adaptor power is good, then
- 2.At least **5mS** after AC_OK is asserted, EC asserts VSUS_ON to enable VSUS power.
- 3.At least **20mS** after VSUS power is stable, waiting for PWR_SW# until user is pressed. (Or waiting for SCH deasserted SLPRDY#, too?)
- 4.EC asserts RSTWARN.
- 5.SUSC_ON is asserted at least 20mS (de-bounce) after receiving PWR_SW#.
- 6.PM_RSMRST# is deasserted at least **5mS** after SUSC power is stable.
- 7.At least **5mS** after PM_RSMRST# is deasserted, SUSB_ON is enabled.
- 8.CPU_VRON is deasserted at least **100mS** after SUSB power is stable.
- 9.Waiting for CPUPWR_GD (VRM_PWRGD) until CPU_VRON power is stable.
- 10.At least **10mS** after receiving CPUPWR_GD, PM_PWROK is asserted, and then deasserts RSTWARN.
- 11.Waiting for RSTRDY# until deasserted by SCH.
- 12.RESET# can be deasserted at lease **100uS** after PM_PWROK is asserted.

S4/S5 to S0(Battery Mode)

This sequence will occur whenever the system is in S4/S5 and the EC initiates a sleep exit sequence from S4/S5 to S0.

Initial EC state: VSUS_ON=0, SUSB_ON=0, SUSC_ON=0, A20GA=X, KBRST=X, CPU_VRON=0, ICH_PWROK=0, RSTWARN=0, and PM_RSMRST#=0, RESET#=0.

- 1.Waiting for BAT_IN until battery power is good, then
- 2.Waiting for PWR_SW# until user is pressed.
- 3.EC asserts VSUS_ON to enable VSUS power.
- 4.At least **20mS** after VSUS power is stable.
- 5.EC asserts RSTWARN.
- 6.SUSC_ON is asserted at least 20mS (de-bounce) after receiving PWR_SW#.
- 7.PM_RSMRST# is deasserted at least 5mS after SUSC power is stable.
- 8.At least 5mS after PM_RSMRST# is deasserted, SUSB_ON is enabled.
- 9.CPU_VRON is deasserted at least 10mS after SUSB power is stable.
- 10.Waiting for CPUPWR_GD (VRM_PWRGD) until CPU_VRON power is stable.
- 11.At least 10mS after receiving CPUPWR_GD, PM_PWROK is asserted, and then deasserts RSTWARN.
- 12.Waiting for RSTRDY# until deasserted by SCH.
- 13.RESET# can be deasserted at lease 100uS after ICH_PWROK is asserted.

S0 to S3/S4/S5

This sequence will occur when system entry to sleep states, or all power planes are shut down.

Initial EC state: VSUS_ON=1, SUSB_ON=1, SUSC_ON=1, CPU_VRON=1, ICH_PWROK=1, and PM_RSMRST#=1, RESET#=1, RSTWARN=0, PM_PWRBTN#=1.

- 1.Waiting for PWR_SW# until user is pressed (go to 2), or waiting for SLPRDY# is asserted (go to 3).
- 2.At least **20mS** after PWR_SW# is asserted, EC asserts PM_PWRBTN# (50mS width) to SCH.
- 3.Waiting for SLPRDY# until has been asserted.
- 4.EC asserts RSTWARN to SCH to begin internal sequence.
- 5.SCH asserts RSTRDY# to EC to indicate all outstanding transactions are completed.
- 6.EC asserts RESET# after detecting RSTRDY# asserted.
- 7.EC deasserts ICH_PWROK.
- 8.EC deasserts SUSB_ON and CPU_VRON to turn off power planes.
- 9.EC asserts PM_RSMRST#.
- 10.EC deasserts SUSC_ON to turn off the other power planes.
- 11.EC deasserts VSUS_ON if in battery mode.
- 12.EC deasserts RSTWARN to save more power.

This completes the entry to S3 (SLPMODE=1).

If SLPMODE=0, this indicates S4/S5 was the desired state, EC takes additional actions:

Power Sequence Description: S3 to S0

This sequence will occur in S3, and wake event is detected by EC or SCH.

Initial EC state: SUSB_ON=0, CPU_VRON=0, ICH_PWROK=0, PM_RSMRST#=1, PM_PWRBTN#=1, and VSUS_ON=1, RSTWARN=1, SUSC_ON=1, RESET#=0.

- 1.For internal wake event, SCH deasserts SLPRDY# to EC, than 4.
- 2.For external wake event (PWR_SW#, keyboard wake up), then
- 3.EC asserts PM_PWRBTN# at least 50mS to wake SCH, and waiting for SLPRDY# until SCH deasserted.
- 4.EC asserts SUSB_ON to enable SUSB power.
- 5.CPU_VRON is deasserted at least **100mS** after SUSB power is stable.
- 6.Waiting for CPUPWR_GD (VRM_PWRGD) until CPU_VRON power is stable.
- 7.At least **5mS** after receiving CPUPWR_GD, ICH_PWROK is asserted.
- 8.Deasserts RSTWARN after ICH_PWROK is asserted.
- 9.RESET# can be deasserted **100uS** after RSTWARN is deasserted.

Warm Reset (SLPMODE=1)

The warm reset sequence results in reset without remove any power supplies.

Initial EC state: SUSB_ON=1, CPU_VRON=1, ICH_PWROK=1, PM_RSMRST#=1, PM_PWRBTN#=1, and VSUS_ON=1, RSTWARN=1, SUSC_ON=1, RESET#=1.

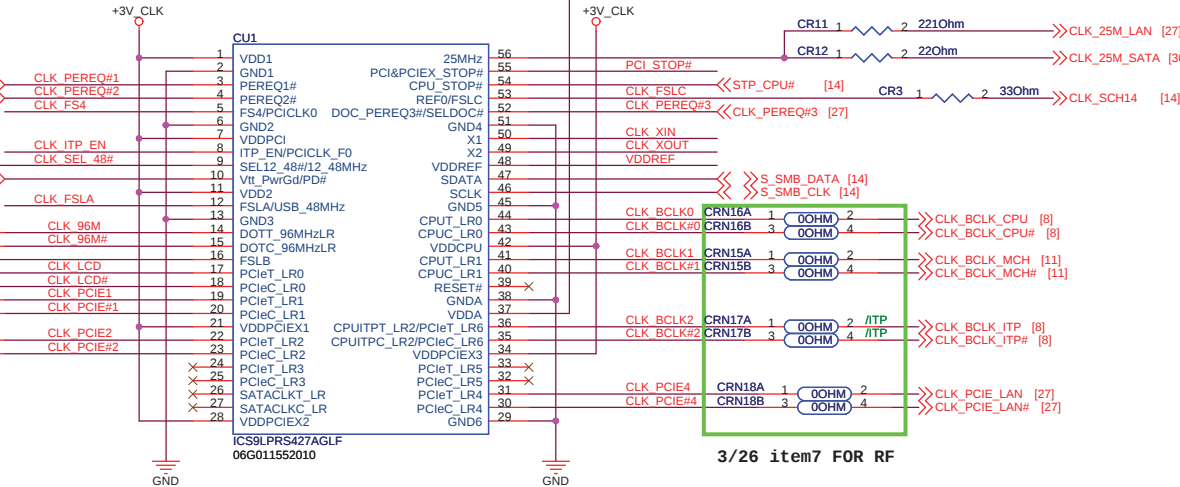
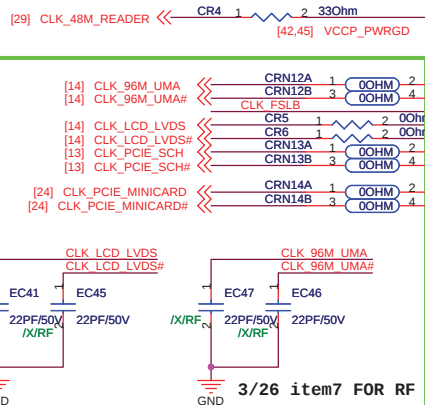
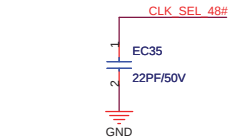
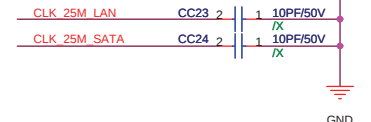
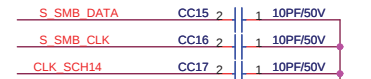
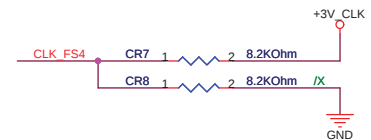
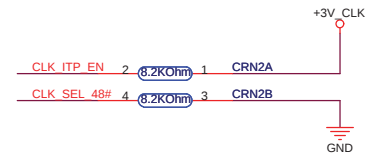
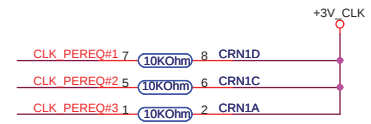
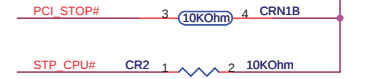
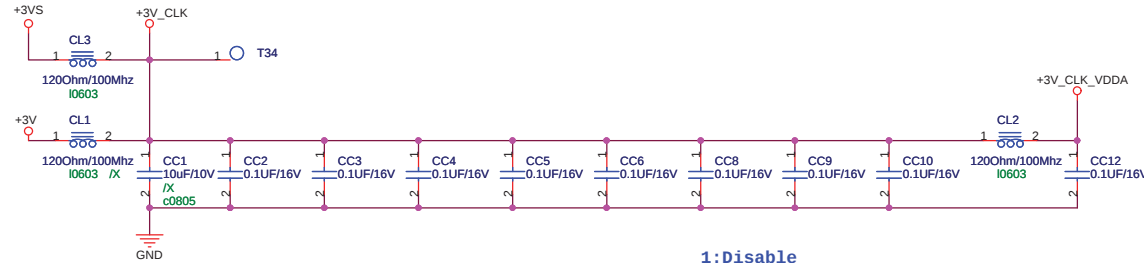
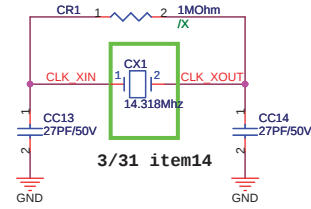
- 1.SCH asserts RSTRDY# at the same time as driving SLPMODE=1 to EC.
- 2.EC asserts RSTWARN to SCH.
- 3.EC asserts RESET# for **1200uS** to SCH after asserts RSTWARN.
- 4.EC deasserts RSTWARN.
- 5.EC deasserts RESET# after at least **100uS** delay from RSTWARN.

Cold Reset (SLPMODE=0)

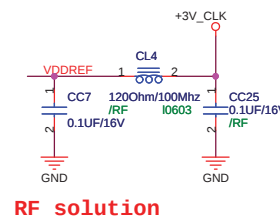
The cold reset sequence results in a power cycling of all but the RTC power well.

Initial EC state: SUSB_ON=1, CPU_VRON=1, ICH_PWROK=1, PM_RSMRST#=1, PM_PWRBTN#=1, and VSUS_ON=1, RSTWARN=1, SUSC_ON=1, RESET#=1.

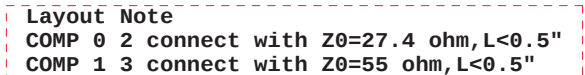
- 1.SCH asserts RSTRDY# at the same time as driving SLPMODE=0 to EC.
- 2.EC asserts RSTWARN to SCH.
- 3.EC asserts RESET# to SCH after asserts RSTWARN.
- 4.EC deasserts PM_PWROK and disables SUSB_ON and CPU_VRON power.
- 5.EC asserts PM_RSMRST# after CPU_VRON power is off.
- 6.EC disables SUSC_ON power for 3-5 seconds.
- 7.S4/S5 to S0 sequence is automatically followed to bring the system back to S0 when SUSC_ON power is enable.

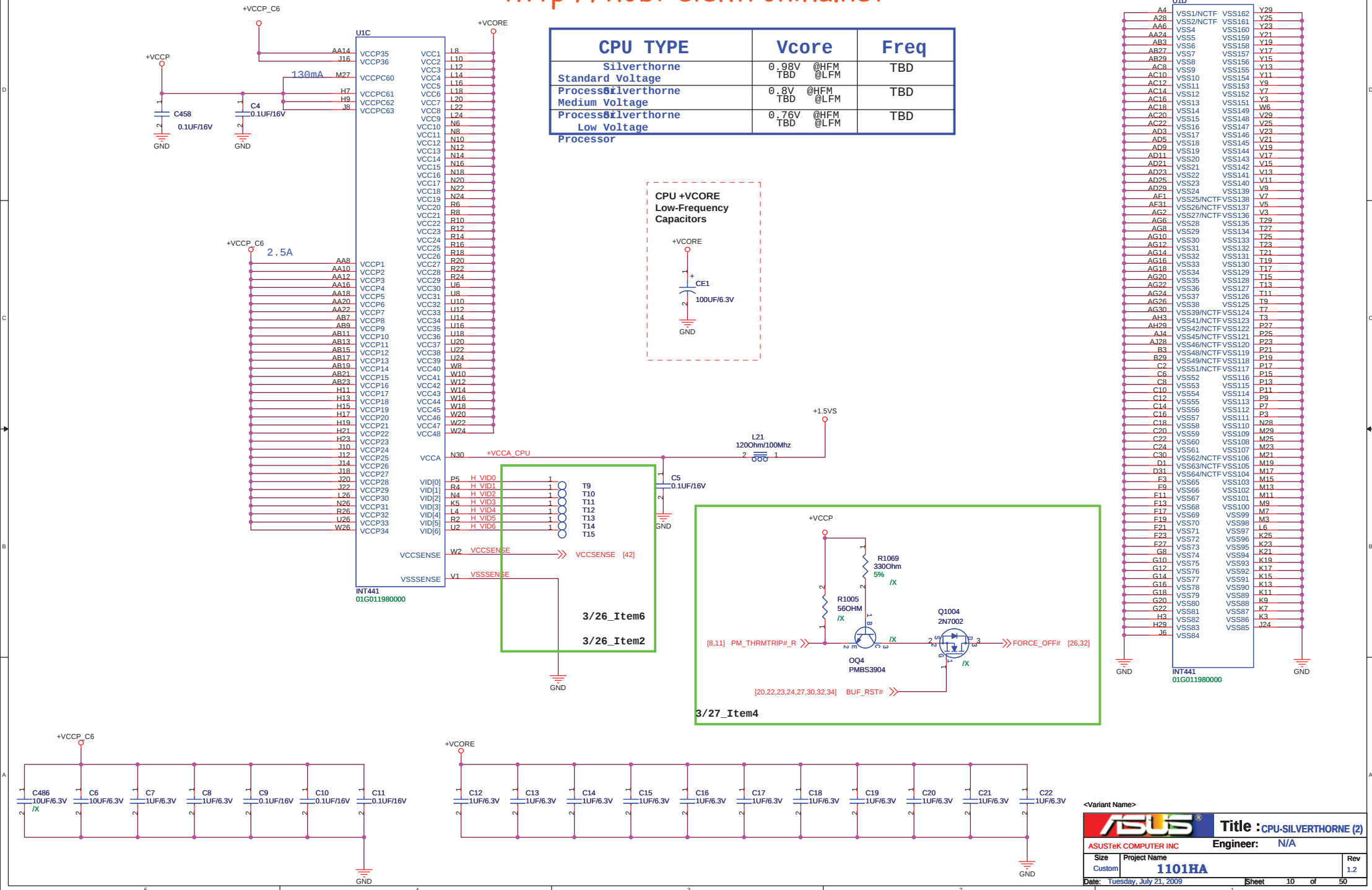


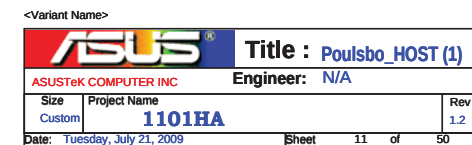
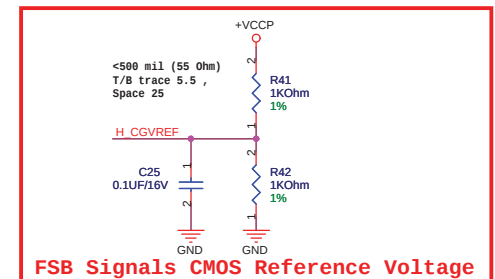
FSC	FSB	FSA	CPU	PCIE
0	0	1	133	100
1	0	1	100	100

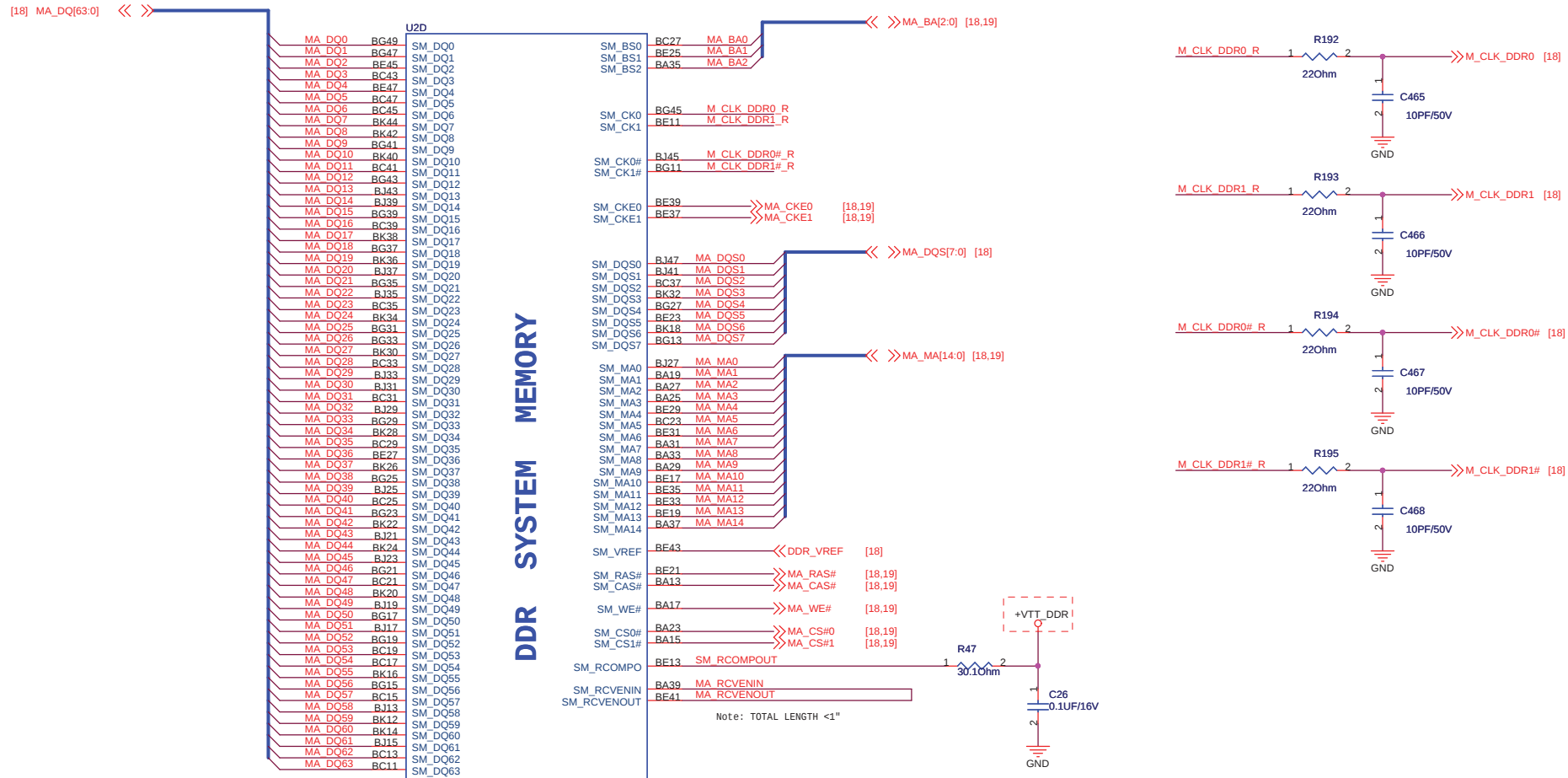


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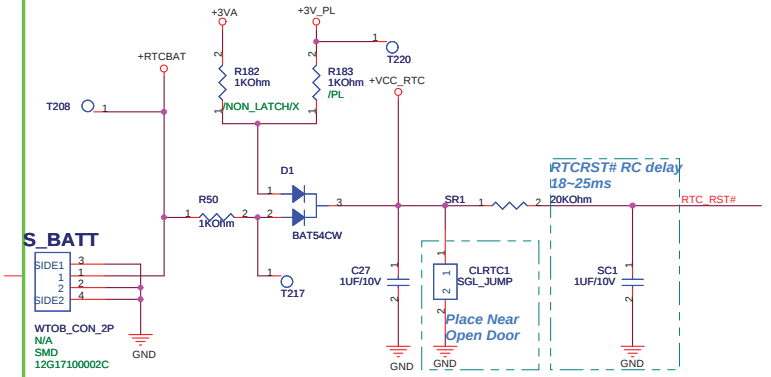


02G010018700

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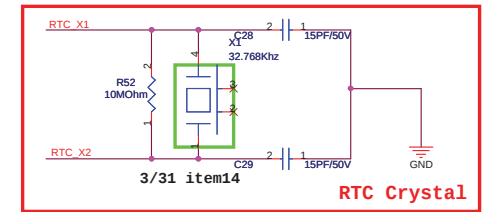
ASUS		Title : Poulsbo_DDR2 (2)	
ASUSTek Computer INC.		Engineer: N/A	
Size Custom	Project Name 1101HA		Rev 1.2
Date: Tuesday, July 21, 2009		Sheet	12 of 50

3/26_Item6 Modify RTC circuit

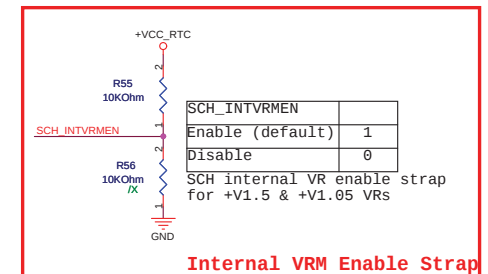


RTC Battery & RTC Reset

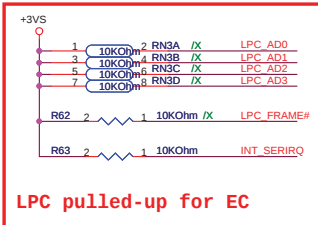
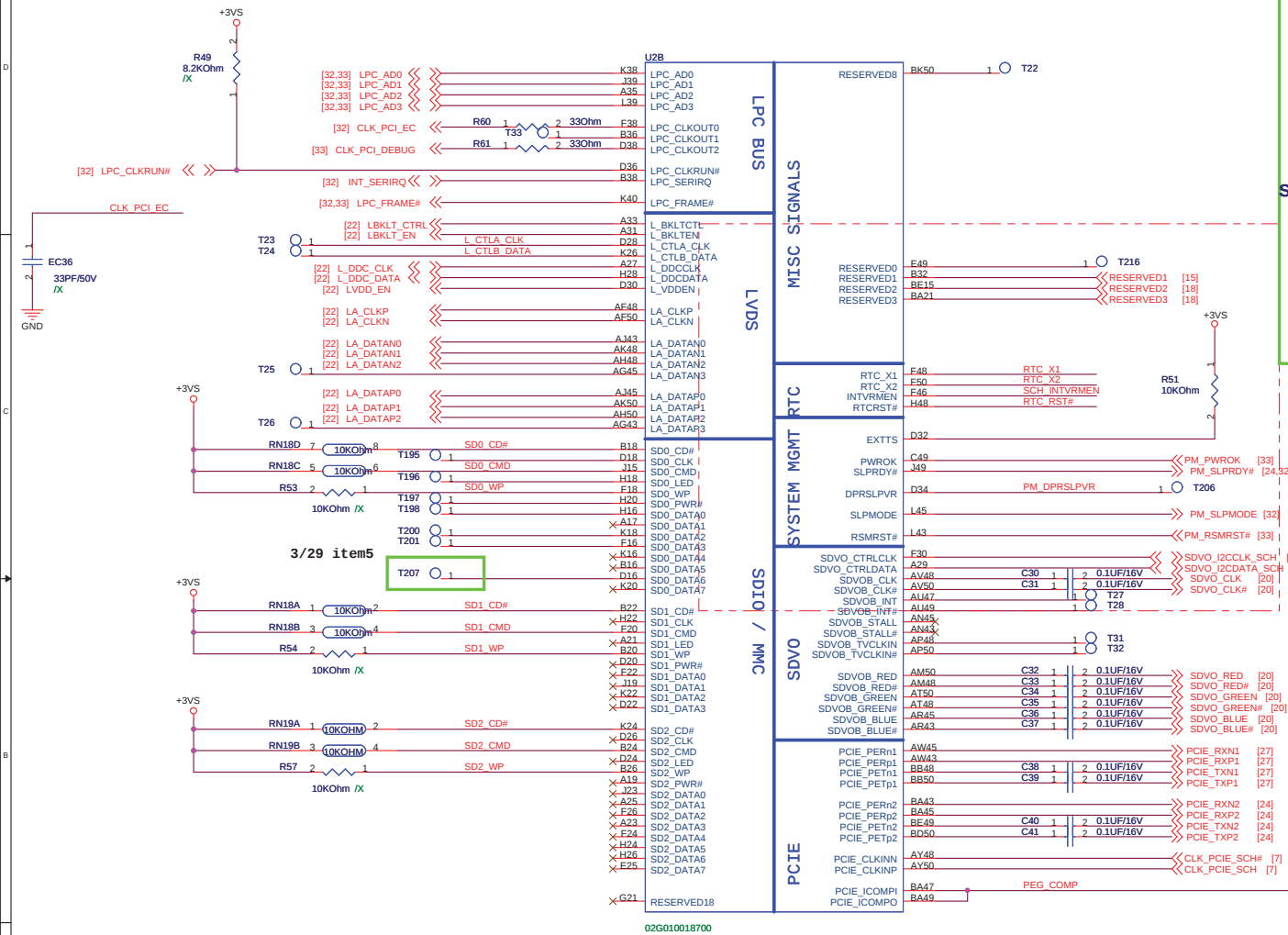
PM_SLPDRY#	PM_SLPMODE	System Behavior
0	1	SCH ready to enter S3
0	0	SCH ready to enter S4/S5



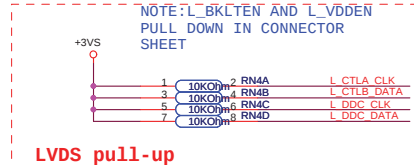
RTC Crystal



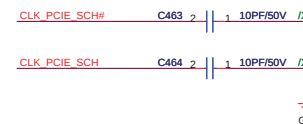
Internal VRM Enable Strap



LPC pulled-up for EC



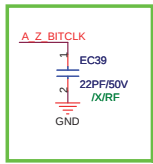
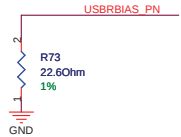
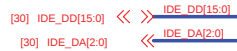
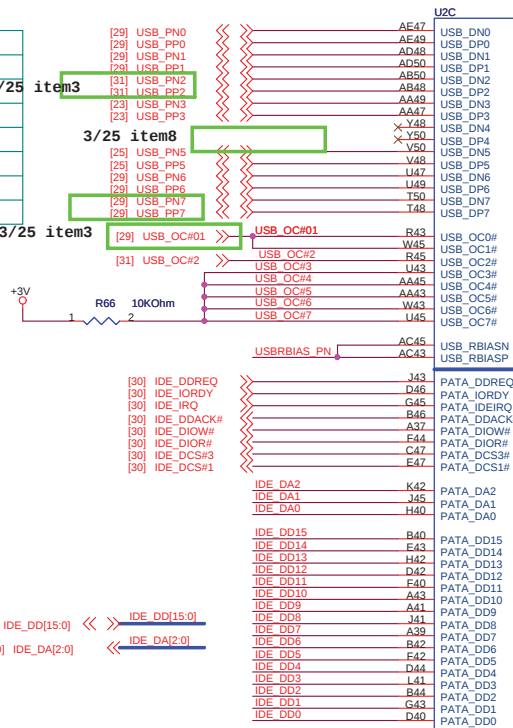
LVDS pull-up



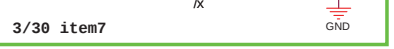
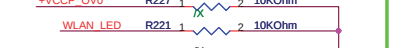
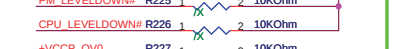
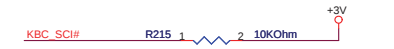
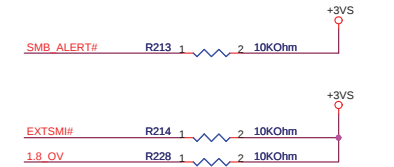
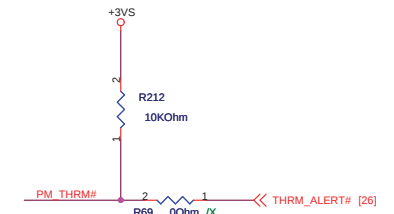
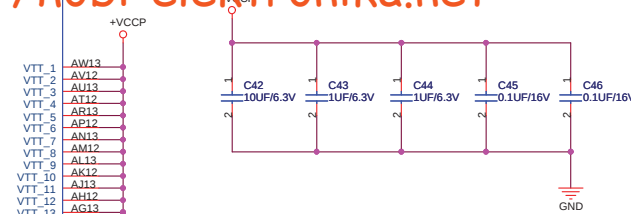
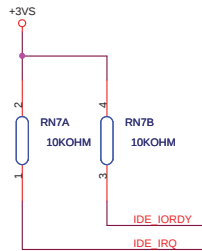
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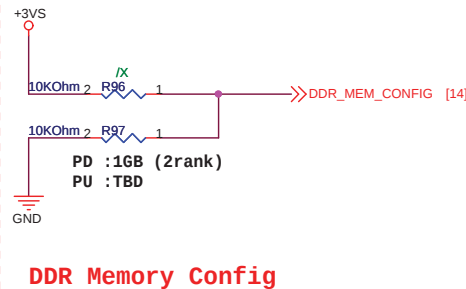
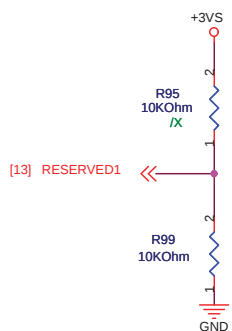
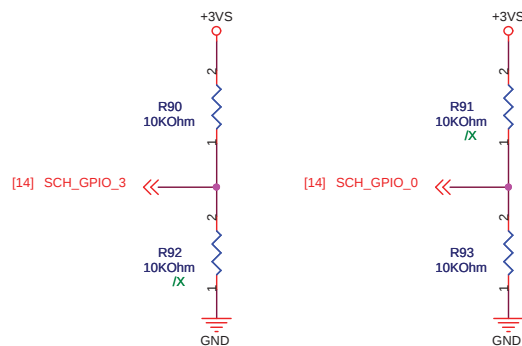
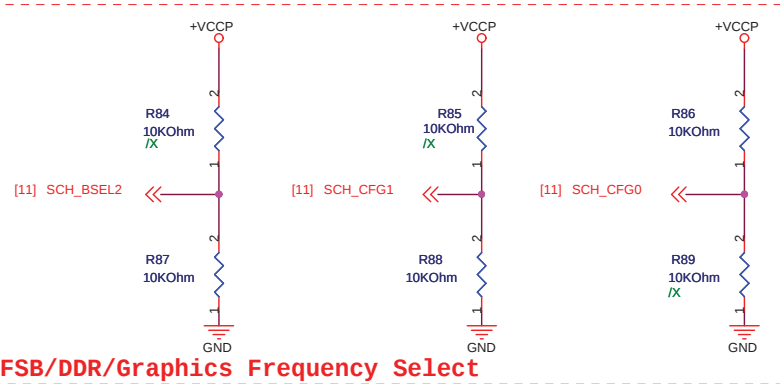
ASUS		Title: Poulsbo LVDS/SDVO	
ASUSTek COMPUTER INC		Engineer: N/A	
Size	Project Name	Rev	
Custom	1101HA	1.2	
Date: Tuesday, July 21, 2009		Sheet 13 of 50	

USB 0	USB PORT	3/25
USB 1	USB PORT	
USB 2	USB PORT	
USB 3	3.5G	
USB 4		
USB 5	Bluetooth	
USB 6	Camera	
USB 7	Card Reader	



3/26_Item7 RF
4/6_Item5

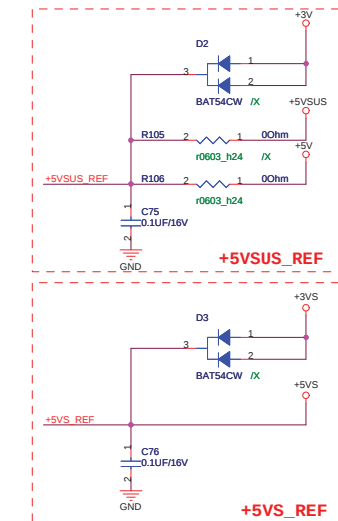


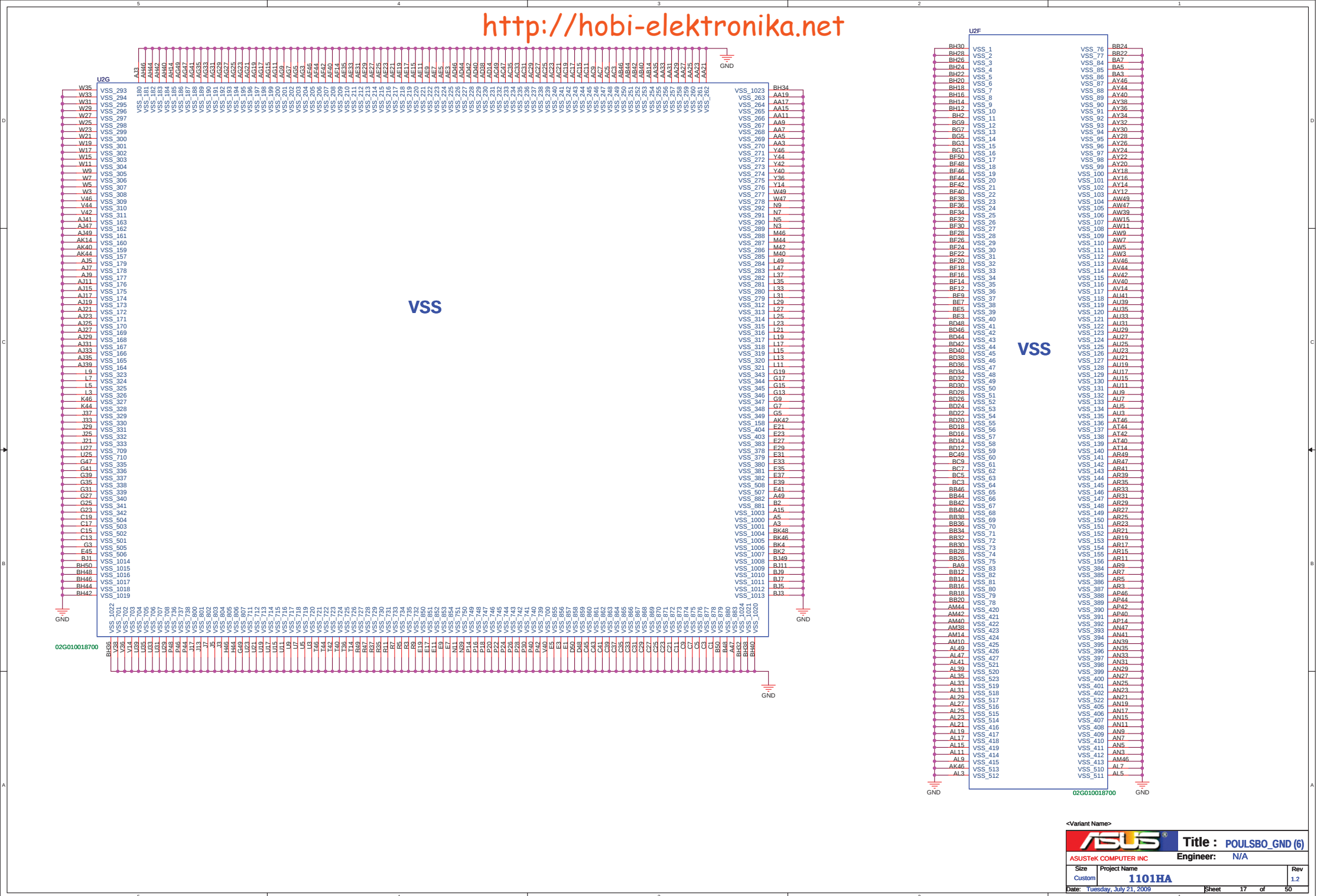


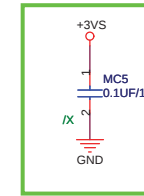
Strap Function	Signal Name			Strap		Comment
FSB/DDR Frequency Select Graphics Frequency Select	SCH_BSEL2	SCH_CFG1	SCH_CFG0	Gfx_Freq	FSB	Note: Clock Frequencies are in Mhz Default Frequency determined by FSB speed
	0	0	0	200	400	
	0	0	1	200	533	
CMC (Chipset Microcode) Base Address	GPIO3		GPIO0	Address		Selects the starting address that the CMC will use to start fetching code. (GPIO3 is the most significant)
	0		0	0xFFFFB0000		
	0		1	0xFFFFC0000		
	1		0	0xFFFFD0000 (default)		
	1		1	0xFFFFE0000		
LPC_CLKOUT[0] Buffer Strength	RESERVED1			Value		Selects the drive strength of the LPC_CLKOUT[0] clock.
	0			Reserved		
	0			1 Load (Default)		
	1			Reserved		
	1			2 Loads		

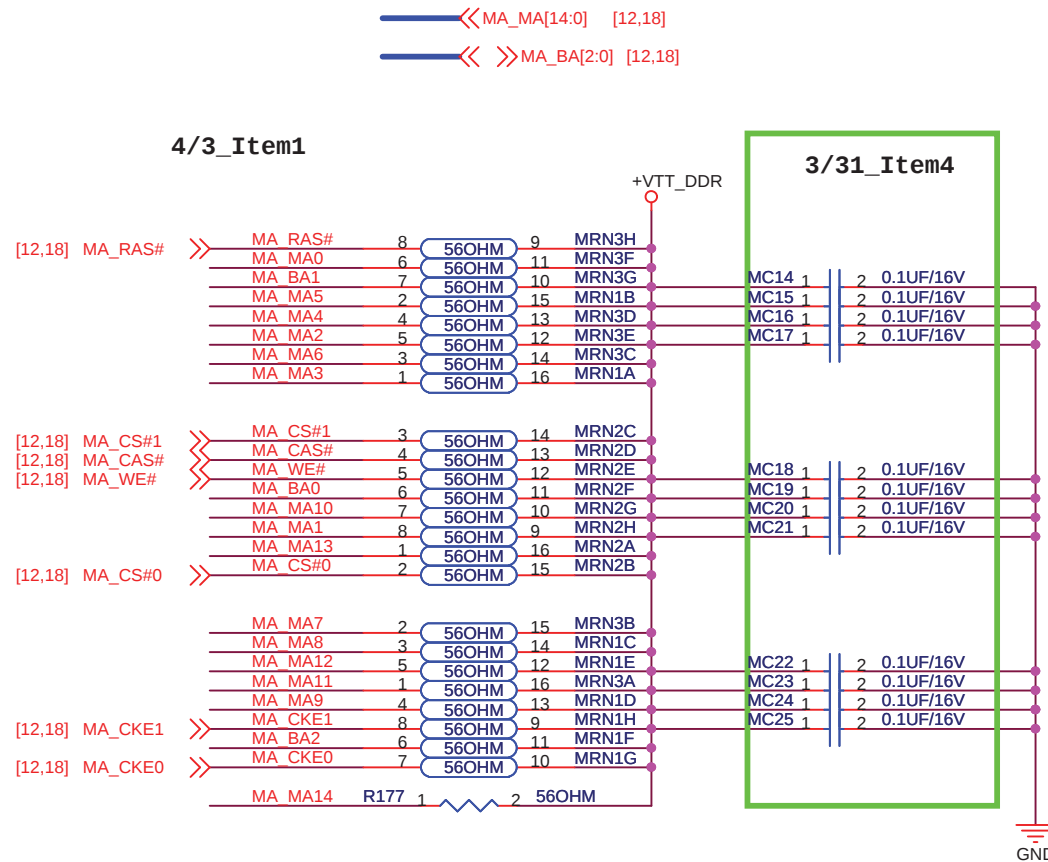
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ASUS		Title :POULSBO_STRAP(5)	
ASUSTek Computer INC.		Engineer: N/A	
Size B	Project Name 1101HA		Rev 1.2
Date: Tuesday, July 21, 2009		Sheet 15 of 50	









<Variant Name>



Title : DDR2_Termination

ASUSTek Computer INC.

Engineer: N/A

Size
A4

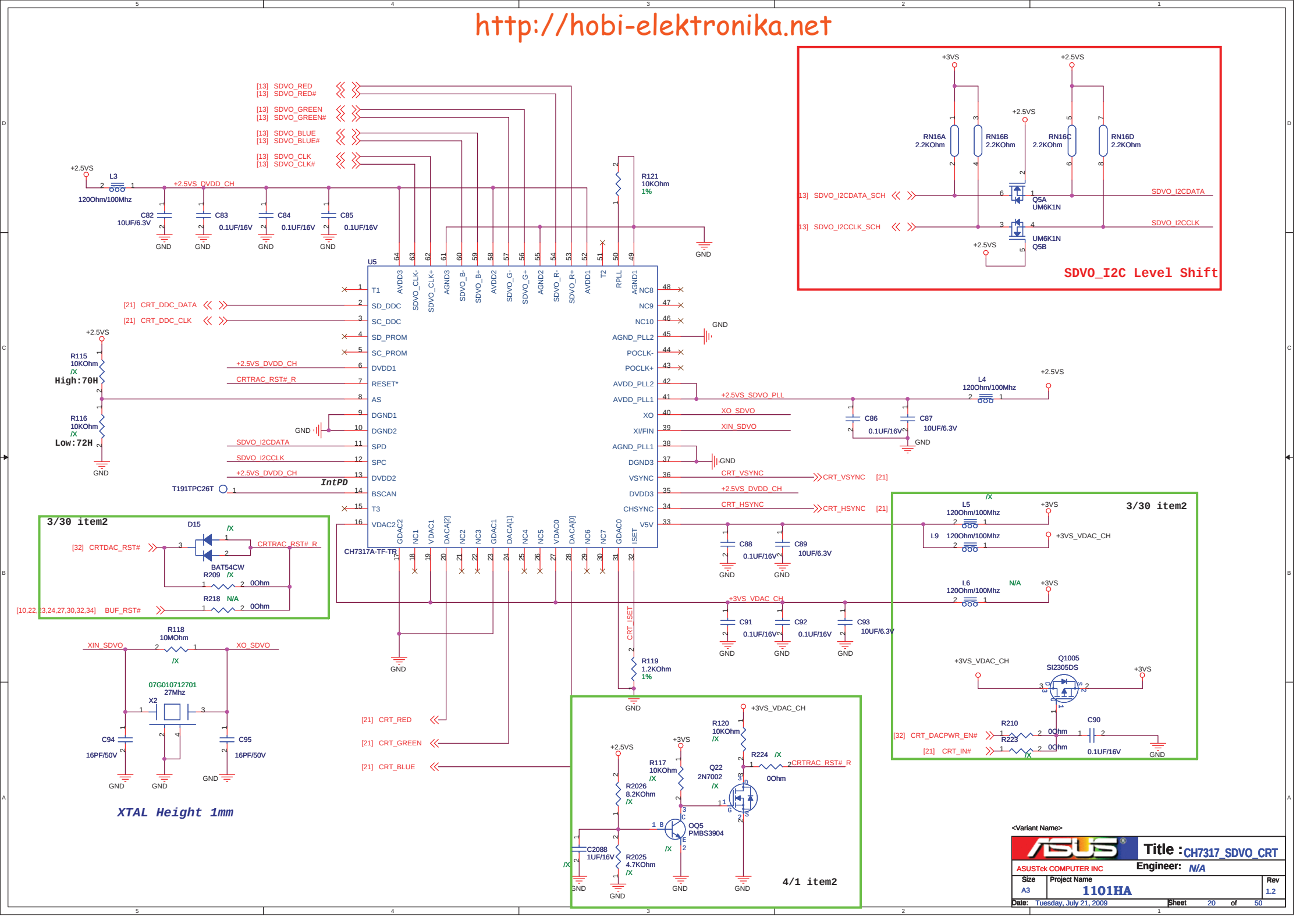
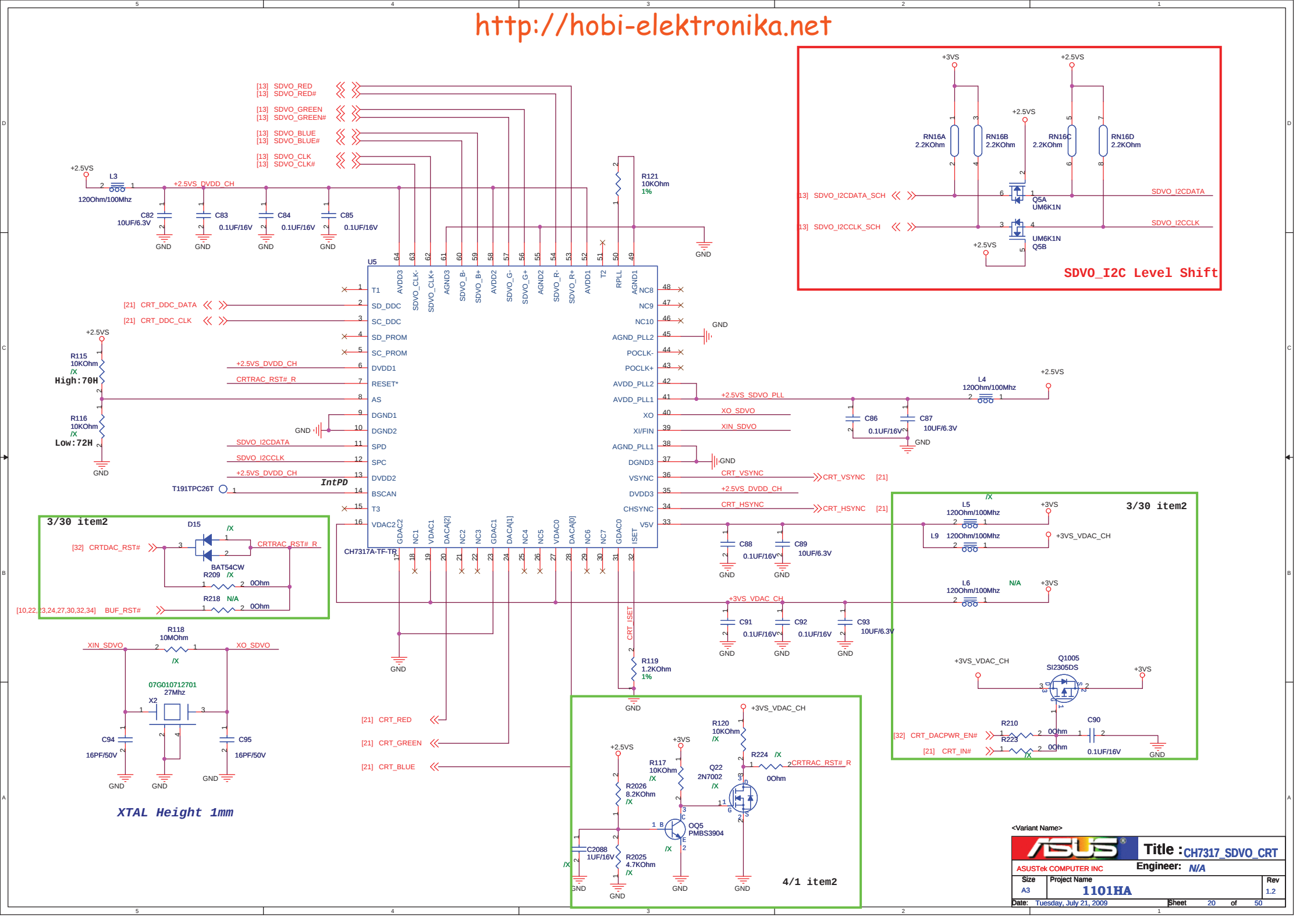
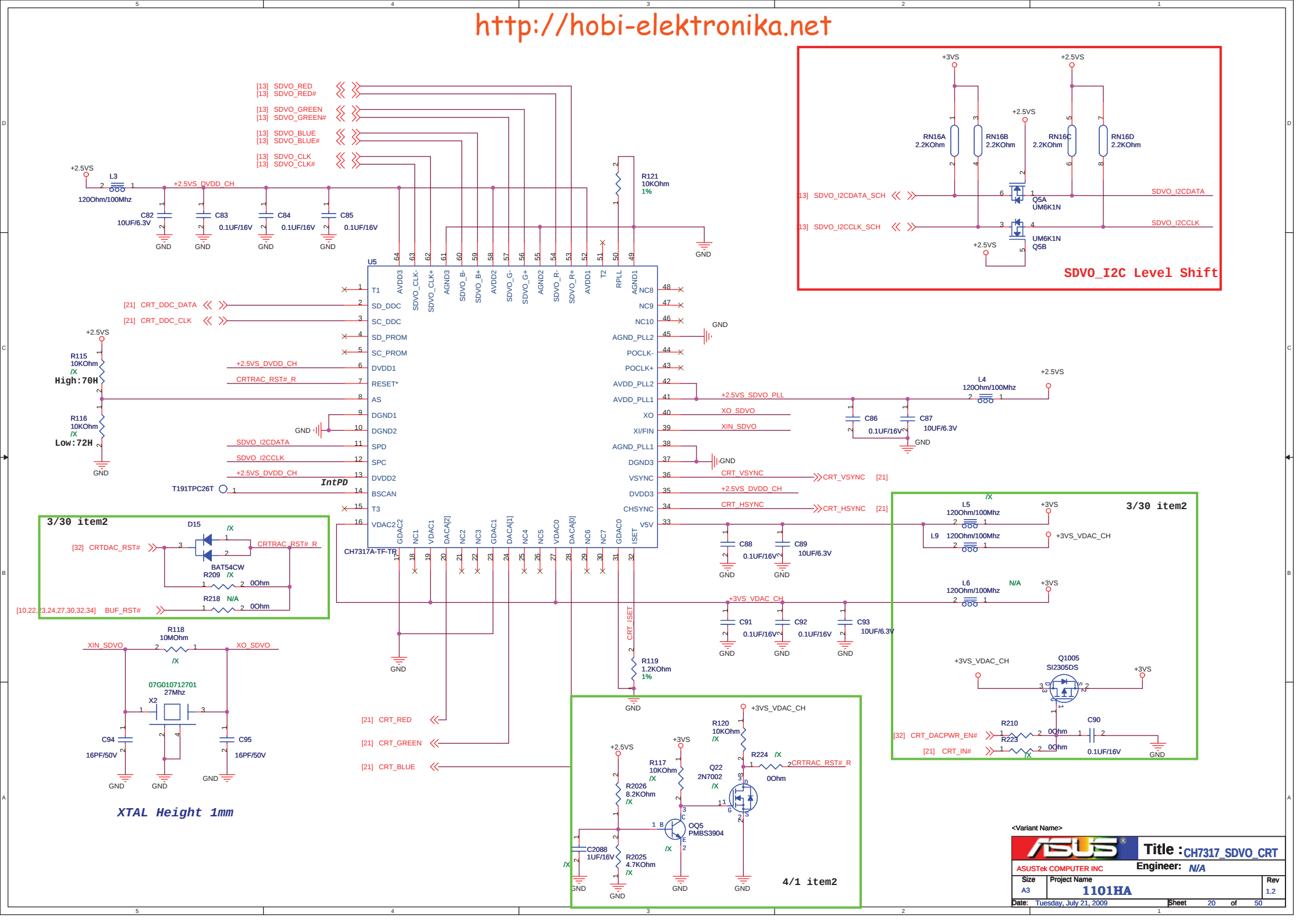
Project Name

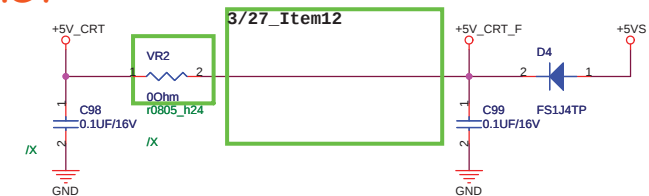
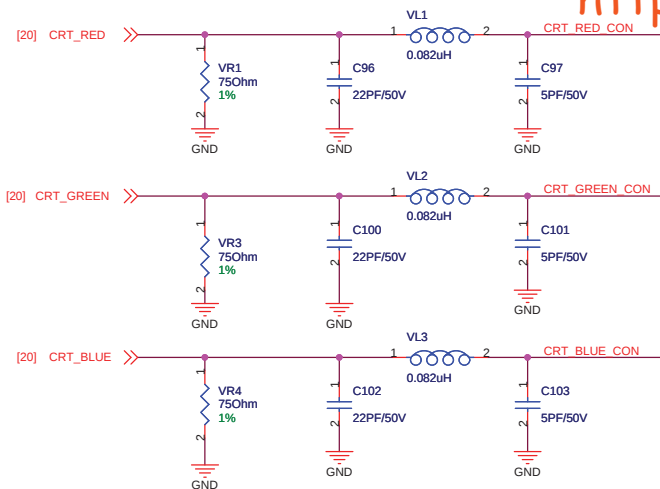
1101HA

Rev
1.2

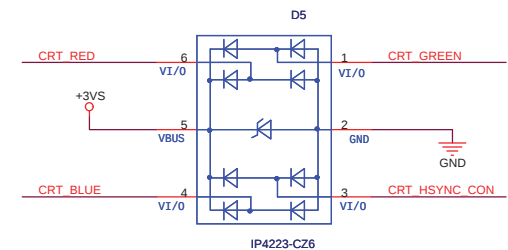
Date: Tuesday, July 21, 2009

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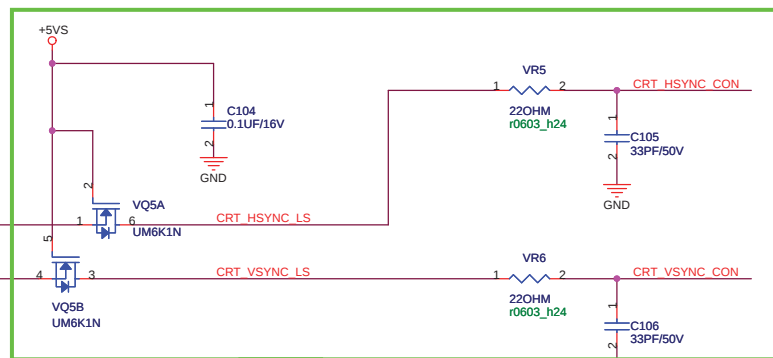


3/27_Item3



3/27_Item12

3/30 item5



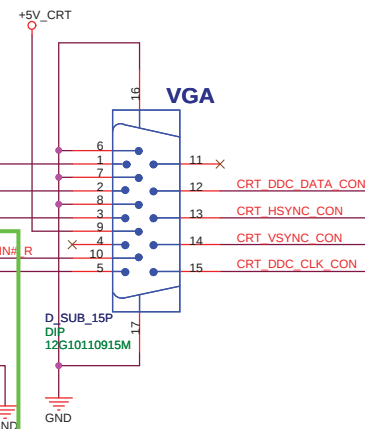
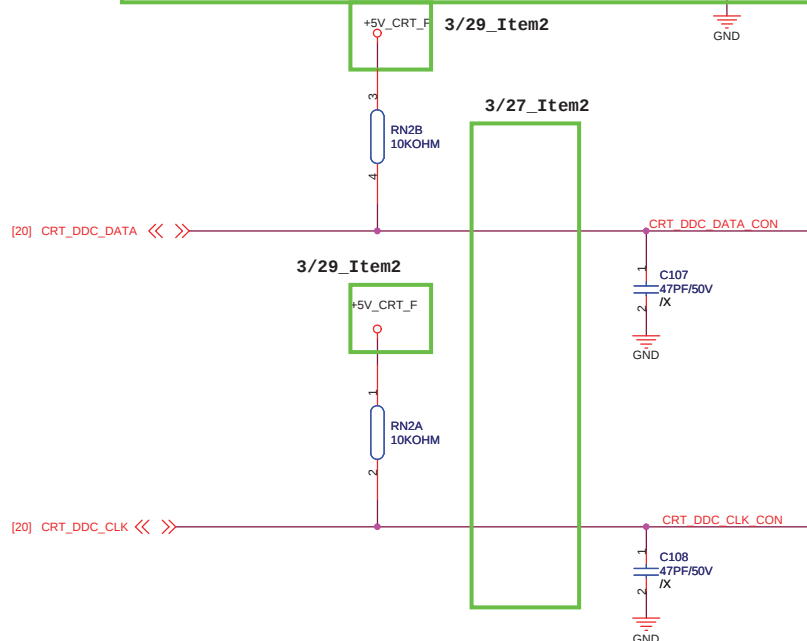
C105 C106 for EA measurement

U6上:VR5 & VR6-->22 OHM
U6 /X :VR5 & VR6 -->0 OHM

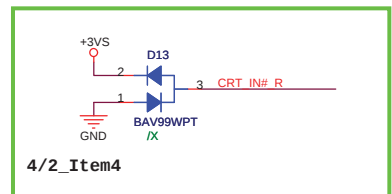
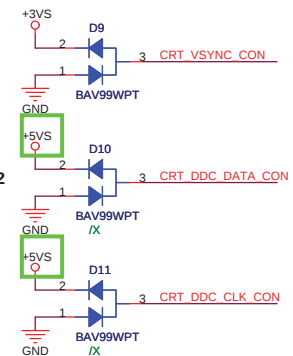
BUS BUFFER:
Unidirectional buffers (high impedance buffers) are required on both HSYNC and VSYNC to prevent potential electrical overstress and illegal operation of the GMCH, since some display monitors may attempt to drive HSYNC and VSYNC signals back to GMCH.

3/29_Item2

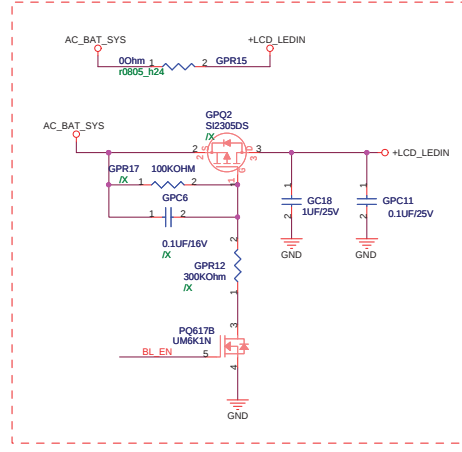
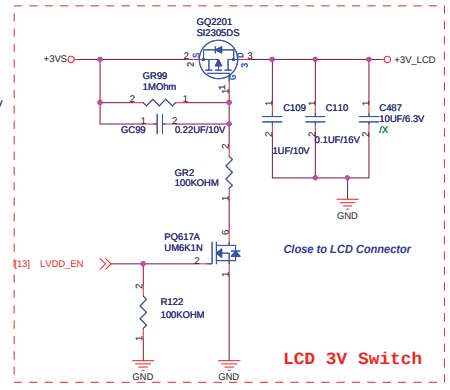
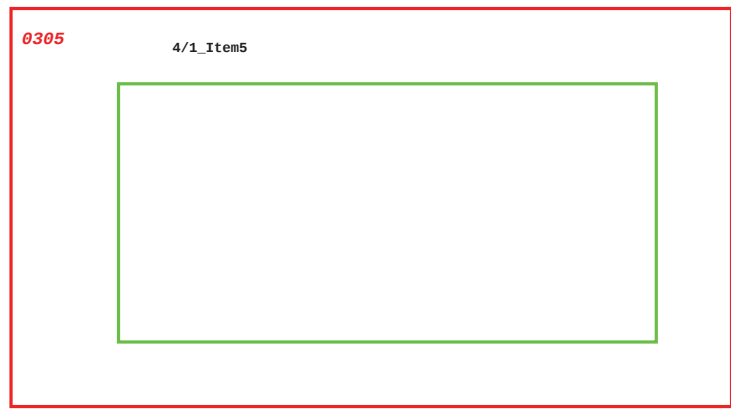
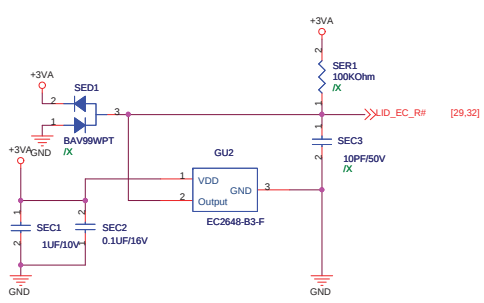
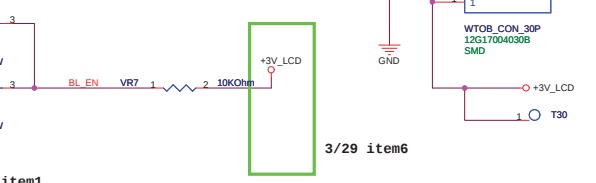
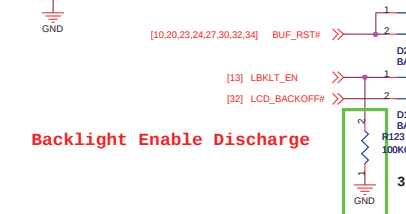
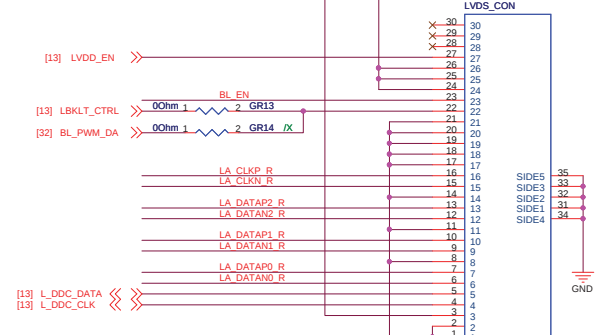
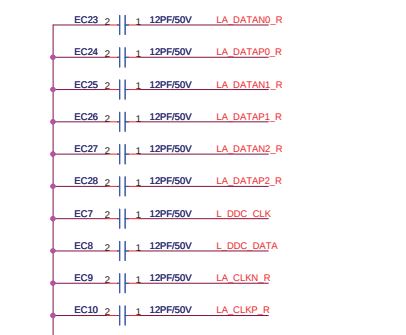
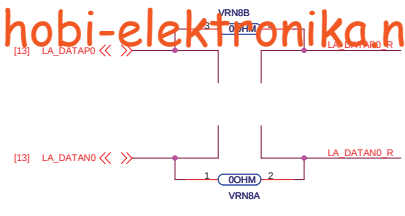
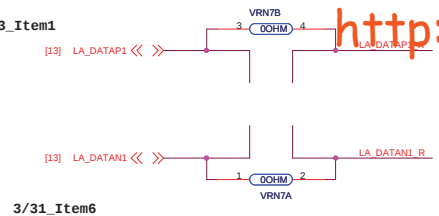
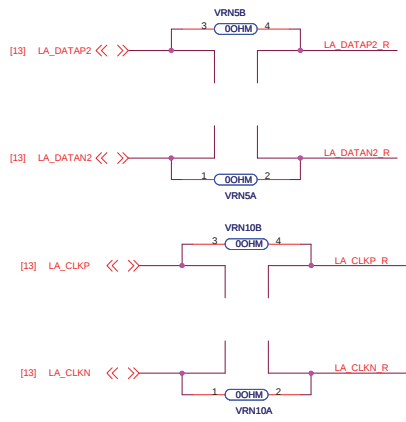
3/27_Item2

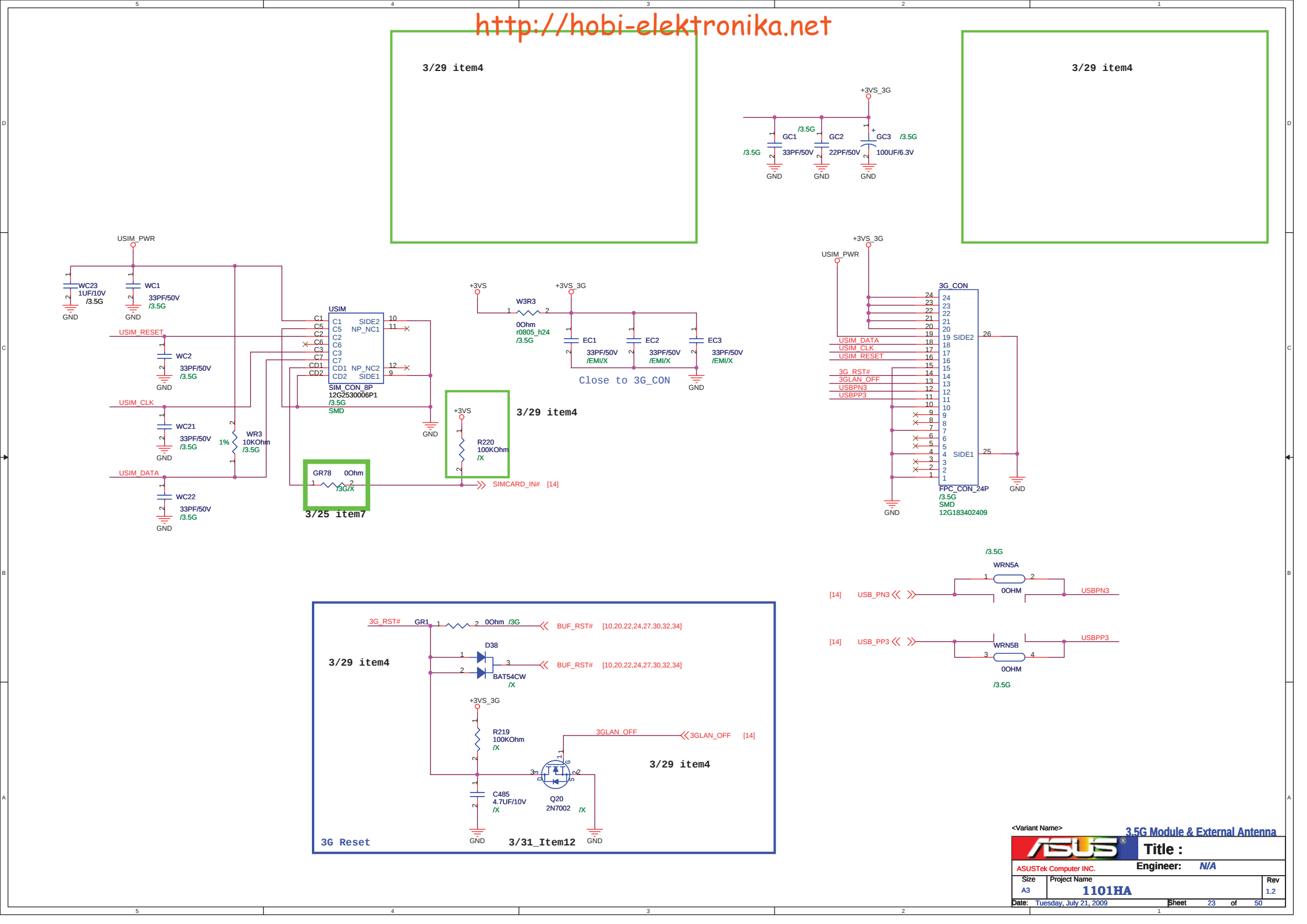
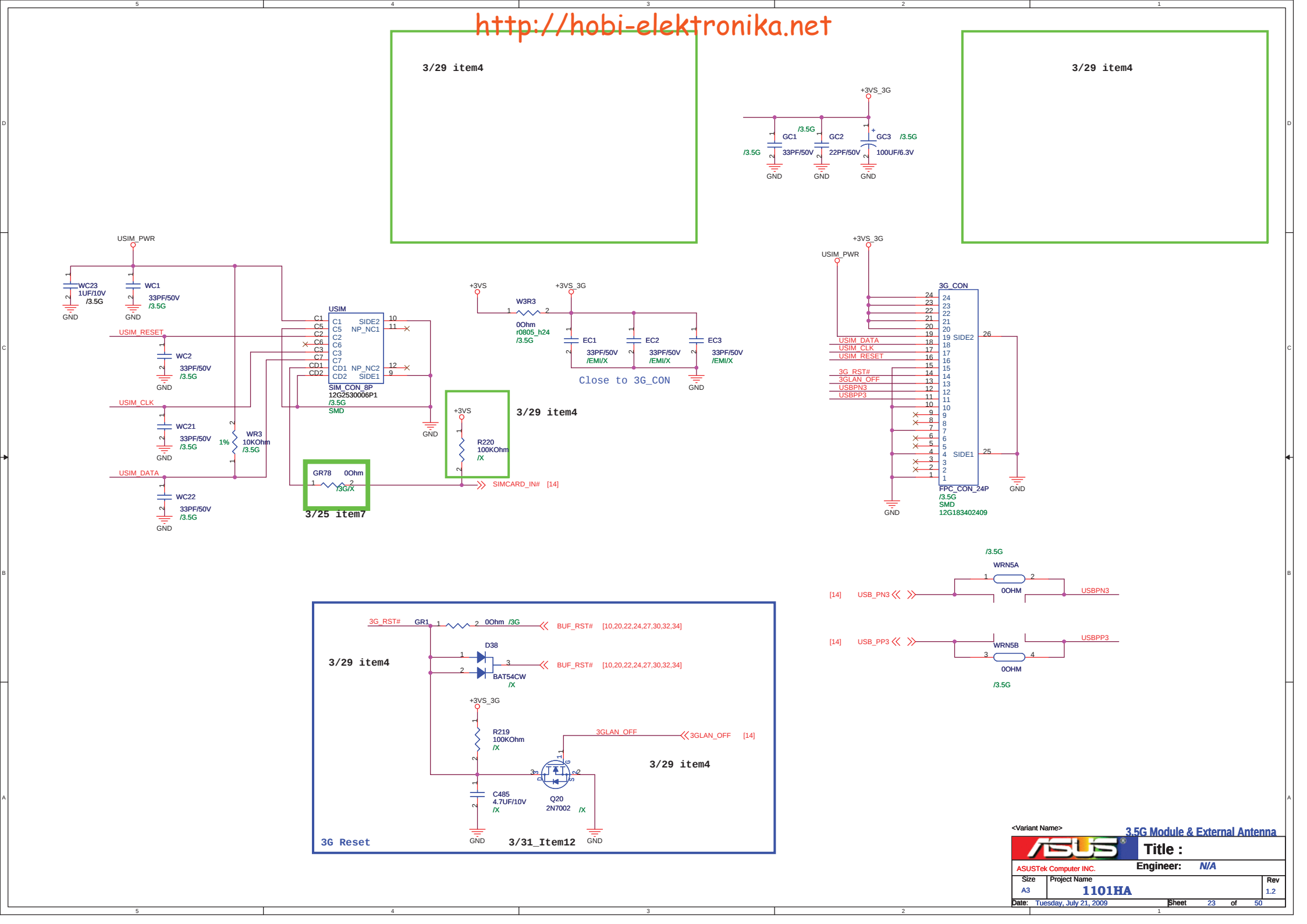
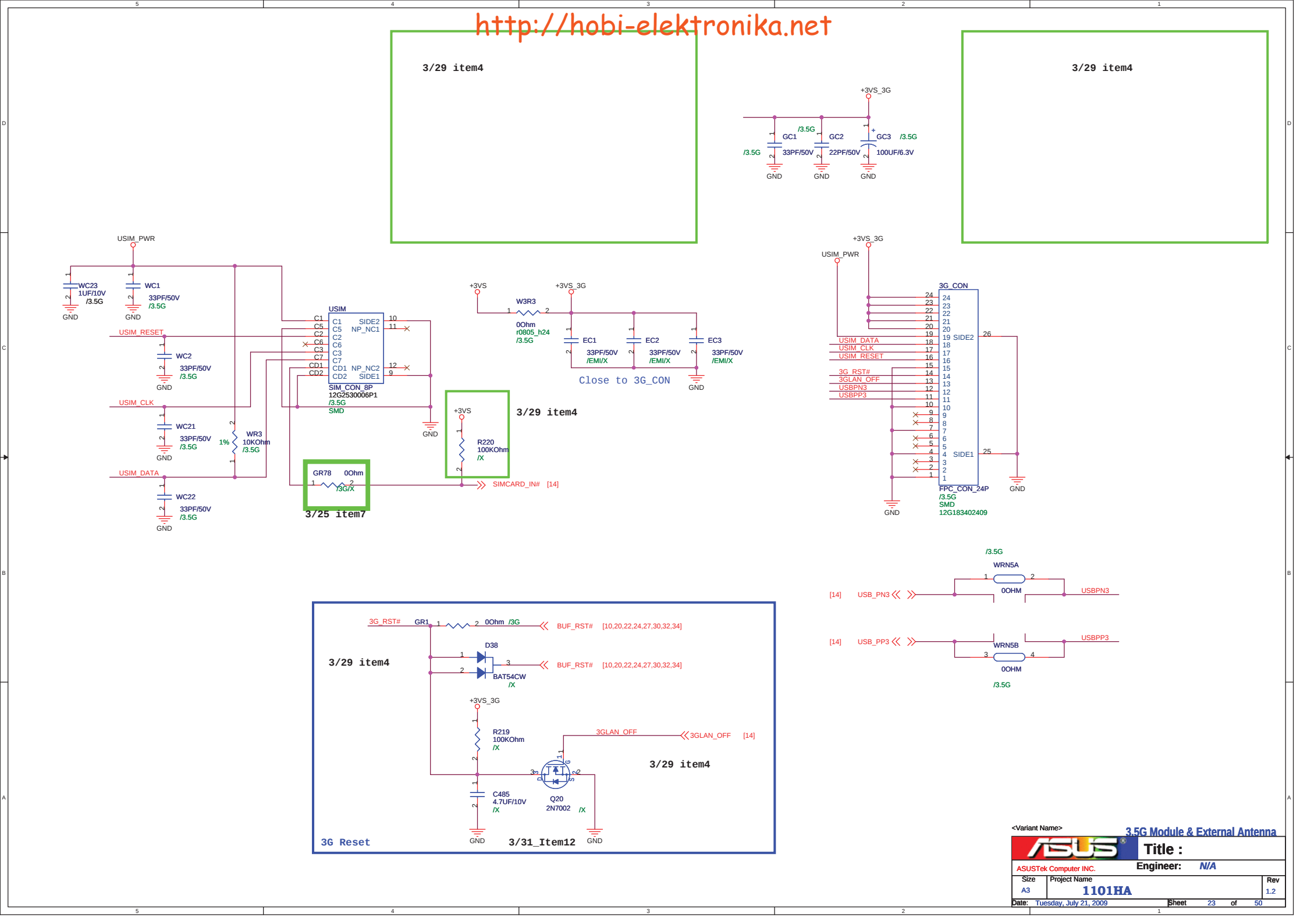
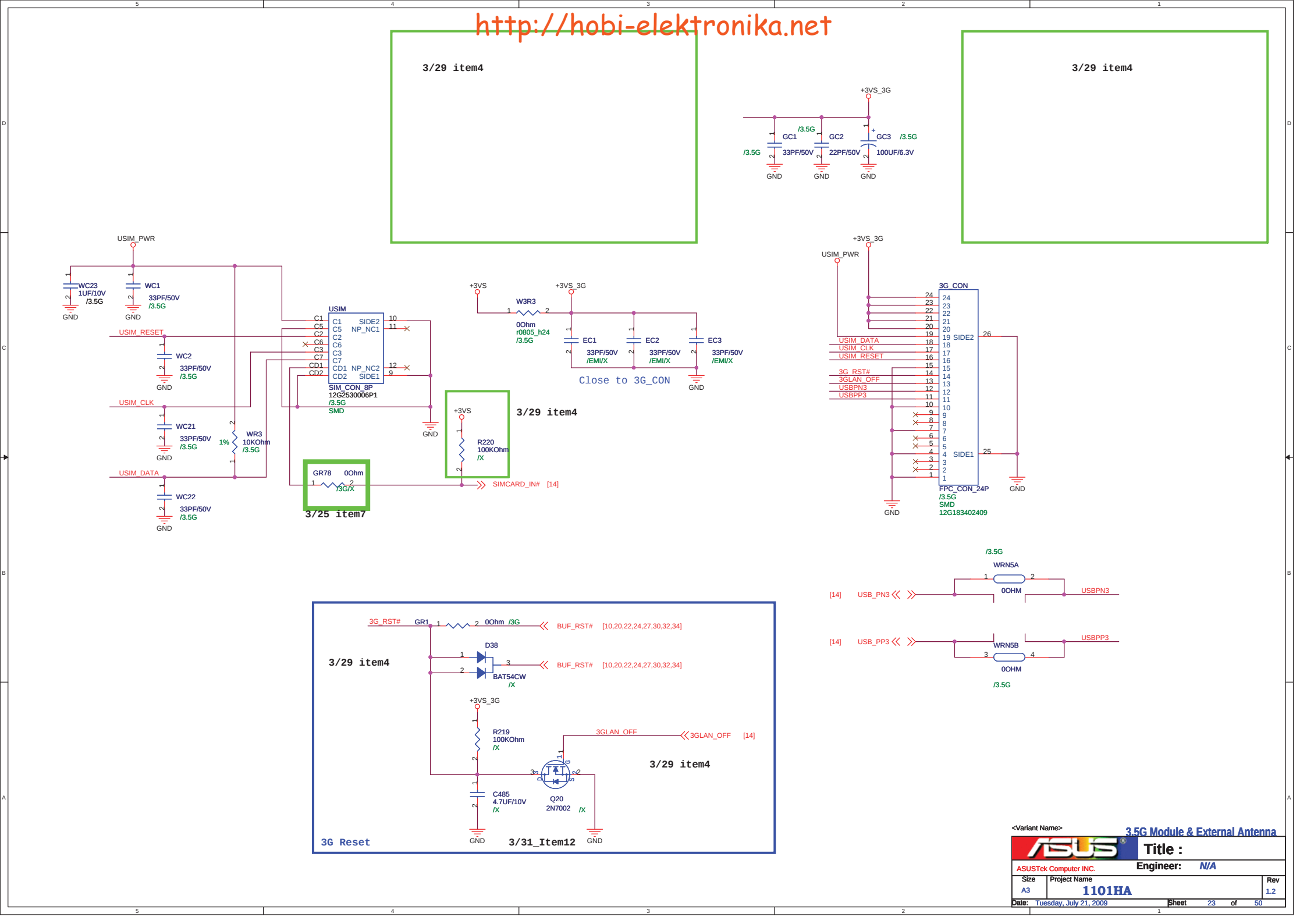
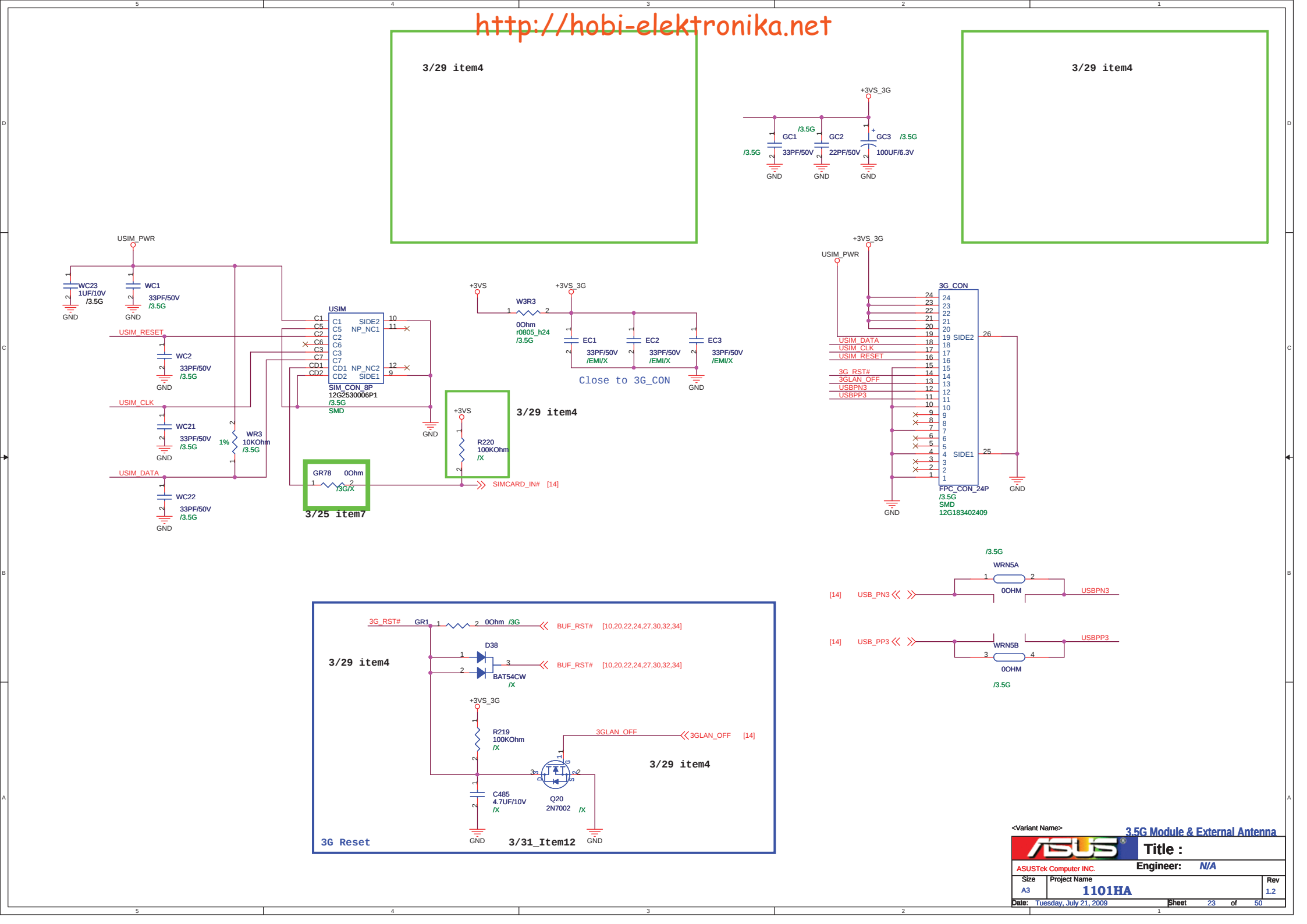


3/29_Item2



<Variant Name>



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http://hobi-elektronika.net

USIM Module Connections:

- USIM PWR:** Connected to +3VS through capacitor WC23 (1uF/10V).
- USIM RESET:** Connected to USIM pin C1 through capacitor WC1 (33PF/50V).
- USIM CLK:** Connected to USIM pin C2 through capacitor WC2 (33PF/50V).
- USIM DATA:** Connected to USIM pin C3 through capacitor WC22 (33PF/50V).

3G Reset Circuit:

- 3G_RST# is connected to GR1 (0Ohm) and then to the base of transistor Q20 (2N7002).
- The emitter of Q20 is connected to GND.
- The collector of Q20 is connected to 3GLAN_OFF through resistor R219 (100KOhm).
- 3GLAN_OFF is connected to the 3G module.

Other Components:

- 3G CON:** 12G183402409 connector.
- 3G_RST#:** Connected to GR1 (0Ohm) and then to the 3G module.
- 3GLAN_OFF:** Connected to the 3G module.
- 3GLAN_ON:** Connected to the 3G module.
- 3GLAN_P3:** Connected to the 3G module.
- 3GLAN_PP3:** Connected to the 3G module.

3G Module Connections:

- 3G_RST#:** Connected to pin 14.
- 3GLAN_OFF:** Connected to pin 13.
- 3GLAN_ON:** Connected to pin 12.
- 3GLAN_P3:** Connected to pin 11.
- 3GLAN_PP3:** Connected to pin 10.
- 3G_CON:** 12G183402409 connector.

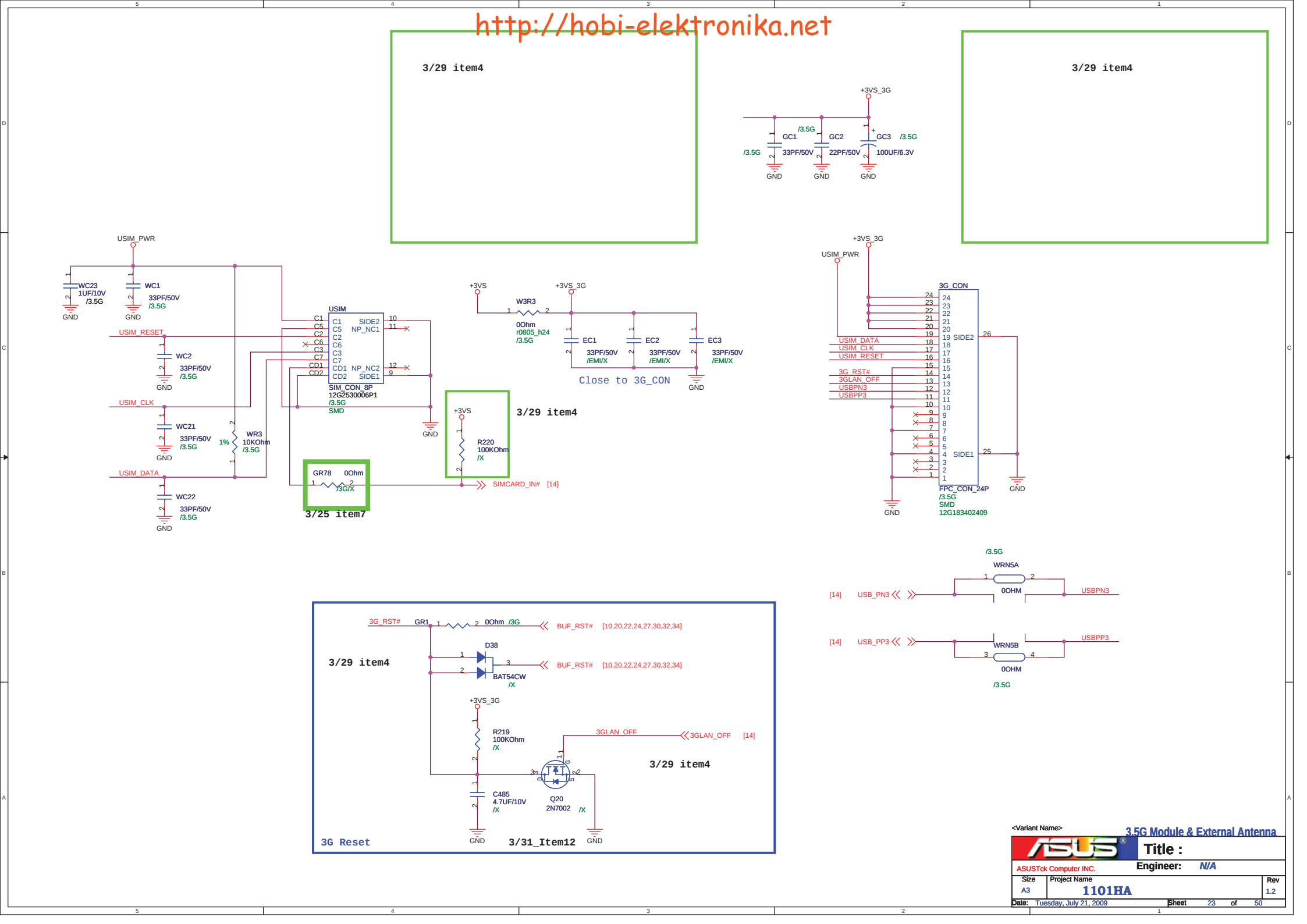
3G Reset Circuit:

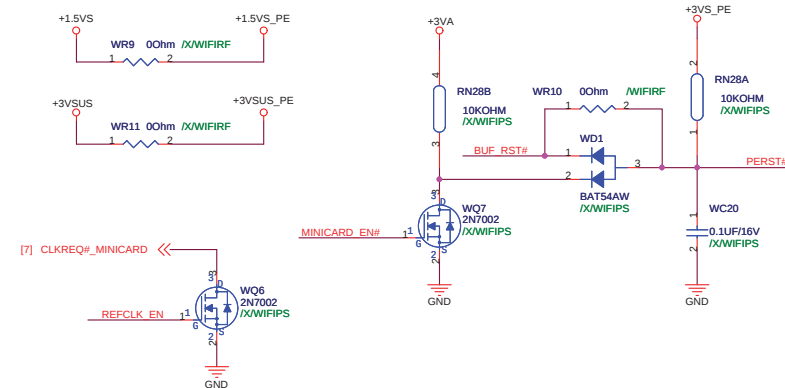
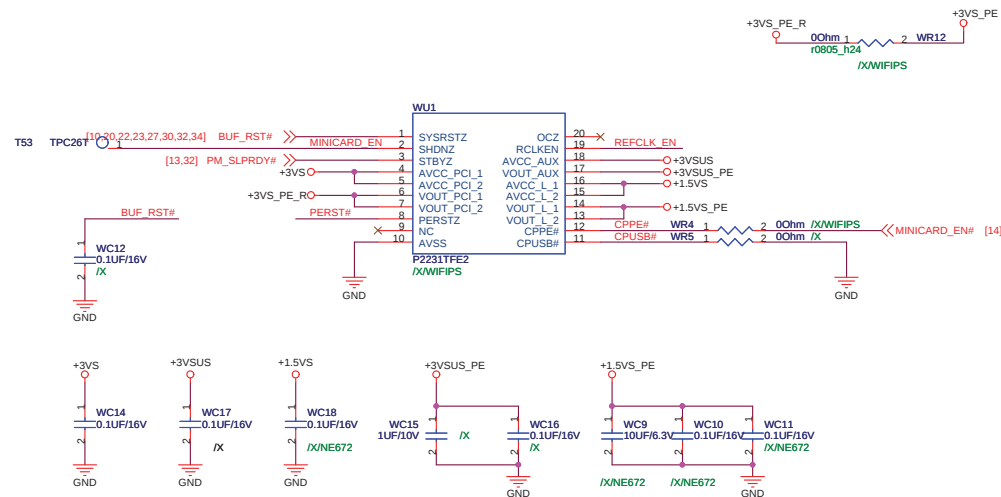
- 3G_RST# is connected to GR1 (0Ohm) and then to the base of transistor Q20 (2N7002).
- The emitter of Q20 is connected to GND.
- The collector of Q20 is connected to 3GLAN_OFF through resistor R219 (100KOhm).
- 3GLAN_OFF is connected to the 3G module.

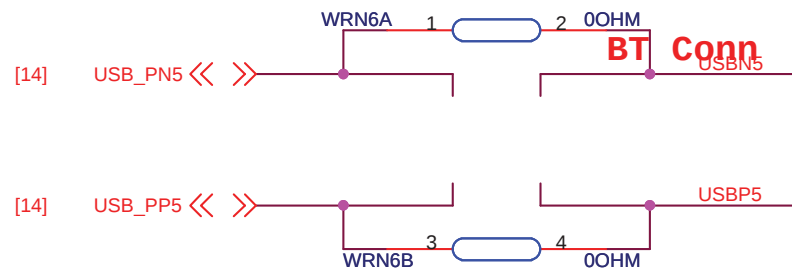
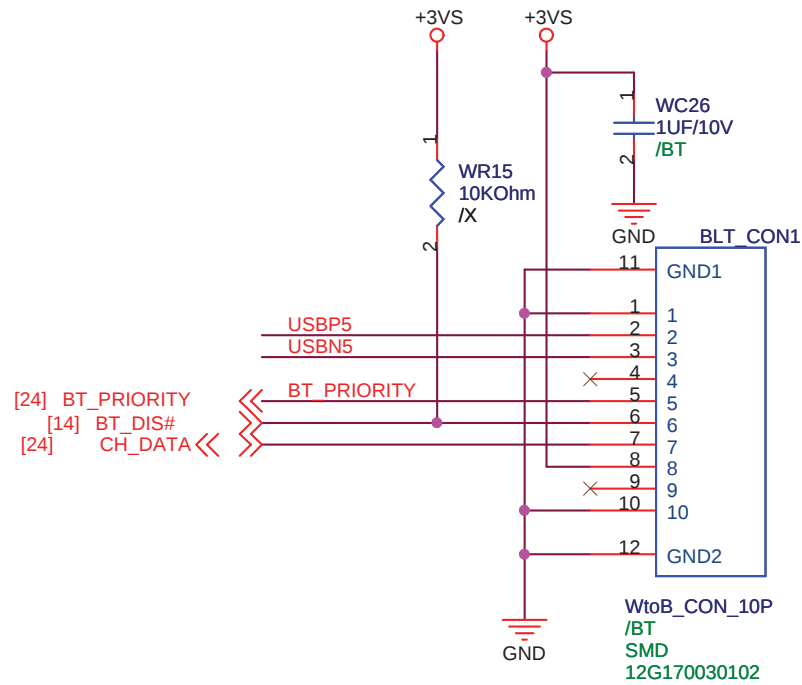
3G Module Connections:

- 3G_RST#:** Connected to pin 14.
- 3GLAN_OFF:** Connected to pin 13.
- 3GLAN_ON:** Connected to pin 12.
- 3GLAN_P3:** Connected to pin 11.
- 3GLAN_PP3:** Connected to pin 10.
- 3G_CON:** 12G183402409 connector.

ASUS		Title :	
ASUSTek Computer INC.		Engineer: N/A	
Size	Project Name	Rev	
A3	1101HA	1.2	
Date: Tuesday, July 21, 2009		Sheet 23 of 50	

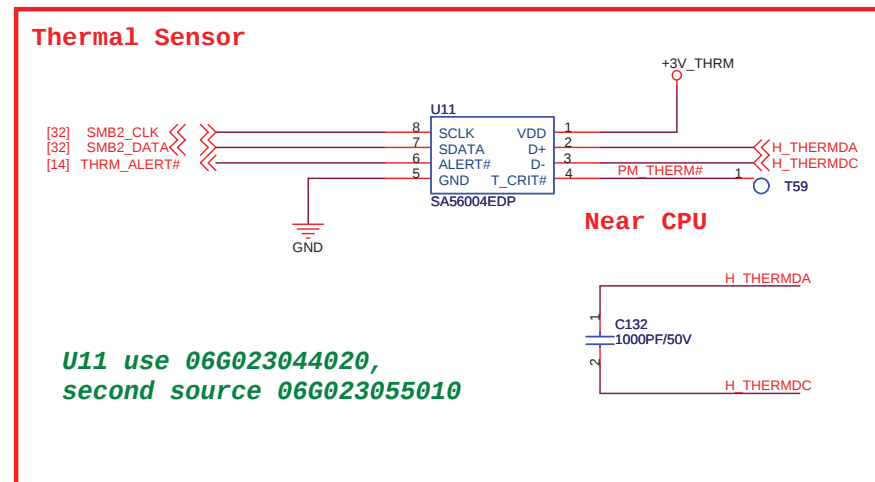
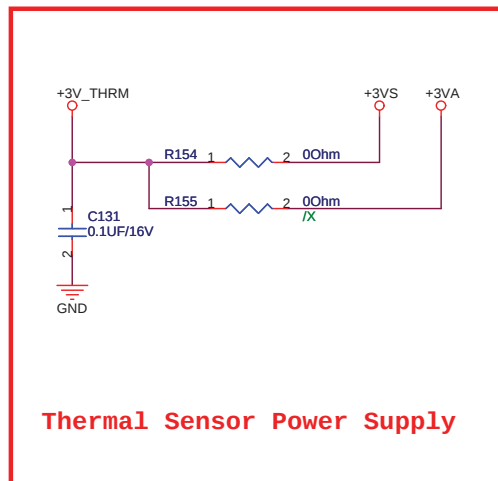
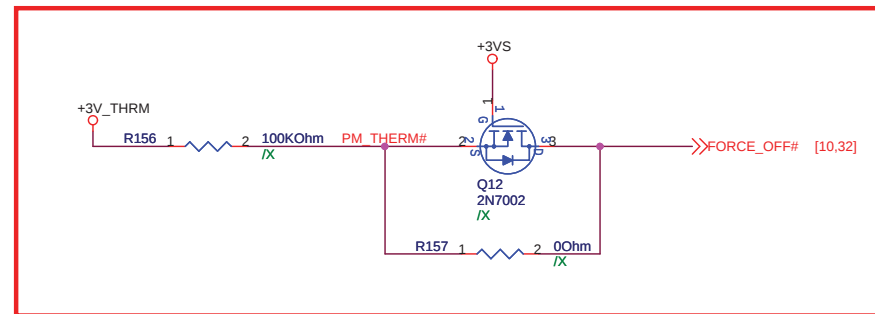
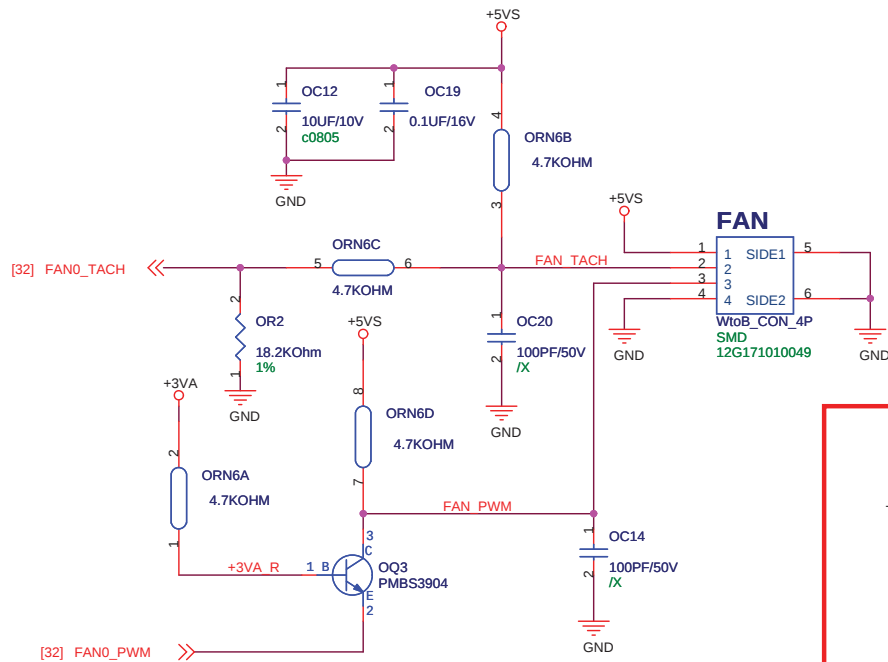
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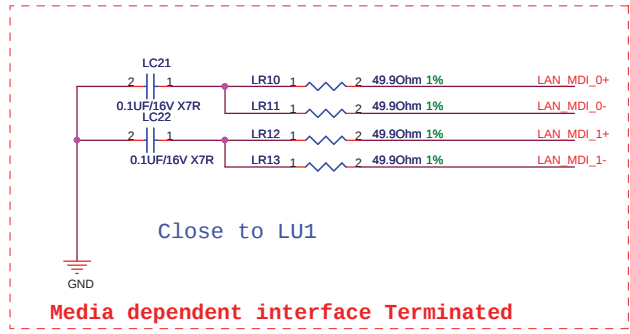
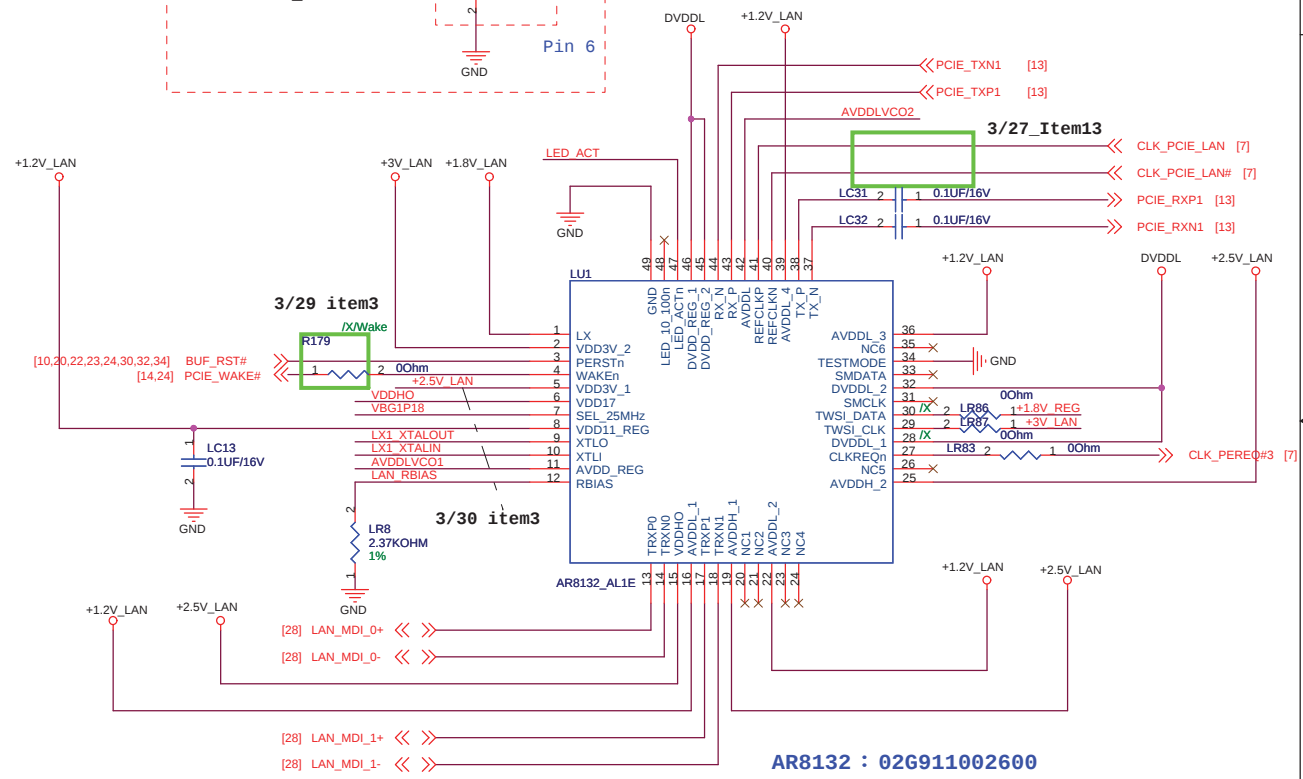
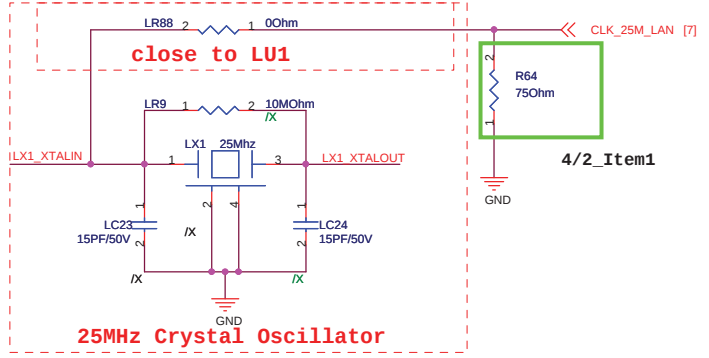
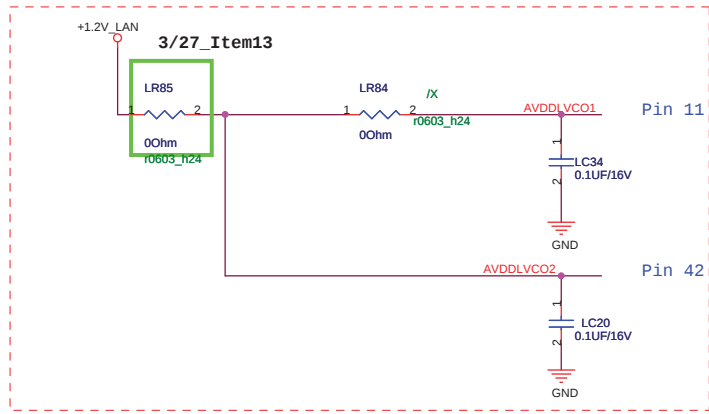
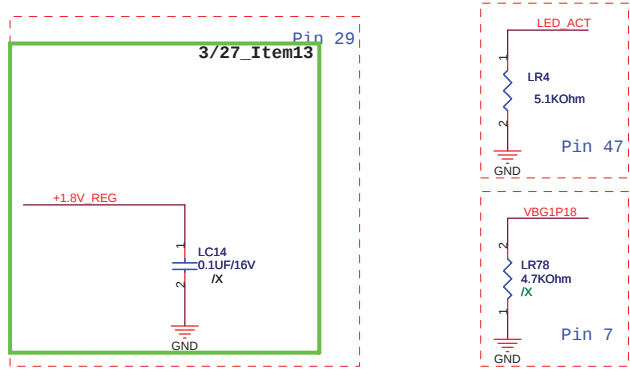
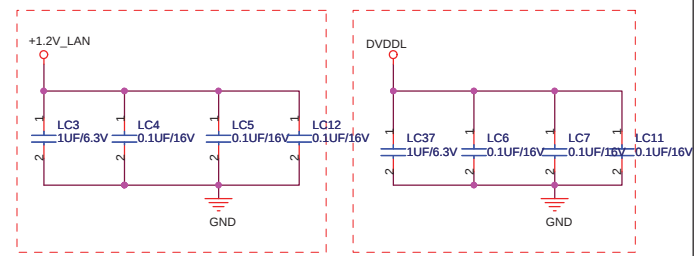
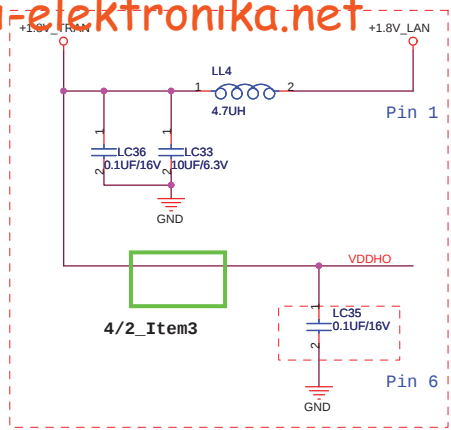
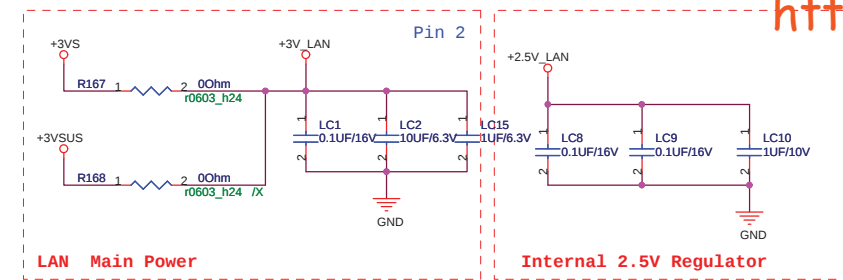
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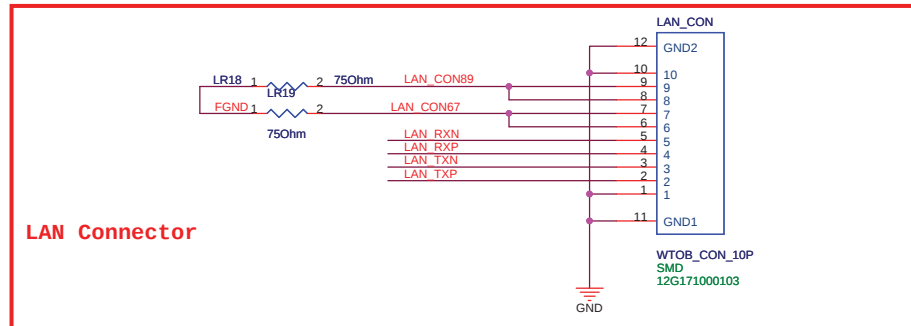
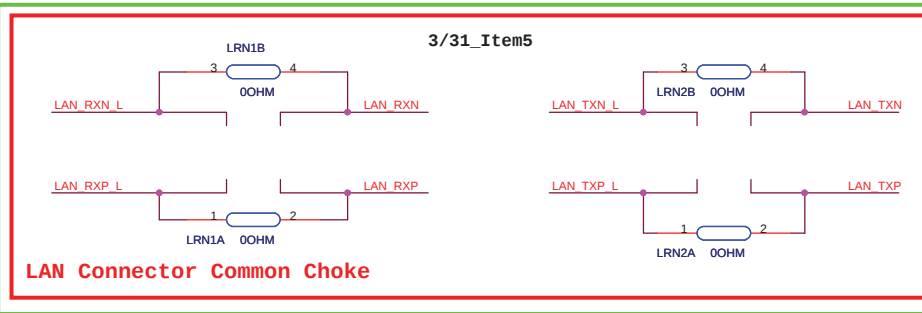
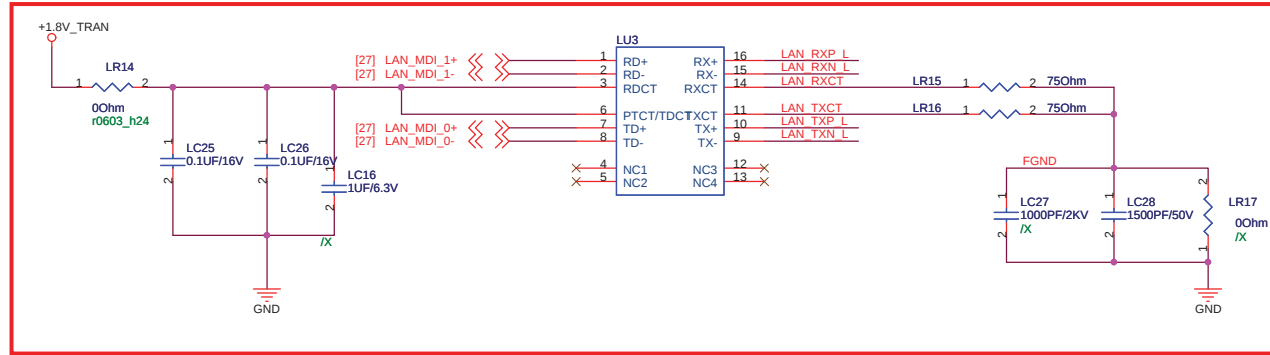
ASUS		Title : Bluetooth	
ASUSTek Computer INC.		Engineer: N/A	
Size A	Project Name 1101HA		Rev 1.2
Date: Tuesday, July 21, 2009		Sheet 25 of 50	



<Variant Name>

ASUS		Title : FAN_THERMAL SENSOR	
ASUSTek Computer INC.		Engineer: N/A	
Size Custom	Project Name 1101HA	Rev 1.2	
Date: Tuesday, July 21, 2009		Sheet 26 of 50	





<Variant Name>

3/31 item7

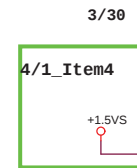
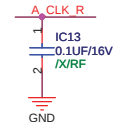
3/25 item4

Camera USB Common Choke

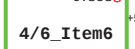


3/27 item8

3/26 item7 FOR RF



3/30 item6

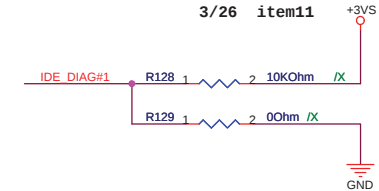


3/25 item3



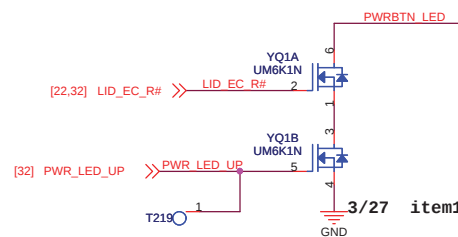
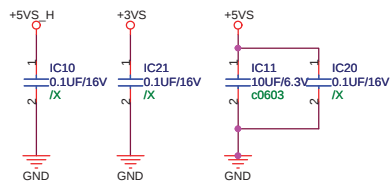
IDE_PCSEL#1 H: Slave
L: Master

IDE Master/ Slave Setting

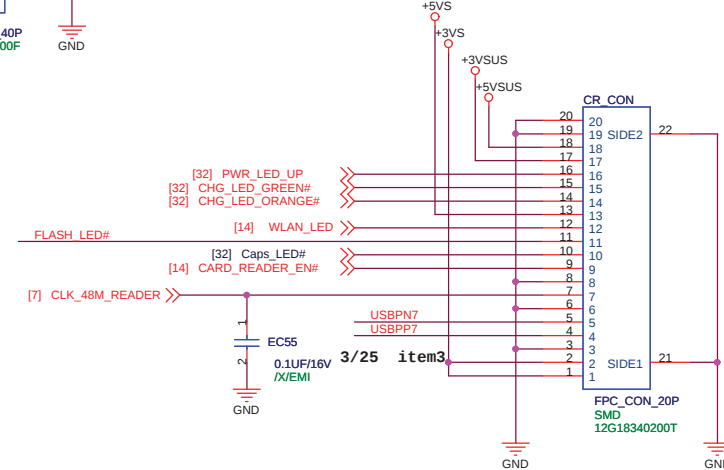


Diag Strapping

IDE_DIAG#1 [30]

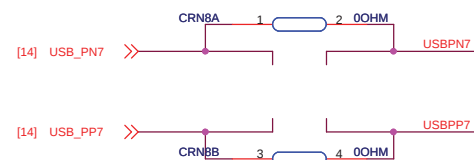


3/25 item2



Flash LED

[30] FLASH_LED_S# FLASH_LED#



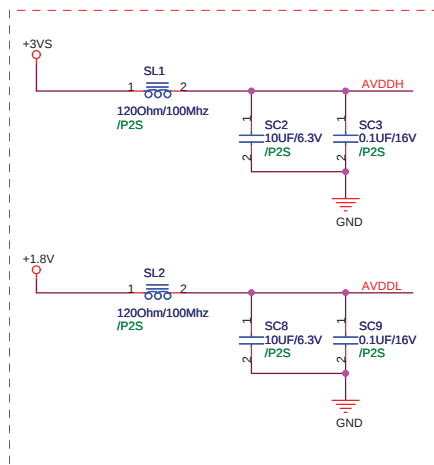
RD debug only

3/26 item11

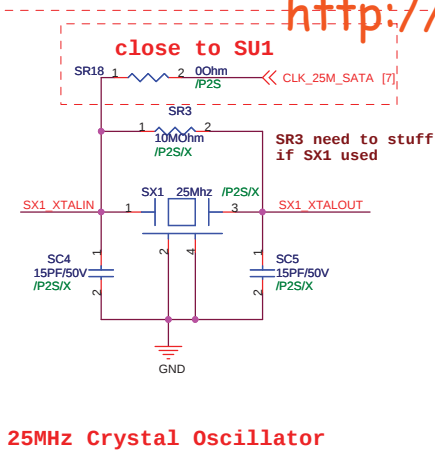
3/25 item3

<Variant Name>

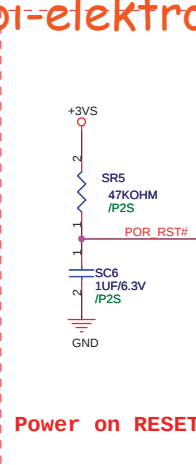
ASUS		Title : Flash Conn	
ASUSTek Computer INC.		Engineer: N/A	
Size A3	Project Name 1101HA	Rev 1.2	
Date: Tuesday, July 21, 2009		Sheet 29 of 50	



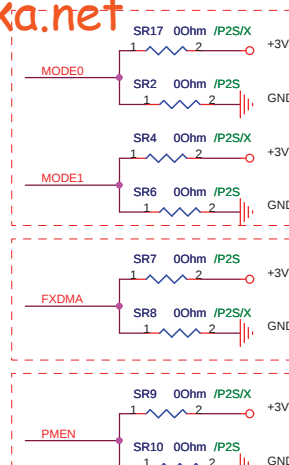
JMH330 only simulate PATA as Device 0



25MHz Crystal Oscillator



Power on RESET

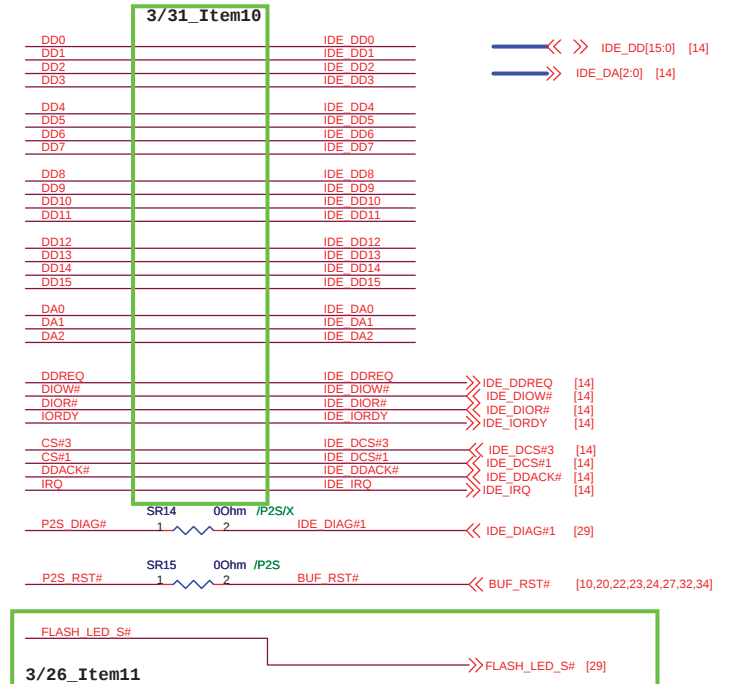
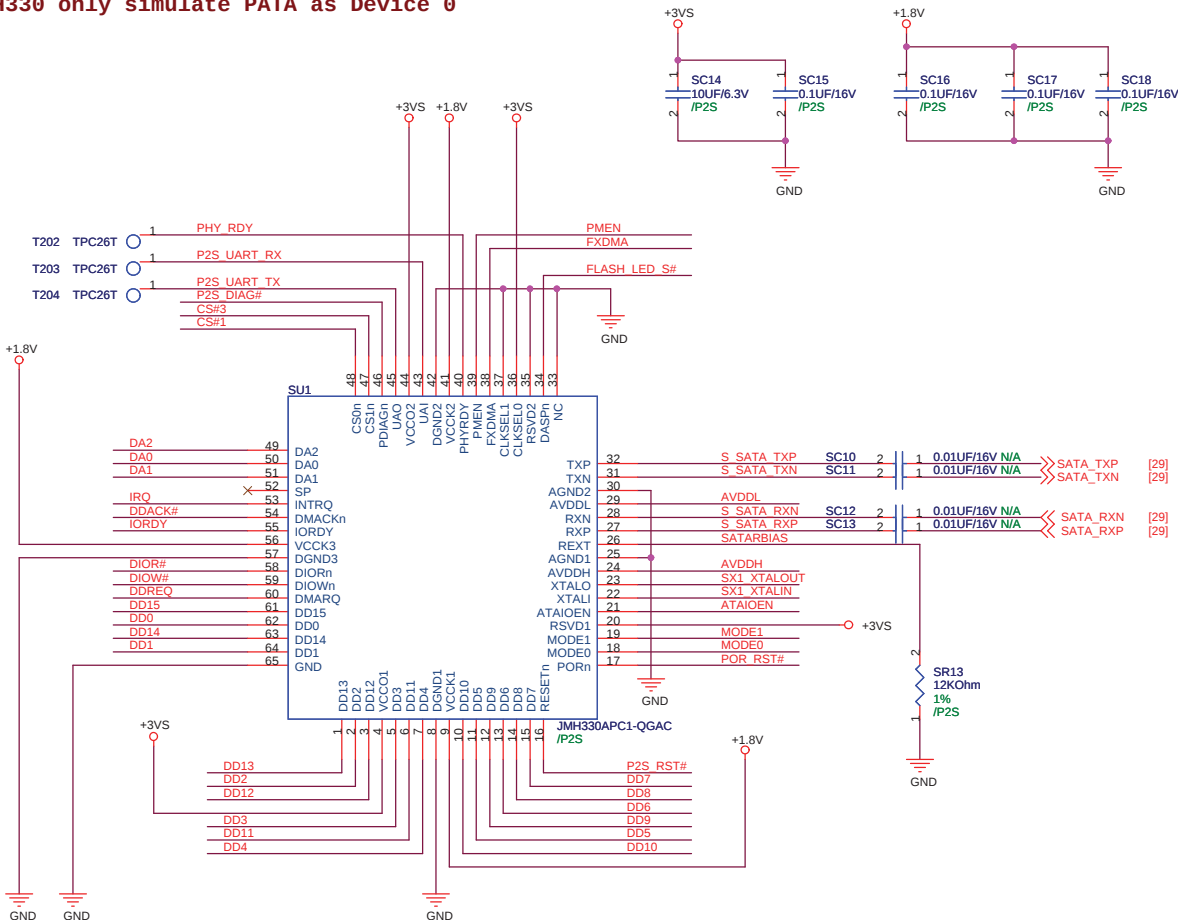
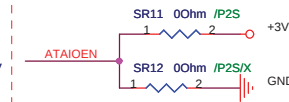


1.MODE[1:0]=Select UDMA speed when FXDMA is set
00:100MB/s ; 01:133MB/s
10:150MB/s ; 11:Reserved

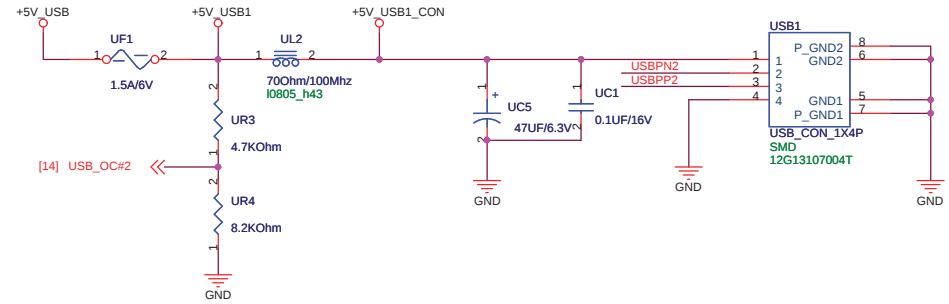
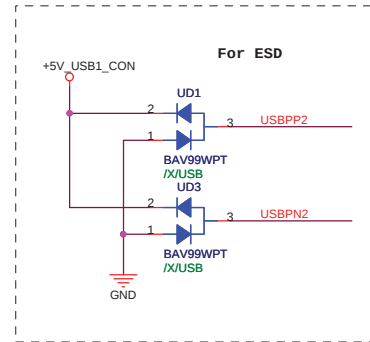
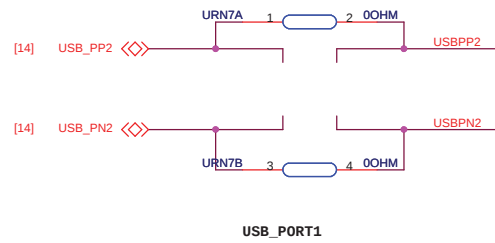
2.FXDMA=0,Auto adjustable speed rate according set Feature Command
FXDMA=1,speed rate depend on Mode[1:0] setting

3.PMEN=0 power management function Disable
PMEN=1 power management function Enable

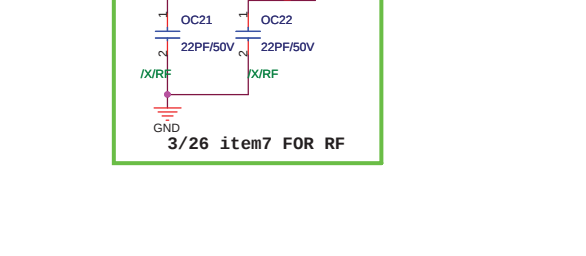
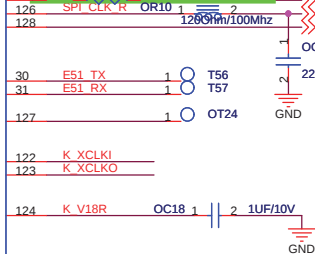
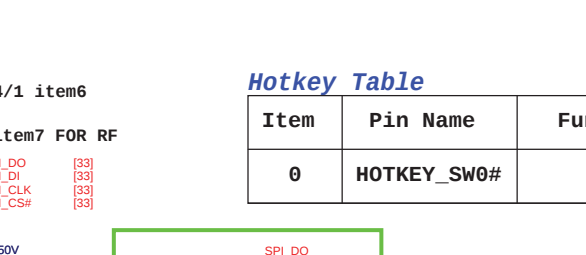
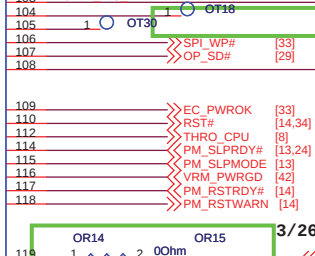
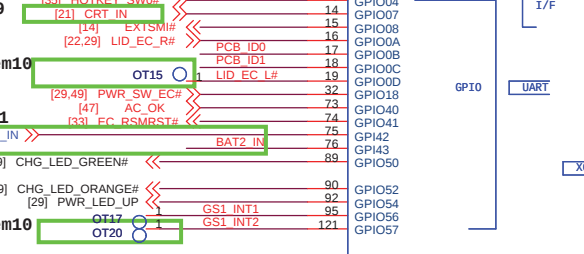
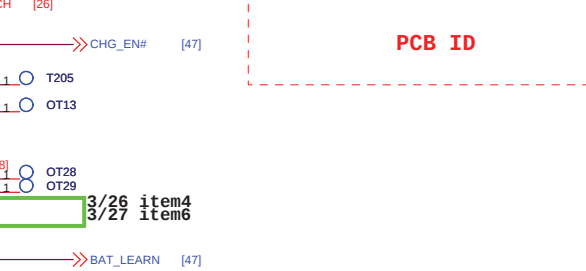
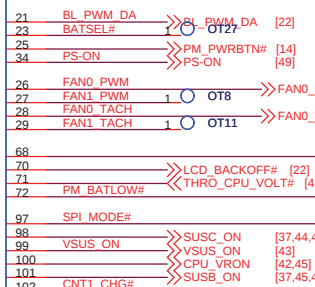
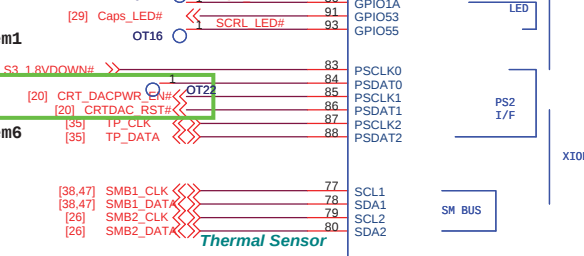
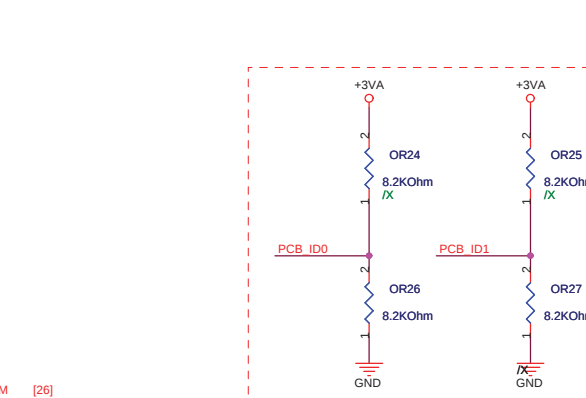
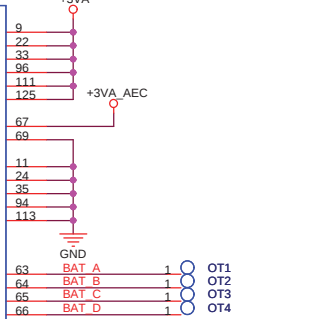
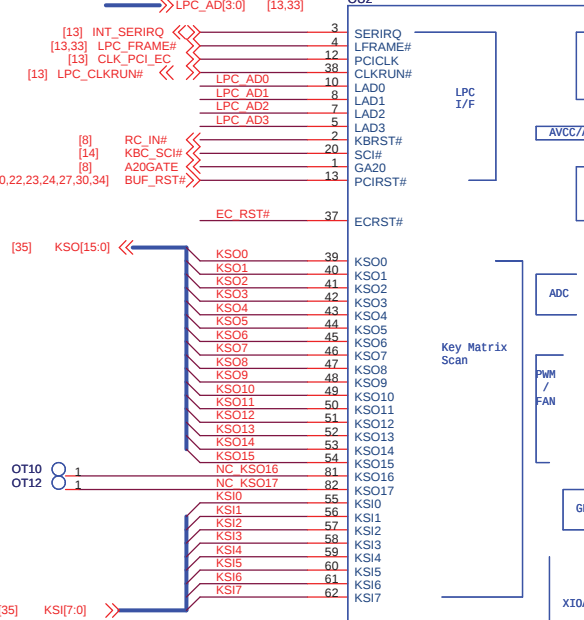
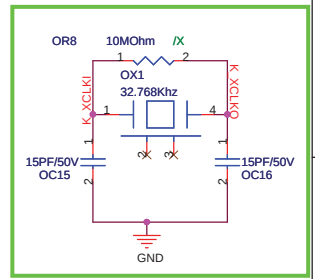
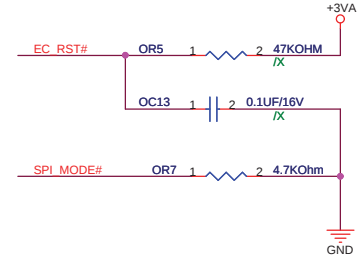
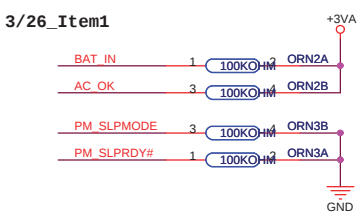
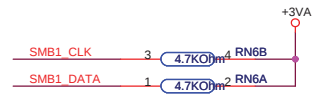
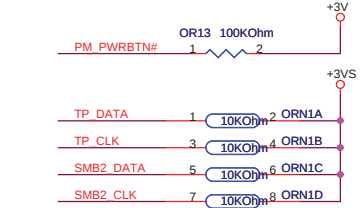
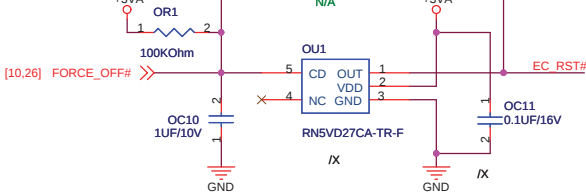
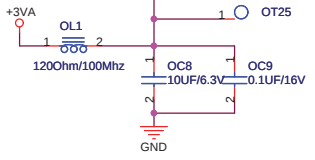
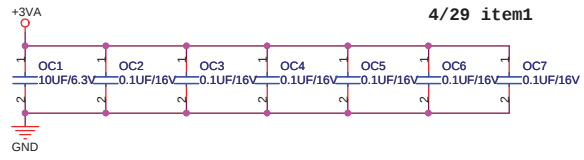
4.ATAIOEN=0,Disable the ATA output pins, ATA I/O output pins are Hi-Z.
ATAIOEN=1,Enable ATA output



<Variant Name>

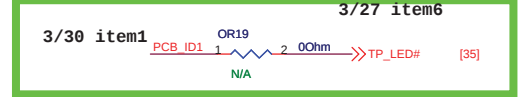
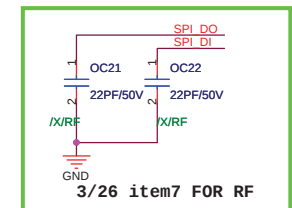


<Variant Name>



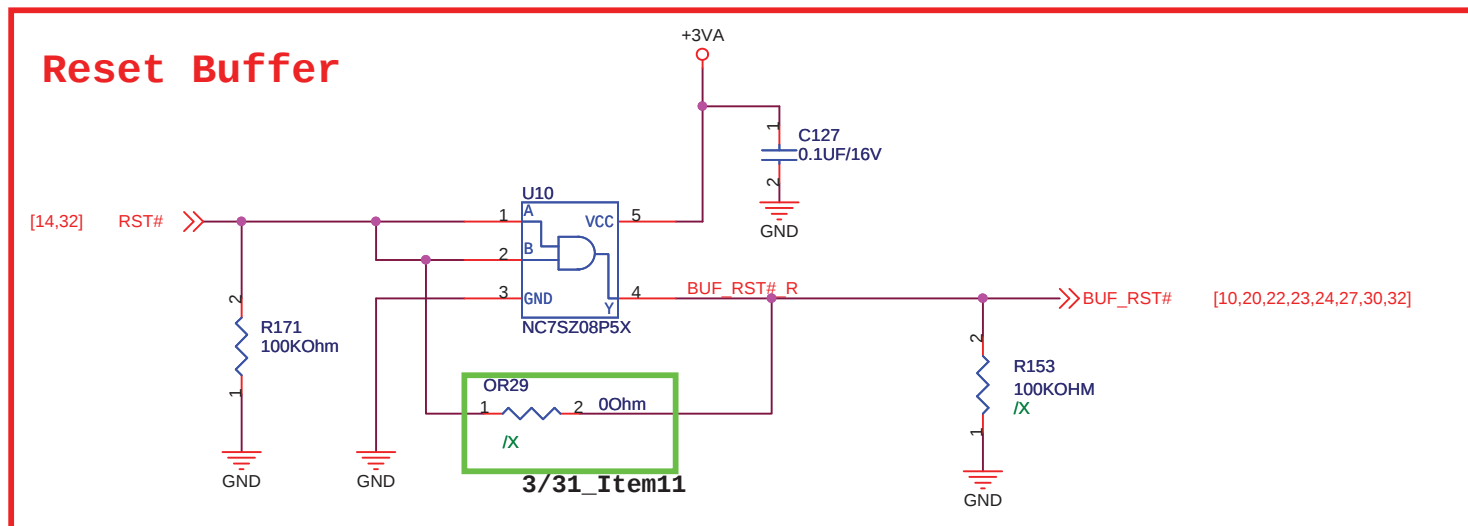
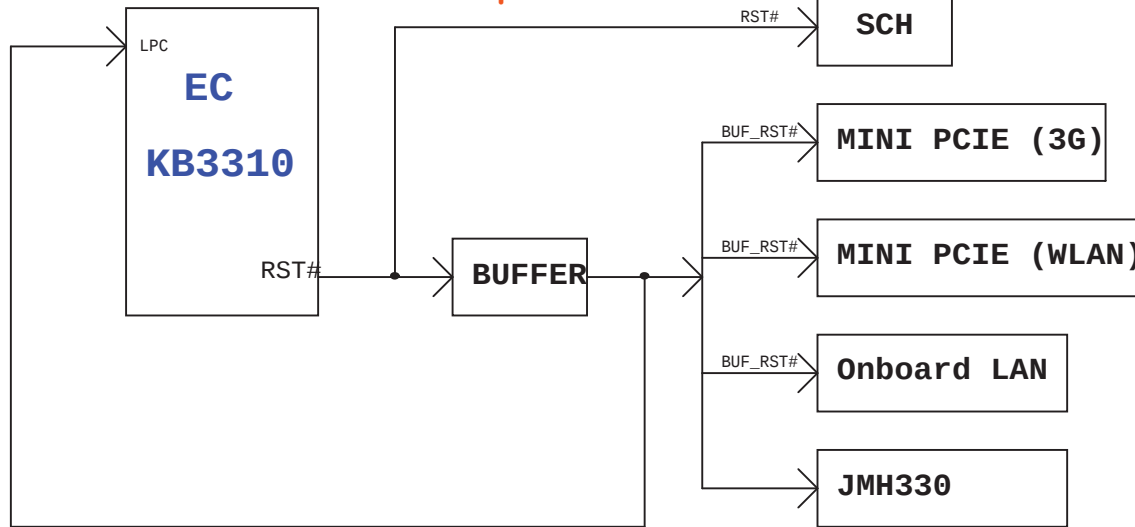
Hotkey Table

Item	Pin Name	Function
0	HOTKEY_SW0#	Home



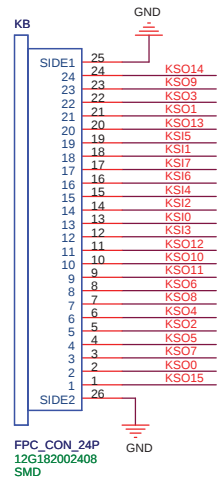
A



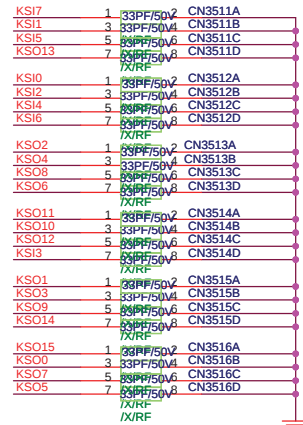


<Variant Name>

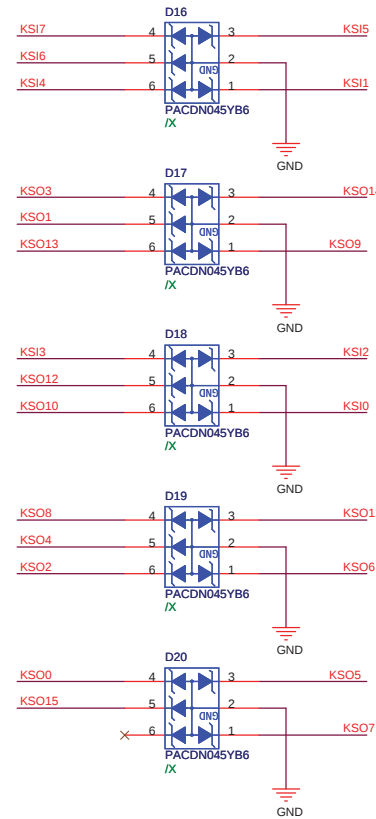
ASUS		Title : Reset Map	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size A4	Project Name 1101HA		Rev 1.2
Date: Tuesday, July 21, 2009		Sheet	34 of 50



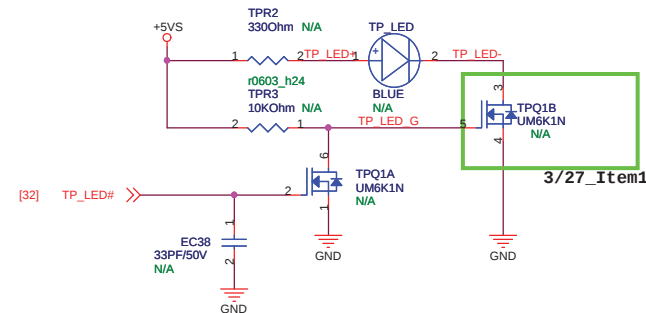
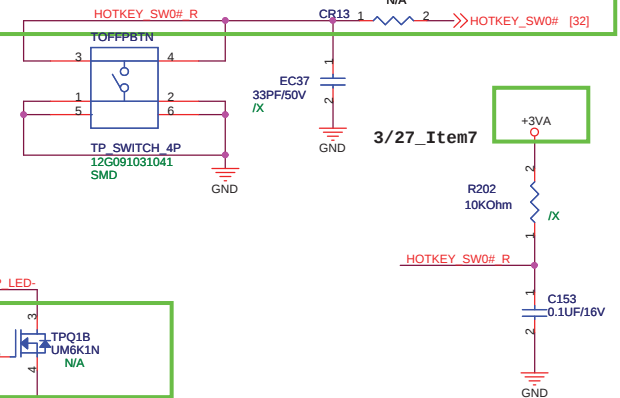
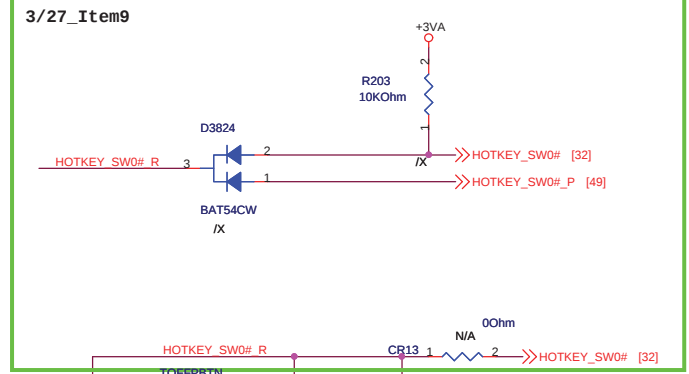
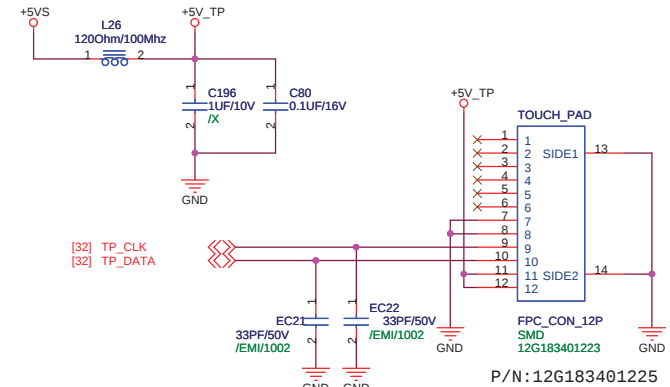
For Keyboard Connector



3/26_Item7 FOR RF



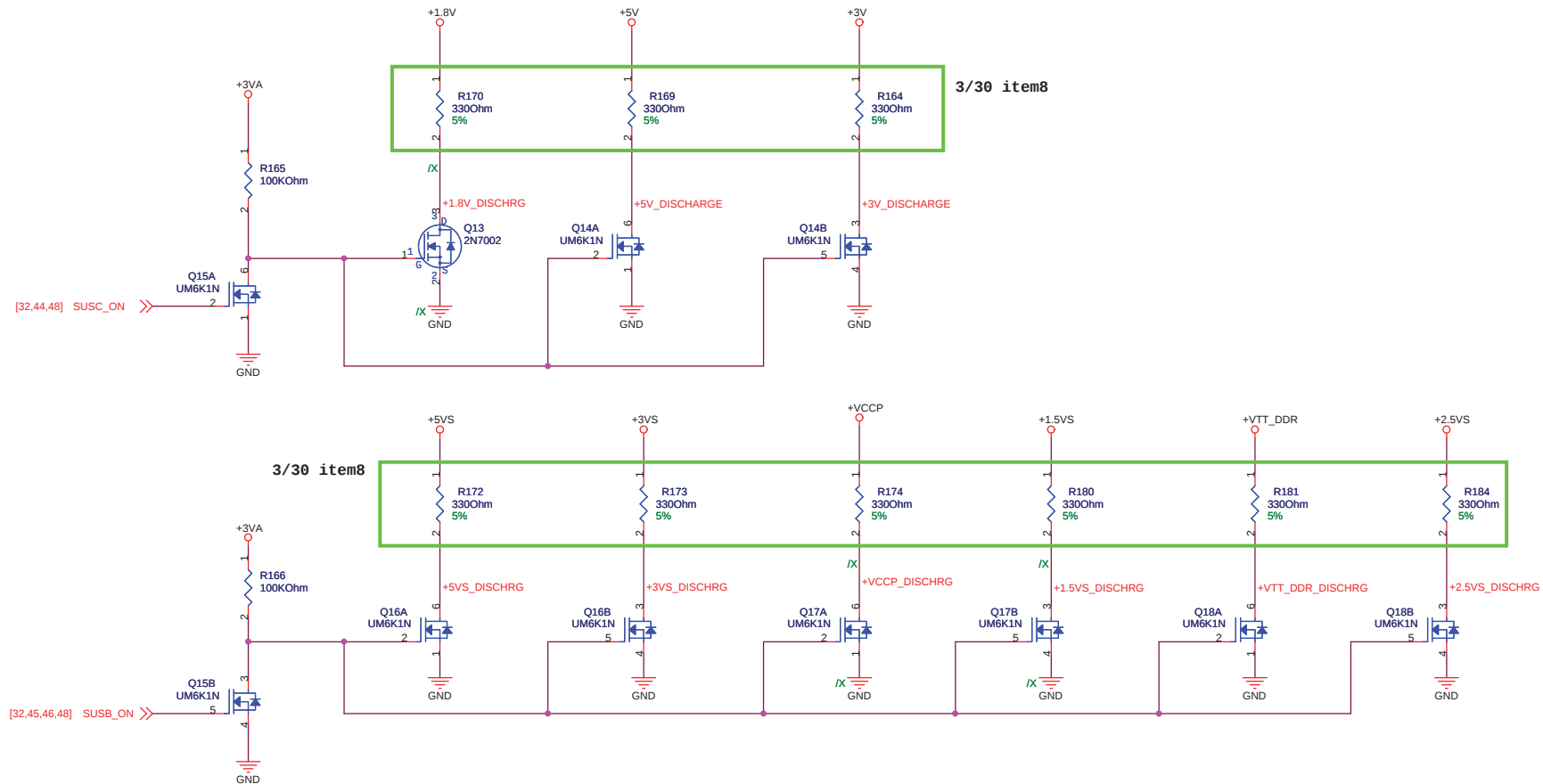
Keyboard ESD Protect



<Variant Name>

<Variant Name>

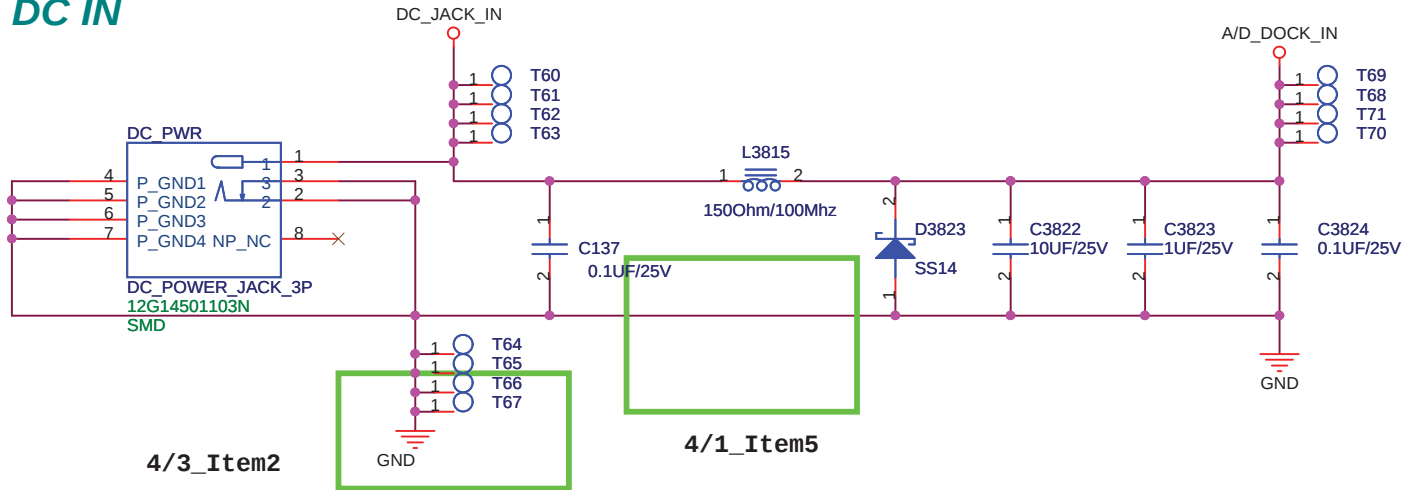
		Title : G-Sensor	
ASUSTek Computer INC.		Engineer: N/A	
Size A4	Project Name 1101HA	Rev 1.2	
Date: Tuesday, July 21, 2009		Sheet 36	of 50



<Variant Name>

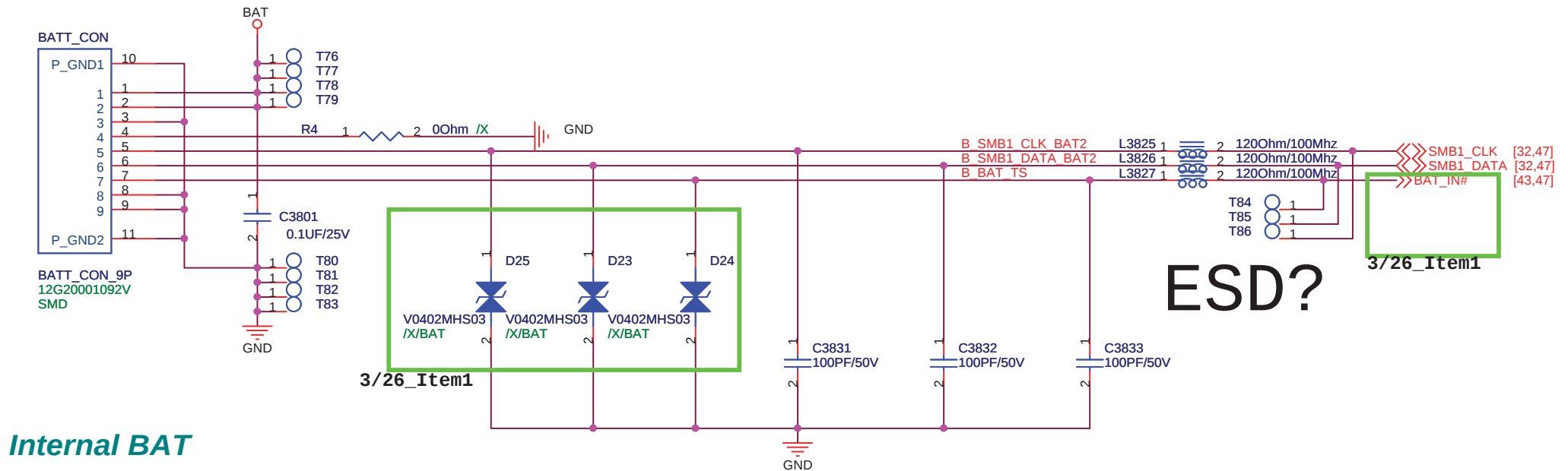
ASUS		Title : Discharge	
ASUSTek Computer INC.		Engineer: N/A	
Size A3	Project Name 1101HA	Rev 1.2	
Date: Tuesday, July 21, 2009		Sheet 37 of 50	

DC IN



4/3_Item2

4/1_Item5



3/26_Item1

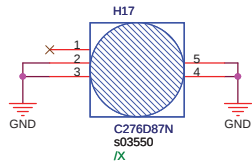
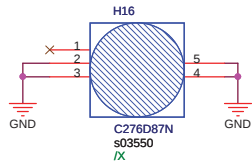
ESD?

3/26_Item1

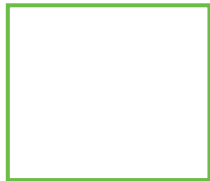
Internal BAT

<Variant Name>

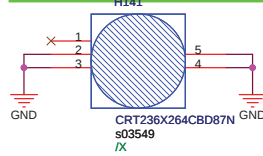
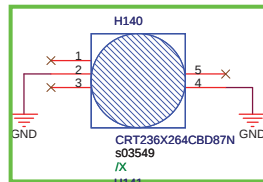
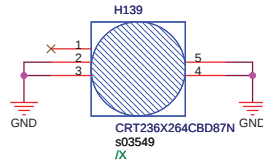
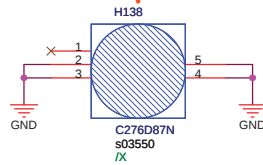
		Title : PWR Jack	
ASUSTek Computer INC.		Engineer: N/A	
Size A4	Project Name 1101HA		Rev 1.2
Date: Tuesday, July 21, 2009	Sheet	38	of 50



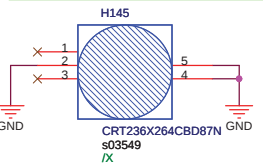
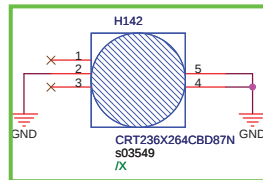
3/27_Item15



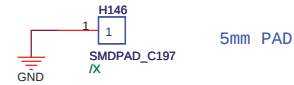
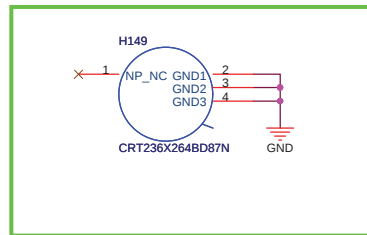
4/3_Item3



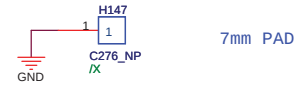
4/8_Item1



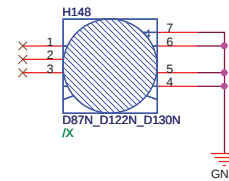
4/6_Item4



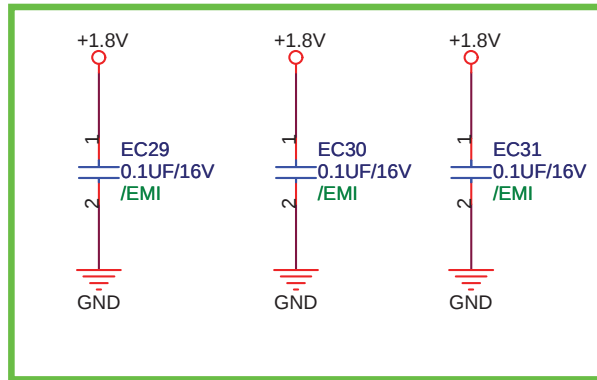
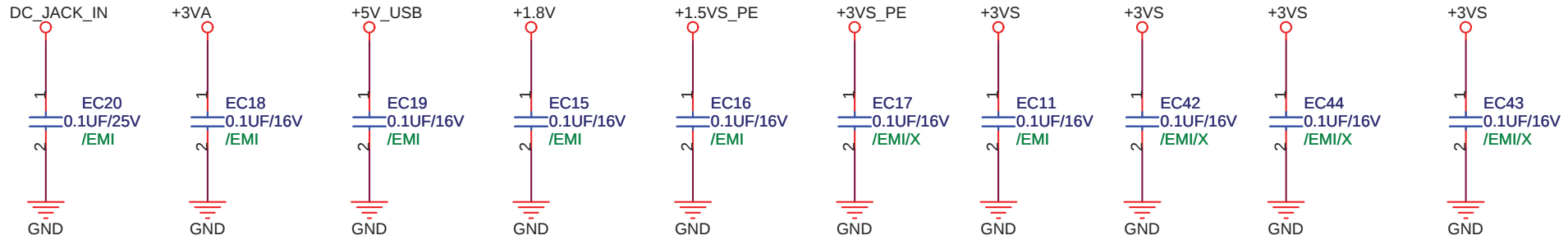
5mm PAD



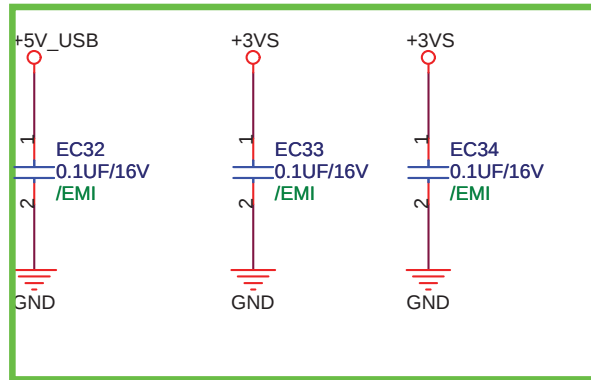
7mm PAD



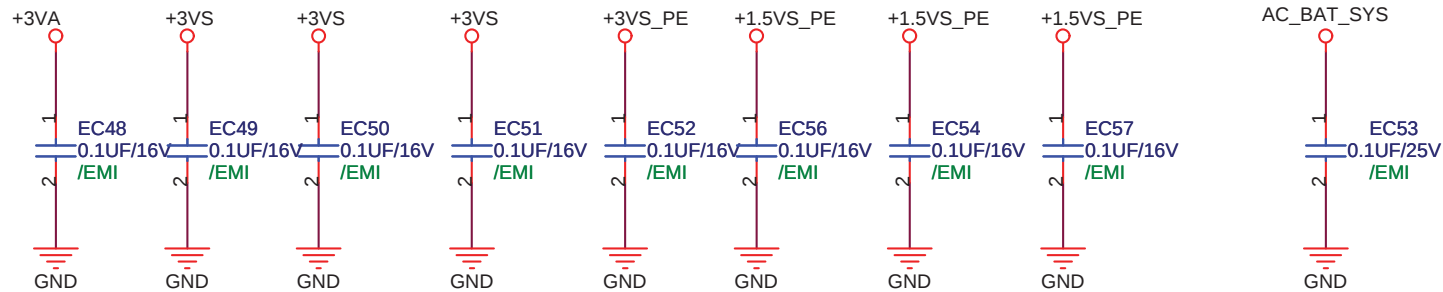
<Variant Name>



4/6_Item1



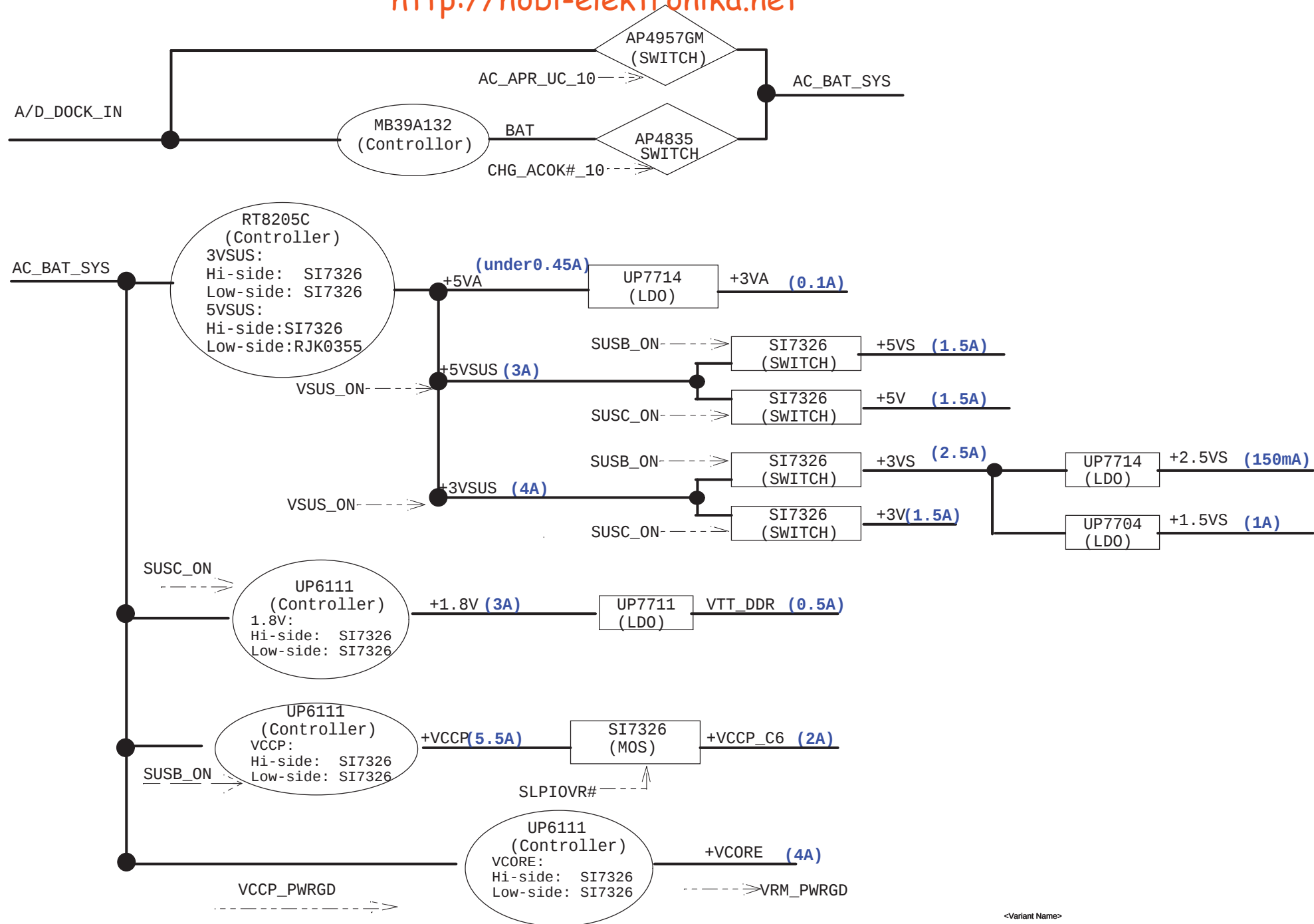
4/6_Item2



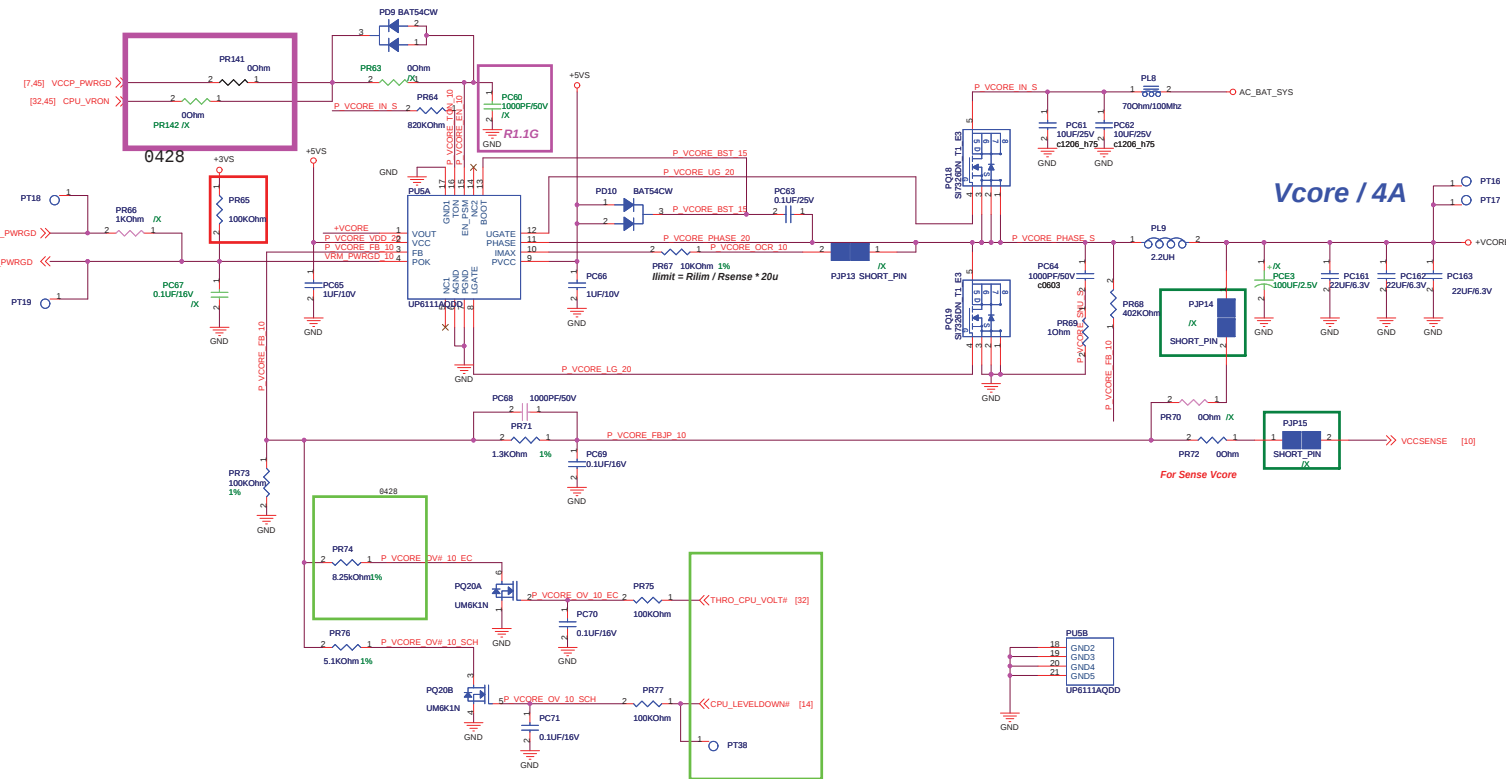
4/8_Item2

<Variant Name>

		Title : EMI	
ASUSTek Computer INC.		Engineer: N/A	
Size A	Project Name 1101HA		Rev 1.2
Date: Tuesday, July 21, 2009		Sheet	40 of 50



<Variant Name>



R1.2G

	Status			
THRO_CPU_VOLT#	H	L	H	L
CPU_LEVELDOWN#	H	H	L	L
Voltage	1.068V	0.9502V	0.8775V	0.7597V
	Normal	Normal + Throttle	Power Saving	Power Saving + Throttle

Controller

1. Voltage & Current:

+0.7598~1.048V@4A

2. Frequency:

PR7=1M ohm Fosc=250KHz

3. OCP:

PR13=10K ohm -> 9.09A

4. POR:

POR Hysteresis =0.2V
V on =3.9V

5. UVP:

Vout*70%

6. OVP:

Vout*115%

7. Enable Voltage:

V = 2.9 V

8. Soft start time:

Tss=1.2 ms

9. Phase selection:

N/A

10. Inrush Current:

C total = 100 uF
I inrush= 0.088 A

Power stage

1. I/P Current:

$I_{in} = V_o \cdot I_o / (0.8 \cdot V_{in}) = 0.47A$

2. Ripple Current:

$I_{rip} = 1.28A$
 $I_{spec} = 2.5A \cdot 2 \text{ pcs}$

3. Dynamic:

$I_{peak} = 4A$
ESR / 1 pcs = 18 mohm
 $\Delta V = 72mV$

4. Inductor Spec:

$I_{sat} = 14A$
 $I_{dc} = 8A$
DCR = 18 mohm

5. MOSFET Spec:

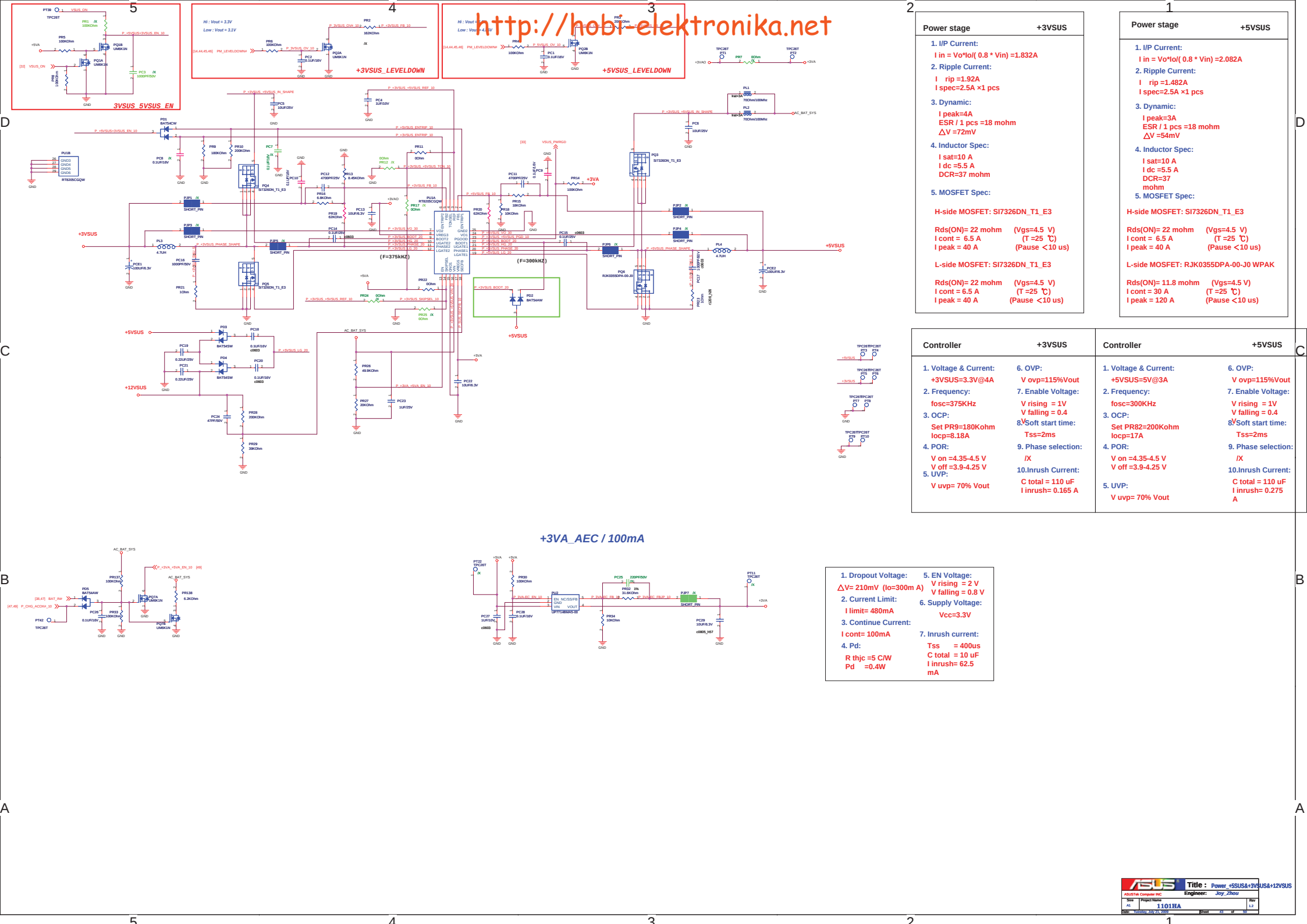
H-side MOSFET: SI7326DN_T1_E3

$R_{ds(ON)} = 22 \text{ mohm}$ ($V_{gs} = 4.5V$)
 $I_{cont} = 6.5A$ ($T = 25^\circ C$)
 $I_{peak} = 40A$ (Pause < 10 us)

L-side MOSFET: SI7326DN_T1_E3

$R_{ds(ON)} = 22 \text{ mohm}$ ($V_{gs} = 4.5V$)
 $I_{cont} = 6.5A$ ($T = 25^\circ C$)
 $I_{peak} = 40A$ (Pause < 10 us)

<Variant Name>



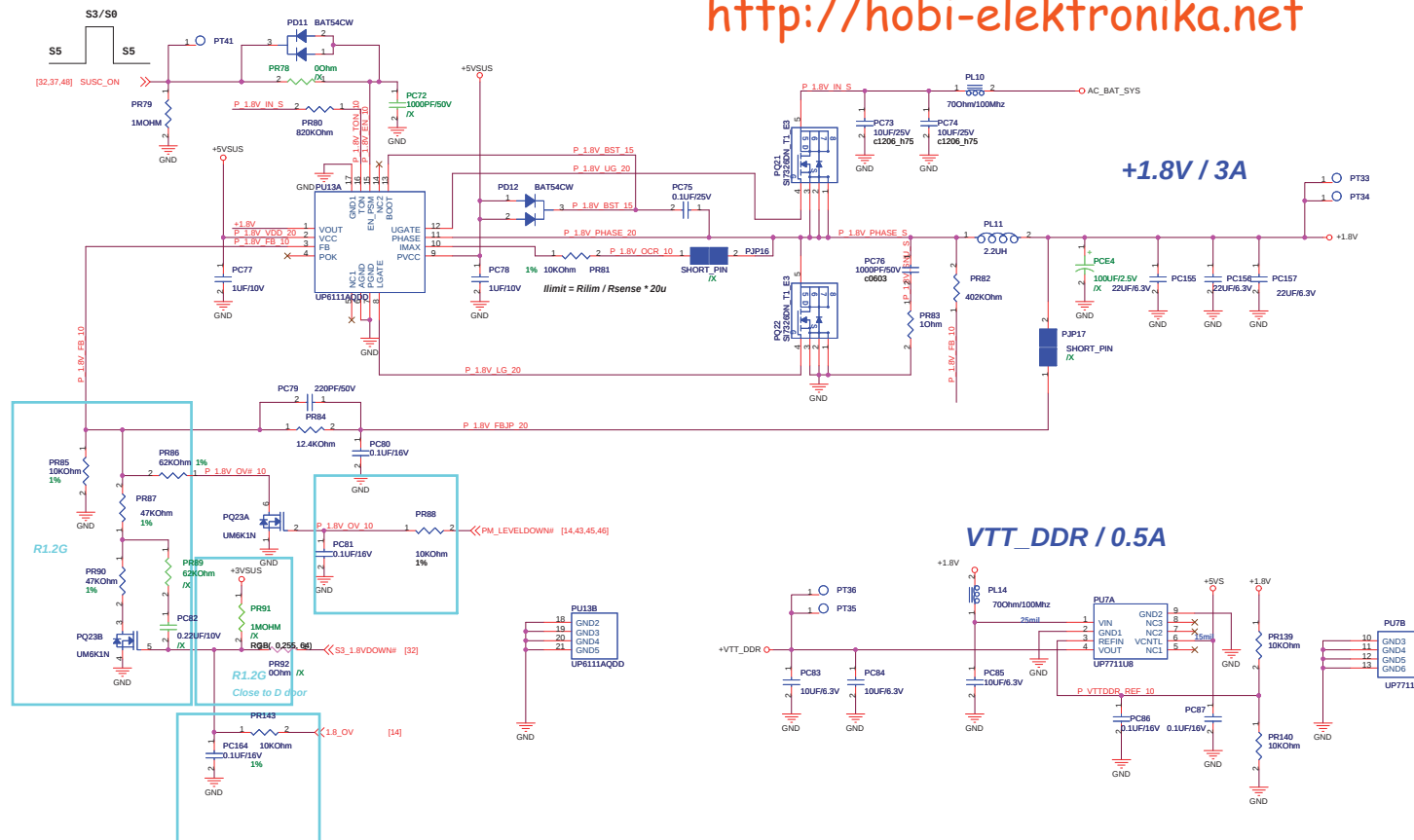
Power stage	+3VSUS
1. I/P Current:	$I_{in} = V_o \cdot I_o / (0.8 \cdot V_{in}) \approx 1.832A$
2. Ripple Current:	$I_{rip} \approx 1.92A$ $I_{spec} = 2.5A \times 1 \text{ pcs}$
3. Dynamic:	$I_{peak} = 4A$ $ESR / 1 \text{ pcs} = 18 \text{ mohm}$ $\Delta V = 72mV$
4. Inductor Spec:	$I_{sat} = 10A$ $I_{dc} = 5.5A$ $DCR = 37 \text{ mohm}$
5. MOSFET Spec:	H-side MOSFET: SI7326DN_T1_E3 $R_{ds(ON)} = 22 \text{ mohm}$ ($V_{gs} = 4.5V$) $I_{cont} = 6.5A$ ($T = 25^\circ C$) $I_{peak} = 40A$ (Pause < 10 us) L-side MOSFET: SI7326DN_T1_E3 $R_{ds(ON)} = 22 \text{ mohm}$ ($V_{gs} = 4.5V$) $I_{cont} = 6.5A$ ($T = 25^\circ C$) $I_{peak} = 40A$ (Pause < 10 us)

Power stage	+5VSUS
1. I/P Current:	$I_{in} = V_o \cdot I_o / (0.8 \cdot V_{in}) \approx 2.082A$
2. Ripple Current:	$I_{rip} \approx 1.482A$ $I_{spec} = 2.5A \times 1 \text{ pcs}$
3. Dynamic:	$I_{peak} = 3A$ $ESR / 1 \text{ pcs} = 18 \text{ mohm}$ $\Delta V = 54mV$
4. Inductor Spec:	$I_{sat} = 10A$ $I_{dc} = 5.5A$ $DCR = 37 \text{ mohm}$
5. MOSFET Spec:	H-side MOSFET: SI7326DN_T1_E3 $R_{ds(ON)} = 22 \text{ mohm}$ ($V_{gs} = 4.5V$) $I_{cont} = 6.5A$ ($T = 25^\circ C$) $I_{peak} = 40A$ (Pause < 10 us) L-side MOSFET: RJK0355DPA-00-J0 WPAK $R_{ds(ON)} = 11.8 \text{ mohm}$ ($V_{gs} = 4.5V$) $I_{cont} = 30A$ ($T = 25^\circ C$) $I_{peak} = 120A$ (Pause < 10 us)

Controller	+3VSUS
1. Voltage & Current:	+3VSUS=3.3V@4A
2. Frequency:	fosc=375KHz
3. OCP:	Set PR9=180Kohm Iocp=8.18A
4. POR:	V on =4.35-4.5V V off =3.9-4.25V
5. UVP:	V uvp= 70% Vout
6. OVP:	V ovp=115%Vout
7. Enable Voltage:	V rising = 1V V falling = 0.4V
8. Soft start time:	Tss=2ms
9. Phase selection:	/X
10. Inrush Current:	C total = 110 uF I inrush= 0.165 A

Controller	+5VSUS
1. Voltage & Current:	+5VSUS=5V@3A
2. Frequency:	fosc=300KHz
3. OCP:	Set PR8=200Kohm Iocp=17A
4. POR:	V on =4.35-4.5V V off =3.9-4.25V
5. UVP:	V uvp= 70% Vout
6. OVP:	V ovp=115%Vout
7. Enable Voltage:	V rising = 1V V falling = 0.4V
8. Soft start time:	Tss=2ms
9. Phase selection:	/X
10. Inrush Current:	C total = 110 uF I inrush= 0.275 A

1. Dropout Voltage:	5. EN Voltage:
$\Delta V = 210mV$ ($I_o = 300mA$)	V rising = 2V V falling = 0.8V
2. Current Limit:	6. Supply Voltage:
I limit= 480mA	Vcc=3.3V
3. Continue Current:	7. Inrush current:
I cont= 100mA	Tss = 400us C total = 10 uF I inrush= 62.5 mA
4. Pd:	
R thjc = 5 C/W Pd = 0.4W	



Power stage

1. I/P Current:
 $I_{in} = V_o \cdot I_o / (0.8 \cdot V_{in}) = 0.75A$

2. Ripple Current:
 $I_{rip} = 1.2A$
 $I_{spec} = 2.5A \cdot 1 \text{ pcs}$

3. Dynamic:
 $I_{peak} = 3A$
 $ESR / 1 \text{ pcs} = 18 \text{ mohm}$
 $\Delta V = 54mV$

4. Inductor Spec:
 $I_{sat} = 14A$
 $I_{dc} = 8A$
 $DCR = 18 \text{ mohm}$

5. MOSFET Spec:

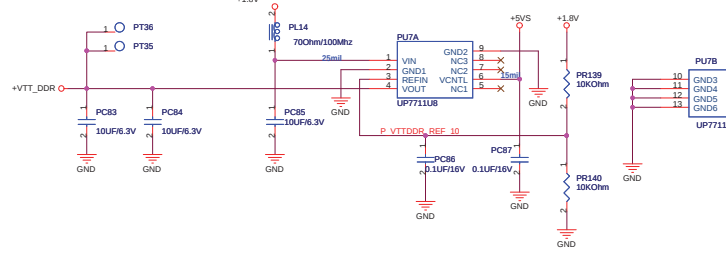
H-side MOSFET: SI7326DN_T1_E3

$R_{ds(ON)} = 22 \text{ mohm}$ ($V_{gs} = 4.5V$)
 $I_{cont} = 6.5A$ ($T = 25^\circ C$)
 $I_{peak} = 40A$ (Pause $< 10 \mu s$)

L-side MOSFET: SI7326DN_T1_E3

$R_{ds(ON)} = 22 \text{ mohm}$ ($V_{gs} = 4.5V$)
 $I_{cont} = 6.5A$ ($T = 25^\circ C$)
 $I_{peak} = 40A$ (Pause $< 10 \mu s$)

VTT_DDR / 0.5A



+VTTDDR@1A

1. Dropout Voltage:

$\Delta V = 0.3V$ ($I_o = 2A$)

2. Current Limit:

$I_{limit} = 4A$

3. Continue Current:

$I_{cont} = 3A$

4. Power Dissipation:

$R_{thjc} = 52^\circ C/W$

$P_d = 1.9W$

5. EN Voltage:

$V_{en} = 1.4V$

$V_{sd} = 0.8V$

6. Supply Voltage:

$V_{cc} = 5V$

7. Inrush current:

$T_{ss} = 5ms$

$C_{total} = 20 \mu F$

$I_{inrush} = 3.6mA$

1.8_OV	PM_LEVELDOWN#	Voltage	Status
L	L	1.65V	Power Saving
L	H	1.795V	Normal
H	H	1.89V	Super performance
H	L	1.746V	

Controller

1. Voltage & Current:

$+1.8V @ 3A$

2. Frequency:

$PR80 = 820K \text{ ohm}$

$F_{osc} = 300KHz$

3. OCP:

$PR184 = 10K \text{ ohm} \rightarrow 9A$

4. POR:

$V_{ccrth} = 3.7-4.1V$

$V_{cchys} = 0.2V$

5. UVP:

$V_{out} * 70\%$

6. OVP:

$V_{out} * 115\%$

7. Enable Voltage:

$V = 2.9V$

8. Soft start time:

$T_{ss} = 1.2ms$

9. Phase selection:

$/X$

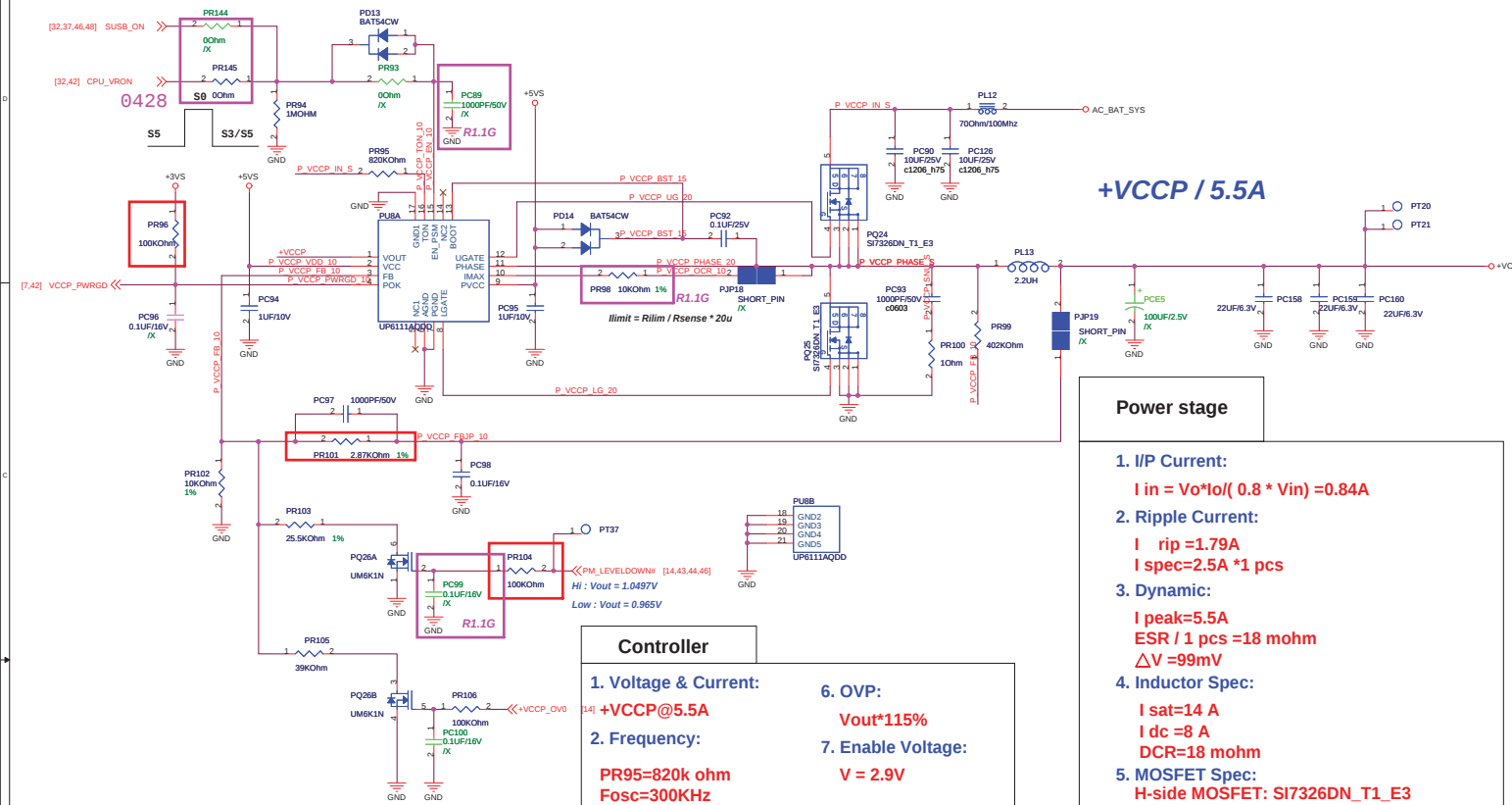
10. Inrush Current:

$C_{total} = 100 \mu F$

$I_{inrush} = 0.15A$

<Variant Name>

ASUS		Title : +1.8V & VTTDDR	
ASUSTek Computer INC.		Engineer: Joy_Zhou	
Size	Project Name	Rev	
A2	1101HA	1.2	
Date: Tuesday, July 21, 2009		Sheet 44 of 50	

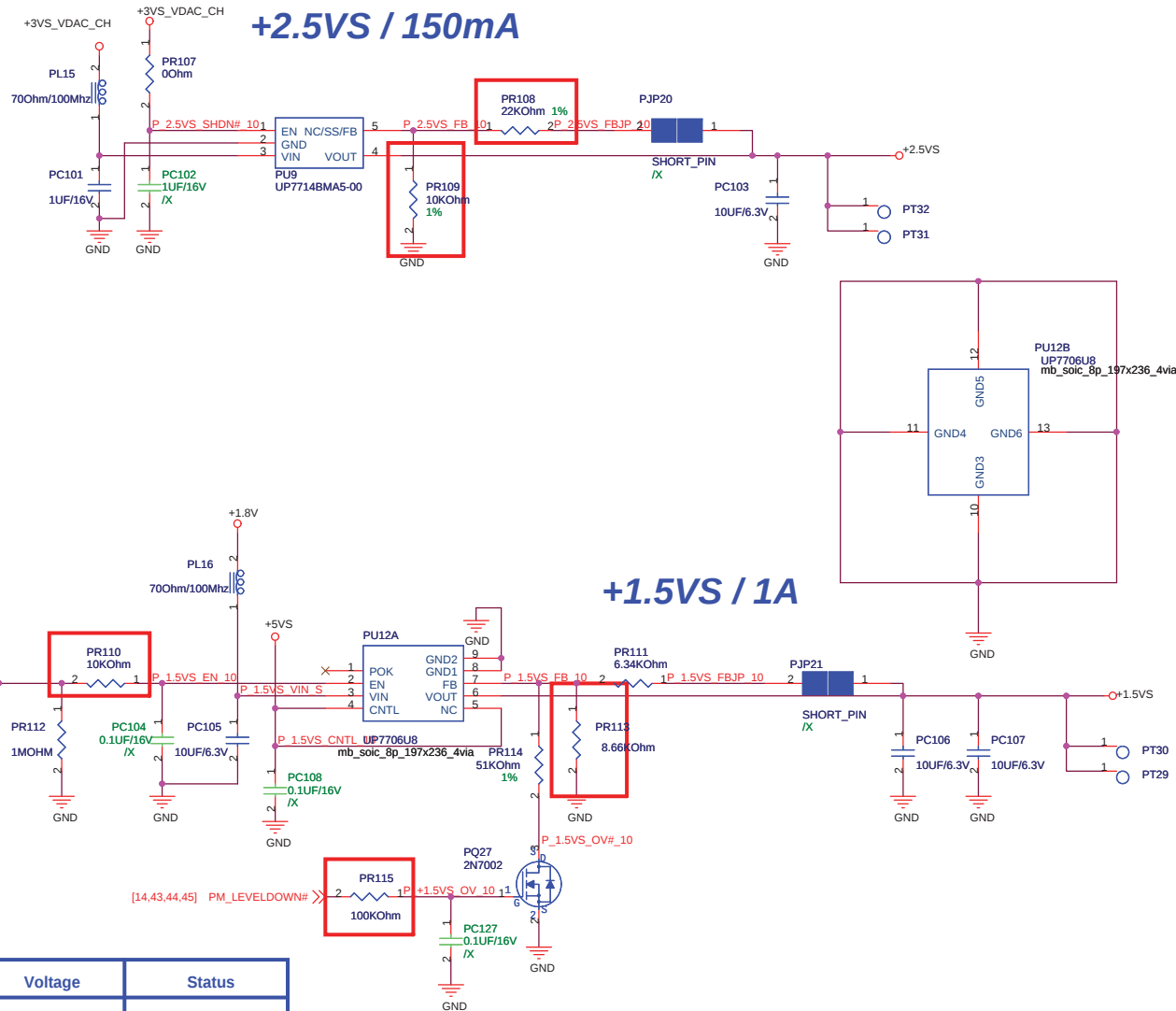


+VCCP_OV0	PM_LEVELDOWN#	Voltage	Status
L	L	0.965V	Power Saving
L	H	1.0497V	Normal
H	L	1.02V	/X
H	H	1.102V	Performance

Controller	
1. Voltage & Current:	6. OVP:
+VCCP@5.5A	Vout*115%
2. Frequency:	7. Enable Voltage:
PR95=820k ohm	V = 2.9V
Fosc=300KHz	8. Soft start time:
3. OCP:	Tss=1.2 ms
PR98=10K ohm -> 9A	9. Phase selection:
4. POR:	/X
Vccrth =3.7~4.1V	10.Inrush Current:
Vchys=0.2V	C total = 100 uF
5. UVP:	I inrush= 0.15 A
Vout*70%	

Power stage

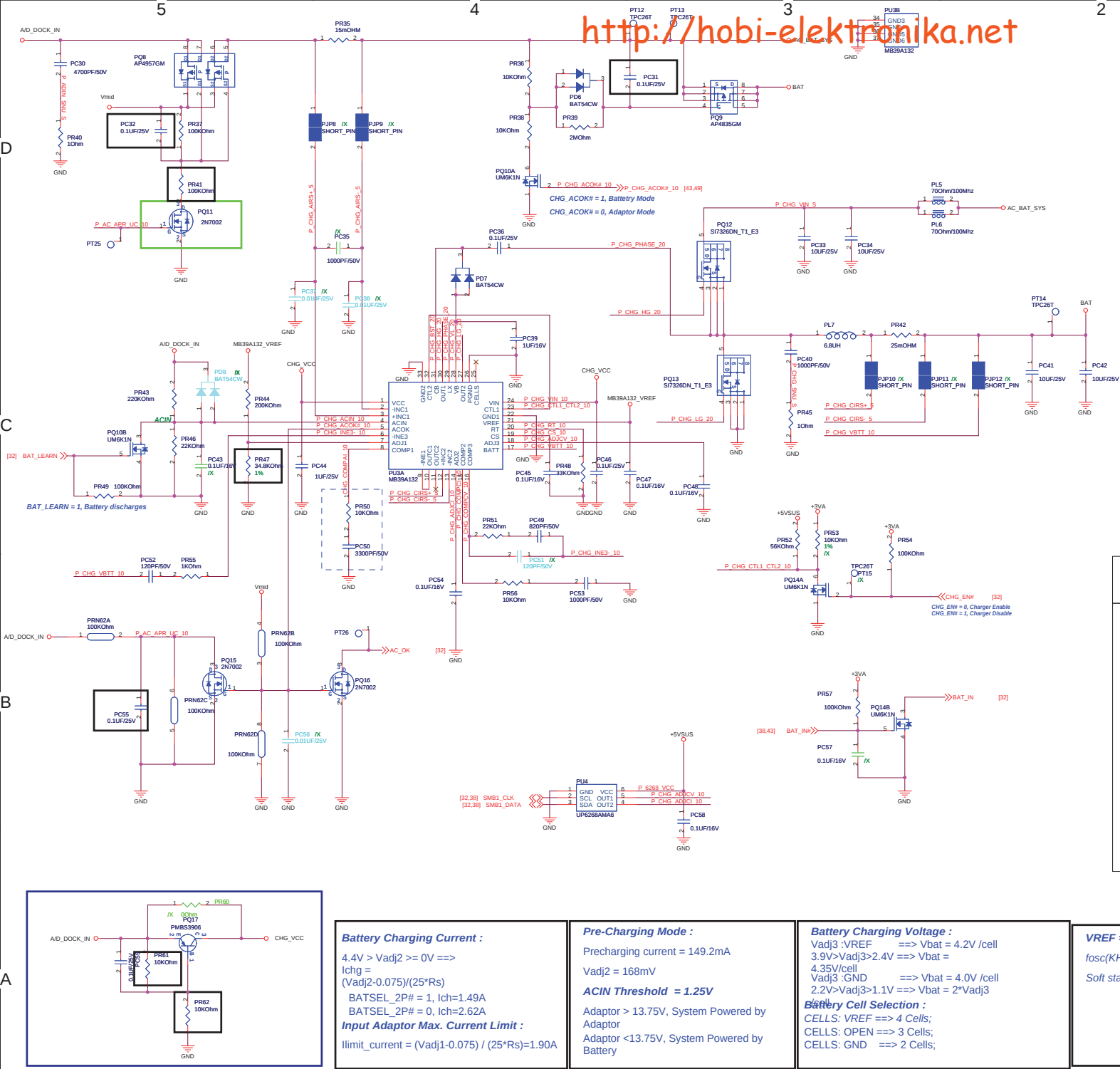
- I/P Current:
 $I_{in} = V_o * I_o / (0.8 * V_{in}) = 0.84A$
- Ripple Current:
 $I_{rip} = 1.79A$
 $I_{spec} = 2.5A * 1 pcs$
- Dynamic:
 $I_{peak} = 5.5A$
 $ESR / 1 pcs = 18 mohm$
 $\Delta V = 99mV$
- Inductor Spec:
 $I_{sat} = 14 A$
 $I_{dc} = 8 A$
 $DCR = 18 mohm$
- MOSFET Spec:
H-side MOSFET: SI7326DN_T1_E3
 $R_{ds(ON)} = 22 mohm$ ($V_{gs} = 4.5 V$)
 $I_{cont} = 6.5 A$ ($T = 25 ^\circ C$)
 $I_{peak} = 40 A$ (Pause < 10 us)
L-side MOSFET: SI7326DN_T1_E3
 $R_{ds(ON)} = 22 mohm$ ($V_{gs} = 4.5 V$)
 $I_{cont} = 6.5 A$ ($T = 25 ^\circ C$)
 $I_{peak} = 40 A$ (Pause < 10 us)



- Dropout Voltage:**
 $\Delta V = 210\text{mV}$ ($I_o = 300\text{mA}$)
- Current Limit:**
 $I_{\text{limit}} = 480\text{mA}$
- Continue Current:**
 $I_{\text{cont}} = 150\text{mA}$
- Pd:**
 $R_{\text{thjc}} = 5\text{ C/W}$
 $P_d = 0.4\text{W}$
- EN Voltage:**
 $V_{\text{rising}} = 2\text{V}$
 $V_{\text{falling}} = 0.8\text{V}$
- Supply Voltage:**
 $V_{\text{cc}} = 3.3\text{V}$
- Inrush current:**
 $T_{\text{ss}} = 400\mu\text{s}$
 $C_{\text{total}} = 10\mu\text{F}$
 $I_{\text{inrush}} = 62.5\text{mA}$

- Dropout Voltage:**
 $\Delta V = 300\text{mV}$ ($I_o = 2\text{A}$)
- Current Limit:**
 $I_{\text{limit}} = 2.8\text{A}$
- Continue Current:**
 $I_{\text{cont}} = 1\text{A}$
- Pd:**
 $R_{\text{thjc}} = 5\text{ C/W}$
 $P_d = 1.9\text{W}$
- EN Voltage:**
 $V_{\text{rising}} = 1.4\text{V}$
 $V_{\text{falling}} = 0.4\text{V}$
- Supply Voltage:**
 $V_{\text{cc}} = 5\text{V}$
- Inrush current:**
 $T_{\text{ss}} = 4\text{ms}$
 $C_{\text{total}} = 20\mu\text{F}$
 $I_{\text{inrush}} = 7.5\text{mA}$

<Variant Name>



Power stage

1. I/P Current:
 $I_{in} = V_o \cdot I_o / (0.8 \cdot V_{in}) = 1.64A$

2. Ripple Current:
 $I_{rip} = 1.18A$
 $I_{spec} = 2A \times 1$
pcs

3. Inductor Spec:
 $I_{sat} = 10A$
 $I_{dc} = 5.5A$
DCR=37mohm

4. MOSFET Spec:
H-side MOSFET: SI7326DN_T1_E3
 $R_{ds(ON)} = 22\text{ mohm}$ ($V_{gs} = 4.5V$)
 $I_{cont} = 6.5A$ ($T = 25^\circ C$)
 $I_{peak} = 40A$ (Pause < 10 us)
L-side MOSFET: SI7326DN_T1_E3
 $R_{ds(ON)} = 22\text{ mohm}$ ($V_{gs} = 4.5V$)
 $I_{cont} = 6.5A$ ($T = 25^\circ C$)
 $I_{peak} = 40A$ (Pause < 10 us)

Controller

1. Voltage & Current:
+12.6V@2.5A

2. Frequency:
PR122=33KOHM,
Fosc=515KHz

3. OCP:
POR:
POR Hysteresis =0.1V
V on =7.5V

5. Enable Voltage:
V = 2.9 V

6. Soft start time:
Tss=23ms

7. Phase selection:
N/A

8. Inrush Current:
C total =20uF
I inrush= 0.01A

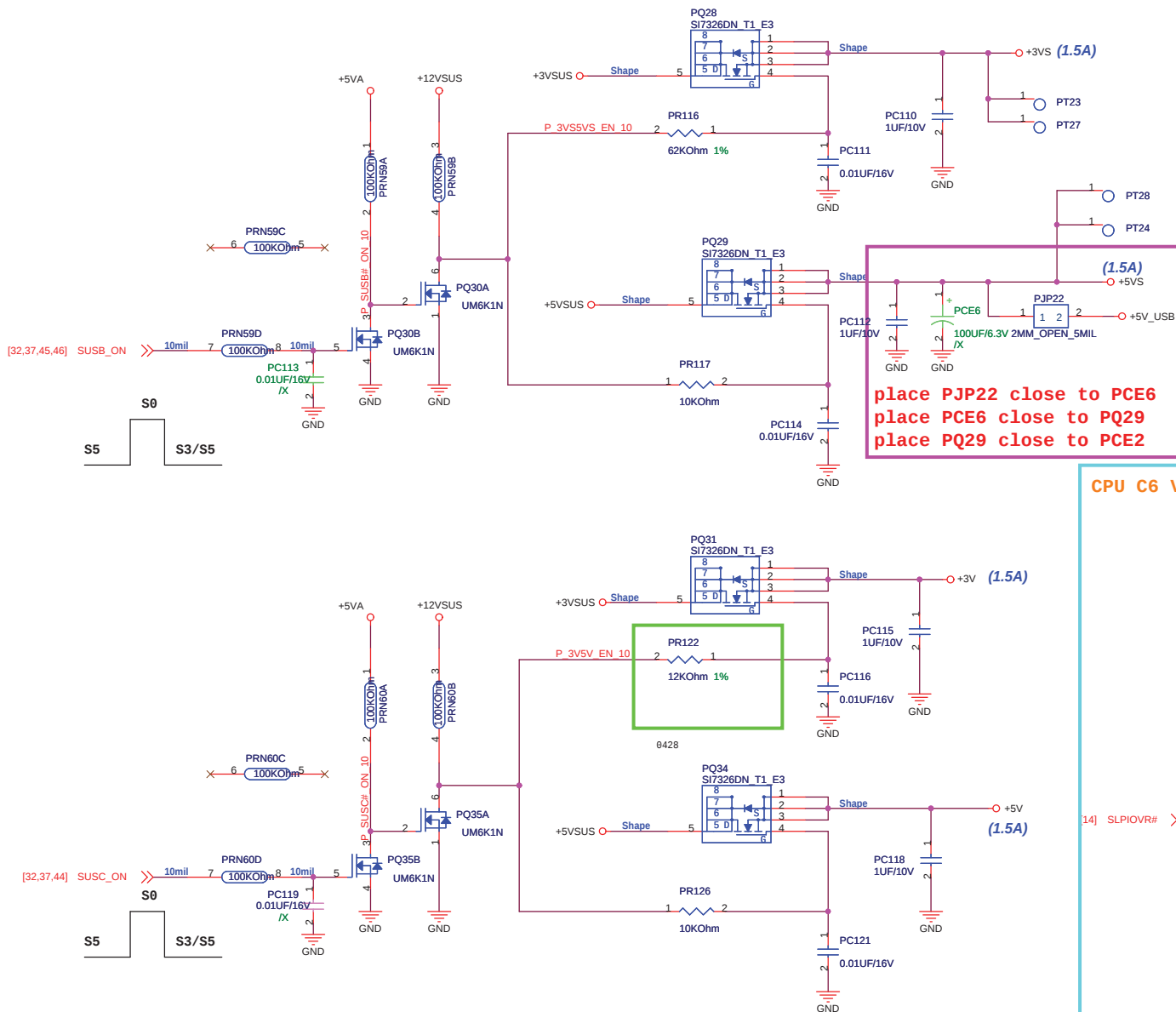
Battery Charging Current :
 $4.4V > V_{adj2} \geq 0V \Rightarrow$
 $I_{chg} = (V_{adj2} - 0.075) / (25 \cdot R_s)$
BATSEL_2P# = 1, $I_{ch} = 1.49A$
BATSEL_2P# = 0, $I_{ch} = 2.62A$
Input Adaptor Max. Current Limit :
 $I_{limit_current} = (V_{adj1} - 0.075) / (25 \cdot R_s) = 1.90A$

Pre-Charging Mode :
Precharging current = 149.2mA
 $V_{adj2} = 168mV$
ACIN Threshold = 1.25V
Adaptor > 13.75V, System Powered by Adaptor
Adaptor < 13.75V, System Powered by Battery

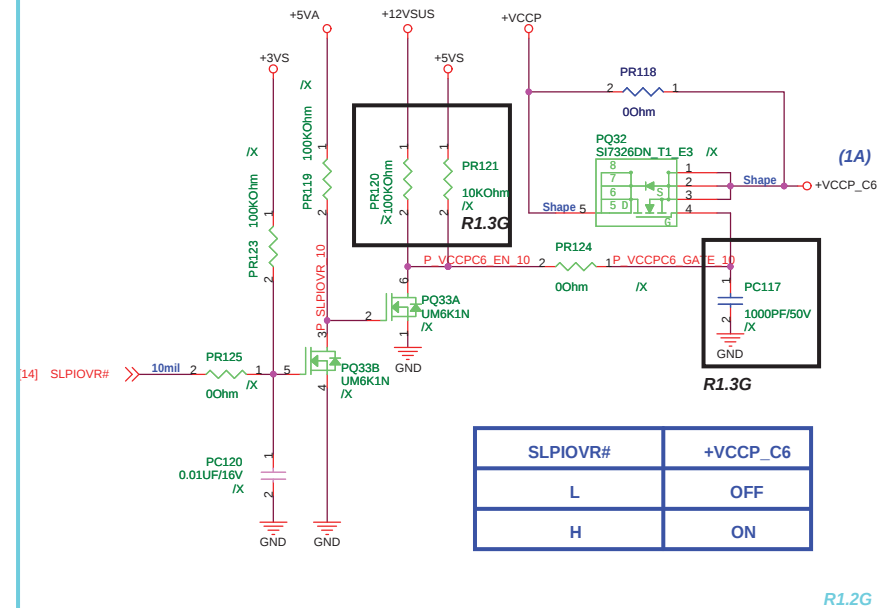
Battery Charging Voltage :
 $V_{adj3} : V_{REF} \Rightarrow V_{bat} = 4.2V / cell$
 $3.9V > V_{adj3} > 2.4V \Rightarrow V_{bat} = 4.35V / cell$
 $V_{adj3} : GND \Rightarrow V_{bat} = 4.0V / cell$
 $2.2V > V_{adj3} > 1.1V \Rightarrow V_{bat} = 2 \cdot V_{adj3}$
Battery Cell Selection :
CELLS: VREF $\Rightarrow 4$ Cells;
CELLS: OPEN $\Rightarrow 3$ Cells;
CELLS: GND $\Rightarrow 2$ Cells;

VREF = 5.0V
 $f_{osc}(KHz) = 17000 / RT (KOhm)$
Soft start: $t_s(s) = 0.13 \cdot CS (\mu F)$

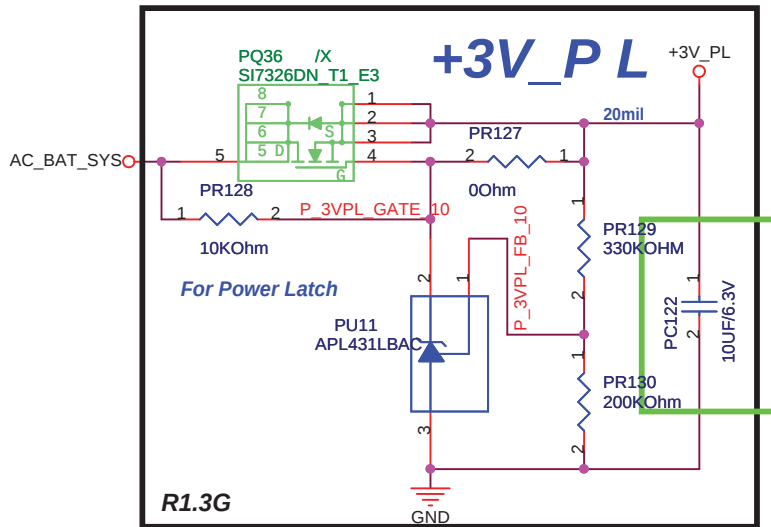
<Variant Name>



CPU C6 VCCP Switch



SLPIOVR#	+VCCP_C6
L	OFF
H	ON

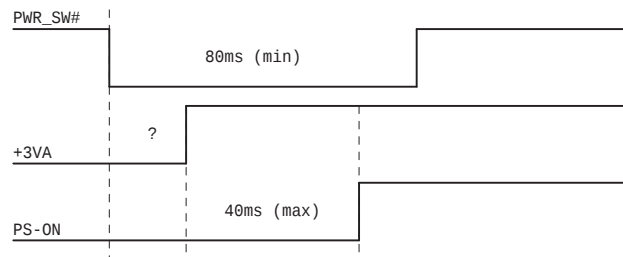
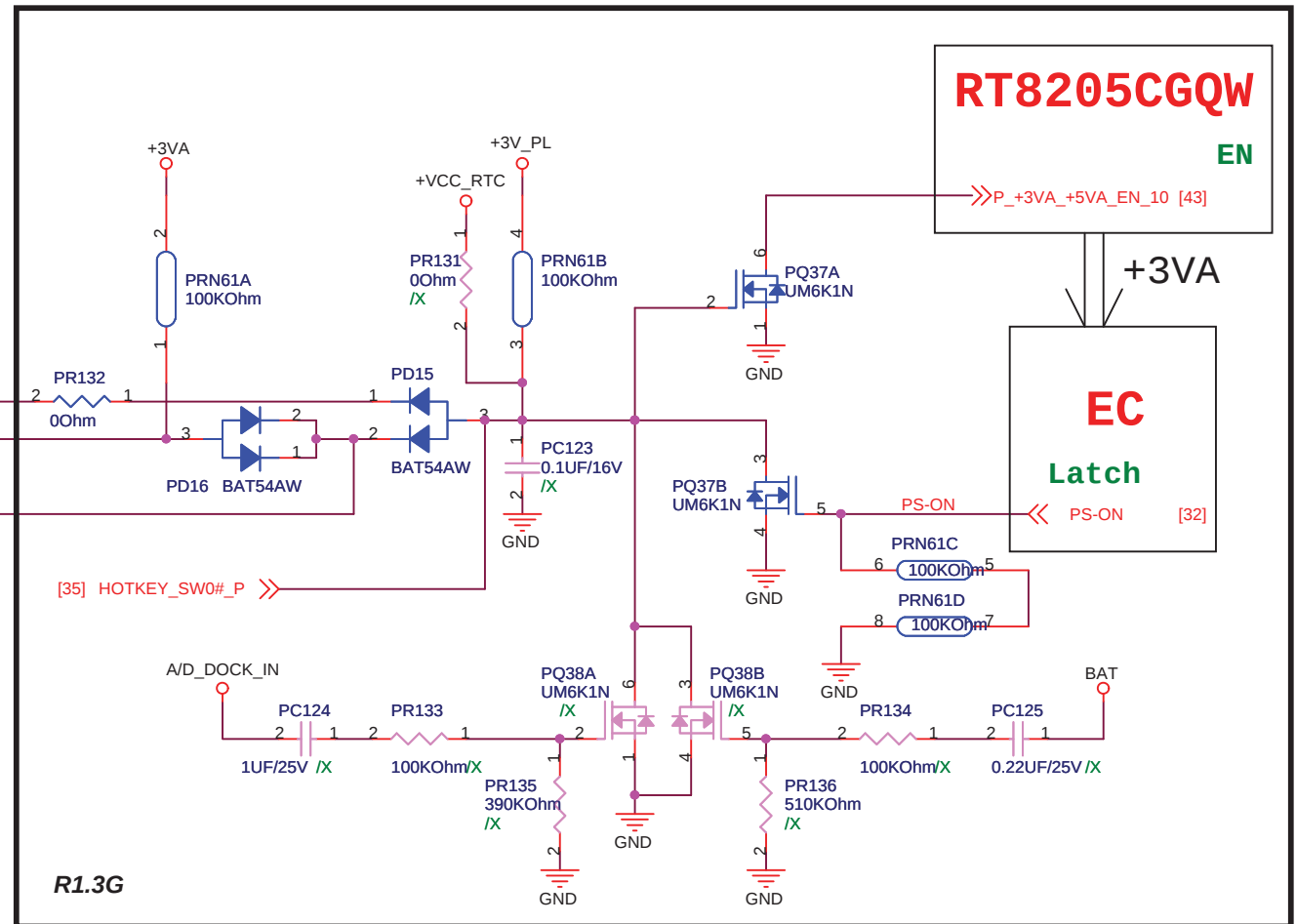


[43,47] P_CHG_ACOK#_10 >>

[29,32] PWR_SW_EC# >>

[29] PWR_SW# >>

[35] HOTKEY_SW0#_P >>



<Variant Name>

ASUS		Title : Power Latch	
ASUSTek Computer INC.		Engineer: Jerry Liu	
Size	Project Name		Rev
A4	1101HA		1.2
Date: Tuesday, July 21, 2009		Sheet	49 of 50

DATE
3/25_Item1 Page30 del IDE_PCSEL#1 circuit
3/25_Item2 Page30 change S_SATALED# to FLASH_LED#
3/25_Item3 Page14 USB_OC#0&USB_OC#1 combine to USB_OC#01 Page30 USB_OC#0 change to USB_OC#01 Page14/30/32 exchange USB port2 /port7 net name
3/25_Item4 Page34 circuit move to Page30
3/25_Item5 Page37 EC pin14 use as TP_LED#
3/25_Item6 Page13 del R196& CLK_PCI_UART
3/25_Item7 Page14 SCH GPIO2--> SIMCARD_IN#;GPIO1 -->HDD_ON Page23 add GR2
3/25_Item8 Page14 add Test point for USB port4&SB_SPKR
3/25_Item9 Page7 del EC34,CLK_48M_READER2
3/25_Item10 Page37 add TP for LID_EC_L#, CNT2_CHG#, CNT2_DIS#, GS1_INT1, GS1_INT2
3/25_Item11 Page32 add +5V_USB source(+5VS&JP3201)
3/26_Item0 DEL unused page& rename page No.
3/26_Item1 P38 BAT2_IN#-->BAT_IN#; Reserve ESD Diode for SMB&BAT_IN# P32 BAT1_IN# -->BAT_IN ; Del BAT2_IN off-page
3/26_Item2 P10-Add VID & VSSSENCE for OC/UG Go back T91 solution
3/26_Item3 P31 Add JP3101 for +5VS /+5V_USB
3/26_Item4 P32 Define EC pin102-->CPU_OV0; pin103-->CPU_OV1— Define EC pin104 -->+VCCP_OV0; pin105-->+VCCP_OV1 —Define EC pin85 -->DDR_OV0; pin86-->DDR_OV1—
3/26_Item5 P08 Add net name H_IGNNE#
3/26_Item6 P13 Modify RTC circuit
3/26_Item7 P07,P14,P22,P32,P33,P35 Add RF optional circuit
3/26_Item8 P39 correct screw hole
3/26_Item9 P24 add short point for intel Echo peak pin define; ADD optinal 0 ohm for Echo peak and NE672 Aux power pin define
3/26_Item10 P27 Decrease component for LAN circuit
3/26_Item11 P29 Del D36 & FLASH_LED_P# & R123; Add CSL2; +VCC_FLASH change to +3VS P30 Del FLASH_LED_P# & SR16
3/26_Item12 P41--P49 add power new schematic
3/26_Item13 P31 del JP3201 (power page has this JP)
3/27_Item1 P29 YQ2B-->YQ1B; P35 TPQ2B-->TPQ1B
3/27_Item2 P21 VR8,VR9 Change to short JP
3/27_Item3 P21 Costdown RGB ESD Diode
3/27_Item4 P10 ADD optional Thermtrip# circuit
3/27_Item5 P41-P49 ADD power new circuit
3/27_Item6 P32 +VCCP_OV0 changed from EC pin104 to SCH GPIOUSUS3 P32 TP_LED# changed from EC pin14 to EC pin85 P14 CARD_READER_EN# changed from SCH GPIOUSUS3 to SCH GPIO1
3/27_Item7 P35 HOTKEY_SW0# Pull up change to +3VA
3/27_Item8 P29 Del HDD_ON CIRCUIT
3/27_Item9 P35 add CIRCUIT for EXPRESS GATE
3/27_Item10 P41-P49 add power new circuit
3/27_Item11 P18 change DIMM con to STD Type
3/27_Item12 P21 cost down U6, Del F1 Fuse
3/27_Item13 P27 LAN chip change to 02G911002601,modify LAN circuit (need check pin define)
3/27_Item14 P08 R14,R16 120 -->56 OHM; R15 68-->56OHM P18 MC5, MC9, MC10 -->/X P19 Cap Change to Array Cap for Costdown
3/27_Item15 P39 del H143,H144 for ME change

3/29_Item1 P22 add pull down 100k for LBLK1_EN
3/29_Item2 model name change to N12L
3/29_Item3 P21+5V_CRT -->+5V_CRT_F ,VR2 --> /X
3/29_Item4 P23 del power control circuit, add pull up for SIMCARD_IN#; 3G reset circuit-->/X
3/29_Item5 P13 add Test point T207 (strap pin)
3/29_Item6 P22 +3VS --> +3V_LCD
3/29_Item7 P27 add R179 -->/X (no WOL function)
3/30_Item1 P32 EC pin32 -->CRT_IN (pull up); pin85-->CRT_DACPWR_EN#; pin86 -->CRTDAC_RST# ; TP_LED#--> Pin18
3/30_Item2 P20 add CRT DAC power control circuit & CRT reset circuit P21 add CRT conn in circuit
3/30_Item3 P27 LAN pin5 connect to pin15 (not +3V_LAN)
3/30_Item4 P18 go back to STD. DIMM Conn
3/30_Item5 P21 correct Vsync & Hsync
3/30_Item6 P29 Re-define +5VSUS for I/O Brd pin 21 for PWR Led
3/30_Item7 P14 add pull down for WLAN_LED; P33 add cost down solution for Auto-boot circuit
3/30_Item8 P37 Array Resitor change to single type for future cost down
3/30_Item9 P32 CRT_IN change to EC pin14 (hot key 1)
3/31_Item1 P39 Add screw hole H149
3/31_Item2 P41-P49 add power new circuit
3/31_Item3 P24 WR9,WR11,WR13,WR14 Change to 0603 type
3/31_Item4 P19 change array cap to single type
3/31_Item5 P28 change 4R8p 0ohm to 2R4p type
3/31_Item6 P22 L84,L85,L86,L87 change to low cost part
3/31_Item7 P29 del camera USB common chock and 0 ohm (I/O brd already has)
3/31_Item8 All Colay 0 OHM Change to array type
3/31_Item9 P29 del IR3 (I/O brd already has a bead)
3/31_Item10 P30 del SRN1--SRN7 for costdown&layout
3/31_Item11 P34 Reserve OR29 for cost down
3/31_Item12 P23 Q20 change to 2N7002
3/31_Item13 P22 chage the RF Cap position for LVDS signals
3/31_Item14 P7,P13,P32 chage the crystal to low cost part
3/31 item15 Reserve CR29 for future cost down power latch circuit
4/1 item1 P14 add Pull up for PM_LEVELDOWN#&CPU_LEVELDOWN#,Pull down for +VCCP_OV0
4/1 item2 P20,21 add back up CRT DAC Reset&Power control solution
4/1 item3 P24 WU1 change to 06G030057013
4/1 item4 P16 Reserve HDA I/O power to +1.5VS ,P29 Camera_EN to +1.5VS P14 del CAMERA_EN
4/1 item5 P22 del GU13(+3V_LCD circuit) , P38 Del L3816 for Layout placement space
4/1 item6 P32 add OSL5,OSL6 for PM_RSTRDY#&PM_RSTWARN (debug)
4/2 item1 P27 swap LAN pin29/30 net name(add LR86,LR87 for 8132), add R64 for clock Voltage swing,add LC11,12,13,15 decoupling
4/2 item2 P32 modify BAT_IN2 pull down,BAT_IN pull High
4/2 item3 P27 del LR80 ,P28 add LC18 (/X)
4/2 item4 P21 reserve D13 for ESD
4/3 item1 P18/19/22/35 swap memory data/address/command, common choke, Keyboard I/O chip capacitors.
4/3 item2 P38 change DCIN_GND to GND.
4/3 item3 P39 change H140 pin 3&5 from GND to NC.
4/3 item4 P32 OR10 change to 0603 size
4/3 item5 P20 R209-->/X,R218,L6-->N/A (for Pre-ER)
4/5 item1 P24 del WLAN SMB for layout routing
4/5 item2 P40 add EMI cap
4/5 item3 swap for DIMM & chip resistors of clock Gen.

4/6 item1 P40 add EC29--EC31 as stitched CAPs.
4/6 item2 P40 add EC32--EC34 for EMI needed.
4/6 item3 swap RN6/RN18.
4/6 item4 P39 change H149 from s03549 to s04146.
4/6 item5 P14 change EC39 PIN1 definition from A_CLK to A_Z_BITCLK for EMI
4/6 item6 P29 exchange DUA_CON PIN 12&21 definition for EMI which was found problem in 1005.
4/7 item1 P39 change H142 pin 3 from GND to NC.
4/7 item2 P40 add CAPs for EMI request.
4/28 item1 P22 GC99 change to 0.22UF
4/28 item2 P24 add WC19,unstuff cut off power circuit
4/28 item3 P14 SCH GPIO8 use as +1.8V OV, and add pull up R228
4/28 item4 P41~P49add power circuit
4/28 item5 P37 /X Q13,Q17,R170,R174,R180 (costdown)
4/28 item6 P22 reserve EC back light control ,reserve C487 for +3V_LCD,reserve D22 for BL_EN control
4/29 item1 P7,P32 reserve PCI_CLK for EC for OC consideration
4/29 item2 P7 CR14 change from 10 to 30 ohm,add CC7 for VDDREF power noise
4/29 item3 P27 C457 change to 0 ohm
5/4 item1 add R145 & C475 for RF request.
5/4 item2 delete SL & JP for factory request.
5/6 VGA connector P/N change to 12G10110915M
5/7 Touchpad connector P/N change to 12G183401225