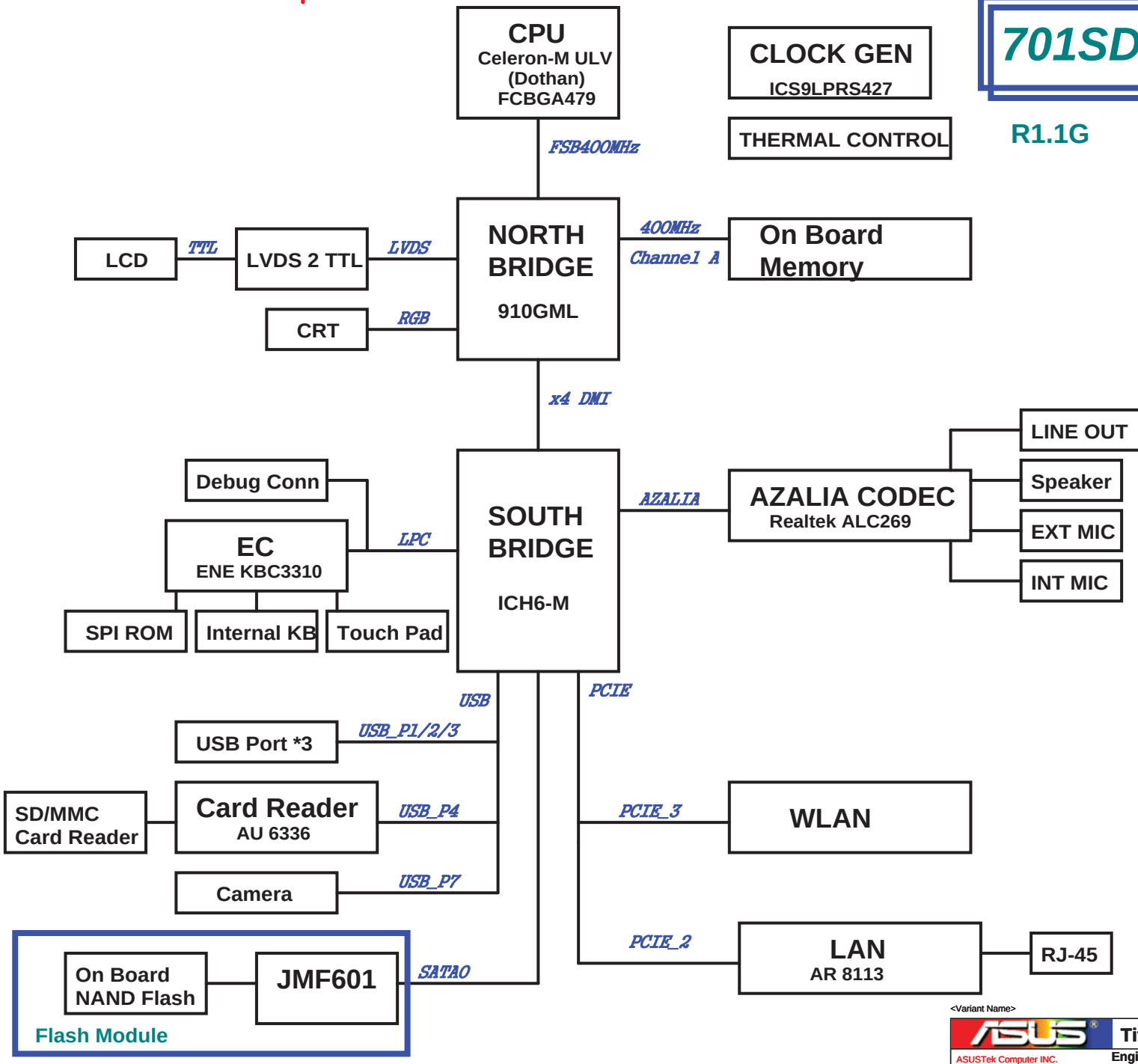
701SDX_MB

R1.1G



<Variant Name>

ASUSTek Computer INC.	Title : Block Diagram	
	Engineer: Hauld_Zhou	
Size: A3	Project Name: 701SDX_MB	Rev: R1.1G
Date: Wednesday, August 13, 2008	Sheet 1 of 49	

ICH6 GPIO SETTING

Pin	Pin Name	Connect to	Type	Input/Output Set
B7	GPI0/REQ6#	10K Pull +3V	I	fixed as Input only
E8	GPI1 / REQ5#	10K Pull +3V	I	fixed as Input only
D9	GPI2 / PIRQE#	10K Pull +3V	I	fixed as Input only
C7	GPI3 / PIRQF#	10K Pull +3V	I	fixed as Input only
C6	GPI4 / PIRQG#	10K Pull +3V	I	fixed as Input only
M3	GPI5 / PIRQH#	10K Pull +3V	I	fixed as Input only
AD19	GPI6 / BMBUSY#	NB BMBUSY#	I	Input
AE19	GPI7	NC	GPI	fixed as Input only
R1	GPI8	EC KBC_SCI#	GPI	fixed as Input only
C23	GPI9/OC4#	10K Pull +3V	I	Input
D23	GPI10/OC5#	10K Pull +3V	I	Input
W6	GPI11 / SMBALERT#	10K Pull +3V	I	Input
M2	GPI12	NC	GPI	fixed as Input only
R6	GPI13	EC EXTSMI#	GPI	fixed as Input only
C25	GPI14/OC6#	10K Pull +3V	I	Input
C24	GPI15 /OC7#	10K Pull +3V	I	Input
D8	GPO16/GTN6#	NC	O	Output
F6	GPO17 / GNT5#	NC	O	Output
AC21	GPO18 / STP_PCI#	Clock GEN STP_PCI#	O	Output
AB21	GPO19	WLAN_LED#	GPO	fixed as Output only
AD22	GPO20 / STP_CPU#	STP_CPU#	O	Output
AD20	GPO21	NC	GPO	fixed as Output only
NA	GPIO22	NA	NA	NA
AD21	GPO23	NC	GPO	fixed as Output only
V3	GPIO24	WLAN	I/O	Output
P5	GPIO25	NC	I/O	Output

Pin	Pin Name	Connect to	Type	Input/Output Set
AF17	GPI26/SATA0GP	NC	GPI	(GPI)Input
R3	GPIO27	NC	I/O	Output
T3	GPIO28	NC	I/O	Output
AE18	GPI29 / SATA1GP	PCBVER0	GPI	(GPI)Input
AF18	GPI30 / SATA2GP	NC	GPI	(GPI)Input
AG18	GPI31 / SATA3GP	PCBVER1	GPI	(GPI)Input
AF19	GPIO32 / CLKRUN#	10K Pull +3V	I/O	Input
AF20	GPIO33	NC	I/O	Output
AC18	GPIO34	NC	I/O	Output
NA	GPIO35	NA	NA	NA
NA	GPIO36	NA	NA	NA
NA	GPIO37	NA	NA	NA
NA	GPIO38	NA	NA	NA
NA	GPIO39	NA	NA	NA
F7	GPI40 / REQ4#	10K Pull +3V	I	Input
P4	GPI41 / LDRQ1#	NC	I	Input
NA	GPIO42	NA	NA	NA
NA	GPIO43	NA	NA	NA
NA	GPIO44	NA	NA	NA
NA	GPIO45	NA	NA	NA
NA	GPIO46	NA	NA	NA
NA	GPIO47	NA	NA	NA
E7	GPO48 /GNT4#	NC	O	Output
AC25	GPO49 / CPUPWRGD	CPU Power Ok	O	Output

<Variant Name>

ASUSTek Computer INC.

Title : System Setting

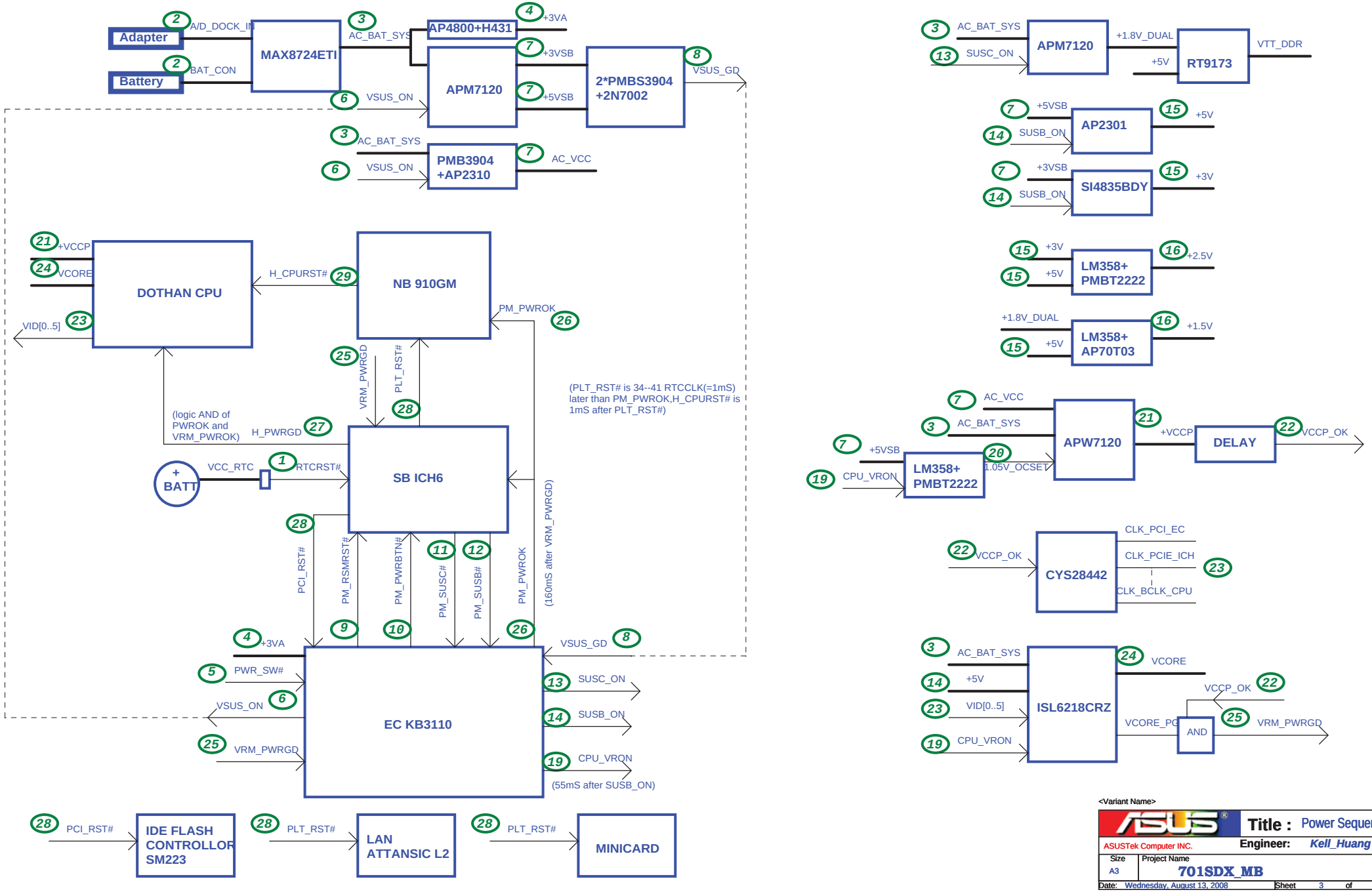
Engineer: Kell_Huang

Size	Project Name	Rev
A3	701SDX_MB	R1.1G

Date: Wednesday, August 13, 2008 Sheet 2 of 49

*This sequence is for Battery Plug-in and no Adapter,
if Adapter Plug-in,the sequence change to:
A/D_DOCK_IN--->AC_BAT_SYS--->+3VA--->VSUS_ON--->+3VSB & +5VSB
--->VSUS_GD--->PM_REMRST#--->PWR_SW#--->PM_PWRBTN--->PM_SUSC#--->PM_SUSB#

	Signal	S0/S1	S3	S4/S5	Power
Only Battery	VSUS_ON	H	H	L	VSB
Adapter In	VSUS_ON	H	H	H	VSB
	SUSB_ON	H	L	L	Main
	SUSC_ON	H	H	L	DUAL



<Variant Name>

ASUSTek Computer INC.

Title : Power Sequence

Engineer: Kell_Huang

Size	Project Name	Rev
A3	701SDX_MB	R1.1G

Date: Wednesday, August 13, 2008 Sheet 3 of 49

EC KB3310 GPIO SETTING

Pin No.	Pin Name	Signal Name	Type	NOTE
1	GA20	A20GATE	O	A20GATE
2	KBRST#	RC_IN#	O	KBRST#
6	GPIO04	CTRL_CAMER_PWR	I	Default : High
13	PCIRST#	PCI_RST#	I	PCI Reset
14	GPIO07	N.C	O	Reserved
15	GPIO08	EXTSMI#	O	EXTSMI#, 10K Pull +3VSUS
16	GPIO0A	LID_EC#	I	LID_EC#, *
17	GPIO0B	LCD_CSB	O	LCD chip select
18	GPIO0C	LCD_SDA	I/O	LCD Data
19	GPIO0D	DISTP_SW#	I	Touch Pad Disabled,*
20	SCI#	KBC_SCI#	O	KBC_SCI#, 10K Pull +3VSUS
21	PWM1	BL_PWM_DA	O	LCD Light Switch
23	PWM2	LCD_SCL	O	LCD clock
25	GPIO11	PM_PWRBTN#	OD	Power Button to SB, *
26	FANPWM1	FAN0_PWM	O	CPU Fan(Unused)
27	FANPWM2	FAN1_PWM	O	VGA Fan(Unused)
28	FANFB1	FAN0_TACH	I	CPU FanTach(Unused)
29	FANFB2	FAN1_TACH	I	VGA FanTach(Unused)
30	GPIO16	E51_TX	O	RS232 debug port
31	GPIO17	N.C	O	Reserved
32	GPIO18	PWR_SW#	I	power button, *
34	GPIO19	MAIL_LED#	O	Mail LED(Unused)
36	GPIO1A	CTRL_Mincard_PWR	O	Default : High
38	CLKRUN#	N.C	O	Reserved
39	KSO0	KSO0	O	For Keyboard interface
40	KSO1	KSO1	O	For Keyboard interface
41	KSO2	KSO2	O	For Keyboard interface
42	KSO3	KSO3	O	For Keyboard interface
43	KSO4	KSO4	O	For Keyboard interface
44	KSO5	KSO5	O	For Keyboard interface
45	KSO6	KSO6	O	For Keyboard interface
46	KSO7	KSO7	O	For Keyboard interface
47	KSO8	KSO8	O	For Keyboard interface
48	KSO9	KSO9	O	For Keyboard interface
49	KSO10	KSO10	O	For Keyboard interface
50	KSO11	KSO11	O	For Keyboard interface
51	KSO12	KSO12	O	For Keyboard interface
52	KSO13	KSO13	O	For Keyboard interface
53	KSO14	KSO14	O	For Keyboard interface
54	KSO15	KSO15	O	For Keyboard interface
55	KSI0	KSI0	I	For Keyboard interface
56	KSI1	KSI1	I	For Keyboard interface
57	KSI2	KSI2	I	For Keyboard interface
58	KSI3	KSI3	I	For Keyboard interface
59	KSI4	KSI4	I	For Keyboard interface
60	KSI5	KSI5	I	For Keyboard interface
61	KSI6	KSI6	I	For Keyboard interface
62	KSI7	KSI7	I	For Keyboard interface
63	AD0	P_PMON_10	I	Sense Power Loading
64	AD1	BAT_IN	I	sense Battery
65	AD2	N.C	I	Reserved
66	AD3	N.C	I	Reserved
68	GPO3C	DOC	O	Trigger Clock Gen

Pin No.	Pin Name	Signal Name	Type	NOTE
70	GPO3D	LCD_BACKOFF#	O	LCD_BACKOFF#
71	GPO3E	CLK_PWRSAVE#	O	Active when BAT_IN=1 and AC_OK=0(Unused)
72	GPO3F	BAT_LL#	O	Battery Low Low
73	GPIO40	AC_OK	I	AC Adaptor Plug in
74	GPIO41	PM_RSMRST#	O	10K Pull GND
75	GPIO42	N.C	O	Reserved
76	GPIO43	N.C	O	Reserved
77	SCL1	SMB0_CLK	I/OD	4.7K Pull +3VA_EC
78	SDA1	SMB0_DAT	I/OD	4.7K Pull +3VA_EC
79	SCL2	SMB1_CLK	I/OD	10K Pull +3VS
80	SDA2	SMB1_DAT	I/OD	10K Pull +3VS
81	KSO16	N.C	O	Reserved
82	KSO17	N.C	O	Reserved
83	PSCLK1	N.C	O	Reserved
84	PSDAT1	N.C	O	Reserved
85	PSCLK2	N.C	O	Reserved
86	PSDAT2	N.C	O	Reserved
87	PSCLK3	TP_CLK	I/OD	10K Pull +3VS
88	PSDAT3	TP_DAT	I/OD	10K Pull +3VS
89	GPIO50	BATSEL_3S	O	Battery series. Hi:3S, Lo:4S(Unused)
90	GPIO52	CHG_LED_UP#	O	charger LED
91	GPIO53	CTRL_L2_PWR	O	Default : High
92	GPIO54	PWR_LED_UP	O	EC H/W blinking
93	GPIO55	SCRL_LED#	O	EC H/W controls
95	GPIO56	PWR4G_SW#	I	*
97	GPXOA00	SPI_MODE#	O	"HW Strap for SPI Flash de External Pull Down 100K ohm to GND"
98	GPXOA01	SUSC_ON	O	
99	GPXOA02	VSUS_ON	O	
100	GPXOA03	CPU_VRON	O	
101	GPXOA04	SUSB_ON	O	
102	GPXOA05	ICH8_PWROK	O	
103	GPXOA06	N.C	O	Reserved
104	GPXOA07	CHG_EN#	O	Battery charging enabled
105	GPXOA08	PRECHG	O	
106	GPXOA09	SPI_WP#	O	
107	GPX0A10	OP_SD#	O	Audio OP
108	GPXOA11	BAT_LEARN	O	
109	GPXID0	BATSEL_2P#	O	Battery parallel. Hi:1P, Lo:2P~3P
110	GPXID1	N.C	O	Reserved
112	GPXID2	THRO_CPU	O	Active if Battery Temperature is
114	GPXID3	SUSB#	I	Pull Down 100K ohm to GND
115	GPXID4	SUSC#	I	Pull Down 100K ohm to GND
116	GPXID5	CPUPWR_GD	I	10K Pull +3VS
117	GPXID6	VSUS_GD	I	Disabled **
118	GPXID7	N.C	O	Reserved
121	GPIO57	INTERNET#	I	*
126	SPICLK	SPI_CLK	O	SPI Clock
127	GPIO59	N.C	O	Reserved

EC KB3310 Other Pin SETTING

Pin No.	Pin Name	Signal Name	Type	NOTE
3	SERIRQ	INT_SERIRQ	I/OD	8.2K Pull +3VS
4	LFRAME#	LPC_FRAME#	I	
5	LAD3	LPC_AD3	I/O	
7	LAD2	LPC_AD2	I/O	
8	LAD1	LPC_AD1	I/O	
9	VCC	+3VA_EC	P	
10	LAD0	LPC_AD0	I/O	
11	GND	GND	P	
12	PCICLK	CLK_PCI_EC	I	
22	VCC	+3VA_EC	P	
24	GND	GND	P	
33	VCC	+3VA_EC	P	
35	GND	GND	P	
37	ECRST#	EC_RST#	I	Add 100K ohm to GND
67	AVCC	+3VACC	P	
69	AGND	AGND	P	
94	GND	GND	P	
96	VCC	+3VA_EC	P	
111	VCC	+3VA_EC	P	
113	GND	GND	P	
119	RD#	SPI_SO	I	
120	WR#	SPI_SI	O	
112	XCLKI	32KXCLKI	I	
123	XCLKO	32KXCLKO	O	
124	V18R	K_V18R		Reserved 1uF to GND
125	VCC	+3VA_EC	P	
128	SPICS#	SPI_CE#	O	

<Variant Name>

ASUSTek Computer INC.

Title : EC Pin Define

Engineer: Kell_Huang

Size	Project Name	Rev
A3	701SDX_MB	R1.1G

Date: Wednesday, August 13, 2008 Sheet 4 of 49

CIRCUIT UPDATED HISTORY

Rev	Date	Description
1.0G		P704 Schematic 1.0G Beginning
701SD-4G 1.0G	2008.7.1	701SD-4G Schematic 1.0G Beginning 1.change the DIMM to onboard SDRAM 2.Add onboard Flash & controller,delete mini-PCIE connector 3.Delete Modem.

<Variant Name>

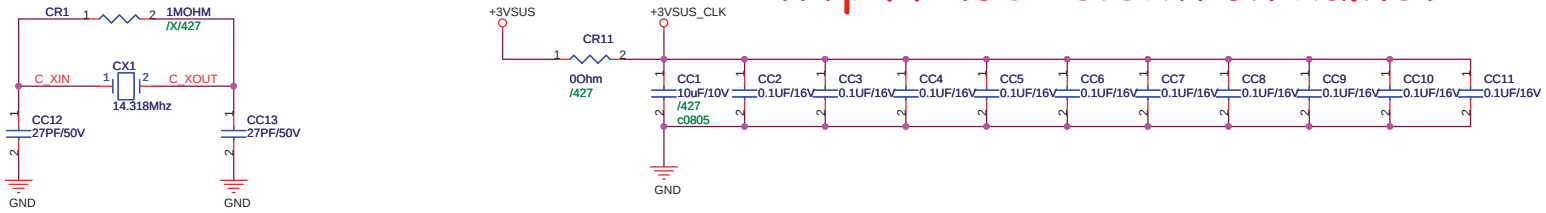
ASUSTek Computer INC.

Title : History

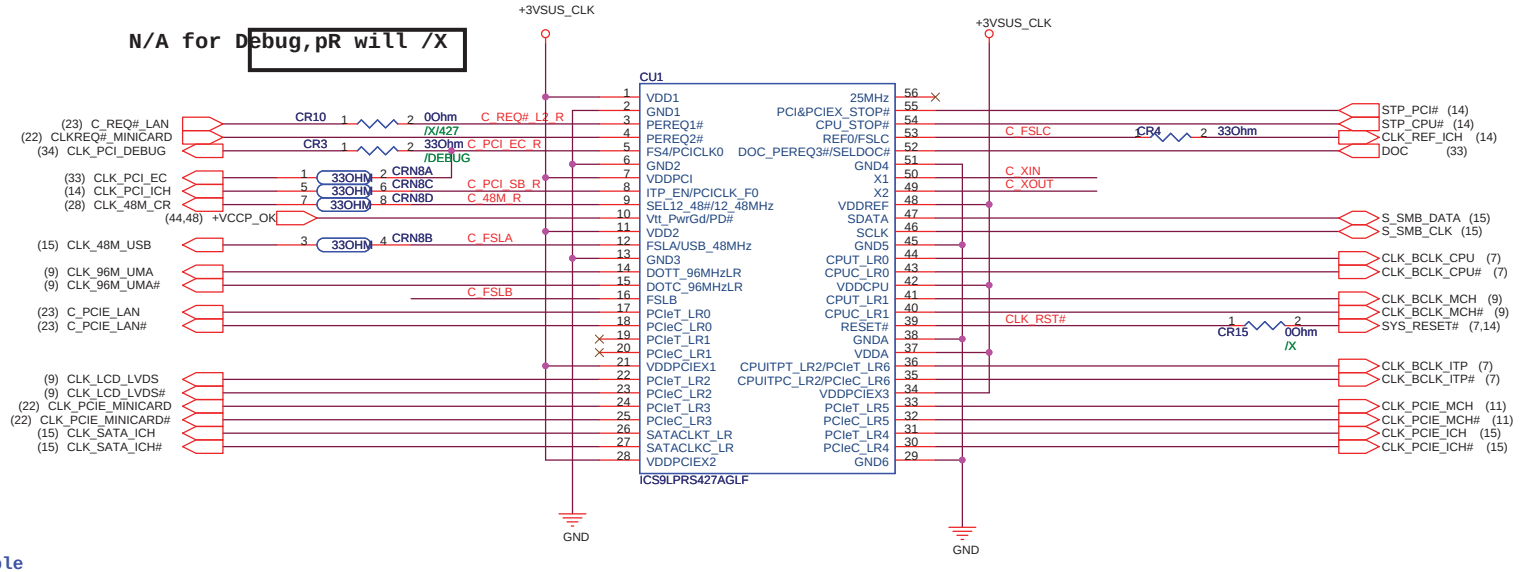
Engineer: Kell_Huang

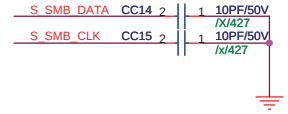
Size	Project Name	Rev
A3	701SDX_MB	R1.1G

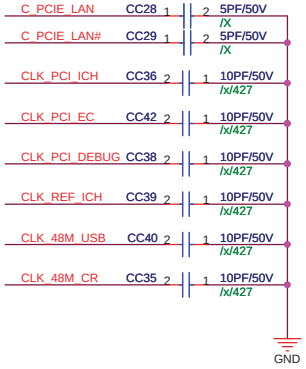
Date: Wednesday, August 13, 2008 Sheet 5 of 49



N/A for Debug,pR will /X

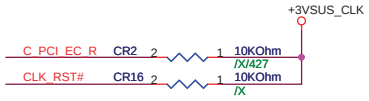


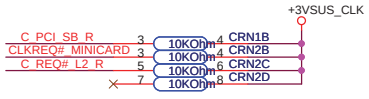


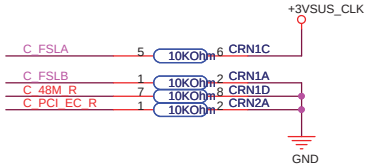


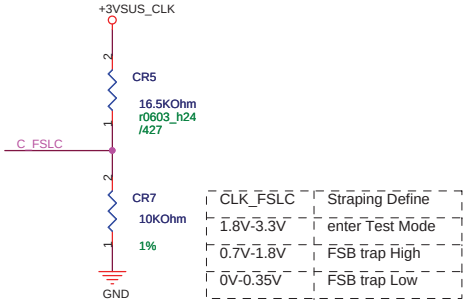
1:Disable
0:Enable

PEREQ1:PCIEx0 & PCIEx1
PEREQ2:PCIEx2 & PCIEx3 & SATA
PEREQ3:PCIEx4 & PCIEx5 & PCIEx6









FSLC	FSLB	FSLA	CPU(MHZ)
0	0	1	133.33
1	0	1	100

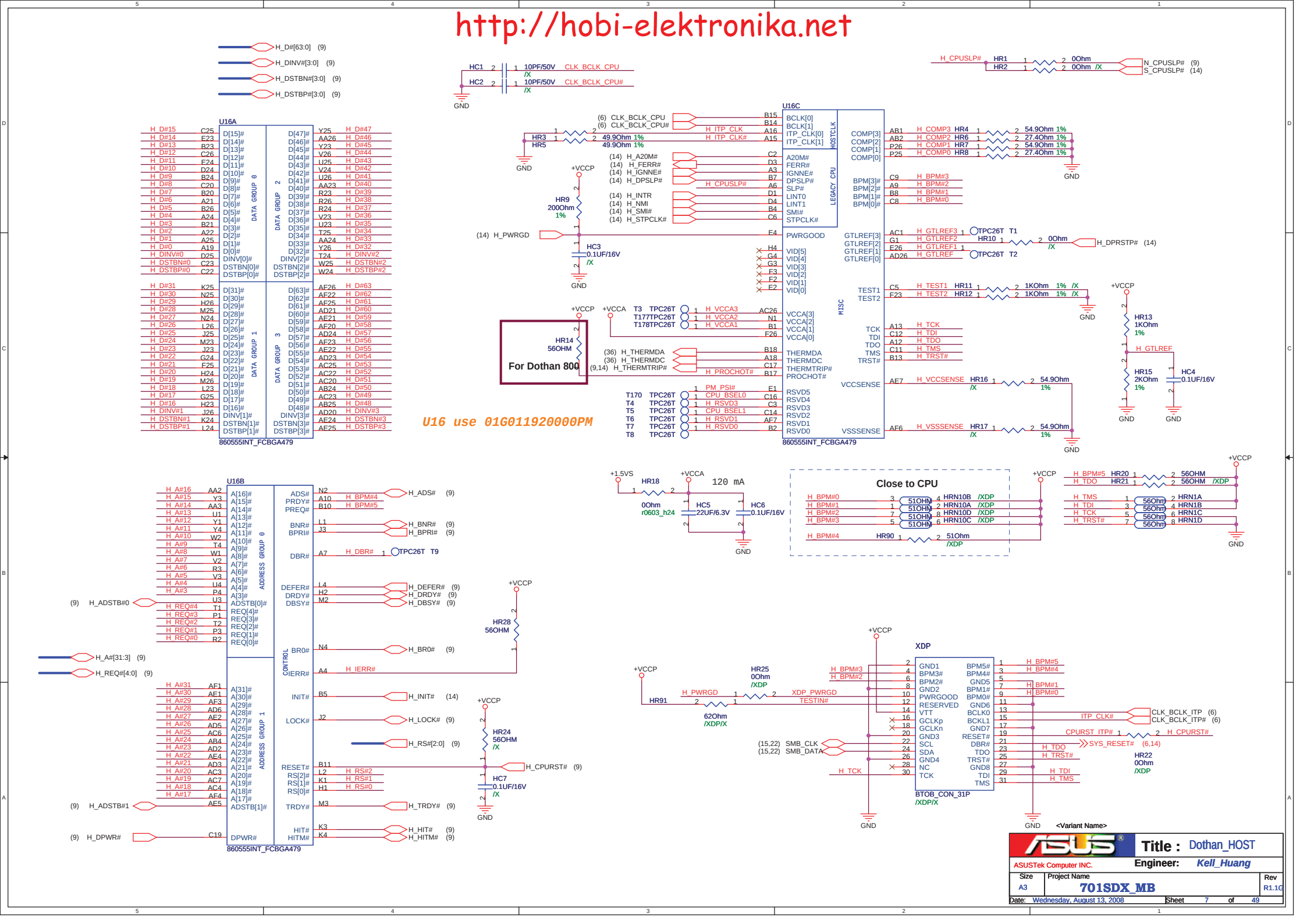
ASUSTek Computer INC.

Title : Clock Gen_ICS9LPR427

Engineer: Henry_Yang

Size	Project Name	Rev
A3	701SDX_MB	R1.1G

Date: Wednesday, August 13, 2008 Sheet 6 of 49



+VCCP 2.5 A

+VCORE Celeron-M(Dothan) ULV max 7 A

U16D

VCCP

860555INT_FCBGA479

U16E

GND

860555INT_FCBGA479

0.1U All X7R

HCE1 10UF/6.3V N/A c0805

HCE2 100UF/2V

HCE3 10UF/6.3V /X c0603

HCE4 100UF/2V /CAP/X

HC23 HC24 HC26 0.1UF/16V /CAP/X

HC27 HC28 HC29 10UF/6.3V /CAP/X

HC20 HC21 HC22 HC25 0.1UF/16V /CAP/X

HC10 HC11 HC12 HC13 HC14 HC15 HC16 10UF/6.3V /CAP/X

HC17 10UF/6.3V N/A c0805

HC18 10UF/6.3V /CAP/X

<Variant Name>

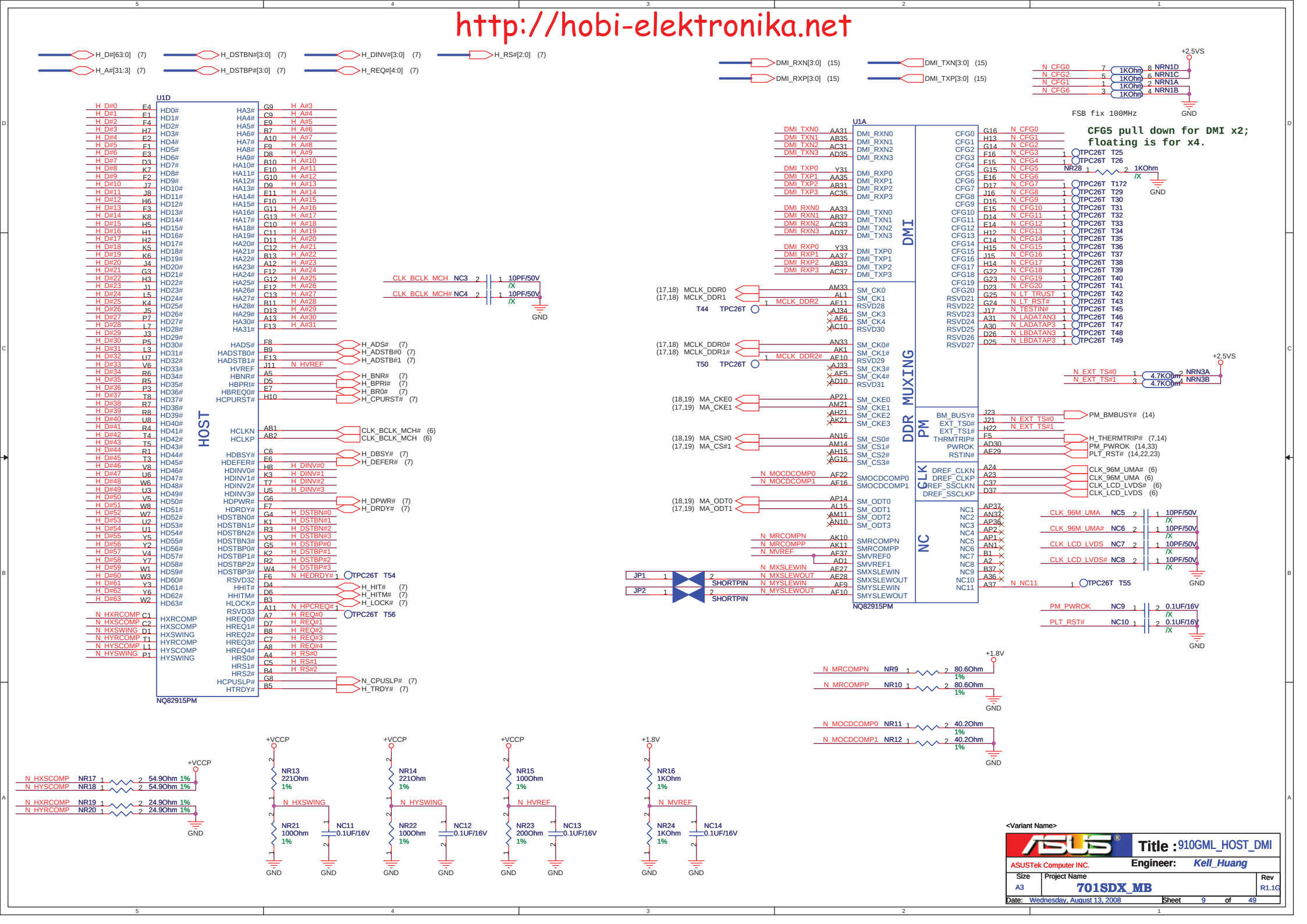
ASUSTek Computer INC.

Title : Dothan_PWR_GND

Engineer: Kell_Huang

Size	Project Name	Rev
A3	701SDX_MB	R1.1G

Date: Wednesday, August 13, 2008 Sheet 8 of 49



<Variant Name>
ASUSTek Computer INC.
Title : 910GML_HOST_DMI
Engineer: Kell_Huang
Size A3
Project Name 701SDX_MB
Rev R1.1G
Date: Wednesday, August 13, 2008
Sheet 9 of 49

MA_DQ[63:0] (17,18)
MA_DQS[7:0] (17,18)
MA_DQS#[7:0] (17,18)
MA_DM[7:0] (17,18)
MA_MA[13:0] (17,18,19)
MA_BA[2:0] (17,18,19)

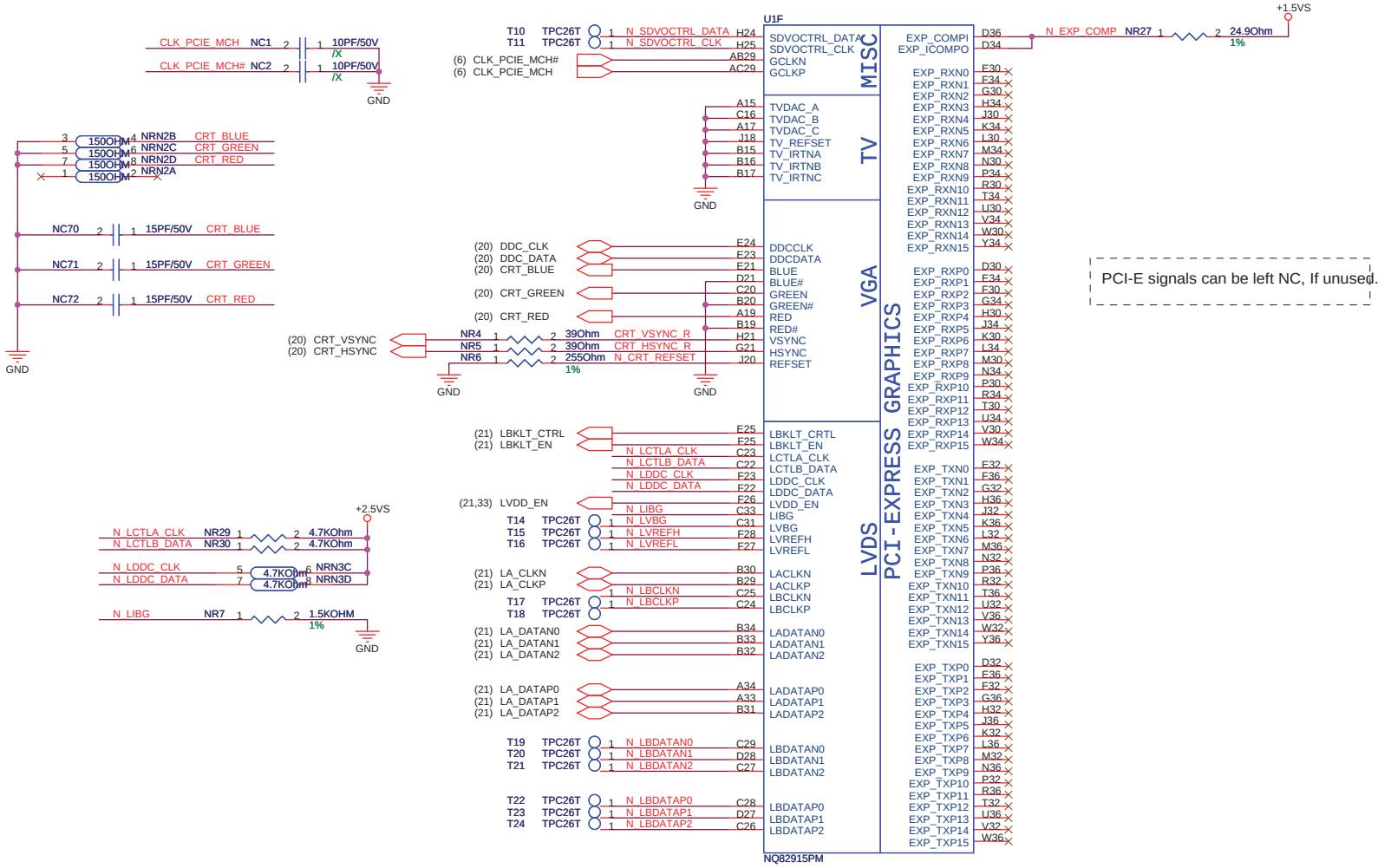
<Variant Name>

ASUSTek Computer INC.	Title : 910GML_DRAM	
	Engineer: Kell_Huang	
Size: A3	Project Name: 701SDX_MB	Rev: R1.1G
Date: Wednesday, August 13, 2008	Sheet 10 of 49	

SDVO SMbus have internal pull down

SDVOCRTL_DATA Int PD
0 : No SDVO device
1 : SDVO device present

U1 use 02G010007610



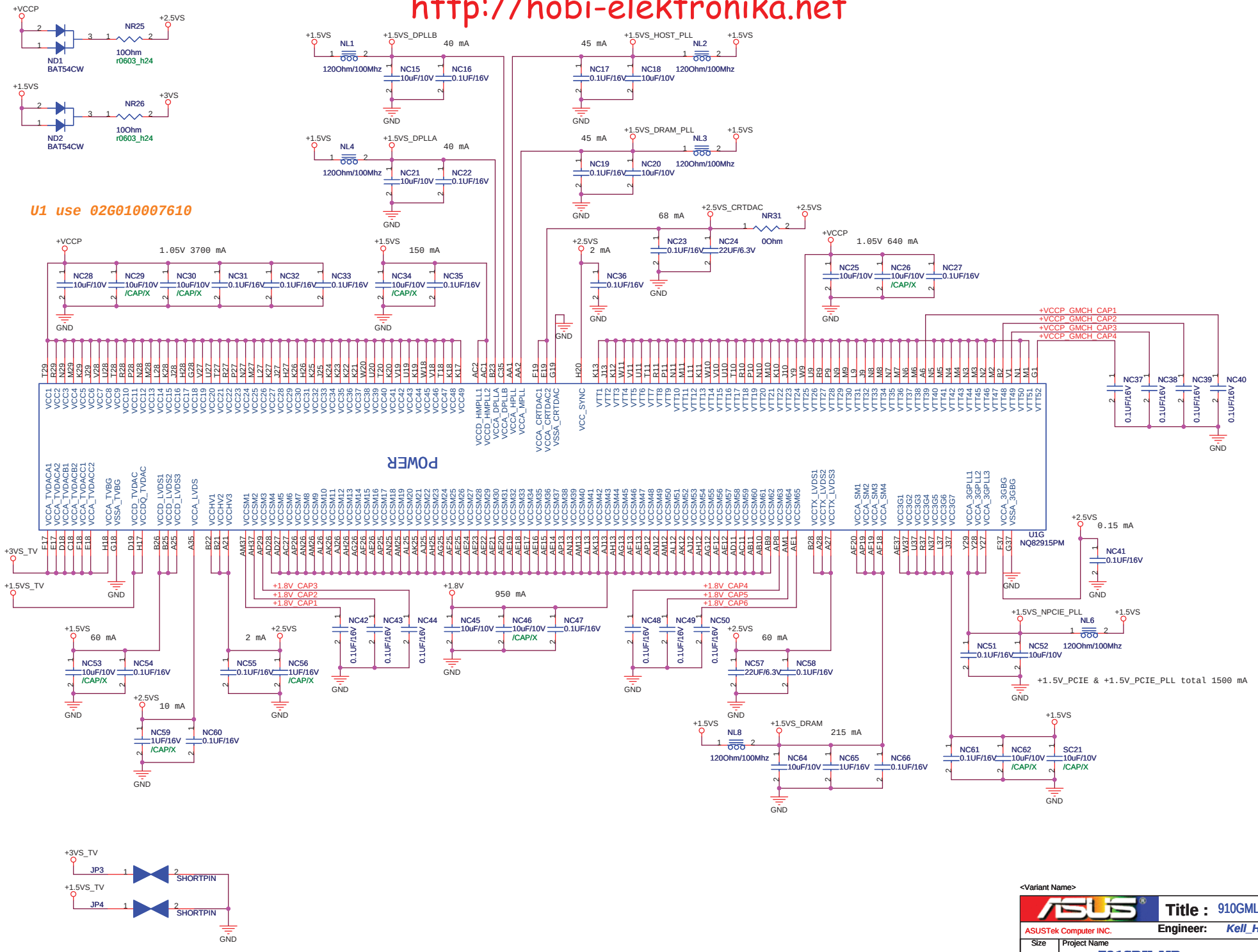
PCI-E signals can be left NC, If unused.

<Variant Name>

ASUSTek Computer INC.	Title : 910GML_VGA_LVDS	
	Engineer: Kell_Huang	
Size: A3	Project Name: 701SDX_MB	Rev: R1.1G
Date: Wednesday, August 13, 2008	Sheet 11 of 49	

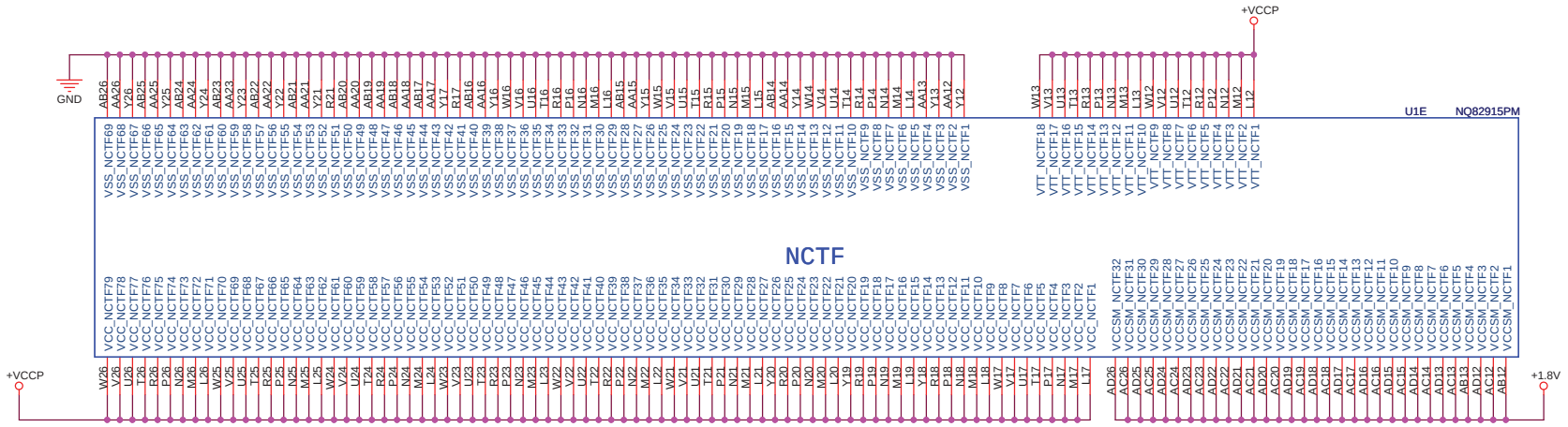
U1 use 02G010007610

POWER



<Variant Name>

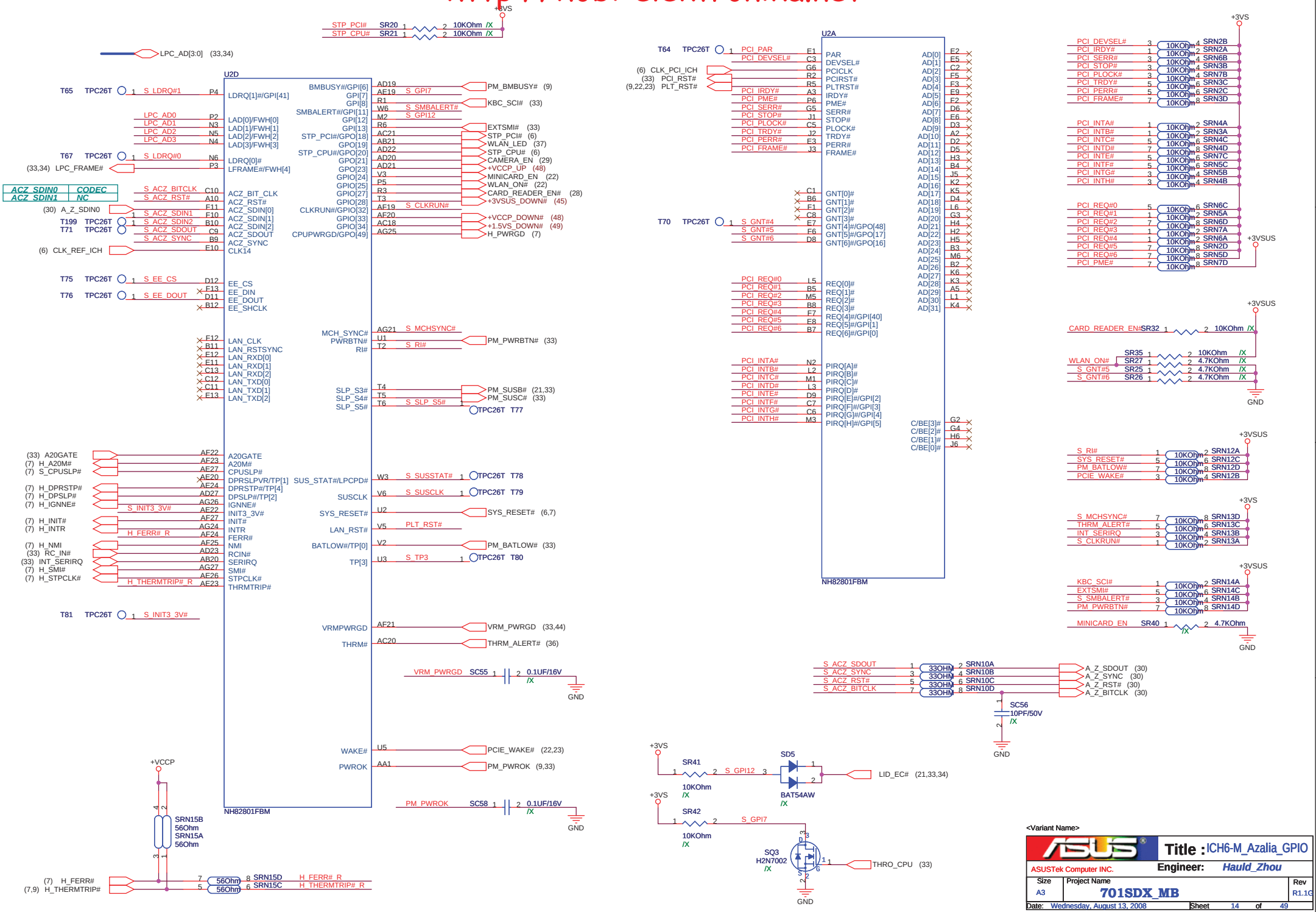
ASUSTek Computer INC.	Title : 910GML_PWR	
	Engineer: Kell_Huang	
Size: A3	Project Name: 701SDX_MB	Rev: R1.1G
Date: Wednesday, August 13, 2008	Sheet 12 of 49	

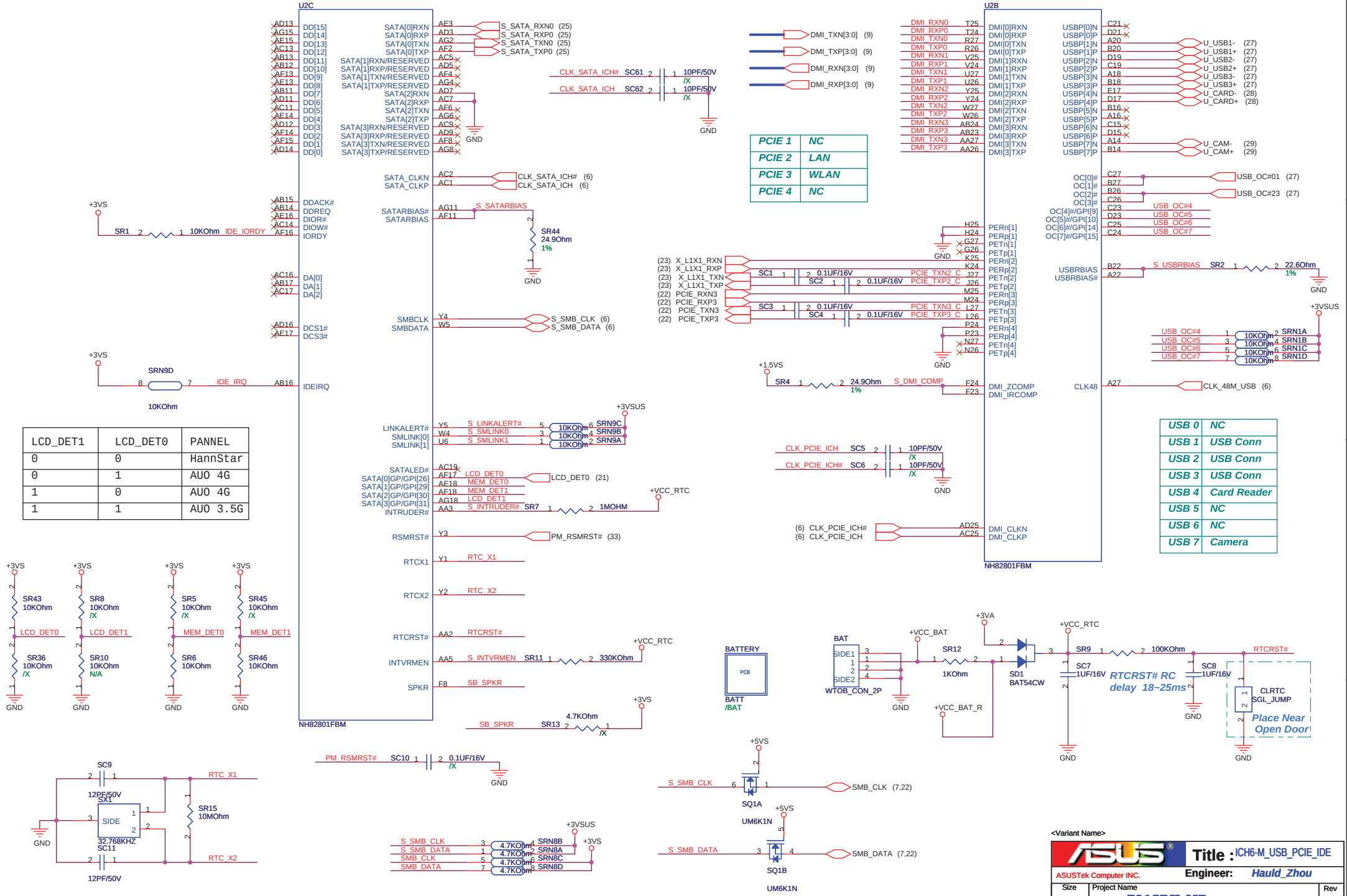


U1 use 02G010007610

<Variant Name>

ASUSTek Computer INC.	Title : 910GML_GND	
	Engineer: Kell_Huang	
Size: A3	Project Name: 701SDX_MB	Rev: R1.1G
Date: Wednesday, August 13, 2008	Sheet 13 of 49	

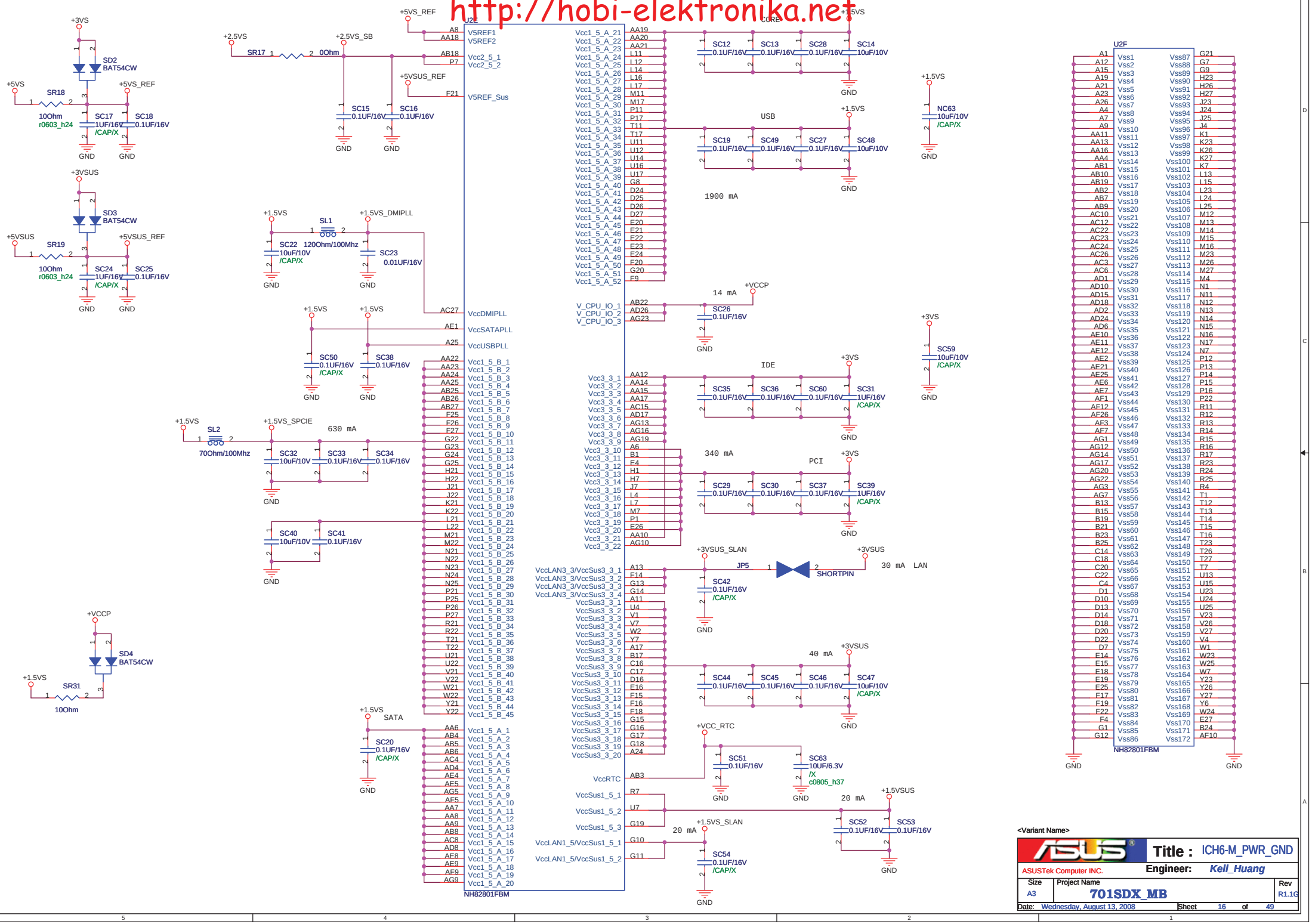




LCD_DET1	LCD_DET0	PANNEL
0	0	HannStar
0	1	AUO 4G
1	0	AUO 4G
1	1	AUO 3.5G

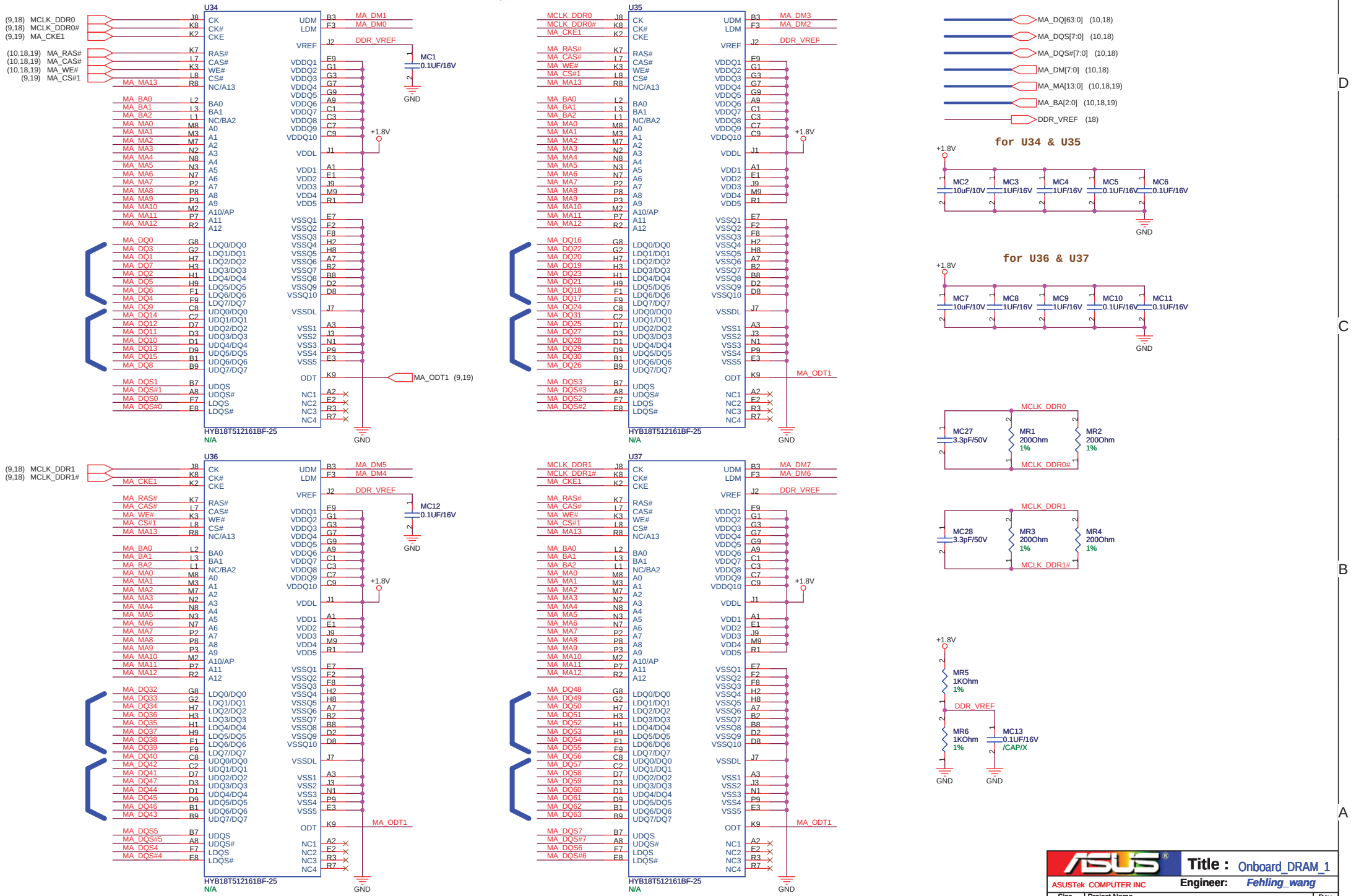
<variant_name>

ASUSTek Computer INC.	Title : ICH6-M_USB_PCIE_IDE		
	Engineer: Hauld_Zhou		
Size: A3	Project Name: 701SDX_MB		Rev: R1.1G
Date: Wednesday, August 13, 2008	Sheet 15 of 49		

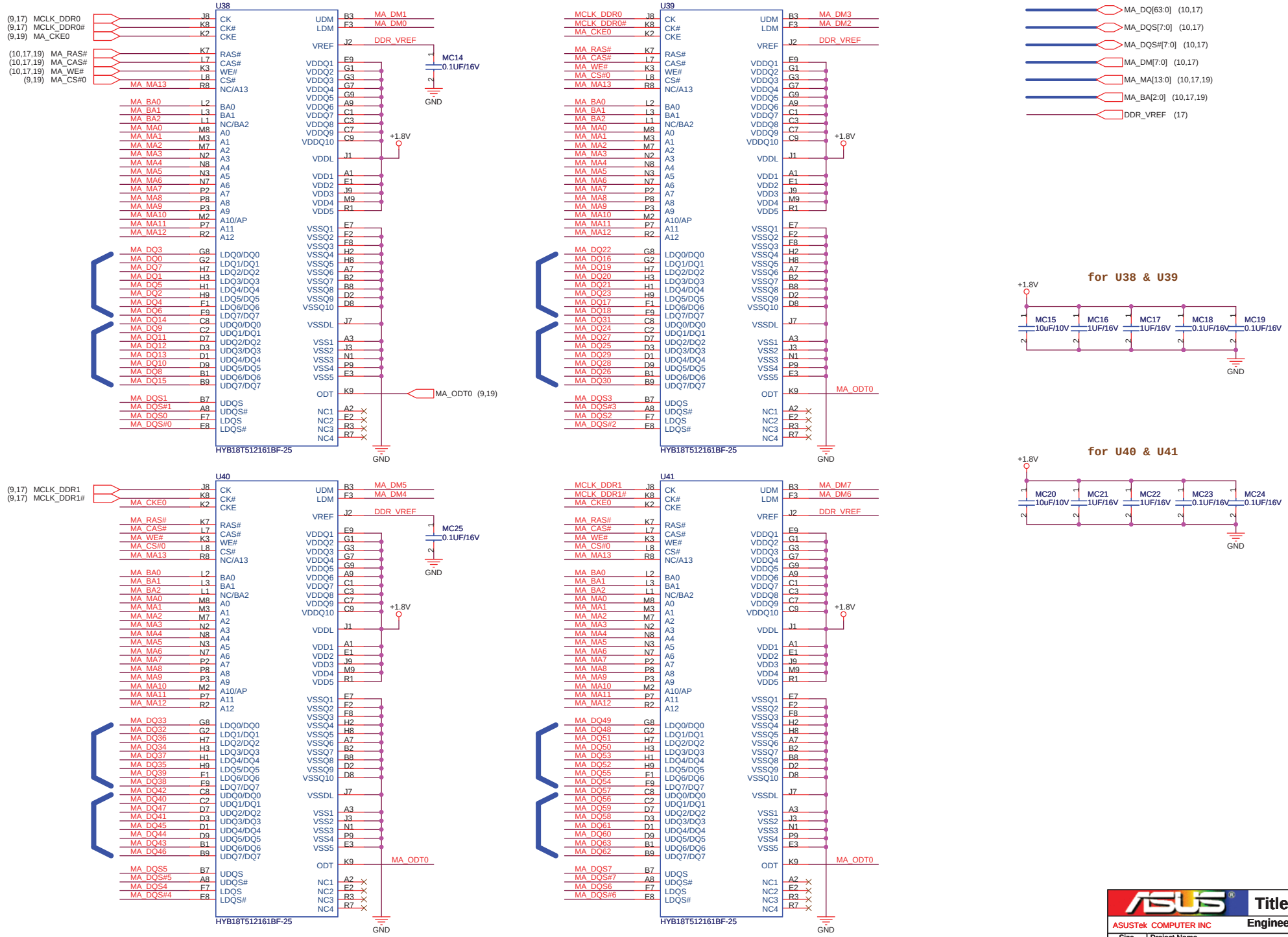


<Variant Name>

ASUSTek Computer INC.	Title : ICH6-M_PWR_GND	
	Engineer: Kell_Huang	
Size: A3	Project Name: 701SDX_MB	Rev: R1.1G
Date: Wednesday, August 13, 2008	Sheet 16 of 49	



ASUSTek COMPUTER INC	Title : Onboard_DRAM_1		
	Engineer: Fehling_wang		
Size: A3	Project Name: 701SDX_MB		Rev: R1.1G
Date: Wednesday, August 13, 2008	Sheet 17 of 49		

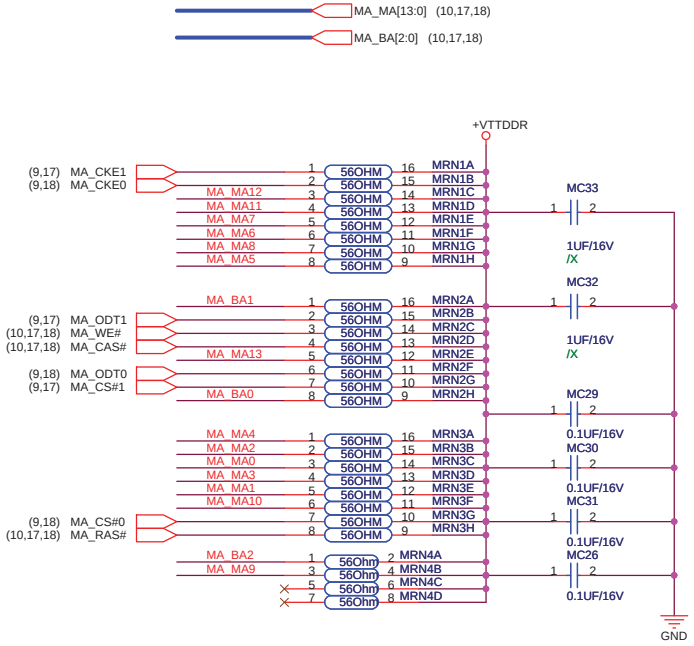


MA_DQ[63:0] (10,17)
MA_DQS[7:0] (10,17)
MA_DQS#[7:0] (10,17)
MA_DM[7:0] (10,17)
MA_MA[13:0] (10,17,19)
MA_BA[2:0] (10,17,19)
DDR_VREF (17)

for U38 & U39

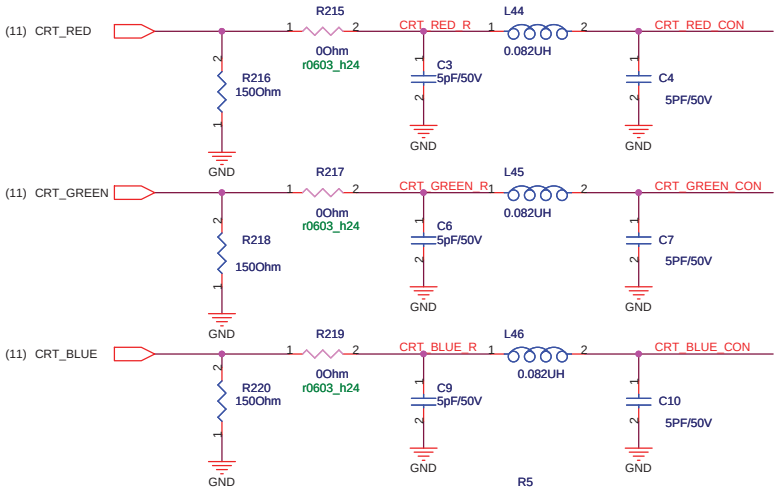
for U40 & U41

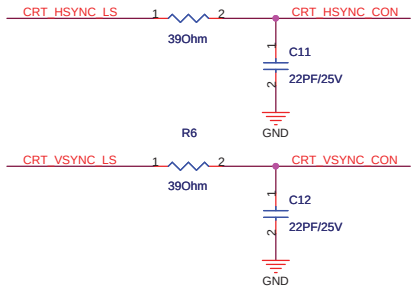
ASUSTek COMPUTER INC	Title : Onboard_DRAM_2		
	Engineer: Fehling_wang		
Size: A3	Project Name: 701SDX_MB		Rev: R1.1G
Date: Wednesday, August 13, 2008	Sheet 18 of 49		

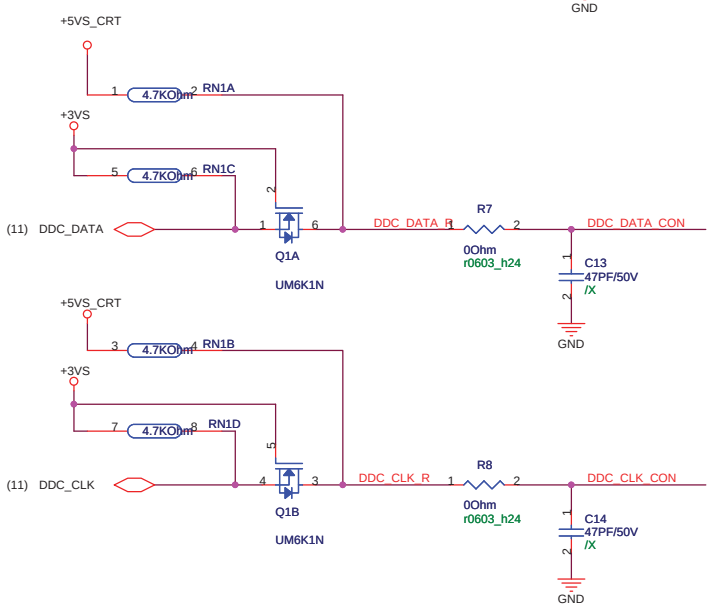


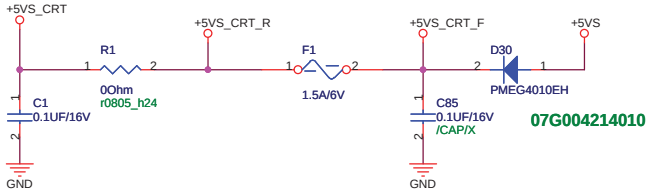
<Variant Name>

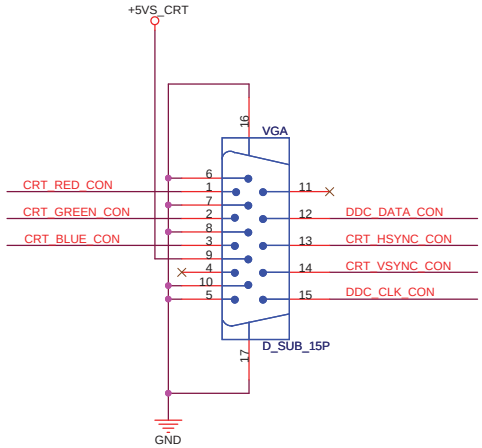
ASUSTek Computer INC.	Title : DDR2_Termination	
	Engineer: Kell_Huang	
Size: A3	Project Name: 701SDX_MB	Rev: R1.1G
Date: Wednesday, August 13, 2008	Sheet 19 of 49	



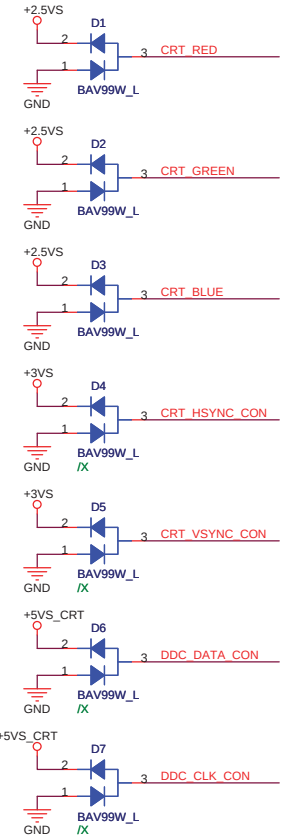


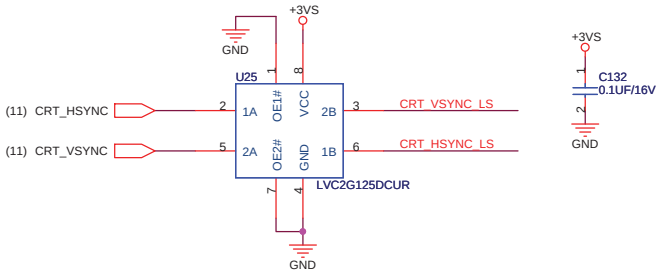






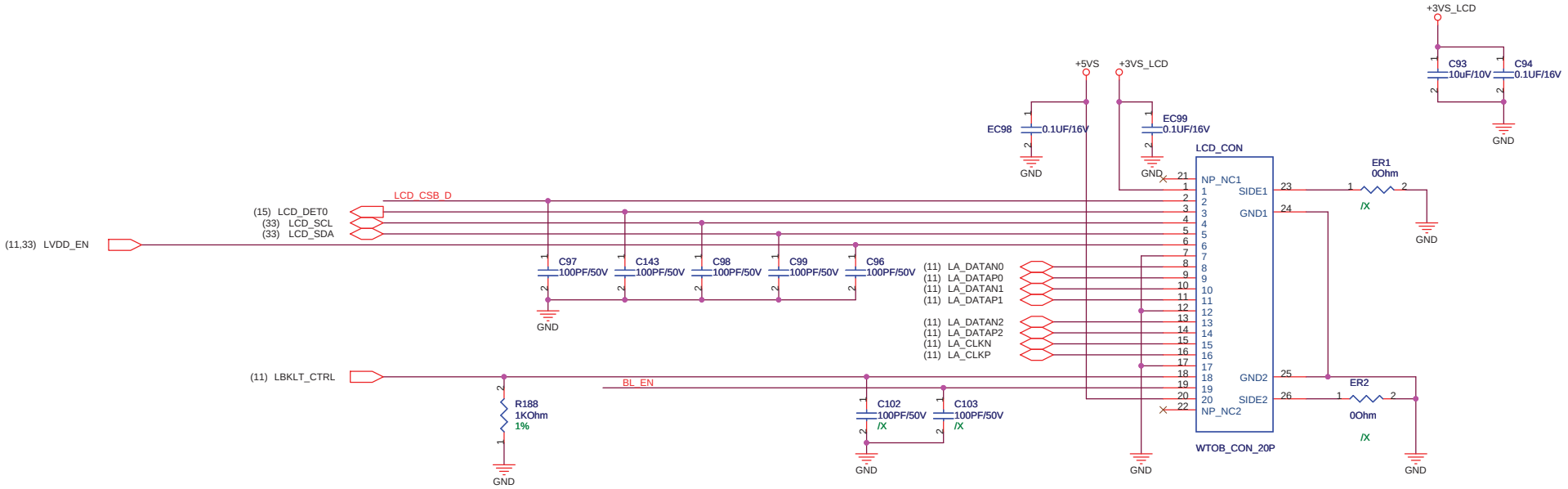
VGA use 12G10110015W or 12G10110015N

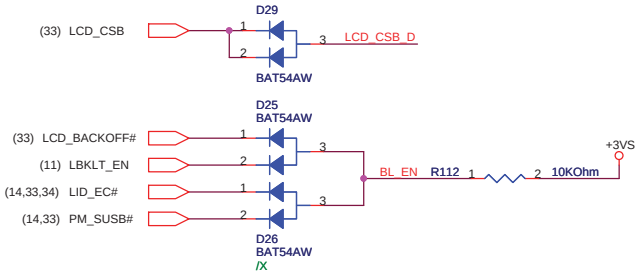


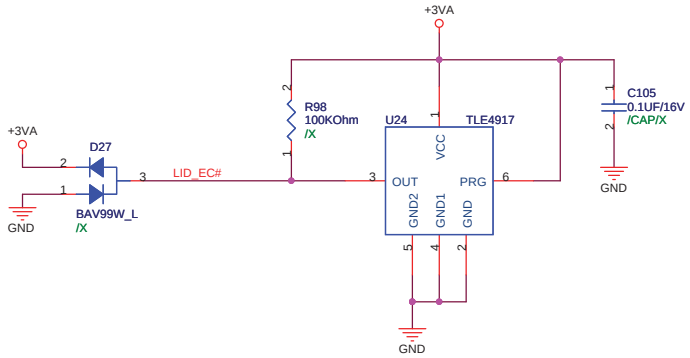


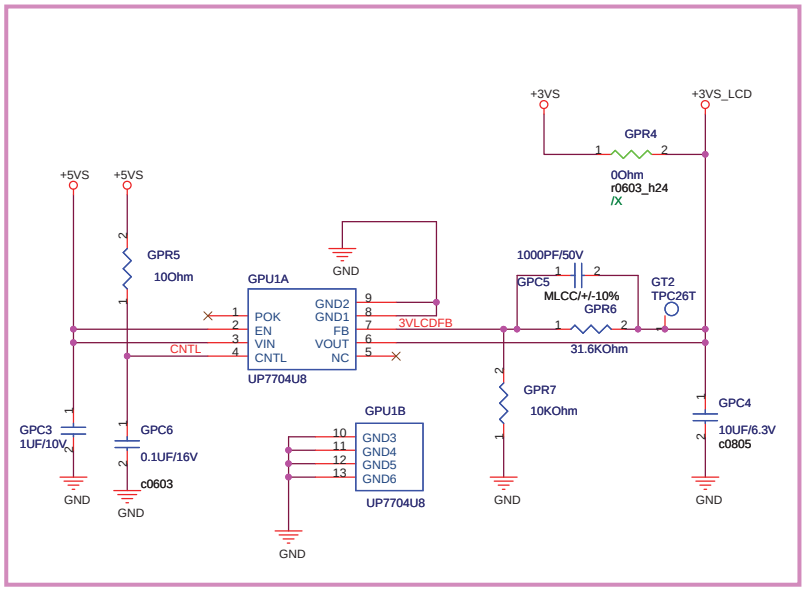
<Variant Name>

ASUSTek Computer INC.	Title : Onboard VGA	
	Engineer: Kell_Huang	
Size: A3	Project Name: 701SDX_MB	Rev: R1.1G
Date: Wednesday, August 13, 2008	Sheet 20 of 49	



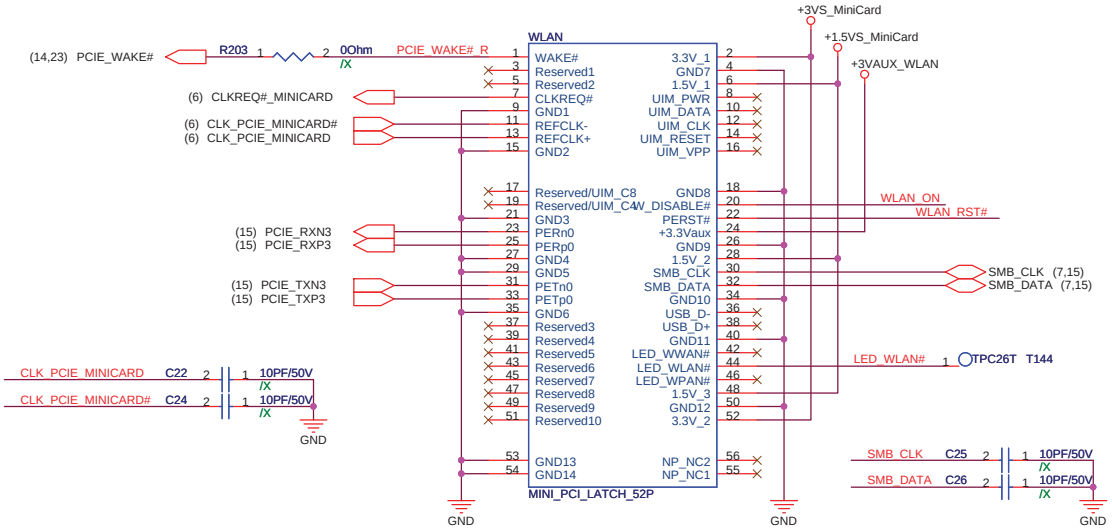


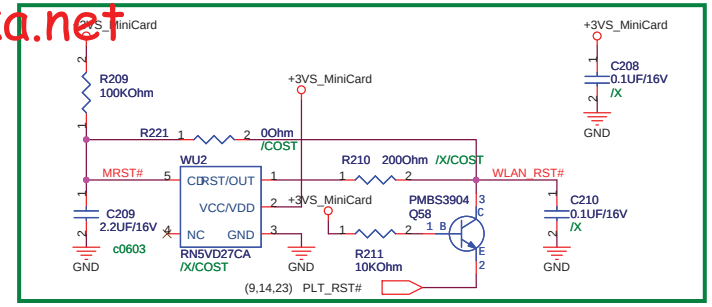


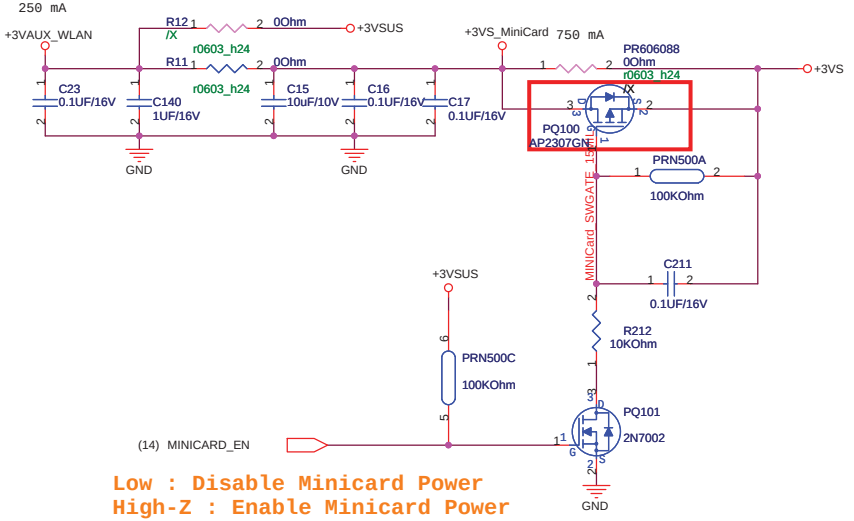


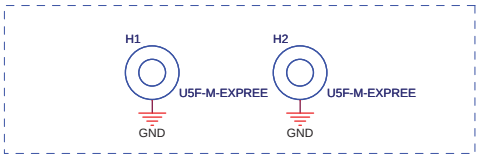
<Variant Name>

ASUSTek Computer INC.	Title : LCD Conn	
	Engineer: Kell_Huang	
Size: A3	Project Name: 701SDX_MB	Rev: R1.1G
Date: Wednesday, August 13, 2008	Sheet 21 of 49	

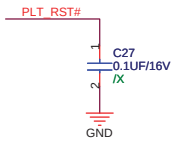


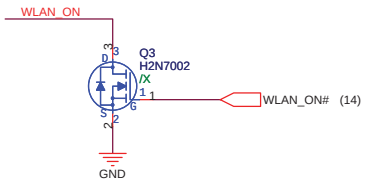


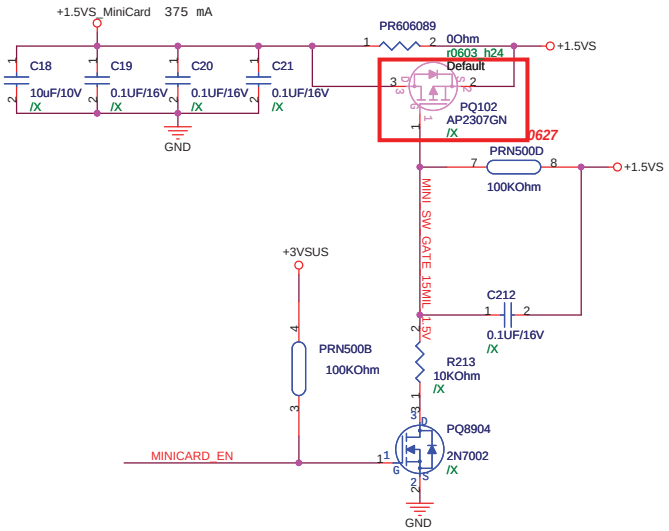




MINI CARD NUT(1.6mm) *2

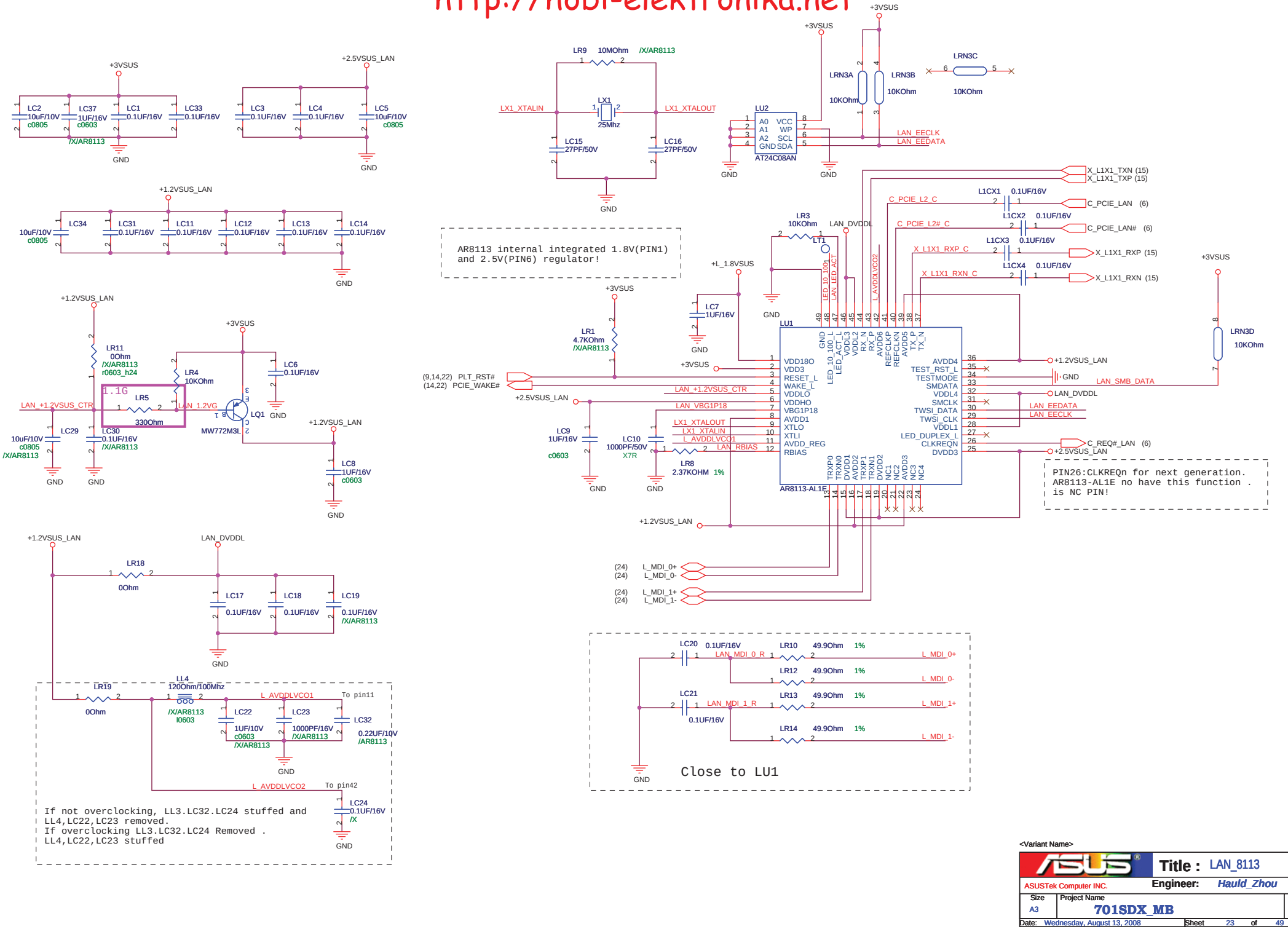






<Variant Name>

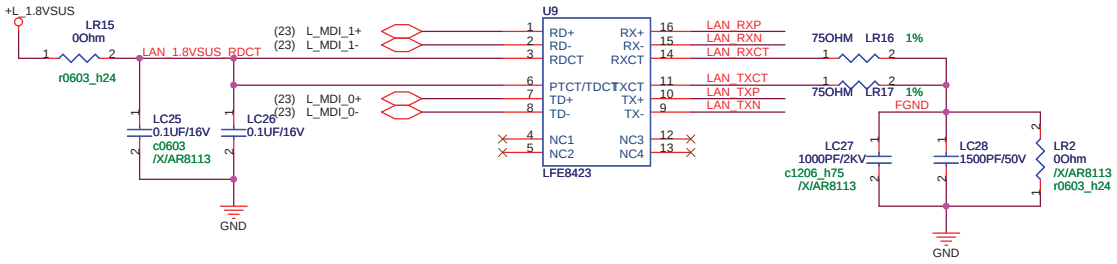
ASUSTek Computer INC.	Title : WLAN	
	Engineer: Kell_Huang	
Size: A3	Project Name: 701SDX_MB	Rev: R1.1G
Date: Wednesday, August 13, 2008	Sheet 22 of 49	

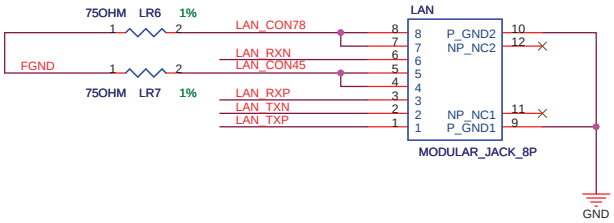


<Variant Name>

ASUSTek Computer INC.	Title : LAN_8113	
	Engineer: Hauld_Zhou	
Size: A3	Project Name: 701SDX_MB	Rev: R1.1G
Date: Wednesday, August 13, 2008	Sheet 23 of 49	

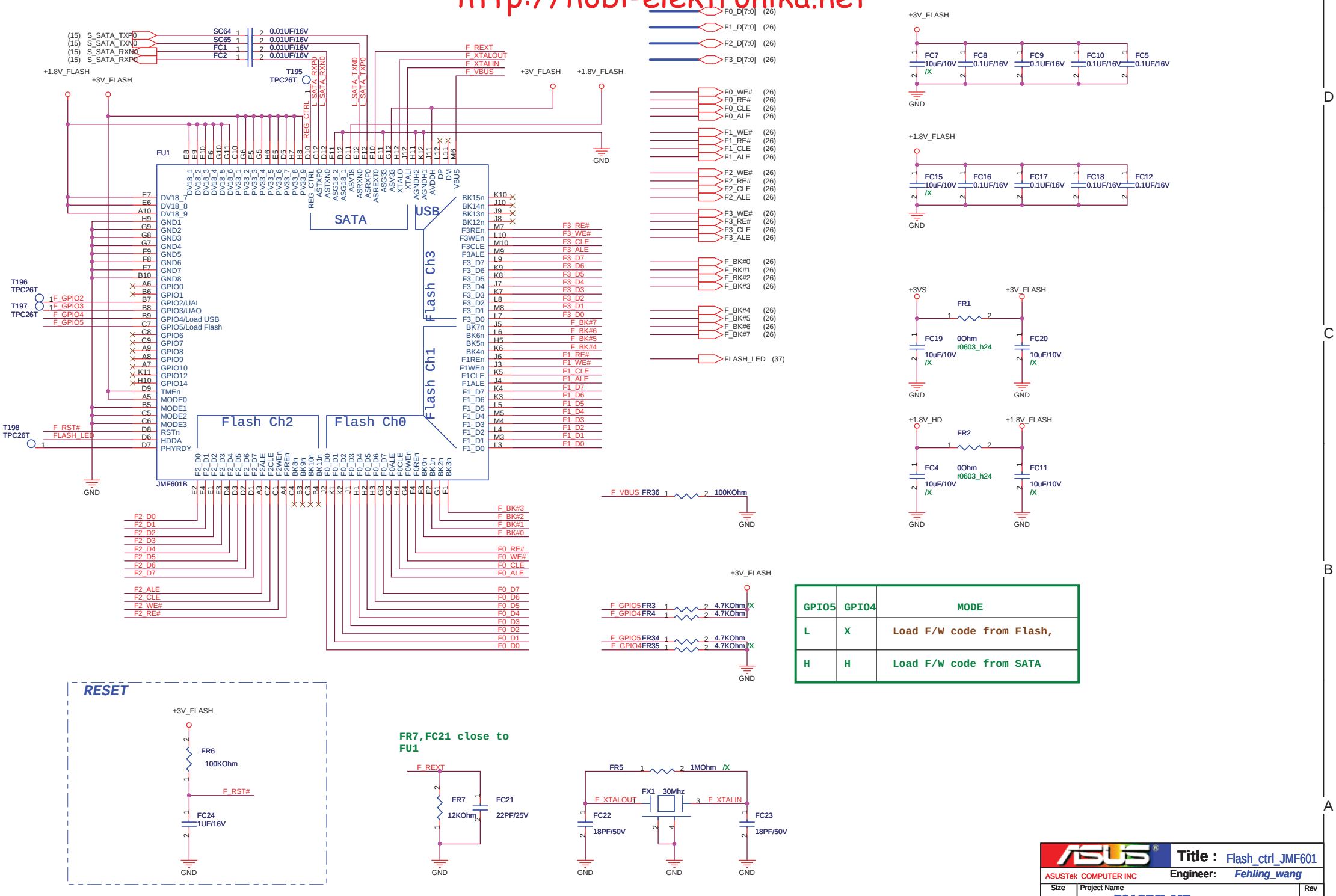
DELETE MODEM





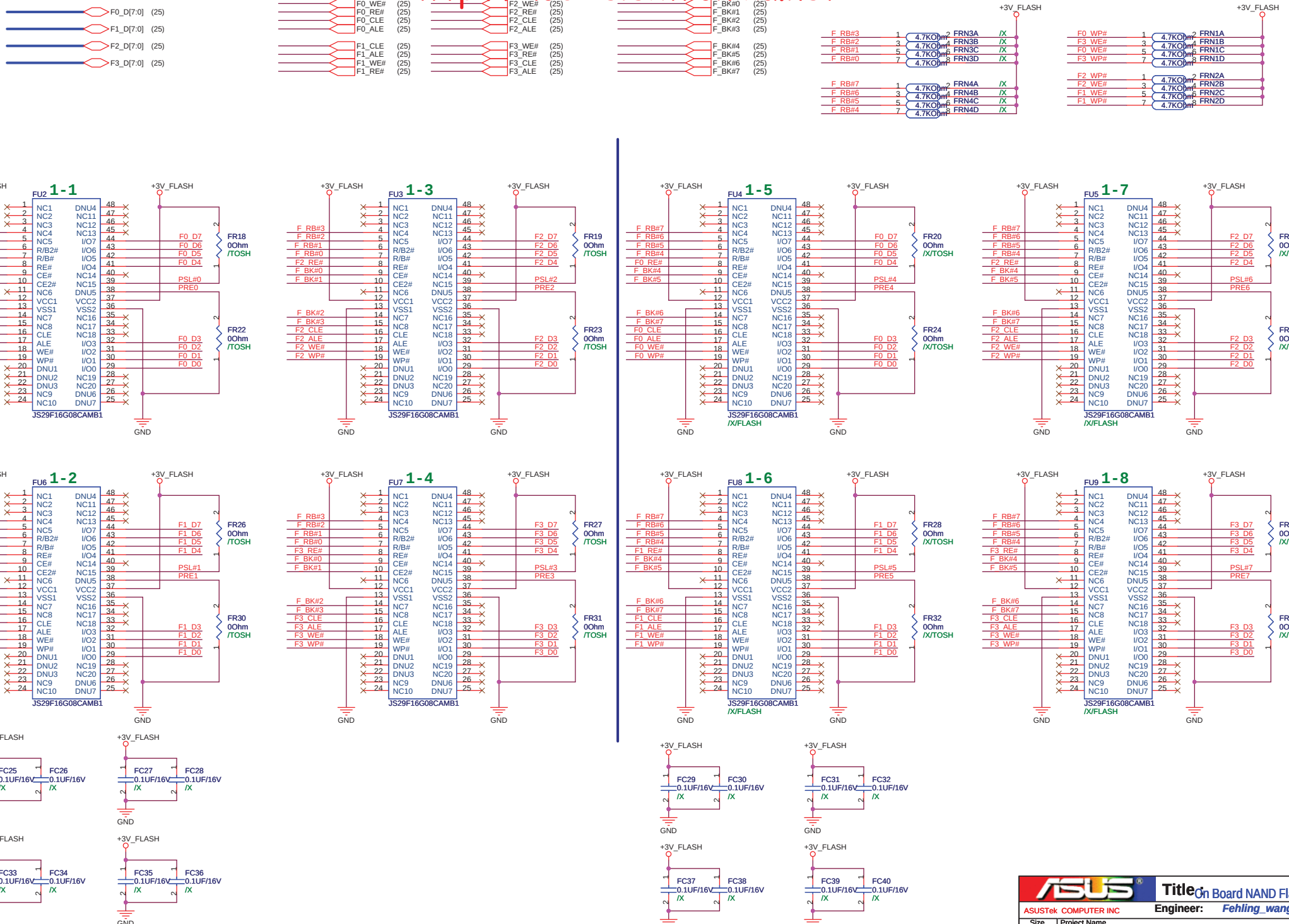
<Variant Name>

ASUSTek Computer INC.	Title : RJ45	
	Engineer: Hauld_Zhou	
Size: A3	Project Name: 701SDX_MB	Rev: R1.1G
Date: Wednesday, August 13, 2008	Sheet 24 of 49	

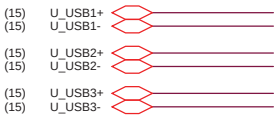


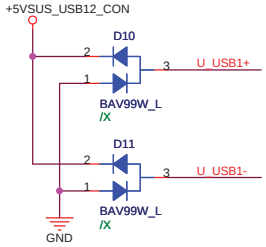
GPIO5	GPIO4	MODE
L	X	Load F/W code from Flash,
H	H	Load F/W code from SATA

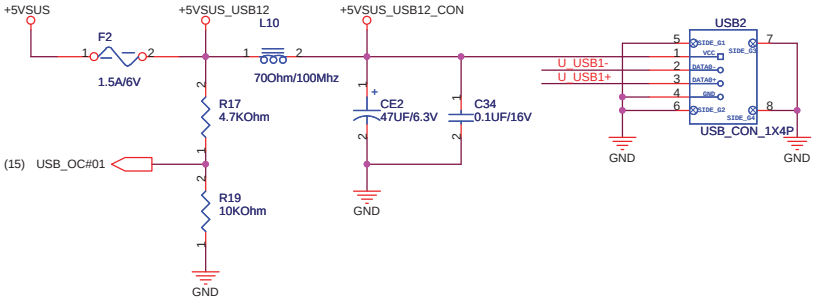
ASUSTek COMPUTER INC	Title :	Flash_ctrl_JMF601
	Engineer:	Fehling_wang
Size: A3	Project Name: 701SDX_MB	Rev: R1.1G
Date: Wednesday, August 13, 2008	Sheet 25 of 49	

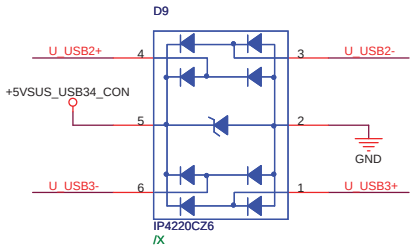


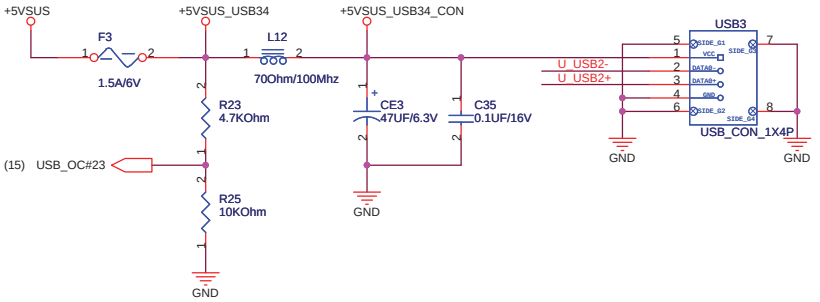
Title:	On Board NAND Flash	
ASUSTek COMPUTER INC	Engineer:	Fehling_wang
Size: A3	Project Name: 701SDX_MB	Rev: R1.1G
Date: Wednesday, August 13, 2008	Sheet 26 of 49	

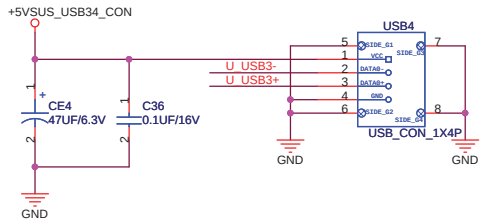






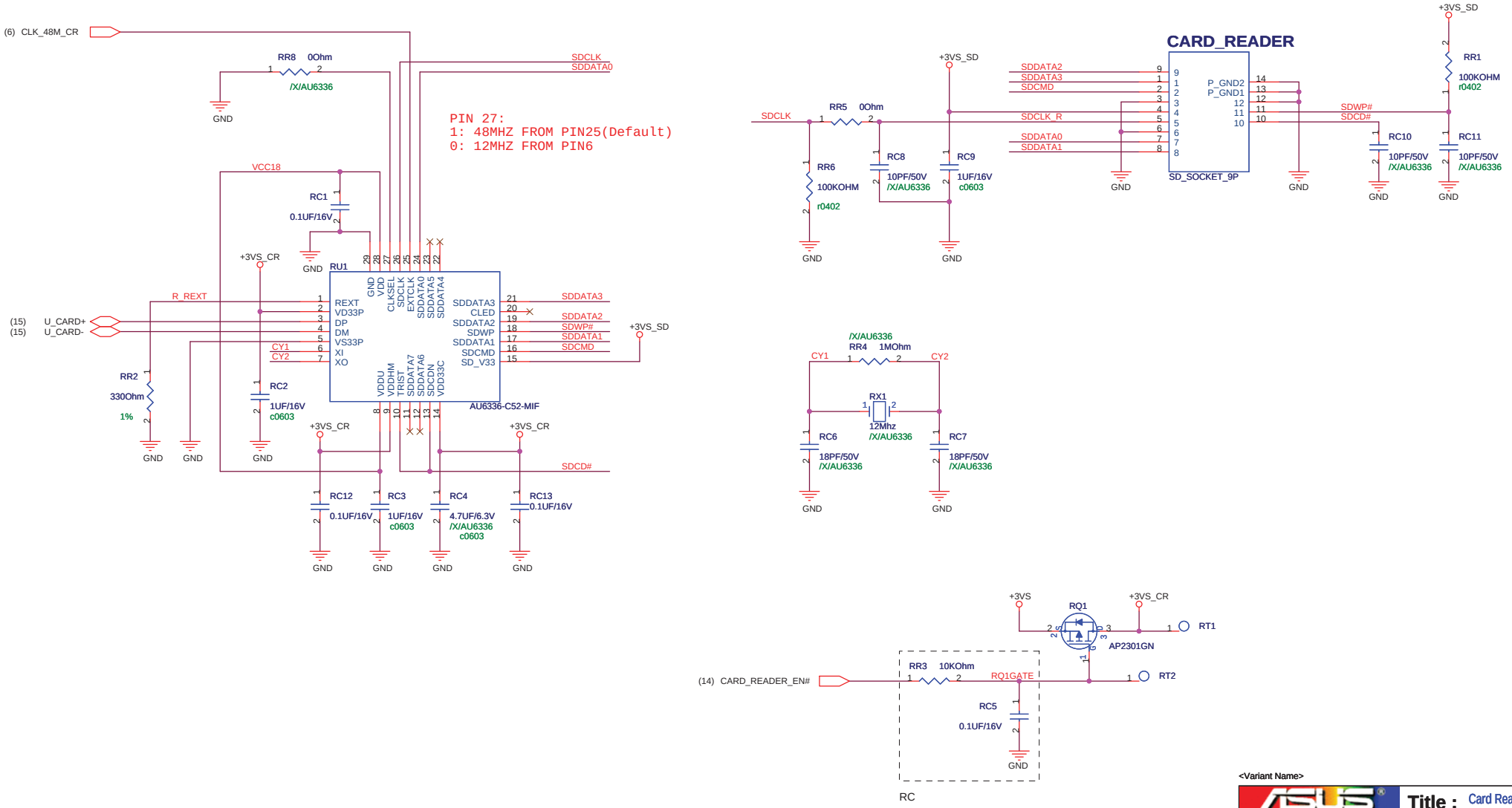






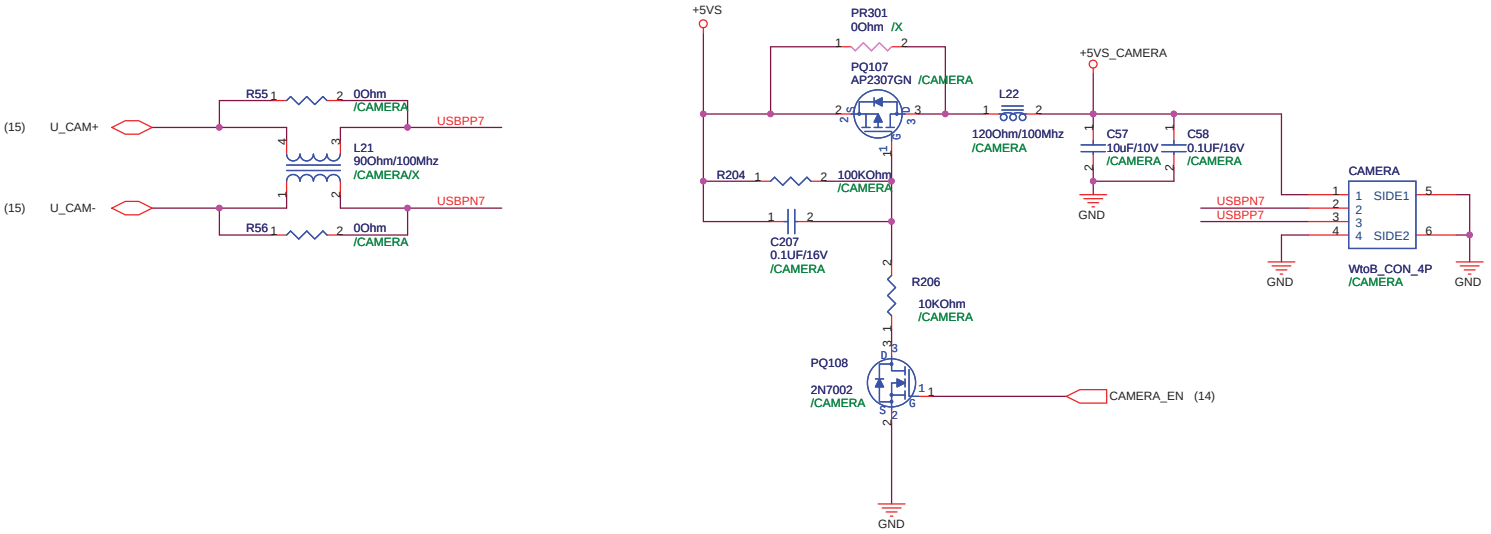
<Variant Name>

ASUSTek Computer INC.	Title : USB Port	
	Engineer: Kell_Huang	
Size: A3	Project Name: 701SDX_MB	Rev: R1.1G
Date: Wednesday, August 13, 2008	Sheet 27 of 49	



<Variant Name>

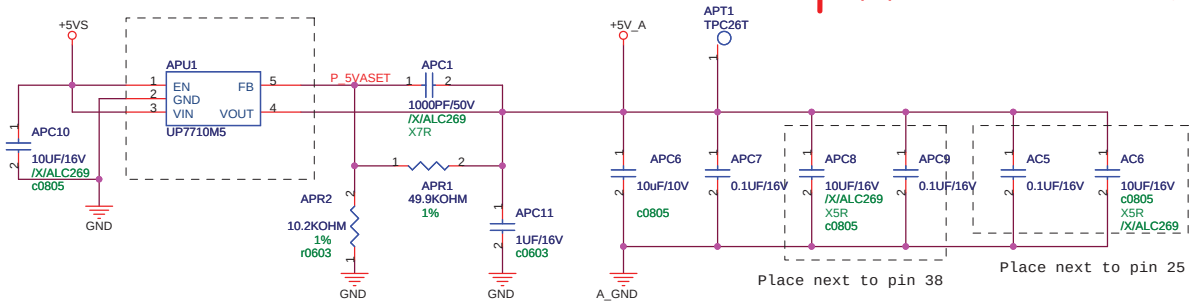
ASUSTek Computer INC.	Title : Card Reader_AU6336	
	Engineer: Hauld_Zhou	
Size: A3	Project Name: 701SDX_MB	Rev: R1.1G
Date: Wednesday, August 13, 2008	Sheet 28 of 49	

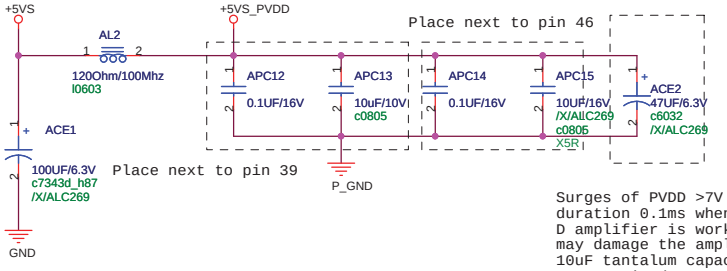


<Variant Name>

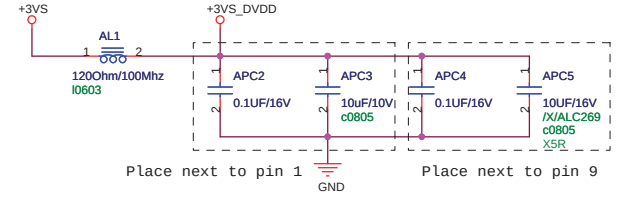
ASUSTek Computer INC.	Title : Camera Conn	
	Engineer: Kell_Huang	
Size: A3	Project Name: 701SDX_MB	Rev: R1.1G
Date: Wednesday, August 13, 2008	Sheet 29 of 49	

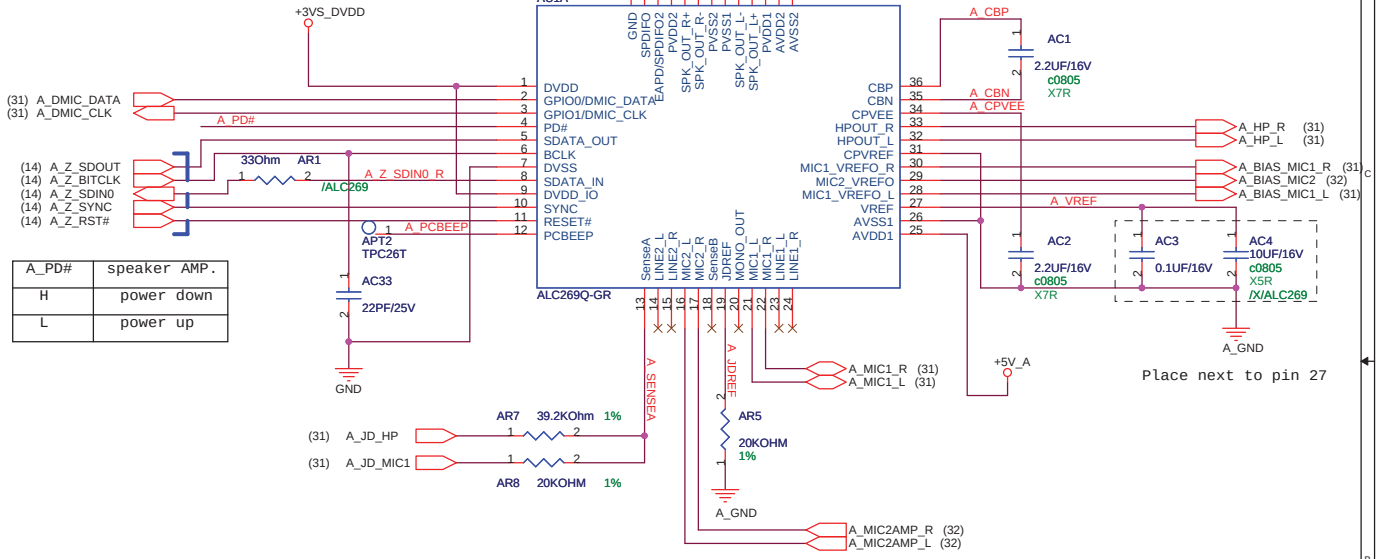
Vout=0.8*(1+(49.9K/10.2K))



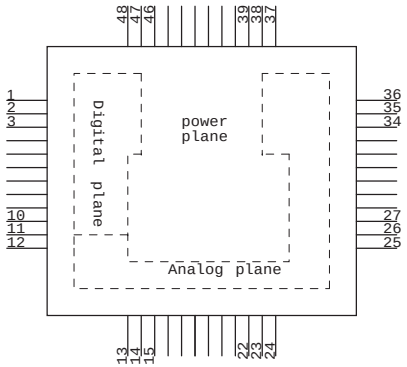


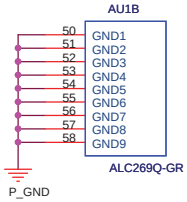
Surges of PVDD >7V duration 0.1ms when class D amplifier is working may damage the amplifier, 10uF tantalum capacitors are required at PVDD1 and PVDD2 to uppress the surge.





A_PD#	speaker AMP.
H	power down
L	power up



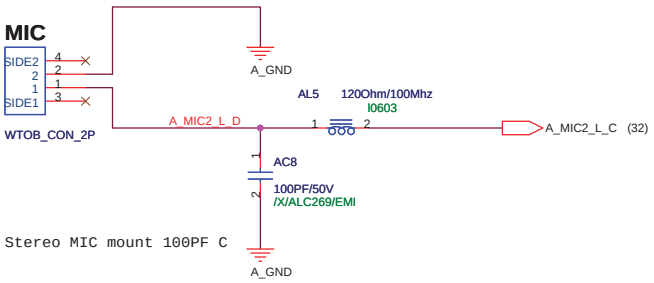


<Variant Name>

ASUSTek Computer INC.	Title : ALC269-1	
	Engineer: Jeff_Li	
Size: A3	Project Name: 701SDX_MB	Rev: R1.1G
Date: Wednesday, August 13, 2008	Sheet 30 of 49	

MIC1

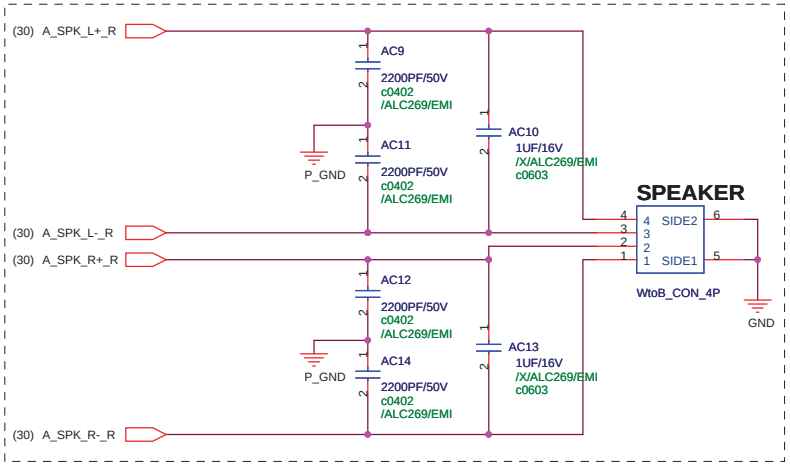
Internal MIC



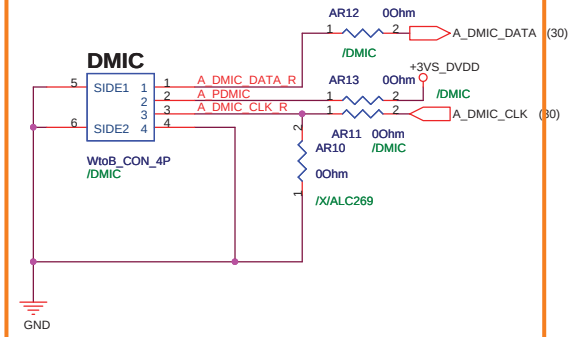
SPEAKER

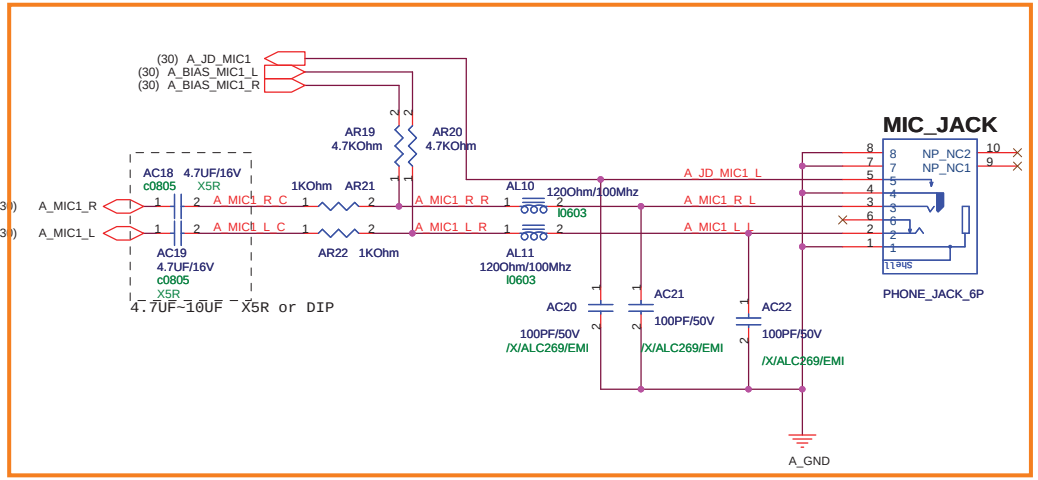
<<Attention>>
you can use LC filter(AR9,AR14,AR15,AR16 mount 8.2uH L ;and mount AC10,AC13) to eliminate the EMI(please don't use general beads,because they may influence the THD+N quality) , AC9/AC11/AC12/AC14 are used for EMI fine-tune ; For EMI issue, All L and C should near to codec

Demodulation Filter
Placement near
Audio Codec

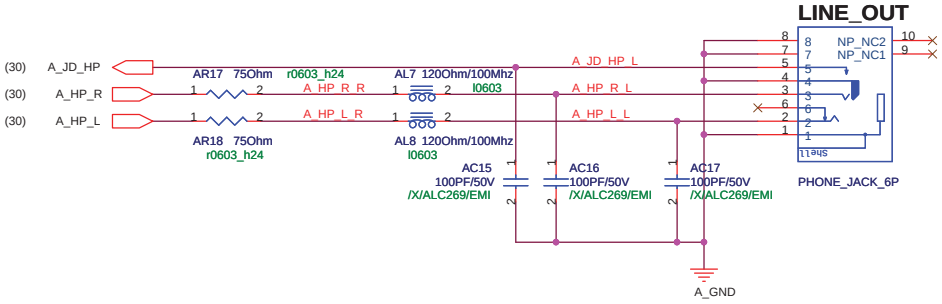


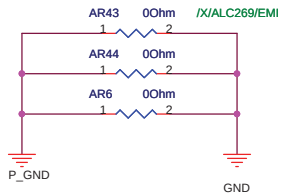
Digital Mic Interface

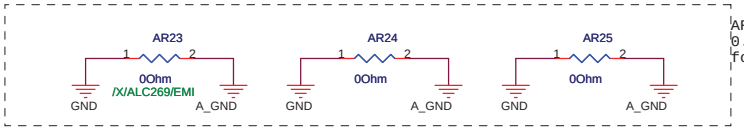




HP



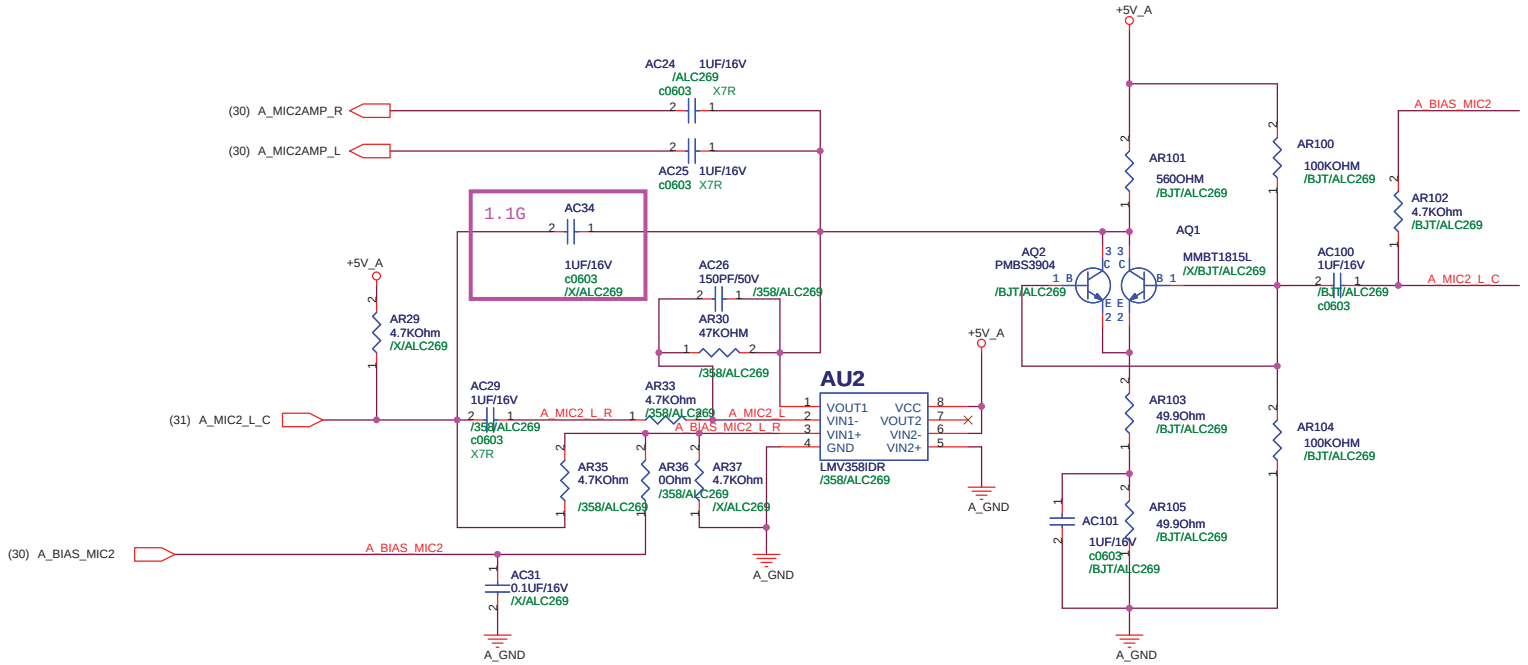




AR24, AR25 can use 0.1UF 11G233310432320 for EMI

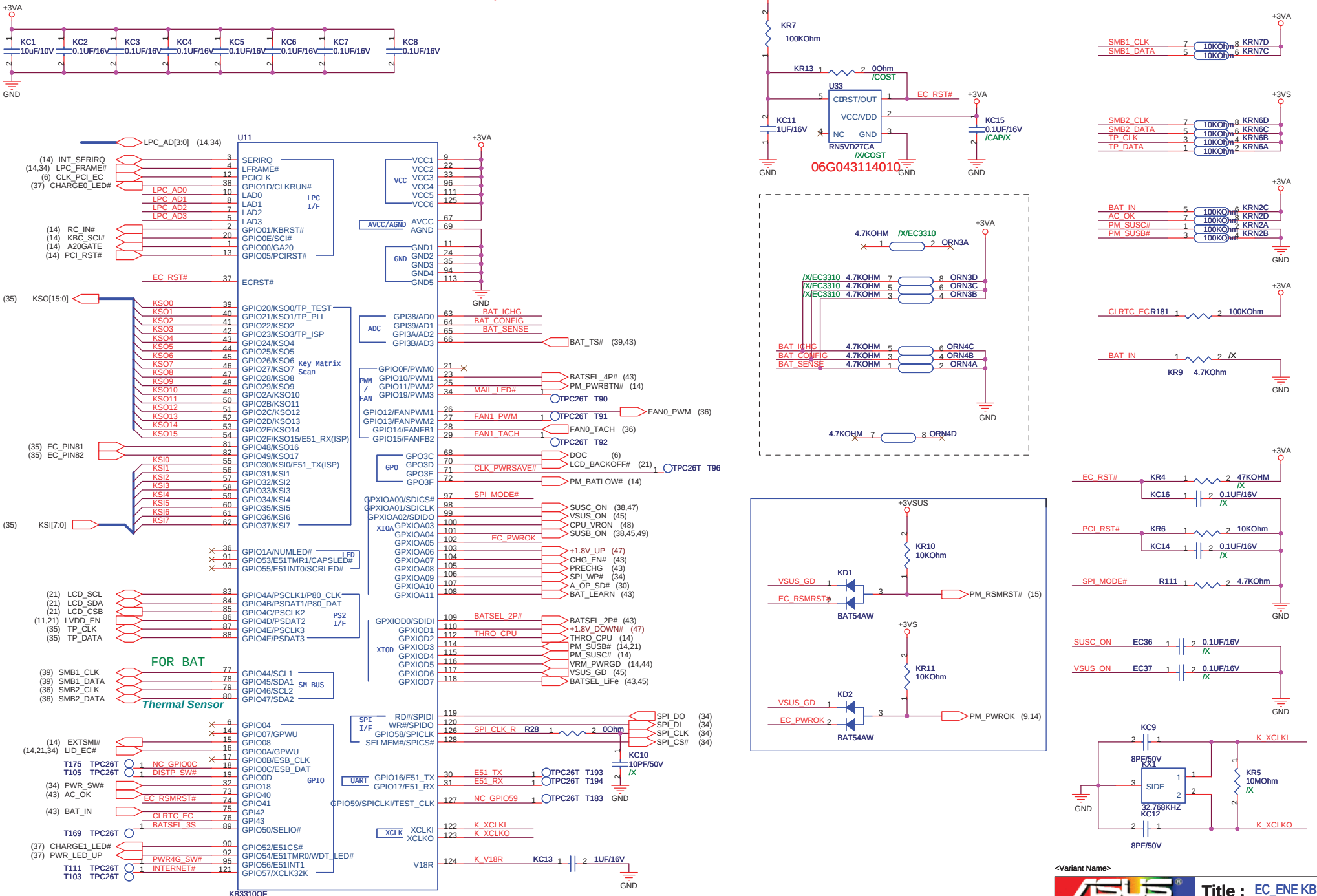
<Variant Name>

ASUSTek Computer INC.	Title : ALC269-2(IO)	
	Engineer: Jeff_Li	
Size: A3	Project Name: 701SDX_MB	Rev: R1.1G
Date: Wednesday, August 13, 2008	Sheet 31 of 49	



<Variant Name>

ASUSTek Computer INC.	Title : ALC269-3(MIC AMP)	
	Engineer: Jeff_Li	
Size: A3	Project Name: 701SDX_MB	Rev: R1.1G
Date: Wednesday, August 13, 2008	Sheet 32 of 49	



<Variant Name>

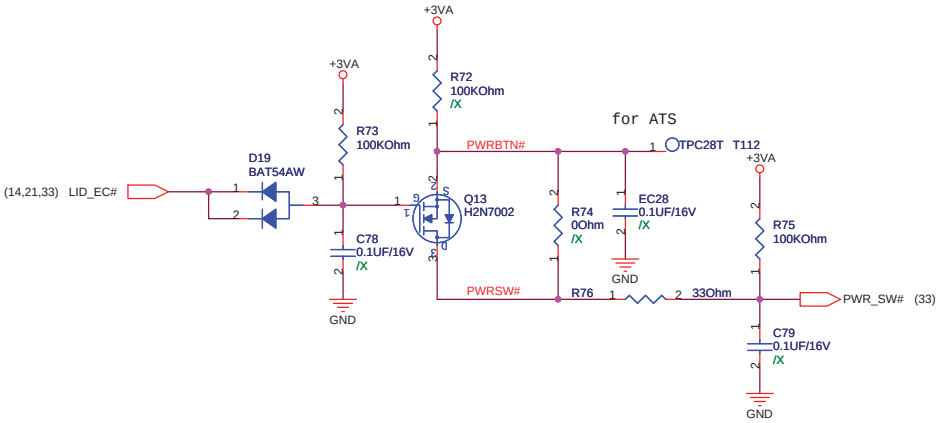
ASUSTek Computer INC.

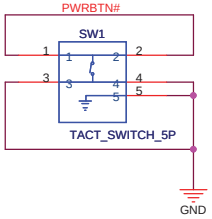
Title : EC_ENE KB3310

Engineer: Kell_Huang

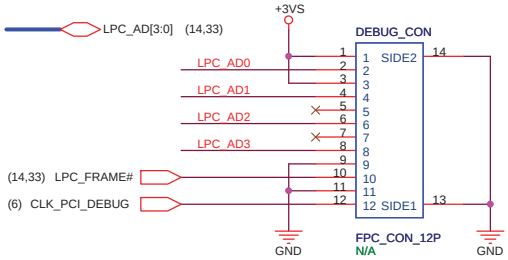
Size	Project Name	Rev
A3	701SDX_MB	R1.1G

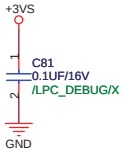
Date: Wednesday, August 13, 2008 Sheet 33 of 49

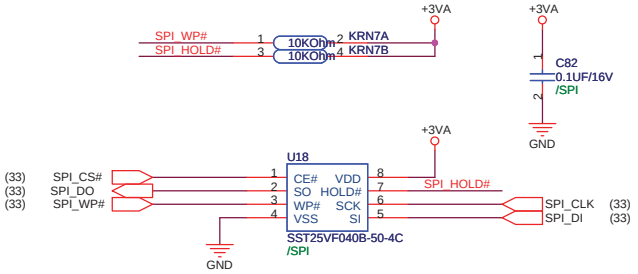




For Debug



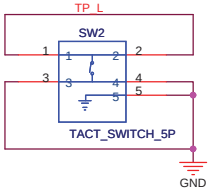


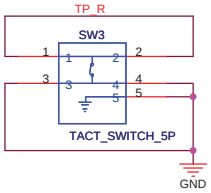


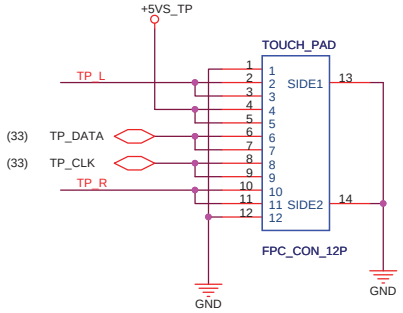
<Variant Name>

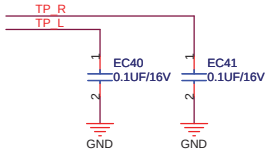
ASUSTek Computer INC.	Title : Switch_SPI ROM	
	Engineer: Kell_Huang	
Size: A3	Project Name: 701SDX_MB	Rev: R1.1G
Date: Wednesday, August 13, 2008	Sheet 34 of 49	

For Touch-Pad

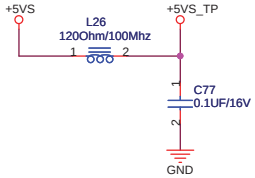


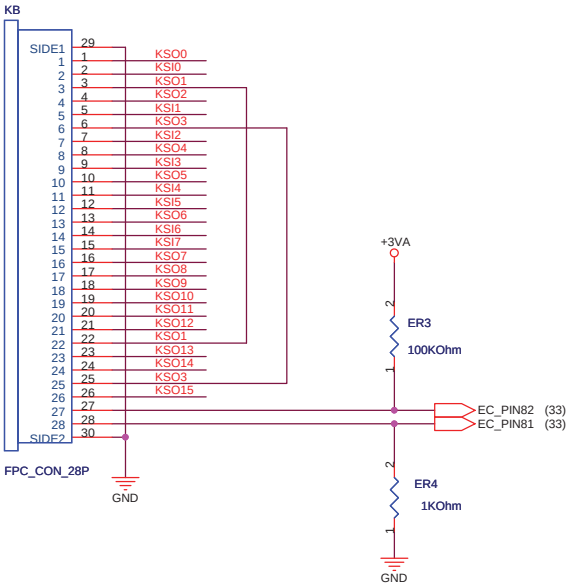


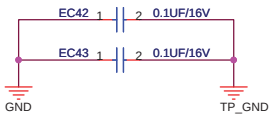


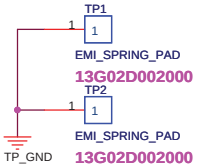


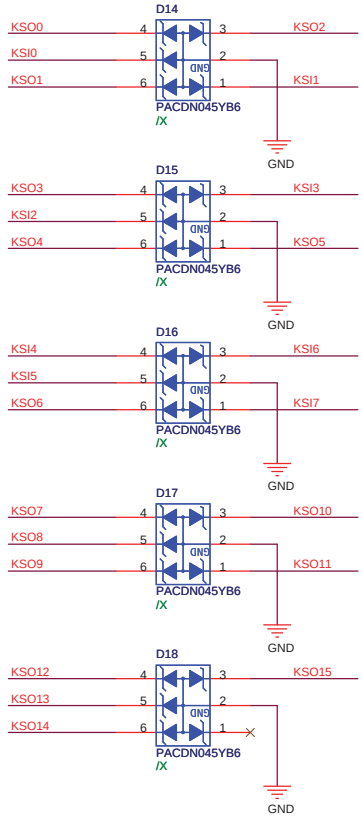
For Keyboard





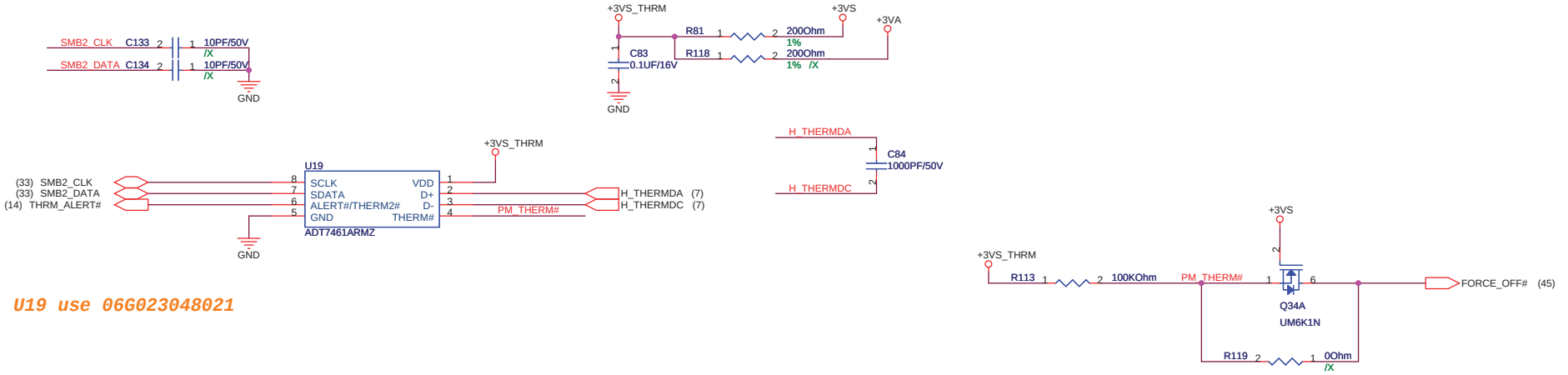




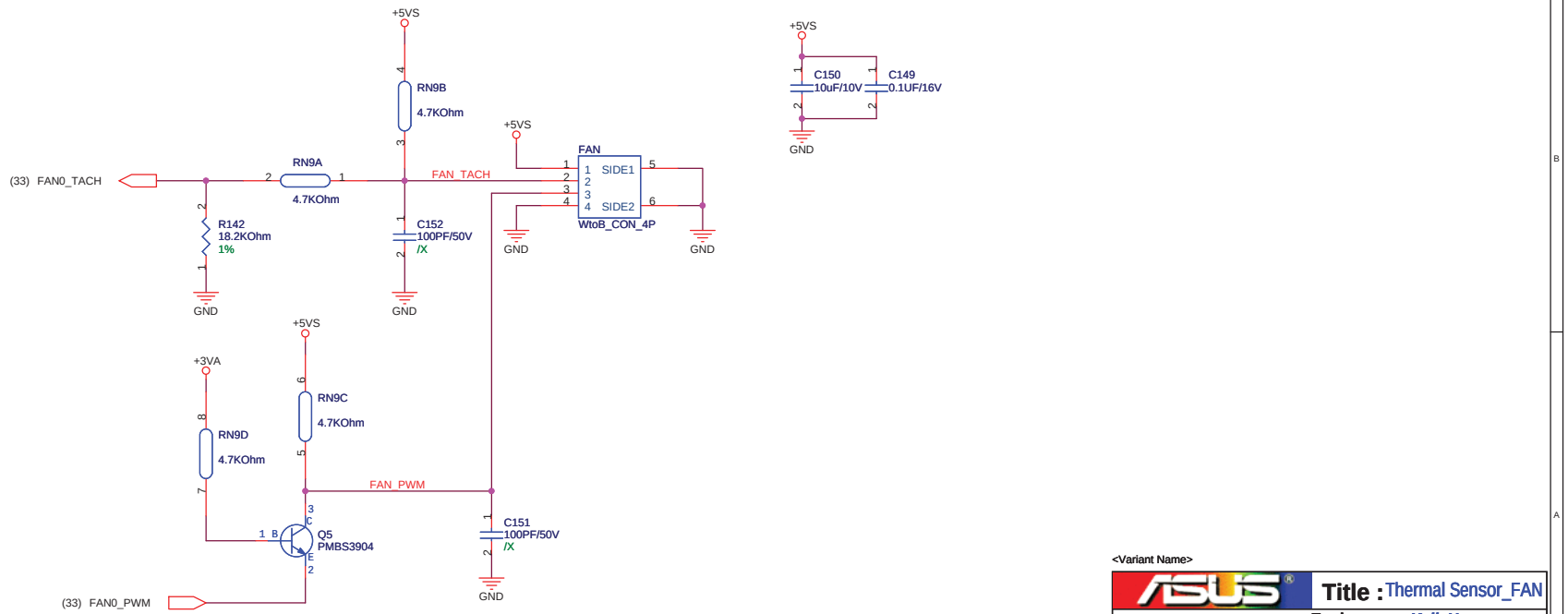


<Variant Name>

ASUSTek Computer INC.	Title : KB_Touch Pad	
	Engineer: Kell_Huang	
Size: A3	Project Name: 701SDX_MB	Rev: R1.1G
Date: Wednesday, August 13, 2008	Sheet 35 of 49	



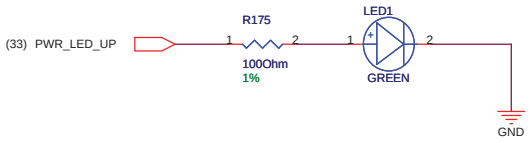
U19 use 06G023048021



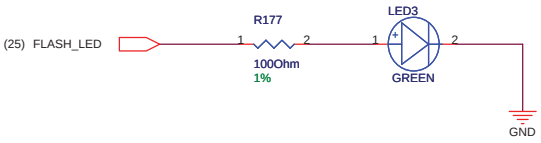
<Variant Name>

ASUSTek Computer INC.	Title : Thermal Sensor_FAN	
	Engineer: Kell_Huang	
Size: A3	Project Name: 701SDX_MB	Rev: R1.1G
Date: Wednesday, August 13, 2008	Sheet 36 of 49	

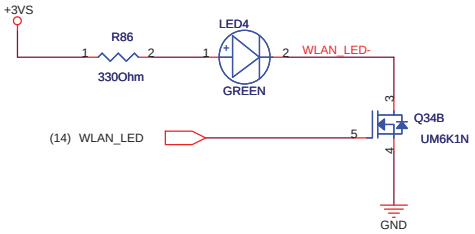
for POWER LED



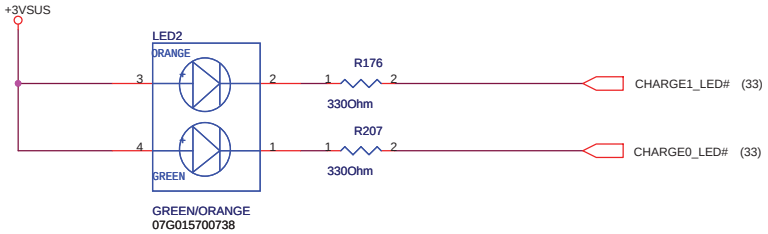
for FLASH LED



for WLAN LED

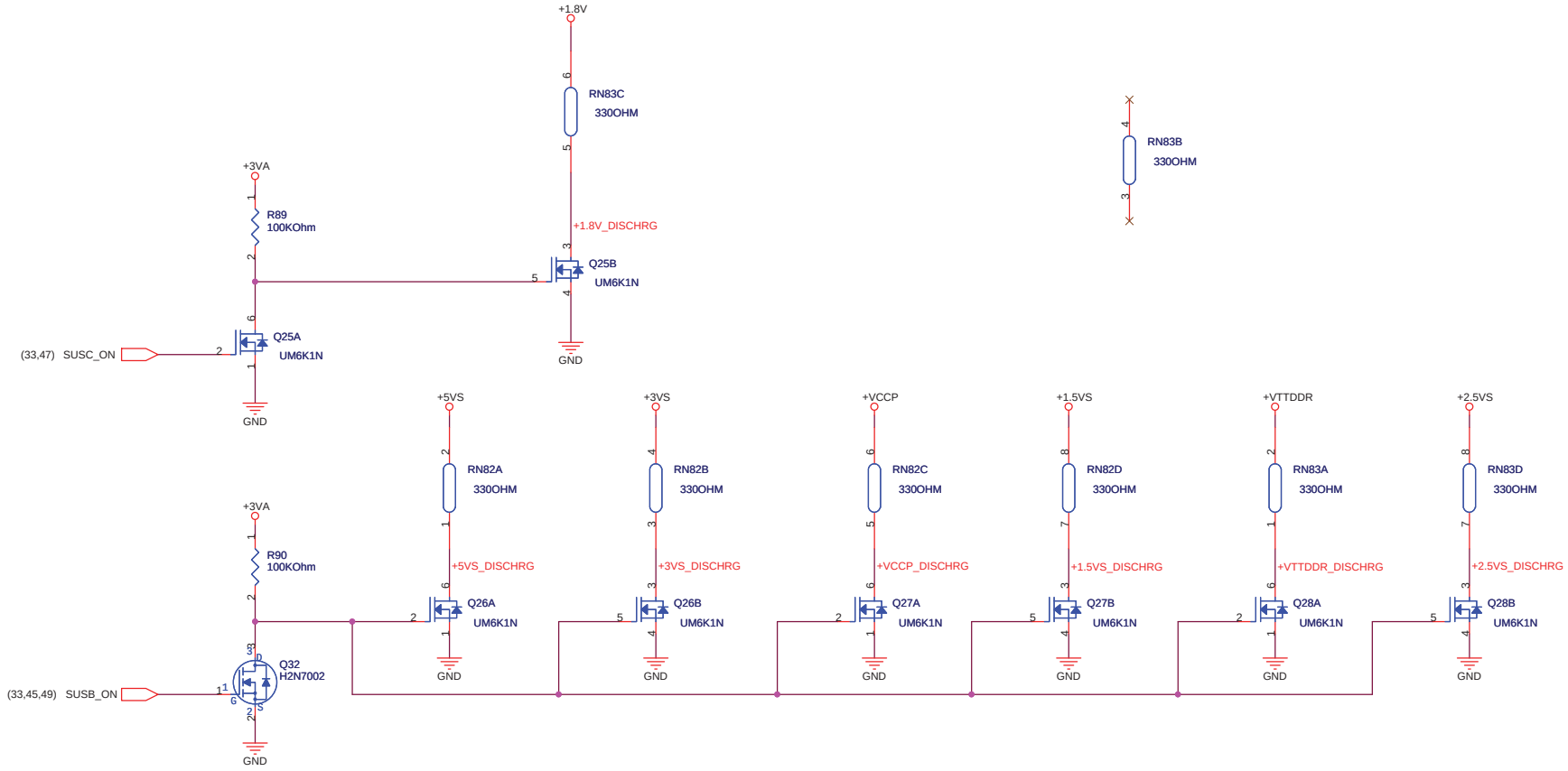


for CHARGE LED



<Variant Name>

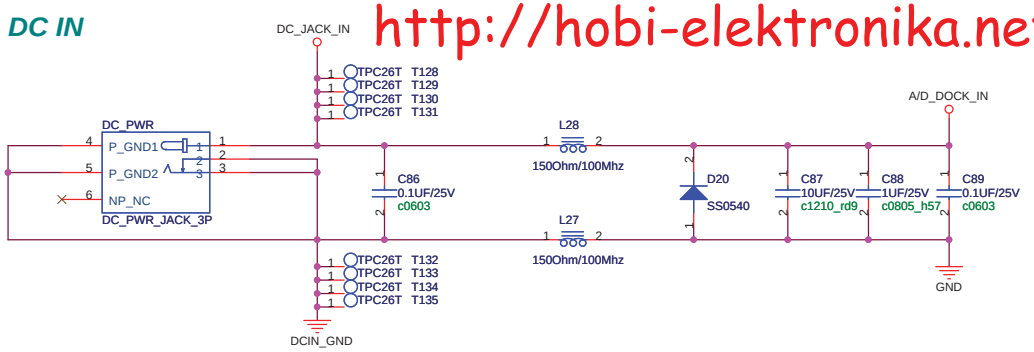
ASUSTek Computer INC.	Title : LED	
	Engineer: Hauld_Zhou	
Size: A3	Project Name: 701SDX_MB	Rev: R1.1G
Date: Wednesday, August 13, 2008	Sheet 37 of 49	



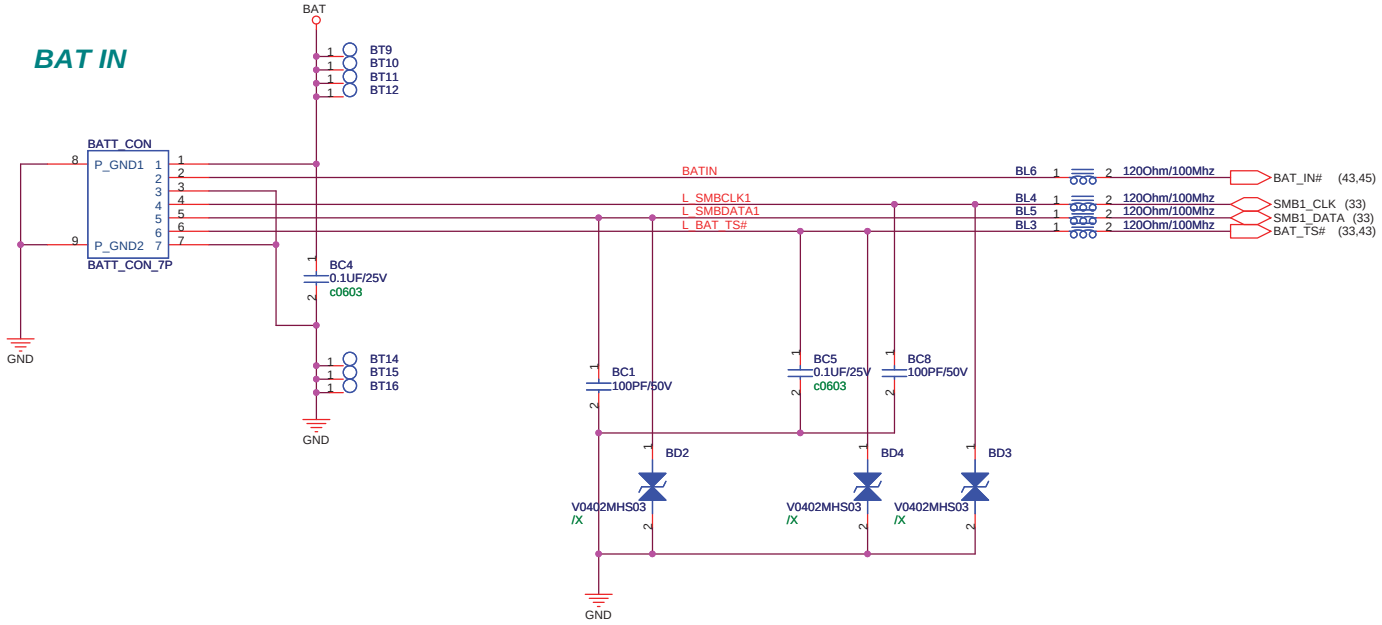
<Variant Name>

ASUSTek Computer INC.	Title : Discharge	
	Engineer: Kell_Huang	
Size: A3	Project Name: 701SDX_MB	Rev: R1.1G
Date: Wednesday, August 13, 2008	Sheet 38 of 49	

DC IN

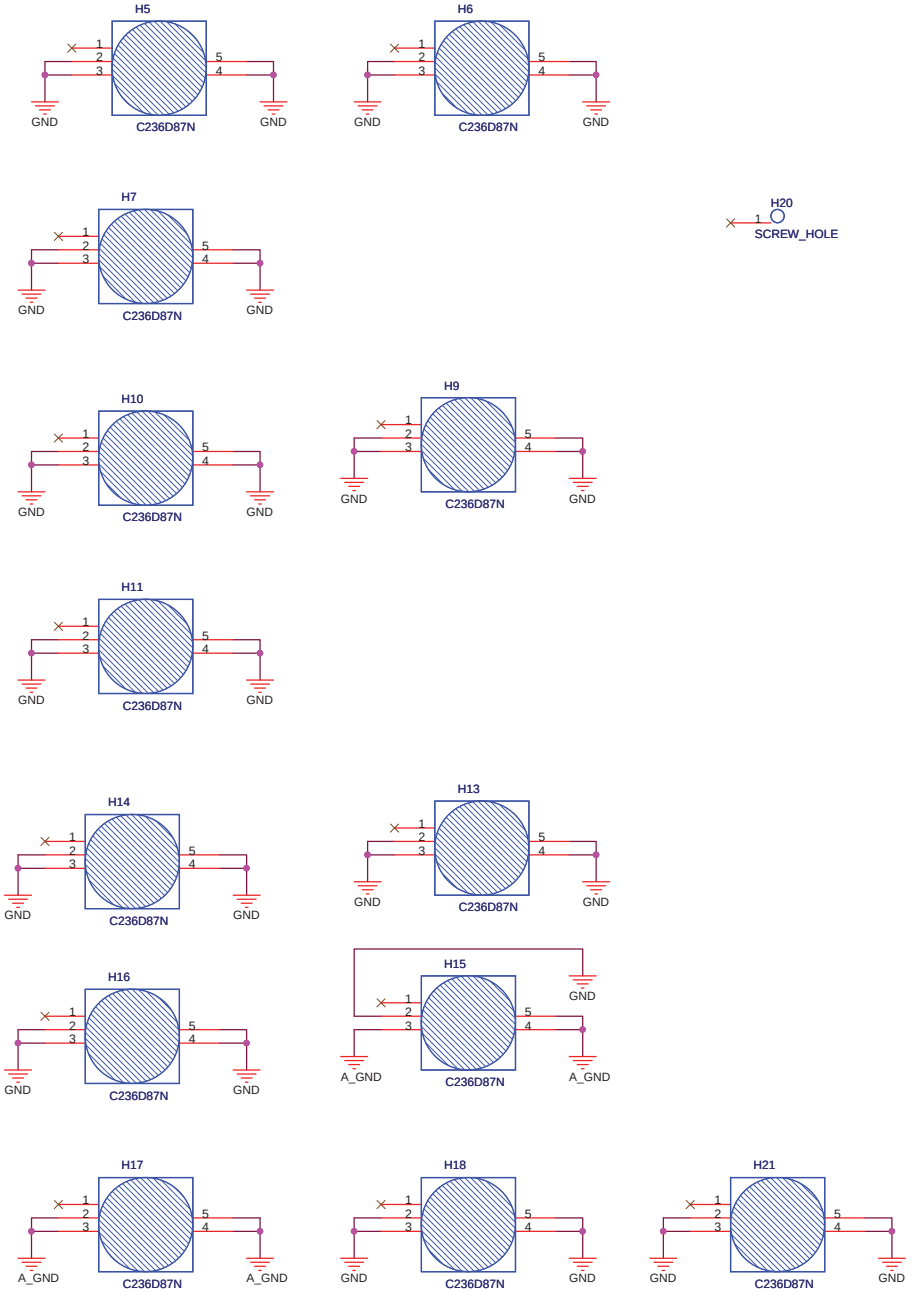


BAT IN



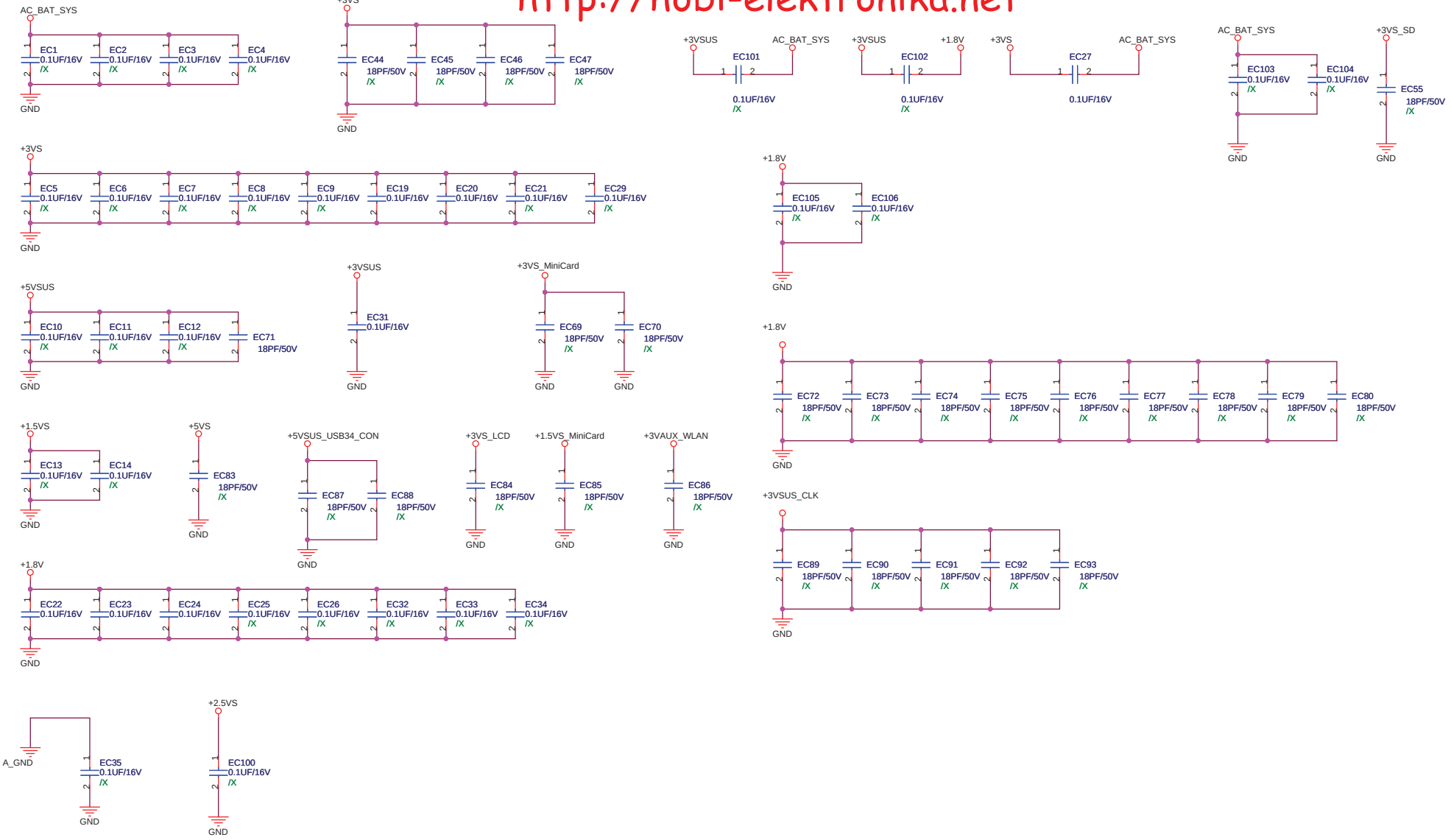
<Variant Name>

ASUSTek Computer INC.	Title : PWR Jack	
	Engineer: Kell_Huang	
Size: A3	Project Name: 701SDX_MB	Rev: R1.1G
Date: Wednesday, August 13, 2008	Sheet 39 of 49	



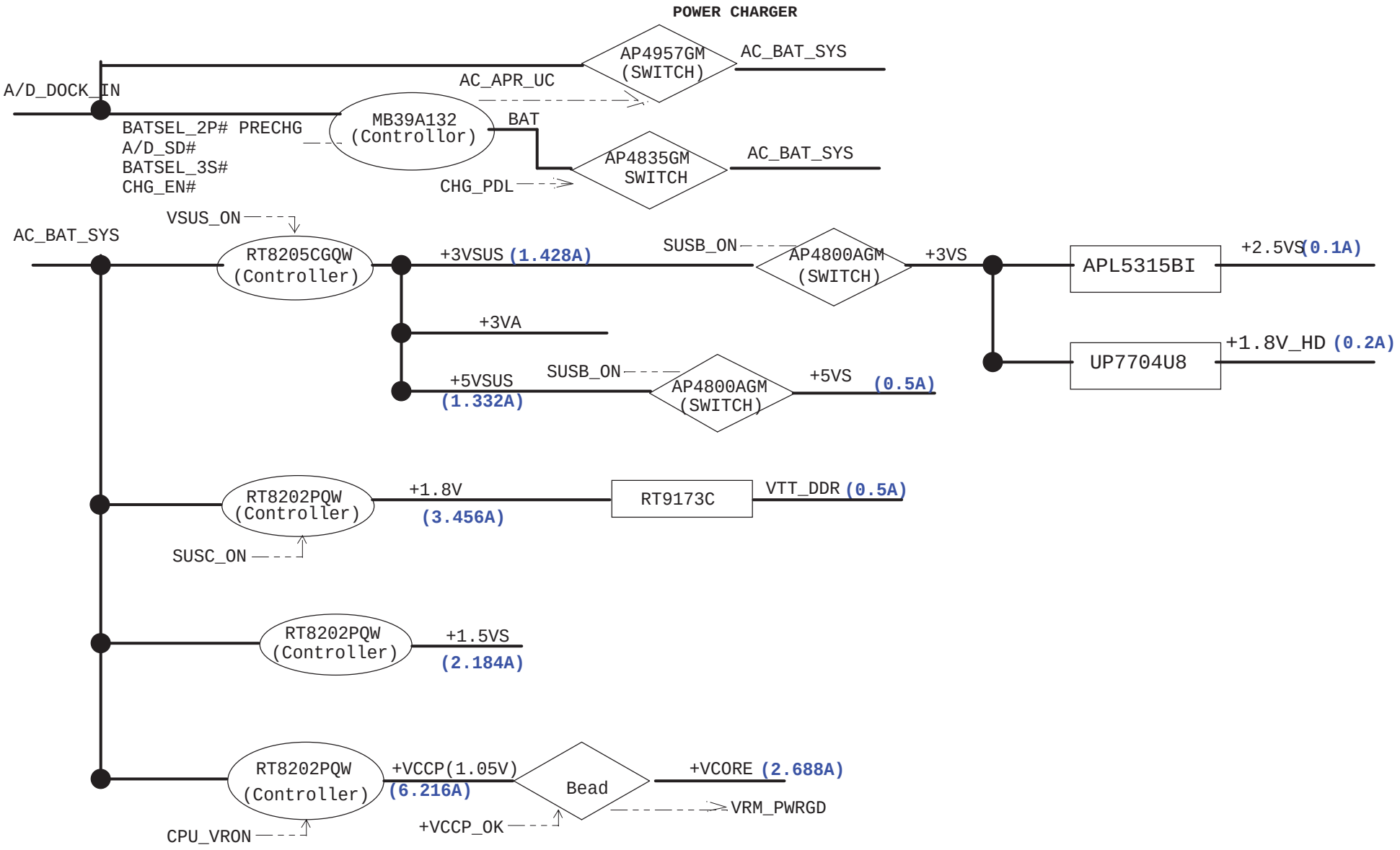
<Variant Name>

ASUSTek Computer INC.	Title : Srew Hole	
	Engineer: Kell_Huang	
Size: A3	Project Name: 701SDX_MB	Rev: R1.1G
Date: Wednesday, August 13, 2008	Sheet 40 of 49	



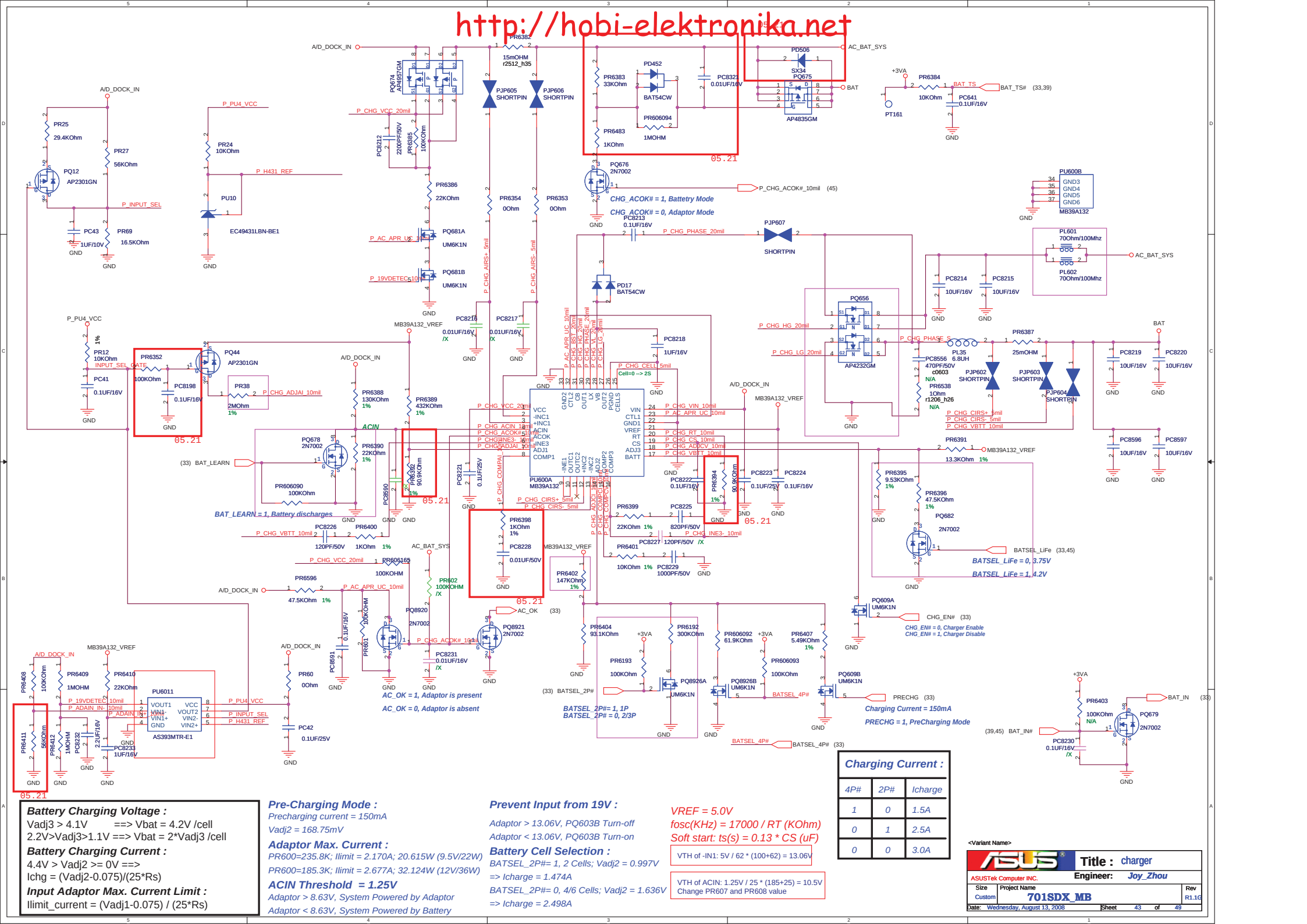
<Variant Name>

ASUSTek Computer INC.	Title : EMI	
	Engineer: Kell_Huang	
Size: A3	Project Name: 701SDX_MB	Rev: R1.1G
Date: Wednesday, August 13, 2008	Sheet 41 of 49	



<Variant Name>

ASUSTek Computer INC.	Title : Power Flow	
	Engineer: Joy_Zhou	
Size: A3	Project Name: 701SDX_MB	Rev: R1.1G
Date: Wednesday, August 13, 2008	Sheet 42 of 49	



Charging Current :		
4P#	2P#	Icharge
1	0	1.5A
0	1	2.5A
0	0	3.0A

Battery Charging Voltage :
Vadj3 > 4.1V ==> Vbat = 4.2V /cell
2.2V>Vadj3>1.1V ==> Vbat = 2*Vadj3 /cell

Battery Charging Current :
4.4V > Vadj2 >= 0V ==>
Ichg = (Vadj2-0.075)/(25*Rs)

Input Adaptor Max. Current Limit :
Ilimit_current = (Vadj1-0.075) / (25*Rs)

Pre-Charging Mode :
Precharging current = 150mA
Vadj2 = 168.75mV

Adaptor Max. Current :
PR600=235.8K; Ilimit = 2.170A; 20.615W (9.5V/22W)
PR600=185.3K; Ilimit = 2.677A; 32.124W (12V/36W)

ACIN Threshold = 1.25V
Adaptor > 8.63V, System Powered by Adaptor
Adaptor < 8.63V, System Powered by Battery

Prevent Input from 19V :
Adaptor > 13.06V, PQ603B Turn-off
Adaptor < 13.06V, PQ603B Turn-on

Battery Cell Selection :
BATSEL_2P#= 1, 2 Cells; Vadj2 = 0.997V
=> Icharge = 1.474A
BATSEL_2P#= 0, 4/6 Cells; Vadj2 = 1.636V
=> Icharge = 2.498A

VREF = 5.0V
fosc(KHz) = 17000 / RT (KOhm)
Soft start: ts(s) = 0.13 * CS (uF)

VTH of -IN1: 5V / 62 * (100+62) = 13.06V

VTH of ACIN: 1.25V / 25 * (185+25) = 10.5V
Change PR607 and PR608 value

<Variant Name>

ASUSTek Computer INC.

Title : charger
Engineer: Joy_Zhou
Size: Custom
Project Name: 701SDX_MB
Rev: R1.1G
Date: Wednesday, August 13, 2008
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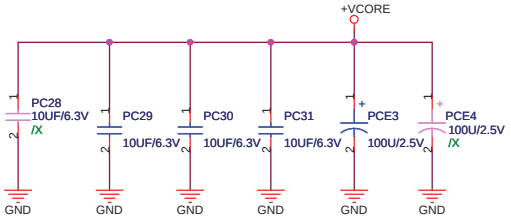
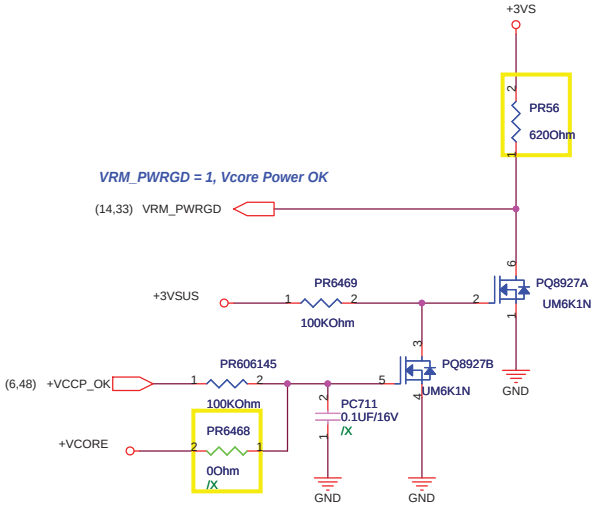
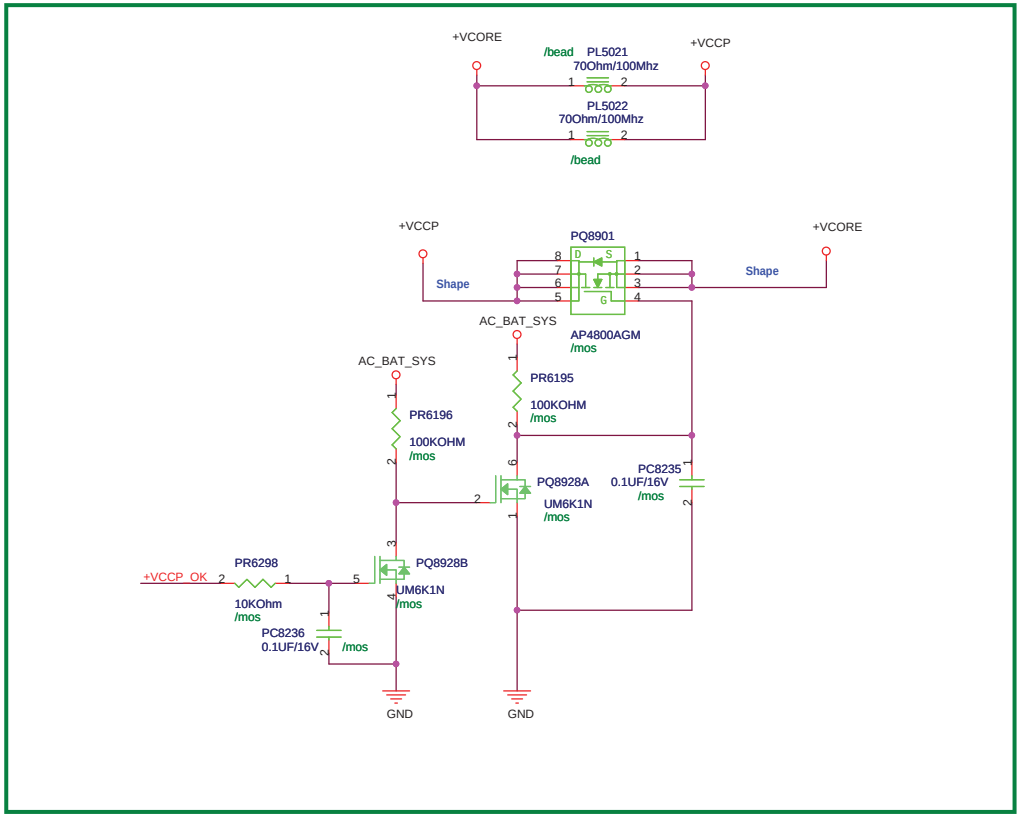
+Vcore / 7A

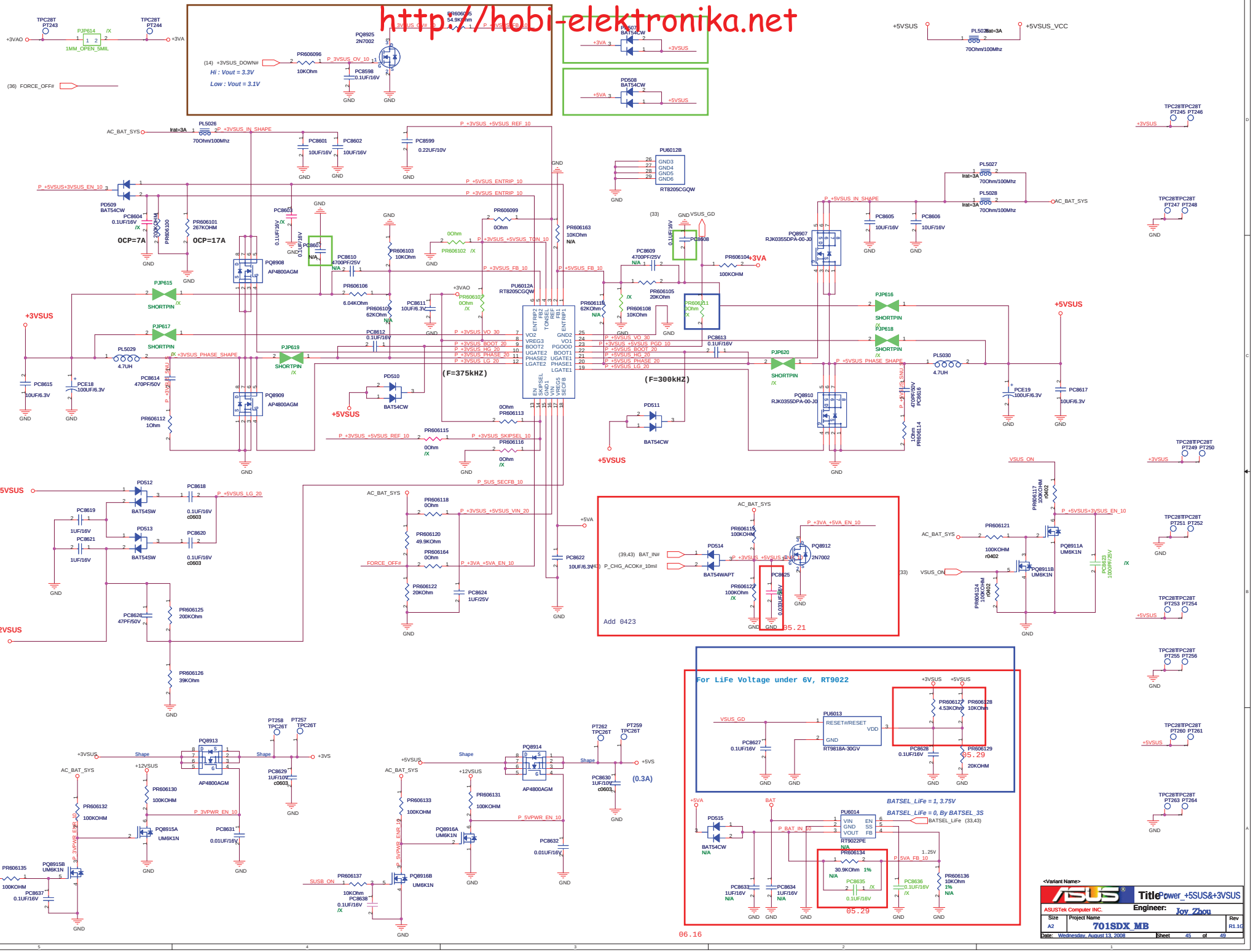


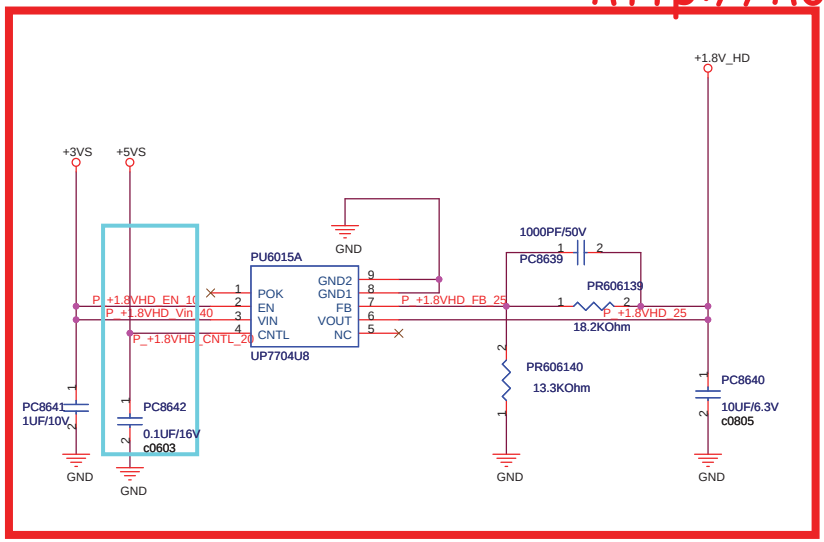


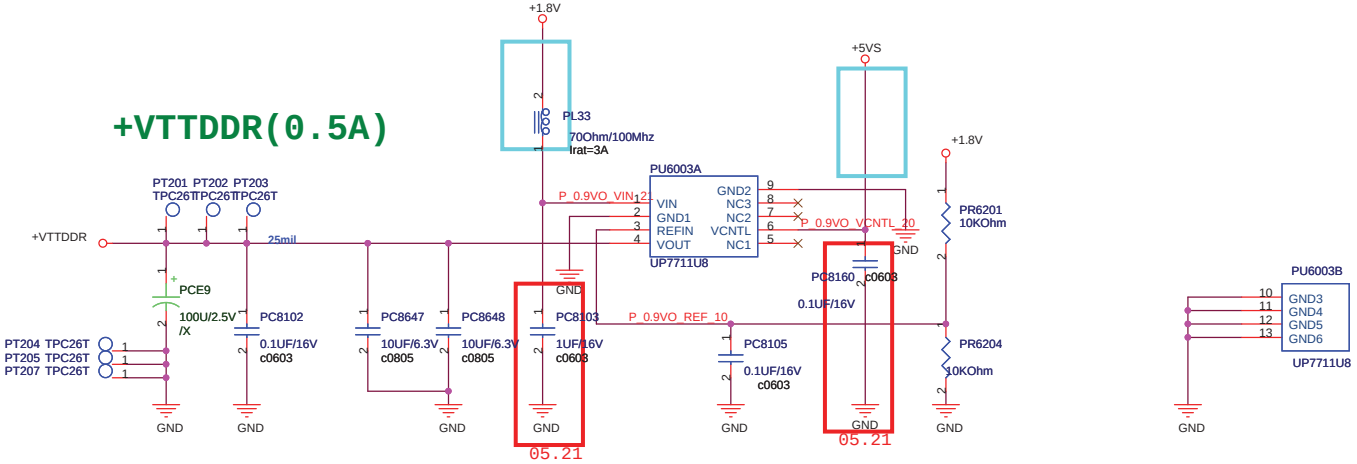


<Variant Name>

ASUSTek Computer INC.	Title : Vcore	
	Engineer: Joy_Zhou	
Size: A3	Project Name: 701SDX_MB	Rev: R1.1G
Date: Wednesday, August 13, 2008	Sheet 44 of 49	

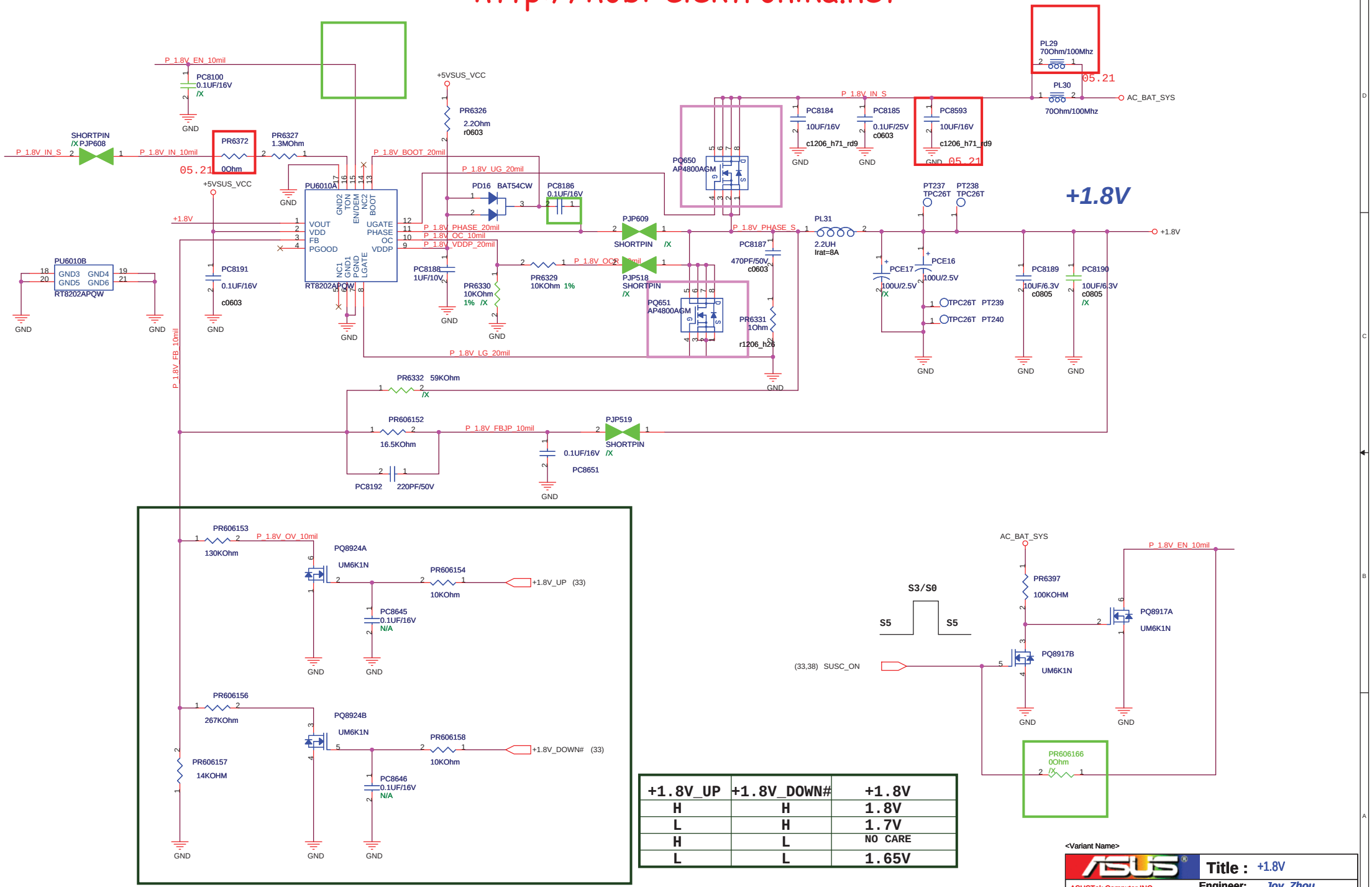






<Variant Name>

ASUSTek Computer INC.	Title : 3V_5V_VTT_DDR	
	Engineer: Joy_Zhou	
Size: A3	Project Name: 701SDX_MB	Rev: R1.1G
Date: Wednesday, August 13, 2008	Sheet 46 of 49	



+1.8V_UP	+1.8V_DOWN#	+1.8V
H	H	1.8V
L	H	1.7V
H	L	NO CARE
L	L	1.65V

<Variant Name>

ASUSTek Computer INC.

Title : +1.8V

Engineer: Joy_Zhou

Size	Project Name	Rev
A3	701SDX_MB	R1.1G

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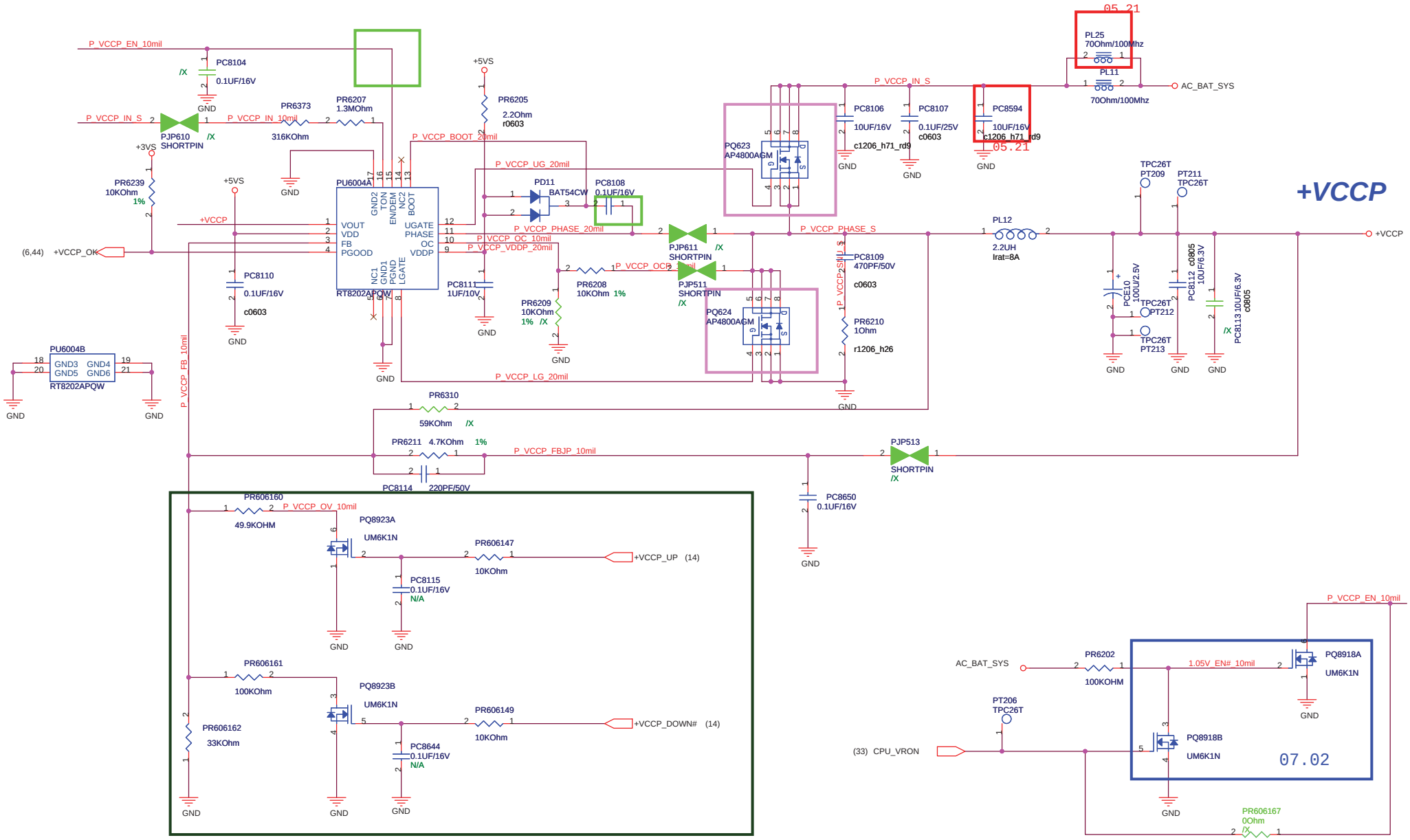
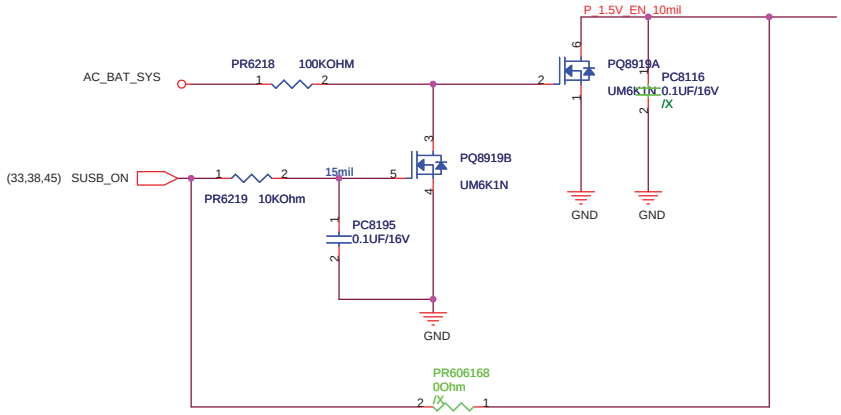
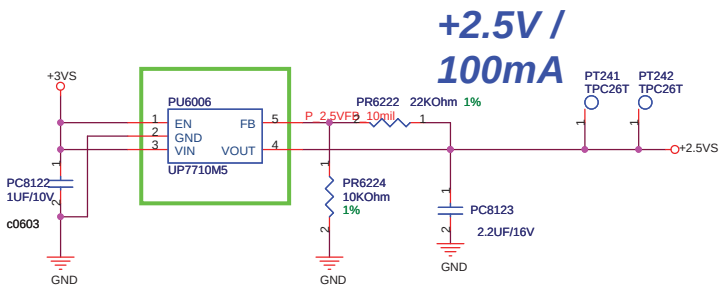


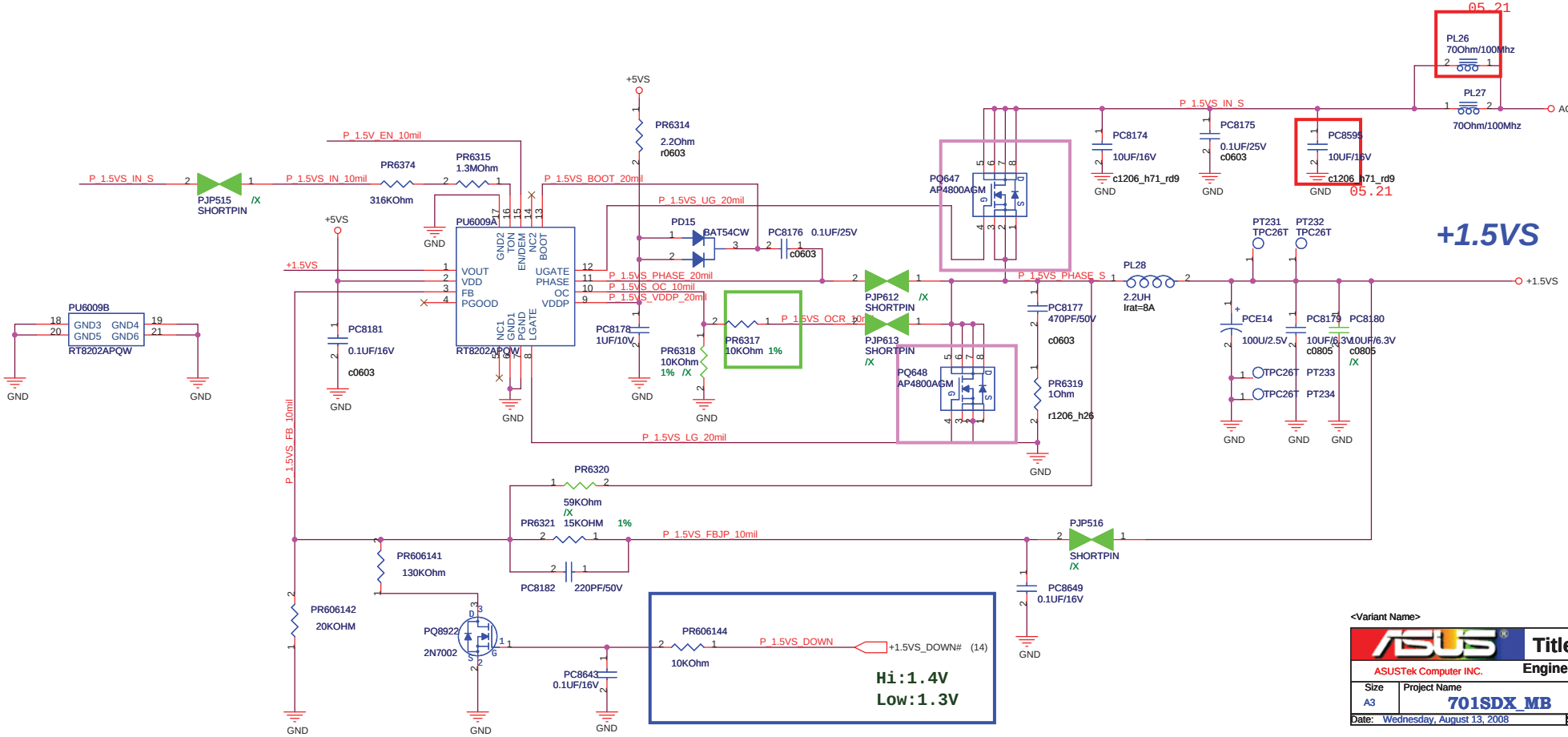
+VCCP_UP	+VCCP_DOWN#	+VCCP
H	H	0.96V
L	H	0.89V
H	L	NO CARE
L	L	0.85V

<Variant Name>

ASUSTek Computer INC.	Title : VCCP	
	Engineer: Joy_Zhou	
Size: A3	Project Name: 701SDX_MB	Rev: R1.1G
Date: Wednesday, August 13, 2008	Sheet 48 of 49	







<Variant Name>

ASUSTek Computer INC.	Title : 1.5V_2.5V	
	Engineer: Joy_Zhou	
Size: A3	Project Name: 701SDX_MB	Rev: R1.1G
Date: Wednesday, August 13, 2008	Sheet 49 of 49	