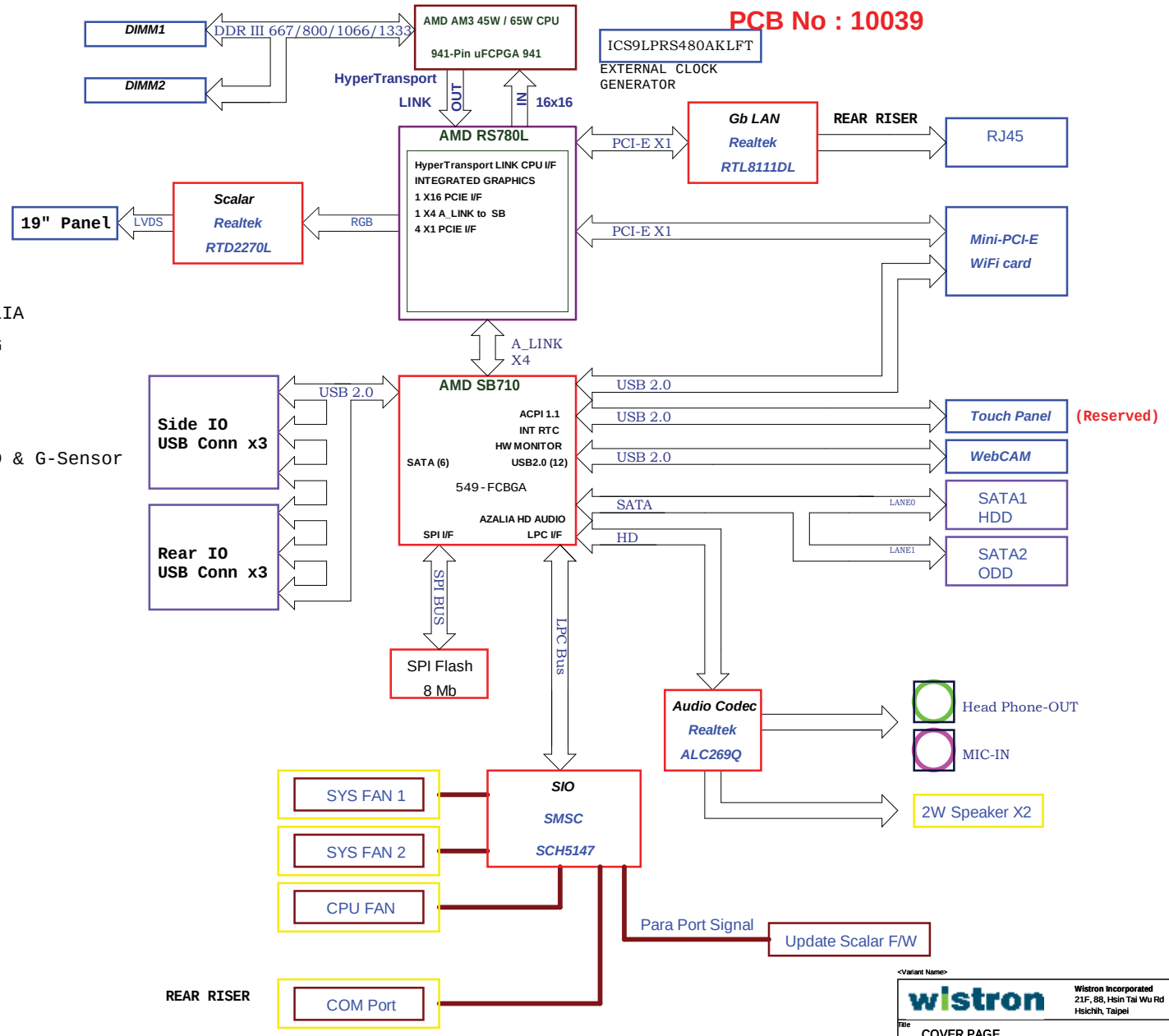
AMD RS780L+SB710 Block Diagram

PROJECT NAME : Creston / PA760F
PROJECT CODE: 91.3DM01.001
BOARD VERSION : SA
SIZE : 150 mm X 268 mm
PCB No : 10039

SHEET

BOM Cofiguration
(R): Unmount
(X): remove after MP



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Size: C
Document Number: Creston
Rev: SA
Date: Wednesday, August 04, 2010
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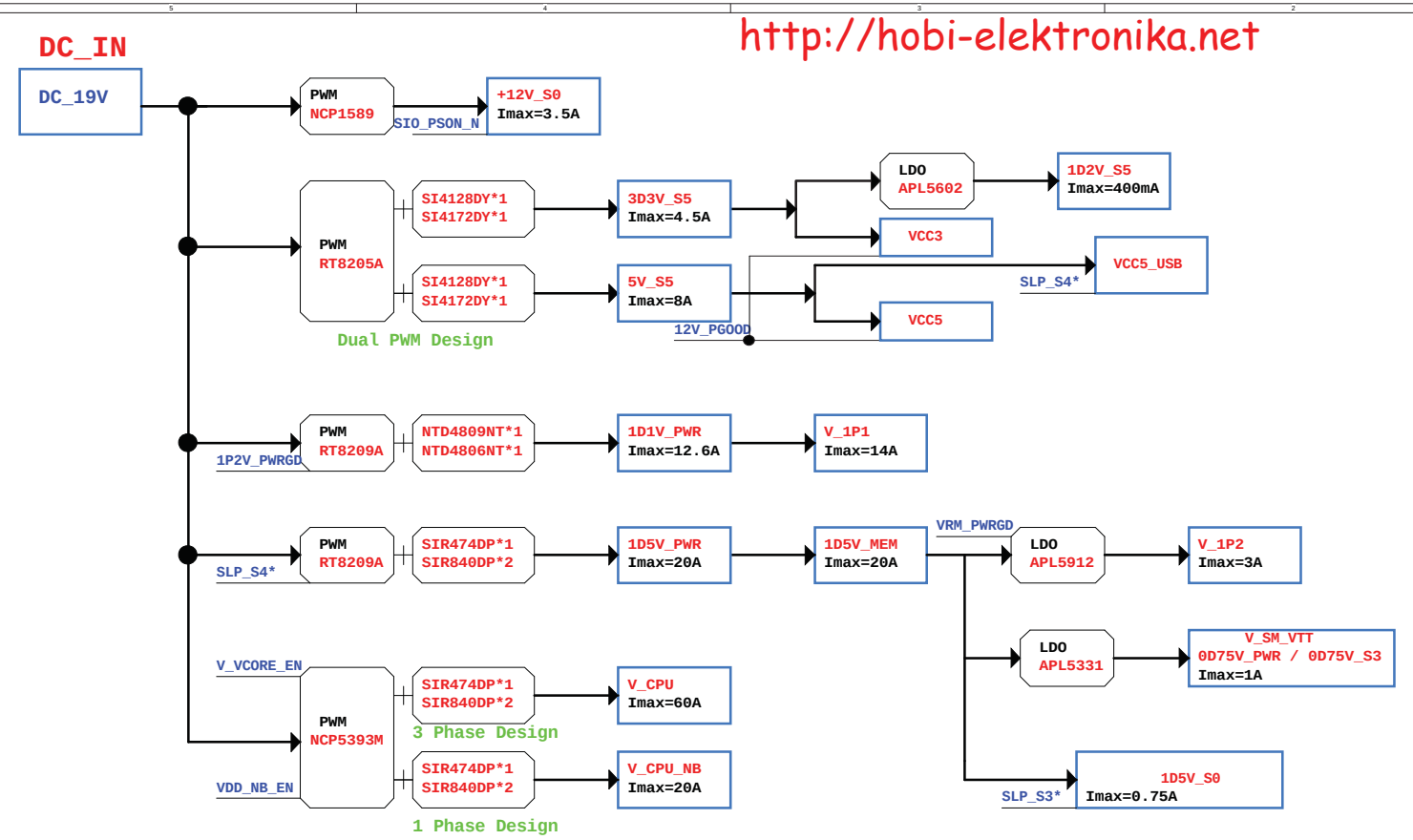

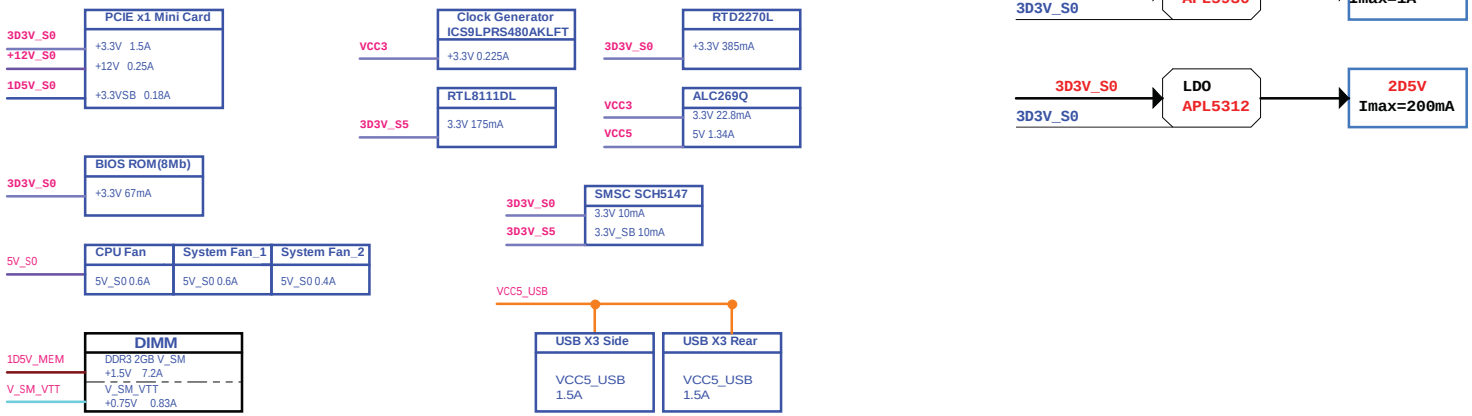

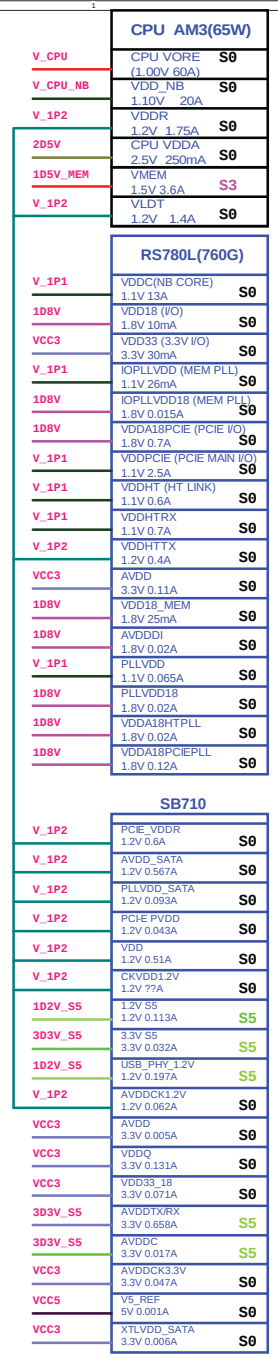

<Variant Name>

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Title: POWER MAP

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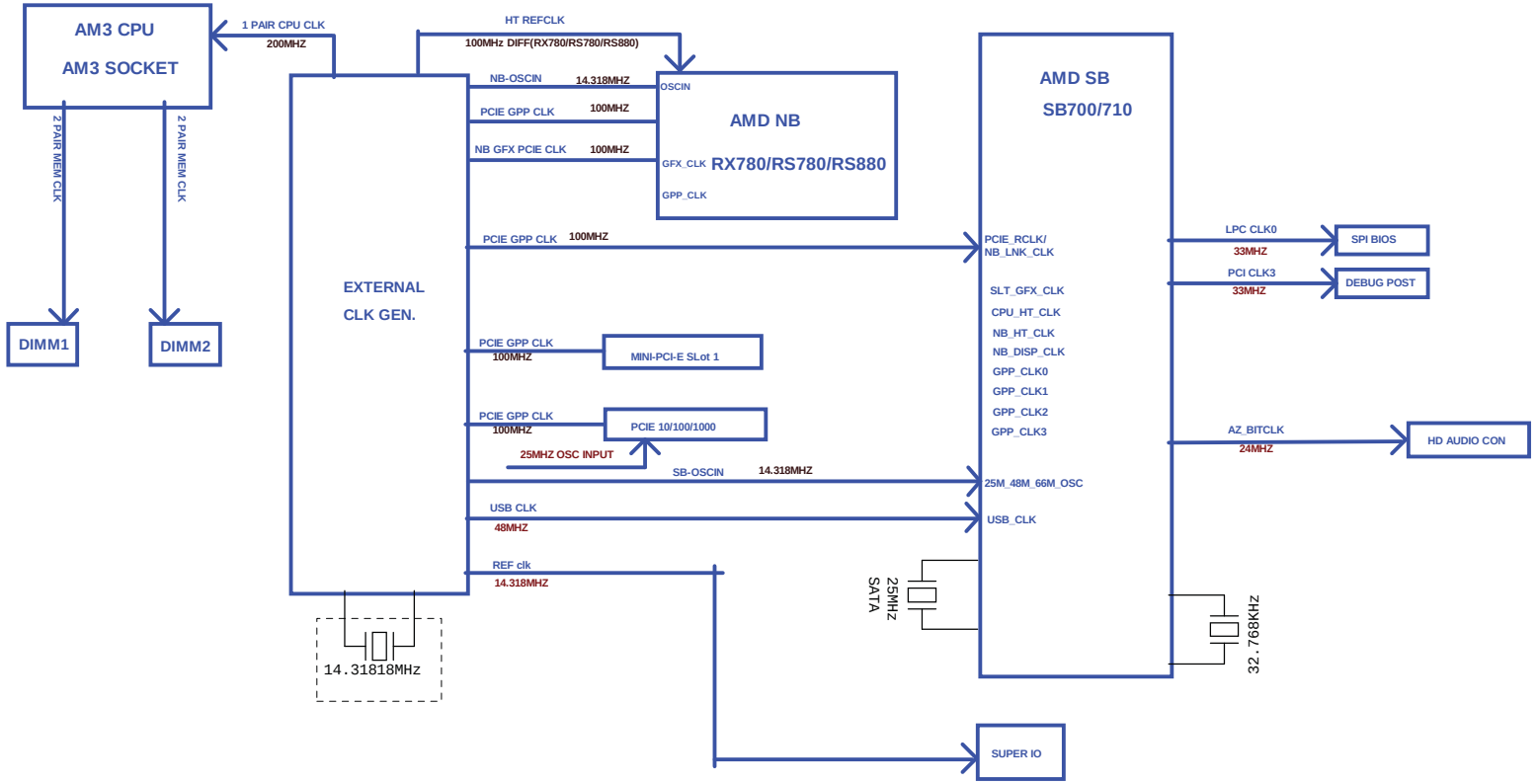

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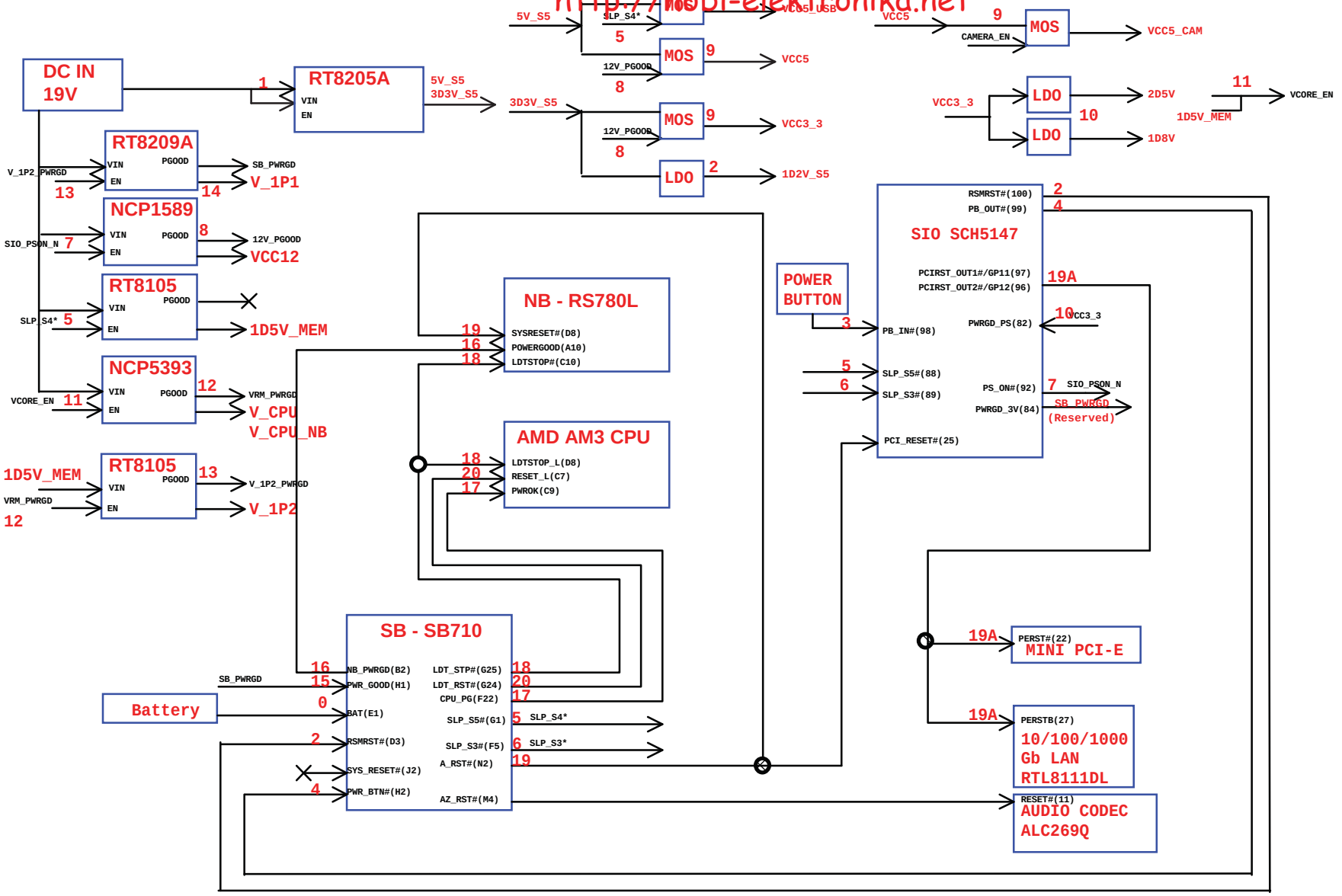
Title: CLOCK MAP

Size	Document Number	Rev
B	Creston	SA

Date: Wednesday, August 04, 2010 Sheet 3 of 44



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Title: SEQUENCE MAP

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Date: Wednesday, August 04, 2010 | Sheet 4 of 44

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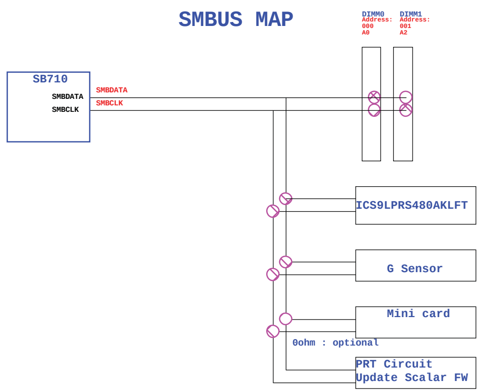
SB710

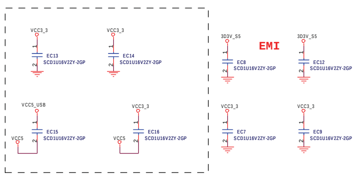
GPIO	PIN	POWER WELL	USAGE	BIOS Pull Value	Pull Type	Pull Value	Notes
[illegible]	[illegible]	[illegible]	NO USE	[illegible]	[illegible]	[illegible]	
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]		[illegible]
[illegible]	[illegible]	[illegible]	[illegible]		[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]		[illegible]		[illegible]
[illegible]	[illegible]	[illegible]	NO USE		[illegible]		
[illegible]	[illegible]	[illegible]	[illegible]		TRI STATE		[illegible]
[illegible]	[illegible]	[illegible]	NO USE		[illegible]		
[illegible]	[illegible]	[illegible]	NO USE		[illegible]		
[illegible]	[illegible]	[illegible]	[illegible]		[illegible]		[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	NO USE		[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]		[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]		[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]		[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	NO USE		[illegible]	[illegible]	

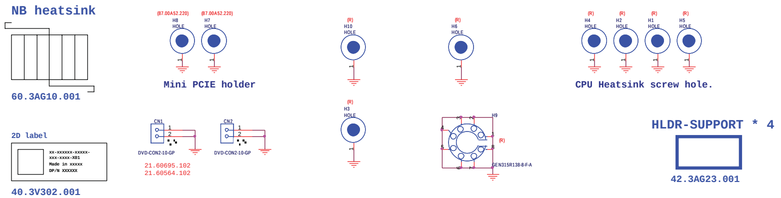
SIO SCH5147

GPIO#	Function Usage	BIOS Default Setting	I/O	IN-POWER	OUT-POWER
[illegible]	[illegible]	[illegible]	O	N/A	AUX (VTR)
GP11	PLTRST*_R [illegible]	[illegible]	O	N/A	AUX (VTR)
[illegible]	PLTRST*_LAN	[illegible]	O	N/A	AUX (VTR)
[illegible]	PLTRST* [illegible]	[illegible]	O	N/A	AUX (VTR)
GP16	[illegible]	[illegible]	O	N/A	AUX (VTR)
GP17	SYS_FAN2_CTRL_SIO	PWM3	O	N/A	AUX (VTR)
[illegible]	[illegible]	[illegible]	I	AUX (VTR)	MAIN (VCC)
GP21	KBDATA	[illegible]	O	AUX (VTR)	MAIN (VCC)
[illegible]	[illegible]	[illegible]	O	AUX (VTR)	MAIN (VCC)
[illegible]	[illegible]	[illegible]	O	AUX (VTR)	AUX (VTR)
[illegible]	MSDATA	[illegible]	O	AUX (VTR)	MAIN (VCC)
[illegible]	[illegible]	[illegible]	O	AUX (VTR)	MAIN (VCC)
GP26	KBRST*	[illegible]	O	AUX (VTR)	MAIN (VCC)
[illegible]	[illegible]	[illegible]	O	AUX (VTR)	MAIN (VCC)
[illegible]	[illegible]	[illegible]	I	AUX (VTR)	AUX (VTR)
[illegible]	[illegible]	[illegible]	O	AUX (VTR)	AUX (VTR)
[illegible]	[illegible]	[illegible]	O	AUX (VTR)	AUX (VTR)
GP43	[illegible]	[illegible]	I/O	AUX (VTR)	MAIN (VCC)
[illegible]	[illegible]	[illegible]	I	AUX (VTR)	AUX (VTR)
[illegible]	[illegible]	[illegible]	O	AUX (VTR)	AUX (VTR)
[illegible]	[illegible]	[illegible]	O	AUX (VTR)	AUX (VTR)
[illegible]	[illegible]	[illegible]	O	AUX (VTR)	AUX (VTR)
[illegible]	[illegible]	[illegible]	I/O	AUX (VTR)	AUX (VTR)
[illegible]	[illegible]	[illegible]	I	AUX (VTR)	AUX (VTR)
[illegible]	[illegible]	[illegible]	I	AUX (VTR)	AUX (VTR)
[illegible]	[illegible]	[illegible]	I	AUX (VTR)	AUX (VTR)
[illegible]	[illegible]	[illegible]	I	AUX (VTR)	AUX (VTR)
[illegible]	[illegible]	[illegible]	I	AUX (VTR)	AUX (VTR)

SMBUS MAP







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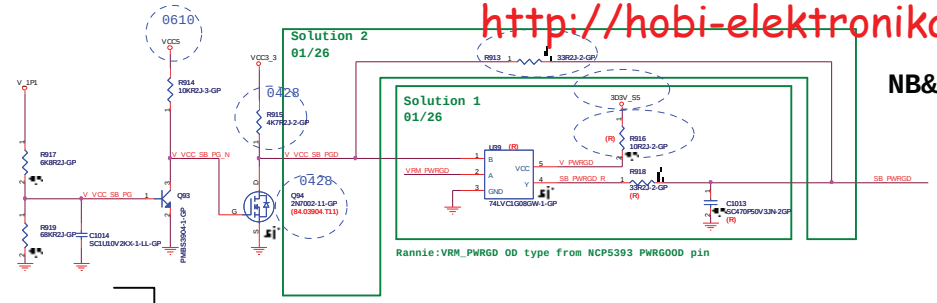
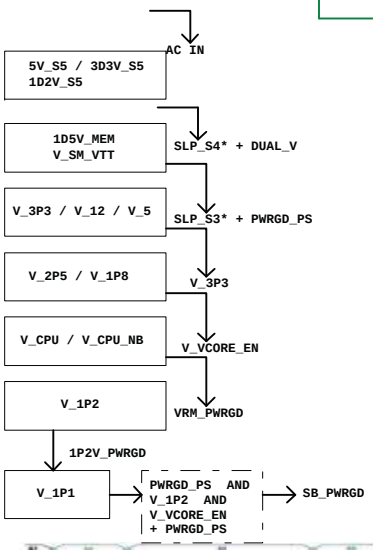
GPIO/HOLE/EMI CAP

NB&SB POWER GOOD

RSMRST

Del Discrete RSMRST circuit





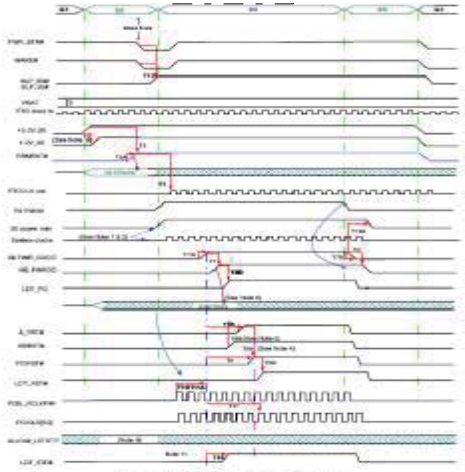


Figure 6-1: SB700 Power Up/Down Sequence

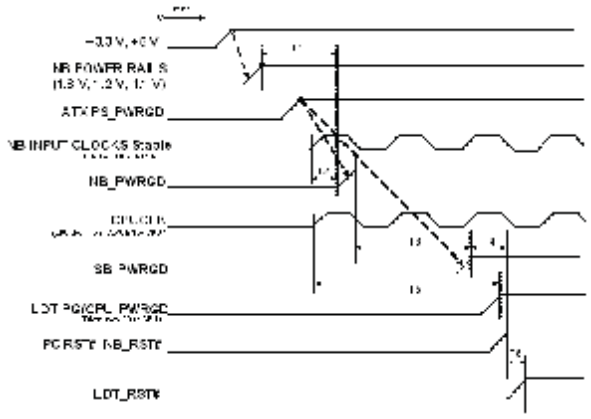


Table 15 RS740/RS780/RX780 Power Up Sequence Timing Data

Symbol	Time Log	Min. (ms)	Typ. (ms)	Max. (ms)
1	All NB Power Rails valid before NB_PWRGD HIGH	1		
2	Stable input Clocks from CLKGEN to NB before NB_PWRGD	1	—	—
3	NB_PWRGD HIGH to SB_PWRGD HIGH Note: These values apply to SB600 only. Refer to SB700 Design Guide for SB700 values. For detailed information, see SB700 and SB710 Design Guides	[illegible]	[illegible]	[illegible]
4	SB_PWRGD HIGH to/or PCIRST#/CB_RST# HIGH (delay in Southbridge)	8		8
5	Stable CPUCLK to LDT_RST# before LDT_PG/CPU_PWRGD HIGH	1	—	—
6	PCIRST#/NB_RST# HIGH to/or LDT_RST# HIGH (delay in Southbridge)	8	—	8

§ Note: Refer to the AMD SB700 Databook and AMD SB600 Databook for the values.

<Variant Name>

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Title: PWR Sequence and PCIRST#

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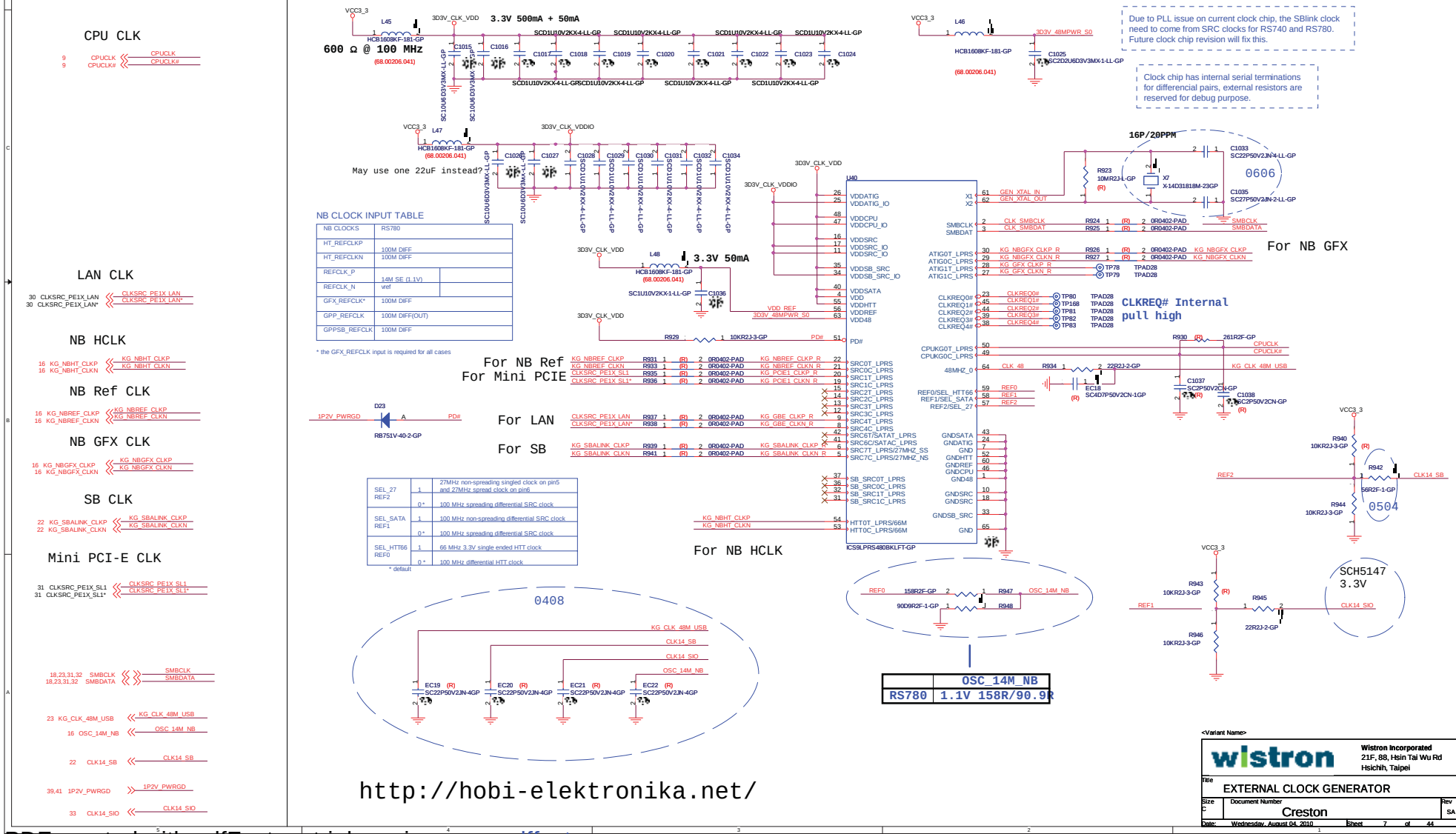

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Title: EXTERNAL CLOCK GENERATOR

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HT Interface

14 HT_CLKIN1_P — HT_CLKIN1_P
14 HT_CLKIN1_N — HT_CLKIN1_N
14 HT_CLKIN0_P — HT_CLKIN0_P
14 HT_CLKIN0_N — HT_CLKIN0_N

14 HT_CTLIN1_P — HT_CTLIN1_P
14 HT_CTLIN1_N — HT_CTLIN1_N
14 HT_CTLIN0_P — HT_CTLIN0_P
14 HT_CTLIN0_N — HT_CTLIN0_N

14 HT_CLKOUT1_P — HT_CLKOUT1_P
14 HT_CLKOUT1_N — HT_CLKOUT1_N
14 HT_CLKOUT0_P — HT_CLKOUT0_P
14 HT_CLKOUT0_N — HT_CLKOUT0_N

14 HT_CTLOUT1_P — HT_CTLOUT1_P
14 HT_CTLOUT1_N — HT_CTLOUT1_N
14 HT_CTLOUT0_P — HT_CTLOUT0_P
14 HT_CTLOUT0_N — HT_CTLOUT0_N

14 HT_CADIN7_P — HT_CADIN7_P
14 HT_CADIN7_N — HT_CADIN7_N
14 HT_CADIN6_P — HT_CADIN6_P
14 HT_CADIN6_N — HT_CADIN6_N
14 HT_CADIN5_P — HT_CADIN5_P
14 HT_CADIN5_N — HT_CADIN5_N
14 HT_CADIN4_P — HT_CADIN4_P
14 HT_CADIN4_N — HT_CADIN4_N
14 HT_CADIN3_P — HT_CADIN3_P
14 HT_CADIN3_N — HT_CADIN3_N
14 HT_CADIN2_P — HT_CADIN2_P
14 HT_CADIN2_N — HT_CADIN2_N
14 HT_CADIN1_P — HT_CADIN1_P
14 HT_CADIN1_N — HT_CADIN1_N
14 HT_CADIN0_P — HT_CADIN0_P
14 HT_CADIN0_N — HT_CADIN0_N

14 HT_CADIN15_P — HT_CADIN15_P
14 HT_CADIN15_N — HT_CADIN15_N
14 HT_CADIN14_P — HT_CADIN14_P
14 HT_CADIN14_N — HT_CADIN14_N
14 HT_CADIN13_P — HT_CADIN13_P
14 HT_CADIN13_N — HT_CADIN13_N
14 HT_CADIN12_P — HT_CADIN12_P
14 HT_CADIN12_N — HT_CADIN12_N
14 HT_CADIN11_P — HT_CADIN11_P
14 HT_CADIN11_N — HT_CADIN11_N
14 HT_CADIN10_P — HT_CADIN10_P
14 HT_CADIN10_N — HT_CADIN10_N
14 HT_CADIN9_P — HT_CADIN9_P
14 HT_CADIN9_N — HT_CADIN9_N
14 HT_CADIN8_P — HT_CADIN8_P
14 HT_CADIN8_N — HT_CADIN8_N

14 HT_CADOUT7_P — HT_CADOUT7_P
14 HT_CADOUT7_N — HT_CADOUT7_N
14 HT_CADOUT6_P — HT_CADOUT6_P
14 HT_CADOUT6_N — HT_CADOUT6_N
14 HT_CADOUT5_P — HT_CADOUT5_P
14 HT_CADOUT5_N — HT_CADOUT5_N
14 HT_CADOUT4_P — HT_CADOUT4_P
14 HT_CADOUT4_N — HT_CADOUT4_N
14 HT_CADOUT3_P — HT_CADOUT3_P
14 HT_CADOUT3_N — HT_CADOUT3_N
14 HT_CADOUT2_P — HT_CADOUT2_P
14 HT_CADOUT2_N — HT_CADOUT2_N
14 HT_CADOUT1_P — HT_CADOUT1_P
14 HT_CADOUT1_N — HT_CADOUT1_N
14 HT_CADOUT0_P — HT_CADOUT0_P
14 HT_CADOUT0_N — HT_CADOUT0_N

14 HT_CADOUT15_P — HT_CADOUT15_P
14 HT_CADOUT15_N — HT_CADOUT15_N
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14 HT_CADOUT14_N — HT_CADOUT14_N
14 HT_CADOUT13_P — HT_CADOUT13_P
14 HT_CADOUT13_N — HT_CADOUT13_N
14 HT_CADOUT12_P — HT_CADOUT12_P
14 HT_CADOUT12_N — HT_CADOUT12_N
14 HT_CADOUT11_P — HT_CADOUT11_P
14 HT_CADOUT11_N — HT_CADOUT11_N
14 HT_CADOUT10_P — HT_CADOUT10_P
14 HT_CADOUT10_N — HT_CADOUT10_N
14 HT_CADOUT9_P — HT_CADOUT9_P
14 HT_CADOUT9_N — HT_CADOUT9_N
14 HT_CADOUT8_P — HT_CADOUT8_P
14 HT_CADOUT8_N — HT_CADOUT8_N

U41A 1 0F 8

OPTERON HT LINK

HT_CLKIN1_P	N6	L0_CLKIN_H1	L0_CLKOUT_H1	AD5	HT_CLKOUT1_P
HT_CLKIN1_N	P6	L0_CLKIN_L1	L0_CLKOUT_L1	AD4	HT_CLKOUT1_N
HT_CLKIN0_P	N3	L0_CLKIN_H0	L0_CLKOUT_H0	AD1	HT_CLKOUT0_P
HT_CLKIN0_N	N2	L0_CLKIN_L0	L0_CLKOUT_L0	AC1	HT_CLKOUT0_N
HT_CTLIN1_P	V4	L0_CTLIN_H1	L0_CTLOUT_H1	Y6	HT_CTLOUT1_P
HT_CTLIN1_N	V5	L0_CTLIN_L1	L0_CTLOUT_L1	W6	HT_CTLOUT1_N
HT_CTLIN0_P	U1	L0_CTLIN_H0	L0_CTLOUT_H0	W2	HT_CTLOUT0_P
HT_CTLIN0_N	V1	L0_CTLIN_L0	L0_CTLOUT_L0	W3	HT_CTLOUT0_N
HT_CADIN15_P	U6	L0_CADIN_H15	L0_CADOUT_H15	Y5	HT_CADOUT15_P
HT_CADIN15_N	V6	L0_CADIN_L15	L0_CADOUT_L15	Y4	HT_CADOUT15_N
HT_CADIN14_P	T4	L0_CADIN_H14	L0_CADOUT_H14	AB6	HT_CADOUT14_P
HT_CADIN14_N	T5	L0_CADIN_L14	L0_CADOUT_L14	AA6	HT_CADOUT14_N
HT_CADIN13_P	R6	L0_CADIN_H13	L0_CADOUT_H13	AB5	HT_CADOUT13_P
HT_CADIN13_N	T6	L0_CADIN_L13	L0_CADOUT_L13	AB4	HT_CADOUT13_N
HT_CADIN12_P	P4	L0_CADIN_H12	L0_CADOUT_H12	AD6	HT_CADOUT12_P
HT_CADIN12_N	P5	L0_CADIN_L12	L0_CADOUT_L12	AC6	HT_CADOUT12_N
HT_CADIN11_P	M4	L0_CADIN_H11	L0_CADOUT_H11	AF6	HT_CADOUT11_P
HT_CADIN11_N	M5	L0_CADIN_L11	L0_CADOUT_L11	AE6	HT_CADOUT11_N
HT_CADIN10_P	L6	L0_CADIN_H10	L0_CADOUT_H10	AF5	HT_CADOUT10_P
HT_CADIN10_N	M6	L0_CADIN_L10	L0_CADOUT_L10	AF4	HT_CADOUT10_N
HT_CADIN9_P	K4	L0_CADIN_H9	L0_CADOUT_H9	AH6	HT_CADOUT9_P
HT_CADIN9_N	K5	L0_CADIN_L9	L0_CADOUT_L9	AG6	HT_CADOUT9_N
HT_CADIN8_P	J6	L0_CADIN_H8	L0_CADOUT_H8	AH5	HT_CADOUT8_P
HT_CADIN8_N	K6	L0_CADIN_L8	L0_CADOUT_L8	AH4	HT_CADOUT8_N
HT_CADIN7_P	U3	L0_CADIN_H7	L0_CADOUT_H7	Y1	HT_CADOUT7_P
HT_CADIN7_N	U2	L0_CADIN_L7	L0_CADOUT_L7	W1	HT_CADOUT7_N
HT_CADIN6_P	R1	L0_CADIN_H6	L0_CADOUT_H6	AA2	HT_CADOUT6_P
HT_CADIN6_N	T1	L0_CADIN_L6	L0_CADOUT_L6	AA3	HT_CADOUT6_N
HT_CADIN5_P	R3	L0_CADIN_H5	L0_CADOUT_H5	AB1	HT_CADOUT5_P
HT_CADIN5_N	R2	L0_CADIN_L5	L0_CADOUT_L5	AA1	HT_CADOUT5_N
HT_CADIN4_P	N1	L0_CADIN_H4	L0_CADOUT_H4	AC2	HT_CADOUT4_P
HT_CADIN4_N	P1	L0_CADIN_L4	L0_CADOUT_L4	AC3	HT_CADOUT4_N
HT_CADIN3_P	L1	L0_CADIN_H3	L0_CADOUT_H3	AE2	HT_CADOUT3_P
HT_CADIN3_N	M1	L0_CADIN_L3	L0_CADOUT_L3	AE3	HT_CADOUT3_N
HT_CADIN2_P	L3	L0_CADIN_H2	L0_CADOUT_H2	AF1	HT_CADOUT2_P
HT_CADIN2_N	L2	L0_CADIN_L2	L0_CADOUT_L2	AE1	HT_CADOUT2_N
HT_CADIN1_P	J1	L0_CADIN_H1	L0_CADOUT_H1	AG2	HT_CADOUT1_P
HT_CADIN1_N	K1	L0_CADIN_L1	L0_CADOUT_L1	AG3	HT_CADOUT1_N
HT_CADIN0_P	J3	L0_CADIN_H0	L0_CADOUT_H0	AH1	HT_CADOUT0_P
HT_CADIN0_N	J2	L0_CADIN_L0	L0_CADOUT_L0	AG1	HT_CADOUT0_N

OPTER
(62.10055.391)

<Variant Name>

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Hsichih, Taipei

Title: CPU HT Interface

Size: A3 | Document Number: Creston | Rev: SA

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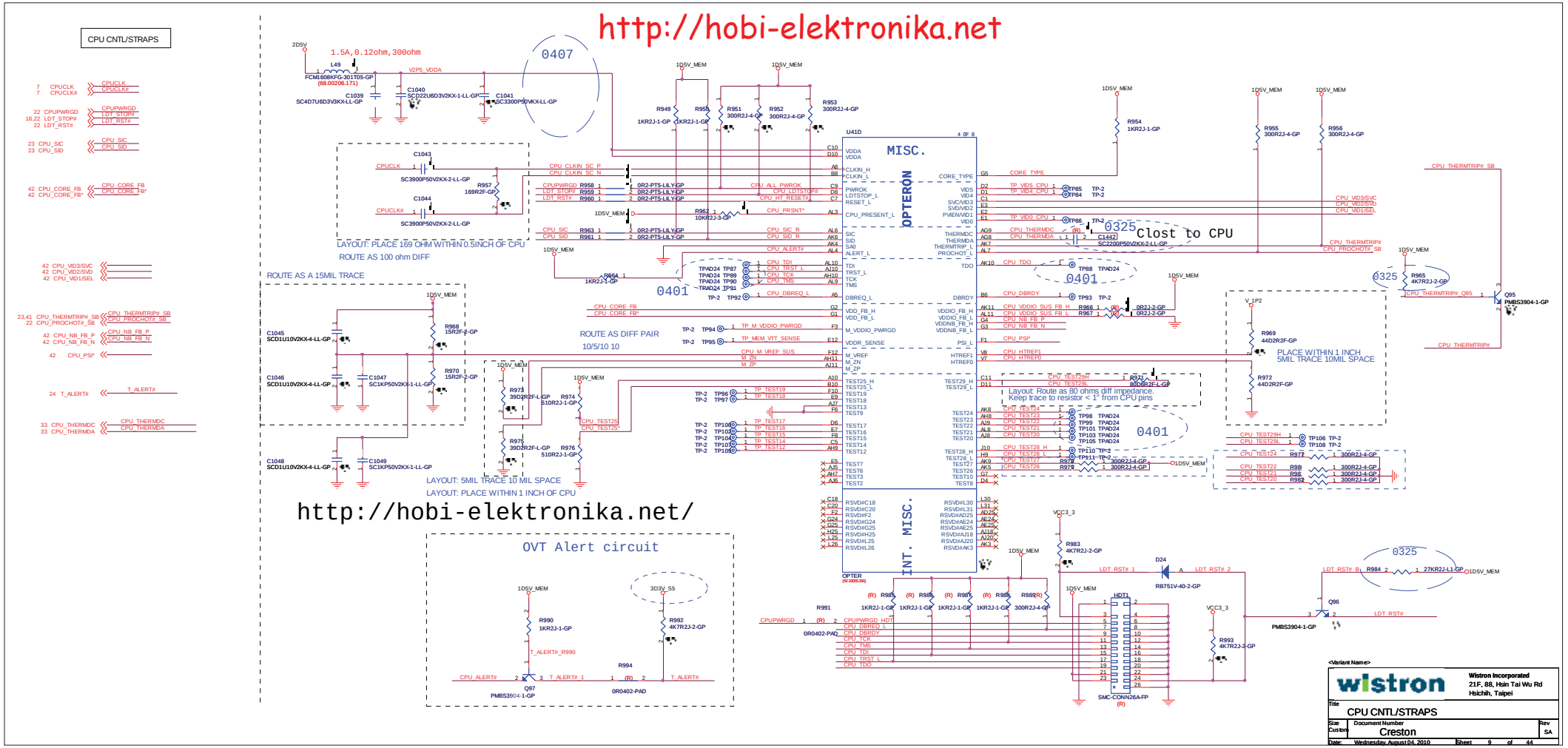

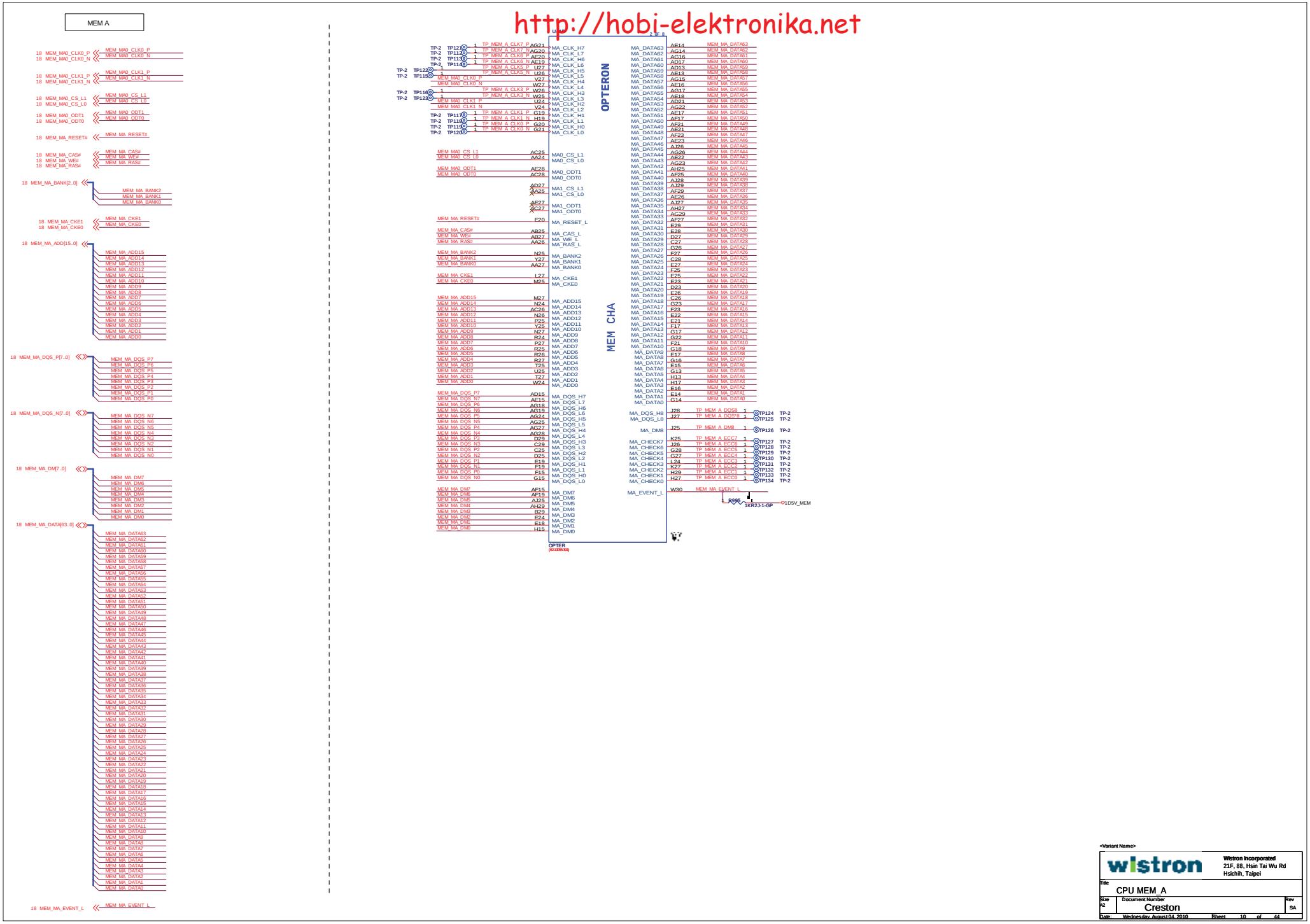

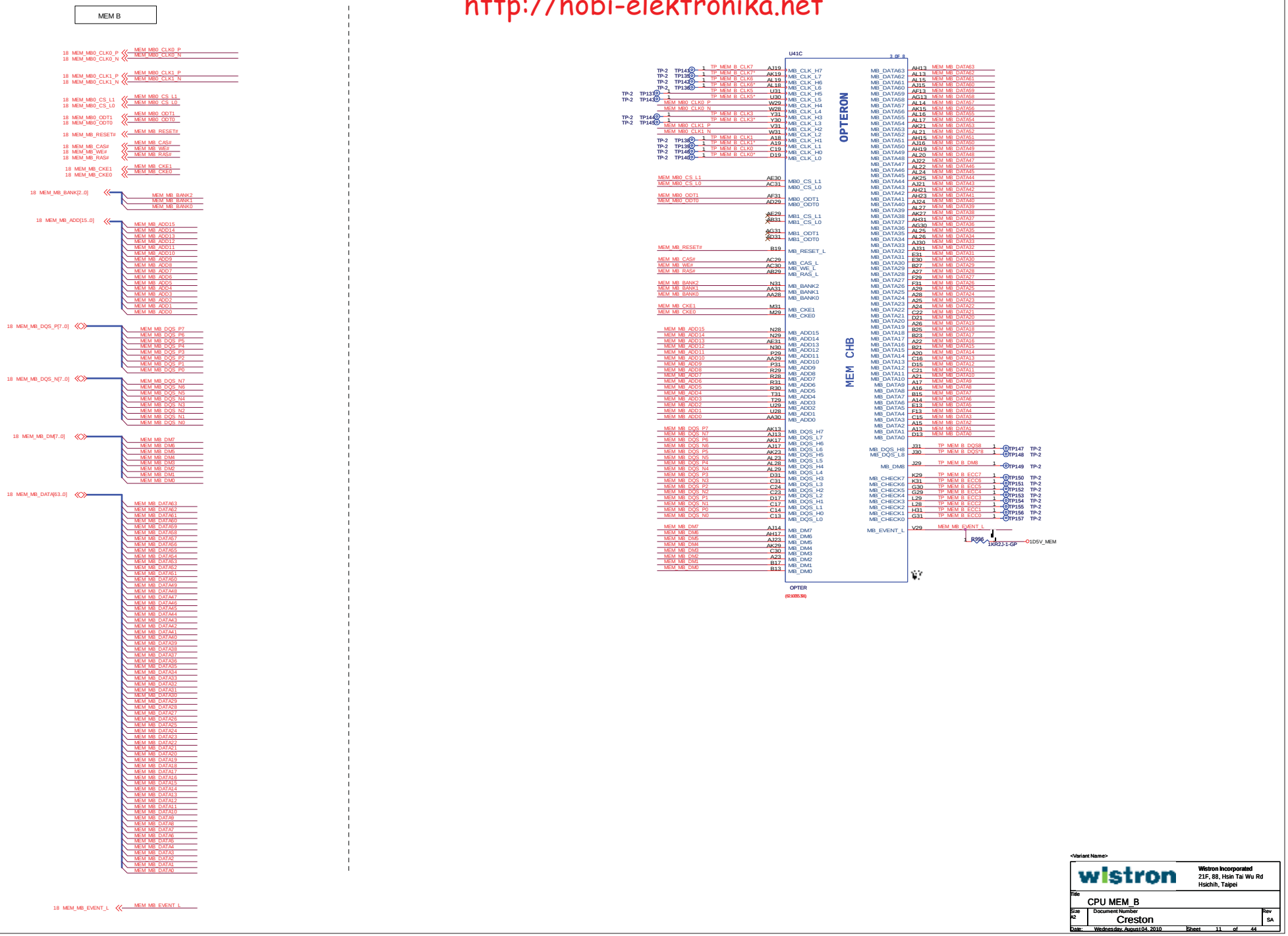

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Hsichih, Taipei

Title: CPU MEM_B

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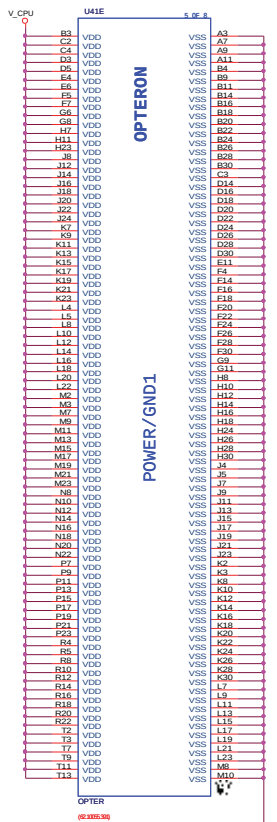
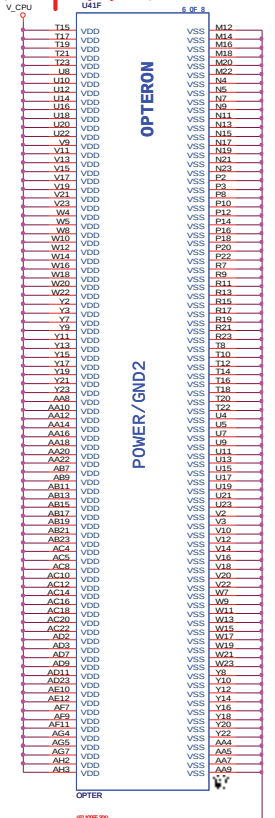
POWER

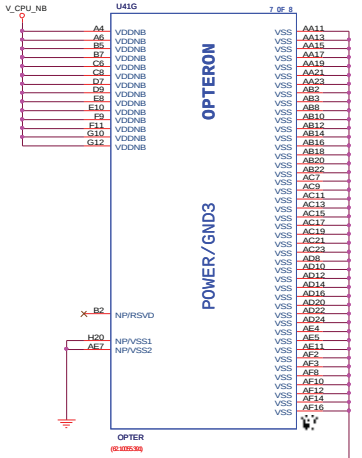
1D5V_MEM 1D5V_MEM

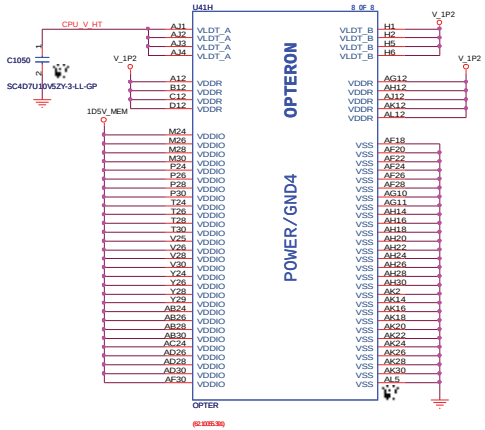
V_CPU V_CPU

V_CPU_NB V_CPU_NB









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wistron	Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title: CPU POWER/GND		
Size: K2	Document Number: Creston	Rev: SA
Date: Wednesday, August 04, 2010	Sheet 12 of 44	

CPU DECOUPLING

1D5V_MEM 1D5V_MEM

V_1P2 V_1P2

V_CPU V_CPU

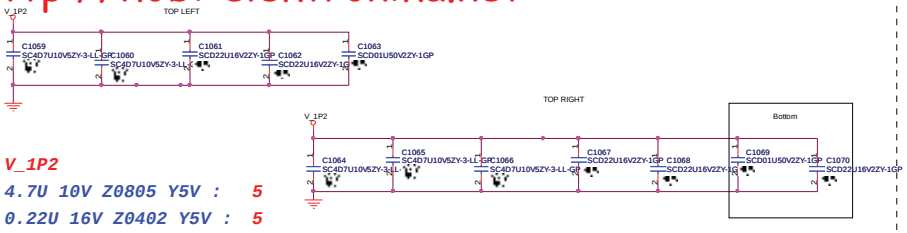
V_CPU_NB V_CPU_NB

PLACE AT CPU

V_1P2

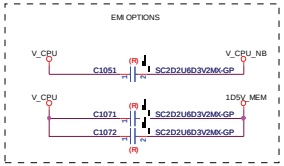
4.7U 10V Z0805 Y5V :	3
0.22U 16V Z0402 Y5V :	2
180P 50V J0402 NPO :	2

PLACE NEAR CPU SOCKET SIDES ALONG VDDR (VTT_CPU/V_1P2 COMBINED) POUR

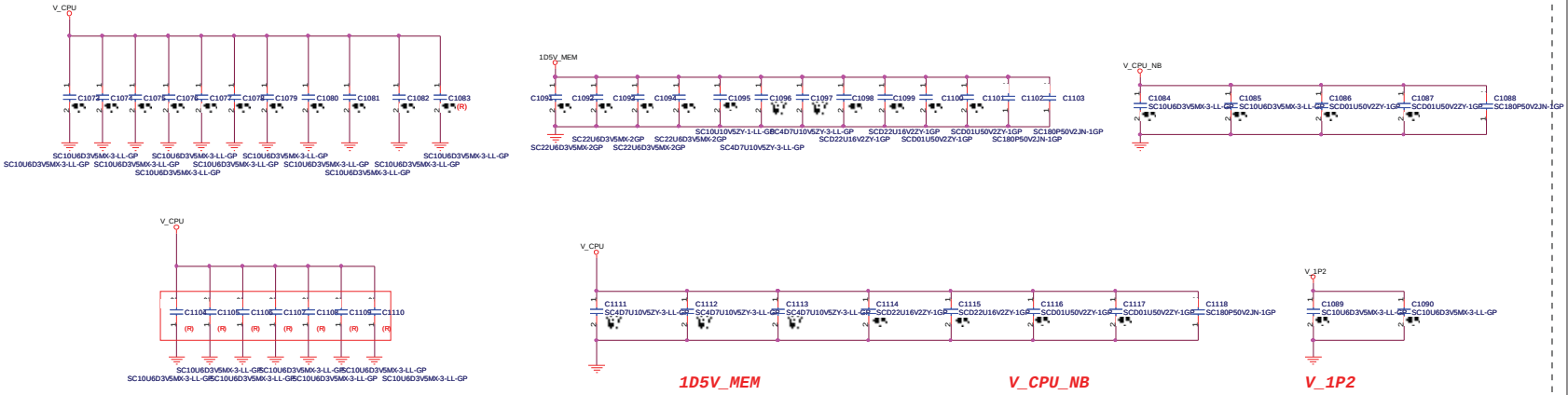


V_1P2

4.7U 10V Z0805 Y5V :	5
0.22U 16V Z0402 Y5V :	5
0.01U 50V Z0402 Y5V :	2



Under the CPU socket



V_CPU

10U 10V Z0805 Y5V :	10
4.7U 10V Z0805 Y5V :	3
0.22U 16V Z0402 Y5V :	2
0.01U 50V Z0402 Y5V :	2
180P 50V J0402 NPO :	1

1D5V_MEM

22U 6.3V M0805 X5R :	4
10U 10V Z0805 Y5V :	1
4.7U 10V Z0805 Y5V :	2
0.22U 16V Z0402 Y5V :	2
0.01U 50V Z0402 Y5V :	2
180P 50V J0402 NPO :	1

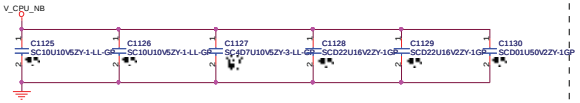
V_CPU_NB

10U 10V Z0805 Y5V :	2
0.01U 50V Z0402 Y5V :	2
180P 50V J0402 NPO :	1

V_1P2

10U 10V Z0805 Y5V : 2

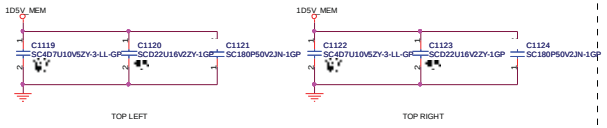
PLACE TOP SIDE CLOSE TO SOCKET



V_CPU_NB

10U 10V Z0805 Y5V :	2
4.7U 10V Z0805 Y5V :	1
0.22U 16V Z0402 Y5V :	2
0.01U 50V Z0402 Y5V :	1

PLACE BETWEEN CPU AND DIMM IN MEM_ADD FIELD



1D5V_MEM

4.7U 10V Z0805 Y5V :	2
0.22U 16V Z0402 Y5V :	2
180P 50V J0402 NPO :	2

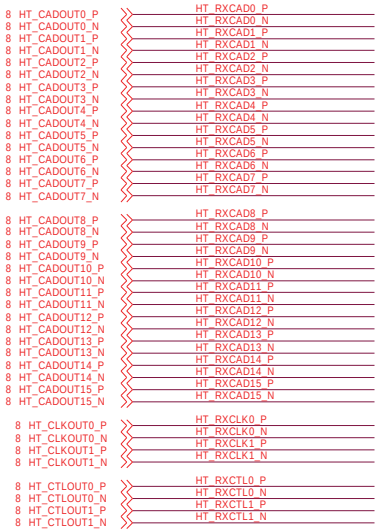
<Variant Name>

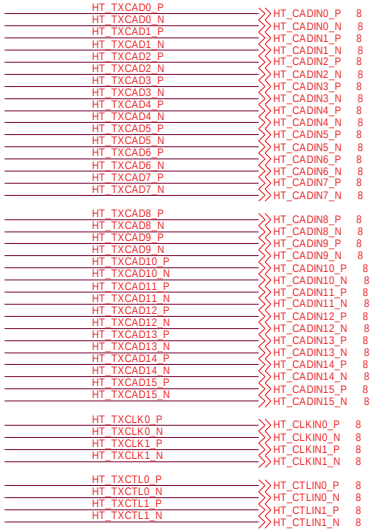
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

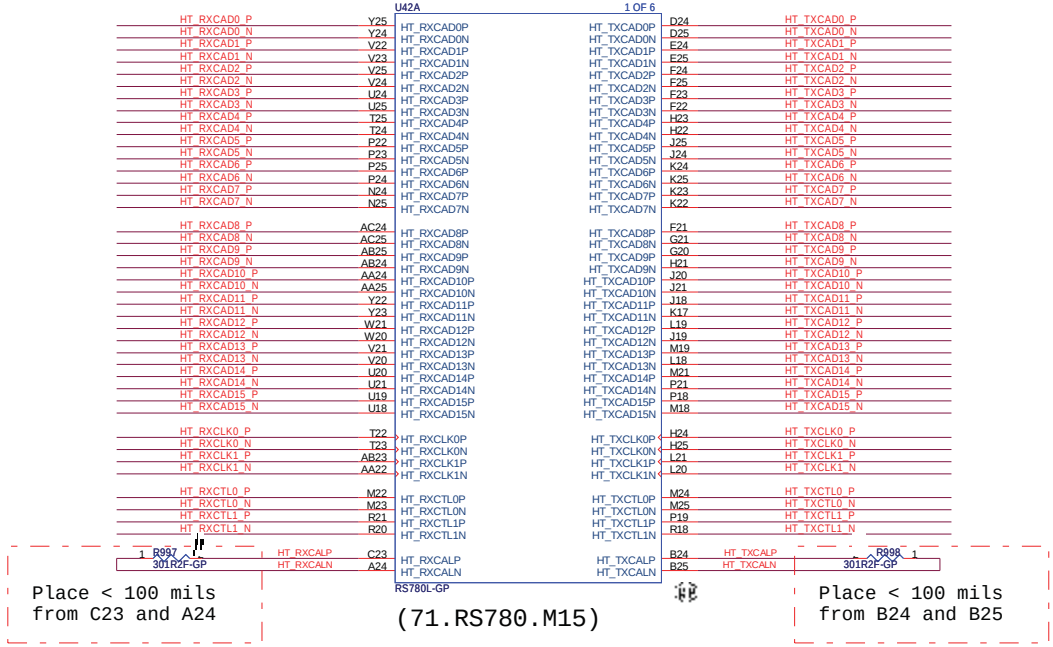
Title: CPU DECOUPLING

Size: X2 | Document Number: Creston | Rev: SA

Date: Wednesday, August 04, 2010 | Sheet 13 of 44







RX780/RS740/RS780 difference table (HT LINK)

SIGNALS	RS740	RX780	RS780
HT_RXCALP	49.9R (GND)	1.21K	301R
HT_RXCALN	49.9R (VDDHT)		
HT_TXCALP HT_TXCALN	100R	1.21K	301R

<Variant Name>

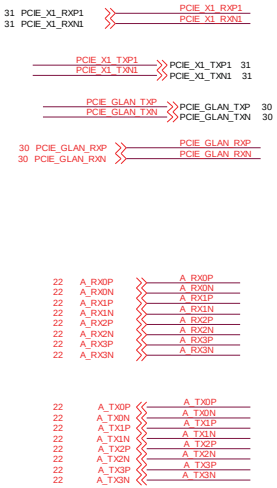
wistron

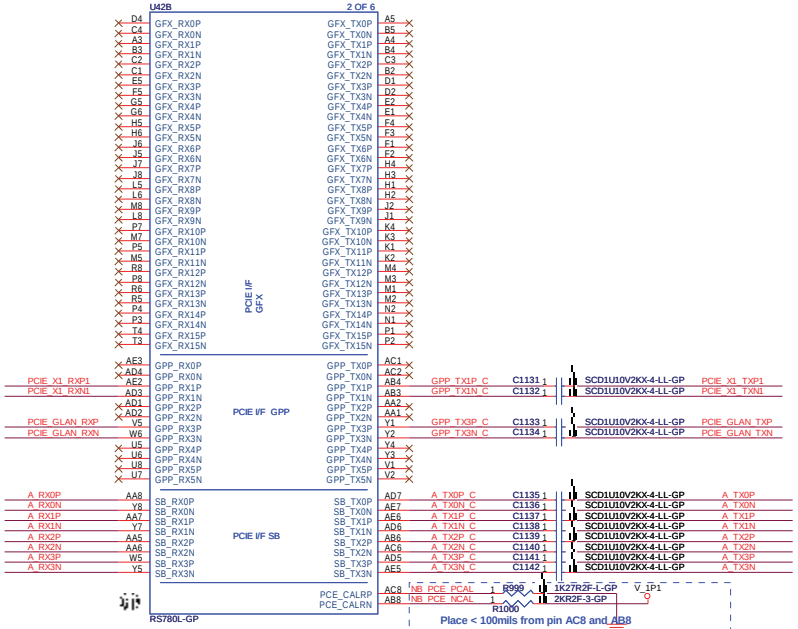
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: RS780L-HT LINK0 I/F

Size	Document Number	Rev
Custom	Creston	SA

Date: Wednesday, August 04, 2010 Sheet 14 of 44





(71.RS780.M15)

VCC_NB=VCC1D1V

RX780/RS740/RS780 GPP difference table

	RS740	RS780
PCE_CALRP	562R (GND)	1.27K (GND)
GPP4	NC	GPP4
GPP5	NC	GPP5

RS780 **RS740/RS780 GPP Routing table**

GPP1	RS740	
GPP X1 CONNECTOR	GPP1	
GIGABIT ETHERNET	GPP3	

RS780 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

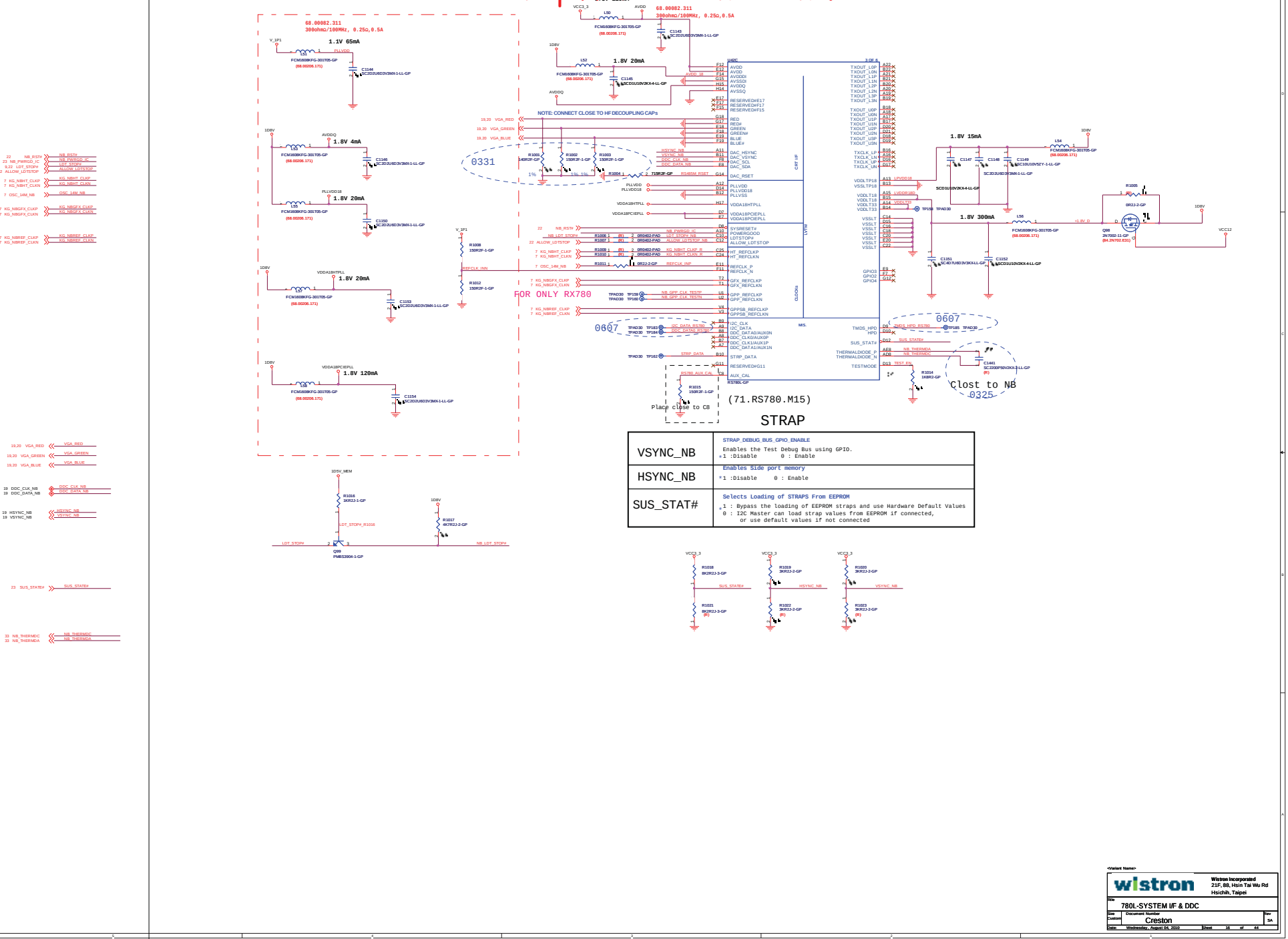
<Variant Name>

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: RS780L-PCIE LINK I/F

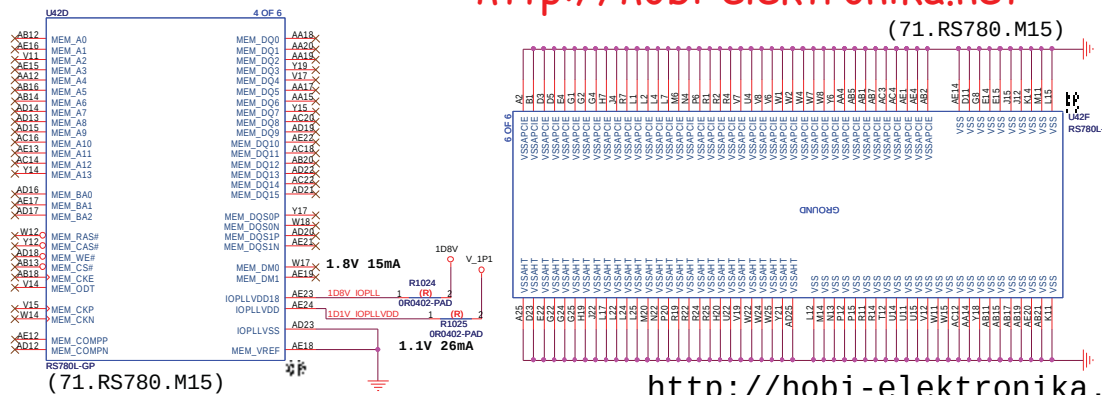
Size: Custom | Document Number: Creston | Rev: SA

Date: Wednesday, August 04, 2010 | Sheet 15 of 44



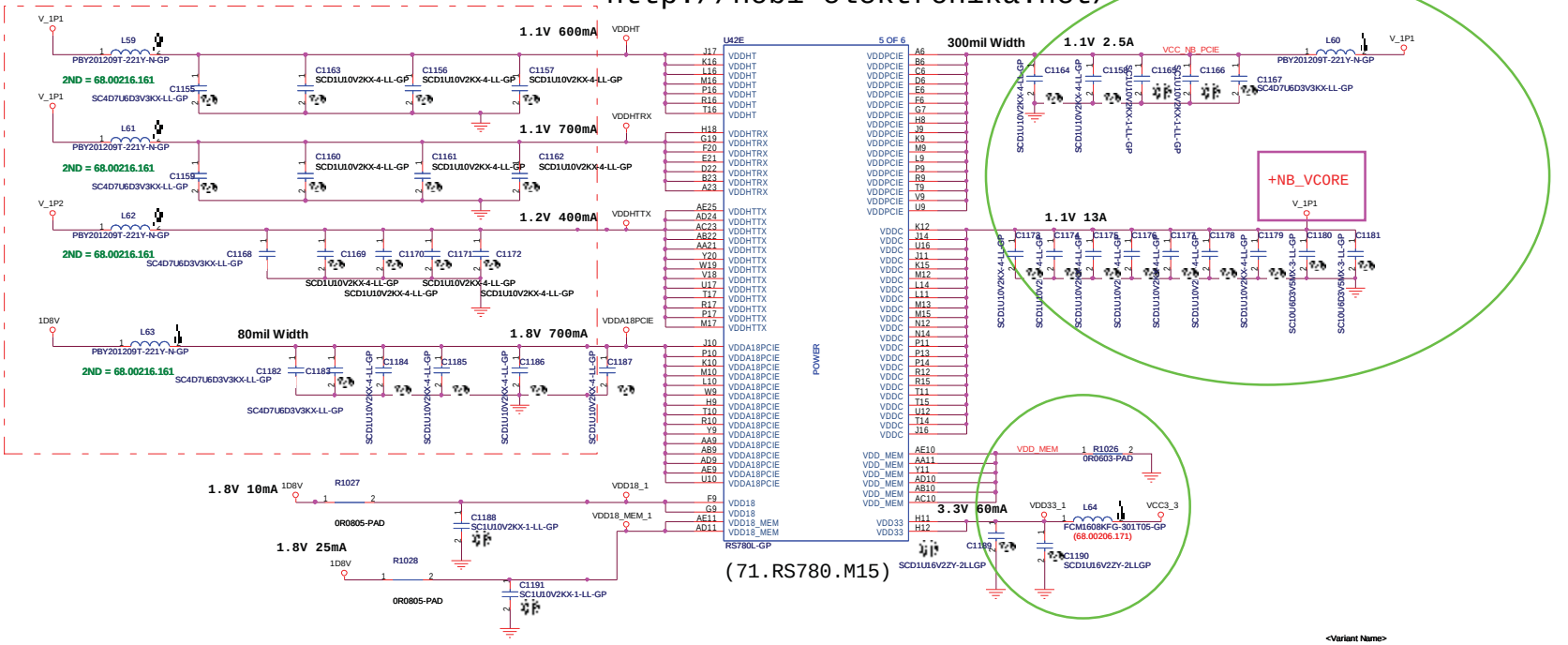
VSYNC_NB	STRAP_DEBUG_BUS_GPIO_ENABLE Enables the Test Debug Bus using GPIO. *1 :Disable 0 : Enable
HSYNC_NB	Enables Side port memory *1 :Disable 0 : Enable
SUS_STAT#	Selects Loading of STRAPS From EEPROM *1 : Bypass the loading of EEPROM straps and use Hardware Default Values 0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

Wistron	Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title	780L-SYSTEM I/F & DDC
Size: Custom	Document Number: Creston
Rev	SA
Date:	Wednesday, August 04, 2010
Sheet	16 of 44



RS740/RX780/RS780 POWER DIFFERENCE TABLE

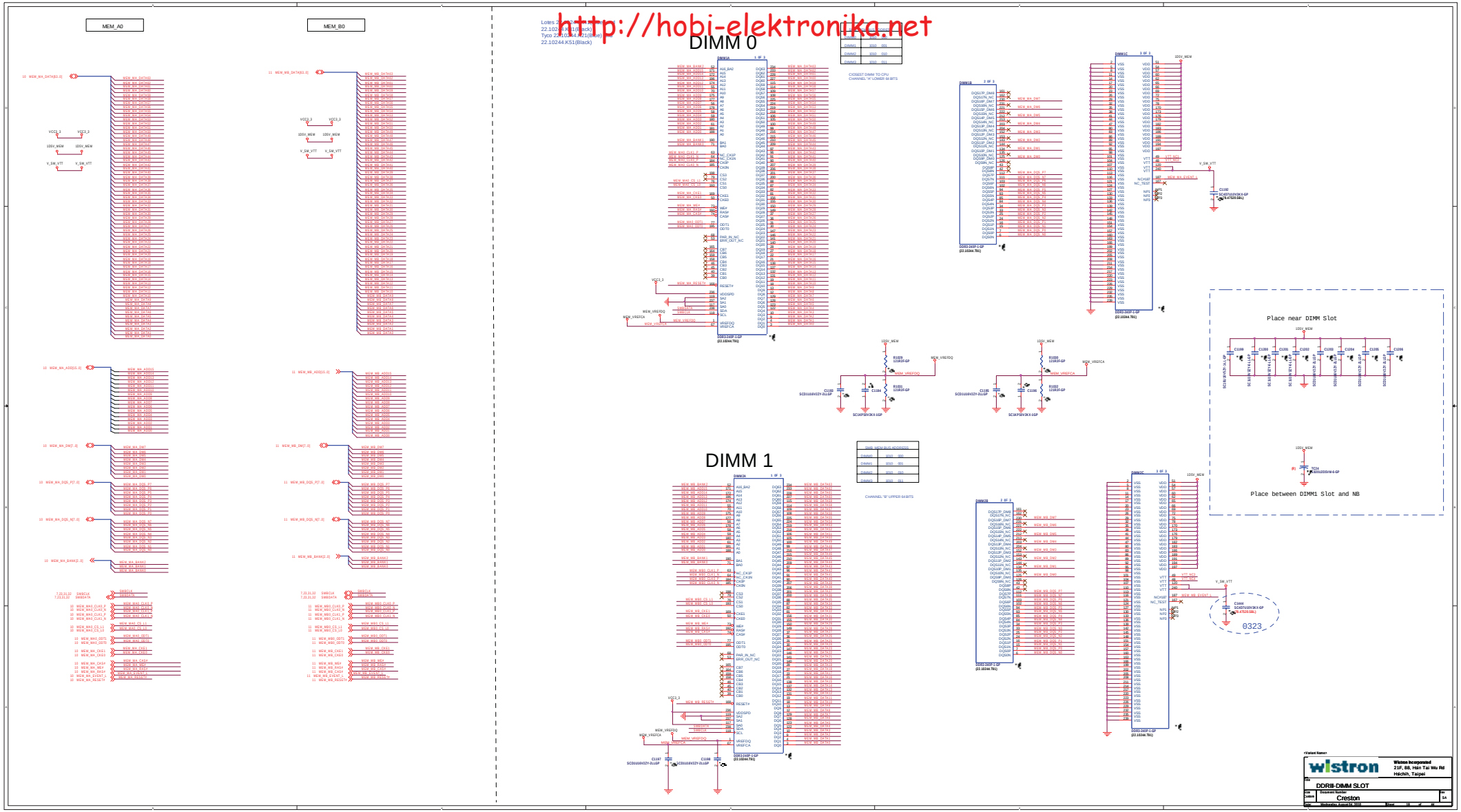
PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVDD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVDD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVDD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V	NC	+1.8V(DDR2) +1.5V(DDR3)	VDDLTP18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDLT18	+1.8V	NC	+1.8V
IOPLLVDD18	+1.8V	NC	+1.8V	VDDLT33	+3.3V	NC	NC



<Variant Name>

wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: RS780L-POWER
Size: Custom
Document Number: Creston
Rev: SA
Date: Wednesday, August 04, 2010
Sheet 17 of 44



From NB

16 HSYNC_NB
16 VSYNC_NB
HSYNC_NB
VSYNC_NB

16 DDC_CLK_NB
16 DDC_DATA_NB
DDC_CLK_NB
DDC_DATA_NB

16,20 VGA_RED
16,20 VGA_GREEN
16,20 VGA_BLUE
VGA_RED
VGA_GREEN
VGA_BLUE

To SCALAR

20 DDC_CLK_VGA
20 DDC_DATA_VGA
20 VSYNC_5V_CON
20 HSYNC_5V_CON
DDC_CLK_VGA
DDC_DATA_VGA
VSYNC_5V_CON
HSYNC_5V_CON

16,20 RED_CONN
16,20 GREEN_CONN
16,20 BLUE_CONN
RED_CONN
GREEN_CONN
BLUE_CONN

HSYNC_NB 1 2 HSYNC_5V_CON
R114 (R) 0R0402-PAD

VSYNC_NB 1 2 VSYNC_5V_CON
R120 (R) 0R0402-PAD

VGA_RED → RED_CONN
VGA_GREEN → GREEN_CONN
VGA_BLUE → BLUE_CONN

0331

R122 150R2F-1-GP 1%
R127 150R2F-1-GP 1%
R133 140R2F-GP 1%

VCC3_3
R1396 10KR2J-3-GP
DDC_CLK_NB → S
D → DDC_CLK_VGA
Q16 2N7002-11-GP
G

VCC3_3
R1397 10KR2J-3-GP
DDC_DATA_NB → S
D → DDC_DATA_VGA
Q19 2N7002-11-GP
G

0405

VCC3_3
R139 1KR2J-1-GP
ISP_EN_N

C87 SCD1U16V2ZY-2GP

CRT1 (X)
ISP_EN_N 2 → 1
RED_CONN 6 → 5 DDC_CLK_VGA
GREEN_CONN 8 → 7 DDC_DATA_VGA
BLUE_CONN 10 → 9 VSYNC_5V_CON
12 → 11 HSYNC_5V_CON
4 → 3
DVD-CONN12D-FP1-GP

21.62698.206,
11pin -1#3,
2.0mm pitch

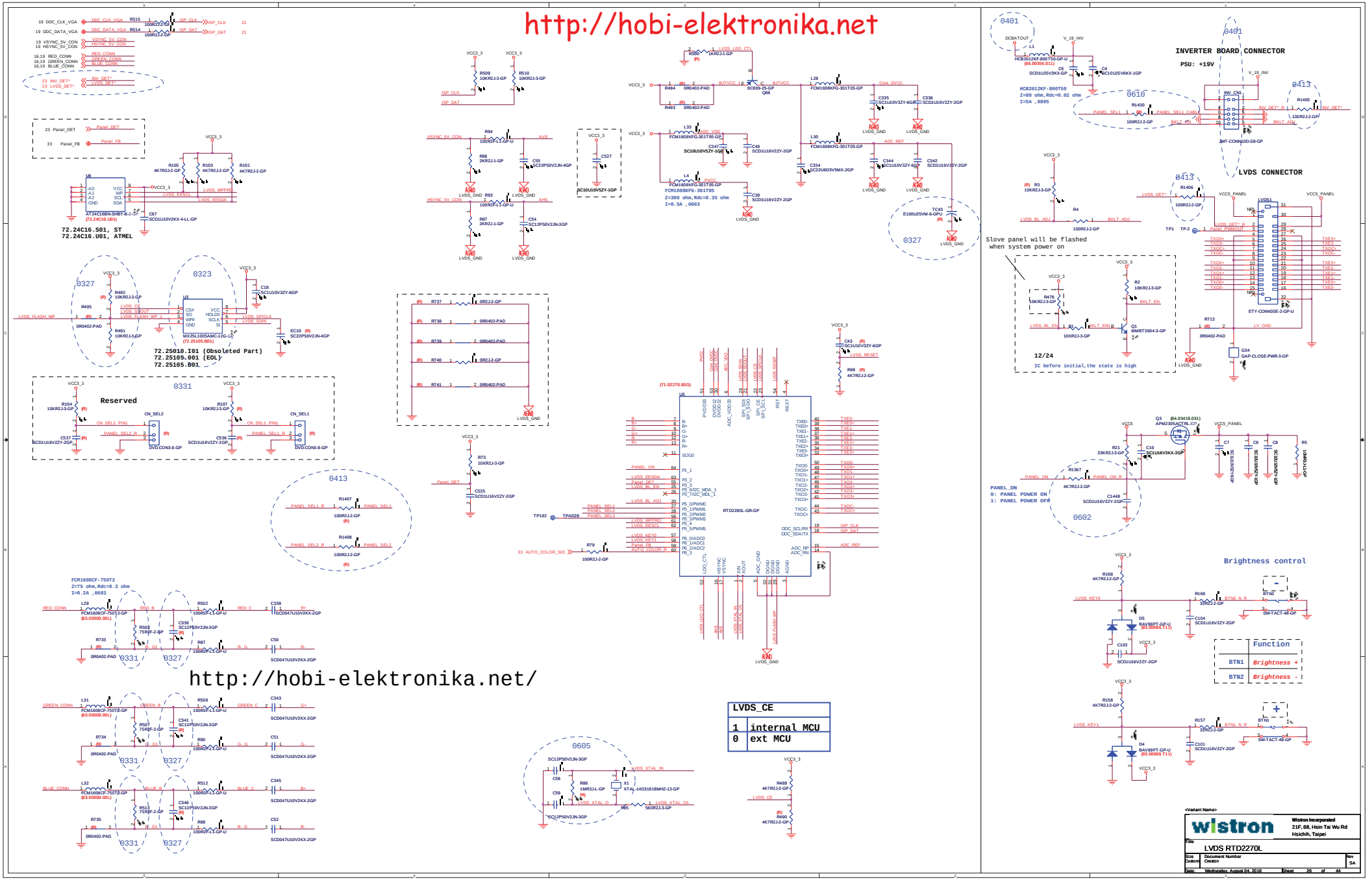
<Variant Name>

wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: VGA CONNECTOR

Size	Document Number	Rev
A	Creston	SA

Date: Wednesday, August 04, 2010 Sheet 19 of 44



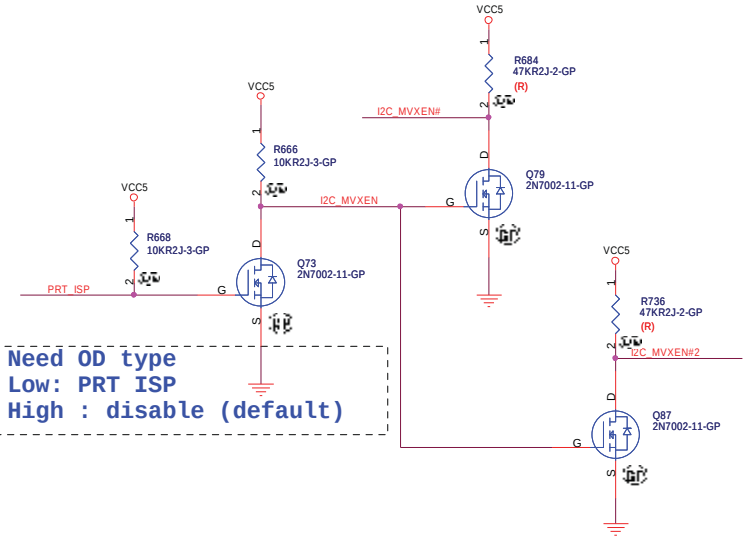
PARALLEL PORT

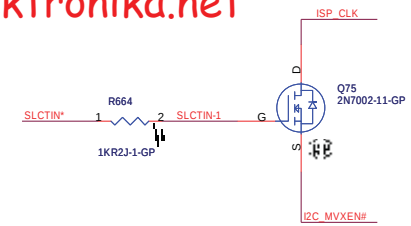
33 ERRORP* — ERRORP*
33 SLCTIN* — SLCTIN*

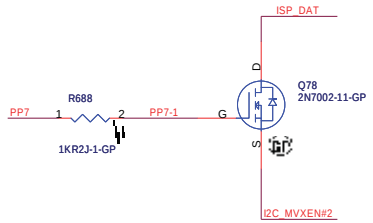
33 BUSYP — BUSYP
33 PP7 — PP7

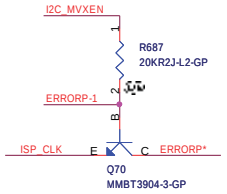
33 SLCT — SLCT
33 PACK* — PACK*

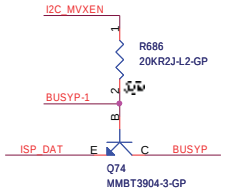
33 PRT_ISP — PRT_ISP
20 ISP_CLK — ISP_CLK
20 ISP_DAT — ISP_DAT

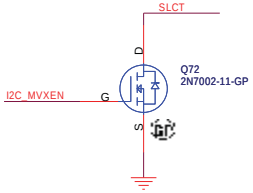


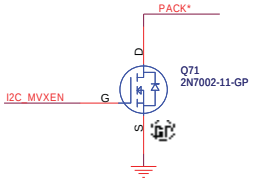


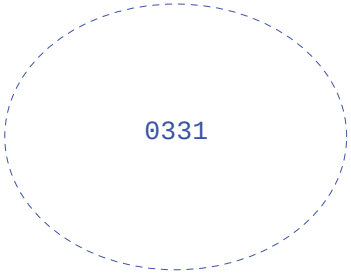












<Variant Name>

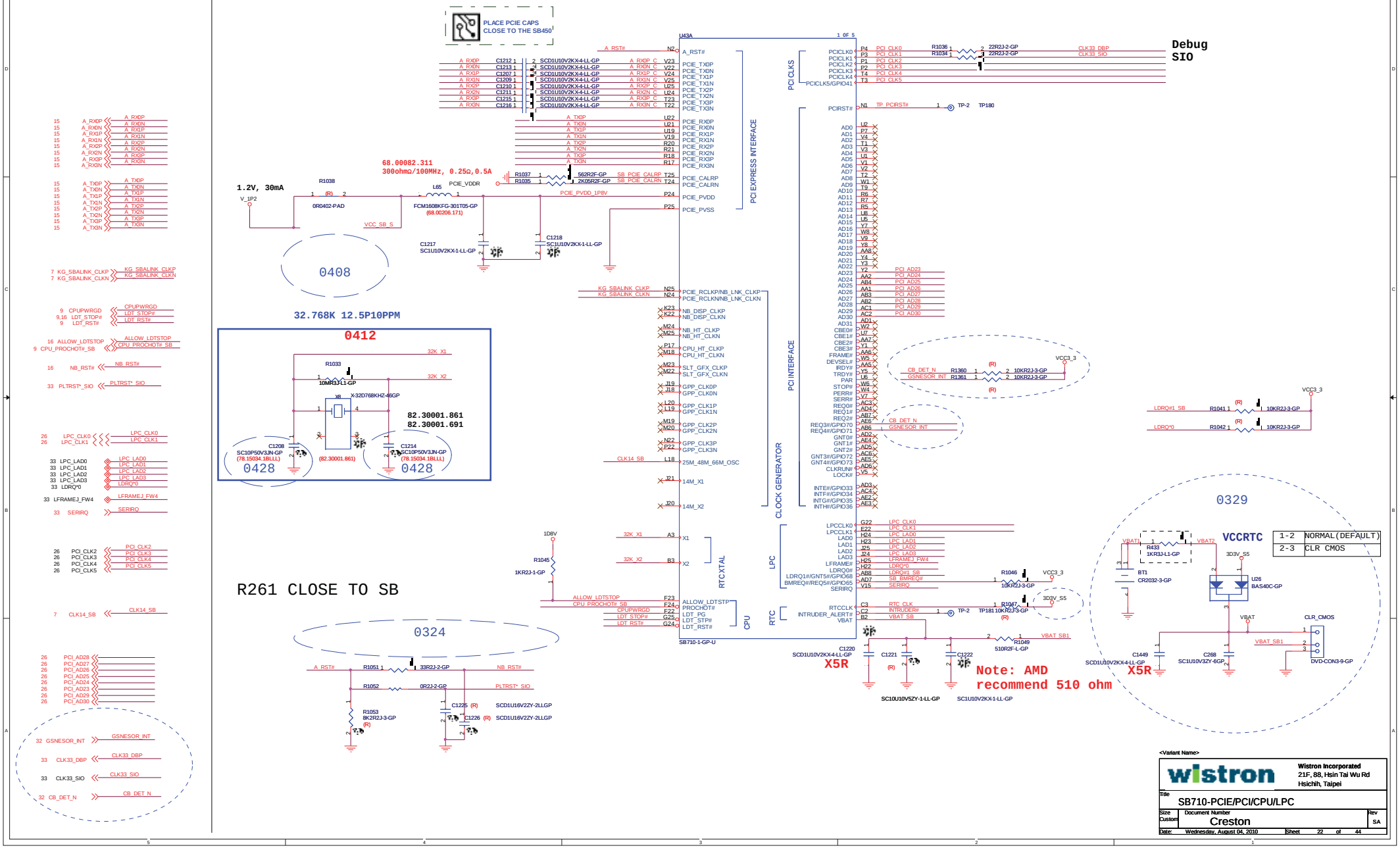
wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

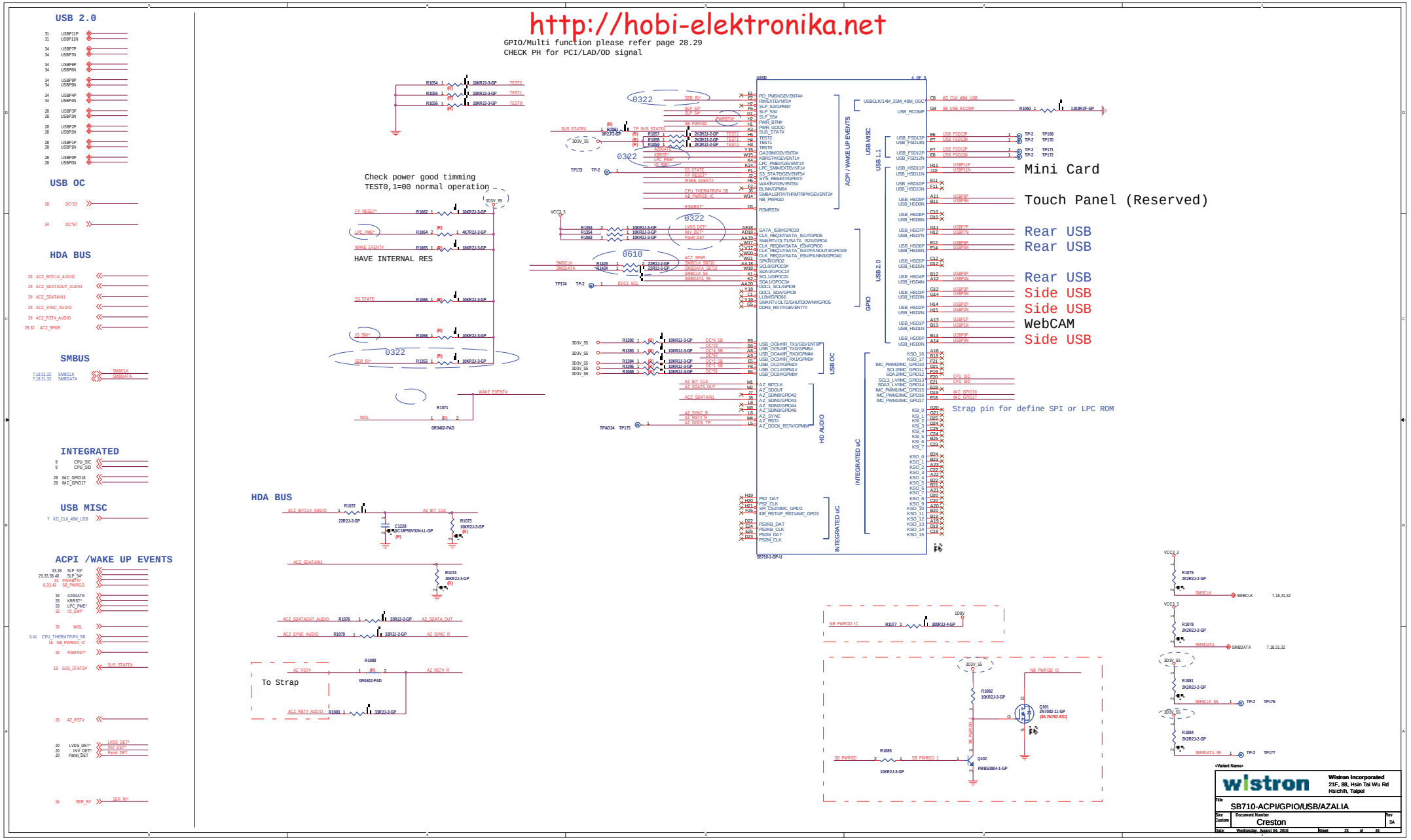
Title: PRT and SMBUS ISP

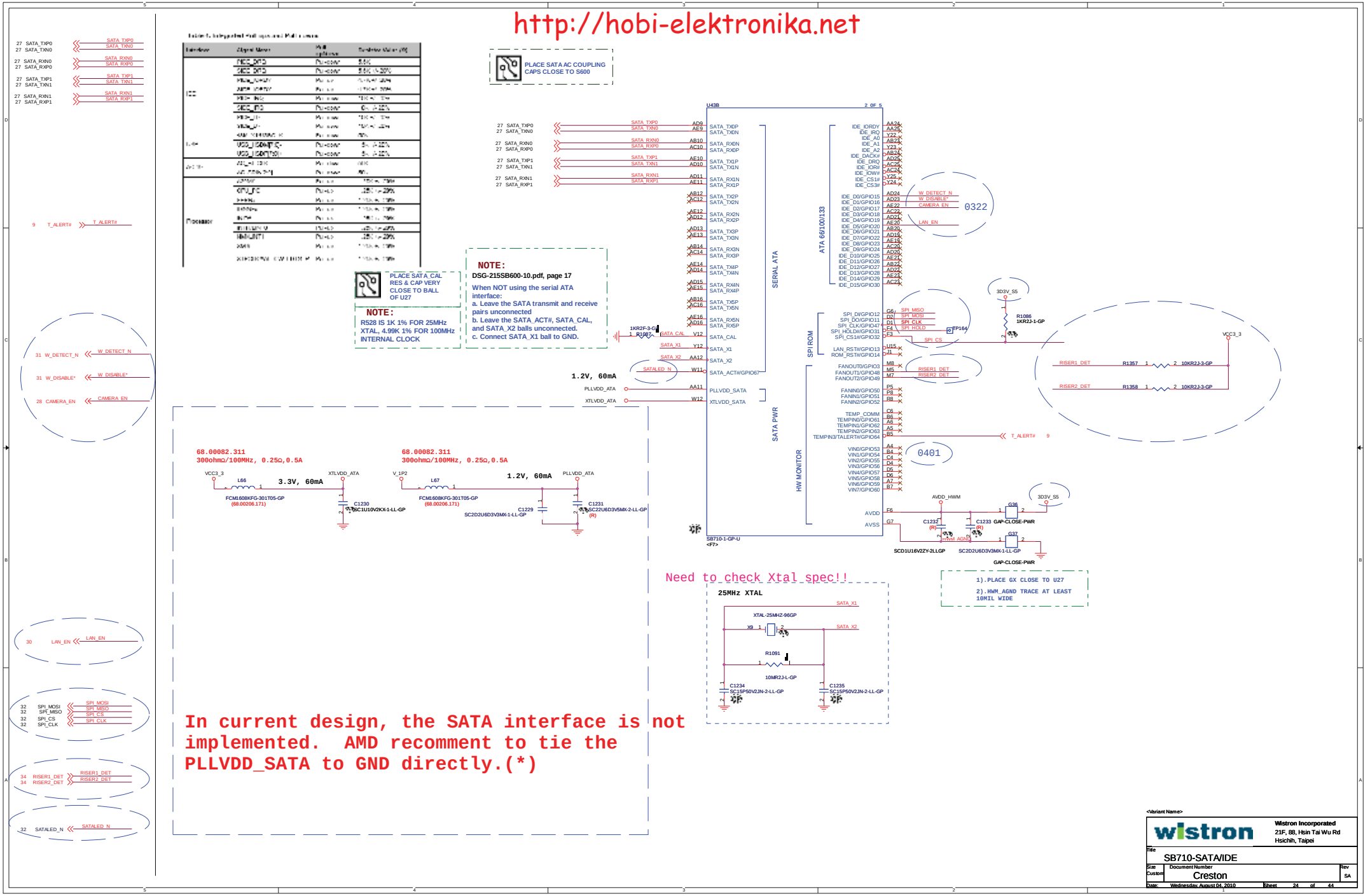
Size	Document Number	Rev
A3	Creston	SA

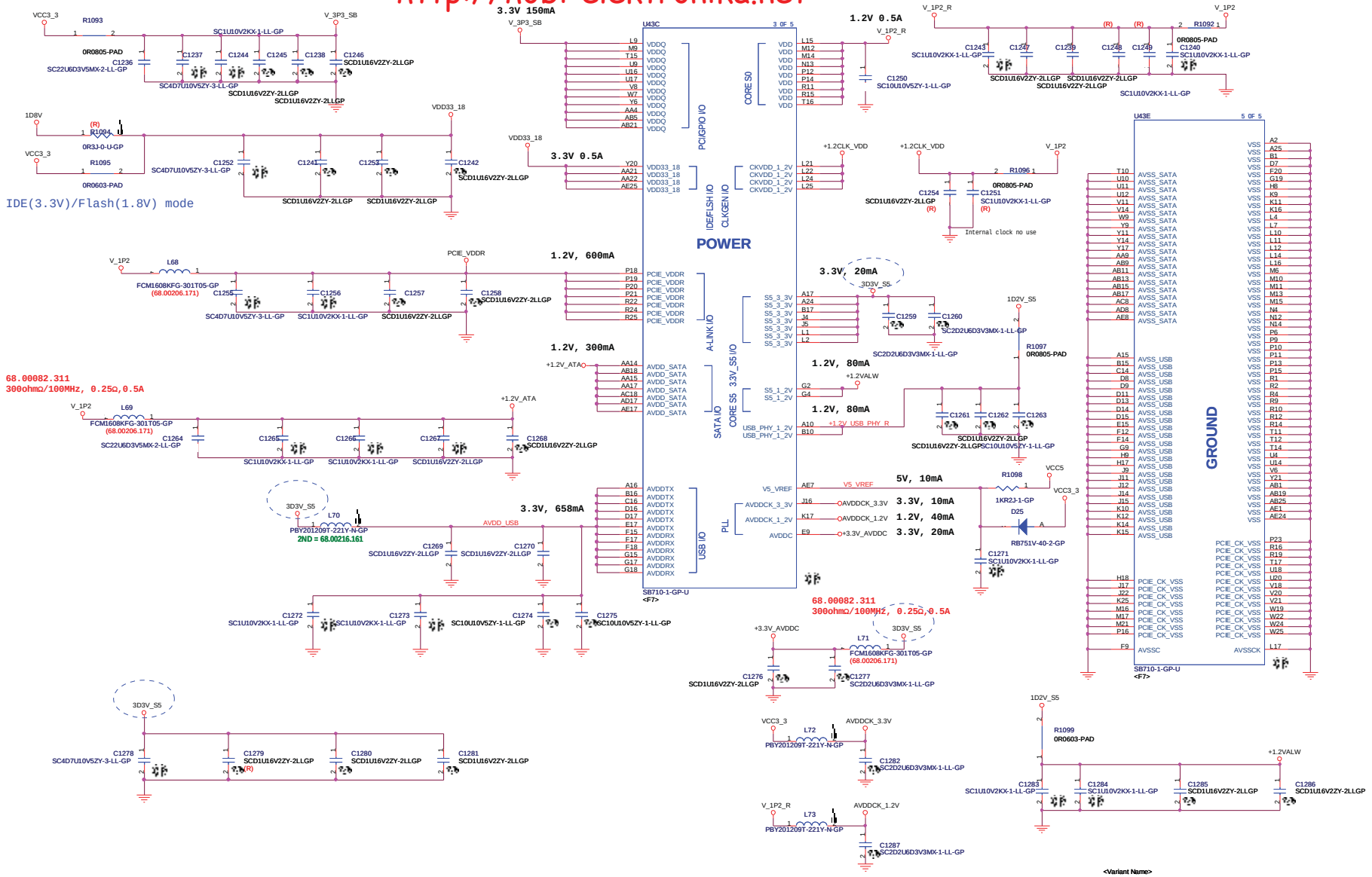
Date: Wednesday, August 04, 2010 Sheet 21 of 44



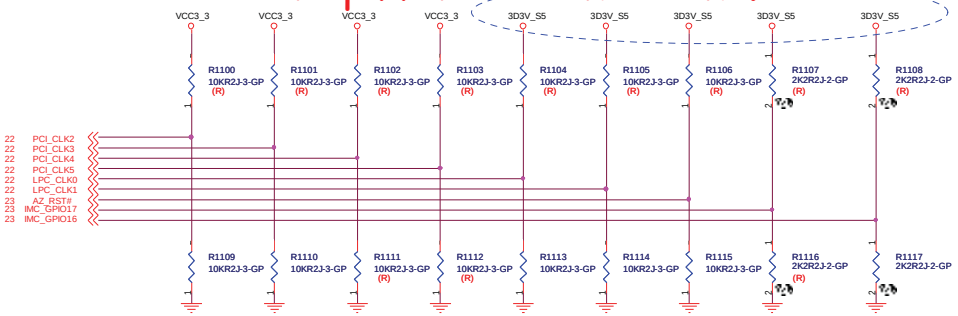
GPIO/Multi function please refer page 28.29
CHECK PH for PCI/LAD/OD signal







NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK



REQUIRED STRAPS

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	AZ_RST#	IMC_GPIO17 IMC_GPIO16
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	IMC ENABLED	ROM TYPE: H, H = Reserved NC, L = SPI ROM DEFAULT
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	IMC DISABLED DEFAULT	L, H = LPC ROM L, L = FWH ROM

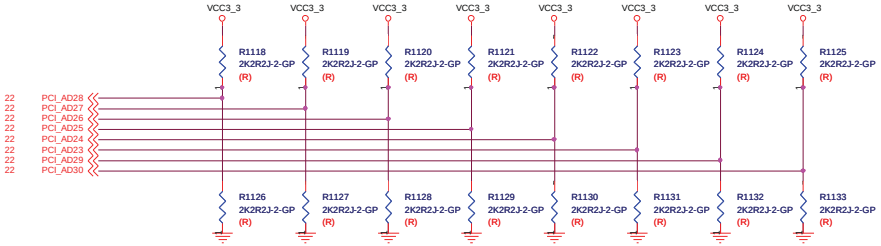
22 PCI_CLK2
22 PCI_CLK3
22 PCI_CLK4
22 PCI_CLK5
22 LPC_CLK0
22 LPC_CLK1
23 AZ_RST#
23 IMC_GPIO17
23 IMC_GPIO16

22 PCI_AD28
22 PCI_AD27
22 PCI_AD26
22 PCI_AD25
22 PCI_AD24
22 PCI_AD23
22 PCI_AD29
22 PCI_AD30

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[30:23]



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD29 PCI_AD30
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOTFAILTIMER DISABLED DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED	

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: SB710 STRAPS

Size: Custom | Document Number: Creston | Rev: SA

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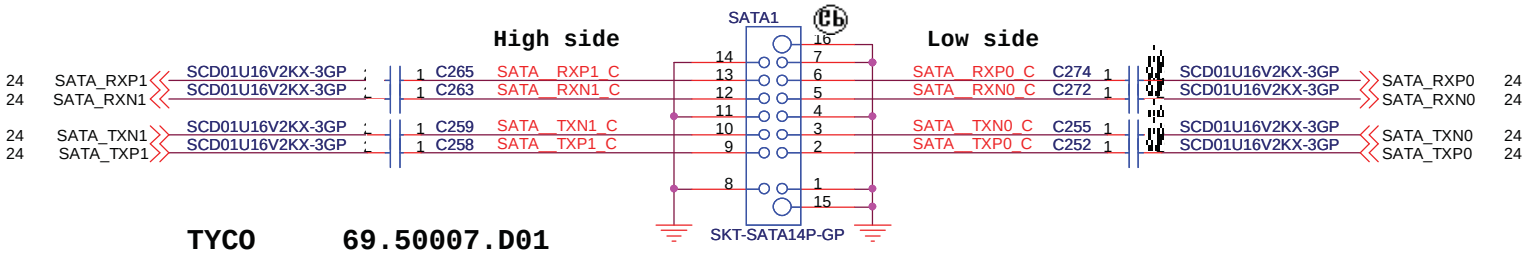
SATA CONNECTORS

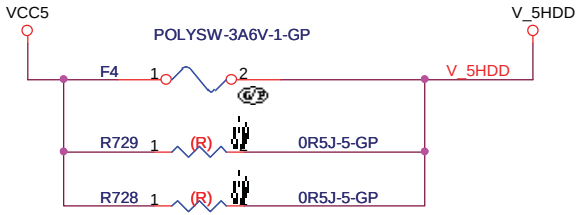
SATA 2Port Right angle : 20.81227.014, 20.81228.014

AMPHENOL 22.10321.A91
KORTAK 22.10300.981

(22.10321.A91)

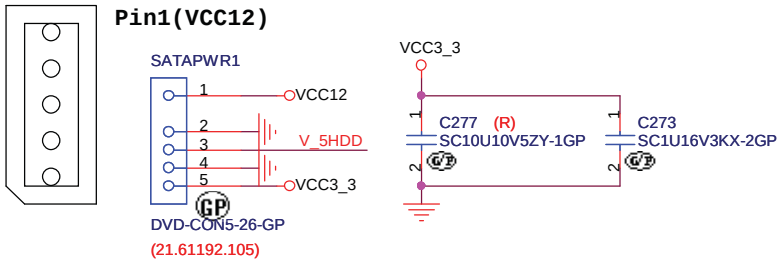


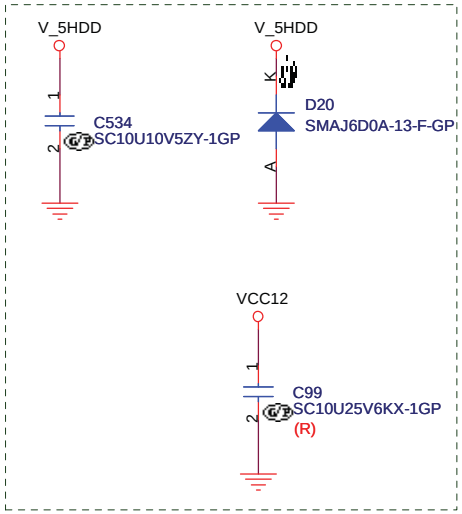
TYCO 69.50007.D01
EVERFUSE 69.50007.B71

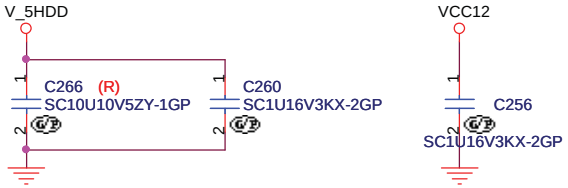


0317

Layout: Please put them together







<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	SATA CONN	
Size A4	Document Number Creston	Rev SA
Date: Wednesday, August 04, 2010	Sheet 27 of 44	

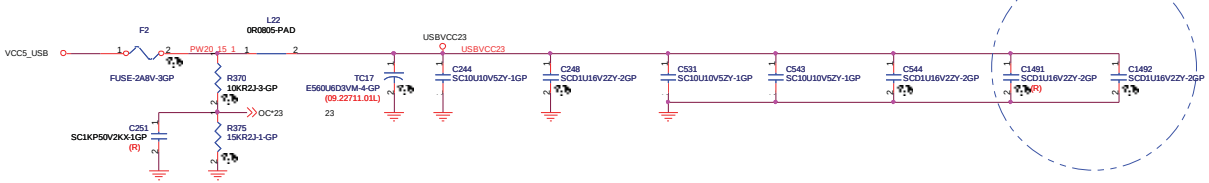
Side USB are Port 2,3,5
Rear USB are Port 4,6,7
Internal USB, Port 1 for Camera
Internal USB, Port 11 is for Mini PCIE slot
Internal USB, Port 0 is for Touch Panel

0331

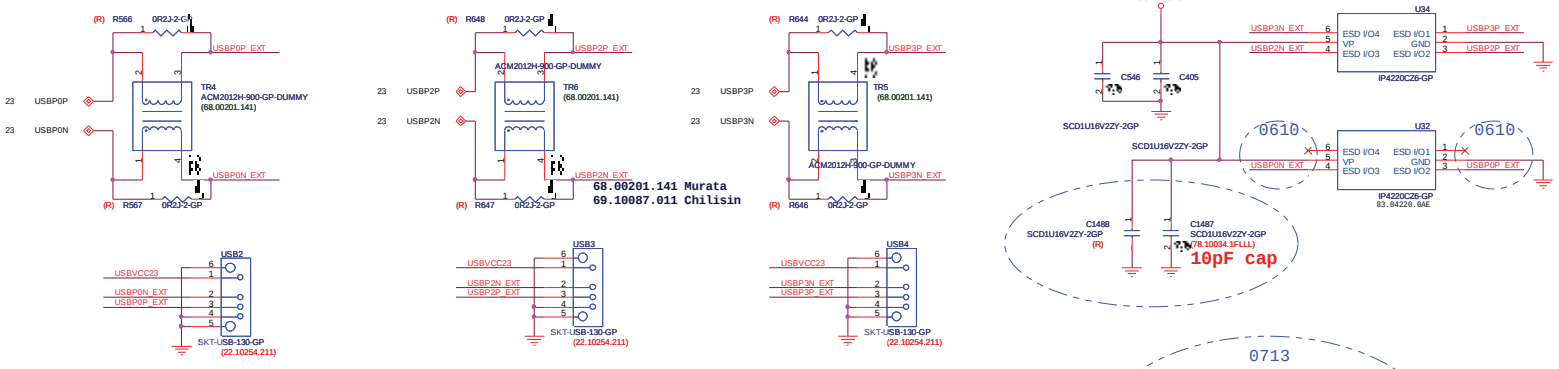
SIDE USB PORT (2/3/5)

0331

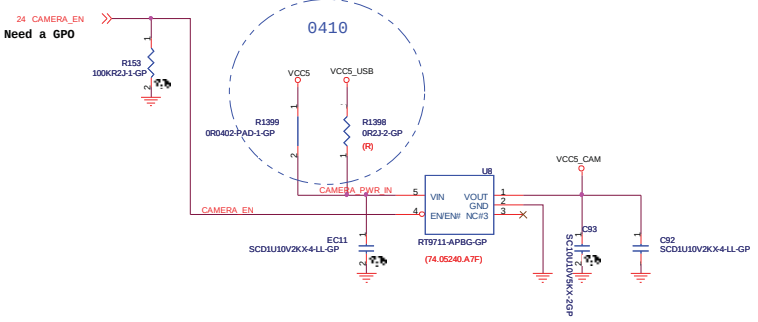
0622

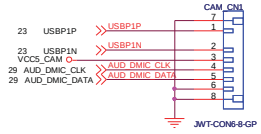


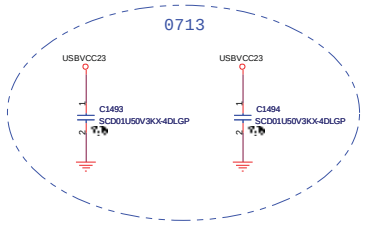
CLOSED TO USB CONNECTOR

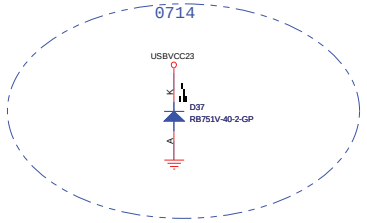


INTERNAL USB PORT (1)
for Camera, Digital Mic









<Variant Name>

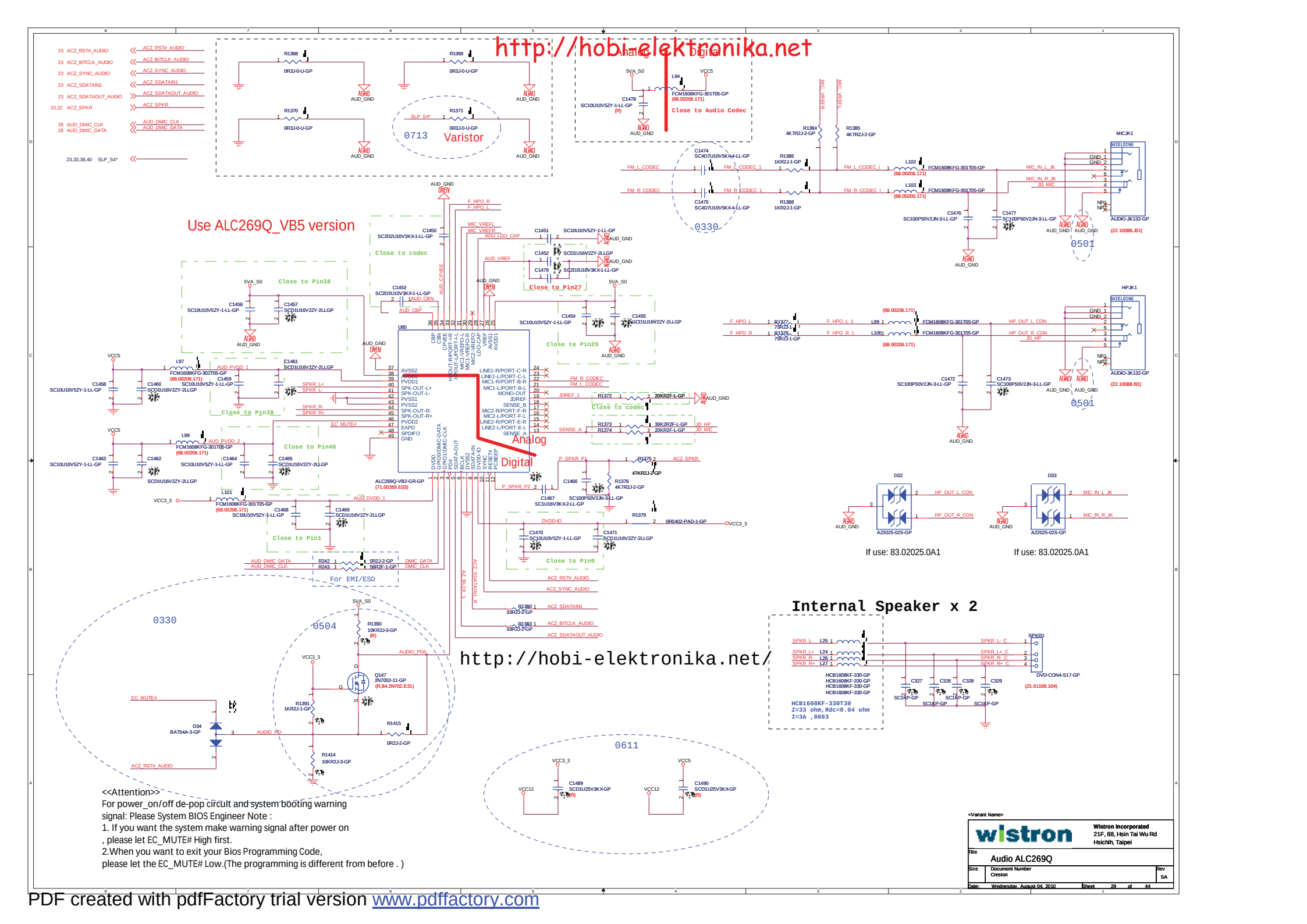
wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: USB CONN

Size: C | Document Number: Creston | Rev: SA

Date: Wednesday, August 04, 2010 | Sheet 28 of 44



<<Attention>>
For power_on/off de-pop circuit and system booting warning signal: Please System BIOS Engineer Note :
1. If you want the system make warning signal after power on , please let EC_MUTE# High first.
2.When you want to exit your Bios Programming Code, please let the EC_MUTE# Low.(The programming is different from before .)

<Variant Name>
wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title: Audio ALC269Q
Size: Document Number: Creston
Rev: SA
Date: Wednesday, August 04, 2010
Sheet 29 of 44

Link to NB

15 PCIE_GLAN_RXP → PCIE_GLAN_RXP
15 PCIE_GLAN_RXN → PCIE_GLAN_RXN
15 PCIE_GLAN_TXP → PCIE_GLAN_TXP
15 PCIE_GLAN_TXN → PCIE_GLAN_TXN
23 WOL → WOL

C295 SCD1U10V2KX-4-LL-GP: PCIE_LAN_TXP3_ICH
C290 SCD1U10V2KX-4-LL-GP: PCIE_LAN_TXN3_ICH

Close LAN Chip

Link to RJ45(RISER1)

34 TRD0N ↔ TRD0N
34 TRD0P ↔ TRD0P
34 TRD1N ↔ TRD1N
34 TRD1P ↔ TRD1P
34 TRD2N ↔ TRD2N
34 TRD2P ↔ TRD2P
34 TRD3N ↔ TRD3N
34 TRD3P ↔ TRD3P
34 LINK*_ACTIVITY_L ↔ LINK*_ACTIVITY_L
34 LANLED_G ↔ LANLED_G
34 LANLED_O ↔ LANLED_O

Link to Clock gen

7 CLKSRC_PE1X_LAN → CLKSRC_PE1X_LAN
7 CLKSRC_PE1X_LAN* → CLKSRC_PE1X_LAN*

Link to SIO

33 PLTRST*_LAN → PLTRST*_LAN

Link to SB

24 LAN_EN → LAN_EN

25MHZ XTAL

18P / 20PPM

X4 XTAL-25MHZ-57GP
LAN_XTALO, LAN_XTALI
R443 (R) 1MR3J-1-GP
C305 SC27P50V2JN-2-GP
C296 SC27P50V2JN-2-GP

EEPROM for RTL8111DL

72.93C46.R01
72.93C46.N01

U23 (R) M93C46-WMN6TP-GP
LAN_EECS, LAN_EESK, LAN_EEDI, LAN_EEDO
V_3P3_LAN
C270 SC1U10V3ZY-6GP

Need to check F/W.

LAN_EEDI — R392 3KK6R2J-GP — V_3P3_LAN

Default Value of LEDS1,0 = 11

DCBATOUT / 3D3V_S5

R430 100KR2J-1-GP (R)
Q55 AO3418-GP
LAN_EN_2
LAN_EN → R445 1KR2J-1-GP (R) → LAN_EN_1
Q59 MMBT3904-3-GP
C294 SCD1U16V2KX-3GP (R)
R431 100KR2J-1-GP (R)
V_3P3_LAN

V_3P3_LAN Rising Time need during 1ms ~ 100ms.

X5R

3D3V_S5 → R424 0R0805-PAD (R) → V_3P3_LAN
V_3P3_LAN → R663 0R0603-PAD → LAN_DDSR

0329
C289 SC4D7U10V5ZY-3GP
C504 SCD1U16V2ZY-2GP
C498 SCD1U16V2ZY-2GP
C503 SCD1U16V2ZY-2GP
C512 SCD1U16V2ZY-2GP
C509 SCD1U25V3KX-GP
C508 SC22U06D3V5MX-2GP

Close to RTL8111DL
Pin1, 29, 37, 40.

IDC=1.3A
Tolerance=+-20
DCR=144m ohm

R660 0R0402-PAD (R) → R658 0R2J-2-GP → GND

Pin43:
High, 1.2VLDO Enable
Low, Disabled

R447 2K49R2F-GP

MAGIC 68.4R710.20N
MAGLAYERS 68.4R71D.10K

Trace >100mil width

Close to Pin 19.

0410
V_1P2_LAN_E → C300 SC1U10V3ZY-6GP, C306 SC1U10V3ZY-6GP
V_1P2_LAN → C518 SCD1U16V2ZY-2GP
C520 SC2U6D3V5MX-2GP
L23 COIL-4D7UH-13-GP (68.4R710.20N)
LAN_1P2_OUT

Close to RTL8111DL
Pin10, 13, 30, 36, 39.

0331
C514 C517 C292 C496 C1480 — SCD1U25V3KX-GP

R682 0R0402-PAD (R) V_1P2_LAN_FB → V_1P2_LAN

U29 RTL8111DL-GR-GP

1 AVDD33
2 MDIP0
3 MDIN0
4 NC/FB12
5 MDIP1
6 MDIN1
7 GND
8 NC/MDIP2
9 NC/MDIN2
10 DVDD12/AVDD12
11 NC/MDIP3
12 NC/MDIN3
13 DVDD12
14 GND
15 HSIP
16 HSIN
17 REFCLK_P
18 REFCLK_N
19 VDDTX/EVDD12
20 HSOP
21 HSON
22 EGND
23 NC/GPO
24 NC/NC
25 LANWAKEB
26 PERSTB
27 ISOLATEB
28 CLKREQB
29 VDD33
30 DVDD12
31 GND
32 EECS
33 LED3/EEDO
34 LED2/EEDI
35 LED1/EESK
36 DVDD12
37 LED0
38 NC/LV_PLL
39 NC/AVDD33
40 LAN_XTALO
41 LAN_XTALI
42 CKTAL2
43 NC/ENSWREG
44 NC/VDDSR
45 VCTR12DVDDSR
46 RSET
47 GND
48 VCTR12AVSROUT12

V_3P3_LAN, V_1P2_LAN, LINK*_ACTIVITY_L
LAN_RSET, LAN_DDSR, LAN_DDSR, LAN_VDD33, LAN_XTALO, LAN_XTALI

TRD0P, TRD0N, V_1P2_LAN_FB, TRD1P, TRD1N, GND, TRD2P, TRD2N, TRD3P, TRD3N

LAN_EESK — R415 0R0402-PAD — SPEED_100*_L
LAN_EEDI — R416 0R0402-PAD — SPEED_10*_L
LAN_EEDO — R417 0R0402-PAD — SPEED_1000*_L
LAN_EECS
RTL_ISOLATE_N
PLTRST*_LAN
WOL
LAN_CLKREQ_N

From SIO PCIRST_OUT2

R655 (R) 10KR2J-3-GP → V_3P3_LAN

NC_LAN_24, NC_LAN_23

PCIE_GLAN_TXP, PCIE_GLAN_TXN, CLKSRC_PE1X_LAN, CLKSRC_PE1X_LAN*, PCIE_LAN_TXP3_ICH, PCIE_LAN_TXN3_ICH

V_1P2_LAN_E

	SPEED_10*_L	SPEED_100*_L	SPEED_100*_L
10Mbps	L	H	H
100Mbps	H	L	H
1000Mbps	H	H	L

LED circuit

V_3P3_LAN → R651 10KR2J-3-GP (R) → LANLED_G
SPEED_100*_L
0317
D16 BAT54A-3-GP (R)
SPEED_10*_L
R694 (R) 0R0402-PAD
R649 (R) 10KR2J-3-GP
SPEED_1000*_L → LANLED_O

VCC3_3

R650 1KR2J-1-GP
RTL_ISOLATE_N
R653 15KR2J-1-GP

In layout
1. The trace of Pin48 shell be within 200mil.
2. The trace of Pin44,45 must be within 40mil.

<Variant Name>

wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Gb LAN RTL8111DL
Size: A3
Document Number: Creston
Rev: SA
Date: Wednesday, August 04, 2010
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Mini PCIE slot 1

INTERNAL USB PORT (0)
for Mini PCIE

24 W_DISABLE* → W_DISABLE*
24 W_DETECT_N → W_DETECT_N

0328
1D5V_S0

Please close to MPE1.

C269 SCD1U16V2ZY-2GP
C286 SCD1U16V2ZY-2GP
C322 SC10U10V5ZY-1GP

VCC3_3

Please close to MPE1.

C495 SCD1U16V2ZY-2GP
C492 SCD1U16V2ZY-2GP
C262 SC10U10V5ZY-1GP
C324 SC10U10V5ZY-1GP

23 USBP11P
23 USBP11N

33 PLTRST*_RISER → PLTRST*_RISER

7 CLKSRC_PE1X_SL1 → CLKSRC_PE1X_SL1
7 CLKSRC_PE1X_SL1* → CLKSRC_PE1X_SL1*

15 PCIE_X1_RXN1 → PCIE_X1_RXN1
15 PCIE_X1_RXP1 → PCIE_X1_RXP1

15 PCIE_X1_TXN1 → PCIE_X1_TXN1
15 PCIE_X1_TXP1 → PCIE_X1_TXP1

7,18,23,32 SMBCLK → SMBCLK
7,18,23,32 SMBDATA → SMBDATA

0328
1D5V_S0

MPE1

6	1.5V	REFCLK+	13 CLKSRC_PE1X_SL1
2	3.3V	REFCLK-	11 CLKSRC_PE1X_SL1*
28	+1.5V	PERN0	23 PCIE_X1_RXN1
48	+1.5V	PERP0	25 PCIE_X1_RXP1
52	+3.3V	PETN0	31 PCIE_X1_TXN1
24	+3.3VAUX	PETP0	33 PCIE_X1_TXP1
		USB_D-	36 USBP11N
		USB_D+	38 USBP11P
3	RESERVED#3	SMB_CLK	30 M_SMB_CLK R413 1 (R) 0R2J-2-GP SMBCLK
5	RESERVED#5	SMB_DATA	32 M_SMB_DATA R402 1 (R) 0R2J-2-GP SMBDATA
8	RESERVED#8	WAKE#	1 W_WAKE_N
10	RESERVED#10	CLKREQ#	7 PLTRST*_RISER
12	RESERVED#12	PERST#	22 PLTRST*_RISER 33
14	RESERVED#14		
16	RESERVED#16	GND	4
17	RESERVED#17	GND	9
19	RESERVED#19	GND	15
20	RESERVED#20	GND	18
37	RESERVED#37	GND	21
39	RESERVED#39	GND	26
41	RESERVED#41	GND	27
43	RESERVED#43	GND	29
45	RESERVED#45	GND	34
47	RESERVED#47	GND	35
49	RESERVED#49	GND	40
51	RESERVED#51	GND	50
		GND	53
42	LED_WWAN#	GND	54
44	LED_WLAN#		
46	LED_WPAN#		

NP1 NP2 NP1 NP2

SKT-MINI52P-1-GPU1

(62.10043.741)

VCC3_3

W_DISABLE*
W_DETECT_N_R

VCC3_3
R744 2 1 W_DETECT_N
10KR2J-3-GP

0413
R1412
W_DETECT_N 1
100R2J-2-GP

TP-2 TP26

C1482 SCD1U16V2ZY-2GP (R)

0411

<Variant Name>

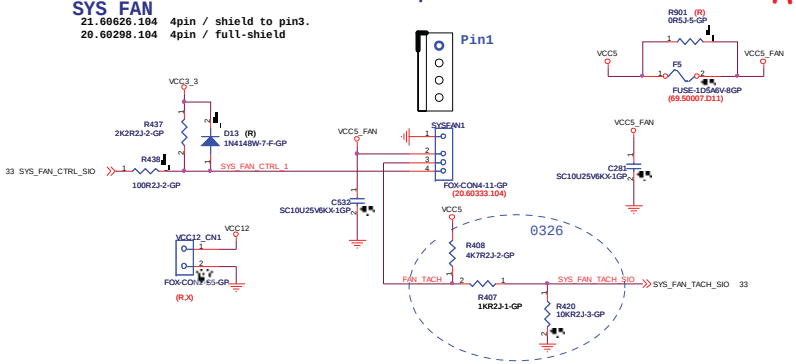
wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	MINI PCIE SLOT	
Size A4	Document Number Creston	Rev SA
Date: Wednesday, August 04, 2010	Sheet 31 of 44	

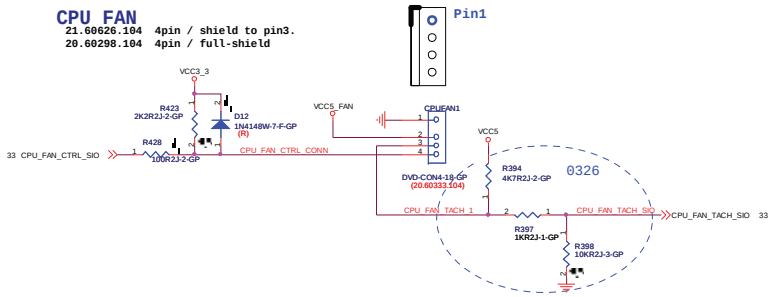
SYS FAN 4pin shield

SYS FAN
21.60626.104 4pin / shield to pin3.
20.60298.104 4pin / full-shield

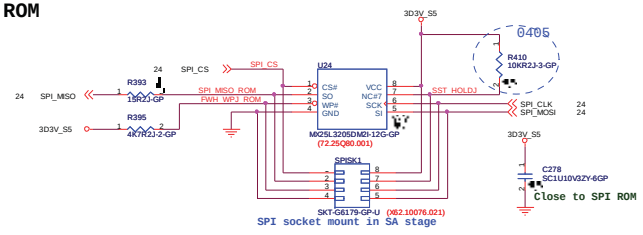


CPU FAN 4pin shield

CPU FAN
21.60626.104 4pin / shield to pin3.
20.60298.104 4pin / full-shield

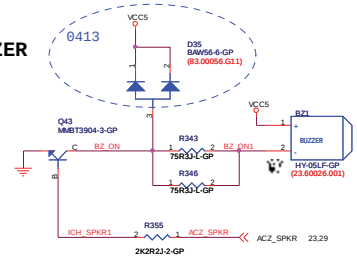


SPI ROM

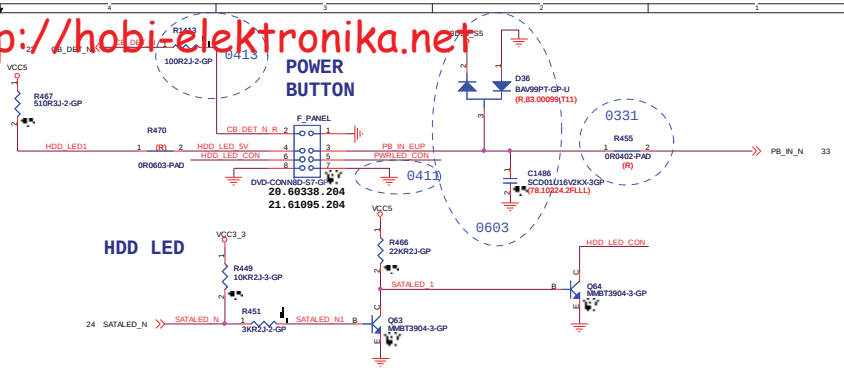


1. Main Source: 72.25X80.A01(Winbond 8Mb) EOL
2. 2nd Source: 72.25805.001 (MXIC 8Mb)
3. 3ns source: 72.26081.001 (ATMEL 8Mb)
4. Main Source: 72.25Q80.001

BUZZER

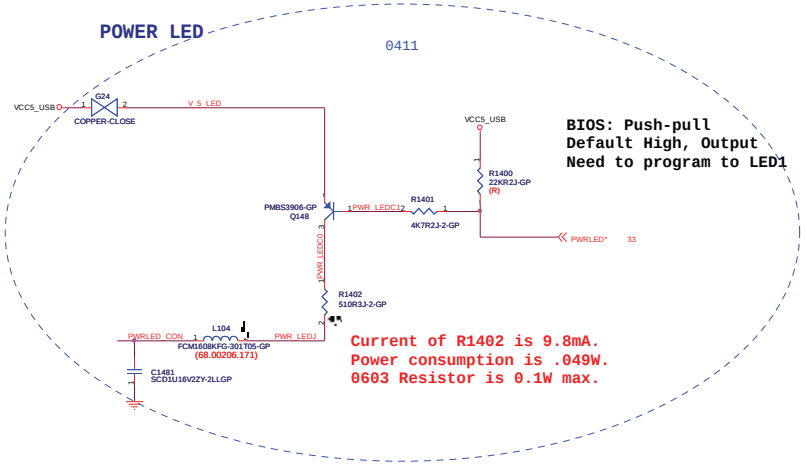


POWER BUTTON



HDD LED

POWER LED

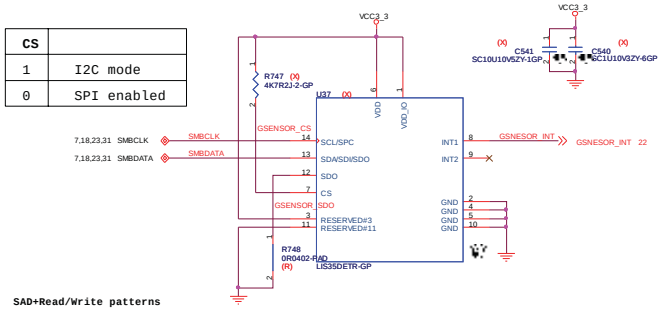


BIOS: Push-pull
Default High, Output
Need to program to LED1

Current of R1402 is 9.8mA.
Power consumption is .049W.
0603 Resistor is 0.1W max.

Power LED Definition
S0: ON
S3: Blink
S5: OFF

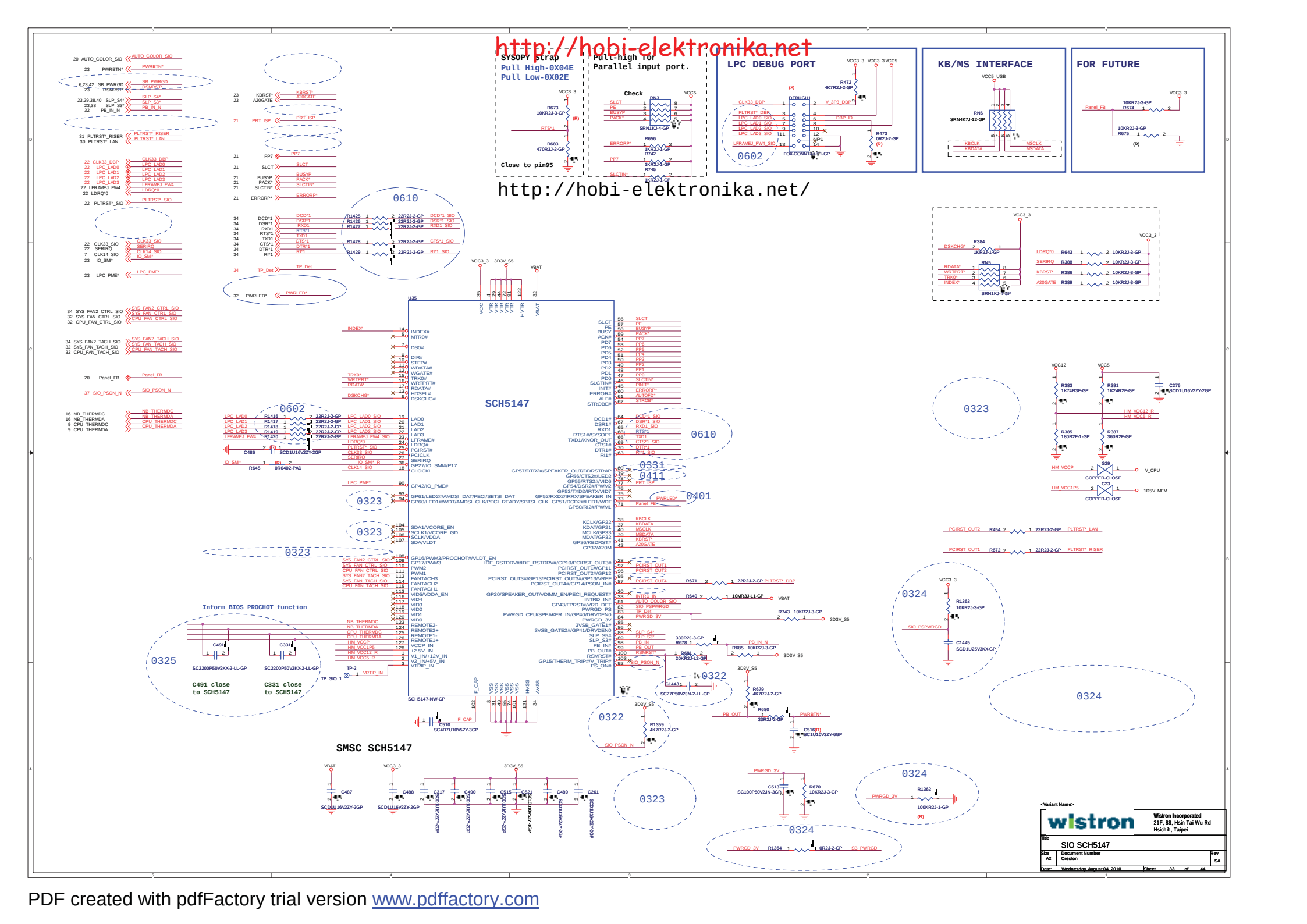
CS	
1	I2C mode
0	SPI enabled



SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0]=SDO	R/W	SAD+R/W
Read	001110	0	1	00111001(39h)
Write	001110	0	0	00111000(38h)
Read	001110	1	1	00111011(3Bh)
Write	001110	1	0	00111010(3Ah)

<Core Design>
wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title: SPI & FAN & BUZZER & LED & G-Sensor
Size: Custom | Document Number: Creston | Rev: SA
Date: Wednesday, August 04, 2010 | Sheet 32 of 44



Gb LAN

TRD0N / TRD0P 30
TRD1N / TRD1P 30
TRD2N / TRD2P 30
TRD3N / TRD3P 30
LINK*_ACTIVITY_L 30
LANLED_G 30
LANLED_O 30

PARALLEL PORT

FAN

33 SYS_FAN2_CTRL_SIO
33 SYS_FAN2_TACH_SIO

USB

23 USBP4N / USBP4P
23 OC*67
23 USBP6N / USBP6P
23 USBP7N / USBP7P

Riser Detect

24 RISER1_DET
24 RISER2_DET

PS2 KB & MS

RISER1
0323
RCTS*1
RDSR*1
RRXD1
RDCD*1
RRI*1
RDTR*1
RRTS*1
RTXD1
SYS_FAN2_CTRL_SIO
SYS_FAN2_TACH_SIO
RISER1_DET_R
VCC3_3
VCC5
R1409
100R2J-2-GP
0413
JWT-CONN40A-GP
20.F1161.040
Pin1 Pin2 Pin39 Pin40

Pin39 is RISER1_DET

RISER2
V_3P3_LAN
TRD3N TRD3P TRD2N TRD2P TRD1N TRD1P TRD0N TRD0P
LINK*_ACTIVITY_L
LANLED_G
LANLED_O
USBP6N USBP6P USBP7N USBP7P
RISER2_DET_R
USBP4N USBP4P
USBVCC67
R1410
100R2J-2-GP
JWT-CONN30F-GP
21.D0301.215
Pin16 Pin1 Pin30 Pin15

Pin28 is RISER2_DET

F3
FUSE-2A8V-3GP
R474 10KR2J-3-GP
R471 15KR2J-1-GP
C330 SC1KP50V2KX-1GP
C325 SC1U10V3ZY-6GP
C323 SC1U10V3ZY-6GP

SERIAL PORT

RXD1 TXD1 RTS*1 CTS*1 DTR*1 DSR*1 DCD*1 RI*1 SER_RI*

MAXIM 74.03243.AFG
ST 74.03243.0FG
Intersil 74.03243.BFG

SERIAL PORT

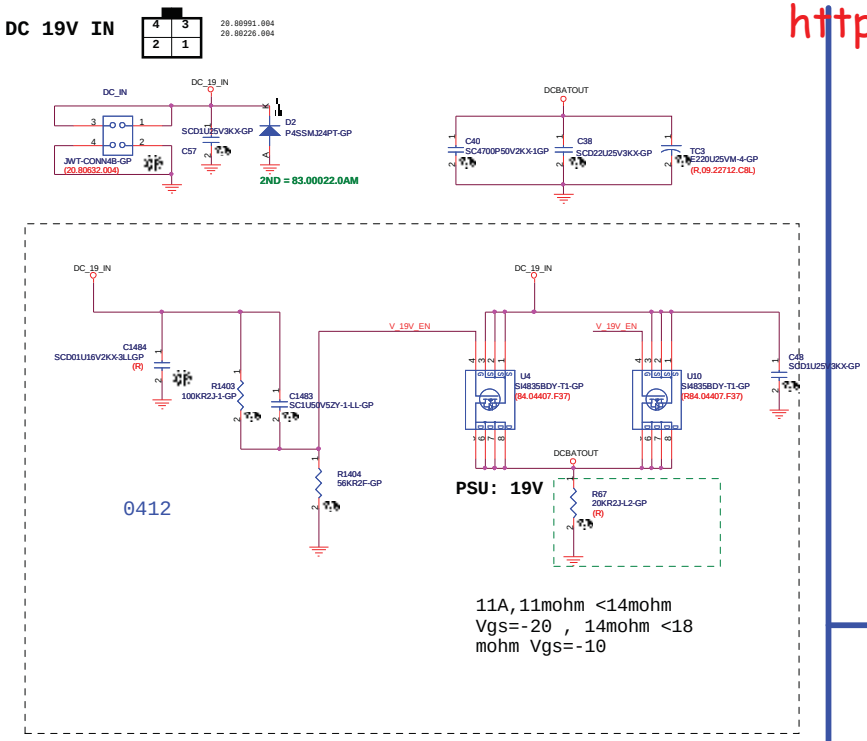
U27
MAX3243ECUI-T-GP
C303 SCD047U10V2KX-2GP
C315 SCD33U16V3KX-1GP
C298 SCD1U10V2KX-4-LL-GP
C310 SCD33U16V3KX-1GP
C311 SCD33U16V3KX-1GP
R421 R427 R422 R432 R419 R426 R414 R403 2K2R2J-2-GP
R444 10KR2J-3-GP
R440 10KR2J-3-GP
Q58 MMBT3904-3-GP

F6
FUSE-1D5A6V-3GP
C539 SC10U10V5ZY-1GP
R1411
100R2J-2-GP
RISER3
DVD-CON5-14-GP

<Variant Name>

wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: REAR IO RISER
Size: A3
Document Number: Creston
Rev: SA
Date: Wednesday, August 04, 2010
Sheet 34 of 44



<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: DC19V & SYS_EN CIRCUIT

Size	Document Number	Rev
C	Creston	SA

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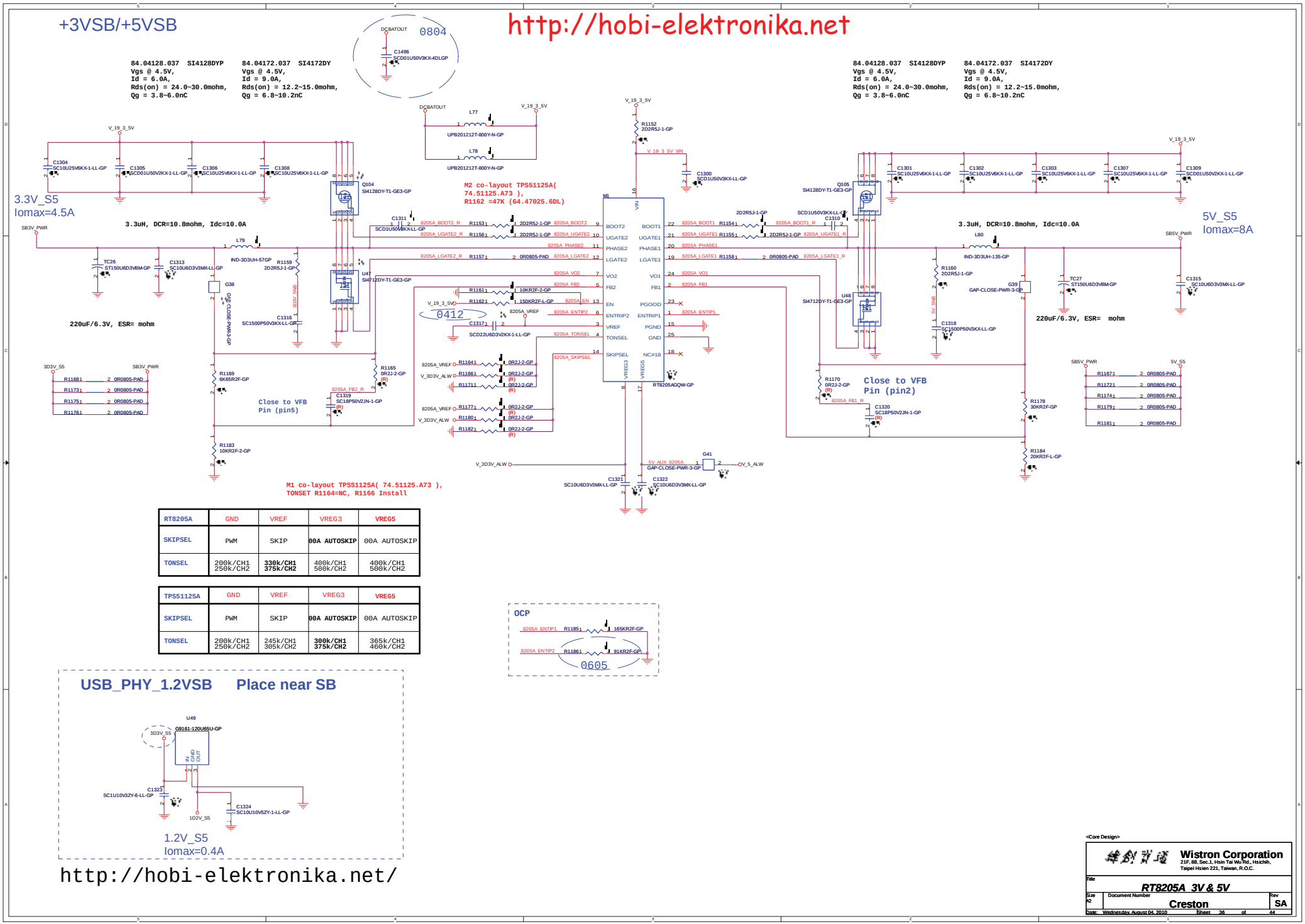

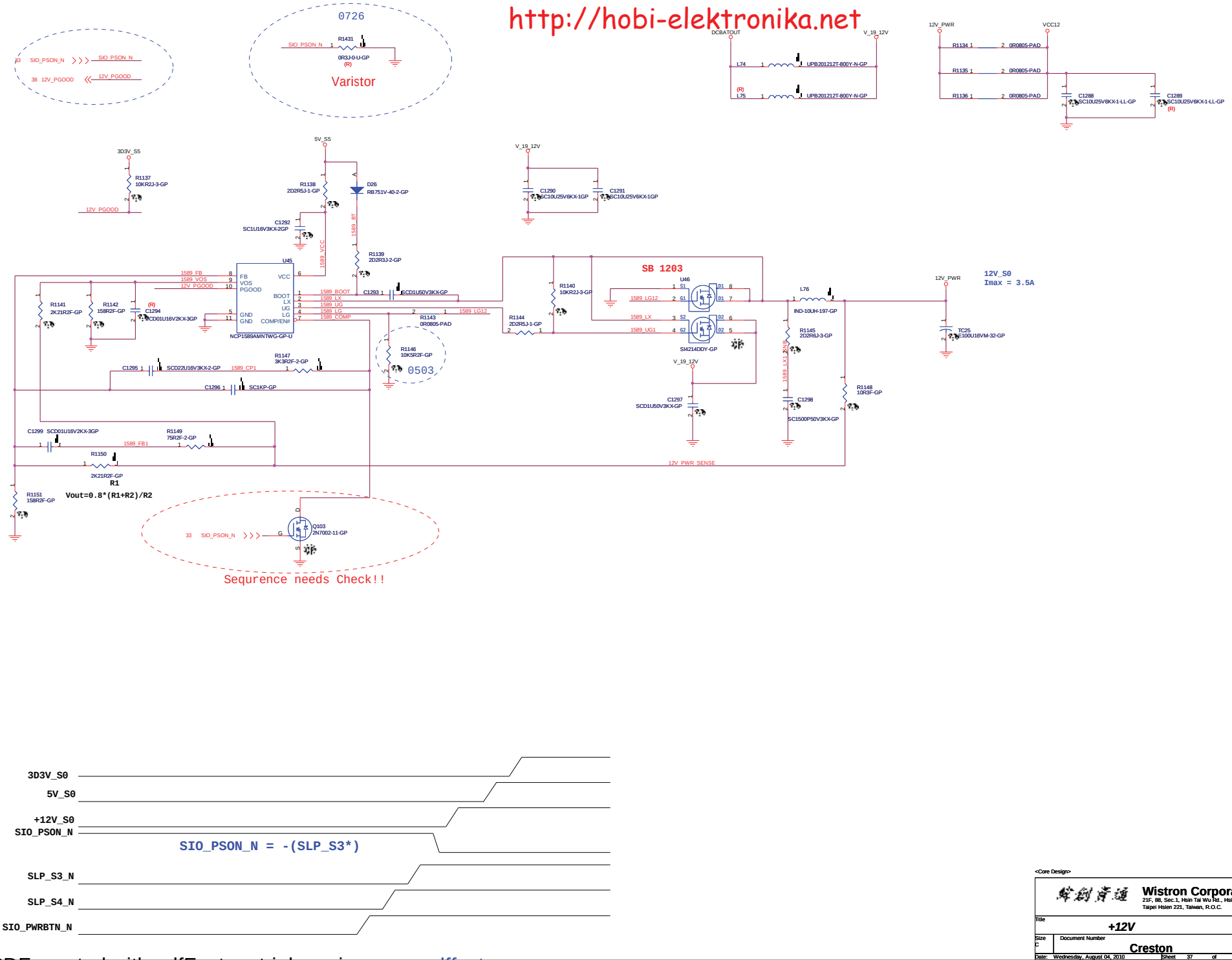

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: +12V

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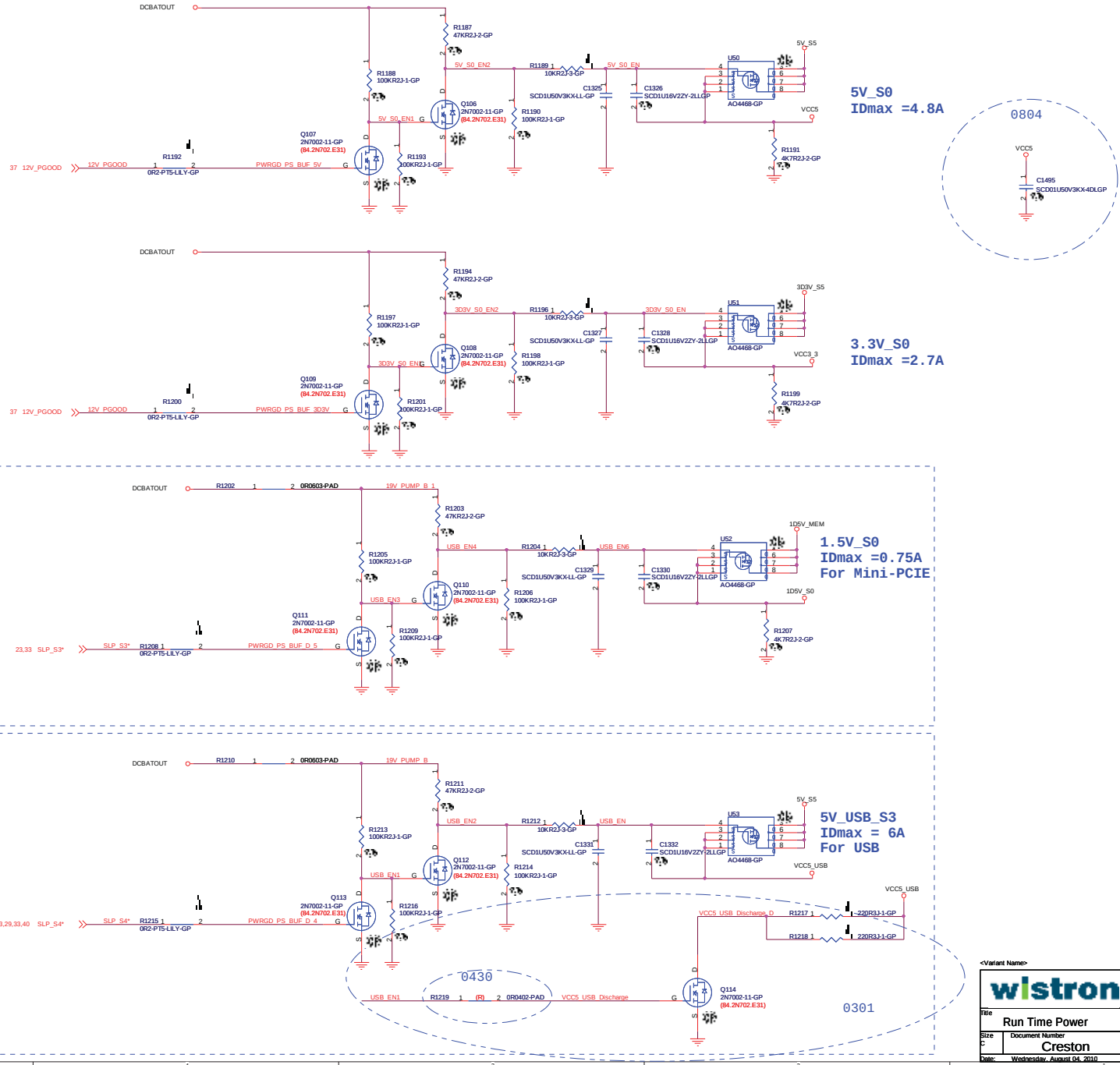
Run Time Power



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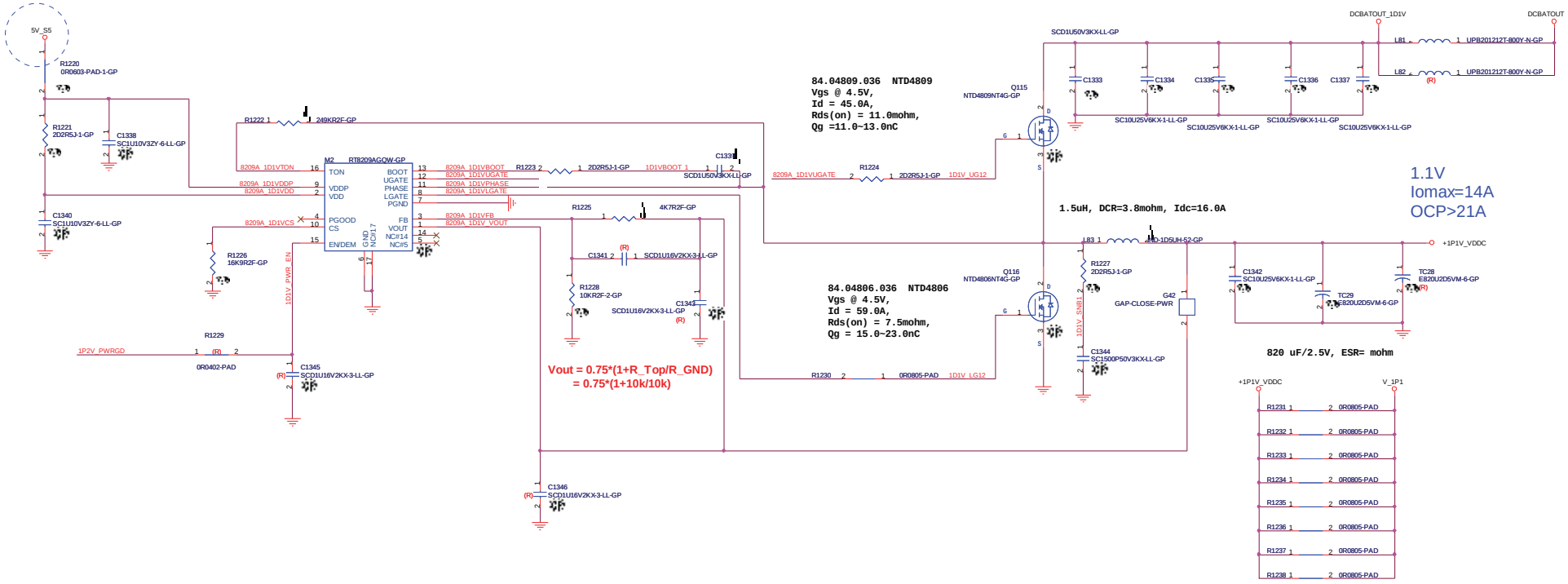

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wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: CHIPSET CORE POWER (V_1P1)

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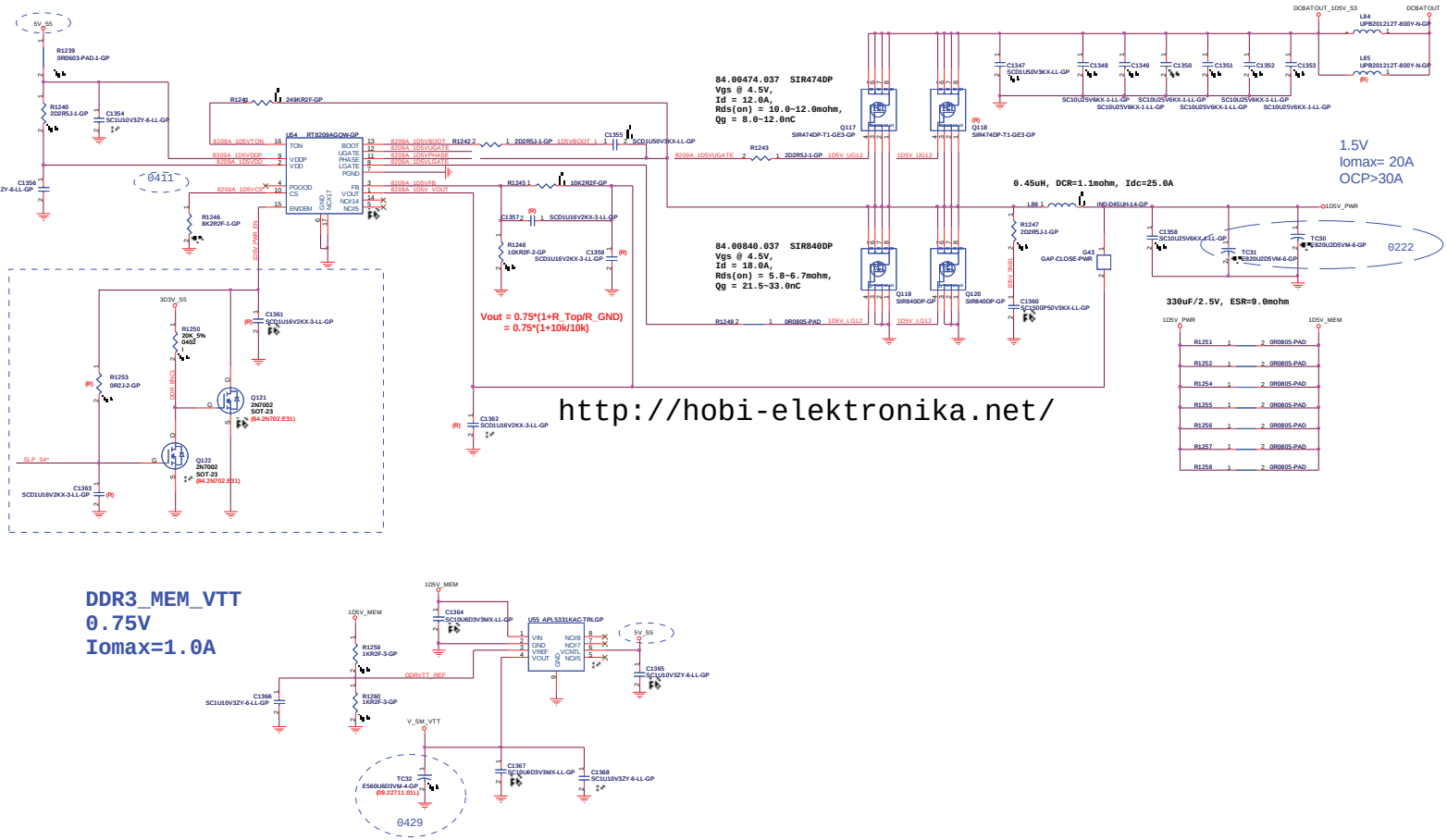
1D5V_S3_RT8209A



DDR3_MEM_VTT
0.75V
Iomax=1.0A

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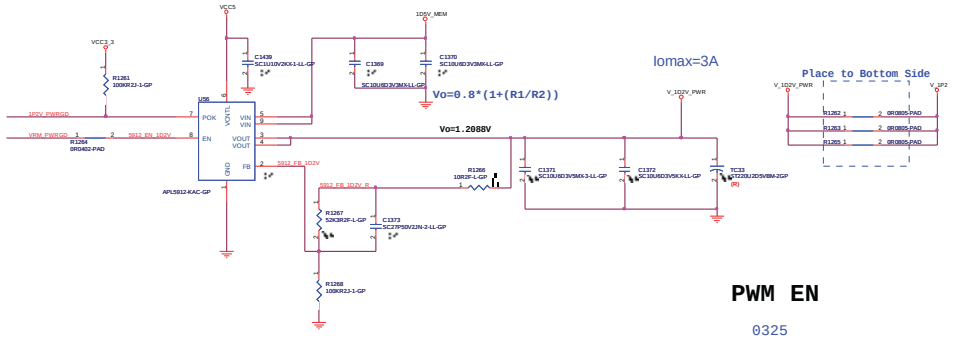
Hsichih, Taipei

DDR & TERM POWER

Creston

+1P2V_SBNB



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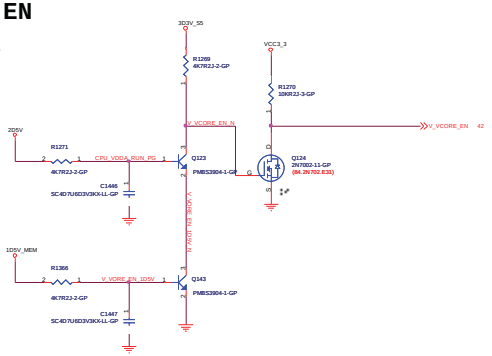

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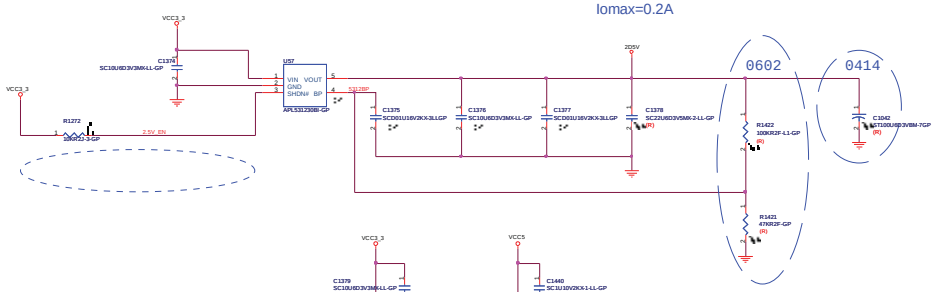

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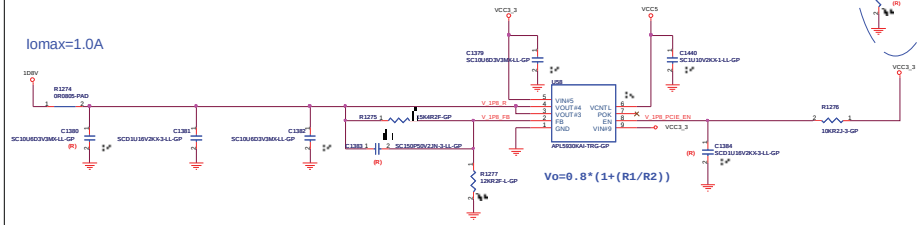
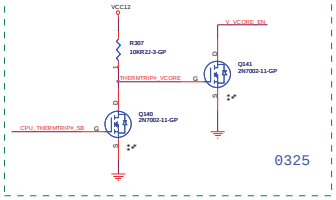
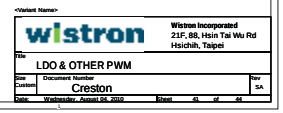
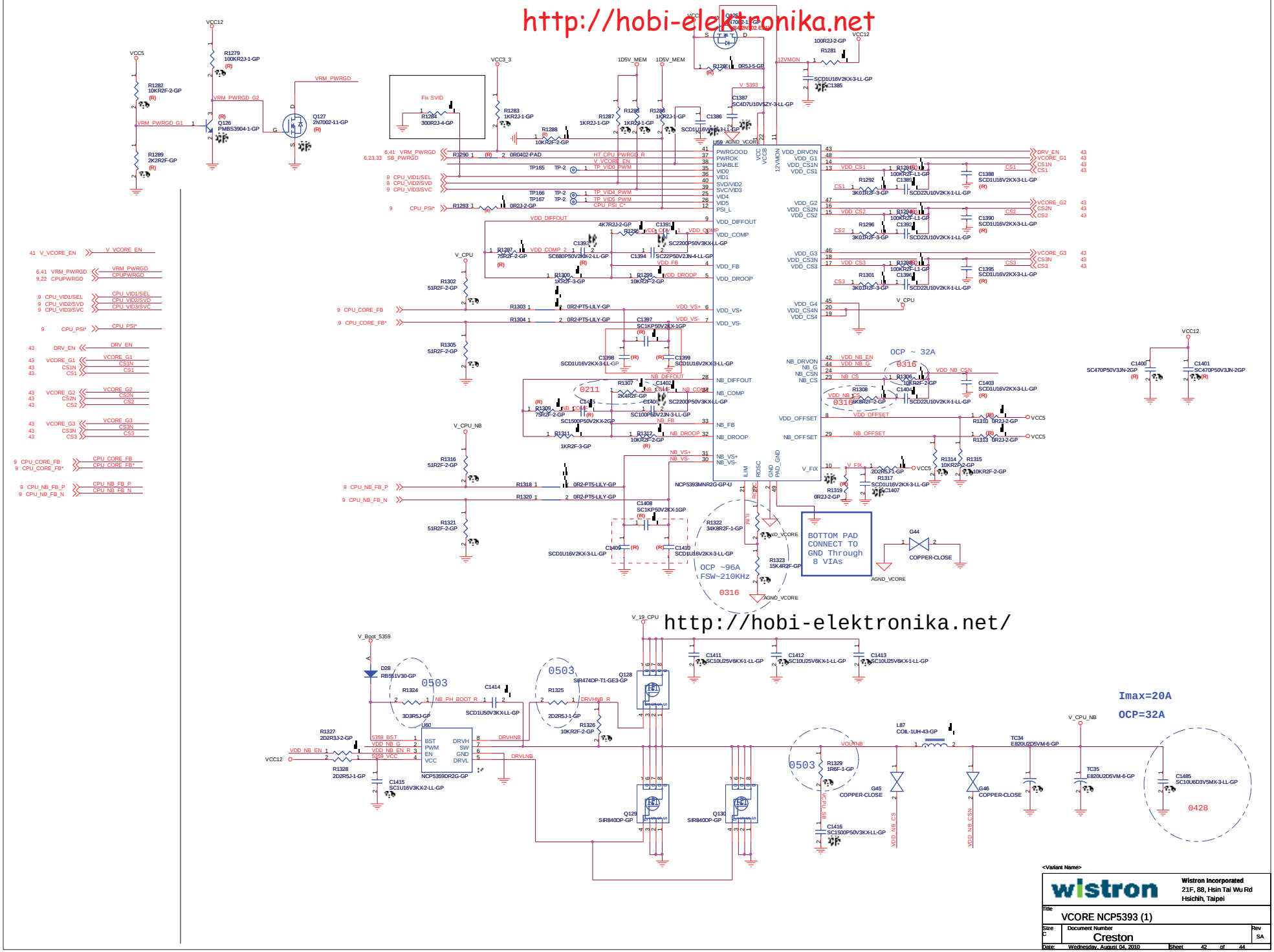
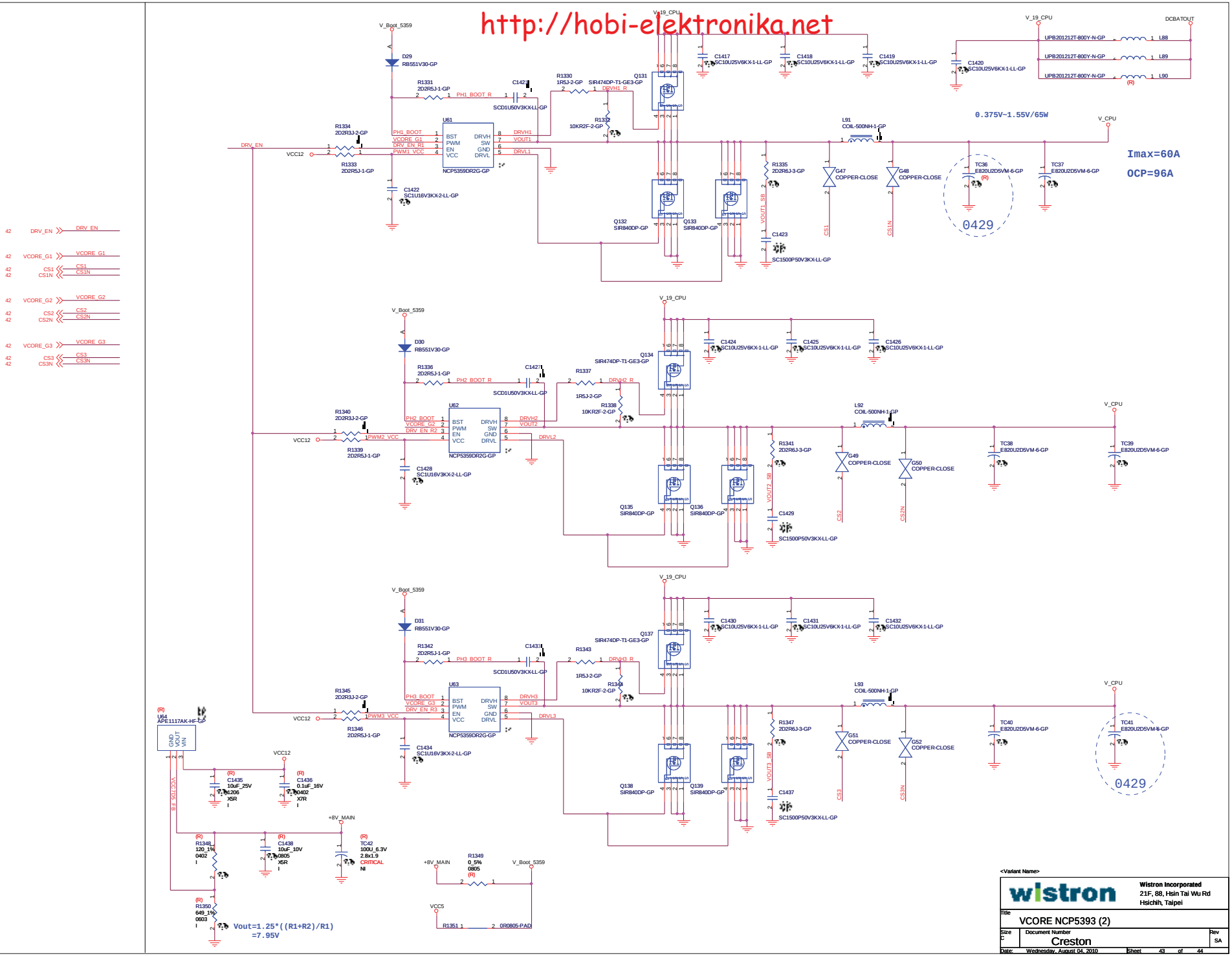


Thermal Protection









<Variant Name>

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Title
TEST COUPON

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A4	Creston	SA

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