

AMD KABINI EA/EG-40/50
PX /UMA Schematics Document
AMD FT3 APU
AMD GPU SUN XT M2/64bit

EAEG50 KB UMA

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Cover Page

Size
A4

Document Number

KABINI

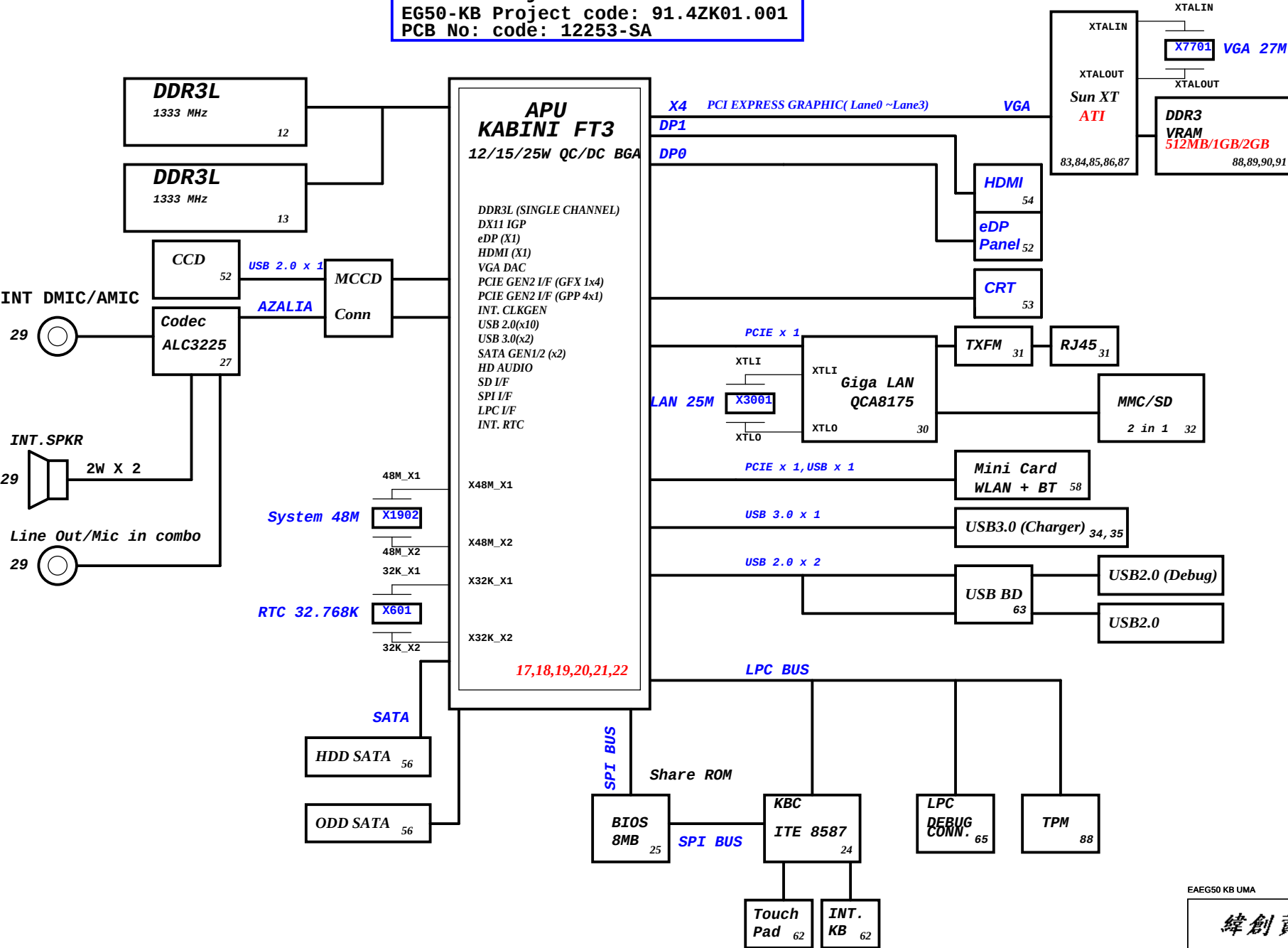
Rev

Date: Wednesday, October 24, 2012

Sheet 1 of 102

AMD KABINI

EA40-KB Project code: 91.4ZF01.001
PCB No: code: 12247-SA
EA50-KB Project code: 91.4YU01.001
EG50-KB Project code: 91.4ZK01.001
PCB No: code: 12253-SA



SYSTEM DC/DC	
TPS51225	45
INPUTS	OUTPUTS
DCBATOUT	5V_CHARGER (6.52A) 3D3V_S5 (5.05A)
SYSTEM DC/DC	
RT8207	49
DCBATOUT	1D5V_S3 (10.5A)
RT8207	
DCBATOUT	0D75_S0 (1.2A)
SYSTEM DC/DC	
RT8068	50
INPUTS	OUTPUTS
3D3V_S5	1D8V_S5 (3.05A)
SY8208	48, 51
DCBATOUT	1D5V_S5 (5.4A)
DCBATOUT	0D95V_S5 (5.6A)
TPS22966	
5V_CHARGER	5V_S5 (5.83A) 5V_S0 (3.5A)
TPS22966	
3D3V_S5	3D3V_S0 (2.8A)
1D5V_S5	1D5V_S0 (0.6A)
TPS22966	
1D8V_S5	1D8V_S0 (1.5A)
0D95V_S5	0D95V_S0 (5.6A)
CHARGER	
BQ24737	44
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 5.5A
CPU DC/DC	
ISL6267	46,47
INPUTS	OUTPUTS
DCBATOUT	APU_VDD 0.3~1.4V, 21A APU_VDDNB 0.7~1.325V, 17A
VGA DC/DC	
TPS51728	82
DCBATOUT	VGA_CORE (35.5A)
TPS22966	
3D3V_S0	3D3V_VGA_S0
1D5V_S5	1D5V_VGA_S0
TPS22966	
1D8V_S5	1D8V_VGA_S0
0D95V_S5	0D95V_VGA_S0

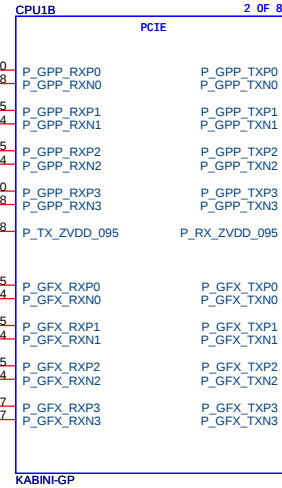
LAN + Card

WLAN

GFX x 4

71.KABIN.B0U
71.KABIN.C0U

IC CPU Kabini 4110 1.5GHz 15W4C FT3 ES2 BGA
IC CPU Kabini 5110 2.0GHz 25W4C FT3 ES2 BGA



PCIE Table

0	LAN + Card
1	WLAN
2	NC
3	NC

LAN + Card

WLAN

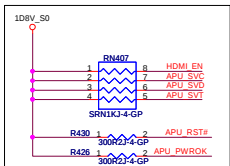
GFX x 4

PEG_TXP[0..3] >> PEG_TXP[0..3] 73
PEG_TXN[0..3] >> PEG_TXN[0..3] 73

PEG_RXP[0..3] << PEG_RXP[0..3] 73
PEG_RXN[0..3] << PEG_RXN[0..3] 73

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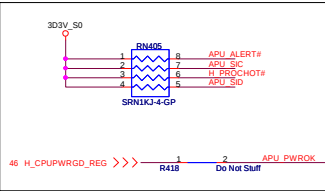
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
CPU PCIE			
Size A3	Document Number		Rev
KABINI			
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20120821 Follow Larne

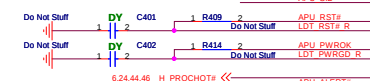
TABLE 6. PRE-PWROK METAL VID CODES

SVC	SVD	OUTPUT VOLTAGE (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

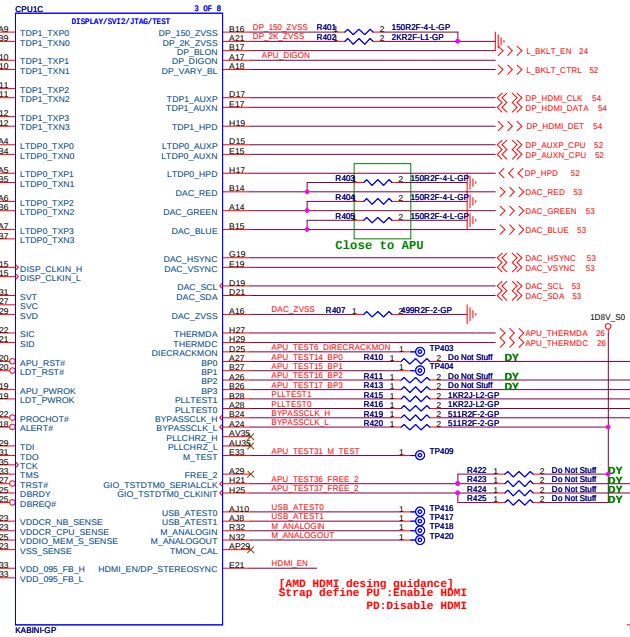
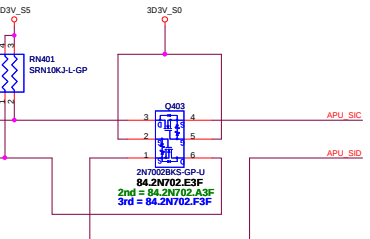


20120820 Follow Larne

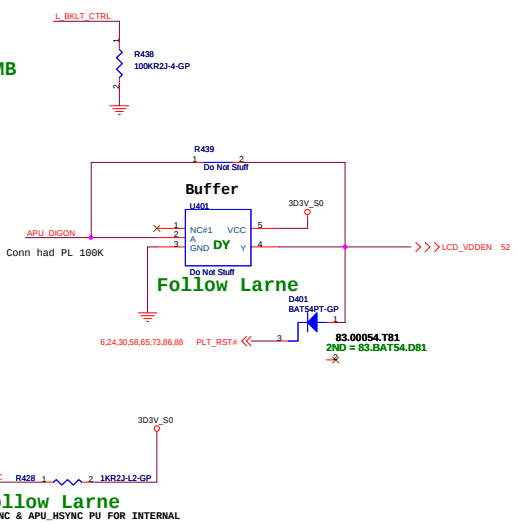
APU HDMI
APU EDP



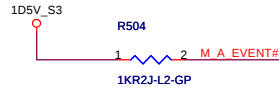
APU core control



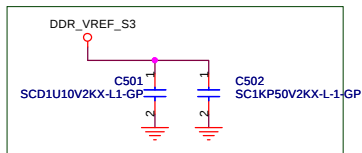
APU EDP
APU HDMI SMB
APU EDP
APU CRT



Follow Larne
DP_STEREO SYNC & APU_HSYNC PU FOR INTERNAL



APU_VREF_DQ



LAYOUT: place them close to APU



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Title		
CPU DDR		
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PSH CLR#

303V_50

R630
Do Not Stuff

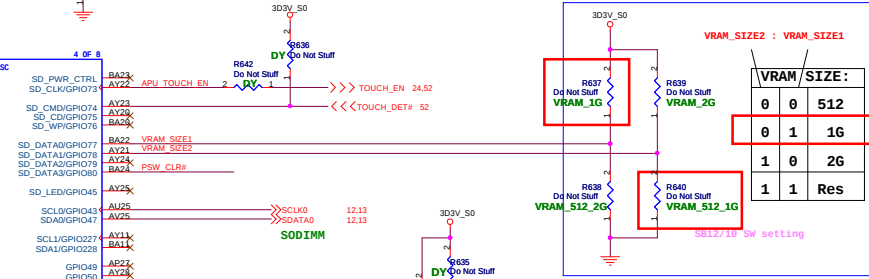
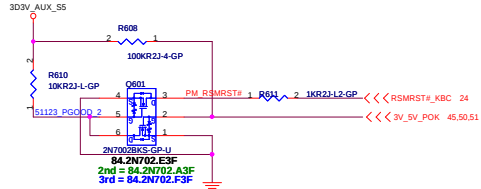
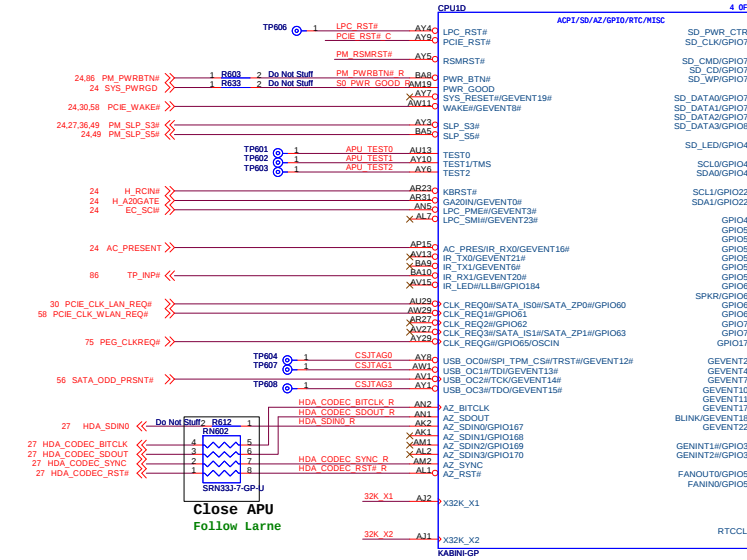
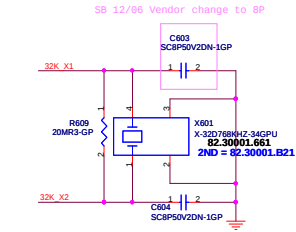
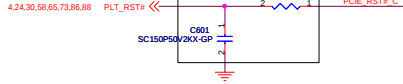
G601
Do Not Stuff

303V_50

R6601
Do Not Stuff

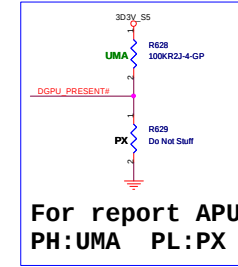
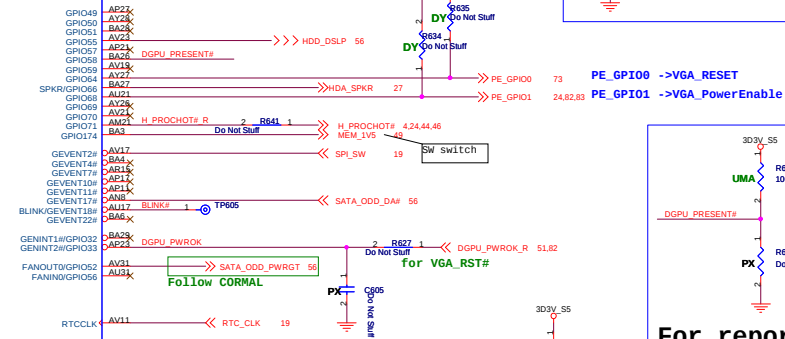
G601
Do Not Stuff

303V_50



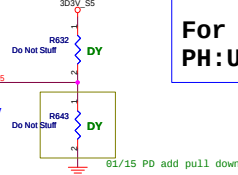
VRAM		SIZE:
0	0	512
0	1	1G
1	0	2G
1	1	Res

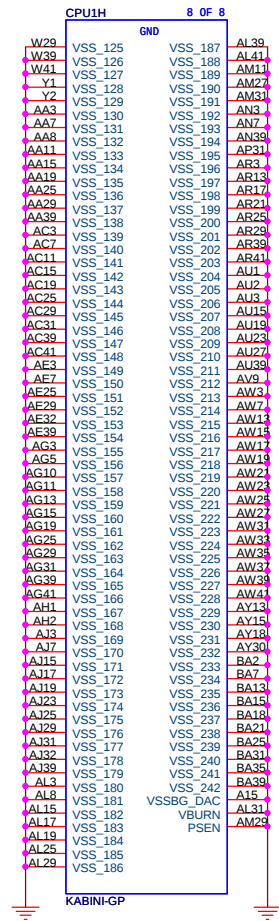
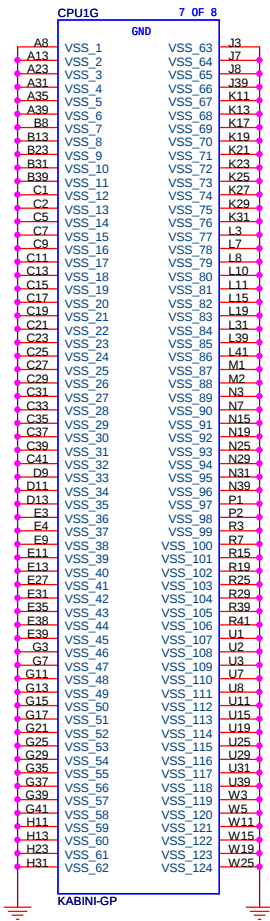
SUN only 4 bank for 1G



For report APU
PH:UMA PL:PX

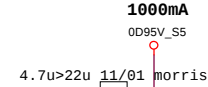
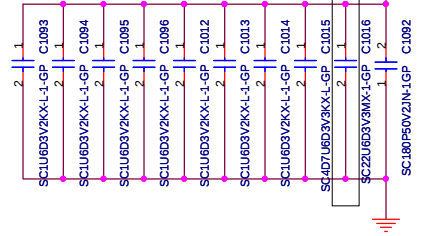
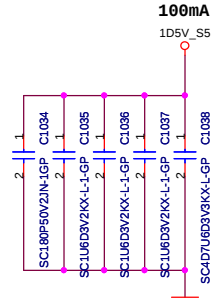
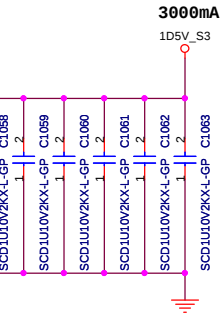
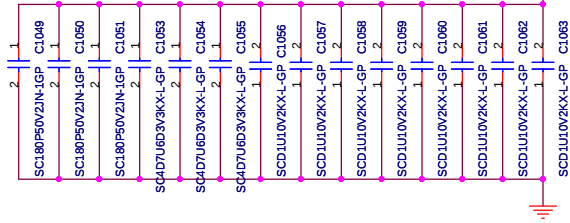
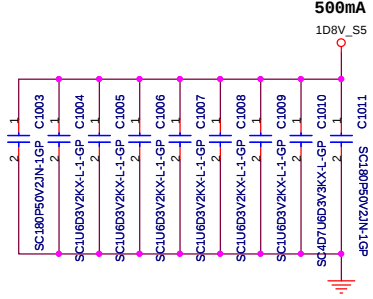
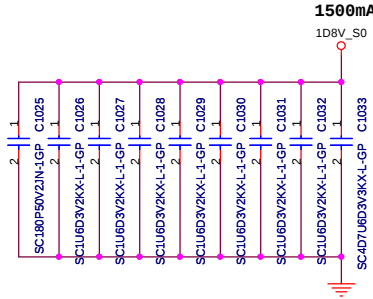
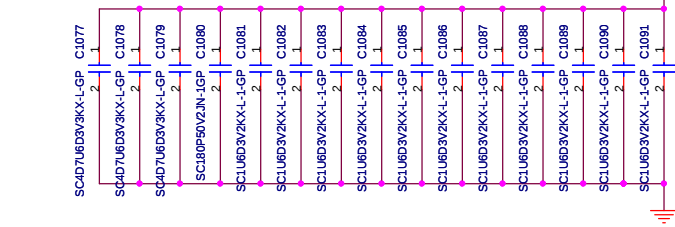
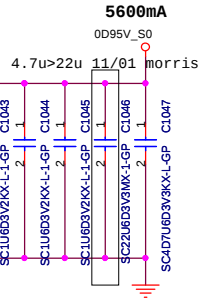
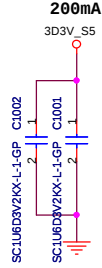
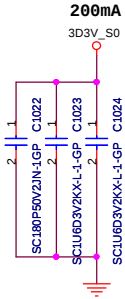
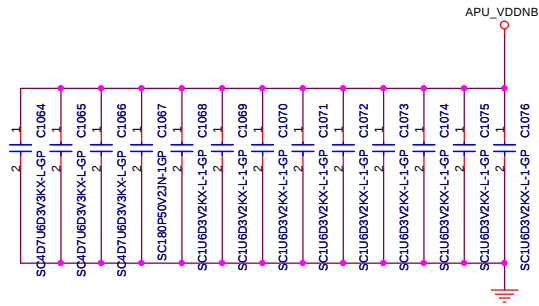
HW setting MEM_1V5 H = 1.5V
L = 1.35V





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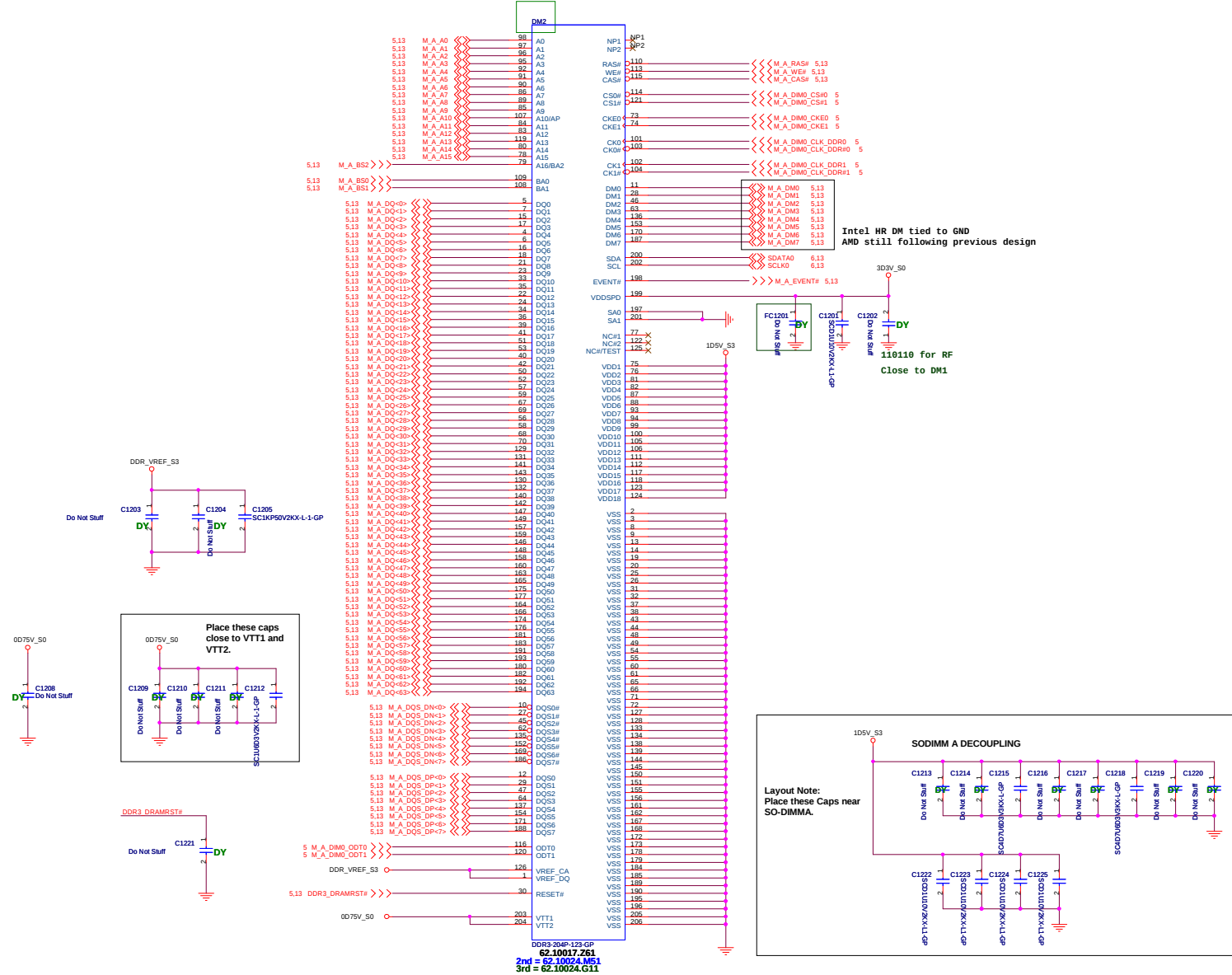
緯創資通 Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title CPU VSS		
Size A3	Document Number KABINI	Rev
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Title		
CPU POWER CAP1		
Size	Document Number	Rev
A3	KABINI	
Date:	Tuesday, January 15, 2013	Sheet 10 of 102

01/14 PD change location name for factory issue



Follow JE50-SB
H = 4mm

01/15 PD remove 62.10017.X31 for factory issue

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θ	HDD
1	ODD

25M X1

R1901
Do Not Stuff

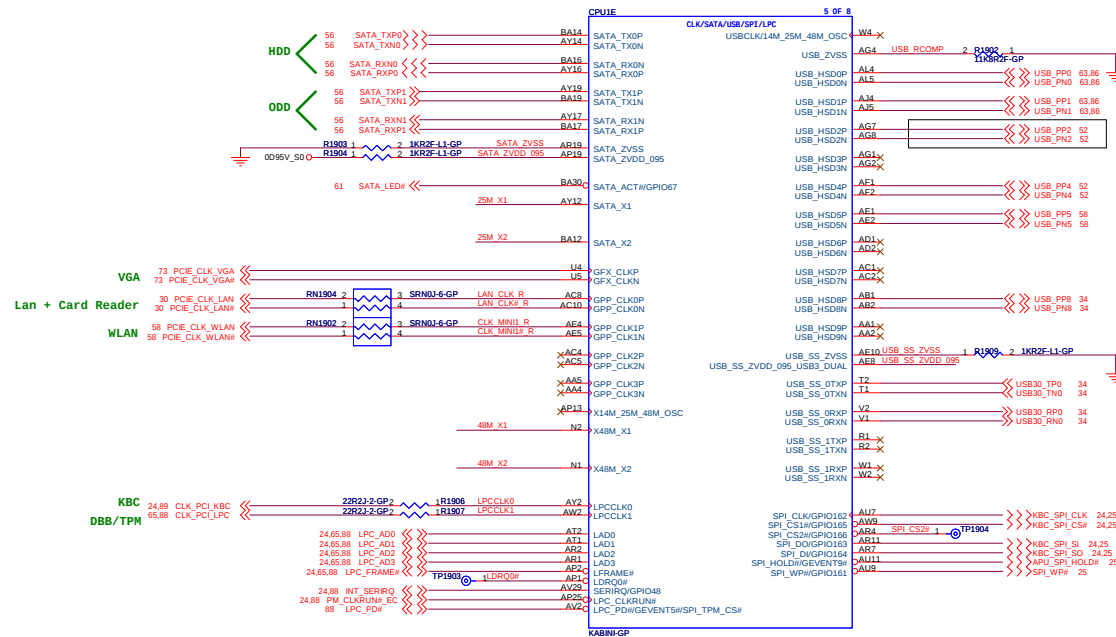
25M X2

X1901
Do Not Stuff

C1901
1
190pF
Do Not Stuff

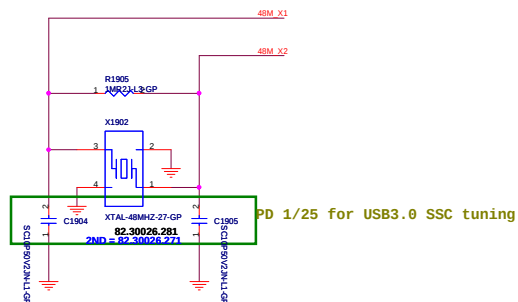
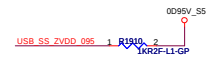
C1902
1
190pF
Do Not Stuff

2nd = 82.30020.G61



Pair	Device
0	USB2.0 Debug (DB Conn)
1	USB2.0 (DB Conn)
2	Touch Panel
3	
4	CCD (CCD Conn)
5	WLAN + BT (Mini PCI-E)
6	
7	
0/8	USB3.0 & USB 2.0 Charger (MB)
1/9	

		CLK
0	System & USB	48M
1	RTC	32.768K
2	SATA	25M
3	LAN	25M
4	VGA	27M

[illegible]

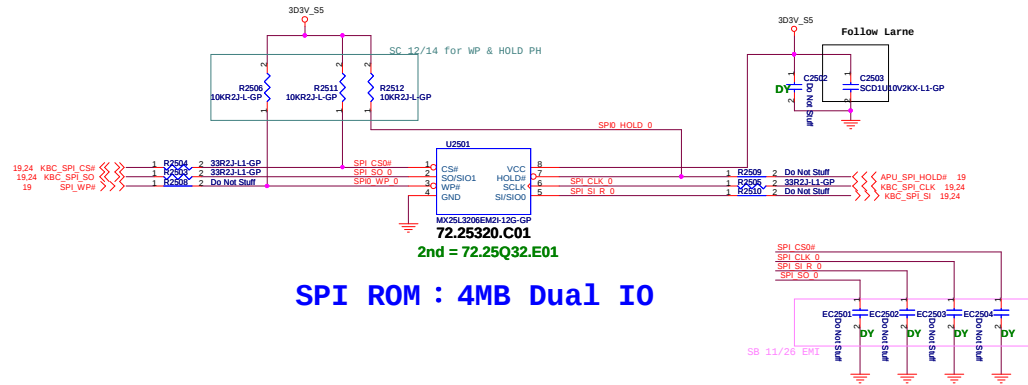
	LPC_CLK0	LPC_CLK1	LFRAME 1	EMPCARD_P0TE_P0REN#	RTC CLK
FULL HIGH	BOOT FAIL TIMER ENABLED	CLOCK ENABLED (DEFAULT)	SPI ROM (DEFAULT)	1.0V SPI ROM (DEFAULT)	NORMAL POWER UP/RESET TIMING (DEFAULT)
PULL LOW	BOOT FAIL TIMER DISABLED (DEFAULT)	CLOCK DISABLED	LPC ROM	3.0V SPI ROM	FAST POWER UP/RESET TIMING FOR SIMULATION

SPI FLASH ROM (4M byte) for KBC

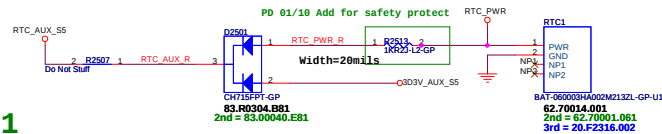
1st. MXIC : 72.25320.C01

2nd. WINBOND : 72.25Q32.E01

(手置件)請PCC移至DIP件



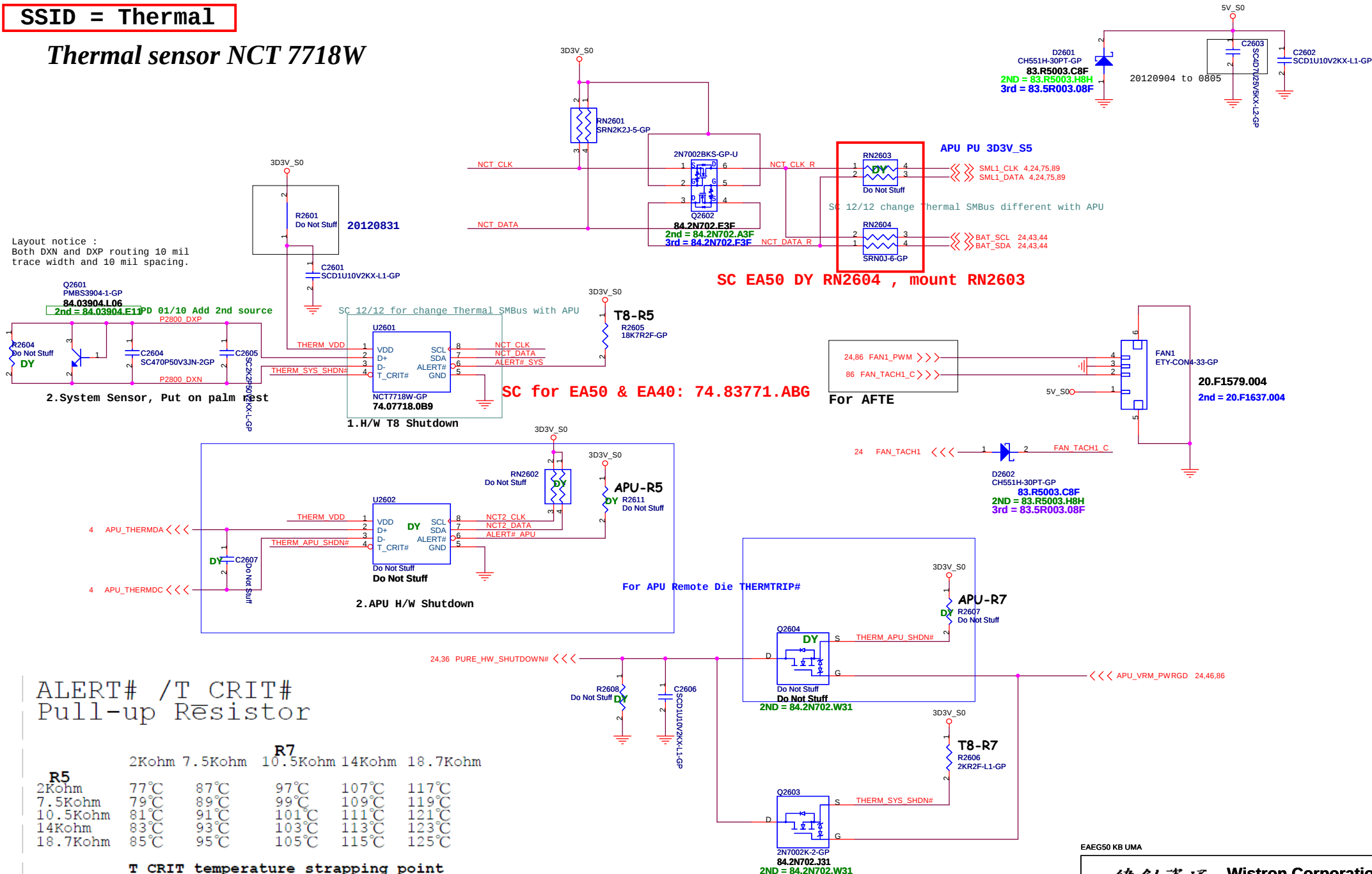
CR2032額外備料:
1.KTS: 23.20068.001
2.DBV: 23.22065.001



SSID = Thermal

Thermal sensor NCT 7718W

Layout notice :
Both DXN and DXP routing 10 mil
trace width and 10 mil spacing.



ALERT# /T CRIT#
Pull-up Resistor

	R7				
R5	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
2Kohm	77°C	87°C	97°C	107°C	117°C
7.5Kohm	79°C	89°C	99°C	109°C	119°C
10.5Kohm	81°C	91°C	101°C	111°C	121°C
14Kohm	83°C	93°C	103°C	113°C	123°C
18.7Kohm	85°C	95°C	105°C	115°C	125°C

T_CRIT temperature strapping point

T8=85 degree
SYS=85 degree
APU=125 degree

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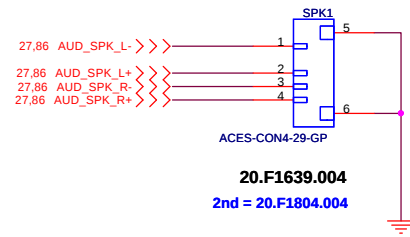
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Taipei Hsien 221, Taiwan, R.O.C.

Title			
Thermal 7718/Fan Controller P2793			
Size	Project Name		Rev
	KABINI		SA
Date:	Monday, February 04, 2013	Sheet	26 of 102

SSID = AUDIO

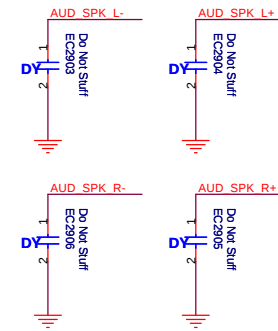
Speaker

2W 4ohm X 2 speaker

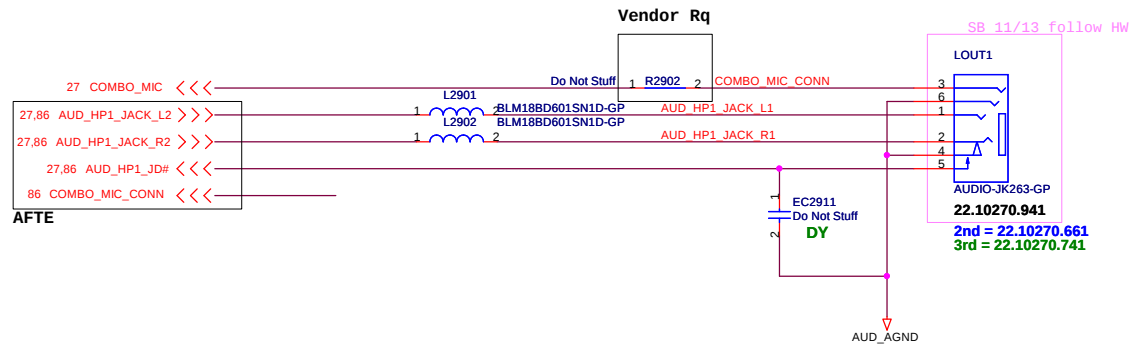


Layout Note:

Trace width=40mil



Combo Jack

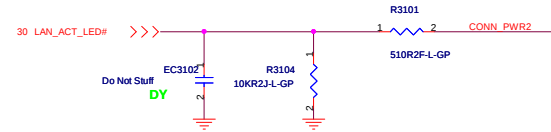
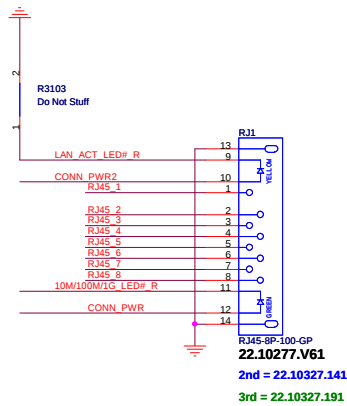
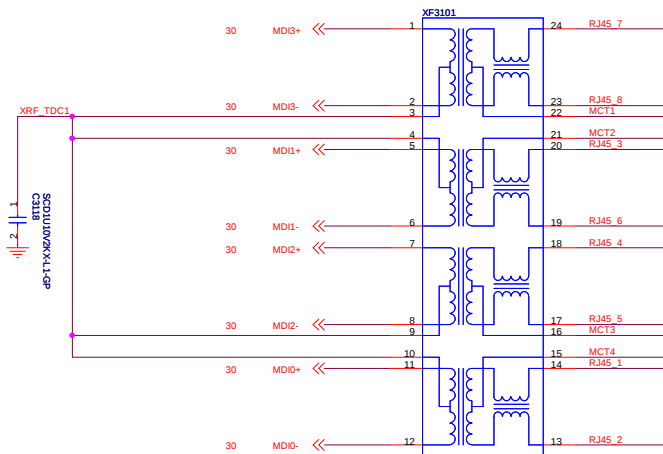


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Taipei Hsien 221, Taiwan, R.O.C.

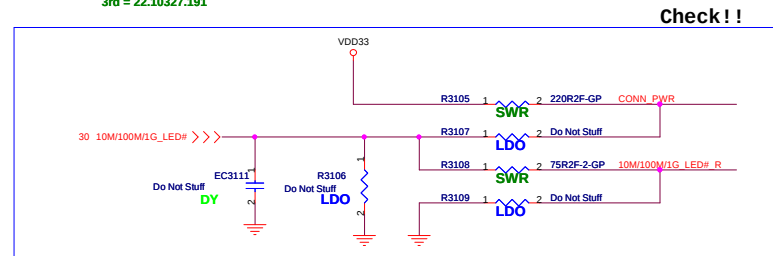
Title				
Audio Jack				
Size	Project Name			Rev
	KABINI			SA
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SSID = LAN

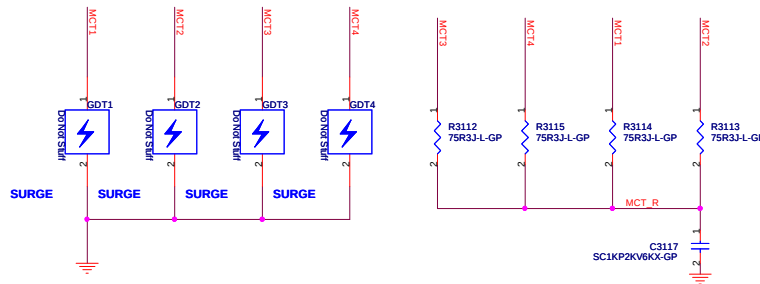
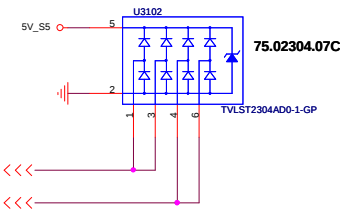
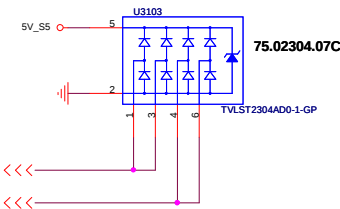
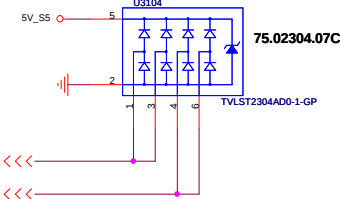
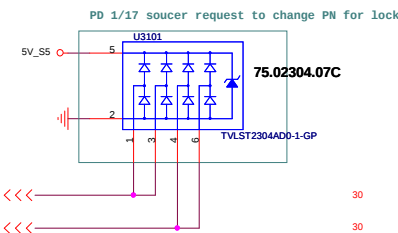
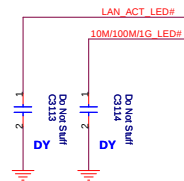
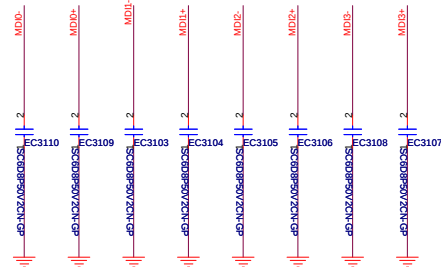
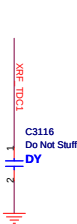


86 RJ45_1 >>>
86 RJ45_2 >>>
86 RJ45_3 >>>
86 RJ45_4 >>>
86 RJ45_5 >>>
86 RJ45_6 >>>
86 RJ45_7 >>>
86 RJ45_8 >>>
86 LAN_ACT_LED#_R >>>
86 10M/100M/1G_LED#_R >>>
86 CONN_PWR >>>
86 CONN_PWR2 >>>

For AFTE



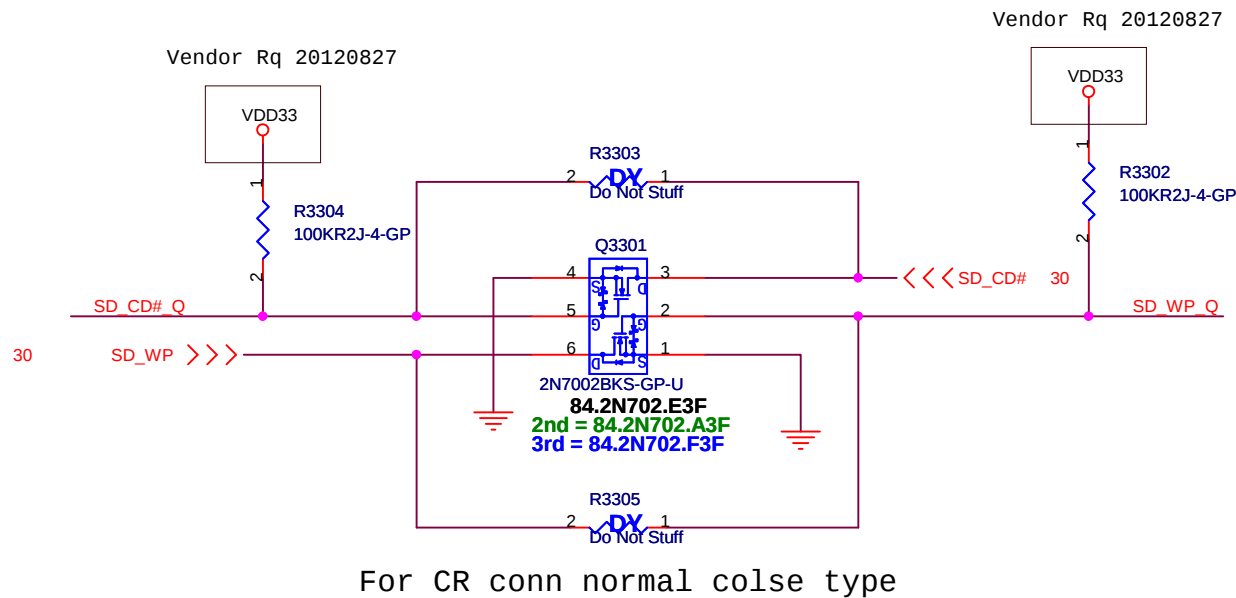
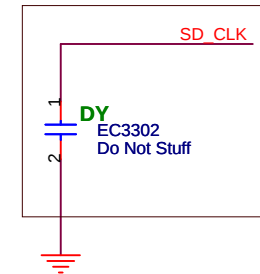
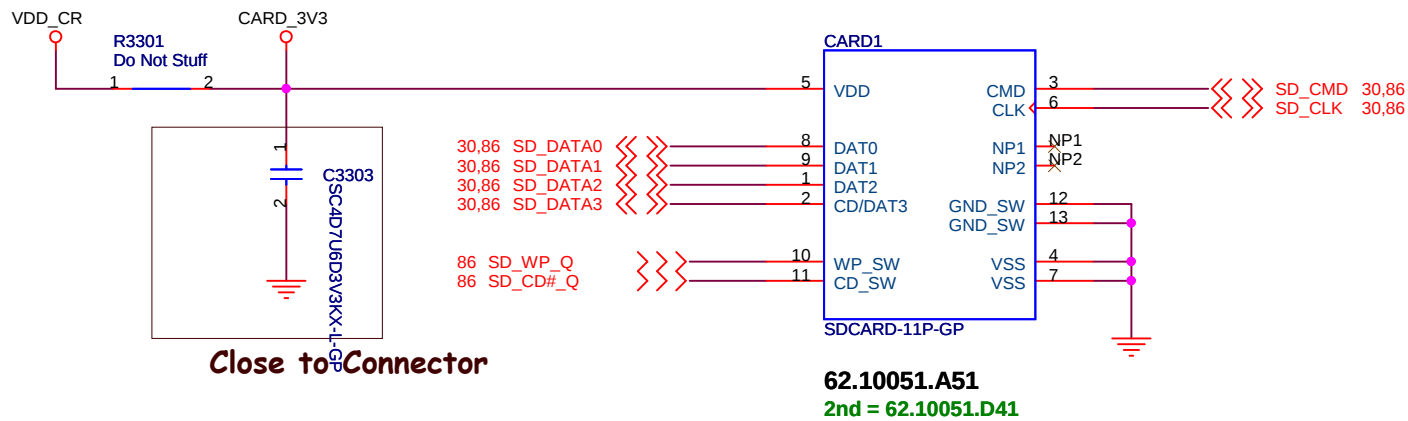
Check !!



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SSID = SDIO

SD//MS Card Reader



EAEG50 KB UMA

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title

CARD Reader CONN

Size

Project Name

KABINI

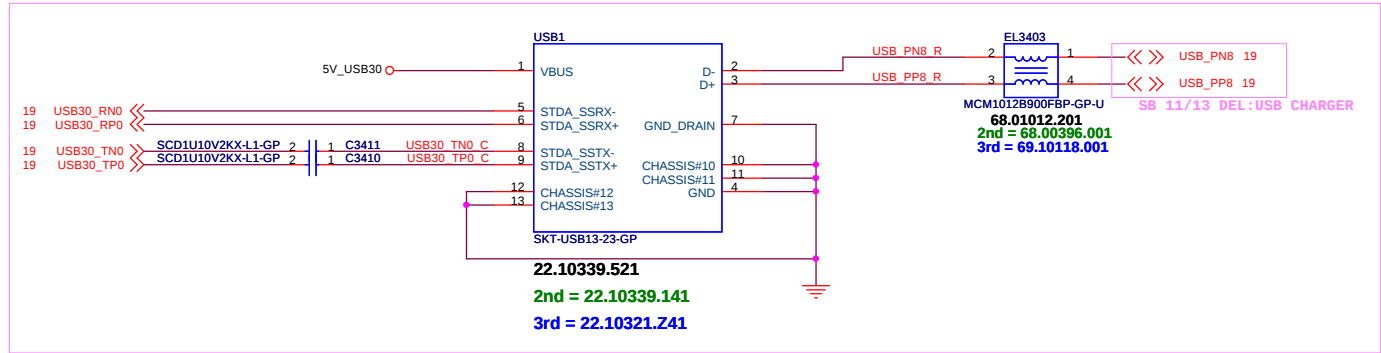
Rev

SA

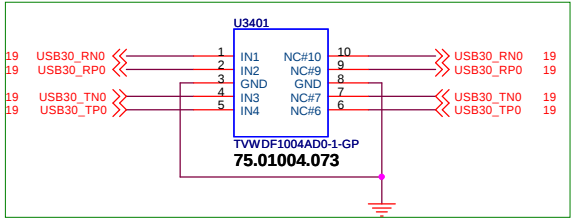
Date: Monday, February 04, 2013

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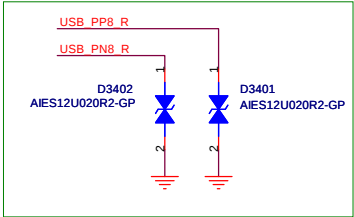
USB 2.0 CONTACT PIN		USB 3.0 CONTACT PIN	
PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME
1	VBUS	5	StdA_SSRX-
2	D-	6	StdA_SSRX+
3	D+	7	GND_DRAIN
4	GND	8	StdA_SSTX-
		9	StdA_SSTX+



SB 11/13 Change USB30 P/N



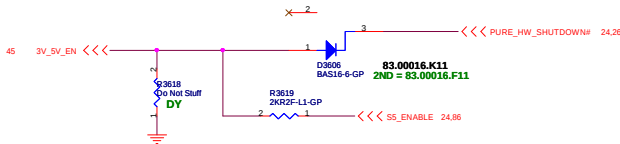
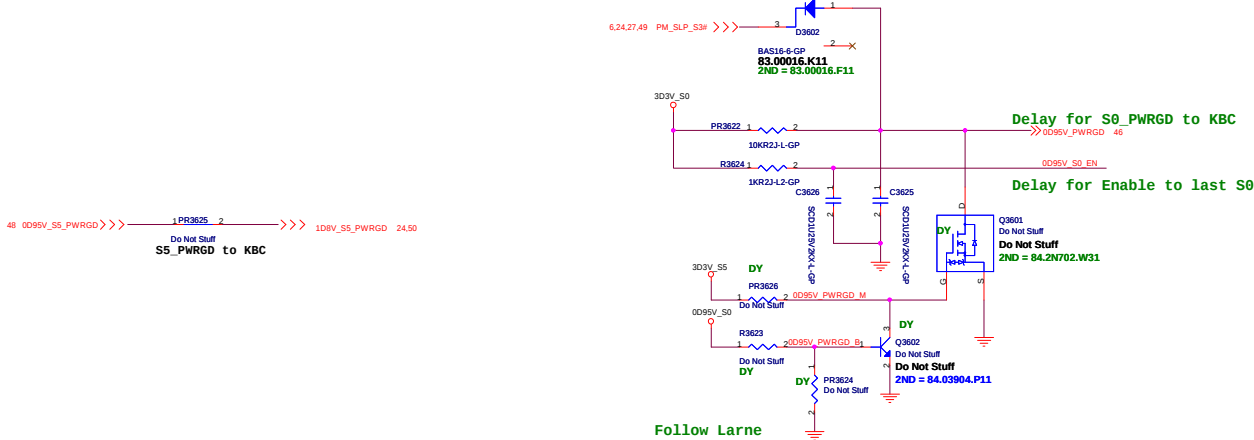
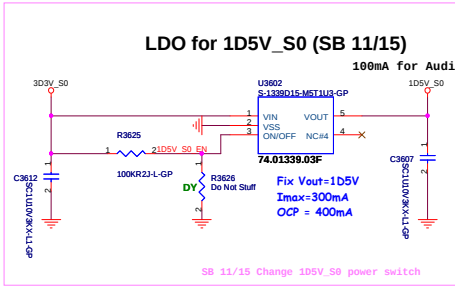
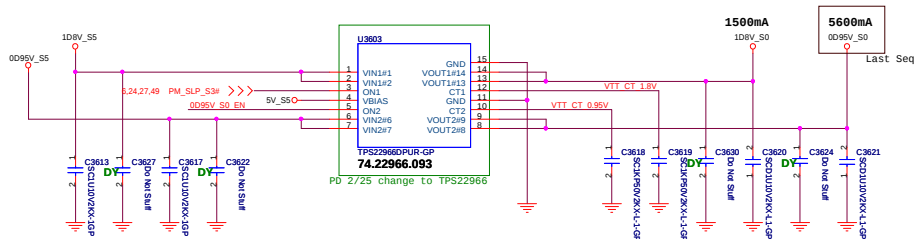
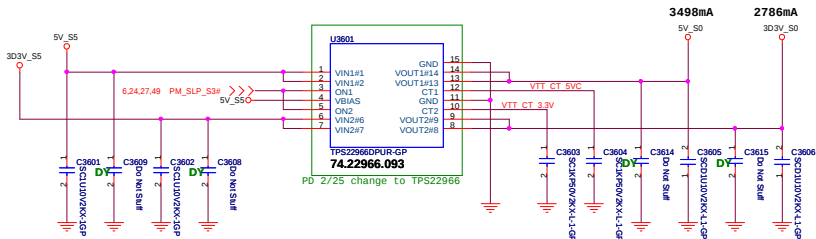
2/4 PD for Factory USB ESD issue.



1/28 PD for Factory USB ESD issue.

EAEG50 KB UMA

Power Sequence



ANNIE solution

Adaptor in to generate DCBATOUT

DCIN1

ACES-CON8-12-GP-U1

20.F0818.008
2nd = 20.F2348.008

PC4201
SCD1U50V3KX-L-GP

PD4201
P6SBMJ27APT-GP
83.P6SBM.DAG
2nd = 83.P6SMB.JAG
3rd = 83.P6SMB.CAG

AD_JK

PC4202
SC1U50V5ZY-1-GP

AD_OFF >>>

PQ4201
LTC024EUB-FS8-GP
84.00024.A1K
2ND = 84.00124.H1K
3rd = 84.05124.011

PWR ADJK EN

PQ4202
PDTA124EU-1-GP
84.00124.K1K
2nd = 84.00024.01K
3rd = 84.05124.A11

AD_JK

PR4201
200KR2F-L-GP

PC4203
SC1U50V5ZY-1-GP

PWR AD+ 2

PR4202
100KR2J-4-GP

PU4201
TPCC8131-GP
84.08131.037
2nd = 84.07129.037
SB 11/23 Raymond

PD 1/24 EMI request

EC4201
SCD1U50V3KX-L-GP

AD+

EAEG50 KB UMA

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Title

DCIN JACK

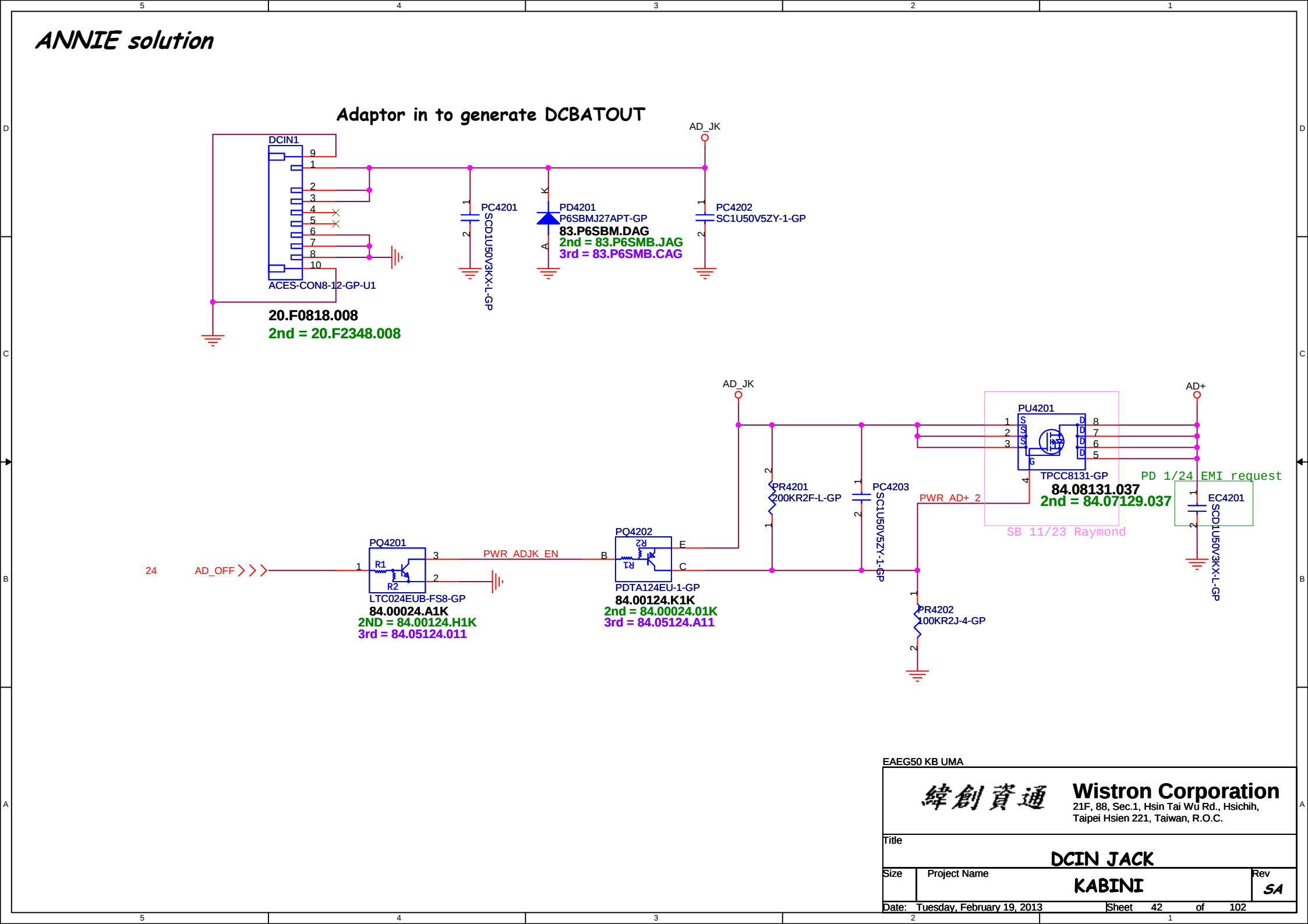
Size Project Name

KABINI

Date: Tuesday, February 19, 2013

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ANNIE solution

Adaptor in to generate DCBATOUT

The circuit diagram illustrates the power supply path for the ANNIE solution. It starts with DCIN1 connected to a multi-pin connector ACES-CON8-12-GP-U1. The signal path includes several capacitors (PC4201, PC4202, PC4203), a diode (PD4201), and two voltage regulators (PQ4201 and PQ4202). The output of the first regulator is labeled PWR ADJK EN, which connects to AD_JK. The second regulator's output is labeled PWR AD+ 2, which connects to AD+. A third capacitor (EC4201) is shown near the AD+ output. Various component values and part numbers are listed throughout the diagram.

Component Values and Part Numbers:

- DCIN1: 20.F0818.008
2nd = 20.F2348.008
- PC4201: SCOD1U50V3KK-L-GP
- PD4201: P6SBMJ27APT-GP
83.P6SMB.DAG
2nd = 83.P6SMB.JAG
3rd = 83.P6SMB.CAG
- PC4202: SC1U50V5ZY-1-GP
- PQ4201: LTC024EUB-FS8-GP
84.00024.A1K
2ND = 84.00124.H1K
3rd = 84.05124.011
- PQ4202: PDTA124EU-1-GP
84.00124.K1K
2nd = 84.00024.01K
3rd = 84.05124.A11
- PR4201: 200KR2F-L-GP
- PC4203: SC1U50V5ZY-1-GP
- PR4202: 100KR2J-4-GP
- PU4201: TPCC8131-GP
84.08131.037
2nd = 84.07129.037
SB 11/23 Raymond
- EC4201: SCOD1U50V3KK-L-GP

AD_OFF >>>

AD_JK

AD+

EMI request

EAEG50 KB UMA

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Title			
		DCIN JACK	
Size	Project Name	KABINI	Rev SA
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[illegible][illegible]

ANNIE solution

Adaptor in to generate DCBATOUT

DCIN1

ACES-CON8-12-GP-U1

20.F0818.008
2nd = 20.F2348.008

PC4201
SCD1U50V3KX-L-GP

PD4201
P6SBMJ27APT-GP
83.P6SBM.DAG
2nd = 83.P6SMB.JAG
3rd = 83.P6SMB.CAG

AD_JK

PC4202
SC1U50V5ZY-1-GP

AD_OFF >>>

PQ4201
LTC024EUB-FS8-GP
84.00024.A1K
2ND = 84.00124.H1K
3rd = 84.05124.011

PWR ADJK EN

PQ4202
PDTA124EU-1-GP
84.00124.K1K
2nd = 84.00024.01K
3rd = 84.05124.A11

AD_JK

PR4201
200KR2F-L-GP

PC4203
SC1U50V5ZY-1-GP

PWR AD+ 2

PR4202
100KR2J-4-GP

PU4201
TPCC8131-GP
84.08131.037
2nd = 84.07129.037
SB 11/23 Raymond

PD 1/24 EMI request

EC4201
SCD1U50V3KX-L-GP

AD+

EAEG50 KB UMA

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Title

DCIN JACK

Size Project Name

KABINI

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ANNIE solution

Adaptor in to generate DCBATOUT

DCIN1

ACES-CON8-12-GP-U1

20.F0818.008
2nd = 20.F2348.008

PC4201
SCD1U50V3KX-L-GP

PD4201
P6SBMJ27APT-GP
83.P6SBM.DAG
2nd = 83.P6SMB.JAG
3rd = 83.P6SMB.CAG

AD_JK

PC4202
SC1U50V5ZY-1-GP

AD_OFF >>>

PQ4201
LTC024EUB-FS8-GP
84.00024.A1K
2ND = 84.00124.H1K
3rd = 84.05124.011

PWR ADJK EN

PQ4202
PDTA124EU-1-GP
84.00124.K1K
2nd = 84.00024.01K
3rd = 84.05124.A11

AD_JK

PR4201
200KR2F-L-GP

PC4203
SC1U50V5ZY-1-GP

PWR AD+ 2

PR4202
100KR2J-4-GP

PU4201
TPCC8131-GP
84.08131.037
2nd = 84.07129.037
SB 11/23 Raymond

PD 1/24 EMI request

EC4201
SCD1U50V3KX-L-GP

AD+

EAEG50 KB UMA

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Title

DCIN JACK

Size Project Name

KABINI

Date: Tuesday, February 19, 2013 Sheet 42 of 102

Rev SA

ANNIE solution

Adaptor in to generate DCBATOUT

DCIN1

ACES-CON8-12-GP-U1

20.F0818.008
2nd = 20.F2348.008

PC4201
SCD1U50V3KX-L-GP

PD4201
P6SBMJ27APT-GP
83.P6SBM.DAG
2nd = 83.P6SMB.JAG
3rd = 83.P6SMB.CAG

AD_JK

PC4202
SC1U50V5ZY-1-GP

AD_OFF >>>

PQ4201
LTC024EUB-FS8-GP
84.00024.A1K
2ND = 84.00124.H1K
3rd = 84.05124.011

PWR ADJK EN

PQ4202
PDTA124EU-1-GP
84.00124.K1K
2nd = 84.00024.01K
3rd = 84.05124.A11

AD_JK

PR4201
200KR2F-L-GP

PC4203
SC1U50V5ZY-1-GP

PWR AD+ 2

PR4202
100KR2J-4-GP

PU4201
TPCC8131-GP
84.08131.037
2nd = 84.07129.037
SB 11/23 Raymond

PD 1/24 EMI request

EC4201
SCD1U50V3KX-L-GP

AD+

EAEG50 KB UMA

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Title

DCIN JACK

Size Project Name

KABINI

Date: Tuesday, February 19, 2013 Sheet 42 of 102

Rev SA

ANNIE solution

Adaptor in to generate DCBATOUT

DCIN1

ACES-CON8-12-GP-U1

20.F0818.008
2nd = 20.F2348.008

PC4201
SCD1U50V3KX-L-GP

PD4201
P6SBMJ27APT-GP
83.P6SBM.DAG
2nd = 83.P6SMB.JAG
3rd = 83.P6SMB.CAG

AD_JK

PC4202
SC1U50V5ZY-1-GP

AD_OFF >>>

PQ4201
LTC024EUB-FS8-GP
84.00024.A1K
2ND = 84.00124.H1K
3rd = 84.05124.011

PWR ADJK EN

PQ4202
PDTA124EU-1-GP
84.00124.K1K
2nd = 84.00024.01K
3rd = 84.05124.A11

AD_JK

PR4201
200KR2F-L-GP

PC4203
SC1U50V5ZY-1-GP

PWR AD+ 2

PR4202
100KR2J-4-GP

PU4201
TPCC8131-GP
84.08131.037
2nd = 84.07129.037
SB 11/23 Raymond

PD 1/24 EMI request

EC4201
SCD1U50V3KX-L-GP

AD+

EAEG50 KB UMA

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Title

DCIN JACK

Size Project Name

KABINI

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ANNIE solution

Adaptor in to generate DCBATOUT

DCIN1

ACES-CON8-12-GP-U1

20.F0818.008
2nd = 20.F2348.008

PC4201
SCD1U50V3KX-L-GP

PD4201
P6SBMJ27APT-GP
83.P6SBM.DAG
2nd = 83.P6SMB.JAG
3rd = 83.P6SMB.CAG

AD_JK

PC4202
SC1U50V5ZY-1-GP

AD_OFF >>>

PQ4201
LTC024EUB-FS8-GP
84.00024.A1K
2ND = 84.00124.H1K
3rd = 84.05124.011

PWR ADJK EN

PQ4202
PDTA124EU-1-GP
84.00124.K1K
2nd = 84.00024.01K
3rd = 84.05124.A11

AD_JK

PR4201
200KR2F-L-GP

PC4203
SC1U50V5ZY-1-GP

PWR AD+ 2

PR4202
100KR2J-4-GP

PU4201
TPCC8131-GP
84.08131.037
2nd = 84.07129.037
SB 11/23 Raymond

PD 1/24 EMI request

EC4201
SCD1U50V3KX-L-GP

AD+

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Title

DCIN JACK

Size Project Name

KABINI

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ANNIE solution

Adaptor in to generate DCBATOUT

DCIN1

9

1

2

3

4

5

6

7

8

10

ACES-CON8-12-GP-U1

20.F0818.008

2nd = 20.F2348.008

PC4201

SCD1U50V3KX-L-GP

PD4201

P6SBMJ27APT-GP

83.P6SBM.DAG

2nd = 83.P6SMB.JAG

3rd = 83.P6SMB.CAG

AD_JK

PC4202

SC1U50V5ZY-1-GP

AD_JK

PR4201

200KR2F-L-GP

PC4203

SC1U50V5ZY-1-GP

PWR AD+ 2

PR4202

100KR2J-4-GP

PU4201

TPCC8131-GP

84.08131.037

2nd = 84.07129.037

PD 1/24 EMI request

EC4201

SCD1U50V3KX-L-GP

AD+

AD_OFF >>>

PQ4201

LTC024EUB-FS8-GP

84.00024.A1K

2ND = 84.00124.H1K

3rd = 84.05124.011

PQ4202

PDTA124EU-1-GP

84.00124.K1K

2nd = 84.00024.01K

3rd = 84.05124.A11

SB 11/23 Raymond

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Title

DCIN JACK

Size Project Name

KABINI

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ANNIE solution

Adaptor in to generate DCBATOUT

DCIN1

9

1

2

3

4

5

6

7

8

10

ACES-CON8-12-GP-U1

20.F0818.008

2nd = 20.F2348.008

PC4201

SCD1U50V3KX-L-GP

PD4201

P6SBMJ27APT-GP

83.P6SBM.DAG

2nd = 83.P6SMB.JAG

3rd = 83.P6SMB.CAG

AD_JK

PC4202

SC1U50V5ZY-1-GP

AD_JK

PR4201

200KR2F-L-GP

PC4203

SC1U50V5ZY-1-GP

PQ4201

LTC024EUB-FS8-GP

84.00024.A1K

2ND = 84.00124.H1K

3rd = 84.05124.011

AD_OFF >>>

PWR ADJK EN

PQ4202

PDTA124EU-1-GP

84.00124.K1K

2nd = 84.00024.01K

3rd = 84.05124.A11

AD_JK

PR4202

100KR2J-4-GP

PW AD+ 2

PU4201

TPCC8131-GP

84.08131.037

2nd = 84.07129.037

PD 1/24 EMI request

SB 11/23 Raymond

EC4201

SCD1U50V3KX-L-GP

AD+

EAEG50 KB UMA

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Title

DCIN JACK

Size Project Name

KABINI

Rev

SA

Date: Tuesday, February 19, 2013

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```

86      BATA_SDA_1>>>_____
86      BATA_SCL_1>>>_____
86      BAT_IN#_1  >>>_____
86      BAT_G      >>>_____

```

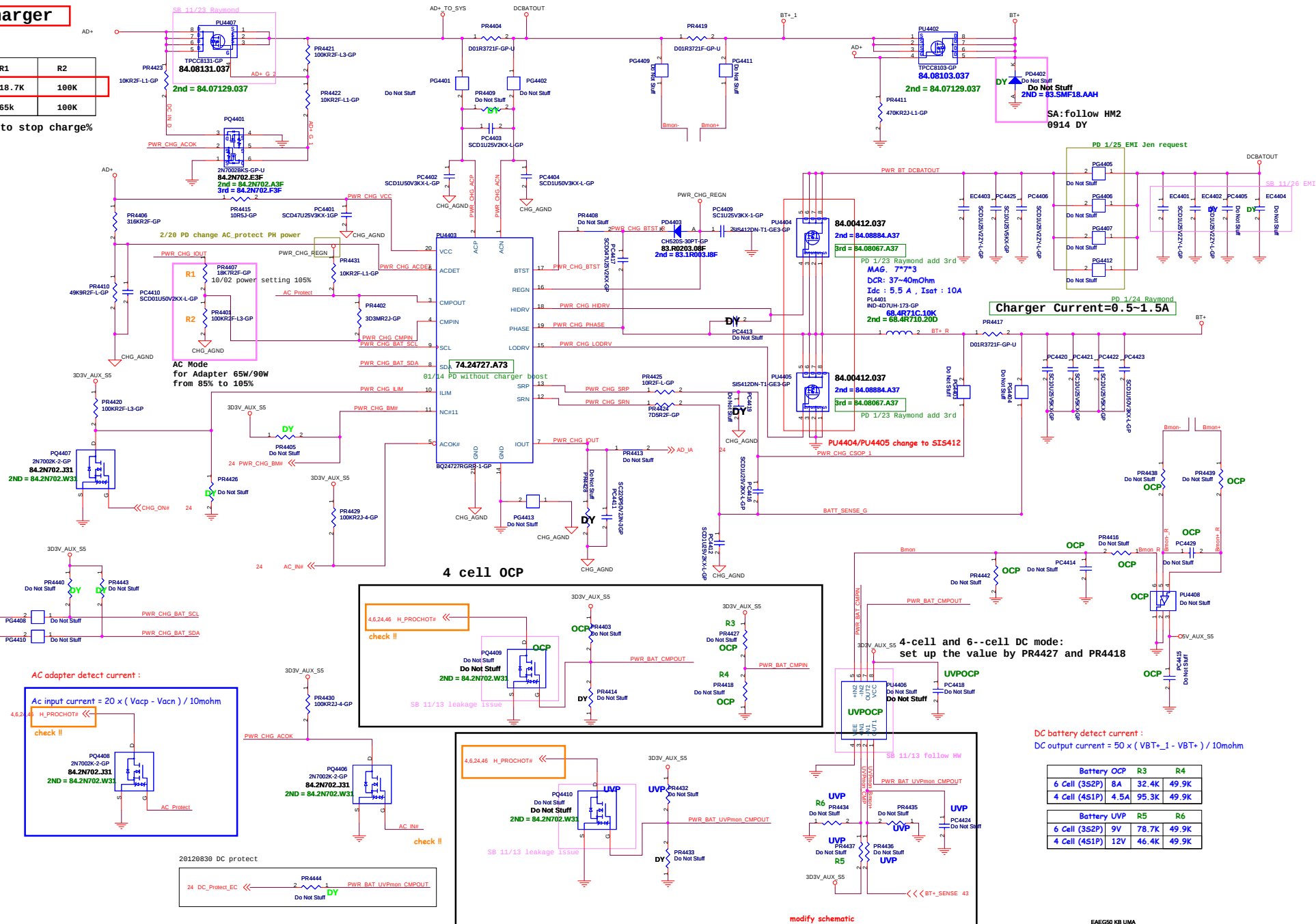
[illegible]

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
BATT CONN KABINI	
Size	Project Name KABINI
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PR4407, PR4401

AD+ total power	R1	R2
65w 105%	18.7K	100K
90w	65k	100K

Change the table to stop charge%



4 cell UVP

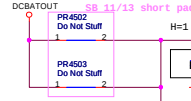
SSID = PWR.Plane.Regulator_3p3v5v

Cut off itself

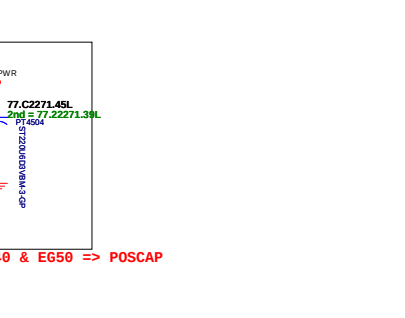
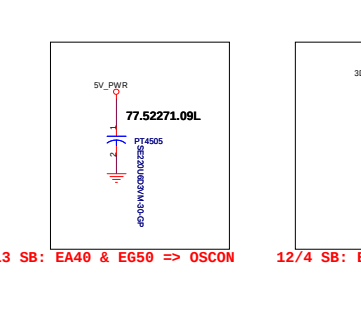
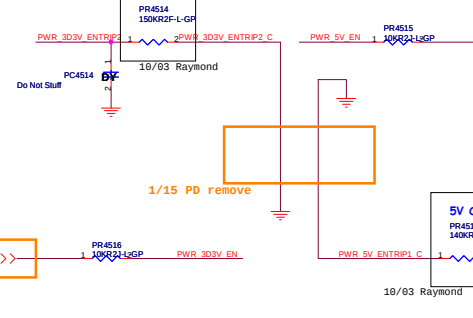
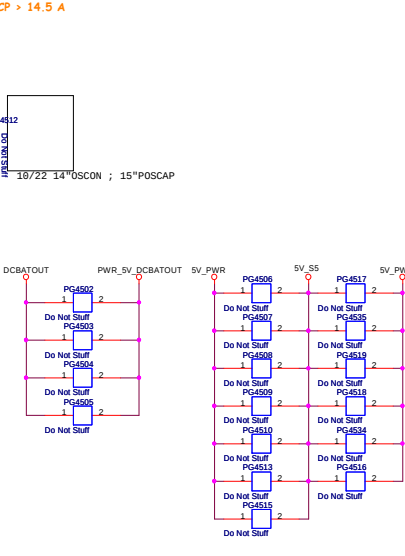
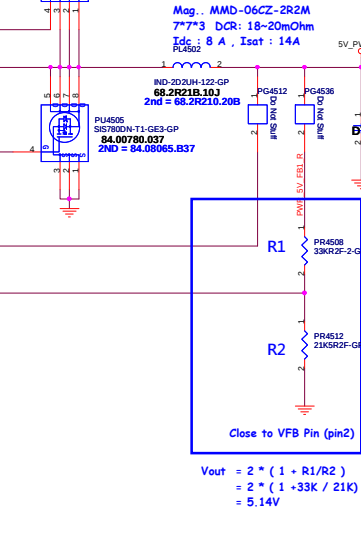
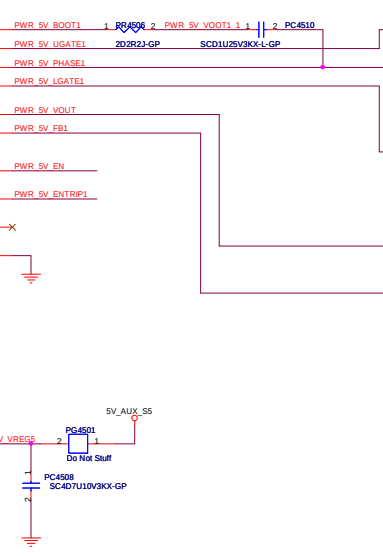
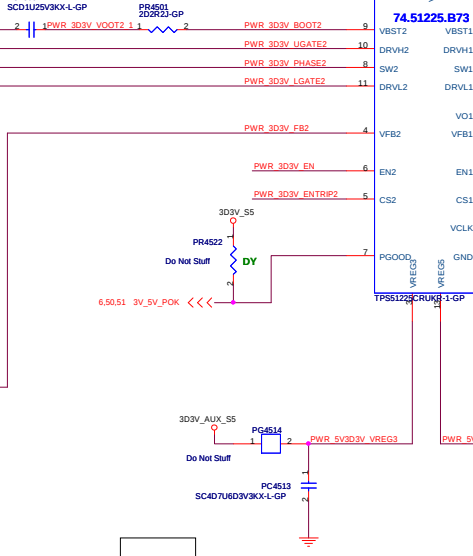
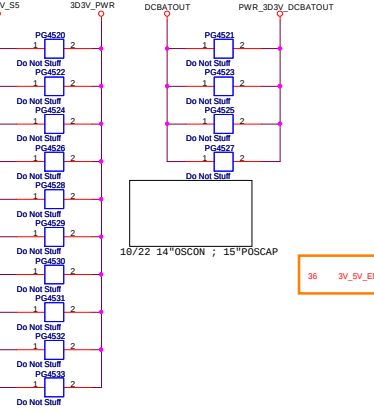
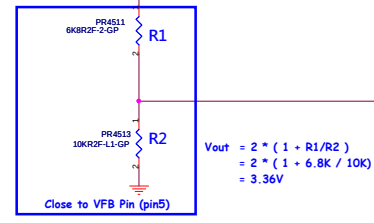
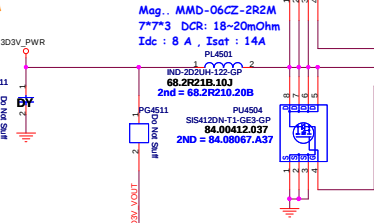
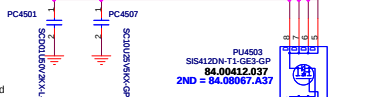
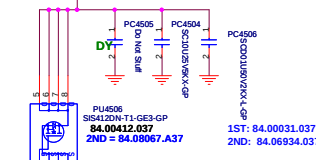
check (UVP)

check (DCBATOUT)

check (DCBATOUT)



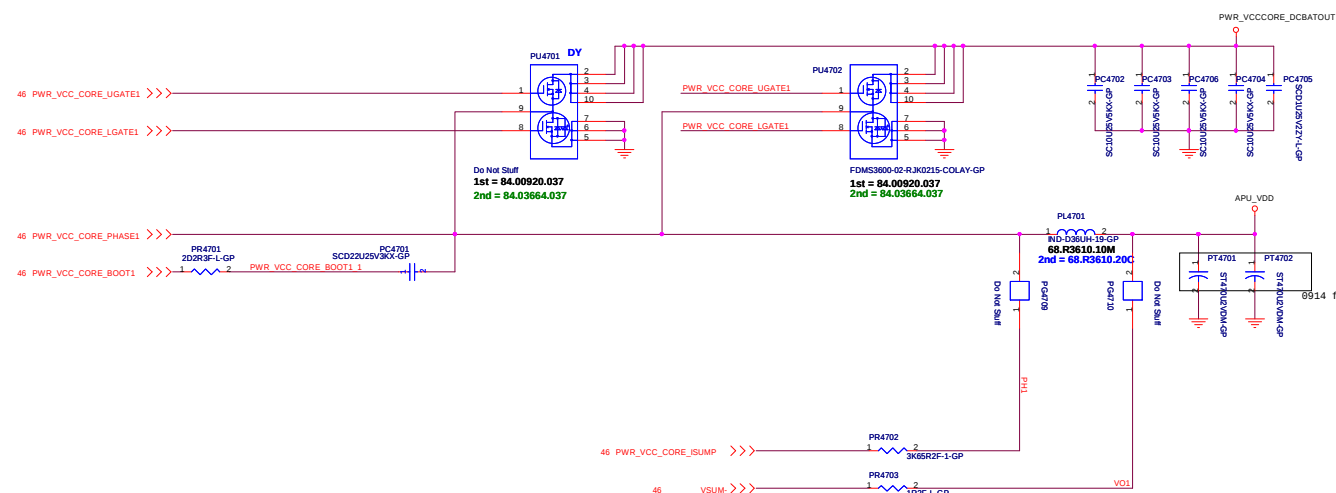
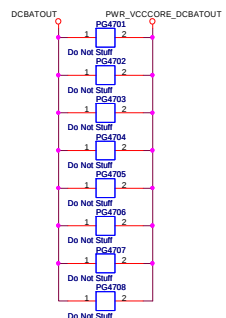
check (DCBATOUT)



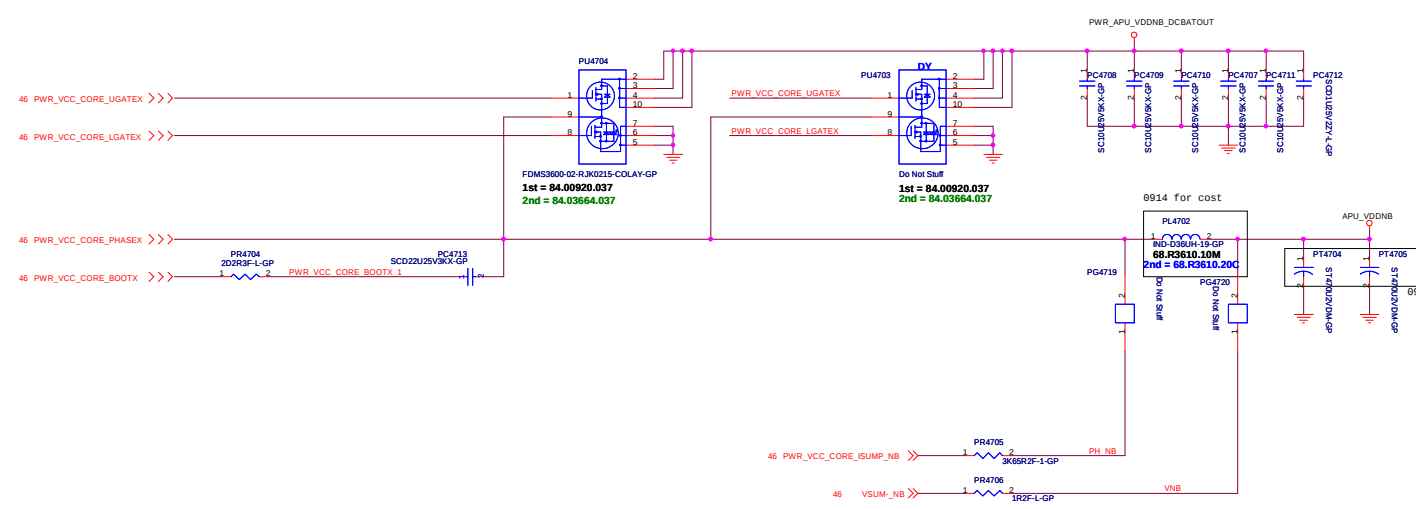
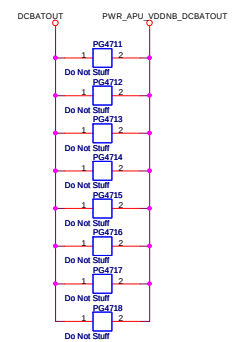
EAE650 KB UMA

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

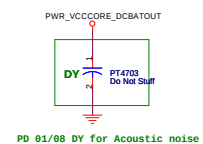
TPS51225 5V/3D3V			
KABINI			
Size	Document Number	Rev	
A2			
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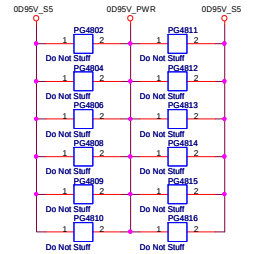
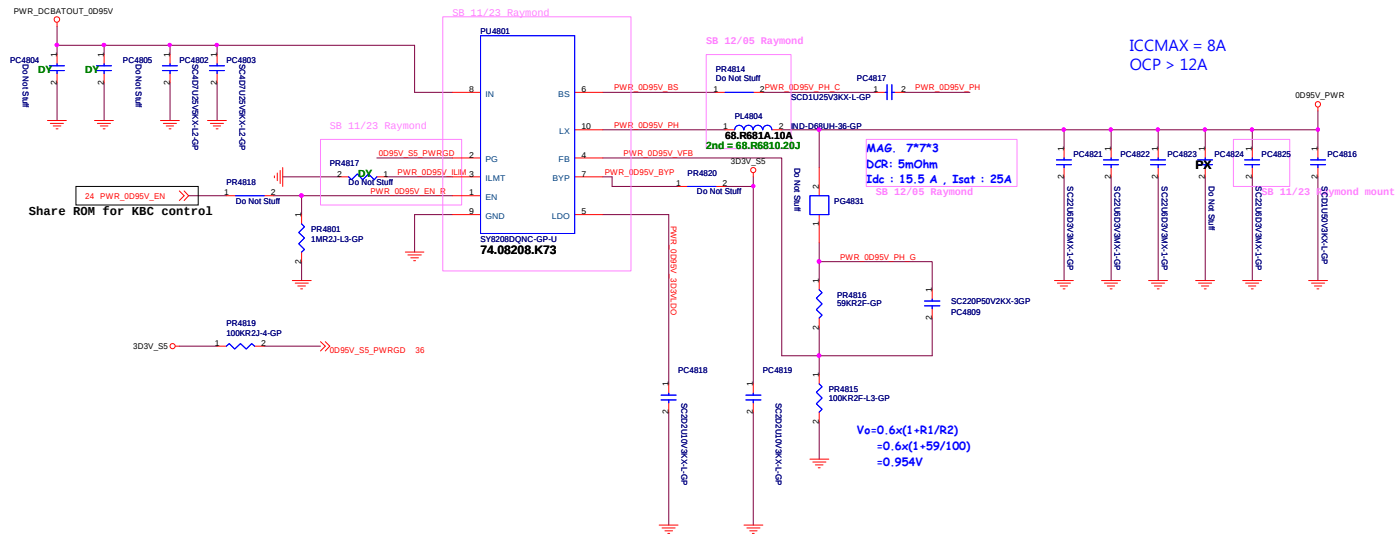
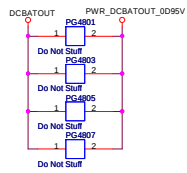


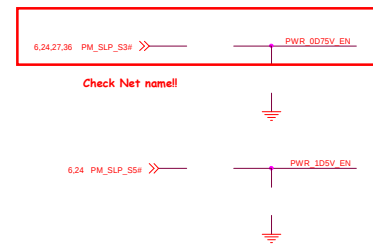
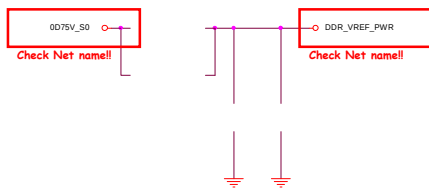
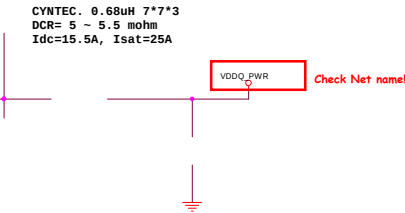
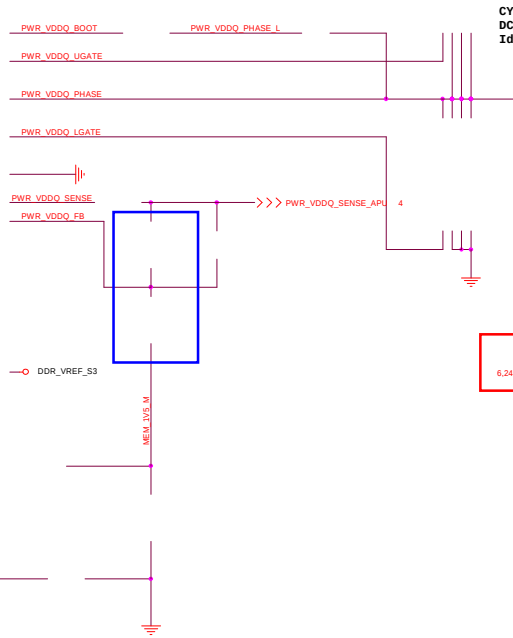
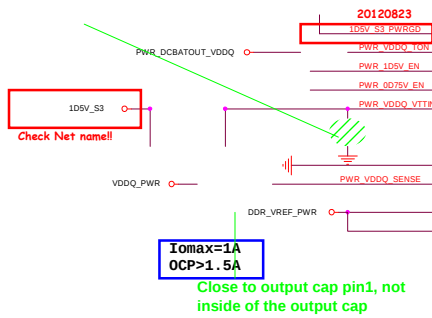
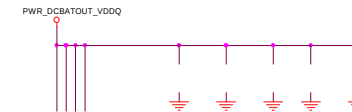
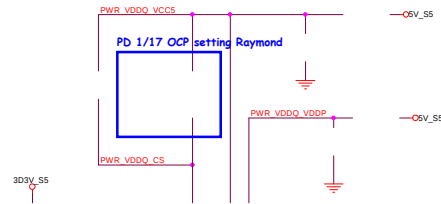
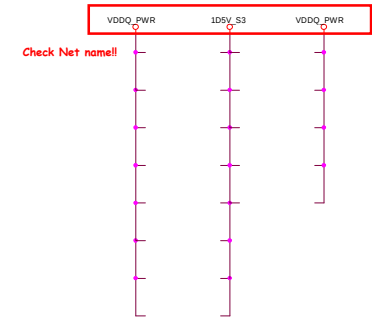
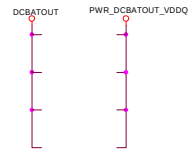
Iccmax=21A
TDC=16.8A
OCP>26.3A



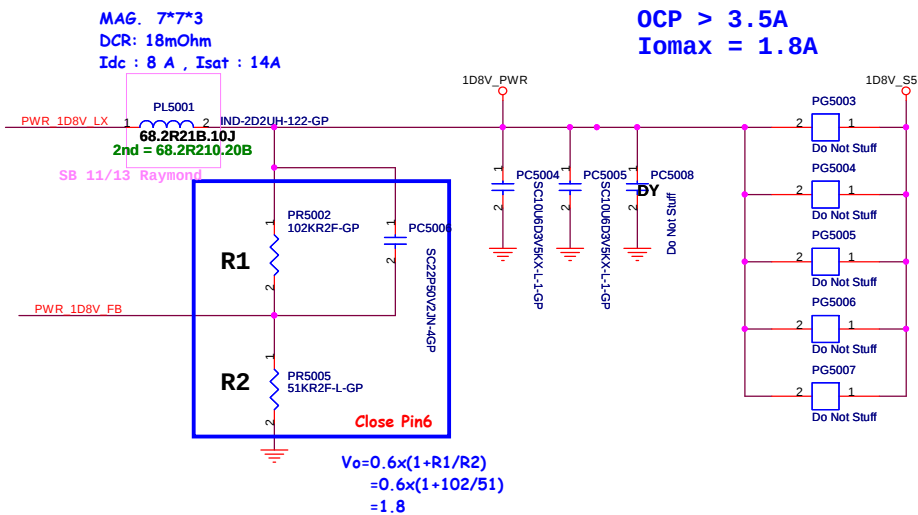
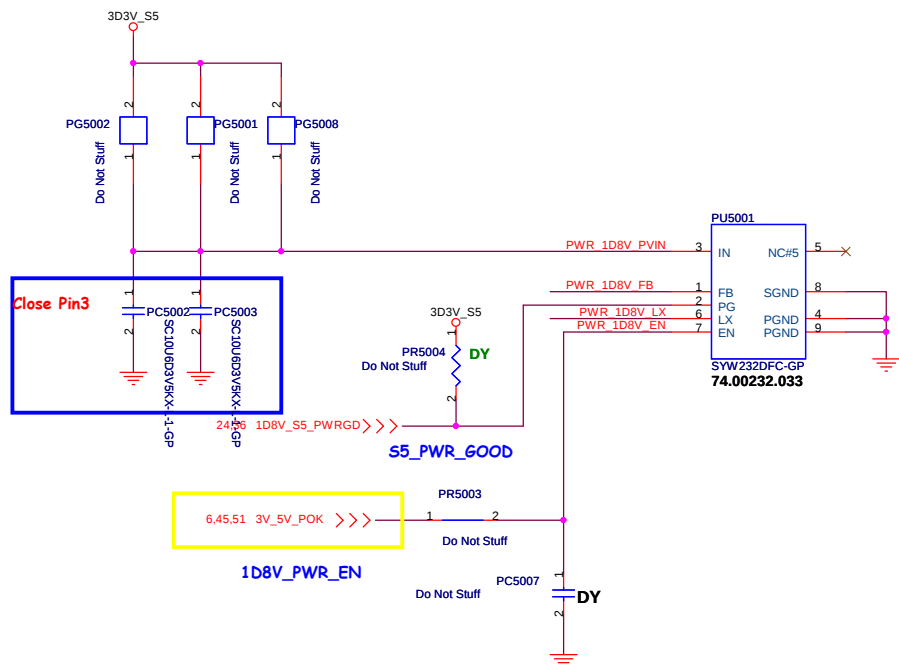
Iccmax=17A
TDC=13.6A
OCP>21.3A



[illegible]



SSID = PWR.Plane.Regulator_1p8v



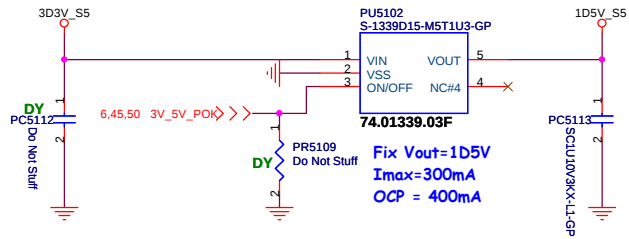
EAEG50 KB UMA

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Taipei Hsien 221, Taiwan, R.O.C.

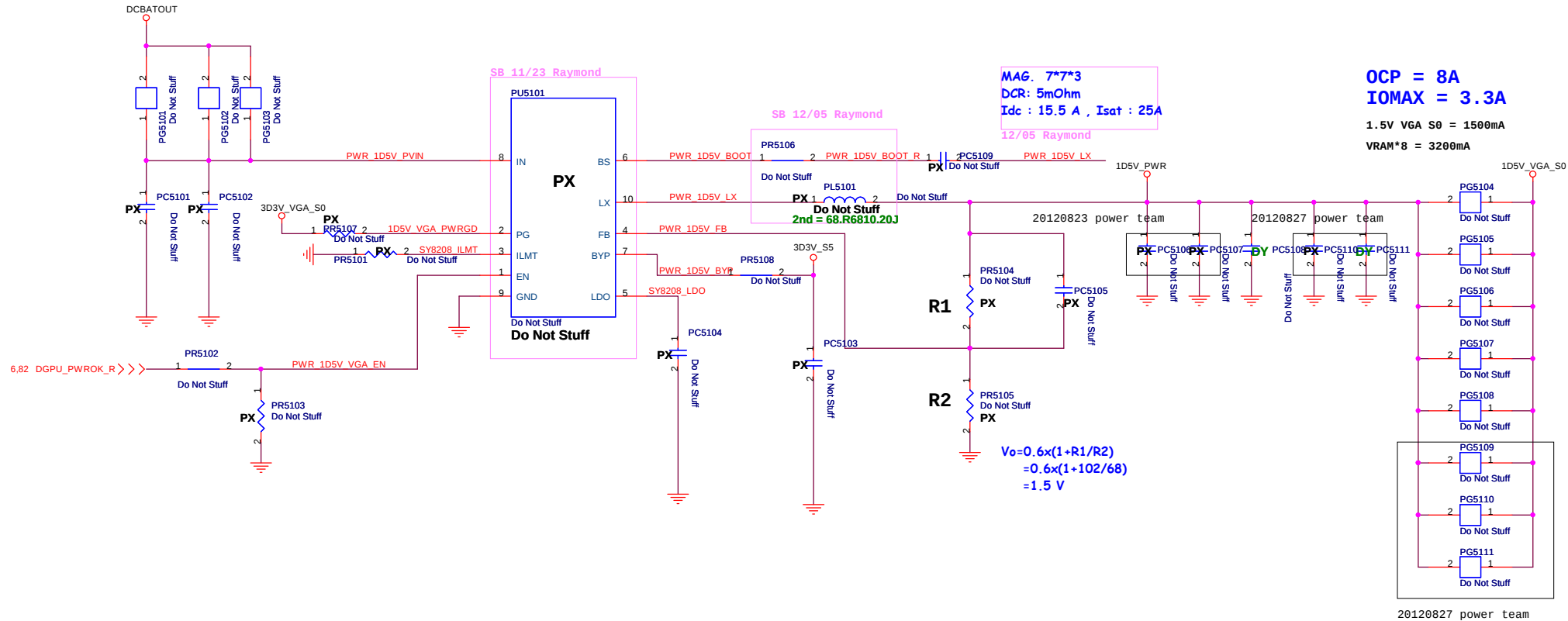
Title			1D8V_S0 SYW232	
Size	Document Number	KABINI		Rev
A3				
Date:	Monday, February 04, 2013	Sheet	50	of 102

LDO for 1D5V_S5 (SB 11/13)

1.5V S0 = 100mA(VDDIO_AZ) + 100mA(Audio) + 600mA(Minicard DY) = 200mA



SY8208D for 1D5V_VGA_S0 (SB 11/13)



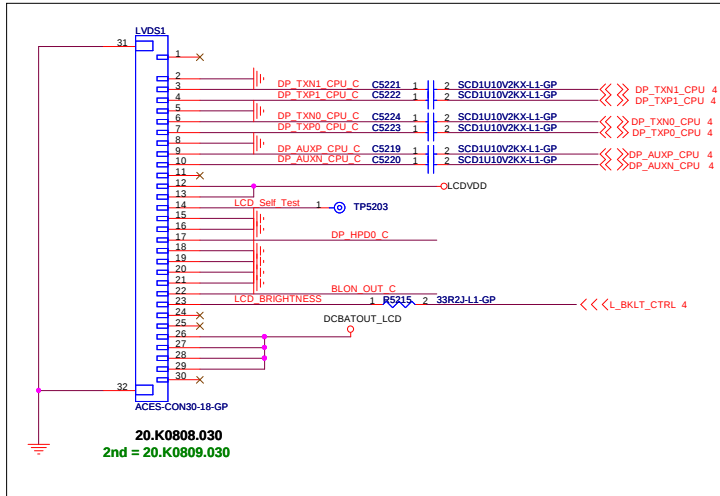
EAEG50 KB UMA

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Title			1D5V_S5 SY8208D
Size	Document Number	KABINI	
A3			
Date:	Tuesday, February 19, 2013	Sheet	51 of 102

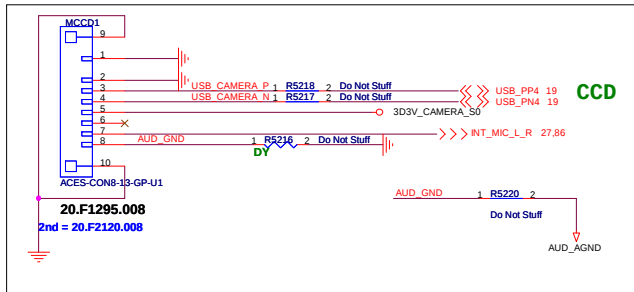
SSID = VIDEO

eDP Conn.



10/04 change to 20.K0808.030 for ME request

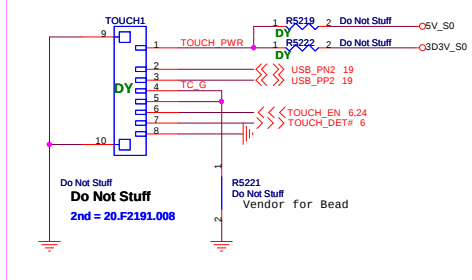
Camera+MIC Conn.



10/03 change to 8pin for del DMIC

10/15 change to 20.F1295.008 follow HW

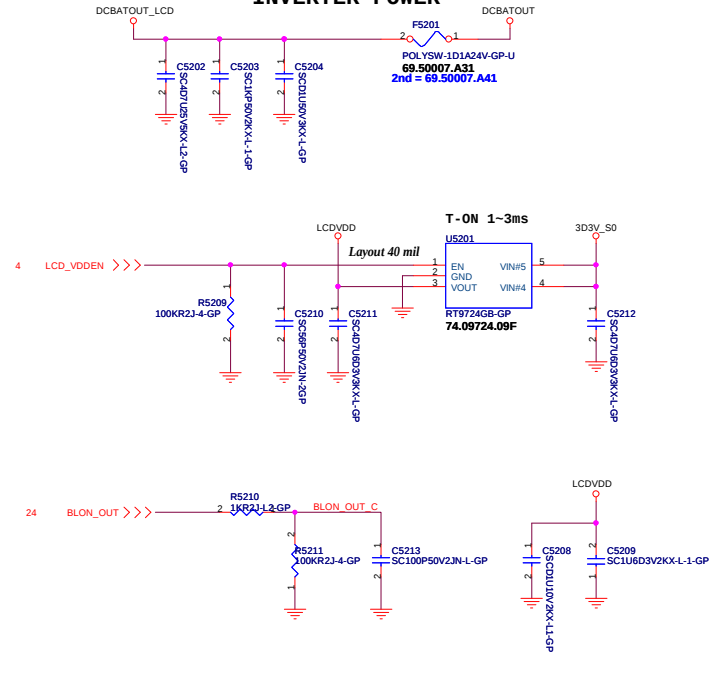
Touch Conn.



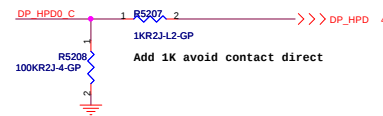
SB 12/12 DUMMY for ME issue

SC NO support

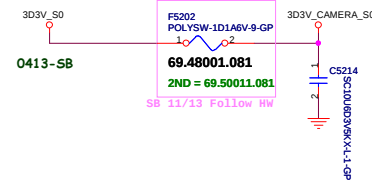
INVERTER POWER



EDP HPD High active



Camera Power



86 AUD_GND <<<
86 DP_HP00_C >>>
86 BLON_OUT_C >>>
86 LCD_BRIGHTNESS >>>
86 DP_TXN1_CPU_C >>>
86 DP_TXP1_CPU_C >>>
86 DP_TXN0_CPU_C >>>
86 DP_TXP0_CPU_C >>>
86 DP_AUXP_CPU_C <<<
86 DP_AUXN_CPU_C <<<

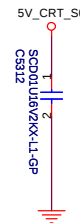
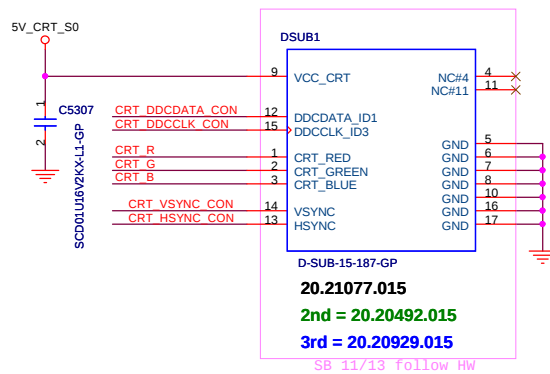
For AFTE

EAEG50 KB UMA

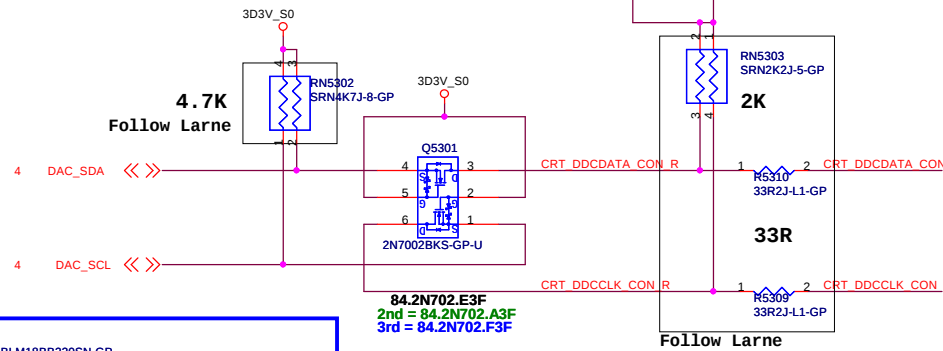
緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

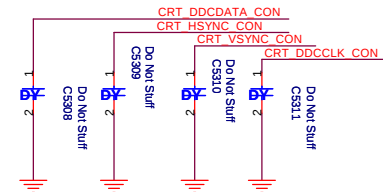
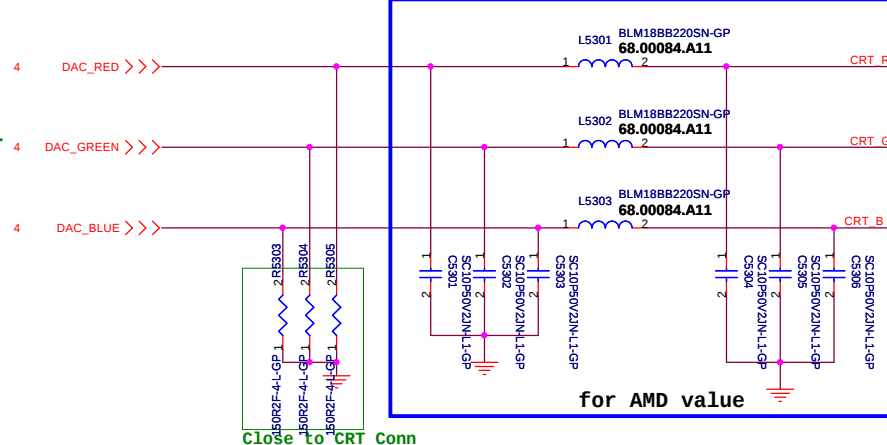
Title			LCD Connector
Size	Project Name	KABINI	Rev SA
Date	Monday, February 25, 2013	Sheet 52	of 102



CRT DDCDATA & DDCCLK level shift

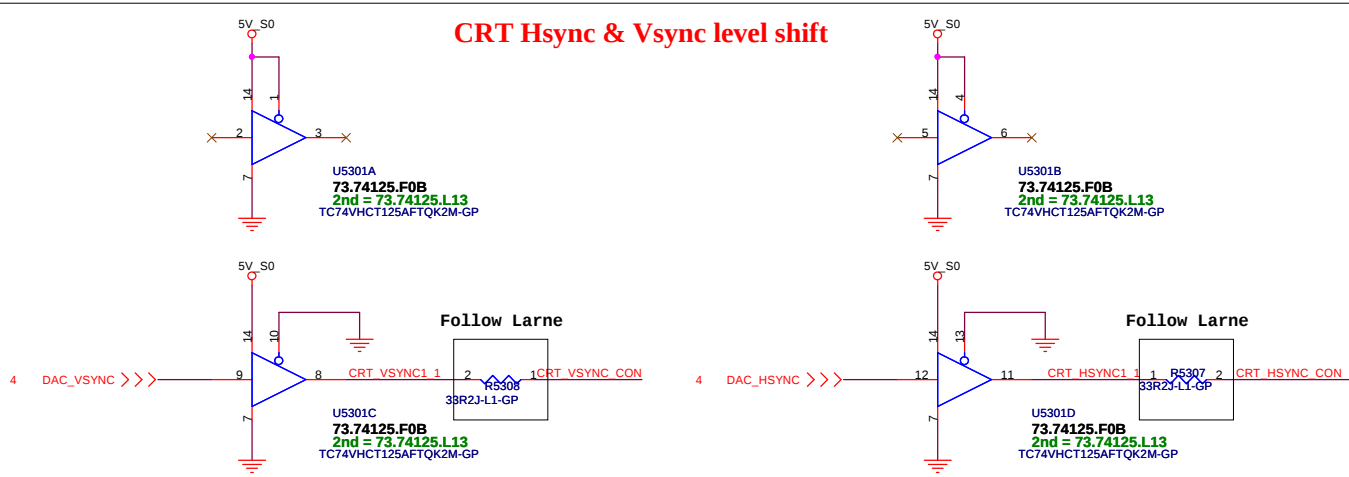


APU to CRT



10/16 follow COMAL

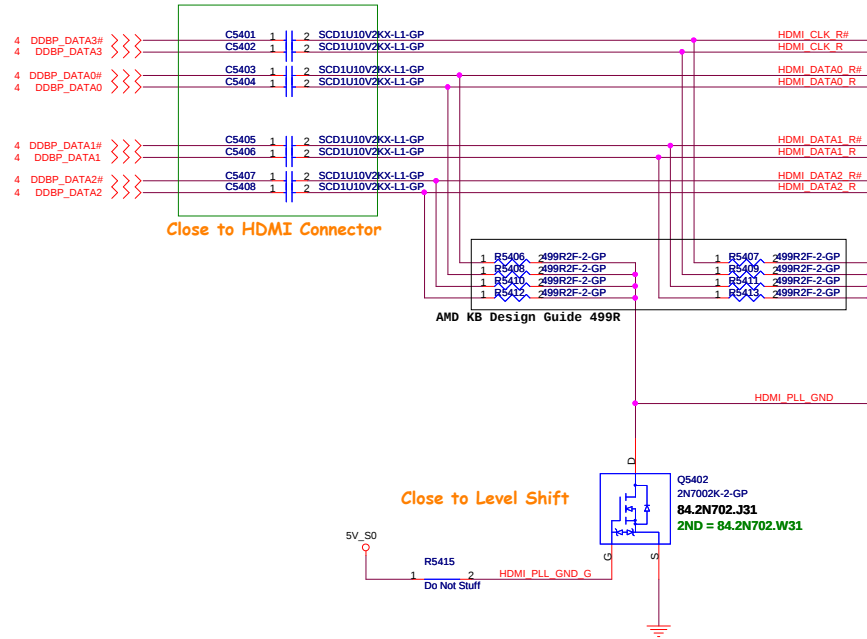
CRT Hsync & Vsync level shift



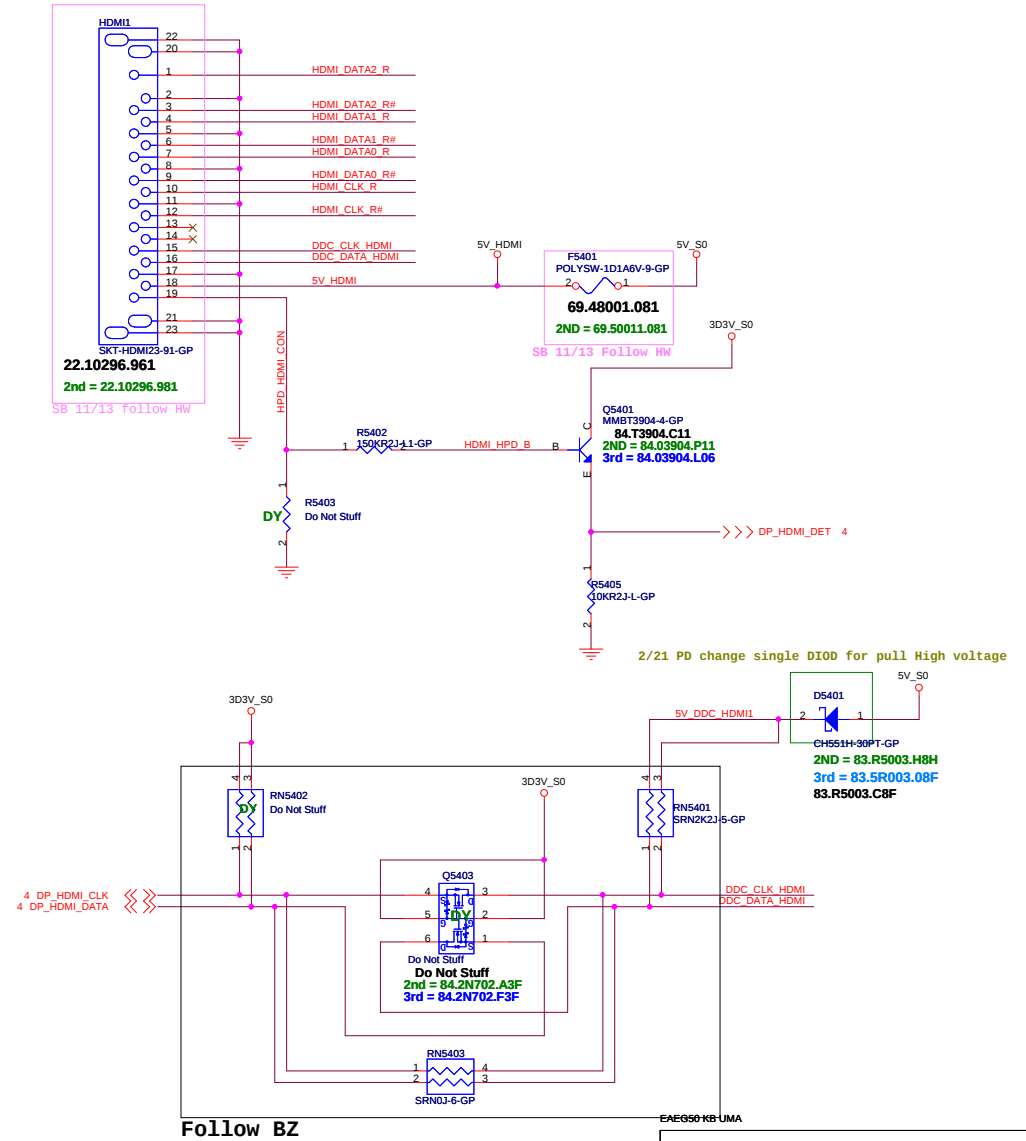
EAEG50 KB UMA

SSID = VIDEO

HDMI Level Shifter & CONNECTOR



HDMI CONN

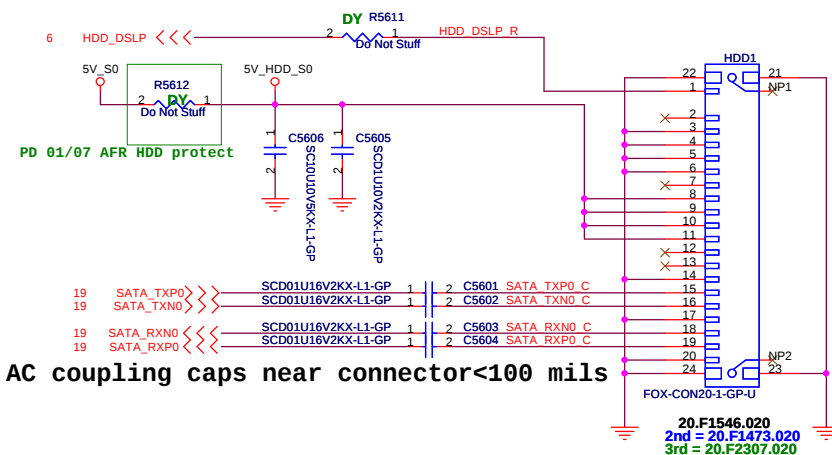
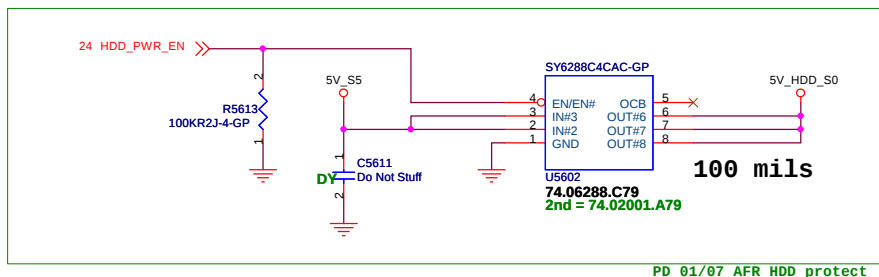


緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title			
HDMI Level Shifter/Connector			
Size	Project Name	Rev	
	KABINI	SA	
Date: Thursday, February 21, 2013		Sheet 54	of 102

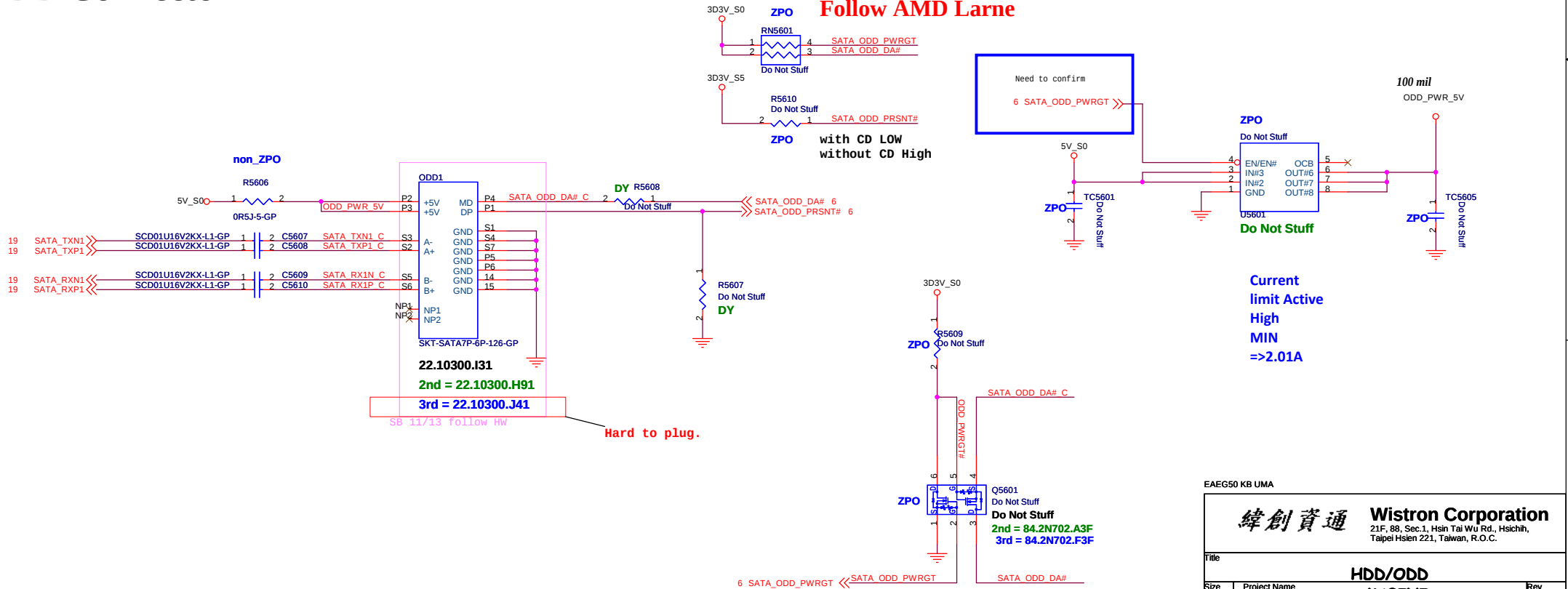
SSID = SATA

SATA HDD Connector

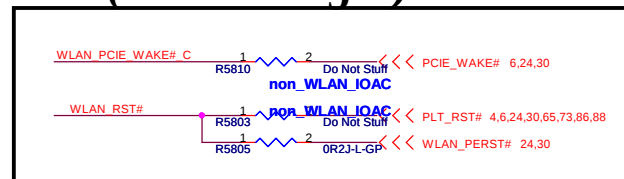
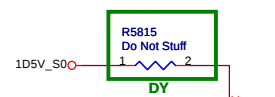


ODD Connector

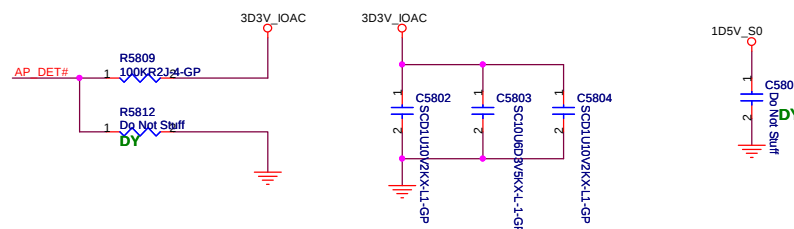
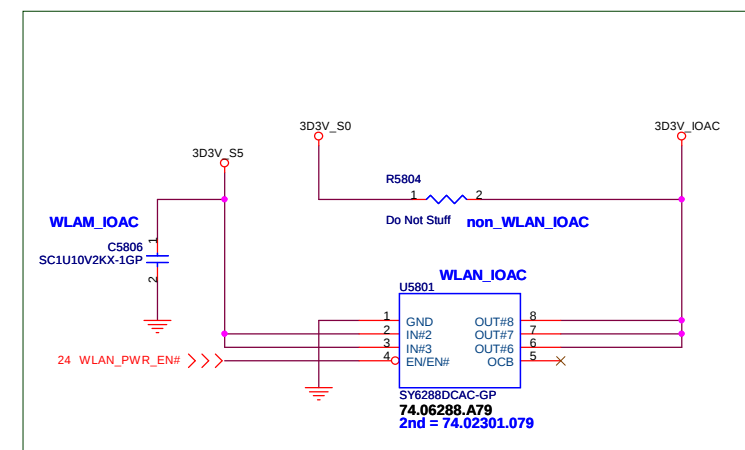
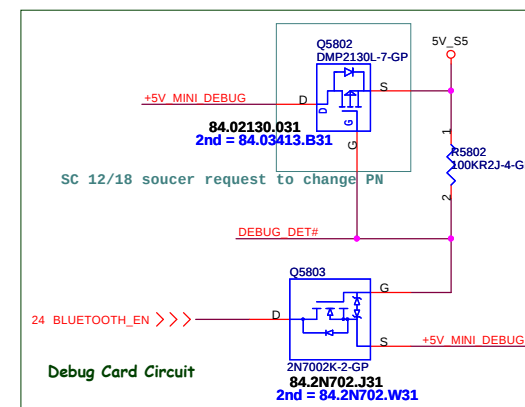
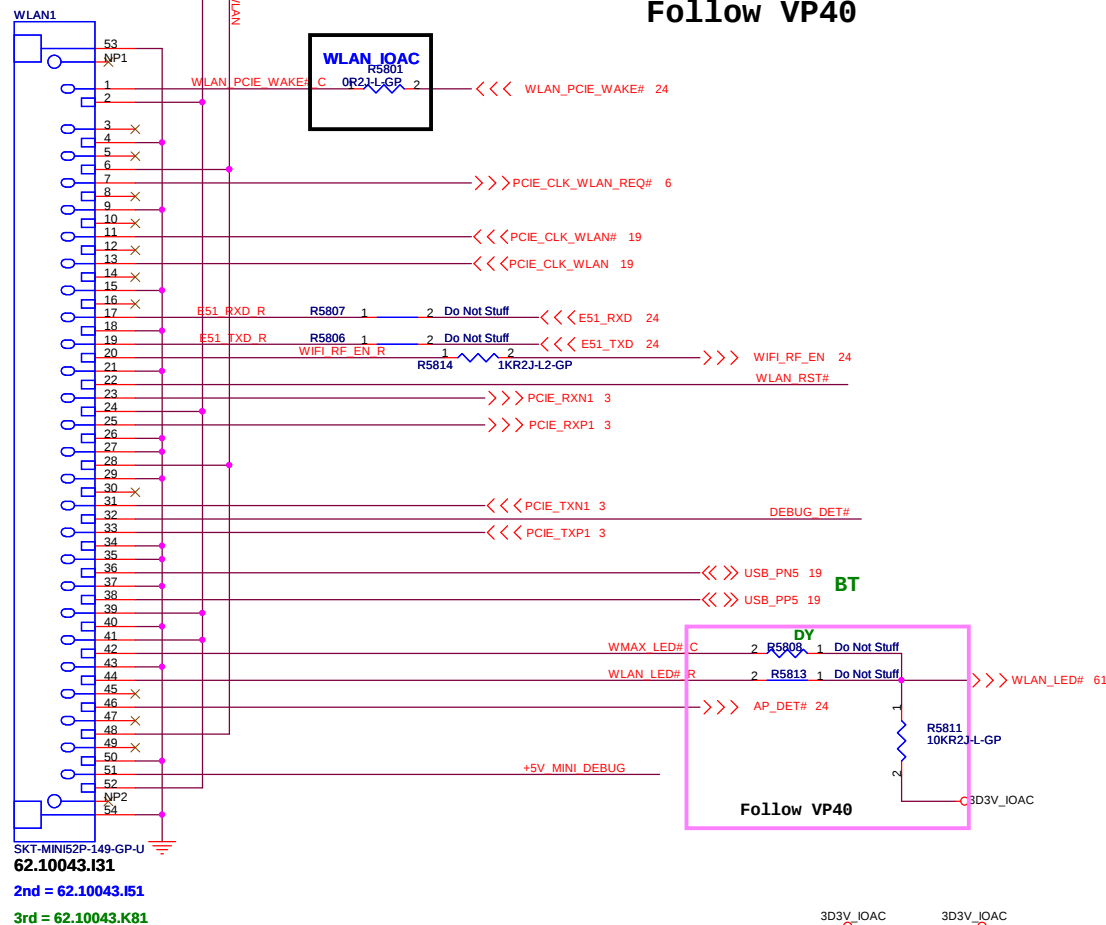
SATA Zero Power ODD Follow AMD Larne



Mini Card Connector(802.11a/b/g/n)



Follow VP40



SSID = Wireless

Mini Card Connector(WWAN)

EAEG50 KB UMA

緯創資通

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Title

WWAN CONN

Size

Project Name

KABINI

Rev

SA

Date: Friday, September 07, 2012

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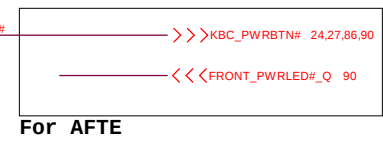
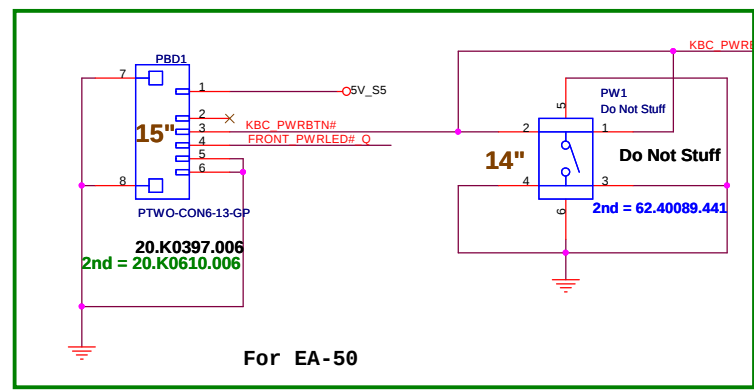
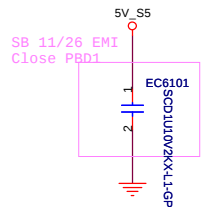
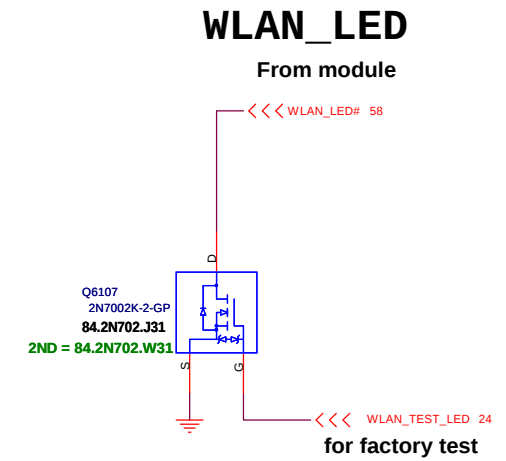
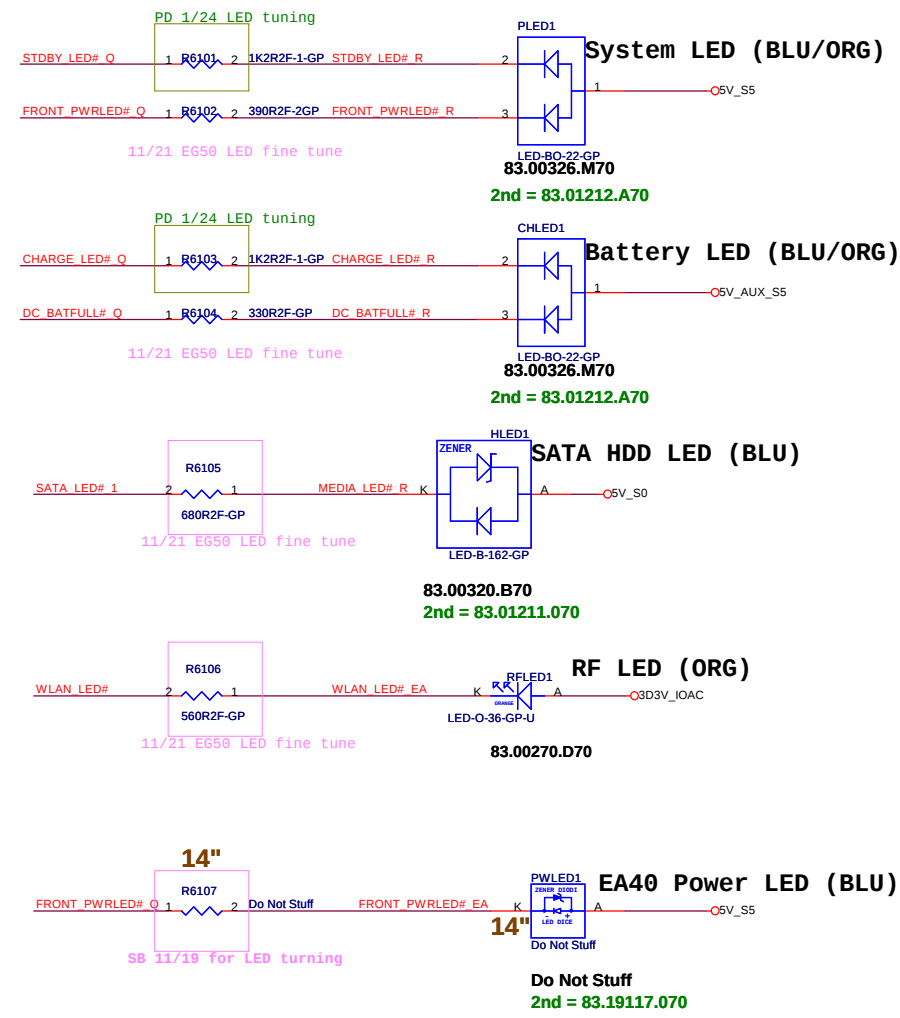
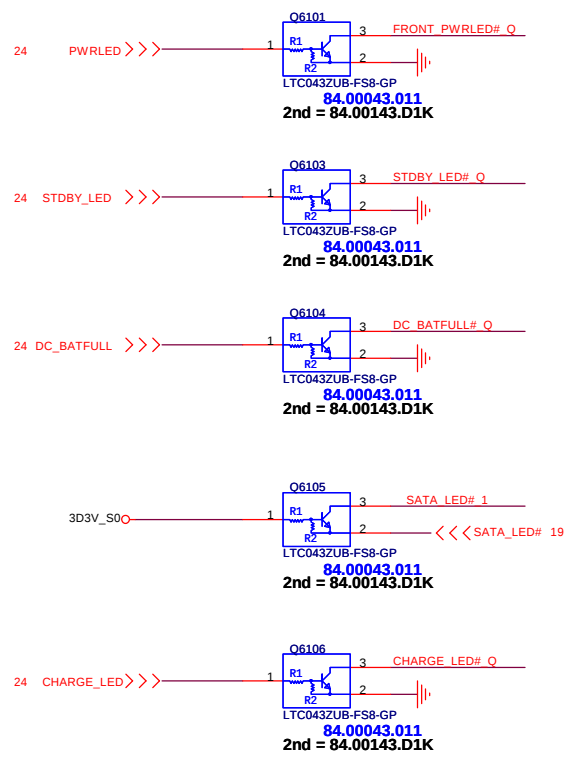
SSID = mSATA

Mini Card Connector(mSATA)

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緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title mSATA Connector		
Size	Project Name KABINI	Rev SA
Date: Friday, September 07, 2012		Sheet 60 of 102

SSID = User.Interface

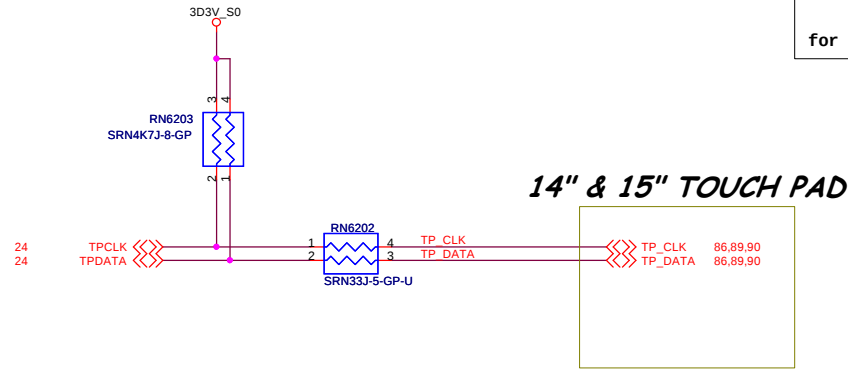


SSID = KBC

Internal KeyBoard Connector

86,89,90 TP_DATA >>>
86,89,90 TP_CLK >>>
86,89,90 SWR >>>
86,89,90 SWL >>>

for AFTP



PD 1/14 Different 14" & 15" TOUCH PAD reversion

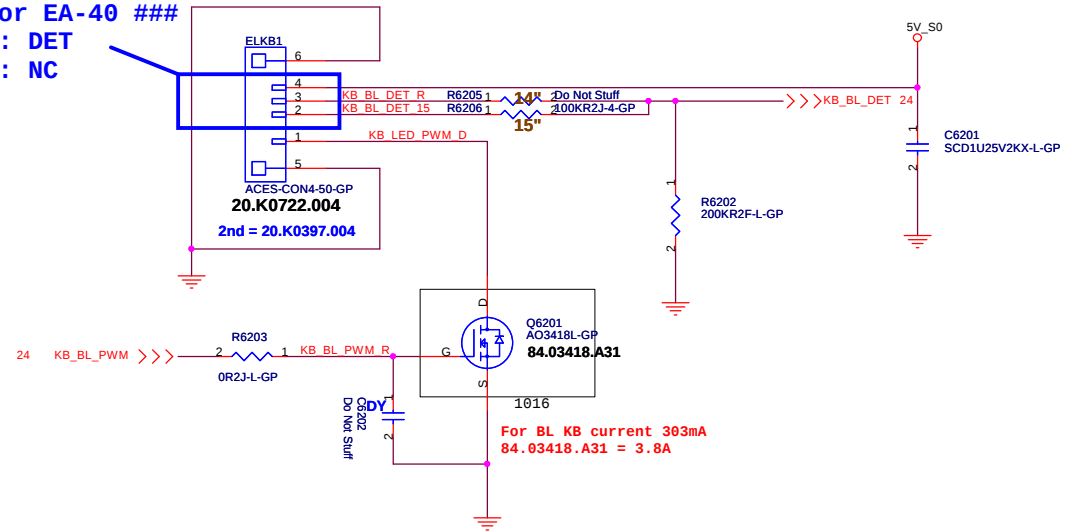
14"& 15" use the same KB

for EA/EG-50

Pin3 : NC
Pin2 : DET

for EA-40

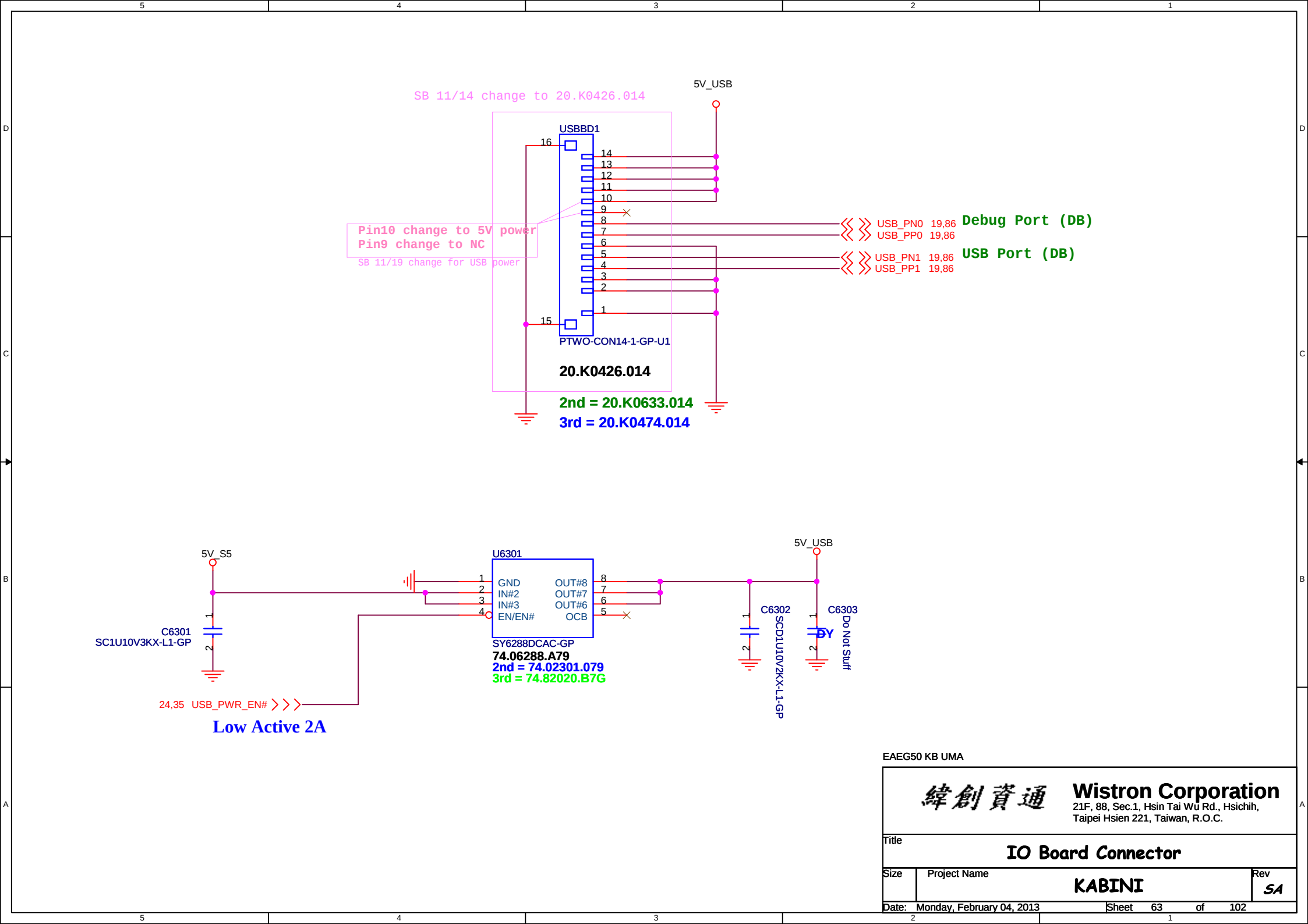
Pin3 : DET
Pin2 : NC



EAEG50 KB UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title Key Board/Touch Pad
Size Project Name KABINI Rev SA
Date: Tuesday, February 19, 2013 Sheet 62 of 102

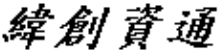


Sheet 64 of 102

Sheet 65 of 102

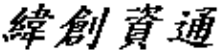
(Blanking)

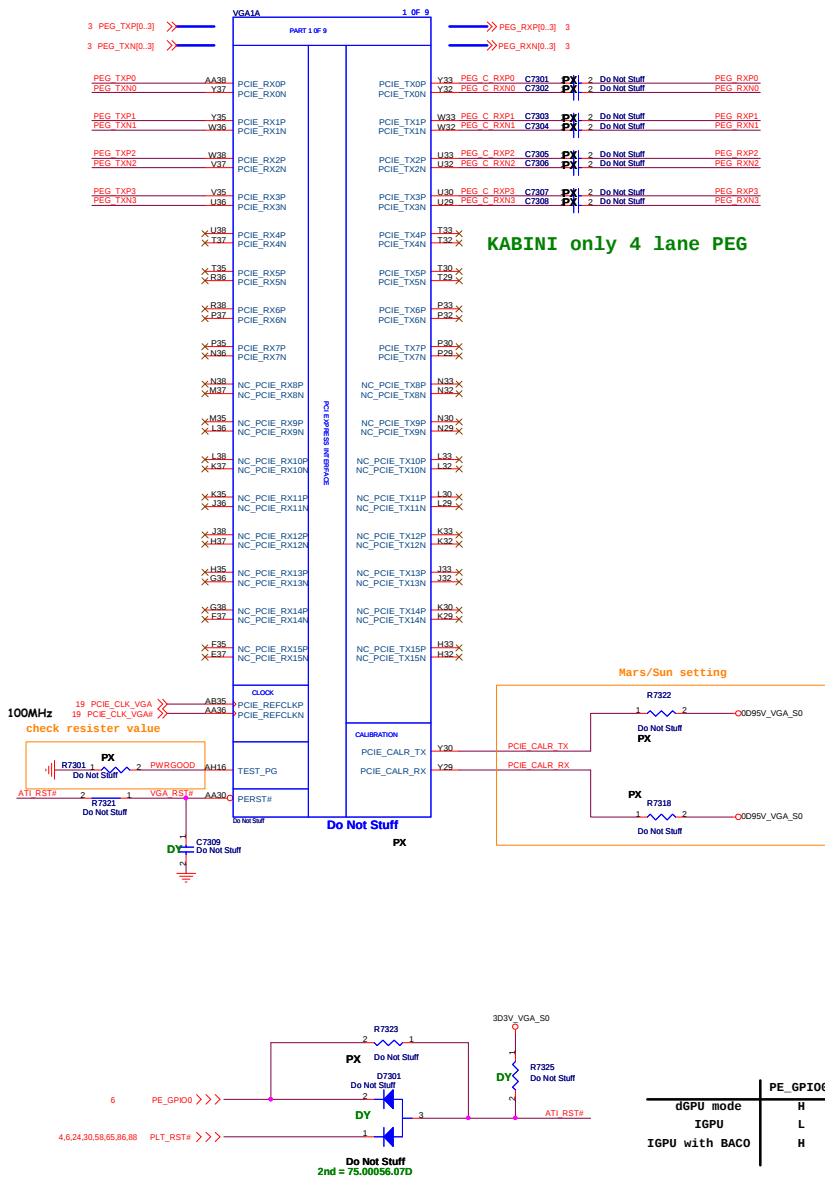
EAEG50 KB UMA

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size	Project Name		Rev
	KABINI		SA
Date: Friday, September 07, 2012		Sheet 66 of 102	

SSID = User.Interface

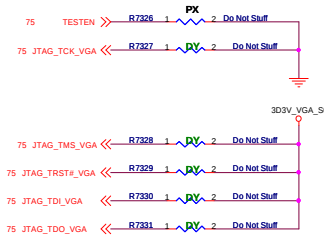
EAEG50 KB UMA

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
G Sensor			
Size	Project Name		Rev
	KABINI		SA
Date: Friday, September 07, 2012		Sheet	67 of 102

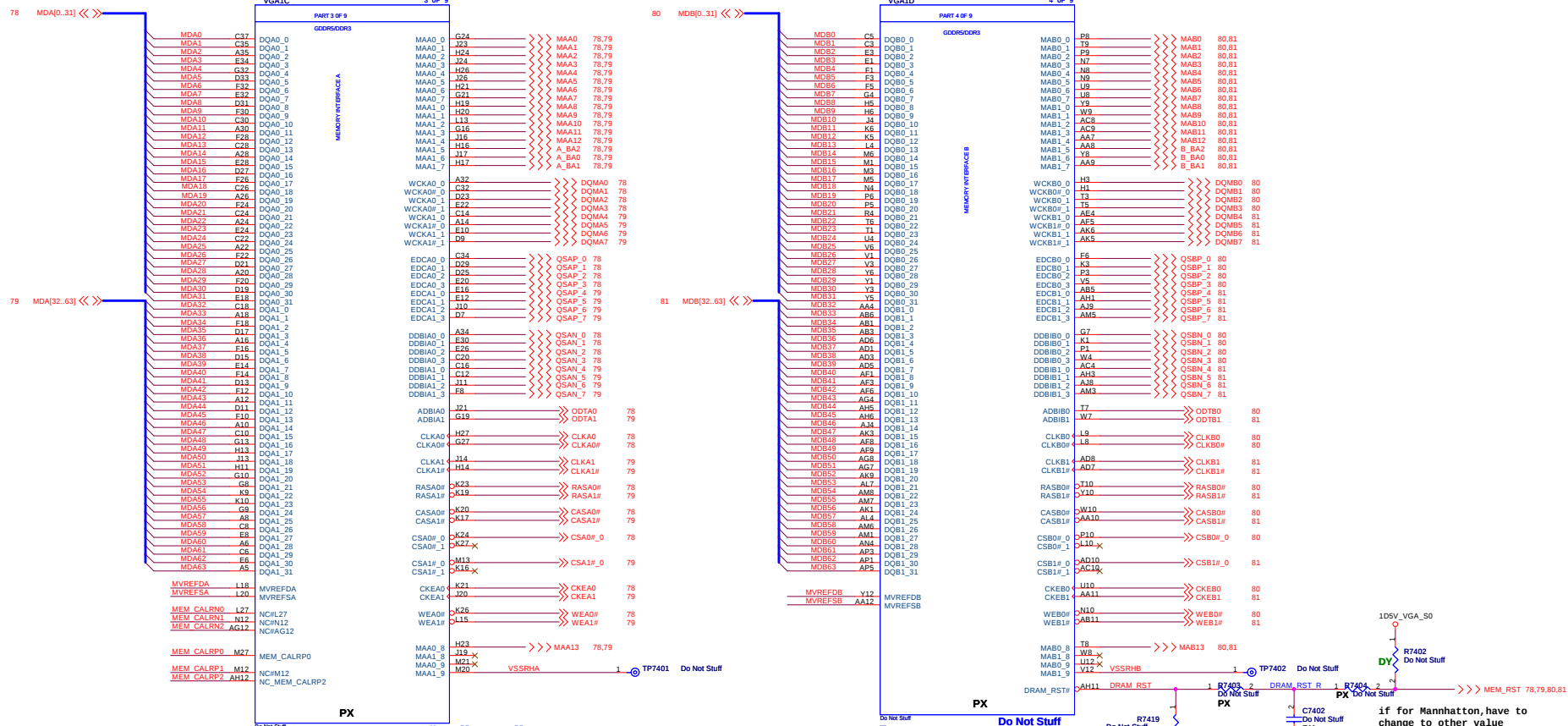


JTAG SIGNAL OPTION

Signal	Normal mode	Debug mode	pilot run mode
TESTEN	"0" (PD)	"1" (PU)	"0" (PD)
JTAG_TRST#	"1" (PU)	"1" (PU)	NC
JTAG_TCK	"0" (PD)	"1" (PU)	NC
JTAG_TMS	"1" (PU)	"1" (PU)	NC



EAE650 KB UMA

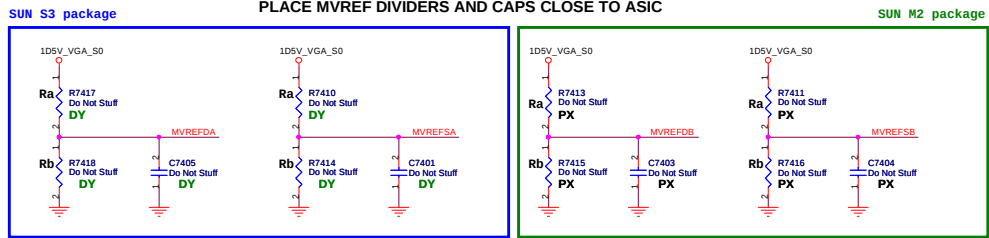


"Sun"-M2 uses memory group B only, while "Sun"-S3 uses memory group A only

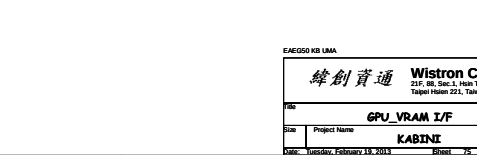
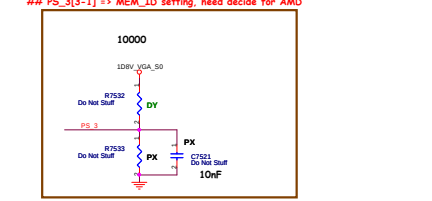
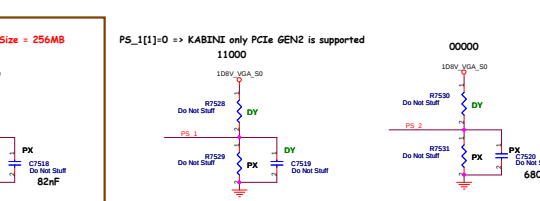
This basic topology should be used for DRAM_RAT for DDR3/GDDR5

DDR3/GDDR3 Memory Stuff Option(Mad/Park)

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

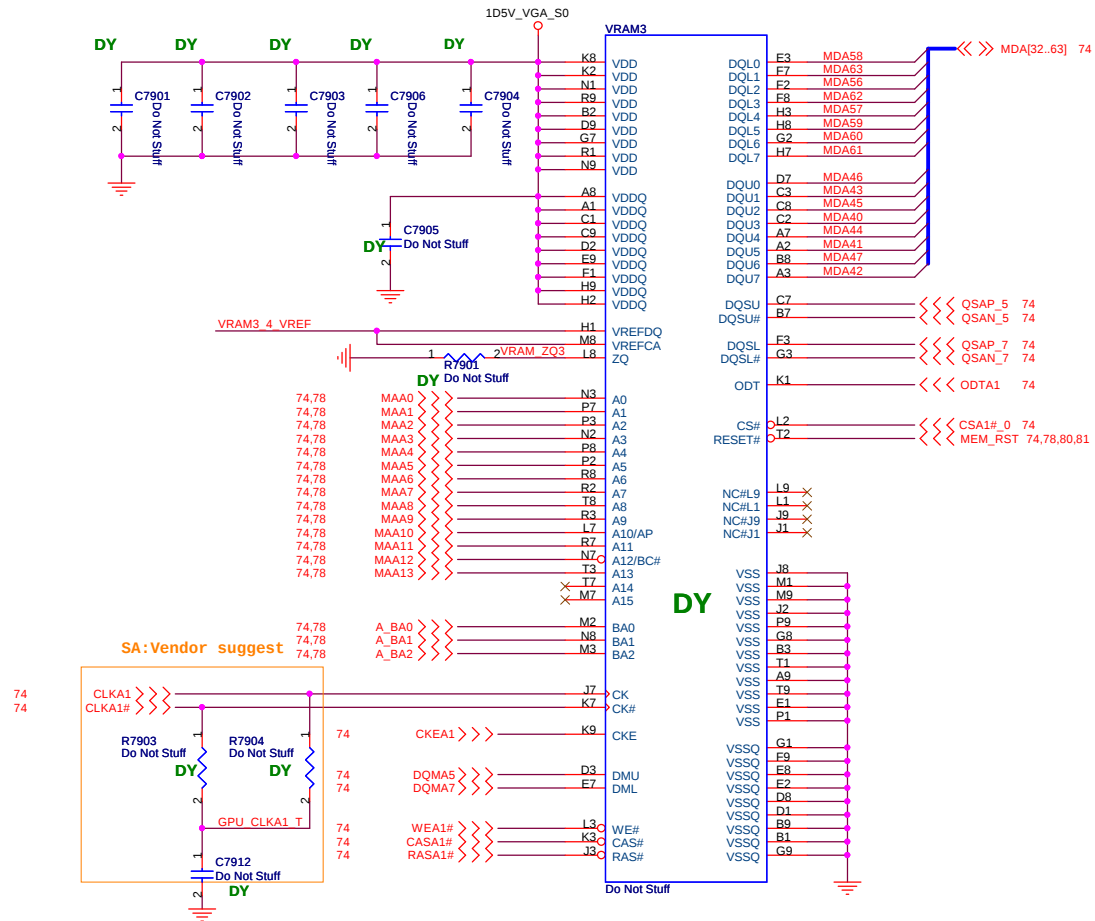


MEM_CALRN0	Whistler/Thames: Connect to VDDR1 through a 240Ω (40.5%) resistor. Prefered resistor tolerance is 0.5%, but 1% is acceptable. Seymour: NC Heathrow/Chelsea: NC	MEM_CALRP0	Whistler/Thames: need a 240 Ω (1%) termination to ground. Seymour: NC Heathrow/Chelsea: Need a 120Ω (1%) termination to ground
MEM_CALRN1	Whistler/Thames: NC Seymour: Connect to VDDR1 through a 240Ω (40.5%) resistor. Heathrow/Chelsea: NC	MEM_CALRP1	Whistler/Thames: NC Seymour: MEM_CALRP1—need a 240Ω (1%) termination to ground
MEM_CALRN2	Whistler/Thames: Connect to VDDR1 through a 240Ω (40.5%) resistor. Seymour: NC Heathrow/Chelsea: NC	MEM_CALRP2	Whistler/Thames: MEM_CALRP2—need a 240Ω (1%) termination to ground. Seymour: NC Heathrow/Chelsea: Need a 120Ω (1%) termination to ground

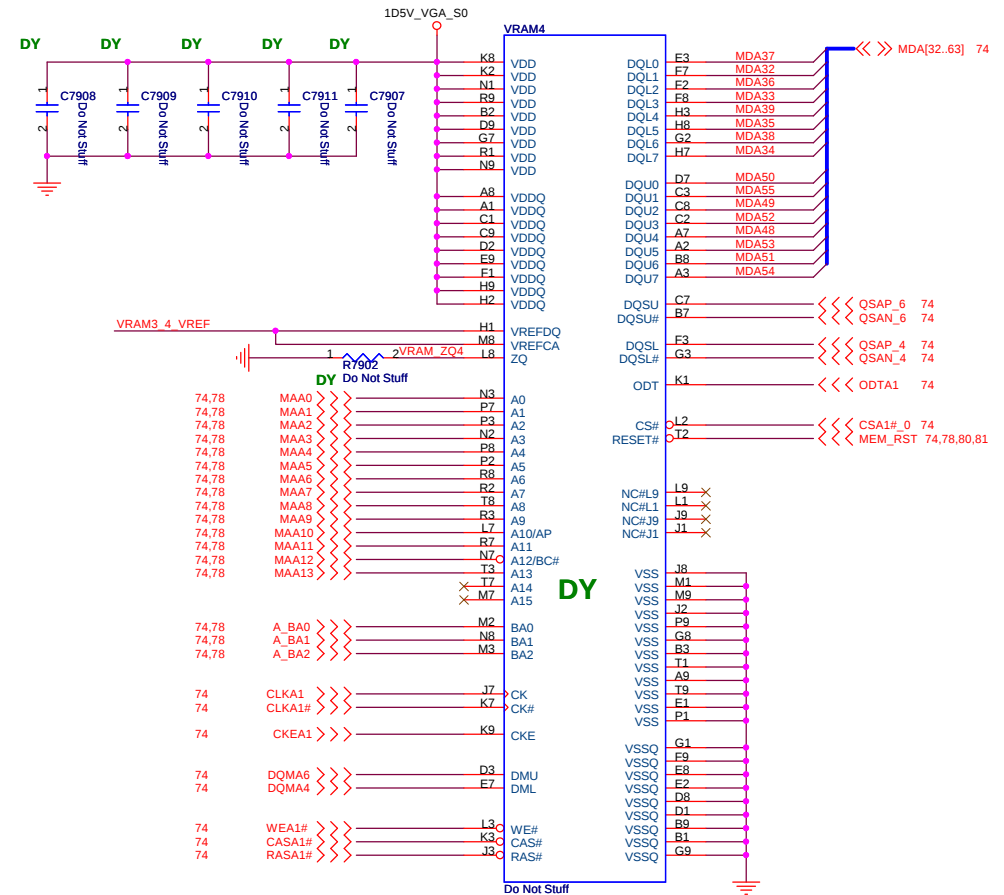


MLPS Bit	Strap Name	Description	Recommended Settings
PS_011	ROM_CONFIG00	If STRAP_BIOS_ROM_EN = 1, ROM_CONFIG00 defines the ROM type	Design dependent see the description.
PS_012	ROM_CONFIG01	If STRAP_BIOS_ROM_EN = 1, ROM_CONFIG01 defines the ROM operation mode. See Primary Memory Operation Use to learn more.	Design dependent see the description.
PS_041	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_051	AUD_PORT_CONV, PORTSTRF0	The L1R (least significant bit) of the strap options that indicates the number of audio-capable display outputs.	Design dependent see the description.
PS_111	STRAP_RIF, GEN3_EN_A	PCIe GEN3 capability. 1 = PCIe GEN3 is supported. 0 = PCIe GEN3 is not supported.	Design dependent see the description.
PS_121	STRAP_RIF, CLK_P9_EN	Determines whether or not the PCIe reference clock power management capability is reported in the PCI configuration space. Validations: there is a CLK_P9_EN 0 = The CLK_P9_EN power management capability is disabled. 1 = The CLK_P9_EN power management capability is enabled.	0
PS_131	N/A	Reserved for internal use only. Must be 1 at reset.	0
PS_141	STRAP_TX_CFG, FULL_SWEN	Control the transmitter full-swing mode. 0 = The transmitter half-swing is enabled. 1 = The transmitter full-swing is enabled.	1
PS_151	STRAP_TX_DEEPEN	PCI EXPRESS6 transmitter deep-sleep mode. 0 = Deep-sleep disabled. 1 = Deep-sleep enabled.	Design dependent see the description.
PS_211	N/A	Reserved.	N/A
PS_221	N/A	Reserved.	N/A
PS_231	STRAP_BIOS_ROM_EN	To enable the external BIOS ROM device. 0 = Enable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	Design dependent see the description.
MLPS Bit	Strap Name	Description	Recommended Settings
PS_241	STRAP_RIF_VGA_DS	VGA enable determines whether or not the DS is reset as the system's VGA controller. Through the DS_VGA_DS field in the PCI configuration space. 0 = VGA controller request is enabled. 1 = The device will not be recognized as the system's VGA controller.	0
PS_251	N/A	Reserved	N/A
PS_311	BOARD_CONFIG00	Board configuration related strap, such as for memory ID.	Design dependent see the description.
PS_312	BOARD_CONFIG01		
PS_313	BOARD_CONFIG02	Determines the maximum number of digital display audio endpoints that can be processed by the OS and used. This should be set to the maximum number of digital display audio outputs that can be enabled simultaneously in the product, which is limited by the ASIC maximum limit, the number and type of connectors on the board (DP, HDMI), and the number of audio for each port connector. The audio policy of the video driver. Usable only if the audio is enabled as an active feature in BIOS to secure audio enable at all endpoints. 111 = No usable endpoints. 110 = One usable endpoint. 101 = Two usable endpoints. 100 = Three usable endpoints. 011 = Four usable endpoints. 010 = Five usable endpoints. 001 = Six usable endpoints. 000 = All endpoints are usable.	Design dependent see the description.

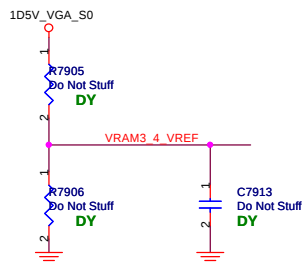
Note: AUD1L (on VSNVC) and AUD1R (on VSNVC) will not be properly pin strapped even if a MLPS board design.



Do Not Stuff

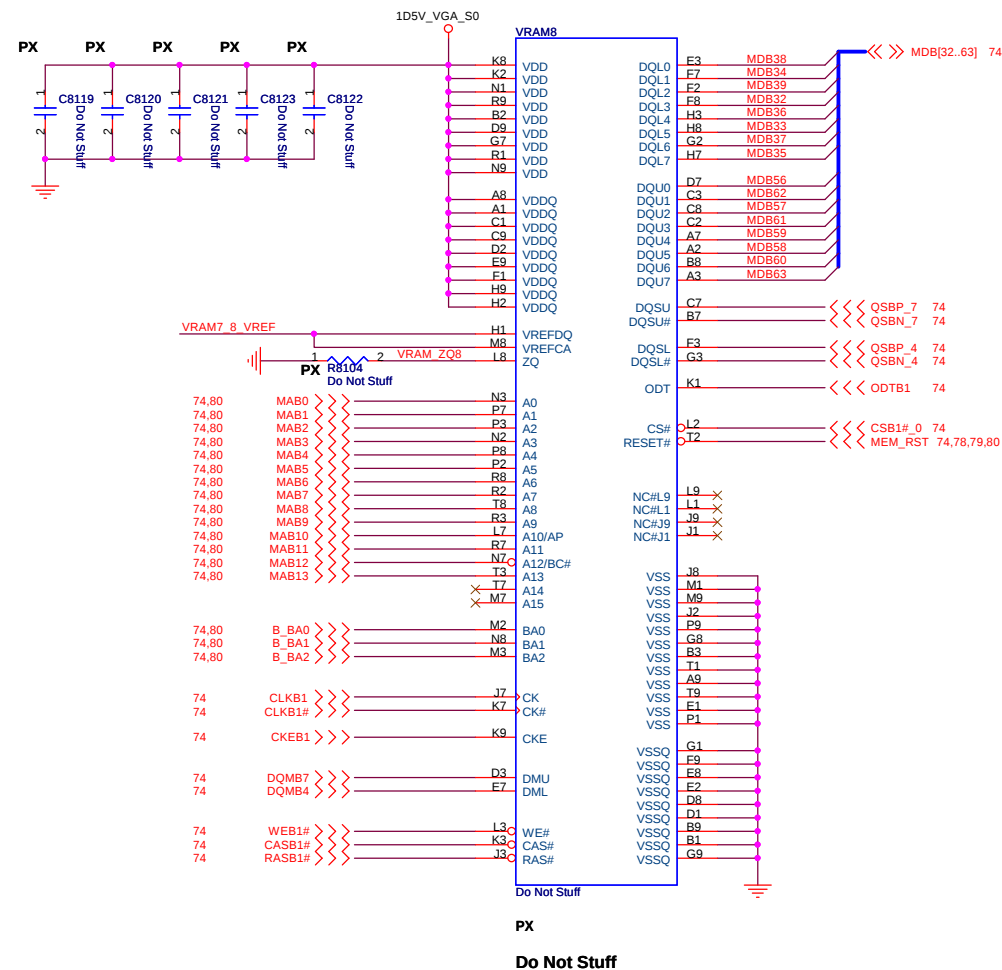
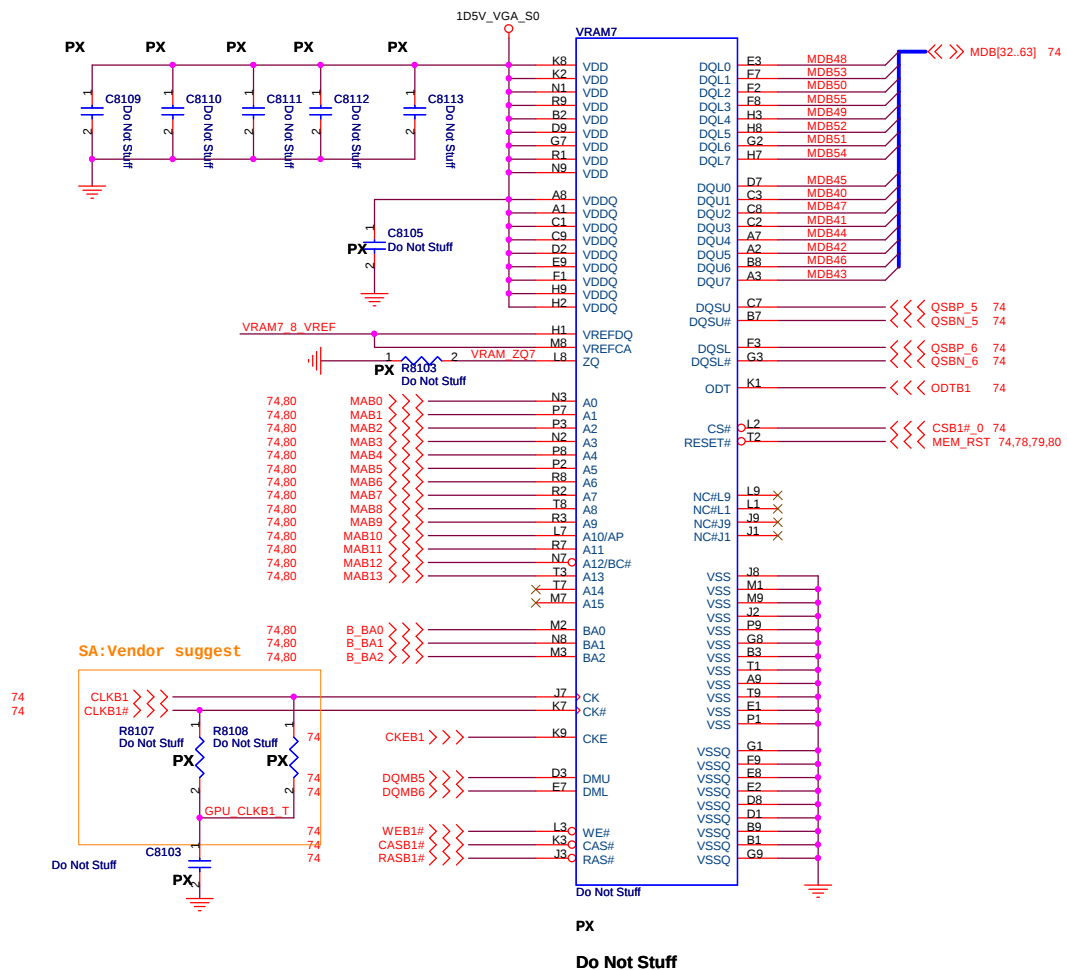


Do Not Stuff



EAEG50 KB UMA

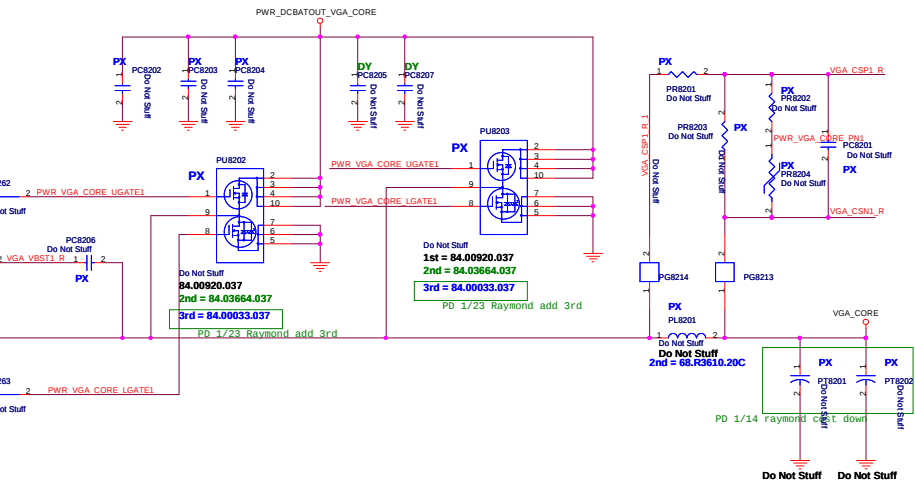
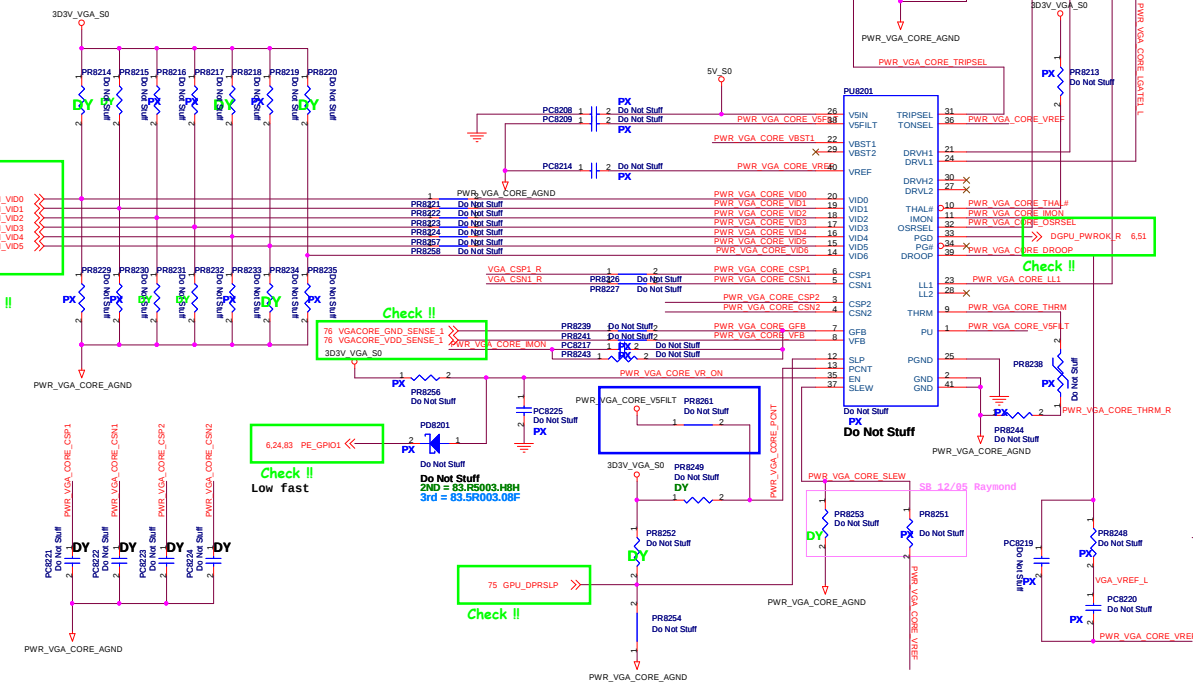
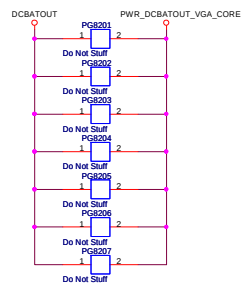
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
VRAM 3,4		
Size	Project Name	Rev
	KABINI	5A
Date:	Monday, February 04, 2013	Sheet 79 of 102



EG50 VRAM: 72.52G63.C0U (VR.2GB0G.005)
IC VRAM H5TQ2G63DFR-11C FBGA 96P 128M*16 x4

EAEG50 KB UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
VRAM 7,8	
Size	Project Name
	KABINI
Date: Monday, February 04, 2013	Rev SA
Sheet 81	of 102

SSID = PWR.Plane.Regulator_GFX

Vga_core
Iccmax=26A
OCP>35A

<<< DGPU_V

Check !!

Check !!

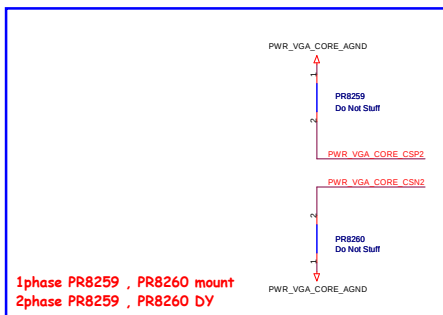
6,24,83 PE_G

Check !!

Low fast

75 GPU_DPRS

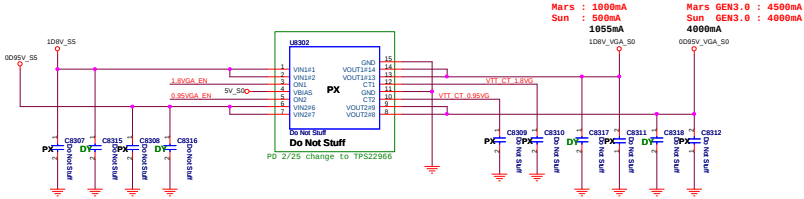
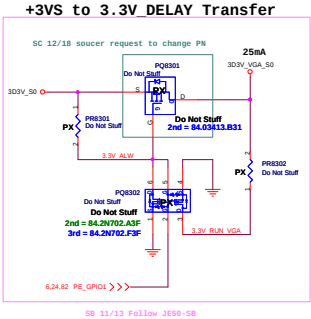
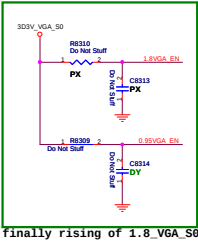
Check !!



1phase PR8259 , PR8260 mount
2phase PR8259 , PR8260 DY

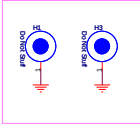
APL3523 for VGA_Power

	PE_GP100	PE_GP101
dGPU mode	H	H
IGPU	L	L
IGPU with BACO	H	H

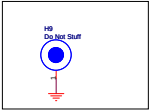


ZZ.00PAD.2N1

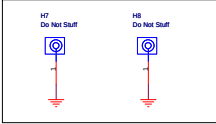
SB 11/14 follow HW for factory issue



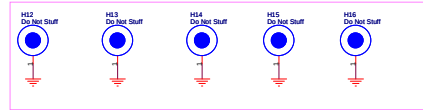
ZZ.00PAD.D01



ZZ.00PAD.E01



SB 11/20 ZZ.00pad.2T1 for change BKT size



Check test point

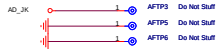


Test Point放在Dimm Door打開可量測處

10/15 follow HW



AD_JK
AD_JK



DC IN connector



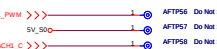
Battery connector



Speaker connector



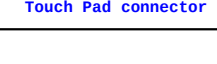
HP connector



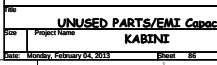
FAN connector



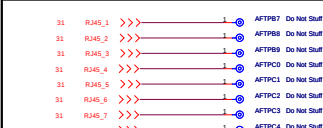
Normal KB connector



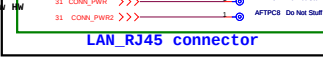
Touch Pad connector



EDP + MIC connector



LAN RJ45 connector



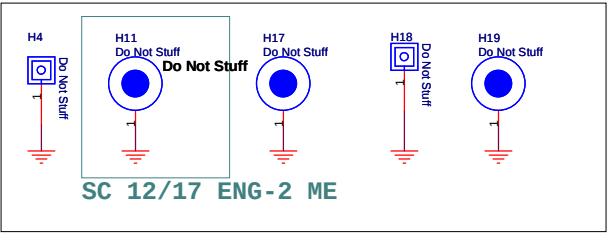
Card reader connector



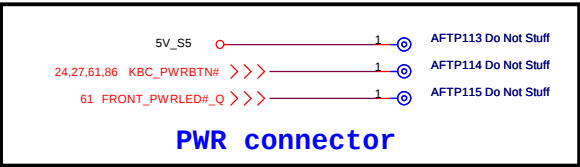
USBBD connector



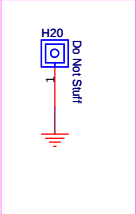
H4 & H11 & H17 & H18 & H19 for EG50



PWRBD AFTP for EG50

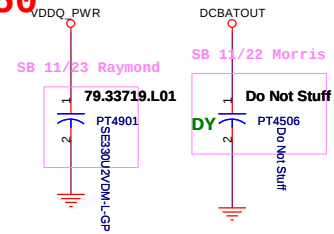
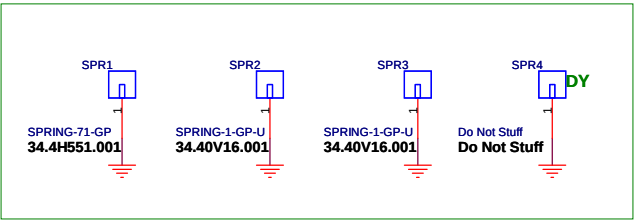


ZZ.00PAD.571



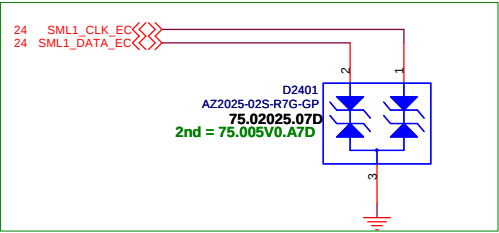
SB 11/20 location same with 14" H2

PD 1/23 EMI Jen



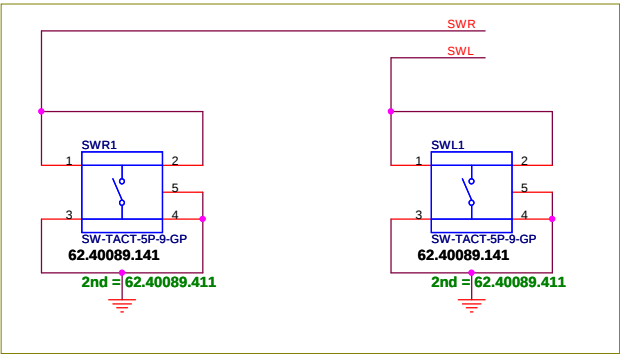
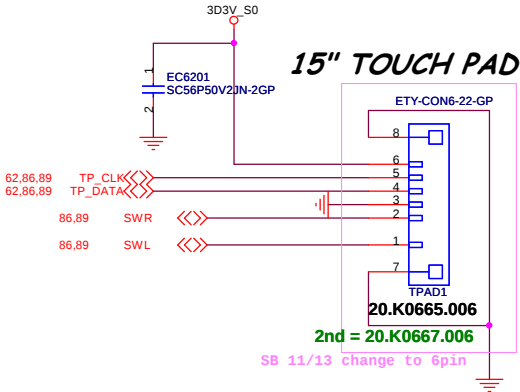
SB 11/23 3mm high limit in EG50

PD 01/31 Different Net name in 14" & 15" for placement

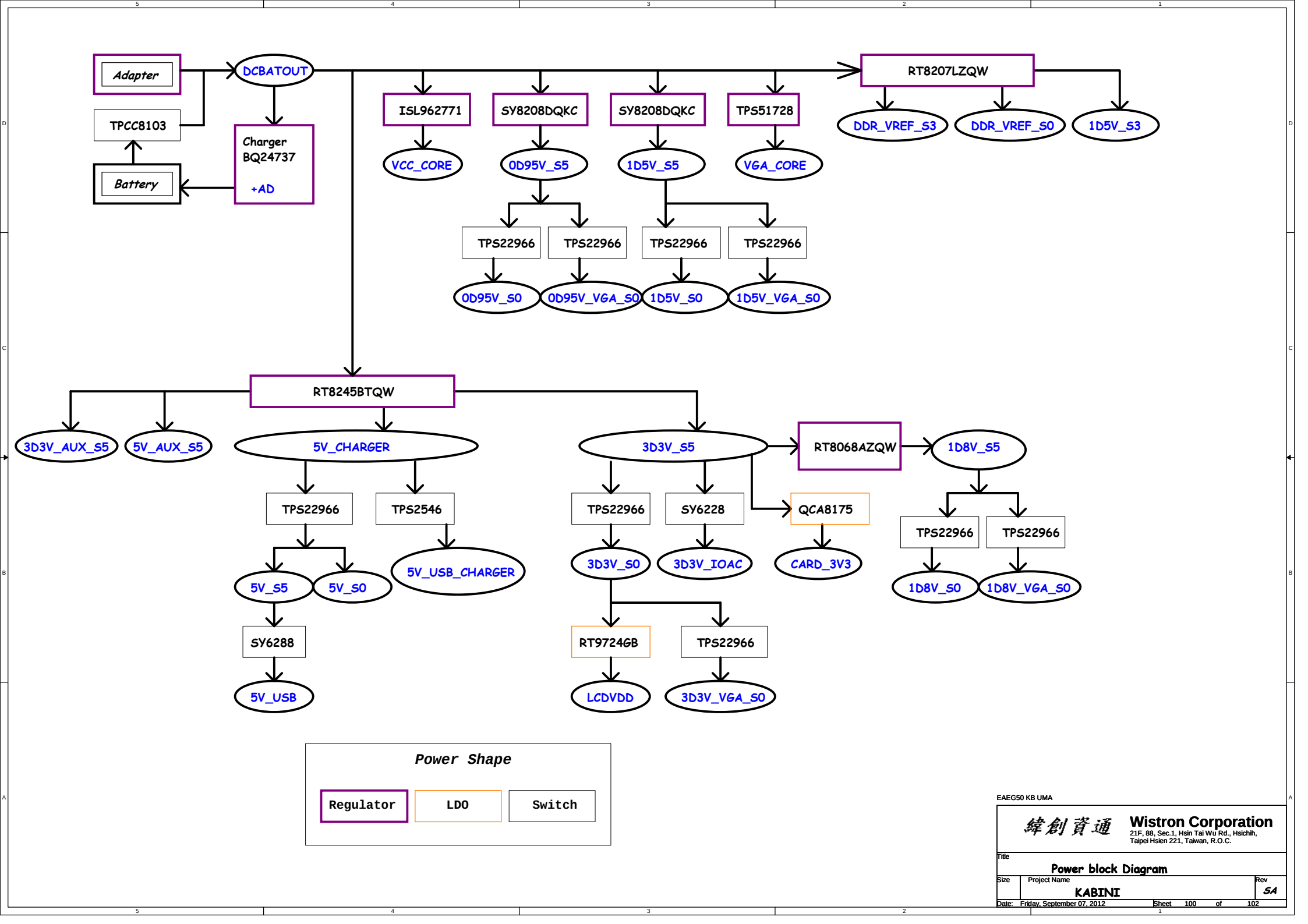


24,62,86	KCOL0	>>>
24,62,86	KCOL1	>>>
24,62,86	KCOL2	>>>
24,62,86	KCOL3	>>>
24,62,86	KCOL4	>>>
24,62,86	KCOL5	>>>
24,62,86	KCOL6	>>>
24,62,86	KCOL7	>>>
24,62,86	KCOL8	>>>
24,62,86	KCOL9	>>>
24,62,86	KCOL10	>>>
24,62,86	KCOL11	>>>
24,62,86	KCOL12	>>>
24,62,86	KCOL13	>>>
24,62,86	KCOL14	>>>
24,62,86	KCOL15	>>>
24,62,86	KCOL16	>>>
24,62,86	KCOL17	>>>
24,62,86	KROW0	>>>
24,62,86	KROW1	>>>
24,62,86	KROW2	>>>
24,62,86	KROW3	>>>
24,62,86	KROW4	>>>
24,62,86	KROW5	>>>
24,62,86	KROW6	>>>
24,62,86	KROW7	>>>

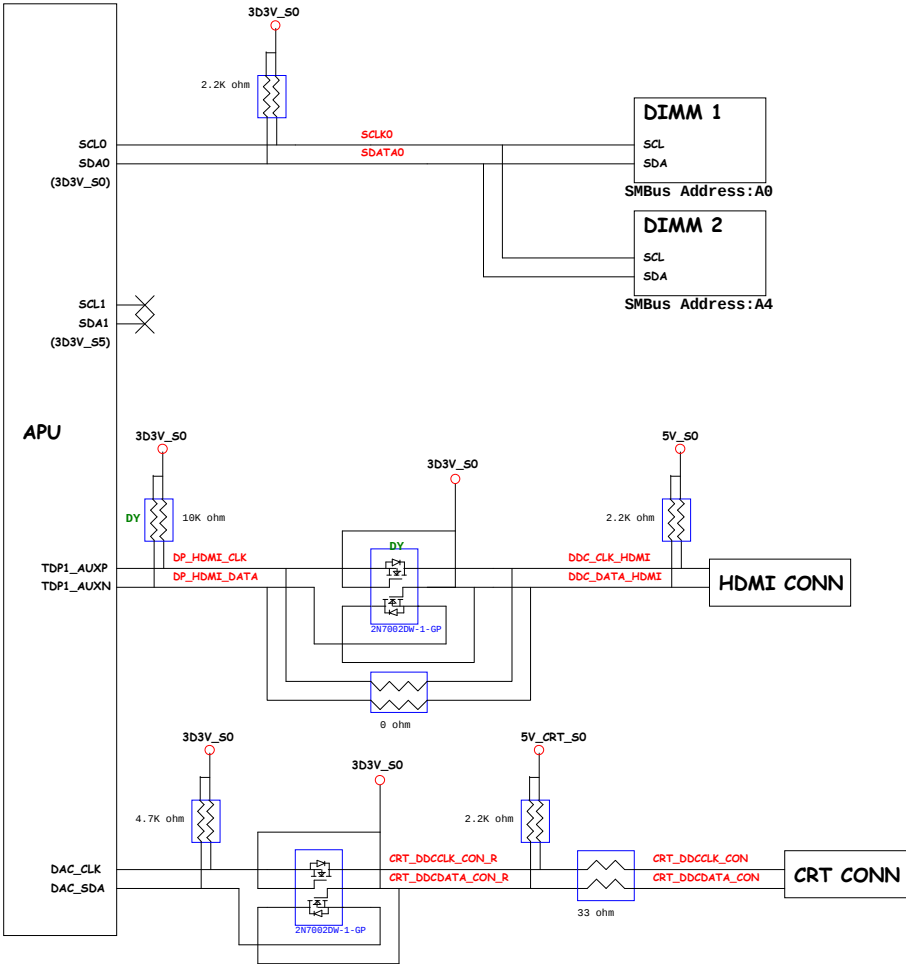
For AFTE



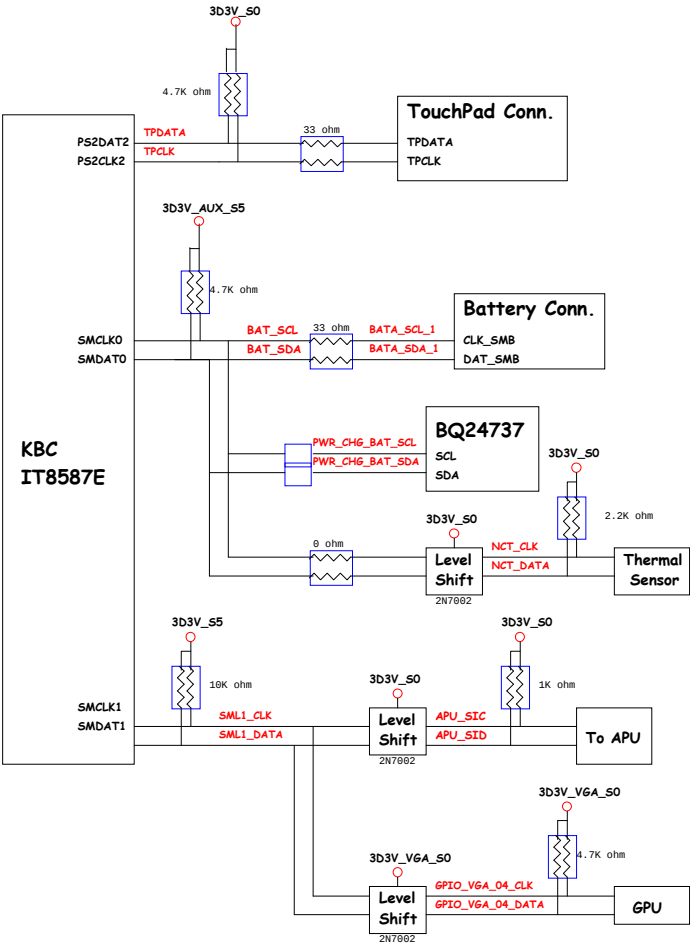
PD 1/21
SWL1 / SWR1 1st change to 62.40089.141, 2nd change to 62.40089.411 ,
because 160kg change to 100kg.



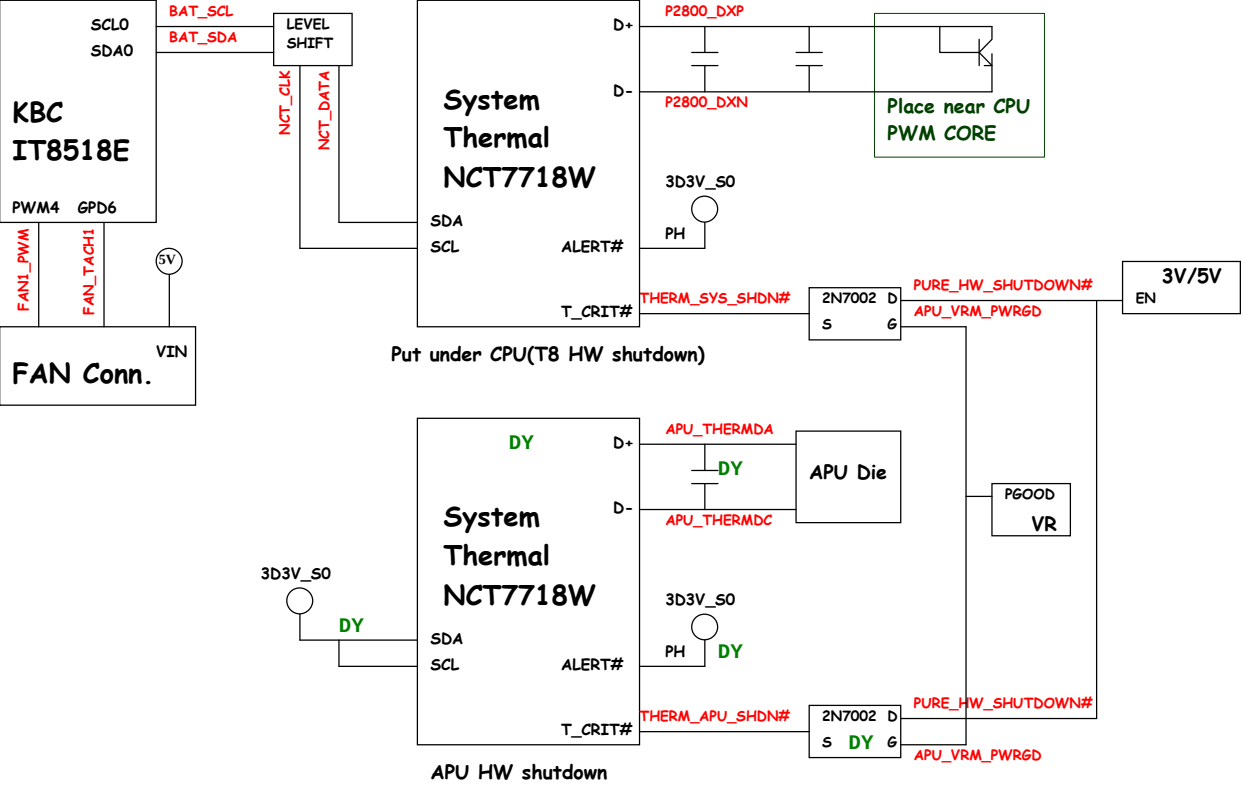
SMBus Block Diagram



KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram

