BMW Z4 14" Schematics Document

Ivy/Sandy Bridge
Panther Point

2012-04-02
REV : A00

DY : None Installed
UMA: UMA only installed
SG: PX solution installed.

<Core Design>

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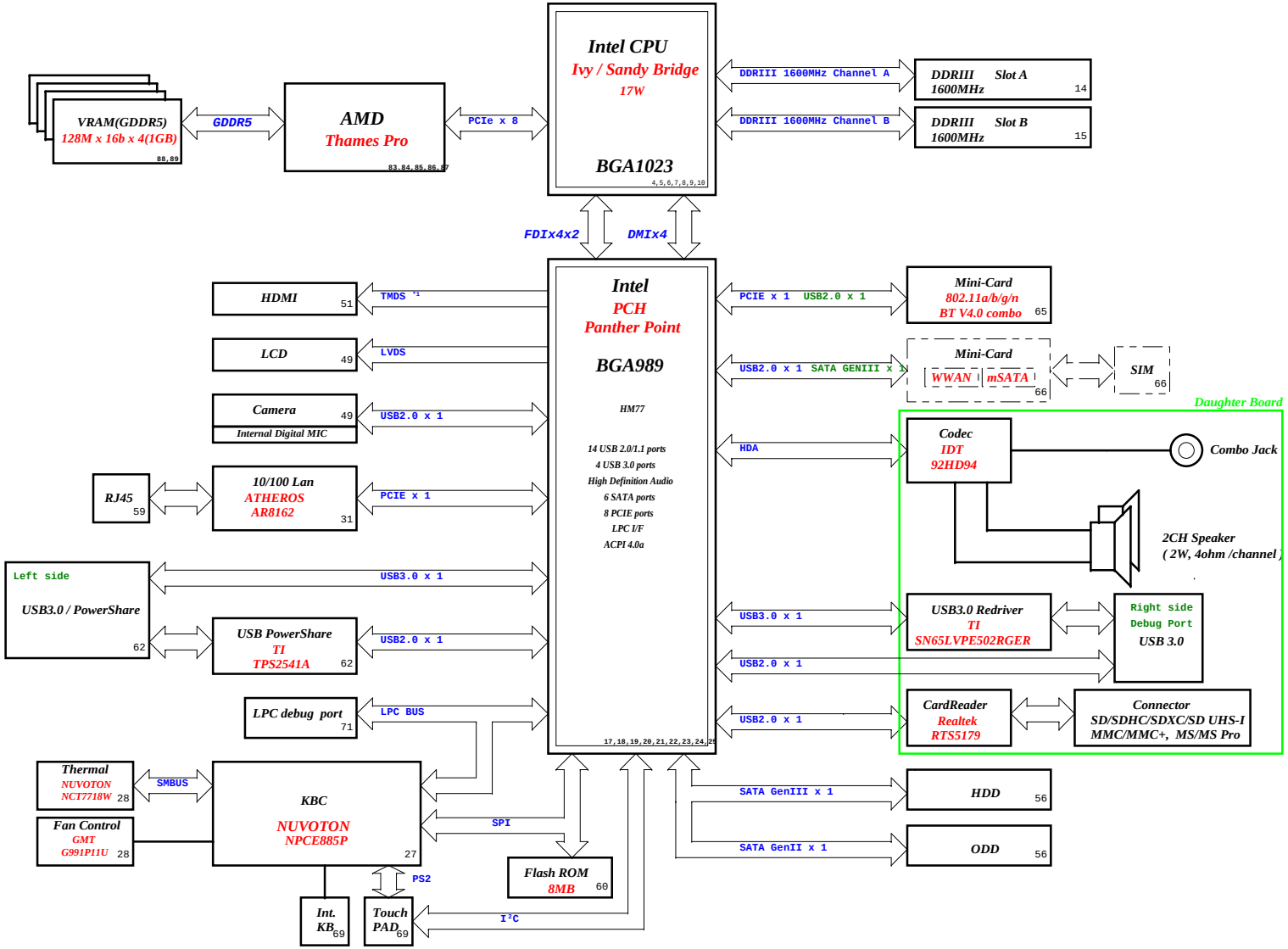
Title: Cover Page		
Size: A3	Document Number: BMW Z4 DIS	Rev: A00
Date: Monday, April 02, 2012	Sheet 1 of 105	

Block Diagram (Discrete / UMA)

Project Code: 91.4UV01.001
PCB P/N : 48.4SB02.011
Revision : 11289-1



*1: Transition minimized differential signaling

CHARGER BQ24727 40	
INPUTS	OUTPUTS
AD+	BT+

SYSTEM DC/DC TPS51125RGER 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5 15V_S5

CPU DC/DC VT1318+VT1326 42,43	
INPUTS	OUTPUTS
5V_S5	VCC_CORE

GFX DC/DC VT1318+VT1323 44	
INPUTS	OUTPUTS
5V_S5	VCC_GFXCORE

SYSTEM DC/DC VT386	
INPUTS	OUTPUTS
5V_S5	1D05V_PCH VCCP_CPU 45

SYSTEM DC/DC VT385(DIS)/RT9026 VT386(UMA)/RT9026	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3 46

SYSTEM DC/DC RT8068A 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

SYSTEM DC/DC APL5916 48	
INPUTS	OUTPUTS
VCCP_CPU	0D85_S0

VGA DC/DC VT358 92	
INPUTS	OUTPUTS
5V_S5	VGA_CORE

VGA DC/DC APL5930 93	
INPUTS	OUTPUTS
1D5V_S3	1V_VGA_S0

Switches	
INPUTS	OUTPUTS
1D5V_S3 5V_S5 3D3V_S5 3D3V_S5 3D3V_S5 1D8V_S0 1D5V_S3	1D5V_S0 5V_S0 3D3V_S0 3D3V_WLAN_AOAC 3D3V_VGA_S0 1D8V_VGA_S0 1D5V_VGA_S0

UMA/Discrete PCB LAYER	
L1:Top	L5:VCC
L2:GND	L6:Signal
L3:Signal	L7:GND
L4:Signal	L8:Bottom

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Title: Block Diagram

Size	Document Number	Rev
A2	BMW Z4 DIS	A00

Date: Friday, March 30, 2012 Sheet 2 of 105

PCH Strapping

Name	Schematics Notes
SPKR	The signal has a weak internal pull-down. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (Panther Point will disable the TCO Timer system reboot feature).
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
INTVRMEN	Integrated 1 V VRMs is enabled when high, External when low.
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
DF_TVS	DF_TVS needs to be pulled up to VccDFTERM power rail through 2.2 kOhms ±5% resistor.
HAD_DOCK_EN# /GPIO[33]	This signal controls the external Intel HD Audio docking isolation logic. This is an active-low-signal. When deasserted the external docking switch is in isolate mode. When asserted the external docking switch electrically connects the Intel HD Audio dock signals to the corresponding Panther Point signals. This signal can instead be used as GPIO33.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (0) Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality

Power Plane

Power Plane	Voltage	Actice Status	Description
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 1V_S0 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 1V 0.85V 0.75V 0.3V to 1.3V 0 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

Sandy & Ivy Bridge Compatibility

Pin Name	Configuration	Schematic Notes
DDR3 VREF	**Sandy Bridge + Ivy Bridge**	DDR3 VREF, M1 and M3 function are required.
	Ivy Bridge	No change.
PROC_SELECT# & DF_TVS	**Sandy Bridge + Ivy Bridge**	Connect DF_TVS signal of the PCH to PROC_SELECT# of the processor through a 1K±5% series resistor. PROC_SELECT# also needs a 2.2K±5% pull up resistor to PCH VccDFTERM rail.
	Ivy Bridge	No change.
VCCIO_SEL	**Sandy Bridge + Ivy Bridge**	The POR for Ivy Bridge mobile parts is now 1.05 V. There is no longer a need for a separate VR for the processor at 1.0 V and the PCH at 1.05 V. A single VR may be shared for both.
	Ivy Bridge	No change.
VCCSA_VID[0:1]	**Sandy Bridge + Ivy Bridge**	VCCSA[0:1] are the select pin of VCCSA's power control.
	Ivy Bridge	No change.

Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value	POP Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**	**0**
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	**1**	**1**
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	**11:** 1x16 PCI Express **10:** 2 x8 - PCI Express **01:** Reserved **00:** 1x8, 2x4 PCI Express	**11**	**10**

USB Table

Pair	Device
0	**USB3.0 port1, with Power Share**
1	**USB3.0 port2, debug port**
2	**NC**
3	**NC**
4	**Touch Panel**
5	**NC**
6	**NC**
7	**NC**
8	**WWAN**
9	**NC**
10	**Card reader**
11	**WLAN**
12	**CAMERA**
13	**NC**

PCIE Table

PCIE	
Lane	Device
1	**NC**
2	**NC**
3	**NC**
4	**WLAN**
5	**NC**
6	**Onboard LAN**
7	**NC**
8	**NC**

SATA Table

SATA	
Pair	Device
0	**HDD1**
1	**mSATA**
2	**NC**
3	**NC**
4	**ODD**
5	**NC**

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Title: *Table of Content*

Size	Document Number	Rev
A3	*BMW Z4 DIS*	*A00*

Date: Friday, March 30, 2012 Sheet 3 of 105

SSID = CPU

Layout Note:
Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

Layout Note:
DMI trace length 2000~8000mil

Layout Note:
FDI trace length 2000~6500mil

Layout Note:
Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

Layout Note:
PEG trace length 1500~9000mil

CPU1A — 1 OF 9 — IVY-BRIDGE-GP-NF — 71.00IVY.A0U

DMI: DMI_TXN[3:0], DMI_TXP[3:0], DMI_RXN[3:0], DMI_RXP[3:0]
FDI: FDI_TXN[7:0], FDI_TXP[7:0], FDI_FSYNC0, FDI_FSYNC1, FDI_INT, FDI_LSYNC0, FDI_LSYNC1
EDP: DP_COMP, EDP_COMPIO, EDP_ICOMPO, EDP_HPD#, EDP_AUX#, EDP_AUX, EDP_TX#0-3, EDP_TX0-3
PCI EXPRESS -- GRAPHICS: PEG_ICOMPI, PEG_ICOMPO, PEG_RCOMPO, PEG_RX#0-15, PEG_RX0-15, PEG_TX#0-15, PEG_TX0-15

R401 24D9R2F-L-GP (PEG_IRCOMP_R) — VCCP_CPU
R402 24D9R2F-L-GP (DP_COMP) — VCCP_CPU

PEG_RXN[7..0] [83]
PEG_RXP[7..0] [83]
PEG_TXN[7..0] [83]
PEG_TXP[7..0] [83]

C401	SCD1U10V2KX-5GP	PEG_C_TXN7	PEG_TXN7
C402	SCD1U10V2KX-5GP	PEG_C_TXN6	PEG_TXN6
C403	SCD1U10V2KX-5GP	PEG_C_TXN5	PEG_TXN5
C404	SCD1U10V2KX-5GP	PEG_C_TXN4	PEG_TXN4
C405	SCD1U10V2KX-5GP	PEG_C_TXN3	PEG_TXN3
C406	SCD1U10V2KX-5GP	PEG_C_TXN2	PEG_TXN2
C407	SCD1U10V2KX-5GP	PEG_C_TXN1	PEG_TXN1
C408	SCD1U10V2KX-5GP	PEG_C_TXN0	PEG_TXN0
C417	SCD1U10V2KX-5GP	PEG_C_TXP7	PEG_TXP7
C418	SCD1U10V2KX-5GP	PEG_C_TXP6	PEG_TXP6
C419	SCD1U10V2KX-5GP	PEG_C_TXP5	PEG_TXP5
C420	SCD1U10V2KX-5GP	PEG_C_TXP4	PEG_TXP4
C421	SCD1U10V2KX-5GP	PEG_C_TXP3	PEG_TXP3
C422	SCD1U10V2KX-5GP	PEG_C_TXP2	PEG_TXP2
C423	SCD1U10V2KX-5GP	PEG_C_TXP1	PEG_TXP1
C424	SCD1U10V2KX-5GP	PEG_C_TXP0	PEG_TXP0

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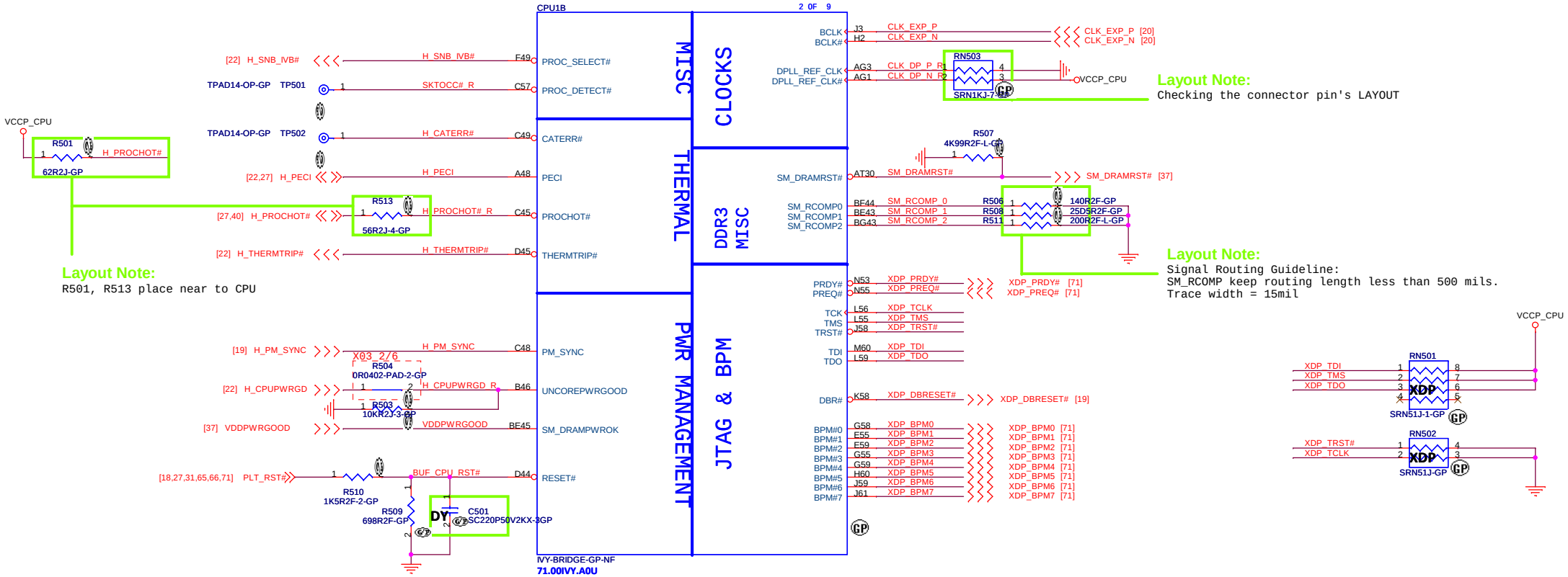
Title: CPU(PCIE/DMI/FDI)

Size	Document Number	Rev
A3	BMW Z4 DIS	A00

Date: Friday, March 30, 2012 Sheet 4 of 105

SSID = CPU



Layout Note:
R501, R513 place near to CPU

Layout Note:
C501 place near to CPU

Layout Note:
Checking the connector pin's LAYOUT

Layout Note:
Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.
Trace width = 15mil

<Core Design>

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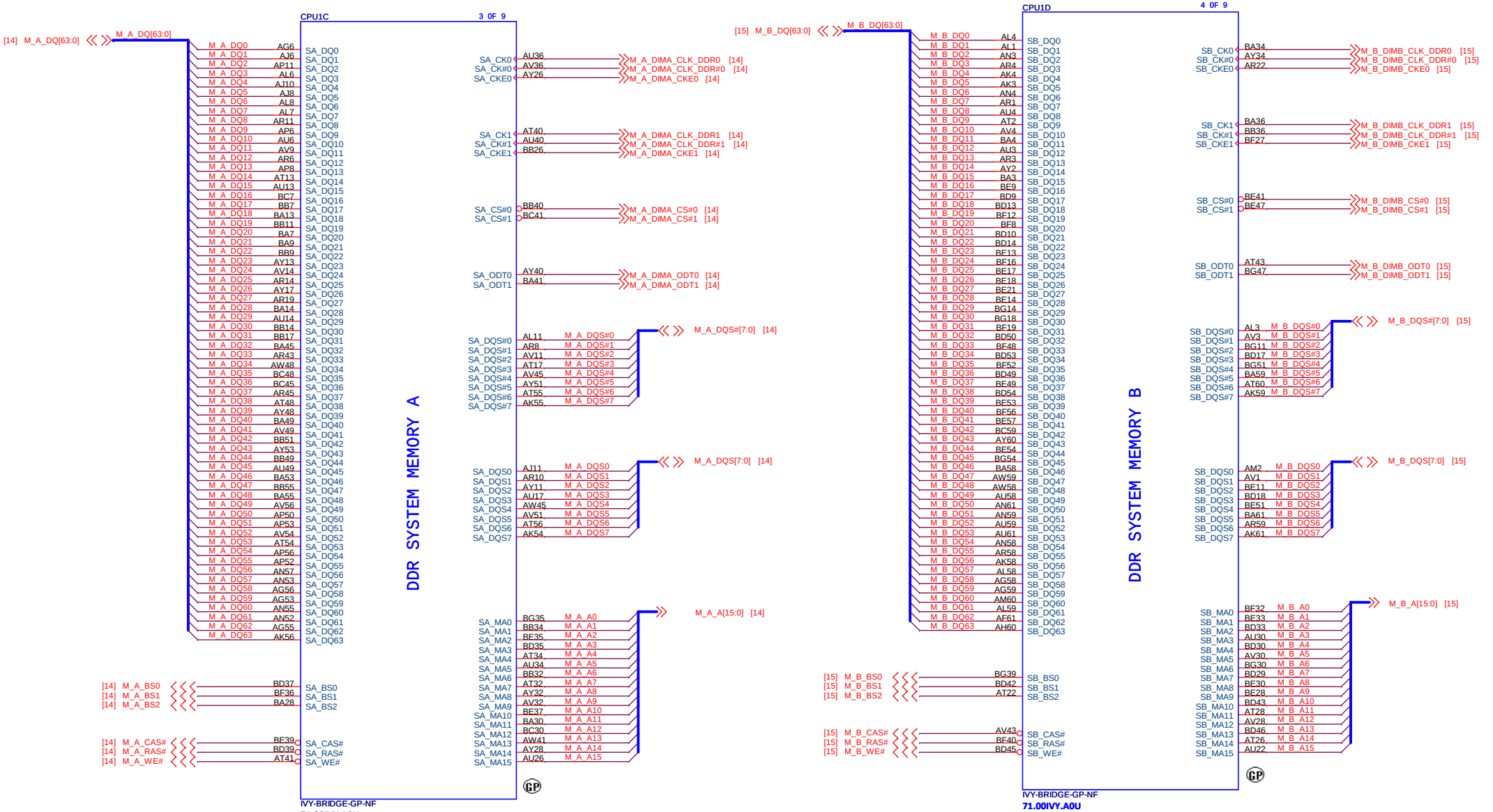
Title: CPU(THERMAL/CLOCK/PM)

Size	Document Number	Rev
A3	BMW Z4 DIS	A00

Date: Friday, March 30, 2012 Sheet 5 of 105

SSID = CPU



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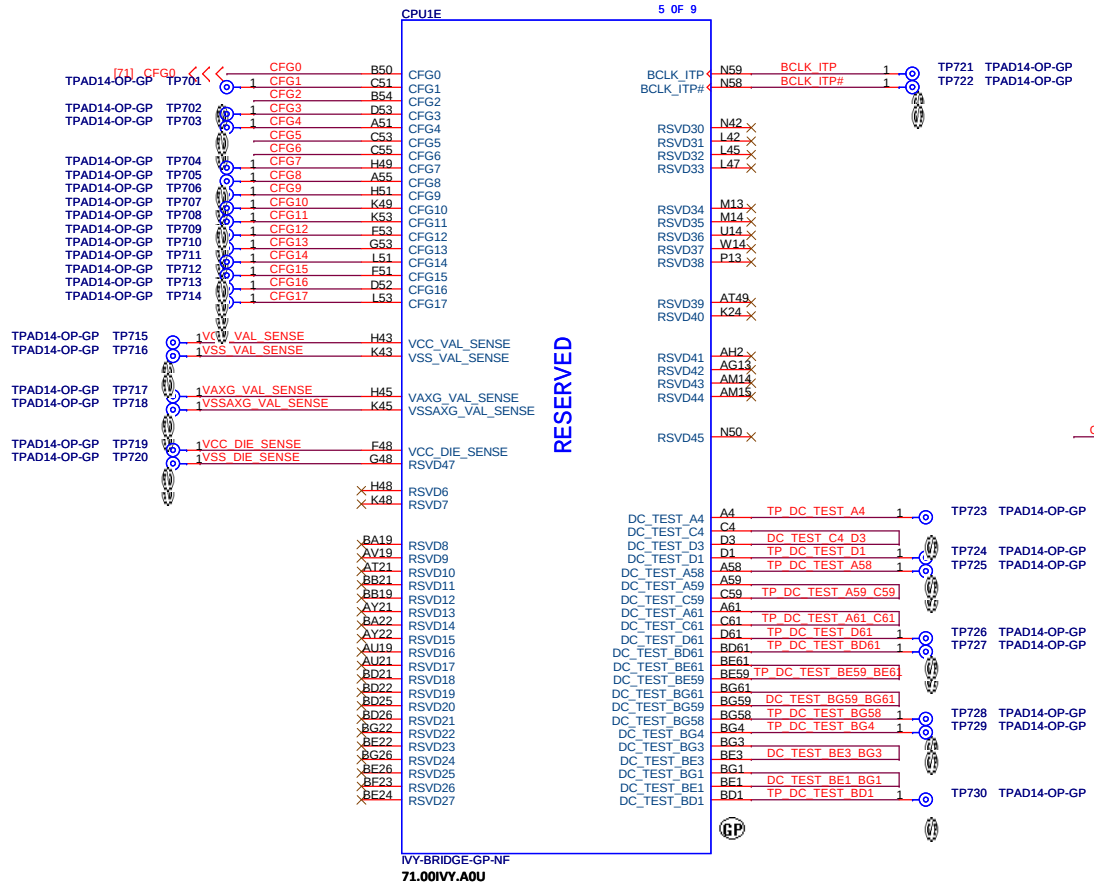
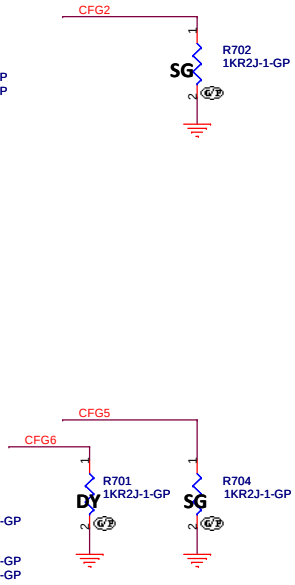
Title: **CPU (DDR)**

Size	Document Number	Rev
A3	BMW Z4 DIS	A00

Date: Friday, March 30, 2012 Sheet 6 of 105

SSID = CPU





PEG Static Lane Reversal

CFG[2]	1: Normal Operation; Lane # definition matches socket pin map definition
	0:Lane Reversed

Display Port Presence Strap

CFG[4]	1: Disabled; No Physical Display Port attached to Embedded Display Port
	0: Enabled; An external Display Port device is connected to the Embedded Display Port

PCIE Port Bifurcation Straps

CFG[6:5]	**11:** 1x16 PCI Express
	10: 2 x8 - PCI Express
	01: Reserved
	00: 1x8, 2x4 PCI Express

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Title: CPU (RESERVED)

Size	Document Number	Rev
A3	BMW Z4 DIS	A00

Date: Friday, March 30, 2012 Sheet 7 of 105

SSID = CPU

A00 3/30
X01 12/21
X01 12/16
X01 12/15
X01 12/09

POWER

6 OF 9

CPU1F

VCC_CORE

33A

CORE SUPPLY

PEG IO AND DDR IO

8.5A

VCCP_CPU

Added, cause the 1.05V far away CPU

Voltage Rail	Voltage(V)	Iccmax(A)
VCC_CORE(ULV)	0.3~1.52	33
VAXG(ULV)	0~1.52	33
VCCIO	1.05	8.5
VDDQ	1.5	5
VCCSA	0.9	4
VCCPLL	1.8	1.2

QUIET RAILS

SVID

SENSE LINES

IVY-BRIDGE-GP-NF
71.00IVY.A0U

Layout Note:
R803, R804, R805 need close to CPU
Alert# signal must be routed between the Clock and Data lines to reduce the cross talk between them

Need place Pull Hi at IMVP page

Layout Note:
1. PH/PL resisors place close CPU
2. SENSE signal recommend differential routing

Layout Note:
1. PH/PL resisors place close CPU
2. SENSE signal recommend differential routing

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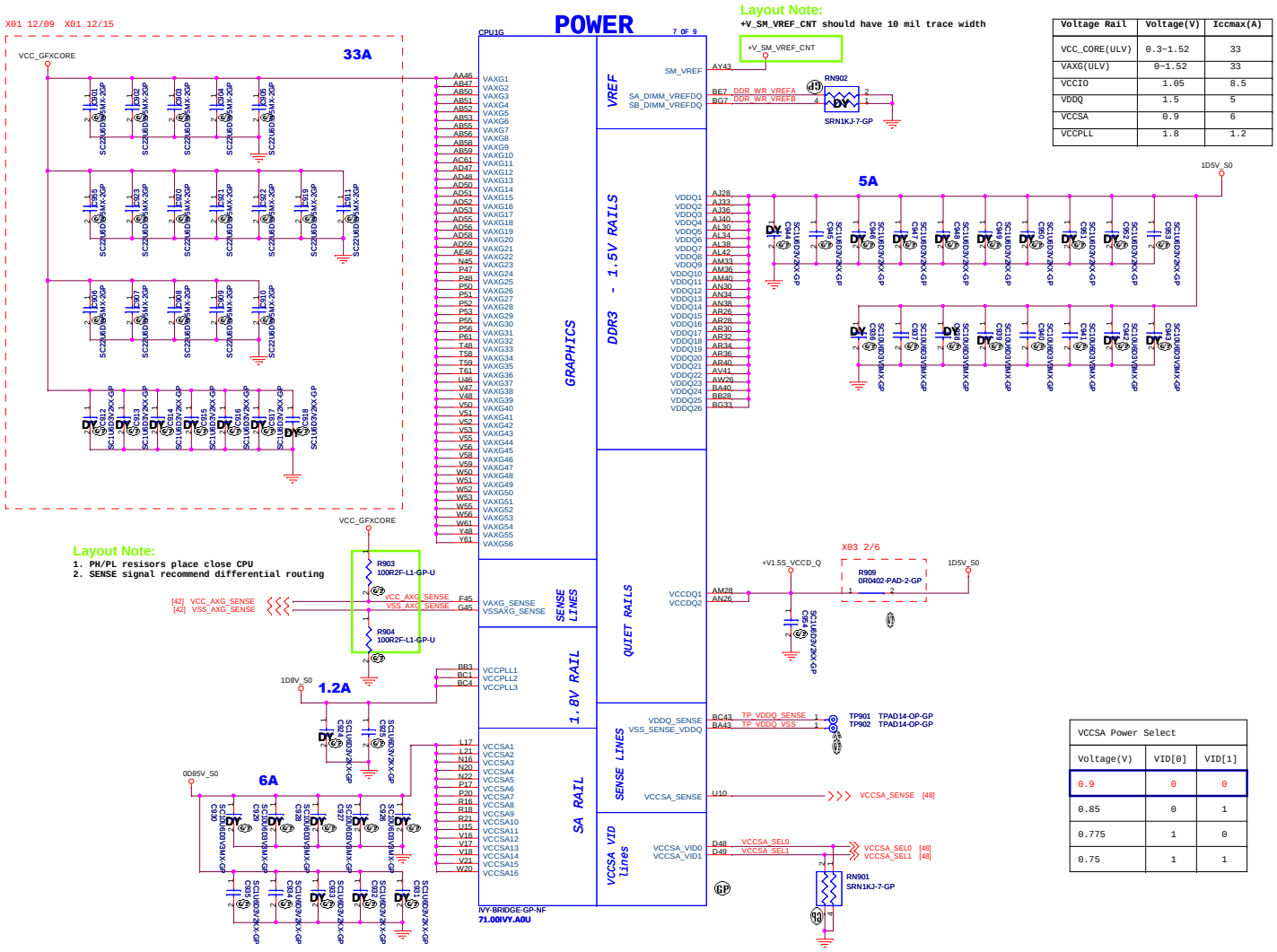
Title: CPU (VCC_CORE)

Size: A2 | Document Number: BMW Z4 DIS | Rev: A00

Date: Friday, March 30, 2012 | Sheet 8 of 105

SSID = CPU



Voltage Rail	Voltage(V)	Iccmax(A)
VCC_CORE(ULV)	0.3~1.52	33
VAXG(ULV)	0~1.52	33
VCCIO	1.05	8.5
VDDQ	1.5	5
VCCSA	0.9	6
VCCPLL	1.8	1.2

VCCSA Power Select		
Voltage(V)	VID[0]	VID[1]
0.9	0	0
0.85	0	1
0.775	1	0
0.75	1	1

<Core Design>

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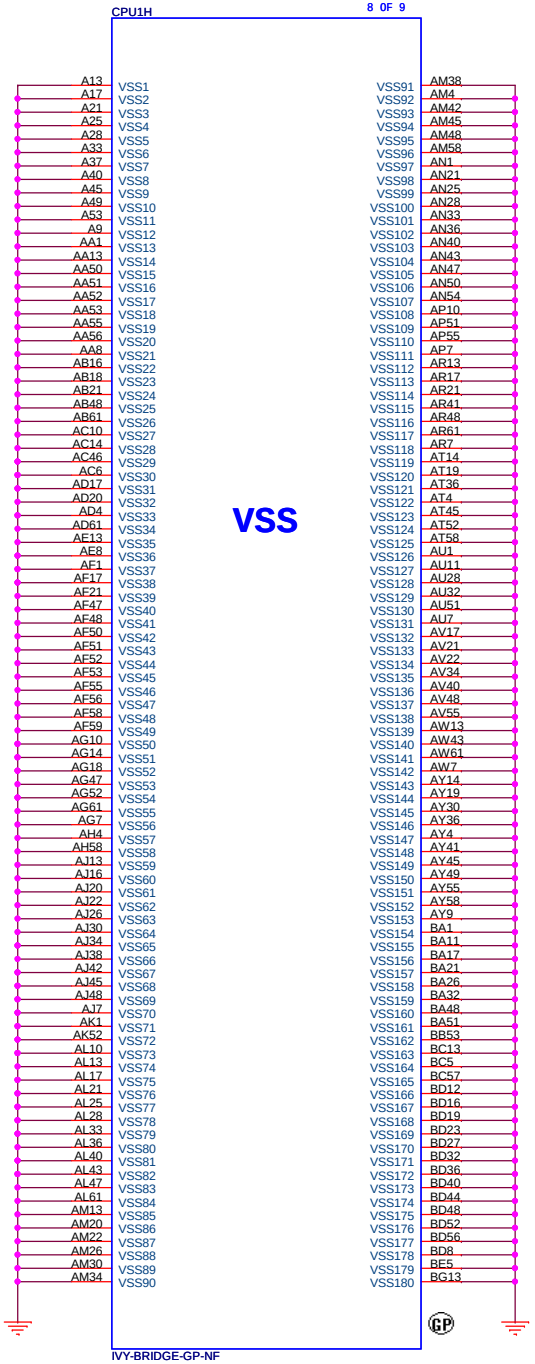
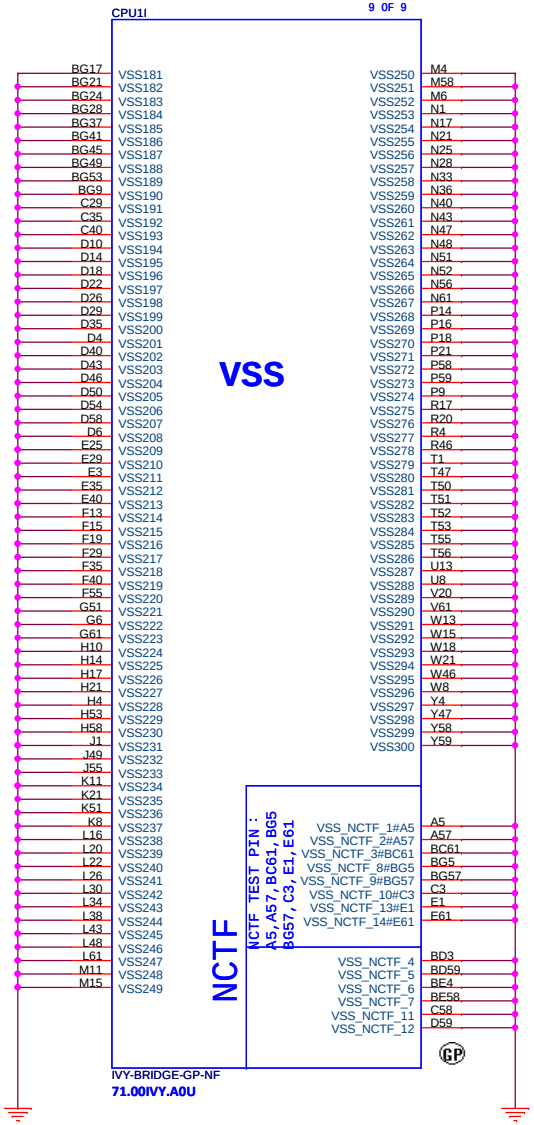
Title: CPU (VCC_GFXCORE)

Size: A2 | Document Number: BMW Z4 DIS | Rev: A00

Date: Friday, March 30, 2012 | Sheet 9 of 105

SSID = CPU





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Title	CPU (VSS)	
Size A3	Document Number BMW Z4 DIS	Rev A00
Date: Friday, March 30, 2012	Sheet 10 of 105	

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Title: XDP

Size: A3 | Document Number: BMW Z4 DIS | Rev: A00

Date: Friday, March 30, 2012 | Sheet 11 of 105

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Title: *Reserved*

Size	Document Number	Rev
A3	*BMW Z4 DIS*	*A00*

Date: Friday, March 30, 2012 Sheet 12 of 105

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Title

(Reserved)

Size	Document Number	Rev
A3	***BMW Z4 DIS***	***A00***

SSID = MEMORY

X01 12/15
X01 12/02

DIM1

DDR3-204P-73-GP

62.10017.U81
2nd = 62.10017.P31
3rd = 62.10017.K11
4th.= 62.10017.N91

Layout Note:
Place these caps close to VREF_CA

Layout Note:
Place these caps close to VREF_DQ

Layout Note:
Place these caps close to VTT1 and VTT2.

Layout Note:
All VREF traces should have width=20mil; spacing=20 mil

Note:
SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

Layout Note:
Place these Caps near SO-DIMMA.

Layout Note:
For S3 reduction circuit's 1D5V return pass.

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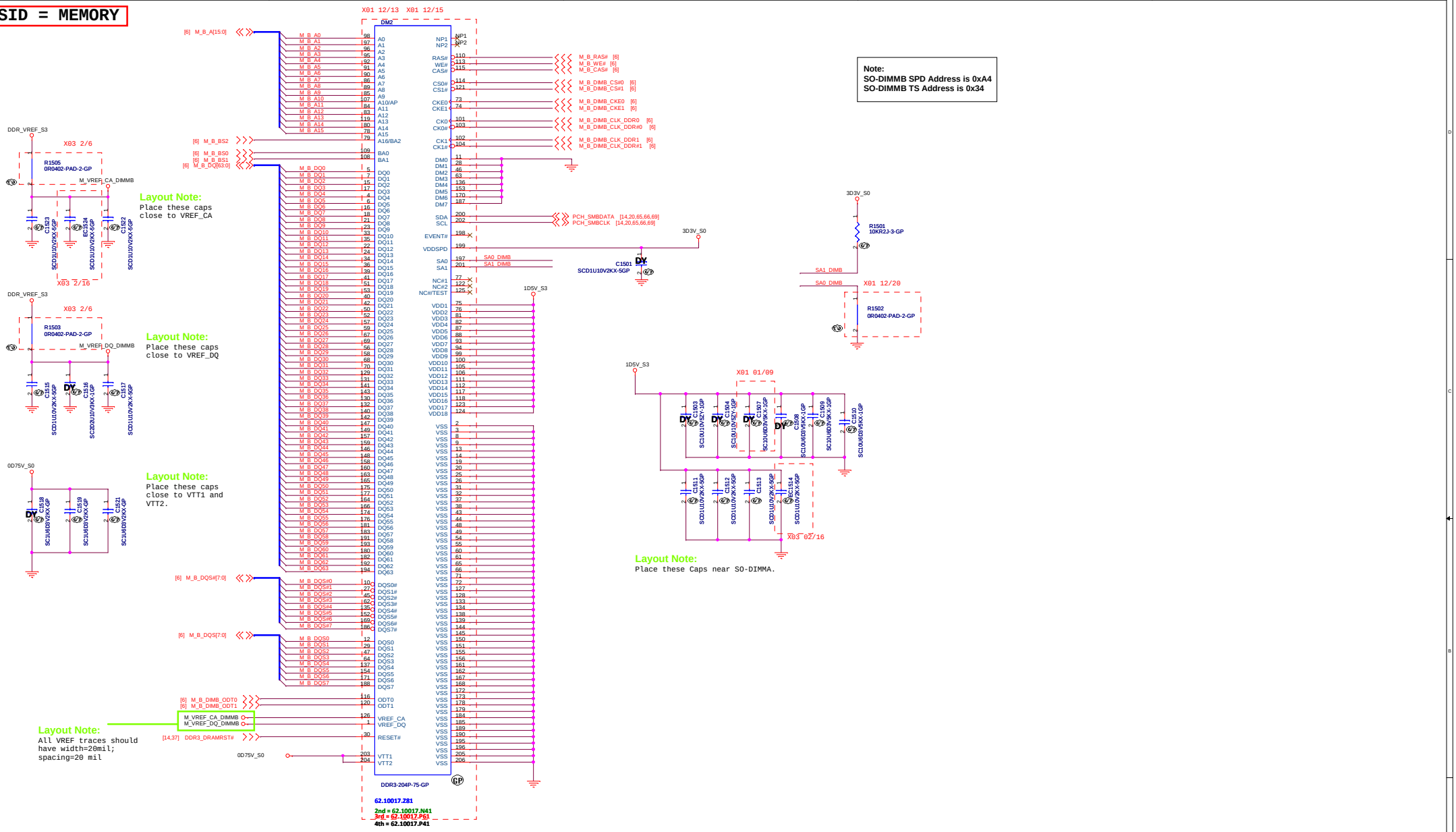
Title: DDR3-SODIMM1
Size: A2 | Document Number: BMW Z4 DIS | Rev: A00
Date: Friday, March 30, 2012 | Sheet 14 of 105

SSID = MEMORY



Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

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Title: **DDR3-SODIMM2**

Size	Document Number	Rev
A2	BMW Z4 DIS	A00

Date: Friday, March 30, 2012 Sheet 15 of 105

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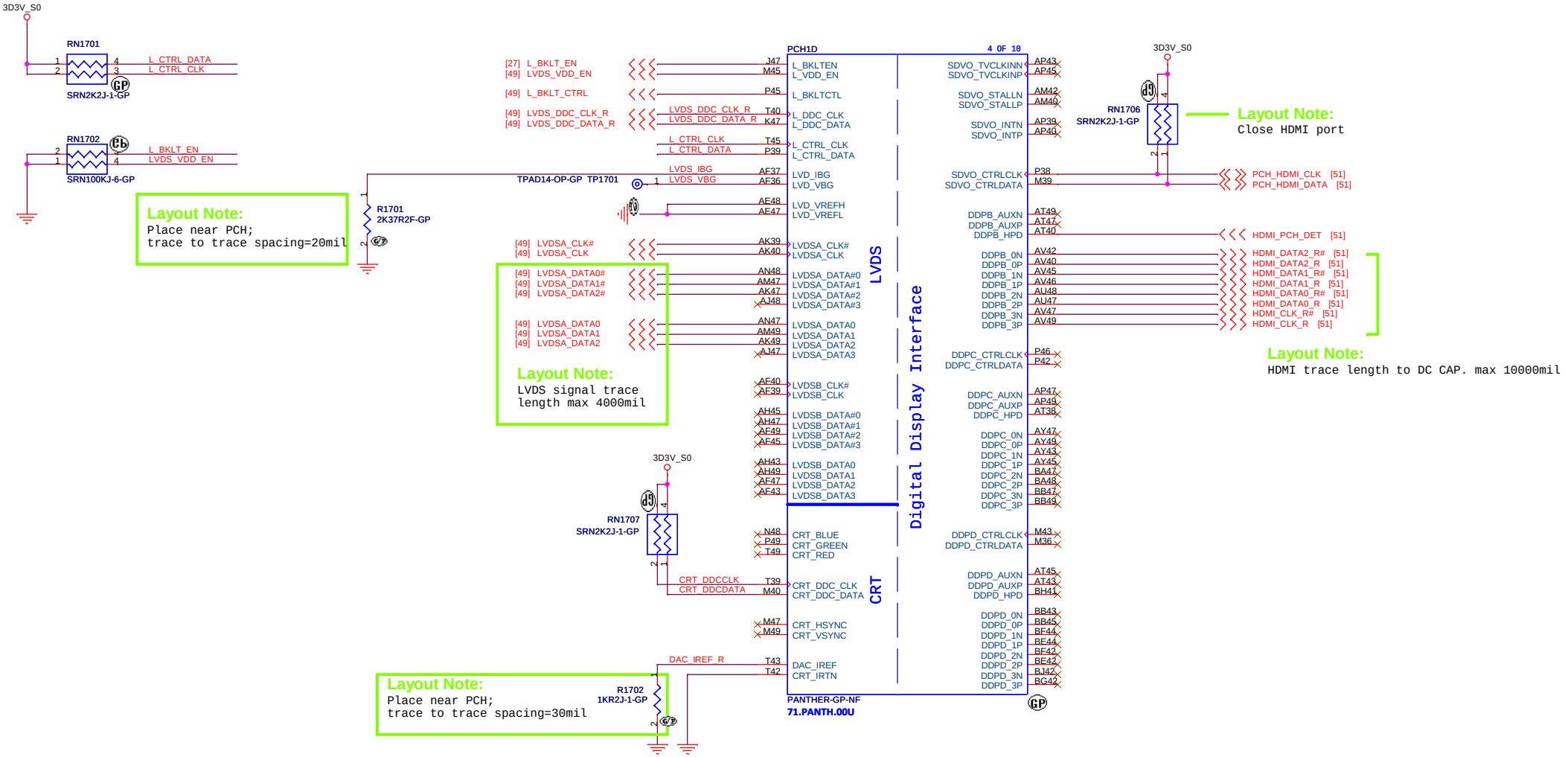
Title: ***Reserved***

Size	Document Number	Rev
A3	***BMW Z4 DIS***	***A00***

Date: Friday, March 30, 2012 Sheet 16 of 105

SSID = PCH



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Title: PCH (LVDS/CRT/DDI)

Size: A3 | Document Number: BMW Z4 DIS | Rev: A00

Date: Friday, March 30, 2012 | Sheet 17 of 105

SSID = PCH

USB3.0/2.0 Mapping Table

USB 3.0 Port	USB 2.0 port
Port 1	Port 0
Port 2	Port 1
Port 3	Port 2
Port 4	Port 3

USB Table

Pair	Device
0	USB3.0 port1, with Power Share
1	USB3.0 port2
2	NC
3	NC
4	Touch Panel
5	NC
6	NC
7	NC
8	WWAN
9	NC
10	Card reader
11	WLAN
12	CAMERA
13	NC

1. USB Ext. port 9 (HS) External debug port use on Chief River platform.
2. 2011 July; Microsoft will support USB3.0 debug--> Port1 useable.

Layout Note:
Trace Length :
PCH ~~9000mil~~Cap~~1000mil~~CONN

Layout Note:
1. USBRBIAS/# use 50ohm single-ended impedance spacing to other signal=15mil
2. Length < 500mil

Boot Bios Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

A16 Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

PCH1E
5 OF 10
PANTHER-GP-NF
RSVD
PCI
USB
USB2.0 Signal Group
X01 12/20
X01 12/13
X02 2/13

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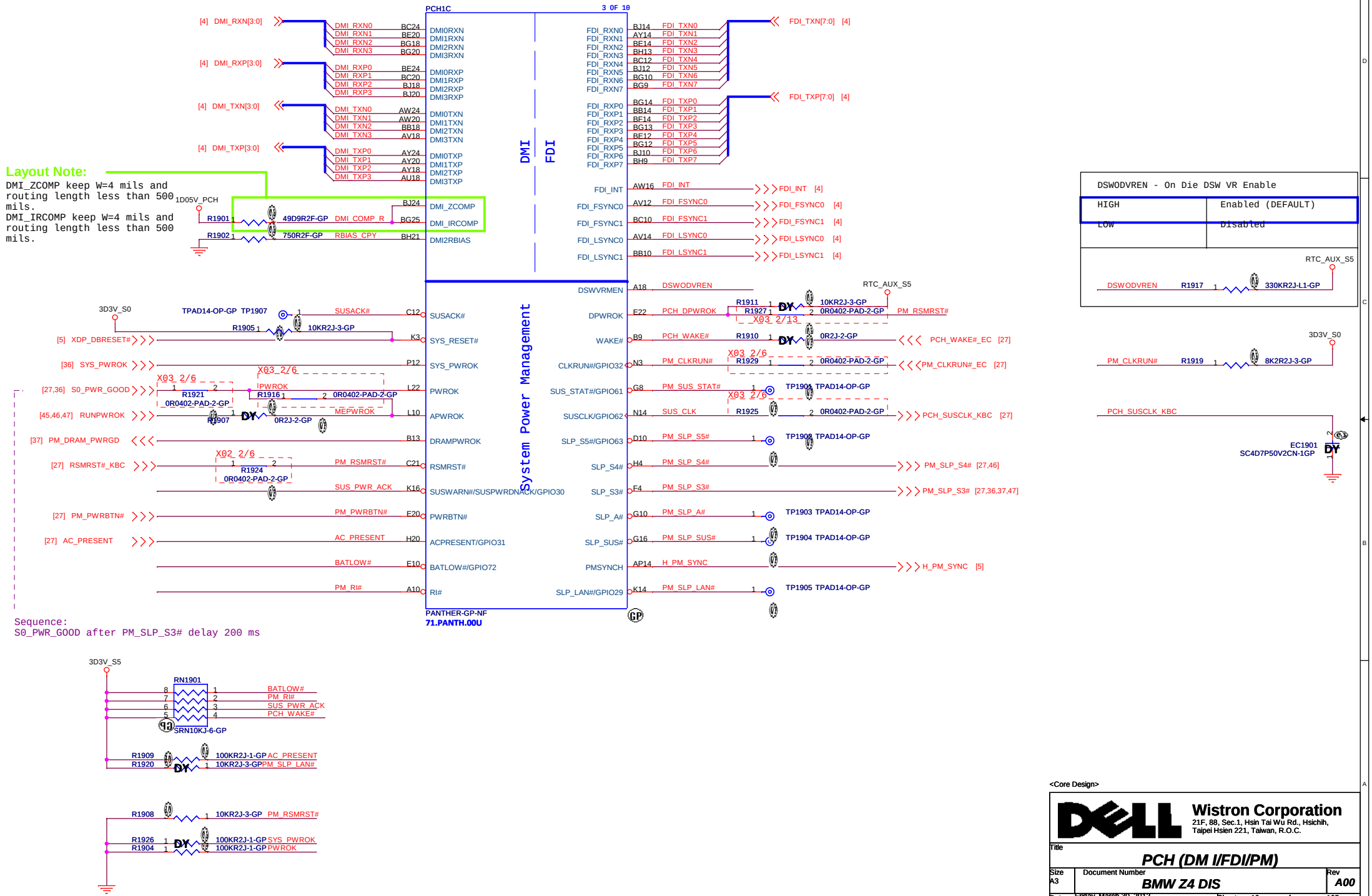
Title: PCH (PCI/USB/NVRAM)
Size: A3
Document Number: BMW Z4 DIS
Rev: A00
Date: Friday, March 30, 2012
Sheet 18 of 105

SSID = PCH



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Title: PCH (DM I/FDI/PM)

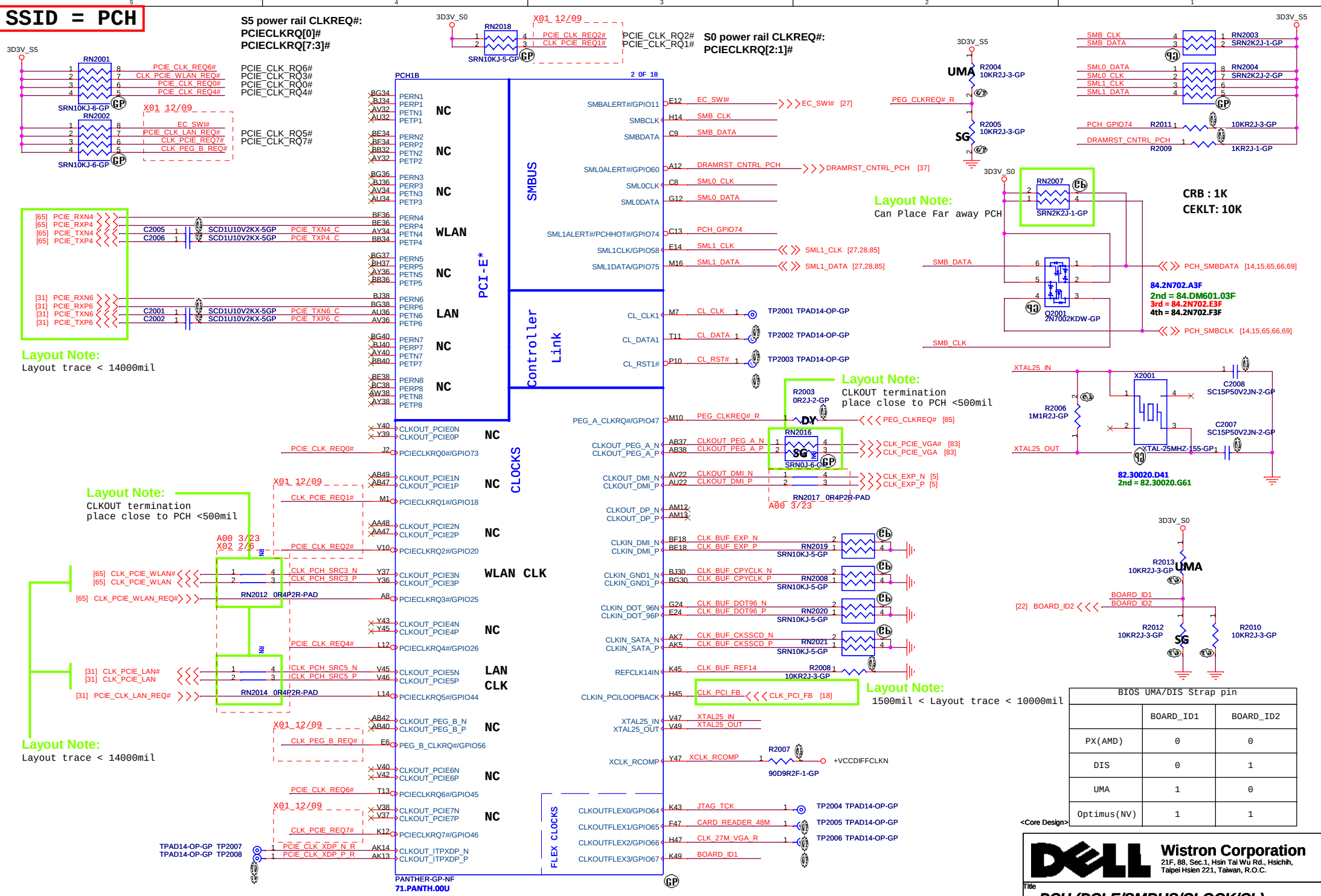
Size: A3 | Document Number: BMW Z4 DIS | Rev: A00

Date: Friday, March 30, 2012 | Sheet 19 of 105

SSID = PCH

S5 power rail CLKREQ#:
PCIECLKRQ[0]#
PCIECLKRQ[7:3]#

S0 power rail CLKREQ#:
PCIECLKRQ[2:1]#



BIOS UMA/DIS Strap pin		
	BOARD_ID1	BOARD_ID2
PX(AMD)	0	0
DIS	0	1
UMA	1	0
Optimus(NV)	1	1

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI-E/SMBUS/CLOCK/CL)

Size: A3 | Document Number: BMW Z4 DIS | Rev: A00

Date: Friday, March 30, 2012 | Sheet 20 of 105

SSID = PCH

Layout Note:
Place it at the open door location.

Integrated SUS 1V VRM Enable	
INTVRMEN	Low = External VRs High = Internal VRs*

Layout Note:
Place near PCH

A00 3/27

Layout Note:
Place close together.
For RNxxxx later.

Layout Note:
HDA_SDO and HDA_BCLK must be
length matched to within 500 mils

Layout Note:
Place at the separated point

Flash Descriptor Security Overide/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default * High = Enable

No Reboot Strap	
HDA_SPKR	Low = Default * High = No Reboot

PLL ODVR VOLTAGE	
HDA_SYNC	Low = 1.8V High = 1.5V *

HDA_SYNC:
This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

HDD1

mSATA

ODD

Layout Note:
HDD < 6000mil, mSATA < 6000mil, ODD < 12500mil

Layout Note:
Place close PCH(<500mil)

<Core Design>

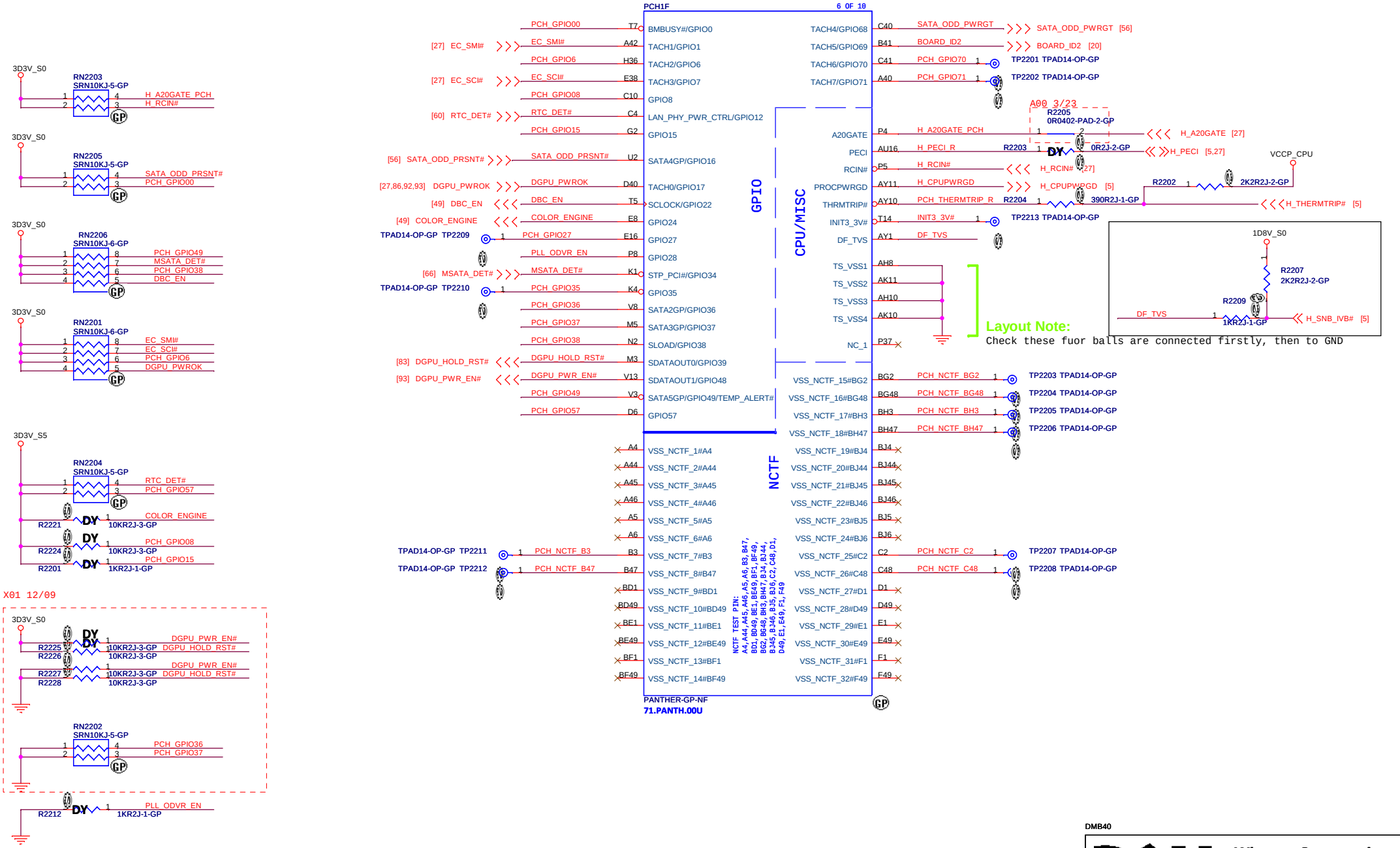
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (SPI/RTC/LPC/SATA/IHDA)

Size	Document Number	Rev
A3	BMW Z4 DIS	A00

Date: Friday, March 30, 2012 Sheet 21 of 105

SSID = PCH



X01 12/09

Layout Note:
Check these fuor balls are connected firstly, then to GND

PLL ON DIE VR ENABLE	
GPIO28 (PLL_ODVR_EN)	Weakly internal pull up 20k. High - Enable LOW - Disable

DMB40

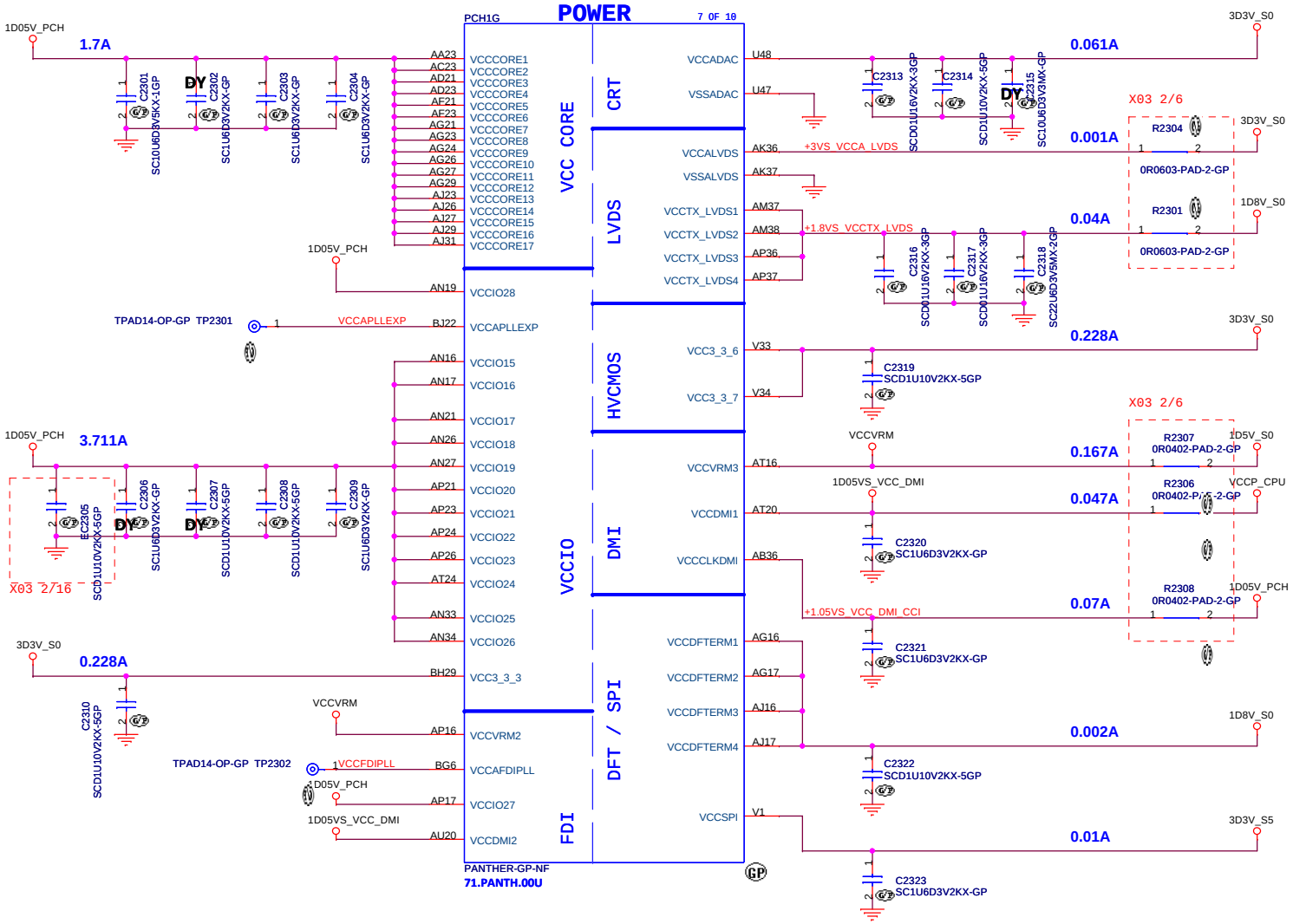
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (GPIO/CPU)**

Size	Document Number	Rev
A3	BMW Z4 DIS	A00

Date: Friday, March 30, 2012 Sheet 22 of 105

SSID = PCH



Voltage Rail	Voltage(V)	Iccmax(A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.063
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.7
VccDMI	1.1	0.047
VccIO	1.05	3.711
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW3_3	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6uA
VccSus3_3	3.3	0.095
VccSusHDA	3.3	0.01
VccVRM	1.5	0.167
VccClkDMI	1.05	0.07
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

Refer to chipset EDS V.0.7

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (POWER1)

Size: A3 | Document Number: BMW Z4 DIS | Rev: A00

Date: Friday, March 30, 2012 | Sheet 23 of 105

SSID = PCH

DG: none
CRB: 10uH

POWER

PCH1J — 10 OF 10

Clock and Miscellaneous

AD49	VCCACLK	VCCACLK
T16	VCCDSW3_3	3D3V_S5
V12	DCPSUSBYP	DCPSUSBYP
T38	VCC3_3_5	+V3.3S_VCC_CLKF33
BH23	VCCAPLLDMI2	+VCCAPLL_CPY_PCH
AL29	VCCIO14	
AL24	DCPSUS3	+VCCSUS1

USB

N26	VCCIO29	1D05V_PCH
P26	VCCIO30	
P28	VCCIO31	
T27	VCCIO32	
T29	VCCIO33	
T23	VCCSUS3_3_7	3D3V_S5
T24	VCCSUS3_3_8	
V23	VCCSUS3_3_9	
V24	VCCSUS3_3_10	
P24	VCCSUS3_3_6	3D3V_S5
T26	VCCIO34	1D05V_PCH
M26	V5REF_SUS	+5VA_PCH_VCC5REFSUS
AN23	DCPSUS4	+VCCA_USBSUS
AN24	VCCSUS3_3_1	3D3V_S5

PCI/GPIO/LPC

P34	V5REF	+5VS_PCH_VCC5REF
N20	VCCSUS3_3_2	3D3V_S5
N22	VCCSUS3_3_3	
P20	VCCSUS3_3_4	3D3V_S0
P22	VCCSUS3_3_5	
AA16	VCC3_3_1	
W16	VCC3_3_8	3D3V_S0
T34	VCC3_3_4	

SATA

AJ2	VCC3_3_2	3D3V_S0
AF13	VCCIO5	
AH13	VCCIO12	1D05V_PCH
AH14	VCCIO13	
AF14	VCCIO6	
AK1	VCCAPLLSATA	+V1.05S_VCCAPLL_SATA3
AF11	VCCVRM1	VCCVRM

MISC

AC16	VCCIO2	
AC17	VCCIO3	1D05V_PCH
AD17	VCCIO4	
T21	VCCASW22	1D05V_PCH
V21	VCCASW23	
T19	VCCASW21	
P32	VCCSUSHDA	+3VS_+1.5VS_HDA_IO

CPU

AA19	VCCASW1	1D05V_PCH
AA21	VCCASW2	
AA24	VCCASW3	
AA26	VCCASW4	
AA27	VCCASW5	
AA29	VCCASW6	
AA31	VCCASW7	
AC26	VCCASW8	
AC27	VCCASW9	
AC29	VCCASW10	
AC31	VCCASW11	
AD29	VCCASW12	
AD31	VCCASW13	
W21	VCCASW14	
W23	VCCASW15	
W24	VCCASW16	
W26	VCCASW17	
W29	VCCASW18	
W31	VCCASW19	
W33	VCCASW20	
N16	DCPRTC	+VCCRTCEXT
Y49	VCCVRM4	VCCVRM
BD47	VCCADPLLA	+1.05VS_VCCA_A_DPL
BF47	VCCADPLLB	+1.05VS_VCCA_B_DPL
AF17	VCCIO7	+VCCDIFFCLK
AF33	VCCDIFFCLKN1	
AF34	VCCDIFFCLKN2	
AG34	VCCDIFFCLKN3	
AG33	VCCSSC	+V1.05S_SSCVCC
V16	DCPSST	+VCCSST
T17	DCPSUS1	TP2405 TPAD14-OP-GP DCPSUS
V19	DCPSUS2	
BJ8	V_PROC_IO	VCCP_CPU
A22	VCCRTC	RTC_AUX_S5

RTC

HDA

PANTHER-GP-NF
71.PANTH.00U

3D3V_S5 — 0.001A — TP2401 TPAD14-OP-GP — C2416 SCD1U10V2KX-5GP

3D3V_S0 — L2401 IND-10UH-218-GP — 68.10050.10Y — 2nd = 68.1001E.10N — C2401 SC10U6D3V5KX-1GP (DY) — C2402 SC1U6D3V2KX-GP

1D05V_PCH — TP2403 TPAD14-OP-GP — C2417 SC4D7U6D3V3KX-GP

TP2402 TPAD14-OP-GP — C2418 SCD1U10V2KX-5GP — C2420 SCD1U10V2KX-5GP

TP2404 TPAD14-OP-GP — C2421 SCD1U10V2KX-5GP — C2422 SCD1U10V2KX-5GP

1D05V_PCH — 0.93A — C2403 SC22U6D3V5MX-2GP (DY) — C2404 SC22U6D3V5MX-2GP — C2406 SC1U6D3V2KX-GP — C2405 SC1U6D3V2KX-GP (DY) — C2419 SC1U6D3V2KX-GP (DY)

X01 1/9

1D05V_PCH — L2402 IND-10UH-218-GP — 68.10050.10Y — 2nd = 68.1001E.10N — 0.08A — +1.05VS_VCCA_A_DPL — C2408 SC10U6D3V5KX-1GP (DY) — C2407 SC1U6D3V2KX-GP

L2403 IND-10UH-218-GP — 68.10050.10Y — 2nd = 68.1001E.10N — 0.08A — +1.05VS_VCCA_B_DPL — EC2409 SCD1U10V2KX-5GP — C2410 SC1U6D3V2KX-GP

X03 2/16

+VCCRTCEXT — C2411 SCD1U10V2KX-5GP

VCCVRM — 0.167A

1D05V_PCH — 0.055A — +VCCDIFFCLKN — R2412 0R0603-PAD-2-GP — C2414 SC1U6D3V2KX-GP

X03 2/6

+V1.05S_SSCVCC — C2415 SCD1U10V2KX-5GP

+VCCSST — TP2405 TPAD14-OP-GP — DCPSUS

VCCP_CPU — 0.001A

RTC_AUX_S5 — 6uA — C2436 SC1U6D3V2KX-GP

X03 2/6

1D05V_PCH — R2403 0R0402-PAD-2-GP — +VCCDIFFCLK — C2412 SC1U6D3V2KX-GP

1D05V_PCH — R2404 0R0402-PAD-2-GP — 0.095A — +V1.05S_SSCVCC — C2413 SC1U6D3V2KX-GP

1D05V_PCH — C2438 SC1U6D3V2KX-GP

3D3V_S5 — 0.095A — C2424 SCD1U10V2KX-5GP

3D3V_S5 — (0.1uFx1) — C2425 SCD1U10V2KX-5GP

1D05V_PCH — 0.001A — +5VA_PCH_VCC5REFSUS

3D3V_S5 — C2437 SC1U10V2KX-1GP (DY) — 0.001A — +5VS_PCH_VCC5REF

3D3V_S5 — C2428 SC1U6D3V2KX-GP

3D3V_S0 — C2430 SCD1U10V2KX-5GP

3D3V_S0 — C2431 SCD1U10V2KX-5GP

3D3V_S0 — C2429 SCD1U10V2KX-5GP

1D05V_PCH — C2432 SC1U6D3V2KX-GP (DY)

+V1.05S_VCCAPLL_SATA3 — TP2406 TPAD14-OP-GP — VCCVRM

1D05V_PCH — C2435 SC1U6D3V2KX-GP

1D05V_PCH — C2433 SCD1U10V2KX-5GP

+3VS_+1.5VS_HDA_IO — 0.01A — R2402 0R0402-PAD-2-GP — 3D3V_S5

X03 2/6

3D3V_S5 — 5V_S5 — 83.R0304.A8F — 2nd = 83.R2004.B8F — D2401 CH751H-40PT-GP — R2408 10R2J-2-GP — C2426 SCD1U10V2KX-5GP

3D3V_S0 — 5V_S0 — 83.R0304.A8F — 2nd = 83.R2004.B8F — D2402 CH751H-40PT-GP — R2407 10R2J-2-GP — C2427 SC1U6D3V2KX-GP

Voltage Rail	Voltage(V)	Iccmax(A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.063
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.7
VccDMI	1.1	0.047
VccIO	1.05	3.711
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW3_3	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6uA
VccSus3_3	3.3	0.095
VccSusHDA	3.3	0.01
VccVRM	1.5	0.167
VccClkDMI	1.05	0.07
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

VCCSUSHDA need to be at either 3.3V or 1.5V.
All the CODEC I/O Voltages need to be at the same level either 3.3 V or 1.5 V.

DMB40

Refer to chipset EDS V.0.7

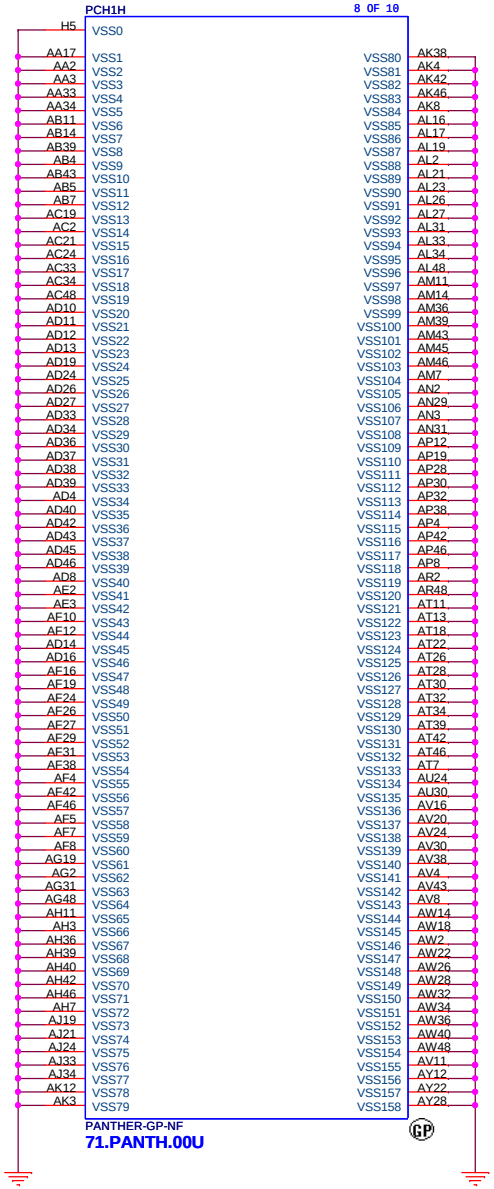
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

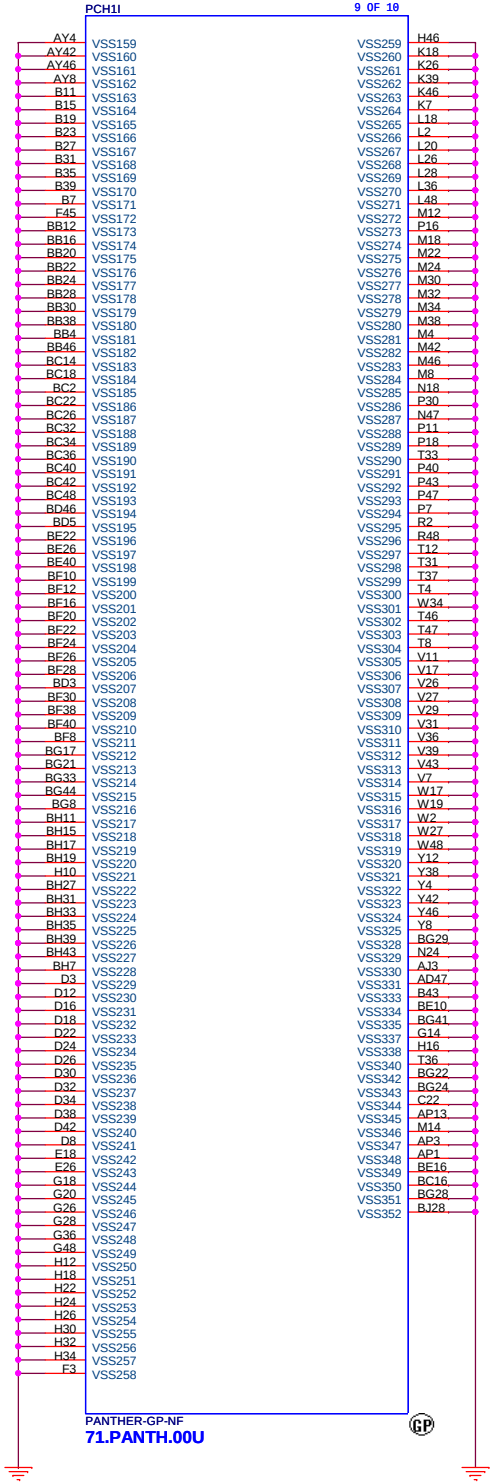
Title: PCH (POWER2)

Size: A3 | Document Number: BMW Z4 DIS | Rev: A00

Date: Friday, March 30, 2012 | Sheet 24 of 105

SSID = PCH





DMB40

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (VSS)

Size: A3 | Document Number: BMW Z4 DIS | Rev: A00

Date: Friday, March 30, 2012 | Sheet 25 of 105

(Blanking)

DMB40

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *BMW Z4 DIS* | Rev: *A00*

Date: Friday, March 30, 2012 | Sheet 26 of 105

SSID = KBC

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
X00	100.0K	10.0K	3.0V
X01	100.0K	20.0K	2.75V
X02	100.0K	33.0K	2.48V
X03	100.0K	47.0K	2.24V
A00	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

MODEL_ID_DET(GPIO07)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
TBD	100.0K	10.0K(64.10025.6DL)	3.0V
TBD	100.0K	13.7K(64.13725.6DL)	2.902V
TBD	100.0K	17.8K(64.17825.6DL)	2.801V
TBD	100.0K	22.1K(64.22125.6DL)	2.702V
TBD	100.0K	27.0K(64.27025.6DL)	2.598V
TBD	100.0K	32.4K(64.32425.6DL)	2.492V
TBD	100.0K	37.4K(64.37425.6DL)	2.402V
TBD	100.0K	43.2K(64.43225.6DL)	2.304V
TBD	100.0K	49.9K(64.49925.6DL)	2.201V
TBD	100.0K	57.6K(64.57625.6DL)	2.093V
TBD	100.0K	64.9K(64.64925.6DL)	2.001V
TBD	100.0K	73.2K(64.73225.6DL)	1.905V
TBD	100.0K	82.5K(64.82525.6DL)	1.808V
TBD	100.0K	93.1K(64.93125.6DL)	1.709V
TBD	100.0K	107K(64.10735.6DL)	1.594V
TBD	100.0K	120K(64.12035.6DL)	1.499V
TBD	100.0K	137K(64.13735.6DL)	1.392V
TBD	100.0K	154K(64.15435.6DL)	1.299V
TBD	100.0K	200K(64.20035.6DL)	1.099V
TBD	100.0K	232K(64.23236.6DL)	0.994V

TP

Charger

PCH

Layout Note:
Need very close to EC

Layout Note:
Need very close to EC

Layout Note:
Connect GND and AGND planes via either 0R resistor or connect directly.

Layout Note:
Need very close to EC

For System Reset.

AOAC Ambient temperature detect

EC_GPIO47 High Active

Power Switch Logic(PSL)

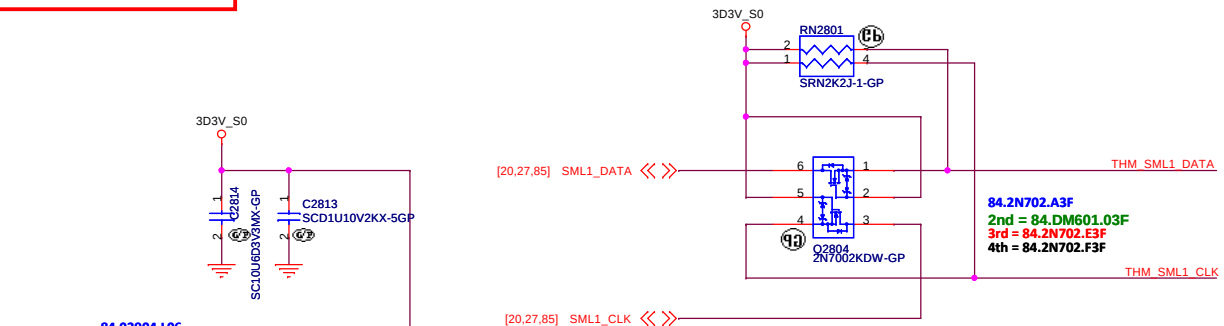
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC Nuvoton NPCE885

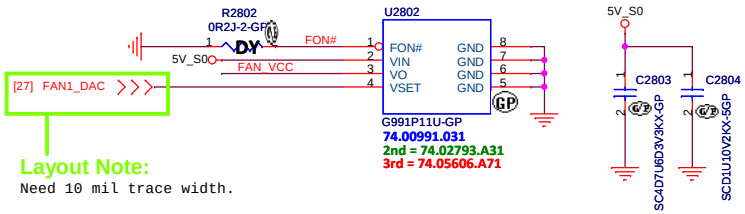
Size: A2 | Document Number: BMW Z4 DIS | Rev: A00

Date: Tuesday, April 03, 2012 | Sheet 27 of 105

SSID = Thermal

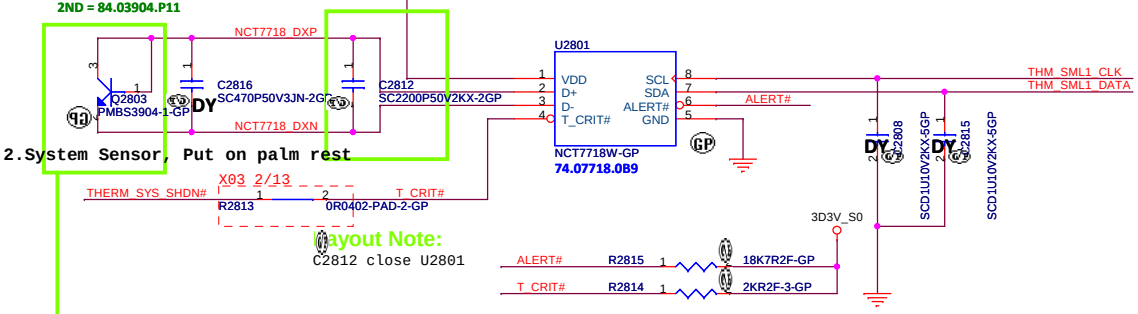


Fan controller



Layout Note:
Need 10 mil trace width.

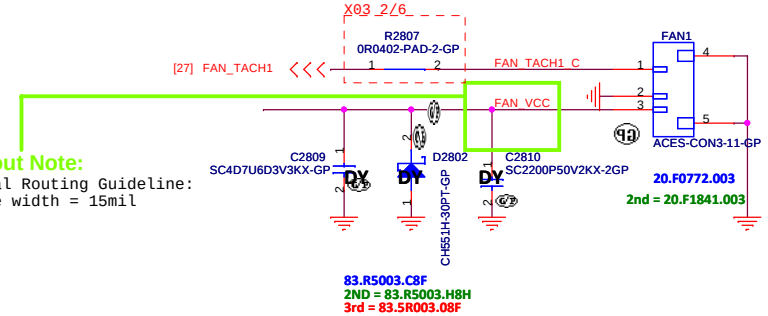
84.03904.L06
2ND = 84.03904.P11



2.System Sensor, Put on palm rest

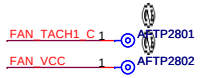
Layout Note:
C2812 close U2801

Layout Note:
Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

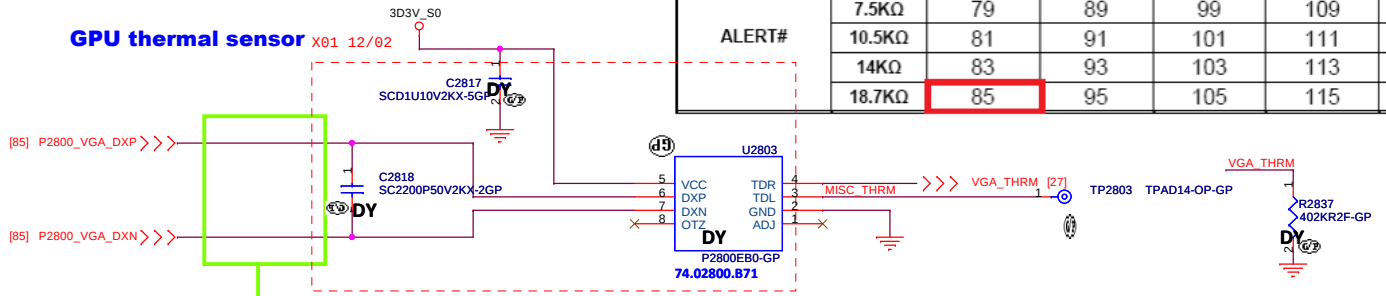


Layout Note:
Signal Routing Guideline:
Trace width = 15mil

TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

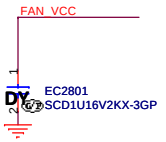


GPU thermal sensor

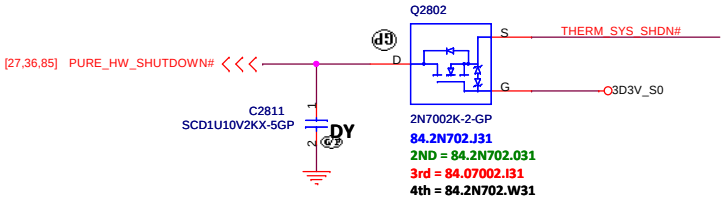


Layout Note:
Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

EMI



Thermal Sensor	
ADJ	Temp.(C)
Pull high	95
Pull low	90
Floating	85



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal NCT7718W/Fan Controllor P2793

Size: A3 | Document Number: BMW Z4 DIS | Rev: A00

Date: Friday, March 30, 2012 | Sheet 28 of 105

(Blanking)

DMB40

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *BMW Z4 DIS* | Rev: *A00*

Date: Friday, March 30, 2012 | Sheet 29 of 105

(Blanking)

DMB40

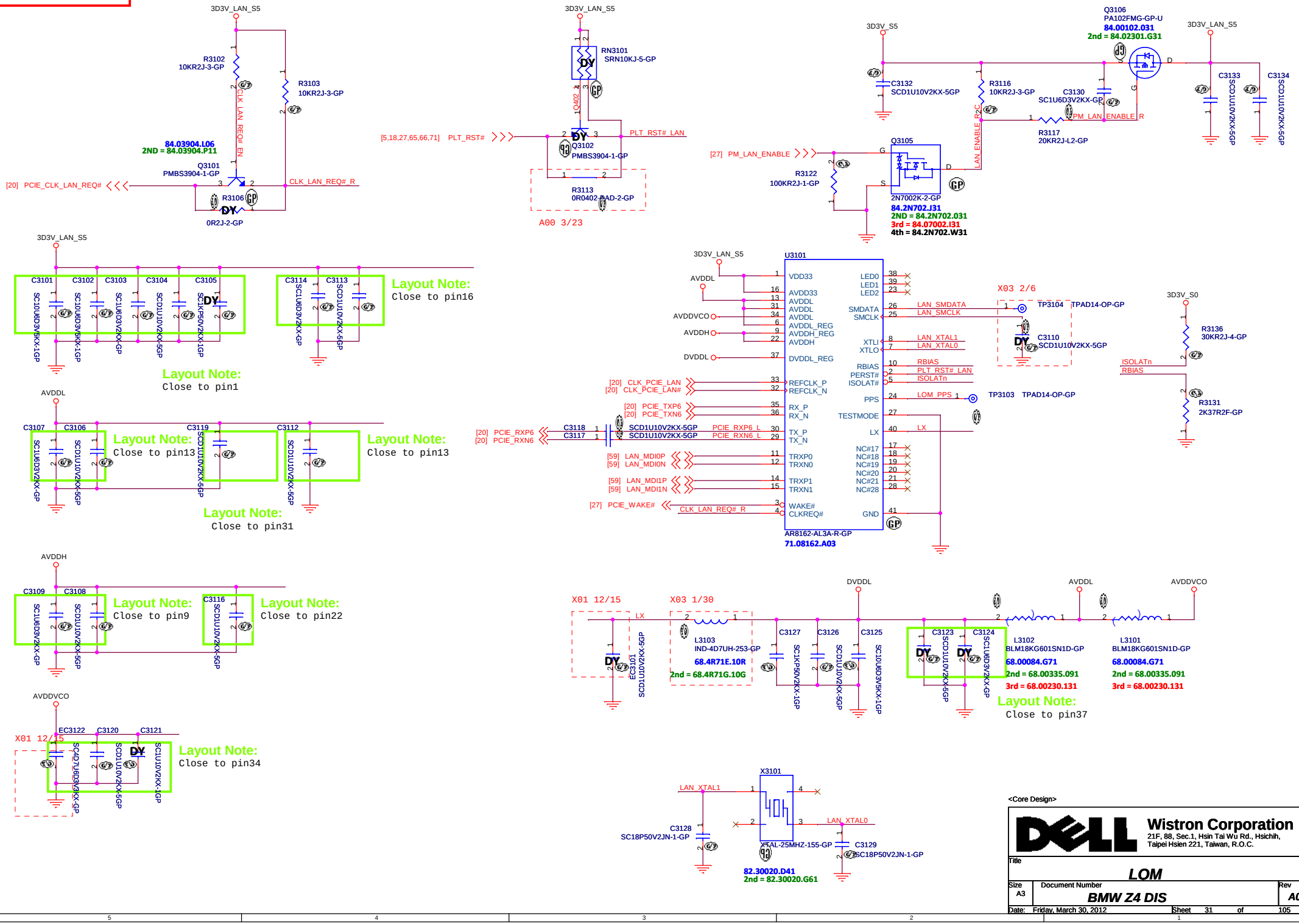
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*BMW Z4 DIS*	*A00*

Date: Friday, March 30, 2012 Sheet 30 of 105

SSID = LOM



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LOM	
Size: A3	Document Number: BMW Z4 DIS	Rev: A00
Date: Friday, March 30, 2012	Sheet 31 of 105	

(Blanking)

DMB40

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*BMW Z4 DIS*	*A00*

Date: Friday, March 30, 2012 Sheet 32 of 105

(Blanking)

DMB40

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*BMW Z4 DIS*	*A00*

Date: Friday, March 30, 2012 Sheet 33 of 105

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DMB40

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *BMW Z4 DIS* | Rev: *A00*

Date: Friday, March 30, 2012 | Sheet 34 of 105

(Blanking)

DMB40

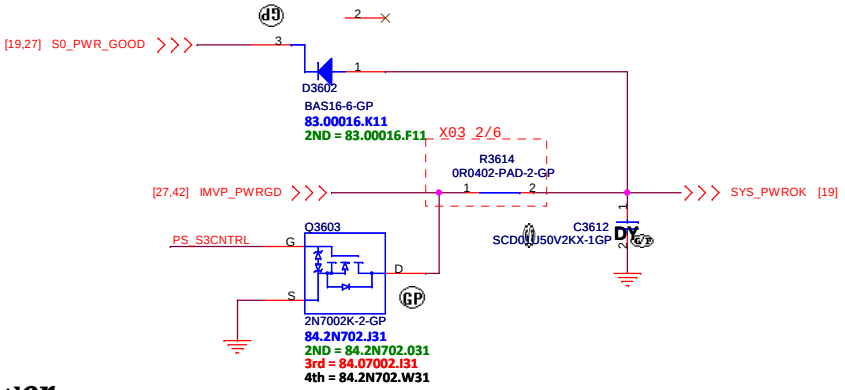
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

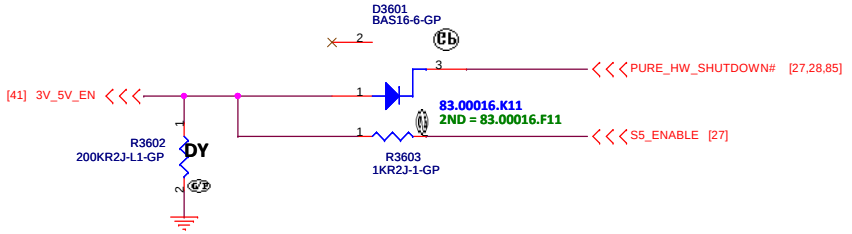
Title: *Reserved*

Size: A3 | Document Number: *BMW Z4 DIS* | Rev: *A00*

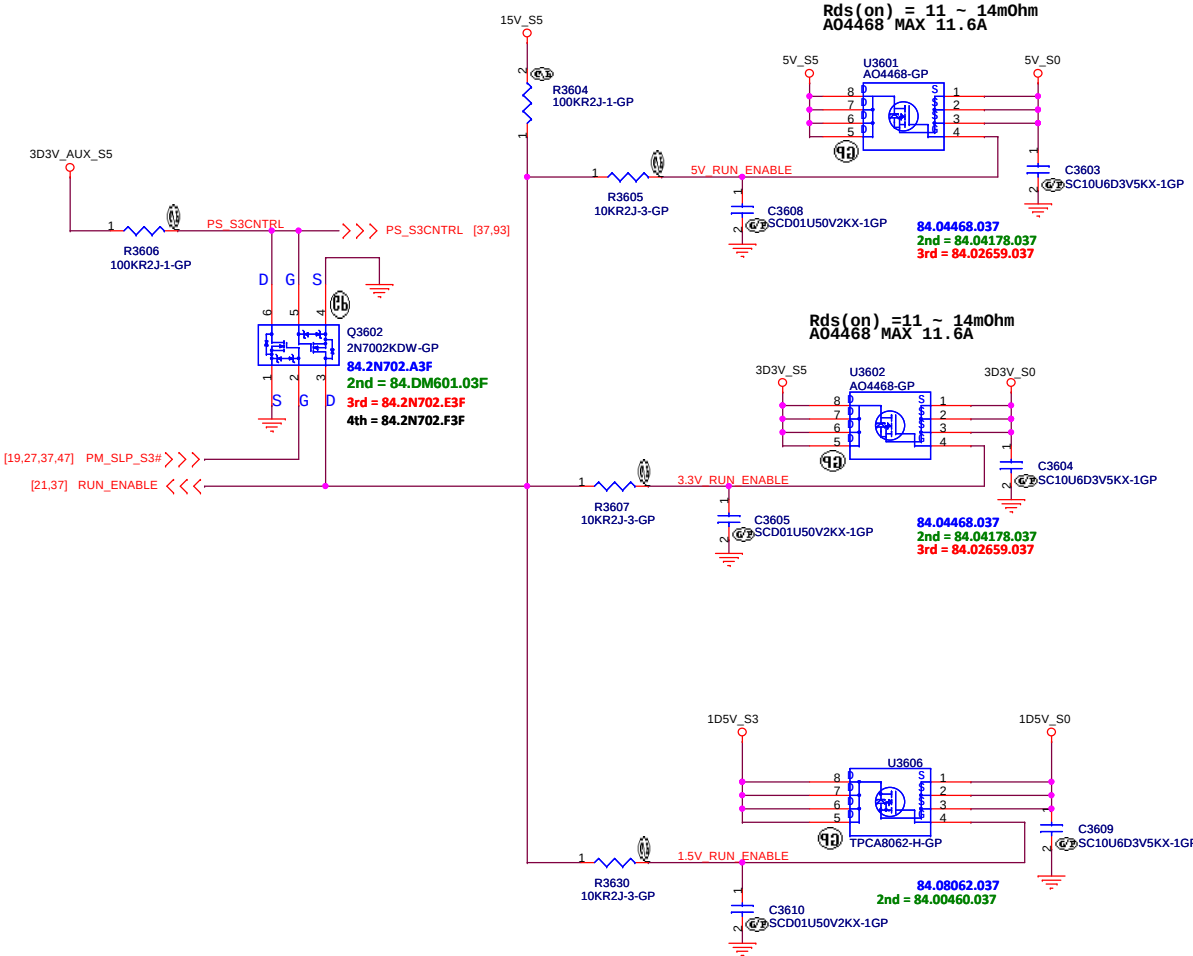
Date: Friday, March 30, 2012 | Sheet 35 of 105

SSID = Reset.Suspend





ROSA Run Power



5V_S0

5V_S0 Comsumption
Peak current 6A

3D3V_S0

3D3V_S0 Comsumption
Peak current 2.5A

1D5V_S0

TPCA8062-H-GP MAX 28A
Rds(on) = 4.1~5.6m Ohm
MAX Current 6A

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

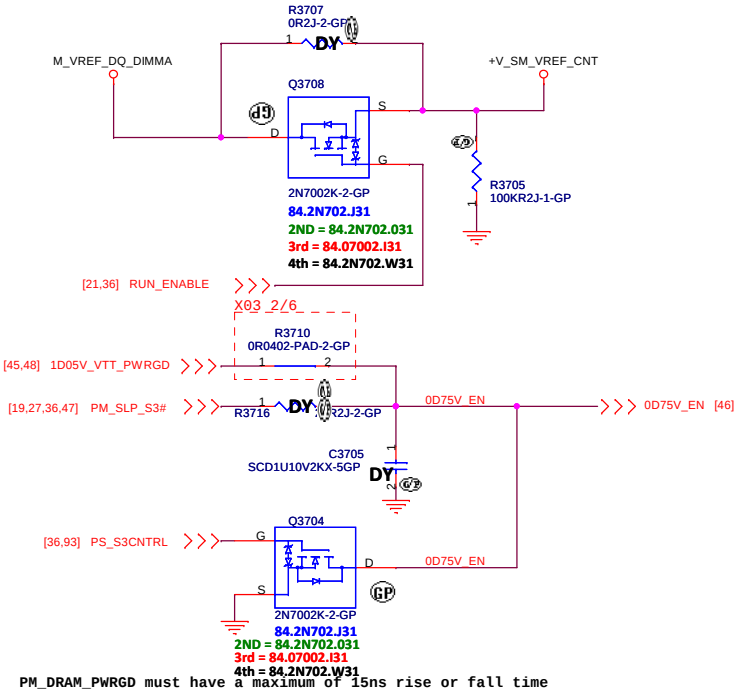
Title: Power Plane Enable

Size	Document Number	Rev
A3	BMW Z4 DIS	A00

Date: Friday, March 30, 2012 Sheet 36 of 105

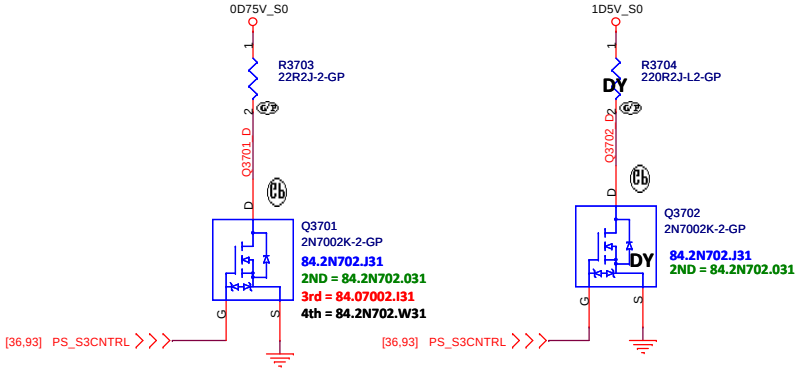
SSID = Reset.Suspend

Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation

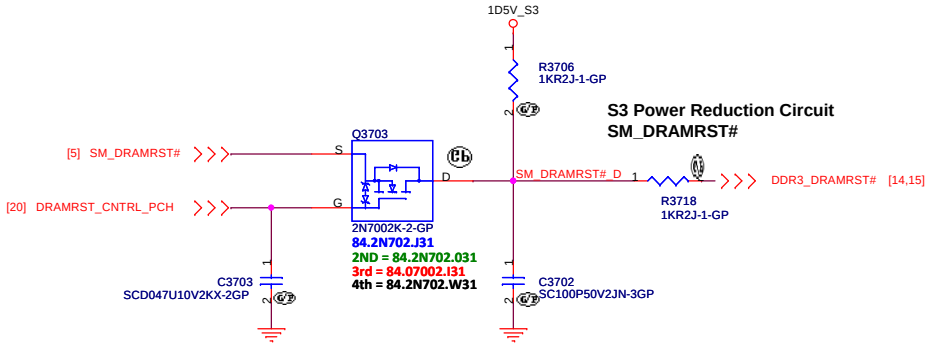


PM_DRAM_PWRGD must have a maximum of 15ns rise or fall time over VDDQ * 0.55± 200mV and the edge must be monotonic

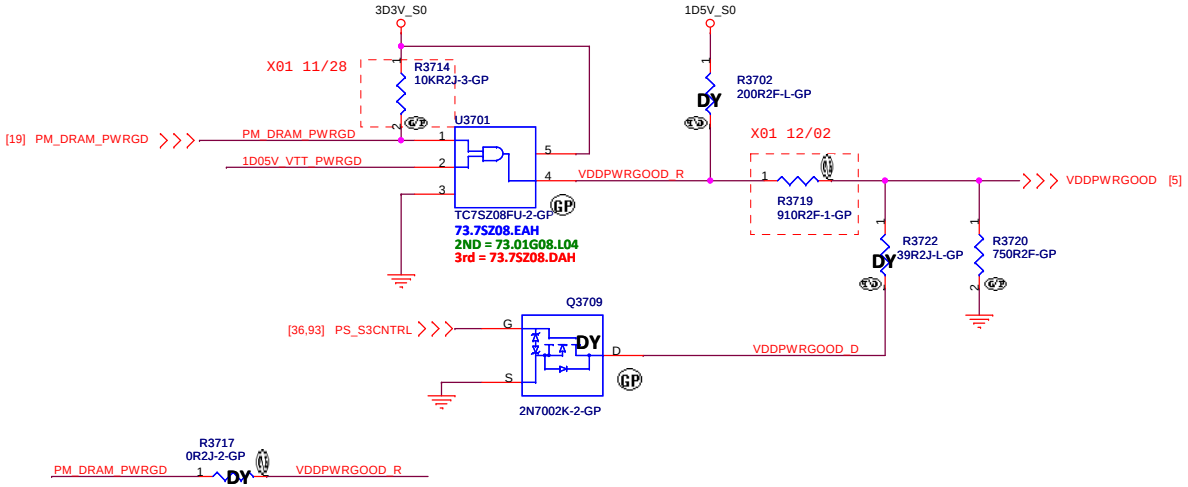
Close to DIMM
S3 Power Reduction Circuit PM_DRAM_PWRGD



Close to CPU
S3 Power Reduction Circuit SM_DRAMRST#



Close to CPU
S3 Power Reduction Circuit PM_DRAM_PWRGD



DMB40

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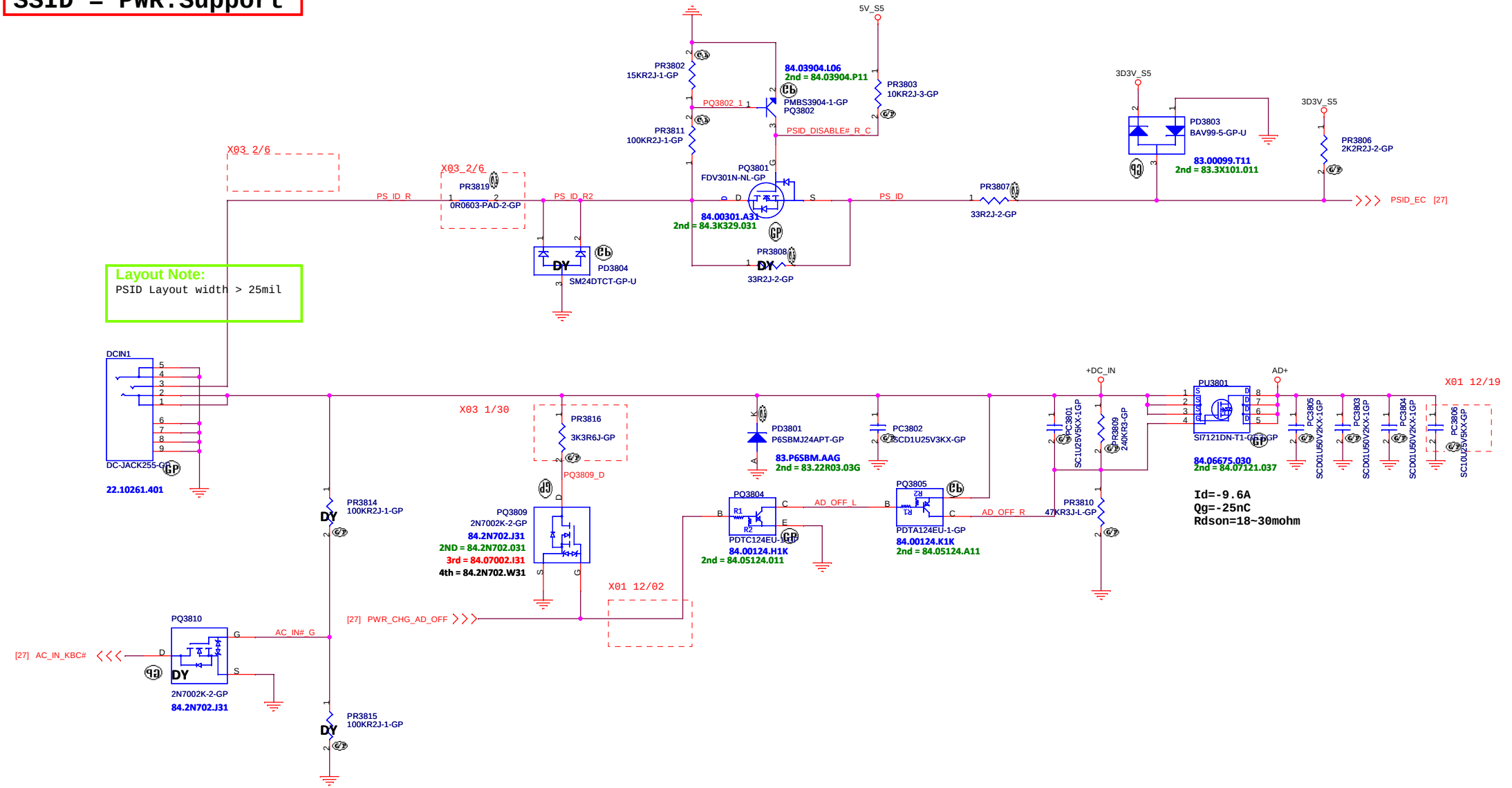
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: S3 Power Reduction		
Size: A3	Document Number: BMW Z4 DIS	Rev: A00
Date: Friday, March 30, 2012	Sheet 37 of 105	

SSID = PWR.Support

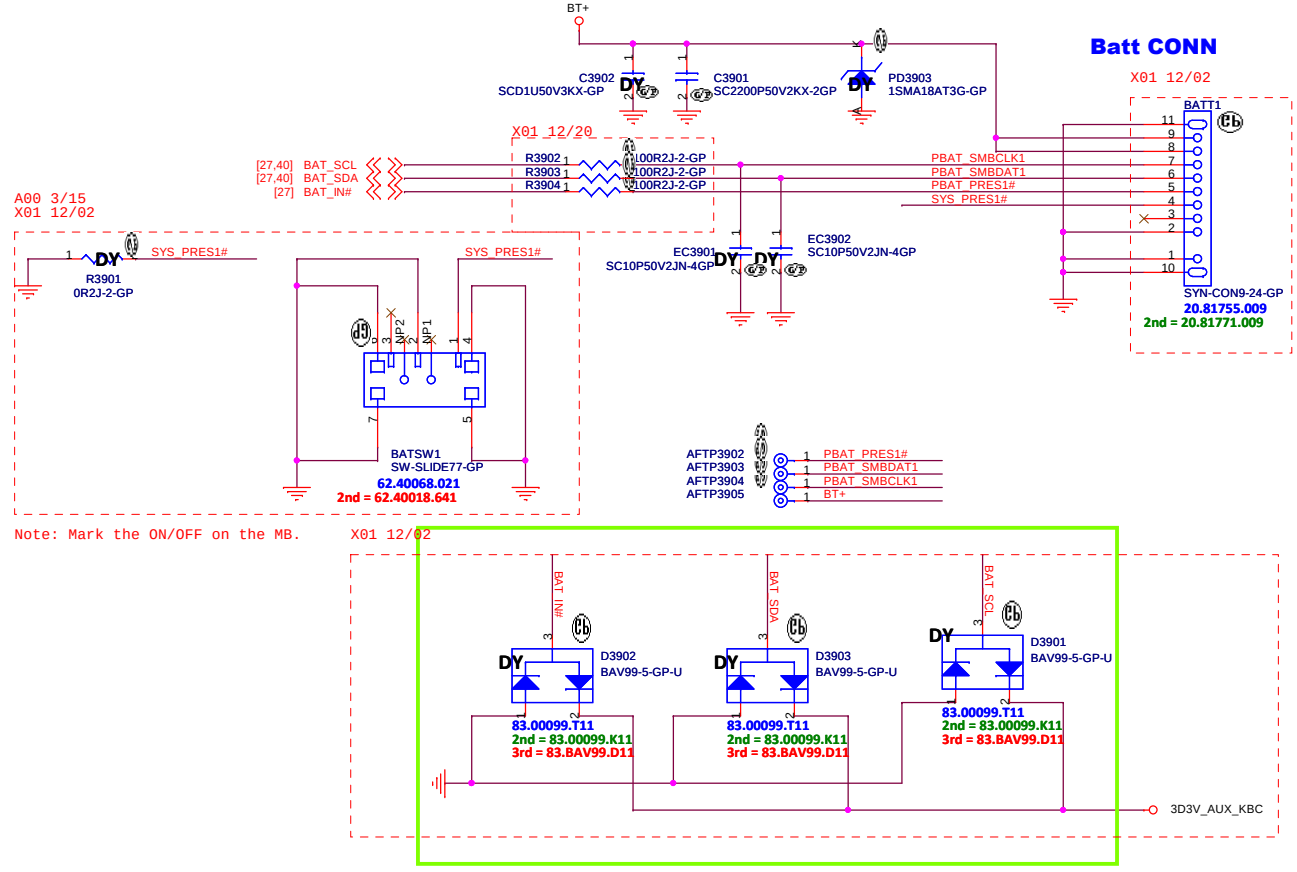


<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	DCIN	
Size: A3	Document Number: BMW Z4 DIS	Rev: A00
Date: Friday, March 30, 2012	Sheet 38 of 105	

SSID = PWR.Support



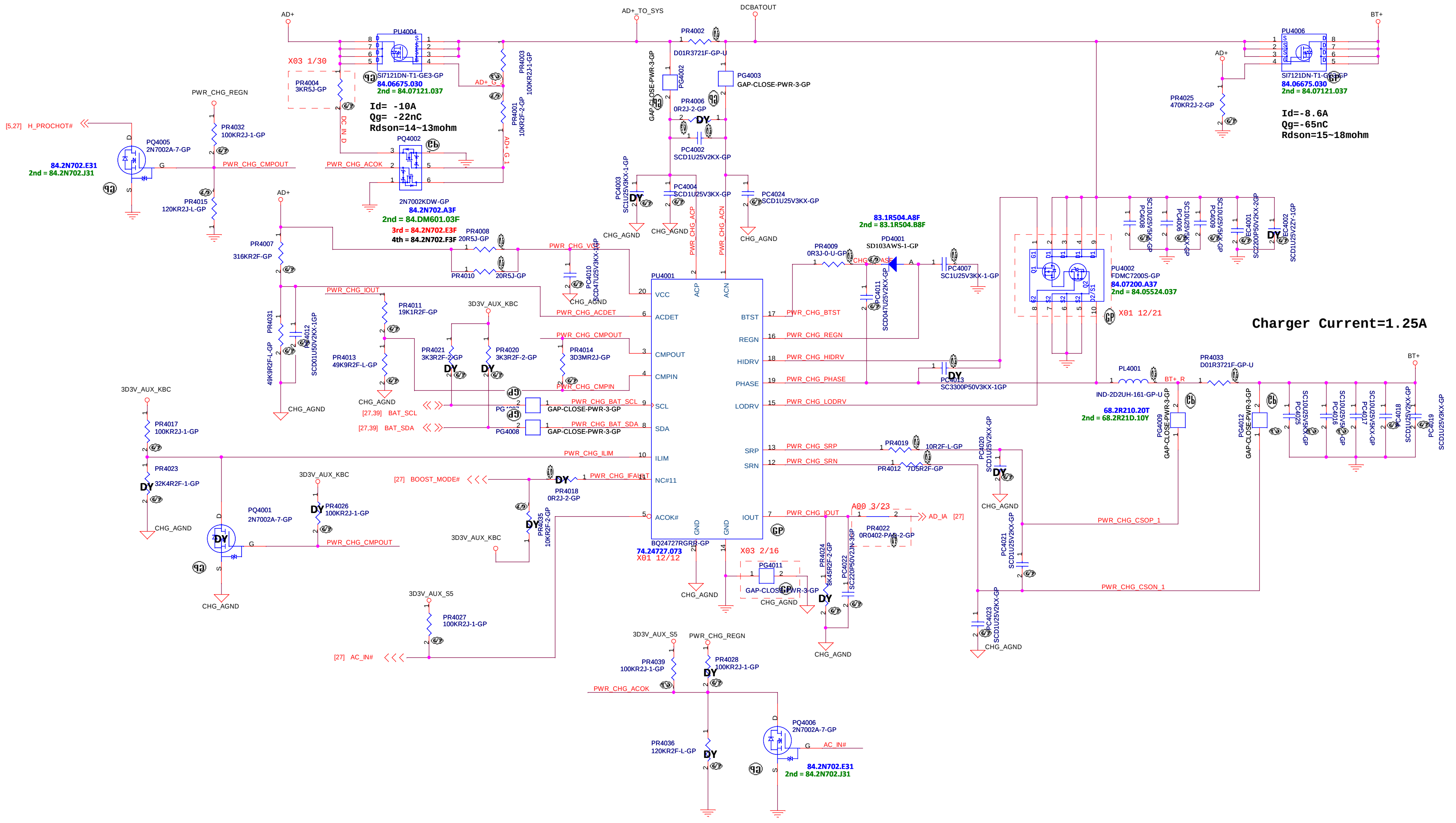
Layout Note:
Place near Battery CONN

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

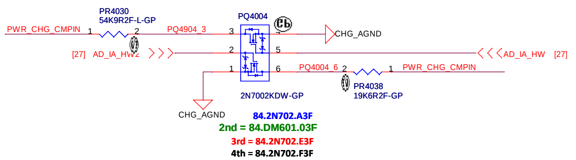
Title		
BATT CONN		
Size: A3	Document Number: BMW Z4 DIS	Rev: A00
Date: Friday, March 30, 2012	Sheet 39 of 105	

SSID = Charger



EC Code for BQ24727

H_PROCHOT#	AD_IA_HW	AD_IA_HW2
65W	0	0
90W	1	0
130W	0	1



<Core Design>

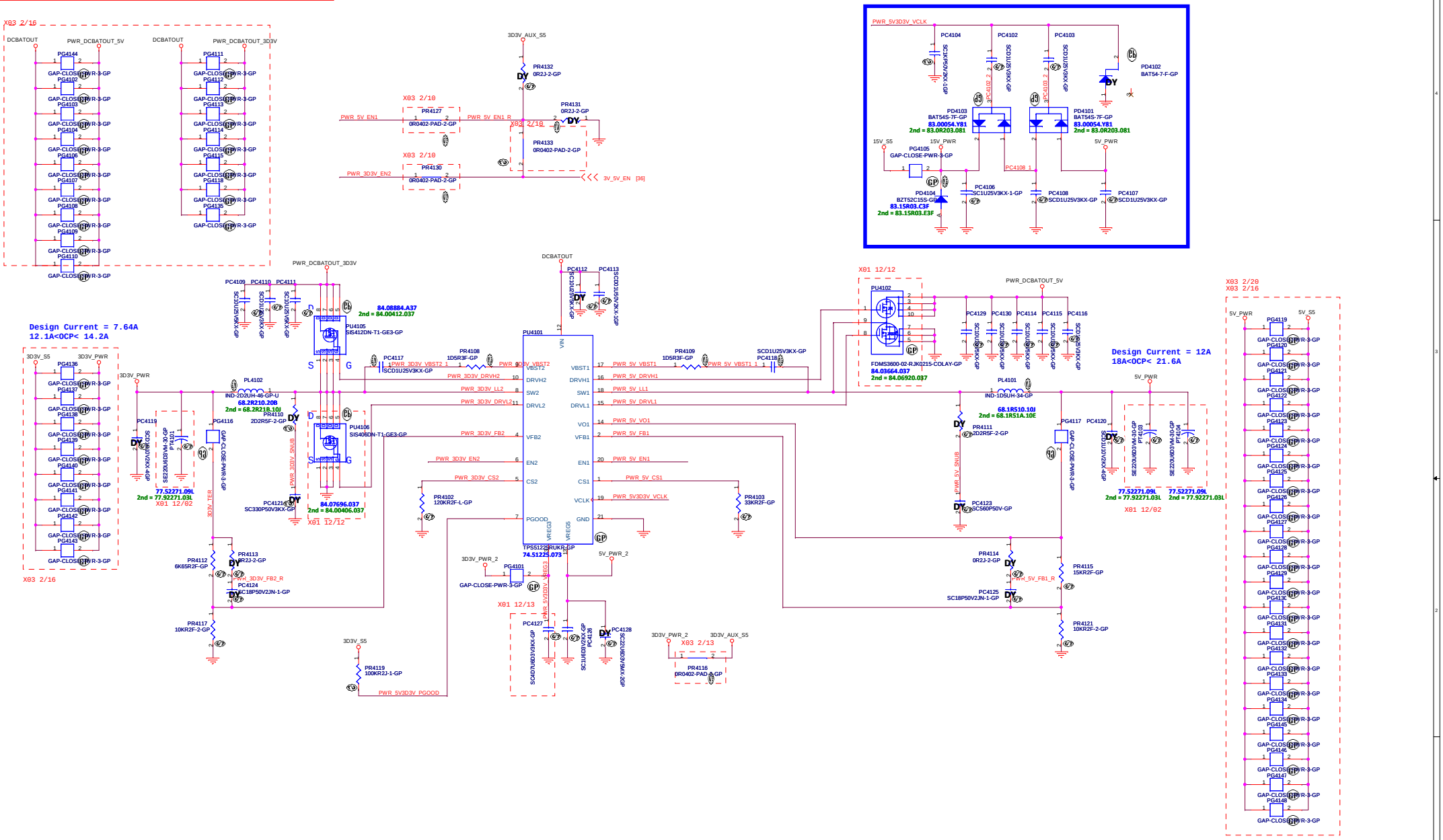
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER BQ24727

Size: A2 | Document Number: BMW Z4 DIS | Rev: A00

Date: Friday, March 30, 2012 | Sheet 40 of 105

SSID = PWR.Plane.Regulator_5v3p3v



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPS51123 5V/3D3V**

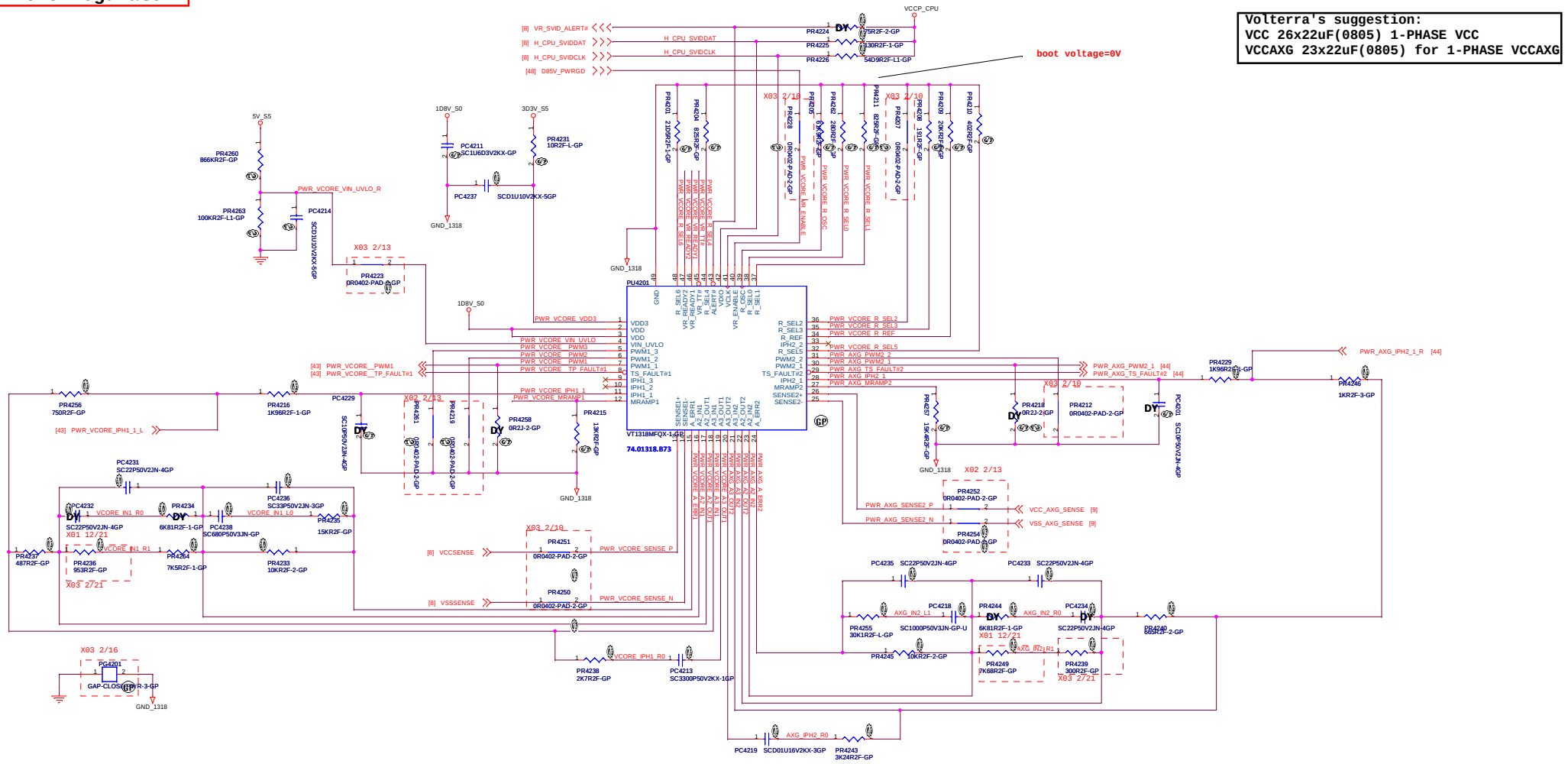
Size: A2 | Document Number: BMW Z4 DIS | Rev: A00

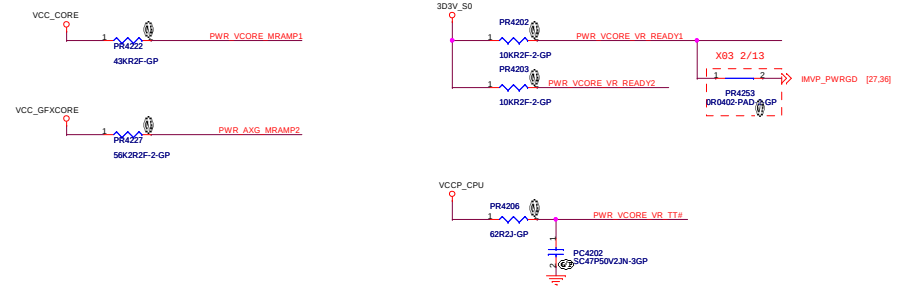
Date: Friday, March 30, 2012 | Sheet 41 of 105

SSID = CPU.Regulator

Volterra's suggestion:
VCC 26x22uF(0805) 1-PHASE VCC
VCCAXG 23x22uF(0805) for 1-PHASE VCCAXG

boot voltage=0V

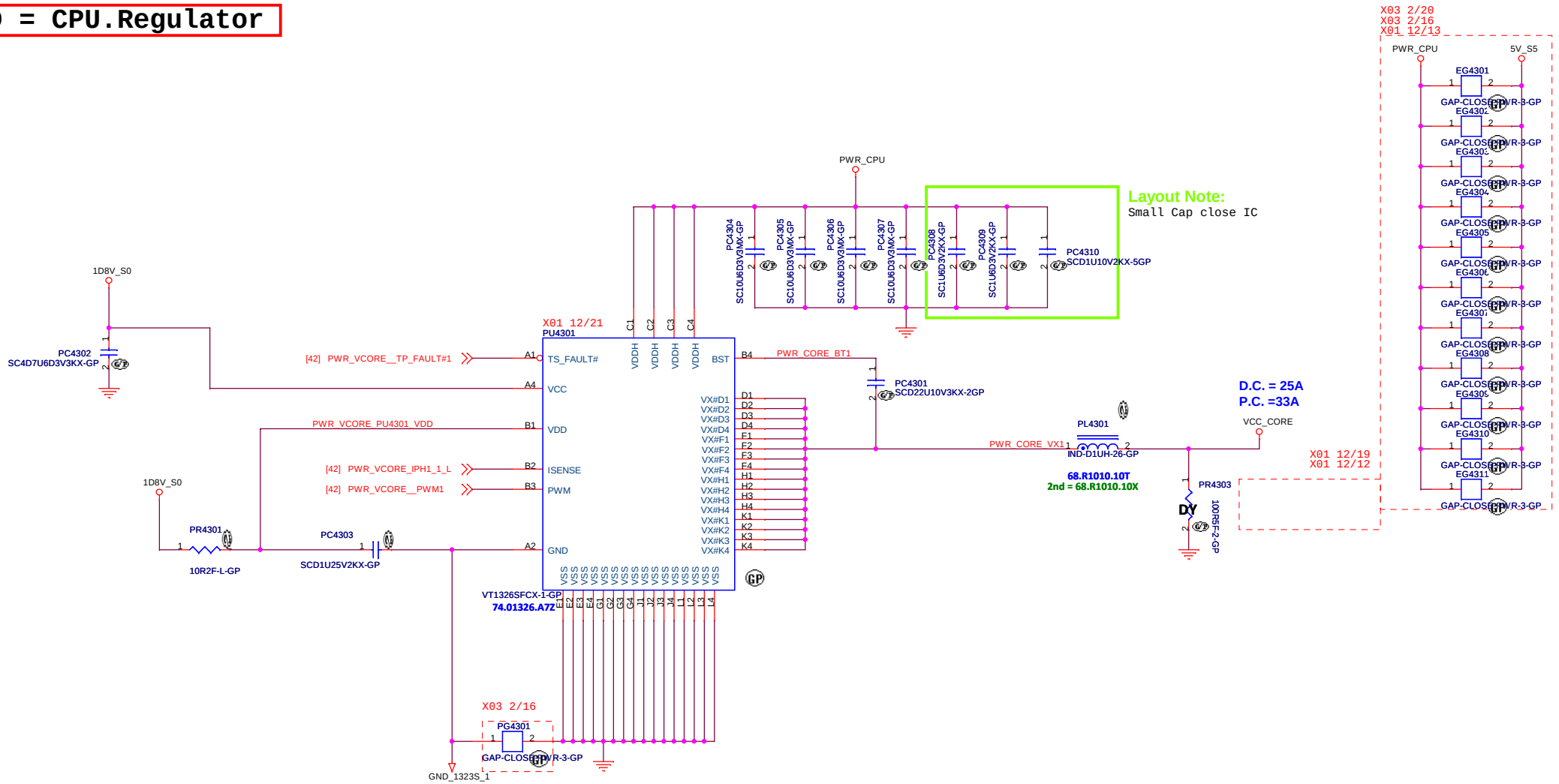




<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VT1318+1323_CPU_CORE1+1(1/3)
Size: A2
Document Number: BMW Z4 DIS
Rev: A00
Date: Friday, March 30, 2012
Sheet 42 of 105

SSID = CPU.Regulator



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *VT1318+1326_CPU_CORE2+1(2/3)*

Size	Document Number	Rev
A3	*BMW Z4 DIS*	*A00*

Date: Friday, March 30, 2012 Sheet 43 of 105

SSID = CPU.Regulator

X03 2/20
X03 2/16
X01 12/20
X01 12/13

PWR_CPU
5V_S5

EG4401 GAP-CLOSE-PWR-3-GP
EG4402 GAP-CLOSE-PWR-3-GP
EG4403 GAP-CLOSE-PWR-3-GP
EG4404 GAP-CLOSE-PWR-3-GP
EG4405 GAP-CLOSE-PWR-3-GP
EG4406 GAP-CLOSE-PWR-3-GP
EG4407 GAP-CLOSE-PWR-3-GP
EG4408 GAP-CLOSE-PWR-3-GP
EG4409 GAP-CLOSE-PWR-3-GP
EG4410 GAP-CLOSE-PWR-3-GP
EG4411 GAP-CLOSE-PWR-3-GP

X01 12/20

PWR_CPU

PC4403 SC10U6D3V3MX-GP
PC4404 SC10U6D3V3MX-GP
PC4405 SC10U6D3V3MX-GP
PC4406 SC10U6D3V3MX-GP
PC4407 SC1U6D3V2KX-GP
PC4408 SCD1U10V2KX-5GP

Layout Note:
Small Cap close IC

1D8V_S0

PC4401 SC4D7U6D3V3KX-GP

X01 12/21

PU4401

[42] PWR_AXG_TS_FAULT#2 → A1 TS_FAULT#
A4 VCC
PWR_AXG_PU4401_VDD → B1 VDD
[42] PWR_AXG_IPH2_1_R → B2 ISENSE
[42] PWR_AXG_PWM2_1 → B3 PWM
A2 GND

C1 C2 C3 C4 VDDH
B4 BST → PWR_AXG_BT3

VX#H4 H4
VX#H3 H3
VX#H2 H2
VX#H1 H1
VX#F4 F4
VX#F3 F3
VX#F2 F2
VX#F1 F1
VX#D4 D4
VX#D3 D3
VX#D2 D2
VX#D1 D1

VSS E1 E2 E3 E4 G1 G2 G3 G4 J1 J2 J3 J4

VT1323SFCX-1-GP
74.01323.A7Z

PC4409 SCD22U10V3KX-2GP

PL4401 IND-D1UH-26-GP
PWR_AVG_VX1

D.C. = 22A
P.C. =33A

VCC_GFXCORE

PR4402 DY 100R5F-2-GP

1D8V_S0

PR4401 10R2F-L-GP

PC4402 SCD1U25V2KX-GP

X03 2/16

PG4401 GAP-CLOSE-PWR-3-GP

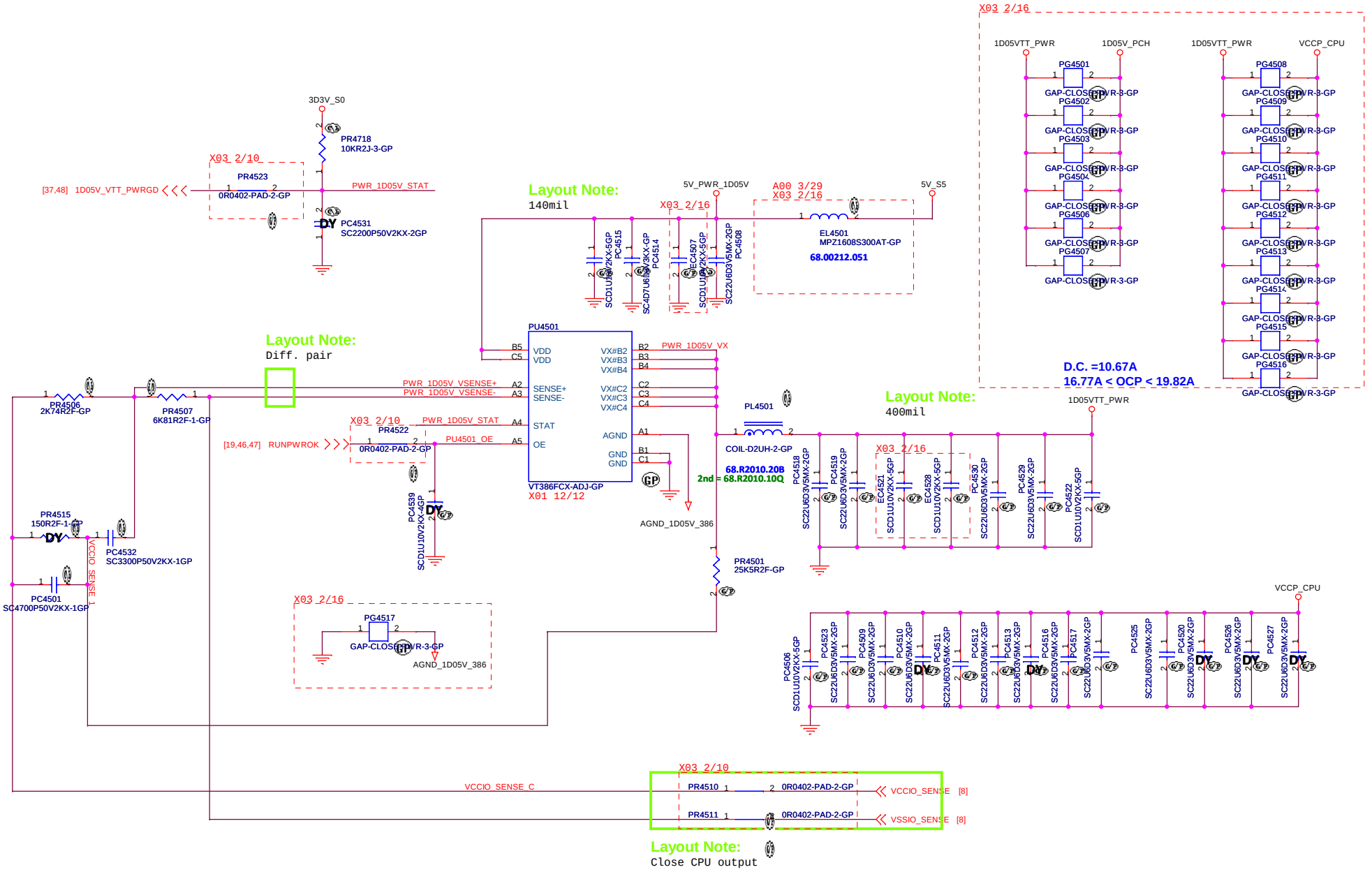
GND_1323S_3

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	VT1318+1323_CPU_CORE1+1(3/3)	
Size A3	Document Number BMW Z4 DIS	Rev A00
Date: Friday, March 30, 2012	Sheet 44 of 105	

SSID = PWR.Plane.Regulator_1p05v



<Core Design>

Wistron Corporation
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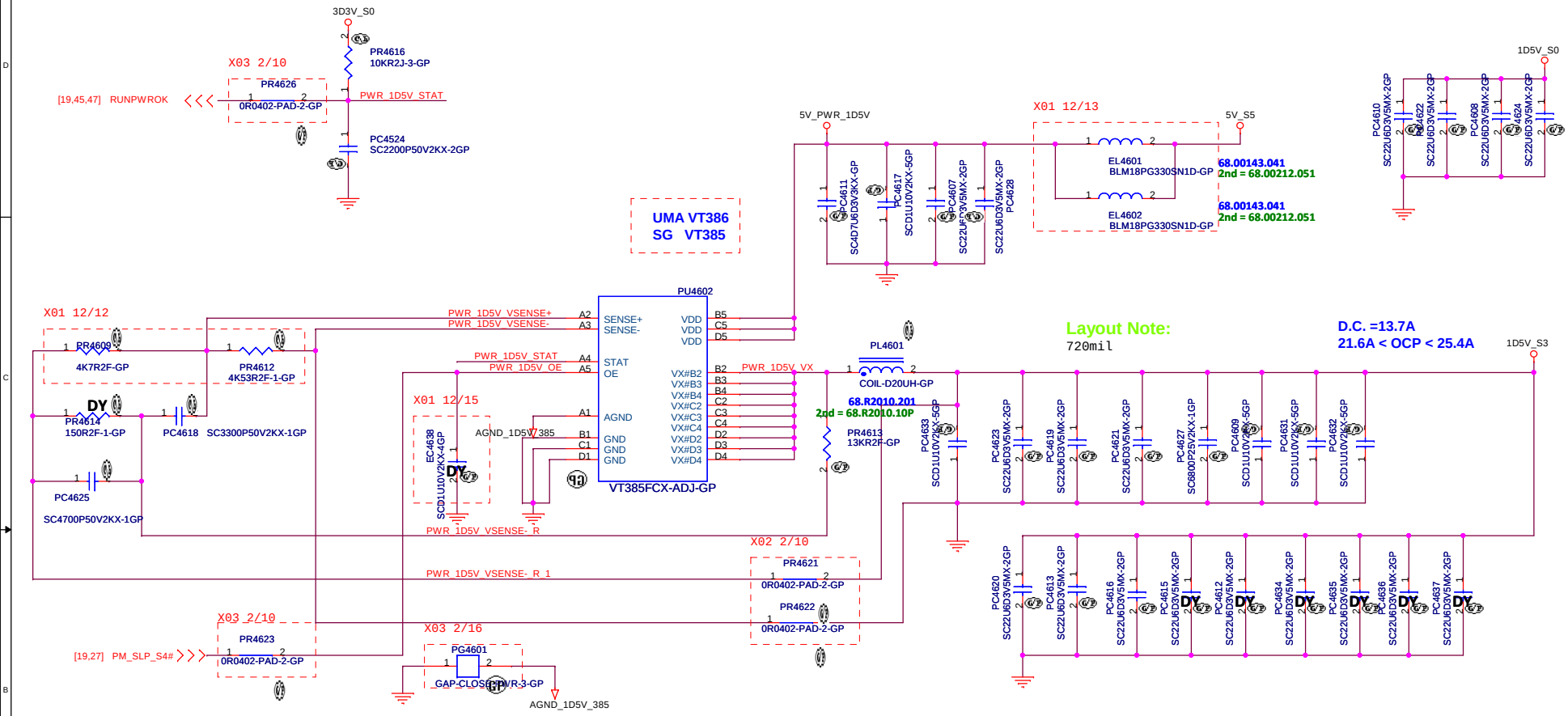
Taipei Hsien 221, Taiwan, R.O.C.

Title: 1D05V_PCH & VCCP_CPU

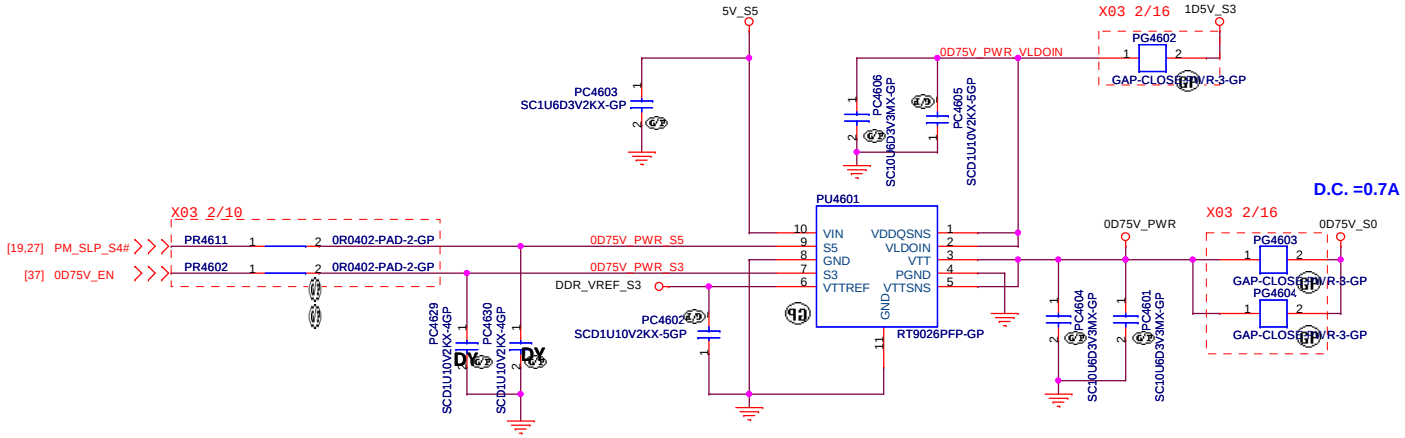
Size	Document Number	Rev
A3	BMW Z4 DIS	A00

Date: Friday, March 30, 2012 Sheet 45 of 105

SSID = PWR.Plane.Regulator_1p5v0p75v



RT9026 for 0D75V_S0



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

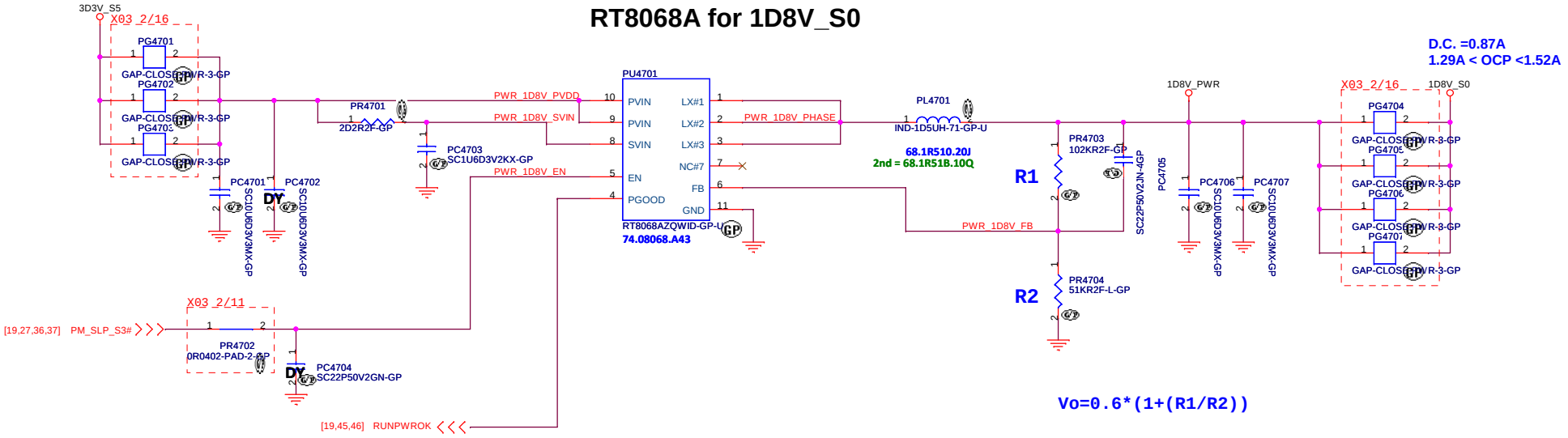
Title: VT385_1D5V_S3/RT9026_0D75V_S0

Size: A3 | Document Number: BMW Z4 DIS | Rev: A00

Date: Friday, March 30, 2012 | Sheet 46 of 105

SSID = PWR.Plane.Regulator_1p8v

RT8068A for 1D8V_S0



D.C. =0.87A
1.29A < OCP <1.52A

Vo=0.6*(1+(R1/R2))

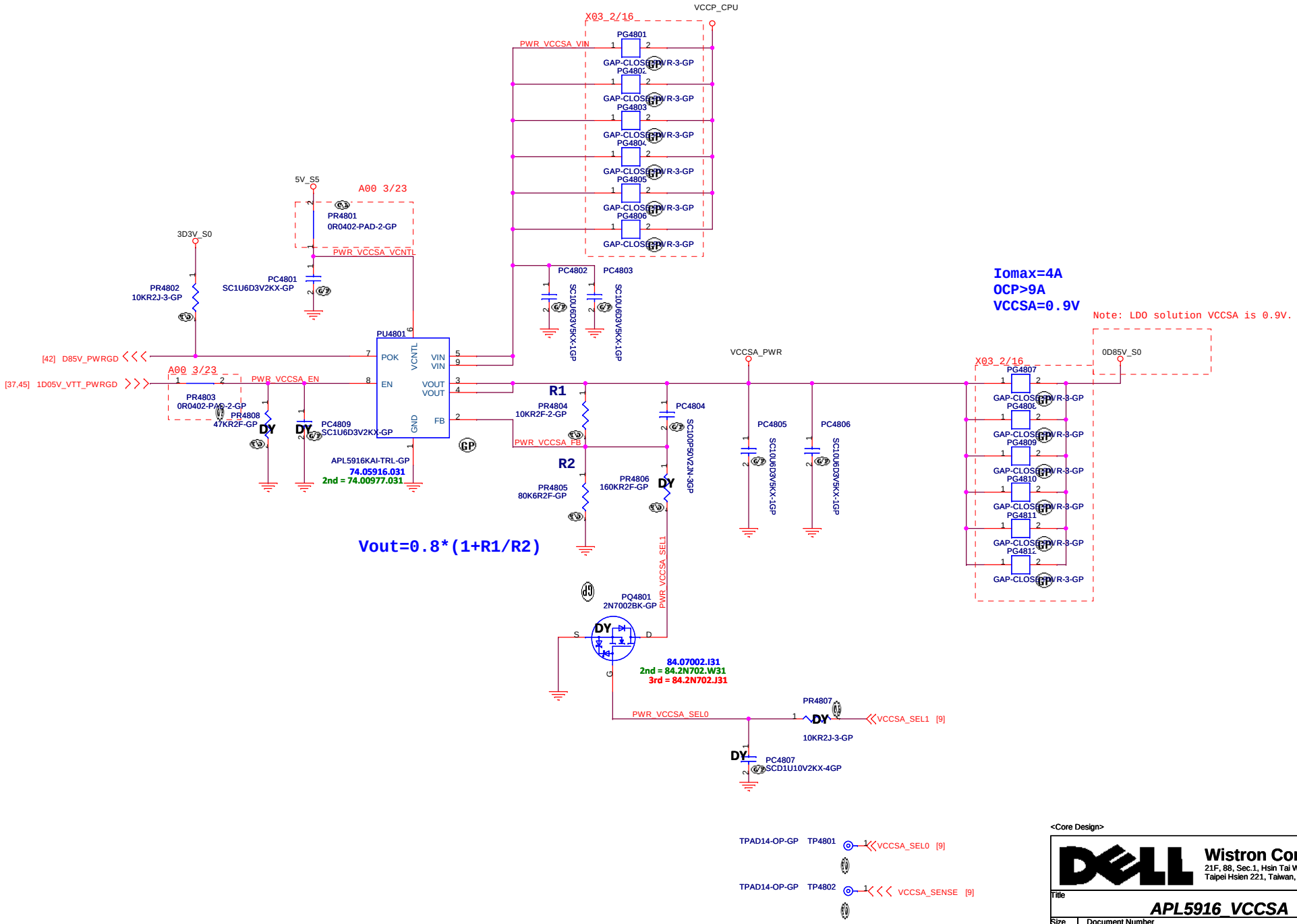
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	RT8068A_1D8V_S0	
Size: A3	Document Number: BMW Z4 DIS	Rev: A00
Date: Friday, March 30, 2012	Sheet 47 of 105	

SSID = PWR.Plane.Regulator_vccsa

X02 1/9



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title	APL5916_VCCSA	
Size A3	Document Number BMW Z4 DIS	Rev A00
Date: Friday, March 30, 2012	Sheet 48 of 105	

SSID = VIDEO

X01 12/20
X01 12/02

LVDS CONN

LCD1
FOX-CON30-GP
20.F2173.030
2nd = 20.F2089.030

DCBATOUT_LCD
X03 2/13
68.00143.041
2nd = 68.00212.051
LCD_POWER
EL4901 BLM18PG330SN1D-GP

R4902 33R2J-2-GP
BLON_OUT_C
LCD_BRIGHTNESS
DBC_EN_C
L_BKLT_CTRL [17]

3D3V_CAMERA_S0
USB_CAMERA#
USB_CAMERA
COLOR_ENGINE_R
AUD_DMIC_CLK [82]
AUD_DMIC_IN0 [82]
LVDSA_CLK [17]
LVDSA_CLK# [17]
LVDSA_DATA2 [17]
LVDSA_DATA2# [17]
LVDSA_DATA1 [17]
LVDSA_DATA1# [17]
LVDSA_DATA0 [17]
LVDSA_DATA0# [17]
LVDS_DDC_DATA_R_1
LVDS_DDC_CLK_R_1
LCD_TST_C
3D3V_LCD_ROM
LCDVDD

C4901 SCD1U10V2KX-5GP DY
C4902 SC1U6D3V2KX-GP

LCD_TST_C
BLON_OUT_C
RN4901 SRN100J-3-GP
LCD_TST [27]
BLON_OUT [27]
R4908 100KR2J-1-GP

3D3V_S0
RN4903 SRN2K2J-1-GP
A00 3/27
LVDS_DDC_DATA_R [17]
LVDS_DDC_CLK_R [17]
RN4902 SRN100J-3-GP

DBC_EN_C
X03 2/6
R4912 0R0402-PAD-GP
DBC_EN [22]
COLOR_ENGINE_R
R4913 0R2J-2-GP DY
COLOR_ENGINE [22]

A00 3/27
X01 12/30
[18] USB_PN12
[18] USB_PP12
TR4902
FILTER-4P-6-GP
69.10103.041
2nd = 68.00201.141
USB_CAMERA#
USB_CAMERA

Camera Power

3D3V_S0
R4904 0R3J-0-U-GP
3D3V_CAMERA_S0
EC4903 SCD1U10V2KX-5GP DY
C4903 SC10U6D3V5KX-1GP

DCBATOUT_LCD
F4901 POLYSW-1D1A24V-GP-U
DCBATOUT
69.50007.A31
2nd = 69.50007.A41
C4904 SC1KP50V2KX-1GP
C4905 SCD1U25V3KX-GP

SSID = VIDEO

LCD Power for ROSA

[17] LVDS_VDD_EN
[27] LCD_TST_EN
D4901 BAT54CPT-GP
83.R2003.E81
2ND = 83.00054.Q81
LCDVDD_EN
R4909 100KR2J-1-GP
LCDVDD
C4908 SC4D7U6D3V3KX-GP
EC4907 SCD1U25V3KX-GP DY

Layout Note:
Trace width = 80mil

U4901 G5285T11U-GP
EN
GND
OUT
IN#5
IN#4
3D3V_S0
C4907 SC4D7U6D3V3KX-GP
74.05285.07F
2nd = 74.09724.09F

3D3V_S0
R4901 0R3J-0-U-GP
F4902 FUSE-2A32V-16-GP DY
3D3V_LCD_ROM

X03 2/16
LVDSA_CLK
LVDSA_CLK#
LVDSA_DATA0
LVDSA_DATA0#
LVDSA_DATA1
LVDSA_DATA1#
LVDSA_DATA2
LVDSA_DATA2#
COLOR_ENGINE_R
EC4901 EC4902 EC4904 EC4905 EC4906 EC4908 EC4909 EC4910 EC4911
SC3D3P50V2CN-GP

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LCD Connector	
Size A3	Document Number BMW Z4 DIS	Rev A00
Date: Tuesday, April 03, 2012	Sheet 49 of 105	

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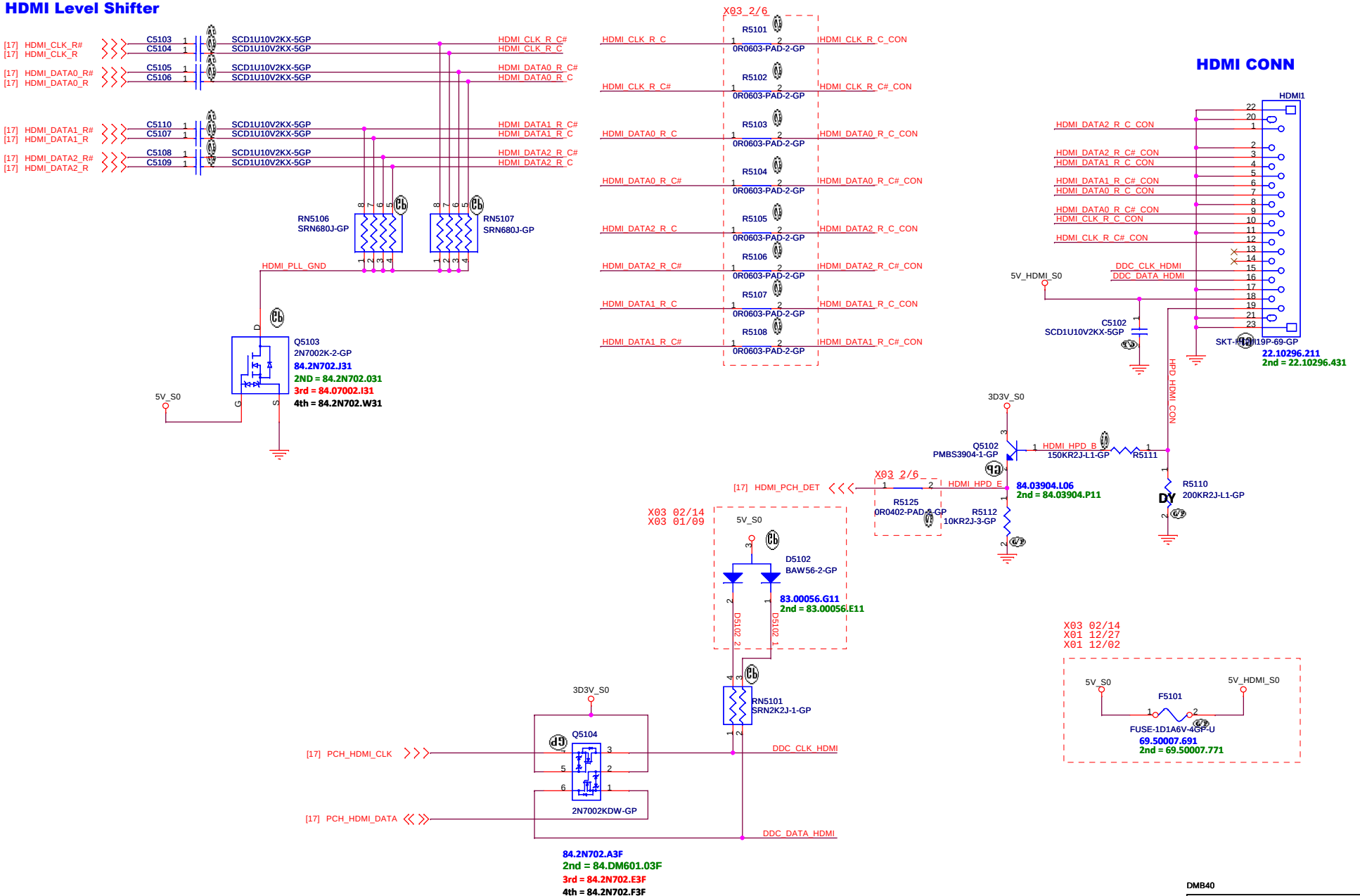
DMB40

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***CRT Connector***	
Size: A3	Document Number: ***BMW Z4 DIS***	Rev: ***A00***
Date: Friday, March 30, 2012	Sheet 50 of 105	

SSID = VIDEO

HDMI Level Shifter



HDMI CONN

DMB40

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *HDMI Level Shifter/Connector*		
Size: A3	Document Number: *BMW Z4 DIS*	Rev: *A00*
Date: Friday, March 30, 2012	Sheet 51 of 105	

(Blanking)

DMB40

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*BMW Z4 DIS*	*A00*

Date: Friday, March 30, 2012 Sheet 52 of 105

(Blanking)

DMB40

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*BMW Z4 DIS*	*A00*

Date: Friday, March 30, 2012 Sheet 53 of 105

(Blanking)

DMB40

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *BMW Z4 DIS* | Rev: *A00*

Date: Friday, March 30, 2012 | Sheet 54 of 105

(Blanking)

DMB40

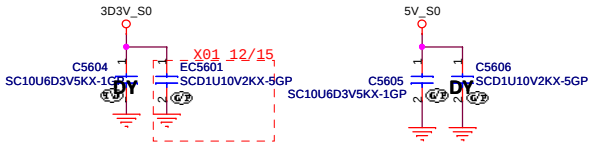
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ITP/Fan Connector

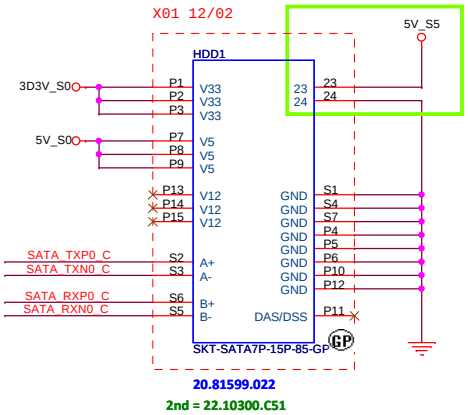
Size	Document Number	Rev
A3	BMW Z4 DIS	A00

Date: Friday, March 30, 2012 Sheet 55 of 105

SSID = SATA

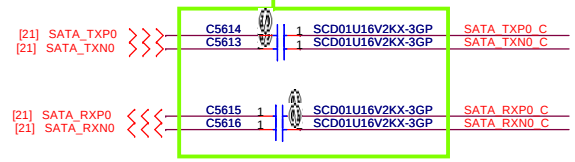


HDD CONN

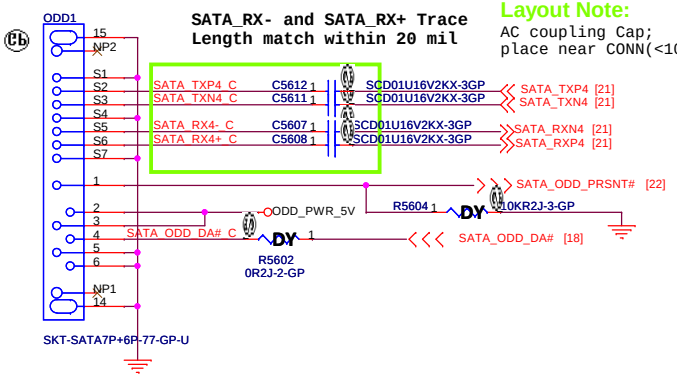


Due to layout, HDD1 pin 23 modify 5V_S5

Layout Note:
AC coupling Cap;
place near CONN(<100mils)

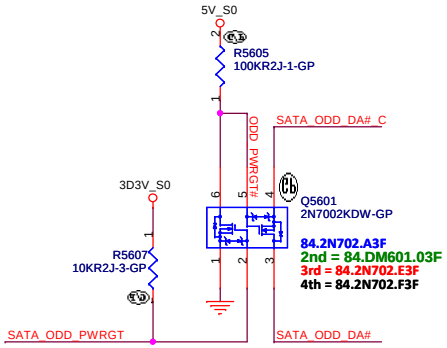


ODD CONN

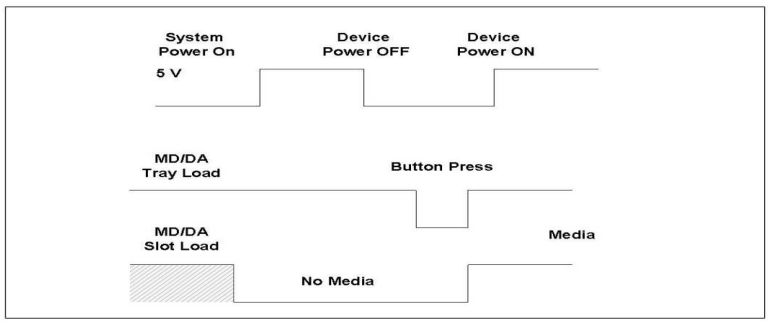


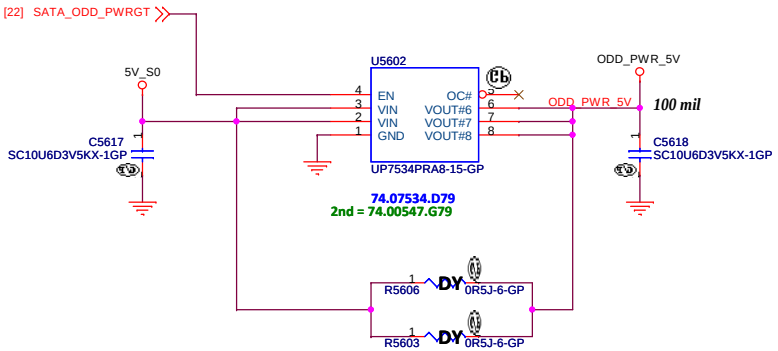
Layout Note:
AC coupling Cap;
place near CONN(<100mils)

2nd = 20.81152.013



Zero Power ODD Power Sequence





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Title: *Reserved*

Size	Document Number	Rev
A3	*BMW Z4 DIS*	*A00*

Date: Friday, March 30, 2012 Sheet 57 of 105

(Blanking)

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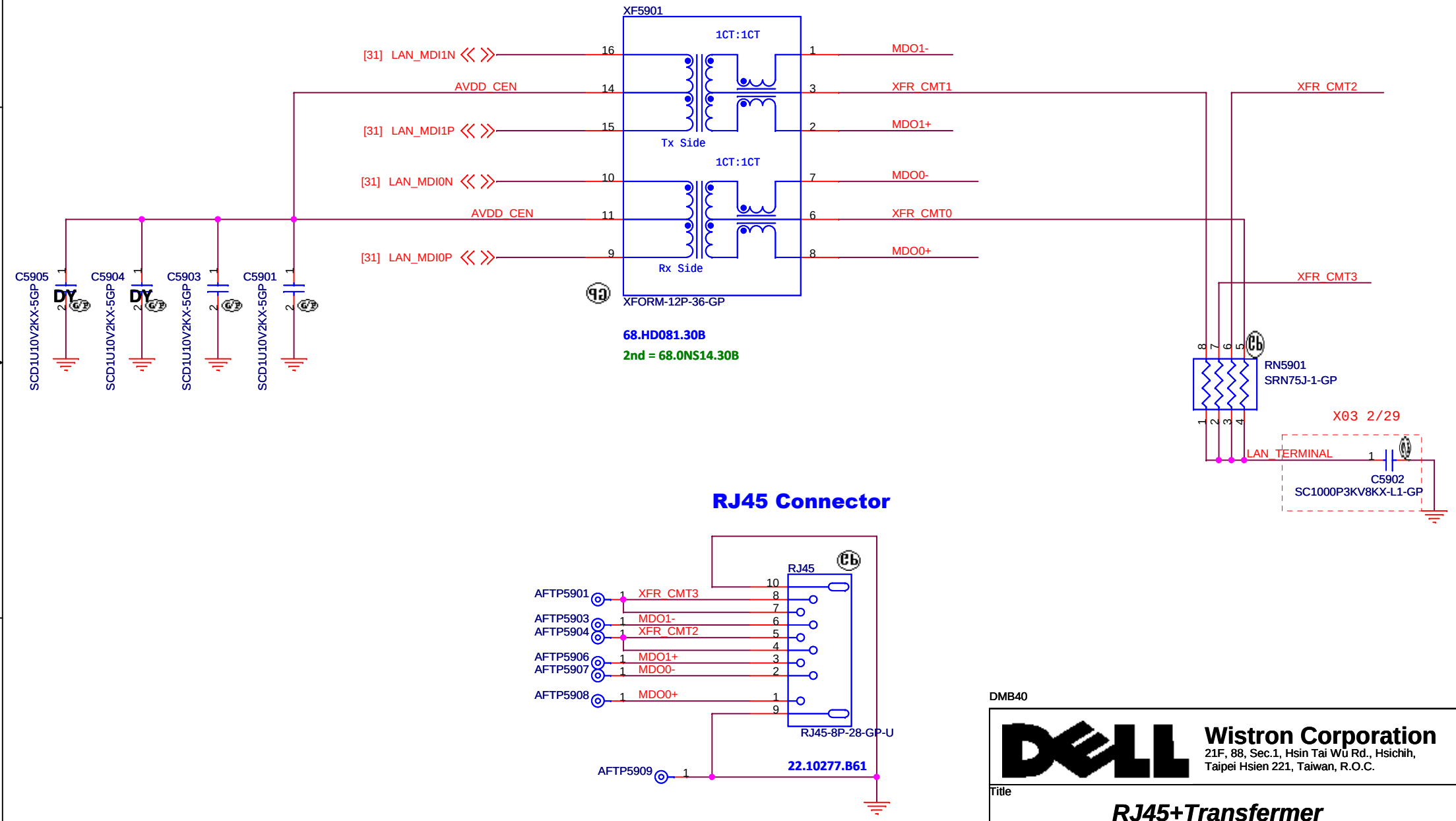
Title: *Reserved*

Size: A3 | Document Number: *BMW Z4 DIS* | Rev: *A00*

Date: Friday, March 30, 2012 | Sheet 58 of 105

SSID = LOM



RJ45 Connector

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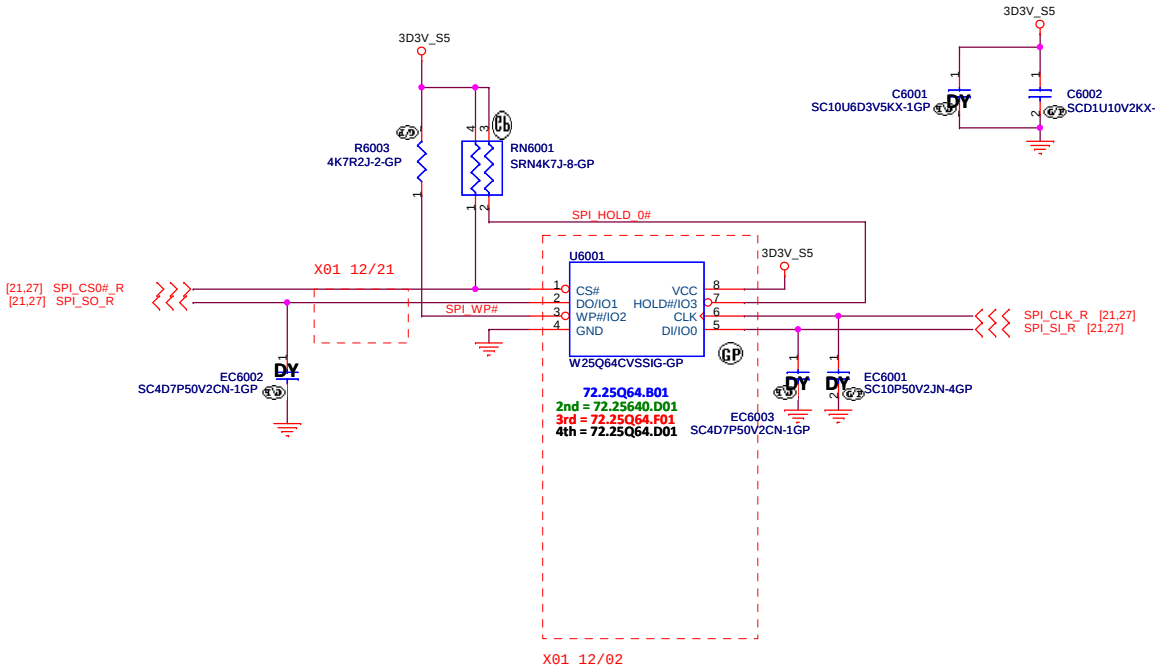
Title: ***RJ45+Transfermer***

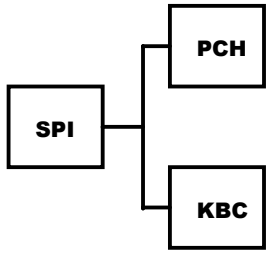
Size	Document Number	Rev
A4	***BMW Z4 DIS***	***A00***

Date: Tuesday, April 03, 2012 Sheet 59 of 105

SSID = Flash.ROM

SPI Flash ROM(8M) for PCH

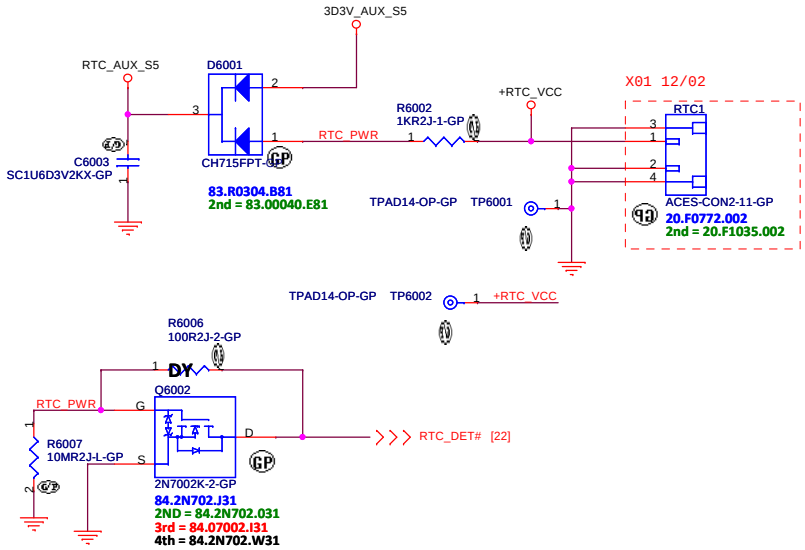




Layout Note:

```
KBC----10"----PCH
KBC----1.5"~6.5"----SPI
PCH----0.5"~6.5"----SPI
```

SSID = RBATT



<Core Design>

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Title: Flash/RTC		
Size: A3	Document Number: BMW Z4 DIS	Rev: A00
Date: Friday, March 30, 2012	Sheet 60 of 105	

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Title: *Reserved*

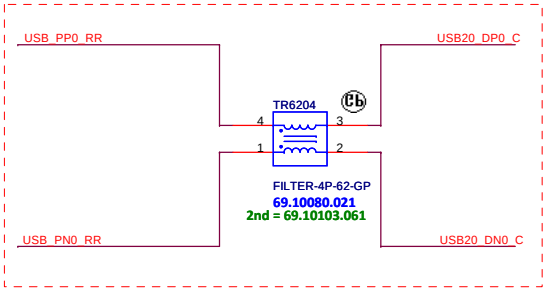
Size | Document Number: *BMW Z4 DIS* | Rev: *A00*

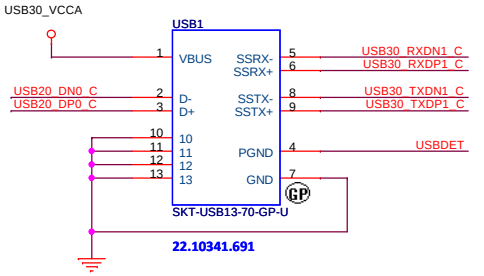
Date: Friday, March 30, 2012 | Sheet 61 of 105

SSID = USB

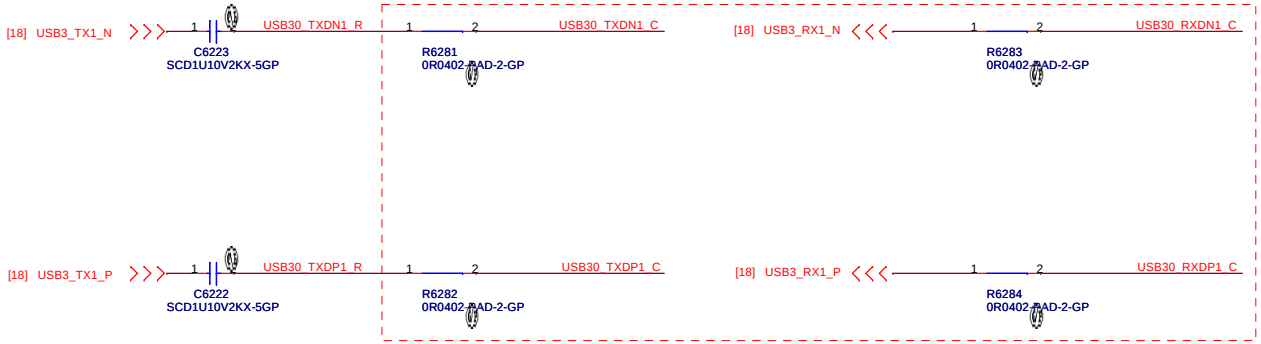
USB3.0 Port1 with power share

A00 3/27
X01 12/23

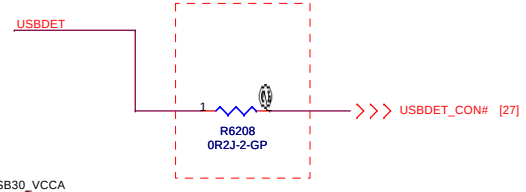


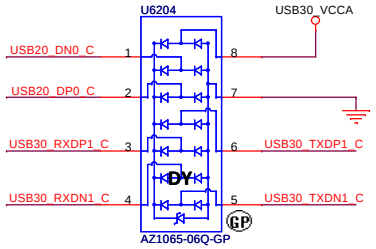


A00 3/23

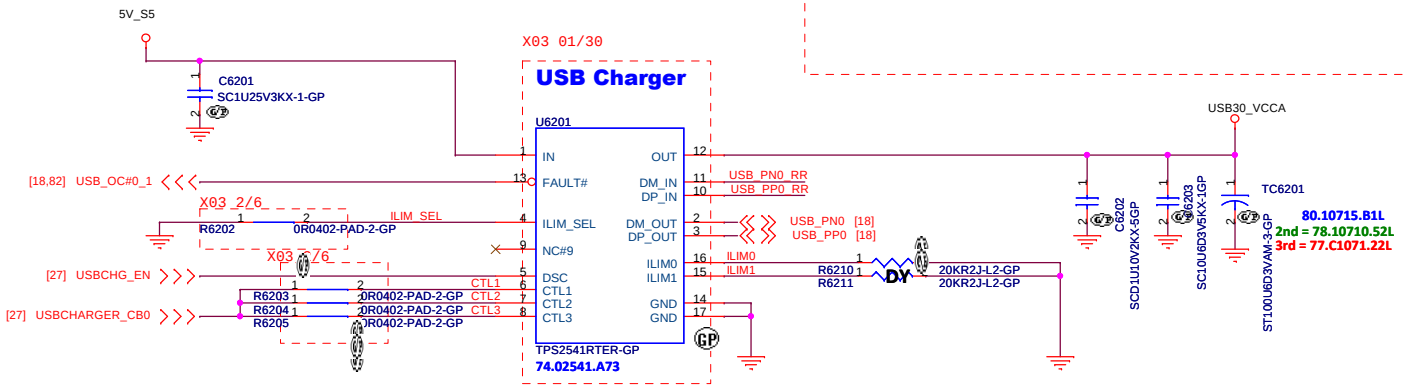


X01 12/15
X01 12/02





X01 12/13



TPS2541 charging type setting			
	CTL1	CTL2	CTL3
CDP	1	1	1
DCP	0	0	X

<Core Design>

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Title		
USB 3.0		
Size: A3	Document Number: BMW Z4 DIS	Rev: A00
Date: Friday, March 30, 2012	Sheet 62 of 105	

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Title

(Reserved)

Size	Document Number	Rev
A3	***BMW Z4 DIS***	***A00***

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Title: *Finger Printer*

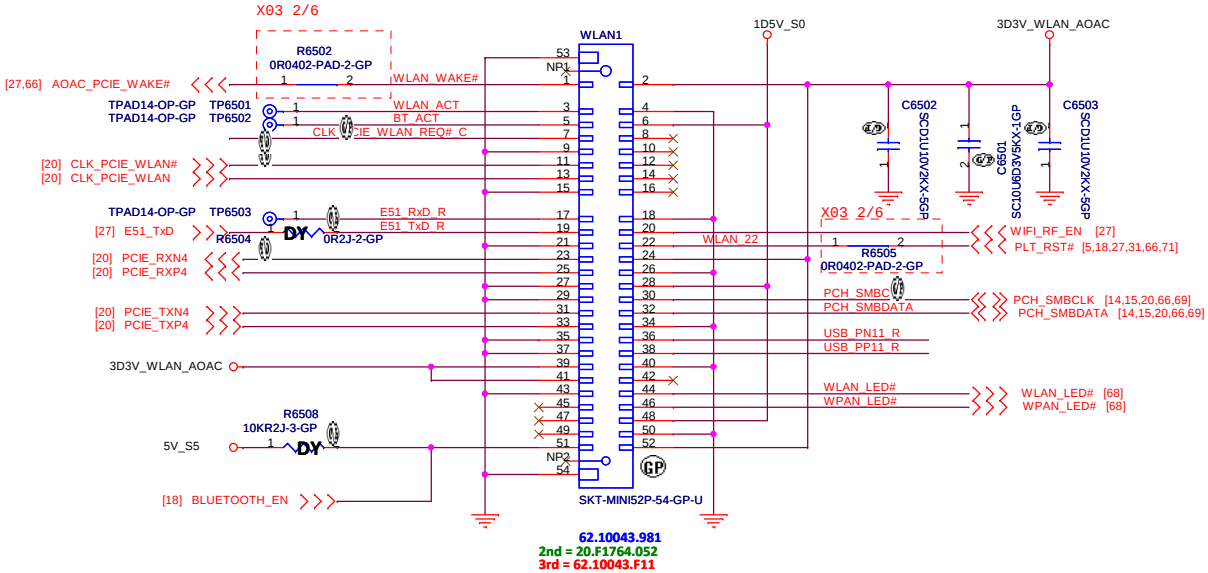
Size: A3 | Document Number: *BMW Z4 DIS* | Rev: *A00*

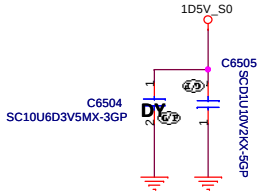
Date: Friday, March 30, 2012 | Sheet 64 of 105

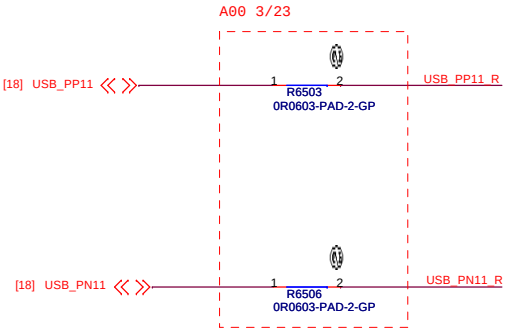
SSID = Wireless

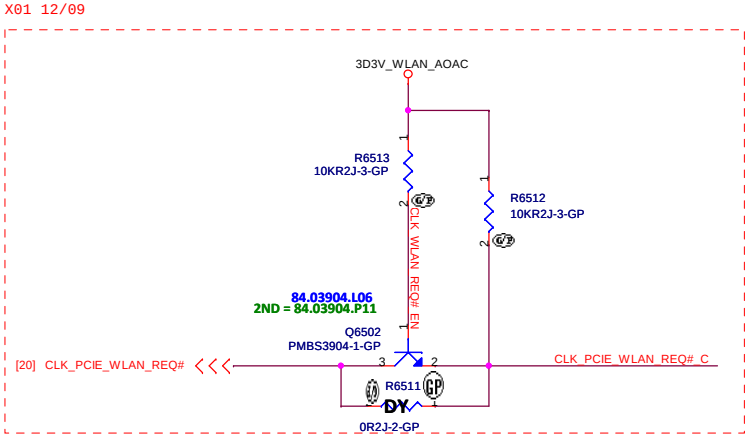
Mini Card Connector(802.11a/b/g/n)

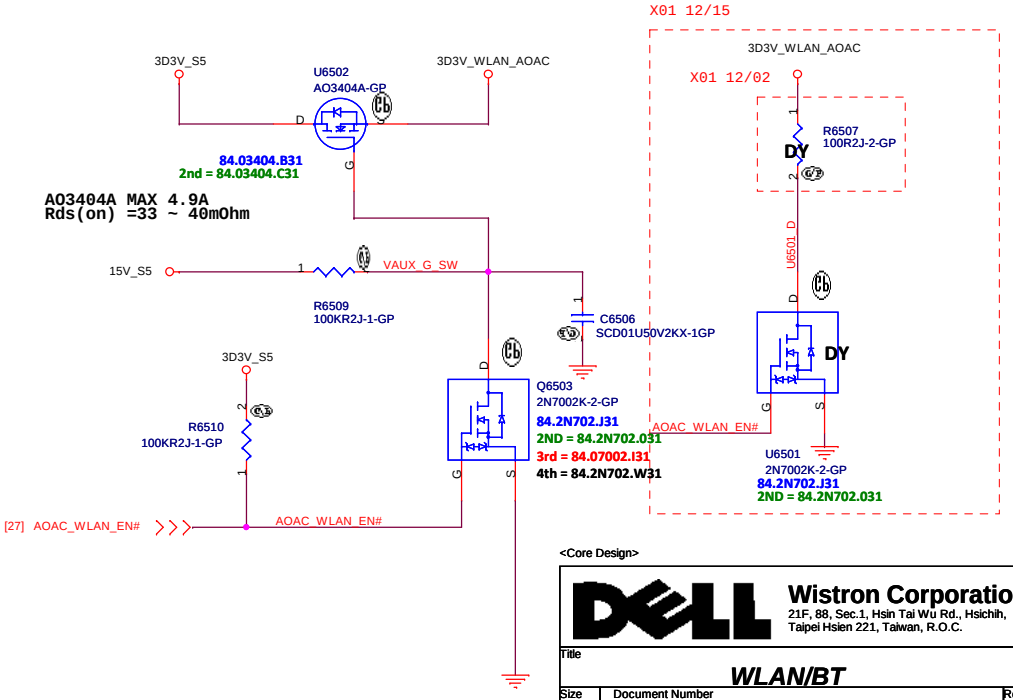
WLAN CONN











<Core Design>

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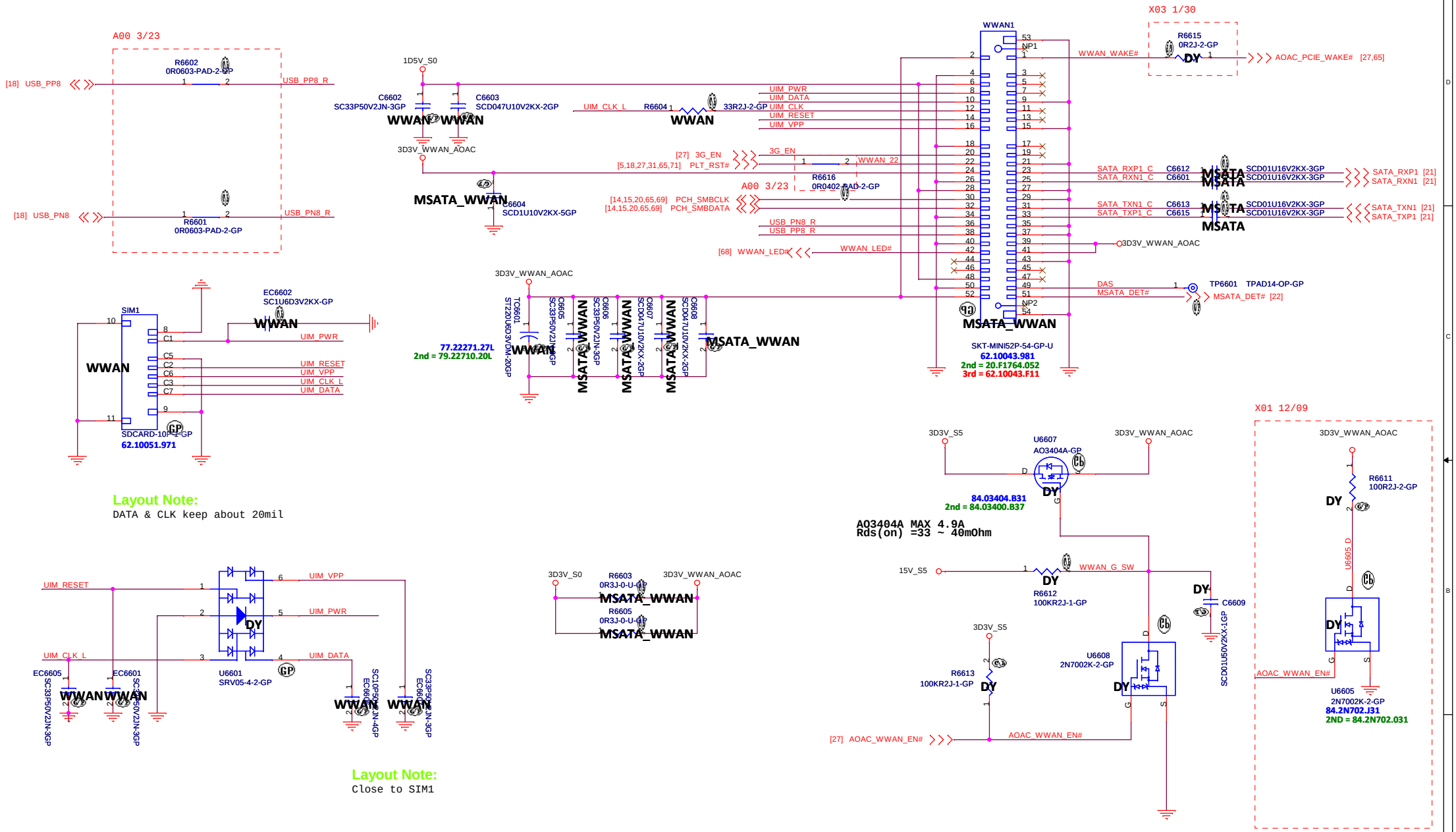
Title	WLAN/BT	
Size A3	Document Number BMW Z4 DIS	Rev A00
Date: Friday, March 30, 2012	Sheet 65 of 105	

SSID = Wireless

WWAN CONN



Layout Note:
DATA & CLK keep about 20mil

Layout Note:
Close to SIM1

AO3404A MAX 4.9A
Rds(on) =33 ~ 40mOhm

<Core Design>

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Title	WWAN/MSATA	
Size: A3	Document Number: BMW Z4 DIS	Rev: A00
Date: Friday, March 30, 2012	Sheet 66 of 105	

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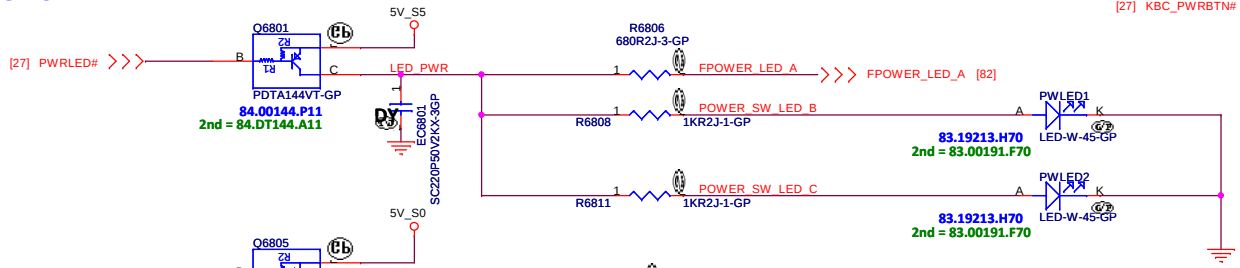
Title

Reserved

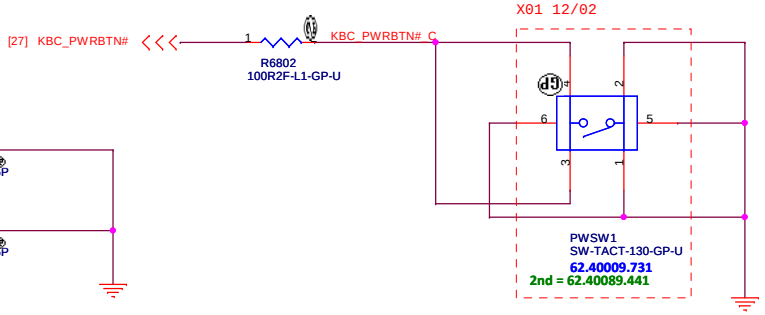
Size	Document Number	Rev
A3	***BMW Z4 DIS***	***A00***

SSID = User.Interface

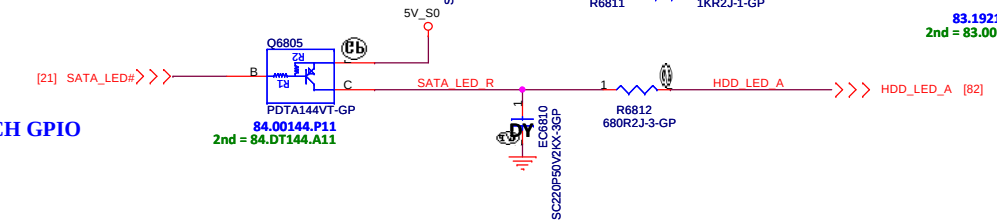
Front Power LED
LOW actived from KBC GPIO



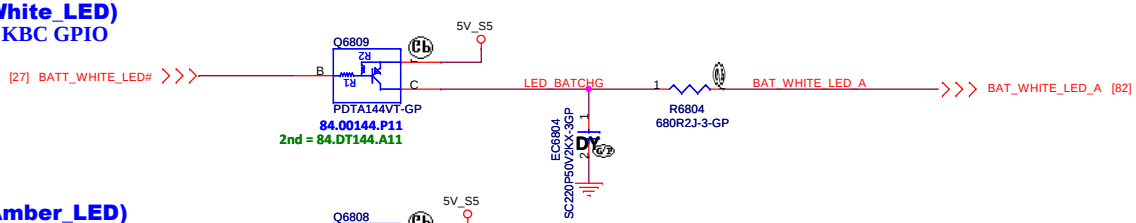
PWRBTN



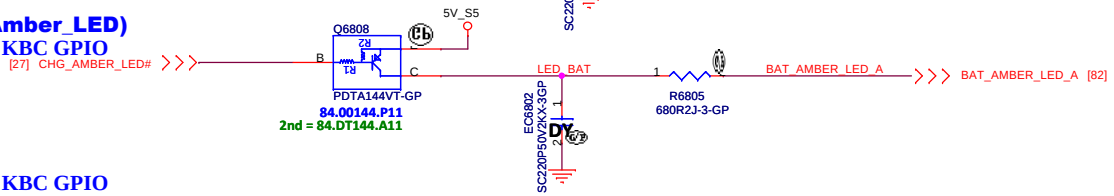
SATA HDD LED
LOW actived from PCH GPIO



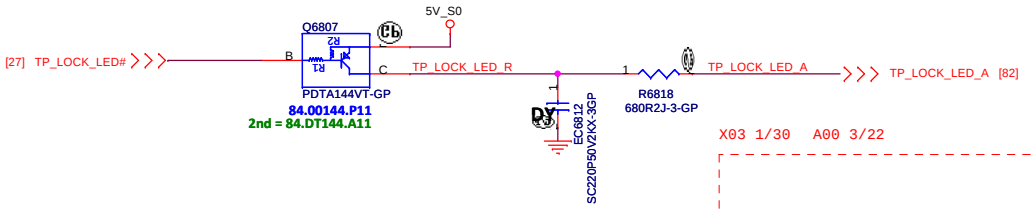
Battery LED2(White_LED)
LOW actived from KBC GPIO



Battery LED1(Amber_LED)
LOW actived from KBC GPIO



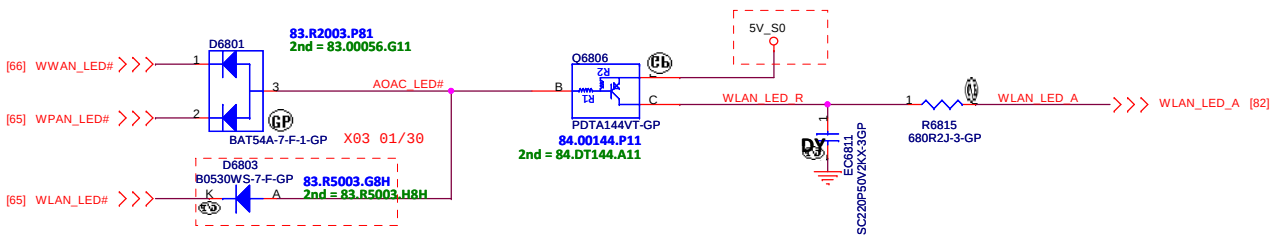
TPLOCK LED
LOW actived from KBC GPIO



X01 12/02 X01 12/15 A00 3/22

X03 1/30 A00 3/22

WLAN LED
LOW actived from KBC GPIO



<Core Design>

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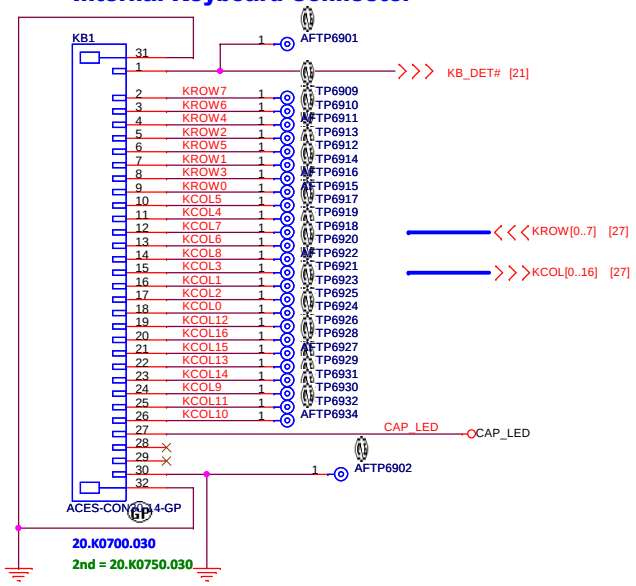
Title: LED Bar/Power Button

Size	Document Number	Rev
A3	BMW Z4 DIS	A00

Date: Friday, March 30, 2012 Sheet 68 of 105

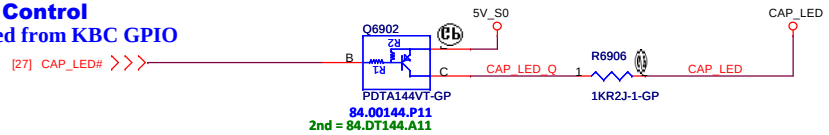
SSID = KBC

Internal Keyboard Connector



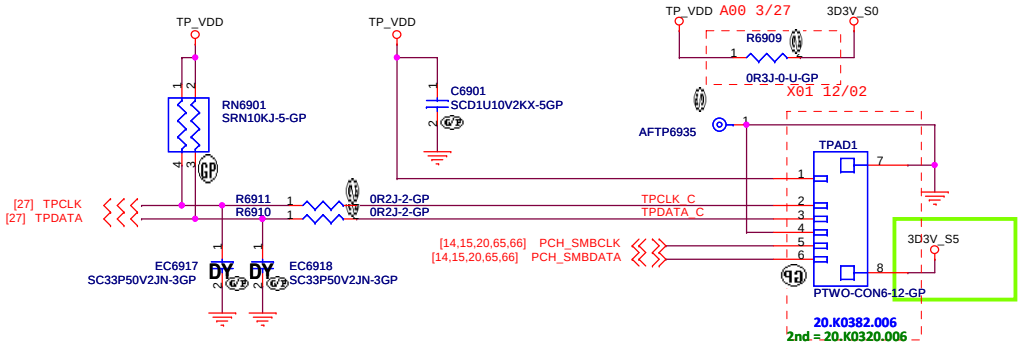
CAP LED Control

LOW actived from KBC GPIO

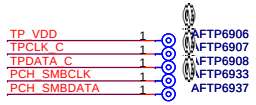


SSID = Touch.Pad

Touch Pad Connector



Due to layout, TPAD1 pin 8 modify to 3D3V_S5



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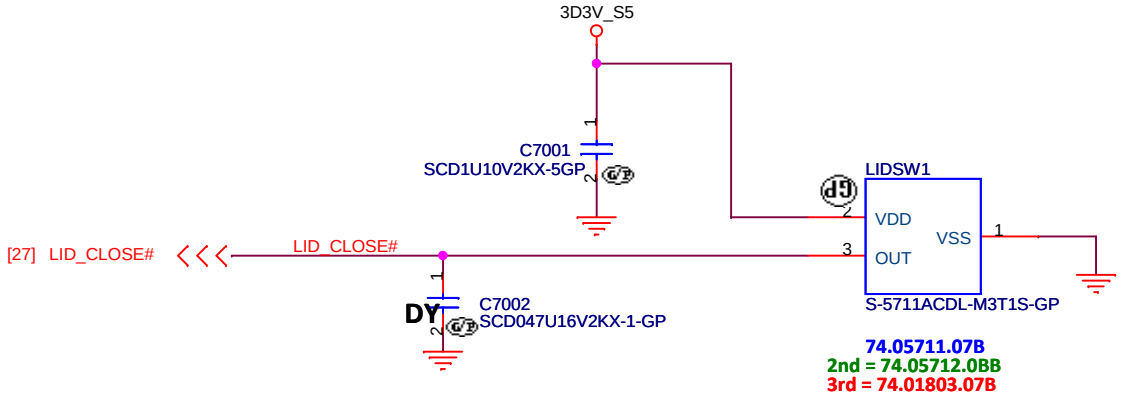
Title	Key Board/Touch Pad	
Size A3	Document Number BMW Z4 DIS	Rev A00
Date: Friday, March 30, 2012	Sheet 69 of 105	

SSID = User.Interface



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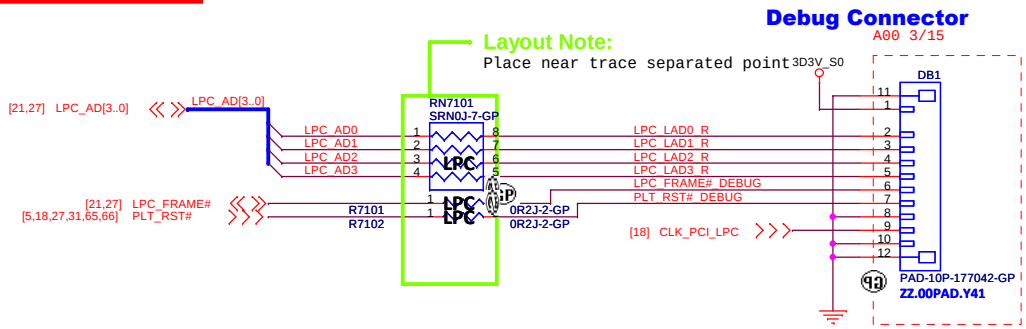
Title: ***Hall Sensor***

Size	Document Number	Rev
A4	***BMW Z4 DIS***	***A00***

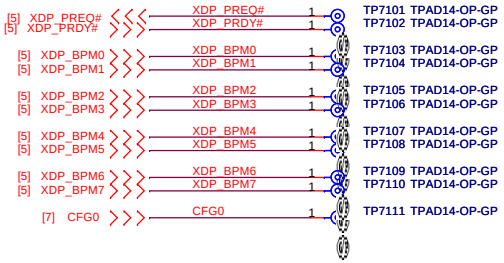
Date: Friday, March 30, 2012 Sheet 70 of 105

SSID = DEBUG PORT



SSID = CPU

CPU XDP



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Title: *Dubug connector*

Size	Document Number	Rev
A3	*BMW Z4 DIS*	*A00*

Date: Friday, March 30, 2012 Sheet 71 of 105

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Title: *Reserved*

Size	Document Number	Rev
A3	*BMW Z4 DIS*	*A00*

Date: Friday, March 30, 2012 Sheet 72 of 105

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Title: *Reserved*

Size	Document Number	Rev
A3	*BMW Z4 DIS*	*A00*

Date: Friday, March 30, 2012 Sheet 73 of 105

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Title: *Reserved*

Size: A3 | Document Number: *BMW Z4 DIS* | Rev: *A00*

Date: Friday, March 30, 2012 | Sheet 74 of 105

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Title: *(Reserved)*

Size	Document Number	Rev
A3	*BMW Z4 DIS*	*A00*

Date: Friday, March 30, 2012 Sheet 75 of 105

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Title: *Reserved*

Size	Document Number	Rev
A3	*BMW Z4 DIS*	*A00*

Date: Friday, March 30, 2012 Sheet 76 of 105

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Title: *Reserved*

Size	Document Number	Rev
A3	*BMW Z4 DIS*	*A00*

Date: Friday, March 30, 2012 Sheet 77 of 105

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Title: *Reserved*

Size	Document Number	Rev
A3	*BMW Z4 DIS*	*A00*

Date: Friday, March 30, 2012 Sheet 78 of 105

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: *Reserved*

Size: A3 | Document Number: *BMW Z4 DIS* | Rev: *A00*

Date: Friday, March 30, 2012 | Sheet 79 of 105

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Title: *Reserved*

Size	Document Number	Rev
A3	*BMW Z4 DIS*	*A00*

Date: Friday, March 30, 2012 Sheet 80 of 105

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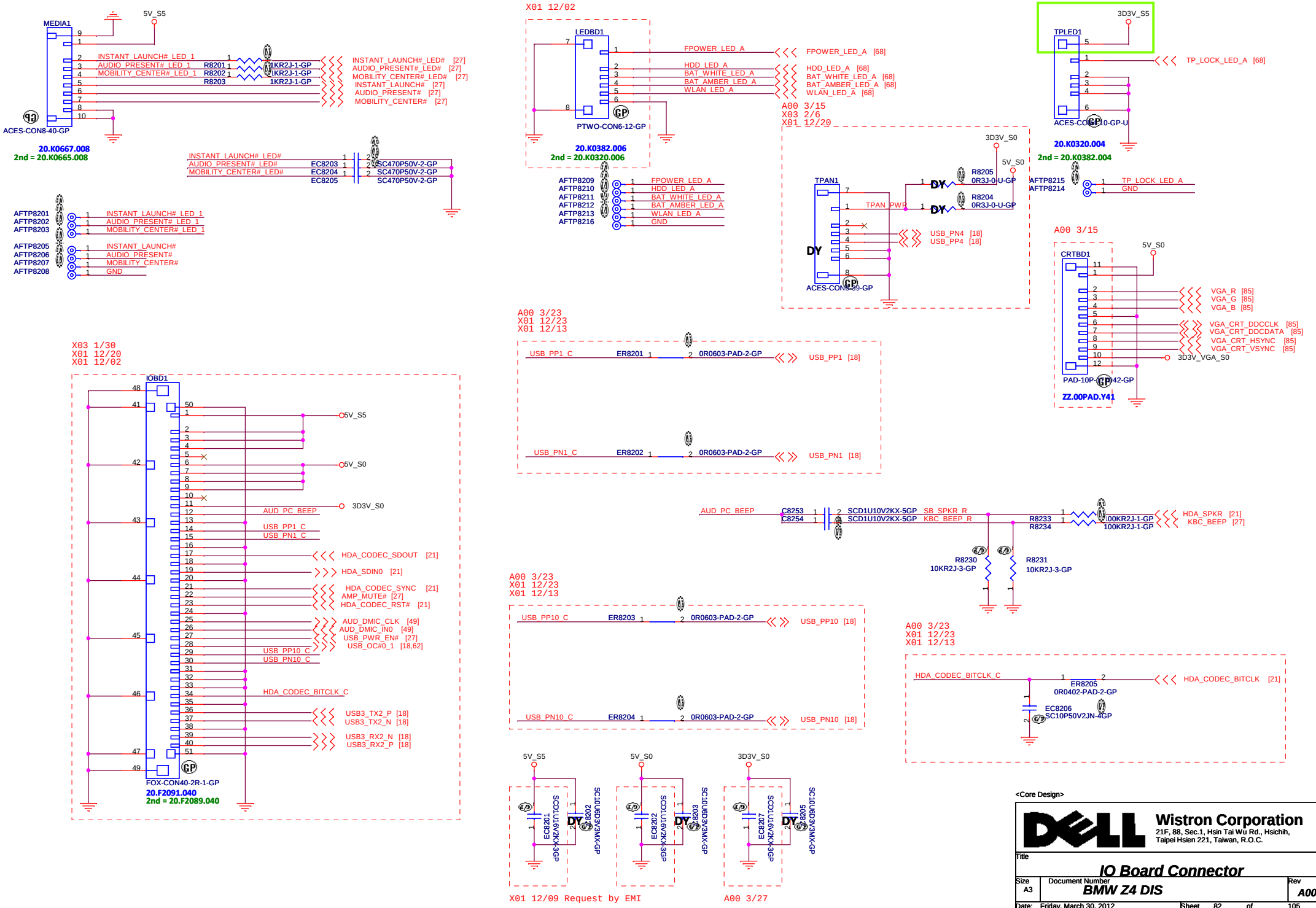
Title: *Reserved*

Size	Document Number	Rev
A3	*BMW Z4 DIS*	*A00*

Date: Friday, March 30, 2012 Sheet 81 of 105

SSID = User.Interface

Due to layout, TPLED1 pin 5 modify 3D3V_S5



<Core Design>

Wistron Corporation
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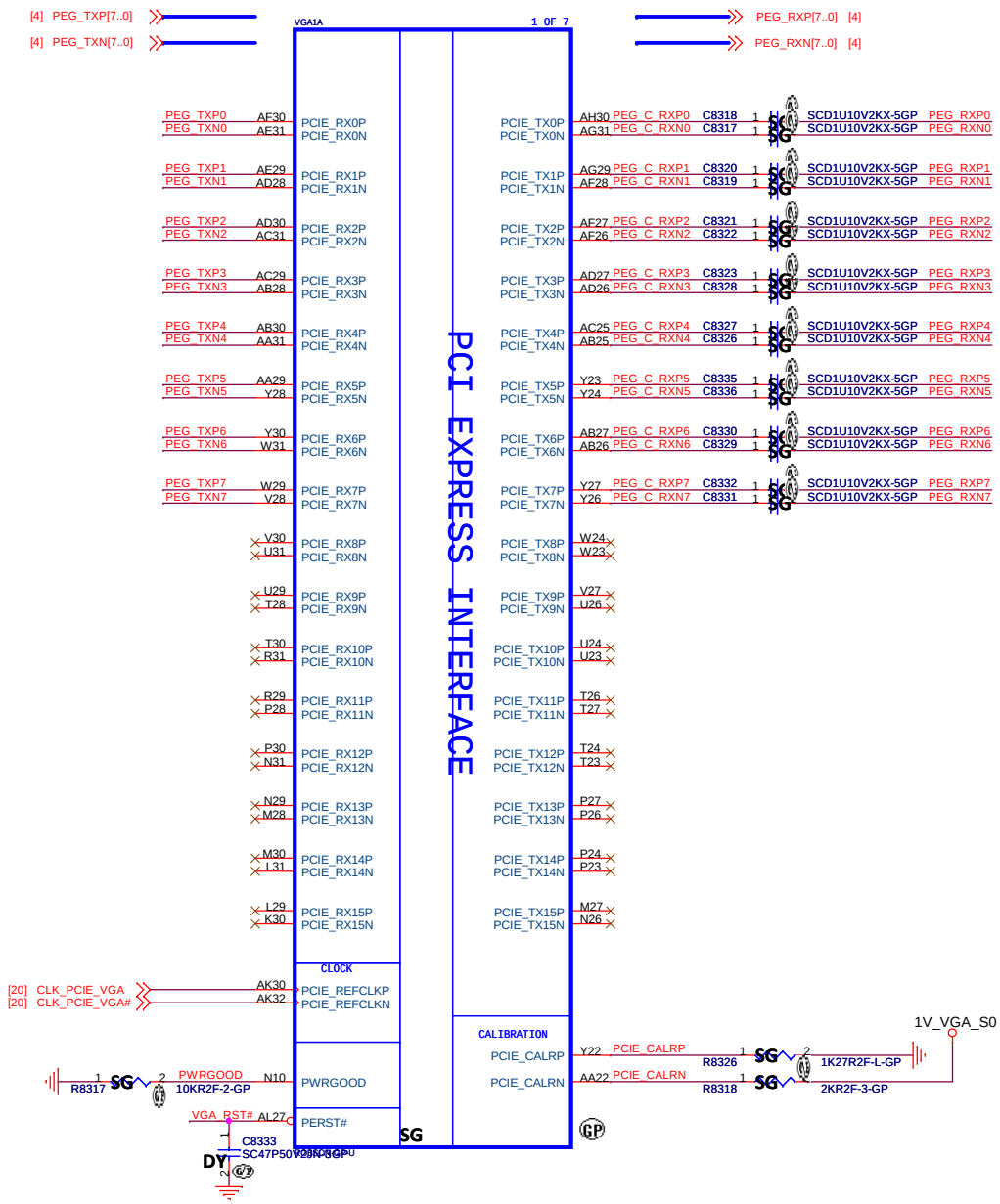
Title: IO Board Connector

Size	Document Number	Rev
A3	BMW Z4 DIS	A00

Date: Friday, March 30, 2012 Sheet 82 of 105

SSID = VIDEO



X01 12/15

[22] DGPU_HOLD_RST# X03 2/6 R8322 0R0402-PAD-2-GP VGA_RST# [85]

<Core Design>

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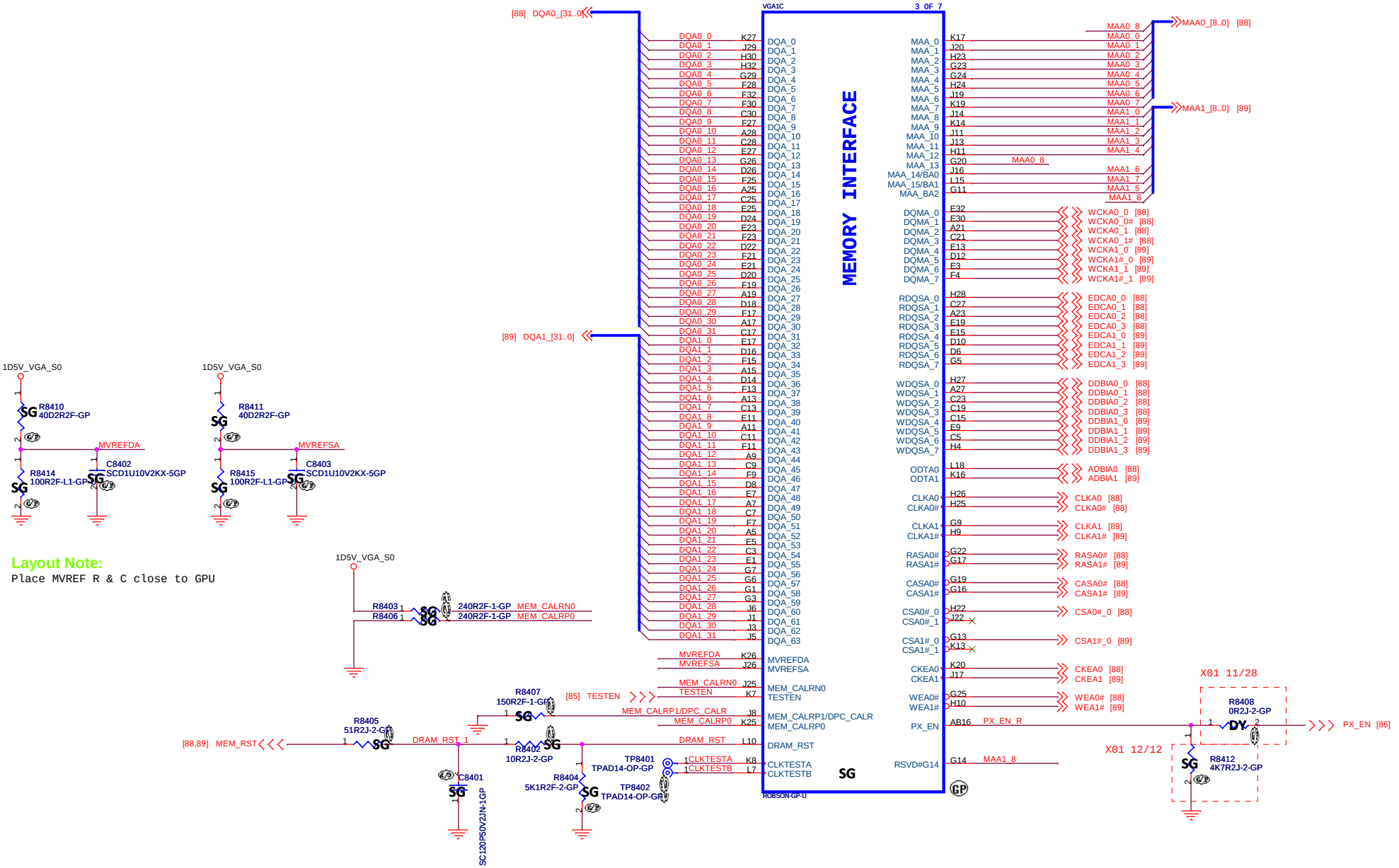
Taipei Hsien 221, Taiwan, R.O.C.

Title	GPU PEG/STRAPPING(1/5)	
Size A3	Document Number BMW Z4 DIS	Rev A00
Date: Friday, March 30, 2012	Sheet 83 of 105	

SSID = VIDEO



Layout Note:
Place MVREF R & C close to GPU

Layout Note:
Place all these components very close to GPU
(Within 25mm) and keep all component close
to each Other (within 5mm) except R_MEM_2

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Title: *GPU Memory(2/5)*

Size	Document Number	Rev
A3	*BMW Z4 DIS*	*A00*

Date: Friday, March 30, 2012 Sheet 84 of 105

SSID = VIDEO

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 1K RESISTOR
X = DESIGN DEPENDENANT
NA = NOT APPLICABLE

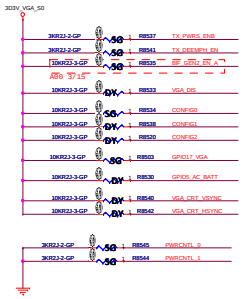
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMEND	PLATFORM SETTING
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	X	1
BIF_GEN2_EN_A	GPIO2	0:Advertises the PCIe device as 2.5GT/s capable at power on. 1:Advertises the PCIe device as 5.0GT/s capable at power on.	0	0
GPIO5_AC_BATT	GPIO5	optional input allow the system to request a fast power reduction by setting GPIO5 to low.	?	0
GPIO8_ROMSO	GPIO8	RESERVED	0	0
VGA_DIS	GPIO9	0:VGA Controller capacity enabled 1:The device won't be recognized as the system's VGA controller	0	0
ROMIDCFG[2:0]	GPIO[13:11]	BIOS_ROM_EN=1, Config[2:0] defines the ROM type BIOS_ROM_EN=0, Config[2:0] defines the primary memory aperture size	x x x	0 0 1 (256MB)
GPIO21_BB_EN	GPIO21	RESERVED	0	0
BIOS_ROM_EN	GPIO_22_ROMCSB	0:Disable external BIOS ROM device 1:Enable external BIOS ROM device	x	0
VIP_DEVICE_STRAP_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver that it sense whether or not a VIP device is connected on the VIP Host interface.	x	0
RSVD	H2SYNC	RESERVED	0	0
RSVD	GENERICC	RESERVED	0	0
AUD[1]	HSYNC	AUD[1:0]:11-Audio for both DisplayPort and HDMI	X	1
AUD[0]	VSYNC		X	1

MEMORY ID Table

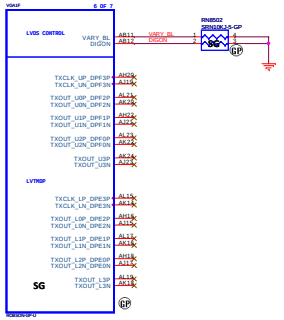
DVPDATA[3:0]	Description
0011	GDDR5 1.25GHZ Hynix-H5GQ2H24AFR-T2C 128M*16
0001	GDDR5 1.25GHZ Hynix-H5GQ2H24MFR-T2C 128M*16
0000	GDDR5 1.25GHZ SAMSUNG-K4G20325FD-FC04 128M*16

DVPDATA[0:3] Default:Pull down

Straps Pin



LVDS Interface



100 MHz Spread Selection Table

S1	S0	Down Spread%
L	L	OFF
L	M	-0.5
L	H	-2.5
M	L	-0.25
M	M	-0.75
M	H	-1.0
H	L	-1.5
H	M	-2.0
H	H	-3.0

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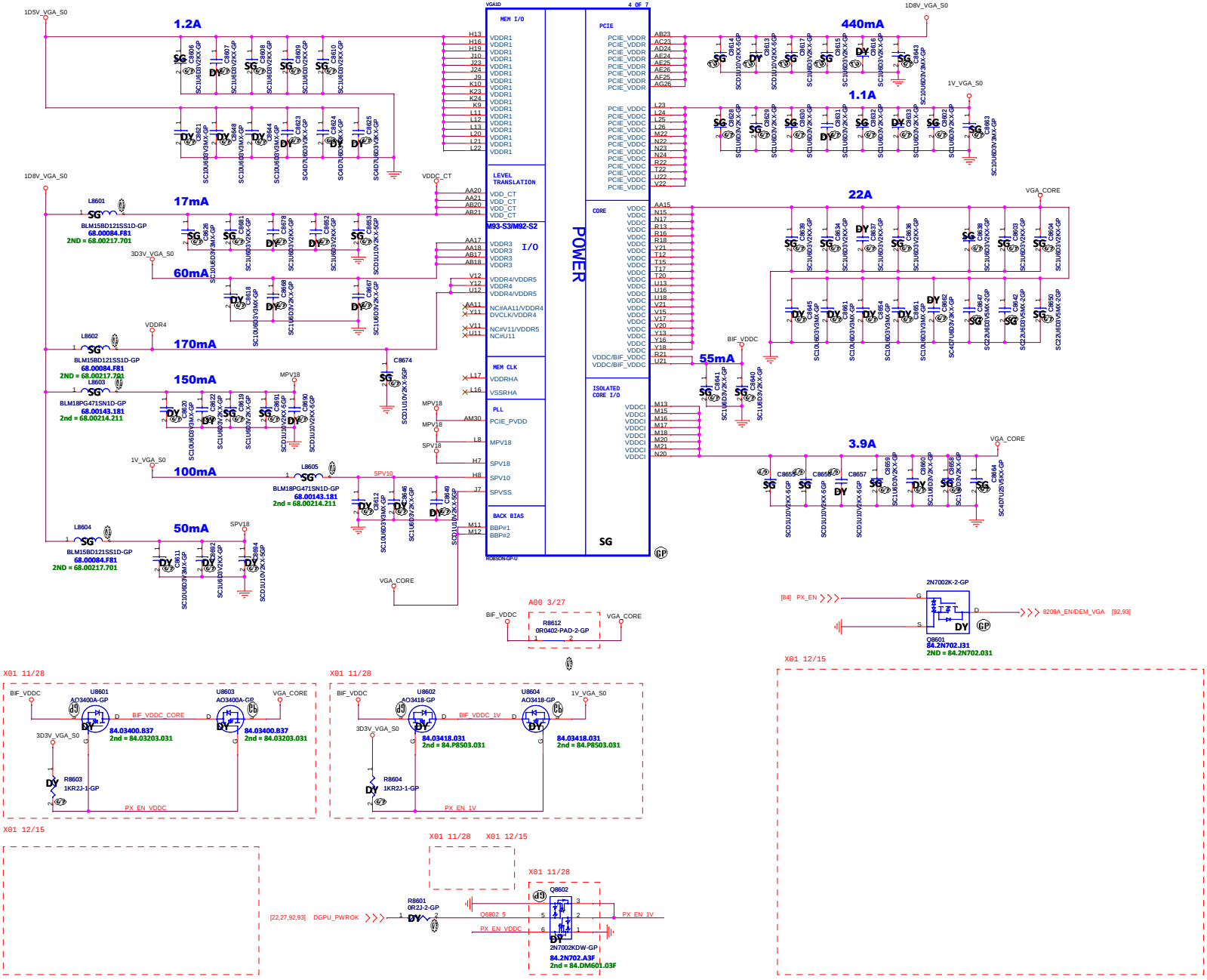
GPU_DP/LVDS/CRT/GPIO(3/5)

Size: A1 | Document Number: BMW Z4 DIS | Rev: A00

Date: Friday, March 30, 2012 | Sheet: 85 of 105

SSID = VIDEO



PX4.0

Mode	PX_EN	PX_EN_1V	PX_EN_VDDC	BIF_VDDC
DIS	Low	Low	High	VGA_CORE
BACO	High	High	Low	1V_VGA_S0

PX4.0

POP	Q8601, Q8602, R8601, U8601, U8602, U8603 U8604, R8603, R8604, R8408
DY	R8612

PX5.0

POP	R8612
DY	Q8601, Q8602, R8601, U8601, U8602, U8603 U8604, R8603, R8604, R8605, R8408

<Core Design>

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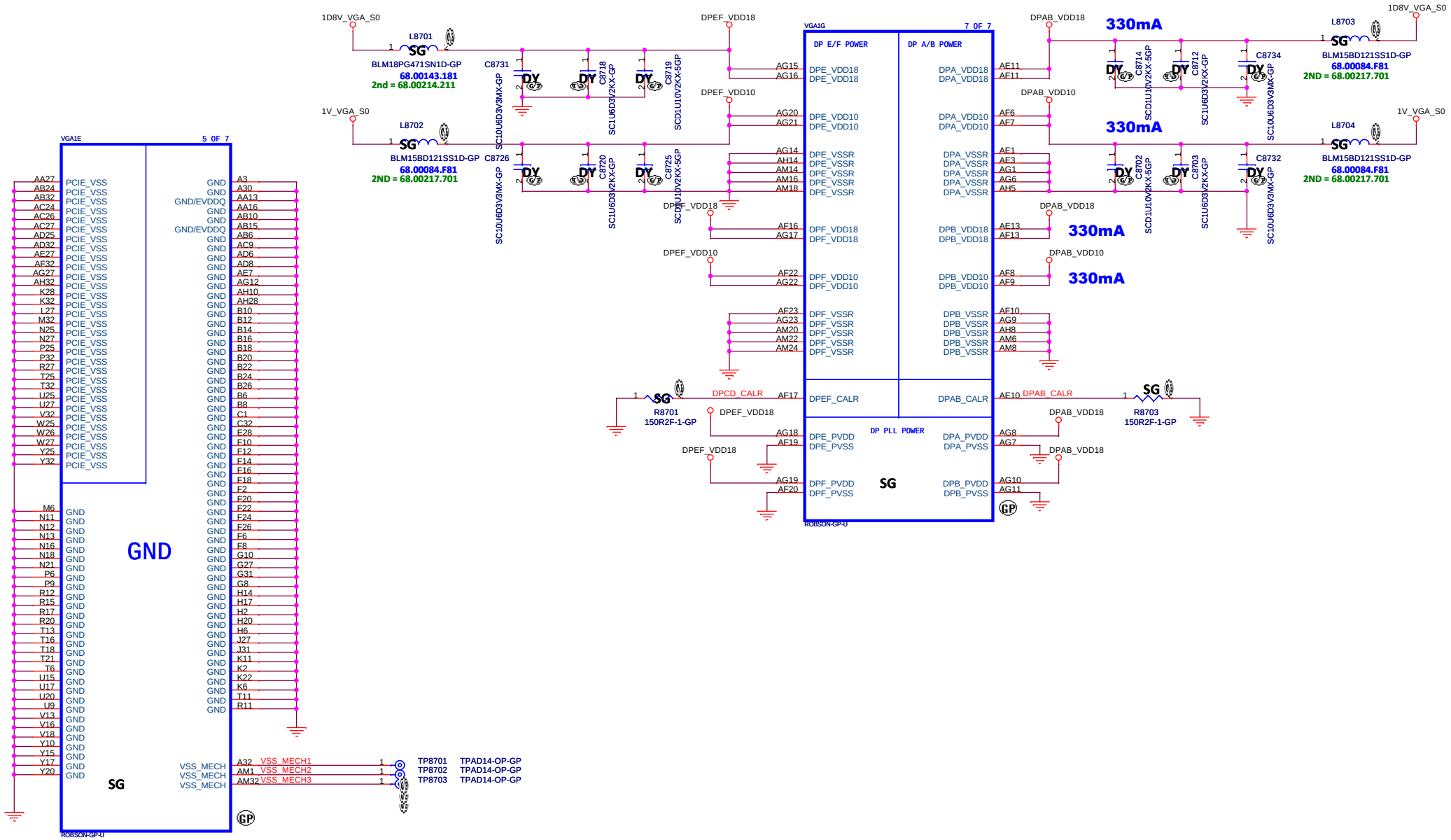
Title: GPU_POWER(4/5)

Size: A2 | Document Number: BMW Z4 DIS | Rev: A00

Date: Friday, March 30, 2012 | Sheet 86 of 105

SSID = VIDEO

For Video output port power rail.



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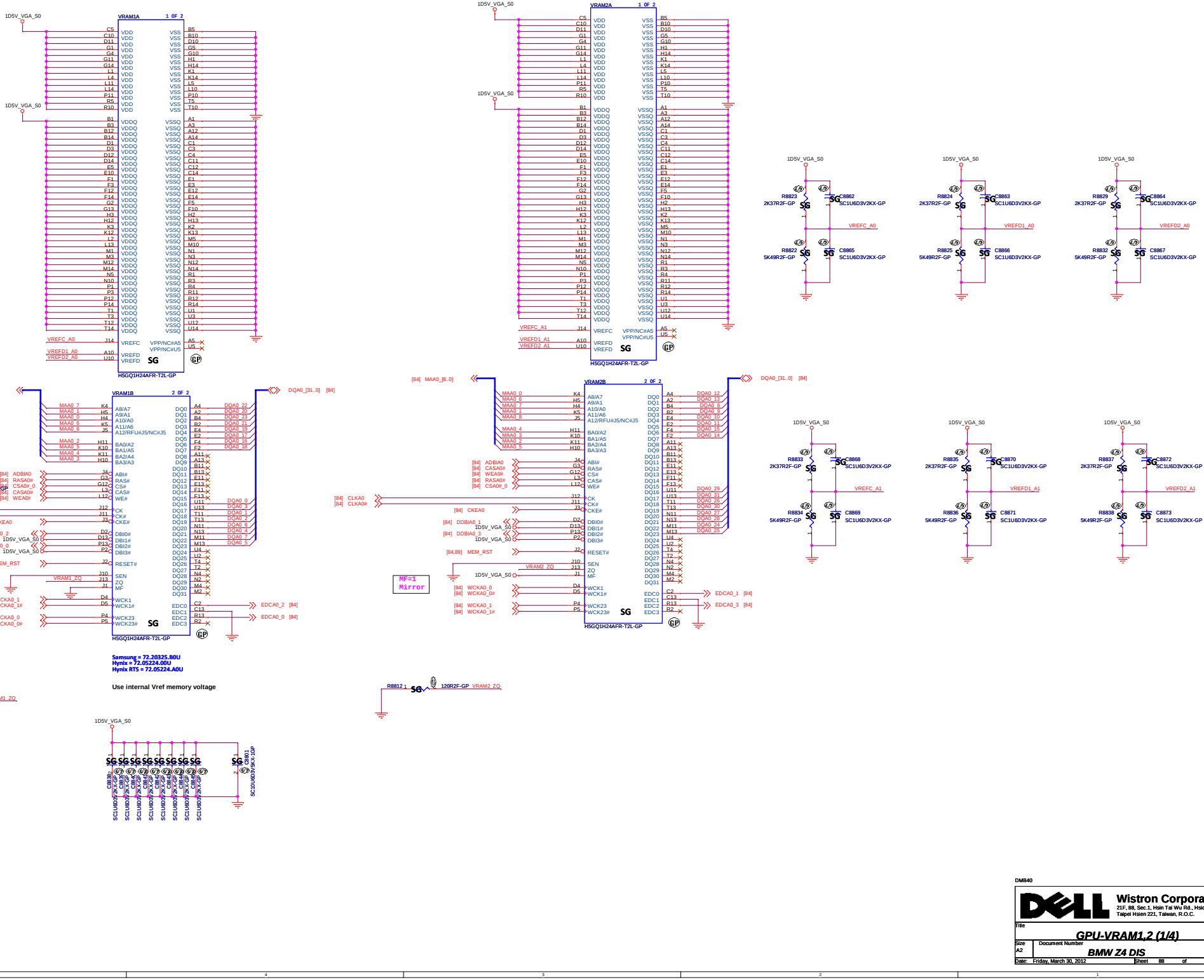
Title: GPU_DPPWR/GND(5/5)

Size	Document Number	Rev
A3	BMW Z4 DIS	A00

Date: Friday, March 30, 2012 Sheet 87 of 105

SSID = VIDEO



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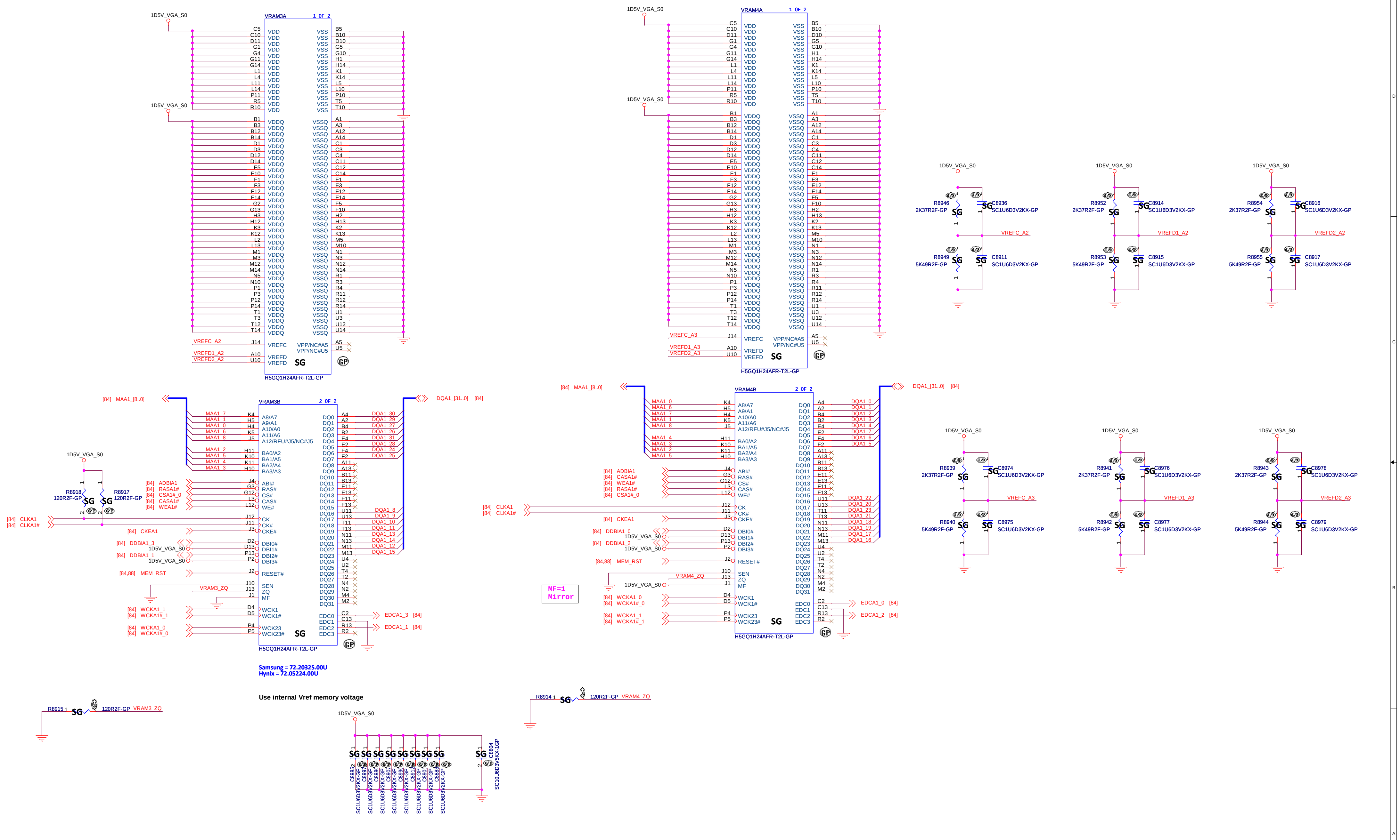
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM1,2 (1/4)

Size: A2 | Document Number: BMW Z4 DIS | Rev: A00

Date: Friday, March 30, 2012 | Sheet 88 of 105

SSID = VIDEO



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Title	GPU-VRAM3,4 (2/4)	
Size A2	Document Number BMW Z4 DIS	Rev A00
Date: Friday, March 30, 2012	Sheet 89 of 105	

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Title: *Reserved*

Size: A3 | Document Number: *BMW Z4 DIS* | Rev: *A00*

Date: Friday, March 30, 2012 | Sheet 90 of 105

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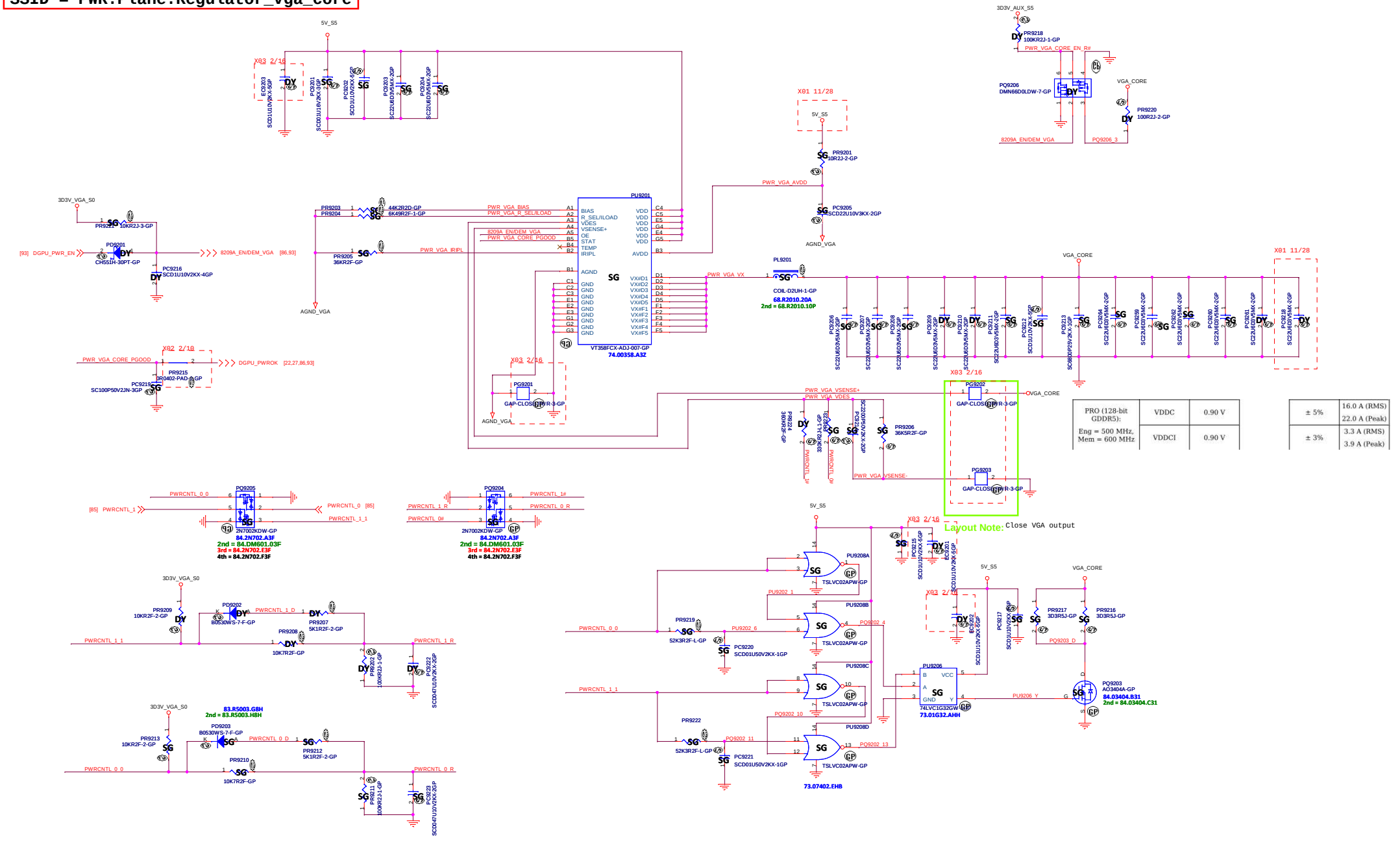
Title: *Reserved*

Size: A3 | Document Number: *BMW Z4 DIS* | Rev: *A00*

Date: Friday, March 30, 2012 | Sheet 91 of 105

SSID = PWR.Plane.Regulator_vga_core



PRO (128-bit GDDR5): Eng = 500 MHz, Mem = 600 MHz	VDDC	0.90 V	± 5%	16.0 A (RMS) 22.0 A (Peak)
	VDDCI	0.90 V	± 3%	3.3 A (RMS) 3.9 A (Peak)

VID0 GPIO15	Voltage
1	1V
0	0.9V

<Core Design>

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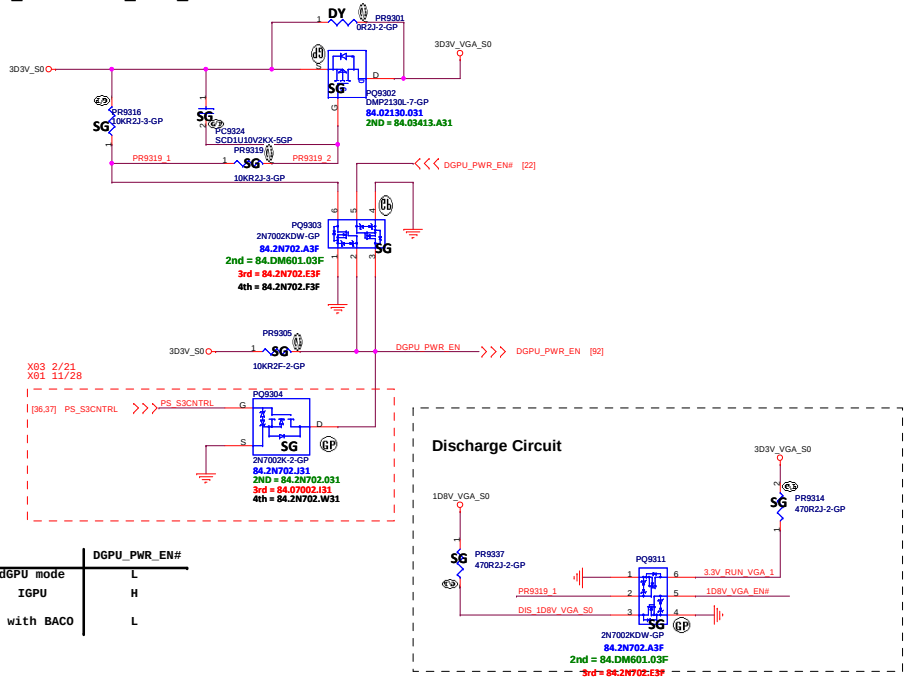
Title: VT357_+VGA_CORE

Size: A2 | Document Number: BMW Z4 DIS | Rev: A00

Date: Friday, March 30, 2012 | Sheet 92 of 105

SSID = PWR.Plane.Regulator_3p3v_vga, 1p8v_vga, 1p5v_vga, 1v_vga

3D3V_S0 to 3D3V_VGA_S0 Transfer

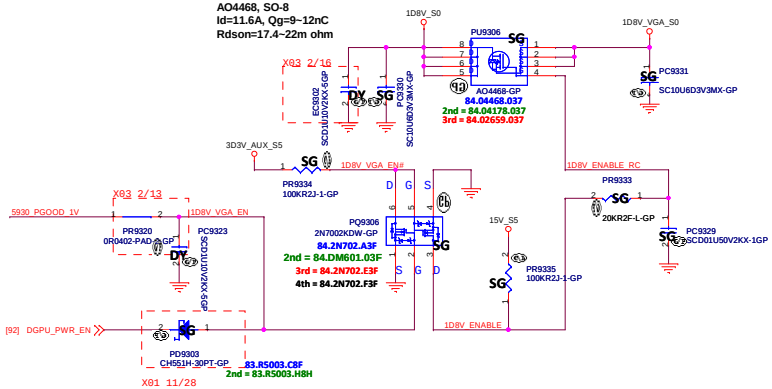


Discharge Circuit

	DGPU_PWR_EN#
dGPU mode	L
IGPU	H
IGPU with BACO	L

1D8V_S0 to 1D8V_VGA_S0 Transfer

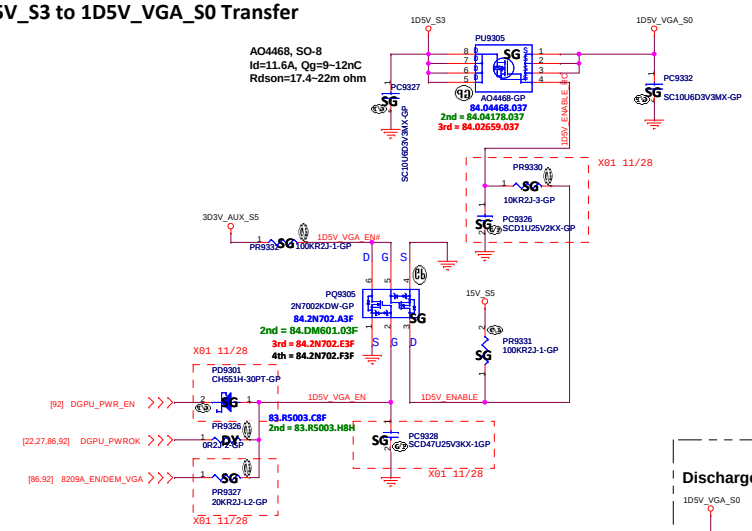
AO4468, SO-8
Id=11.6A, Qg=9~12nC
Rdson=17.4~22m ohm



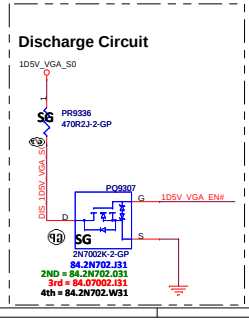
X01 12/15

1D5V_S3 to 1D5V_VGA_S0 Transfer

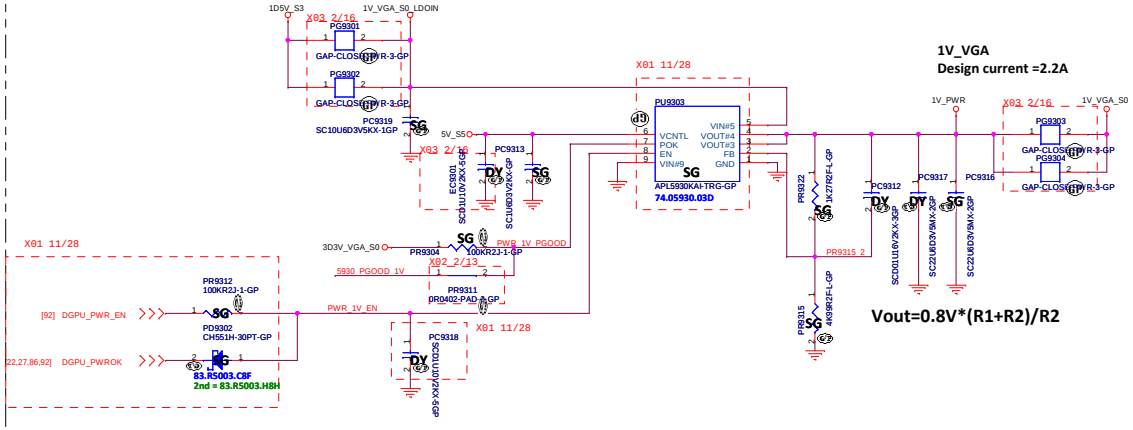
AO4468, SO-8
Id=11.6A, Qg=9~12nC
Rdson=17.4~22m ohm



Discharge Circuit



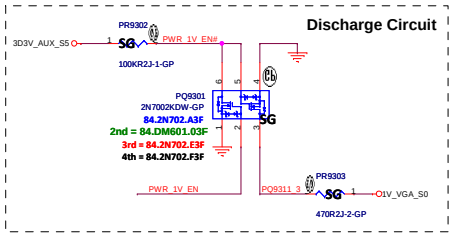
APL5930 for 1V_VGA_S0



1V_VGA
Design current =2.2A

Vout=0.8V*(R1+R2)/R2

Discharge Circuit



<Core Design>

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Title: DISCRETE VGA POWER

Size	Document Number	Rev
A2	BMW Z4 DIS	A00

Date: Friday, March 30, 2012 Sheet 93 of 105

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Title: *Reserved*

Size	Document Number	Rev
A3	*BMW Z4 DIS*	*A00*

Date: Friday, March 30, 2012 Sheet 94 of 105

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Title: *Reserved*

Size	Document Number	Rev
A3	*BMW Z4 DIS*	*A00*

Date: Friday, March 30, 2012 Sheet 95 of 105

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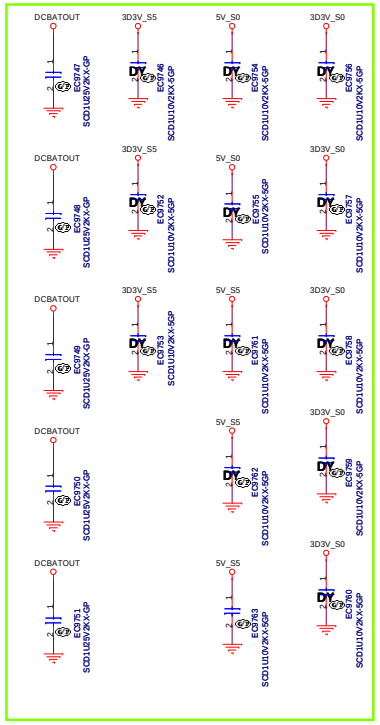
Title: *Reserved*

Size: A3 | Document Number: *BMW Z4 DIS* | Rev: *A00*

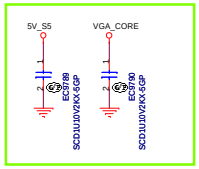
Date: Friday, March 30, 2012 | Sheet 96 of 105

SSID = User.Interface

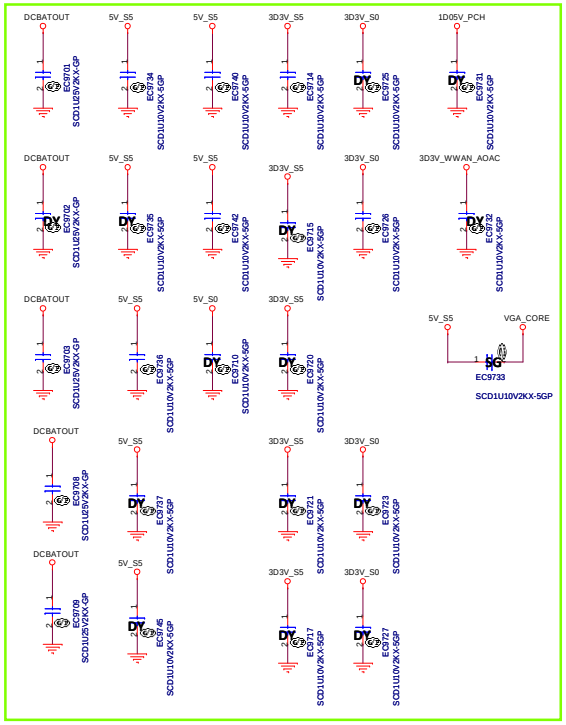
RF



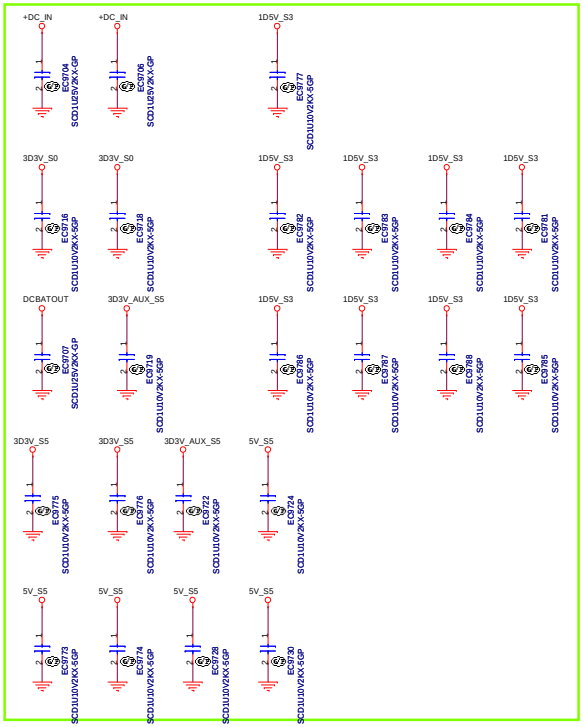
RF X03 2/16



EMI X03 2/13 A00 3/27 A00 3/29

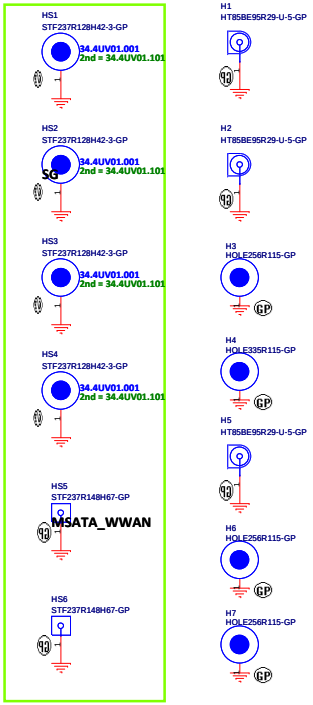


EMI X03 2/16 X03 2/21



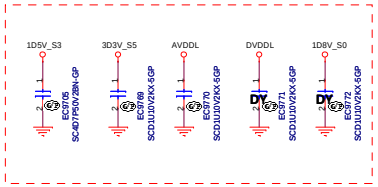
SSID = Mechanical

On the TOP side

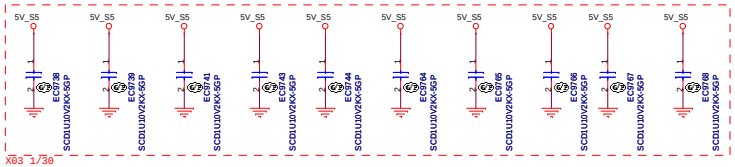


X01 12/23

X01 12/15 For RF



X01 12/09 For EMI X01 12/30



X03 1/30

<Core Design>

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Title: UNUSED PARTS/EMI Capacitors

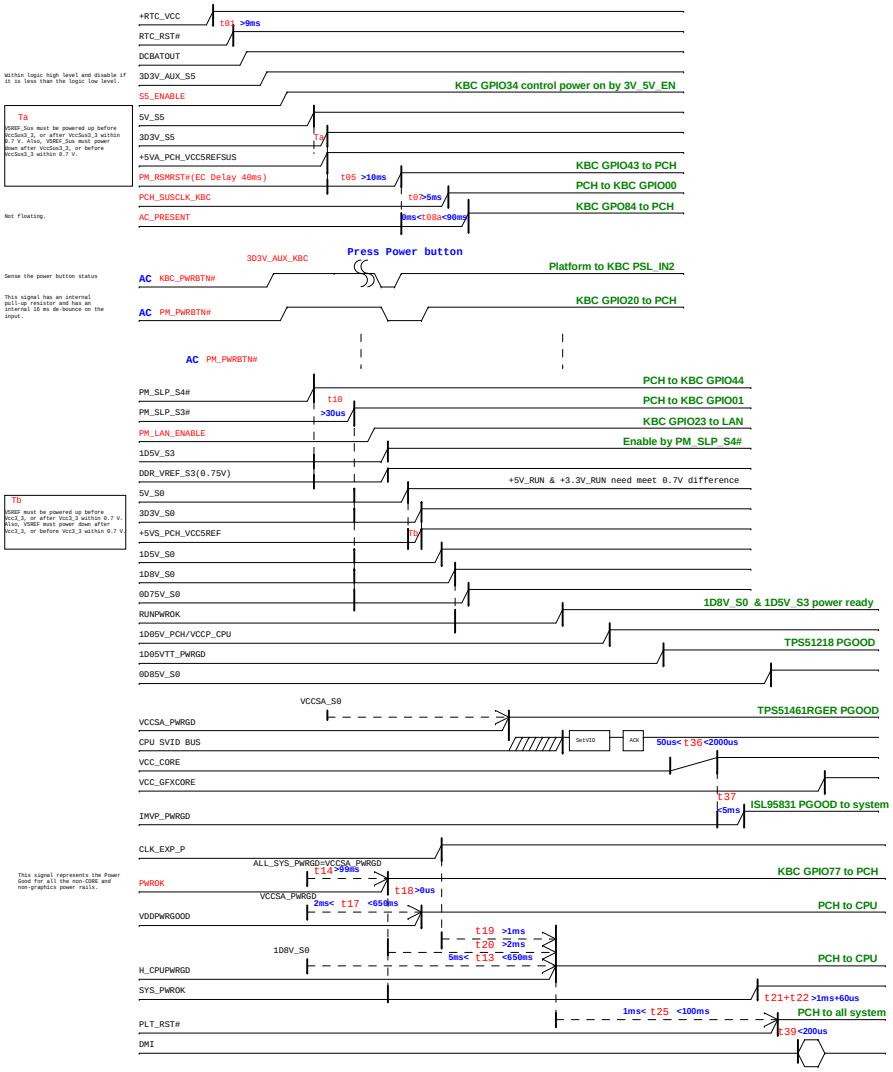
Size: A2 | Document Number: BMW Z4 DIS | Rev: A00

Date: Friday, March 30, 2012 | Sheet 97 of 105

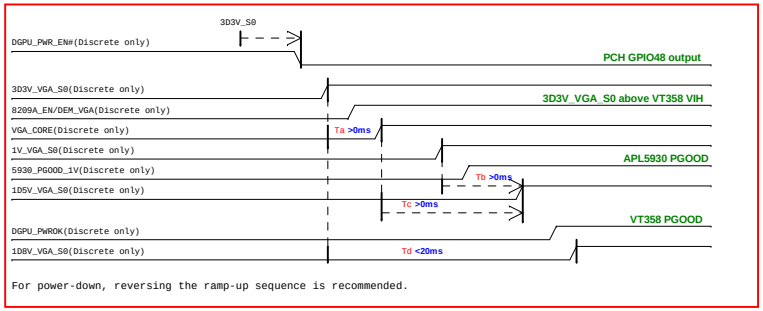
Huron River Platform Power Sequence

(AC mode)

red word: KBC GPIO

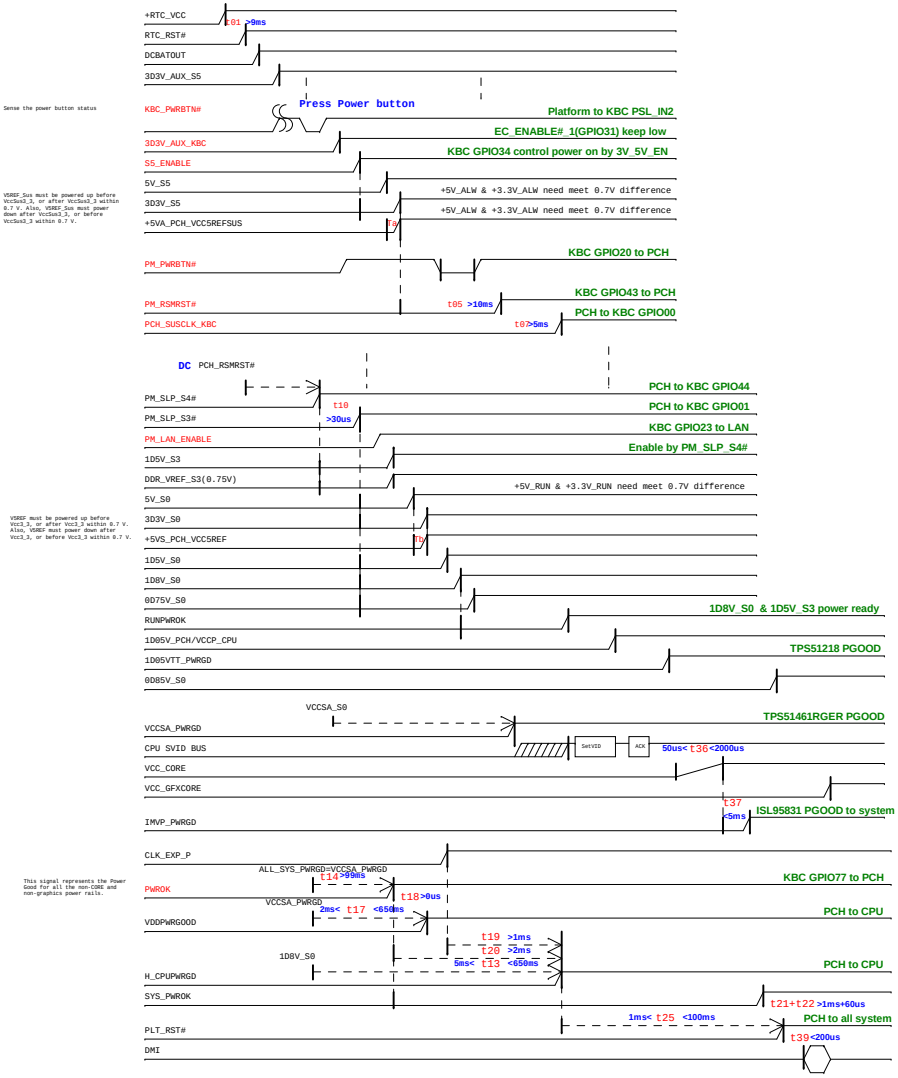


Thames PRO Power-Up/Down Sequence



(DC mode)

red word: KBC GPIO



CMB40

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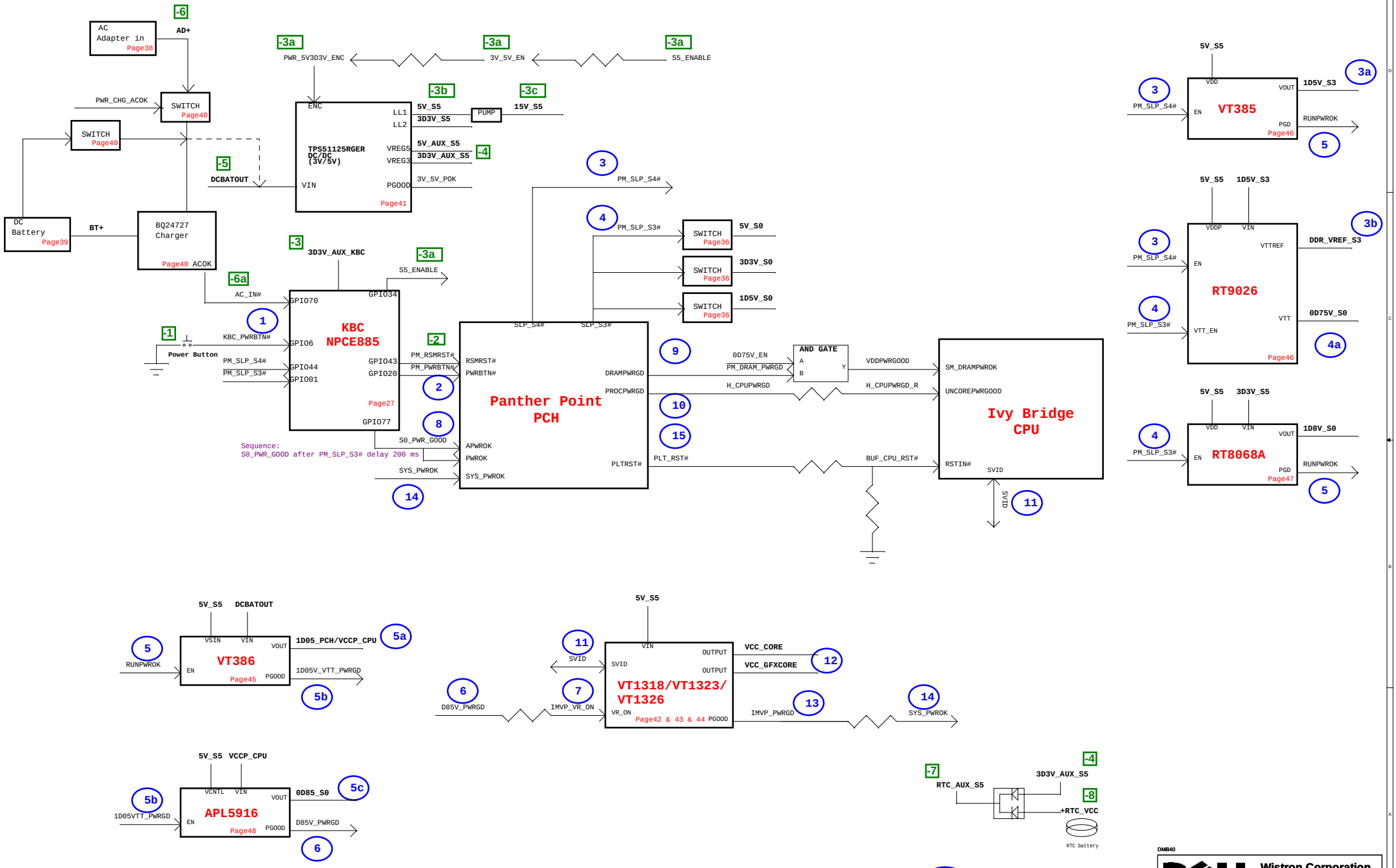
Title: Power Sequence

Size	Document Number	Rev
A1	BMW Z4 DIS	A00

Date: Friday, March 30, 2012 Sheet 98 of 105

Wistron CHIEF RIVER POWER UP SEQUENCE DIAGRAM



Power Up Sequence: -8 ~ 15

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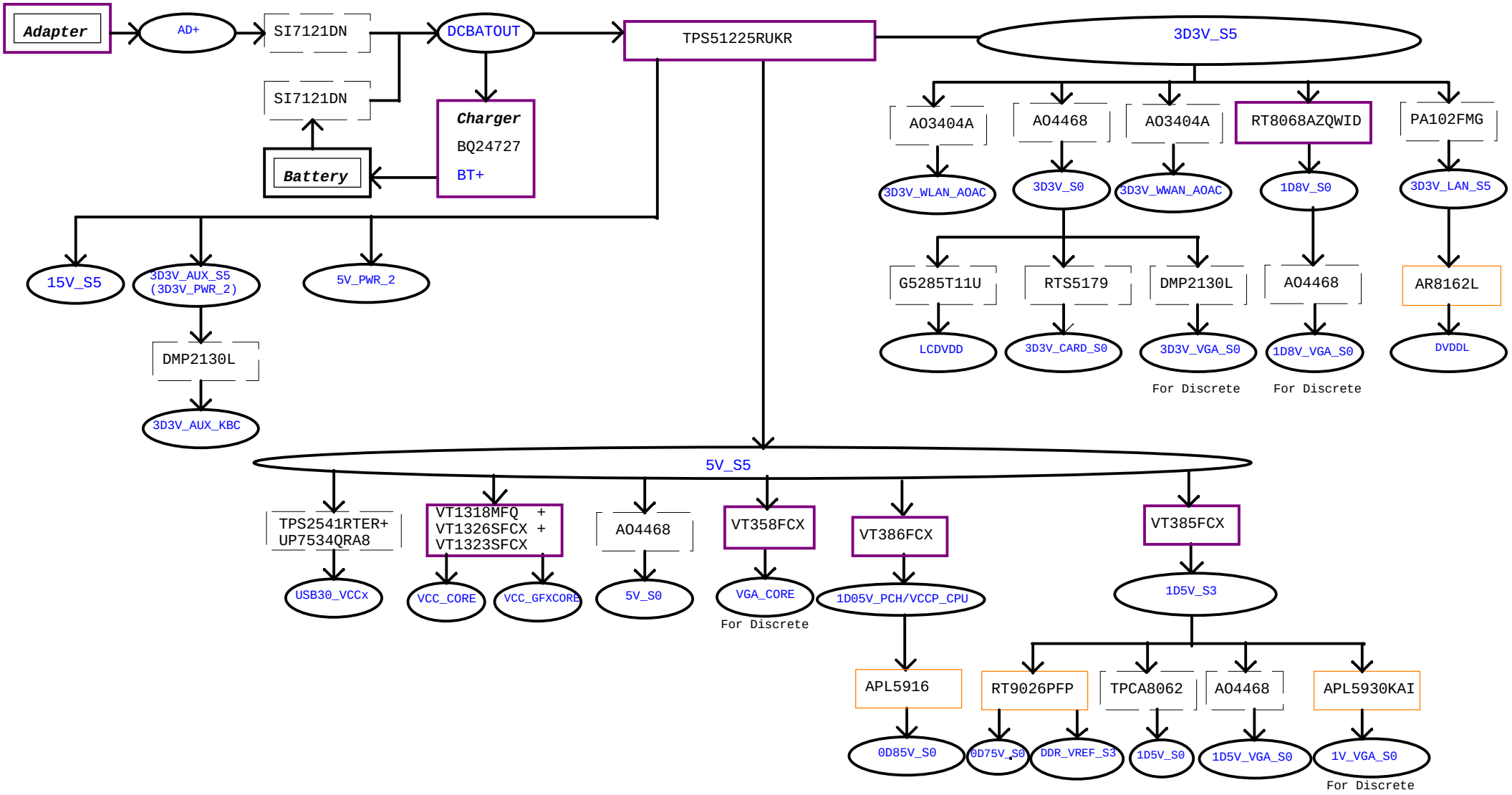
Title: Power Sequence Diagram

Size	Document Number	Rev
A2	BMW Z4 DIS	A00

Date: Friday, March 30, 2012 Sheet 99 of 105



Power Shape

Regulator	LDO	Switch

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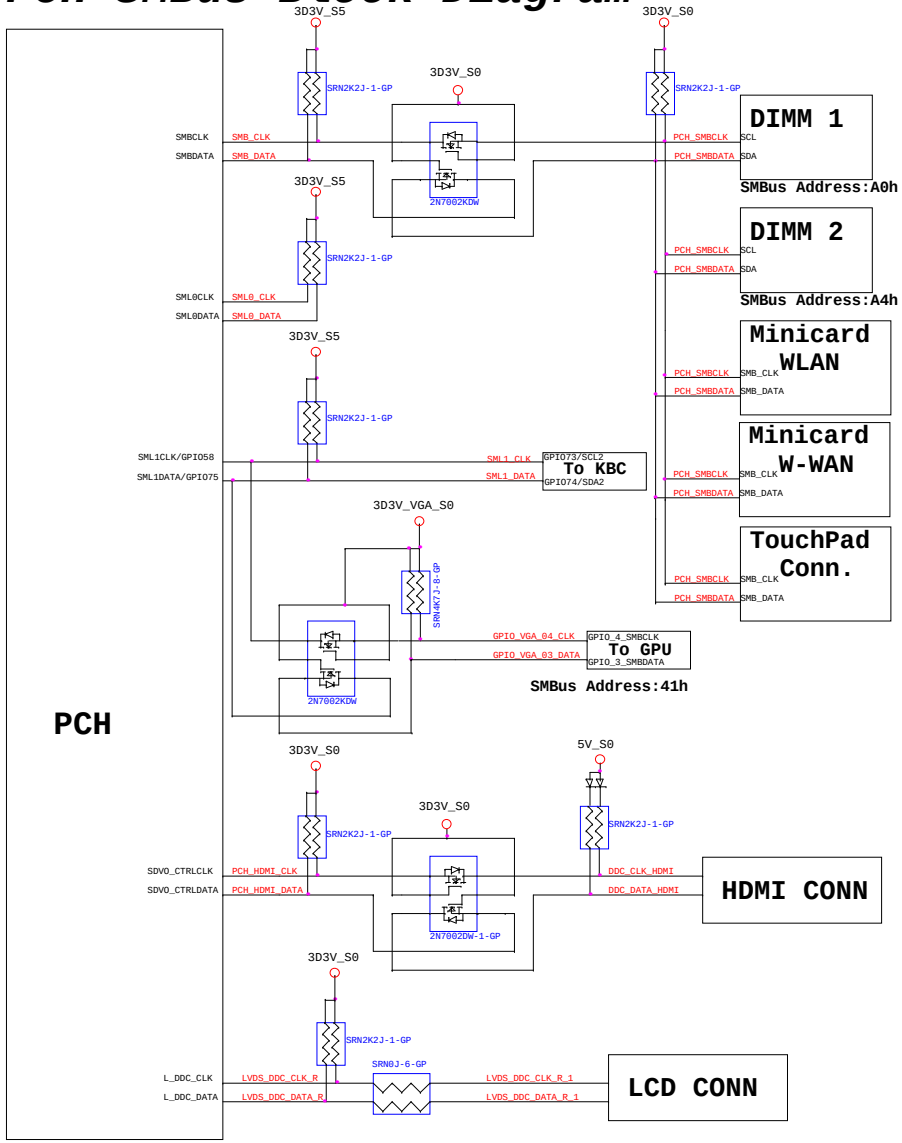
Title: **Power Block Diagram**

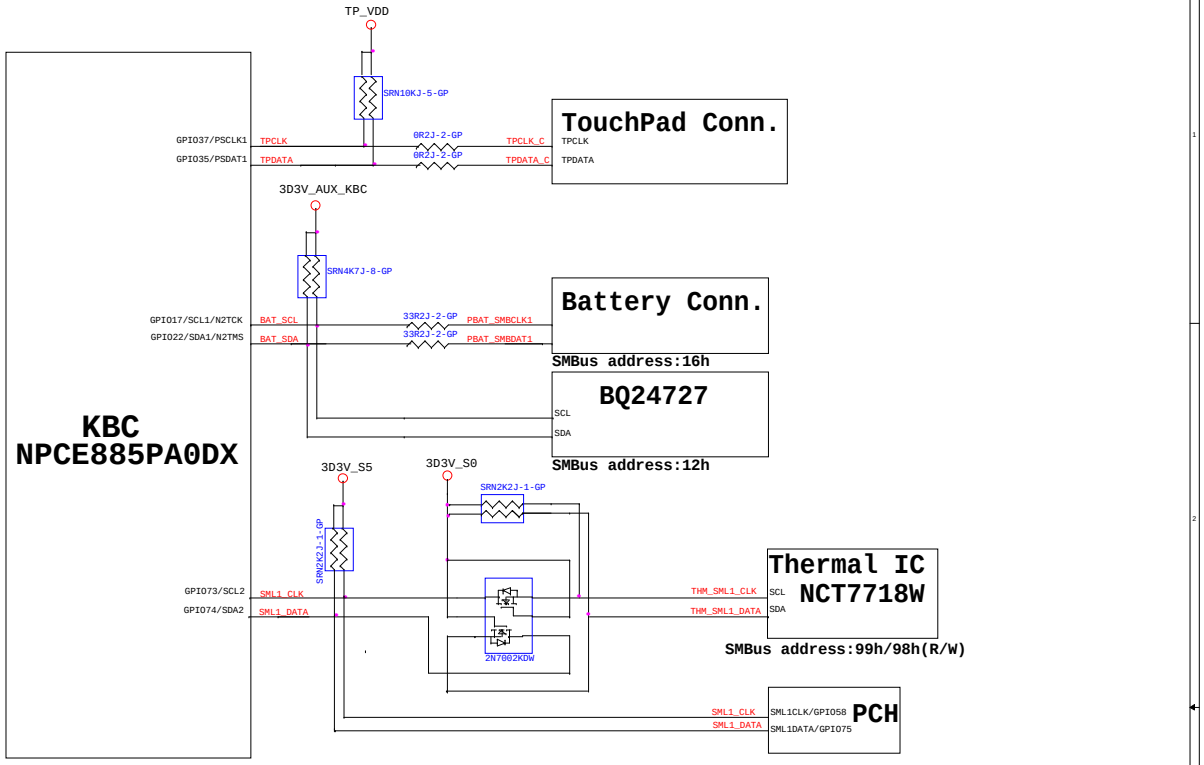
Size	Document Number	Rev
A3	BMW Z4 DIS	A00

Date: Friday, March 30, 2012 Sheet 100 of 105

PCH SMBus Block Diagram



KBC SMBus Block Diagram



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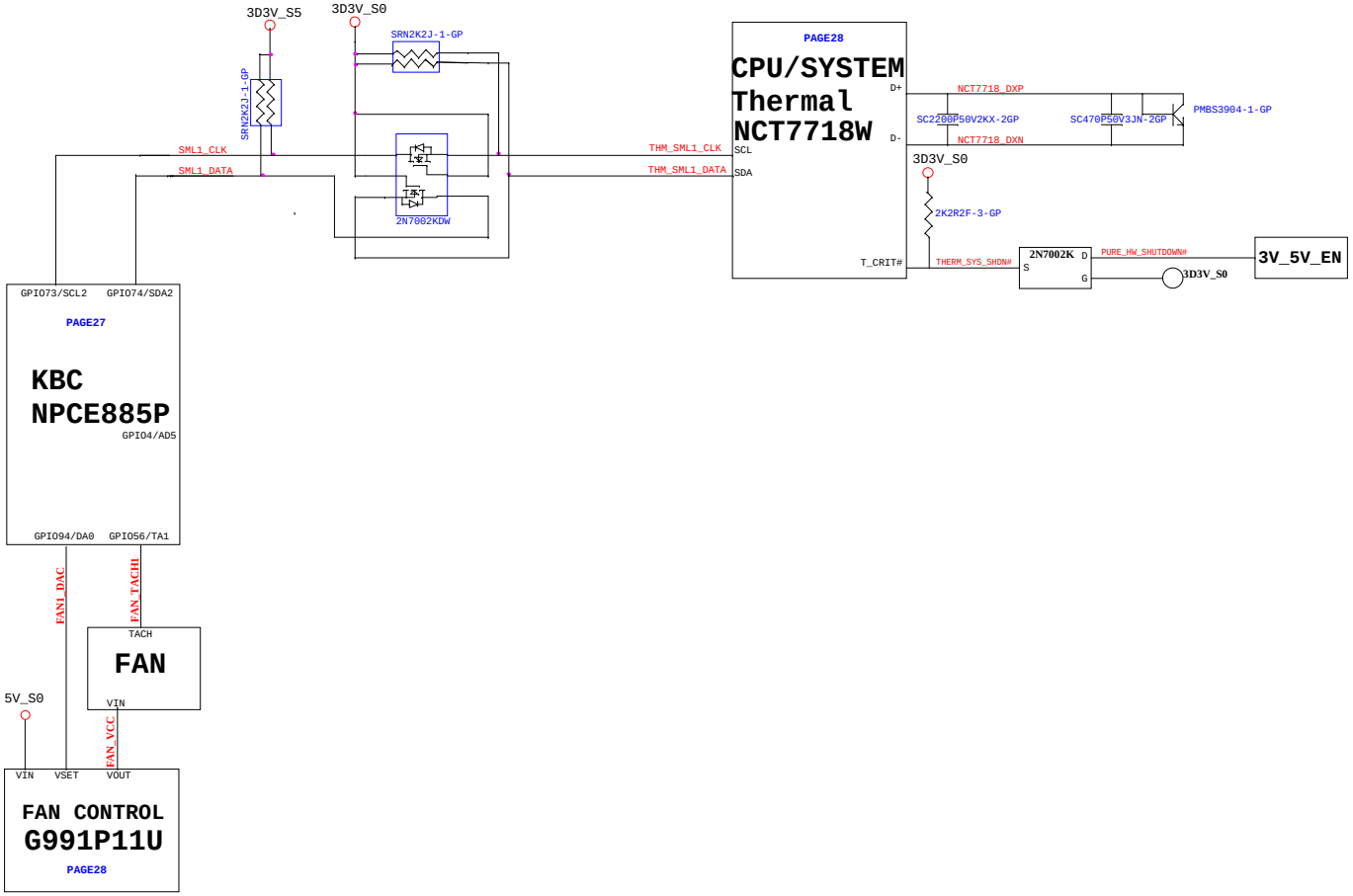
Title: SMBUS Block Diagram

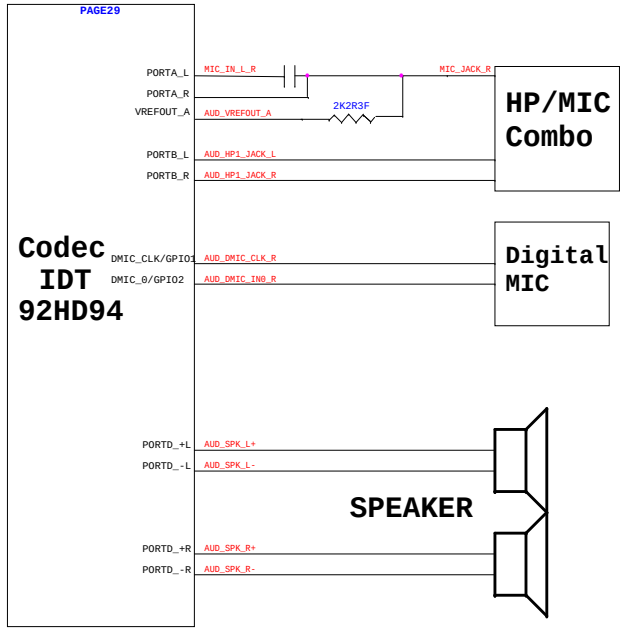
Size	Document Number	Rev
A2	BMW Z4 DIS	A00

Date: Friday, March 30, 2012 Sheet 101 of 105

Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

Size	Document Number	Rev
Custom	BMW Z4 DIS	A00

Date: Friday, March 30, 2012 Sheet 102 of 105

DATE	PAGE	Change Iteam	Owner	Version
2011 11/28	92	Change VT358 AVDD power rail to 5V_S5 to avoide leakage	Power	X01
2011 11/28	92	Re-name Cap PC4663 to PC9218.	EE	X01
2011 11/28	85	Change U8506 power rail and select pin to 3D3V_VGA_S0 to avoid leakage	EE	X01
2011 11/28	93	Change PU9303 to 74.05930.03D by design	EE	X01
2011 11/28	93	POP PD9301, PD9302, PD9303, PD9304, PC9328, change PR9327 to 20K, PR9330 to 10K, PC9326 to 0.1u, PR9312 to 100K, PR9312 re-connect to DGPU_PWR_EN, PD9302 re-connect to DGPU_PWROK for GPU power sequence	EE	X01
2011 11/28	37	Change R3714 to 10K to fix step-like waveform	EE	X01
2011 11/28	84	DY R8408 cause GPU support PX5.0	EE	X01
2011 11/28	86	DY R8605, Q8602, R8603, R8604, U8601, U8602, U8603, U8604, cause GPU support PX5.0	EE	X01
2011 12/02	27	Reserved DGPU_PWROK signal to inform KBC	EE	X01
2011 12/02	62	POP R6208, DY R6201 for USB charging function.	EE	X01
2011 12/02	85	Change VRAM type setting.	EE	X01
2011 12/02	41	Change PT4101, PT4103, PT4104 to 77.52271.09L for design change	EE	X01
2011 12/02	27	Add R2737 for avoiding KBC power drop.	EE	X01
2011 12/02	37	Change R3719 to 0402 type	EE	X01
2011 12/02	69	Change TPAD1 conn by ME	ME	X01
2011 12/02	82	Change LEDBD1 conn by ME	ME	X01
2011 12/02	56	Change HDD1 conn by ME	ME	X01
2011 12/02	68	Change PWSW1 conn by ME	ME	X01
2011 12/02	27	Change RSTSW1 conn by ME	ME	X01
2011 12/02	39	Add BATSW1 and R3901 for avoiding MB crack on assembling.	ME	X01
2011 12/02	60	Change RTC1 conn by ME	ME	X01
2011 12/02	39	DY D3901, D3902, D3903 cause the battery is internal type.	EE	X01
2011 12/02	51	Re-name D5001 and F5001 to D5101 and F5101, and DY F5101 and add R5109 due to no current leakage problem	EE	X01
2011 12/02	14	Change DM1 conn by ME	ME	X01
2011 12/02	27	Change R2724 to 20K for X01 version	EE	X01
2011 12/02	85	DY C8523, cause VGA temp detect by SMBUS.	EE	X01
2011 12/02	28	DY U2803, C2817, C2818 cause VGA temp detect by SMBUS.	EE	X01
2011 12/02	38	Del PR3812.	EE	X01
2011 12/02	49	Change LCD1 conn by ME	ME	X01
2011 12/02	60	POP U6001 and del ROMSK1 for X01 version	EE	X01
2011 12/02	65	Change R6507 to J type	EE	X01
2011 12/02	39	Change BATT1 conn by ME	ME	X01
2011 12/02	82	Change IOBD1 conn by ME	ME	X01
2011 12/02	68	Add WLAN/WWAN LED power control circuit	EE	X01

DATE	PAGE	Change Iteam	Owner	Version
2011 12/09	27	Change AOAC_PCIE_WAKE# pull high to 3D3V_WLAN_AOAC and PCIE_WAKE# to 3D3V_LAN_S5	EE	X01
2011 12/09	66	Change WWAN power to 3D3V_S0	EE	X01
2011 12/09	8	Change VCC_CORE MLCC by power team request	Power	X01
2011 12/09	9	Change AXG_CORE MLCC by power team request	Power	X01
2011 12/09	22	Reserved DGPU_HOLD_RST# & DGPU_PWR_EN# pull high and down	EE	X01
2011 12/09	97	Follow EMI request added Cap.	EMI	X01
2011 12/09	20	Rename PCIE request pin	EE	X01
2011 12/09	65	Add WLAN requirst circuit	EE	X01
2011 12/12	40	design change PU4001 by Power team request	Power	X01
2011 12/12	41	design change PU4106 by Power team request	Power	X01
2011 12/12	41	Change PU4102 to colay symbol by Power team request	Power	X01
2011 12/12	45	Change PU4501to VT386 by Power team request	Power	X01
2011 12/12	46	Change PR4609 and PR4612 by Power team request	Power	X01
2011 12/12	48	Change PU4801 by Power team request	Power	X01
2011 12/12	43	Reserved PT4301 by Power team request	Power	X01
2011 12/12	84	Change R8412 to 4.7k.	EE	X01
2011 12/12	27	Change U2701 to new P/N	EE	X01
2011 12/13	82	Add ER8201, ER8202, ER8203, ER8204 by EMI request.	EMI	X01
2011 12/13	18	Reserved USB_PN13, USB_PP13 test point.	EE	X01
2011 12/13	62	Del USB3.0 Redriver circuit.	EE	X01
2011 12/13	27	Change R2735 and R2737 to 20K for fix AUX power overshoot.	EE	X01
2011 12/13	41	Change PC4127 to 4.7uF for fix AUX power overshoot.	EE	X01
2011 12/13	82	Add ER8205, EC8206 by EMI request.	EMI	X01
2011 12/13	46	Add EL4601, EL4602 by EMI request.	EMI	X01
2011 12/13	43	Add EG4301,EG4302EG4303,EG4304,EG4305,EG4306,EG4307 by EMI request.	EMI	X01
2011 12/13	44	Add EG4401,EG4402,EG4403,EG4404,EG4405,EG4406,EG4407 by EMI request.	EMI	X01
2011 12/13	15	Change DM2 conn by ME request	ME	X01
2011 12/15	97	Add EC9736, EC9726, EC9750 EC9708, EC9709, EC9770, EC9705, EC9769 by RF request.	RF	X01
2011 12/15	56	Add EC5601 by RF request.	RF	X01
2011 12/15	46	Add EC4638 by RF request.	RF	X01
2011 12/15	31	Add EC3122 by RF request.	RF	X01

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Title: **Change History**

Size: A3 | Document Number: **BMW Z4 DIS** | Rev: **A00**

Date: Friday, March 30, 2012 | Sheet 103 of 105

DATE	PAGE	Change Iteam	Owner	Version
2011 12/15	14	Change DM1 P/N to 62.10017.S81	EE	X01
2011 12/15	15	Change DM2 P/N to 62.10017.T01	EE	X01
2011 12/15	62	Del R6201 change by USB detect function	EE	X01
2011 12/15	65	DY R6507, U6501 for design change	EE	X01
2011 12/15	68	Add R6809, DY C6802, R6803, D6802, WLAN LED power control by AOAC_WLAN_EN#.	EE	X01
2011 12/15	8	Change C825, C830, C831, C832 to 0805 type.	EE	X01
2011 12/15	9	Change C906, C907, C908, C909, C910 to 0805 type.	EE	X01
2011 12/15	93	Del 1D8V_VGA_S0 power good circuit.	EE	X01
2011 12/15	83	Del VGA_RST# circuit.	EE	X01
2011 12/15	86	Del 1D5V_VGA_S0 power good circuit.	EE	X01
2011 12/15	31	Reserved EC3101 by RF request.	RF	X01
2011 12/15	97	Reserved EC9771, EC9772 by RF request.	RF	X01
2011 12/16	86	Change C8642, C8650, C8647 to 22u 0805 size.	EE	X01
2011 12/16	62	Pop TR6204, DY R6279, R6280.	EMI	X01
2011 12/16	49	Pop TR4902, DY R4903, R4906.	EMI	X01
2011 12/16	8	Change C847 to 22u 0805 size.	EE	X01
2011 12/16	68	Pop C6802, for soft start.	EE	X01
2011 12/19	38	Change PC3806 to 0805 type	Power	X01
2011 12/19	43	Del PT4301 cause no layout area.	Power	X01
2011 12/20	44	Change PWR_GFX to PWR_CPU	Power	X01
2011 12/20	18	Change touch panel USB signal to port 4.	EE	X01
2011 12/20	82	Reserved TPAN1, and swap IOBD1's main and 2nd source.	EE	X01
2011 12/20	49	Swap LCD1's main and 2nd source.	EE	X01
2011 12/20	14	Change R1401, R1402 to short pad	EE	X01
2011 12/20	15	Change R1502 to short pad	EE	X01
2011 12/20	39	Change R3902, R3903, R3904 to 100 ohm to avoid break KBC when battery in.	EE	X01
2011 12/20	27	Del RN2703, add R2714, R2715.	EE	X01
2011 12/21	48	POP PR4814, change PR4811 to 365ohm, PR4813 to 100Kohm	Power	X01
2011 12/21	21	Add R2115 and del R6001 for SPI louting setting	EE	X01
2011 12/21	8	DY C807, C843, C824.	Power	X01
2011 12/21	42	Change PR4236 to 374ohm, PR4249 to 7.68Kohm.	Power	X01
2011 12/21	43	Change PU4301 IC to lastly version.	Power	X01
2011 12/21	44	Change PU4401 IC to lastly version.	Power	X01
2011 12/21	40	Design change PU4002 by power request	Power	X01
2011 12/21	27	Add R2716 to modify PSL circuit.	EE	X01
2011 12/23	82	Swap USB1, USB10 signal to TR8202 TR8201 for layout	EE	X01

DATE	PAGE	Change Iteam	Owner	Version
2011 12/23	62	Swap USB0 signal to TR6204 for layout	EE	X01
2011 12/23	97	Del H8.	ME	X01
2011 12/27	51	Pop D5101, DY R5109.	EE	X01
2011 12/30	93	Change PD9301, PD9302, PD9303, PD9304's 2nd source to 83.R5003.H8H	EE	X01
2011 12/30	31	Change U3101 to 71.08162.A03 due to vendor update new version.	EE	X01
2011 12/30	97	Pop EC9738, EC9739, EC9741, EC9743, EC9744, EC9764, EC9765, EC9766, EC9767, EC9768	EMI	X01
2011 12/30	36, 93	Change U3601 U3602 PU9305 PU9306 2nd to 84.04178.037	Power	X01
2011 12/30	49	Change TR4902 to 69.10103.041	EMI	X01
2012 01/09	15, 24	DY C1507 and C2403 by PI testing result.	EE	X01
2012 01/09	48	Change VCCSA to LDO type.	Power	X02
2012 01/09	51	Change HDMI SMBUS pull up power to 5V_HDMI_S0_R	EE	X03
2012 01/30	48	Reserved PC4818 PC4819 to prevent VCCSA power IC VID setting(PWM solution)	EE	X03
2012 01/30	68	Add D6803 to fix DW1703 BT LED behavior. and change WLAN LED power rail to 5V_S0.	EE	X03
2012 01/30	97, 38	Take off EC9704, del PS_ID_R.	EE	X03
2012 01/30	82	Move IO BD conn signal for coaxial cable	EE	X03
2012 01/30	66	DY R6615.	EE	X03
2012 01/30	40, 38	Change PR4004 to 3K and PR3816 to 3.3K for hiccup mode adaptor.	EE	X03
2012 01/30	62	Change U6201 to lastly version.	EE	X03
2012 01/30	31	Change L3101 to prevent the shortage problem.	EE	X03
2012 02/06	82	Change TPAN1 P/N by ME request and modify conn pin define.	EE	X03
2012 02/06	31	Reserved C3110 for Lan IC.	EE	X03
2012 02/06	5, 8, 9, 14, 15, 19, 23, 24, 27, 28, 36, 37, 38, 49, 51, 62, 65, 66, 83, 85	Change R504, R812, R909, R1404, R1405, R1505, R1503, R1921, R1916, R1924, R1929, R1925, R2304, R2301, R2307, R2306, R2308, R2403, R2404, R2412, R2402, R2702, R2765, R2794, R2778, R2792, R2733, R2767, R2768, R2720, R2764, R2723, R2727, R2807, R3614, R3710, PR3819, R4912, R4913, R5125, R5101,R5102, R5149, R5103, R5108, R5107, R5106, R5105, R6202, R6203, R6204, R6205, R6505, R6502, R6616, R8322, R8504, R8506, R8507, to short pad	EE	X03
2012 02/10	41, 42, 45, 46, 47, 95	Change PR4127, PR4130, PR4133, PR4116, PR4251, PR4250, PR4212, PR4207, PR4228, PR4523, PR4522, PR4510, PR4511, PR4626, PR4621, PR4622, PR4623, PR4611, PR4602, PR4702 ,PR9215 to short pad	Power	X03
2012 02/13	51	Change HDMI output power design	EE	X03
2012 02/13	41, 42, 18 19, 28, 93	Change PR9311, PR9320, PR4116, PR4219, PR4223, PR4252, PR4254, PR4261, R1823, R1927 R2813 to short pad	Power	X03
2012 02/13	97	Add EC9704, EC9706, EC9716, EC9718, EC9722, EC9724, EC9728, EC9730, EC9775, EC9776, EC9773, EC9774,EC9701, EC9751, EL4901 by EMI required	EMI	X03

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Title: **Change History**

Size: A3 | Document Number: **BMW Z4 DIS** | Rev: **A00**

Date: Friday, March 30, 2012 | Sheet 104 of 105

DATE	PAGE	Change Iteam	Owner	Version
2012 2/16	27	Change PCB version to X03, X02 is for VCCSA LDO version verify.	EE	X03
2012 2/16	97	Add EC9777, EC9778, EC9779, EC9780, EC9781, EC9782, EC9783, EC9784, EC9785, EC9786, EC9787, EC9788 by EMI required	EMI	X03
2012 2/16	8	Del C819, add C815	EE	X03
2012 2/16	40, 41, 42 43, 44, 45 46, 47, 48 92, 93	Change Pad type, change to green cover type.	EE	X03
2012 2/16	45	Add EL4501, EL4502 by EMI required.	EMI	X03
2012 2/16	92, 93	Reserved EC9201, EC9202, EC9203, EC9301, EC9302, EC9303 by RF required.	RF	X03
2012 2/16	49	Add EC4901, EC4902, EC4904, EC4905, EC4906, EC4908, EC4909, EC4910, EC4911, EC1524, EC1428, EC2409, EC2305, EC4528, EC4521, EC4507, EC9789, EC9790 by RF required.	RF	X03
2012 2/20	41, 43, 44	Add Power Gap PG4115, PG4116, PG4117 EG4308, EG4309, EG4310. EG4311, EG4408 EG4409, EG4410, EG4411 for power team	Power	X03
2012 2/21	93	Add PQ9304 for fine tune GPU sequence	EE	X03
2012 2/21	42	Change PR4236 to 953ohm, PR4239 to 300ohm	Power	X03
2012 2/21	14, 97	Change EC9778, EC9779, EC9780 to EC1406, EC1407, EC1408 by layout.	EE	X03
2012 2/29	59	Change C5902 P/N.	EE	X03
2012 3/15	82, 85, 39	DY R8501, R8204, TPAN1, R3901	EE	A00
2012 3/15	27	Change R2724 to 64.9k for A00 PCB version	EE	A00
2012 3/15	71, 82	Change DB1 and CRTBD1 to green cover type symbol.	EE	A00
2012 3/15	85	Pop R8535	EE	A00
2012 3/22	68	Del WLAN LED control power rail circuit.	EE	A00
2012 3/23	20, 22, 62 65, 48, 40 66, 82	Change ER8201, ER8202, ER8203, ER8204, R6503, R6506, R6601, R6602, ER8205, R2205, R3113, R6281, R6282, R6283, R6284, R6616, PR4022, PR4801, PR4803, RN2012, RN2014, RN2017, to short pad and del TR6501, TR6601, TR8201, TR8202, TR6205, TR6206.	EE	A00
2012 3/27	82, 97	Pop EC8207, EC9734, reserved ER1807 by EMI request.	EMI	A00
2012 3/27	49, 62	Del R6279, R6280, R4903, R4906 by PSE request	EE	A00
2012 3/27	69	Change R6909 to 0603 type.	EE	A00
2012 3/27	49	Change RN4902 to 100 Ohm.	EE	A00
2012 3/27	21	Change R2136 R8612 to short pad, and change RN2101 to R2116, R2121, R2127, R2128 short pad	EE	A00
2012 3/29	45, 97	Del EL4502 and EC9729 for layout.	EE	A00
2012 3/30	8	Del C819 for layout.	EE	A00

DATE	PAGE	Change Iteam	Owner	Version

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Title: **Change History**

Size: A3 | Document Number: **BMW Z4 DIS** | Rev: **A00**

Date: Monday, April 02, 2012 | Sheet 105 of 105