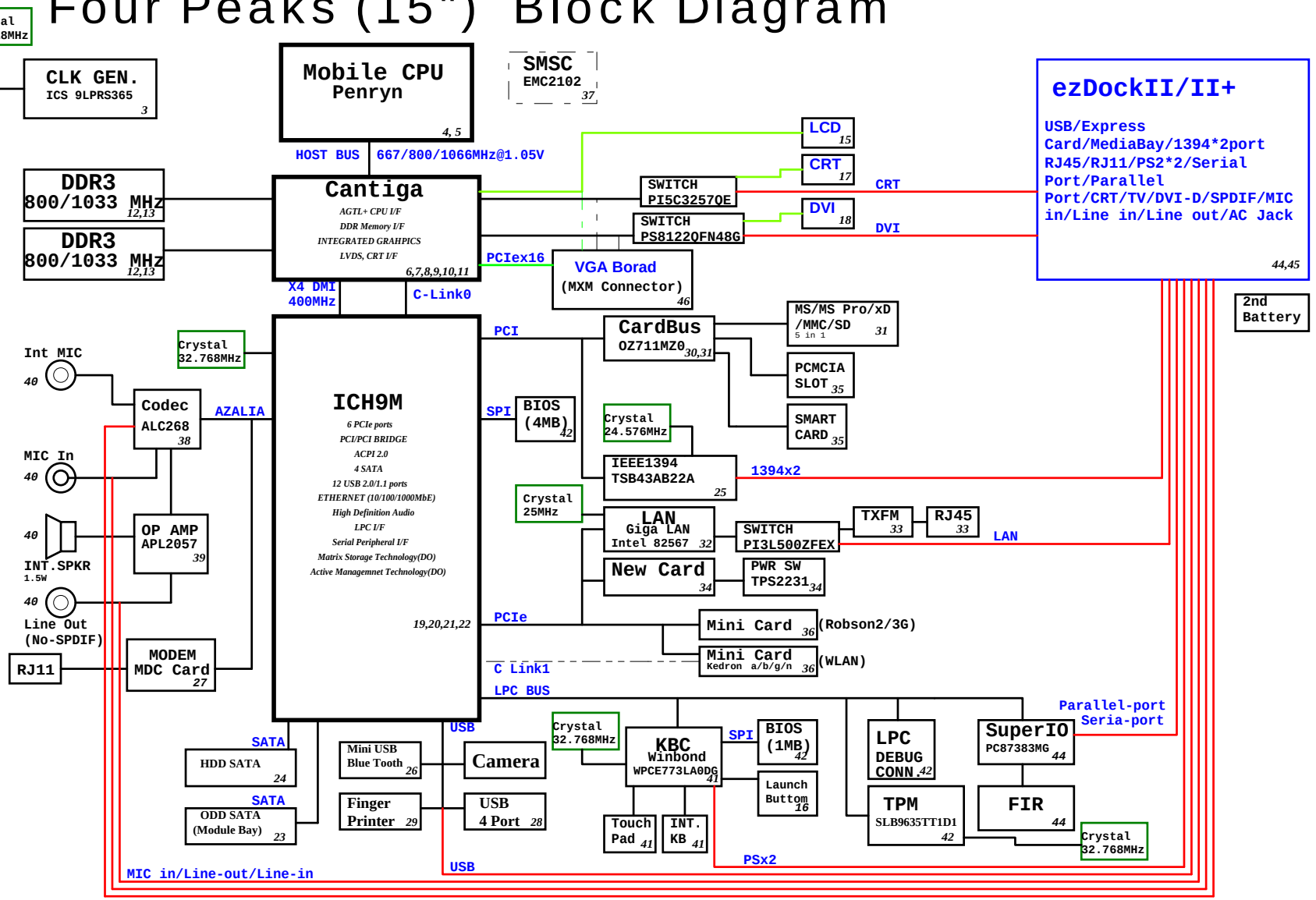
Four Peaks (15") Block Diagram

Project code: 91.4Z901.001
PCB P/N : 48.4Z901.011
REVISION : -1M



SYSTEM DC/DC TPS51125 50

INPUTS	OUTPUTS
DCBATOUT	5V_S5(7A) 3D3V_S5(7A) 5V_AUX_S5 3D3V_AUX_S5

SYSTEM DC/DC TPS51124 51

INPUTS	OUTPUTS
DCBATOUT	1D05V_M(16A) 1D5V_S3(12A)

RT9026 52

1.5V_S3	DDR_VREF_S3 (1.2A)

G9131 52

3D3V_S0	2D5V_S0 (300mA)

TPS51117 54

DCBATOUT	1D8V_S0 (9.4A)

CHARGER BQ24750 55

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A

CPU DC/DC ISL6266A 49

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0~1.3V 38A

GFX DC/DC ISL6263 53

INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE 0~1.3V 6.5A

PCB STACKUP

TOP
VCC
S
S
GND
BOTTOM

Four Peaks
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: BLOCK DIAGRAM
Size: A2 | Document Number: Four Peaks | Rev: -1M
Date: Friday, November 21, 2008 | Sheet 1 of 57

ICH9M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9M Integrated Pull-up and Pull-down Resistors

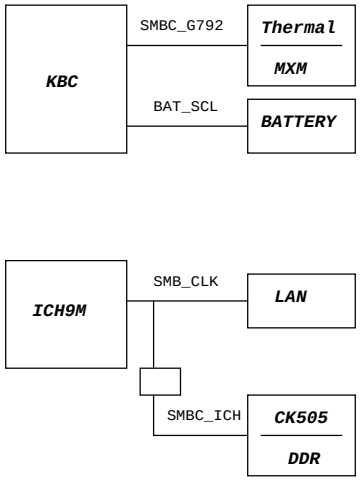
SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) **1=The iTPM Host Interface is disalbed(default)**
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality (default)**
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1= Disabled (default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) **11 = Disabled (default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation(Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 =Digital display Port and PCIe are operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	**0 =No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG/12/CFG13 straps can be enabled at any time.

SMBus



PCI Routing

page 17

	IDSEL	INT	REQ	GNT
TI7412	AD22	G:CARDBUS B:1394 F:Flash Media G:SD Host	0	0

PCIE Routing

LANE1	LAN BCM5787M
LANE2	MiniCard WLAN
LANE3	NewCard WLAN

USB Table

USB	
Pair	Device
0	NC
1	NC
2	USB2
3	USB4
4	USB3
5	BLUETOOTH
6	WEBCAM
7	FT
8	MINICARD
9	NEW1

Four Peaks

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Title: **Reference**

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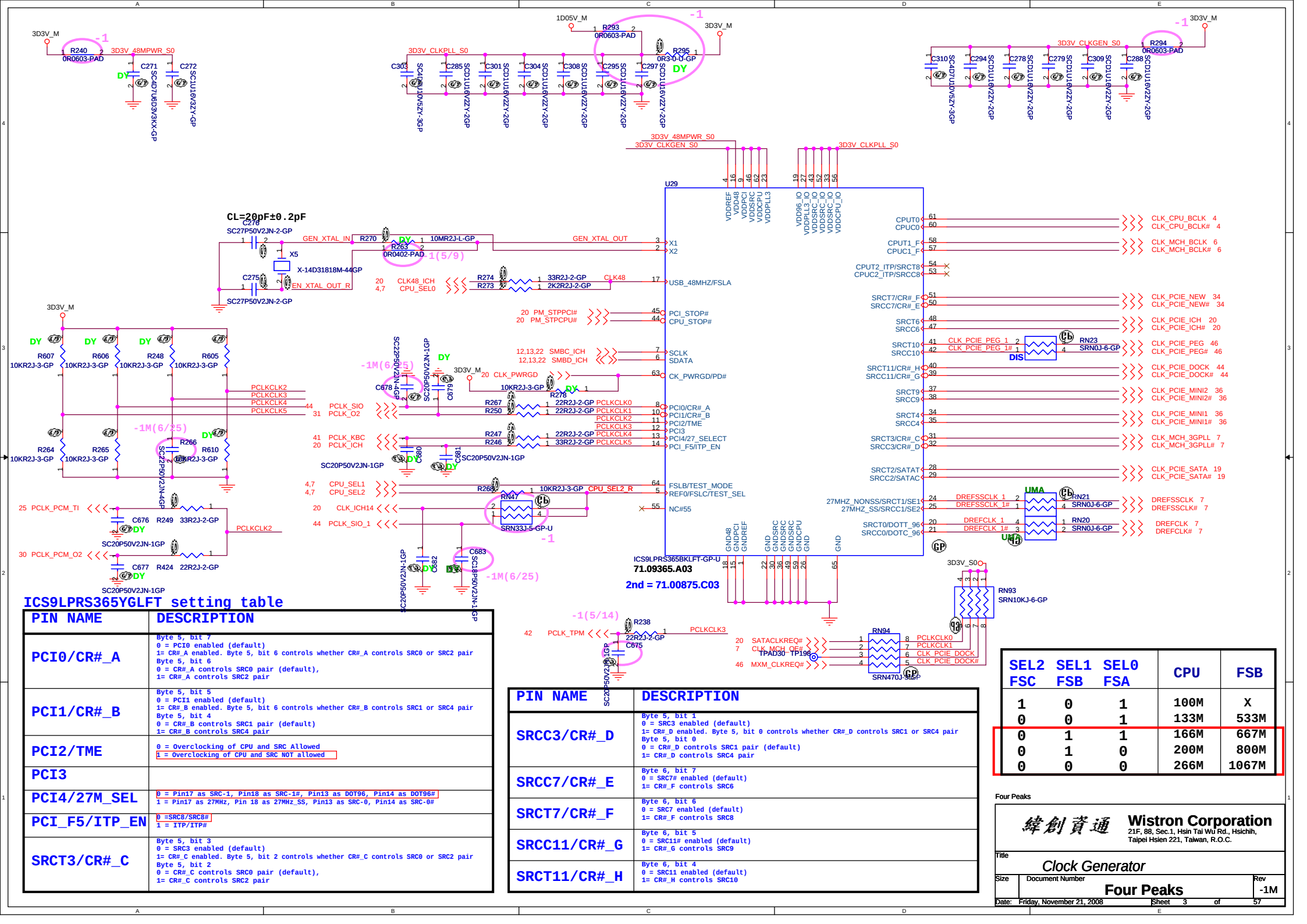

ICS9LPRS365YGLFT setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3	
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#
SRCT3/CR#_C	Byte 5, bit 3 0 = SRC3 enabled (default) 1= CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1= CR#_C controls SRC2 pair

PIN NAME	DESCRIPTION
SRCC3/CR#_D	Byte 5, bit 1 0 = SRC3 enabled (default) 1= CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1= CR#_D controls SRC4 pair
SRCC7/CR#_E	Byte 6, bit 7 0 = SRC7# enabled (default) 1= CR#_F controls SRC6
SRCT7/CR#_F	Byte 6, bit 6 0 = SRC7 enabled (default) 1= CR#_F controls SRC8
SRCC11/CR#_G	Byte 6, bit 5 0 = SRC11# enabled (default) 1= CR#_G controls SRC9
SRCT11/CR#_H	Byte 6, bit 4 0 = SRC11 enabled (default) 1= CR#_H controls SRC10

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M

Four Peaks

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Title: Clock Generator

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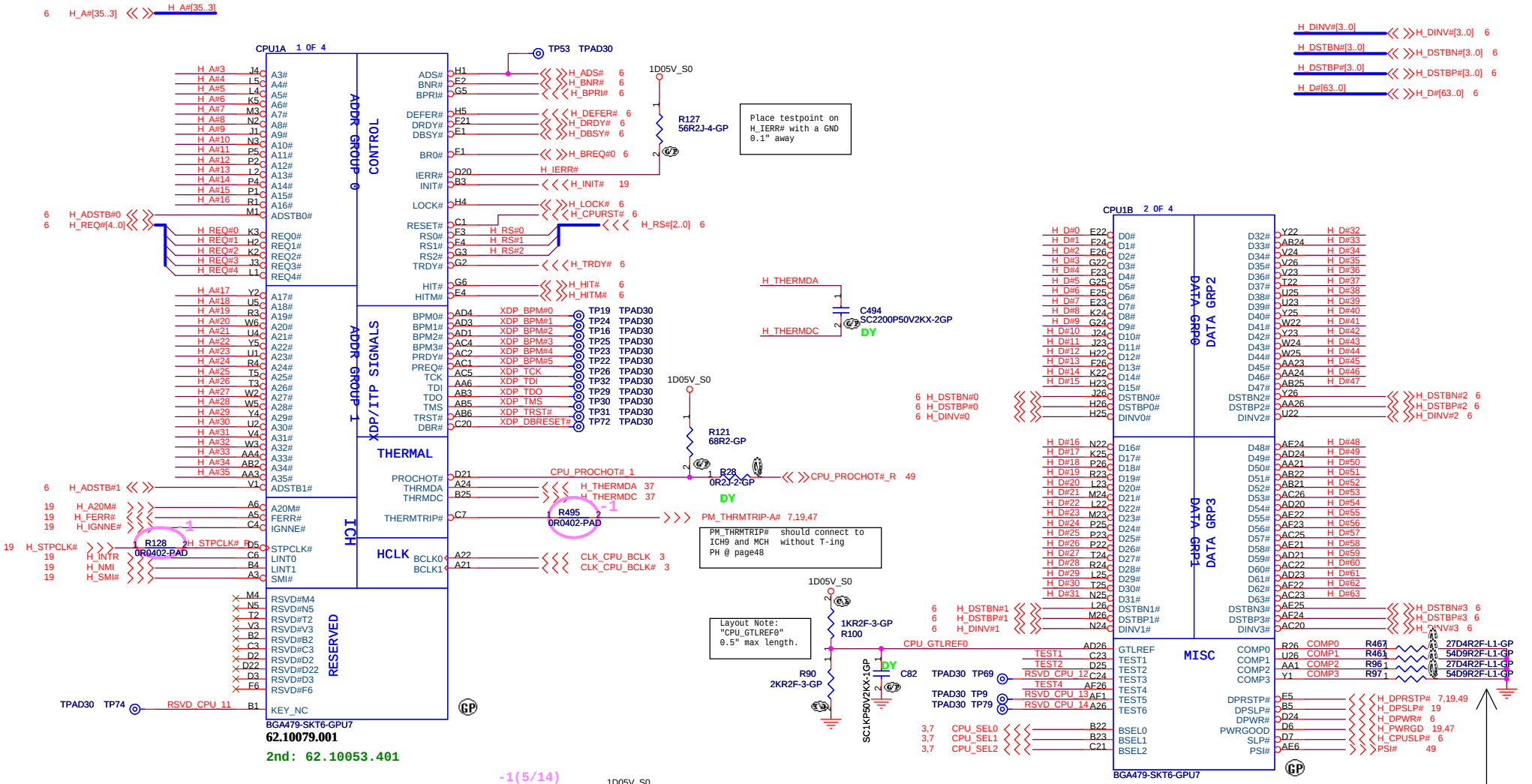

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Title	**CPU (1 of 2)**	
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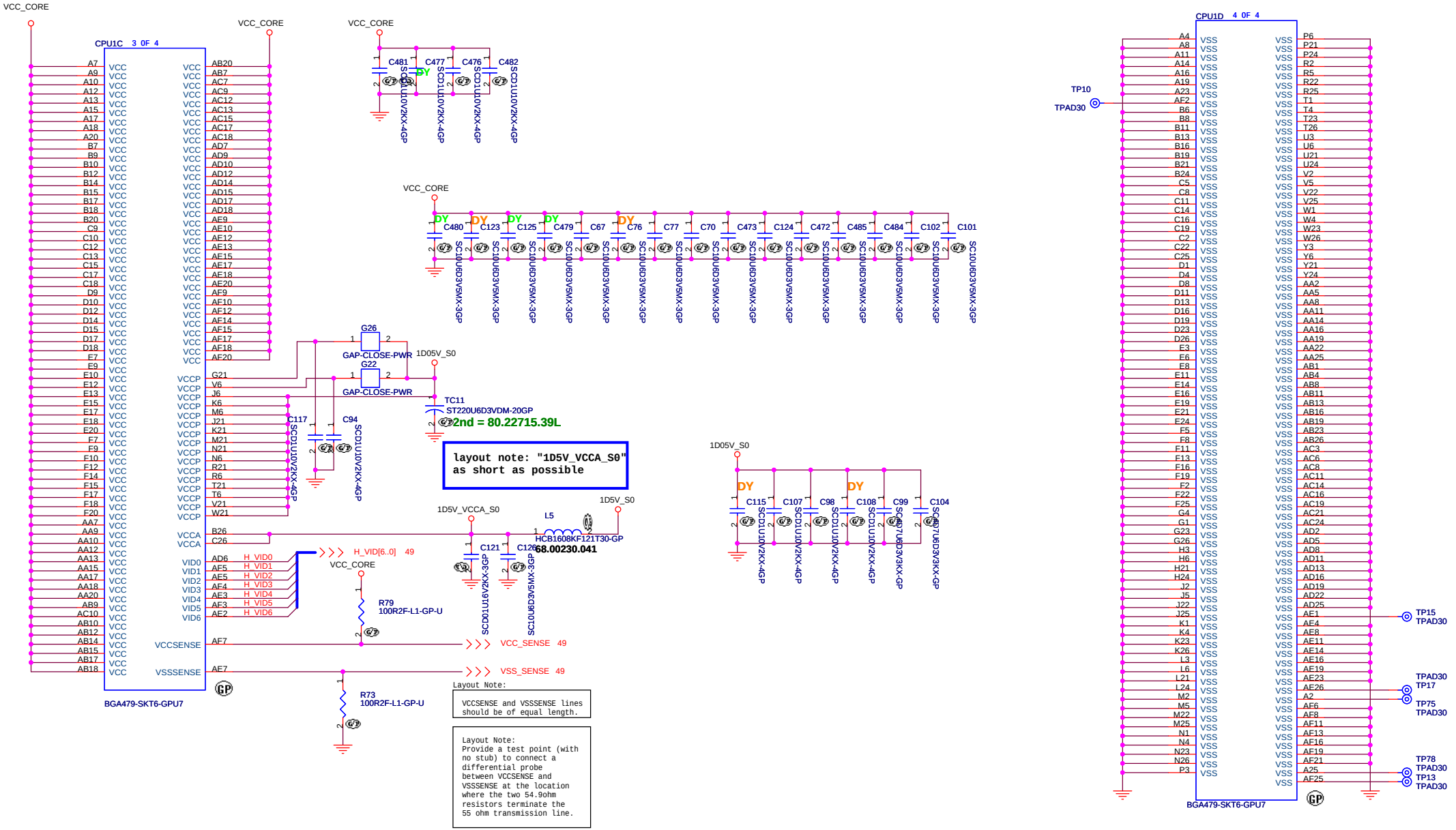

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Title	***CPU (2 of 2)***	
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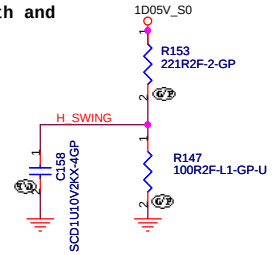
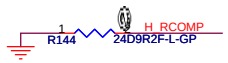
H_SWING routing Trace width and Spacing use 10 / 20 mil

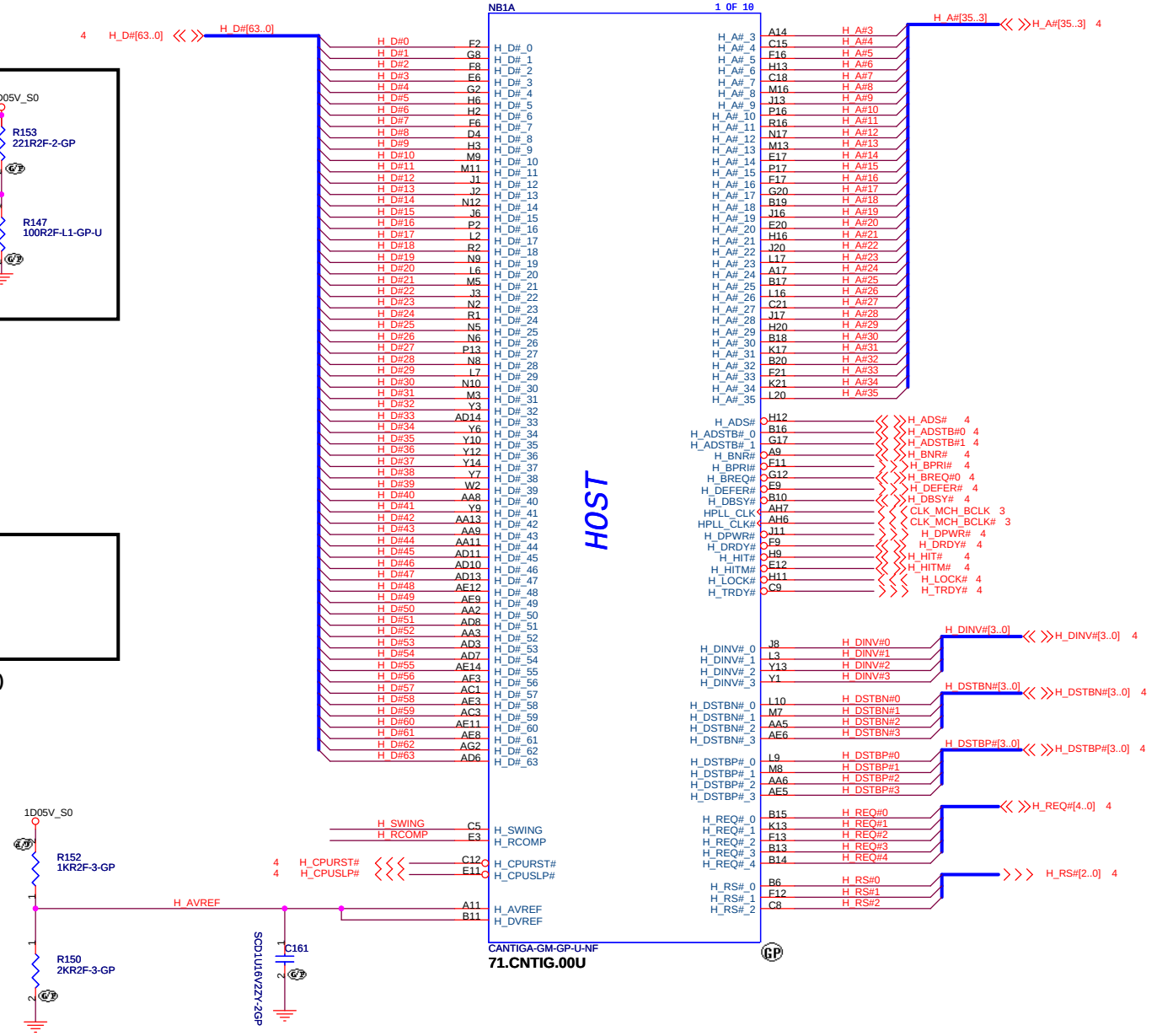
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")



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Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1067MHz 011 = FSB 667MHz 010 = FSB 800MHz Others = Reserved
CFG4:3; 8; 11; 14:15; 17; 18	Reserved
CFG5 (DMI select)	Low = DMI x 2 High = DMI x 4 *
CFG6 (ITPM Host Interface)	High = The ITPM Host Interface is disabled Low = The ITPM Host Interface is enabled *
CFG7 (Intel Management Engine Crypto Strap)	Low = Intel Management Engine Crypto Transport Layer Security (TLS) cipher site with no confidentiality High = Intel Management Engine Crypto TLS Cipher suite with confidentiality *
CFG9 (PCIE Graphics Lane)	Low = Reverse Lanes, 15->0, 14->1 etc... High = Normal operation:Lane Numbered in Order *
CFG10 (PCIE Loopback enable)	Low = Enabled High = Disabled *
CFG12 (ALLZ)	Low = ALLZ mode Enabled High = Disabled *
CFG13 (XOR)	Low = XOR mode Enabled High = Disabled *
CFG16 (FSB Dynamic ODT)	Low = Dynamic ODT Disabled High = Dynamic ODT Enabled *
CFG19 (DMI Lane Reversal)	Low = Noraml operation: Lane Numbered in Order * High = Reverse Lanes DMI x 4 mode[MCH->ICH]: (0->3, 2->1, 1->2 and 0->3) DMI x 2 mode[MCH->ICH]: (3->0, 2->1)
CFG20 (Digital Display Port (SDVO/DP /iHDMI) Concurrent with PCIE)	Low = Only Digital Display Port (SDVO/iHDMI) or PCIE is operational * High = Digital Display Port (SDVO/DP/iHDMI) and PCIE are operating simulatneously via the PEG port
SDVO_CTRLDATA (SDVO Present)	Low = No SDVO Card Present * High = SDVO Card Present
L_DDC_DATA (Local Flat Panel (LFP) Present)	Low = LFP Disabled * High = LFP Card Present; PCIE disabled
DDPC_CTRLDATA (Digital Display Present)	Low = DisplayPort Disabled * High = DisplayPort Device Present

Close to GMCH as 500 mils.

CRT_IREF routing Trace width use 20 mil

FOR Cantiga: 1.02k_1% ohm
Teenah: 1.3k ohm

for HDMI port C

FOR Cantiga:500 ohm
Teenah: 392 ohm

layout take note

FOR Discrete,change to 0 ohm
63.R0034.1DL

CANTIGA-GM-GP-U-NF
71.CNTIG.00U

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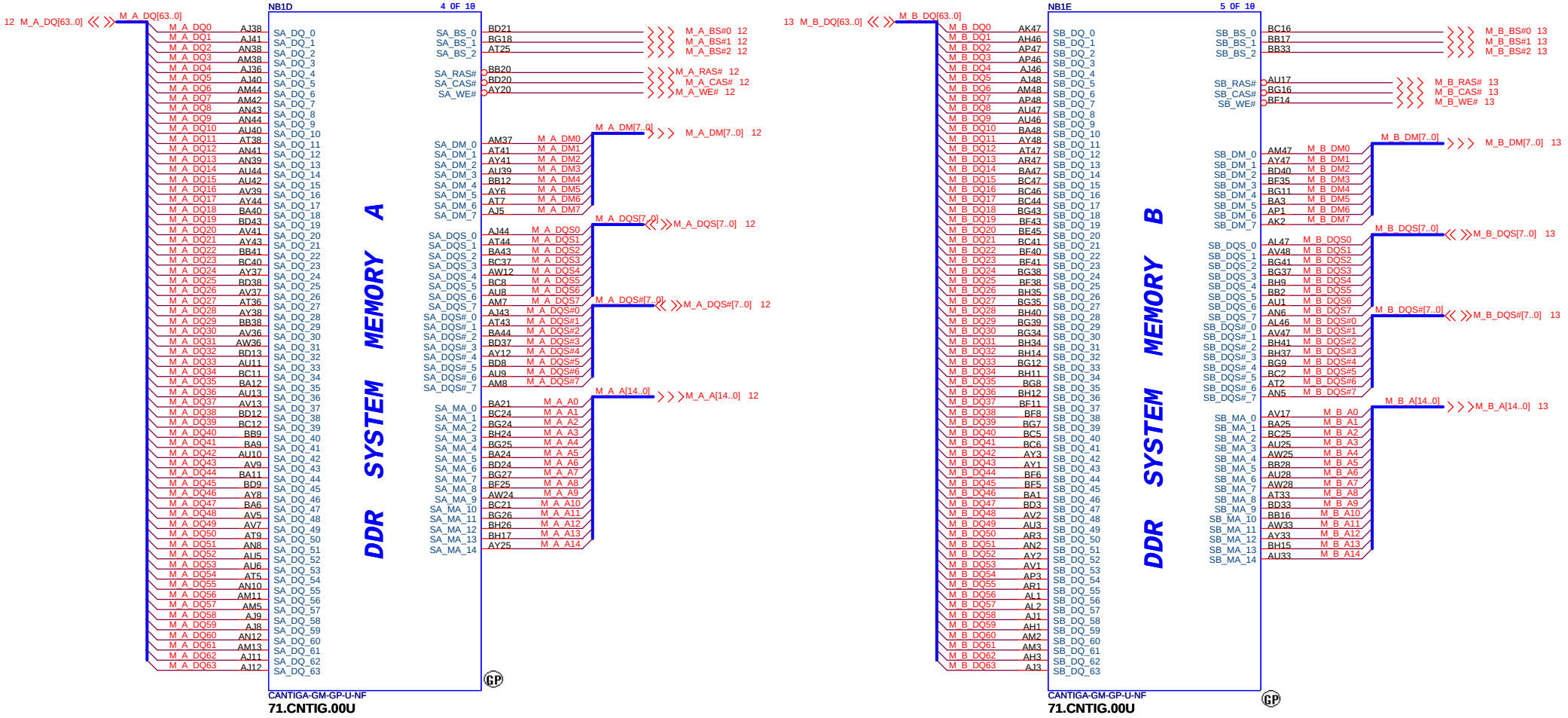

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Title: Cantiga (3 of 6)

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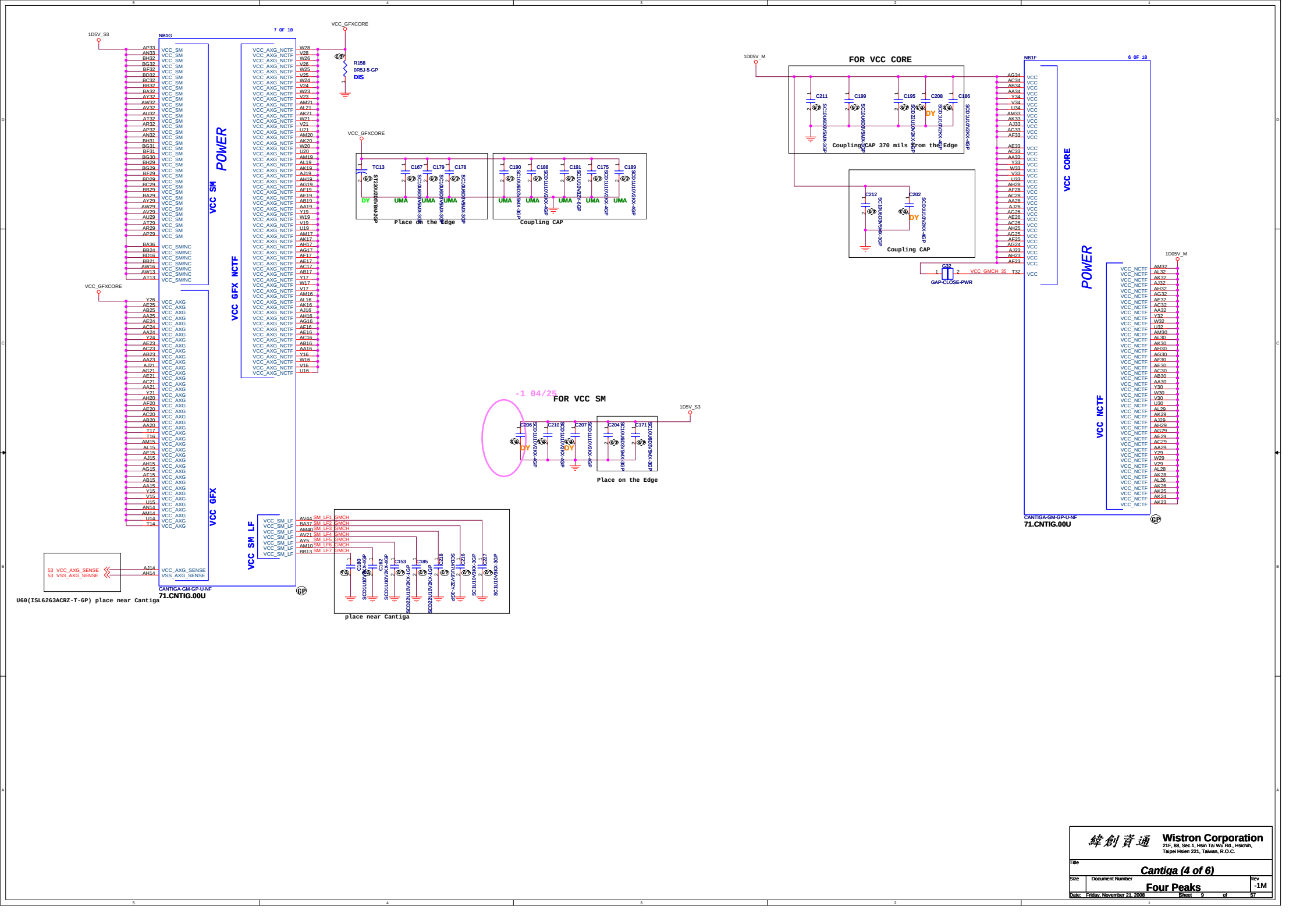

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Title: Cantiga (4 of 6)	
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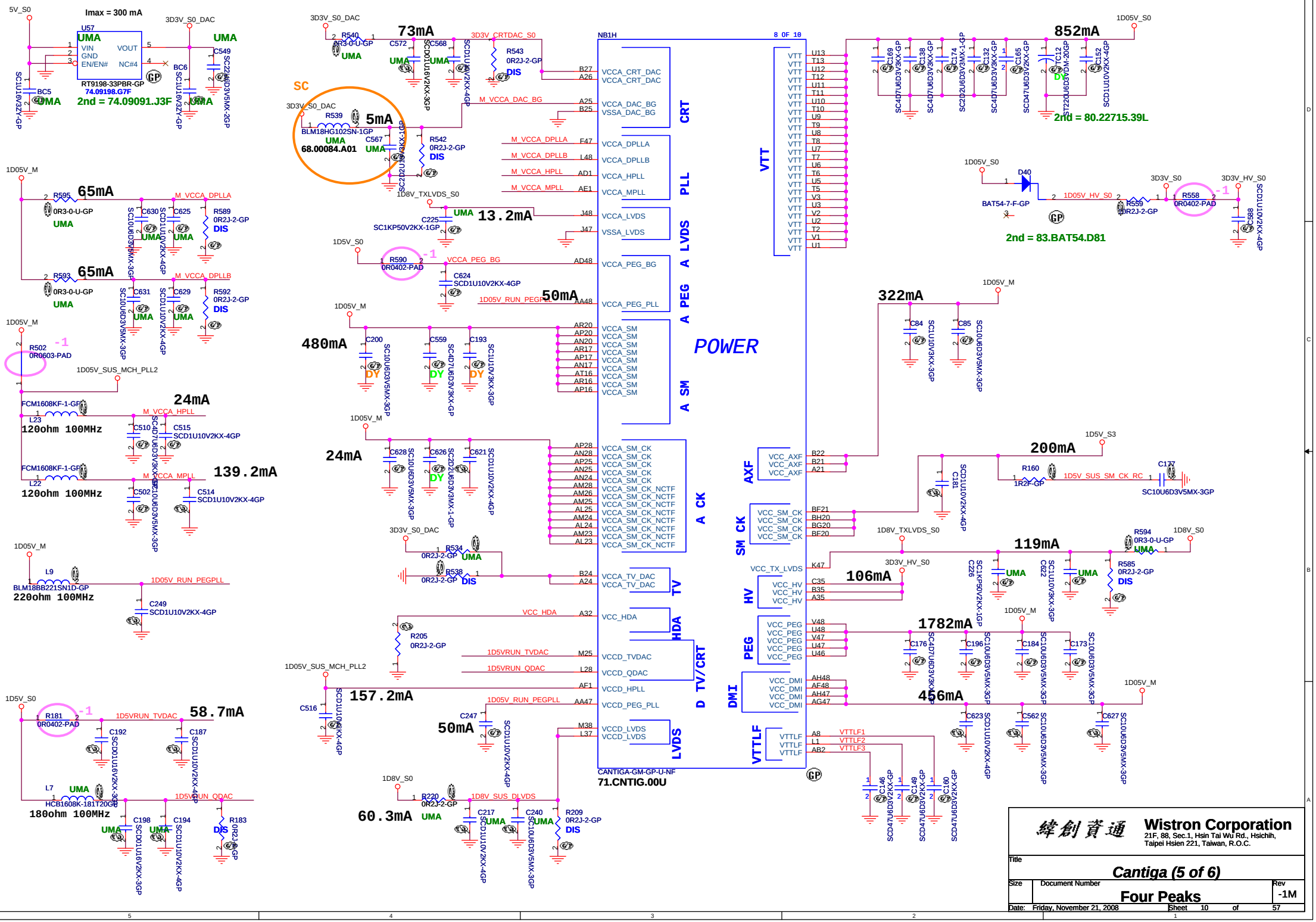
Imax = 300 mA
U57
RT9198-33PBR-GP
74.09198.G7F
2nd = 74.09091.J3F
73mA
5mA
68.00084.A01
13.2mA
65mA
65mA
24mA
120ohm 100MHz
139.2mA
120ohm 100MHz
480mA
50mA
24mA
157.2mA
50mA
60.3mA
322mA
200mA
119mA
106mA
1782mA
456mA
852mA
2nd = 80.22715.39L
2nd = 83.BAT54.D81
58.7mA
180ohm 100MHz
NB1H
CRT
PLL
A LVDS
A PEG
A SM
A CK
TV
HDA
D TV/CRT
LVDS
AXF
SM CK
HV
PEG
DMI
VTTLF
VTT
8 OF 10
POWER
CANTIGA-GM-GP-U-NF
71.CNTIG.00U
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Title
Cantiga (5 of 6)
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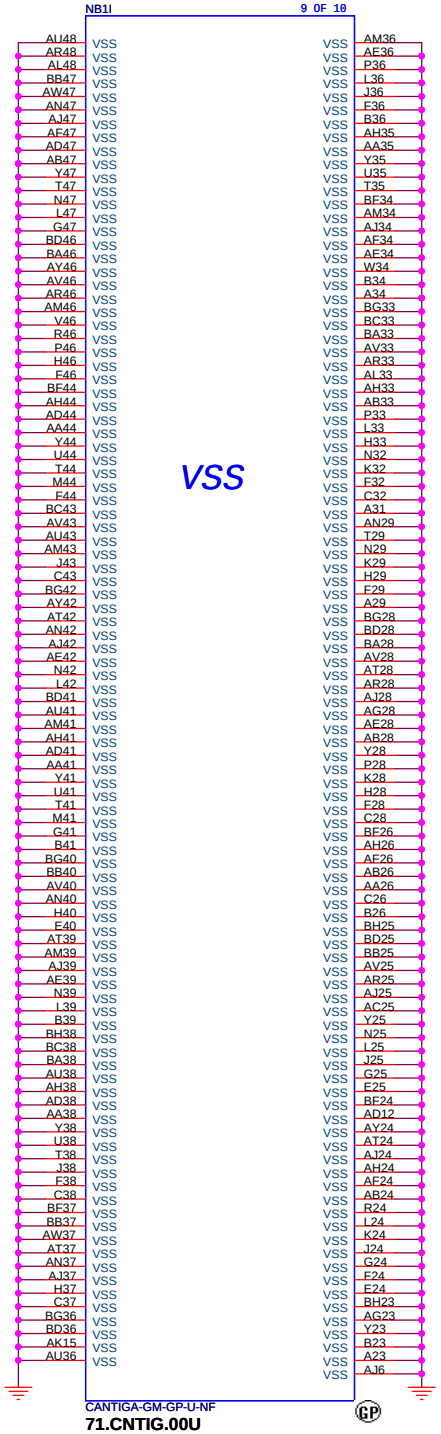

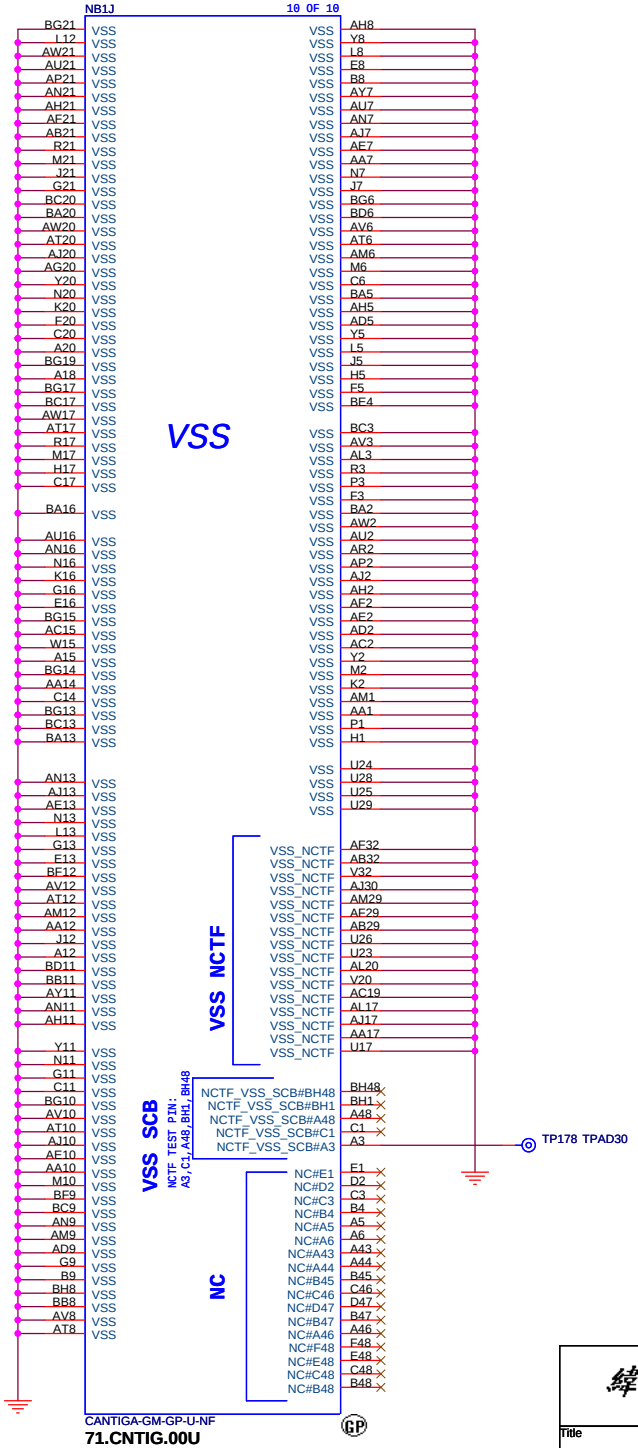

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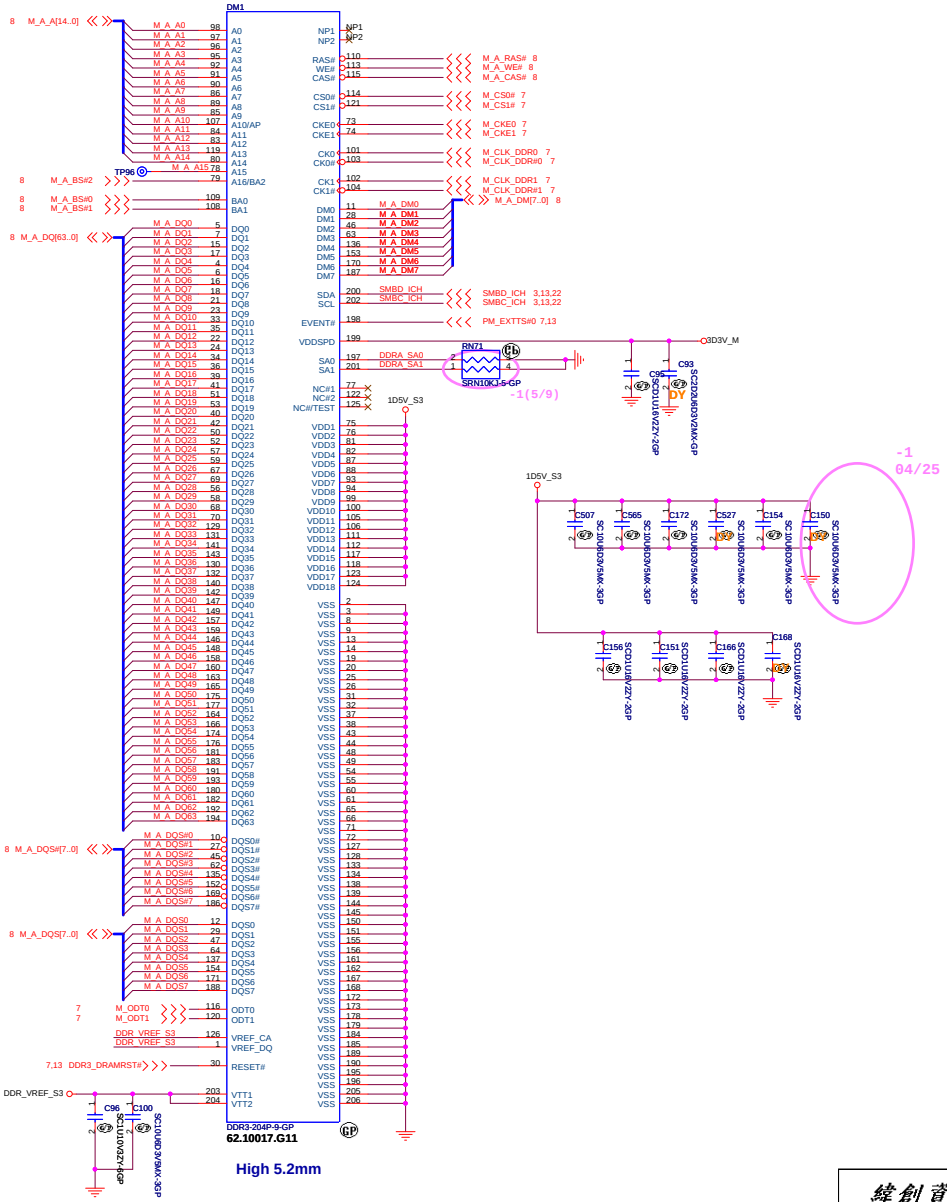
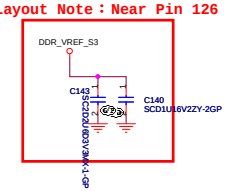
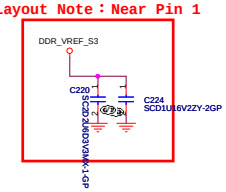
DDR3 SOCKET_1



Layout Note：Near Pin 126



Layout Note：Near Pin 1



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Title: DDR3 Socket			
Size	Document Number: Four Peaks	Rev: -1M	
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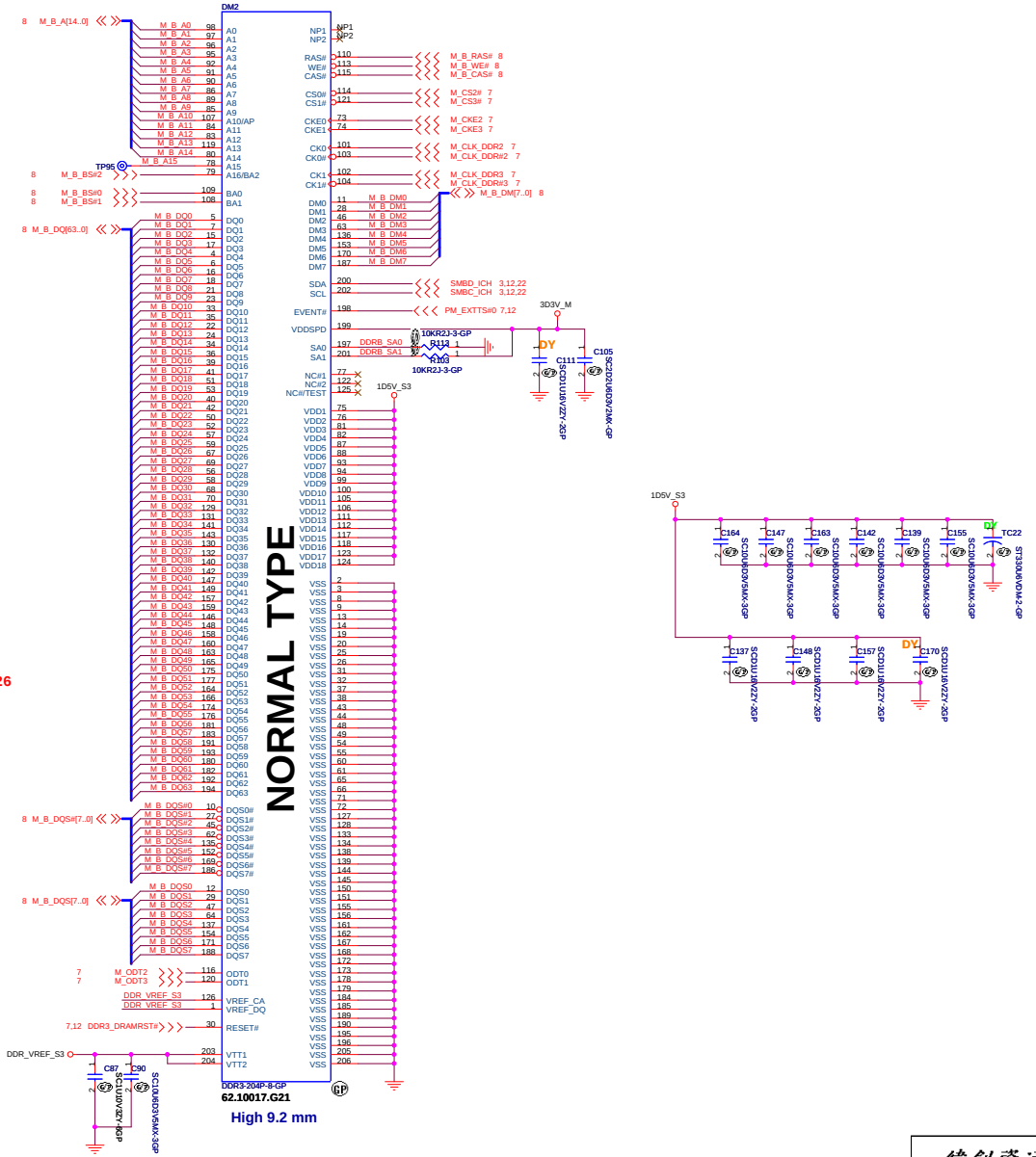
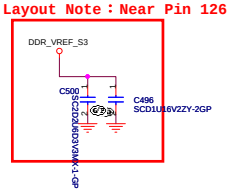
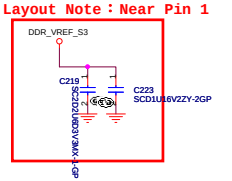
DDR3 SOCKET_2



Layout Note：Near Pin 126



Layout Note：Near Pin 1



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Title: DDR3 Termination Resistor			
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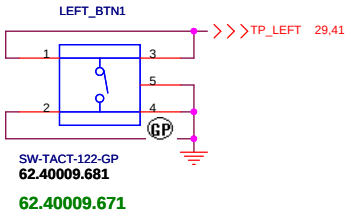
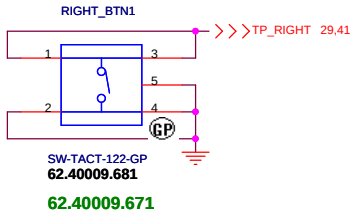
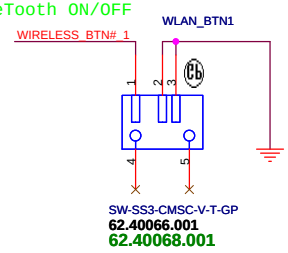


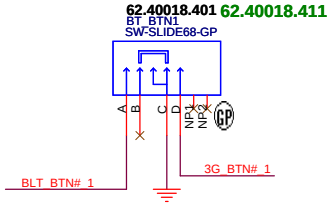


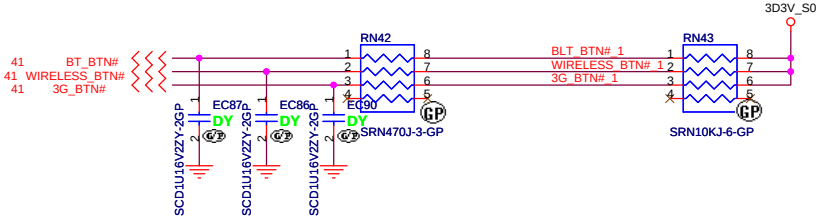
BlueTooth ON/OFF



Wireless ON/OFF

Check Wireless Button left or right





Four Peaks

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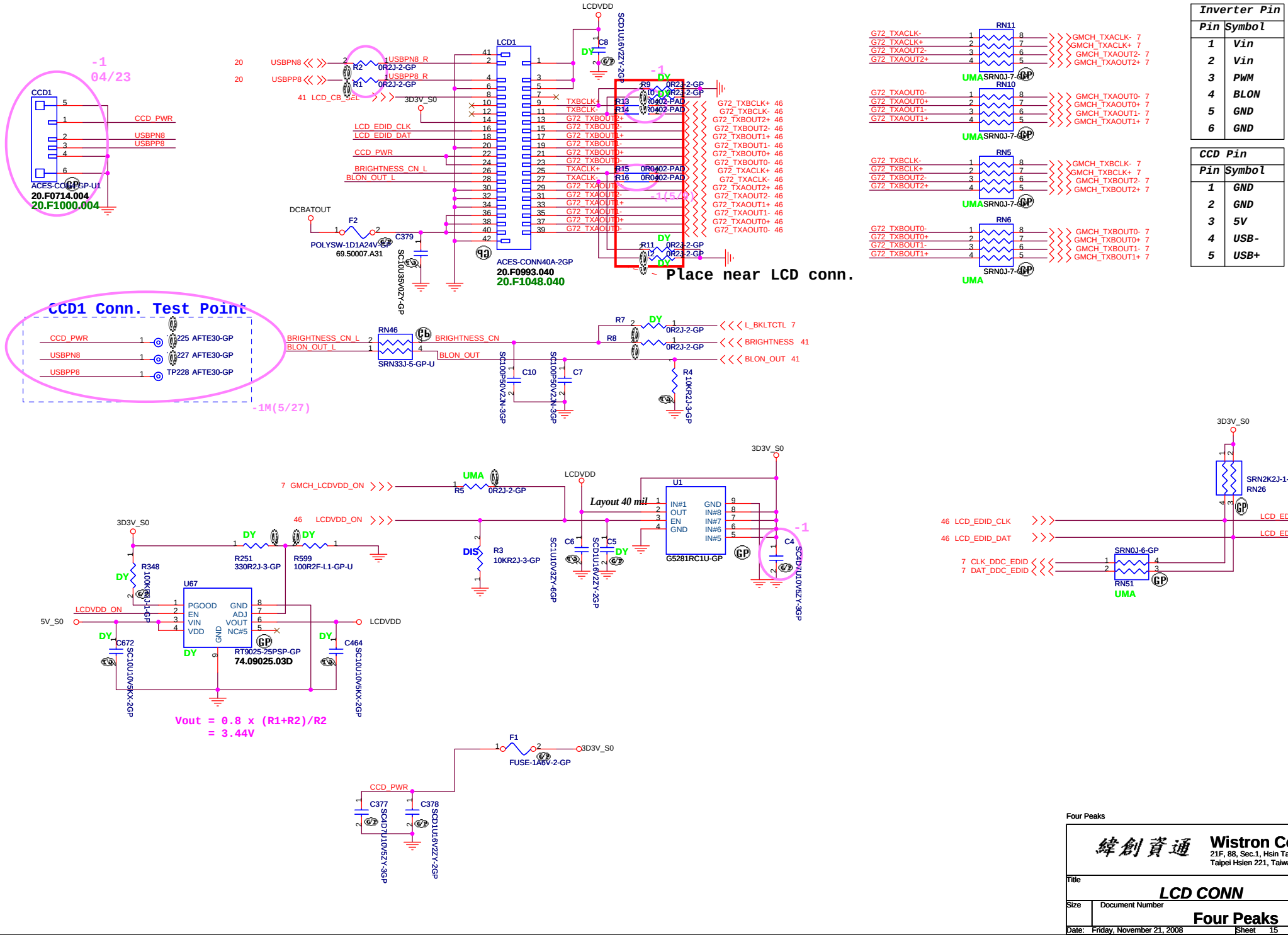
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***SWITCH / Button***

Size | Document Number: **Four Peaks** | Rev: -1M

Date: Friday, November 21, 2008 | Sheet 14 of 57

LCD/INVERTER/CCD CONN



Four Peaks

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **LCD CONN**

Size	Document Number	Rev
	Four Peaks	-1M

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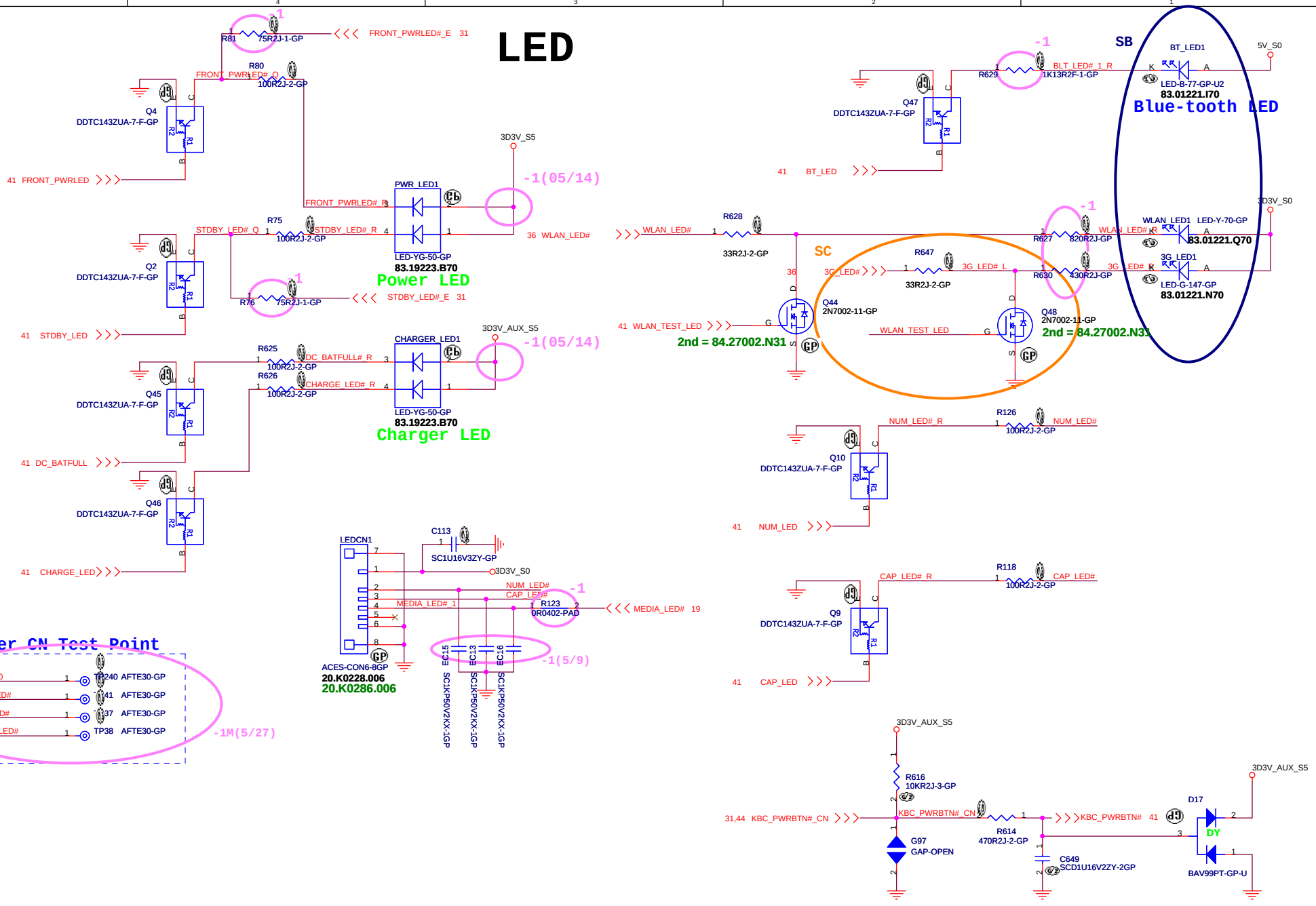
LED



Four Peaks

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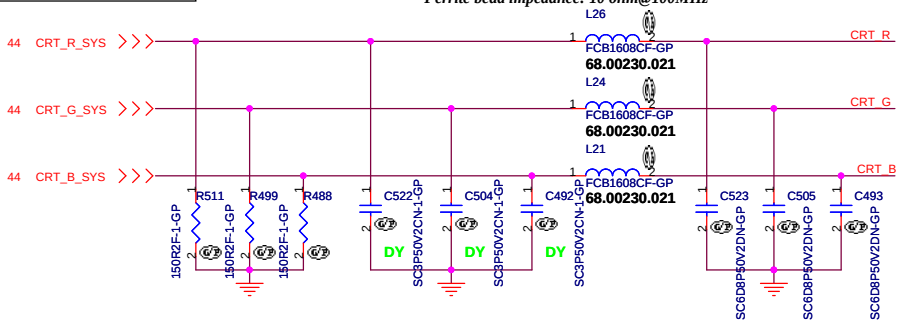
Taipei Hsien 221, Taiwan, R.O.C.

Title	***LED&POWERBD CONN***	
Size	Document Number: **Four Peaks**	Rev: -1M
Date: Friday, November 21, 2008	Sheet 16 of 57	

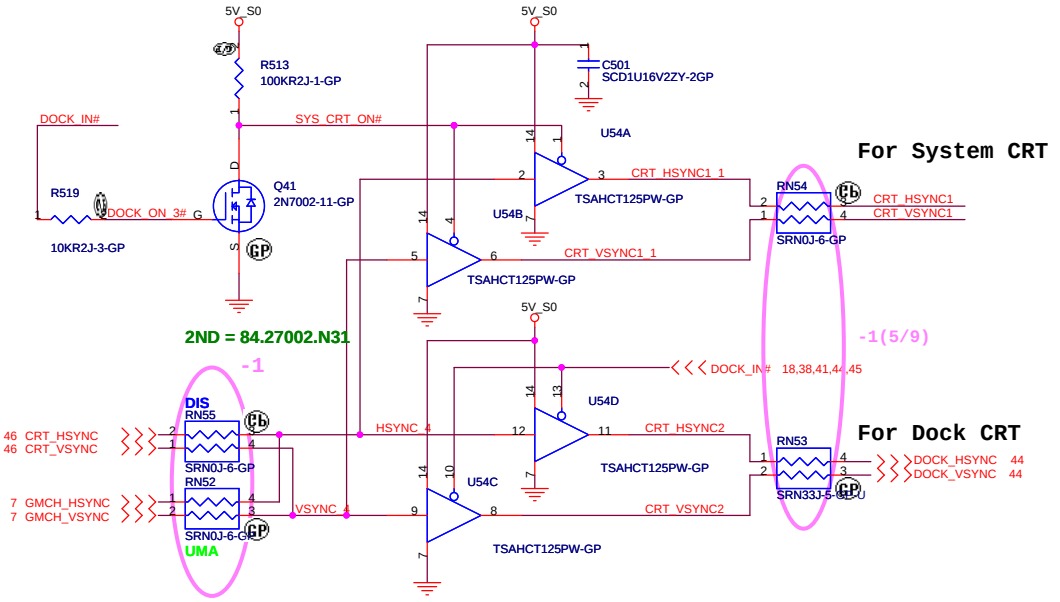
Layout Note:
Place these resistors close to the CRT-out connector

Ferrite bead impedance: 10 ohm@100MHz



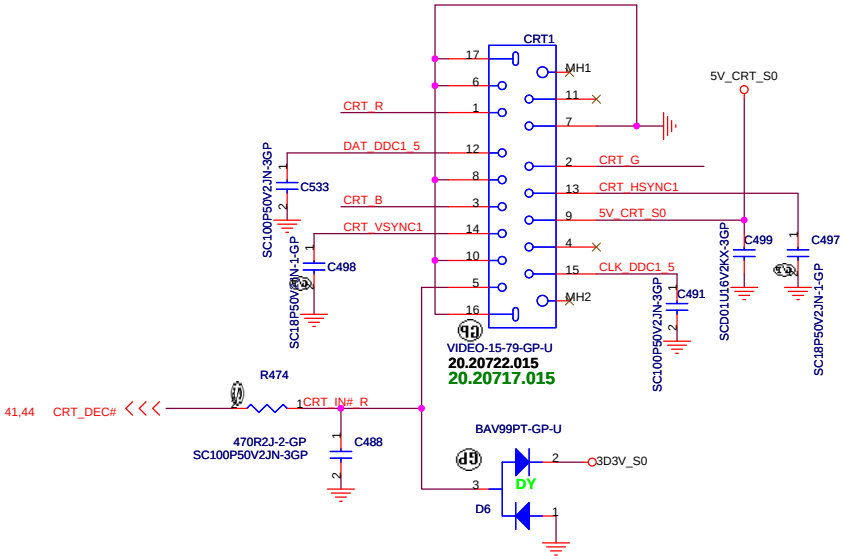
Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift

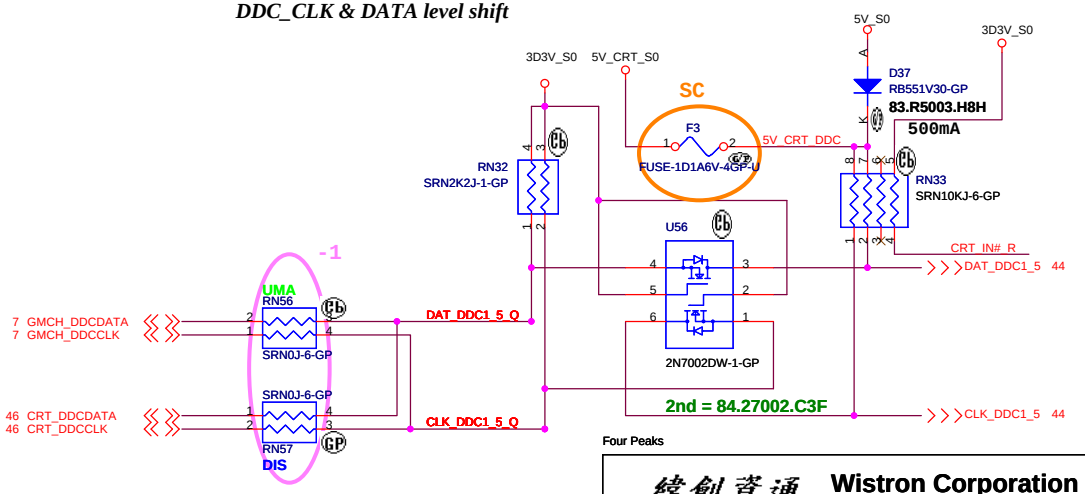


Function	DOCK_CRT_SEL#
SYSTEM	H
DOCK	L

CRT I/F & CONNECTOR



DDC_CLK & DATA level shift



6 1 7 2 8 3 9 4 10 5

Four Peaks

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Title: **CRT CONN**

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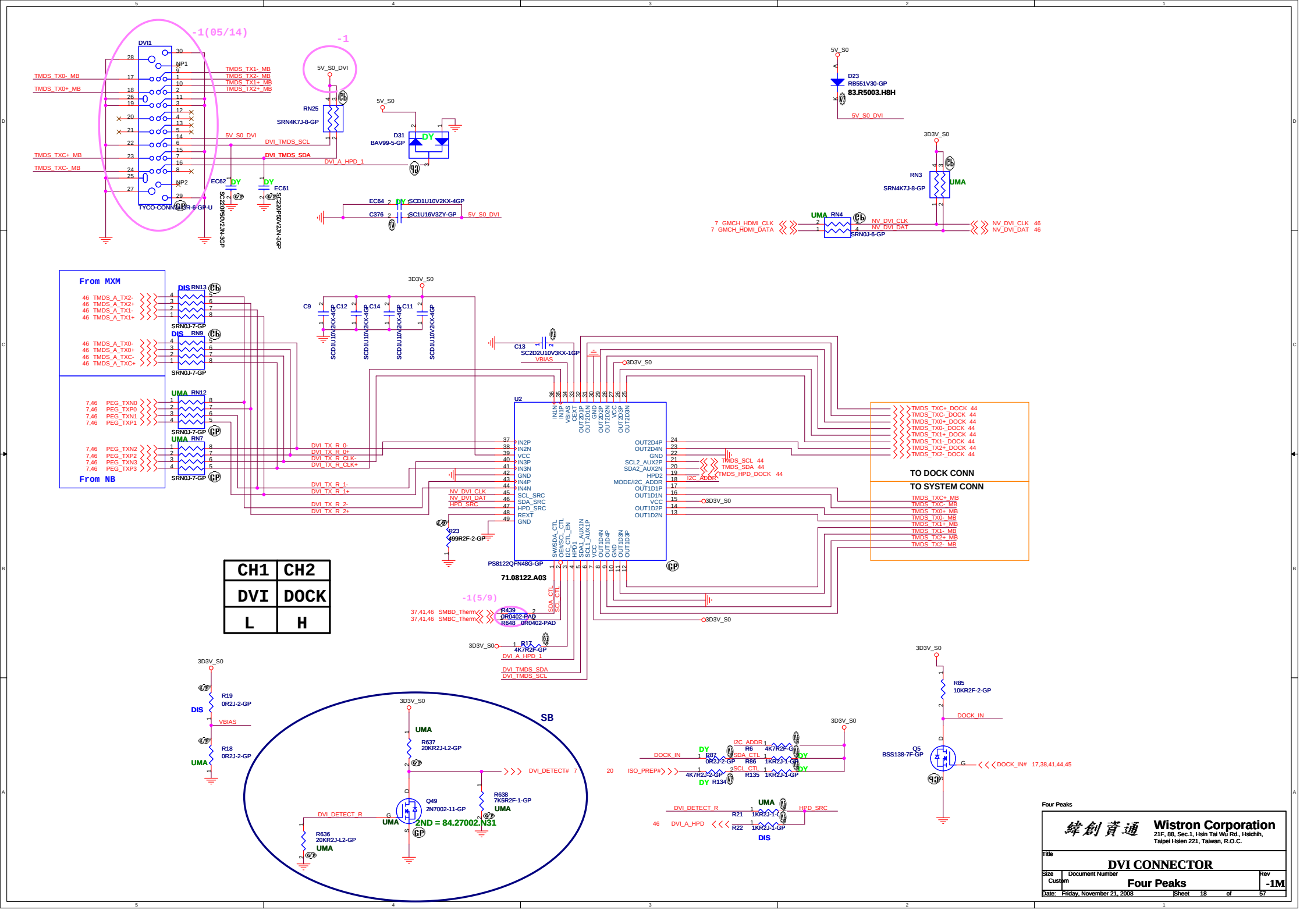

Four Peaks

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Title: DVI CONNECTOR

Size: Custom | Document Number: Four Peaks | Rev: -1M

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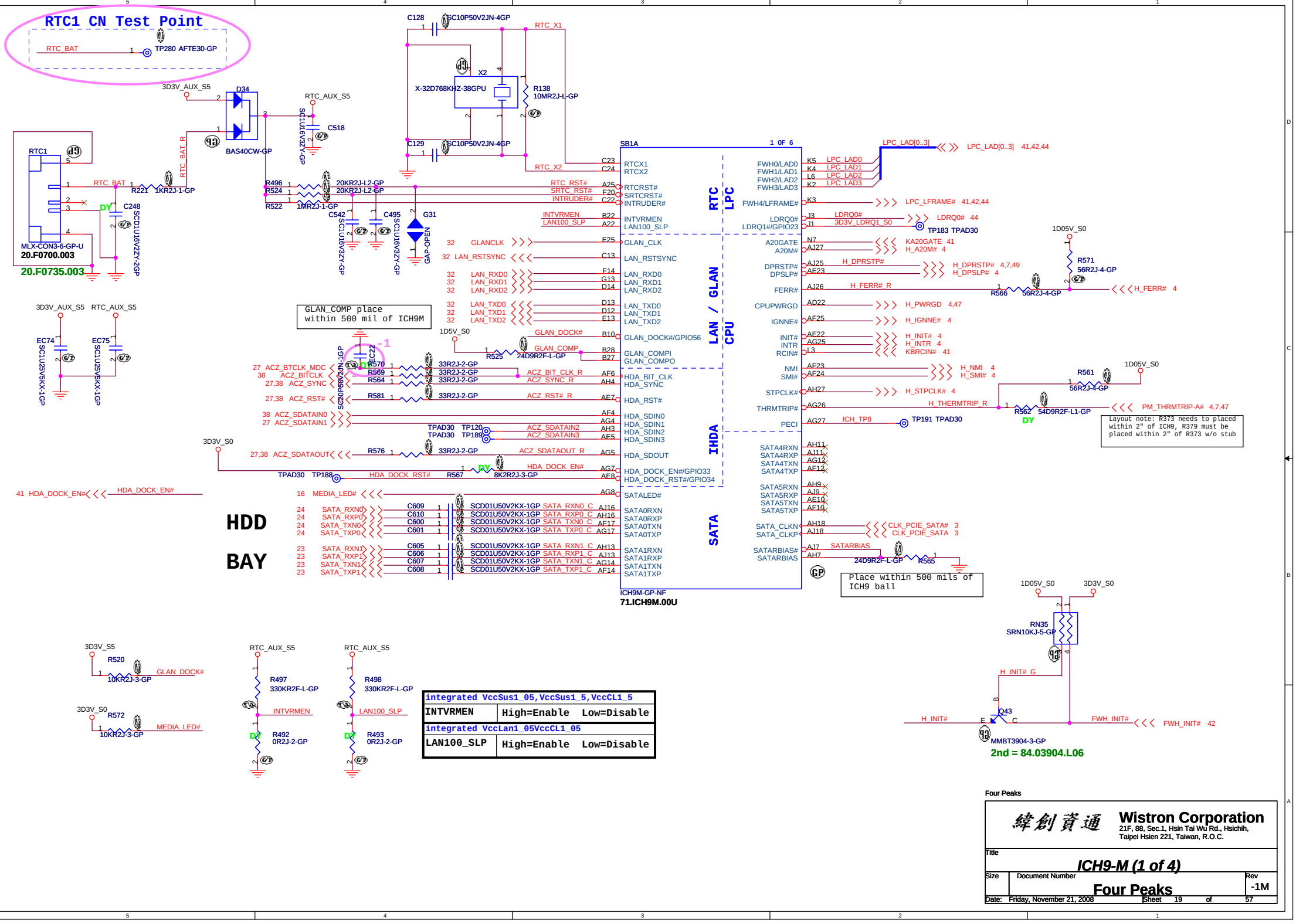

Four Peaks

Wistron Corporation
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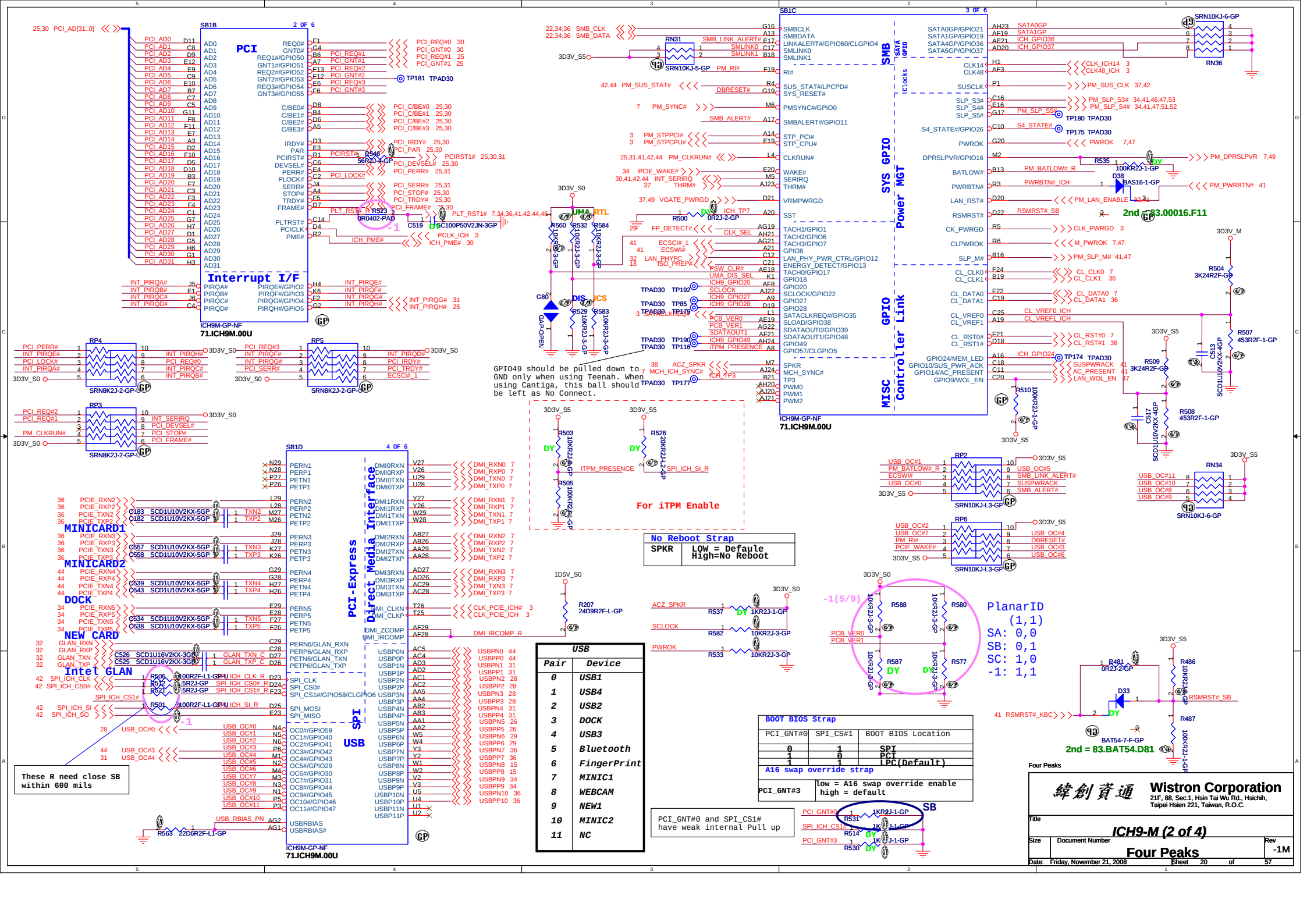
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH9-M (1 of 4)

Size	Document Number	Rev
	Four Peaks	-1M

Date: Friday, November 21, 2008 Sheet 19 of 57


SB1B 2 OF 6
PCI
Interrupt I/F
ICH9M-GP-NF
71.ICH9M.00U
SB1C 3 OF 6
SMB
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
ICH9M-GP-NF
71.ICH9M.00U
SB1D 4 OF 6
PCI-Express
Direct Media Interface
SPI
USB
ICH9M-GP-NF
71.ICH9M.00U
GPIO49 should be pulled down to GND only when using Teenah. When using Cantiga, this ball should be left as No Connect.
For iTPM Enable
No Reboot Strap
SPKR LOW = Defaule High=No Reboot
USB
Pair Device
0 USB1
1 USB4
2 USB2
3 DOCK
4 USB3
5 Bluetooth
6 FingerPrint
7 MINIC1
8 WEBCAM
9 NEW1
10 MINIC2
11 NC
BOOT BIOS Strap
PCI_GNT#0 SPI_CS#1 BOOT BIOS Location
0 1 SPI
1 0 PCI
1 1 LPC(Default)
A16 swap override strap
PCI_GNT#3 low = A16 swap override enable high = default
PCI_GNT#0 and SPI_CS1# have weak internal Pull up
These R need close SB within 600 mils
PlanarID (1,1)
SA: 0,0
SB: 0,1
SC: 1,0
-1: 1,1
2nd = 83.00016.F11
2nd = 83.BAT54.D81
Four Peaks
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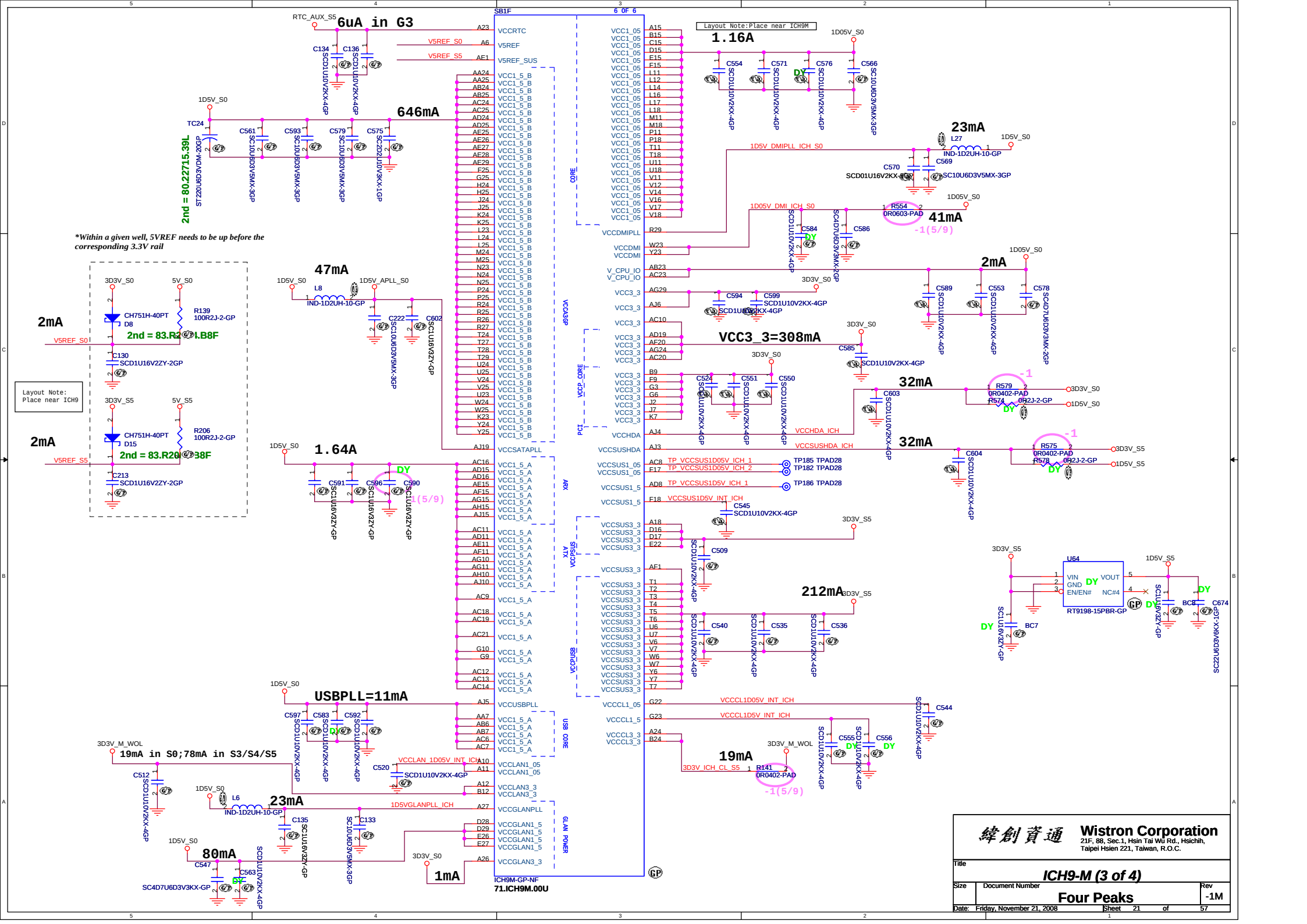
Title
ICH9-M (2 of 4)
Size
Document Number
Four Peaks
Rev
-1M
Date: Friday, November 21, 2008
Sheet 20 of 57


SB1F
6 OF 6
ICH9M-GP-NF
71.ICH9M.00U
6uA in G3
646mA
2nd = 80.22715.39L
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
2mA
47mA
1.64A
USBPLL=11mA
19mA in S0;78mA in S3/S4/S5
23mA
80mA
1mA
1.16A
23mA
41mA
2mA
VCC3_3=308mA
32mA
32mA
212mA
19mA
Layout Note:Place near ICH9M
Layout Note: Place near ICH9
Wistron Corporation
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ICH9-M (3 of 4)
Four Peaks
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Friday, November 21, 2008
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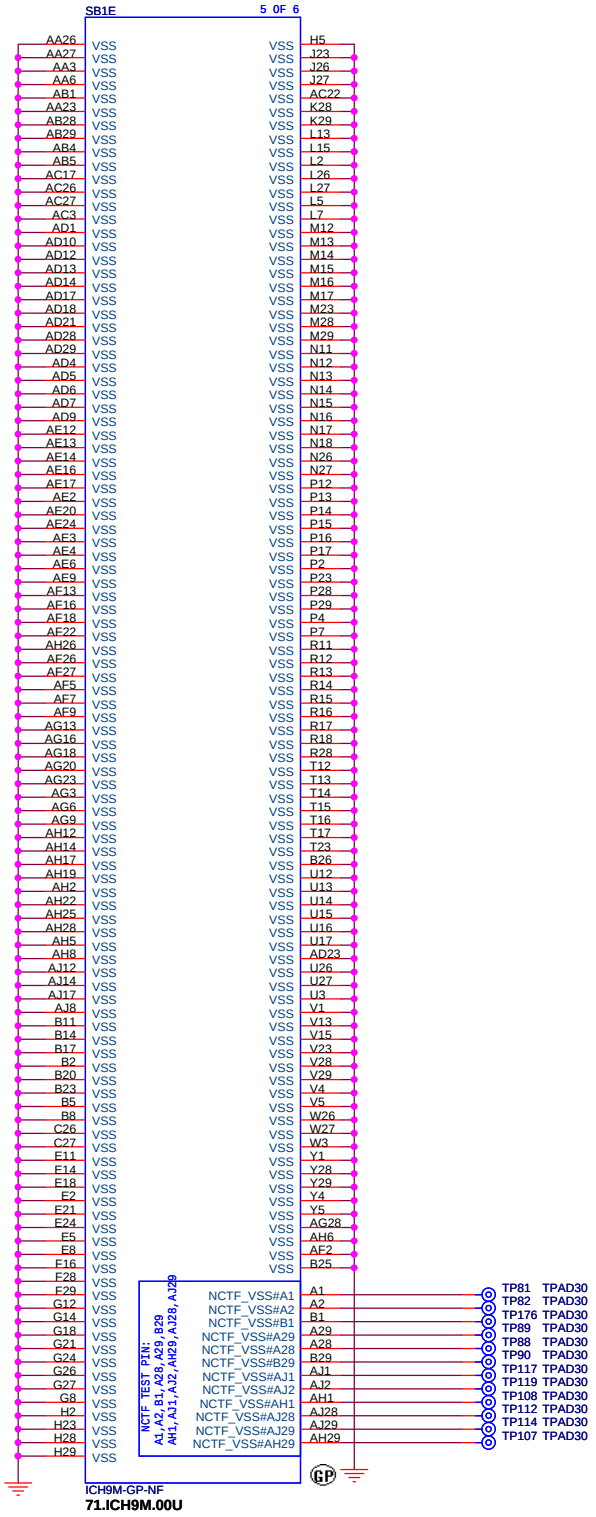

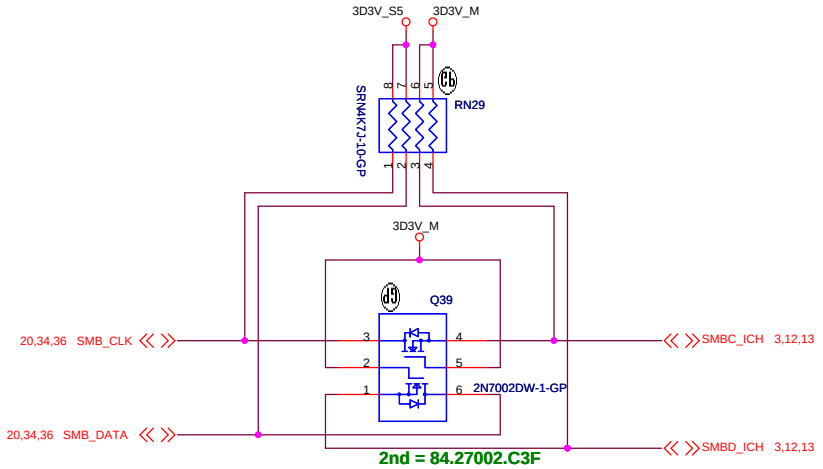

緯創資通 **Wistron Corporation**
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Title: *ICH9-M (4 of 4)*

Size | Document Number: **Four Peaks** | Rev: -1M

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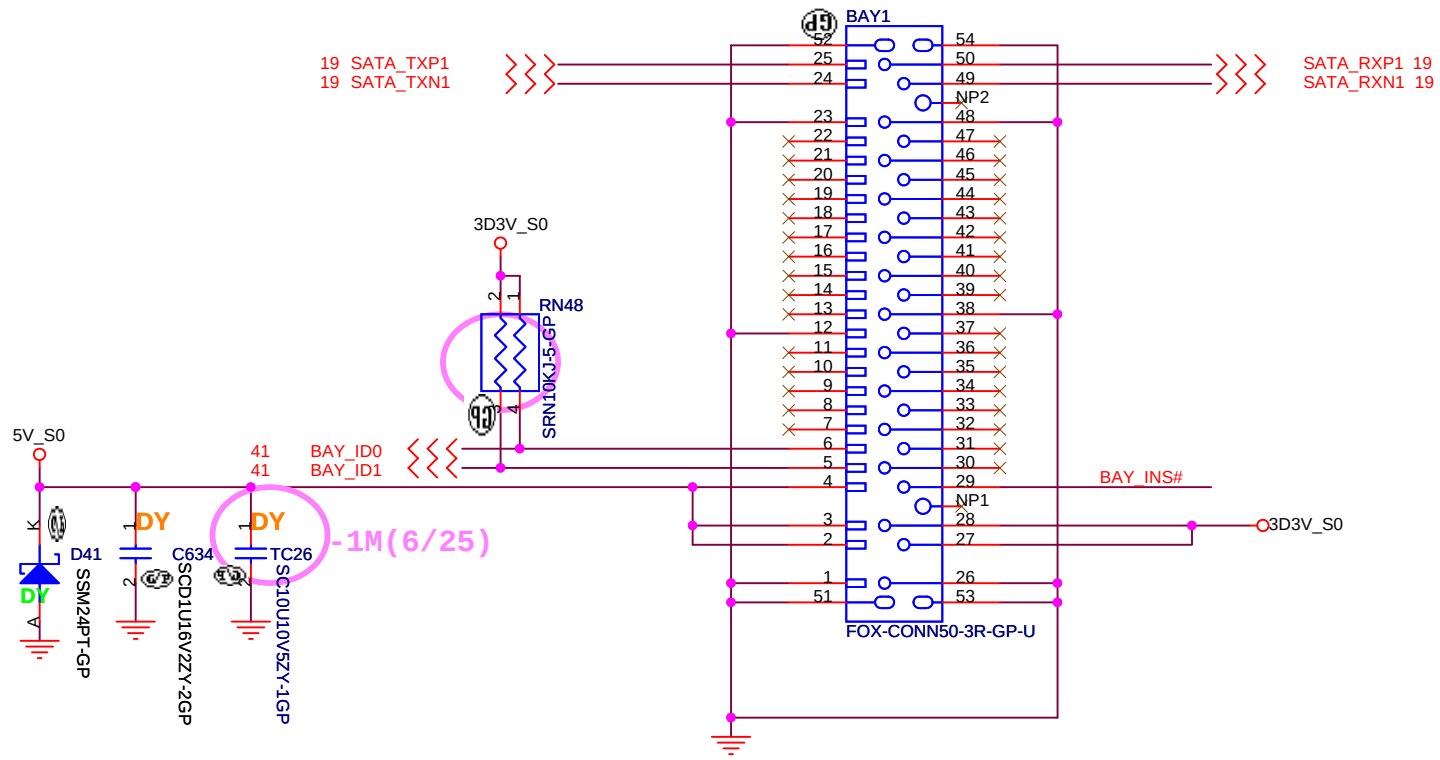
ODD Connector

ODD Conn. Test Point

SATA_TXP1	TP125 TPAD30
SATA_TXN1	TP124 TPAD30
SATA_RXP1	TP127 TPAD30
SATA_RXN1	TP126 TPAD30
BAY_ID0	TP194 TPAD30
BAY_ID1	TP195 TPAD30
BAY_INS#	TP193 TPAD30
3D3V_S0	TP277 TPAD30
5V_S0	TP278 TPAD30



	BAY_ID0	BAY_ID1
SATA ODD	0	0
SATA HDD	1	1

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Title: ODD

Size	Document Number	Rev
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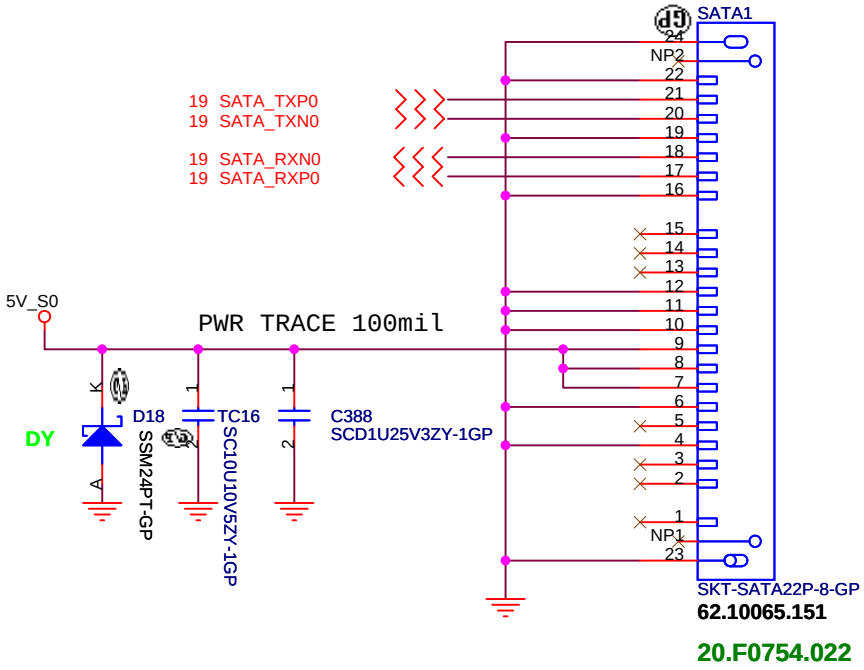
SATA Connector



HDD Conn. Test Point

Four Peaks

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Title	***HDD CONN***	
Size	Document Number **Four Peaks**	Rev -1M
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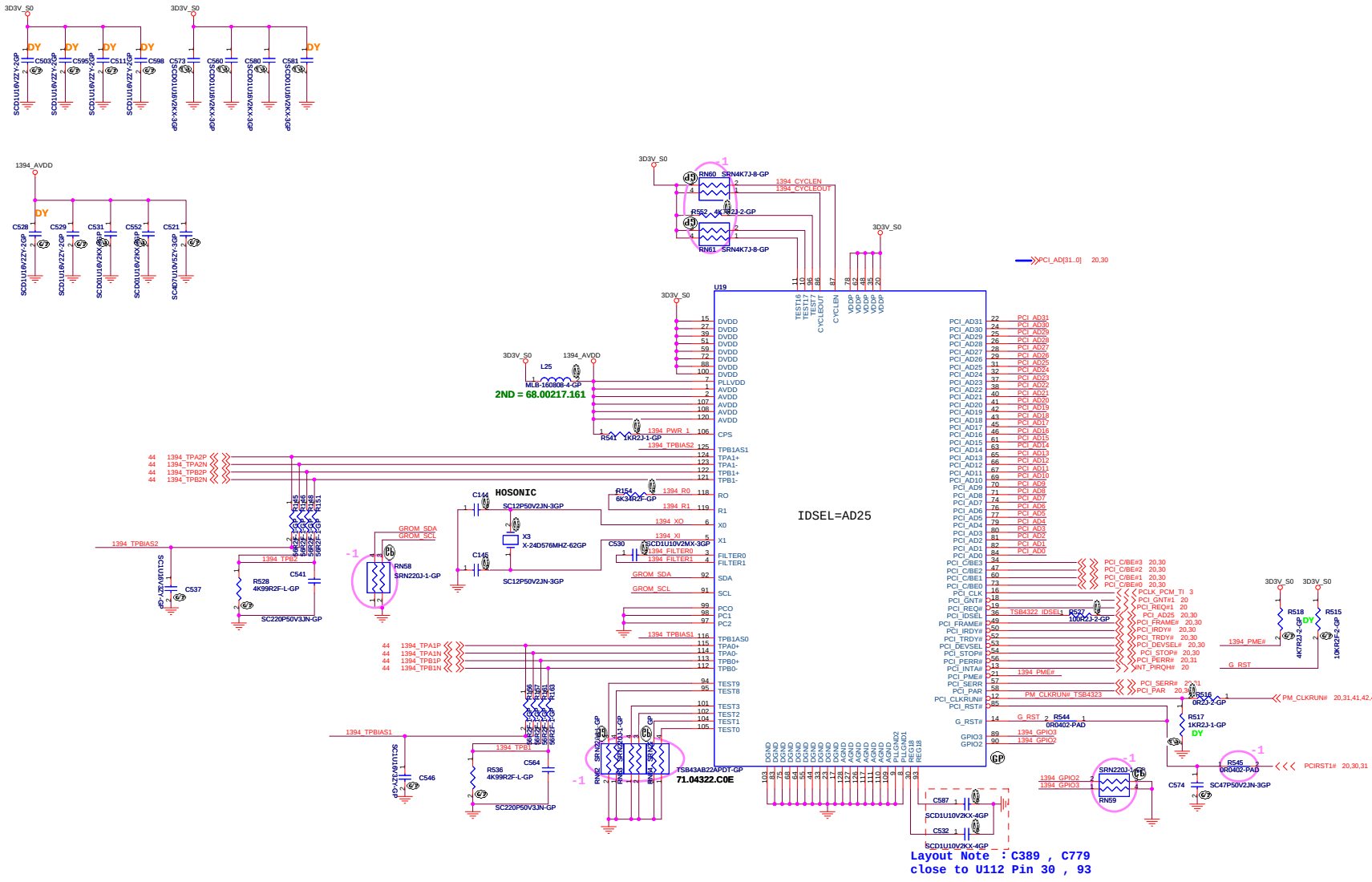

Four Peaks

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Title: *TSB43AB22A*

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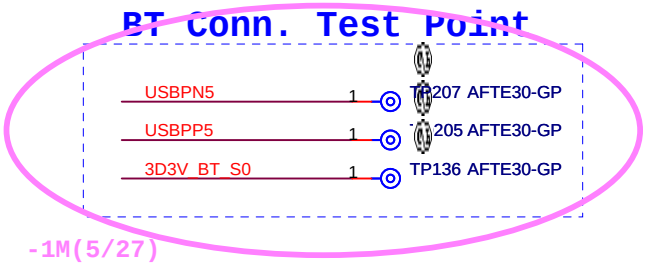
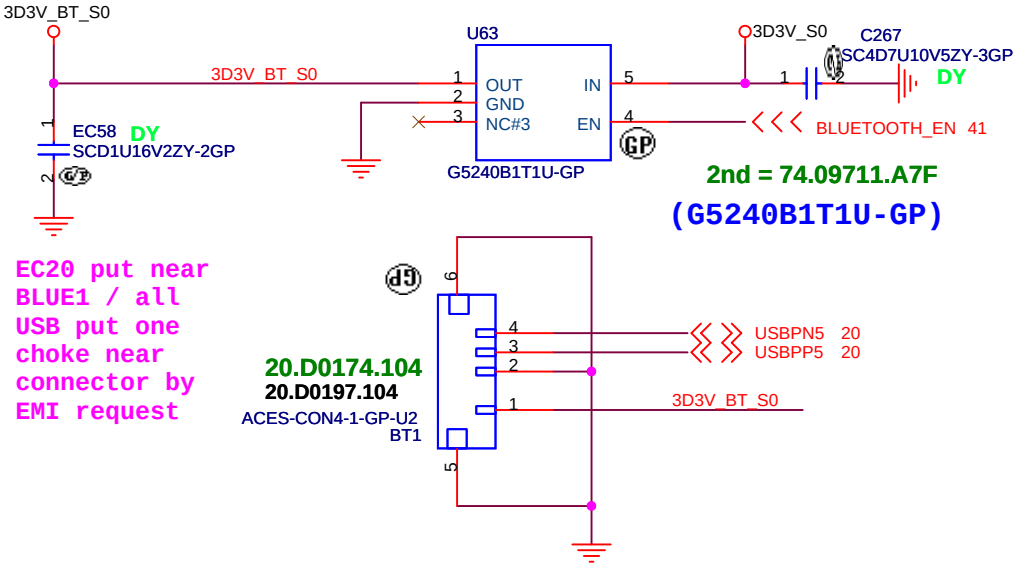
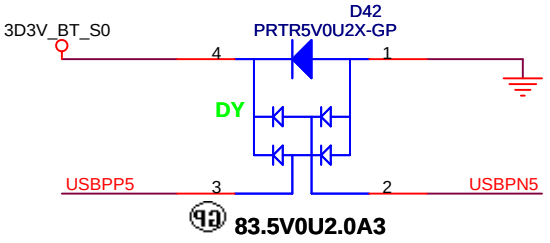
BLUETOOTH MODULE







Need check conn.

Four Peaks

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***BLUETOOTH***		
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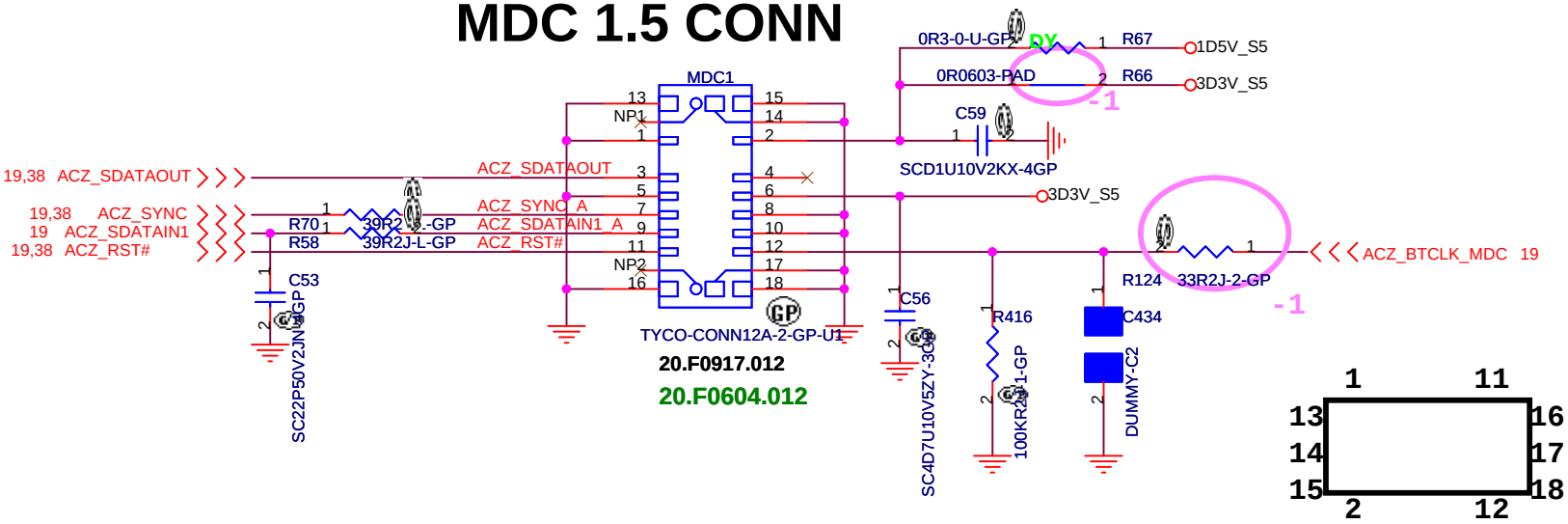
MDC 1.5 CONN



Four Peaks

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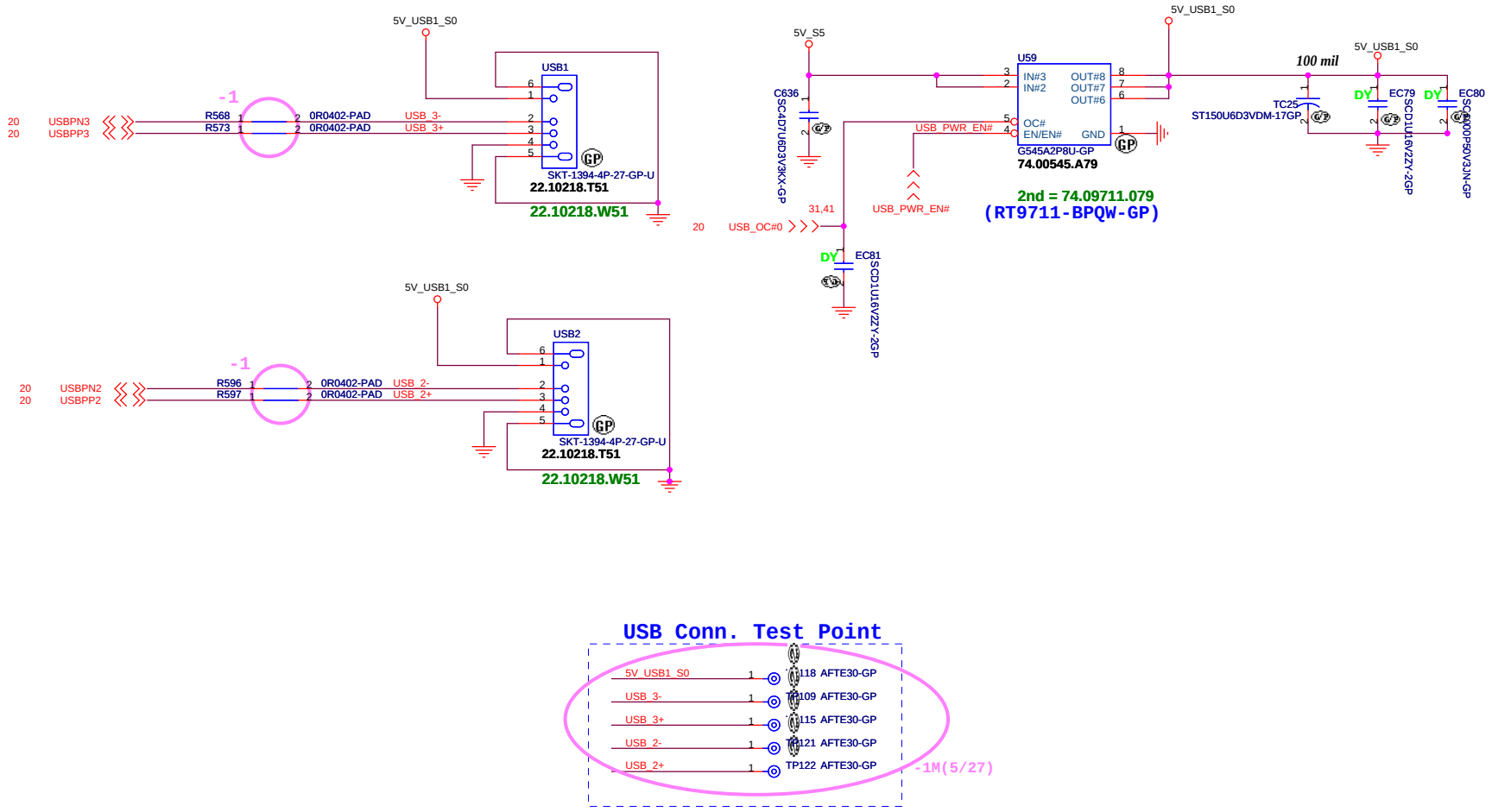
Title	***MDC***	
Size	Document Number **Four Peaks**	Rev -1M
Date: Friday, November 21, 2008	Sheet 27 of	57



USB Conn. Test Point

Four Peaks

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *USB*

Size	Document Number	Rev
	Four Peaks	-1M

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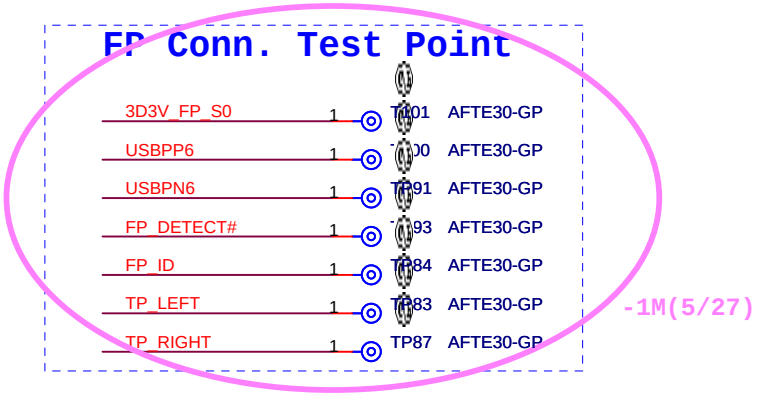
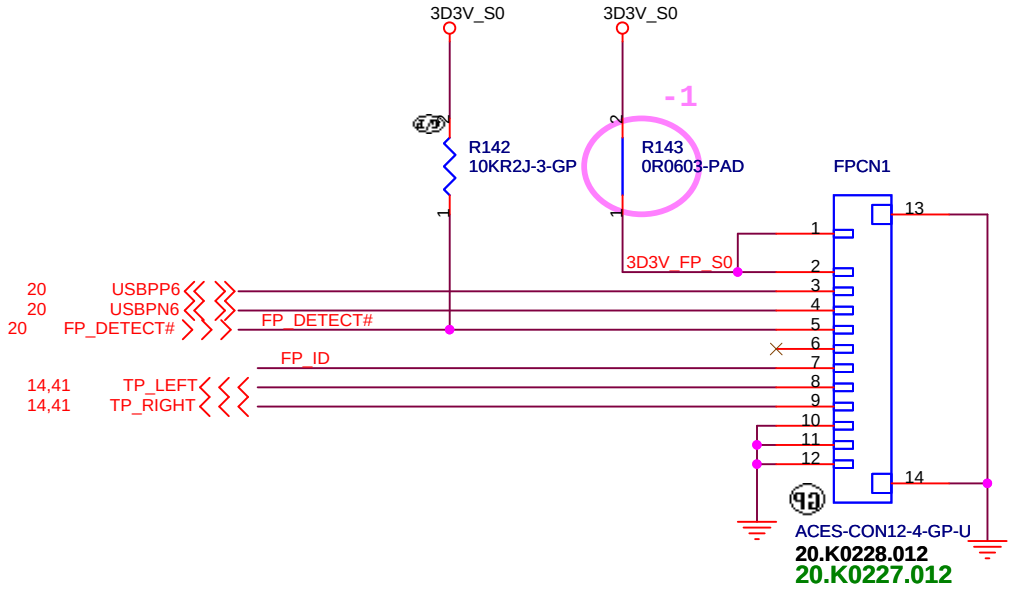
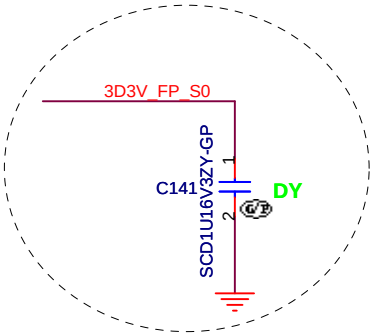
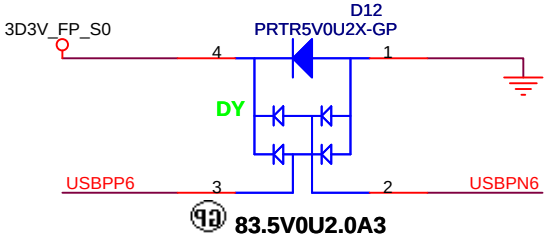
Finger printer







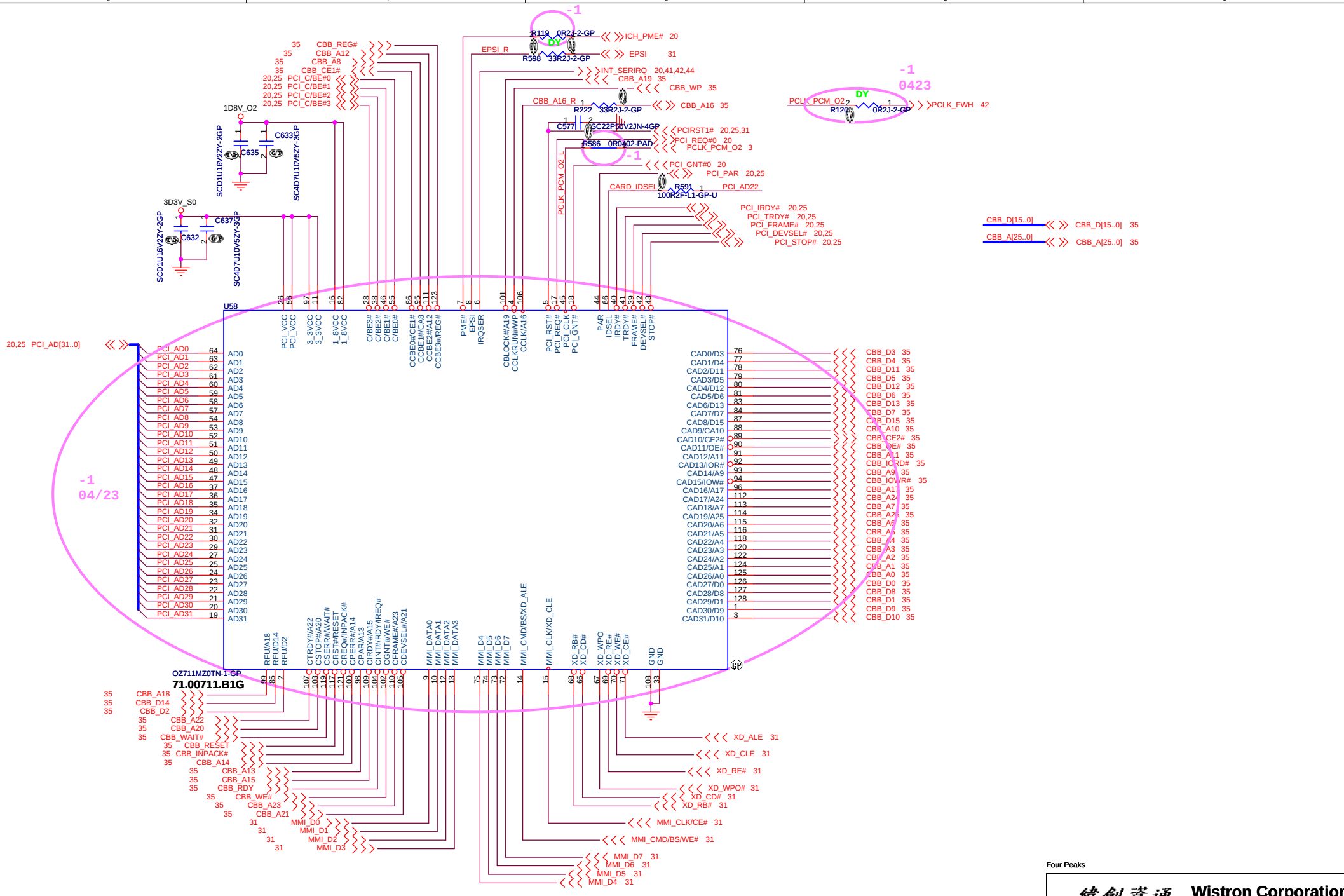
For EMI



Four Peaks

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Finger Printer*		
Size	Document Number: Four Peaks	Rev: -1M
Date: Friday, November 21, 2008	Sheet 29 of 57	



Four Peaks

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Card Reader - OZ711MZ0*

Size	Document Number	Rev
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Date: Friday, November 21, 2008 Sheet 30 of 57

USB_CN1 & CR_CN1 Conn. Test Point

USB_OC#4 — TP221 AFTE30-GP
USBPN1 — TP186 AFTE30-GP
USBPP1 — TP190 AFTE30-GP
USBPN4 — TP228 AFTE30-GP
USBPP4 — TP227 AFTE30-GP
USB_PWR_EN# — TP218 AFTE30-GP
5V_S5 — TP205 AFTE30-GP

MMI_D0 — TP197 AFTE30-GP
MMI_D1 — TP129 AFTE30-GP
MMI_D2 — TP142 AFTE30-GP
MMI_D3 — TP145 AFTE30-GP
MMI_D4 — TP146 AFTE30-GP
MMI_D5 — TP147 AFTE30-GP
MMI_D6 — TP148 AFTE30-GP
MMI_D7 — TP149 AFTE30-GP
3D3V_CR_S0 — TP170 AFTE30-GP
XD_RB# — TP199 AFTE30-GP
XD_RE# — TP202 AFTE30-GP
XD_CLE — TP203 AFTE30-GP
XD_ALE — TP213 AFTE30-GP
XD_WPO# — TP214 AFTE30-GP
XD_CD# — TP215 AFTE30-GP
MMI_CMD/BS/WE# — TP217 AFTE30-GP
MS_CD# — TP216 AFTE30-GP
MMI_CLK/CE# — TP218 AFTE30-GP

SD_CD# — TP219 AFTE30-GP
SD_WP — TP220 AFTE30-GP
STDBY_LED#_E — TP221 AFTE30-GP
3D3V_S0 — TP222 AFTE30-GP
FRONT_PWRLED#_E — TP223 AFTE30-GP
3D3V_S5 — TP224 AFTE30-GP
KBC_PWRBTN#_CN — TP226 AFTE30-GP

-1M(5/30)

SC

USB_CN1
ACES-CON14-1-GP
20.K0276.014
20.K0227.014

CR_CN1
RTWO-CON28-GP
20.K0275.028

EC9 DY SCD1U16V2ZY-2GP
C66 DY SC1U16V2ZY-GP
EC14 DY SCD1U16V2ZY-2GP
C106 DY SC1U16V3ZY-GP
EC11 DY SC1KP50V2KX-1GP
EC12 DY SC1KP50V2KX-1GP
EC10 DY SC1KP50V2KX-1GP

20 USB_OC#4
20 USBPN1
20 USBPP1
20 USBPN4
20 USBPP4
28,41 USB_PWR_EN#
5V_S5
3D3V_CR_S0
30 MMI_D0
30 MMI_D1
30 MMI_D2
30 MMI_D3
30 MMI_D4
30 MMI_D5
30 MMI_D6
30 MMI_D7
30 XD_RB#
30 XD_RE#
30 XD_CLE
30 XD_ALE
30 XD_WPO#
30 XD_CD#
30 MMI_CMD/BS/WE#
30 MMI_CLK/CE#
16 STDBY_LED#_E
16 FRONT_PWRLED#_E
16,44 KBC_PWRBTN#_CN
MS_CD#
SD_CD#
SD_WP
3D3V_S0
3D3V_S5

5V_S0
3D3V_S0
DY C318 SCD1U16V2ZY-2GP
C319 SC4D7U10V5ZY-3GP
DY C306 SCD1U16V2ZY-2GP
C307 SC4D7U10V5ZY-3GP
5V_COMBO_S0
VCC_ASKT_S0

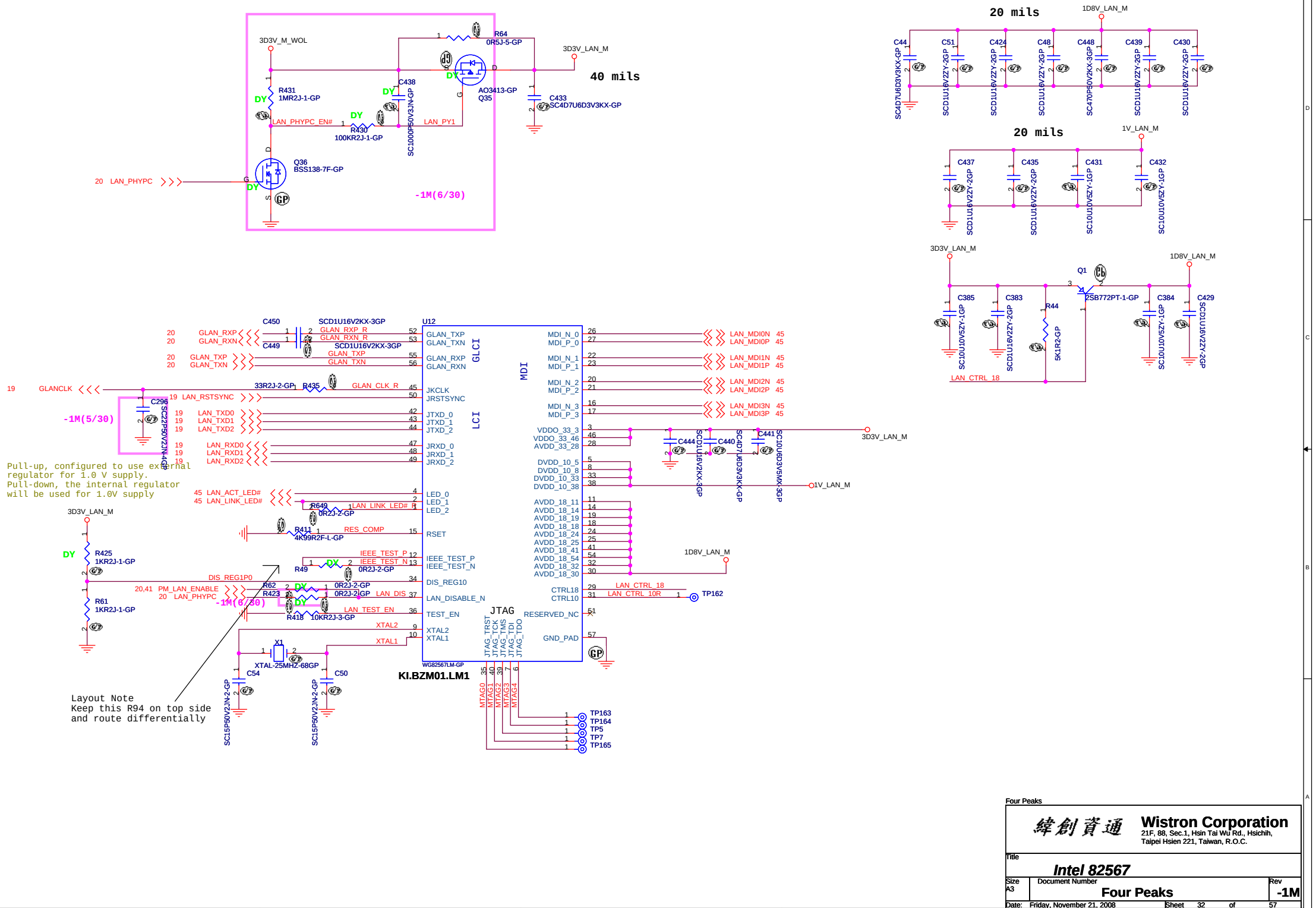
U34
OZ2544LN-GP-U
VCC/VPP
VCC/VPP
SC_VCC
5VIN
5VIN
3_3VIN
3_3VIN
NC#23
NC#24
CD1#
CD2#
MS_CD#
SD_CD#
SC_CD#
VS1
VS2
SERR#
PERR#
MMI_WP#
MMI_VCC3#
1_8VOUT
CAUDIO
GND
GND
CLKRUN#
PCI_CLK
SC_CLK
SC_RST
SC_IO
CSTSCHG/BVD1
EPSI
RESET#
INTA#
35 CBB_CD1#
35 CBB_CD2#
34 SC_CD#
35 CBB_VS1#
35 CBB_VS2#
20,25 PCI_SERR#
20,25 PCI_PERR#
PM_CLKRUN# 20,25,41,42,44
PCLK_O2 3
SC_CLK 34
SC_RST 34
SC_IO 34
CBB_BVD1# 35
EPS' 30
C314 DY SC100P50V2JN-3GP
PCIRST1# 20,25,30
INT_PIRQG# 20
1D8V_O2
SD_WP
CARD_EN#

3D3V_CR_S0
U65
G5240B2T1U-GP-U
OUT
GND
NC#3
IN
EN#
C667 SCD1U16V2ZY-2GP
C666 SC1U16V3ZY-GP
3D3V_S0
CARD_EN#

Four Peaks

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Card Reader Connector
Size | Document Number: Four Peaks | Rev: -1M
Date: Friday, November 21, 2008 | Sheet 31 of 57



Four Peaks

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

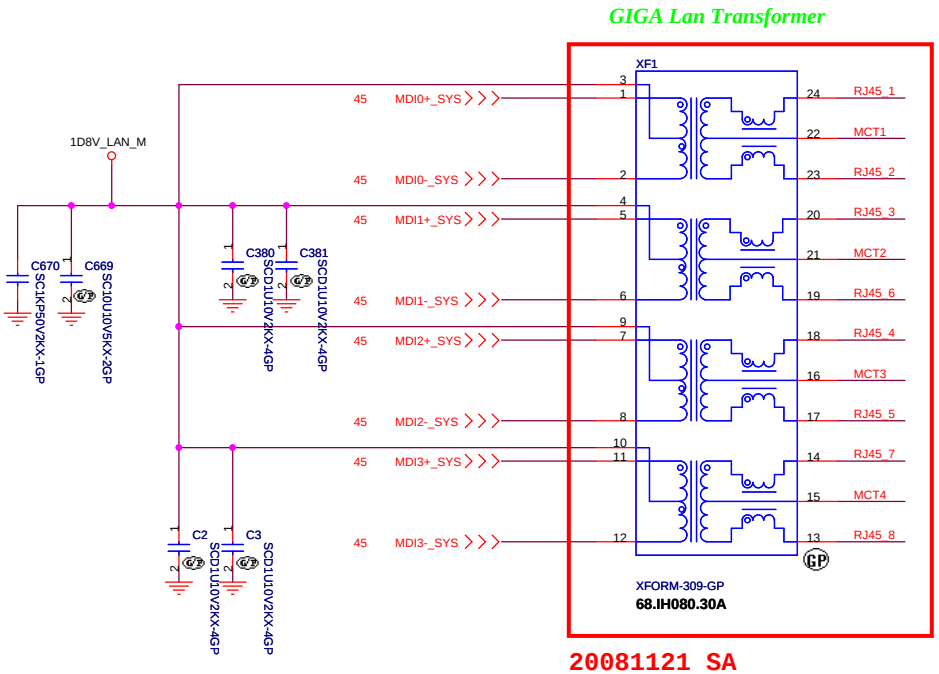
Title: ***Intel 82567***

Size	Document Number	Rev
A3	**Four Peaks**	**-1M**

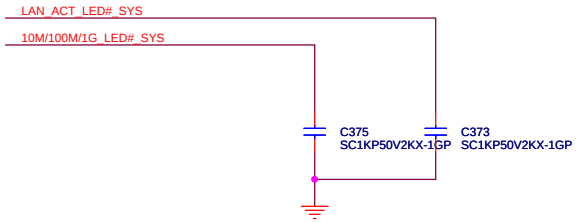
Date: Friday, November 21, 2008 Sheet 32 of 57

LAN Connector

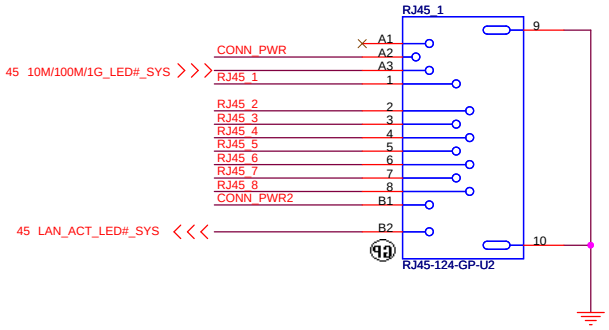
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

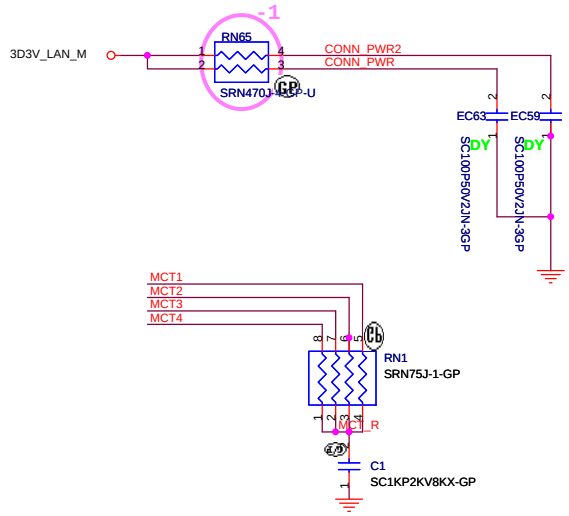


20081121 SA
change to 68.IH080.30A



LAN Connector

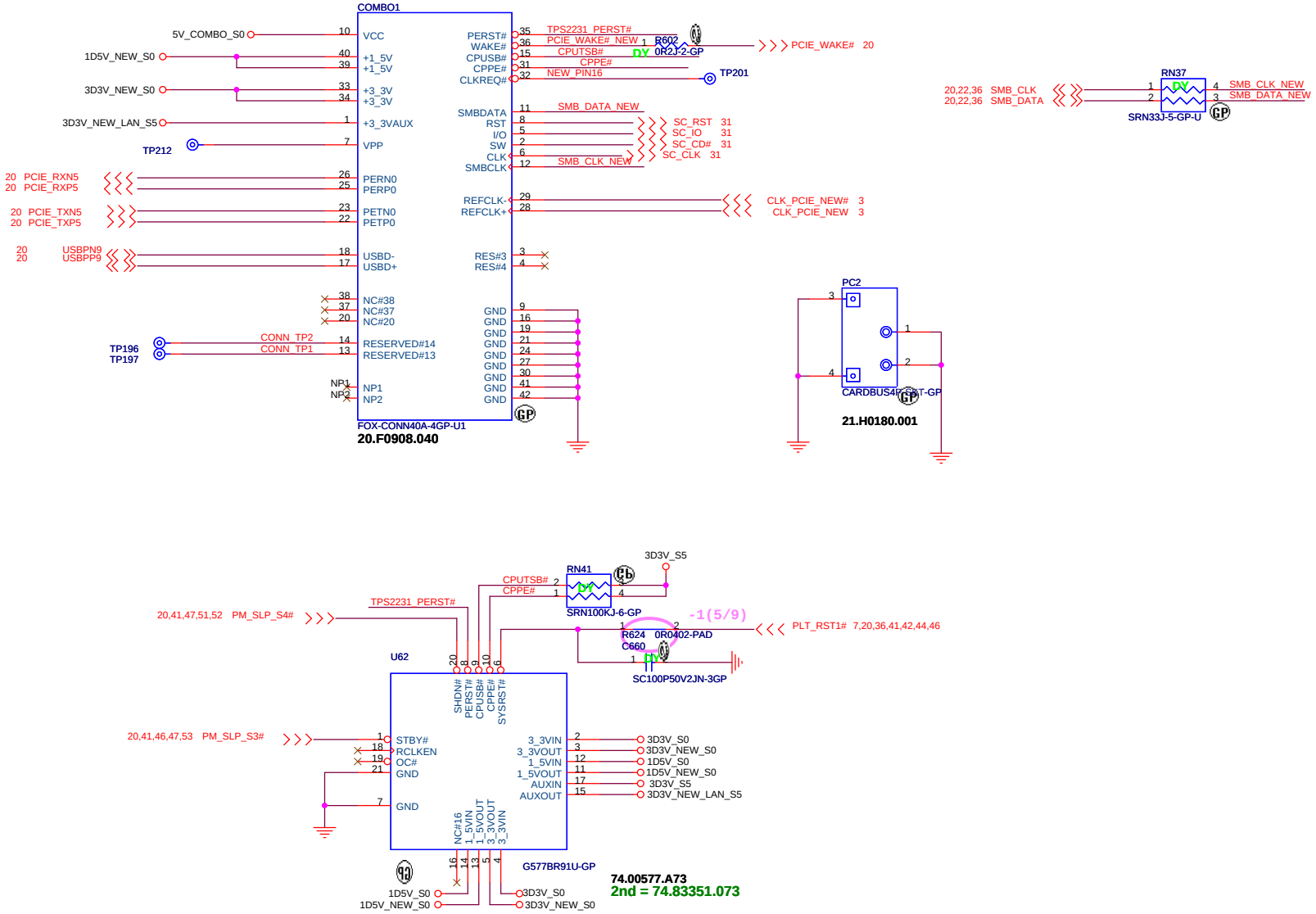




Four Peaks

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	**LAN CONN**	
Size A3	Document Number	Rev -1M
Date: Friday, November 21, 2008	Sheet 33 of 57	



Four Peaks

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

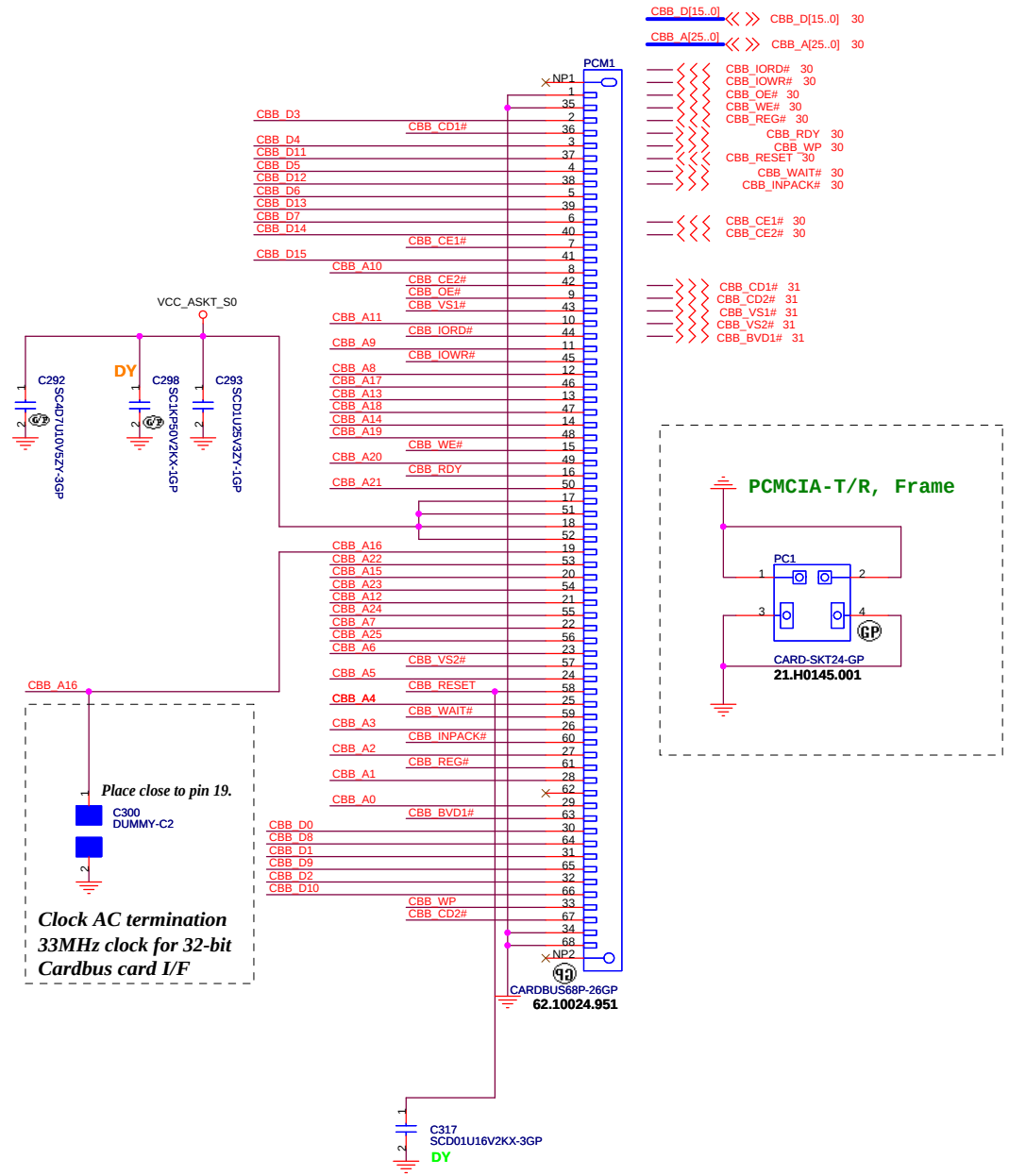
Title: **NEW CARD**

Size | Document Number: **Four Peaks** | Rev: -1M

Date: Friday, November 21, 2008 | Sheet 34 of 57

PCMCIA Socket

Cardbus I/F

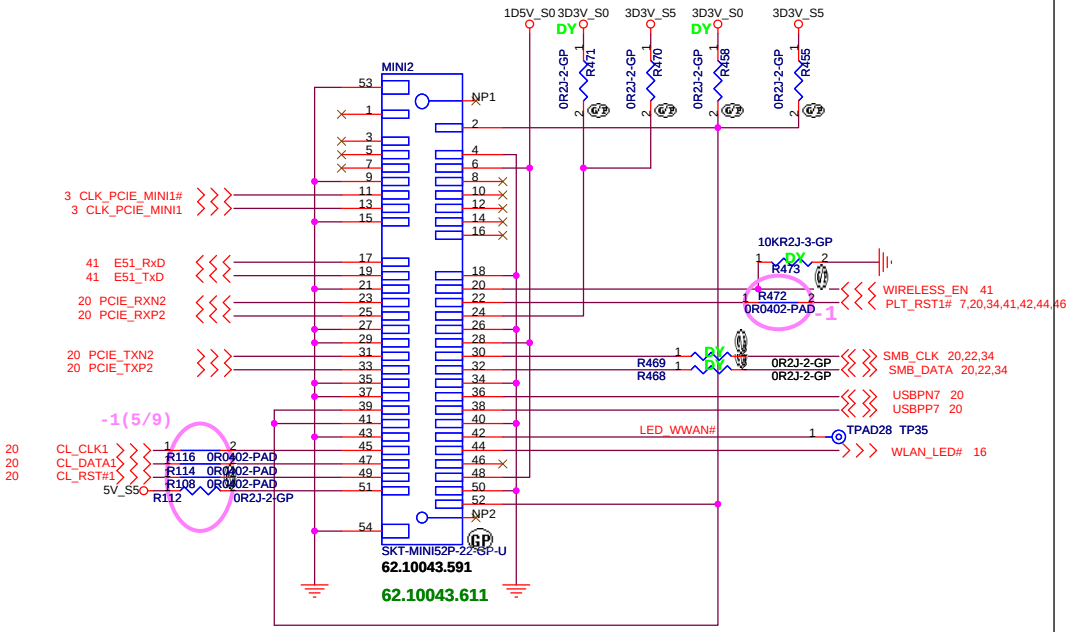


Four Peaks

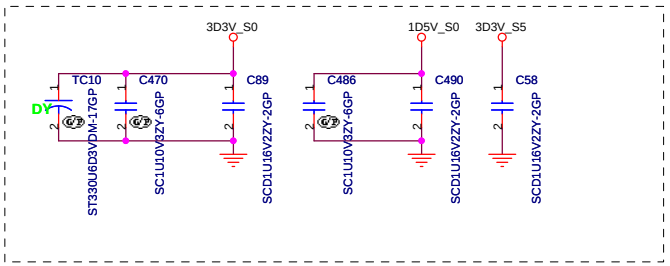
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCMCIA**		
Size: A3	Document Number: **Four Peaks**	Rev: **-1M**
Date: Friday, November 21, 2008	Sheet 35 of 57	

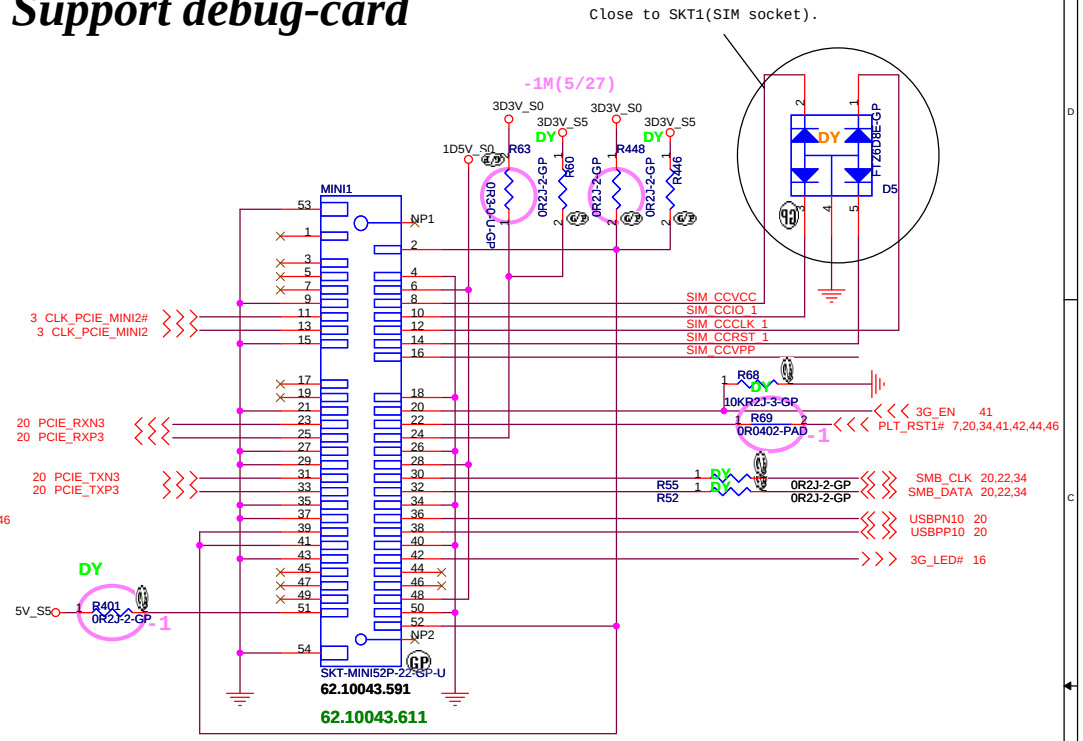
Mini Card Connector(WLAN)



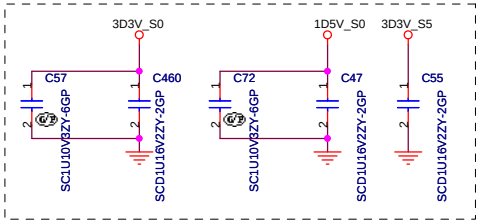
Place near MINIC1

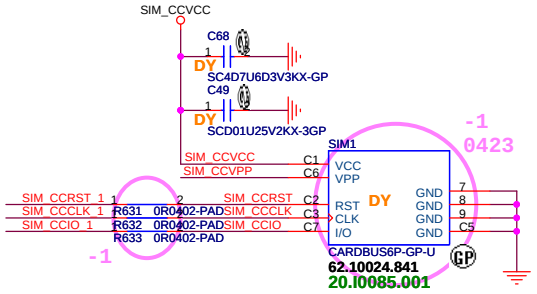


Mini Card Connector(Robson2 and 3G)
Support debug-card



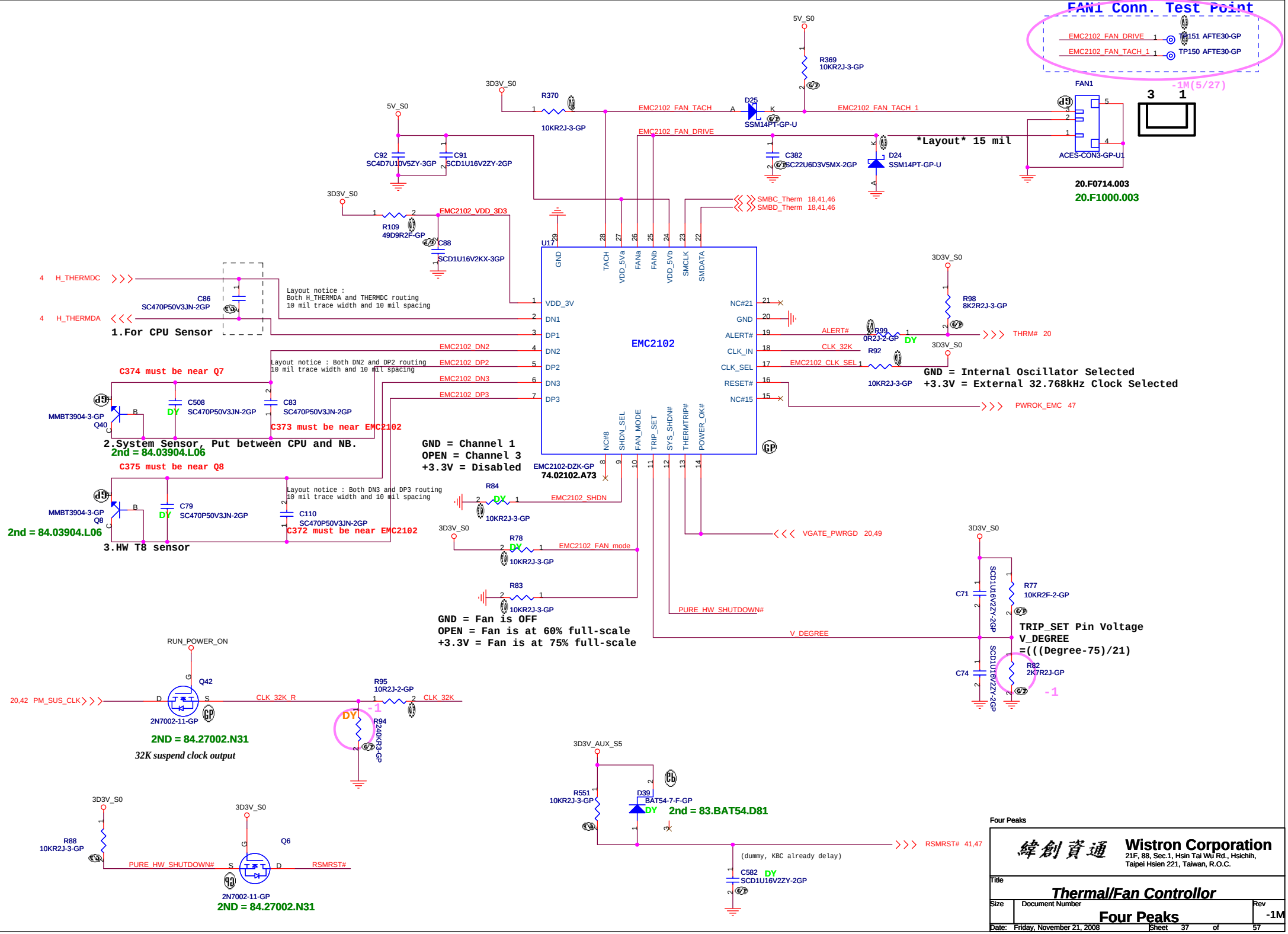
Place near MINIC2





Four Peaks

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MINI CARD		
Size: A3	Document Number: Four Peaks	Rev: -1M
Date: Friday, November 21, 2008	Sheet 36 of 57	



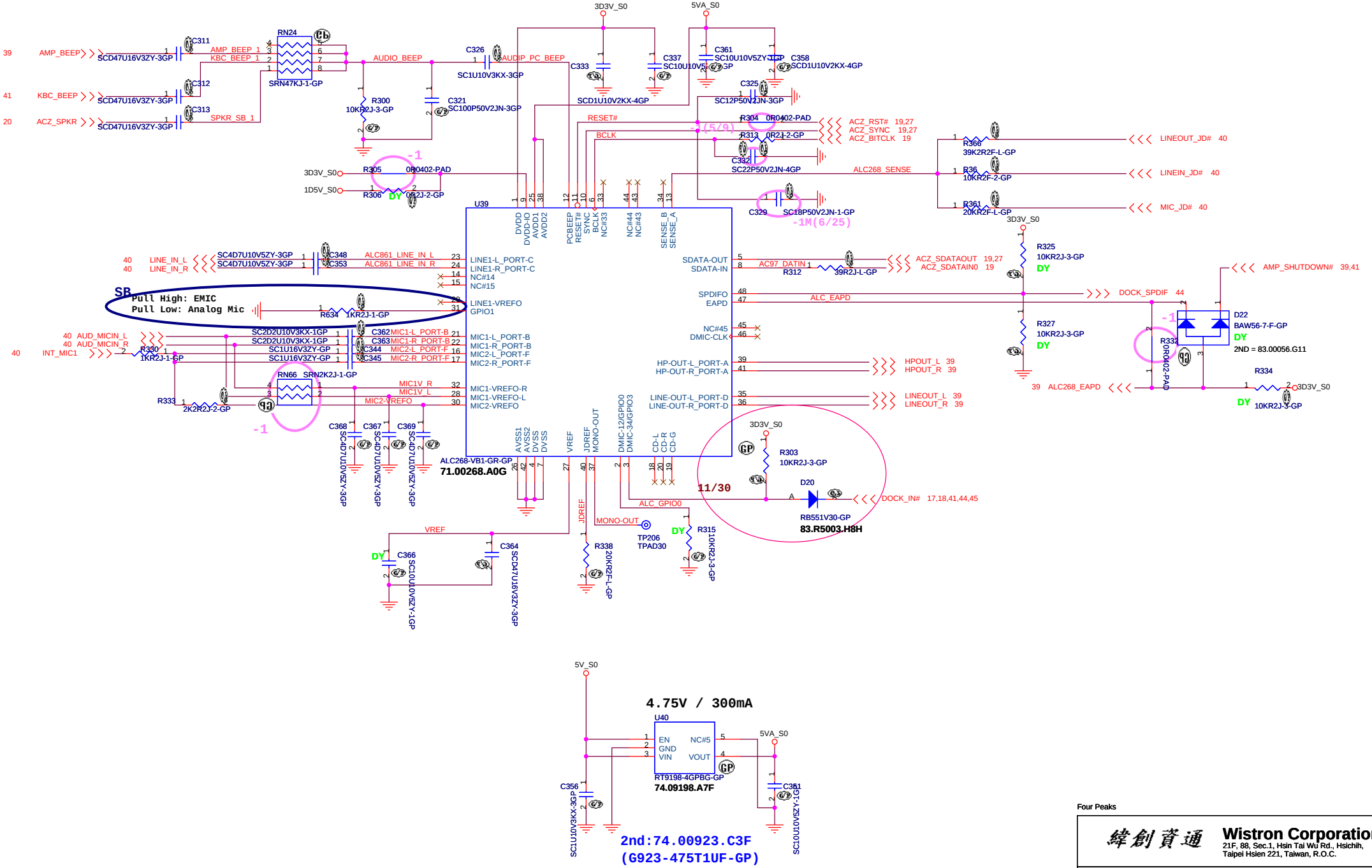
Four Peaks

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor

Size	Document Number	Rev
	Four Peaks	-1M

Date: Friday, November 21, 2008 Sheet 37 of 57



Four Peaks

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Azalia codec ALC268***	
Size A3	Document Number **Four Peaks**	Rev **-1M**
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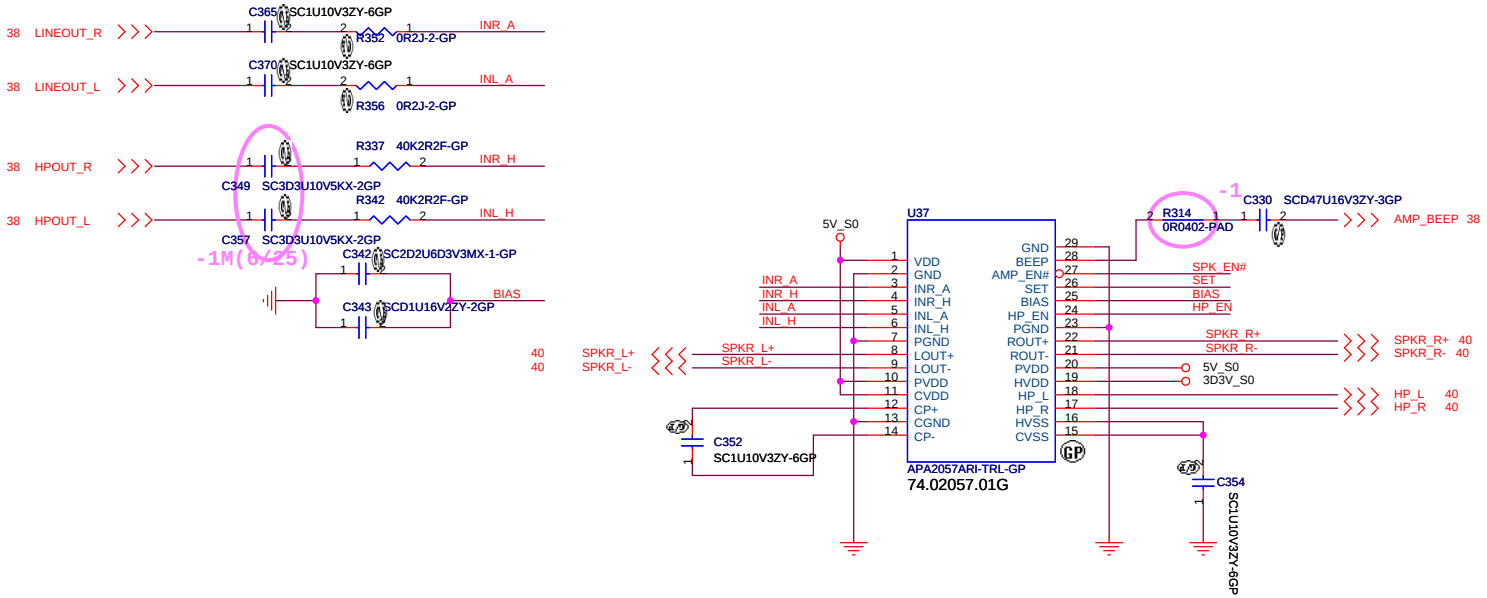
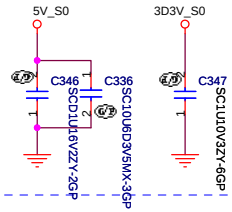
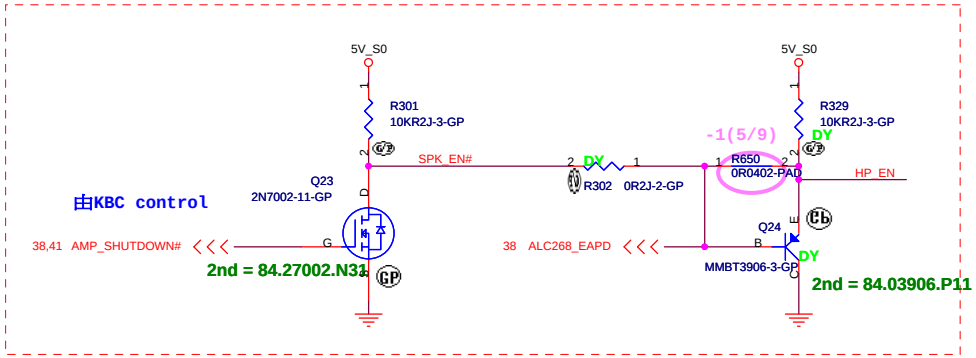
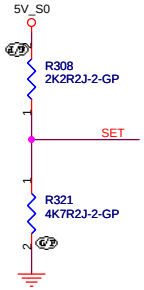
AUDIO OP AMPLIFIER



Layout Note :
C218,C219,C220 near U110







Four Peaks

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	AUDIO AMP	
Size	Document Number: Four Peaks	Rev: -1M
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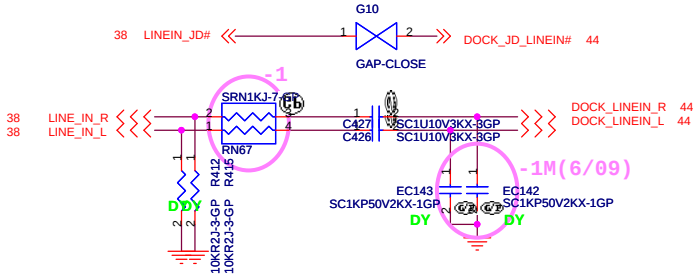
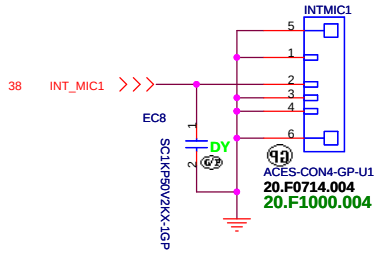
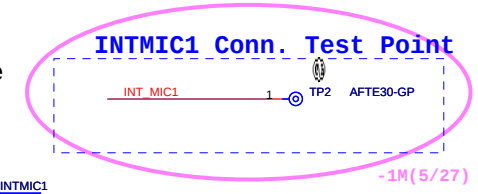
LINE IN



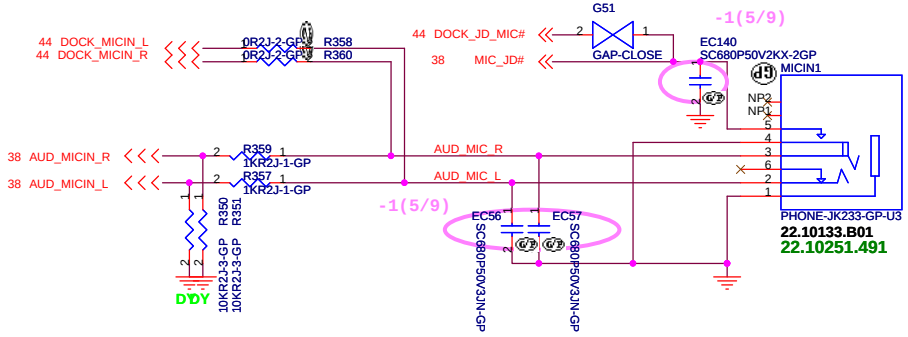
Internal Microphone



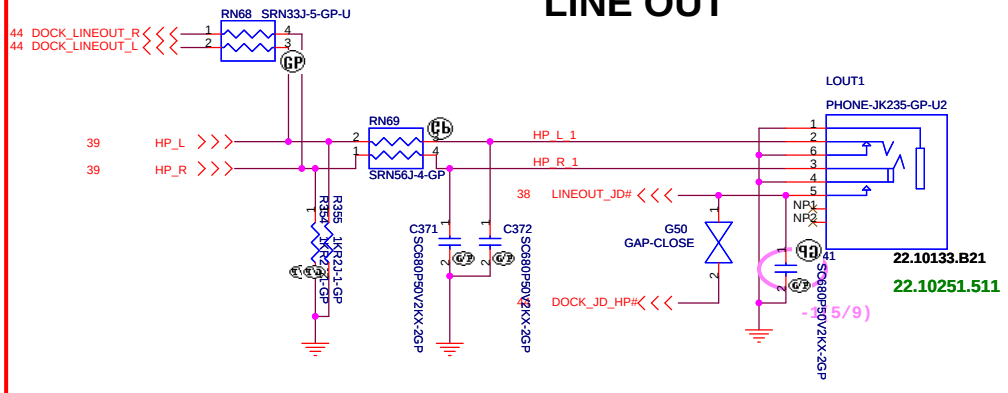
INTMIC1 Conn. Test Point



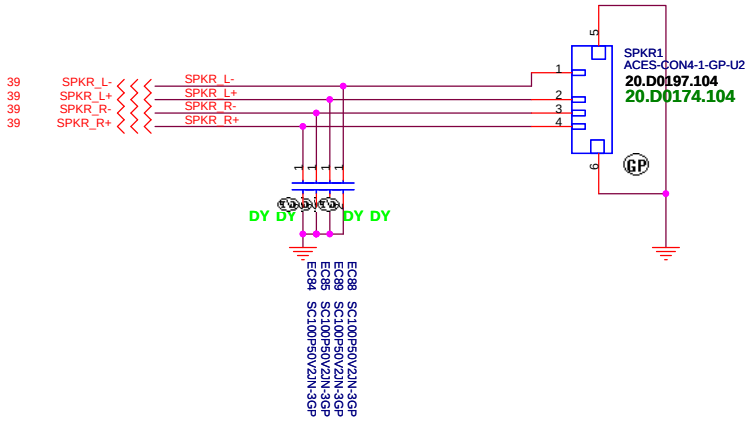
MIC IN



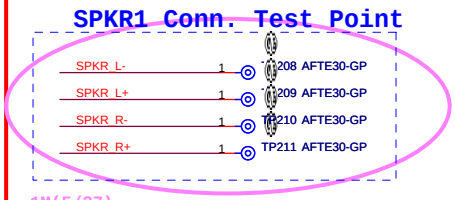
LINE OUT



Internal Speaker



SPKR1 Conn. Test Point



Four Peaks

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	AUDIO JACK	
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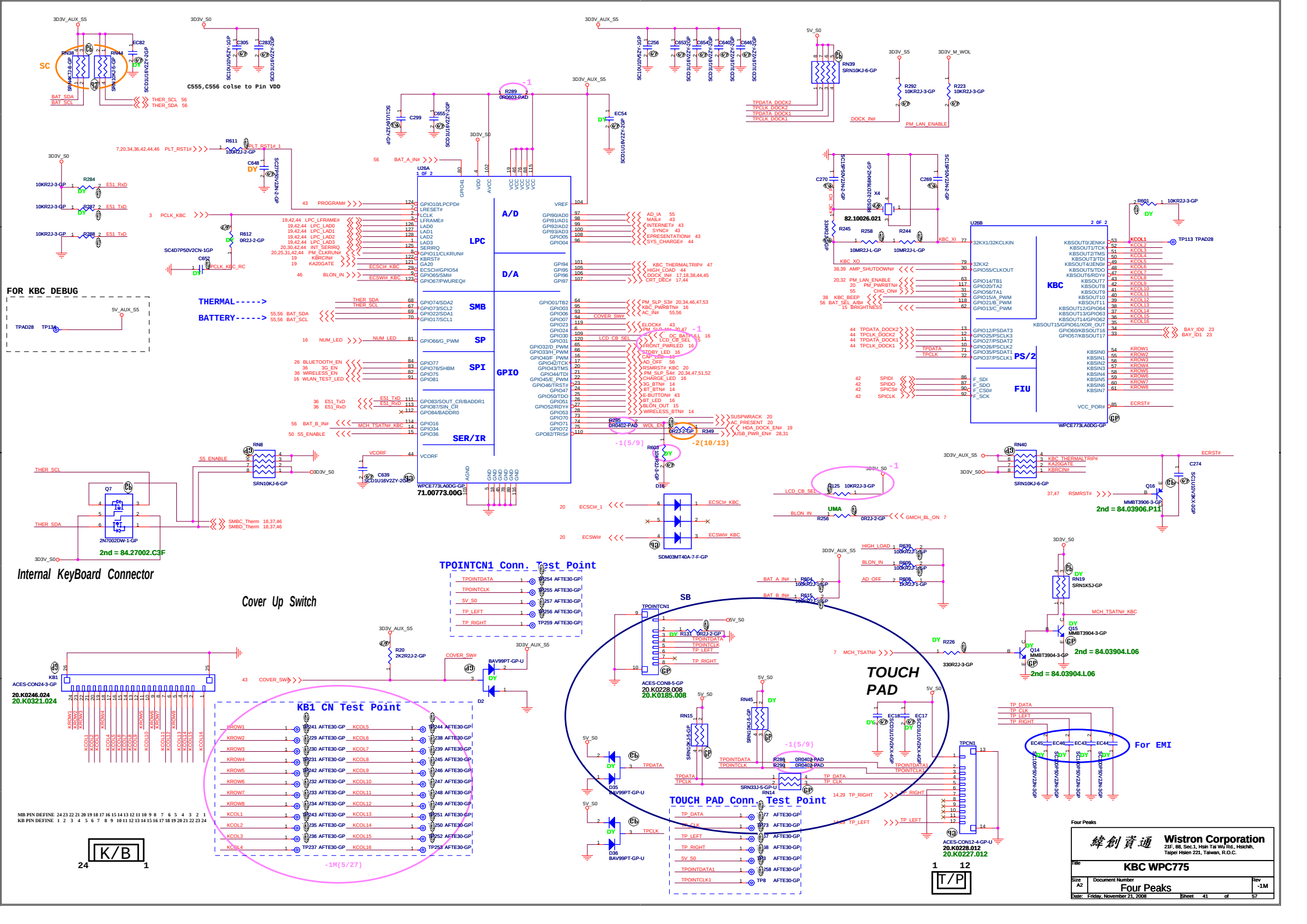
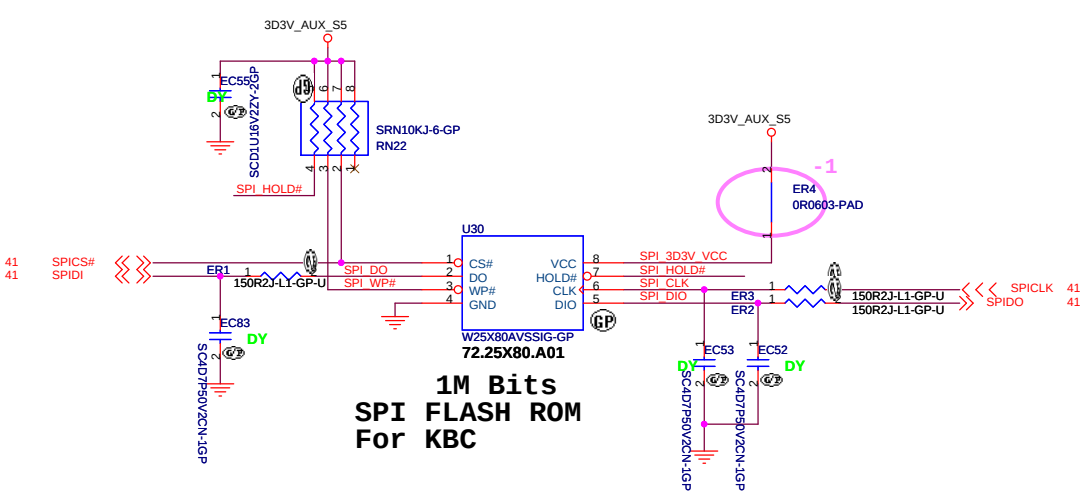
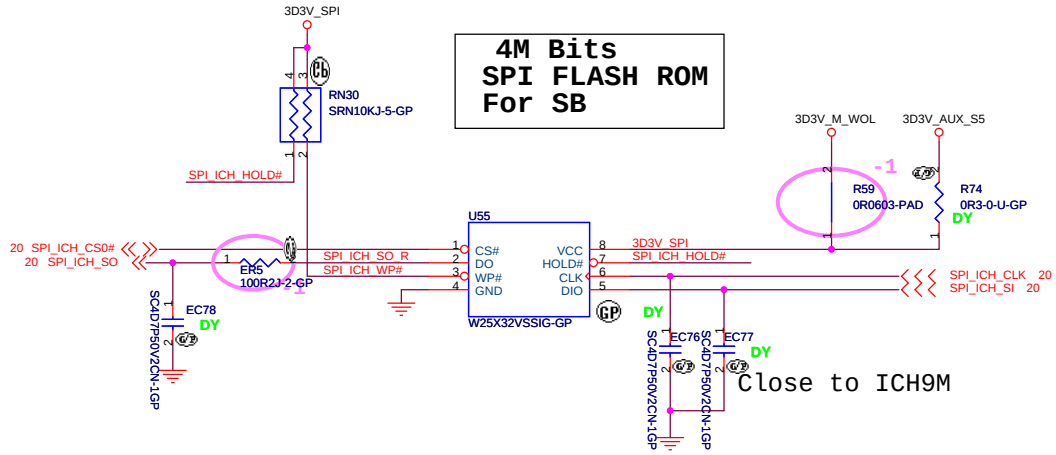
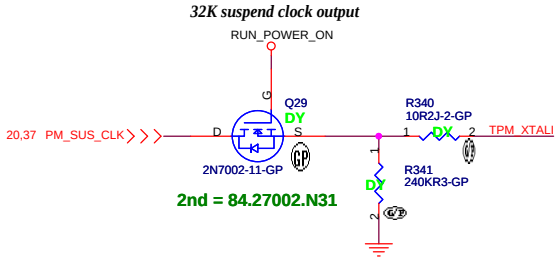
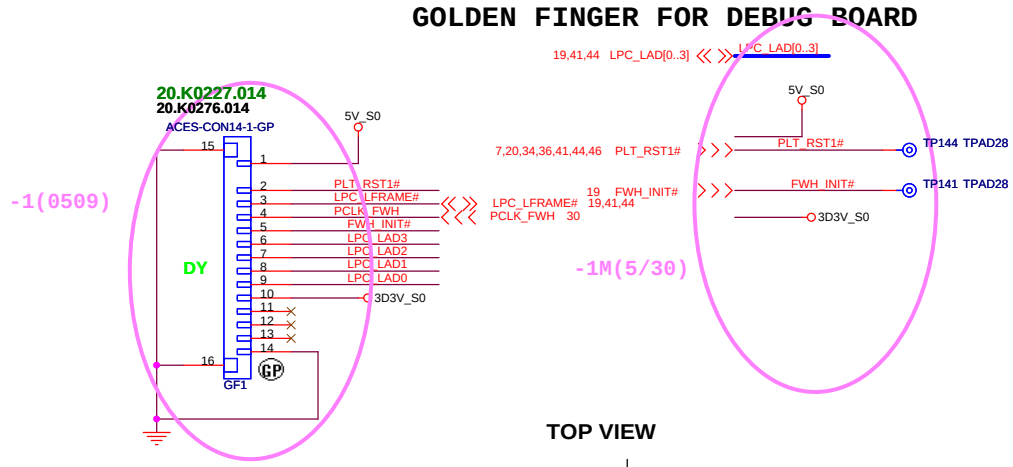
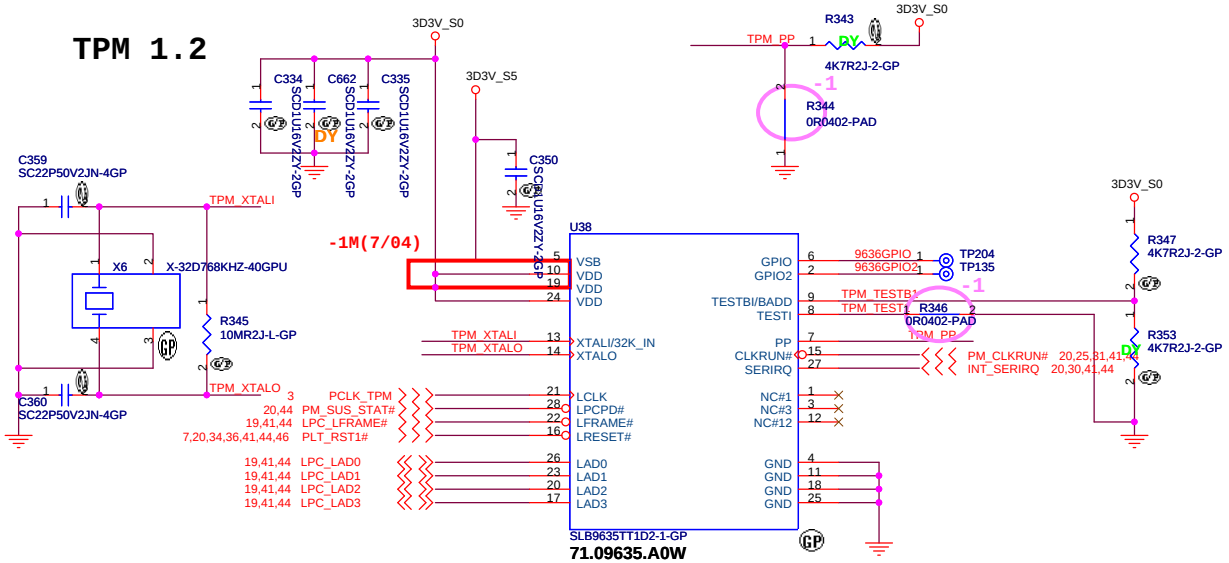

FOR KBC DEBUG
Internal KeyBoard Connector
Cover Up Switch
TPOINTCN1 Conn. Test Point
KB1 CN Test Point
TOUCH PAD Conn. Test Point
TOUCH PAD
SB
THERMAL----->
BATTERY----->
A/D
D/A
LPC
SMB
SP
SPI
GPIO
SER/IR
PS/2
FIU
KBC
UMA
For EMI
C555,C556 colse to Pin VDD
2nd = 84.27002.C3F
2nd = 84.03906.P11
2nd = 84.03904.L06
2nd = 84.03904.L06
82.10026.021
71.00773.00G
20.K0246.024
20.K0321.024
20.K0228.008
20.K0185.008
20.K0228.012
20.K0227.012
Wistron Corporation
KBC WPC775
Four Peaks
Friday, November 21, 2008











TOP VIEW

A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

(BOTTOM VIEW)

Four Peaks

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	BIOS & TPM	
Size	Document Number: Four Peaks	Rev: -1M
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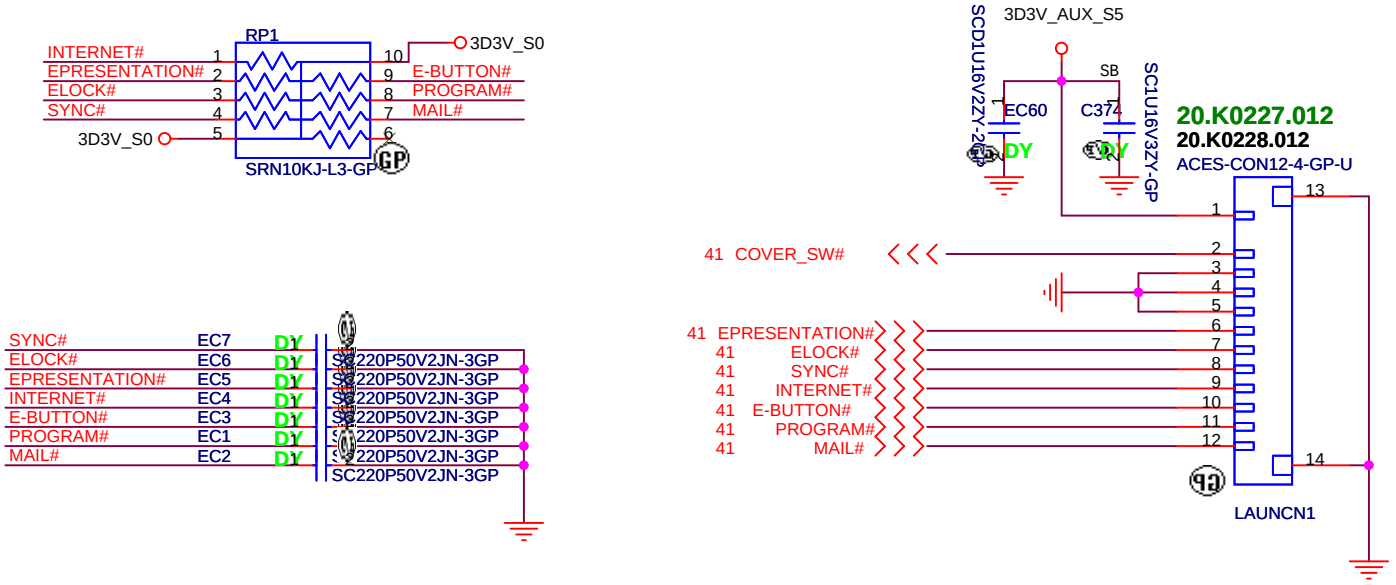

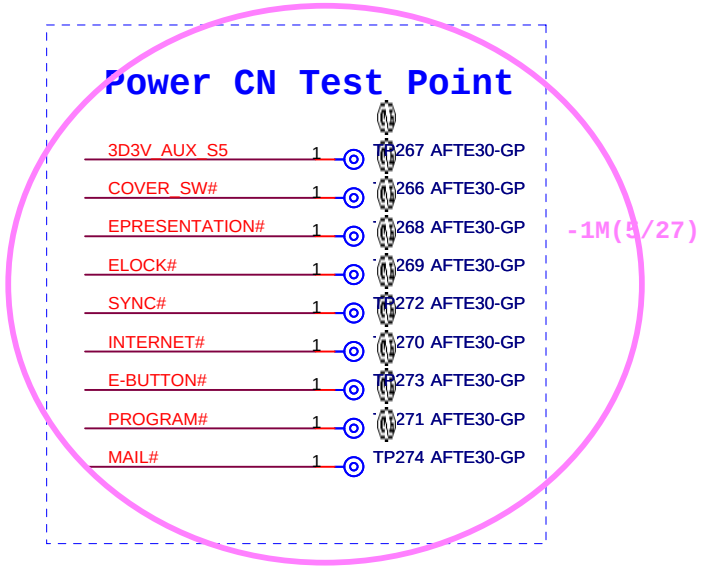

Four Peaks

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***LAUNCH***

Size	Document Number	Rev
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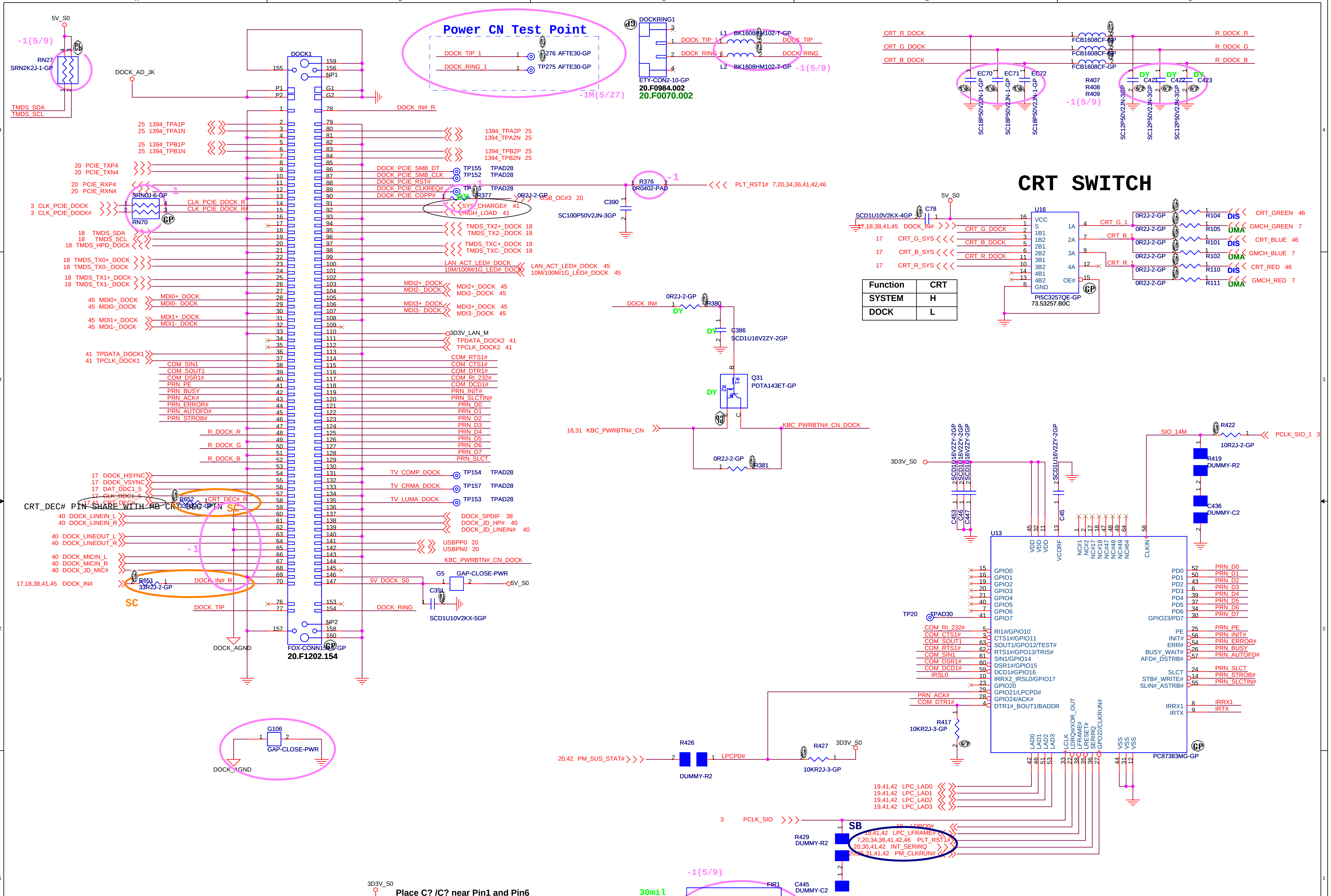

Function	CRT
SYSTEM	H
DOCK	L

Four Peaks

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
EASY PORT4 (1/2) SIO

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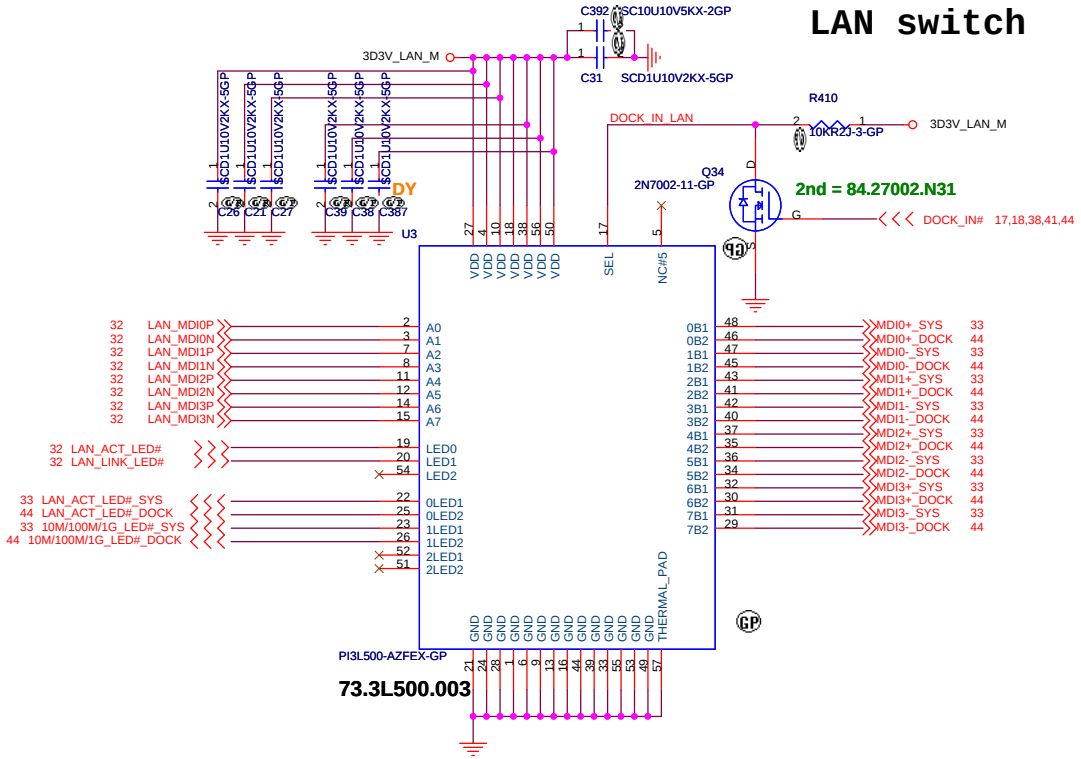
LAN switch



Function	SEL	
to An	L	DOCK
to Bn	H	SYSTEM

Four Peaks

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***EASY PORT4 (2/2)***

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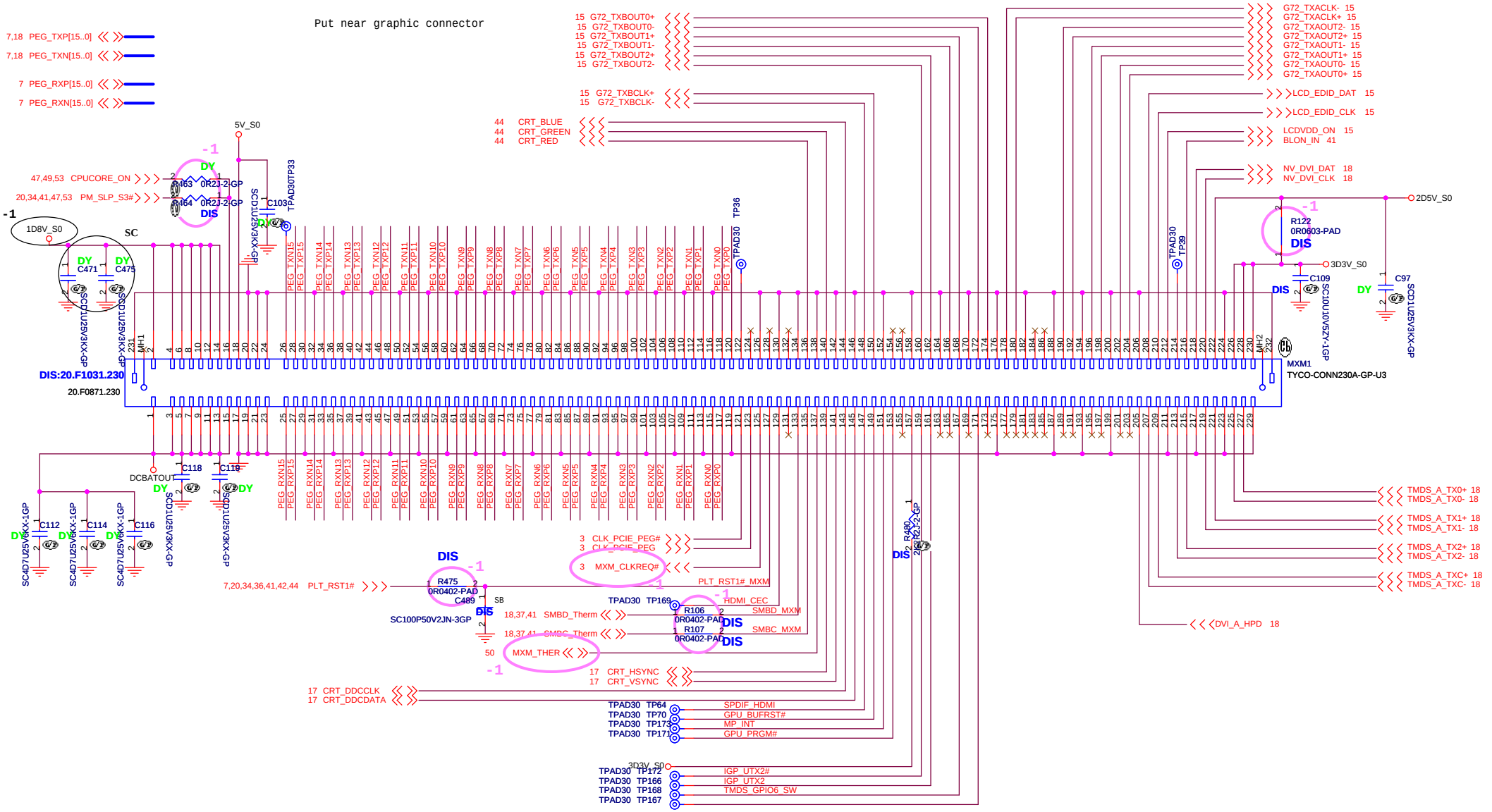
NV SMBus
A(pin143&145) : VGA(CRT) / DOCK
B(pin218&220) : DVI
C(pin208&210) : HDMI / TPI / LVDS

Put near graphic connector



Four Peaks

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Graphic MXM CONN**

Size	Document Number	Rev
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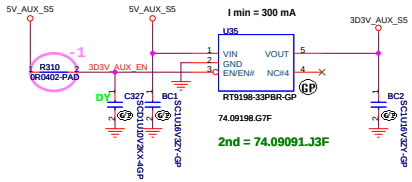
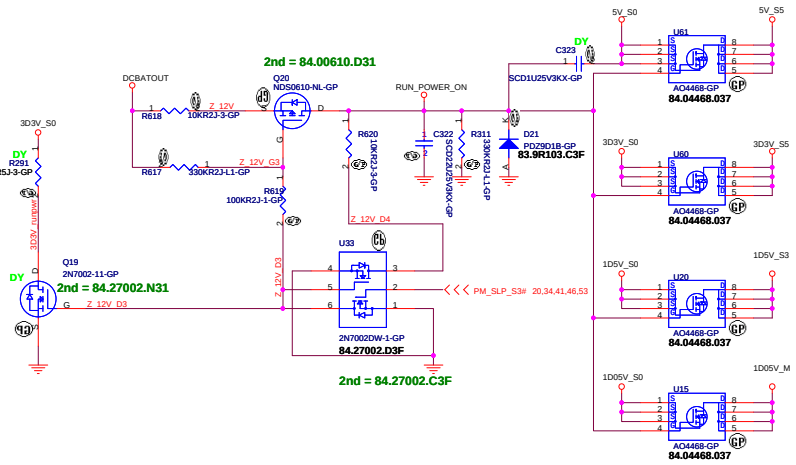
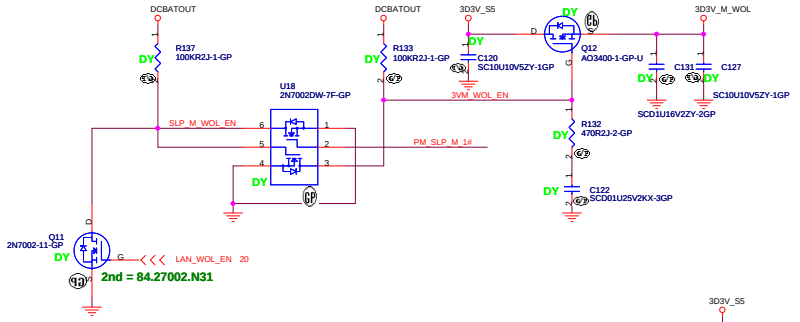
Aux Power

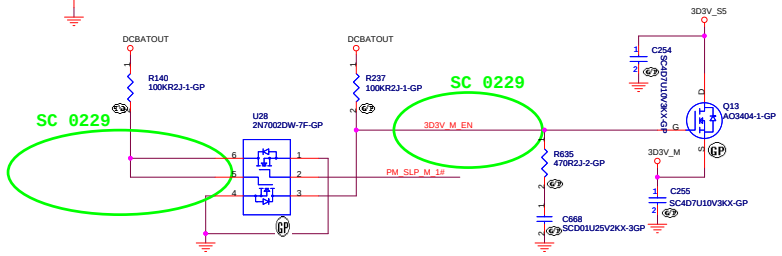
3D3V_AUX_S5

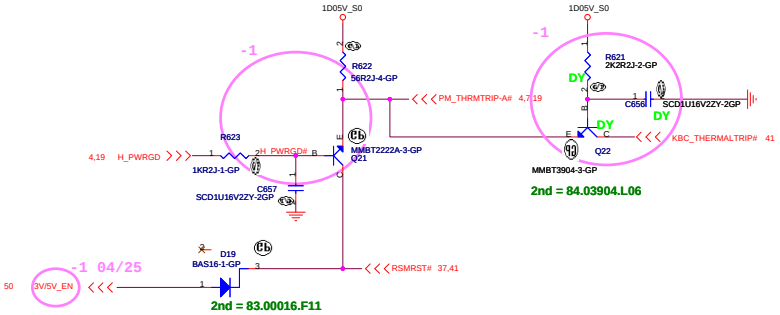
Run Power

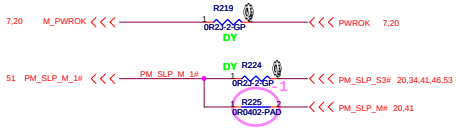


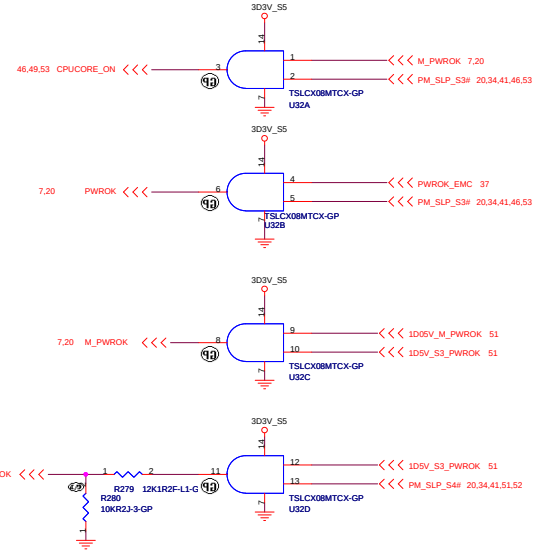


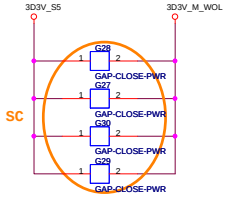












Four Peaks

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RUN POWER and 3D3V_AUX_S5

Size	Document Number	Rev
	Four Peaks	-1M

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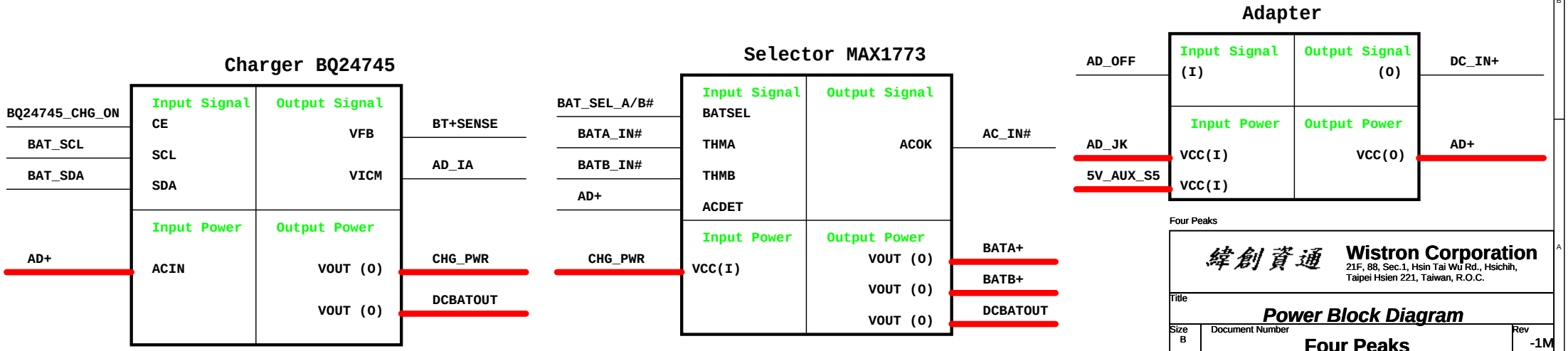

Four Peaks

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Power Block Diagram***

Size	Document Number	Rev
B	Four Peaks	-1M

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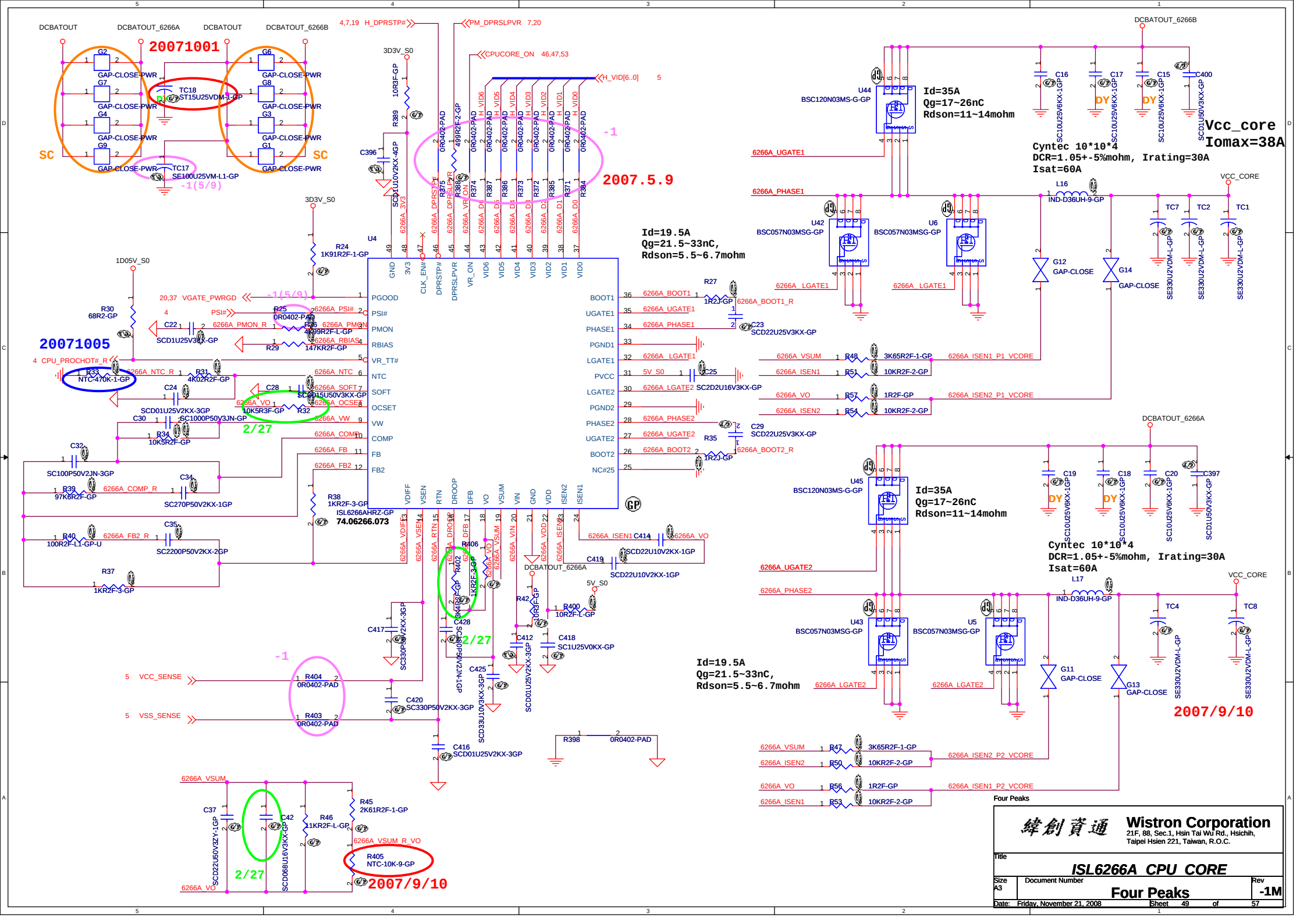
DCBATOUT
DCBATOUT_6266A
DCBATOUT
DCBATOUT_6266B
20071001
SC
SC
-1(5/9)
4,7,19 H_DPRSTP#
PM_DPRSLPVR 7,20
CPUCORE_ON 46,47,53
H_VID[6..0] 5
3D3V_S0
2007.5.9
-1
Id=19.5A
Qg=21.5~33nC,
Rdson=5.5~6.7mohm
U4
ISL6266AHRZ-GP
74.06266.073
20071005
1D05V_S0
20,37 VGATE_PWRGD
4 CPU_PROCHOT#_R
PSI#
PGOOD
PMON
RBIAS
VR_TT#
NTC
SOFT
OCSET
VW
COMP
FB
FB2
BOOT1
UGATE1
PHASE1
PGND1
LGATE1
PVCC
LGATE2
PGND2
PHASE2
UGATE2
BOOT2
NC#25
VDIFF
VSEN
RTN
DROOP
DFB
VO
VSUM
VIN
GND
VDD
ISEN2
ISEN1
2/27
2/27
2/27
-1
5 VCC_SENSE
5 VSS_SENSE
R404 0R0402-PAD
R403 0R0402-PAD
R398 0R0402-PAD
2007/9/10
Id=35A
Qg=17~26nC
Rdson=11~14mohm
Cyntec 10*10*4
DCR=1.05+-5%mohm, Irating=30A
Isat=60A
Vcc_core
Iomax=38A
VCC_CORE
Id=19.5A
Qg=21.5~33nC,
Rdson=5.5~6.7mohm
Id=35A
Qg=17~26nC
Rdson=11~14mohm
Cyntec 10*10*4
DCR=1.05+-5%mohm, Irating=30A
Isat=60A
2007/9/10
Four Peaks
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL6266A CPU CORE
Size A3
Document Number
Four Peaks
Rev -1M
Date: Friday, November 21, 2008
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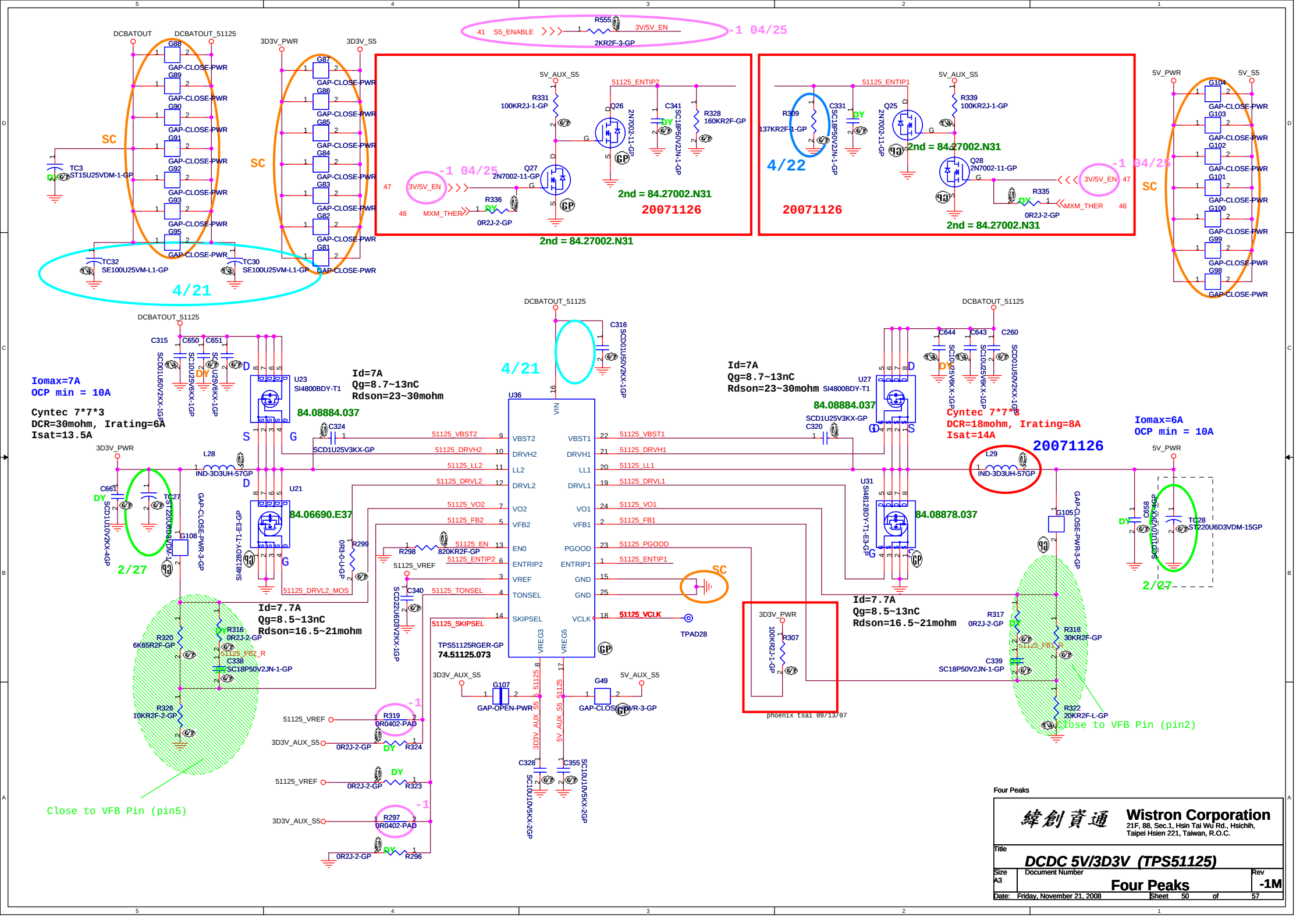
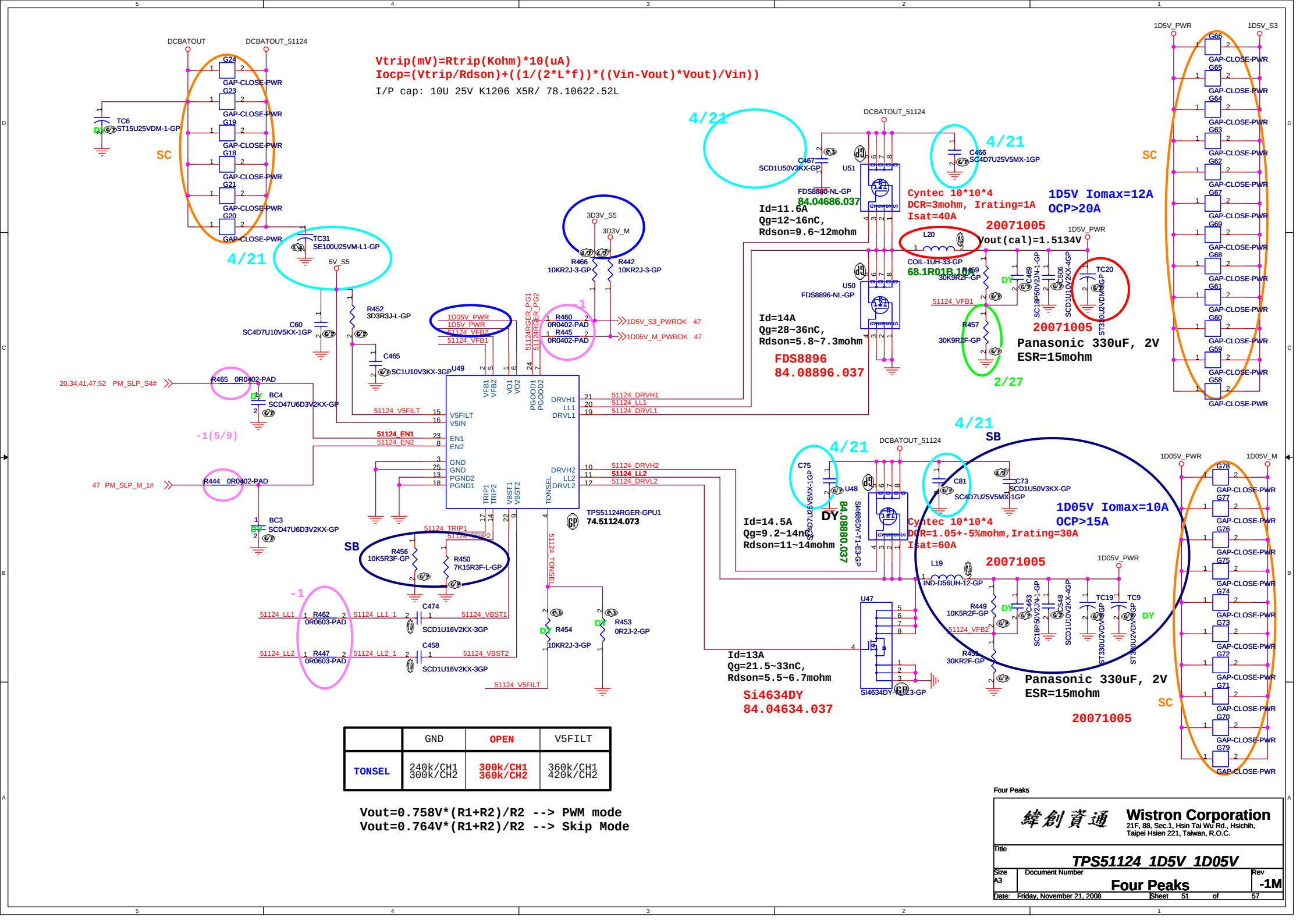

DCBATOUT
DCBATOUT_51125
3D3V_PWR
3D3V_S5
5V_AUX_S5
5V_PWR
5V_S5
SC
GAP-CLOSE-PWR
TC3 ST15U25VDM-1-GP
TC32 SE100U25VM-L1-GP
TC30 SE100U25VM-L1-GP
4/21
41 S5_ENABLE
R555
3V/5V_EN
2KR2F-3-GP
-1 04/25
R331 100KR2J-1-GP
Q26 2N7002-11-GP
C341 SC18P50V2JN-1-GP
R328 160KR2F-GP
Q27 2N7002-11-GP
R336 0R2J-2-GP
MXM_THER
2nd = 84.27002.N31
20071126
R309 137KR2F-1-GP
C331 SC18P50V2JN-1-GP
Q25 2N7002-11-GP
R339 100KR2J-1-GP
4/22
Q28 2N7002-11-GP
R335 0R2J-2-GP
Iomax=7A
OCP min = 10A
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
U23 SI4800BDY-T1
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
84.08884.037
C324 SCD1U25V3KX-GP
U36 TPS51125RGER-GP
74.51125.073
51125_VBST2
51125_DRVH2
51125_LL2
51125_DRVL2
51125_VO2
51125_FB2
51125_EN
51125_ENTIP2
51125_VREF
51125_TONSEL
51125_SKIPSEL
51125_VBST1
51125_DRVH1
51125_LL1
51125_DRVL1
51125_VO1
51125_FB1
51125_PGOOD
51125_ENTIP1
51125_VCLK
L28 IND-3D3UH-57GP
U21 SI4812BDY-T1-E3-GP
84.06690.E37
2/27
R298 820KR2F-GP
R299 0R3-0-U-GP
C340 SCD22U6D3V2KX-1GP
R320 6K65R2F-GP
R316 0R2J-2-GP
C338 SC18P50V2JN-1-GP
R326 10KR2F-2-GP
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
Close to VFB Pin (pin5)
R319 0R0402-PAD
R324 0R2J-2-GP
R323 0R2J-2-GP
R297 0R0402-PAD
R296 0R2J-2-GP
TPAD28
G107 GAP-OPEN-PWR
G49 GAP-CLOSE-PWR-3-GP
C328 SC10U10V5KX-2GP
C355 SC10U10V5KX-2GP
C316 SCD01U50V2KX-1GP
SCD1U25V3KX-GP
C320
U27 SI4800BDY-T1
84.08884.037
U31 SI4812BDY-T1-E3-GP
84.08878.037
Cyntec 7*7*3
DCR=18mohm, Irating=8A
Isat=14A
20071126
L29 IND-3D3UH-57GP
Iomax=6A
OCP min = 10A
C644 C643 C260
SCD01U50V2KX-1GP
SC10U25V6KX-1GP
C658 SCD1U10V2KX-4GP
TC28 ST220U6D3VDM-15GP
R307 100KR2J-1-GP
phoenix tsai 09/13/07
R317 0R2J-2-GP
R318 30KR2F-GP
C339 SC18P50V2JN-1-GP
R322 20KR2F-L-GP
Close to VFB Pin (pin2)
Four Peaks
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DCDC 5V/3D3V (TPS51125)
Size A3
Document Number
Four Peaks
Rev -1M
Date: Friday, November 21, 2008
Sheet 50 of 57



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

Vout=0.758V*(R1+R2)/R2 --> PWM mode
Vout=0.764V*(R1+R2)/R2 --> Skip Mode

Four Peaks

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51124 1D5V 1D05V

Size	Document Number	Rev
A3	Four Peaks	-1M

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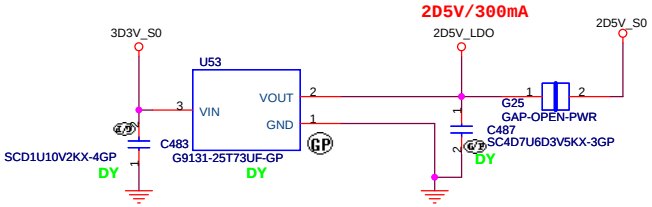
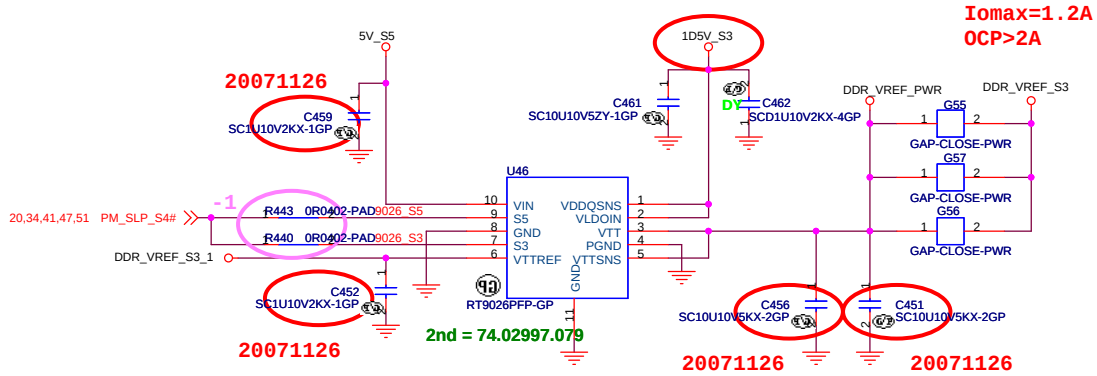
2D5V_S0
Iomax=0.3A





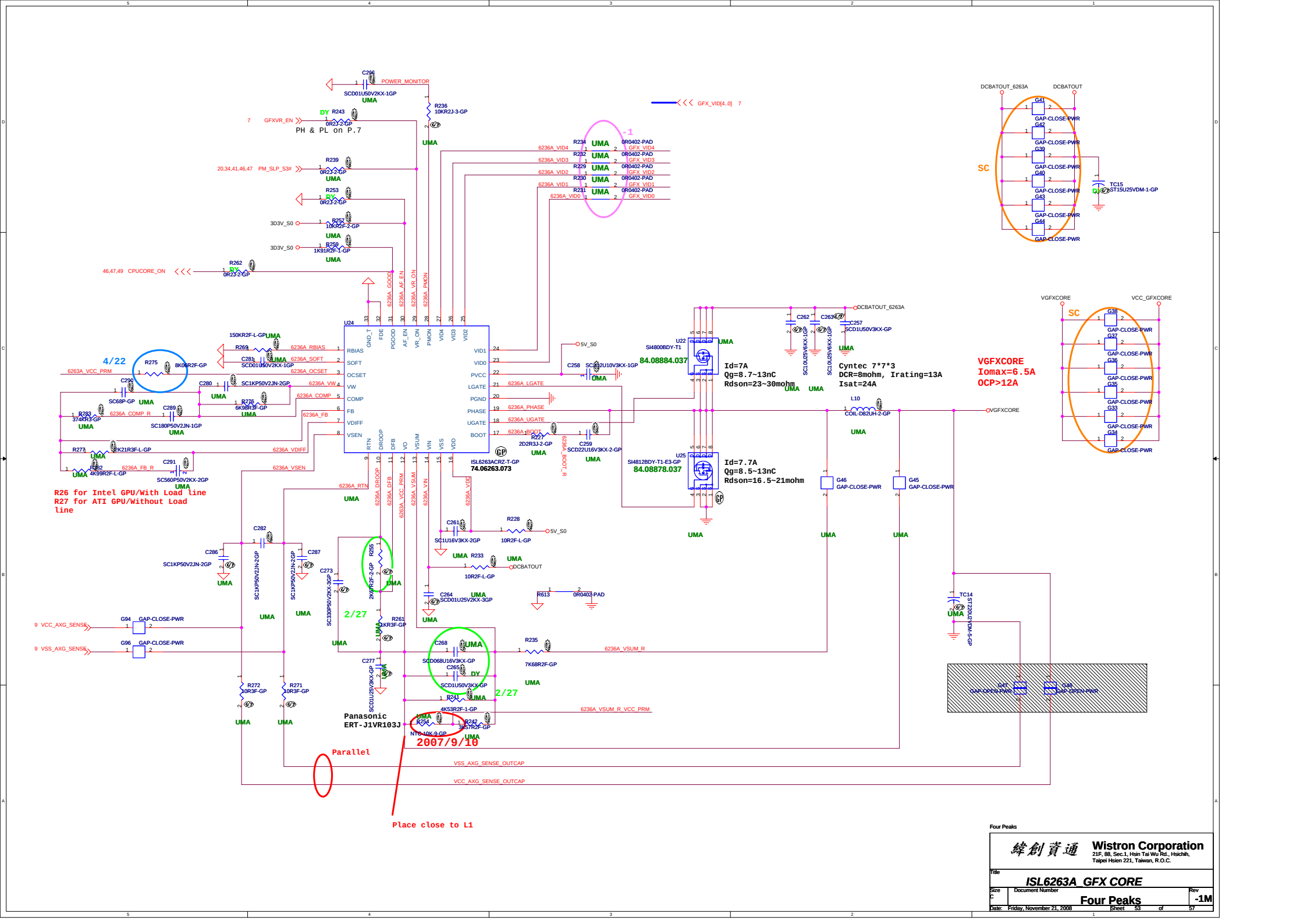
Four Peaks

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***0D75V & 2D5V***

Size	Document Number	Rev
A3	**Four Peaks**	**-1M**

Date: Friday, November 21, 2008 Sheet 52 of 57



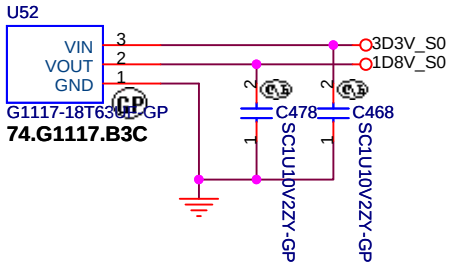
Four Peaks

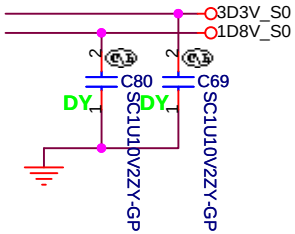
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL6263A_GFX CORE

Size	Document Number	Rev
C	Four Peaks	-1M

Date: Friday, November 21, 2008 Sheet 53 of 57





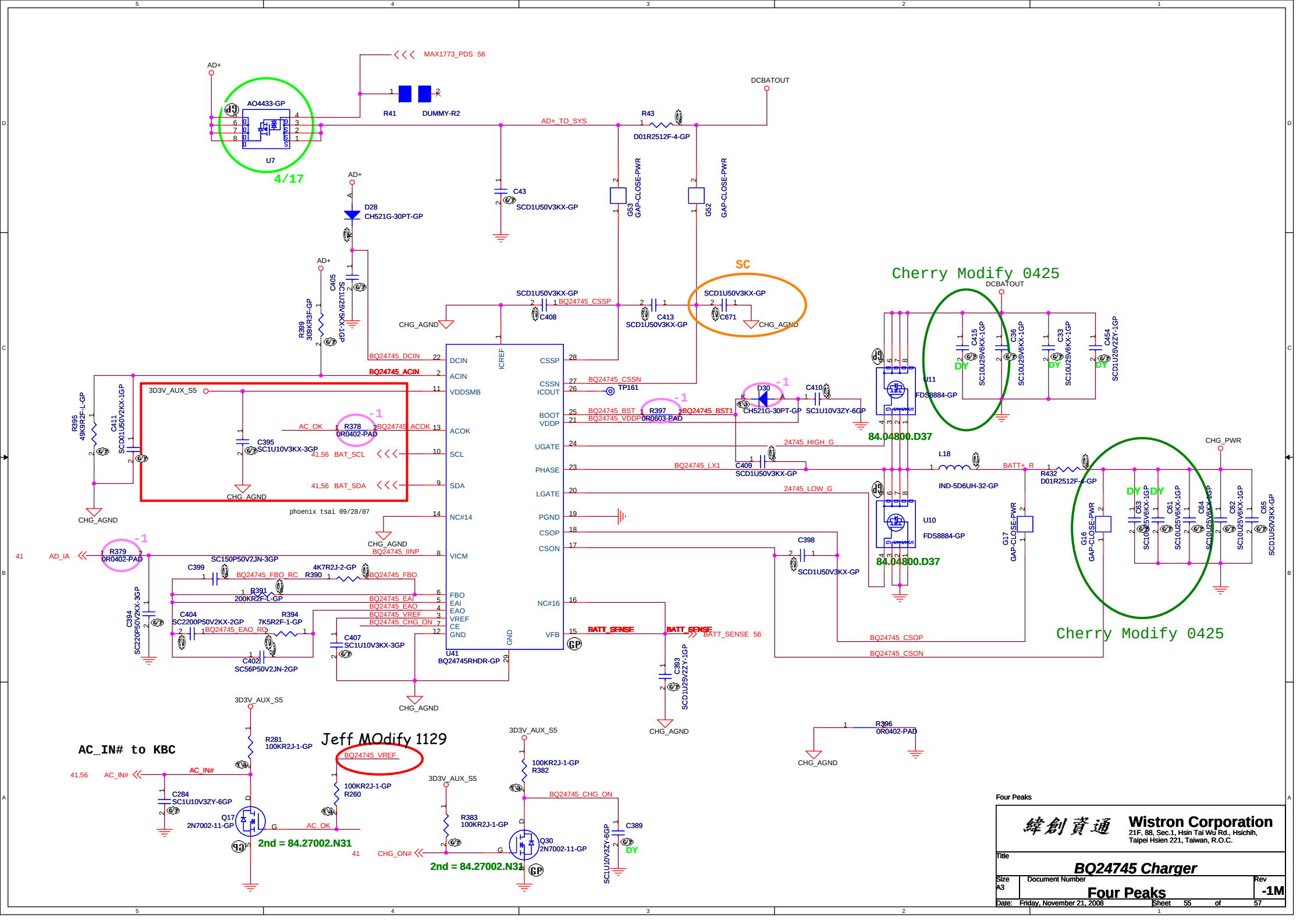
Four Peaks

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***VGA_CORE_S0 (UMA)***

Size	Document Number	Rev
A4	**Four Peaks**	**-1M**

Date: Friday, November 21, 2008 Sheet 54 of 57



Four Peaks

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **BQ24745 Charger**

Size	Document Number	Rev
A3	Four Peaks	-1M

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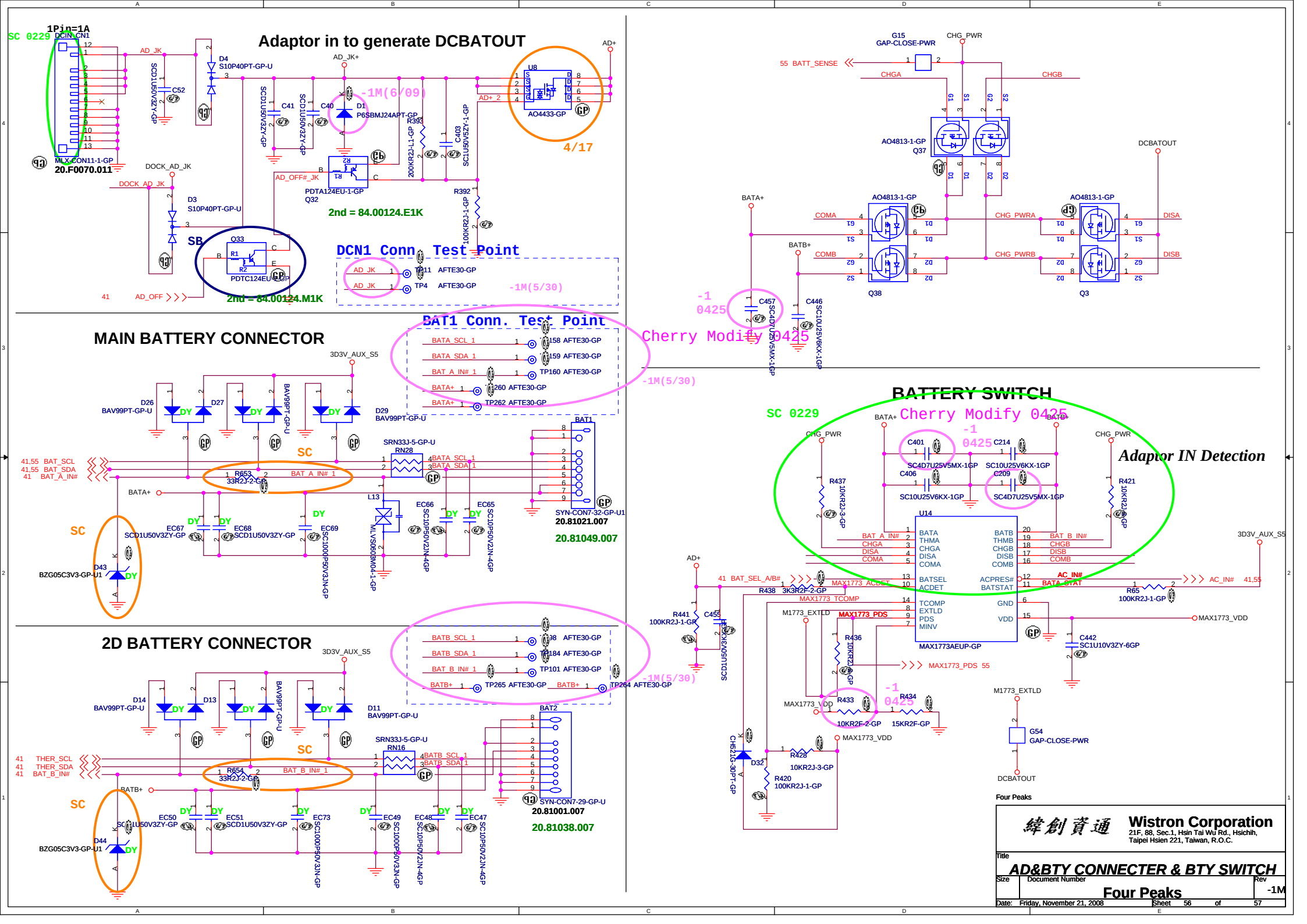
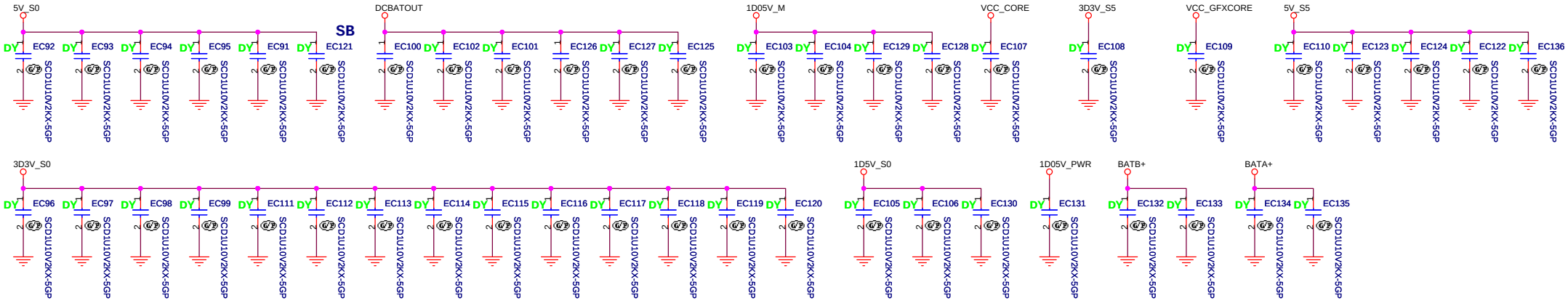
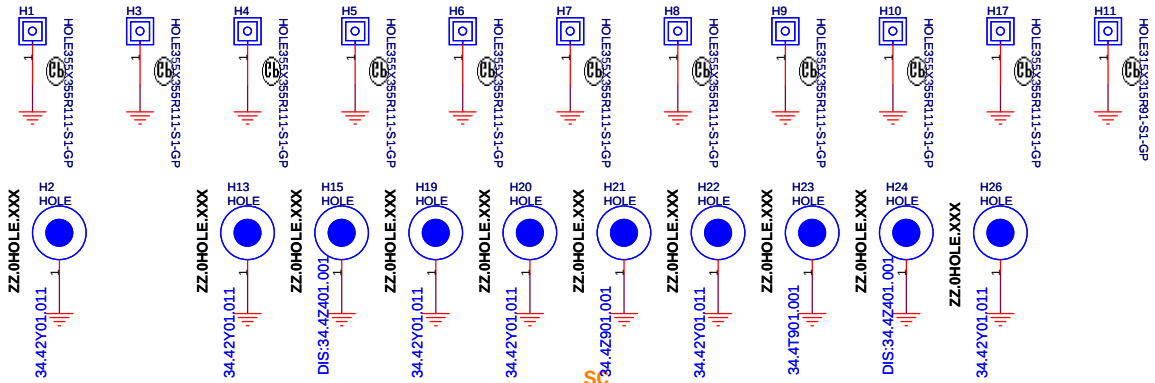
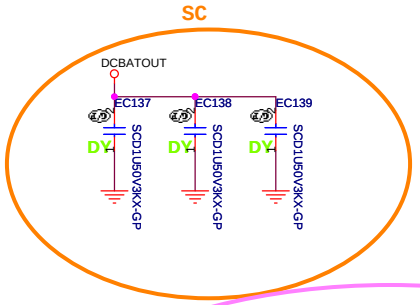
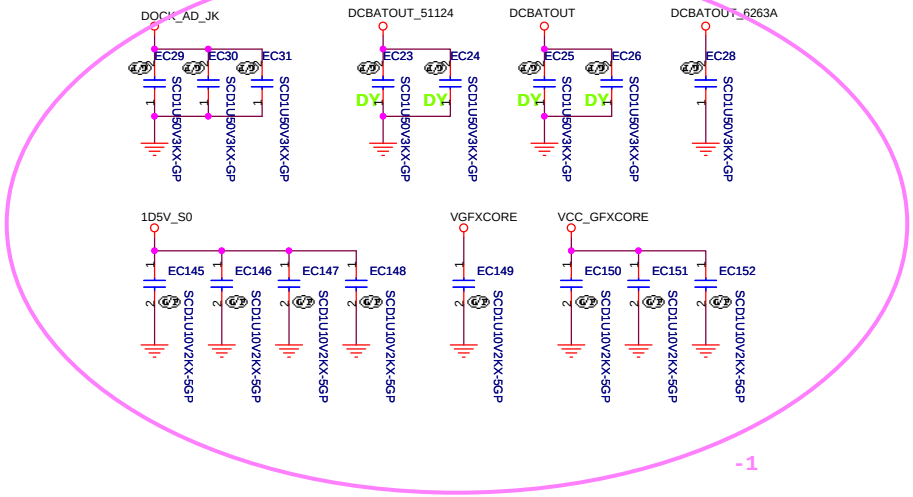

Adaptor in to generate DCBATOUT
1Pin=1A
SC 0229
DCIN_CN1
MLX-CON11-1-GP
20.F0070.011
AD_JK
DOCK_AD_JK
D4
S10P40PT-GP-U
D3
S10P40PT-GP-U
C52
C41
C40
D1
P6SBMJ24APT-GP
-1M(6/09)
R393
200KR2J-L1-GP
C403
SC1U50V5ZY-1-GP
U8
AO4433-GP
AD+
AD+ 2
4/17
AD_JK+
AD_OFF#_JK
PDTA124EU-1-GP
Q32
2nd = 84.00124.E1K
R392
100KR2J-1-GP
SB
Q33
PDTC124EU-1-GP
2nd = 84.00124.M1K
41
AD_OFF
DCN1 Conn. Test Point
AD_JK 1
TP11 AFTE30-GP
AD_JK 1
TP4 AFTE30-GP
-1M(5/30)
MAIN BATTERY CONNECTOR
3D3V_AUX_S5
D26
BAV99PT-GP-U
D27
D29
BAV99PT-GP-U
BAT1 Conn. Test Point
BATA_SCL_1
TP158 AFTE30-GP
BATA_SDA_1
TP159 AFTE30-GP
BAT_A_IN#_1
TP160 AFTE30-GP
BATA+ 1
TP260 AFTE30-GP
BATA+ 1
TP262 AFTE30-GP
SRN33J-5-GP-U
RN28
BATA_SCL_1
BATA_SDA_1
41,55 BAT_SCL
41,55 BAT_SDA
41 BAT_A_IN#
R653
33R2J-2-GP
BAT_A_IN#_1
BATA+
L13
MLVS0603N04-1-GP
EC66
EC65
EC67
EC68
EC69
SC1000P50V3JN-GP
SC10P50V2JN-4GP
BAT1
SYN-CON7-32-GP-U1
20.81021.007
20.81049.007
D43
BZG05C3V3-GP-U1
SC
DY
2D BATTERY CONNECTOR
3D3V_AUX_S5
D14
BAV99PT-GP-U
D13
D11
BAV99PT-GP-U
BATB_SCL_1
TP238 AFTE30-GP
BATB_SDA_1
TP184 AFTE30-GP
BAT_B_IN#_1
TP101 AFTE30-GP
BATB+ 1
TP265 AFTE30-GP
BATB+ 1
TP264 AFTE30-GP
-1M(5/30)
SRN33J-5-GP-U
RN16
BATB_SCL_1
BATB_SDA_1
41 THER_SCL
41 THER_SDA
41 BAT_B_IN#
R654
33R2J-2-GP
BAT_B_IN#_1
BATB+
EC50
EC51
EC73
EC49
EC48
EC47
SC1000P50V3JN-GP
SC10P50V2JN-4GP
BAT2
SYN-CON7-29-GP-U
20.81001.007
20.81038.007
D44
BZG05C3V3-GP-U1
SC
DY
G15
GAP-CLOSE-PWR
55 BATT_SENSE
CHG_PWR
CHGA
CHGB
AO4813-1-GP
Q37
DCBATOUT
BATA+
BATB+
COMA
COMB
CHG_PWRA
CHG_PWRB
DISA
DISB
Q38
Q3
-1
0425
C457
SC4D7U25V5MX-1GP
C446
SC10U25V6KX-1GP
Cherry Modify 0425
-1M(5/30)
BATTERY SWITCH
SC 0229
Cherry Modify 0425
-1
0425
Adaptor IN Detection
C401
SC4D7U25V5MX-1GP
C214
SC10U25V6KX-1GP
C406
SC10U25V6KX-1GP
C209
SC4D7U25V5MX-1GP
R437
10KR2J-3-GP
R421
10KR2J-3-GP
U14
BATA
THMA
CHGA
DISA
COMA
BATB
THMB
CHGB
DISB
COMB
BAT_A_IN#
BAT_B_IN#
BATSEL
ACDET
ACPRES#
BATSTAT
AC_IN#
TCOMP
EXTLD
PDS
MINV
GND
VDD
MAX1773AEUP-GP
41 BAT_SEL_A/B#
MAX1773_ACDET
R438
3K3R2F-2-GP
MAX1773_TCOMP
M1773_EXTLD
MAX1773_PDS
R436
10KR2J-3-GP
MAX1773_PDS 55
R441
100KR2J-1-GP
C455
SC1K50V5ZY-1-GP
R65
100KR2J-1-GP
AC_IN#
AC_IN# 41,55
3D3V_AUX_S5
MAX1773_VDD
C442
SC1U10V3ZY-6GP
R433
10KR2F-2-GP
R434
15KR2F-GP
-1
0425
D32
CH521G-30PT-GP
R428
10KR2J-3-GP
R420
100KR2J-1-GP
G54
GAP-CLOSE-PWR
Four Peaks
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AD&BTY CONNECTER & BTY SWITCH
Size
Document Number
Four Peaks
Rev
-1M
Date: Friday, November 21, 2008
Sheet 56 of 57

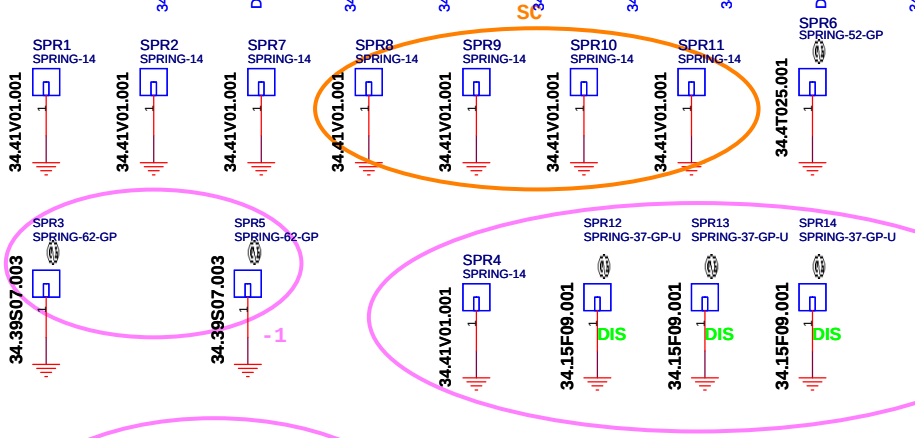


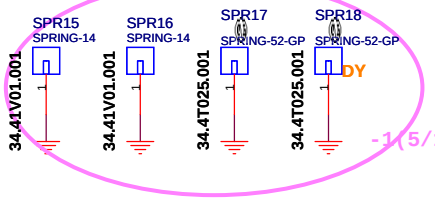
Stand off Location











Four Peaks

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: EMI/Spring/Boss

Size | Document Number: Four Peaks | Rev: -1M

Date: Friday, November 21, 2008 | Sheet 57 of 57