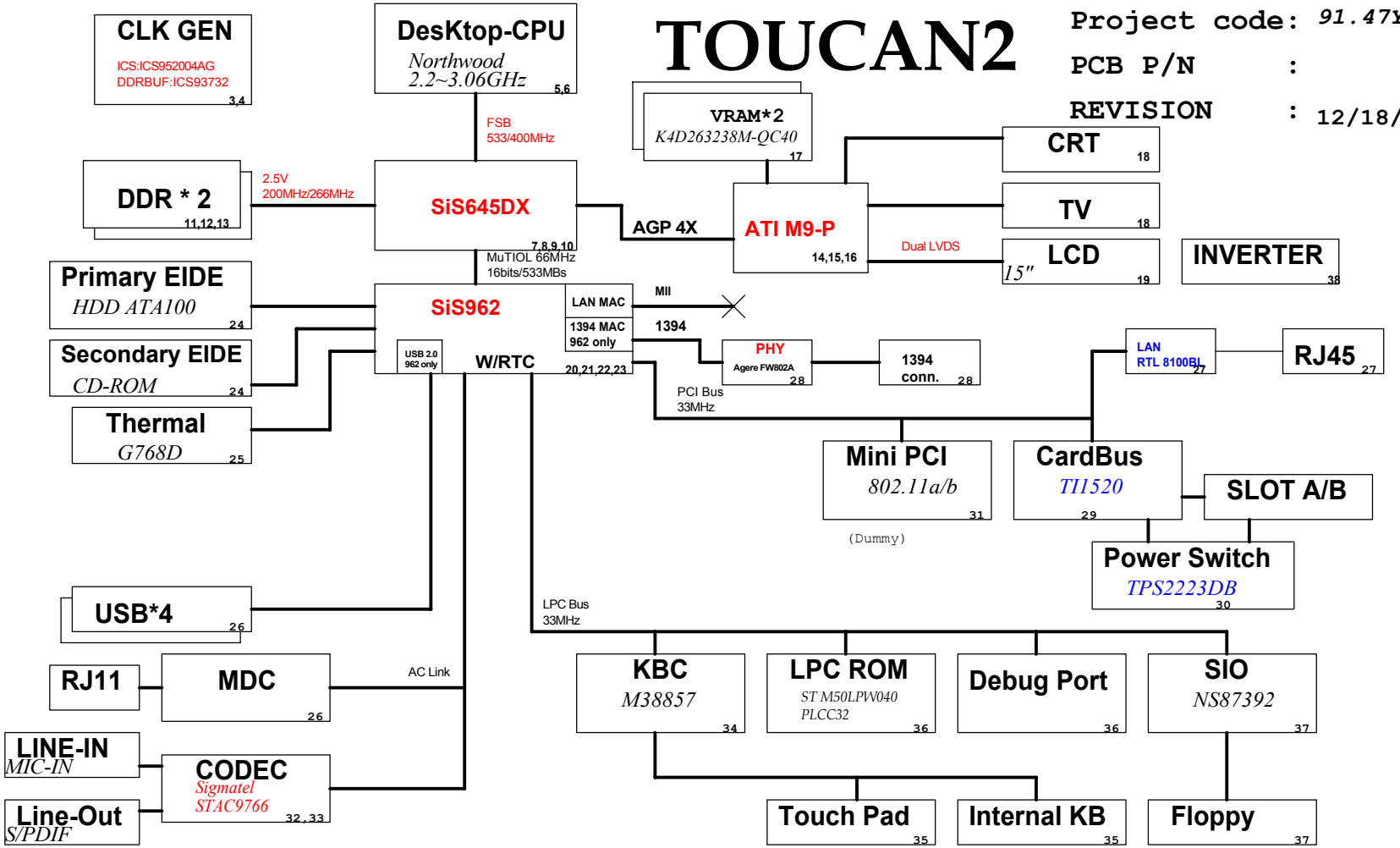
TOUCAN2

Project code: 91.47Y01.001
PCB P/N :
REVISION : 12/18/2002

PCB LAYER
- L1: Signal 1
- L2: GND
- L3: Signal 2
- L4: Signal 3
- L5: VCC
- L6: GND
- L7: Signal 4
- L8: Signal 5



POWER BOARD

SYSTEM DC/DC

MAX1631

INPUT	OUTPUT
DCBATOUT	5V_S5
	5V_S3
	3D3V_S5

CHARGER

PIC12C509 / MAX1645

INPUT	OUTPUT
AD+	BT+
AD+, BT+	UP+5V

SYSTEM DC/DC

MAX1715 / FDS9412 / APL1085 / G913C / S2N3906

INPUT	OUTPUT
DCBATOUT	5V_S0
5V_S3	3D3V_S3
3D3V_S5	3D3V_S0
	3D3V_LANAC
	1D8V_S5
	2D5V_LANAC
3D3V_LANAC	1D8V_S0
2D5V_S3 or 3D3V_S0	1D5V_S0

43,45

DDR & VDDR DC/DC

MAX1715 / CM8501 / FDS9412 / 2SB1184F5 / FDC653N

INPUT	OUTPUT
DCBATOUT	DDR_VDD = 2D5V_S3
2D5V_S3	DDR_VTT = 1D25V_S3
	VCC_VDDR = 2D5V_S0

44

CPU VCC_CORE DC/DC

DESKTOP CPU

Controller-ISL6301 Drive-ISL6207 * 3 (3 Phase)

INPUT	OUTPUT
DCBATOUT	VCC_CORE
RANGE	RANGE
9V~20V	1.1Vcore~1.85Vcore
V_VID	V_AGTL+ BUS
1D2V_VID(Northwood only) VCC_CORE(Willamette)	VCC_CORE

WILLAMETTE/NORTHWOOD) CPU

39,40,41

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Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM

Size	Document Number	Rev
A3	TOUCAN2	1

Date: Wednesday, December 18, 2002 Sheet 1 of 47

REVISION HISTORY

SA-2:

1.GPIO 16,pull-high take it away,(DUMMY R537)
2.CODEC,S/PDIF,10K PULL DOWN (ADD R539)
3.PANEL ID FROM SIO
4.LCDPOWER_S0 FUSE/1A (RAYCHEM)
5.USB .fuse-->RAYCHEM
6.RTL8100.PIN80-->1K-->3D3V
7.FDD POWER RAIL-->1A FUSE
8.CODECP/N UPDATE:71.09766.A0G
9.DB1,DB3,DB4 CHANGE SOURCE

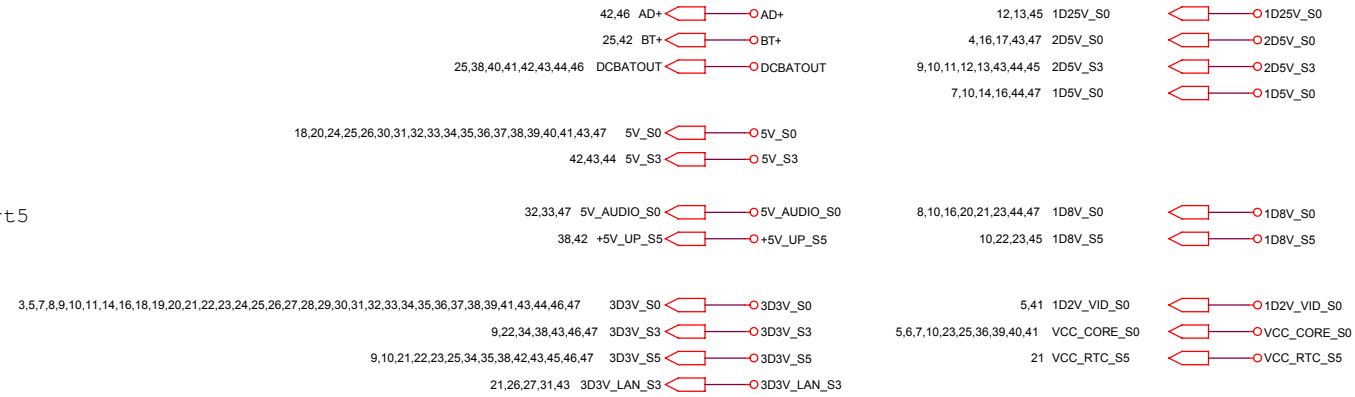
NOTE:
1.F2 : NOT RAYCHEM

SB:
1. REPLACE F5 with type of F1 (ok)
2. U35,pin4 MUST PH 47K(R280)? (No)
3. PUT R537 BACK? (no)
4. audio:short BC617,BC584?(no)
5. audio:remove BC583,R139,R138,BC135(no)
5. audio:remove BC618,R180,R181,BC164(no)
7. audio:modify BC584 and BC617 to 33nF(no)
8. CPU ripple issue:capacitor-->77.22271.071(ok)
9. BC8,BC21-->DUMMY
10. EMI:L5,L8,L11,L14,L15,L33,L40,L41,L42,L43(68.00082.321)-->0805 0Ohm
EMI:L1(68.00089.081)-->delete
EMI:L30(63.R0003.161)-->0805 0Ohm
EMI:L31(68.4R72B.1F1)-->0805 0Ohm
11.USB,1 fuse for 1 port
12. 2*4P 14.318MHz
13 DB10
14 MIC C42
15 BL3
16 WOL
17 text on Page21
18 TC11 shift 1mm
19 CLK33_PCM

SC
1.Board revision ID
2.USB controller change;replace USB port3 with port5
3.KBC-P60-->EN_MINI_PCI
4.VGA floating input-->PD "SSIN","SSOUT",HPD"
5.

PCI RESOURCE TABLE

DEVICE	IDSEL	PCI IRQ	REQ# / GNT#
INTERNAL_LAN	AD13	INTC#/INTG#	
EXTERNAL_LAN	AD18	INTD#	REQ4#/GNT4#
Mini-PCI	AD21	INTC#	REQ3#/GNT3#
IEEE 1394	AD13		
USB 2.0	AD14		
USB 1.1	AD14	INTD#/INTE# INTD#/INTH#	
CARDBUS	AD20	INTA#	REQ1#/GNT1#
LPC	AD13		
AC97	AD13	INTC#/INTF#	
IDE	AD13	INTH#	



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Title: **REVISION HISTORY**

Size	Document Number	Rev
A3	TOUCAN2	1

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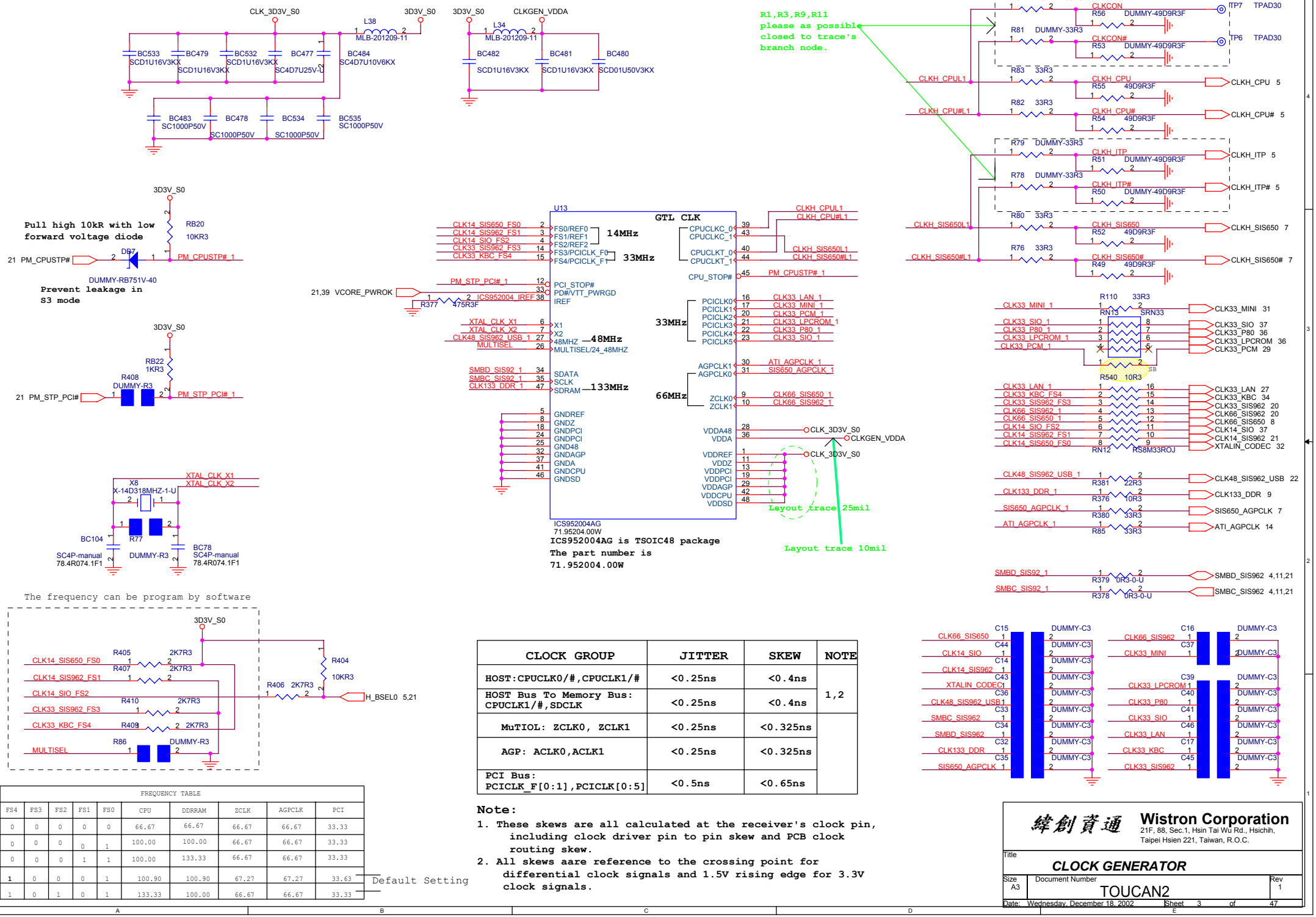

CLOCK GROUP	JITTER	SKEW	NOTE
HOST:CPUCLK0/#,CPUCLK1/#	<0.25ns	<0.4ns	1,2
HOST Bus To Memory Bus: CPUCLK1/#,SDCLK	<0.25ns	<0.4ns	
MuTIOL: ZCLK0, ZCLK1	<0.25ns	<0.325ns	
AGP: ACLK0,ACLK1	<0.25ns	<0.325ns	
PCI Bus: PCICLK_F[0:1],PCICLK[0:5]	<0.5ns	<0.65ns	

FREQUENCY TABLE

FS4	FS3	FS2	FS1	FS0	CPU	DDRRAM	ZCLK	AGPCLK	PCI
0	0	0	0	0	66.67	66.67	66.67	66.67	33.33
0	0	0	0	1	100.00	100.00	66.67	66.67	33.33
0	0	0	1	1	100.00	133.33	66.67	66.67	33.33
1	0	0	0	1	100.90	100.90	67.27	67.27	33.63
1	0	1	0	1	133.33	100.00	66.67	66.67	33.33

Default Setting

Note:

1. These skews are all calculated at the receiver's clock pin, including clock driver pin to pin skew and PCB clock routing skew.
2. All skews aare reference to the crossing point for differential clock signals and 1.5V rising edge for 3.3V clock signals.

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Title: **CLOCK GENERATOR**

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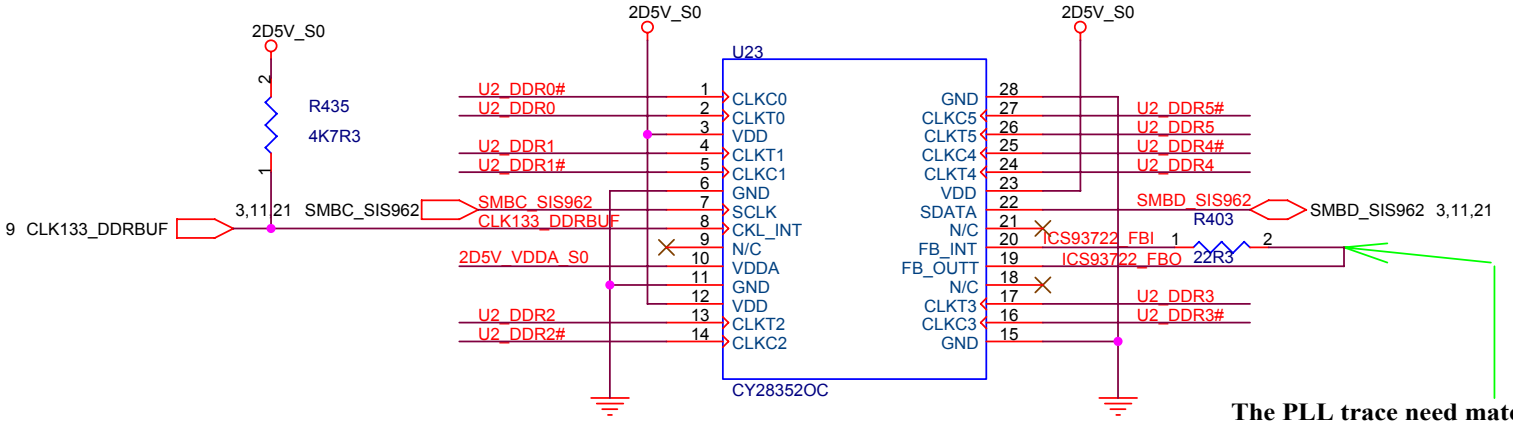
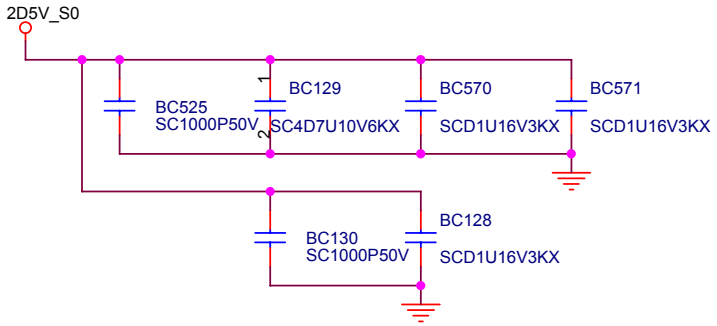
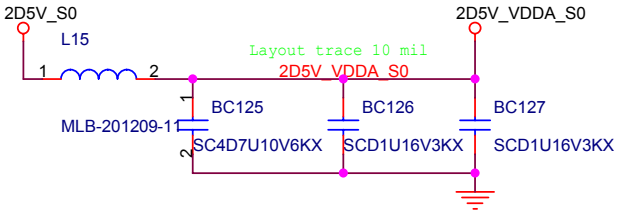
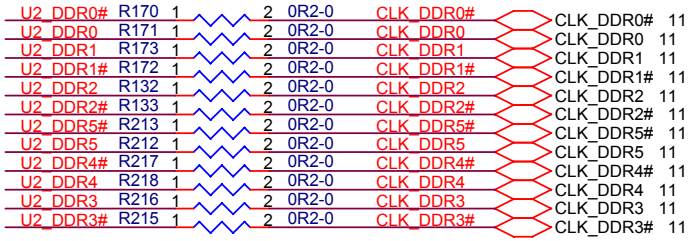


H2U
P/N:71.93732.00I

The PLL trace need match the specific
L4 = L2+L3-L1+3.2"
L2 : SiS645 to Buffer length.(< 6")
L3 : Buffer to DIMM socket length.(<4")
L1 : 2 " ~ 4"(SIS645 to DDR-Socket)
L4 = need less 12.6"







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Title: ***DDRCLK_BUFFER***

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A4	TOUCAN2	1

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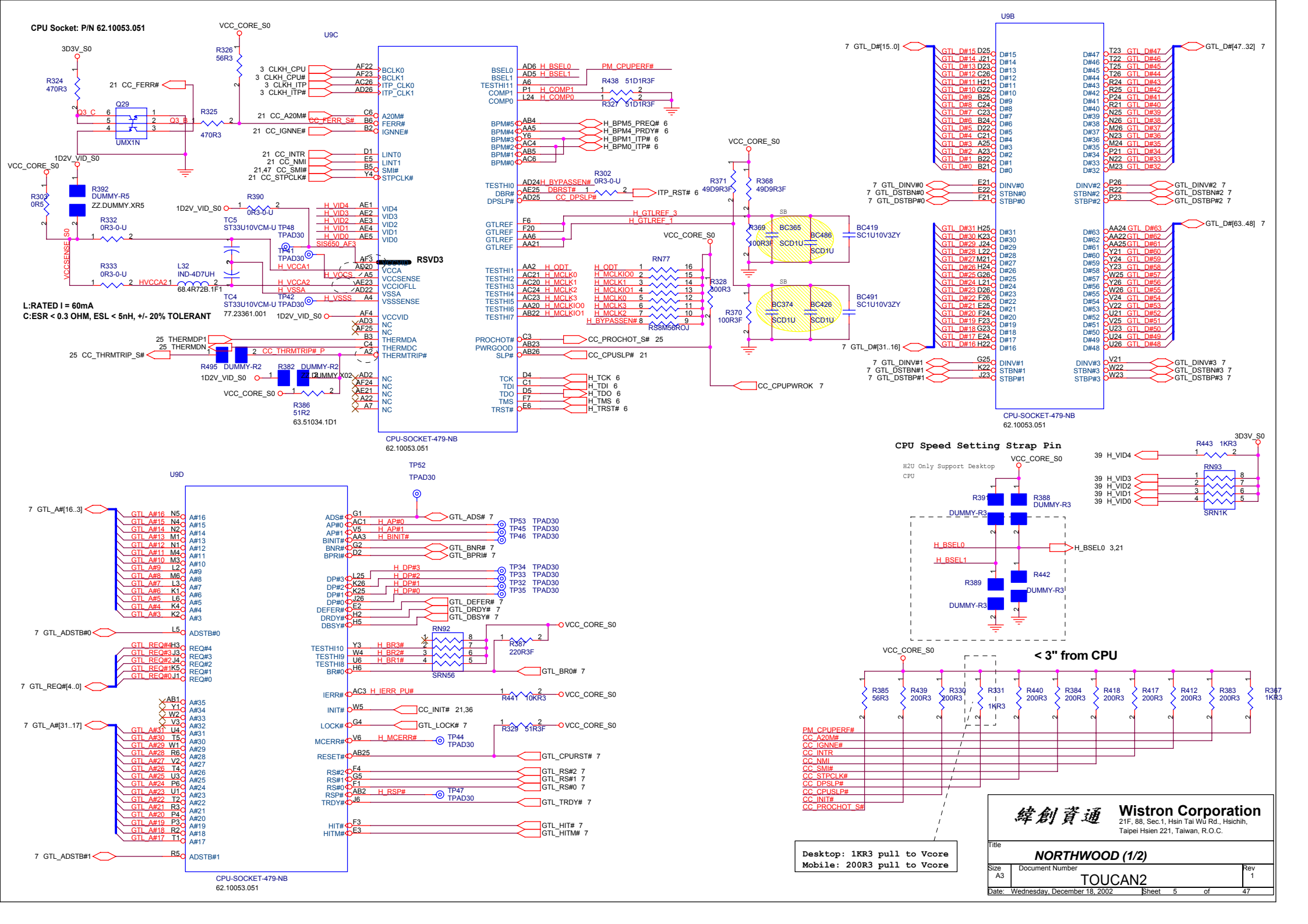
CPU Socket: P/N 62.10053.051
U9C
CPU-SOCKET-479-NB
62.10053.051
L:RATED I = 60mA
C:ESR < 0.3 OHM, ESL < 5nH, +/- 20% TOLERANT
RSVD3
U9B
CPU-SOCKET-479-NB
62.10053.051
CPU Speed Setting Strap Pin
H2U Only Support Desktop CPU
< 3" from CPU
Desktop: 1KR3 pull to Vcore
Mobile: 200R3 pull to Vcore
U9D
CPU-SOCKET-479-NB
62.10053.051
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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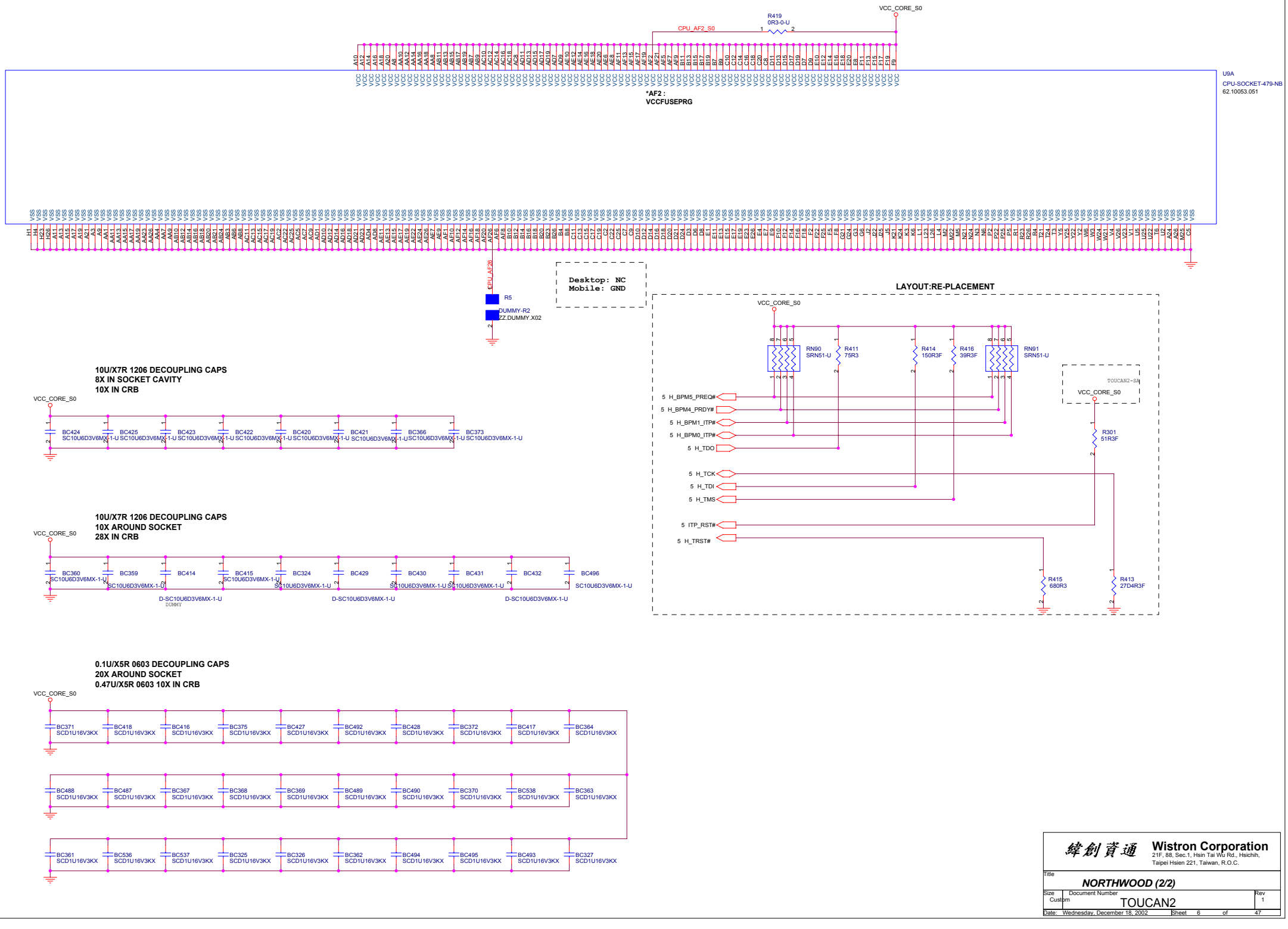
Title
NORTHWOOD (1/2)
Size A3
Document Number
TOUCAN2
Rev 1
Date: Wednesday, December 18, 2002
Sheet 5 of 47



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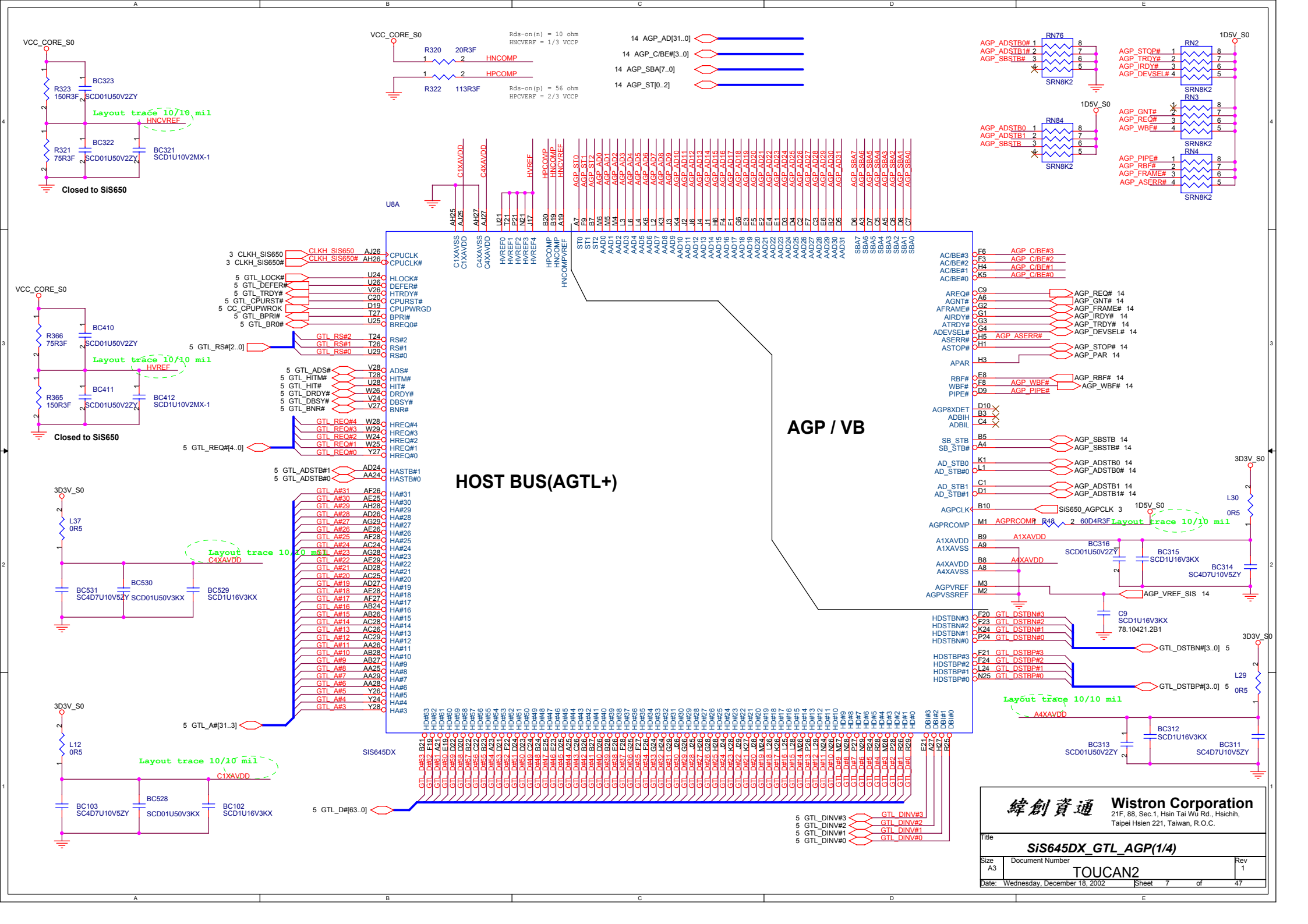
Title: ***NORTHWOOD (2/2)***

Size: Custom | Document Number: TOUCAN2 | Rev: 1

Date: Wednesday, December 18, 2002 | Sheet 6 of 47


HOST BUS(AGTL+)
AGP / VB
SIS645DX
U8A
VCC_CORE_S0
Layout trace 10/10 mil
Closed to SiS650
HNCVREF
HVREF
C4XAVDD
C1XAVDD
A4XAVDD
1D5V_S0
3D3V_S0
Rds-on(n) = 10 ohm
HNCVERF = 1/3 VCCP
Rds-on(p) = 56 ohm
HPCVERF = 2/3 VCCP
HNCOMP
HPCOMP
14 AGP_AD[31..0]
14 AGP_C/BE#[3..0]
14 AGP_SBA[7..0]
14 AGP_ST[0..2]
5 GTL_A#[31..3]
5 GTL_D#[63..0]
5 GTL_REQ#[4..0]
5 GTL_RS#[2..0]
5 GTL_DSTBN#[3..0]
5 GTL_DSTBP#[3..0]
5 GTL_DINV#3
5 GTL_DINV#2
5 GTL_DINV#1
5 GTL_DINV#0
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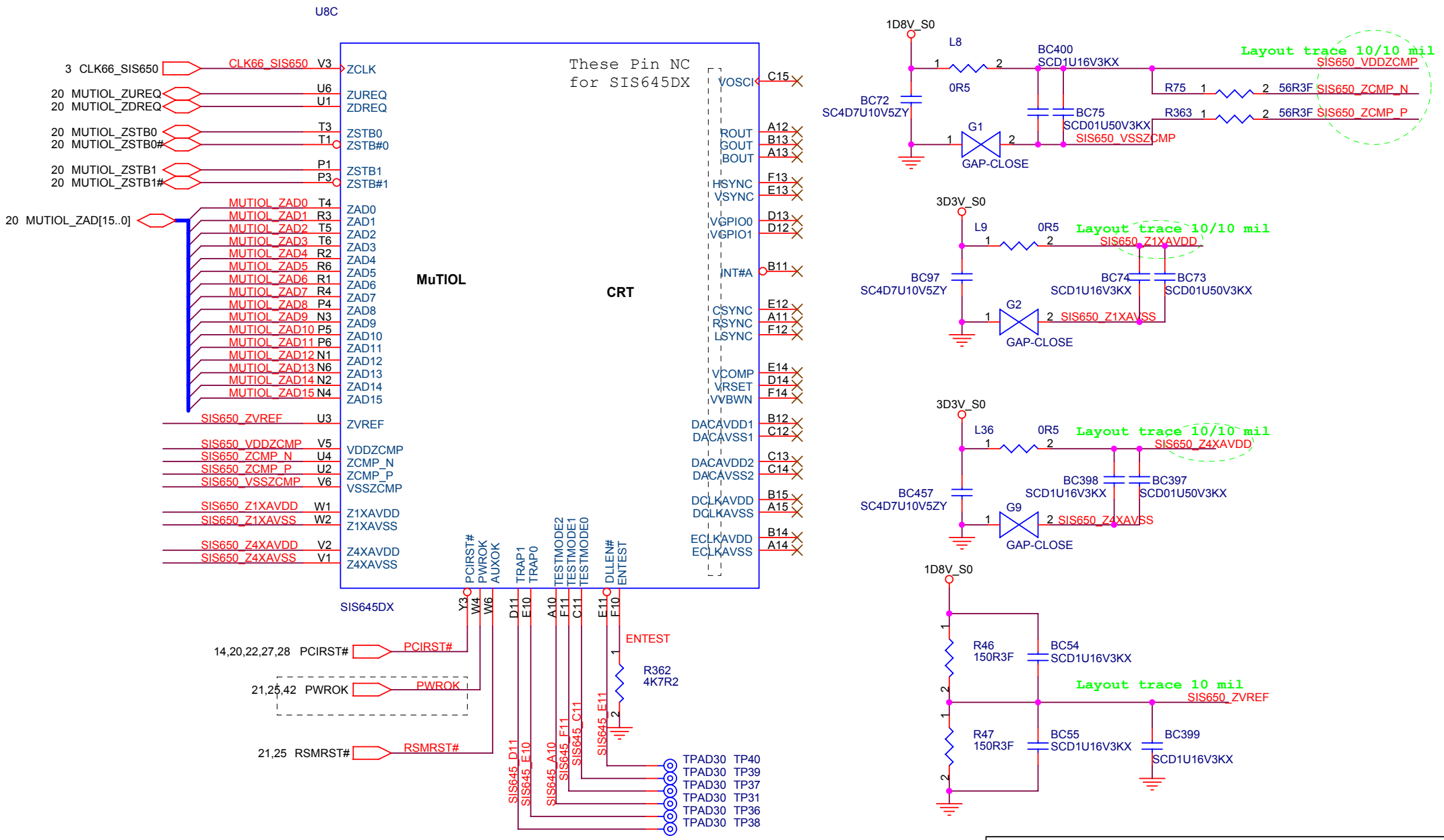
SiS645DX_GTL_AGP(1/4)
TOUCAN2
Size A3
Rev 1
Date: Wednesday, December 18, 2002
Sheet 7 of 47



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Title: ***SiS645DX_MuTIOL(2/4)***

Size	Document Number	Rev
A4	TOUCAN2	1

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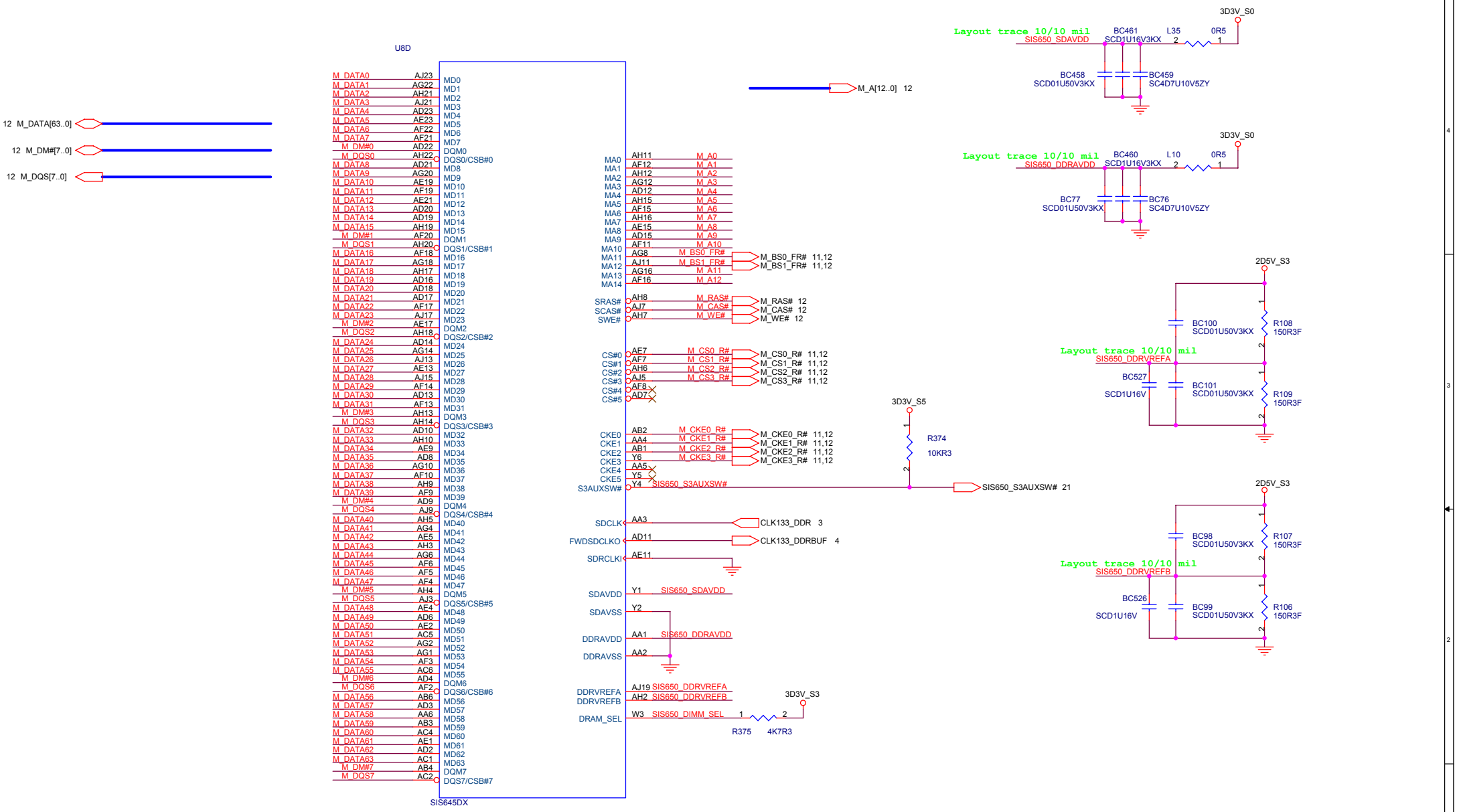

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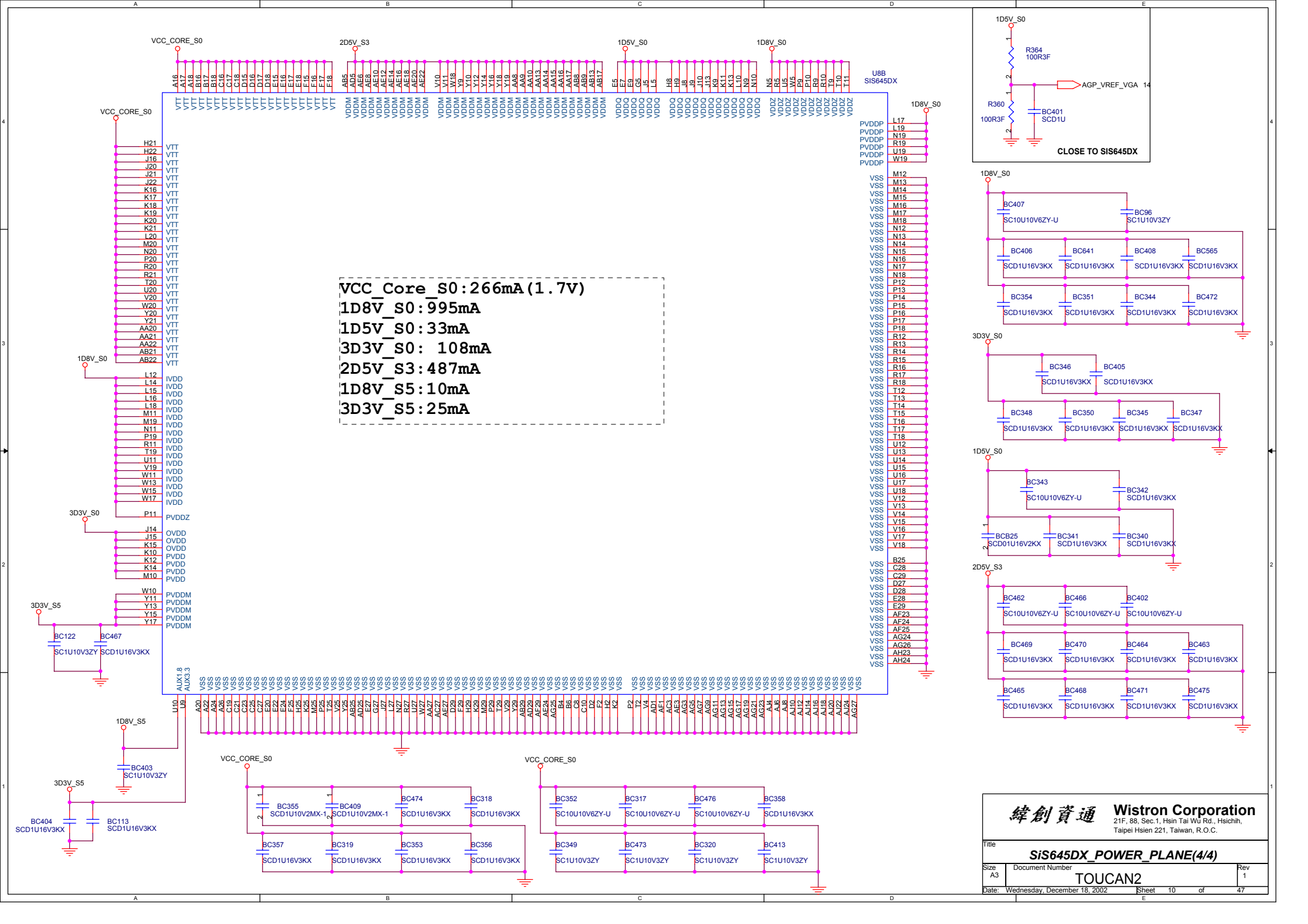
Title: *SiS645DX-DDRRAM(3/4)*	
Size: A3	Document Number: TOUCAN2
Rev: 1	
Date: Wednesday, December 18, 2002	Sheet 9 of 47


VCC_Core_S0:266mA(1.7V)
1D8V_S0:995mA
1D5V_S0:33mA
3D3V_S0: 108mA
2D5V_S3:487mA
1D8V_S5:10mA
3D3V_S5:25mA
U8B
SIS645DX
CLOSE TO SIS645DX
R364
100R3F
R360
100R3F
BC401
SCD1U
AGP_VREF_VGA
Wistron Corporation
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SiS645DX_POWER_PLANE(4/4)
TOUCAN2
Size A3
Rev 1
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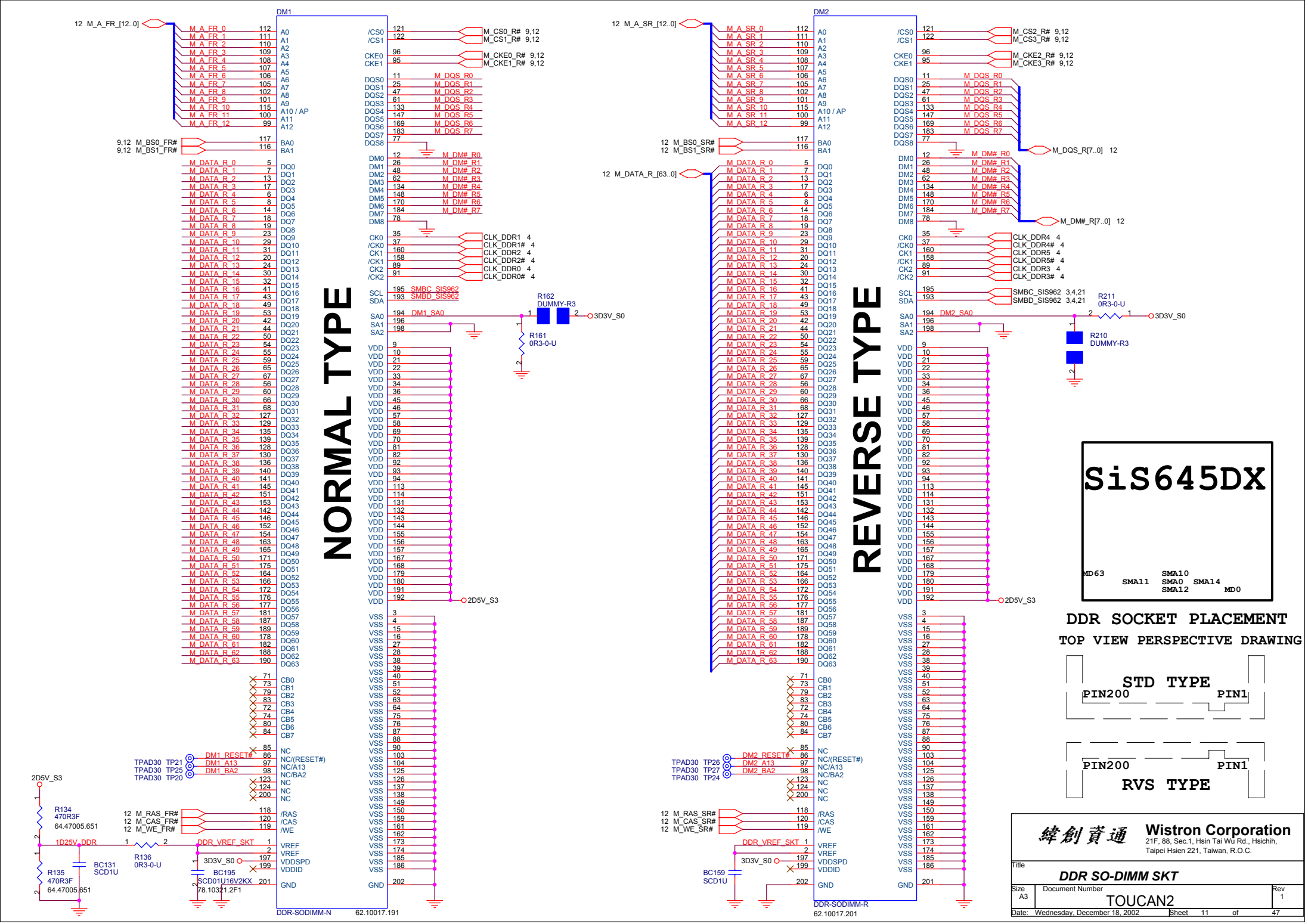
DM1
NORMAL TYPE
DDR-SODIMM-N
62.10017.191
DM2
REVERSE TYPE
DDR-SODIMM-R
62.10017.201
SiS645DX
MD63
SMA10
SMA11
SMA0
SMA14
SMA12
MD0
DDR SOCKET PLACEMENT
TOP VIEW PERSPECTIVE DRAWING
STD TYPE
PIN200
PIN1
PIN200
PIN1
RVS TYPE
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Title
DDR SO-DIMM SKT
Size
A3
Document Number
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1
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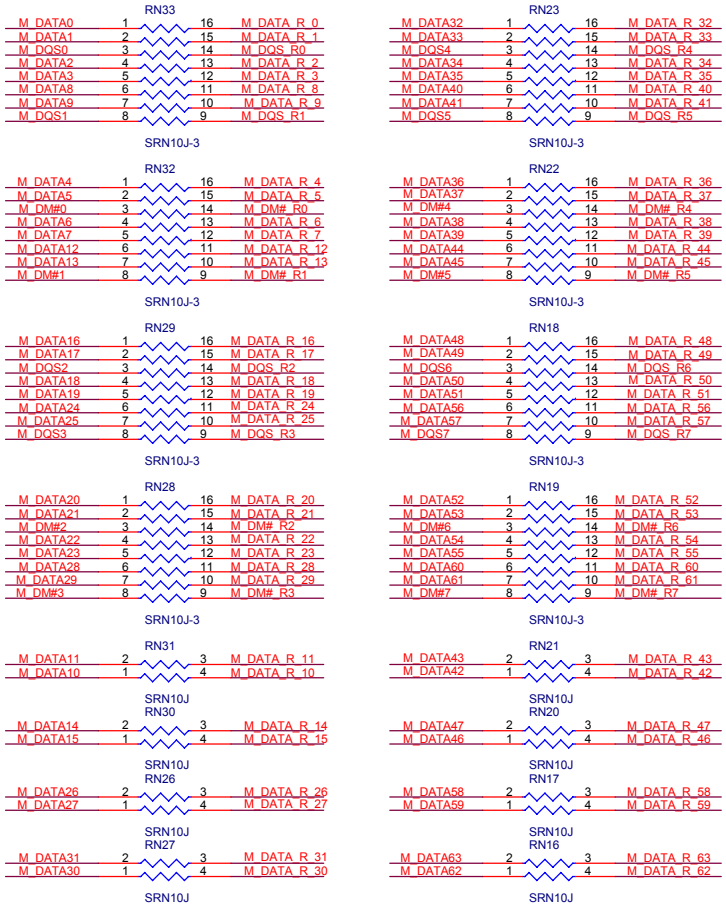
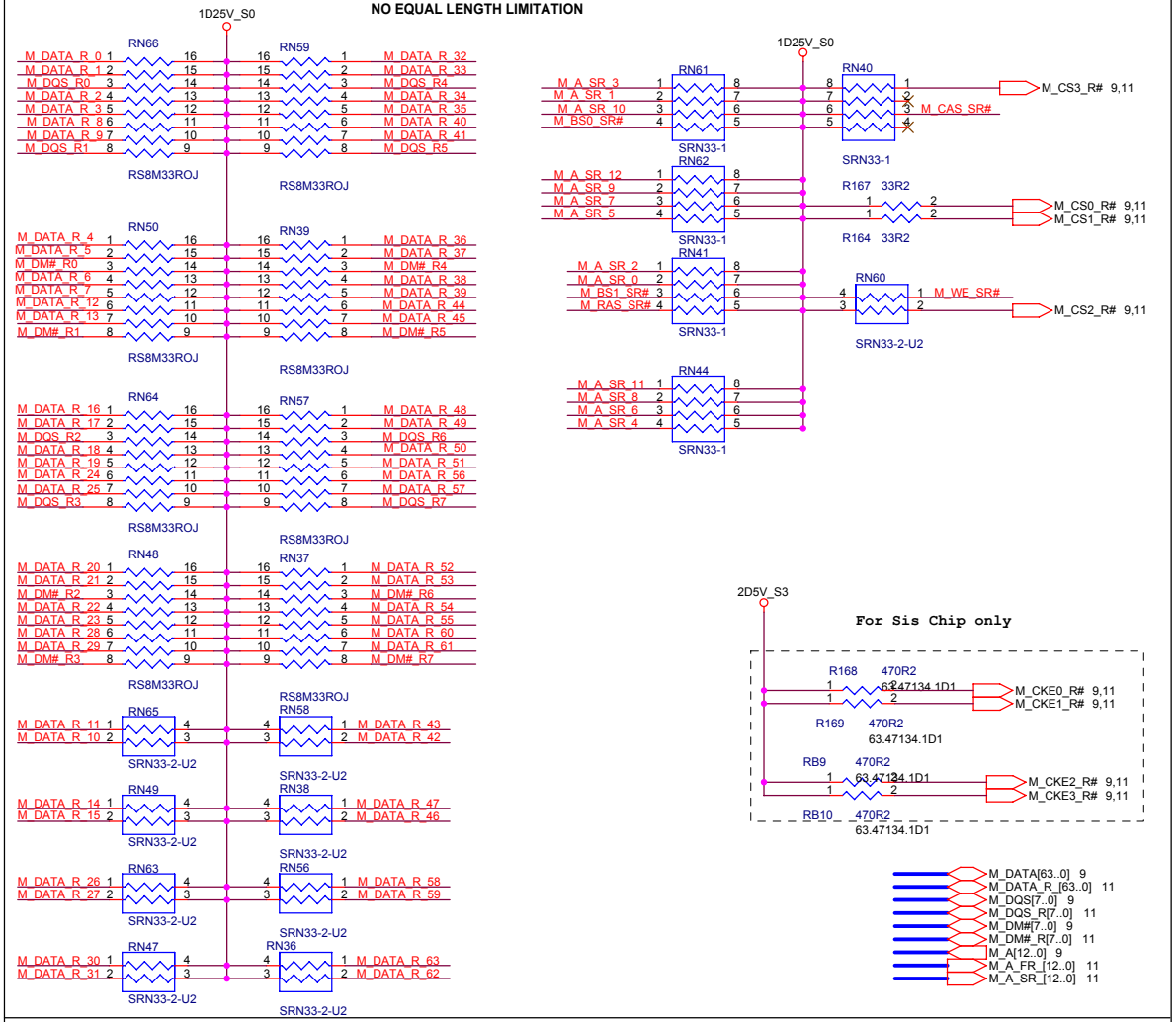
SERIES DAMPING

PLACE RNs CLOSE TO FIRST DM (DM2), < 0.75"
STRICT EQUAL LENGTH LIMITATION WITH DQS, CB PINS

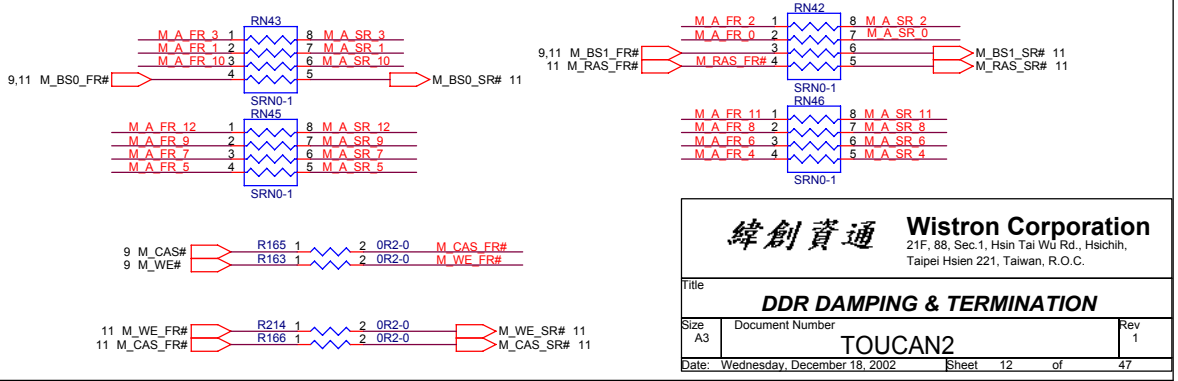


PARALLEL TERMINATION

PULL HIGH STUBS < 0.8", PLACE RPs CLOSE TO SECOND DM (DM1)
NO EQUAL LENGTH LIMITATION



PLACE BETWEEN DM1, DM2
CLOSE TO FIRST DM (DM 2) < 0.2", TO SECOND DM (DM1) < 1.1"
EQUAL LENGTH LIMITATION WITH SCK/SCK#



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Title: ***DDR DAMPING & TERMINATION***

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A3	TOUCAN2	1

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PLACE ONE CAP CLOSE TO EVERY 2 PULL-UP TERMINATION RESISTORS,
CRB-P13
DATA(64)+ADD(13)+DQS(9)+CB(8)+CMD(13)=107
0.1UF 0603 Y5V 27X

1D25V_S0

BC225 SCD1U, BC224 SCD1U, BC222 SCD1U, BC221 SCD1U, BC185 SCD1U, BC187 SCD1U, BC191 SCD1U, BC196 SCD1U, BC181 SCD1U, BC179 SCD1U, BC188 SCD1U

BC218 SCD1U, BC223 SCD1U, BC226 SCD1U, BC219 SCD1U, BC178 SCD1U, BC213 SCD1U, BC220 SCD1U, BC182 SCD1U, BC183 SCD1U, BC176 SCD1U, BC193 SCD1U

BC212 SCD1U, BC211 SCD1U, BC190 SCD1U, BC197 SCD1U, BC184 SCD1U, BC215 SCD1U, BC214 SCD1U

PLACE CAPS BETWEEN AND NEAR DDR SKTS
PLACE EACH 0.1UF CAP CLOSE TO POWER PIN

2D5V_S3

BC576 SCD1U, BC575 SCD1U, BC157 SCD1U, BC155 SCD1U, BC568 SCD1U, BC569 SCD1U, BC572 SCD1U, BC573 SCD1U

BC574 SCD1U, BC194 SCD1U, BC192 SCD1U, BC189 SCD1U, BC180 SCD1U, BC186 SCD1U, BC177 SCD1U, BC153 SCD1U

BC156 SCD1U, BC158 SC4D7U16V6ZY-U, BC154 SC4D7U16V6ZY-U

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Title: ***DDR DECOUPLING***

Size	Document Number	Rev
A4	TOUCAN2	1

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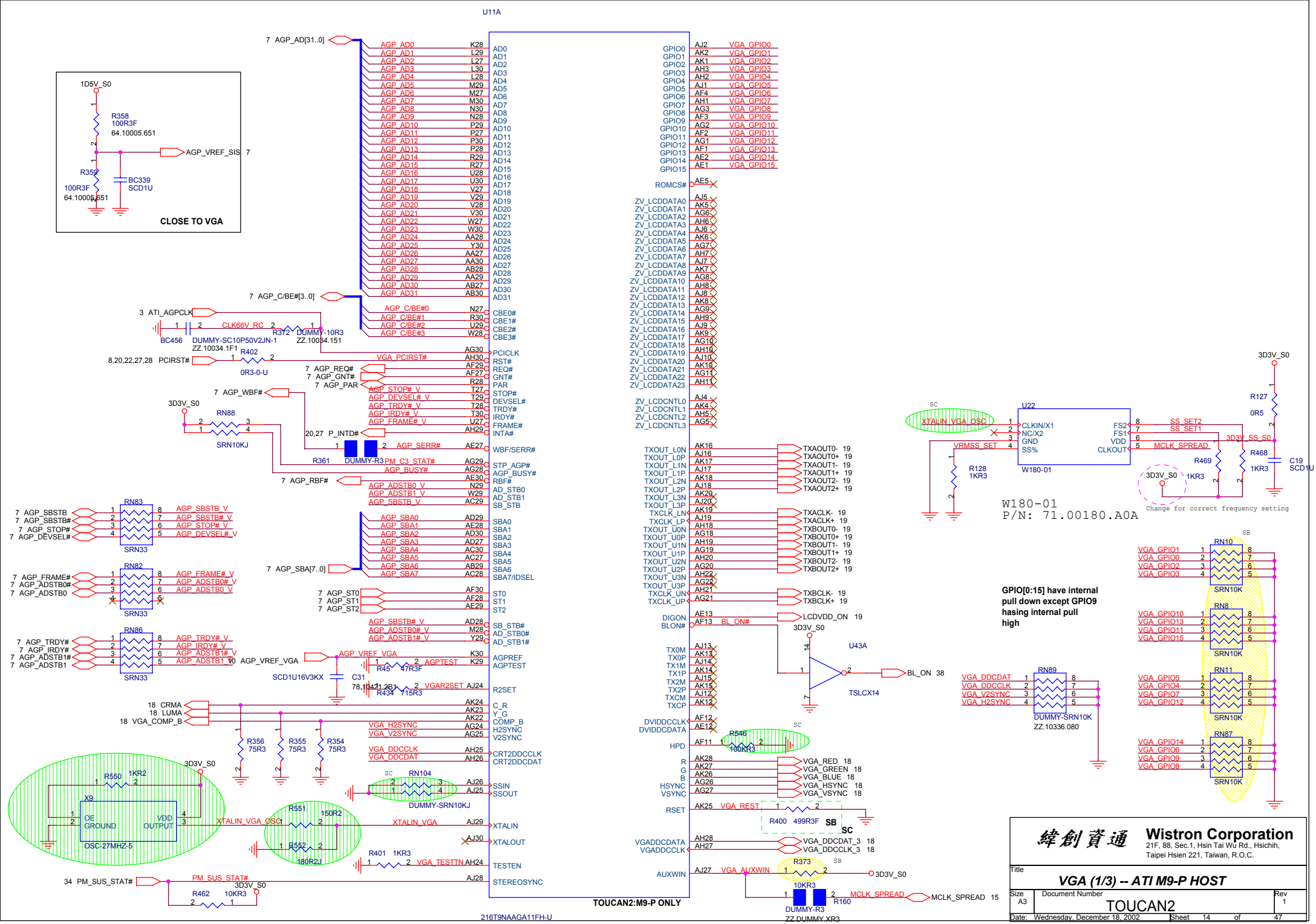
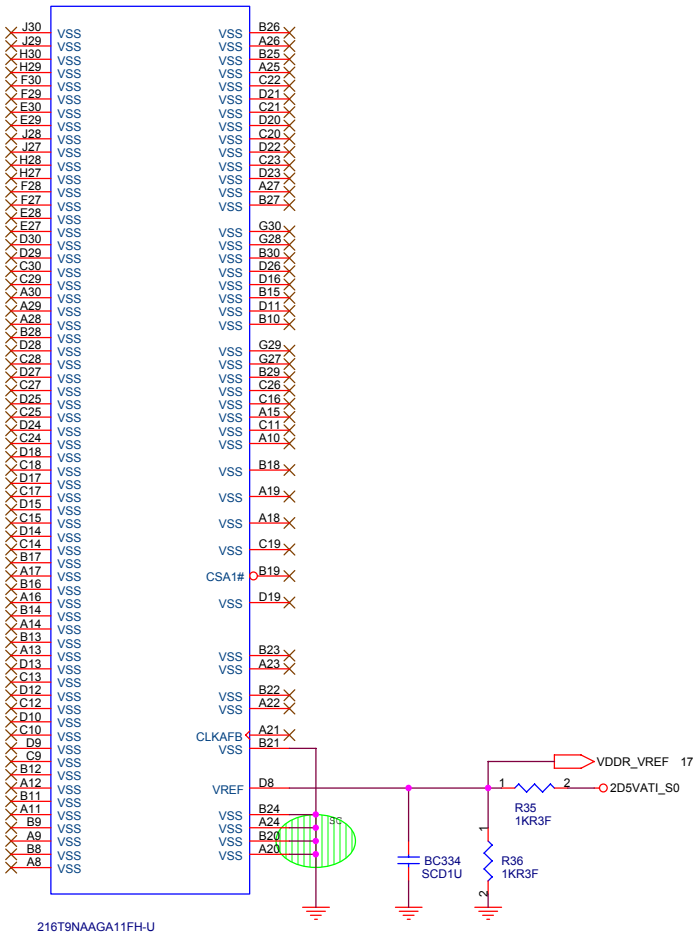

U11A
TOUCAN2:M9-P ONLY
216T9NAAGA11FH-U
CLOSE TO VGA
1D5V_S0
R358 100R3F 64.10005.651
R359 100R3F 64.10005.651
BC339 SCD1U
AGP_VREF_SIS 7
7 AGP_AD[31..0]
7 AGP_C/BE#[3..0]
3 ATI_AGPCLK
CLK66V_RC
BC456 DUMMY-SC10P50V2JN-1 ZZ.10034.1F1
R372 DUMMY-10R3 ZZ.10034.151
8,20,22,27,28 PCIRST#
R402 0R3-0-U
VGA_PCIRST#
7 AGP_REQ#
7 AGP_GNT#
7 AGP_PAR
7 AGP_WBF#
7 AGP_RBF#
3D3V_S0
RN88 SRN10KJ
20,27 P_INTD#
R361 DUMMY-R3
PM_C3_STAT#
AGP_BUSY#
AGP_SERR#
AGP_STOP# AGP_DEVSEL# AGP_TRDY# AGP_IRDY# AGP_FRAME# AGP_ADSTB0_V AGP_ADSTB1_V AGP_SBSTB_V
RN83 SRN33
RN82 SRN33
RN86 SRN33
7 AGP_SBA[7..0]
7 AGP_ST0 7 AGP_ST1 7 AGP_ST2
AGP_SBSTB# AGP_ADSTB0# AGP_ADSTB1#
AGP_VREF_VGA
SCD1U16V3KX C31
R45 47R3F
R434 715R3
VGAR2SET
18 CRMA 18 LUMA 18 VGA_COMP_B
R356 75R3 R355 75R3 R354 75R3
VGA_H2SYNC VGA_V2SYNC VGA_DDCCLK VGA_DDCDAT
SC RN104 DUMMY-SRN10KJ
3D3V_S0
R550 1KR2
X9 OSC-27MHZ-5
XTALIN_VGA_OSC
R551 150R2
R552 180R2U
XTALIN_VGA
XTALOUT
R401 1KR3
VGA_TESTTN
TESTEN
STEREOSYNC
34 PM_SUS_STAT#
R462 10KR3
AGP_AD0 AGP_AD1 AGP_AD2 AGP_AD3 AGP_AD4 AGP_AD5 AGP_AD6 AGP_AD7 AGP_AD8 AGP_AD9 AGP_AD10 AGP_AD11 AGP_AD12 AGP_AD13 AGP_AD14 AGP_AD15 AGP_AD16 AGP_AD17 AGP_AD18 AGP_AD19 AGP_AD20 AGP_AD21 AGP_AD22 AGP_AD23 AGP_AD24 AGP_AD25 AGP_AD26 AGP_AD27 AGP_AD28 AGP_AD29 AGP_AD30 AGP_AD31
AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10 AD11 AD12 AD13 AD14 AD15 AD16 AD17 AD18 AD19 AD20 AD21 AD22 AD23 AD24 AD25 AD26 AD27 AD28 AD29 AD30 AD31
AGP_C/BE#0 AGP_C/BE#1 AGP_C/BE#2 AGP_C/BE#3
CBE0# CBE1# CBE2# CBE3#
PCICLK RST# REQ# GNT# PAR STOP# DEVSEL# TRDY# IRDY# FRAME# INTA# WBF/SERR# STP_AGP# AGP_BUSY# RBF# AD_STB0 AD_STB1 SB_STB
SBA0 SBA1 SBA2 SBA3 SBA4 SBA5 SBA6 SBA7/IDSEL
ST0 ST1 ST2
SB_STB# AD_STB0# AD_STB1#
AGPREF AGPTEST R2SET C_R Y_G COMP_B H2SYNC V2SYNC CRT2DDCCLK CRT2DDCDAT SSIN SSOUT XTALIN XTALOUT TESTEN STEREOSYNC
GPIO0 GPIO1 GPIO2 GPIO3 GPIO4 GPIO5 GPIO6 GPIO7 GPIO8 GPIO9 GPIO10 GPIO11 GPIO12 GPIO13 GPIO14 GPIO15
VGA_GPIO0 VGA_GPIO1 VGA_GPIO2 VGA_GPIO3 VGA_GPIO4 VGA_GPIO5 VGA_GPIO6 VGA_GPIO7 VGA_GPIO8 VGA_GPIO9 VGA_GPIO10 VGA_GPIO11 VGA_GPIO12 VGA_GPIO13 VGA_GPIO14 VGA_GPIO15
ROMCS#
ZV_LCDDATA0 ZV_LCDDATA1 ZV_LCDDATA2 ZV_LCDDATA3 ZV_LCDDATA4 ZV_LCDDATA5 ZV_LCDDATA6 ZV_LCDDATA7 ZV_LCDDATA8 ZV_LCDDATA9 ZV_LCDDATA10 ZV_LCDDATA11 ZV_LCDDATA12 ZV_LCDDATA13 ZV_LCDDATA14 ZV_LCDDATA15 ZV_LCDDATA16 ZV_LCDDATA17 ZV_LCDDATA18 ZV_LCDDATA19 ZV_LCDDATA20 ZV_LCDDATA21 ZV_LCDDATA22 ZV_LCDDATA23
ZV_LCDCNTL0 ZV_LCDCNTL1 ZV_LCDCNTL2 ZV_LCDCNTL3
TXOUT_L0N TXOUT_L0P TXOUT_L1N TXOUT_L1P TXOUT_L2N TXOUT_L2P TXOUT_L3N TXOUT_L3P TXCLK_LN TXCLK_LP TXOUT_U0N TXOUT_U0P TXOUT_U1N TXOUT_U1P TXOUT_U2N TXOUT_U2P TXOUT_U3N TXOUT_U3P TXCLK_UN TXCLK_UP
TXAOUT0- 19 TXAOUT0+ 19 TXAOUT1- 19 TXAOUT1+ 19 TXAOUT2- 19 TXAOUT2+ 19
TXACLK- 19 TXACLK+ 19 TXBOUT0- 19 TXBOUT0+ 19 TXBOUT1- 19 TXBOUT1+ 19 TXBOUT2- 19 TXBOUT2+ 19
TXBCLK- 19 TXBCLK+ 19
DIGON BLON# BL_ON#
LCDVDD_ON 19
3D3V_S0
U43A TSLCX14
BL_ON 38
TX0M TX0P TX1M TX1P TX2M TX2P TXCM TXCP
DVIDDCCLK DVIDDCDATA
HPD
R546 160KR3
R G B HSYNC VSYNC
VGA_RED 18 VGA_GREEN 18 VGA_BLUE 18 VGA_HSYNC 18 VGA_VSYNC 18
RSET
R400 499R3F SB SC
VGADDCDATA VGADDCCLK
VGA_DDCDAT_3 18 VGA_DDCCLK_3 18
AUXWIN VGA_AUXWIN
R373 10KR3
R160 DUMMY-R3 ZZ.DUMMY-XR3
MCLK_SPREAD MCLK_SPREAD 15
U22 W180-01
XTALIN_VGA_OSC
CLKIN/X1 NC/X2 GND SS%
VRMSS_SET
FS2 FS1 VDD CLKOUT
SS_SET2 SS_SET1 3D3V_SS_S0 MCLK_SPREAD
R128 1KR3 R469 R468 1KR3 C19 SCD1U
Change for correct frequency setting
W180-01
P/N: 71.00180.A0A
GPIO[0:15] have internal pull down except GPIO9 hasing internal pull high
RN10 RN8 RN11 RN87 SRN10K
RN89 DUMMY-SRN10K ZZ.10336.080
VGA_DDCDAT VGA_DDCCLK VGA_V2SYNC VGA_H2SYNC
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
VGA (1/3) -- ATI M9-P HOST
Size A3
Document Number TOUCAN2
Rev 1
Date: Wednesday, December 18, 2002
Sheet 14 of 47

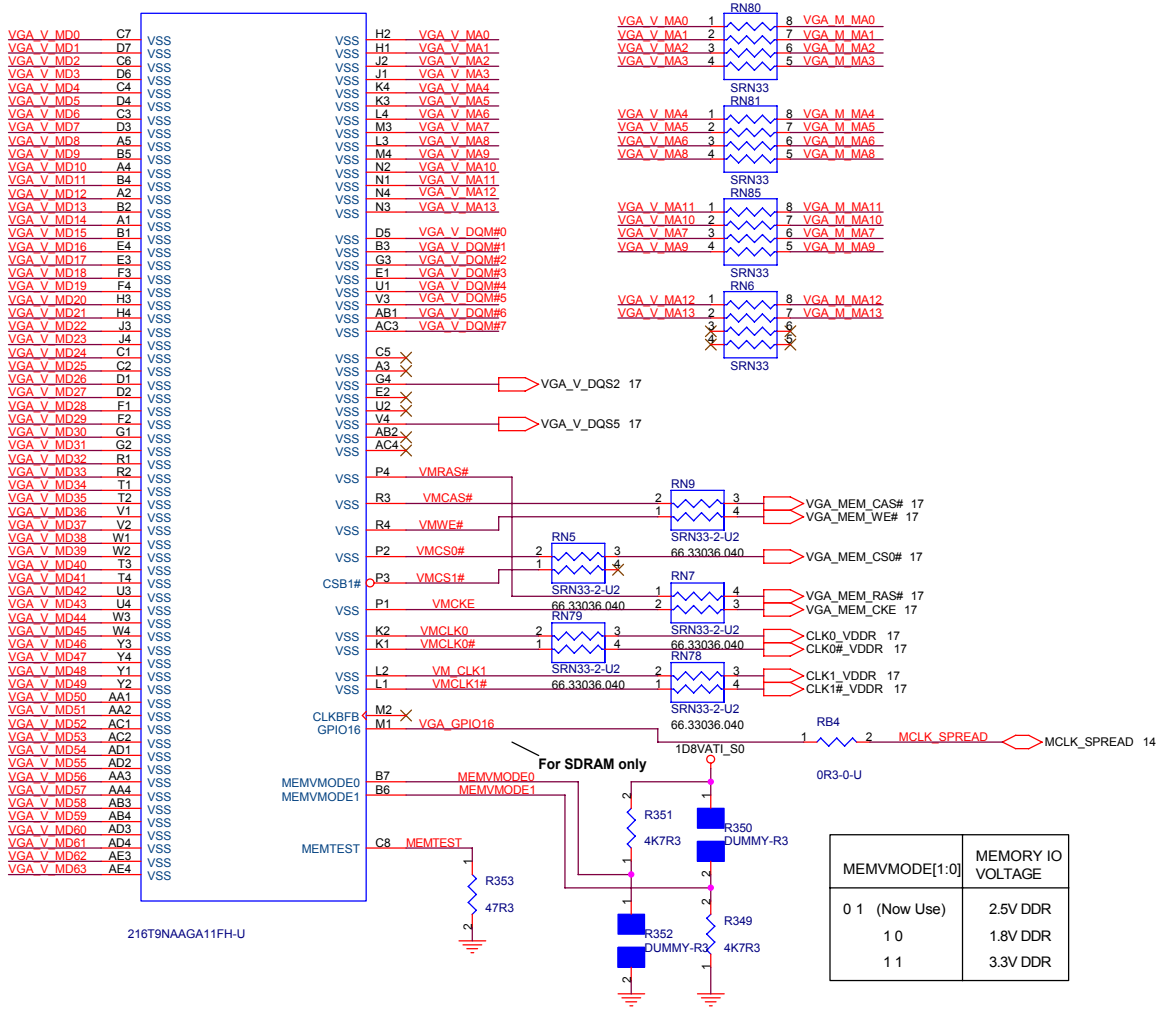
17 VGA_V_MD[0..63]
17 VGA_M_MA[0..13]
17 VGA_V_DQM#[0..7]

U11B



U11C

All these dampings must near M9-P.



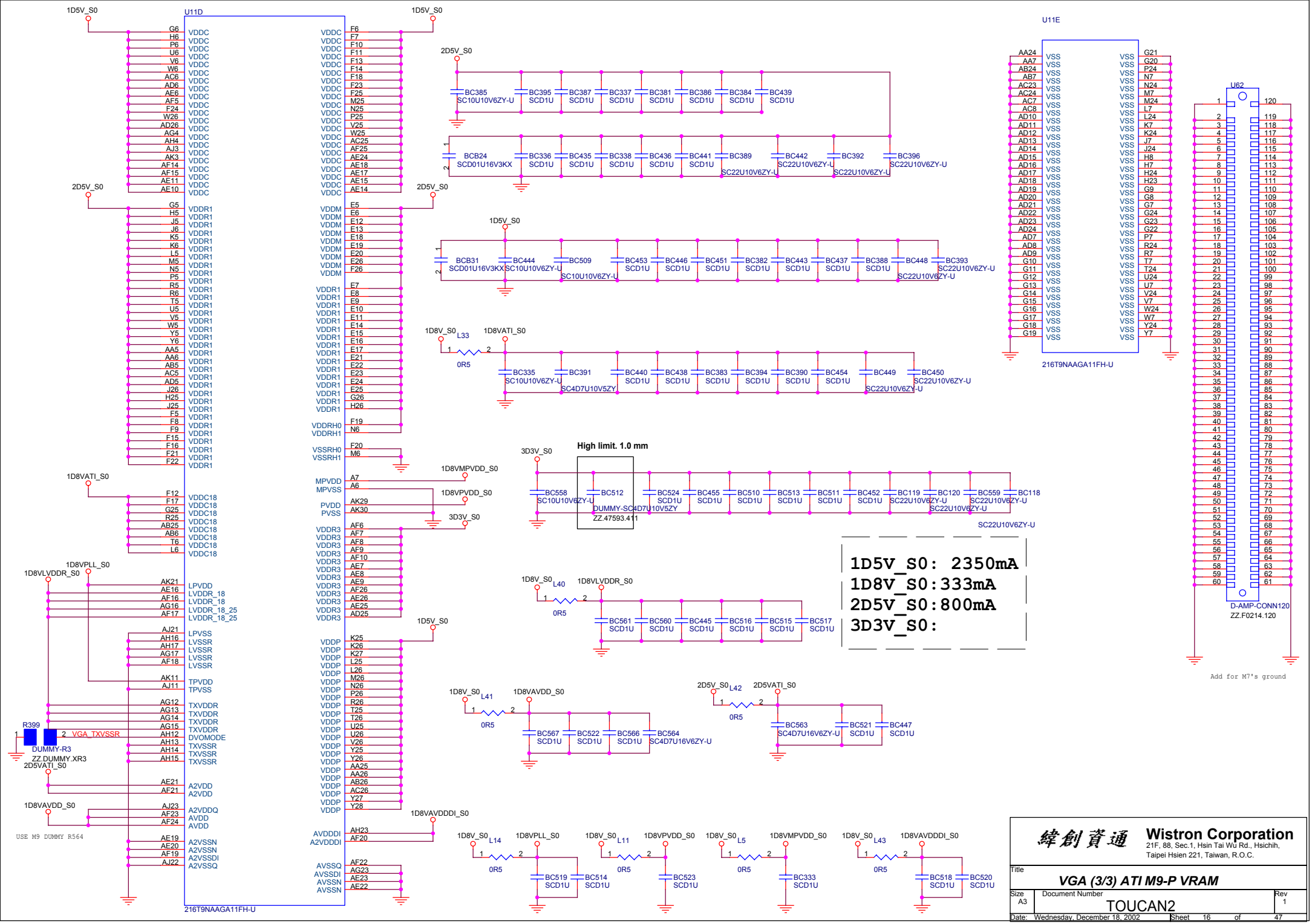
MEMVMODE[1:0]	MEMORY IO VOLTAGE
0 1 (Now Use)	2.5V DDR
1 0	1.8V DDR
1 1	3.3V DDR

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
VGA (2/3) ATI M9-P MEM

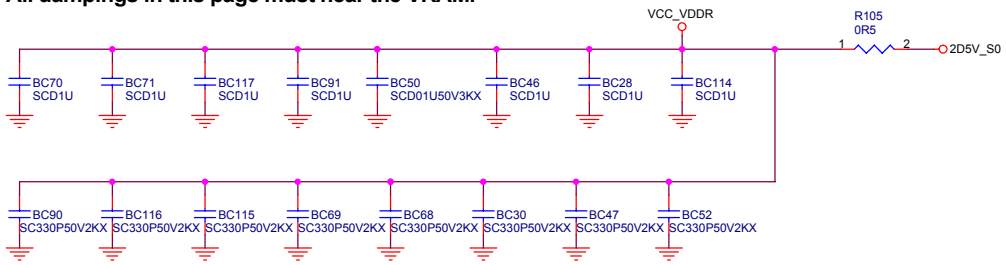
Size	Document Number	Rev
A3	TOUCAN2	1

Date: Wednesday, December 18, 2002 Sheet 15 of 47

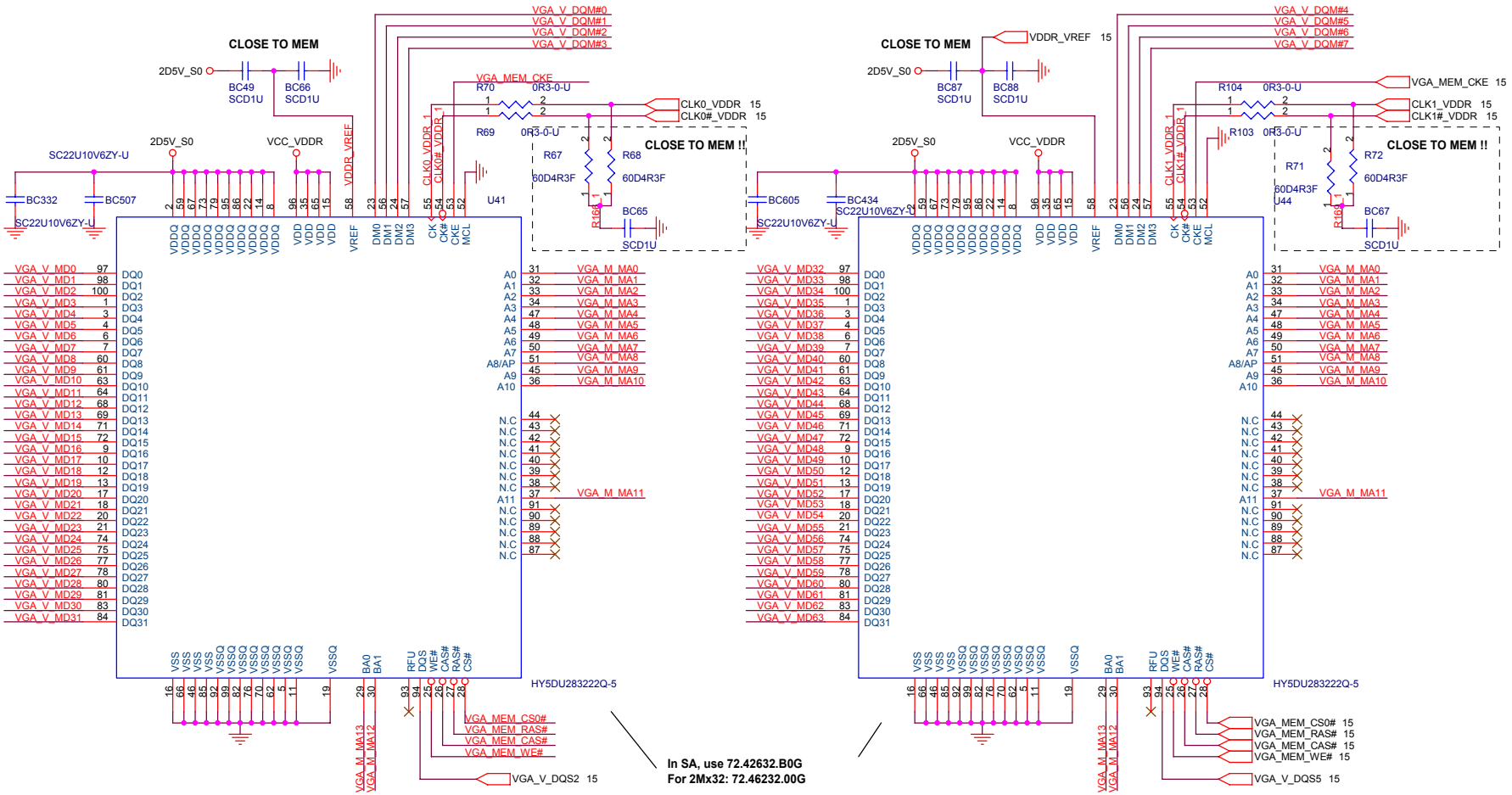


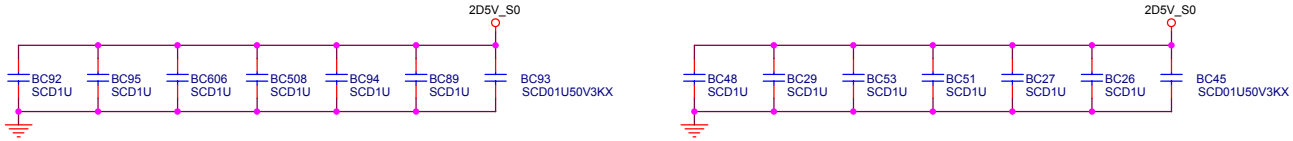
Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	VGA (3/3) ATI M9-P VRAM
Size: A3	Document Number: TOUCAN2
Rev: 1	
Date: Wednesday, December 18, 2002	Sheet 16 of 47

All dampings in this page must near the VRAM.



15 VGA_V_MD[0..63]
15 VGA_M_MA[0..13]
15 VGA_V_DQM#[0..7]





緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **VGA VRAM (DDR)**

Size	Document Number	Rev
A3	TOUCAN2	1

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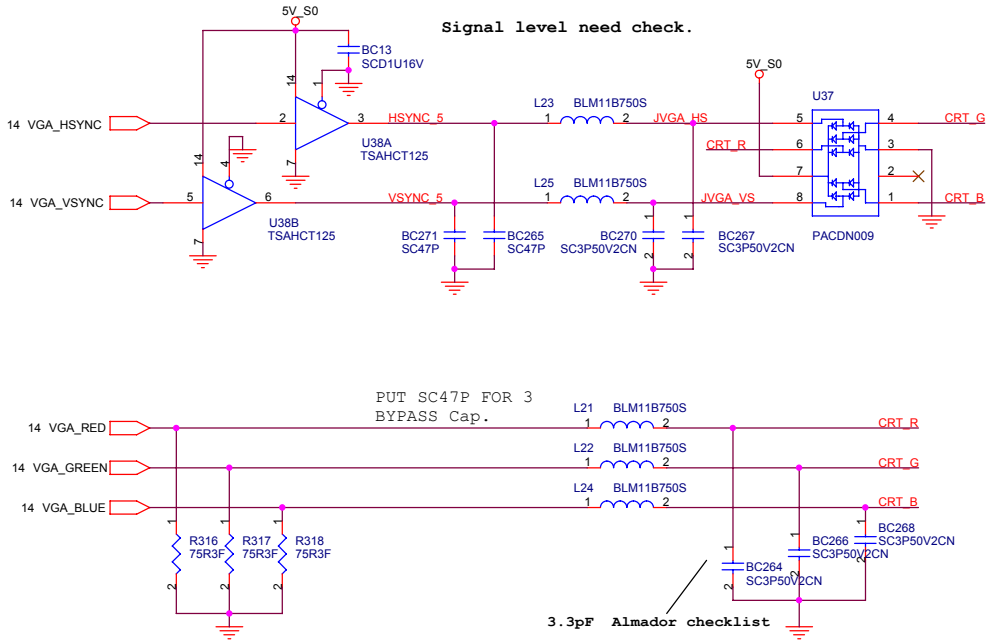
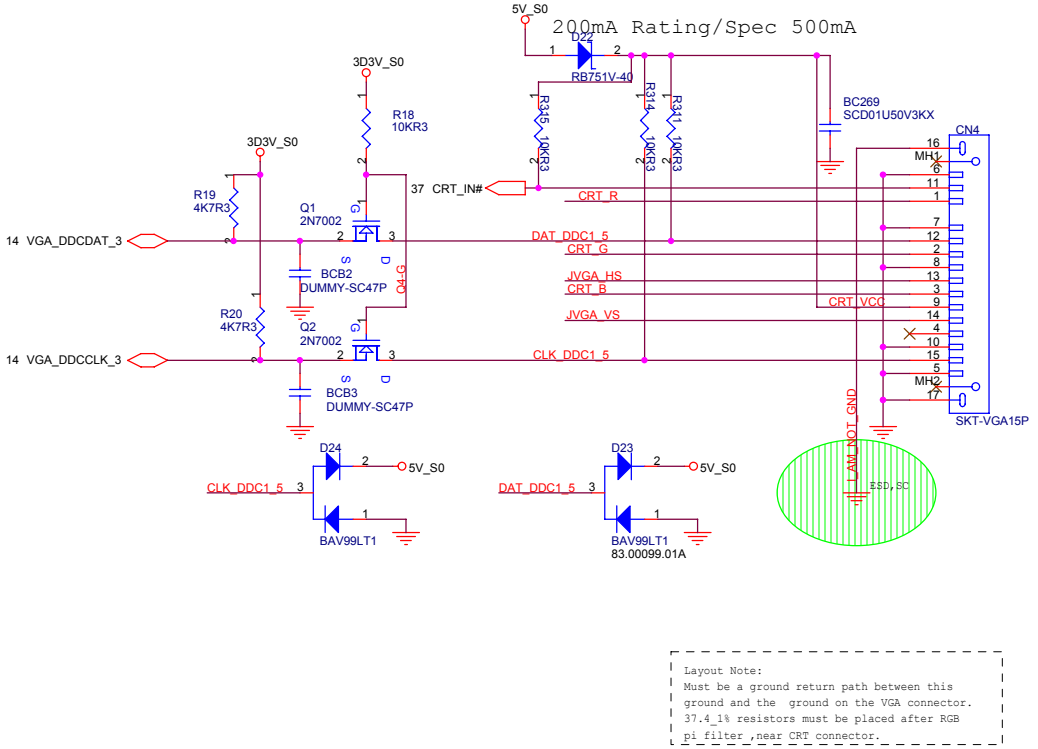
CRT

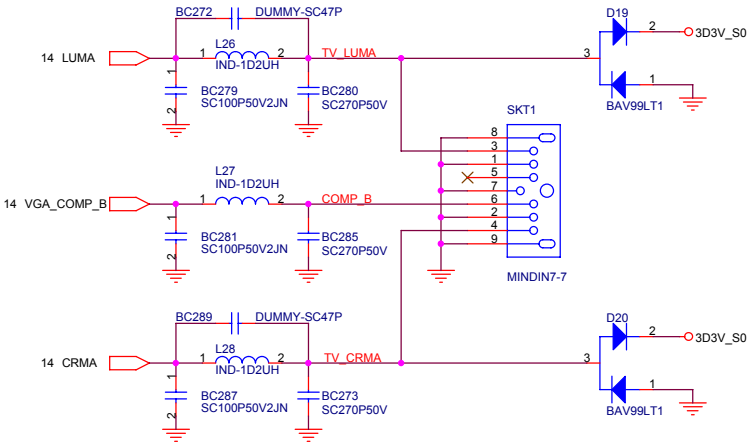


CRT CONN



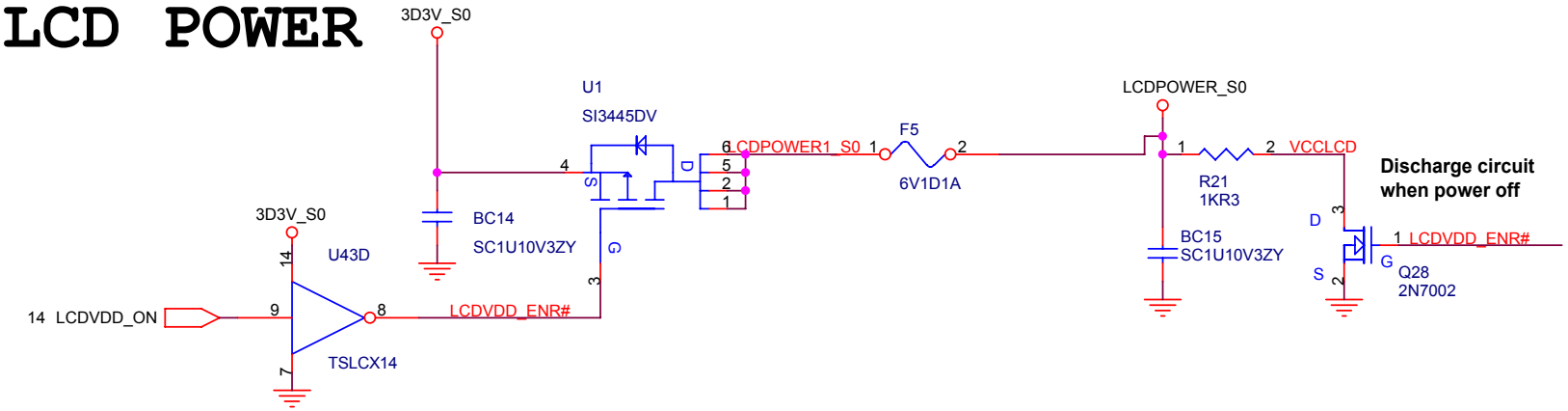
Layout Note:
Must be a ground return path between this ground and the ground on the VGA connector.
37.4_1% resistors must be placed after RGB pi_filter ,near CRT connector.

TV CONN

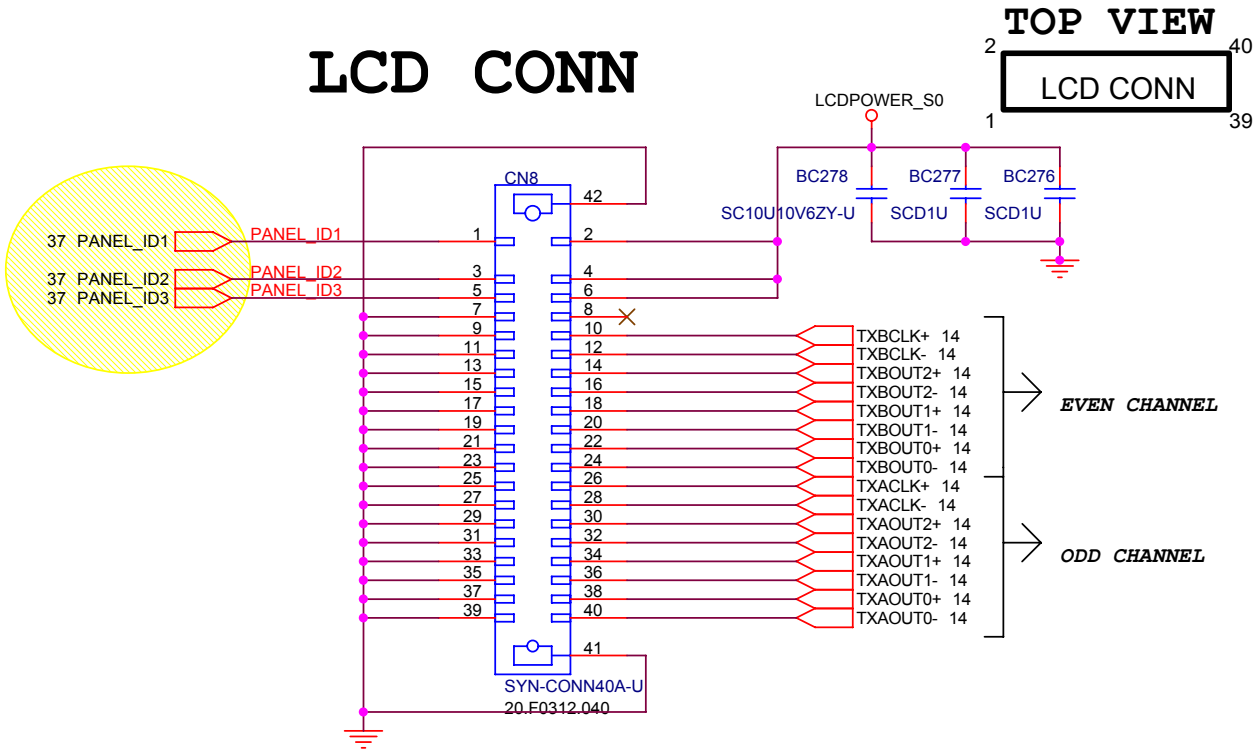


緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CRT / TV***	
Size A3	Document Number TOUCAN2	Rev 1
Date: Wednesday, December 18, 2002	Sheet 18 of 47	

LCD POWER

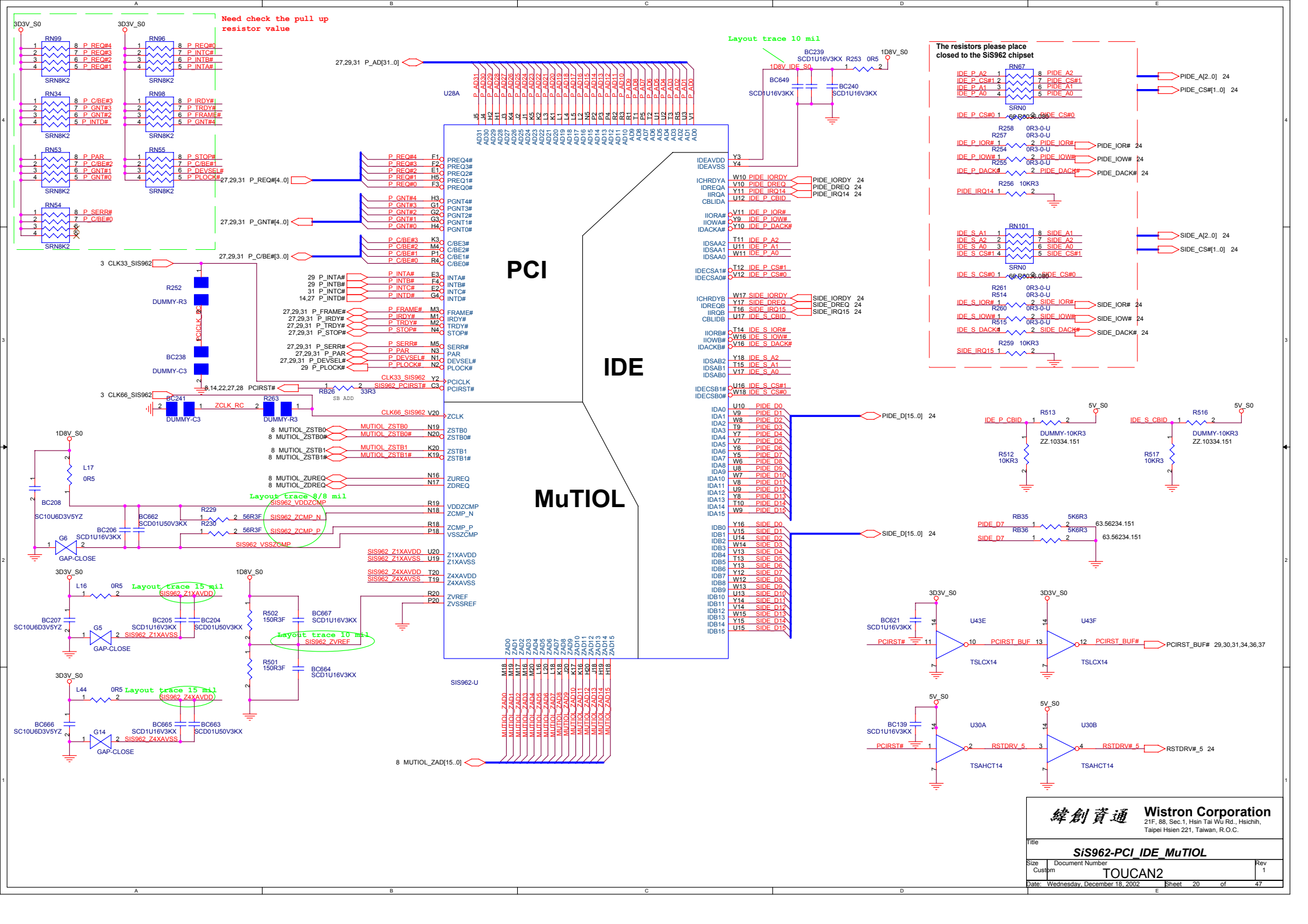


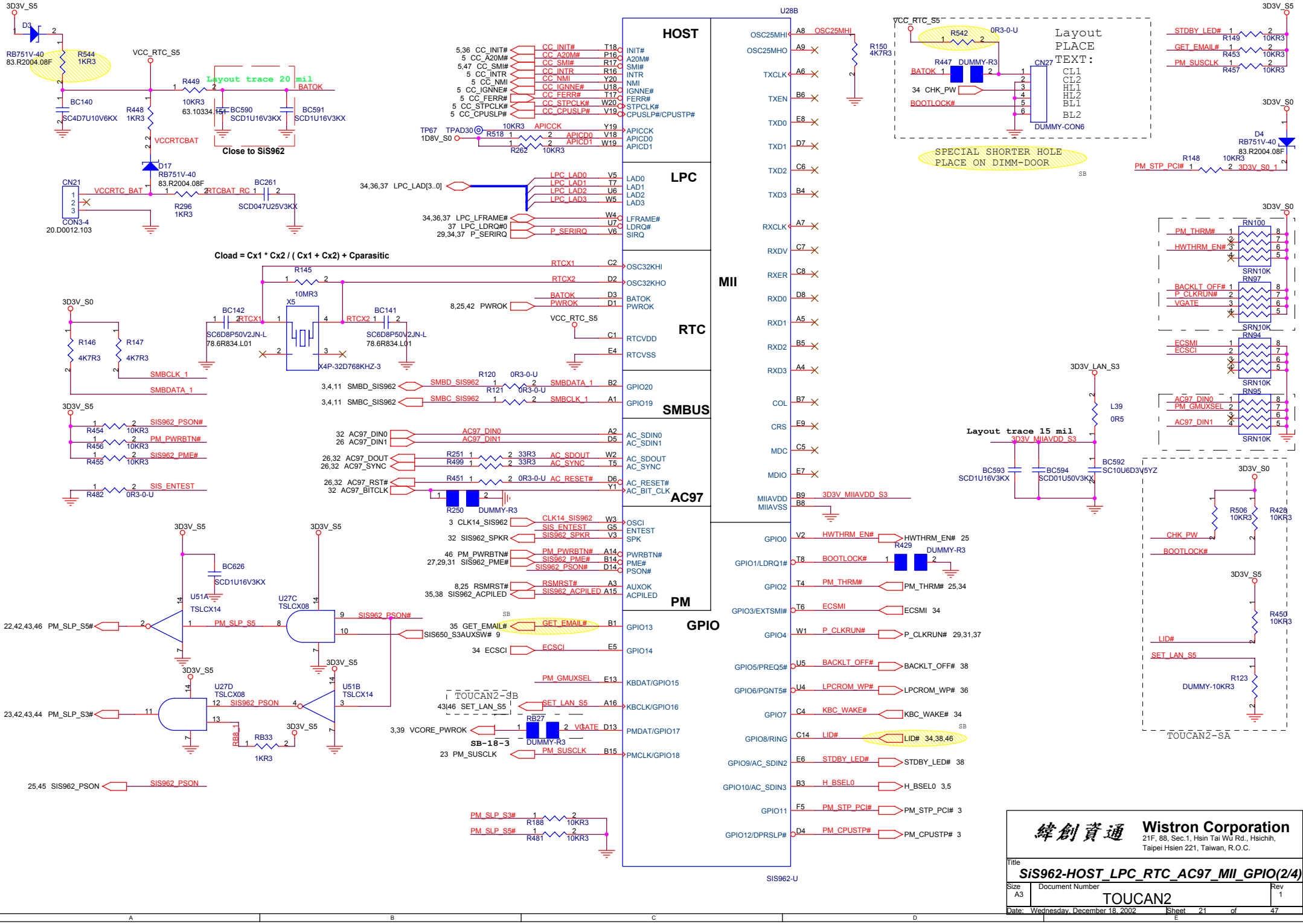
LCD CONN

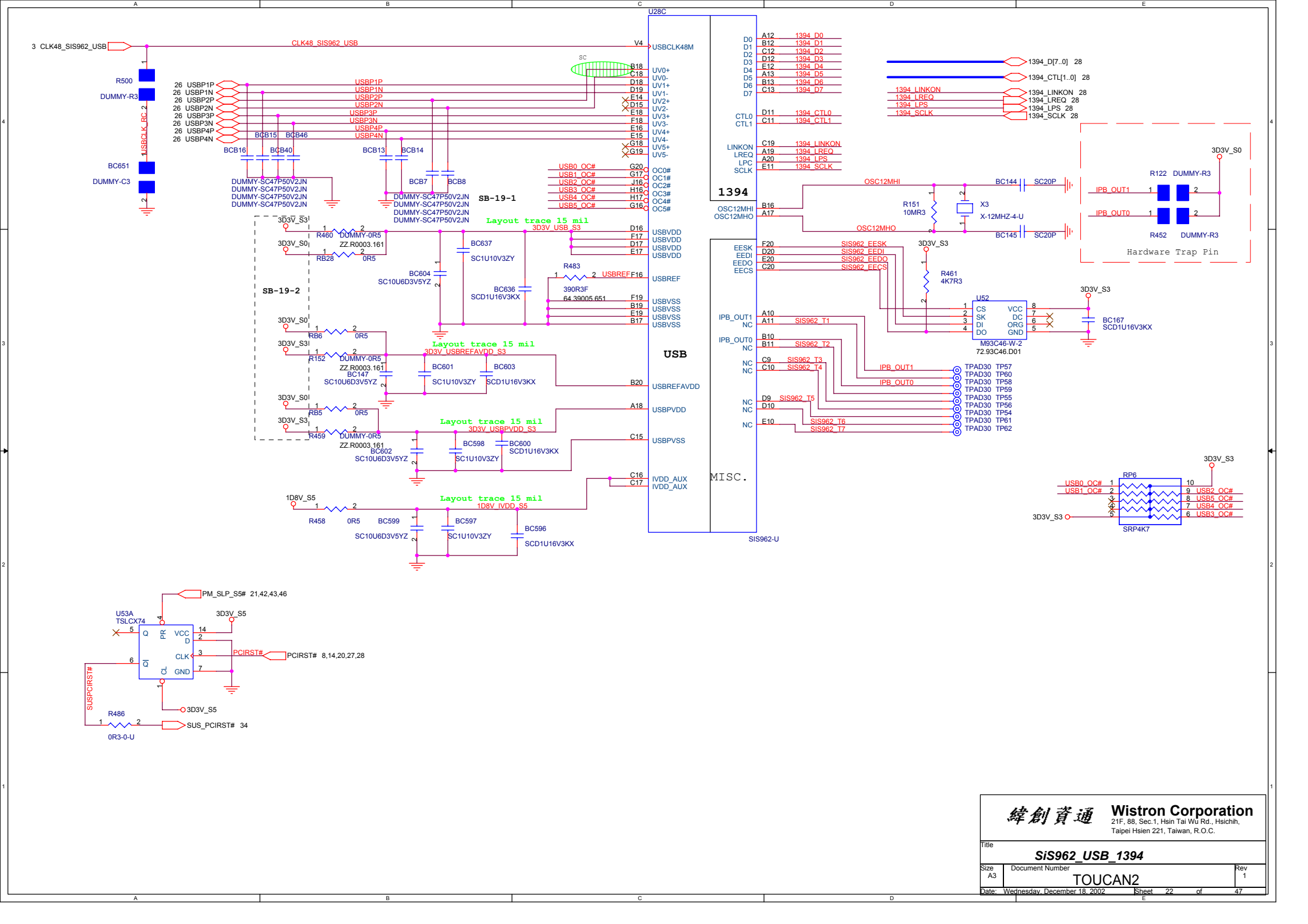


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

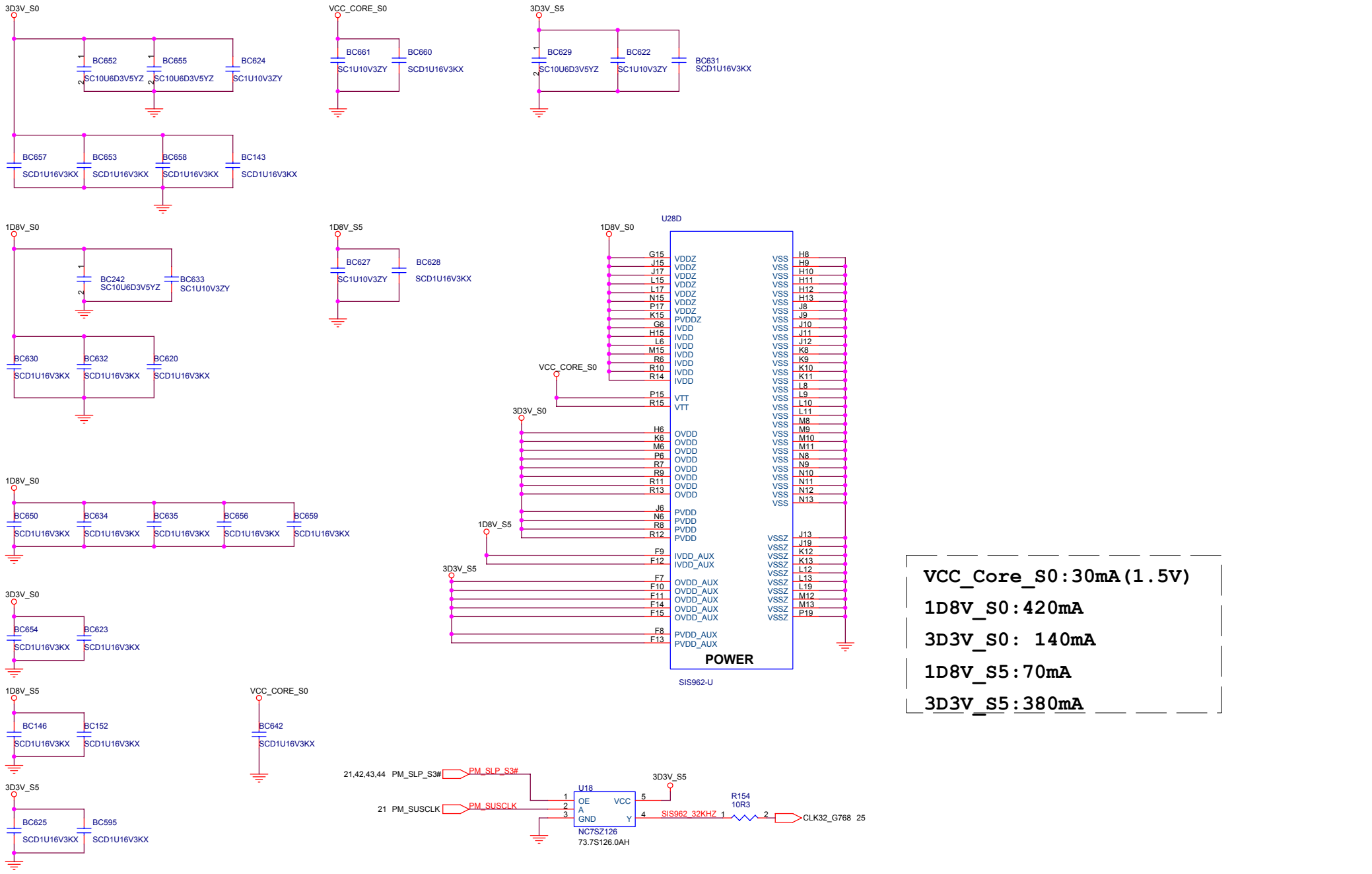
Title: LCD		
Size: A4	Document Number: TOUCAN2	Rev: 1
Date: Wednesday, December 18, 2002	Sheet 19 of 47	


Need check the pull up resistor value
Layout trace 10 mil
The resistors please place closed to the SiS962 chipset
PCI
IDE
MuTIOL
U28A
SIS962-U
Layout trace 8/8 mil
Layout trace 15 mil
Layout trace 10 mil
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
SiS962-PCI_IDE_MuTIOL
TOUCAN2
Date: Wednesday, December 18, 2002
Sheet 20 of 47


HOST
LPC
RTC
SMBUS
AC97
PM
GPIO
MII
SIS962-U
U28B
Cload = Cx1 * Cx2 / (Cx1 + Cx2) + Cparasitic
Layout trace 20 mil
Close to SiS962
Layout trace 15 mil
SPECIAL SHORTER HOLE PLACE ON DIMM-DOOR
Layout PLACE TEXT:
TOUCAN2-SB
TOUCAN2-SA
SB-18-3
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
SiS962-HOST_LPC_RTC_AC97_MII_GPIO(2/4)
TOUCAN2
Wednesday, December 18, 2002
21
47



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***SiS962_USB_1394***	
Size A3	Document Number TOUCAN2	Rev 1
Date: Wednesday, December 18, 2002	Sheet 22 of 47	



VCC_Core_S0:30mA(1.5V)

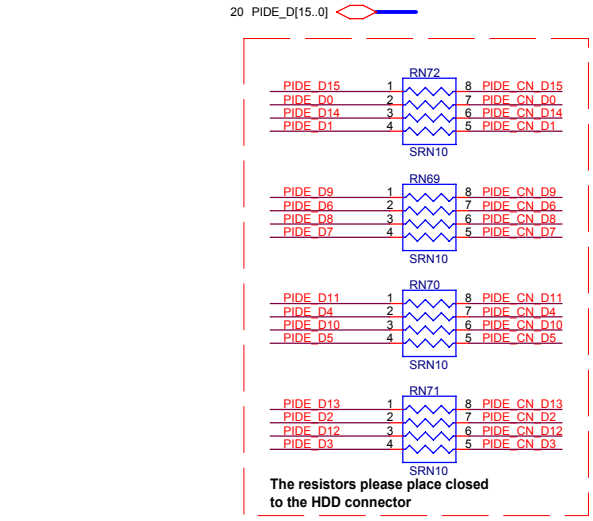
1D8V_S0:420mA

3D3V_S0: 140mA

1D8V_S5:70mA

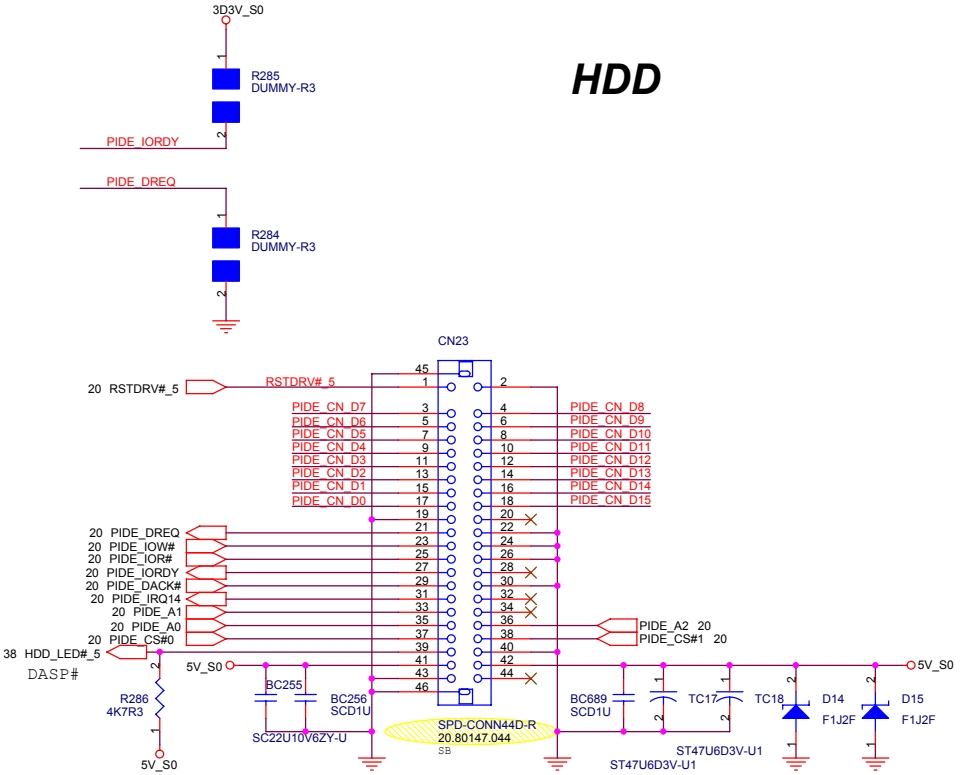
3D3V_S5:380mA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***SiS962_POWER_PLANE(4/4)***	
Size A3	Document Number TOUCAN2	Rev 1
Date: Wednesday, December 18, 2002	Sheet 23 of 47	



TOUCAN2:COULD REMOVE DAMP RESISTER

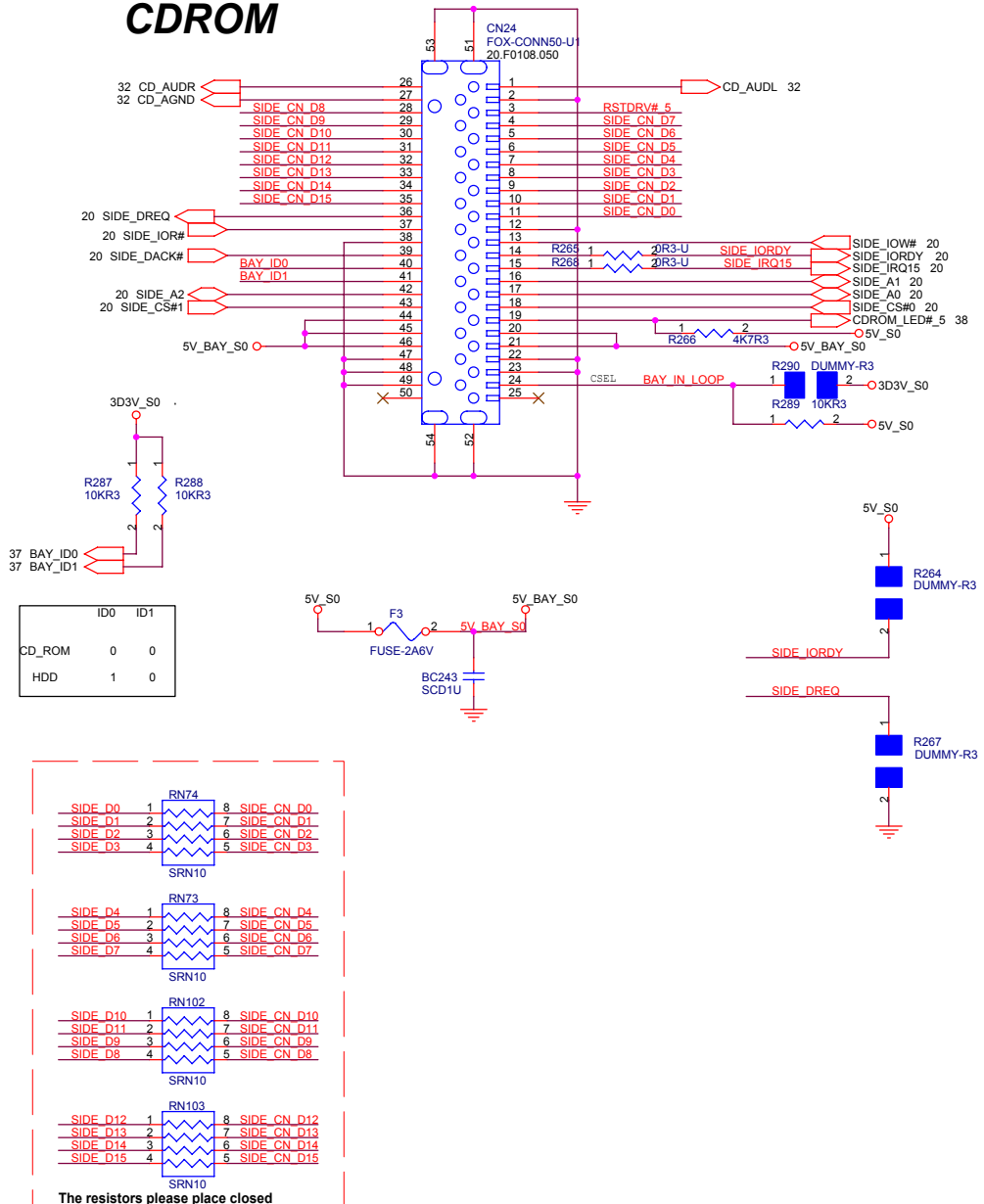
HDD



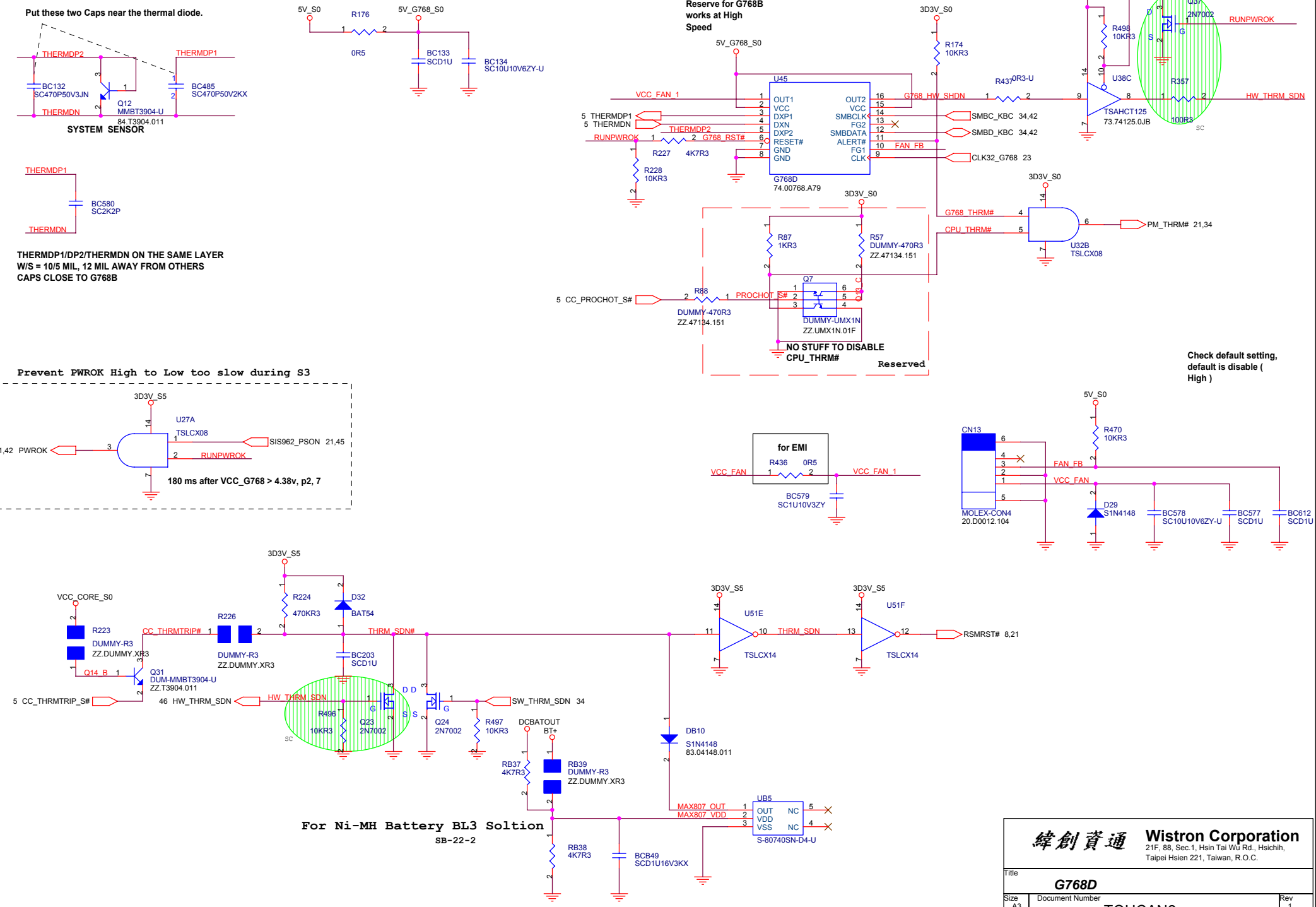
PWR TRACE 100mil

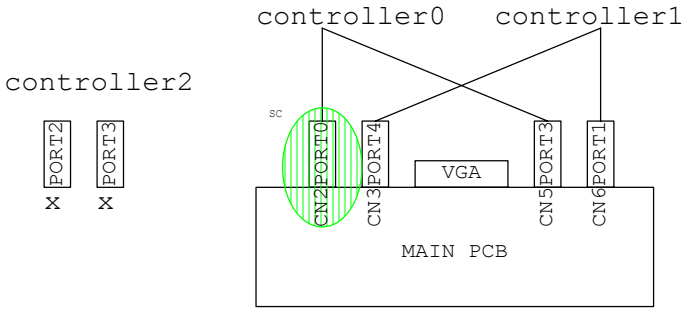
20 SIDE_D[15..0]

CDROM

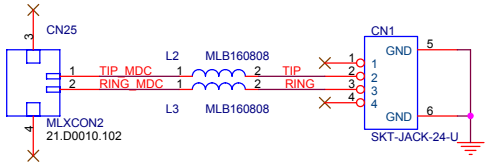


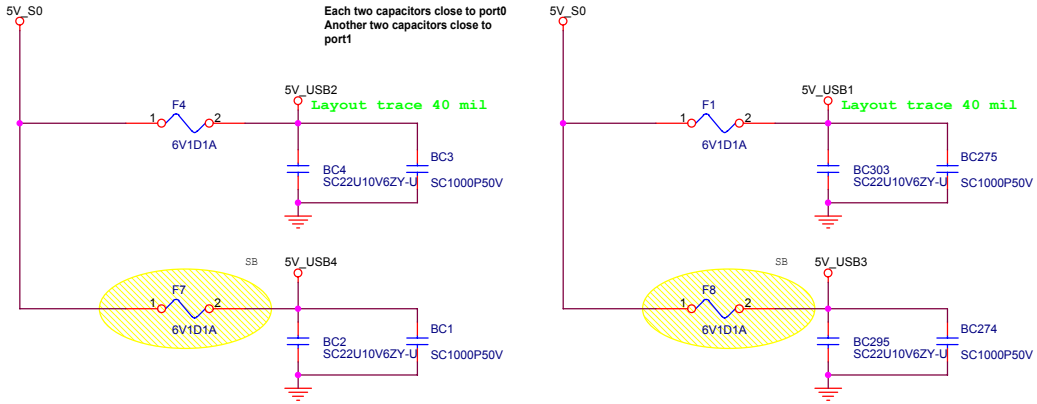
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***HDD / CDROM***
Size: A3	Document Number: TOUCAN2
Rev: 1	
Date: Wednesday, December 18, 2002	Sheet 24 of 47

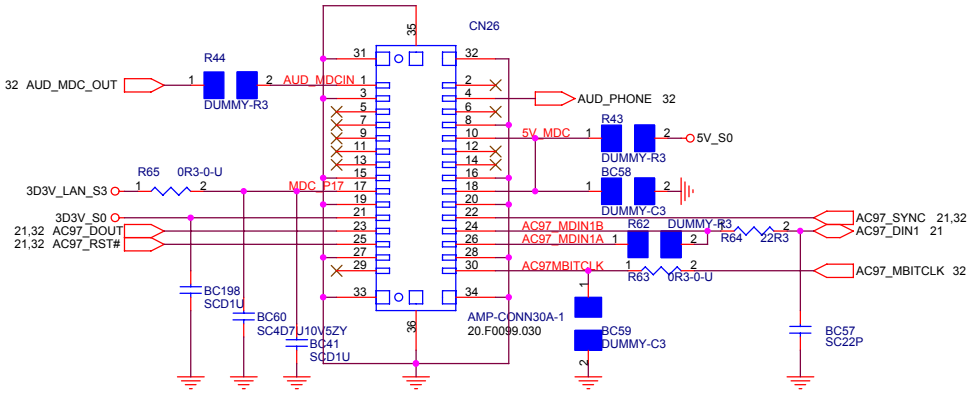

Put these two Caps near the thermal diode.
THERMDP2
THERMDP1
BC132
SC470P50V3JN
BC485
SC470P50V2KX
Q12
MMBT3904-U
84.T3904.011
THERMDN
SYSTEM SENSOR
5V_S0
R176
0R5
5V_G768_S0
BC133
SCD1U
BC134
SC10U10V6ZY-U
THERMDP1
BC580
SC2K2P
THERMDN
THERMDP1/DP2/THERMDN ON THE SAME LAYER
W/S = 10/5 MIL, 12 MIL AWAY FROM OTHERS
CAPS CLOSE TO G768B
Reserve for G768B
works at High
Speed
5V_G768_S0
3D3V_S0
R174
10KR3
U45
VCC_FAN_1
OUT1
VCC
DXP1
DXN
DXP2
RESET#
GND
GND
OUT2
VCC
SMBCLK
FG2
SMBDATA
ALERT#
FG1
CLK
G768_HW_SHDN
R437
0R3-U
SMBC_KBC 34,42
SMBD_KBC 34,42
FAN_FB
CLK32_G768 23
5 THERMDP1
5 THERMDN
THERMDP2
RUNPWROK
G768_RST#
R227
4K7R3
R228
10KR3
G768D
74.00768.A79
5V_S0
HWTHRM_EN# 21
Q37
2N7002
RUNPWROK
R498
10KR3
U38C
R357
HW_THRM_SDN
TSAHCT125
73.74125.0JB
100R3
SC
3D3V_S0
G768_THRM#
CPU_THRM#
U32B
TSLCX08
PM_THRM# 21,34
R87
1KR3
R57
DUMMY-470R3
ZZ.47134.151
Q7
R88
DUMMY-470R3
ZZ.47134.151
5 CC_PROCHOT_S#
PROCHOT_S#
DUMMY-UMX1N
ZZ.UMX1N.01F
NO STUFF TO DISABLE
CPU_THRM#
Reserved
Check default setting,
default is disable (
High)
Prevent PWROK High to Low too slow during S3
3D3V_S5
U27A
TSLCX08
8,21,42 PWROK
SIS962_PSON 21,45
RUNPWROK
180 ms after VCC_G768 > 4.38v, p2, 7
for EMI
R436
0R5
VCC_FAN
VCC_FAN_1
BC579
SC1U10V3ZY
CN13
MOLEX-CON4
20.D0012.104
5V_S0
R470
10KR3
FAN_FB
VCC_FAN
D29
S1N4148
BC578
SC10U10V6ZY-U
BC577
SCD1U
BC612
SCD1U
3D3V_S5
VCC_CORE_S0
R223
DUMMY-R3
ZZ.DUMMY.XR3
CC_THRMTRIP#
R226
DUMMY-R3
ZZ.DUMMY.XR3
R224
470KR3
D32
BAT54
THRM_SDN#
BC203
SCD1U
Q14_B
Q31
DUM-MMBT3904-U
ZZ.T3904.011
5 CC_THRMTRIP_S#
46 HW_THRM_SDN
HW_THRM_SDN
R496
10KR3
Q23
2N7002
Q24
2N7002
R497
10KR3
SW_THRM_SDN 34
U51E
TSLCX14
THRM_SDN
U51F
TSLCX14
RSMRST# 8,21
DB10
S1N4148
83.04148.011
DCBATOUT
BT+
RB37
4K7R3
RB39
DUMMY-R3
ZZ.DUMMY.XR3
RB38
4K7R3
BCB49
SCD1U16V3KX
UB5
MAX807_OUT
MAX807_VDD
OUT
VDD
VSS
NC
NC
S-80740SN-D4-U
For Ni-MH Battery BL3 Soltion
SB-22-2
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
G768D
Size
A3
Document Number
TOUCAN2
Rev
1
Date: Wednesday, December 18, 2002
Sheet 25 of 47

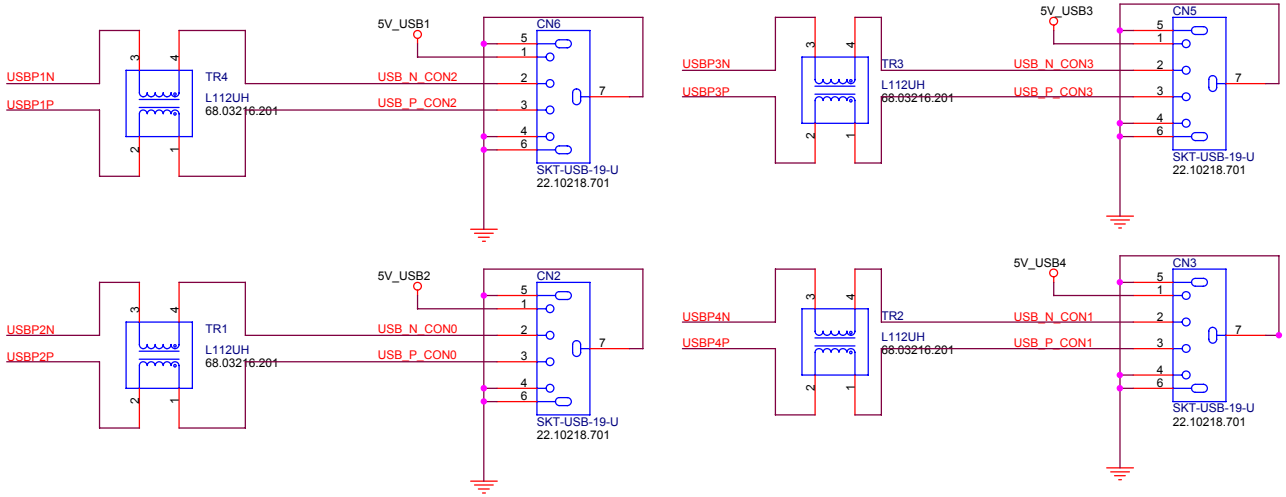


MDC









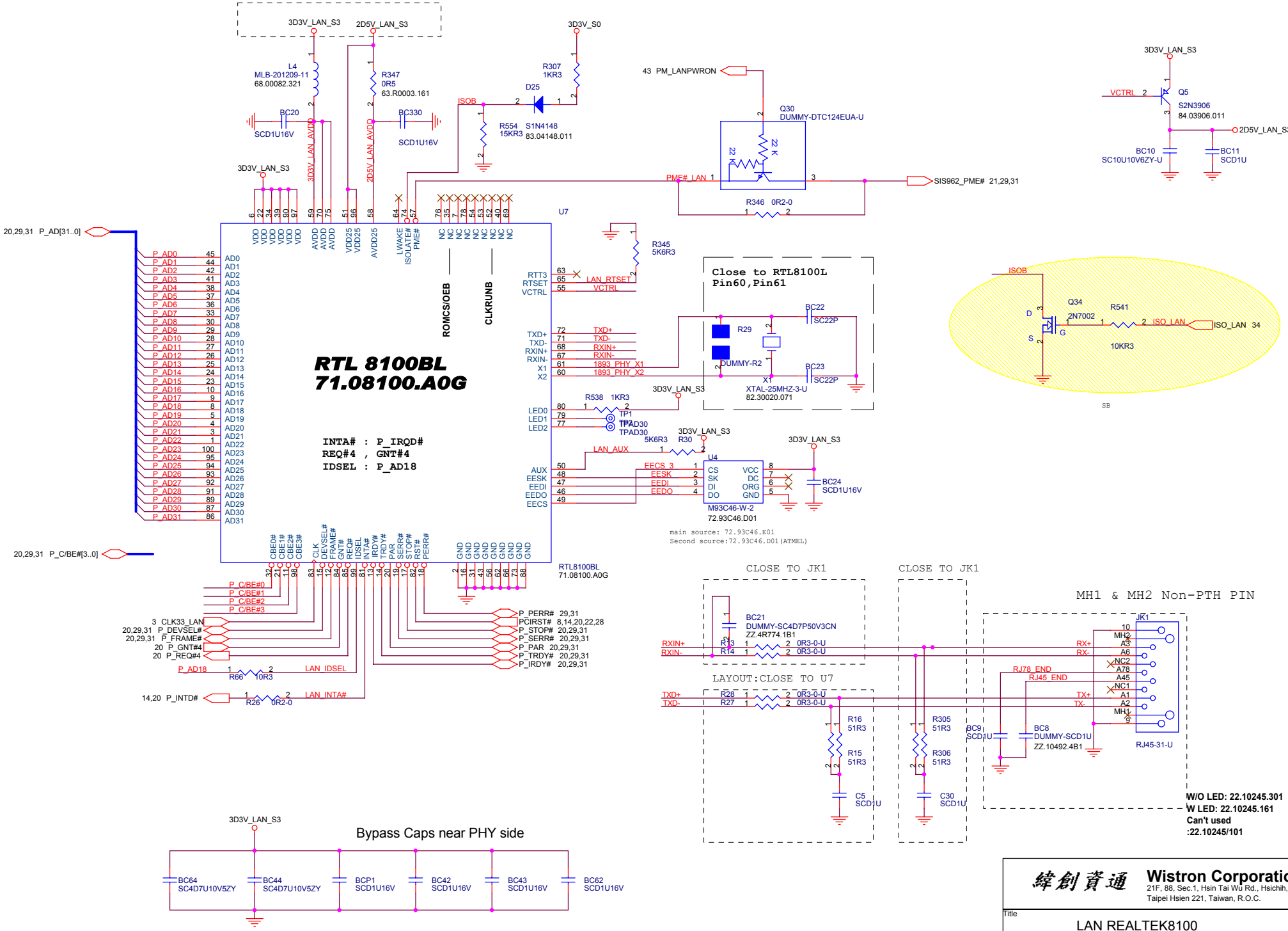
22 USBP1P
22 USBP1N
22 USBP2P
22 USBP2N
22 USBP3P
22 USBP3N
22 USBP4P
22 USBP4N

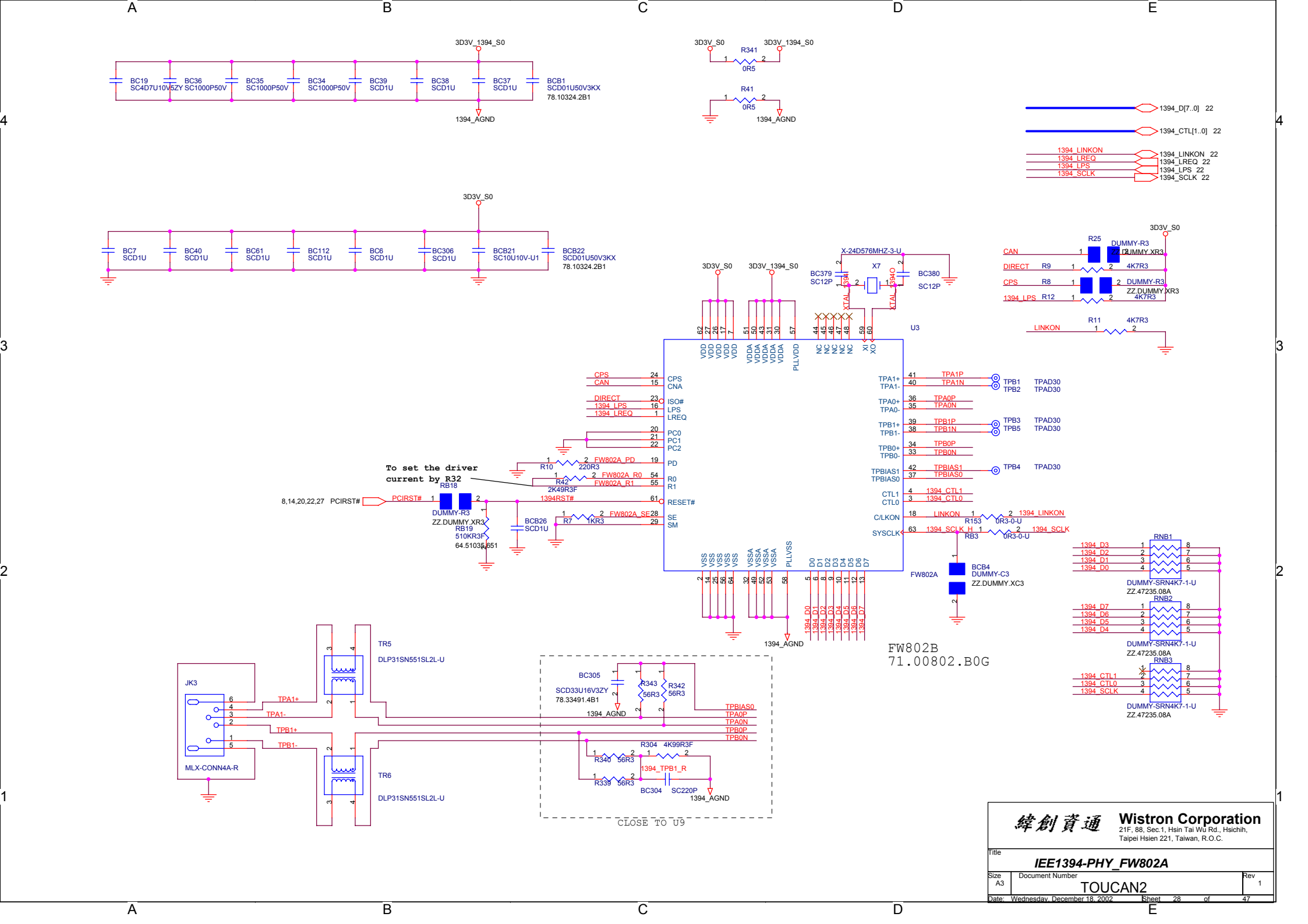
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

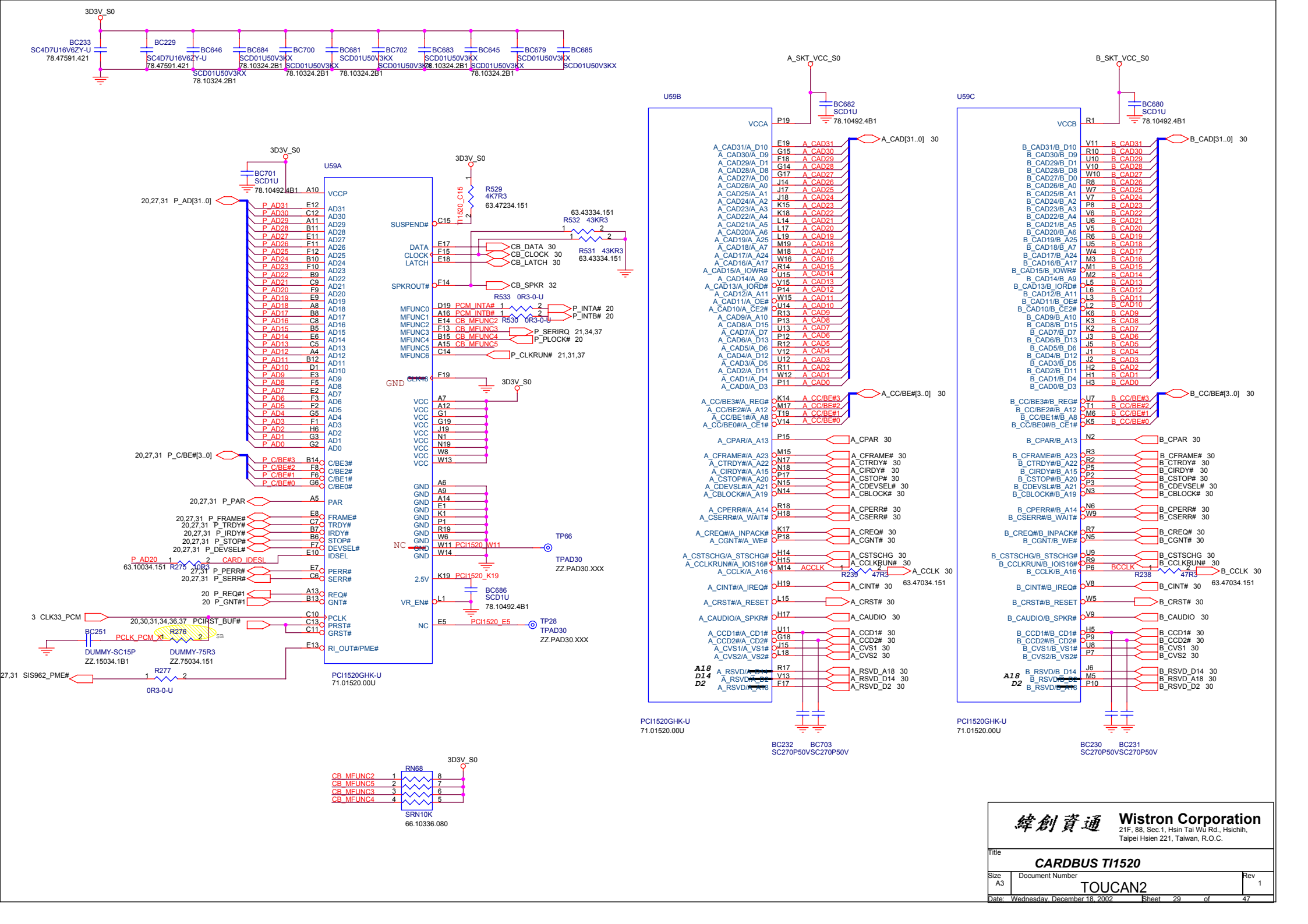
Title: **MDC / USB**

Size	Document Number	Rev
A3	TOUCAN2	1

Date: Wednesday, December 18, 2002 Sheet 26 of 47


RTL 8100BL
71.08100.A0G
INTA# : P_IRQD#
REQ#4 , GNT#4
IDSEL : P_AD18
Close to RTL8100L
Pin60,Pin61
Bypass Caps near PHY side
CLOSE TO JK1
CLOSE TO JK1
LAYOUT:CLOSE TO U7
MH1 & MH2 Non-PTH PIN
W/O LED: 22.10245.301
W LED: 22.10245.161
Can't used
:22.10245/101
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
LAN REALTEK8100
TOUCAN2
Wednesday, December 18, 2002


3D3V_1394_S0
BC19 SC4D7U10V5ZY
BC36 SC1000P50V
BC35 SC1000P50V
BC34 SC1000P50V
BC39 SCD1U
BC38 SCD1U
BC37 SCD1U
BCB1 SCD01U50V3KX 78.10324.2B1
1394_AGND
3D3V_S0
3D3V_1394_S0
R341 0R5
R41 0R5
1394_AGND
1394_D[7..0] 22
1394_CTL[1..0] 22
1394_LINKON
1394_LREQ
1394_LPS
1394_SCLK
1394_LINKON 22
1394_LREQ 22
1394_LPS 22
1394_SCLK 22
3D3V_S0
BC7 SCD1U
BC40 SCD1U
BC61 SCD1U
BC112 SCD1U
BC6 SCD1U
BC306 SCD1U
BCB21 SC10U10V-U1
BCB22 SCD01U50V3KX 78.10324.2B1
X-24D576MHZ-3-U
X7
BC379 SC12P
BC380 SC12P
XTAL_1394I
XTAL_1394O
U3
VDD VDD VDD VDD VDD
VDDA VDDA VDDA VDDA VDDA
PLLVDD
NC NC NC NC NC
XI XO
CPS CAN DIRECT 1394_LPS 1394_LREQ
CPS CNA ISO# LPS LREQ
PC0 PC1 PC2
PD
R0 R1
RESET#
SE SM
To set the driver current by R32
RB18
PCIRST# 8,14,20,22,27
DUMMY-R3 ZZ.DUMMY.XR3
RB19 510KR3F 64.51035.651
BCB26 SCD1U
R10 220R3
R42 2K49R3F
R7 1KR3
FW802A_PD
FW802A_R0
FW802A_R1
FW802A_SE
1394RST#
TPA1+ TPA1- TPA0+ TPA0- TPB1+ TPB1- TPB0+ TPB0-
TPBIAS1 TPBIAS0
CTL1 CTL0
C/LKON
SYSCLK
TPA1P TPA1N TPA0P TPA0N TPB1P TPB1N TPB0P TPB0N TPBIAS1 TPBIAS0
1394_CTL1 1394_CTL0
LINKON R153 0R3-0-U 1394_LINKON
1394_SCLK_H RB3 0R3-0-U 1394_SCLK
TPB1 TPB2 TPAD30
TPB3 TPB5 TPAD30
TPB4 TPAD30
FW802A
BCB4 DUMMY-C3 ZZ.DUMMY.XC3
VSS VSSA PLLVSS
D0 D1 D2 D3 D4 D5 D6 D7
1394_AGND
FW802B
71.00802.B0G
3D3V_S0
R25 DUMMY-R3 ZZ.DUMMY.XR3
CAN R9 4K7R3
DIRECT R8 DUMMY-R3 ZZ.DUMMY.XR3 4K7R3
1394_LPS R12 4K7R3
LINKON R11 4K7R3
RNB1 1394_D3 1394_D2 1394_D1 1394_D0 DUMMY-SRN4K7-1-U ZZ.47235.08A
RNB2 1394_D7 1394_D6 1394_D5 1394_D4 DUMMY-SRN4K7-1-U ZZ.47235.08A
RNB3 1394_CTL1 1394_CTL0 1394_SCLK DUMMY-SRN4K7-1-U ZZ.47235.08A
JK3
MLX-CONN4A-R
TPA1+ TPA1- TPB1+ TPB1-
TR5 DLP31SN551SL2L-U
TR6 DLP31SN551SL2L-U
BC305 SCD33U16V3ZY 78.33491.4B1
R343 56R3
R342 56R3
R304 4K99R3F
R340 56R3
R339 56R3
1394_TPB1_R
BC304 SC220P
TPBIAS0 TPA0P TPA0N TPB0P TPB0N
CLOSE TO U9
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
IEE1394-PHY_FW802A
Size A3
Document Number
TOUCAN2
Rev 1
Date: Wednesday, December 18, 2002
Sheet 28 of 47



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***CARDBUS TI1520***
Size A3	Document Number TOUCAN2 Rev 1
Date: Wednesday, December 18, 2002	Sheet 29 of 47

A_CC/BE#[3..0] 29

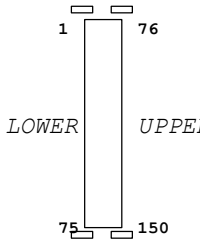
B_CC/BE#[3..0] 29

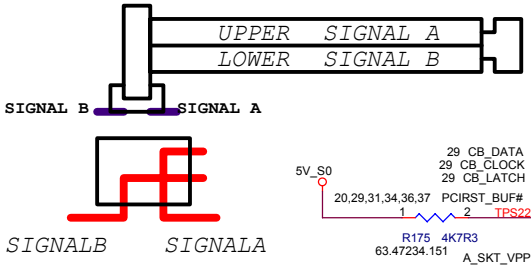
A_CAD[31..0] 29

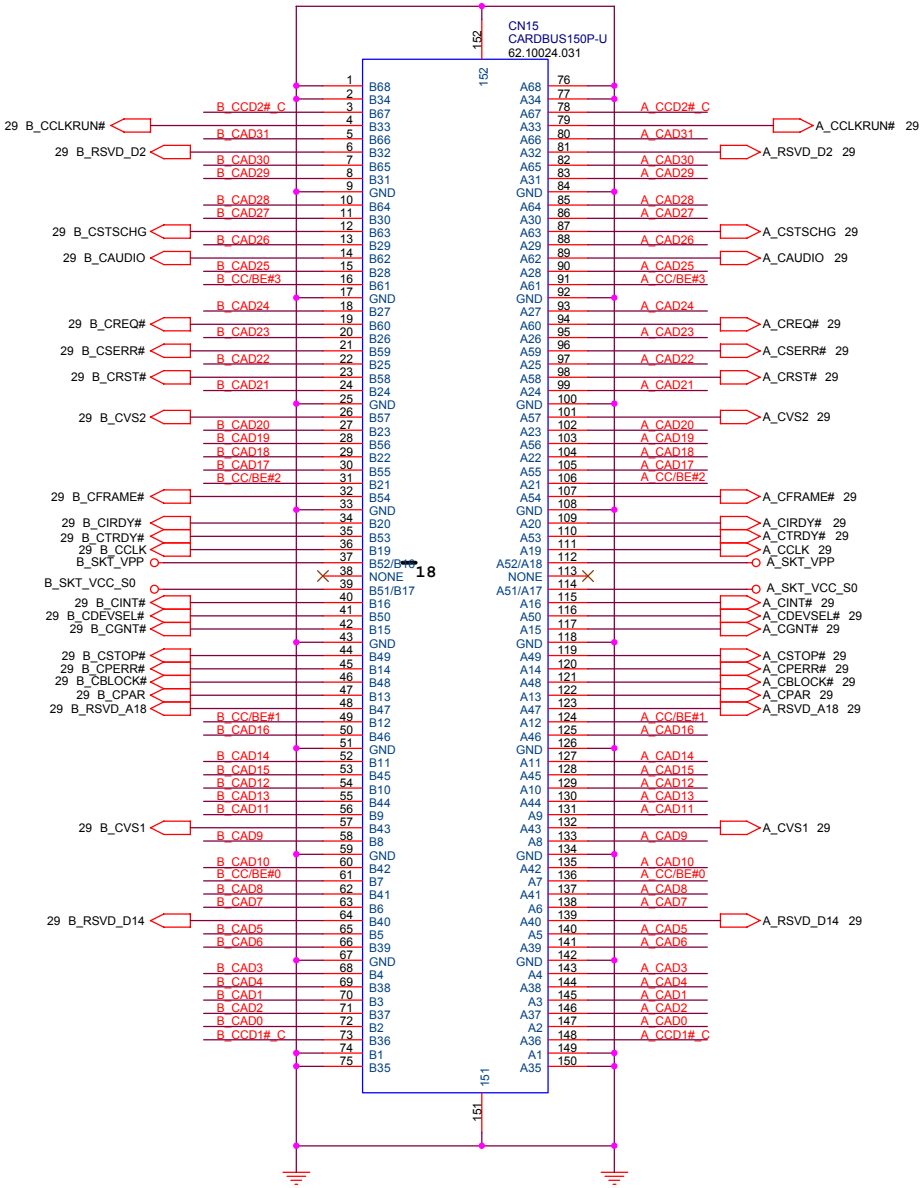
B_CAD[31..0] 29

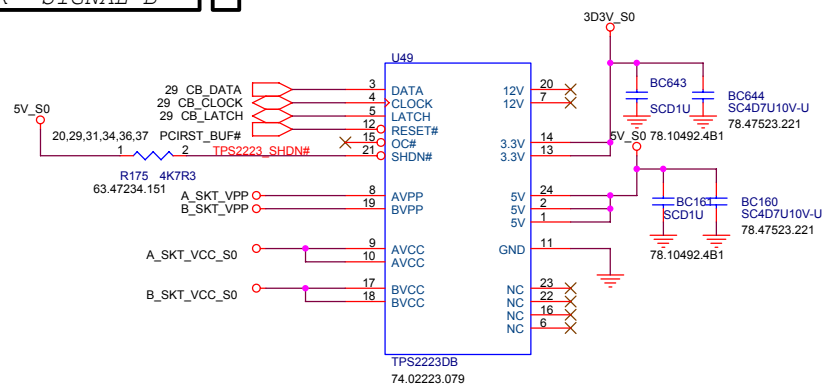
UPPER = SLOT 0 / SIGNAL A

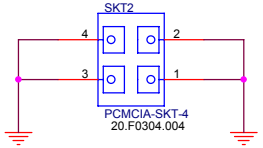
LOWER=SLOT 1/ SIGNAL B

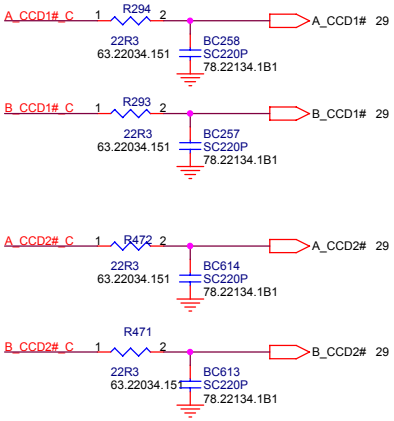


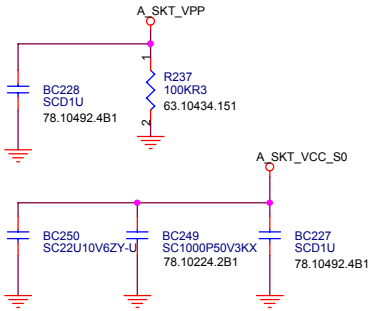


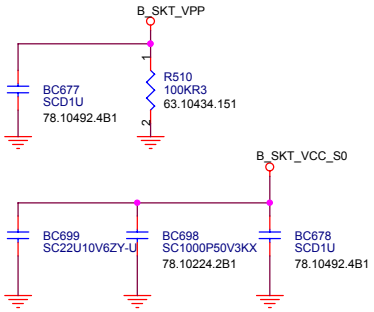






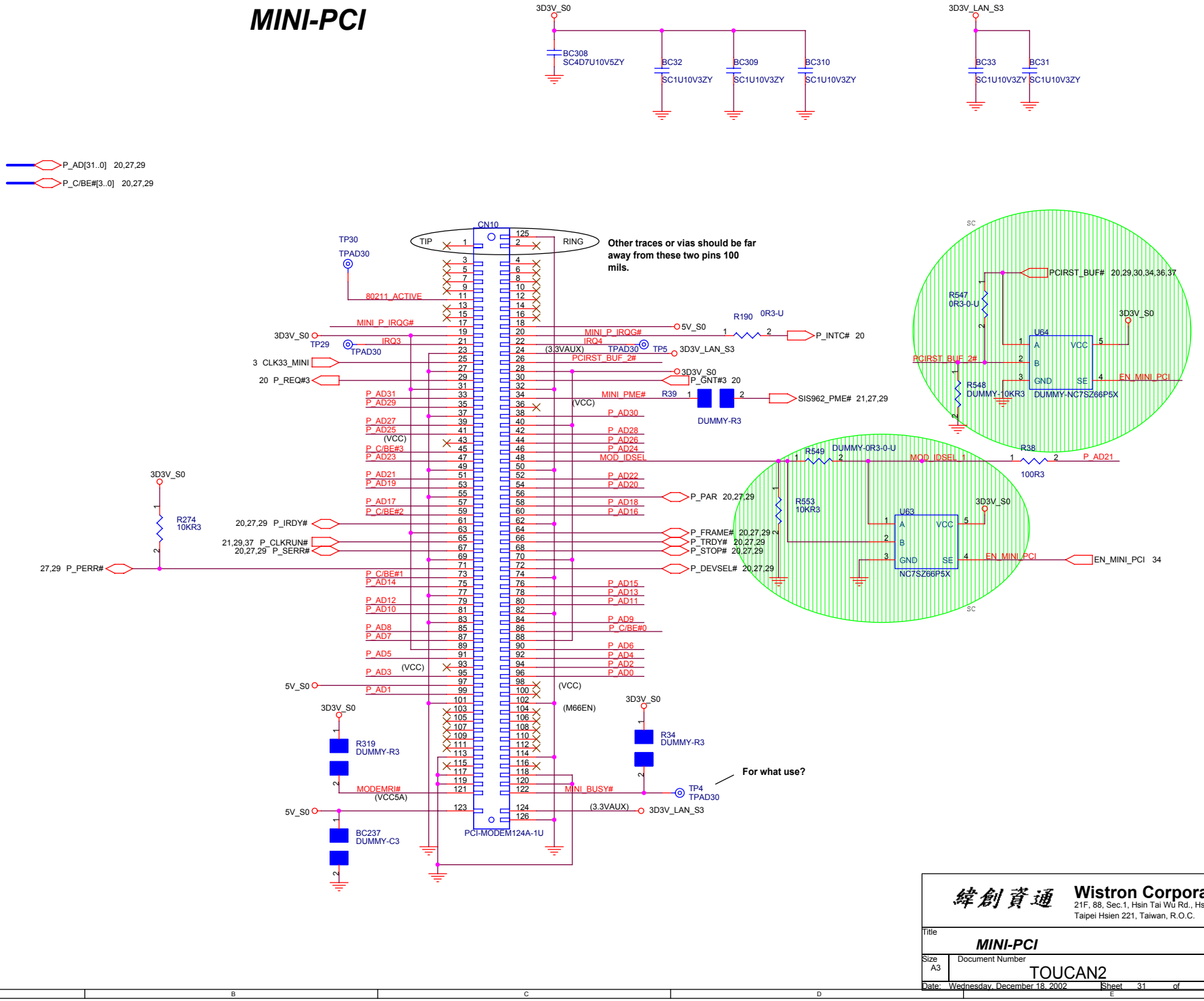




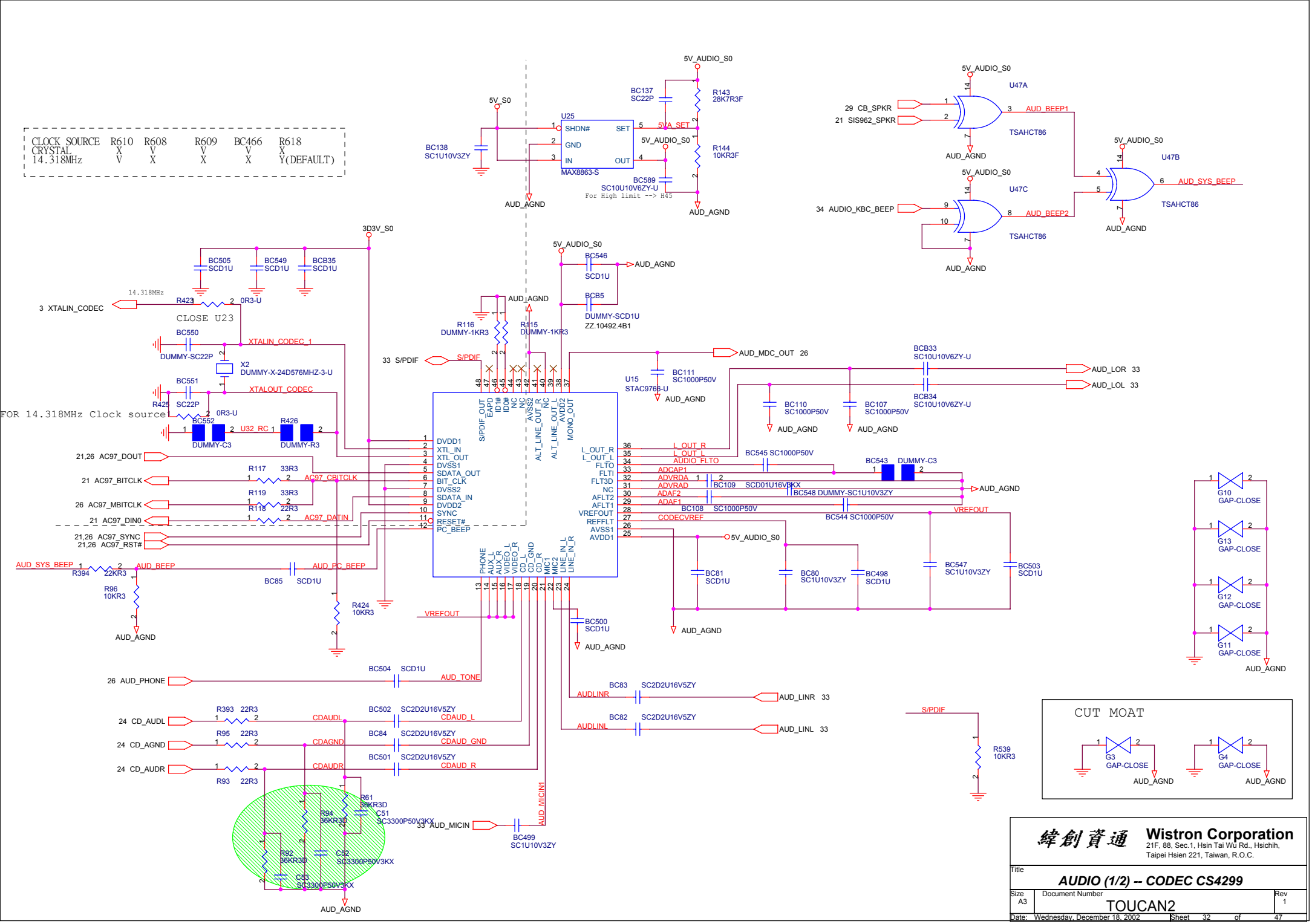


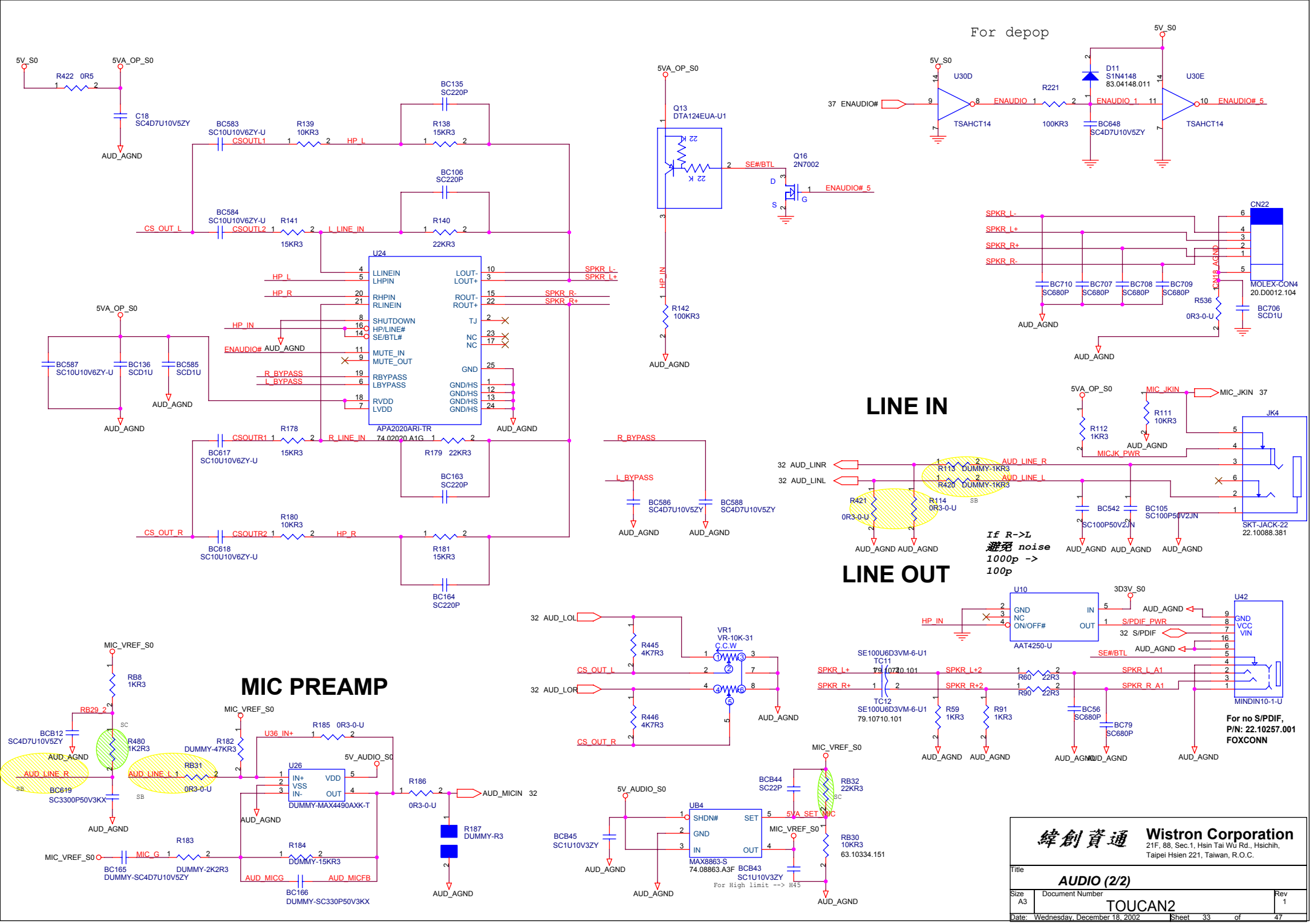
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CARDBUS CONN / PWR SW***	
Size A3	Document Number TOUCAN2	Rev 1
Date: Wednesday, December 18, 2002	Sheet 30 of 47	

MINI-PCI



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***MINI-PCI***	
Size A3	Document Number TOUCAN2	Rev 1
Date: Wednesday, December 18, 2002	Sheet 31 of 47	


CLOCK SOURCE R610 R608 R609 BC466 R618
CRYSTAL X V V V X
14.318MHz V X X X Y(DEFAULT)
FOR 14.318MHz Clock source
CLOSE U23
U25
MAX8863-S
U15
STAC9766-U
U47A
U47B
U47C
TSAHCT86
CUT MOAT
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
AUDIO (1/2) -- CODEC CS4299
TOUCAN2
Date: Wednesday, December 18, 2002
Sheet 32 of 47


For depop
LINE IN
LINE OUT
MIC PREAMP
U24
APA2020ARI-TR
74.02020.A1G
U30D
U30E
TSAHT14
D11
S1N4148
83.04148.011
Q13
DTA124EUA-U1
Q16
2N7002
CN22
MOLEX-CON4
20.D0012.104
JK4
SKT-JACK-22
22.10088.381
If R->L
避免 noise
1000p ->
100p
U10
AAT4250-U
U42
MINDIN10-1-U
SE100U6D3VM-6-U1
U26
DUMMY-MAX4490AXK-T
UB4
MAX8863-S
74.08863.A3F
VR1
VR-10K-31
For no S/PDIF,
P/N: 22.10257.001
FOXCONN
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
AUDIO (2/2)
TOUCAN2
Wednesday, December 18, 2002
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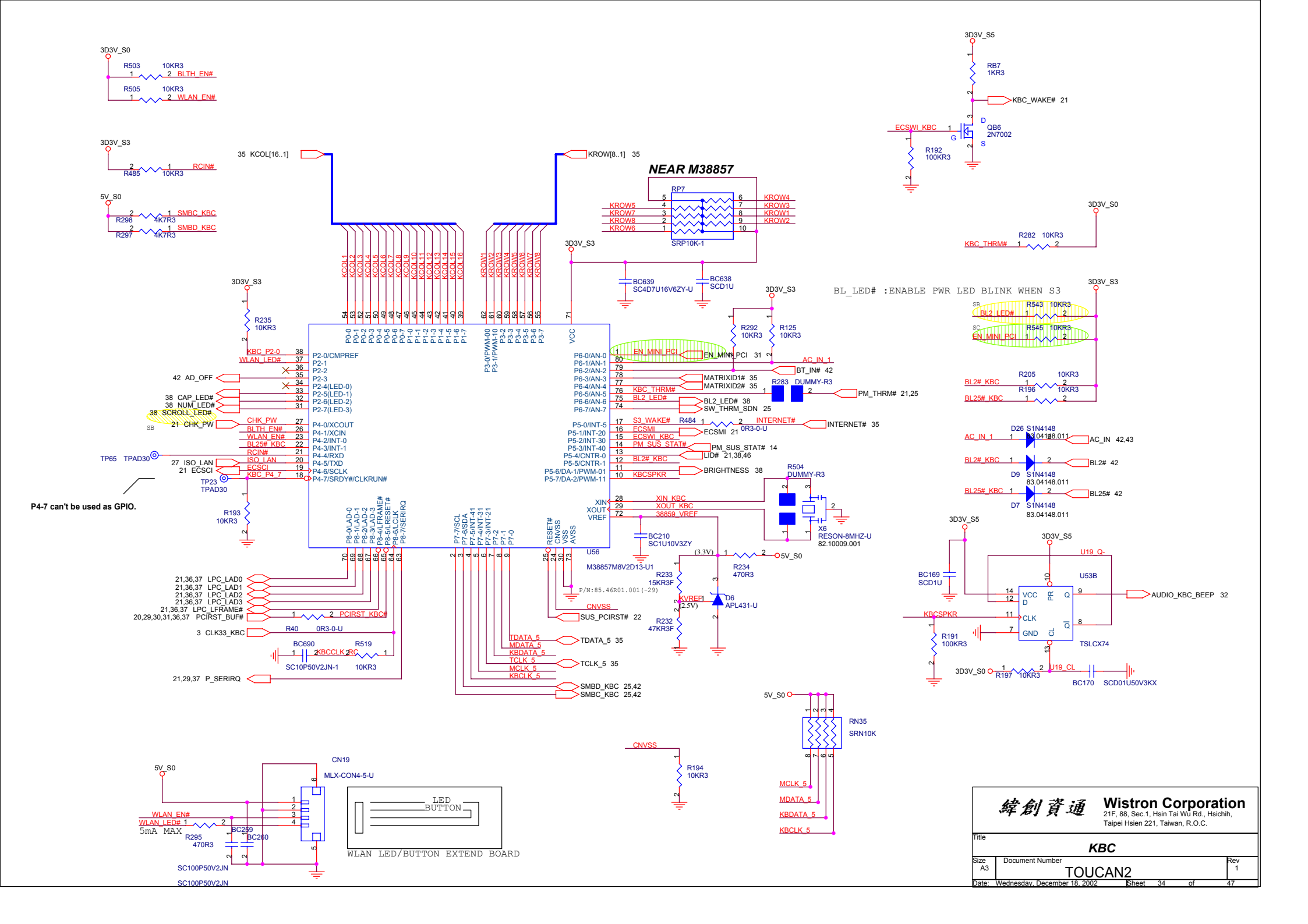
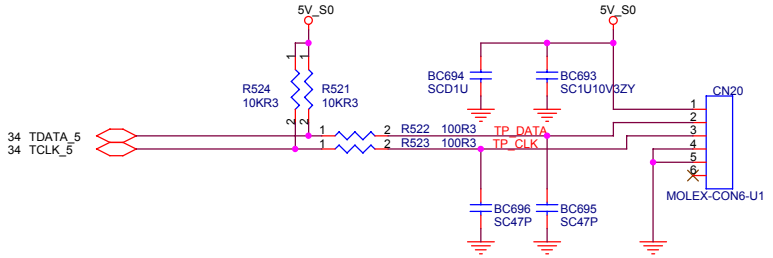

NEAR M38857
U56
M38857M8V2D13-U1
P4-7 can't be used as GPIO.
BL_LED# :ENABLE PWR LED BLINK WHEN S3
LED BUTTON
WLAN LED/BUTTON EXTEND BOARD
5mA MAX
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
KBC
Size A3
Document Number
TOUCAN2
Rev 1
Date: Wednesday, December 18, 2002
Sheet 34 of 47

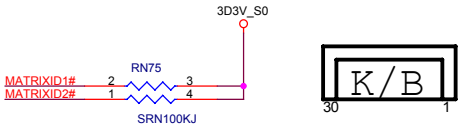
TOUCH PAD

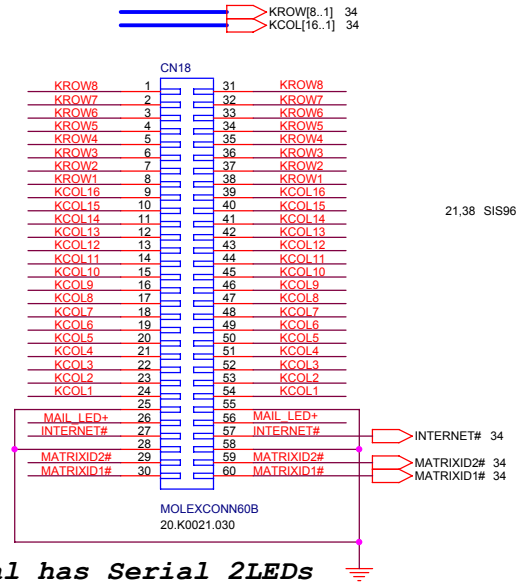


TOUCAN2:SA

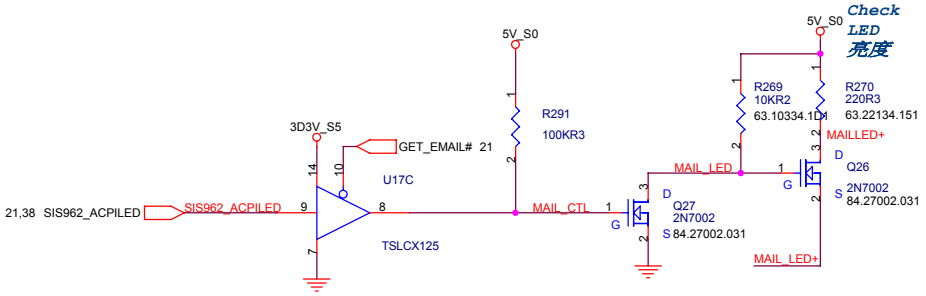
ALPS,KGDDET014A

Internal KeyBoard CONN





Internal has Serial 2LEDs



Follow H2U Design

SB

Keyboard matrix (from vendor)

		US	Eur	Jap	Other
Low Bit	MATRIXID1#	1	0	1	0
High Bit	MATRIXID2#	1	1	0	0

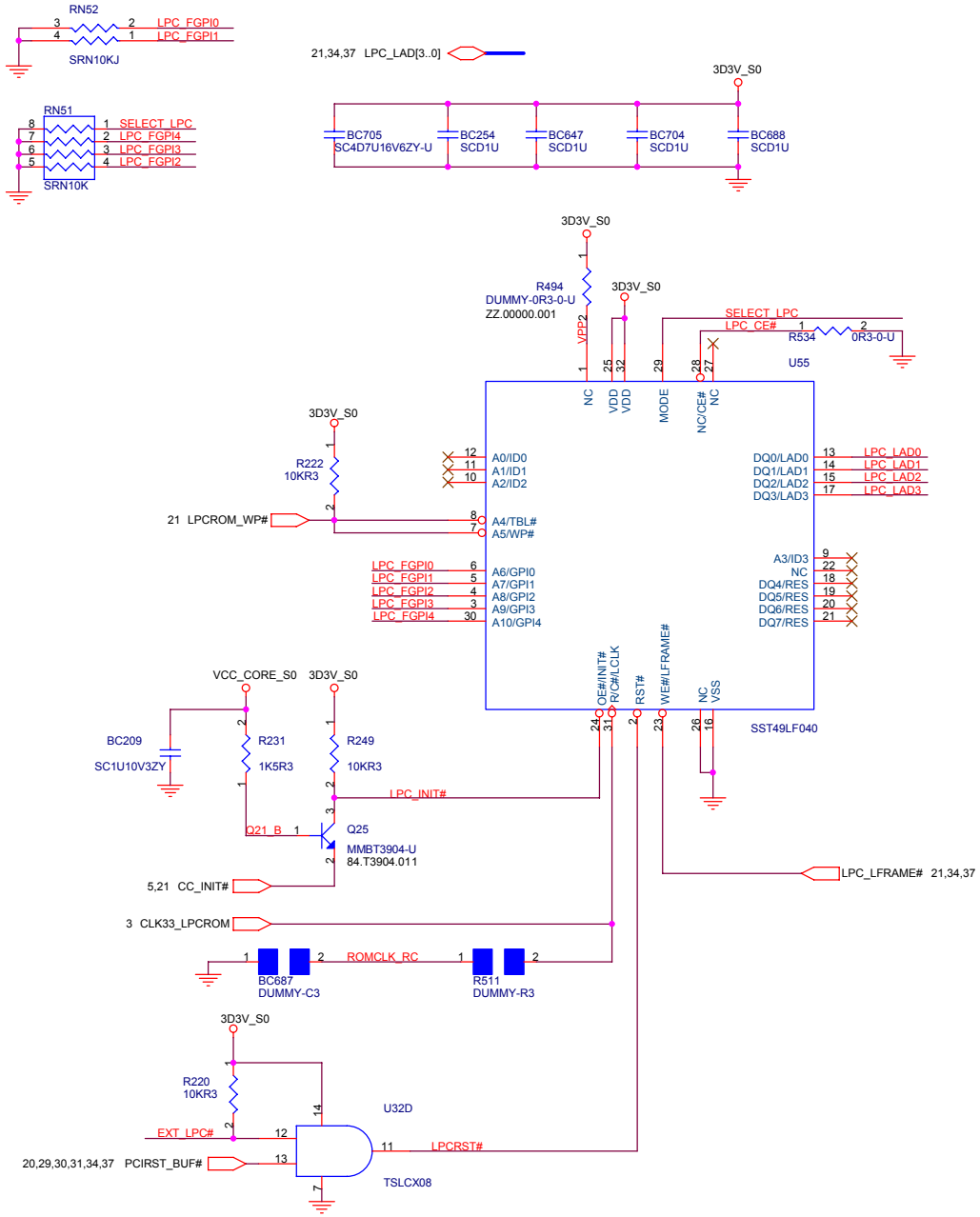
緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **TOUCHPAD / KB CONN**

Size: A3 | Document Number: TOUCAN2 | Rev: 1

Date: Wednesday, December 18, 2002 | Sheet 35 of 47

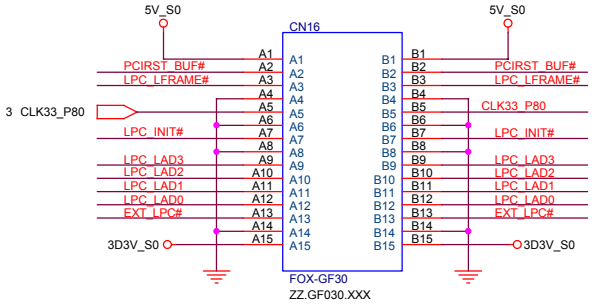


TOP VIEW

A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

(BOTTOM VIEW)

GOLDEN FINGER FOR DEBUG BOARD



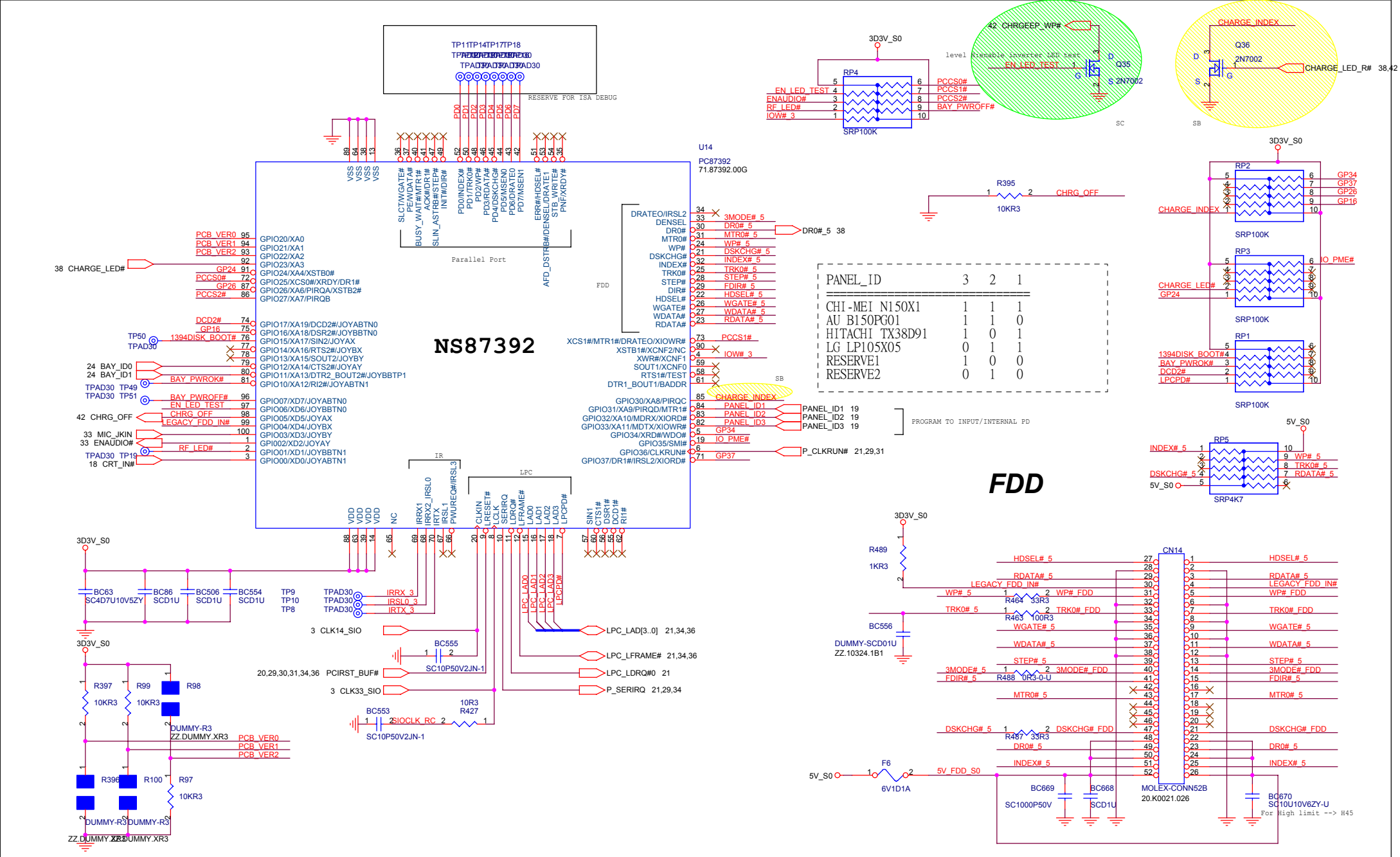
PLCC 32pin ST: 72.50040.003
PLCC 32pin SST:
72.49004.B03

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

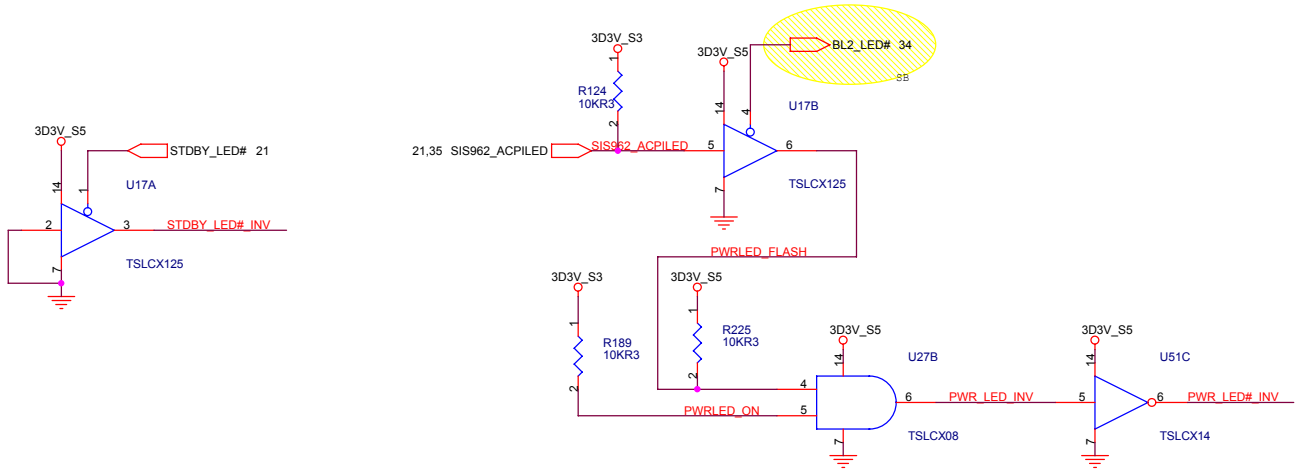
Title: ***LPCROM / DEBUG PORT***

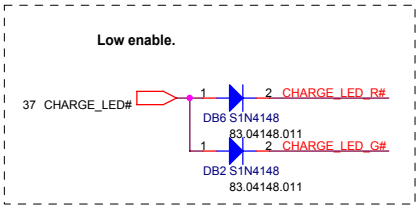
Size	Document Number	Rev
A3	TOUCAN2	1

Date: Wednesday, December 18, 2002 Sheet 36 of 47

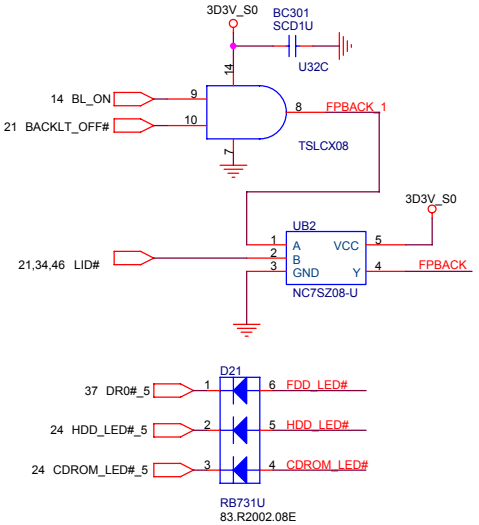

NS87392
U14
PC87392
71.87392.00G
FDD
Parallel Port
RESERVE FOR ISA DEBUG
IR
LPC
SB
SC
PANEL_ID 3 2 1
CHI-MEI N150X1 1 1 1
AU B150PG01 1 1 0
HITACHI TX38D91 1 0 1
LG LP105X05 0 1 1
RESERVE1 1 0 0
RESERVE2 0 1 0
PROGRAM TO INPUT/INTERNAL PD
FDD
Board Ver. Setting
Ver. PCB_VER0 PCB_VER1 PCB_VER2
SA 0 1 1
SB 1 0 1
1 1 0
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
SUPER IO
TOUCAN2
Size A3
Rev 1
Date: Friday, December 27, 2002
Sheet 37 of 47

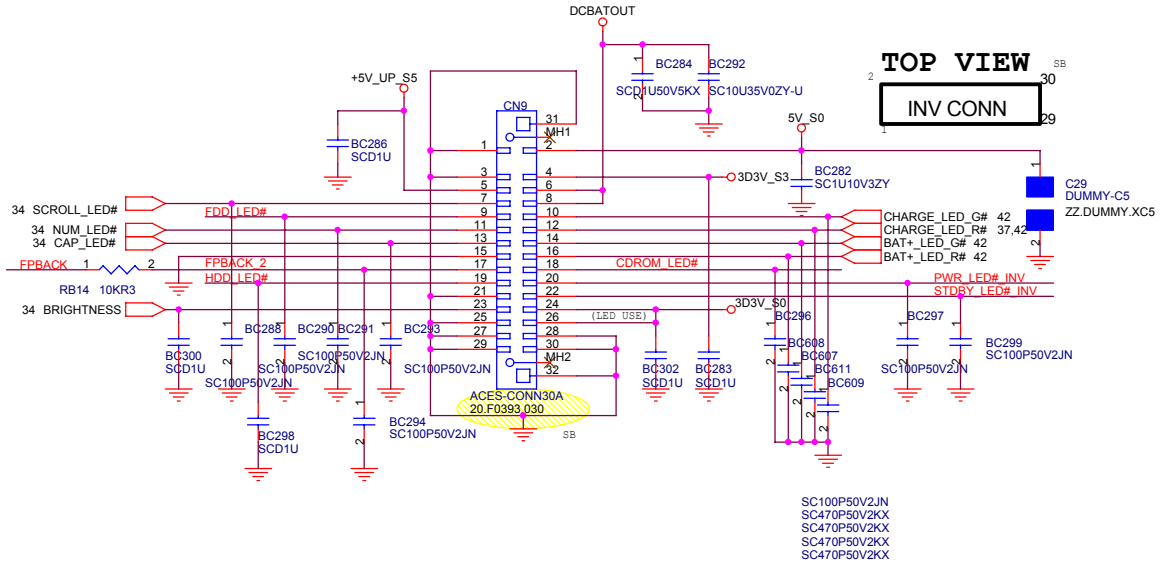
BL_LED# :ENABLE PWR LED BLINK WHEN S3





INVERTER/LED





緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

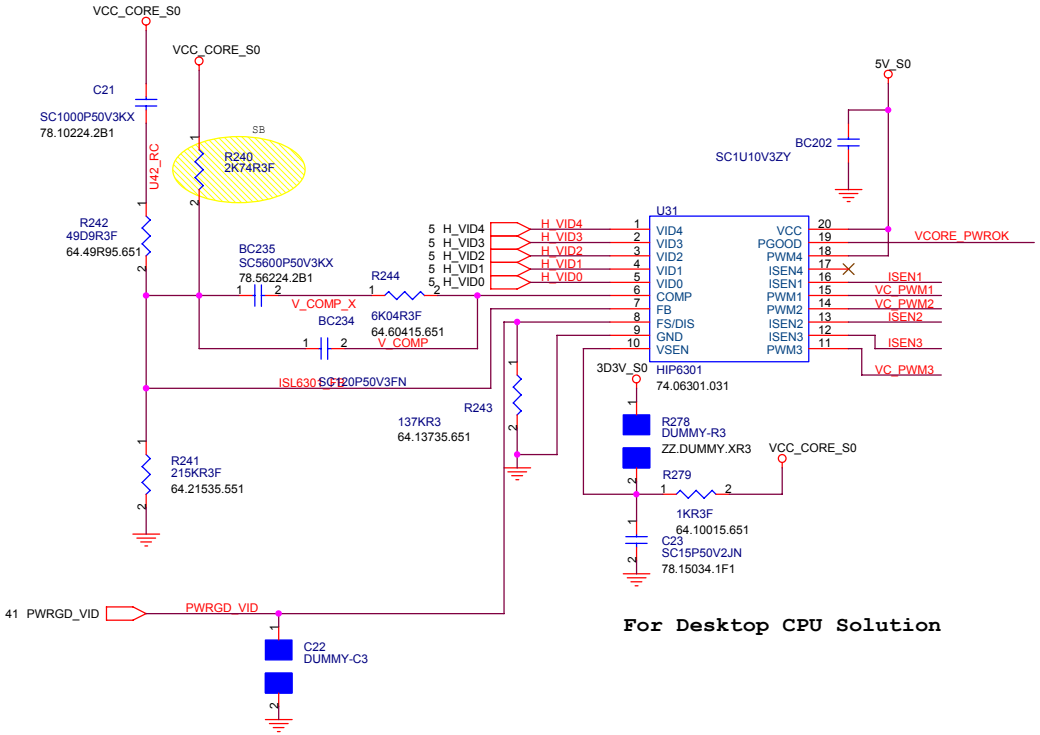
Title: **INVERTER**

Size	Document Number	Rev
A3	TOUCAN2	1

Date: Tuesday, December 31, 2002 Sheet 38 of 47

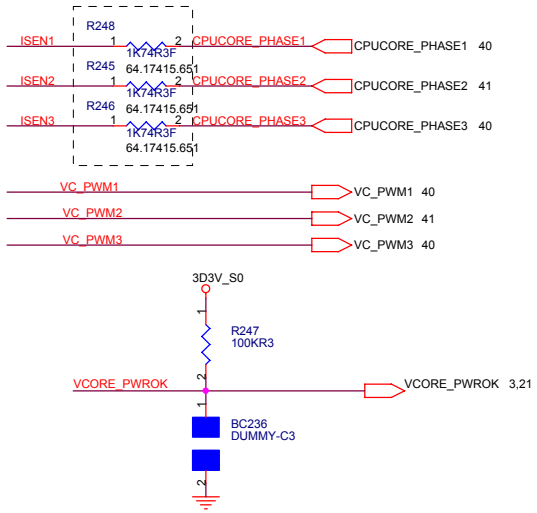
Voltage Identication Codes

VID4	VID3	VID2	VID1	VID0	VDAC
1	1	1	1	1	OFF
1	1	1	1	0	1.100
1	1	1	0	1	1.125
1	1	1	0	0	1.150
1	1	0	1	1	1.175
1	1	0	1	0	1.200
1	1	0	0	1	1.225
1	1	0	0	0	1.250
1	0	1	1	1	1.275
1	0	1	1	0	1.300
1	0	1	0	1	1.325
1	0	1	0	0	1.350
1	0	0	1	1	1.375
1	0	0	1	0	1.400
1	0	0	0	1	1.425
1	0	0	0	0	1.450
0	1	1	1	1	1.475
0	1	1	1	0	1.500
0	1	1	0	1	1.525
0	1	1	0	0	1.550
0	1	0	1	1	1.575
0	1	0	1	0	1.600
0	1	0	0	1	1.625
0	1	0	0	0	1.650
0	0	1	1	1	1.675
0	0	1	1	0	1.700
0	0	1	0	1	1.725
0	0	1	0	0	1.750
0	0	0	1	1	1.775
0	0	0	1	0	1.800
0	0	0	0	1	1.825
0	0	0	0	0	1.850



For Desktop CPU Solution

R451,R470,R480,These three resistors place close to controller IC

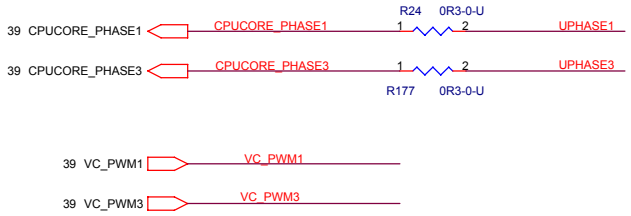


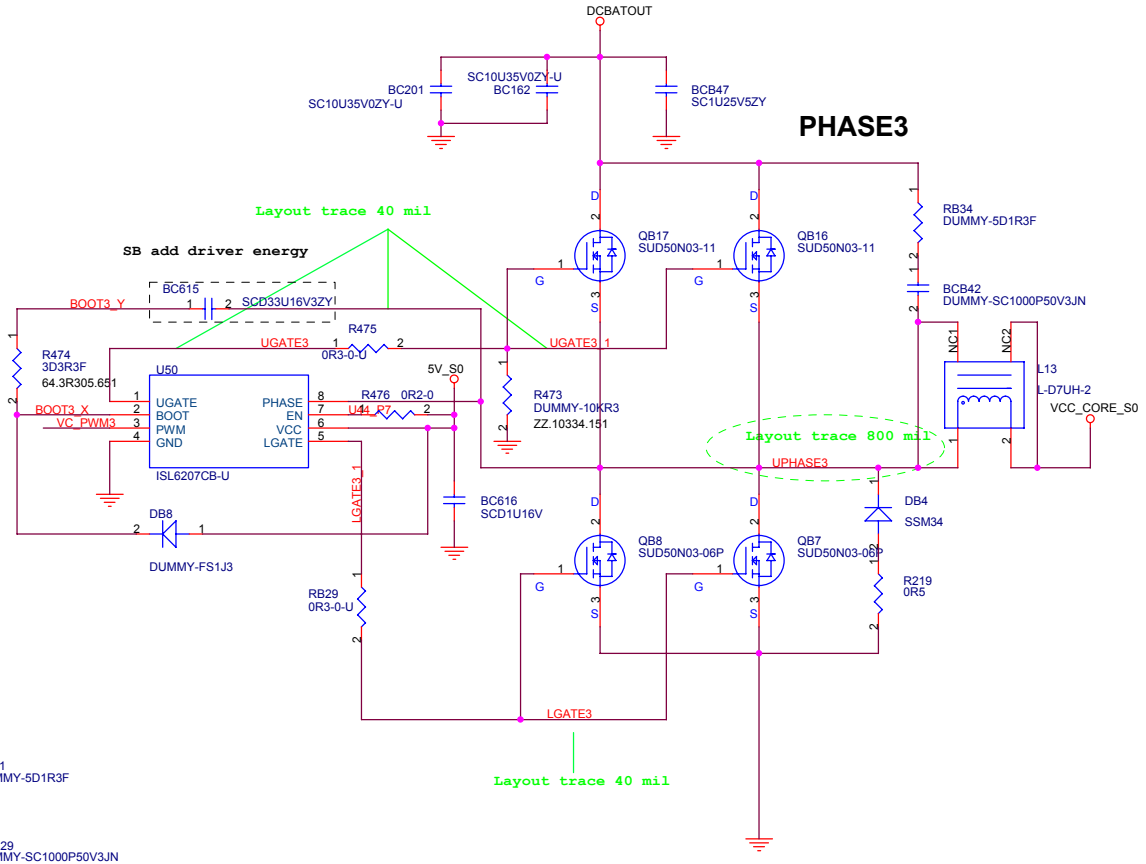
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

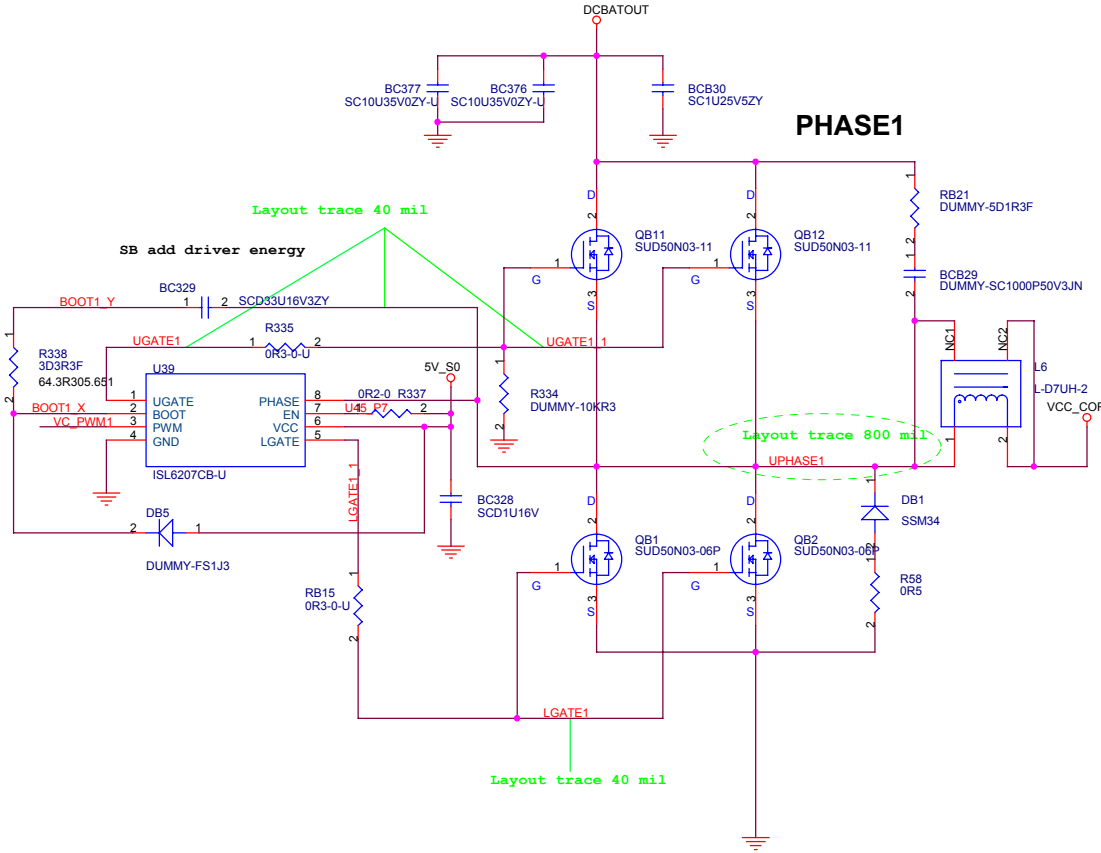
Title: CPU D/D +VCC_CORE(1/3)

Size: A3 | Document Number: TOUCAN2 | Rev: 1

Date: Wednesday, December 18, 2002 | Sheet 39 of 47







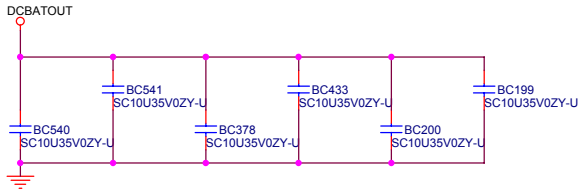
VCC_CORE_S0 : 1.5V or 1.525V

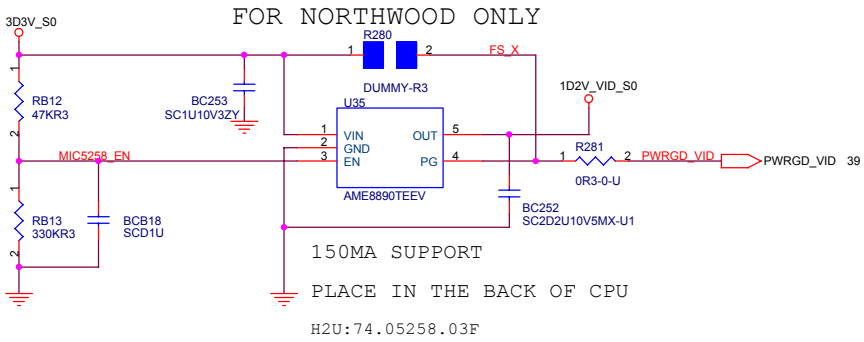
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

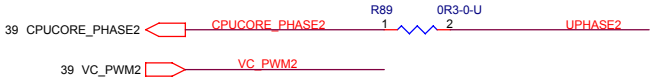
Title: CPU D/D +VCC_CORE(2/3)

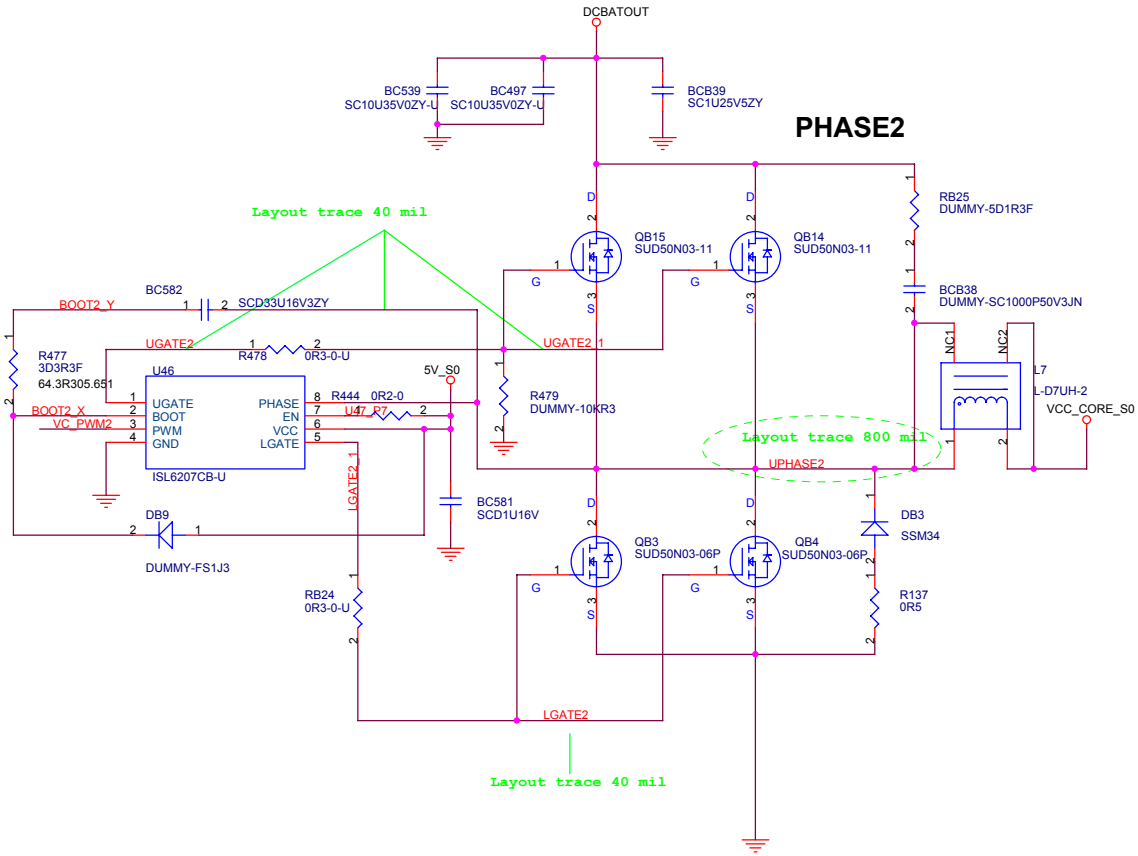
Size: A3 | Document Number: TOUCAN2 | Rev: 1

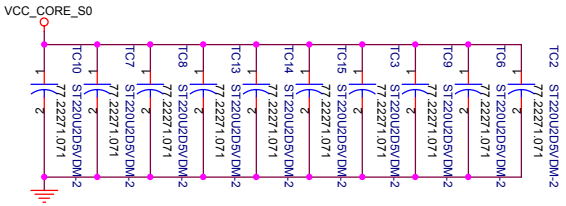
Date: Wednesday, December 18, 2002 | Sheet 40 of 47











緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	CPU D/D +VCC_CORE(3/3)	
Size A3	Document Number TOUCAN2	Rev 1
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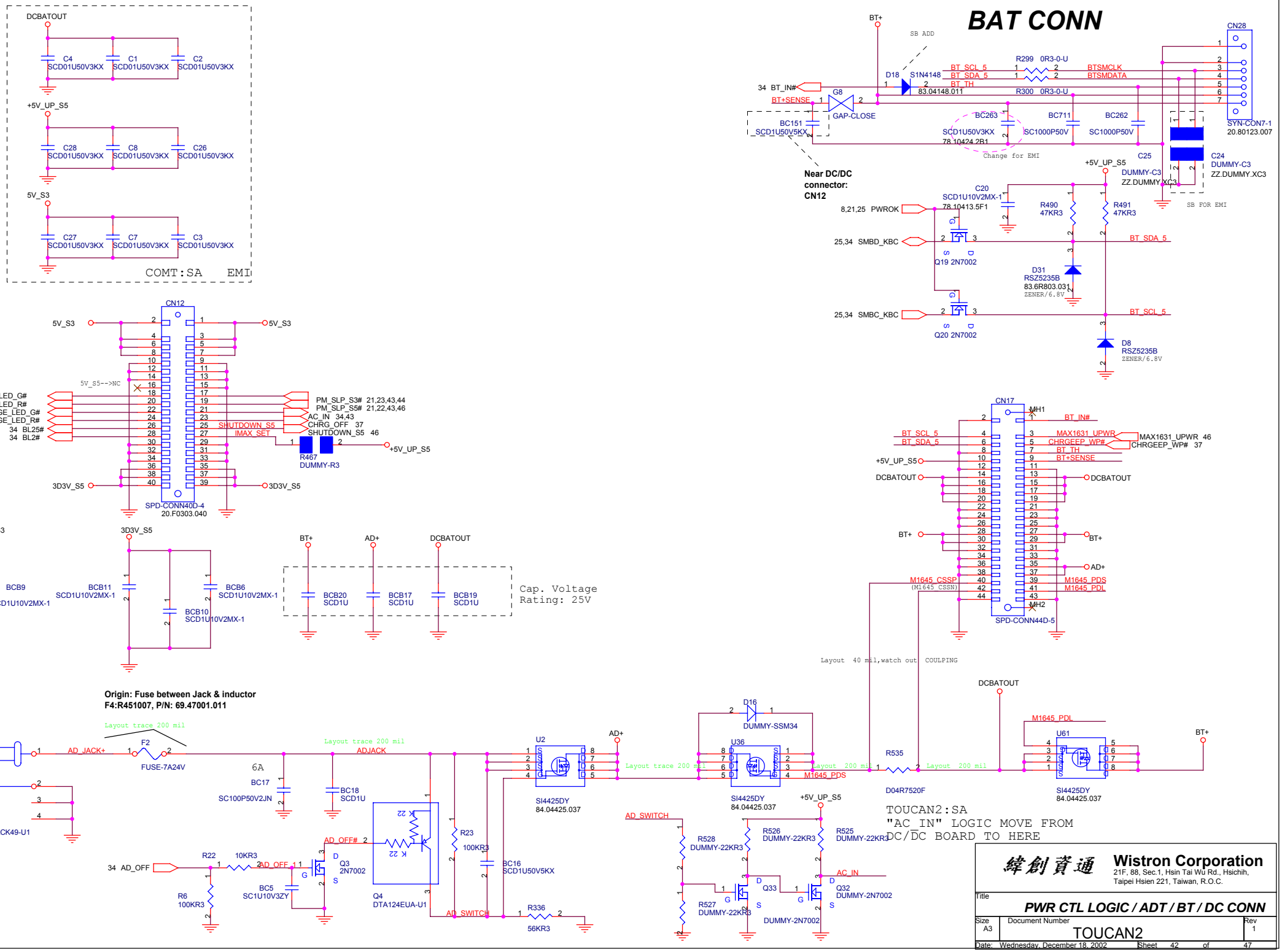
BAT CONN



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**PWR CTL LOGIC / ADT / BT / DC CONN**	
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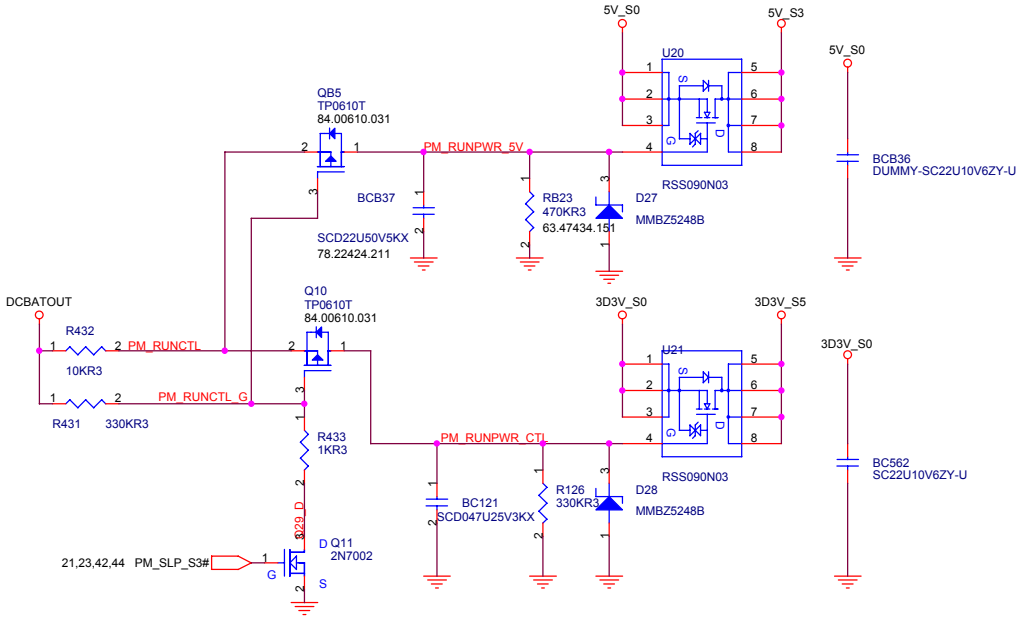
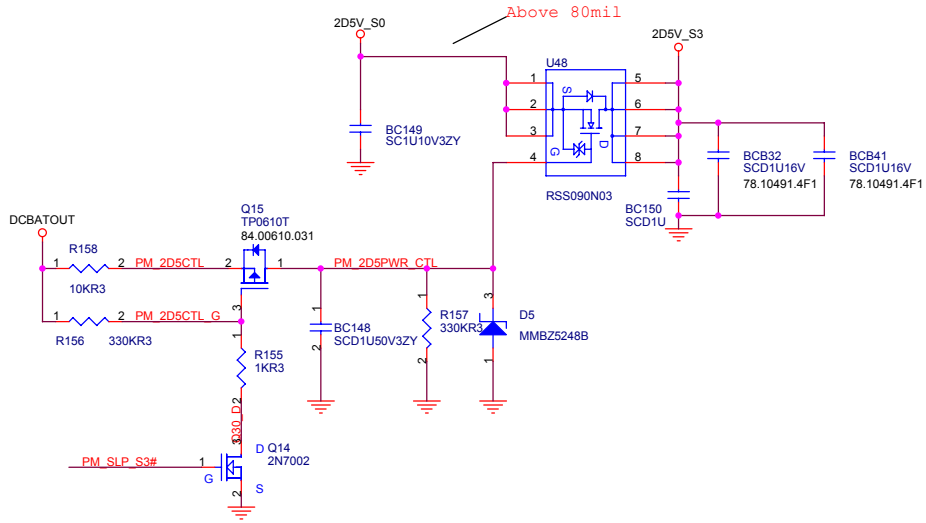
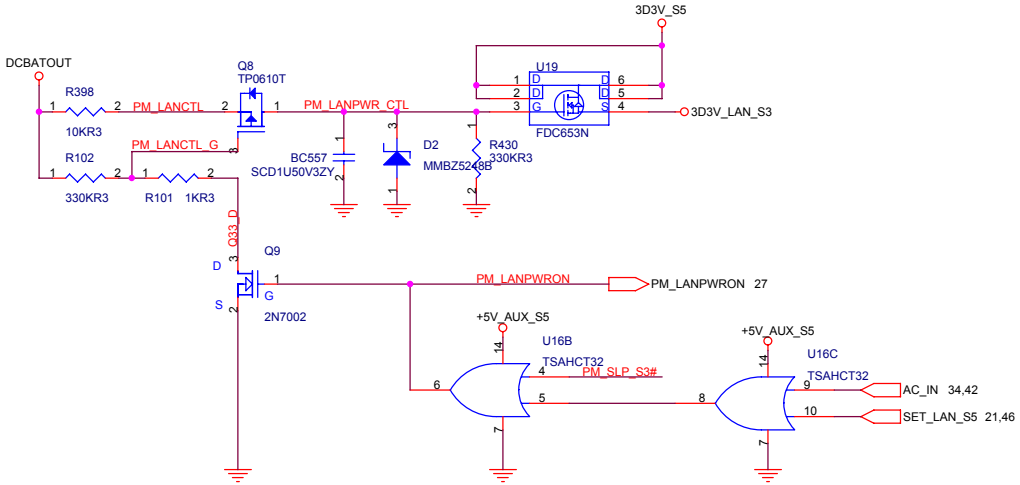
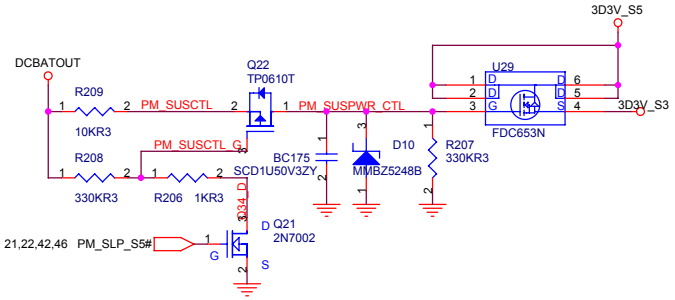


2.5VS0 --FOR DDRCLK_BUFFER







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Title	***DC/DC (1/3) -- 5V / 3.3V / 2.5V***	
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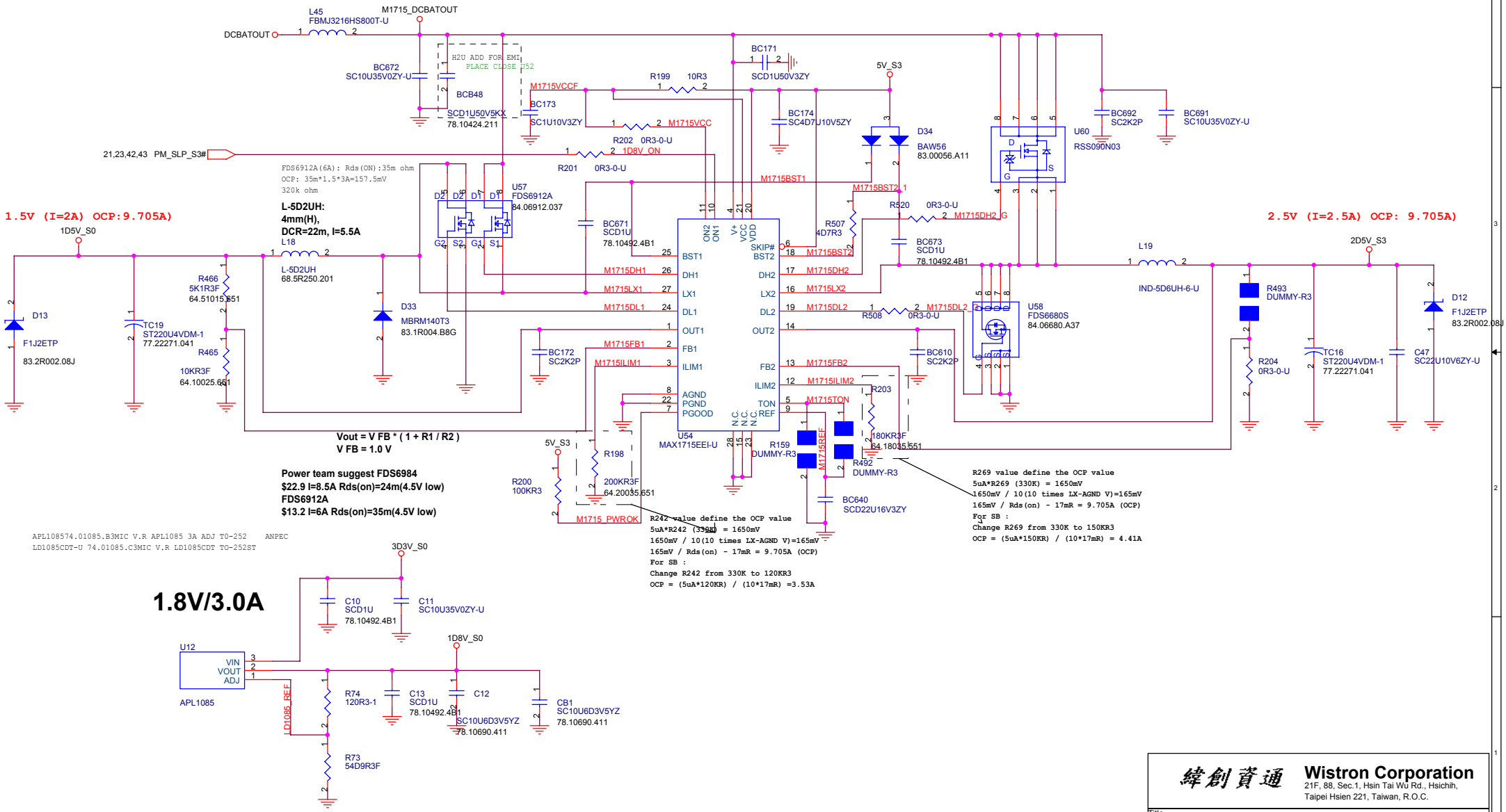

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***DC/DC (2/3) -- 2.5V /1.8V***	
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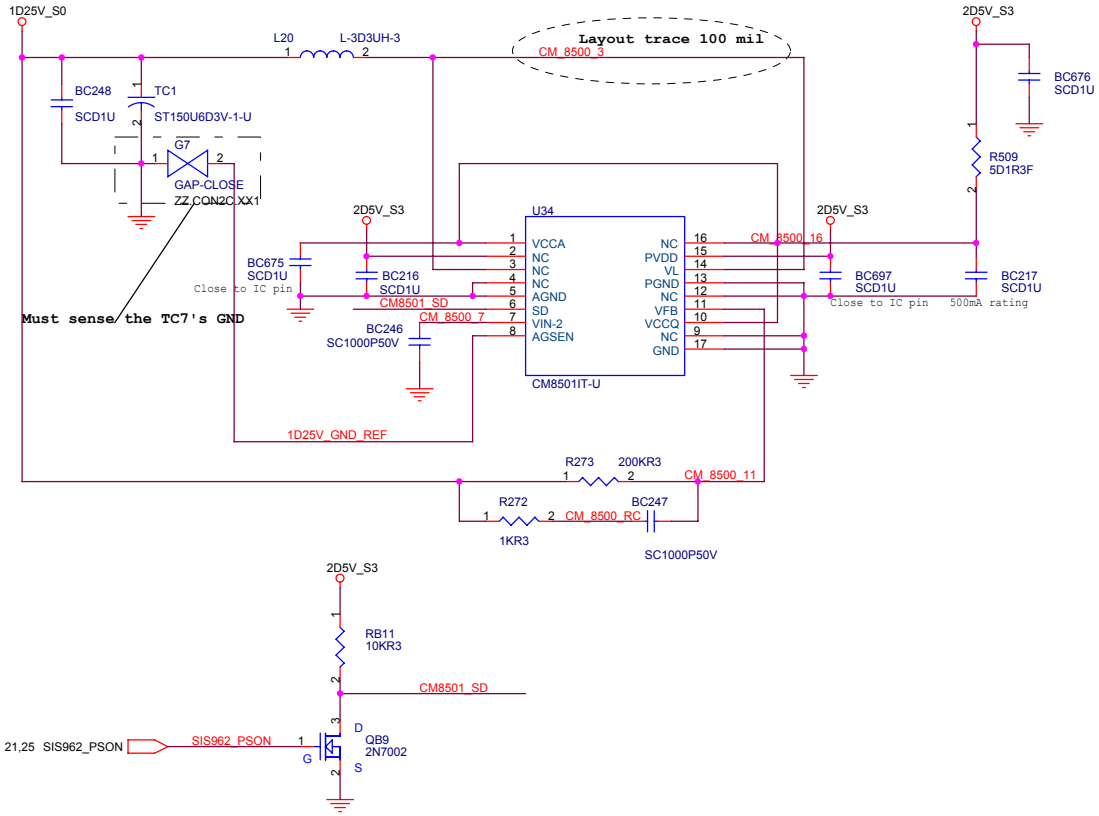
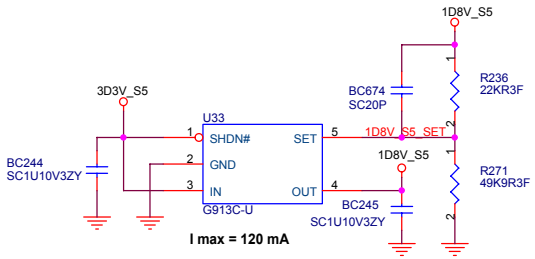
CM8501 can support 1.5A





緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: DC/DC (3/3) 1.8V_S5 / 1.25V		
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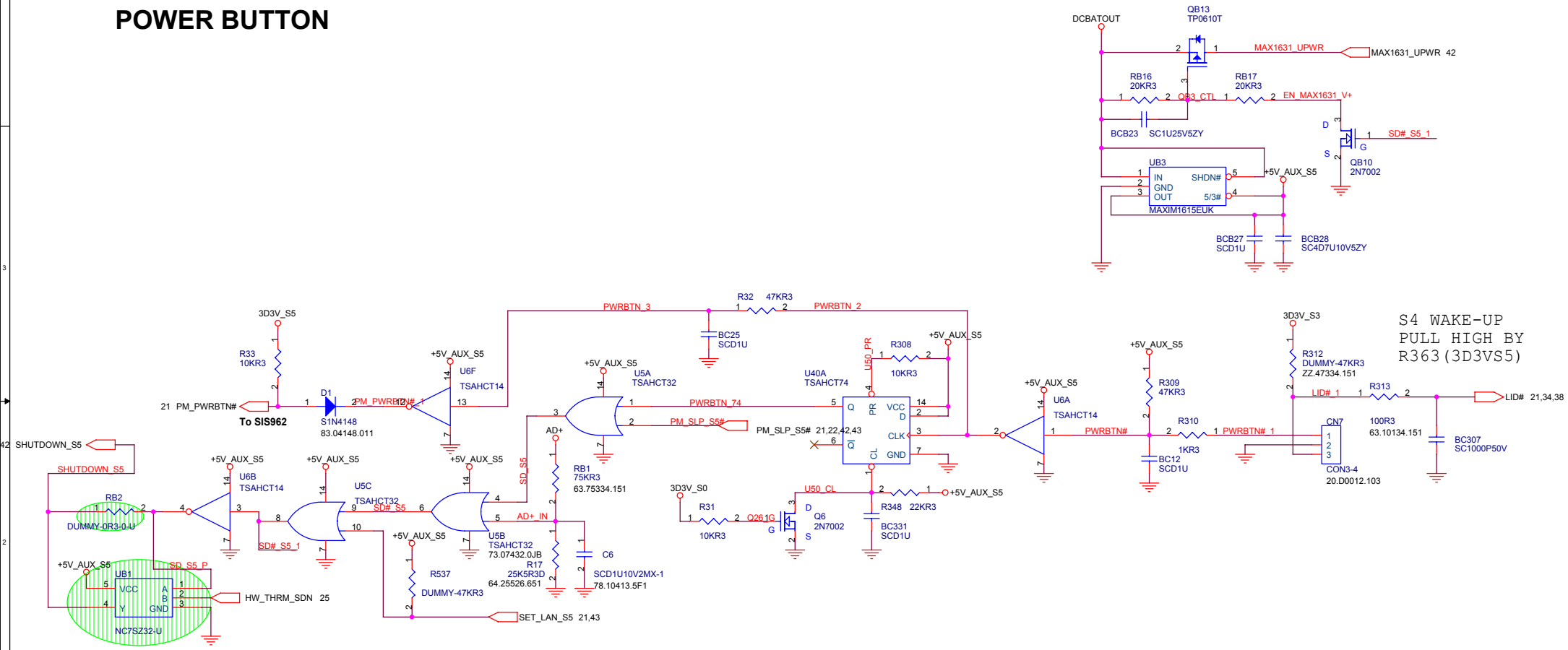
POWER BUTTON



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Title	***Power Button***	
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NEAR CPU

5,21 CC_SMI# — TP43

+5V_AUX_S5 — U6C, U6D, U6E — TSAHCT14

5V_S0 — U30F — TSAHCT14

3D3V_S5 — U17D — TSLCX125

5V_AUDIO_S0 — U47D — TSAHCT86 — AUD_AGND, AUD_AGND

+5V_AUX_S5 — U5D — TSAHCT32

5V_S0 — U30C — TSAHCT14

3D3V_S0 — U32A — TSLCX08

3D3V_S5 — U51D — TSLCX14

3D3V_S0 — U43C — TSLCX14

3D3V_S0 — U43B — TSLCX14

+5V_AUX_S5 — U40B — VCC, D, CLK, GND, PR, CL, Q, QI — TSAHCT74

5V_S0 — U38D — TSAHCT125 — 73.74125.0JB

1D5V_S0 — C48 SCD1U16V3KX

3D3V_S3 — C49 SCD1U16V3KX

1D8V_S0 — C50 SCD1U16V3KX

+5V_AUX_S5 — U16A — TSAHCT32

+5V_AUX_S5 — U16D — TSAHCT32

SB: EMI

3D3V_S0 — BC715 — 1D8VLVDDR_S0 — SC470P50V2KX

3D3V_S0 — BC716 — 1D5V_S0 — SC470P50V2KX

2D5V_S0 — BC717, BC718 — 1D5V_S0 — SC470P50V2KX, SC470P50V2KX

2D5V_S0 — BC719, BC720, BC721, BC722 — 3D3V_S0 — SC470P50V2KX, SC470P50V2KX, SC470P50V2KX, SC470P50V2KX

GND29 GNDPAD

GND25 GNDPAD, GND26 GNDPAD, GND27 GNDPAD, GND28 GNDPAD

EMI-88

GND23 GNDPAD-S1, GND24 GNDPAD-S1 — 34.34S02.001

MDC Stand Off
P/N:
34.41Q08.001

HOLE31 HOLELCD, HOLE32 HOLELCD — 34.41T01.001

LCD Stand Off
P/N:
34.41T01.001

HOLE3 HOLELCD — 34.41T01.001

DC/DC Stand Off
P/N:
34.41T02.001

HOLE21 HOLEDC, HOLE25 HOLEDC — 34.41T02.001

SPARE GATES

HOLE6 HOLE — ZZ.0HOLE.XXX
HOLE7 HOLE
HOLE8 HOLE
HOLE10 HOLE
HOLE4 HOLE
HOLE13 HOLE
HOLE14 HOLE
HOLE5 HOLE
HOLE2 HOLE
HOLE17 HOLE
HOLE18 HOLE

HOLE19 HOLE
HOLE20 HOLE
HOLE1 HOLE
HOLE23 HOLE
HOLE24 HOLE
HOLE16 HOLE — AUD_AGND
HOLE26 HOLE
HOLE27 HOLE
HOLE28 HOLE
HOLE29 HOLE
HOLE30 HOLE

HOLE22 HOLE2 — ZZ.HOLE2.XXX

S1:34.39S03.001

FOR 1394 MASK

HOLE9 HOLE, HOLE11 HOLE, HOLE15 HOLE, HOLE12 HOLE

GND20 GNDPAD-S1

GND8 GNDPAD — ZZ.NDPAD.XXX
GND9 GNDPAD
GND13 GNDPAD
GND15 GNDPAD
GND16 GNDPAD

GND1 GNDPAD
GND18 GNDPAD

GND14 GNDPAD-S2, GND17 GNDPAD-S2, GND19 GNDPAD-S2

S2:34.41T19.001

GND21 GNDPAD-S3, GND22 GNDPAD-S3, GND10 GNDPAD-S3

GND11 GNDPAD-S3, GND12 GNDPAD-S3, GND2 GNDPAD-S3 — 34.42P26.001

S3:34.42P26.001

GND5 GNDPAD-S1 — 34.39S03.001

GND3 GNDPAD-S1, GND6 GNDPAD-S1

GND4 GNDPAD-S1, GND7 GNDPAD-S1

Spring for ME

34.39S03.001	GND6 / GND7 / GND8 / GND15
34.41T19.001	GND11 / GND12 / GND17
34.42P26.001	GND1 / GND2 / GND5 GND14 / GND18 / GND 20

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: MISC

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