Olan (TM15") Block Diagram

Project code: 91.4Z701.001
PCB P/N : 48.4Z701.001
REVISION : 07249-1

DDR2 667/800 MHz 8,9
DDR2 667/800 MHz 8,9
667/800MHz
667/800MHz
AMD Giffin CPU S1G2 (35W)
638-Pin uFCPGA638
4,5,6,7
OUT
IN
16X16
G792 25
CLK GEN.
SILEGO SLG8SP628 3
North Bridge
AMD RS780M
CPU I/F LVDS, CRT I/F
INTEGRATED GRAHPICS
11,12,13
A-Link 4X4
CRT 18
LCD 16
HDMI 19
PCIex16
VGA Borad 37
45,46
CRT
DVI
RJ45
Port Replicator
USBX4
HP OUT
MIC IN
LINE IN
LAN
Giga LAN BCM5764M 35
TXFM 36
RJ45 36
New card 38
PWR SW TPS2231 38
Mini Card Kedron a/b/g/n 39
PCIex1
Line In 42
MIC In 42
42
Line Out (No-SPDIF)
Codec ALC268 40
AZALIA
South Bridge
AMD SB700
USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
ATA 66/100
ACPI 1.1
LPC I/F
PCI/PCI BRIDGE
20,21,22,23,24
42
INT.SPKR
OP AMP G1454R 41
RJ11
MODEM MDC Card 29
PCI
Cardbus OZ711MZ 32
MS/MS Pro/xD /MMC/SD/SD IO 5 in 1 33
PCMCIA SLOT 34
LPC BUS
USB
SATA
KBC Winbond WPC775 43
BIOS Winbond W25X80 44
LPC DEBUG CONN 44
Launch Buttom 15
Mini USB Blue Tooth 28
Camera
Finger Printer 31
USB 4 Port 30
Touch Pad 43
INT. KB 43
HDD SATA 27
ODD SATA 26

PCB STACKUP

TOP
VCC
S
S
GND
BOTTOM

SYSTEM DC/DC TPS51125 51

INPUTS	OUTPUTS
DCBATOUT	5V_S5(7A) 3D3V_S5(7A)

SYSTEM DC/DC TPS51124 52

INPUTS	OUTPUTS
DCBATOUT	1D1V_S0(9A) 1D2V_S0(5A)

SYSTEM DC/DC TPS51117 53

INPUTS	OUTPUTS
DCBATOUT	1D8V_S3(10A)

RT9026PFP 54

5V_S5	DDR_VREF_S3 0D9V_S3

RT9166 54

3D3V_S0	2D5V_S0 (300mA)

G957 54

3D3V_S0	1D5V_S0 (1A)

G9161 54

3D3V_S5	1D2V_S5 (400mA)

CHARGER BQ24745 55

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A UP+5V 5V 100mA

CPU DC/DC ISL6265HR 50

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0_0 0~1.55V 18A VCC_CORE_S0_1 0~1.55V 18A VDDNB 0~1.55V 18A

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM
Size: A3 | Document Number: Olan | Rev: -1
Date: Friday, April 18, 2008 | Sheet 1 of 58

5.Page 19: "HDMI1" add 2'nd source 62.10078.171.
6.Page 18: "F3" change to FUSE-1A6V-2-GP.
7.Page 30: "USBCN1" change to "20.F0765.020"
8.Page 26: ODD connector "SKT1" change to "62.10065.291"
9.Page 40: Add analog MIC schematic.
10.Page 46: Add "RN65" for NO duck LAN LED
11.Page All: Close PWR GAP
12.Page 03: Update "U18" foot print
13.Page 57: Add test point under Dimm Door
14.Page 55: "R32" pull hi from "3D3V_AUX_S5" to "BQ24745_VREF"
15.Page 41: Change audio AMP to G1454R41
16.Page 55: Change C34 size from 0402 to 0603
17.Page 57: Add EMI capacitor follow EMI recommend
18.Page 22: Add E-SATA schematic
==========
2007/12/20
1.Page 12: "R109" change to "768R2F-1-GP"
2.Page 46: Remove "RN19" "RN21" "RN22" "RN23" "RN53" "RN54" "RN55" "RN56"
3.Page 46" connect U12 HDMI switch to PEG_TX
4.Page 51 : Modify 5V & 3D3V 51125_ENTIP1 & 51125_ENTIP2 schematic.
5.Page 06: PH 300 ohmo on "CPU_DBREQ#"; PL 300 ohmo on "CPU_TEST21" & "CPU_TEST24"
6.Page 12: PH "SUS_STAT#" 10K ohmo to 3D3V_S0
7.Page 45: Add "DOCK1" PIN 51 "CRT_DEC#"
8.Page 46: Modify HDMI switch to "PS8122QFN48G-GP"
==========
2007/12/25
1.Page 46: Connect "3D3V_S0" to U12 remove "3D3V_S0_PI"
2.Page 45: Add "R497" "R498" "R499" for DIS CRT switch
3.Page 46: Add Pi filter before dock & C818 C819 for VSYNC_5 and HSYNC_5
4.Page 37: Add "R618" PU for "AC/BAT_DET"
==========
2007/12/26
1.Page 21: Swap USB port 8 and Port 10.
2.Page 45: Follow net swap report.
3.Page 41: Add "R633" DY PL "1451_SD"
4.Page 46: RN19~RN23, RN42~RN45 & RN65 change to SRN0J-10-GP
5.page 43: Add R634 ,U17 pin120 connect “SPI_WP_R#”
6.Page 30: Follow Homa modify "USBCN1"
==========
2007/12/27
1.Page 11: NEW CARD PCIE channel change to channel 3.
2.Page 21: "DOCK_DT1#" change to "GEVENT7#" and DY 0 ohmo resistor
3.Page 37: Add "R618" PU for "AC/BAT_DET" on MXM pin 157, Connect MXM SMB with "RN53"
4.Page 45: Add Pi filter before dock
5.Page 18: change R113, R114, R106 and R99 to 33ohm. change C471, C468 and C466 to 2.2pf.
6.Page 43: Change R186 to 150ohm for PLT_RST1#_1 (KBC U20A)
7.Page 35: Change C86 to 150pf LAN_RST (LAN U8)
8.Page 32: Change C631 to 150pf PLT_RST1#_MXM (U58 OZ711)
9.Page 37: Change C510 to 330pf for PLT_RST1#_MXM (MXM)
10.Page 33: Add C650 to 220pf for PCIRST1# (CR U67)
11.Page 38: Add C639 to 220pf for NEW_RST# (NEW U66)
12.Page 43: R181 change to 30KF for BOM integrate
13.Page 39: Change R226 to 470ohm for MINI_RST# (MINI MINIC1)
14.Page 12: Add 330pf C551 between R313 and ground for SYSREST# (NB U43C).
15.Page 40: Change C379 to 56pf for RESET# (AUDIO U24)
16.Page 06: Change R298 to 33ohm for LDT_RST#_CPU
17.Page 45: Change RN4 connect to "CRT_R_S" "CRT_G_S" "CRT_B_S"
18.Page 24: Change R89 to 10R2J-2-GP for BOM integrate
19.Page 46: Follow net swap report.
20.Page 57: Add Spring "GND1" "GND2"
==========
2007/12/28
1.Page 57: Add EMI capacitor follow EMI recommend.
2.Page 45: ADD EC191 EC192 EC193 follow EMI recommend.
==========
2007/12/28a
1.Page 40: Codec IC change to ALC268.
2.Page 41: ADD U69 G1412 AMP for Line out.
3.Page 33: Add EMI capacitor Follow EMI recommend
==========
2007/12/31
1.Page 22: Change PlanarID to SB and ADD CLK_ID to identify Clock Gen.
2.Page 42: Modify "INTMIC1: to MONO MIC
3.Page 40: Modify ALC_268 to MONO MIC schematic, Add "DOCK_DT1#" on "GPIO1"
==========
2008/01/02
1.Page 40: Change Speaker and Line-out channel.
2.Page 40: Chanhe "DOCK_DT1#" connect to GPIO3 U24 pin 3.
3.Page 40: Modify "MIC" and "Line_in" schematic.
4.Page 30: Modify "USBCN1" schematic follow Homa.
5.Page 43: Add "R654" 10K PU 3D3V_S0 for "FP_DETECT#".
6.Page 21: Add "R200" 10K PU 3D3V_S0 for "FP_ID"
7.Page 51: Add "R549" 0 ohm for "MXM_THER".
8.Page 40: Change R196 to 64.39225.6DL 39.2K.
9.Page 21: Remove "R397" "R489" R490" "R491", add "RN56" for component count.
==========
2008/01/03
1.Page 50: Change C4 to SC1U10V3KX-3GP for BOM integrate
2.Page 55: Change C296 form SC1U25V5KX-1GP (P/N 78.10522.21L) to SC1U25V0KX-GP (P/N 78.10522.5BL)
3.Page 43: Remove "R188" "R177" "R185" "R189", add "RN56" for component count.
4.Page 46: Swap U12 Pin 29 & Pin 28; add C394, C395 D01u.
5.Page 22: Add U41 E-STAT solution
6.Page 21: Add R326 for NB_PWRGD
7.Page 48: Add R498 for NB_PWRGD
==========
2008/01/03a
1.Page 46: Modify SM BUS PH resistor
2.Page 40: Add "R119" and "R177" for ALC268 GPIO1
==========
2008/01/04
1.Page 22: Swap RN68 net
==========
2008/01/04a
1.Page 57: Remove H23; H24.
2.Page 06: Remove R300, R301, change to "RN71"
==========
2008/01/07
1.Page All: Follow Net swap report.
==========
2008/01/07a
1.Page 22: Swap U41 Pin 3, 4 & Pin 17, 18.
==========
2008/01/07b
1.Page 57: Add H23 screw holl.
==========
2008/01/07c
1.Page All: Follow Net swap report.
==========
2008/02/01
1.Page 45: Change "DOCK1" to 20.F1257.001.
==========
2008/02/04
1.Page 40: Add R327, R328, EC200, EC201 for EMI solution.
==========
2008/02/05
1.Page 22: Add R397 follow caystal FAE recommend.
2.Page All: Short 0 ohm resistor with PAD.
3.Page 18: Remove "D2" "D3" "D4" for ME & Layout
==========
2008/02/13
1.Page 41 & 42: Modify Line-out jack connection.
==========
2008/02/13a
1.Page 06: Follow AMD recommend Add & Dummy "R503" to PU "CPU_LDT_REQ#".
==========
2008/02/13b
1.Page 06: Change "R503" to "R304" to PU "ALLOW_LDTSTOP".
2.Page 06 & 12: Remove net "CPU_LDT_REQ#" Replace with "ALLOW_LDTSTOP"
3.Page 21: Add "R134" & "R185" for "HDMI" on SB700 "GPIO0".
4.Page 42: Change "C400" "C401" to "R301" & "R218"
==========
2008/03/03
page3, remove RN31 (control by SW)
page12,merge R105,R107 to RN29
merge R309,R310,R311 to RN72 (R309 can use 3K)
page14 merge R477,R476 to RN73
page16 RN1 change to 2 pcs 0ohm PAD "R476" "R477"
merge R29,R30 to RN53
page18 merge R106,R99 to RN75
merge R113,R114 to RN74
merge R283,R284 to RN30
merge R275,R276 to RN32
merge R319,R98 to RN31
page20 change R165,R164,R404,R403 to 0 ohm PAD (only use for strap,don't need 22 ohm)
page21 merge R170,R159 to RN34
merge R162,R160 to RN33
R185 for Dock(input can't floating)
page22 Short R140,R138
C672,C671,C673,C674 for E-SATA only,need add DIS
check with SW to remove CLK_ID setting(use SMBus)
dummy all E-SATA re-driver
change RN67,RN68 to PAD
page24 merge R437,R421 to RN35
merge R344,R355 to RN36
del R360,R366,merge R361,R365 to RN37
page35 change R265,R263,R67,R87,R72,R269,R270,R79,R260,R58,R54,R56,R38,R44,R42,R46,R74,R83 TO 0ohm PAD
page37 change r456 to PAD
page39 check R224/R225,R222/R229, need confirm spec

page40 check R327,R328 with EMI
change RN55,R325 to PAD
Modify schematic for current leackage on "DOCK_DT1#"
R119 for Dock (input can't floating)
page42 merge R217,R220 to RN55
merge R214,R215 to RN67
merge R475,R479 to RN76 (need change to 48 ohm)
page44 change ER1, ER2,ER4 to PAD
dummy EC69
change ER3 to 33 ohm
page47 change R316 to PAD
page48 level shift for NB_PWRGD
page50 change R12,R13,R14,R3,R4,R7 to PAD
page53 change R261 to PAD
page54 change R317,R318 to PAD
page55 change R148,R147,R132,R131 to PAD
merge R28,R32,R31,R37 to RN77 (please take care R32 power)
==========
2008/03/04
1.Page 26: Modify "SKT1" ODD connector.
2.Page 45: Merge "R292" "R293" to "RN68".
3.Page 51: change R416,R441 to PAD for noise issue.
4.Page 16: "F2" change to "69.50007.A31".
==========
2008/03/04b
1.Page 51: change R416,R442 to PAD and DY "R441" for noise issue.
2.Page 17: "LED3" change to "3D3V_S5" "LED2" change to "3D3V_AUX_S5".
3.Page 30: Modify "USBCN1" pin define.
4.Page 40: Remove "C377" "C379" short them
5.Page 40: Remove "R177" for new INTMIC connector
6.Page 42: Modify "INTMIC" schematic.
7.Page 45: Merge R497, R498, R499 to RN68; R287, R286, R289 to RN78.
8.Page 16: Add RN79 for ESD.
9.Page 45: "DOCK1" "PIN S51" change to "CRT_IN#_R" for ESD.
10.Page 45: Add "RN80" for ESD
11.Page 56: Add "D30" on "BAT_IN#" for ESD, Change "RN59" to 8P4R for "BAT_IN#" ESD
==========
2008/03/05
1.Page 32: Add "R220" and Dummy for "PME" issue.
2.Page 39: Change "3D3V_S5_MINI1" to "3D3V_S5" and Change "3D3V_S0_MINI" to "3D3V_S5".
3.Page 17: Merge "R485" "R486" to "RN81"; Merge "R487" "R488" to "RN82".
4.Page 17: Change "R473" to "453R2F-1-GP"; Change "R480" to "150R2F-1-GP".
5.Page 14: Merge "R179" "R180" to "RN83".
6.Page All: Follow Swap report.
==========
2008/03/06
1.Page 30: "USBCN1" pin 15 change to GND.
2.Page 22: Remove "U41" relative schematic.
3.Page 40: "RN41" change to 4P2R
4.Page 42: Merge "R474" "R475" to "RN84".
5.Page 42: Change "EC6" "EC7" "EC8" "EC9" to 0603
6.Page 40: Change "EC200" "EC201" to 0603
7.Page 38: "U66" change to 74.00577.A73
8.Page 57: ADD EMI capacitor "EC203" ~ "EC220".
9.Page 40: Merge "R329" "R330" "R325" to "RN85" for ESD.
10.Page 42: Short "RN67" with PAD.
==========
2008/03/06a
1.Page 51: Change "TC17" "TC10" to 77.21561.00L & mount.
2.Page 50: Change "C7" "C8" to 77.21561.00L & mount.
3.Page 52: Change "TC19" to 79.10712.L02.
4.Page 55: Add "C826" for Vendor suggest added decoupling capacitor in CSSN to ground.
==========
2008/03/07
1.Page 55: Change "D9" to 83.R0203.08F & mount.
2.Page 57: Add Spring "GND5 and EMI capacitor "EC221" ~ "EC229".
==========
2008/03/10
1.Page 57: Add "GND11" for EMI, "GND8" "GND9" "GND10" change to "34.15F09.001".
2.Page 52: Change "TC21" to SE100U25VM-L1-GP.
3.Page All: Follow Swap net.
==========
2008/03/10a
1.Page 55: Change "TC21" to SE100U25VM-L1-GP.
2.Page 57: Remove "GND6" "GND7".
==========
2008/03/11
1.Page 57: Remove "EC204" "EC205".
==========
2008/03/11a
1.Page 40: "R194" change to "51R2J-2-GP".
2.Page 29: "R235" change to "15R2J-GP" & DY "C424".
3.Page 21: Change "RN33" to "R655" & "R656" with "27R2J-1-GP"; Change "RN34" to "SRN47J-7-GP"; UNdummy "EC61" "EC62".
4.Page 48: Add "U70" for "NB_PWRGD" level shift.
==========

<Core Design>

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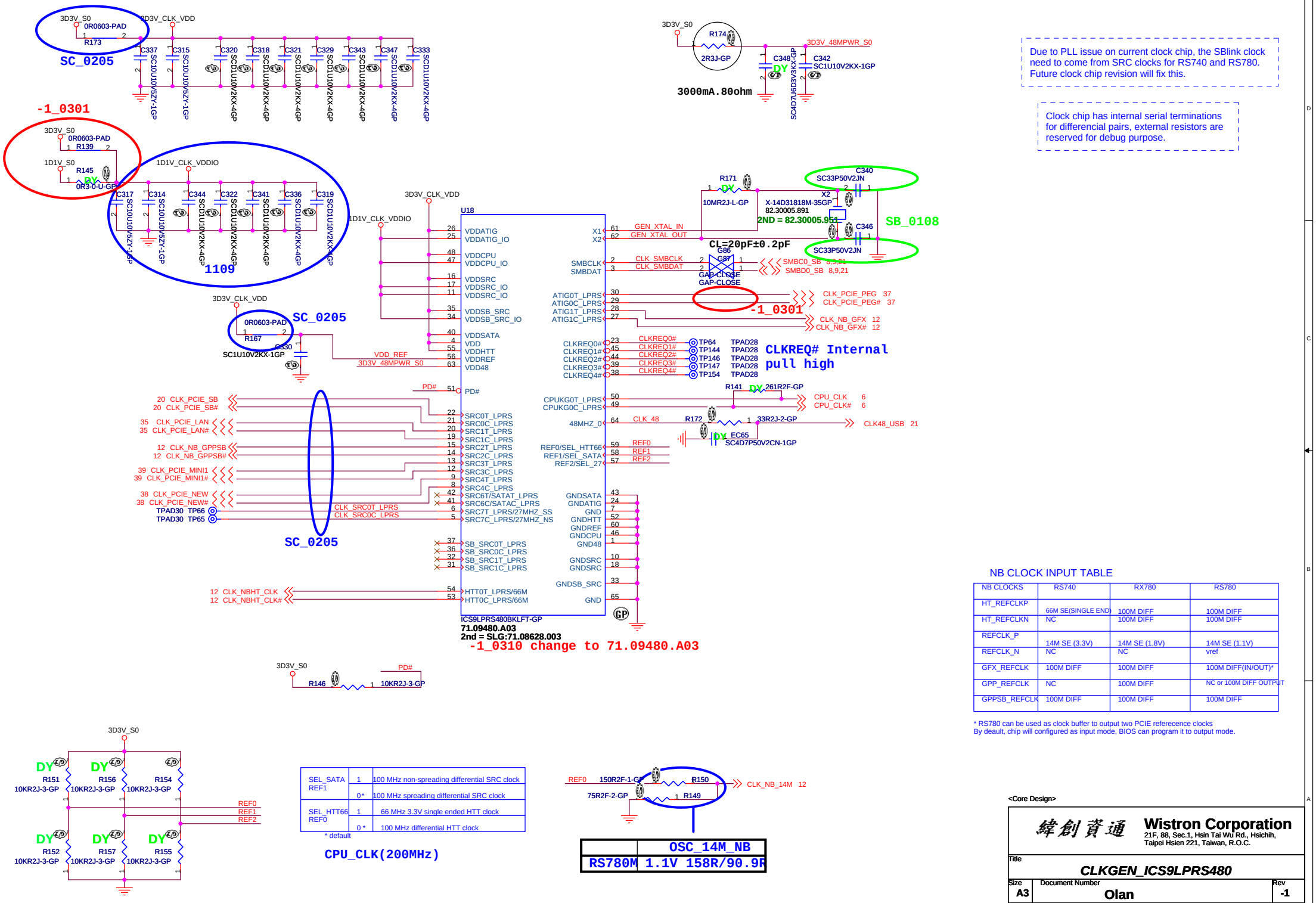
Title: HISTORY

Size	Document Number	Rev
A3	Olan	-1

Date: Friday, April 18, 2008 Sheet 2 of 58



NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

* RS780 can be used as clock buffer to output two PCIE referecence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.

SEL_SATA REF1	1	100 MHz non-spreading differential SRC clock
	0*	100 MHz spreading differential SRC clock
SEL_HTT66 REF0	1	66 MHz 3.3V single ended HTT clock
	0 *	100 MHz differential HTT clock

* default

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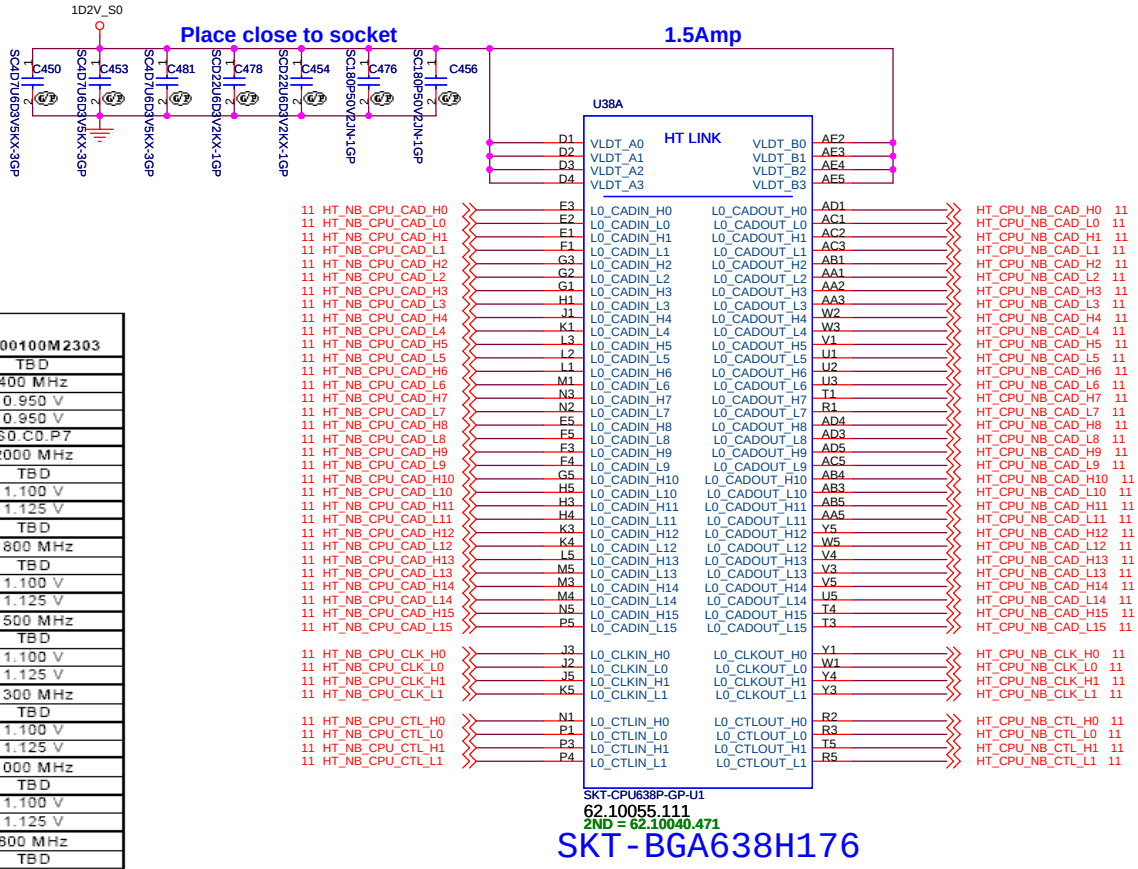
Title: CLKGEN_ICS9LPRS480

Size: A3 | Document Number: Olan | Rev: -1

Date: Friday, April 18, 2008 | Sheet 3 of 58



State	Specification	Notes	2M200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P2	CPU COF	1	1500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P3	CPU COF	1	1300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P4	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P6	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P7	CPU COF	1	300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V

<Core Design>

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Title: ***CPU_HT_LINK I/F_(1/4)***

Size	Document Number	Rev
A3	Olan	-1

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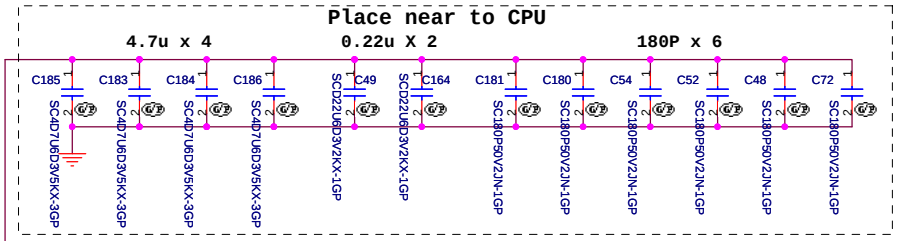

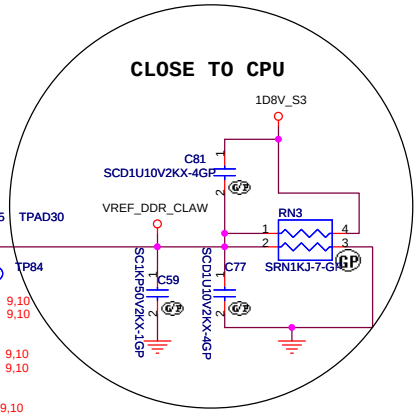

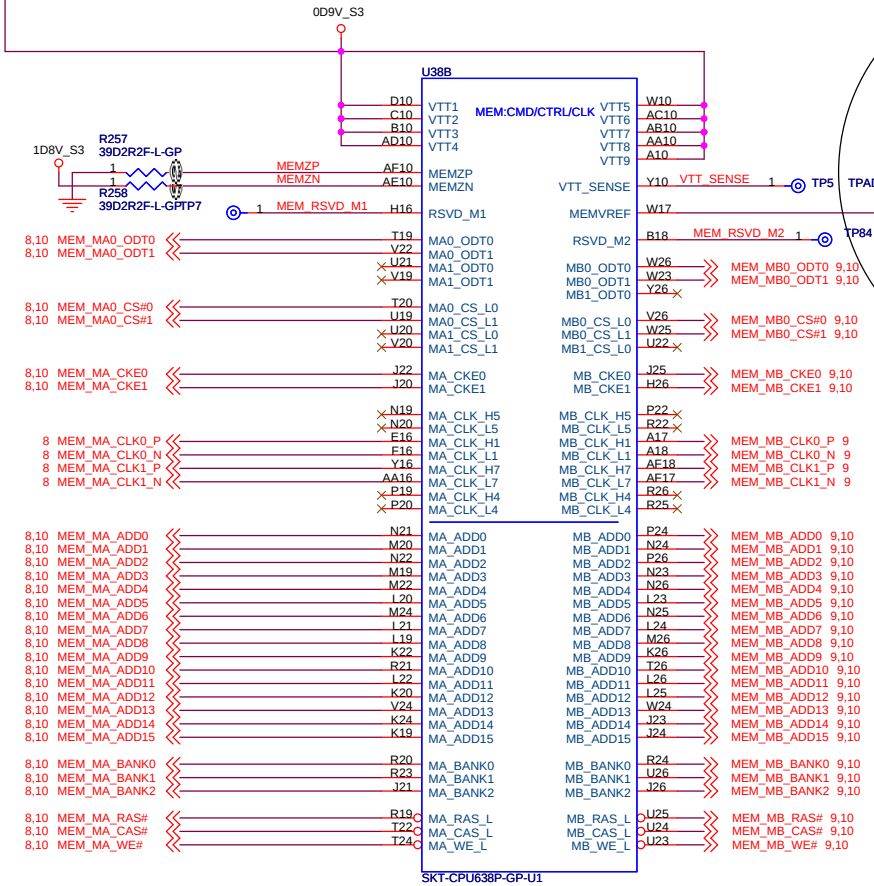

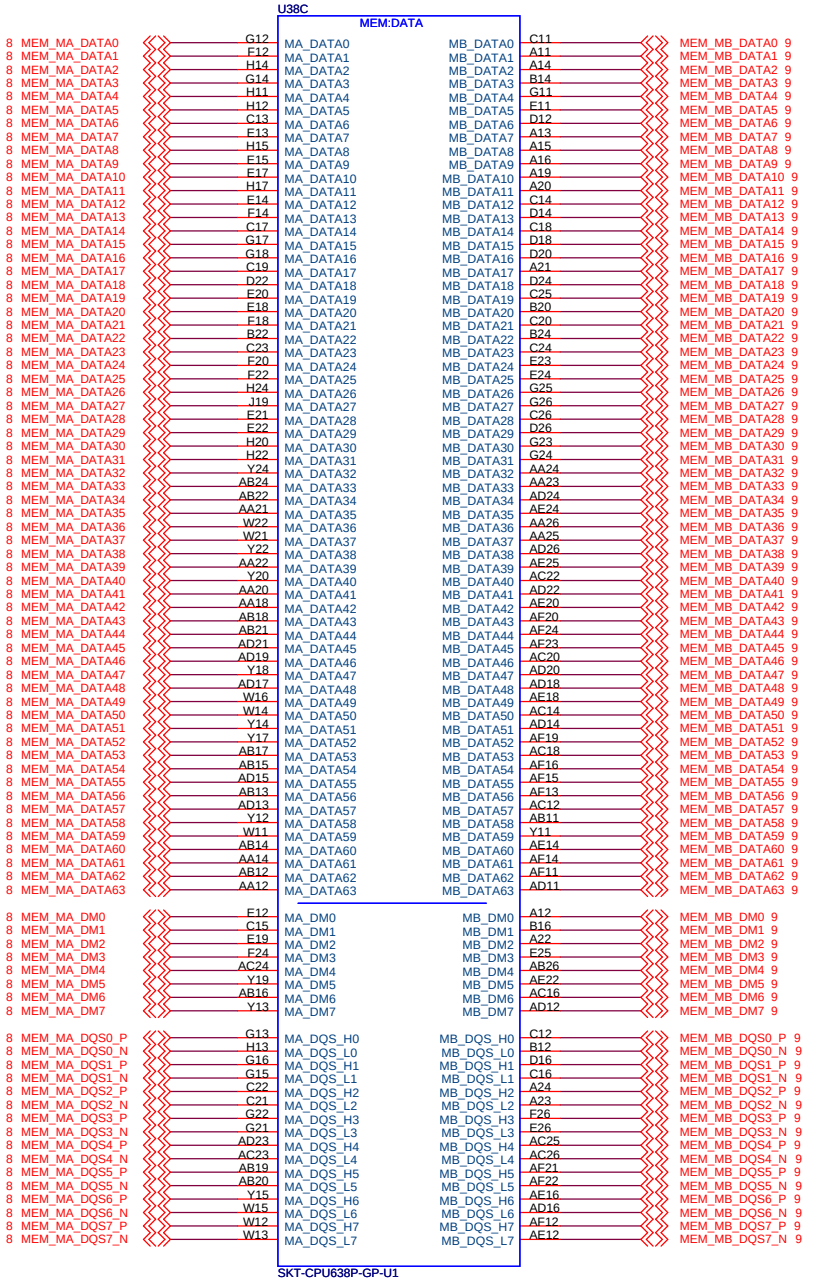

<Core Design>

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Title	***CPU_DDR_(2/4)***	
Size: A3	Document Number: **Olan**	Rev: -1
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The Processor has reached a preset maximum operating temperature. 100℃
I=Active HTC
O=FAN

SC_0213

SB

SB with 0402 PAD

IF 0 ohm IS NOT GOOD ENOUGH, TRY 68.00082.491

LYAOUT:ROUTE VDDA TRACE APPROX. 50mils WIDE(USE 2X25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

SC_0205

Cloce To CPU

For HDT DBG

internal pull high 300 ohm

LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

SB

SC_0205

U38D

SKT-CPU638P-GP-U1

SB

Near CPU PIN

2ND = 84.03904.H11

CPU exceeds 125℃

2ND = 84.03904.H11

HDT Connectors

SMC-CONN26A-FP

<Core Design>

緯創資通 **Wistron Corporation**
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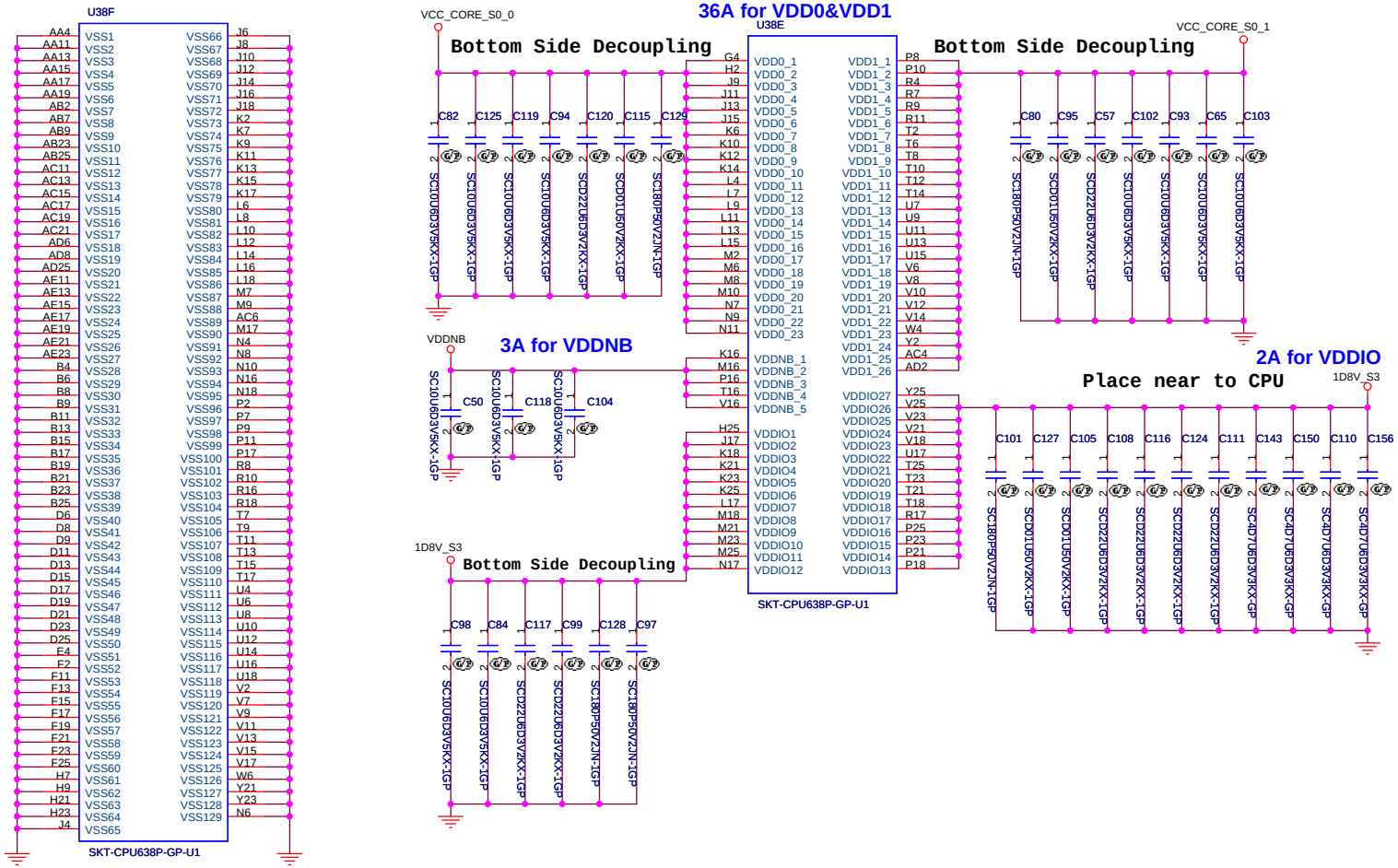
Title: ***CPU_Control&Debug_(3/4)***

Size	Document Number	Rev
A3	Olan	-1

Date: Friday, April 18, 2008 Sheet 6 of 58



<Core Design>

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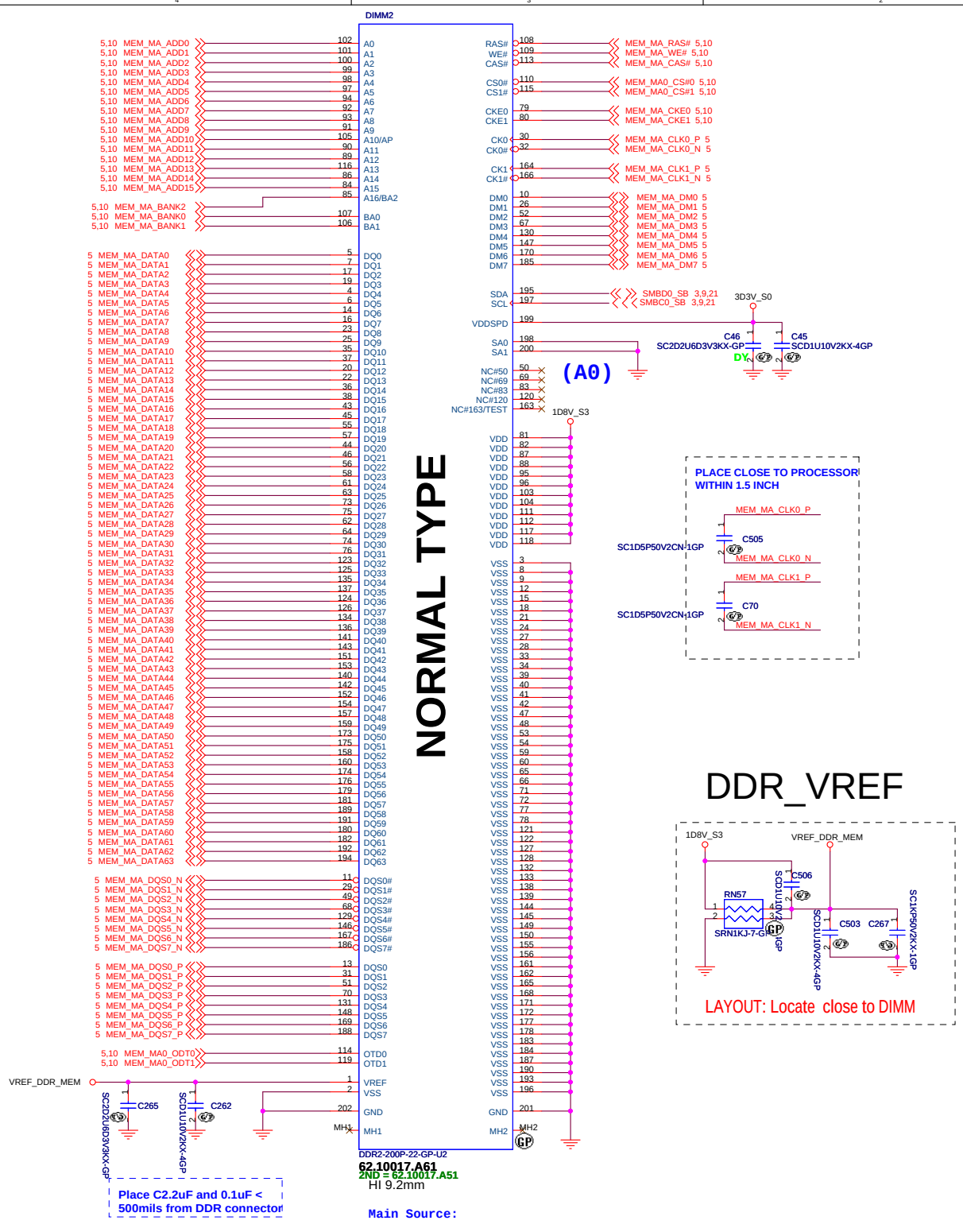
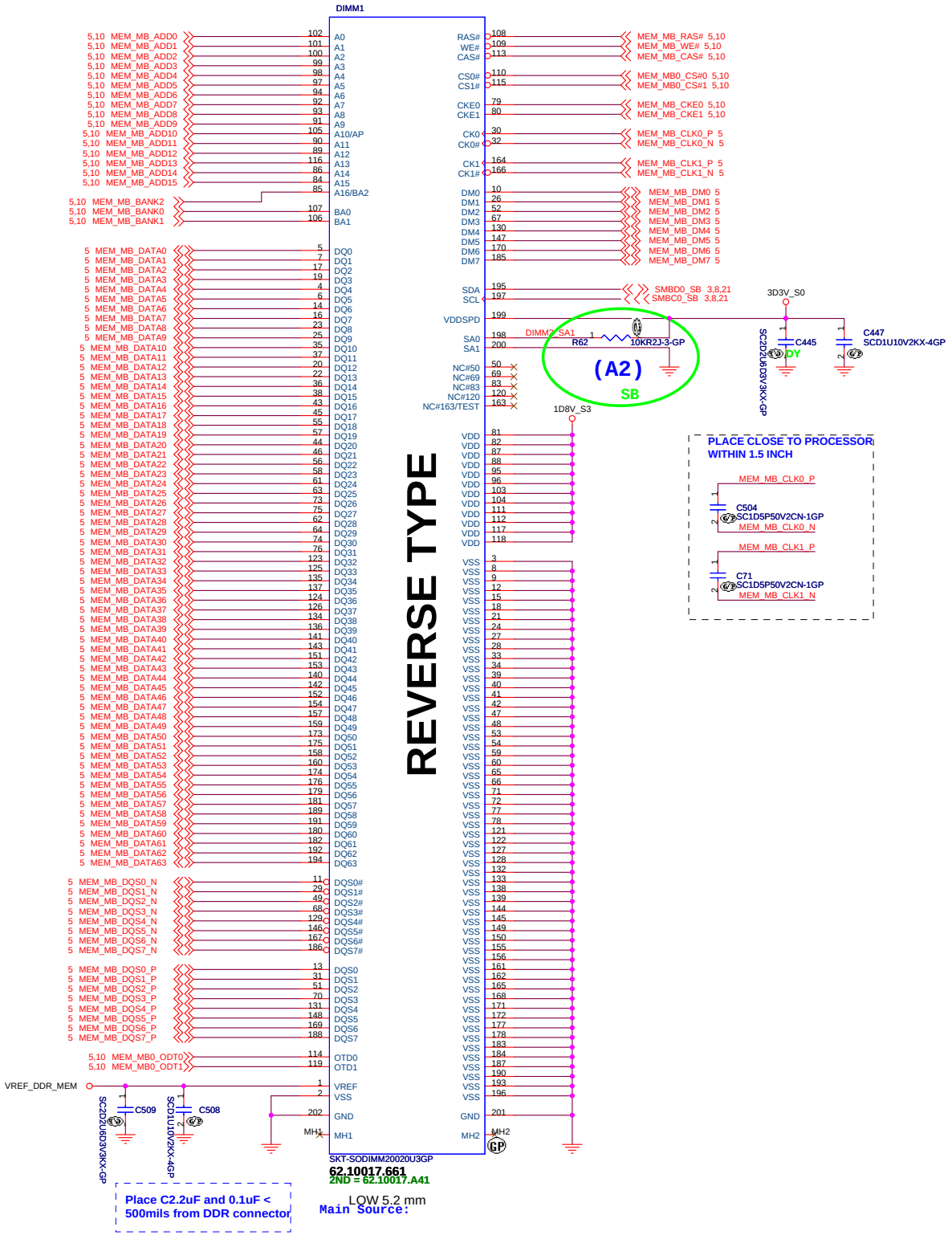
Title	***CPU_Power_(4/4)***	
Size: A3	Document Number: **Olan**	Rev: -1
Date: Friday, April 18, 2008	Sheet 7 of 58	



<Core Design>

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	DDR_SO-DIMM SKT_1
Size: Custom	Document Number: Olan
Rev: -1	
Date: Friday, April 18, 2008	Sheet 8 of 58



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

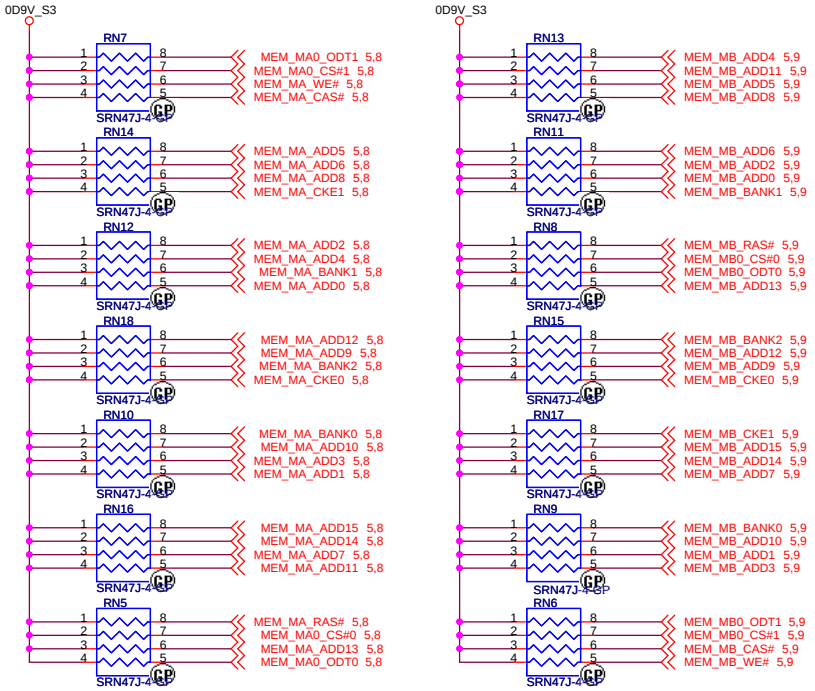
Title: DDR_SO-DIMM SKT_2

Size	Document Number	Rev
Custom	Olan	-1

Date: Friday, April 18, 2008 Sheet 9 of 58

PARALLEL TERMINATION

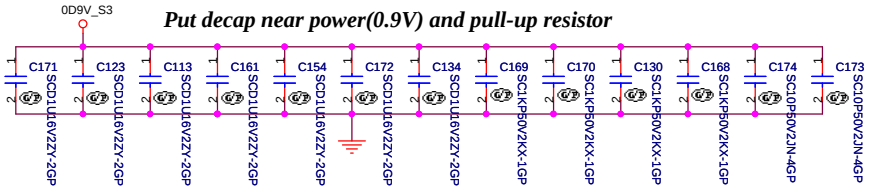
Put decap near power(0.9V) and pull-up resistor



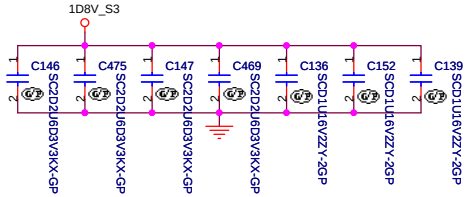
Do not share the Term resistor between the DDR addess and Control Signals.

Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

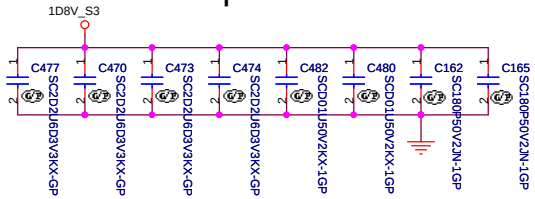


Place these Caps near DM1



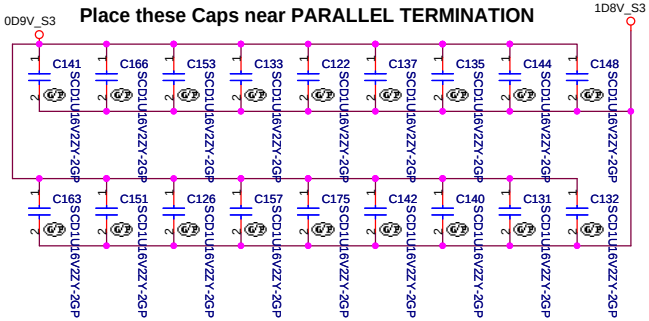
Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near DM2



Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near PARALLEL TERMINATION



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR_DAMPING & TERMINATION***

Size	Document Number	Rev
A3	Olan	-1

Date: Friday, April 18, 2008 Sheet 10 of 58

U43A

PART 1 OF 6

HYPER TRANSPORT CPU I/F

RS780M-GP-U1

Place < 100mils from pin C23 and A24

Place < 100mils from pin B25 and B24

Placement: close RS780

U43B

PART 2 OF 6

PCIE I/F GFX

PCIE I/F GPP

PCIE I/F SB

RS780M-GP-U1

Place < 100mils from pin AC8 and AB8

SB

LAN

MINICARD

NEW CARD

A-LINK

RS780M Display Port Support(muxed on GFX)

DP0	GFX_TX0,TX1,TX2,TX3,AUX0,HPD0
DP1	GFX_TX4,TX5,TX6,TX7,AUX1,HPD1

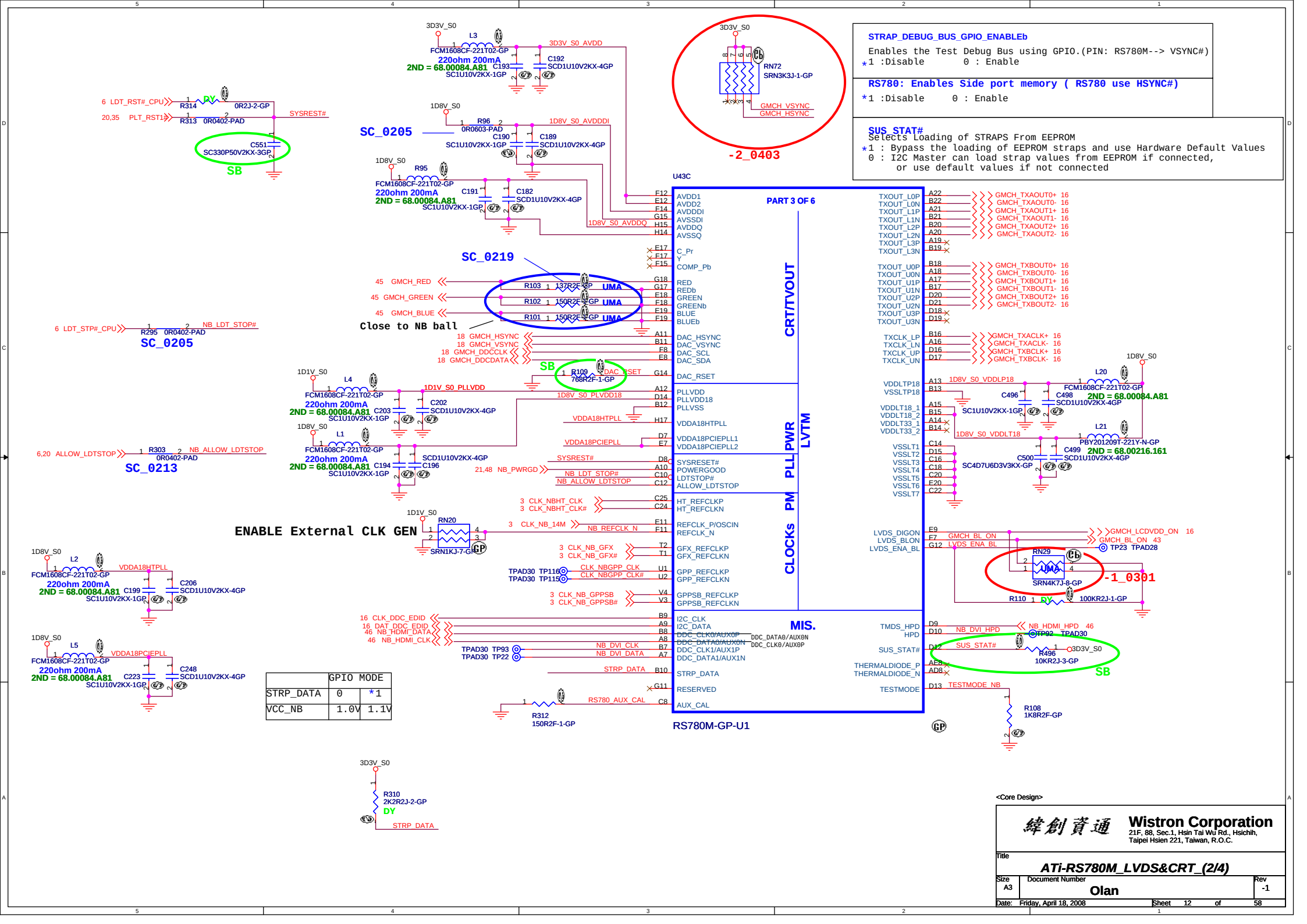
<Core Design>

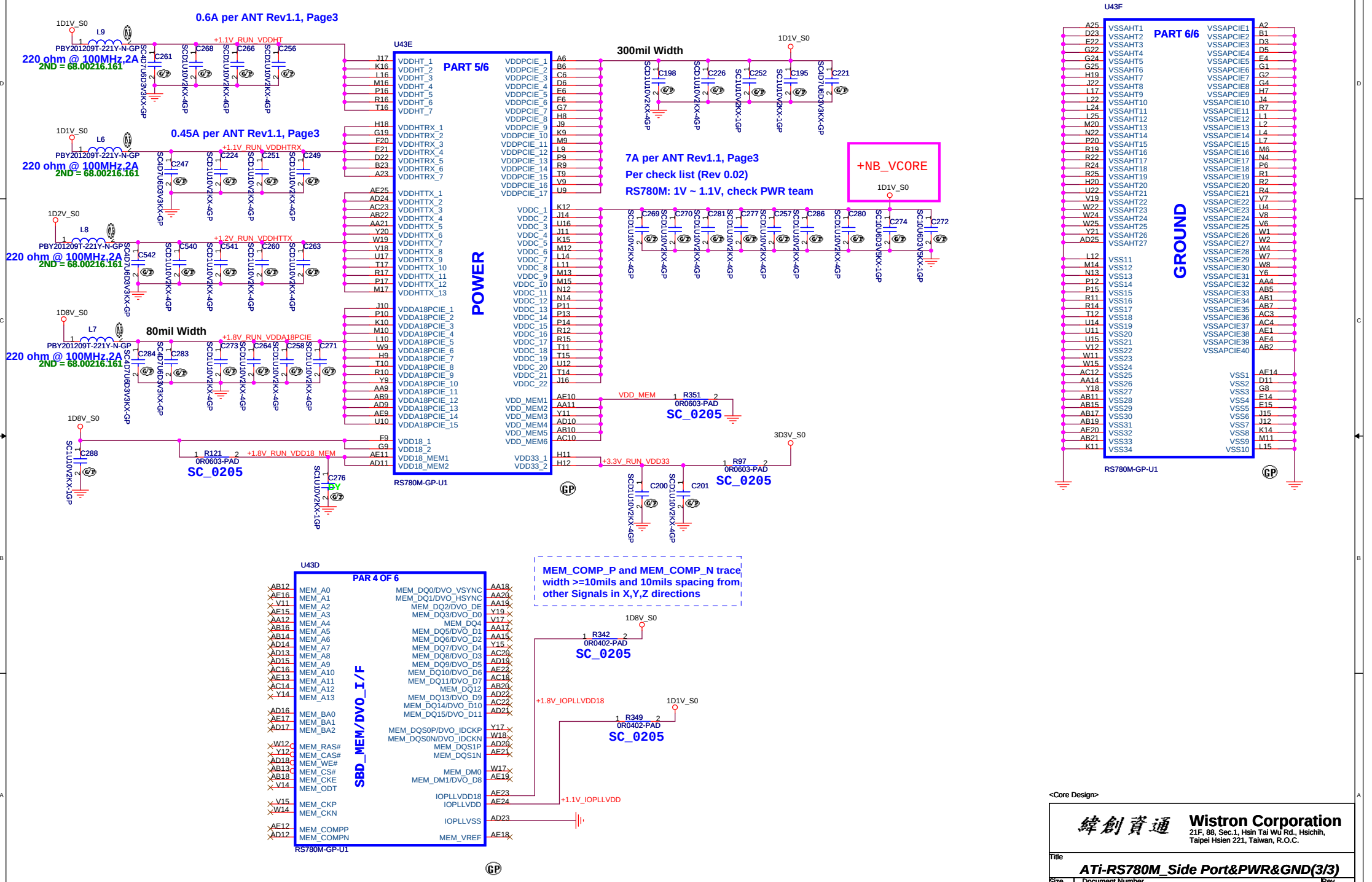
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-RS780M_HT LINK&PCIe(1/3)

Size: A3 | Document Number: Olan | Rev: -1

Date: Friday, April 18, 2008 | Sheet 11 of 58


STRAP_DEBUG_BUS_GPIO_ENABLEb
Enables the Test Debug Bus using GPIO.(PIN: RS780M--> VSYNC#)
*1 :Disable 0 : Enable
RS780: Enables Side port memory (RS780 use HSYNC#)
*1 :Disable 0 : Enable
SUS_STAT#
Selects Loading of STRAPS From EEPROM
*1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected,
or use default values if not connected
SC_0205
SC_0219
SC_0213
-2_0403
-1_0301
Close to NB ball
ENABLE External CLK GEN
SB
UMA
U43C
PART 3 OF 6
CRT/TVOUT
PWR
PLL
LVTM
PM
CLOCKs
MIS.
RS780M-GP-U1
AVDD1
AVDD2
AVDDDI
AVSSDI
AVDDQ
AVSSQ
C_Pr
Y
COMP_Pb
RED
REDb
GREEN
GREENb
BLUE
BLUEb
DAC_HSYNC
DAC_VSYNC
DAC_SCL
DAC_SDA
DAC_RSET
PLLVDD
PLLVDD18
PLLVSS
VDDA18HTPLL
VDDA18PCIEPLL1
VDDA18PCIEPLL2
SYSRESET#
POWERGOOD
LDTSTOP#
ALLOW_LDTSTOP
HT_REFCLKP
HT_REFCLKN
REFCLK_P/OSCIN
REFCLK_N
GFX_REFCLKP
GFX_REFCLKN
GPP_REFCLKP
GPP_REFCLKN
GPPSB_REFCLKP
GPPSB_REFCLKN
I2C_CLK
I2C_DATA
DDC_CLK0/AUX0P
DDC_DATA0/AUX0N
DDC_CLK1/AUX1P
DDC_DATA1/AUX1N
STRP_DATA
RESERVED
AUX_CAL
TXOUT_L0P
TXOUT_L0N
TXOUT_L1P
TXOUT_L1N
TXOUT_L2P
TXOUT_L2N
TXOUT_L3P
TXOUT_L3N
TXOUT_U0P
TXOUT_U0N
TXOUT_U1P
TXOUT_U1N
TXOUT_U2P
TXOUT_U2N
TXOUT_U3P
TXOUT_U3N
TXCLK_LP
TXCLK_LN
TXCLK_UP
TXCLK_UN
VDDLTP18
VSSLTP18
VDDLT18_1
VDDLT18_2
VDDLT33_1
VDDLT33_2
VSSLT1
VSSLT2
VSSLT3
VSSLT4
VSSLT5
VSSLT6
VSSLT7
LVDS_DIGON
LVDS_BLON
LVDS_ENA_BL
TMDS_HPD
HPD
SUS_STAT#
THERMALDIODE_P
THERMALDIODE_N
TESTMODE
3D3V_S0
1D8V_S0
1D1V_S0
1D8V_S0_AVDDQ
1D8V_S0_PLVDD18
1D8V_S0_VDDLP18
1D8V_S0_VDDLT18
1D1V_S0_PLLVDD
VDDA18HTPLL
VDDA18PCIEPLL
3D3V_S0_AVDD
1D8V_S0_AVDDDI
GMCH_VSYNC
GMCH_HSYNC
GMCH_RED
GMCH_GREEN
GMCH_BLUE
GMCH_HSYNC
GMCH_VSYNC
GMCH_DDCCLK
GMCH_DDCDATA
DAC_RSET
SYSRESET#
NB_PWRGD
NB_LDT_STOP#
NB_ALLOW_LDTSTOP
CLK_NBHT_CLK
CLK_NBHT_CLK#
CLK_NB_14M
NB_REFCLK_N
CLK_NB_GFX
CLK_NB_GFX#
CLK_NBGPP_CLK
CLK_NBGPP_CLK#
CLK_NB_GPPSB
CLK_NB_GPPSB#
CLK_DDC_EDID
DAT_DDC_EDID
NB_HDMI_DATA
NB_HDMI_CLK
NB_DVI_CLK
NB_DVI_DATA
STRP_DATA
RS780_AUX_CAL
GMCH_LCDVDD_ON
GMCH_BL_ON
LVDS_ENA_BL
NB_DVI_HPD
SUS_STAT#
TESTMODE_NB
LDT_RST#_CPU
PLT_RST1#
SYSREST#
LDT_STP#_CPU
NB_LDT_STOP#
ALLOW_LDTSTOP
NB_ALLOW_LDTSTOP
R314 0R2J-2-GP DY
R313 0R0402-PAD
C551 SC330P50V2KX-3GP
R295 0R0402-PAD
R303 0R0402-PAD
R96 0R0603-PAD
R95 FCM1608CF-221T02-GP
220ohm 200mA
2ND = 68.00084.A81
L3 FCM1608CF-221T02-GP
C192 SCD1U10V2KX-4GP
C193 SC1U10V2KX-1GP
C190 SC1U10V2KX-1GP
C189 SCD1U10V2KX-4GP
C191 SC1U10V2KX-1GP
C182 SCD1U10V2KX-4GP
R103 137R2F-GP UMA
R102 150R2F-GP UMA
R101 150R2F-GP UMA
R109 768R2F-1-GP
L4 FCM1608CF-221T02-GP
C202 SCD1U10V2KX-4GP
C203 SC1U10V2KX-1GP
L1 FCM1608CF-221T02-GP
C196 SCD1U10V2KX-4GP
C194 SC1U10V2KX-1GP
RN20 SRN1KJ-7-GP
L2 FCM1608CF-221T02-GP
C206 SCD1U10V2KX-4GP
C199 SC1U10V2KX-1GP
L5 FCM1608CF-221T02-GP
C248 SCD1U10V2KX-4GP
C223 SC1U10V2KX-1GP
R312 150R2F-1-GP
R310 2K2R2J-2-GP DY
RN72 SRN3K3J-1-GP
L20 FCM1608CF-221T02-GP
C498 SCD1U10V2KX-4GP
C496 SC1U10V2KX-1GP
L21 PBY201209T-221Y-N-GP
C499 SCD1U10V2KX-4GP
C500 SC4D7U6D3V3KX-GP
RN29 SRN4K7J-8-GP
R110 100KR2J-1-GP
R496 10KR2J-3-GP
R108 1K8R2F-GP
TP23 TPAD28
TP92 TPAD30
TPAD30 TP116
TPAD30 TP115
TPAD30 TP93
TPAD30 TP22
DDC_DATA0/AUX0N
DDC_CLK0/AUX0P
DDC_CLK1/AUX1P
DDC_DATA1/AUX1N
GMCH_TXAOUT0+ 16
GMCH_TXAOUT0- 16
GMCH_TXAOUT1+ 16
GMCH_TXAOUT1- 16
GMCH_TXAOUT2+ 16
GMCH_TXAOUT2- 16
GMCH_TXBOUT0+ 16
GMCH_TXBOUT0- 16
GMCH_TXBOUT1+ 16
GMCH_TXBOUT1- 16
GMCH_TXBOUT2+ 16
GMCH_TXBOUT2- 16
GMCH_TXACLK+ 16
GMCH_TXACLK- 16
GMCH_TXBCLK+ 16
GMCH_TXBCLK- 16
GMCH_LCDVDD_ON 16
GMCH_BL_ON 43
NB_HDMI_HPD 46
STRP_DATA 0 *1
VCC_NB 1.0V 1.1V
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-RS780M_LVDS&CRT_(2/4)
Size A3
Document Number Olan
Rev -1
Date: Friday, April 18, 2008
Sheet 12 of 58



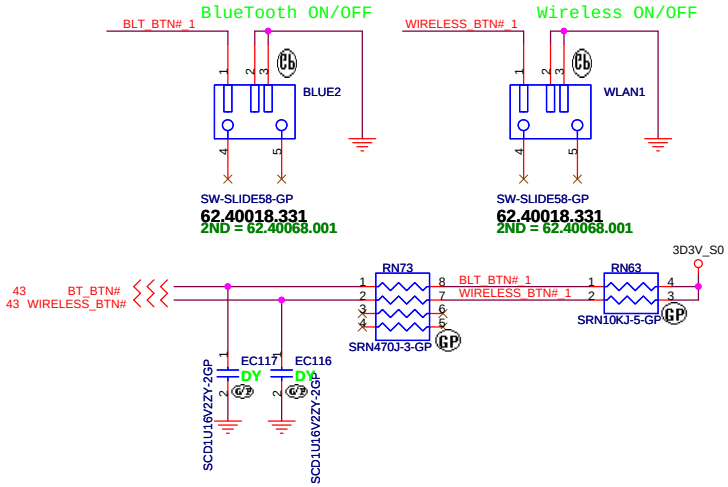
<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: ***ATi-RS780M_Side Port&PWR&GND(3/3)***

Size	Document Number	Rev
A3	Olan	-1

Date: Friday, April 18, 2008 Sheet 13 of 58



<Core Design>

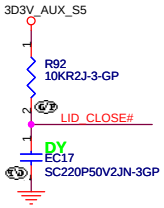
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

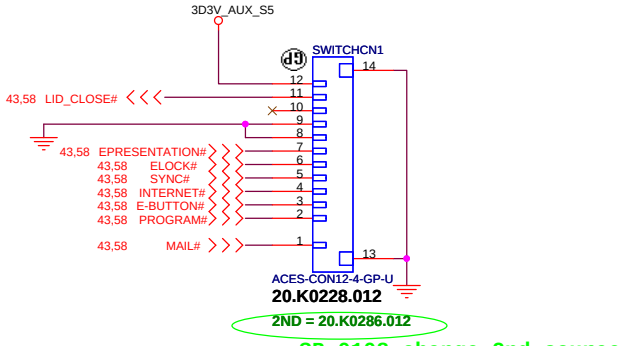
Title: **SWITCH**

Size	Document Number	Rev
A3	Olan	-1

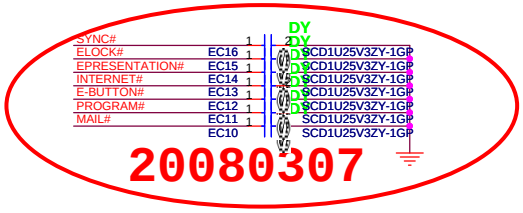
Date: Friday, April 18, 2008 Sheet 14 of 58

LAUNCH





SB_0108_change 2nd source

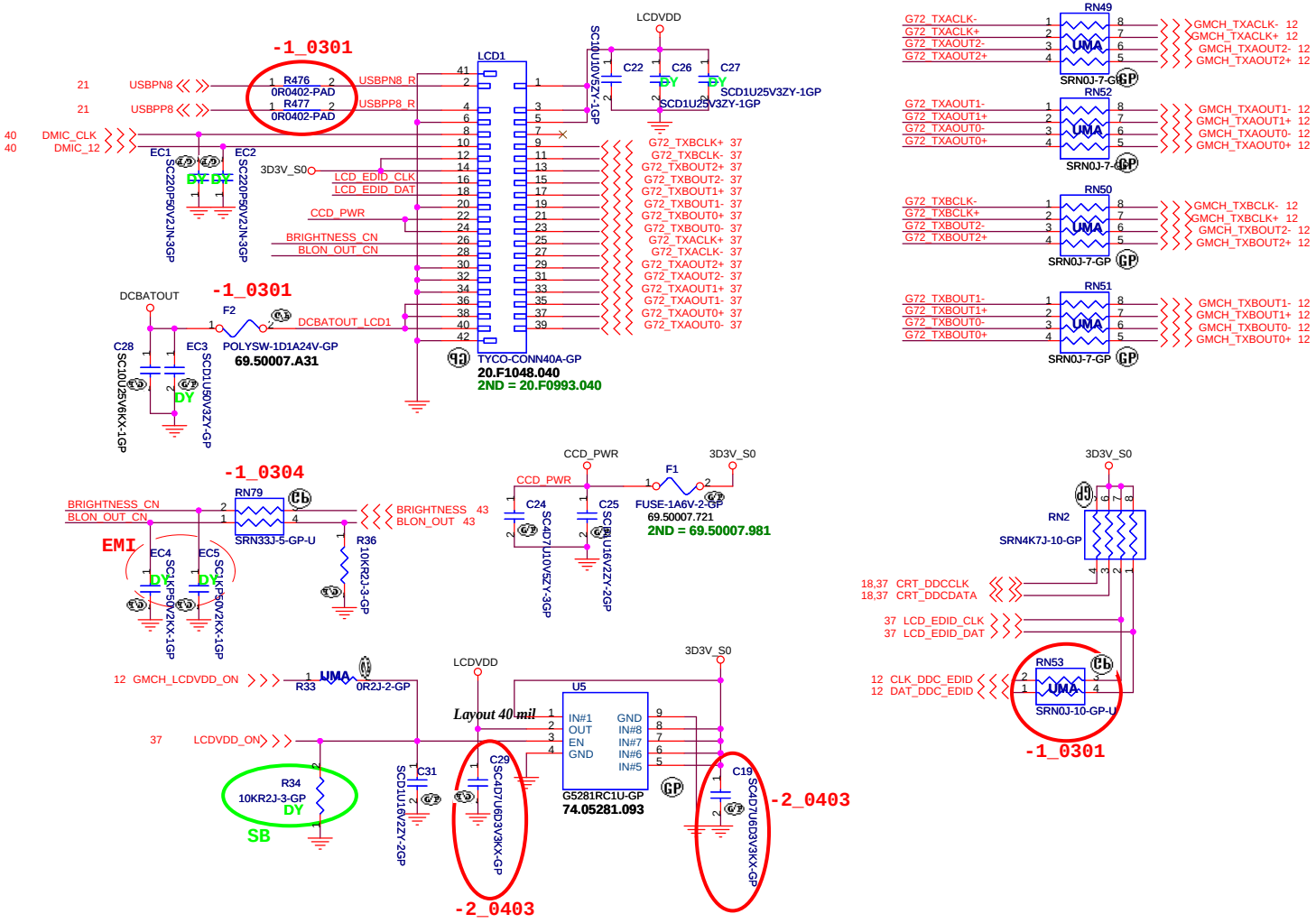


<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

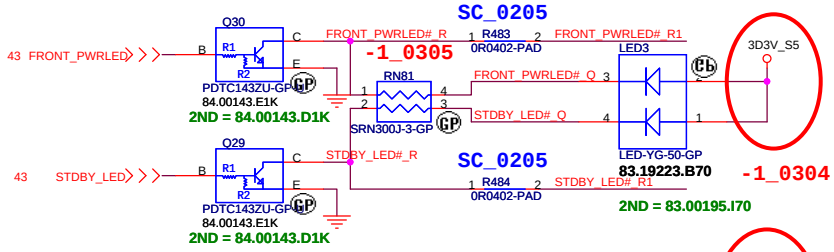
Title			
LAUNCH			
Size: A3	Document Number: Olan		Rev: -1
Date: Friday, April 18, 2008	Sheet 15 of 58		

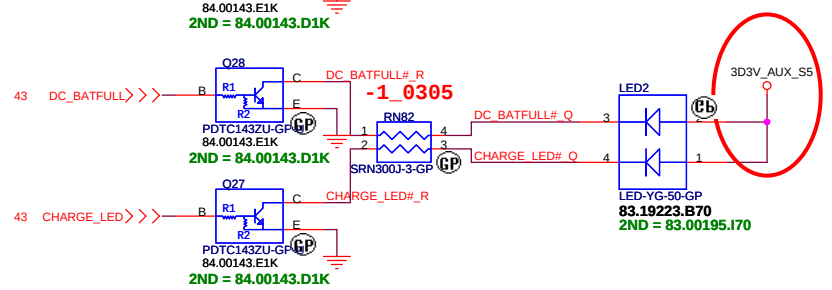
LCD/INVERTER/CCD CONN

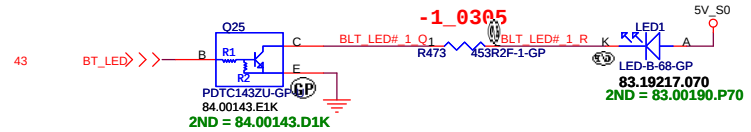


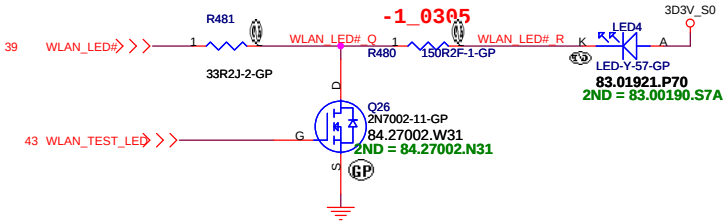
Title	LCD CONN	
Size: A3	Document Number: Olan	Rev: -1
Date: Friday, April 18, 2008	Sheet 16 of 58	

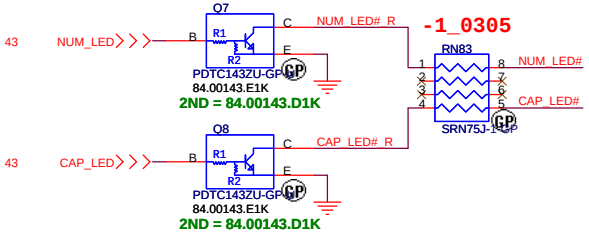
LED

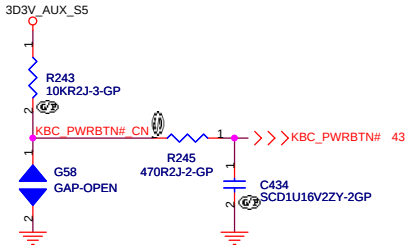


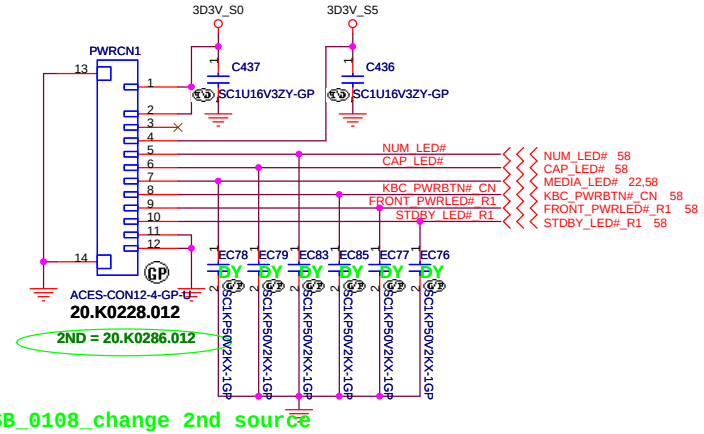






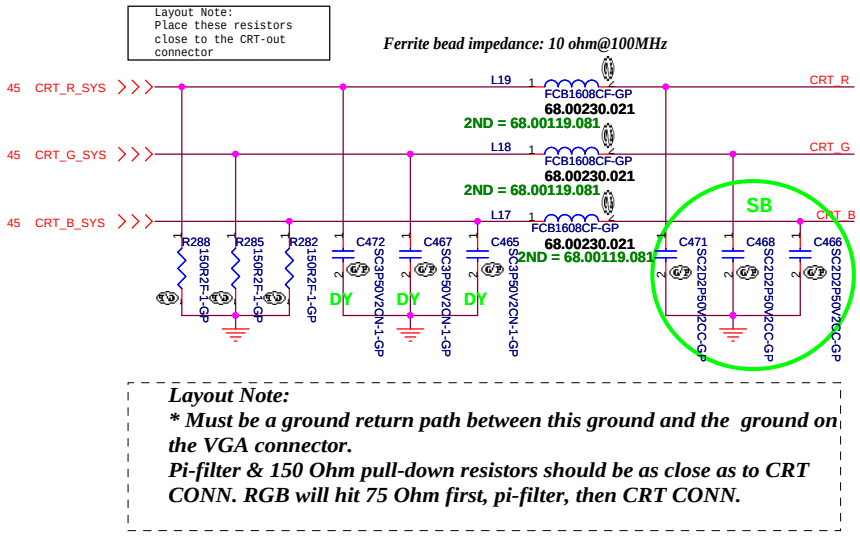




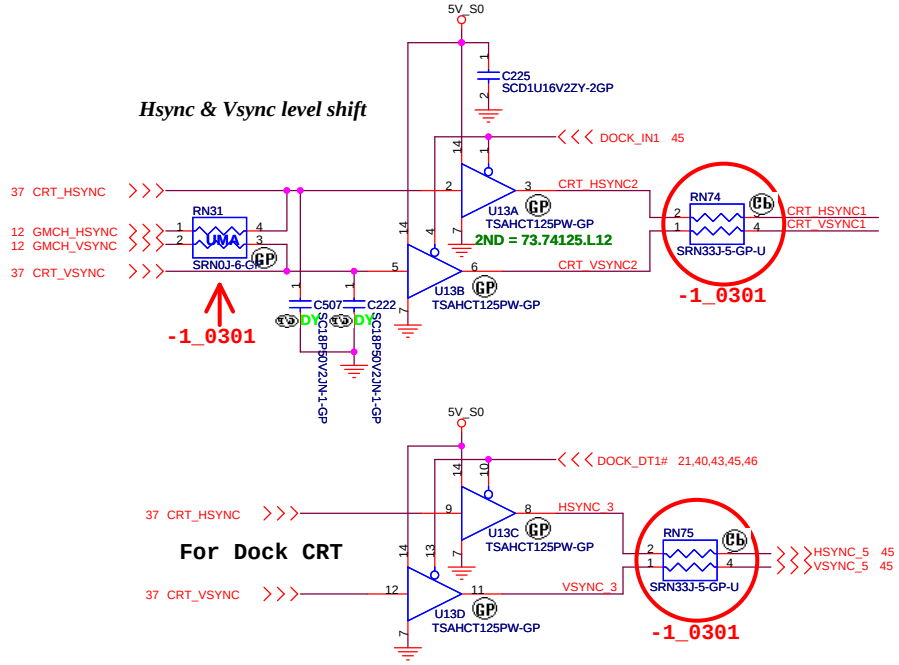


SB_0108_change 2nd source

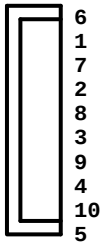
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***LED & LAUNCH***	
Size: A3	Document Number: **Olan**	Rev: -1
Date: Friday, April 18, 2008	Sheet 17 of 58	

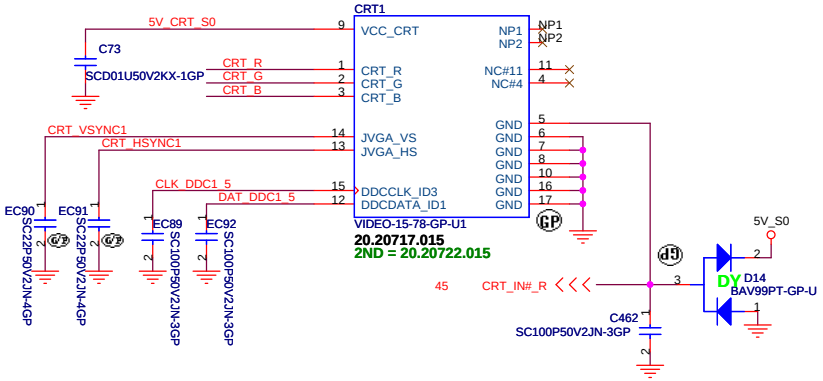


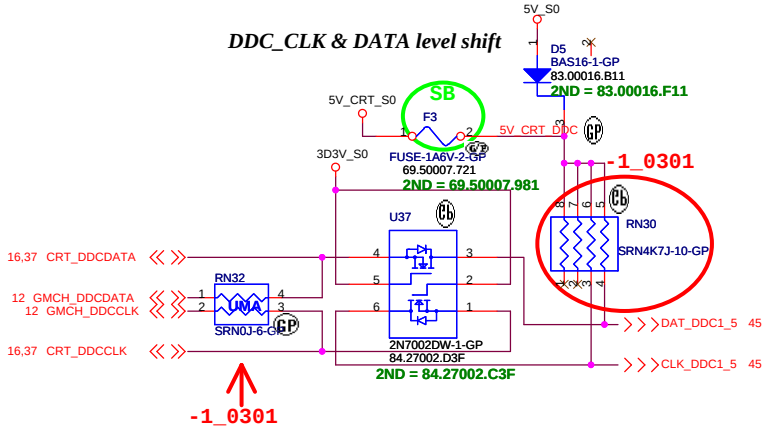
Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



CRT I/F & CONNECTOR







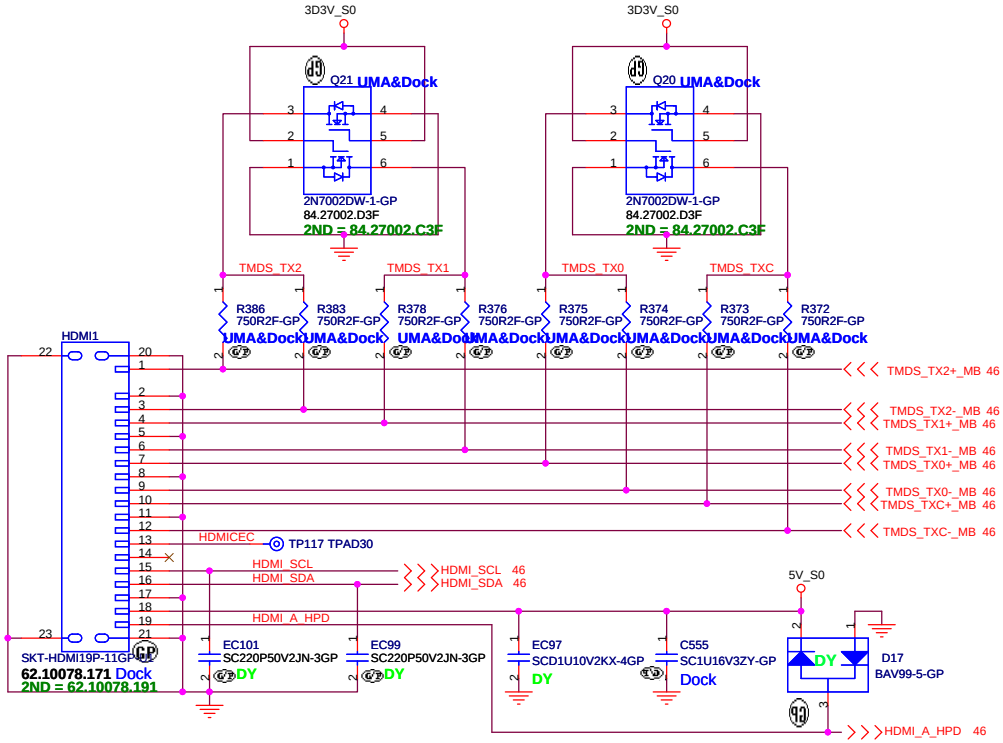
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT Connector**

Size	Document Number	Rev
	Olan	-1

Date: Friday, April 18, 2008 Sheet 18 of 58



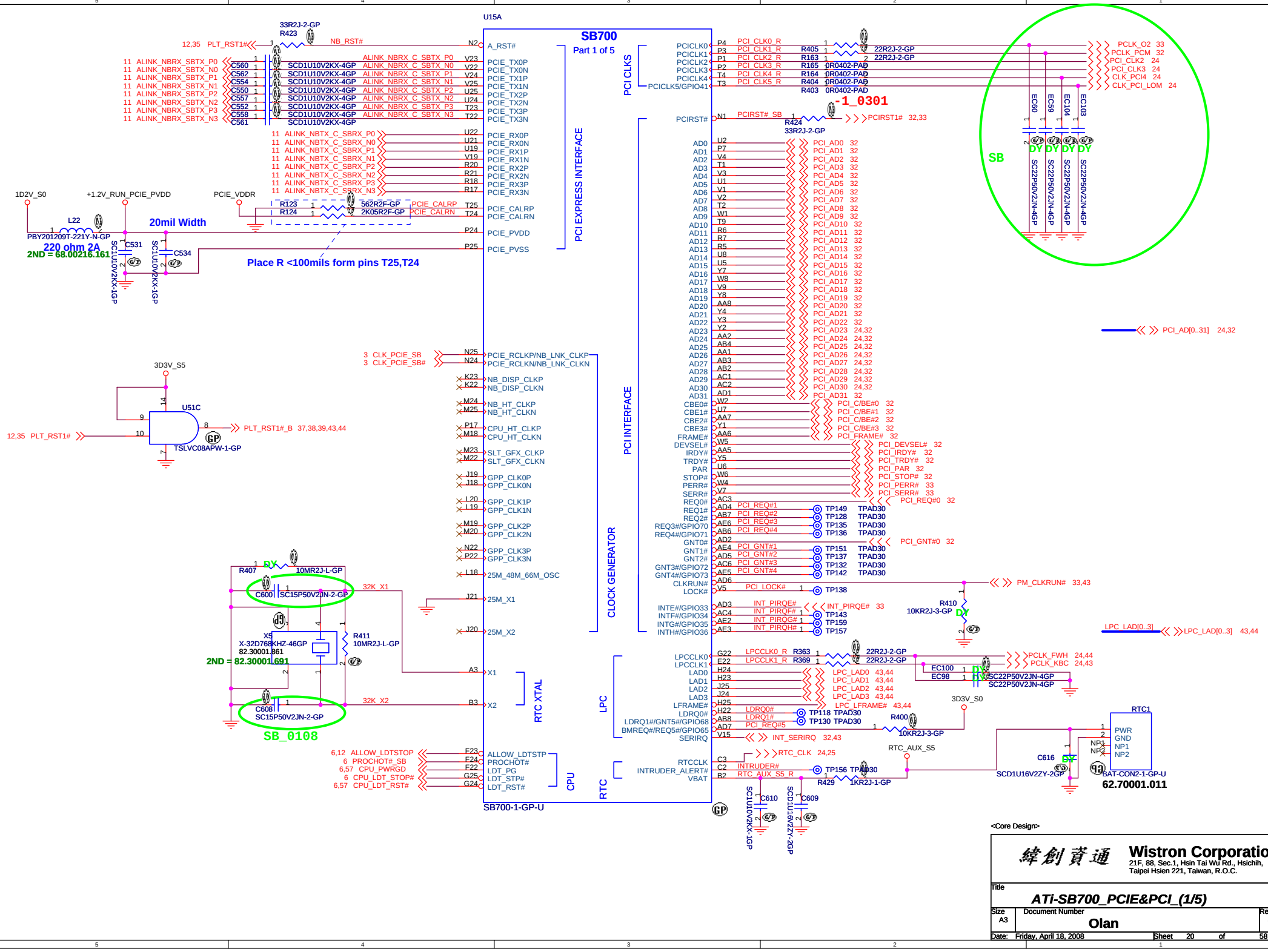
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

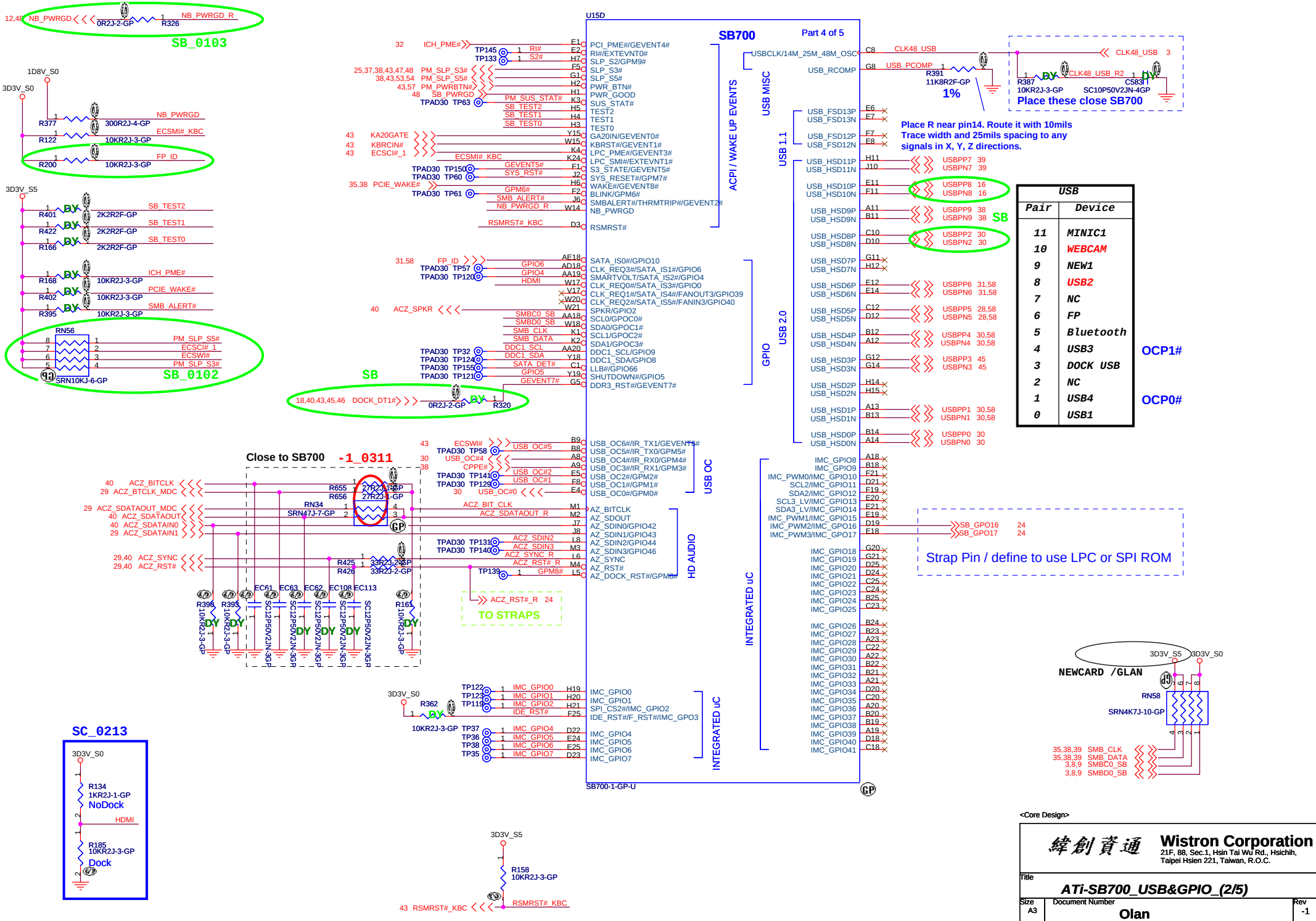
Title: **HDMI CONNECTOR**

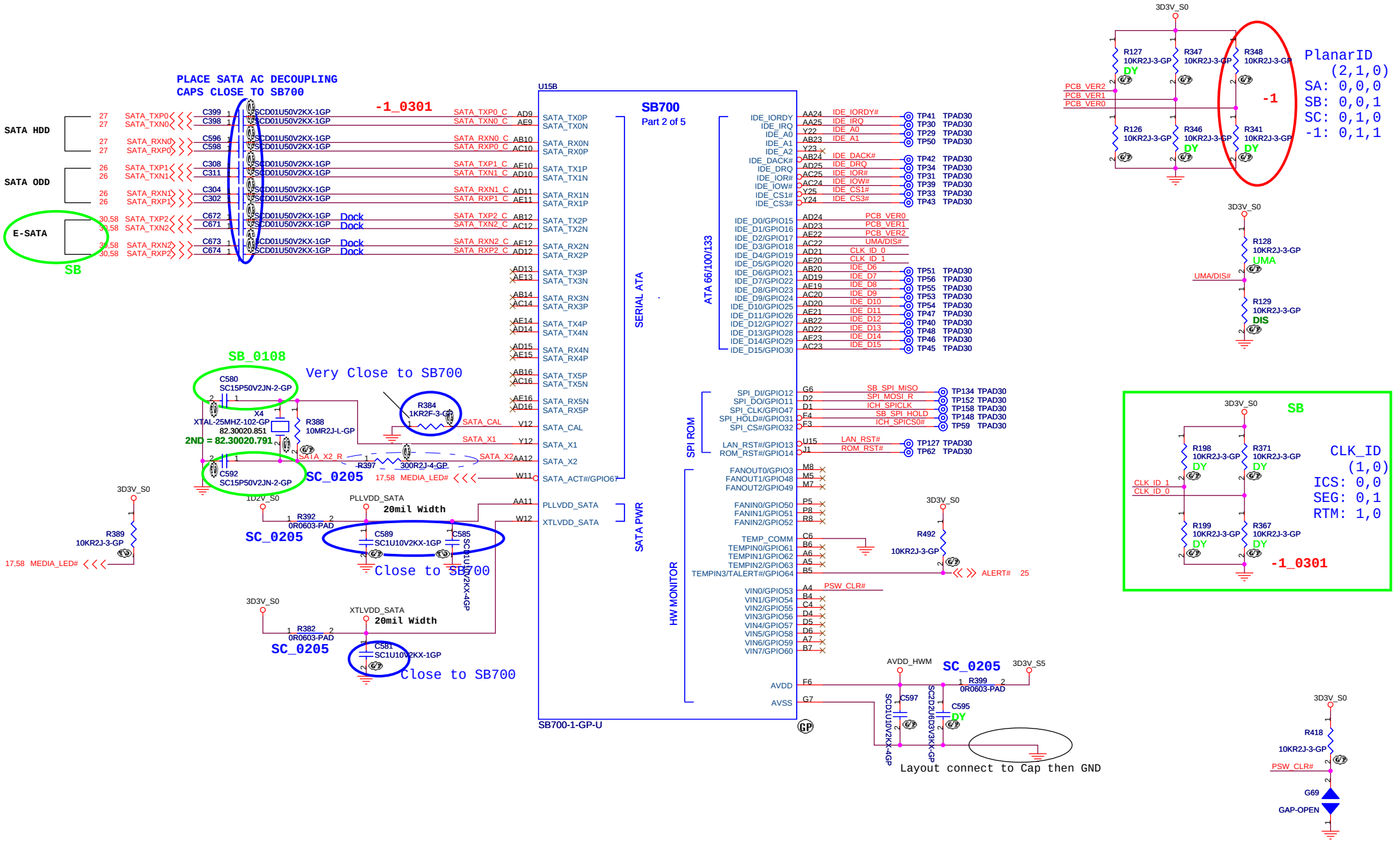
Size	Document Number	Rev
A3	Olan	-1

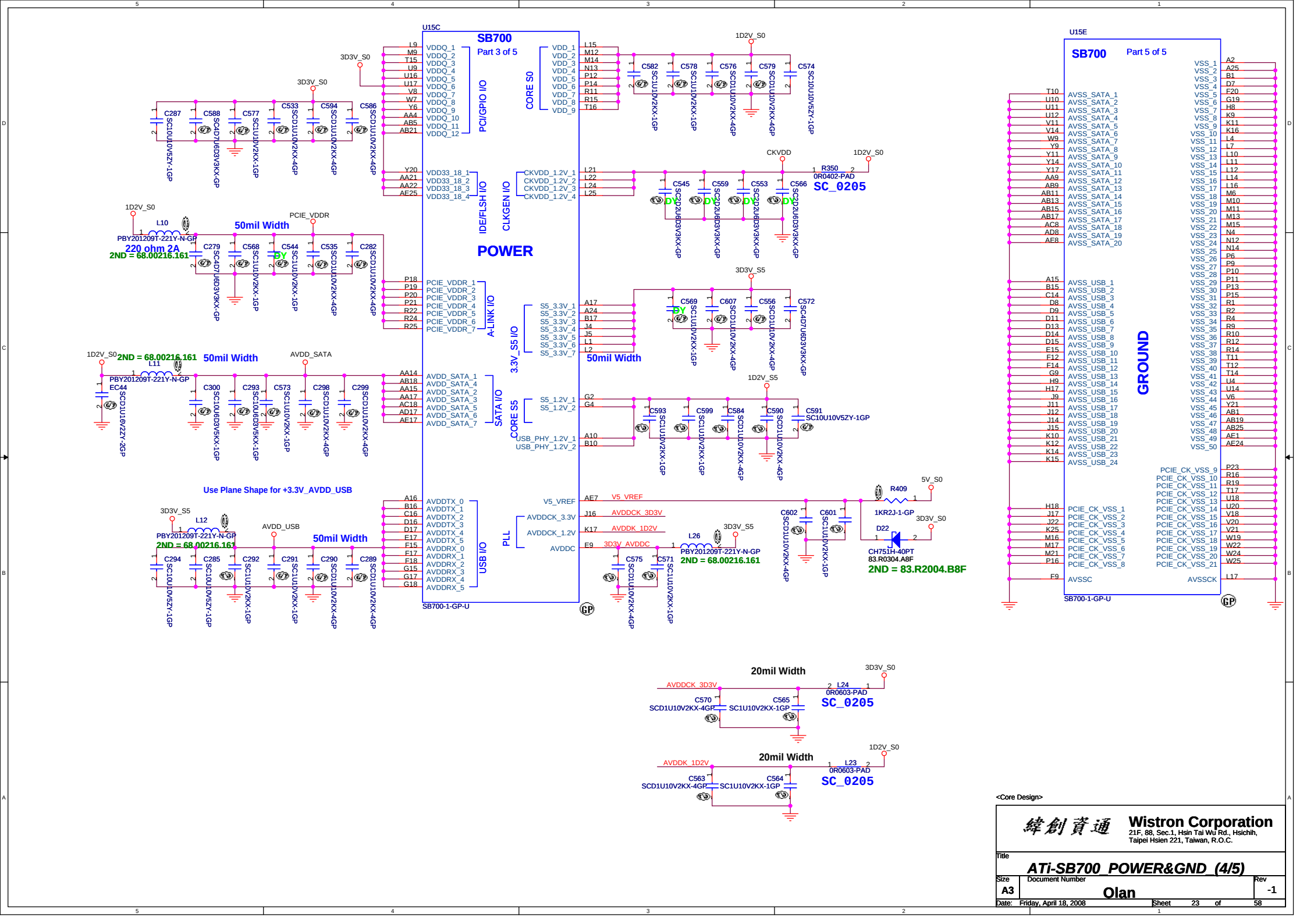
Date: Friday, April 18, 2008 Sheet 19 of 58



緯創資通	Wistron Corporation	
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	ATi-SB700_PCIE&PCI_(1/5)	
Size: A3	Document Number: Olan	Rev: -1
Date: Friday, April 18, 2008	Sheet 20 of 58	

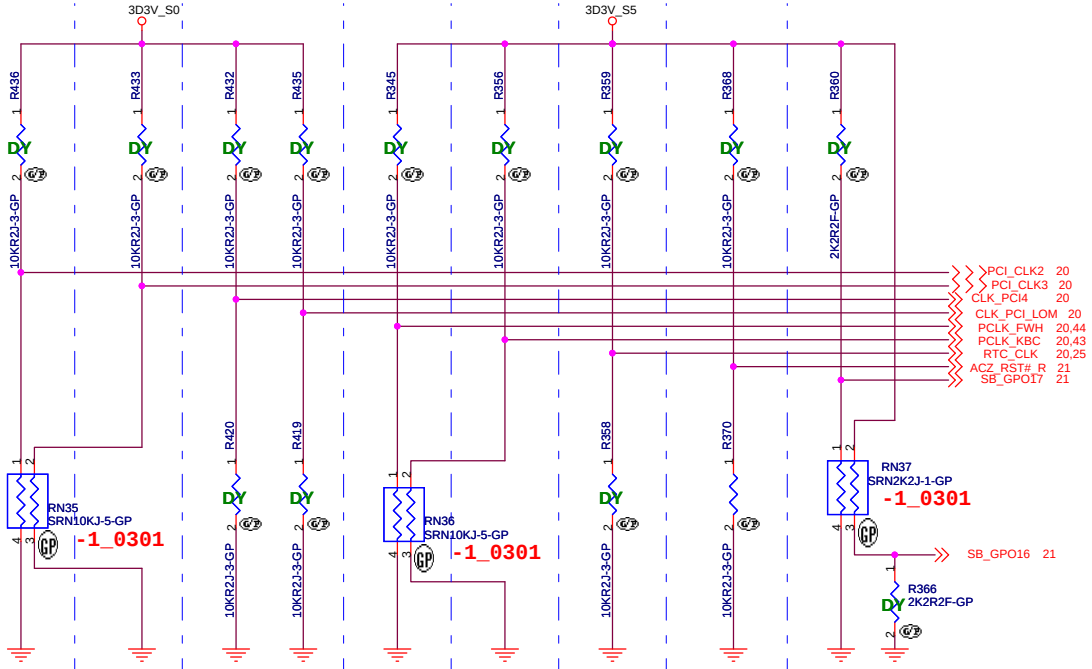

SB_0103
SB_0102
SC_0213
Close to SB700 -1_0311
SB700
Part 4 of 5
U15D
SB700-1-GP-U
ACPI / WAKE UP EVENTS
USB MISC
USB 1.1
USB 2.0
GPIO
USB OC
HD AUDIO
INTEGRATED uC
Place these close SB700
Place R near pin14. Route it with 10mils Trace width and 25mils spacing to any signals in X, Y, Z directions.
Strap Pin / define to use LPC or SPI ROM
TO STRAPS
NEWCARD /GLAN
USB
Pair Device
11 MINIC1
10 WEBCAM
9 NEW1
8 USB2
7 NC
6 FP
5 Bluetooth
4 USB3
3 DOCK USB
2 NC
1 USB4
0 USB1
OCP1#
OCP0#
SB
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ATi-SB700_USB&GPIO_(2/5)
Olan
Friday, April 18, 2008


PLACE SATA AC DECOUPLING
CAPS CLOSE TO SB700
-1_0301
SATA HDD
SATA ODD
E-SATA
SB
U15B
SB700
Part 2 of 5
SERIAL ATA
ATA 66/100/133
SPI ROM
SATA PWR
HW MONITOR
SB700-1-GP-U
SB_0108
Very Close to SB700
SC_0205
Close to SB700
20mil Width
PLLVDD_SATA
XTLVDD_SATA
Layout connect to Cap then GND
PlanarID
(2,1,0)
SA: 0,0,0
SB: 0,0,1
SC: 0,1,0
-1: 0,1,1
CLK_ID
(1,0)
ICS: 0,0
SEG: 0,1
RTM: 1,0
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ATi-SB700_SATA-IDE_(3/5)
Olan
Size A3
Rev -1
Date: Friday, April 18, 2008
Sheet 22 of 58


U15C
SB700
Part 3 of 5
POWER
PCI/GPIO I/O
CORE S0
IDE/FLSH I/O
CLKGEN I/O
A-LINK I/O
3.3V_S5 I/O
SATA I/O
CORE S5
USB I/O
PLL
SB700-1-GP-U
U15E
SB700
Part 5 of 5
GROUND
SB700-1-GP-U
50mil Width
220 ohm 2A
2ND = 68.00216.161
Use Plane Shape for +3.3V_AVDD_USB
20mil Width
SC_0205
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-SB700_POWER&GND_(4/5)
Size
A3
Document Number
Olan
Rev
-1
Date: Friday, April 18, 2008
Sheet 23 of 58

REQUIRED STRAPS

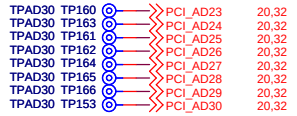
REQUIRED SYSTEM STRAPS



	PCI_CLK2	PCI_CLK3	CLK_PCI_LOM CLK_PCI4	PCLK_FWH	PCLK_KBC	RTCCLK	AZ_RST#	SB_GPO17 , SB_GPO16
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	IMC ENABLED	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT	ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		IMC DISABLED DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT	L, H = LPC ROM L, L = FWH ROM

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

DEBUG STRAPS



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

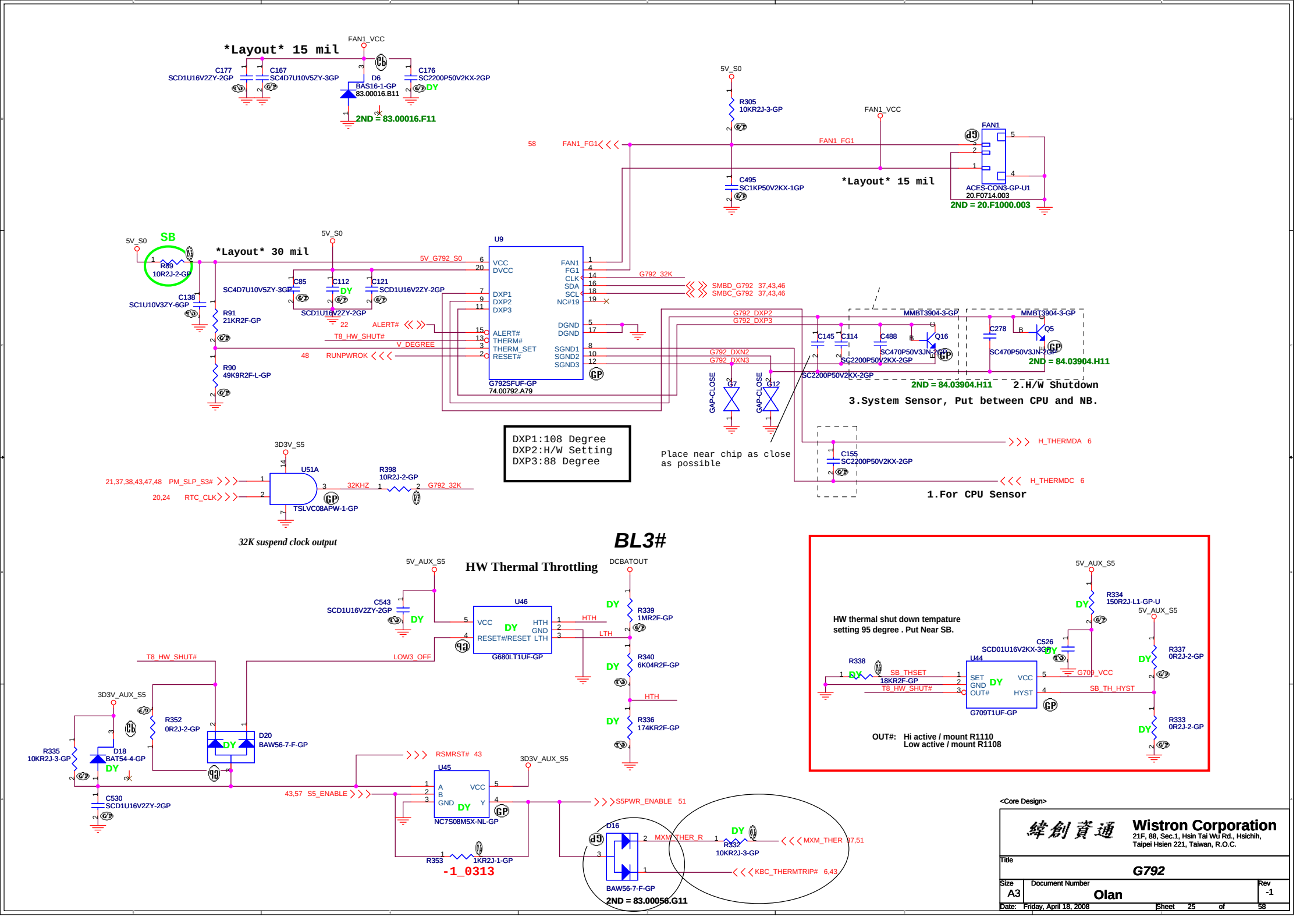
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB700_STRAPPING_(5/5)

Size: A3 | Document Number: Olan | Rev: -1

Date: Friday, April 18, 2008 | Sheet 24 of 58


Layout 15 mil
FAN1_VCC
C177 SCD1U16V2ZY-2GP
C167 SC4D7U10V5ZY-3GP
D6 BAS16-1-GP 83.00016.B11
C176 SC2200P50V2KX-2GP
DY
2ND = 83.00016.F11
5V_S0
R305 10KR2J-3-GP
FAN1_VCC
58 FAN1_FG1
FAN1_FG1
FAN1
C495 SC1KP50V2KX-1GP
Layout 15 mil
ACES-CON3-GP-U1 20.F0714.003
2ND = 20.F1000.003
5V_S0
SB
Layout 30 mil
R89 10R2J-2-GP
C138 SC1U10V3ZY-6GP
R91 21KR2F-GP
R90 49K9R2F-L-GP
C85 SC4D7U10V5ZY-3GP
C112 DY
C121 SCD1U16V2ZY-2GP
SCD1U16V2ZY-2GP
5V_S0
U9
5V_G792_S0
VCC
DVCC
DXP1
DXP2
DXP3
ALERT#
THERM#
THERM_SET
RESET#
FAN1
FG1
CLK
SDA
SCL
NC#19
DGND
DGND
SGND1
SGND2
SGND3
G792_32K
SMBD_G792 37,43,46
SMBC_G792 37,43,46
G792SFUF-GP 74.00792.A79
22 ALERT#
T8_HW_SHUT#
V_DEGREE
48 RUNPWROK
G792_DXP2
G792_DXP3
G792_DXN2
G792_DXN3
MMBT3904-3-GP
MMBT3904-3-GP
C145
C114
C488
Q16
C278
Q5
SC470P50V3JN-2GP
SC470P50V3JN-2GP
SC2200P50V2KX-2GP
SC2200P50V2KX-2GP
2ND = 84.03904.H11
2ND = 84.03904.H11
2.H/W Shutdown
3.System Sensor, Put between CPU and NB.
GAP-CLOSE
G7
GAP-CLOSE
G12
DXP1:108 Degree
DXP2:H/W Setting
DXP3:88 Degree
Place near chip as close as possible
C155 SC2200P50V2KX-2GP
H_THERMDA 6
H_THERMDC 6
1.For CPU Sensor
3D3V_S5
U51A
21,37,38,43,47,48 PM_SLP_S3#
20,24 RTC_CLK
32KHZ
R398 10R2J-2-GP
G792_32K
TSLVC08APW-1-GP
32K suspend clock output
BL3#
HW Thermal Throttling
5V_AUX_S5
DCBATOUT
C543 SCD1U16V2ZY-2GP
U46
VCC
RESET#/RESET
HTH
GND
LTH
G680LT1UF-GP
R339 1MR2F-GP
R340 6K04R2F-GP
R336 174KR2F-GP
T8_HW_SHUT#
LOW3_OFF
3D3V_AUX_S5
R352 0R2J-2-GP
R335 10KR2J-3-GP
D18 BAT54-4-GP
D20 BAW56-7-F-GP
C530 SCD1U16V2ZY-2GP
RSMRST# 43
43,57 S5_ENABLE
U45
A
B
GND
VCC
Y
NC7S08M5X-NL-GP
R353 1KR2J-1-GP
-1_0313
S5PWR_ENABLE 51
D16
BAW56-7-F-GP
MXM_THER_R
R332 10KR2J-3-GP
MXM_THER 37,51
KBC_THERMTRIP# 6,43
2ND = 83.00056.G11
HW thermal shut down tempature setting 95 degree . Put Near SB.
R334 150R2J-L1-GP-U
R337 0R2J-2-GP
R333 0R2J-2-GP
C526 SCD01U16V2KX-3GP
G709_VCC
U44
SET
GND
OUT#
VCC
HYST
G709T1UF-GP
R338
SB_THSET
18KR2F-GP
T8_HW_SHUT#
SB_TH_HYST
OUT#: Hi active / mount R1110
Low active / mount R1108
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
G792
Size A3
Document Number Olan
Rev -1
Date: Friday, April 18, 2008
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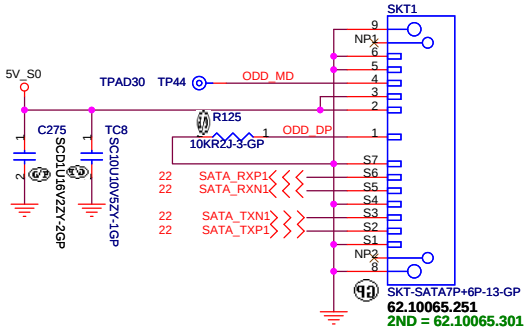
ODD Connector



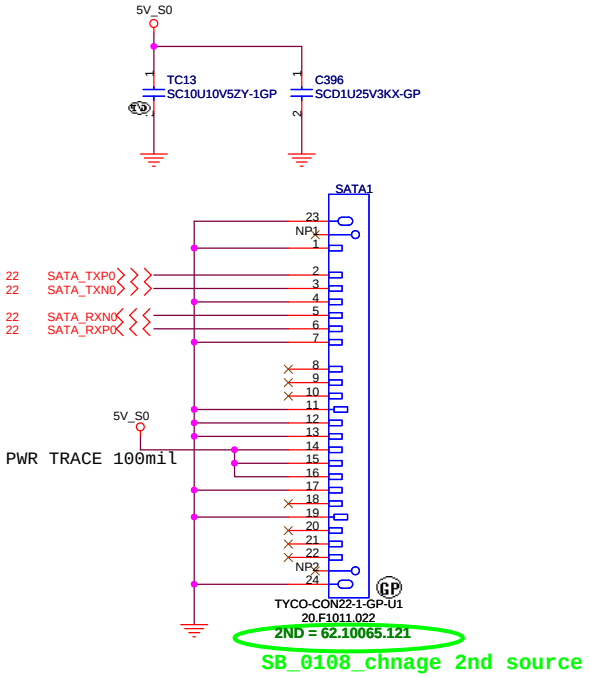
-1_0305

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CDROM	
Size	Document Number: Olan	Rev: -1
Date: Friday, April 18, 2008	Sheet 26 of 58	

SATA HDD Connector



<Core Design>

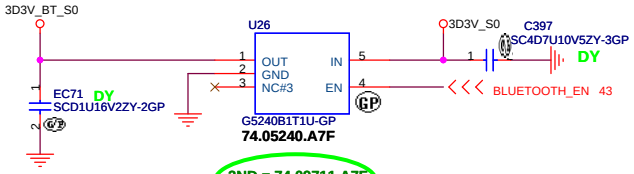
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD

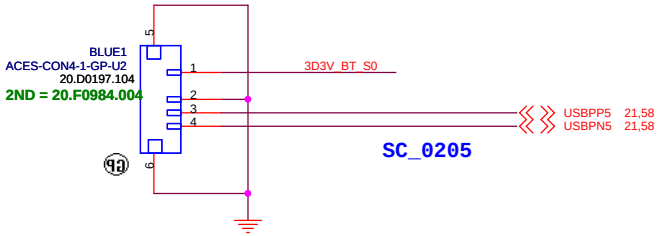
Size | Document Number: Olan | Rev: -1

Date: Friday, April 18, 2008 | Sheet 27 of 58

BLUETOOTH MODULE



EC40 put near BLUE1 / all USB put one choke near connector by EMI request

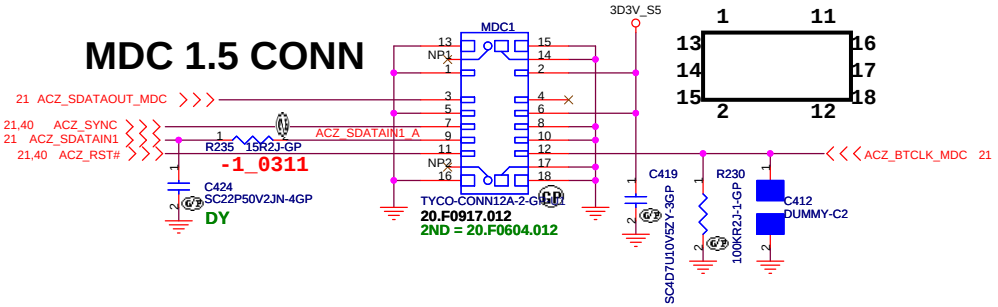


<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***BLUETOOTH***	
Size	Document Number: **Olan**	Rev: -1
Date: Friday, April 18, 2008	Sheet 28 of 58	

MDC 1.5 CONN



<Core Design>

緯創資通 **Wistron Corporation**
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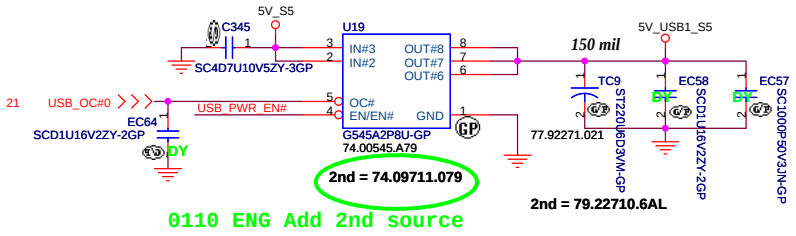
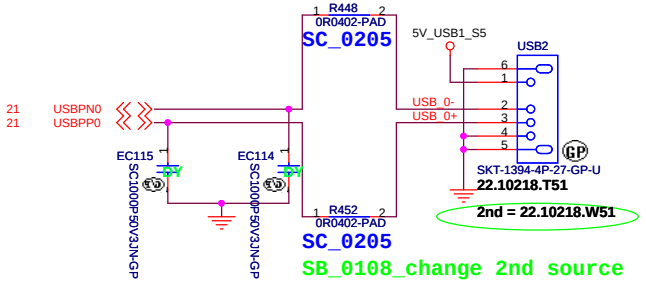
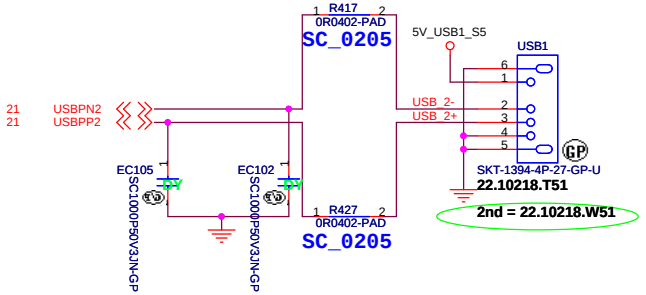
Taipei Hsien 221, Taiwan, R.O.C.

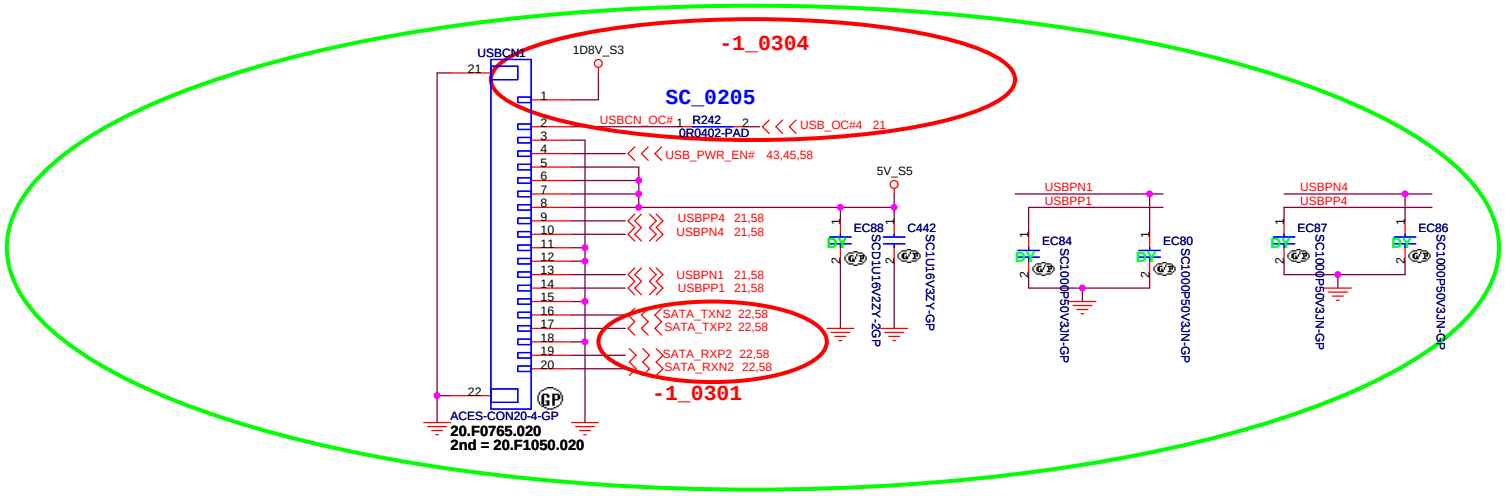
Title	***MDC***	
Size	Document Number **Olan**	Rev -1
Date: Friday, April 18, 2008	Sheet 29 of 58	







SB_0102



58 USBCN_OC# USBCN_OC#

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB

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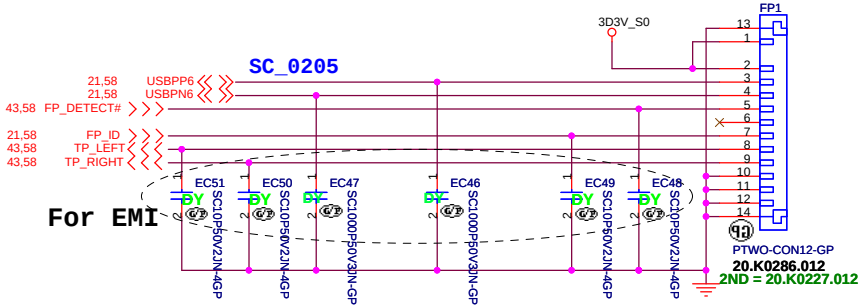
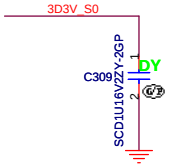
Finger printer

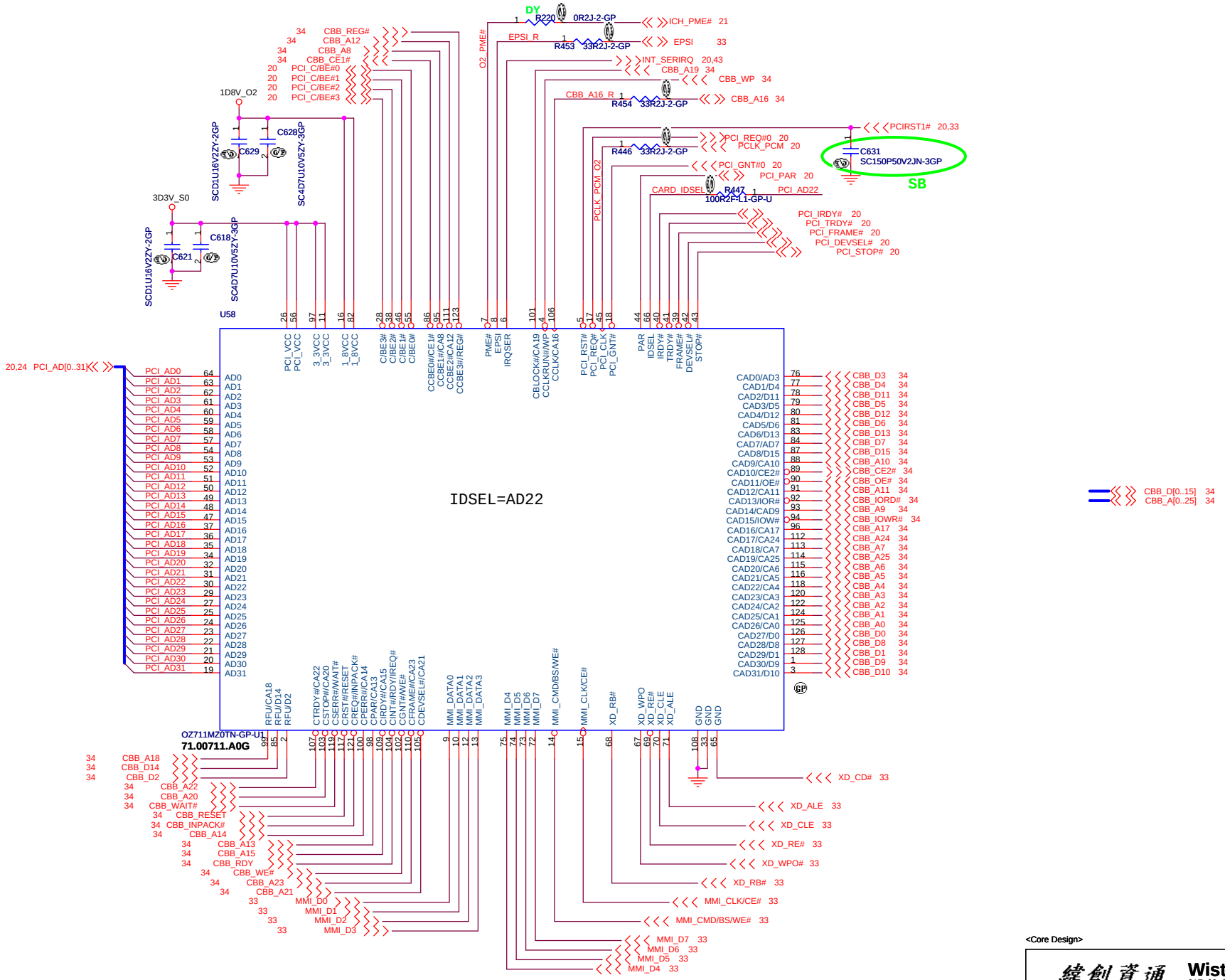




For EMI

<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Finger Printer*		
Size	Document Number: Olan	Rev: -1
Date: Friday, April 18, 2008	Sheet 31 of 58	



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*OZ711MZ0*	
Size: A3	Document Number: Olan	Rev: -1
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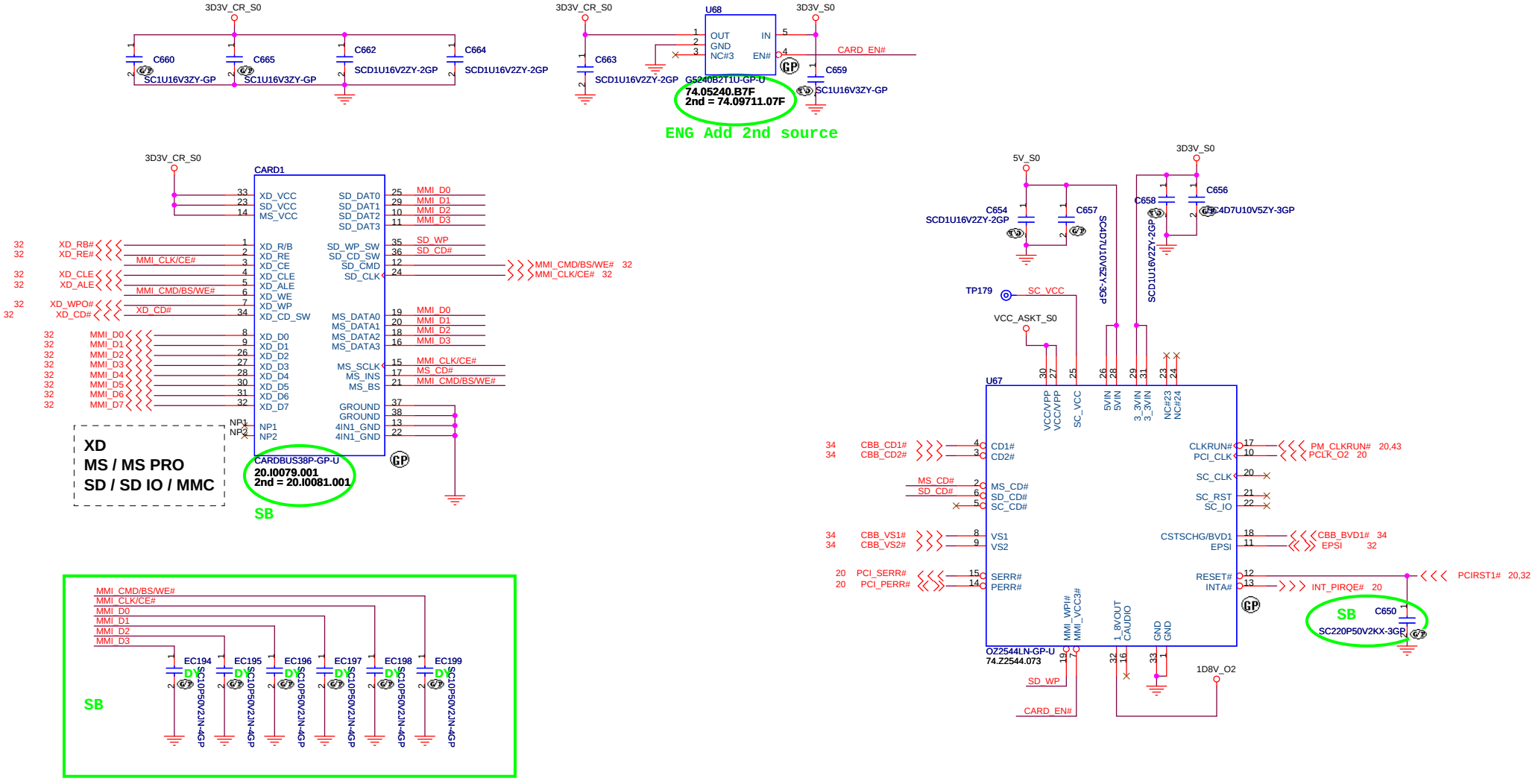


<Core Design>

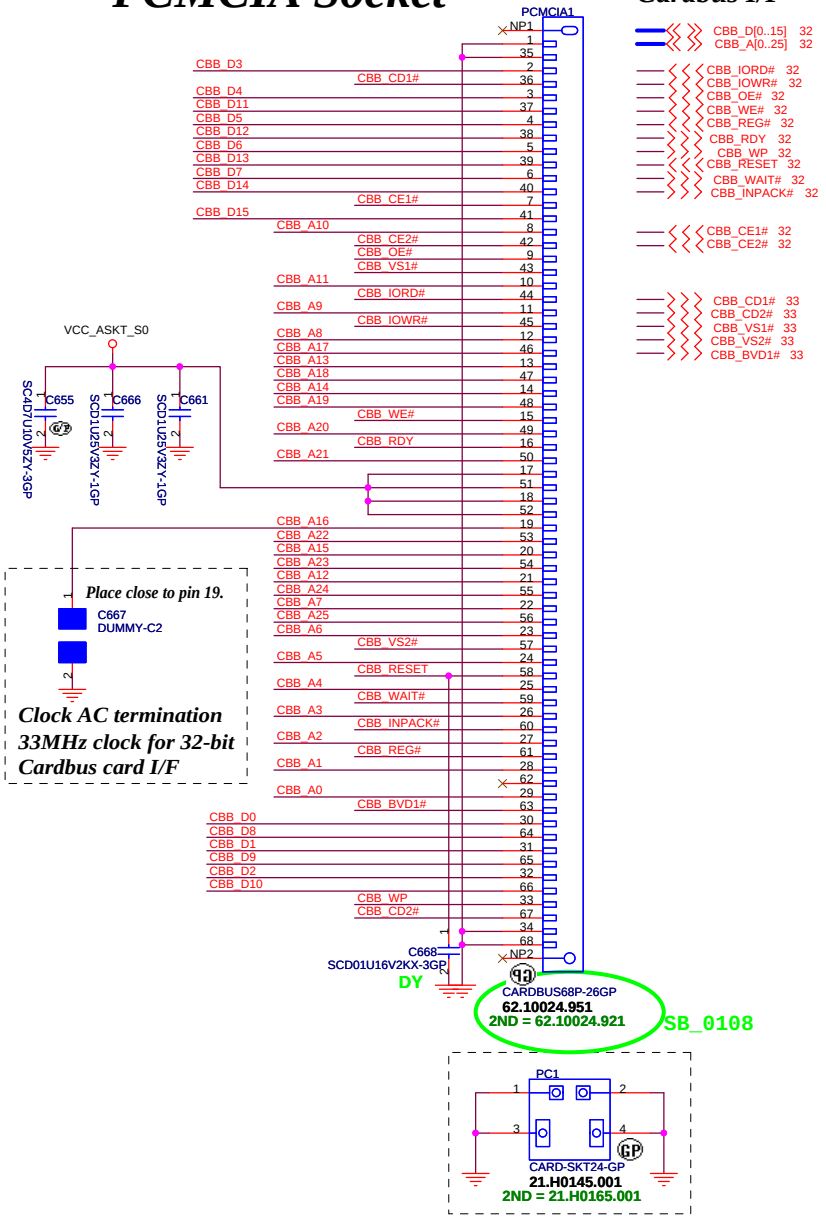
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Card Reader Connector*

Size	Document Number	Rev
A3	Olan	-1

Date: Friday, April 18, 2008 Sheet 33 of 58

PCMCIA Socket



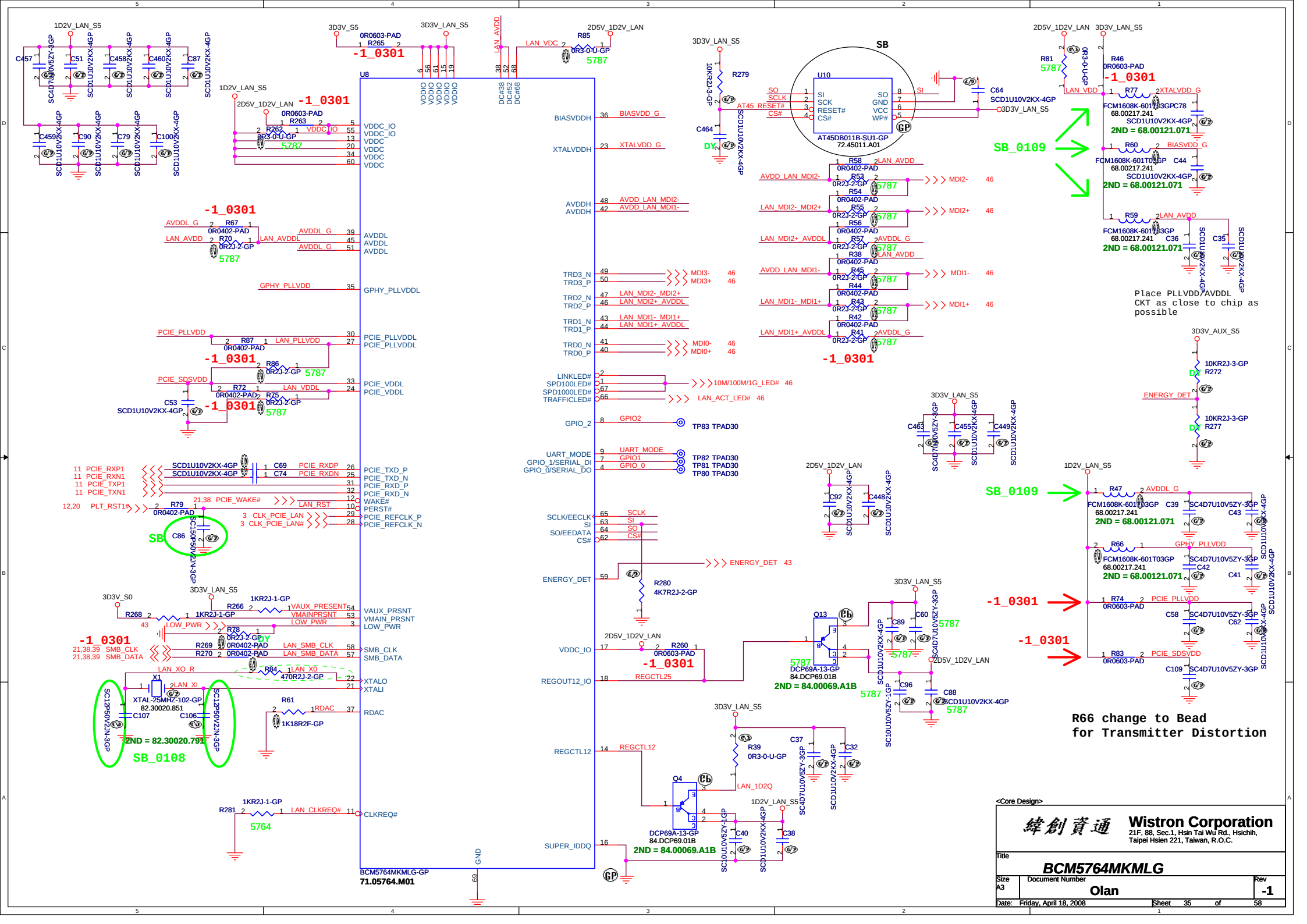
Cardbus I/F

CBB_D[0..15] 32
CBB_A[0..25] 32
CBB_IORD# 32
CBB_IOWR# 32
CBB_OE# 32
CBB_WE# 32
CBB_REG# 32
CBB_RDY 32
CBB_WP 32
CBB_RESET 32
CBB_WAIT# 32
CBB_INPACK# 32
CBB_CE1# 32
CBB_CE2# 32
CBB_CD1# 33
CBB_CD2# 33
CBB_VS1# 33
CBB_VS2# 33
CBB_BVD1# 33

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *PCMCIA*		
Size: A3	Document Number: Olan	Rev: -1
Date: Friday, April 18, 2008	Sheet 34 of 58	


U8
BCM5764MKMLG-GP
71.05764.M01
SB
SB_0109
SB_0108
-1_0301
Place PLLVDD/AVDDL CKT as close to chip as possible
R66 change to Bead for Transmitter Distortion
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
BCM5764MKMLG
Size A3
Document Number
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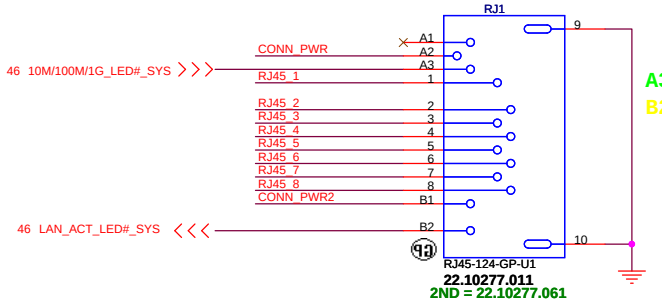
Sheet 35 of 58

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

LAN Connector

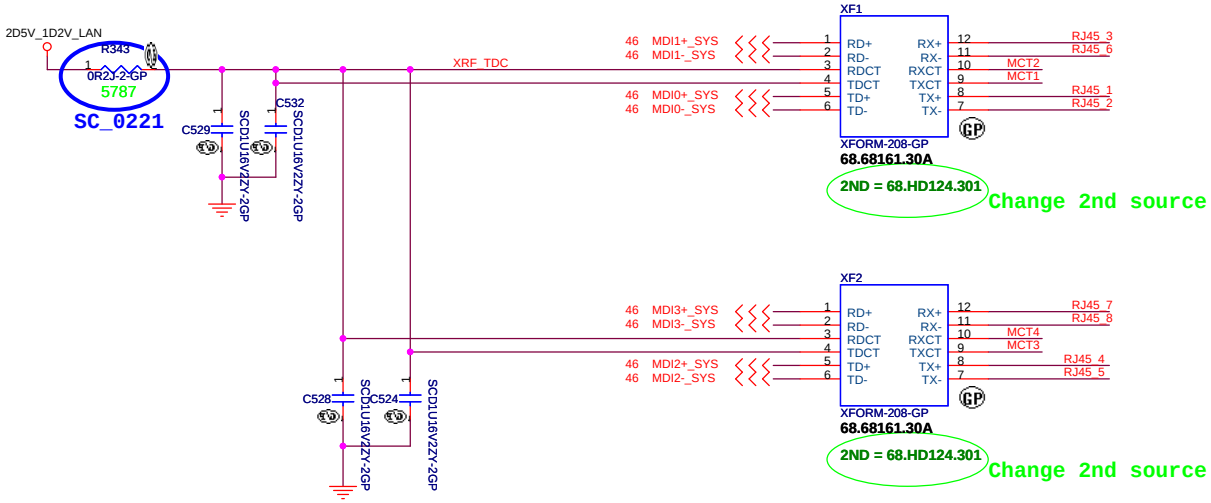


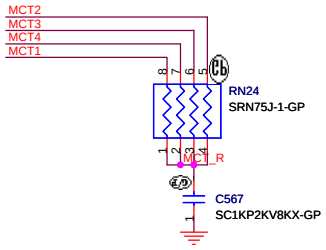
A3:GREEN
B2:Orange

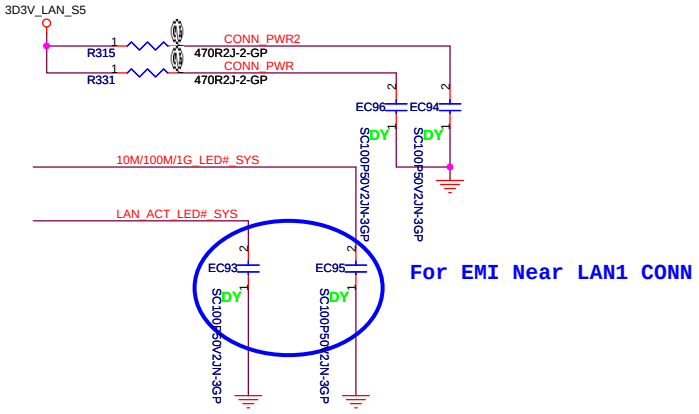
LAN Link: Green(A3), behavior is the same for 10/100/1000 bits

LAN Data: Yellow(B2), when LAN is transfering data.

GIGA Lan Transformer







For EMI Near LAN1 CONN

<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN CONN
Size: A3 | Document Number: Olan | Rev: -1
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NV SMBus
A(pin143&145) : VGA(CRT) / DOCK
B(pin218&220) : DVI
C(pin208&210) : HDMI / TPI / LVDS

Put near graphic connector

11 PEG_TXP[15..0]
11 PEG_TXN[15..0]
11 PEG_RXP[15..0]
11 PEG_RXN[15..0]

5V_S0
48,50,52 VCORE_EN
R457 0R2J-2-GP DY
21,25,38,43,47,48 PM_SLP_S3#
R456 0R0402-PAD
1D8V_S0_MXM
-1_0301
? CHECK ATI NEED?
C492 C493 SCD1U25V3KX-GP DY
C494 SCD1U25V3KX-GP DY
TPAD30 TP85

DIS
20.F1031.230
MXM1
SPD-CONN230A-4-GP-U1

DCBATOUT_MXM
C515 C514 C513 SC4D7U25V6KX-1GP DY
C511 C512 SCD1U25V3KX-GP DY

16 G72_TXBOUT0+
16 G72_TXBOUT0-
16 G72_TXBOUT1+
16 G72_TXBOUT1-
16 G72_TXBOUT2+
16 G72_TXBOUT2-
TPAD30 TP91
MXM_SPDIF
16 G72_TXBCLK+
16 G72_TXBCLK-
45 CRT_BLUE
45 CRT_GREEN
45 CRT_RED
TPAD30 TP90
MXM_ACZ_RST#

G72_TXACLK- 16
G72_TXACLK+ 16
G72_TXAOUT2- 16
G72_TXAOUT2+ 16
G72_TXAOUT1- 16
G72_TXAOUT1+ 16
G72_TXAOUT0- 16
G72_TXAOUT0+ 16
LCD_EDID_DAT 16
LCD_EDID_CLK 16
LCDVDD_ON 16
BLON_IN 43
NV_DVI_DAT 46
NV_DVI_CLK 46
2D5V_S0
R307 0R3-0-U-GP DY
3D3V_S0
C491 SC100U10V5ZY-1GP DIS
C497 SCD1U25V3KX-GP DY

TMDS_A_TX0+ 46
TMDS_A_TX0- 46
TMDS_A_TX1+ 46
TMDS_A_TX1- 46
TMDS_A_TX2+ 46
TMDS_A_TX2- 46
TMDS_A_TXC+ 46
TMDS_A_TXC- 46
MXM_DVI_HPD 46

3 CLK_PCIE_PEG#
3 CLK_PCIE_PEG
TP101 TPAD30

SB_remove TP

SC_0205
20,38,39,43,44 PLT_RST1#_5
R324 0R0402-PAD
C510 SC330P50V2KX-3GP DIS
SB
PLT_RST1#_MXM
TPAD30 TP102
TPAD30 TP99
MXM_ACZ_SYNC
MXM_ACZ_BITCLK
25,43,46 SMBD_G792
25,43,46 SMBC_G792
SC_0205

AC/DC_DET
R618 10KR2J-3-GP DY
3D3V_S0
SB

25,51 MXM_THER
18 CRT_HSYNC
18 CRT_VSYNC
16,18 CRT_DDCCLK
16,18 CRT_DDCDATA
TPAD30 TP97
TPAD30 TP98
MXM_ACZ_SDIN2
MXM_ACZ_SDATAOUT

TPAD30 TP111
TPAD30 TP109
NV_HDMI_DAT
NV_HDMI_CLK

TPAD30 TP94
TPAD30 TP95
TMDS_GPIO6_SW
MXM_171

DCBATOUT
DCBATOUT_MXM
G24 G22 G23 G25 G105 G106
GAP-CLOSE-PWR-3-GP

<Core Design>

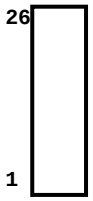
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

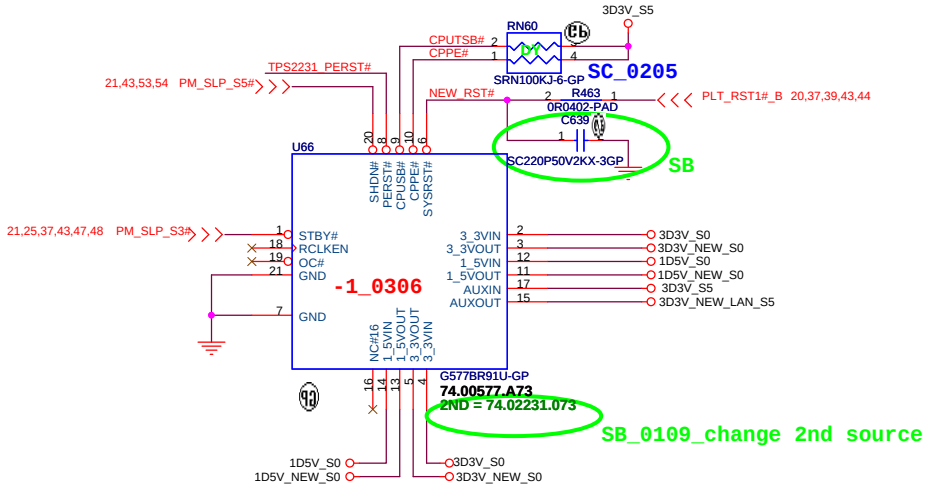
Title: Graphic MXM CONN
Size: A3
Document Number: Olan
Rev: -1
Date: Friday, April 18, 2008
Sheet 37 of 58

NEWCARD Connector

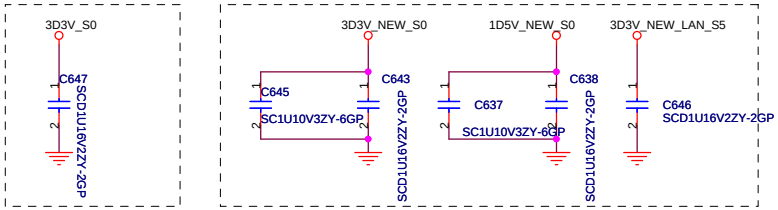
Reserve the symbol
for bottom side
connector

TOP VIEW





Place them Near to ChipPlace them Near to Connector



<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **NEW CARD**

Size	Document Number	Rev
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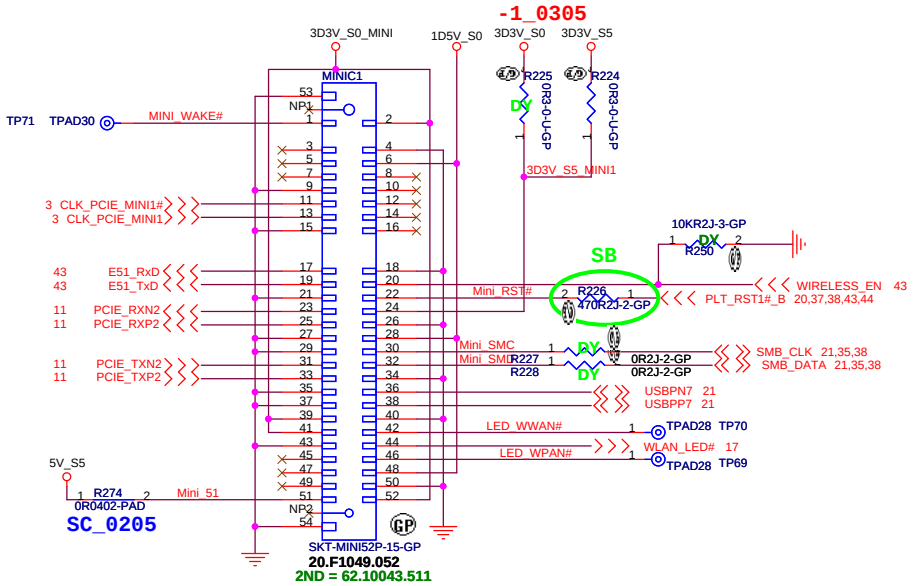
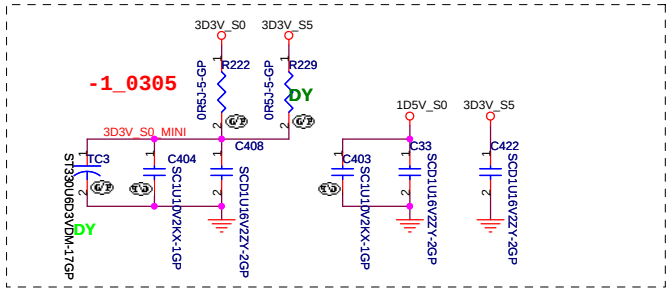
Mini Card Connector(WLAN)



Place near MINIC1



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Mini Card

Size	Document Number	Rev
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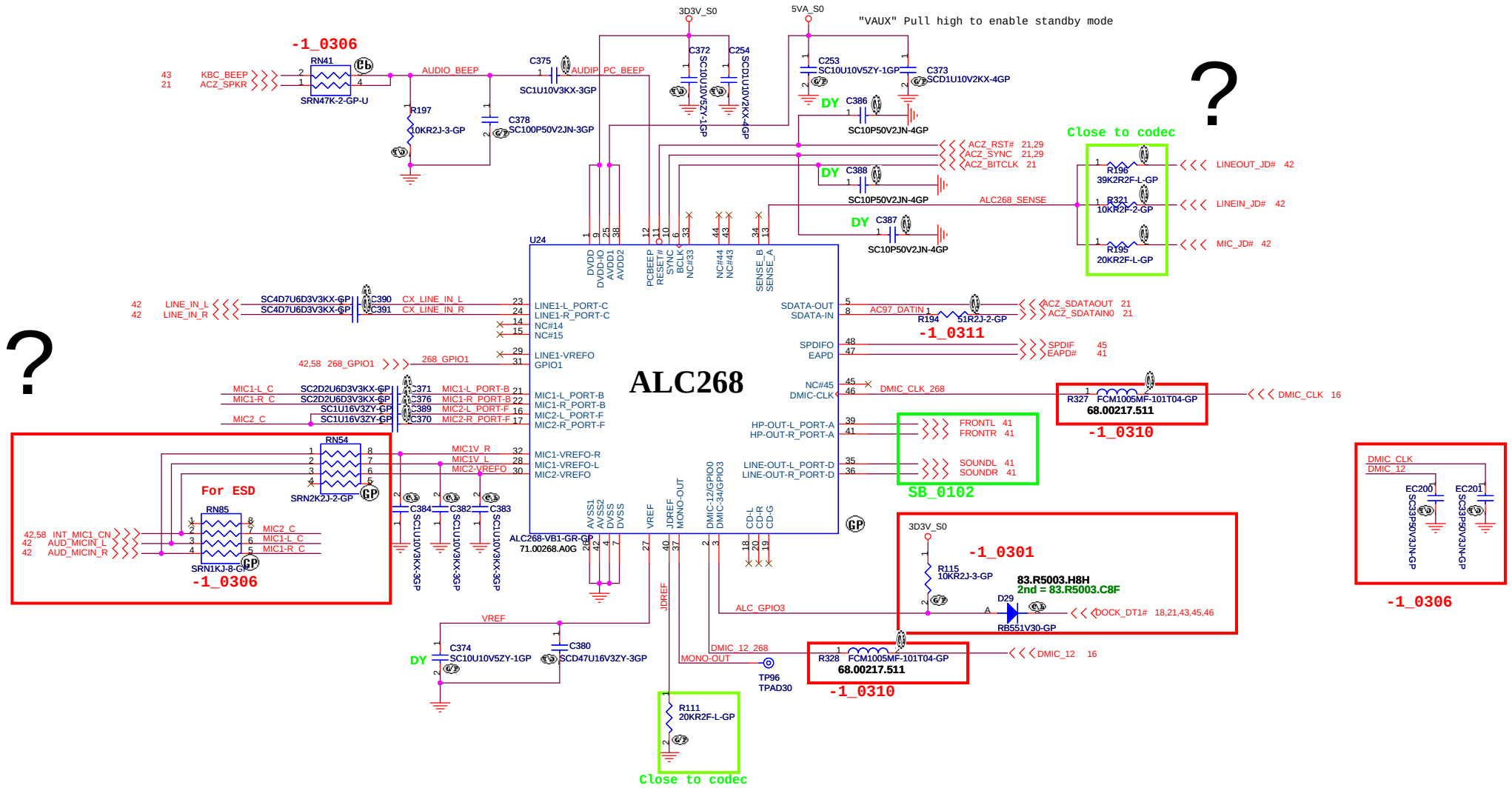
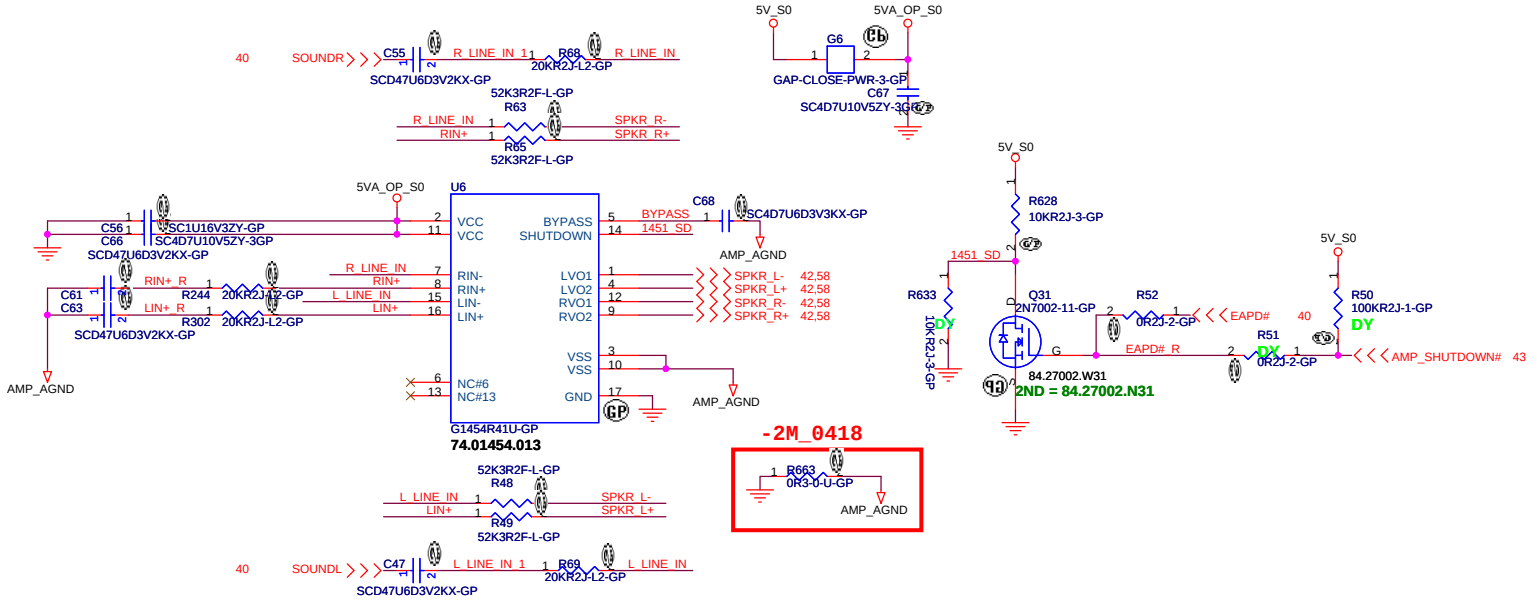
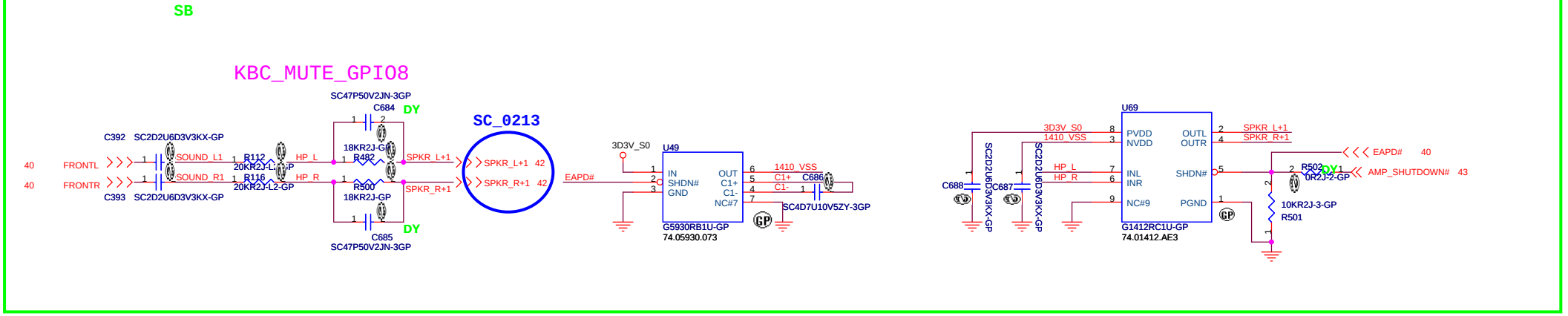

"VAUX" Pull high to enable standby mode
-1_0306
ALC268
U24
ALC268-VB1-GR-GP
71.00268.A0G
Close to codec
-1_0311
-1_0310
SB_0102
-1_0301
-1_0304
For ESD
Close to codec
POWER GENERATE
Layout
20 mil
? Add 2nd source
RT9198-4GPBG-GP
74.09198.A7F
2nd = 74.00923.C3F
(G923-475T1UF)
83.R5003.H8H
2nd = 83.R5003.C8F
68.00217.511
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Azalia codec ALC268
Olan
Friday, April 18, 2008

AUDIO OP AMPLIFIER





<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *AUDIO AMP*

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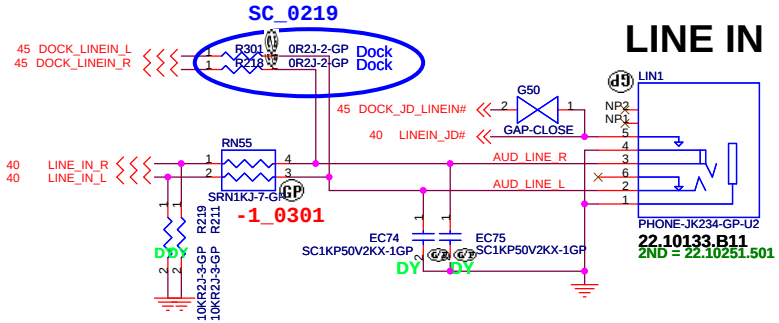
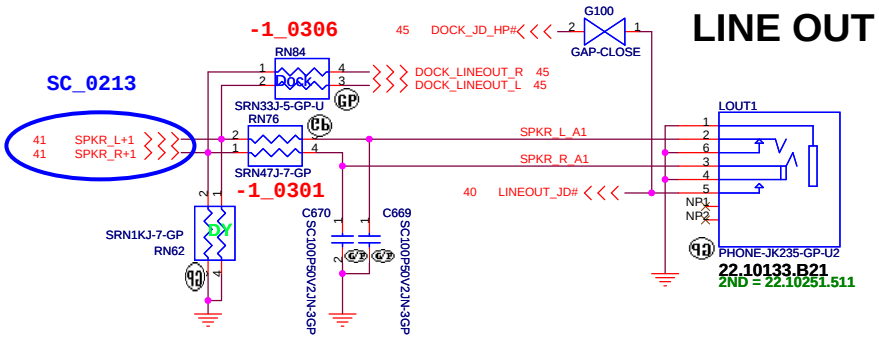
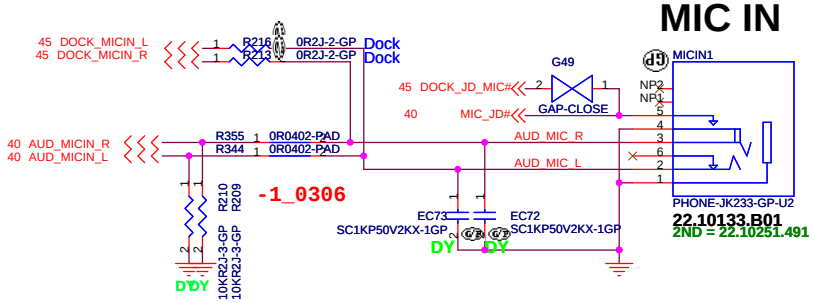
LINE IN



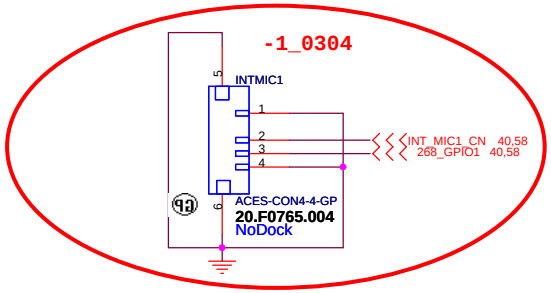
LINE OUT



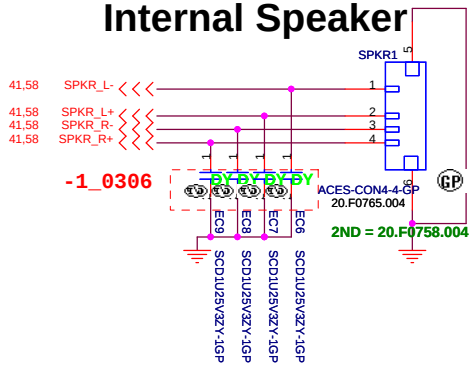
MIC IN



Internal MIC



Internal Speaker



<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *AUDIO JACK*		
Size: A3	Document Number: Olan	Rev: -1
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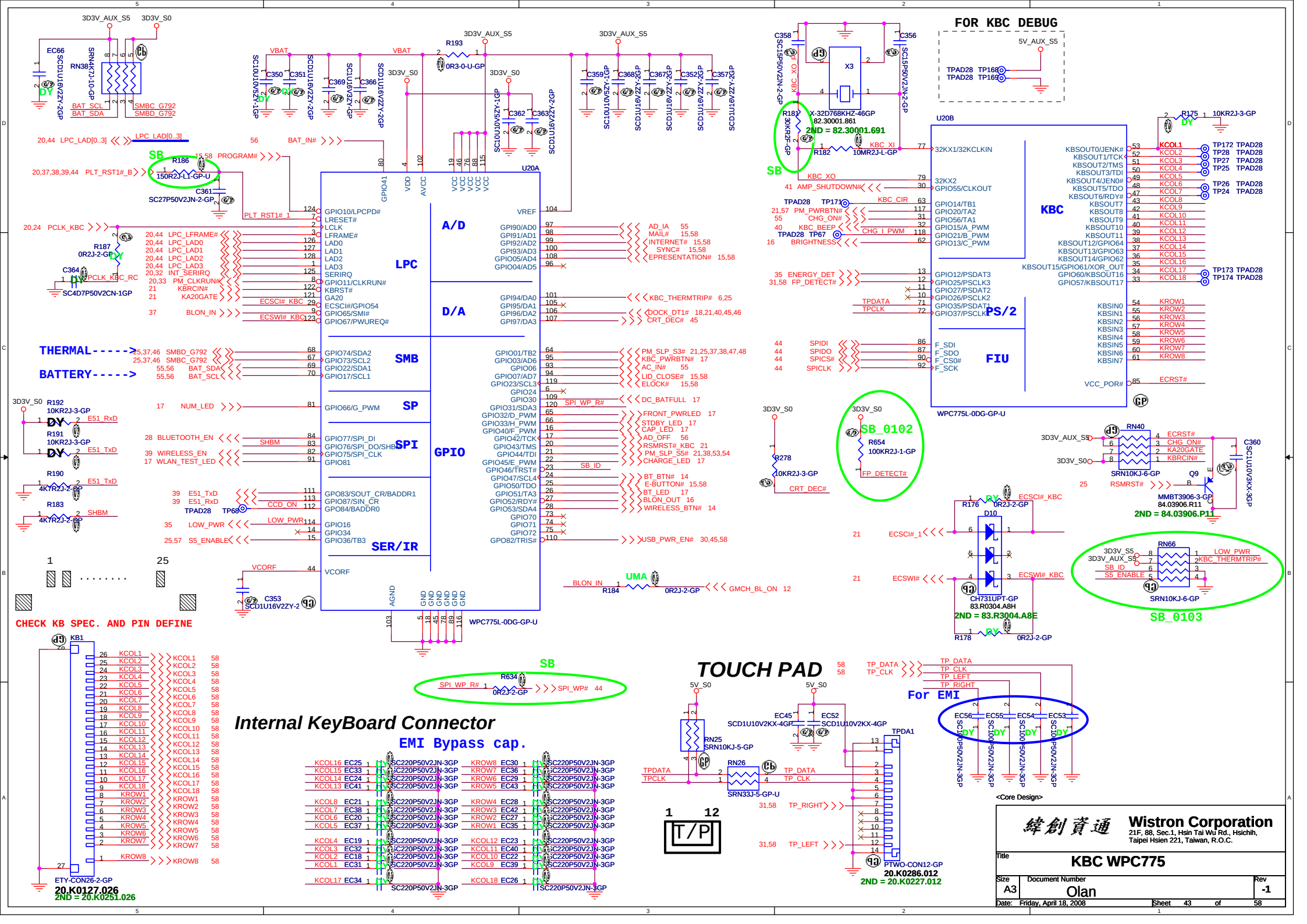
FOR KBC DEBUG
5V_AUX_S5
TPAD28 TP168
TPAD28 TP169
U20A
U20B
KBC
PS/2
FIU
LPC
A/D
D/A
SMB
SP
SPI
GPIO
SER/IR
WPC775L-0DG-GP-U
THERMAL----->
BATTERY----->
CHECK KB SPEC. AND PIN DEFINE
Internal KeyBoard Connector
EMI Bypass cap.
TOUCH PAD
For EMI
SB
SB_0102
SB_0103
2ND = 82.30001.691
2ND = 84.03906.P11
2ND = 83.R3004.A8E
20.K0127.026
2ND = 20.K0251.026
20.K0286.012
2ND = 20.K0227.012
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC775
Olan
Size A3
Rev -1
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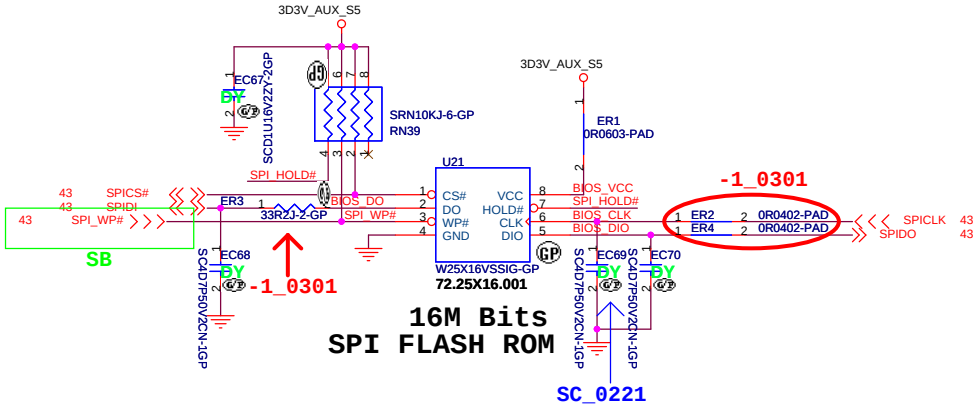

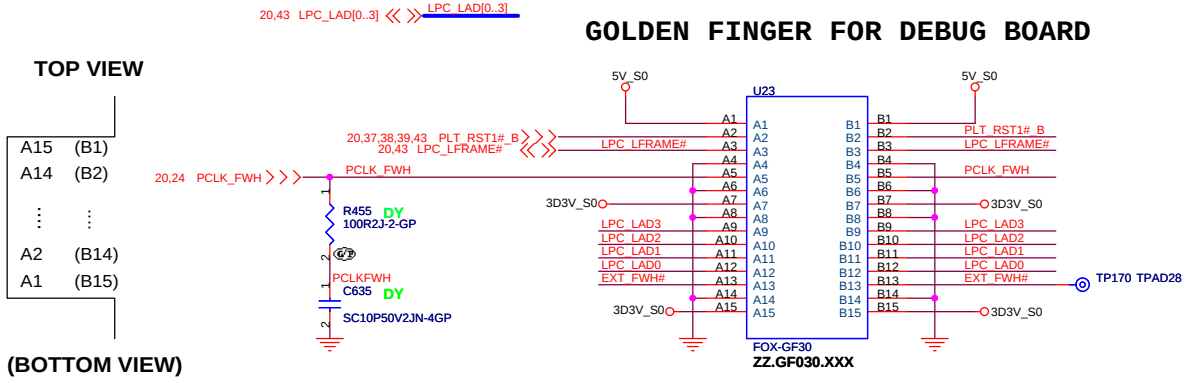

<Core Design>

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Title: BIOS

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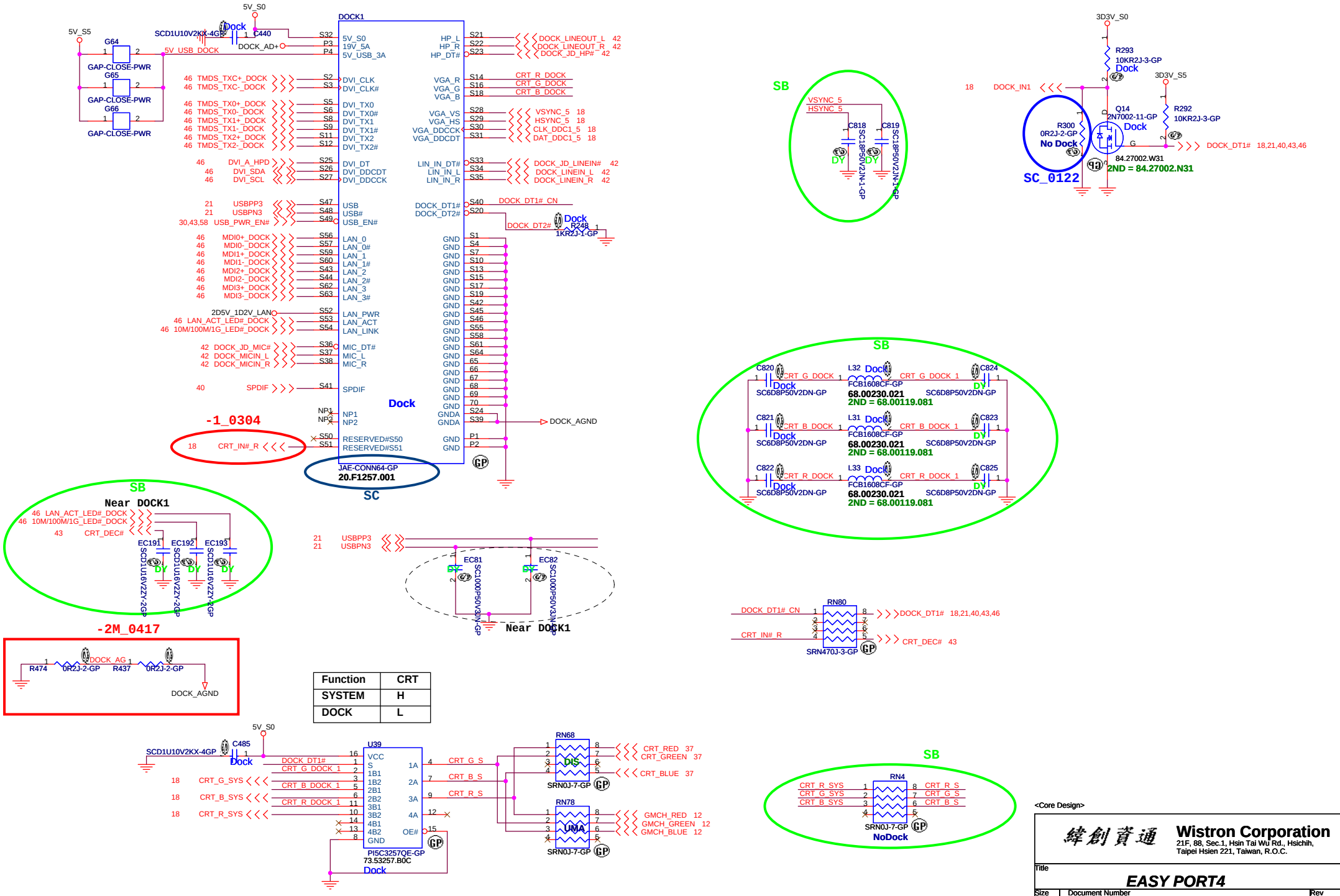

Function	CRT
SYSTEM	H
DOCK	L

<Core Design>

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Title: EASY PORT4

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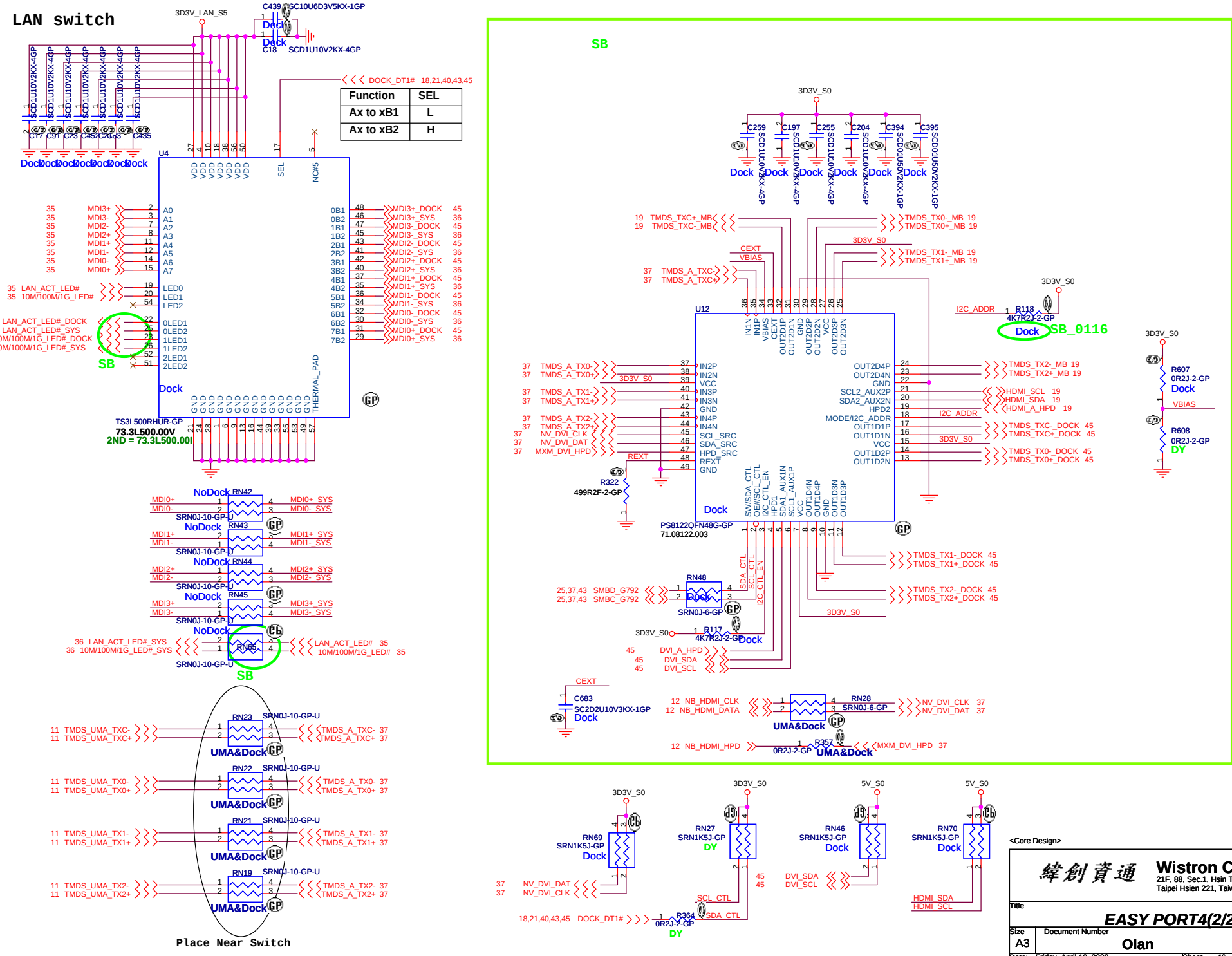
LAN switch
SB
Dock
NoDock
UMA&Dock
Place Near Switch
TS3L500RHUR-GP
PS8122QFN48G-GP
71.08122.003
SB_0116
Function
SEL
Ax to xB1
L
Ax to xB2
H
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
EASY PORT4(2/2)
Olan
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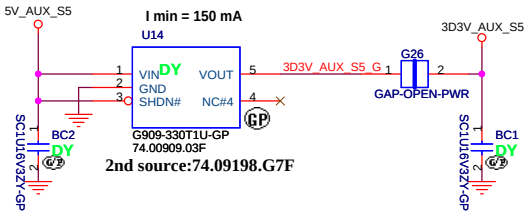
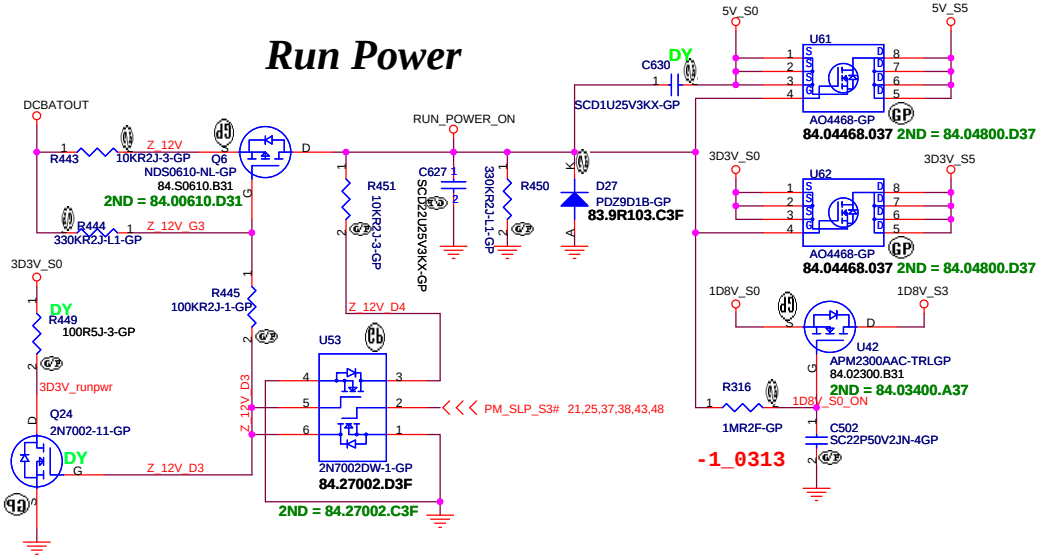
Aux Power 3D3V_AUX_S5



Run Power



<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: RUN POWER and 3D3V_AUX_S5

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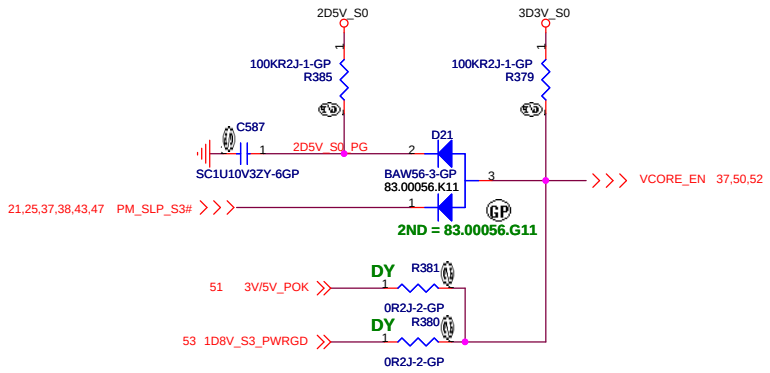
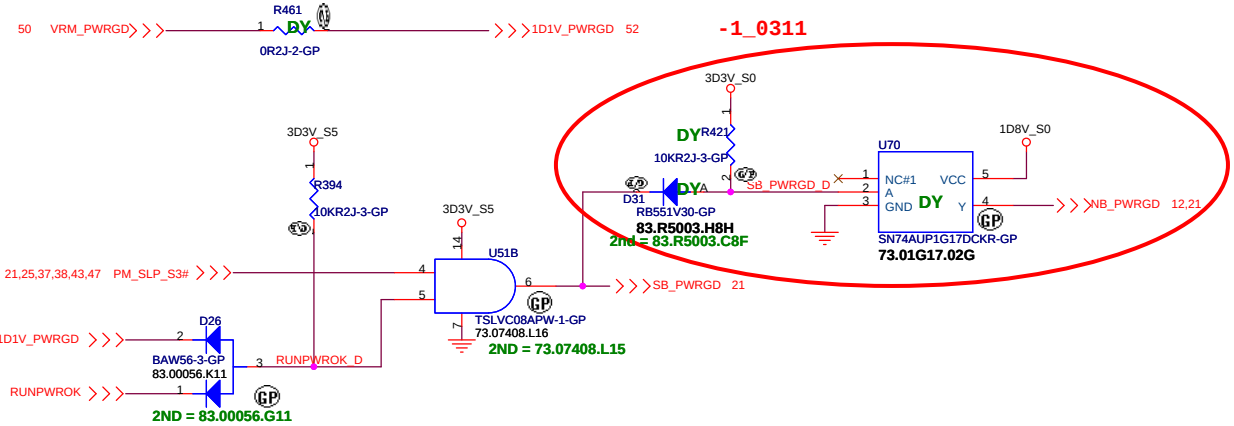


P/H @ 1D8V_S3 PAGE



<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***POWER ON LOGIC***

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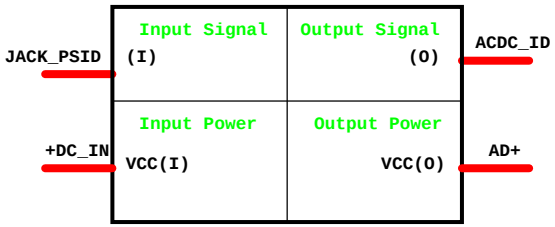
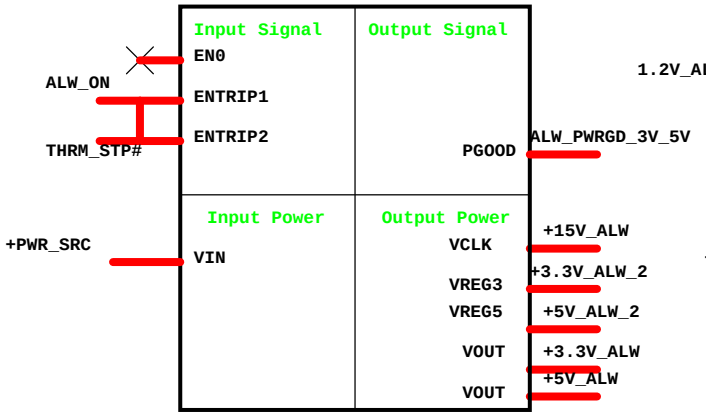
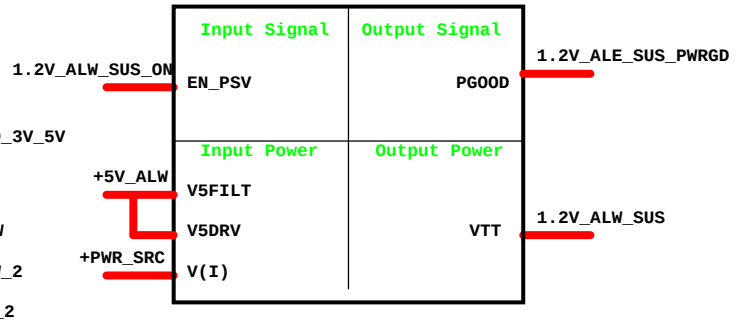
Adapter



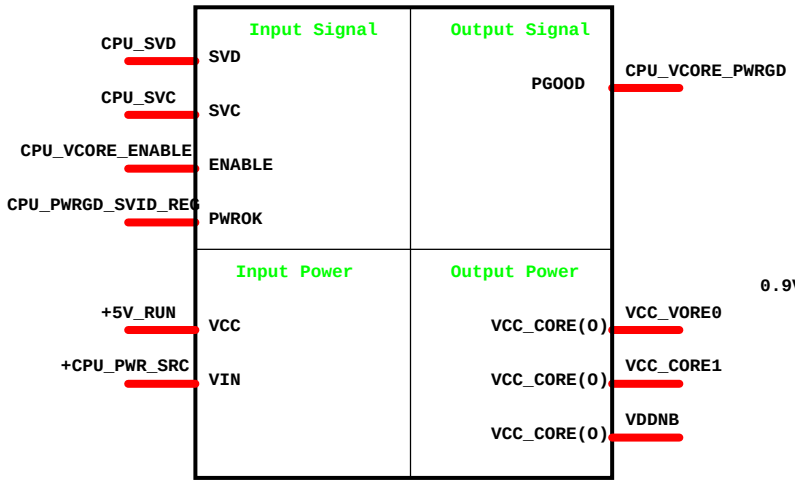
SN0608098



DCDC 1D2V(TPS5117)

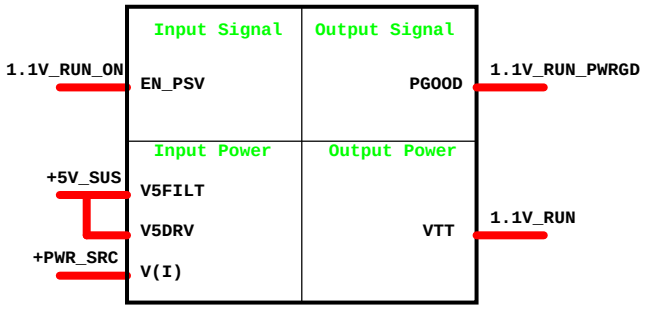


CPU_CORE
ISL6265HRTZ

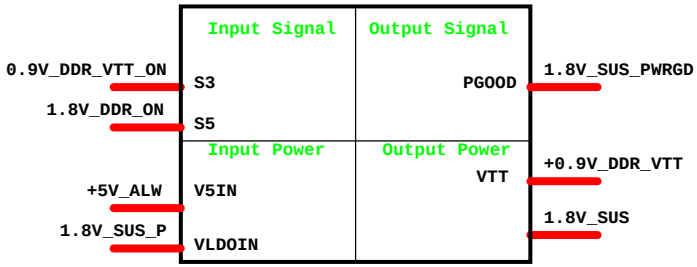


	S3	S5	VDDQ	VTTREF	VTT
S0 S3	1	1	1	1	1
S4 S5	0	0	0	0	0

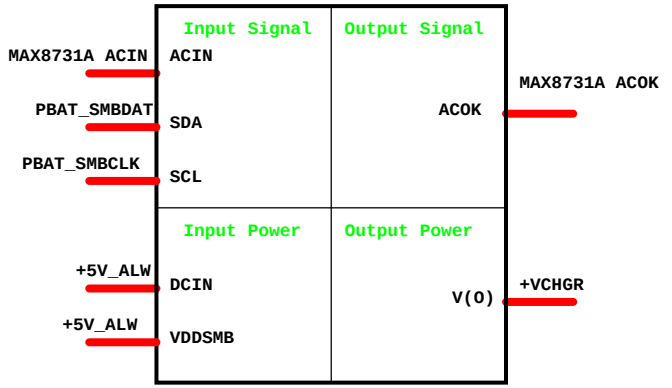
1D1V(TPS5117)



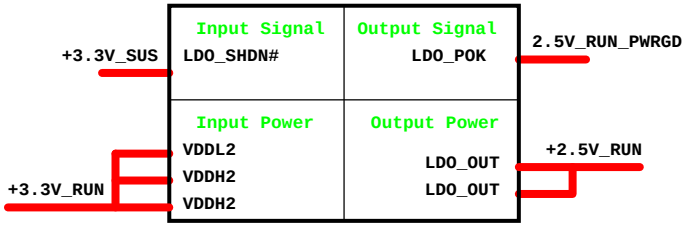
1D8V/0D9V(TPS5116)



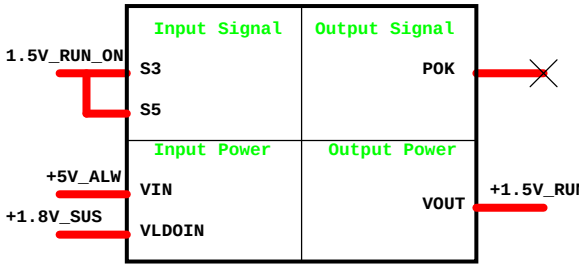
CHARGER BQ24745



2.5V LDO
EMC4002



1.5V_LDO



<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

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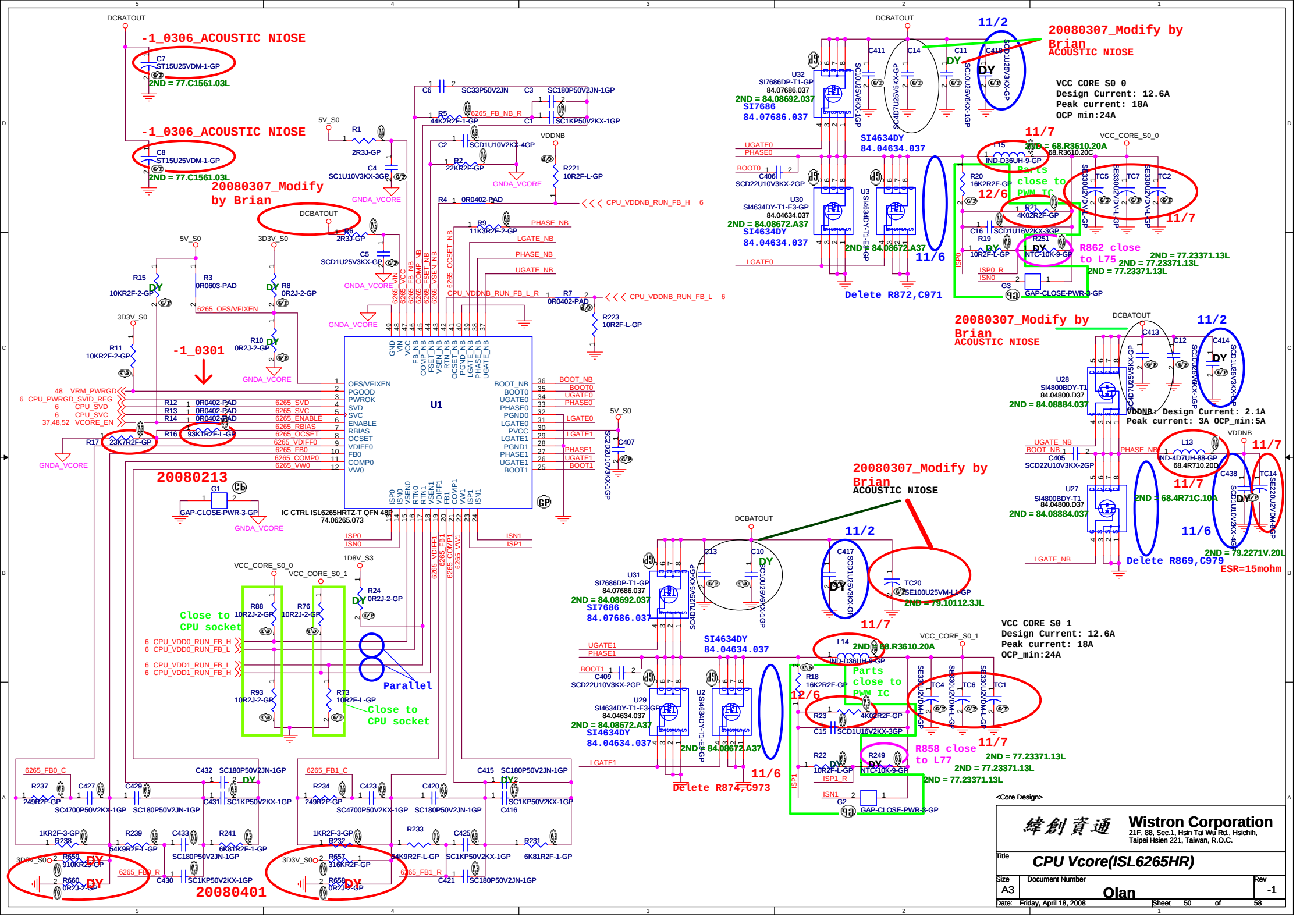
-1_0306_ACOUSTIC NIOSE
2ND = 77.C1561.03L
20080307_Modify by Brian
-1_0301
20080213
IC CTRL ISL6265HRTZ-T QFN 48P
74.06265.073
U1
Close to CPU socket
Parallel
20080401
20080307_Modify by Brian
ACOUSTIC NIOSE
11/2
11/7
11/6
12/6
VCC_CORE_S0_0
Design Current: 12.6A
Peak current: 18A
OCP_min:24A
SI7686
84.07686.037
SI4634DY
84.04634.037
Parts close to PWM IC
R862 close to L75
Delete R872,C971
VDDNB: Design Current: 2.1A
Peak current: 3A OCP_min:5A
Delete R869,C979
ESR=15mohm
VCC_CORE_S0_1
Design Current: 12.6A
Peak current: 18A
OCP_min:24A
R858 close to L77
Delete R874,C973
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
CPU Vcore(ISL6265HR)
Size A3
Document Number Olan
Rev -1
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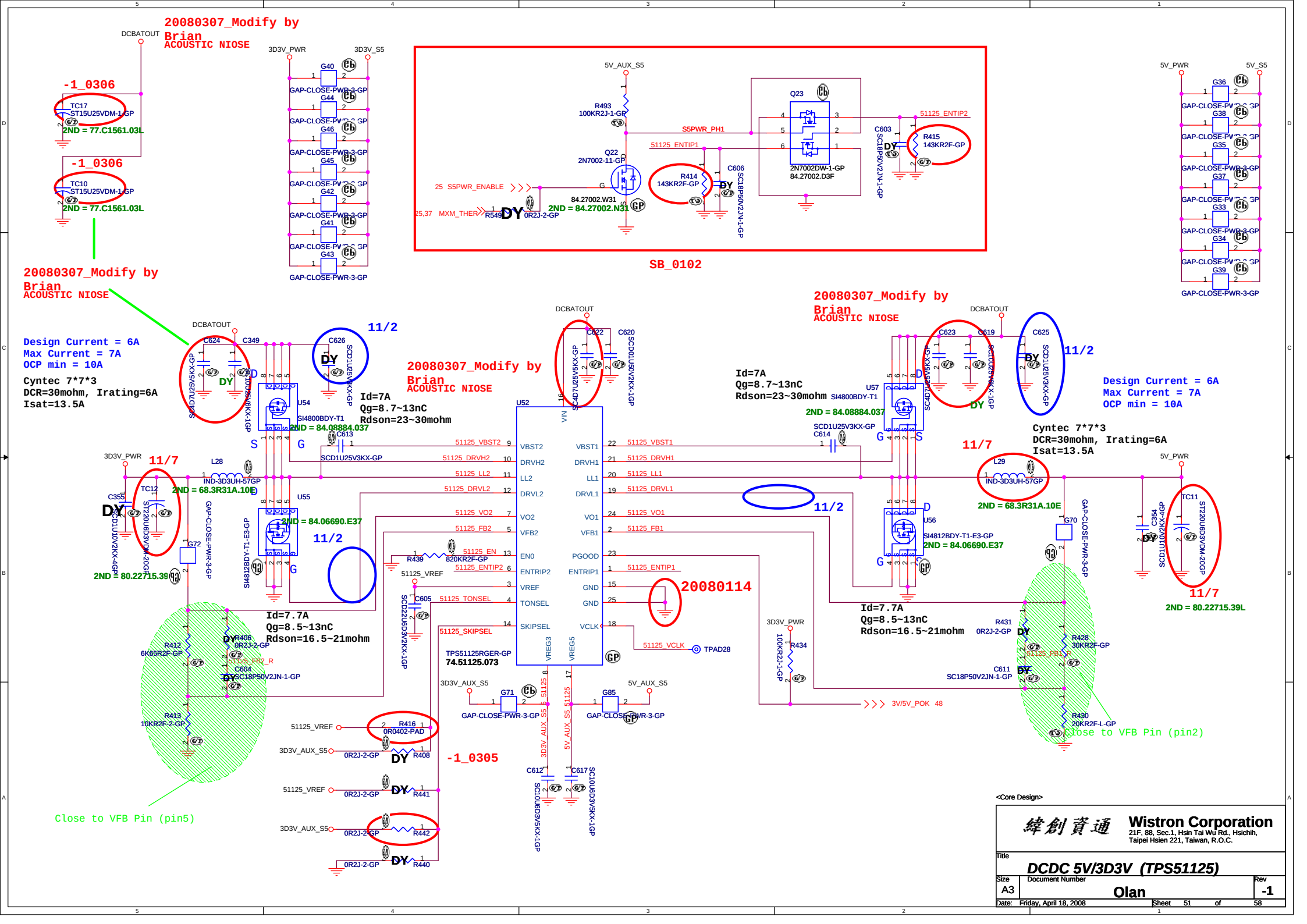
20080307_Modify by Brian
ACOUSTIC NIOSE
-1_0306
TC17 ST15U25VDM-1-GP
2ND = 77.C1561.03L
TC10 ST15U25VDM-1-GP
SB_0102
Design Current = 6A
Max Current = 7A
OCP min = 10A
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
SI4800BDY-T1
2ND = 84.08884.037
SI4812BDY-T1-E3-GP
2ND = 84.06690.E37
TPS51125RGER-GP
74.51125.073
20080114
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
-1_0305
Close to VFB Pin (pin5)
Close to VFB Pin (pin2)
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DCDC 5V/3D3V (TPS51125)
Olan
Friday, April 18, 2008

20080307_Modify by Brian
ACOUSTIC NIOSE

Vtrip(mV)=Rtrip(Kohm)*10(uA)
Iocp=(Vtrip/Rdson)+((1/(2*L*f))*((Vin-Vout)*Vout)/Vin))

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L

DCBATOUT

-1_0306

TC19 SE100U25VM-L1-GP
2ND = 79.10112.3JL

R309 0R2J-2-GP

3D3V_S0

5V_S5

R460 10KR2J-3-GP

11/9

R467 3D3R3J-L-GP

C642 SC4D7U10V5ZY-3GP

C644 SC1U10V3KX-3GP

1D2V_PWR
1D1V_PWR
51124_VFB2
51124_VFB1

1D1V_PWRGD
1D2V_PWRGD

1D1V_PWRGD 48

TP177TPAD30

R462 10KR2J-3-GP
37,48,50 VCORE_EN

DY BC3 SC1U10V3KX-3GP

U65

51124_V5FILT

51124_EN1
51124_EN2

R471 1KR2J-1-GP
37,48,50 VCORE_EN

DY BC4 SCD47U6D3V2KX-GP

VFB1 VFB2 VO1 VO2 PGOOD1 PGOOD2

V5FILT
V5IN
EN1
EN2
GND
GND
PGND2
PGND1
TRIP1
TRIP2
VBST1
VBST2
TONSEL
DRVH1
LL1
DRVL1
DRVH2
LL2
DRVL2

51124_DRVH1
51124_LL1
51124_DRVL1
51124_DRVH2
51124_LL2
51124_DRVL2

TPS51124RGER-GPU1
74.51124.073

51124_TRIP1
51124_TRIP2

R465 16K5R3F-GP
R468 14K3R3F-GP

20071206

51124_LL1
C641 SCD1U16V2KX-3GP
51124_VBST1

51124_LL2
C652 SCD1U16V2KX-3GP
51124_VBST2

51124_TONSEL

R458 10KR2J-3-GP
DY
R459 0R2J-2-GP
DY

51124_V5FILT

20080307_Modify by Brian
ACOUSTIC NIOSE

DCBATOUT

U59 SI4800BDY-T1 84.04800.D37
2ND = 84.08884.037

TC21 SE100U25VM-L1-GP
2ND = 79.10112.3JL

C633 SCD1U25V3KX-GP
DY

11/7

Iomax=8A

Vo(cal)=1.1060V

L27 COIL-1UH-34-GP 68.1R01A.20B
11/7
2ND = 68.1R10A.10S

U60 SI4812BDY-T1-E3-GP 84.04812.A37
2ND = 84.06690.E37
11/7

R464 18KR2F-GP
DY
SC18P50V2JN-1-GP

C640

R466 39K2R2F-L-GP

51124_VFB1

C615 SCD1U10V2KX-4GP
DY

TC16 ST330U2D5VDM9GP
11/7
ESR=9mohm
2ND = 80.3371V.L01

Close to VFB Pin (pin5)

1D1V_PWR

G29 GAP-CLOSE-PWR-3-GP
G32 GAP-CLOSE-PWR-3-GP
G75 GAP-CLOSE-PWR-3-GP
G73 GAP-CLOSE-PWR-3-GP
G31 GAP-CLOSE-PWR-3-GP
G74 GAP-CLOSE-PWR-3-GP
G68 GAP-CLOSE-PWR-3-GP
G30 GAP-CLOSE-PWR-3-GP
G76 GAP-CLOSE-PWR-3-GP
G101 GAP-CLOSE-PWR-3-GP
G102 GAP-CLOSE-PWR-3-GP

1D1V_S0

20080307_Modify by Brian
ACOUSTIC NIOSE

DCBATOUT

C649 SC4D7U25V5KX-GP

U64 SI4800BDY-T1 84.04800.D37
2ND = 84.08884.037
11/7

C653 SCD10U25V3KX-1GP
DY

C648 SCD1U25V3KX-GP
DY

11/7

1D2V Iomax=5A
OCP>10A

L30 IND-1D5UH-23-GP 68.1R510.10K
2ND = 68.1R510.10V

R470 17K8R2F-GP
DY

C651 SC18P50V2JN-1-GP

51124_VFB2

R472 30KR2F-GP

U63 SI4812BDY-T1-E3-GP 84.04812.A37
2ND = 84.06690.E37
11/7

C632 SCD1U10V2KX-4GP
DY

TC18 SSE220U2D5VDM-6GP
11/7
ESR=15mohm
2ND = 80.2271V.A9L

1D2V_PWR

G93 GAP-CLOSE-PWR-3-GP
G90 GAP-CLOSE-PWR-3-GP
G92 GAP-CLOSE-PWR-3-GP
G91 GAP-CLOSE-PWR-3-GP
G88 GAP-CLOSE-PWR-3-GP
G89 GAP-CLOSE-PWR-3-GP
G103 GAP-CLOSE-PWR-3-GP
G104 GAP-CLOSE-PWR-3-GP

1D2V_S0

	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

Vout=0.758V*(R1+R2)/R2 --> PWM mode
Vout=0.764V*(R1+R2)/R2 --> Skip Mode

<Core Design>

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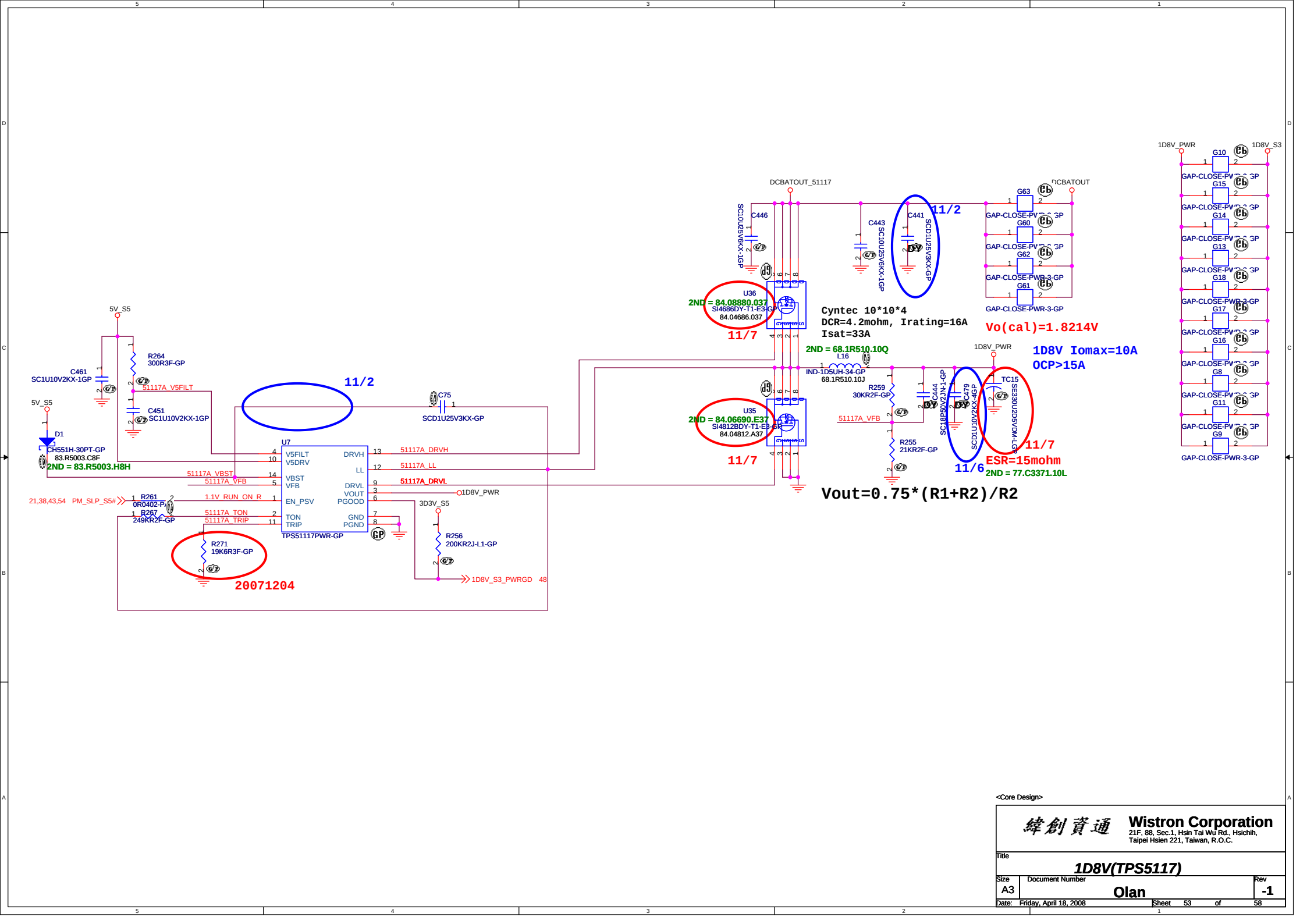
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51124_1D1V_1D2V

Size	Document Number	Rev
A3	Olan	-1

Date: Friday, April 18, 2008 Sheet 52 of 58



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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***1D8V(TPS5117)***

Size	Document Number	Rev
A3	Olan	-1

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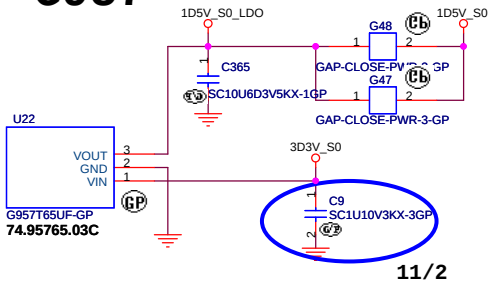
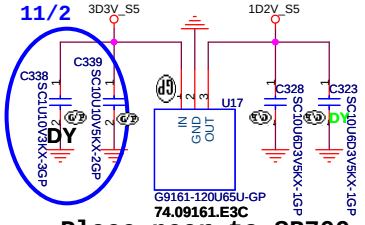
1D5V_S0
Iomax=1A

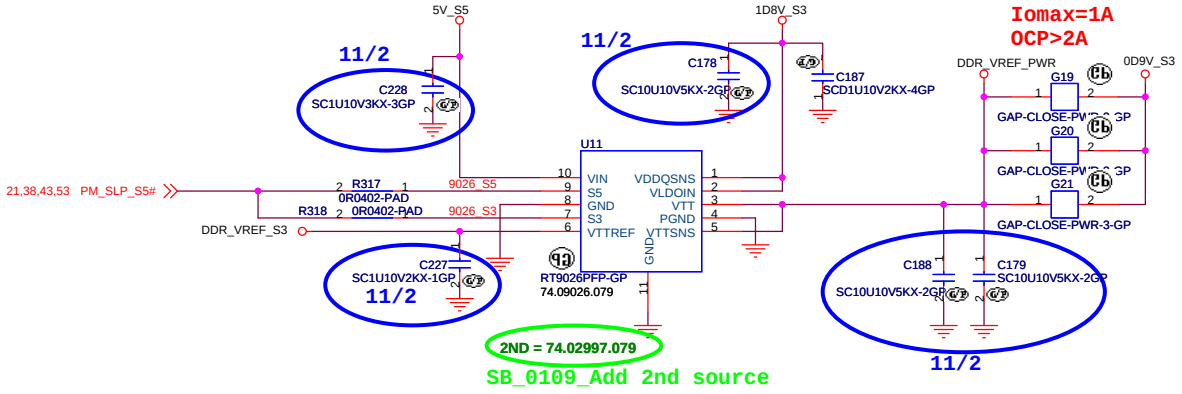
G957



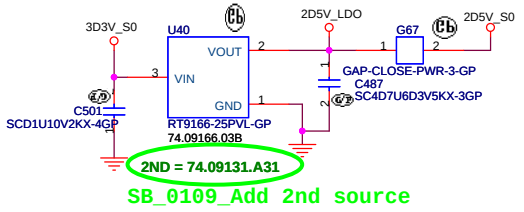
1D2V_S5
Iomax=400mA



Place near to SB700



2D5V_S0
Iomax=0.3A 2D5V/300mA



SB_0109_Add 2nd source

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: 0D9V&2D5V&1D25V&1D5V

Size	Document Number	Rev
A3	Olan	-1

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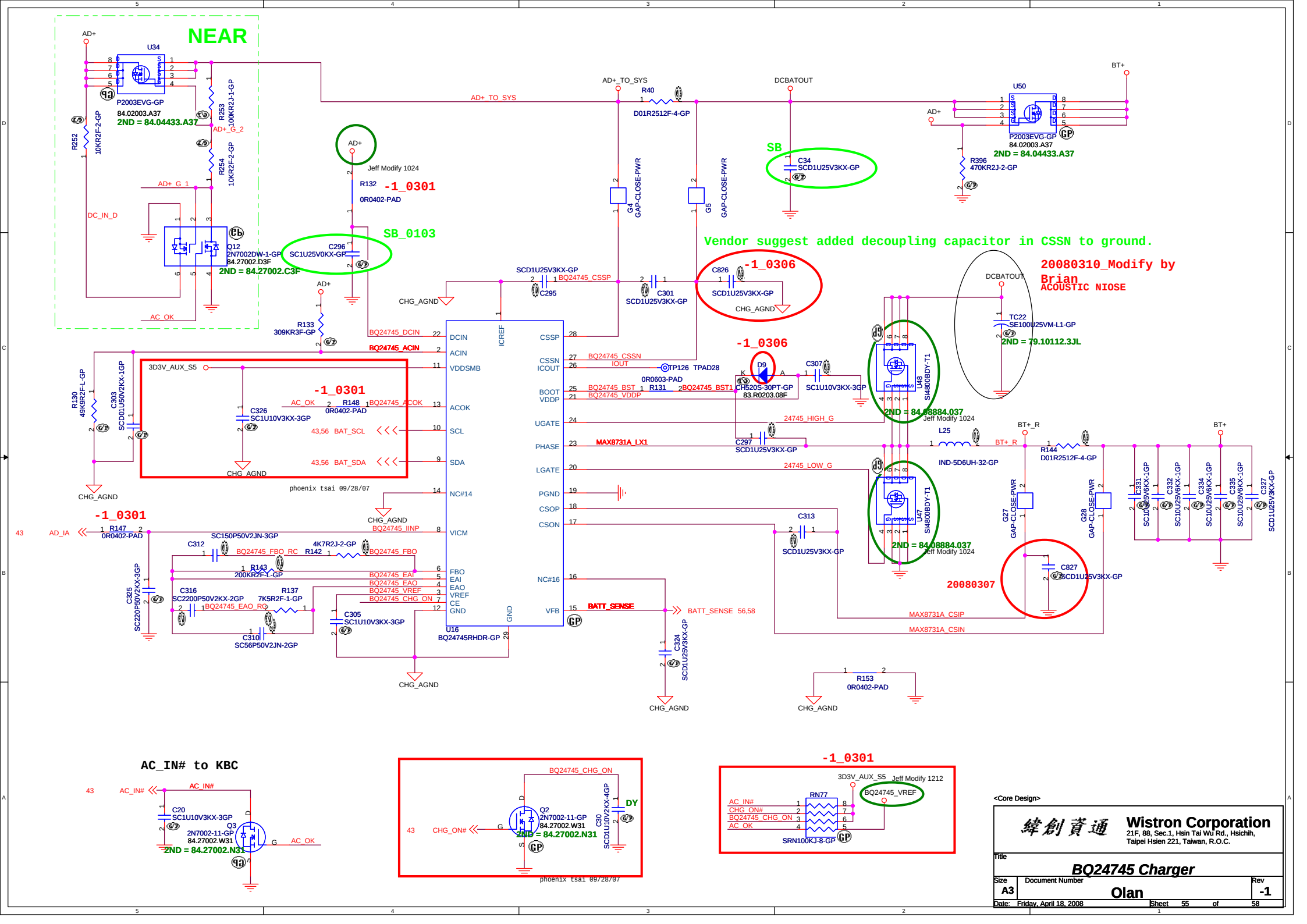
NEAR
U34
P2003EVG-GP
84.02003.A37
2ND = 84.04433.A37
R252 10KR2F-2-GP
R253 100KR2J-1-GP
R254 10KR2F-2-GP
AD+_G_2
AD+_G_1
DC_IN_D
Q12
2N7002DW-1-GP
84.27002.D3F
2ND = 84.27002.C3F
AC_OK
AD+
Jeff Modify 1024
R132 -1_0301
0R0402-PAD
SB_0103
C296
SC1U25V0KX-GP
R133
309KR3F-GP
AD+_TO_SYS
R40
D01R2512F-4-GP
DCBATOUT
SB
C34
SCD1U25V3KX-GP
U50
P2003EVG-GP
84.02003.A37
2ND = 84.04433.A37
R396
470KR2J-2-GP
BT+
G4 GAP-CLOSE-PWR
G5 GAP-CLOSE-PWR
Vendor suggest added decoupling capacitor in CSSN to ground.
20080310_Modify by Brian
ACOUSTIC NIOSE
SCD1U25V3KX-GP
C295
BQ24745_CSSP
C301
SCD1U25V3KX-GP
C826
-1_0306
SCD1U25V3KX-GP
CHG_AGND
TC22
SE100U25VM-L1-GP
2ND = 79.10112.3JL
-1_0306
D9
CH520S-30PT-GP
83.R0203.08F
0R0603-PAD
R131
C307
SC1U10V3KX-3GP
U48
SI4800BDY-T1
2ND = 84.08884.037
Jeff Modify 1024
L25
IND-5D6UH-32-GP
BT+_R
R144
D01R2512F-4-GP
U47
SI4800BDY-T1
2ND = 84.08884.037
Jeff Modify 1024
G27 GAP-CLOSE-PWR
G28 GAP-CLOSE-PWR
C331 SC10U25V6KX-1GP
C332 SC10U25V6KX-1GP
C334 SC10U25V6KX-1GP
C335 SC10U25V6KX-1GP
C327 SCD1U25V3KX-GP
C827
SCD1U25V3KX-GP
20080307
3D3V_AUX_S5
R130 49K9R2F-L-GP
C303 SCD01U50V2KX-1GP
-1_0301
C326
SC1U10V3KX-3GP
R148
0R0402-PAD
AC_OK
BQ24745_ACOK
43,56 BAT_SCL
43,56 BAT_SDA
phoenix tsai 09/28/07
-1_0301
43 AD_IA
R147
0R0402-PAD
C312
SC150P50V2JN-3GP
BQ24745_FBO_RC
R142
4K7R2J-2-GP
BQ24745_FBO
R143
200KR2F-L-GP
C325 SC220P50V2KX-3GP
C316
SC2200P50V2KX-2GP
BQ24745_EAO_RC
R137
7K5R2F-1-GP
C310
SC56P50V2JN-2GP
C305
SC1U10V3KX-3GP
BQ24745_EAI
BQ24745_EAO
BQ24745_VREF
BQ24745_CHG_ON
BQ24745_IINP
U16
BQ24745RHDR-GP
DCIN
ACIN
VDDSMB
ACOK
SCL
SDA
NC#14
VICM
FBO
EAI
EAO
VREF
CE
GND
ICREF
CSSP
CSSN
ICOUT
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC#16
VFB
BQ24745_DCIN
BQ24745_ACIN
BQ24745_CSSN
IOUT
TP126 TPAD28
BQ24745_BST
BQ24745_VDDP
BQ24745_BST1
24745_HIGH_G
MAX8731A_LX1
24745_LOW_G
BATT_SENSE
BATT_SENSE 56,58
MAX8731A_CSIP
MAX8731A_CSIN
C313
SCD1U25V3KX-GP
C324
SCD1U25V3KX-GP
R153
0R0402-PAD
AC_IN# to KBC
43 AC_IN#
C20
SC1U10V3KX-3GP
Q3
2N7002-11-GP
84.27002.W31
2ND = 84.27002.N31
AC_OK
BQ24745_CHG_ON
43 CHG_ON#
Q2
2N7002-11-GP
84.27002.W31
2ND = 84.27002.N31
C30
SCD1U10V2KX-4GP
DY
phoenix tsai 09/28/07
-1_0301
3D3V_AUX_S5
Jeff Modify 1212
BQ24745_VREF
RN77
AC_IN#
CHG_ON#
BQ24745_CHG_ON
AC_OK
SRN100KJ-8-GP
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
BQ24745 Charger
Size A3
Document Number Olan
Rev -1
Date: Friday, April 18, 2008
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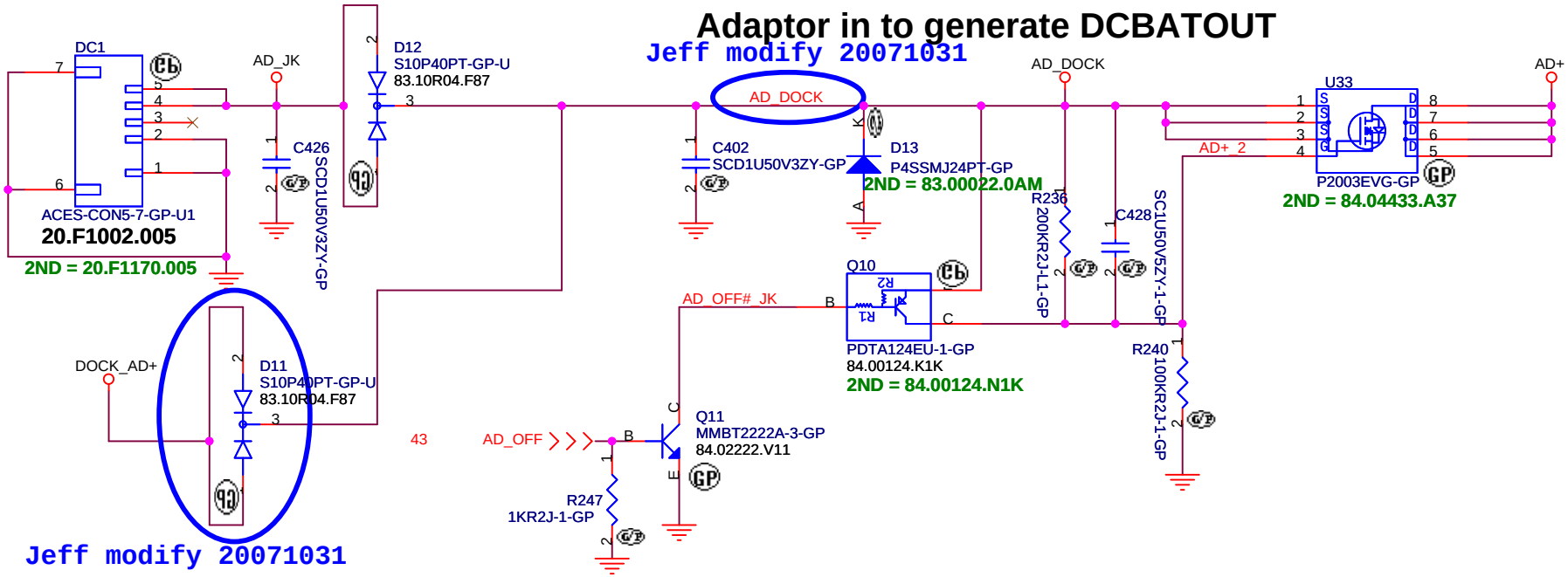
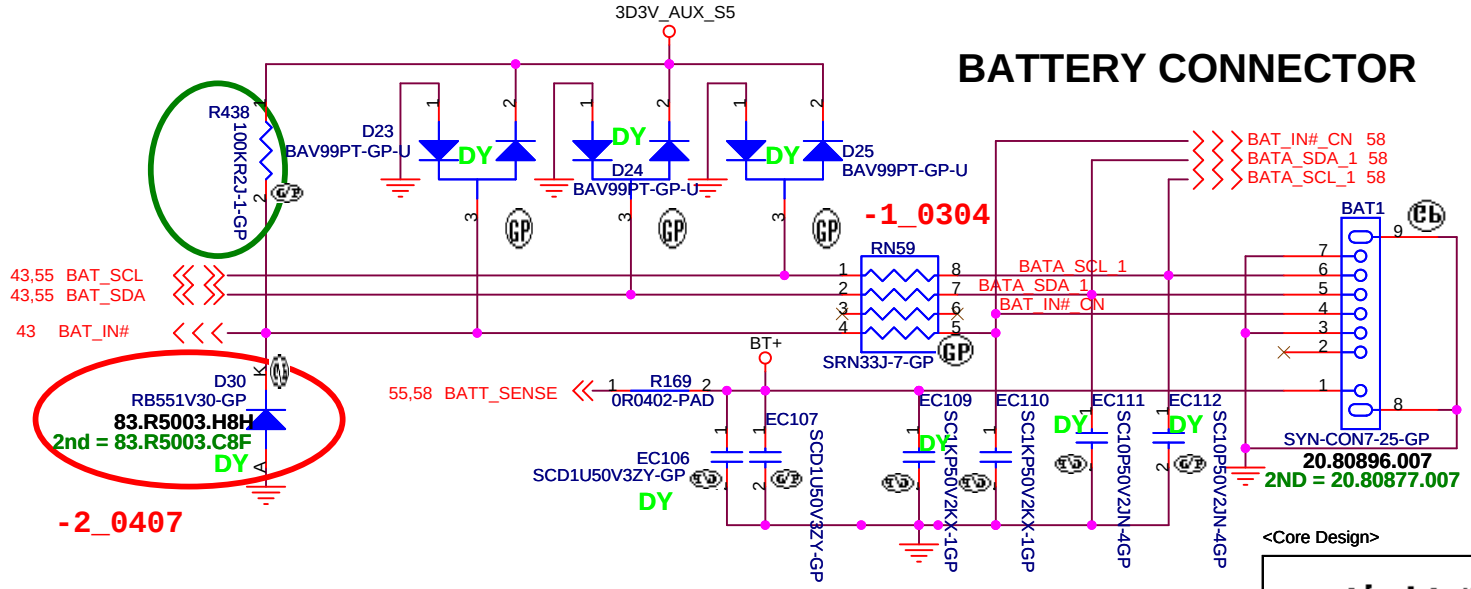
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***AD/BATT CONN***

Size	Document Number	Rev
A4	Olan	-1

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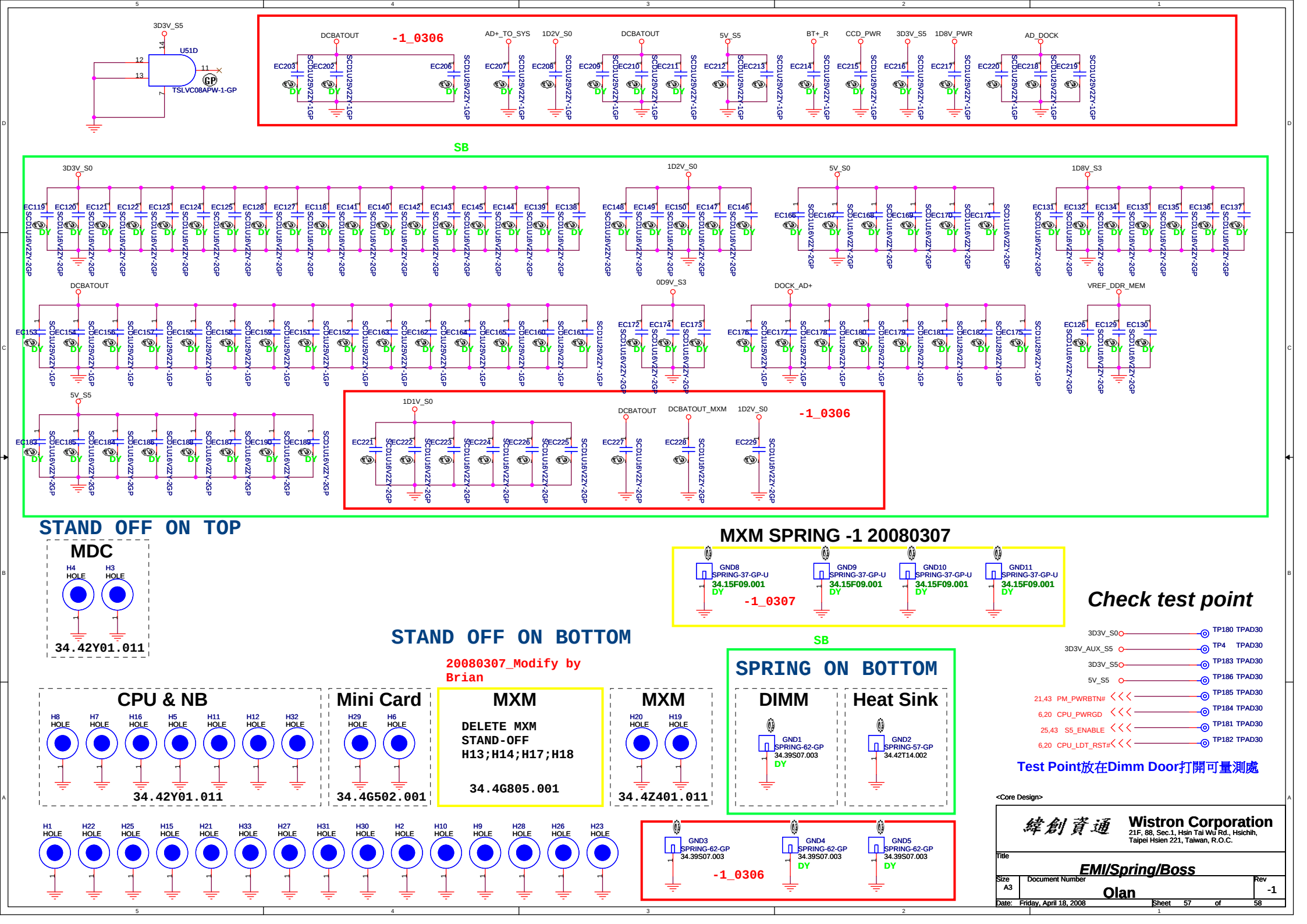
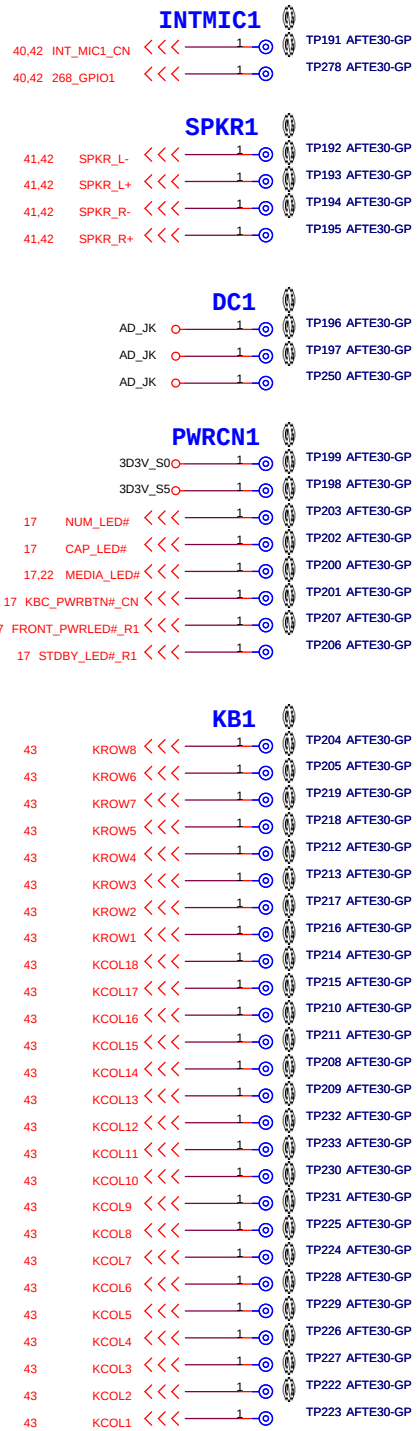

3D3V_S5
U51D
TSLVC08APW-1-GP
DCBATOUT
-1_0306
AD+_TO_SYS
1D2V_S0
5V_S5
BT+_R
CCD_PWR
3D3V_S5
1D8V_PWR
AD_DOCK
SB
3D3V_S0
1D2V_S0
5V_S0
1D8V_S3
DCBATOUT
0D9V_S3
DOCK_AD+
VREF_DDR_MEM
5V_S5
1D1V_S0
DCBATOUT
DCBATOUT_MXM
1D2V_S0
-1_0306
STAND OFF ON TOP
MDC
H4 HOLE
H3 HOLE
34.42Y01.011
MXM SPRING -1 20080307
GND8 SPRING-37-GP-U 34.15F09.001 DY
GND9 SPRING-37-GP-U 34.15F09.001 DY
GND10 SPRING-37-GP-U 34.15F09.001 DY
GND11 SPRING-37-GP-U 34.15F09.001 DY
-1_0307
Check test point
3D3V_S0 TP180 TPAD30
3D3V_AUX_S5 TP4 TPAD30
3D3V_S5 TP183 TPAD30
5V_S5 TP186 TPAD30
21,43 PM_PWRBTN# TP185 TPAD30
6,20 CPU_PWRGD TP184 TPAD30
25,43 S5_ENABLE TP181 TPAD30
6,20 CPU_LDT_RST# TP182 TPAD30
Test Point放在Dimm Door打開可量測處
STAND OFF ON BOTTOM
20080307_Modify by Brian
SB
SPRING ON BOTTOM
CPU & NB
H8 HOLE
H7 HOLE
H16 HOLE
H5 HOLE
H11 HOLE
H12 HOLE
H32 HOLE
34.42Y01.011
Mini Card
H29 HOLE
H6 HOLE
34.4G502.001
MXM
DELETE MXM
STAND-OFF
H13;H14;H17;H18
34.4G805.001
MXM
H20 HOLE
H19 HOLE
34.4Z401.011
DIMM
GND1 SPRING-62-GP 34.39S07.003 DY
Heat Sink
GND2 SPRING-57-GP 34.42T14.002
H1 HOLE
H22 HOLE
H25 HOLE
H15 HOLE
H21 HOLE
H33 HOLE
H27 HOLE
H31 HOLE
H30 HOLE
H2 HOLE
H10 HOLE
H9 HOLE
H28 HOLE
H26 HOLE
H23 HOLE
GND3 SPRING-62-GP 34.39S07.003
GND4 SPRING-62-GP 34.39S07.003 DY
GND5 SPRING-62-GP 34.39S07.003 DY
-1_0306
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
EMI/Spring/Boss
Size A3
Document Number
Olan
Rev -1
Date: Friday, April 18, 2008
Sheet 57 of 58



<Core Design>

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Title: AFTE TP

Size	Document Number	Rev
A3	Olan	-2

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