AMD BRAZOS
Muxless Discrete/UMA Schematics Document
AMD Ontario CPU FT1
AMD GPU Seymour XT S3
2010-12-01

REV : SA

DY :None Installed
UMA:UMA platform installed
PARK:DIS PARK platform installed
MADISON:DIS MADISON platform installed
Colay :Manual modify BOM
MUX : PX
ROB:ROBSON

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cover Page

Size	Document Number	Rev
A3	B575	-1

Date: Friday, March 25, 2011 Sheet 1 of 103

PROJECT CODE : 91.4PN01.001
PCB P/N : 10332
REVISION : SA

Block Diagram

LAN BD
POWER BD
CR BD
LED BD
BlueTooth MD
FPR BD

CRT 50 — RGB CRT

AMD APU
Zacate-FT1
SINGLE CHANNEL DDR3
DISPLAY PORT X2
DX11 IGP
4 X1 PCIE GEN2 GPP
1 X4 UMI-LINK GEN1
VGA DAC 4,5,6,7,8

DDR III 1066 — DDRIII DIMM1 800/1066 14
DDRIII DIMM2 800/1066 15
DP0 LVDS — LVDS 49
DP1 HDMI — HDMI 51

VRAM 88,89
gDDR3
64M*16b*4(512MB)
128Mx16b*4(1GB)

AMD dGPU
Seymour -XT
83,84,85,86,87

Muxless (Share PCIe x 4)
PCIe x 4 Gen 2

UMIx4

AMD
HUDSON-M1 FCH
PCIE GEN1 1/F (4 x 1)
USB2.0(12) + 1.1(2)
SATAII (3 PORTS)
INT. CLKGEN
AZALIA HD AUDIO
GB MAC
SPI I/F
LPC I/F
HW MONITOR
17,18,19,20,21,22

BD USB x 2
Bluetooth 63
CAMERA 49
Finger Print 64
USB2.0 x 5

PCIE x 1 — GLAN RTL8111E 31 — RJ45 CONN SB
PCIE x 1/USB2.0 x 1 — Mini-Card WLAN 65
SATA x 1/USB2.0 x 1 — Mini-Card WWAN 66 — SIM 67
USB 2.0 x 1 — MB USB x 1 62
USB 2.0 x 1/SATAII x 1 — E-SATA/USB comb 57
SATA x 2 — HDD 56, ODD 55
LPC Bus — LPC debug port 71

SD/MMC+/MS/ MS Pro/xD SB
CardReader
Realtek RTS5139 SB
USB2.0

Internal DMIC
HP1
MIC IN
Azalia CODEC
CONEXANT CX20671 29
AZALIA

I/O BD
1.5W 2CH SPEAKER

KBC
NUVOTON NPCE791G 27
SPI

Flash ROM 2MB 60
Touch PAD 69
Int. KB 69
Thermal EMC2103-2-AP 28
Fan 28

PCB STACKUP

TOP		L1
VCC		L2
S		L3
S		L4
GND		L5
BOTTOM		L6

VGA RT8208B 92

INPUTS	OUTPUTS
DCBATOUT	VGA_CORE_PWR

AMD GPU CORE TPS51218D 47

INPUTS	OUTPUTS
DCBATOUT	1D8V_S0

SYSTEM DC/DC TPS51123 41

INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5 5V_AUX_S5 3D3V_AUX_S5

TPS51218D 45

INPUTS	OUTPUTS
DCBATOUT	1D0V_S0

DDRIII SUS TPS51218 46

INPUTS	OUTPUTS
DCBATOUT	1D5V_S3

RT9026 46

INPUTS	OUTPUTS
5V_S5	DDR_VREF_S3

TPS51218 46

INPUTS	OUTPUTS
DCBATOUT	1D1V_S5

CHARGER BQ24745 40

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR

CPU DC/DC ISL6265C 42

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

GFX Core ISL6265C 45

INPUTS	OUTPUTS
DCBATOUT	VDD_NB

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM
Size: A3 | Document Number: B575 | Rev: -1
Date: Friday, March 25, 2011 | Sheet 2 of 103

REQUIRED SYSTEM STRAPS ?

	AZ_SDOUT	PCI_CLK1	CLK_PCI_LPC	PCI_CLK4	LPC_CLK0	LPC_CLK1	LPC_CLK2
PULL HIGH	LOW POWER MODE	Allow PCIE GEN2 DEFAULT	USE DEBUG STRAPS	non_Fusion CLOCK mode	ENABLE EC	CLKGEN ENABLED (Use Internal) DEFAULT	Enable boot timer function
PULL LOW	PERFORMANCE MODE DEFAULT	Force PCIE GEN1	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode DEFAULT	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External)	Disable boot fail timer function DEFAULT

USB Table

Pair	Device
0	Internal #3(MB)
1	WLAN/WiMAX
2	WWAN
3	E-SATS/LUSB
4	BLUETOOTH
5	External #1(IO BD)
6	External #2(IO BD)
7	CAMERA(HS)
8	Finger Print
9	CardReader
10	NC
11	NC
12	NC
13	NC

PCIe Routing

	APU
LANE0	PEG
LANE1	
LANE2	
LANE3	

	FCH
LANE0	LAN
LANE1	~~WWAN~~
LANE2	WLAN
LANE3	~~CardReader~~

TYPE ENABLED	EC_PWM2	EC_PWM3
Reserved	2.2-kohm 5% pull-down	2.2-kohm 5% pull-down
LPC ROM	Not connected.	2.2-kohm 5% pull-down
SPI ROM	2.2-kohm 5% pull-down	Not connected.
Reserved	Not connected.	Not connected.

Note: EC_PWM2, EC_PWM3 default have internal 10kohm PU.

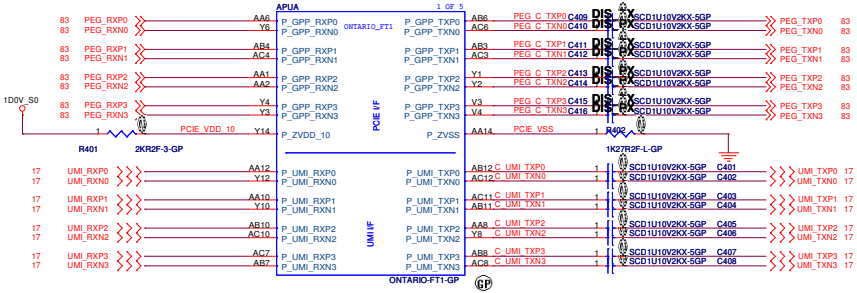
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Table of Content

Size: A3 | Document Number: B575 | Rev: -1

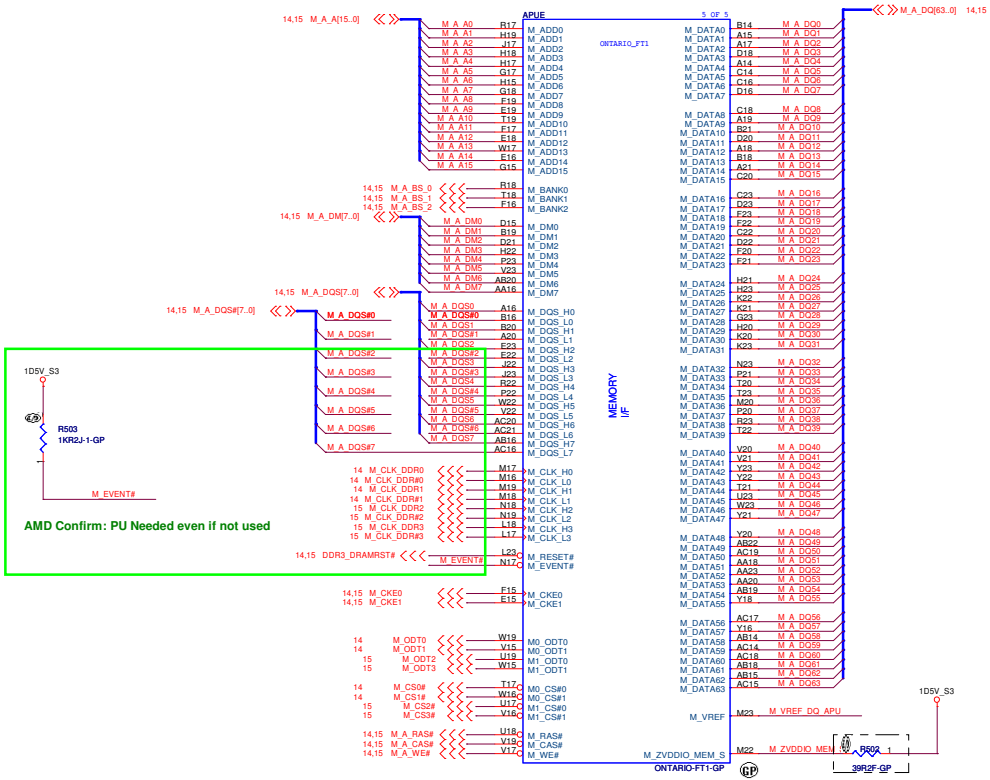
Date: Friday, March 25, 2011 | Sheet 3 of 102



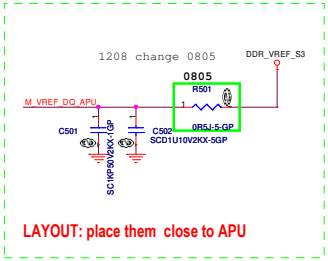
lenovo_PN_102-001093

<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**APU 1 of 5(UMI/PCIE)**	
Size A3	Document Number **B575**	Rev **-1**
Date: Monday, March 28, 2011	Sheet 4 of 103	

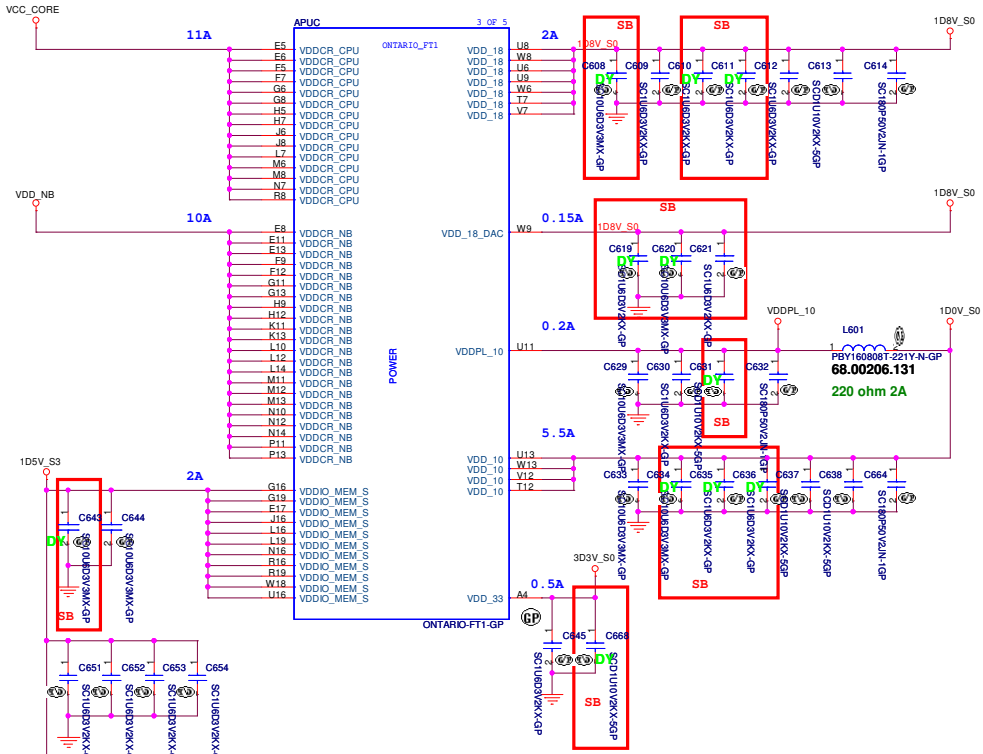


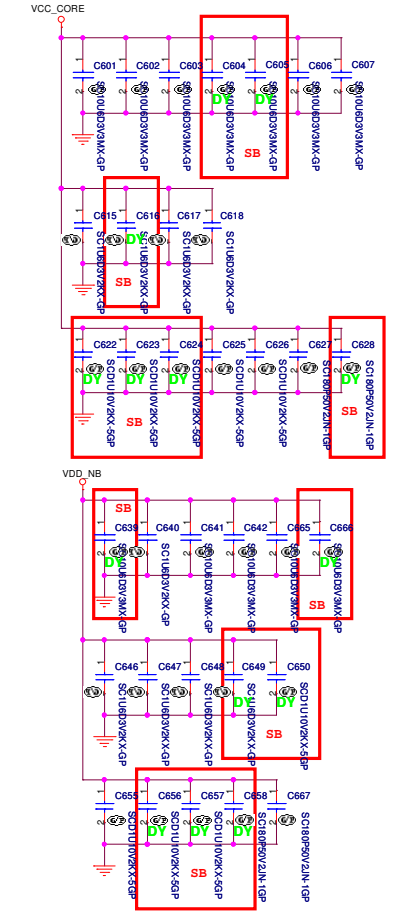
APU_VREF



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: APU 2 of 5(DDR)		
Size: A3	Document Number: B575	Rev: -1
Date: Monday, March 28, 2011	Sheet 5 of 103	





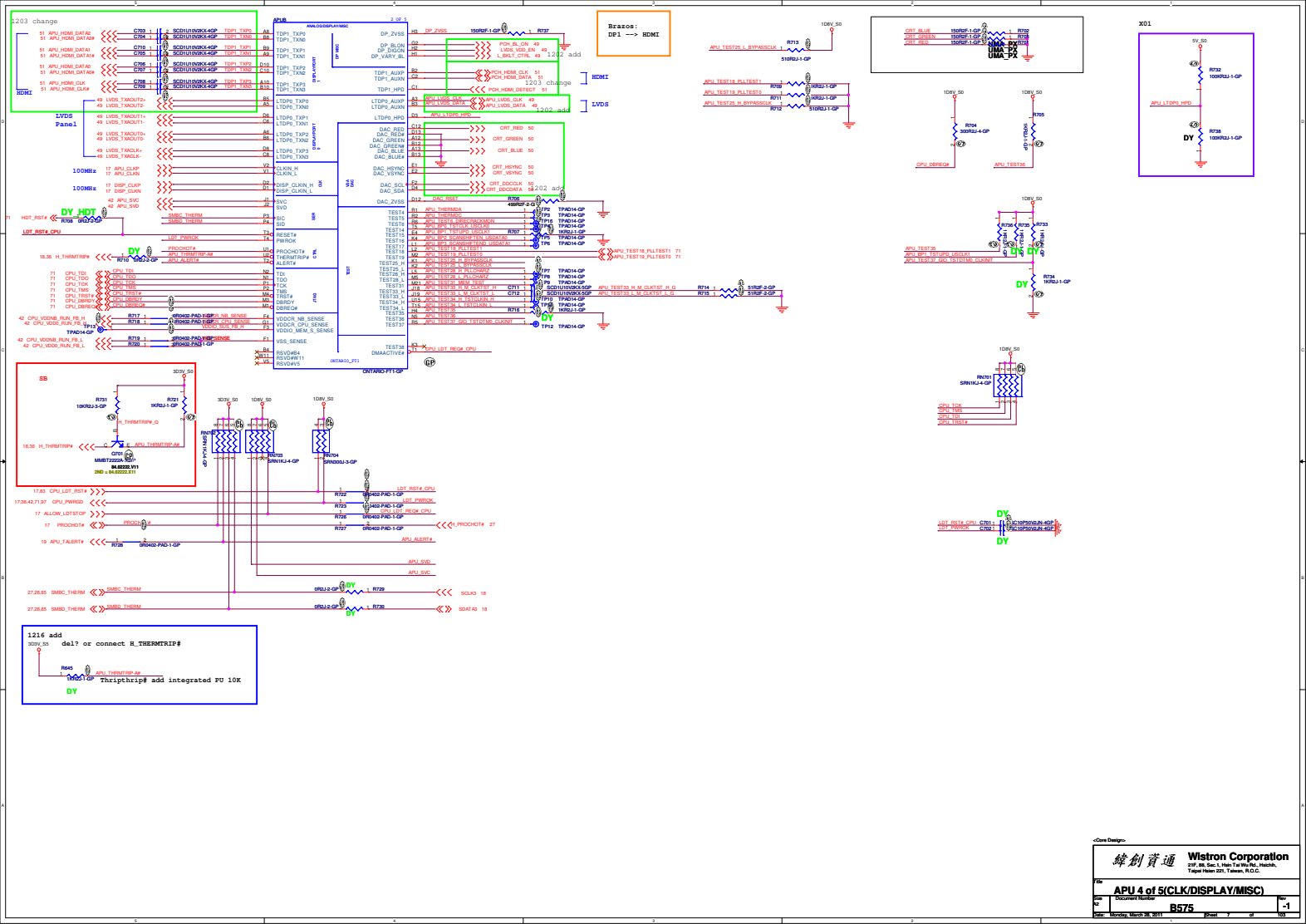
<Core Design>

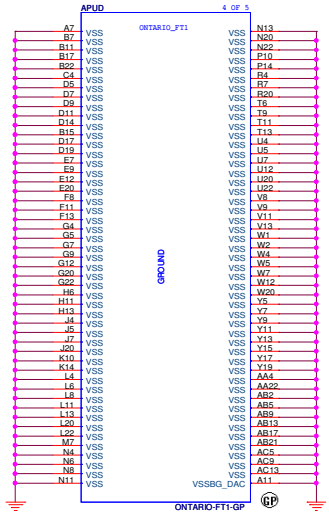
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: APU 3 of 5(POWER)

Size: Custom | Document Number: B575 | Rev: -1

Date: Friday, March 25, 2011 | Sheet 6 of 103


1203 change
HDMI
LVDS
Panel
100MHz
100MHz
DY_HDT
LDT_RST# _CPU
DY
TPAD14-GP
SB
1216 add
3DV_S5
del? or connect H_THERMTRIP#
Thriptrip# add integrated PU 10K
DY
Brazos:
DP1 --> HDMI
1202 add
1203 change
1202 add
1202 add
HDMI
LVDS
X01
5V_S0
APU 4 of 5(CLK/DISPLAY/MISC)
B575
Wistron Corporation
Taipei Hsien 221, Taiwan, R.O.C.
Monday, March 28, 2011



<Core Design>

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **APU 5 of 5(VSS)**

Size	Document Number	Rev
A3	B575	SA

Date: Friday, March 25, 2011 Sheet 8 of 103

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***G-Sensor***

Size	Document Number	Rev
	B575	SA

Date: Friday, March 25, 2011 Sheet 9 of 103

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
G-Sensor

Size	Document Number	Rev
	B575	SA

Date: Friday, March 25, 2011 Sheet 10 of 103

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***G-Sensor***

Size	Document Number	Rev
	B575	SA

Date: Friday, March 25, 2011 Sheet 11 of 103

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
G-Sensor

Size	Document Number	Rev
	B575	SA

Date: Friday, March 25, 2011 Sheet 12 of 103

<Core Design>

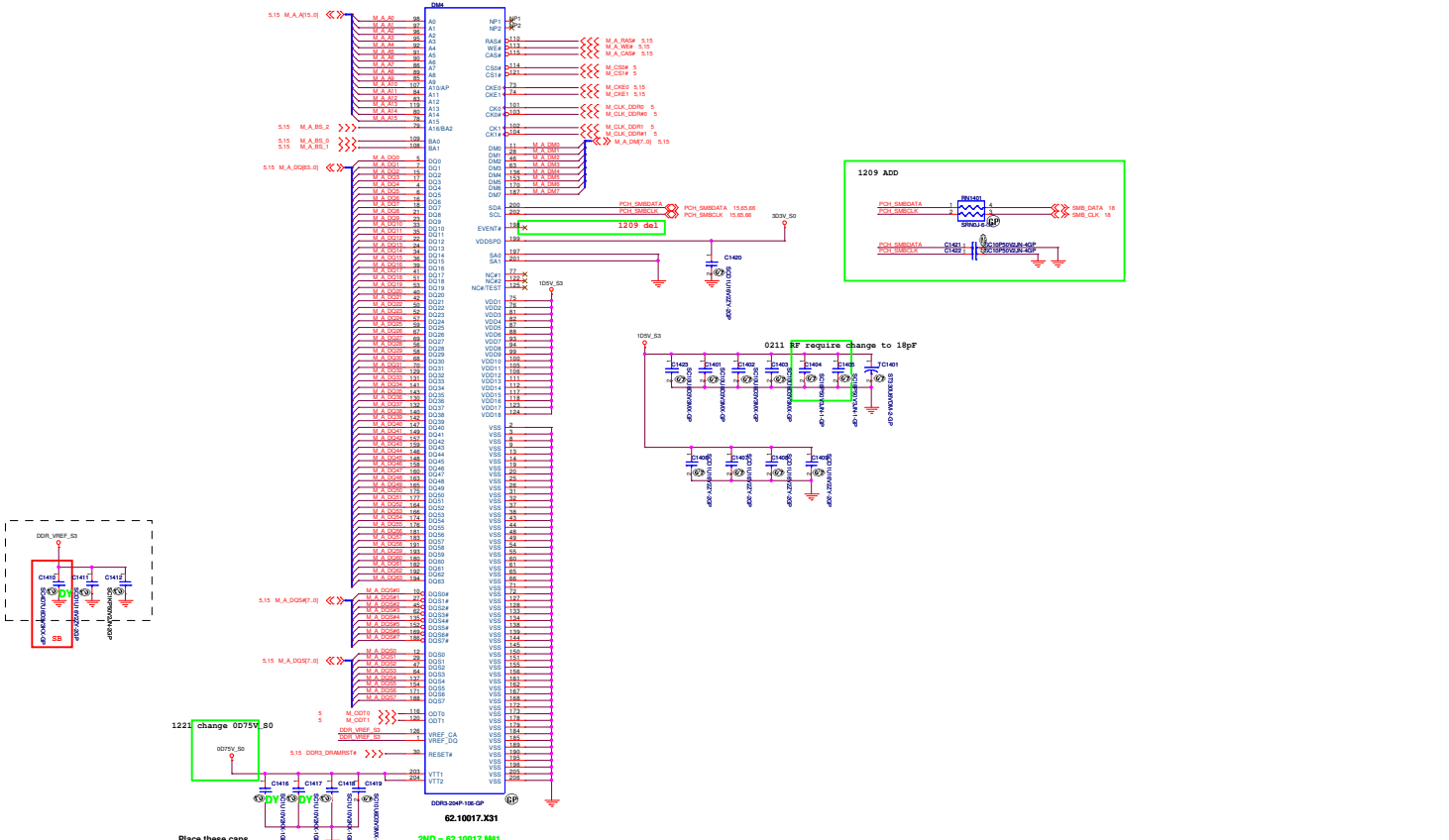
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***G-Sensor***

Size	Document Number	Rev
	B575	SA

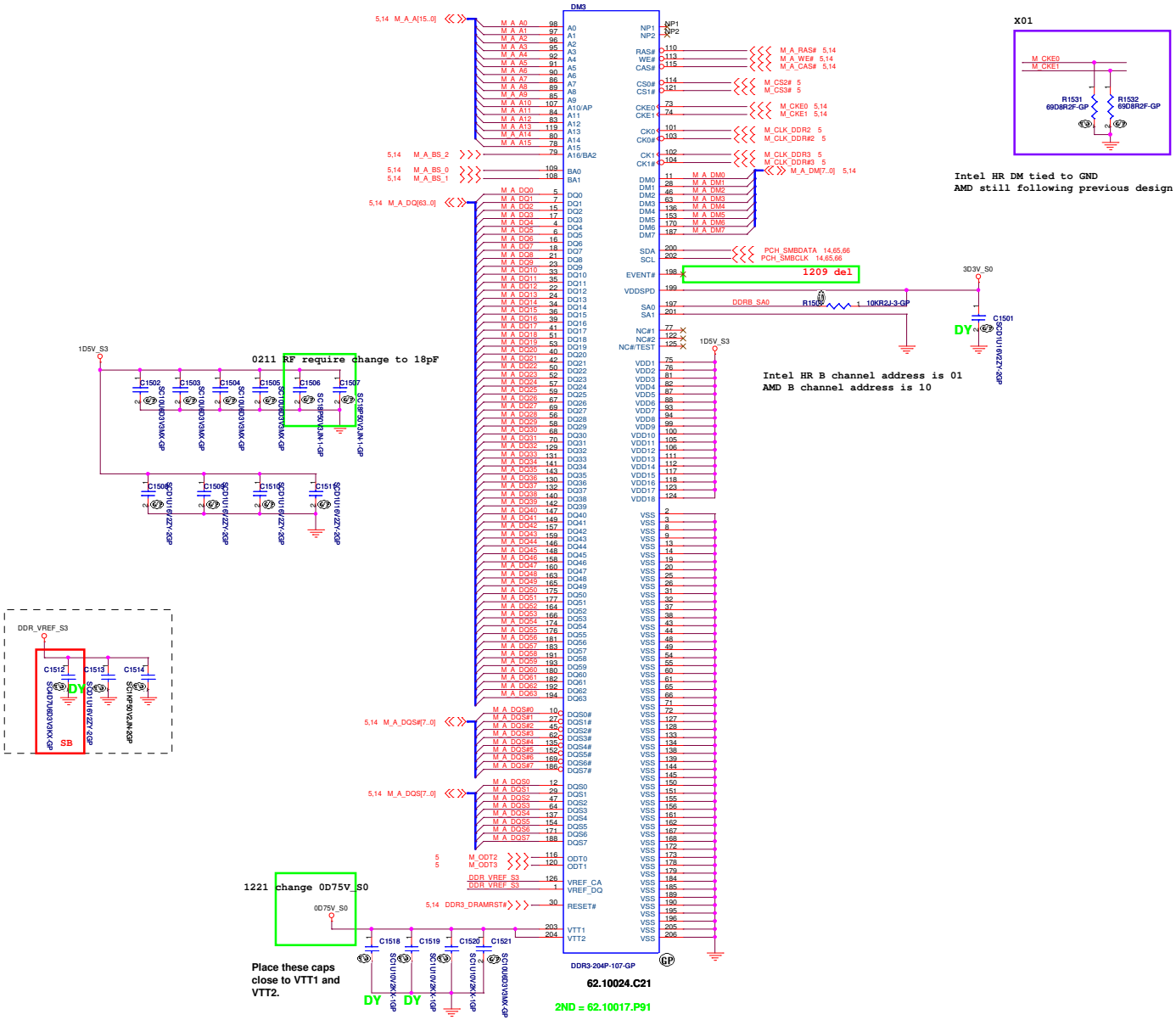
Date: Friday, March 25, 2011 Sheet 13 of 103

DDR3 SOCKET_1



緯創資通	Wistron Corporation		
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	DDR3 Socket1		
Size	Document Number		Rev
	B575		SA
Date: Monday, March 28, 2011		Sheet 14 of 103	

DDR3 SOCKET_2



緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	DDR3 Socket2		
Size	Document Number		Rev
	B575		SA
Date: Monday, March 28, 2011		Sheet 15 of 103	

緯創資通 **Wistron Corporation**

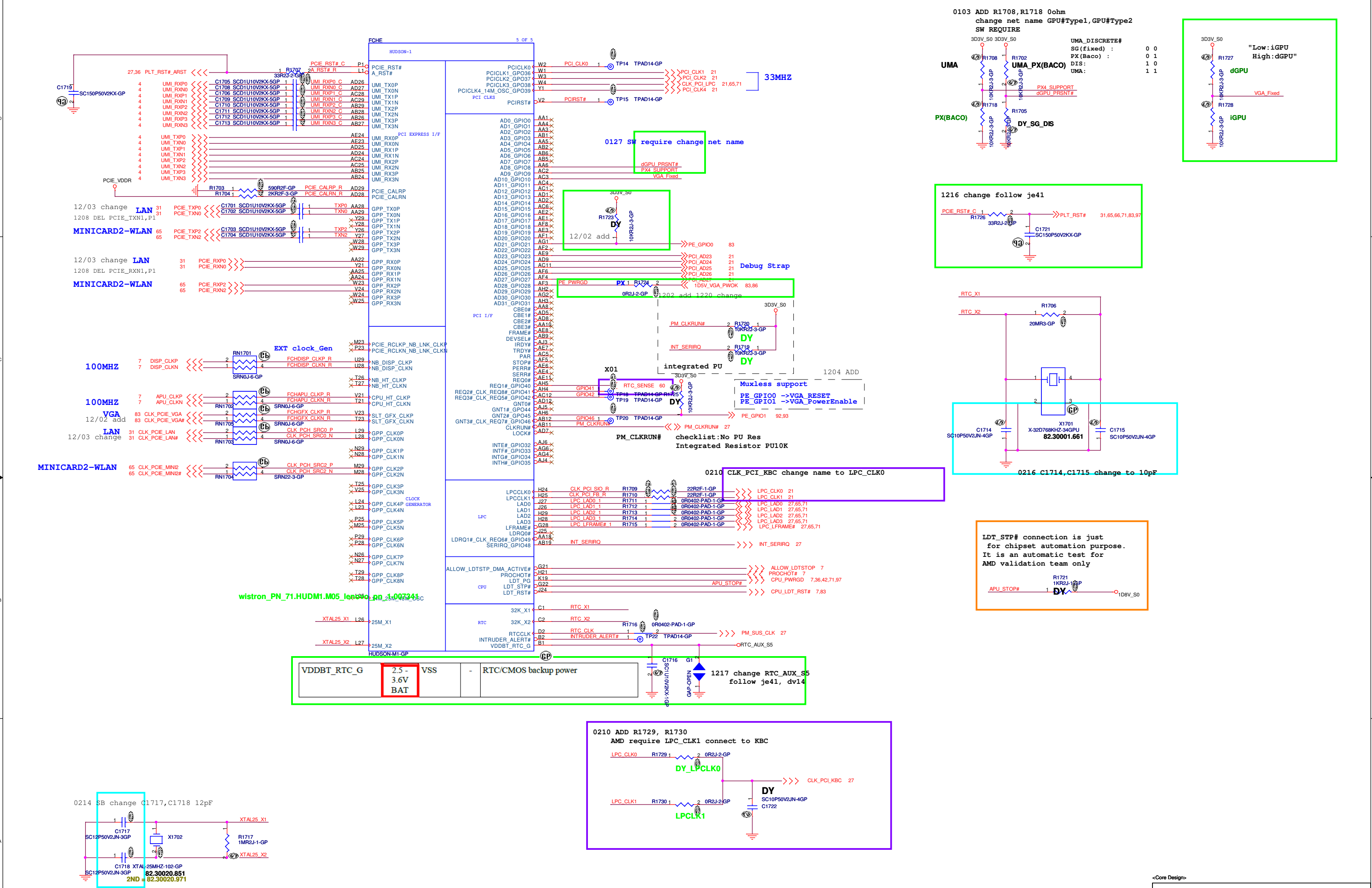
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

DDR3 Socket3

Size	Document Number	Rev
	B575	SA

Date: Friday, March 25, 2011 Sheet 16 of 103


0103 ADD R1708,R1718 0ohm
change net name GPU#Type1,GPU#Type2
SW REQUIRE
UMA_DISCRETE#
SG(fixed) : 0 0
PX(Baco) : 0 1
DIS: 1 0
UMA: 1 1
UMA
UMA_PX(BACO)
PX(BACO)
DY_SG_DIS
"Low:iGPU
High:dGPU"
dGPU
iGPU
VGA_Fixed
FCHE
HUDSON-1
5 OF 5
PCI EXPRESS I/F
PCI CLKS
33MHZ
0127 SW require change net name
dGPU_PRSNT#
PX4_SUPPORT
1216 change follow je41
PLT_RST#
12/02 add
12/03 change LAN
1208 DEL PCIE_TXN1,P1
MINICARD2-WLAN
1208 DEL PCIE_RXN1,P1
Debug Strap
PE_PWRGD
1202 add 1220 change
integrated PU
1204 ADD
Muxless support
PE_GPIO0 ->VGA_RESET
PE_GPIO1 ->VGA_PowerEnable
EXT clock_Gen
100MHZ
VGA
LAN
12/02 add
12/03 change
MINICARD2-WLAN
PM_CLKRUN#
checklist:No PU Res
Integrated Resistor PU10K
0210 CLK_PCI_KBC change name to LPC_CLK0
0216 C1714,C1715 change to 10pF
CLOCK GENERATOR
LPC
LDT_STP# connection is just for chipset automation purpose.
It is an automatic test for AMD validation team only
CPU
RTC
wistron_PN_71.HUDM1.M05_lenovo_pn_1.007241
VDDBT_RTC_G
2.5 - 3.6V BAT
VSS
RTC/CMOS backup power
1217 change RTC_AUX_S5
follow je41, dv14
0210 ADD R1729, R1730
AMD require LPC_CLK1 connect to KBC
DY_LPCLK0
LPCLK1
CLK_PCI_KBC
0214 SB change C1717,C1718 12pF
XTAL-25MHZ-102-GP
82.30020.851
2ND = 82.30020.971

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	FCH 1 of 6(UMI/CLK/RTC/LPC)
Size A2	Document Number B575
Rev	SA
Date:	Sunday, March 27, 2011
Sheet	17 of 103

1209 ADD USB_OC#0
E-SATA / USB

Sandra: Dummy
Standard: AMD recommand external PU

1208 DEL WWAN_CLKREQ#

1205 ADD
DV14 ON, JE41 DY

0318 ADD R1821 DY

0106 EMI ADD ER1810 NEAR PCH

1208 DEL PCIE_CLK_RQ1#

0214 SB ADD R1820 10Kohm PD

Sandra: 1K ohm
Standard: 0 ohm

Sandra: Mount

229 change to USB1.1

USB 1.0 Table

Pair	Device
0	Finger Print
1	NC

USB 2.0 Table

Pair	Device
0	Internal #3(MB)
1	WLAN/WiMAX
2	WWAN
3	E-SATS/LUSB
4	BLUETOOTH
5	External #1(LAN BD)
6	External #2(IO BD)
7	CAMERA(HS)
8	NC
9	CardReader
10	NC
11	NC
12	NC
13	NC

1229 SCLK2, SDATA2 PD 10K
follow dv14

SCLK2, SDATA2 if not used SMBUS or GPIO ,PD 10K

Function	Name	Integrated Resistor	External Resistor	
GA20IN	KA20GATE	8.2K PU	8.2K PU 3.3_S0	
KBRST#	KBRCIN#	8.2K PU	10K PU 3.3_S0	
PME#	EC_SCI#	10K PU	10K PU 3.3_S5	
THRIPTRIP#	PM_THRMTRIP-A#	10K PU	10K PU 3.3_S5	
PCIE_RST2#	PCH_PCIE_RST#	10K PU		?
Gevent5	MEM_Hot#	10K PU		?
Gevent6	EC_SWI#	10K PU	10K PU 3.3_S5	
WAKE#	PCIE_WAKE#	10K PU	10K PU 3.3_S5	
USB_OC0#	USB_OC#0	10K PU		
USB_OC1#	USB_OC#1	10K PU		
USB_OC2#	USB_OC#2	10K PU		
Gevent15#	USB_OC#3	10K PU		
Gevent16#	USB_OC#4	10K PU		
USB_OC5#	USB_OC#5	10K PU		
USB_OC7#	USB_OC#7	10K PU		
IPC_SMI#	EC_SMI#	8.2K PU	10K PU 3.3_S0	
SERIRQ	INT_SERIRQ	8.2K PU	10K PU 3.3_S0	DY
CLK_REQ0	CLK_PCIE_NEW_REQ#	8.2K PU		
CLK_REQ1	CLK_PCIE_WLAN_REQ#	8.2K PU		
CLK_REQ2	CLK_PCIE_WWAN_REQ#	8.2K PU		
CLK_REQ3	PCIE_CLK_LAN_RQ1#	8.2K PU		
CLK_REQG	PEG_CLKREQ#	8.2K PU		

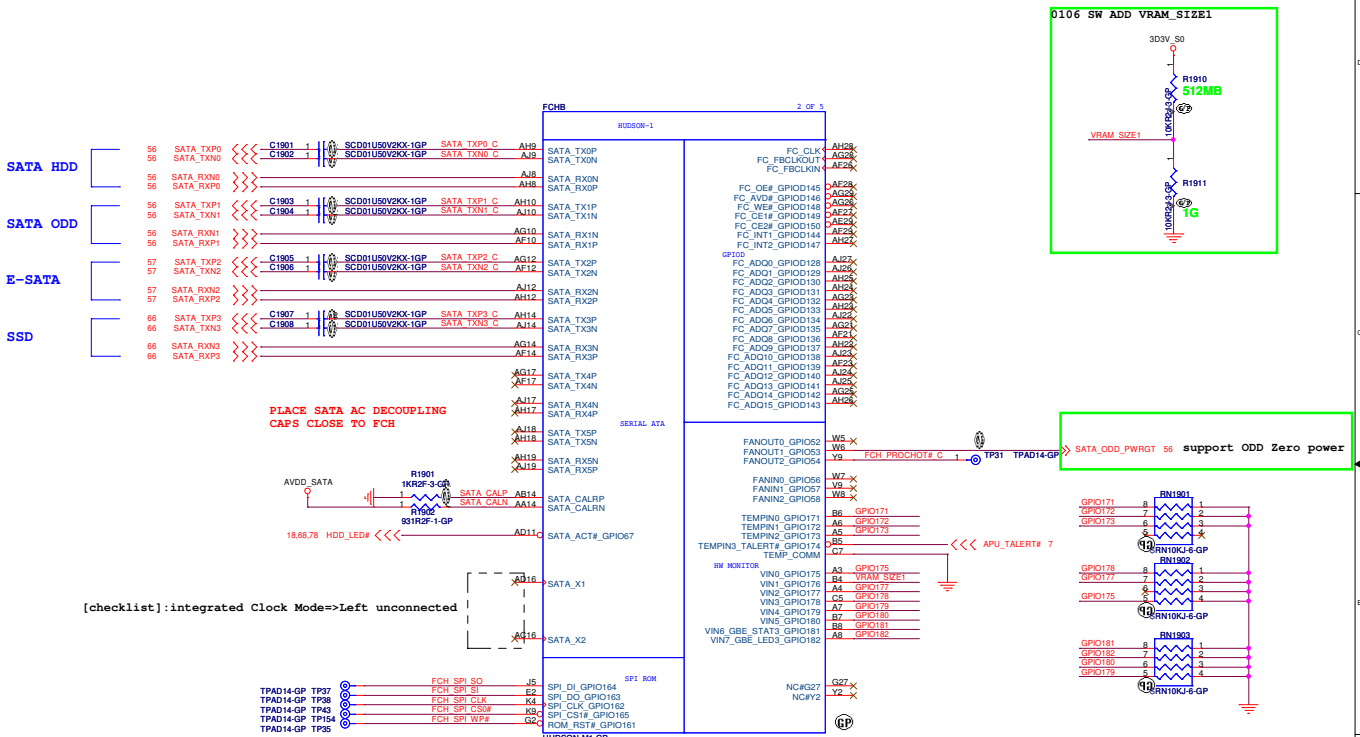
DVT 1ST

Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

FCH 2 of 6(USB/HDA/GPIO)

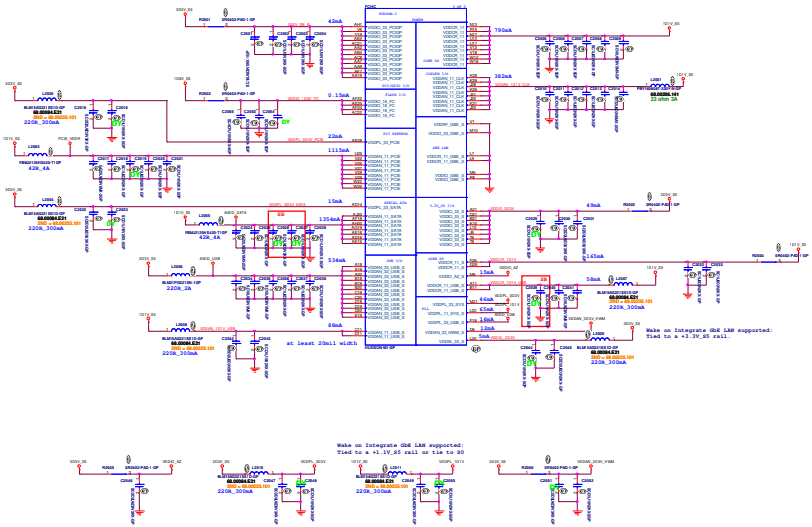
Size: A2 | Document Number: B575 | Rev: SA

Date: Monday, March 28, 2011 | Sheet 18 of 103



DVT 1ST

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	FCH 2 of 6(USB/HDA/GPIO)	
Size: A3	Document Number: B575	Rev: SA
Date: Monday, March 28, 2011	Sheet 19 of 103	



Wistron Corporation
8F, No. 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

FCH 4 of 6(PWR)

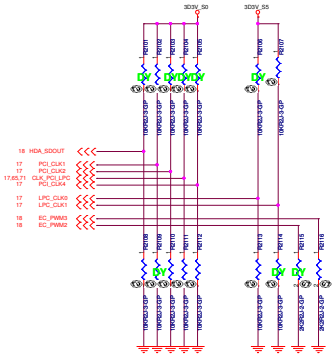
B575

8A

SSID = S.B

REQUIRED STRAPS

CRB:PU 3.3V_AUX_S5
checklist:PU 3.3V_S5
confirm by AMD,following CRB suggestion



REQUIRED SYSTEM STRAPS

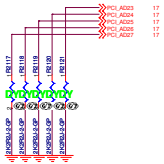
	AZ_SDOUT (ACZ_SDATAOUT_1)	PCI_CLK1	PCI_CLK2	PCI_CLK3 (CLK_PCI_LPC)	PCI_CLK4	LPC_CLK0	LPC_CLK1
PULL HIGH	Low Power Mode	Allow PCIE GEN2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAPS	non_Fusion CLOCK mode	ENABLE EC	CLKGEN ENABLED (Use Internal) DEFAULT
PULL LOW	Performance Mode DEFAULT	Force PCIE GEN1	Watchdog Timer Disabled DEFAULT	iGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode DEFAULT	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External)

USE this pin to determine INT/EXT CLK

TYPE ENABLED	EC_PWM2	EC_PWM3
Reserved	2.2-kohm 5% pull-down	2.2-kohm 5% pull-down
LPC ROM	Not connected.	2.2-kohm 5% pull-down
SPI ROM	2.2-kohm 5% pull-down	Not connected.
Reserved	Not connected.	Not connected.

Note: EC_PWM2, EC_PWM3 default have internal 10kohm PU.

DEBUG STRAPS



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL (DEFAULT)	Disable ILA AUTORUN (DEFAULT)	USE FC PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Disable PCI MEM BOOT (DEFAULT)
PULL LOW	BYPASS PCI PLL	Enable ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	Enable PCI MEM BOOT

Note: FCH has 15K internal PU FOR PCI_AD[27:23]

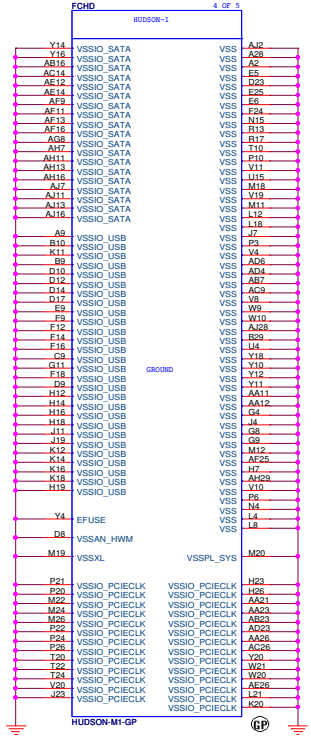
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: FCH 5 of 6(STRAPPINGS)

Size: A2 | Document Number: B575 | Rev: SA

Date: Monday, March 28, 2011 | Sheet 21 of 103



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **FCH 6 of 6(VSS)**

Size	Document Number	Rev
A3	B575	SA

Date: Friday, March 25, 2011 Sheet 22 of 103

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***G-Sensor***

Size	Document Number	Rev
	B575	SA

Date: Friday, March 25, 2011 Sheet 23 of 103

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
G-Sensor

Size	Document Number	Rev
	B575	SA

Date: Friday, March 25, 2011 Sheet 24 of 103

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
G-Sensor

Size	Document Number	Rev
	B575	SA

Date: Friday, March 25, 2011 Sheet 25 of 103

blanking

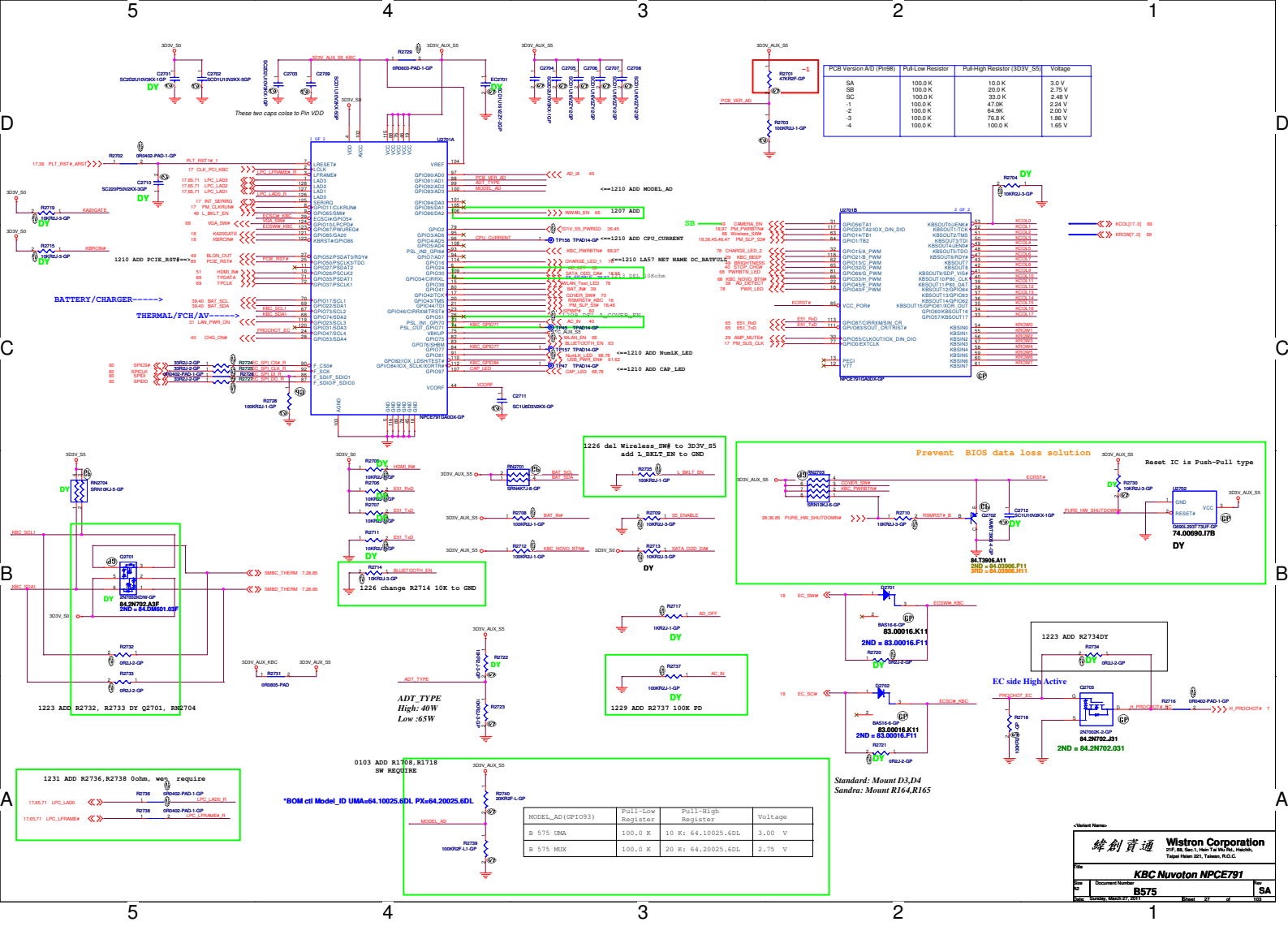
<Core Design>

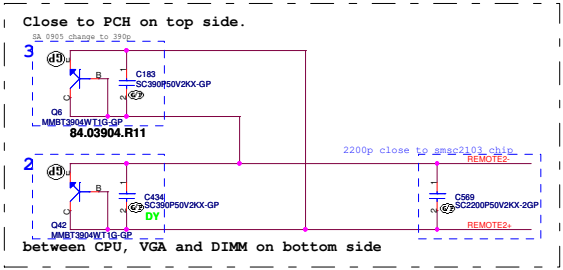
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

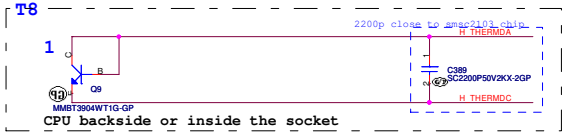
Title: Power Button

Size	Document Number	Rev
A3	B575	SA

Date: Friday, March 25, 2011 Sheet 26 of 103


PCB Version A/D (Pin98) | Pull-Low Resistor | Pull-High Resistor (3D3V_S5) | Voltage
SA | 100.0 K | 10.0 K | 3.0 V
SB | 100.0 K | 20.0 K | 2.75 V
SC | 100.0 K | 33.0 K | 2.48 V
-1 | 100.0 K | 47.0K | 2.24 V
-2 | 100.0 K | 64.9K | 2.00 V
-3 | 100.0 K | 76.8 K | 1.86 V
-4 | 100.0 K | 100.0 K | 1.65 V
These two caps colse to Pin VDD
1210 ADD PCIE_RST#==>
BATTERY/CHARGER
THERMAL/FCH/AV
<=1210 ADD MODEL_AD
1207 ADD
<=1210 ADD CPU_CURRENT
<=1210 LA57 NET NAME DC_BATFULL
<=1210 ADD NumLK_LED
<=1210 ADD CAP_LED
1226 del Wireless_SW# to 3D3V_S5
add L_SKLT_EN to GND
1226 change R2714 10K to GND
Prevent BIOS data loss solution
Reset IC is Push-Pull type
ADT_TYPE
High: 40W
Low :65W
1223 ADD R2732, R2733 DY Q2701, RN2704
1223 ADD R2734DY
EC side High Active
1229 ADD R2737 100K PD
1231 ADD R2736,R2738 0ohm, wen require
0103 ADD R1708,R1718
SW REQUIRE
*BOM ctl Model_ID UMA=64.10025.6DL PX=64.20025.6DL
Standard: Mount D3,D4
Sandra: Mount R164,R165
MODEL_AD(GPIO93) | Pull-Low Register | Pull-High Register | Voltage
B 575 UMA | 100.0 K | 10 K: 64.10025.6DL | 3.00 V
B 575 MUX | 100.0 K | 20 K: 64.20025.6DL | 2.75 V
Wistron Corporation
KBC Nuvoton NPCE791
B575
SA
Sunday, March 27, 2011

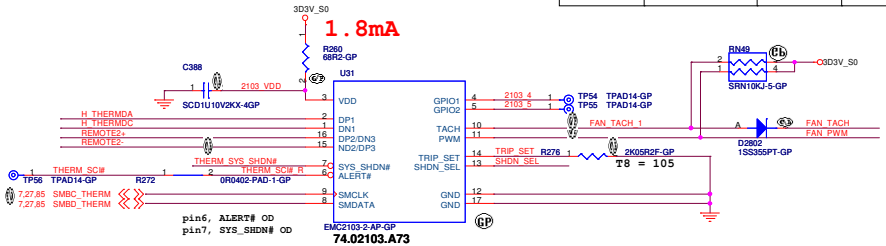


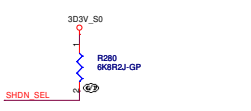


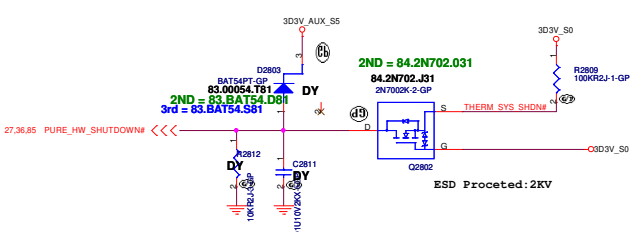
CPU TEMP:
H_THERMDA and H_THERMDC routing 10mil trace width and spacing. Locate Capacity near Thermal diode.

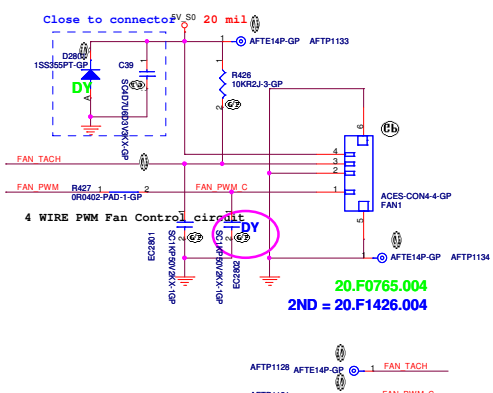
Table 28.1- General Purpose Transistors multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
ON	MMBT3904WT1G	N/A	84.03904.R11
PANJIT	MMBT3904W	N/A	84.M3904.A11









1210 10886-1 D1/D2/R15/R16/C15 DY
EC1/EC2/EC3 100pF
R17/R18 100ohm
C17/C18 100pF
R23/R24 100pF
BOM Control

Layout Note: Path from +5V to LPWR_5.0 and RPWR_5.0 must be very low resistance (<0.01 ohms). Place bypass caps very close to device.

Port Configuration

Port A: Headphone jack
Port B:
Port C: Microphone jack
Port G: Internal stereo speakers
Port J: Internal stereo digital mic

Place these EMI components close to speaker connector.

Only needed if speaker connector is physically far from audio codec. When in doubt, it's always a good idea to have population option.

1210 ADD 5.1 ohm

Please see Design Guide for audio grounding.

1209 ADD 2pcs 0805 short pad

place them under CODEC bottom

Place EMI components close to audio codec.

<Core Design>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Codec	
Size	Document Number: B575	Rev: SA
Date: Monday, March 28, 2011	Sheet 29 of 103	

blanking

LA57 UMA

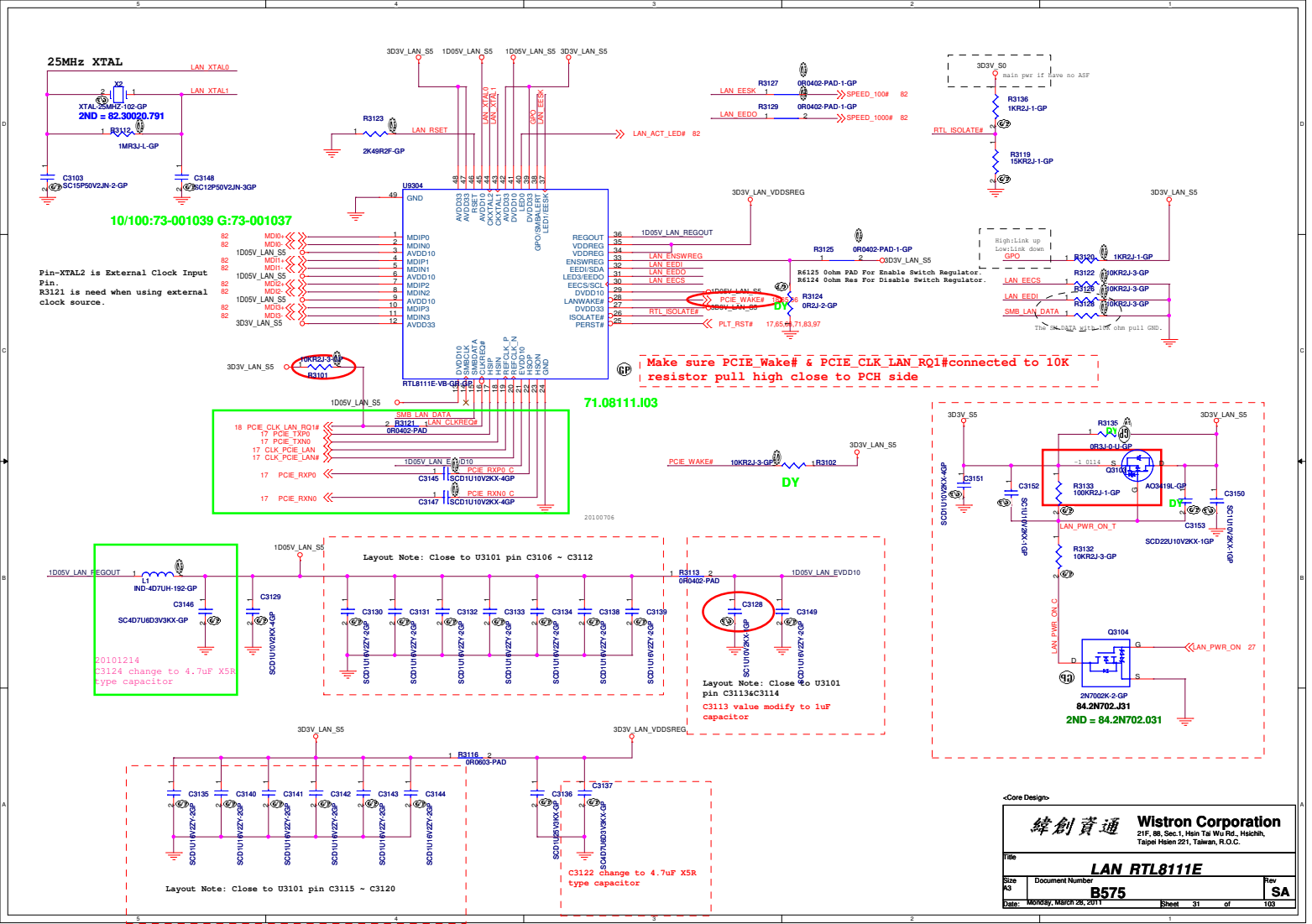
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

reserved

Size	Document Number	Rev
A4	B575	SA

Date: Friday, March 25, 2011 Sheet 30 of 103



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	LAN_RTL8111E	
Size: A3	Document Number: B575	Rev: SA
Date: Monday, March 28, 2011	Sheet 31 of 103	

<Core Design>

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

RTS5159 (CARD READER)

Size	Document Number	Rev
A3	**B575**	**SA**

Date: Friday, March 25, 2011 Sheet 32 of 103

(Blanking)

<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***Reserved***
Size: A4	Document Number: **B575**
Rev: **SA**	
Date: Friday, March 25, 2011	Sheet 33 of 103

(Blanking)

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	B575	SA

Date: Friday, March 25, 2011 Sheet 34 of 103

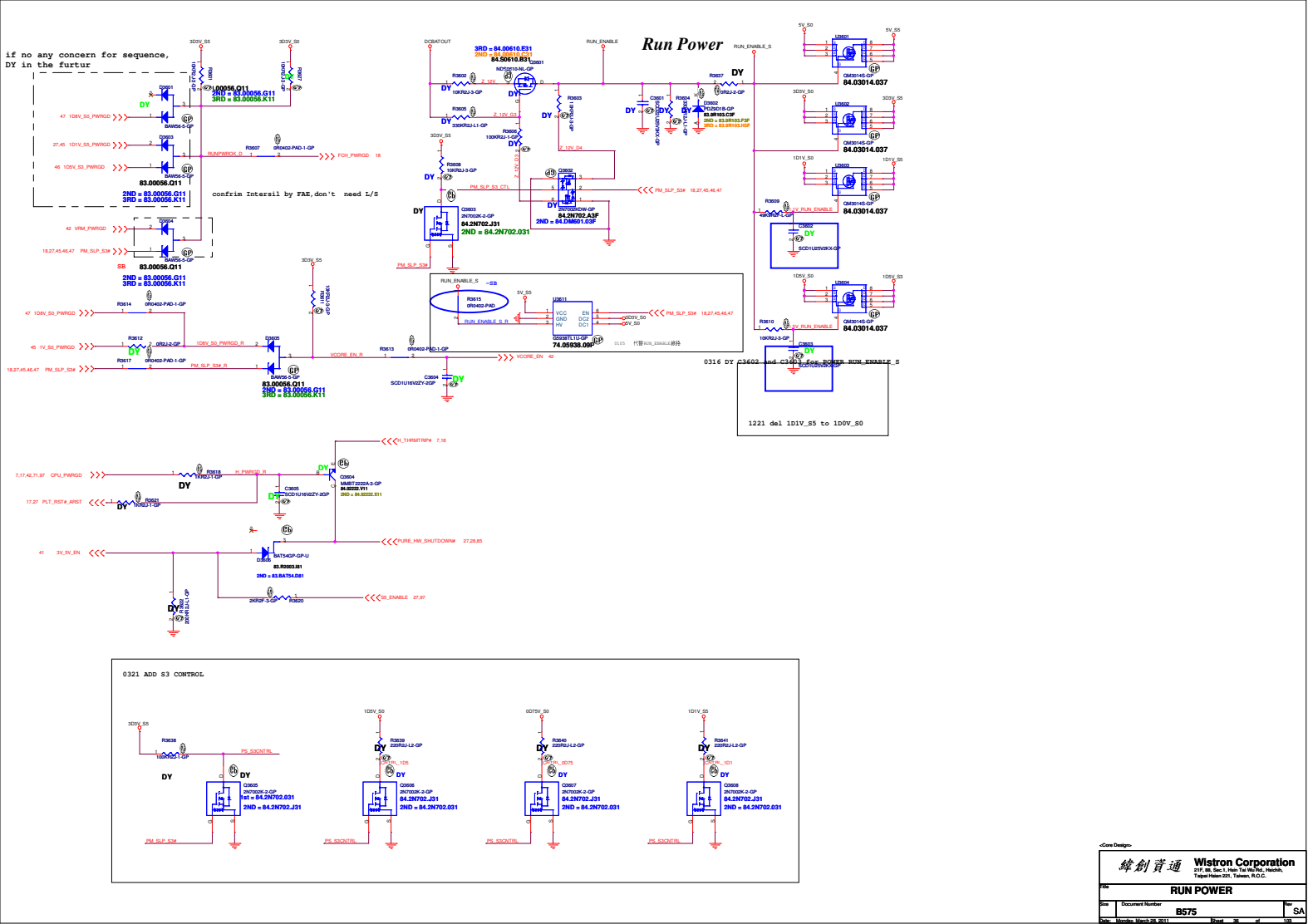
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB3.0***

Size	Document Number	Rev
Custom	B575	SA

Date: Friday, March 25, 2011 Sheet 35 of 103


Run Power
if no any concern for sequence,
DY in the furtur
confrim Intersil by FAE,don't need L/S
0316 DY C3602 and C3603 for POWER_RUN_ENABLE_S
1221 del 1D1V_S5 to 1D0V_S0
0321 ADD S3 CONTROL
Wistron Corporation
RUN POWER
B575

<Core Design>

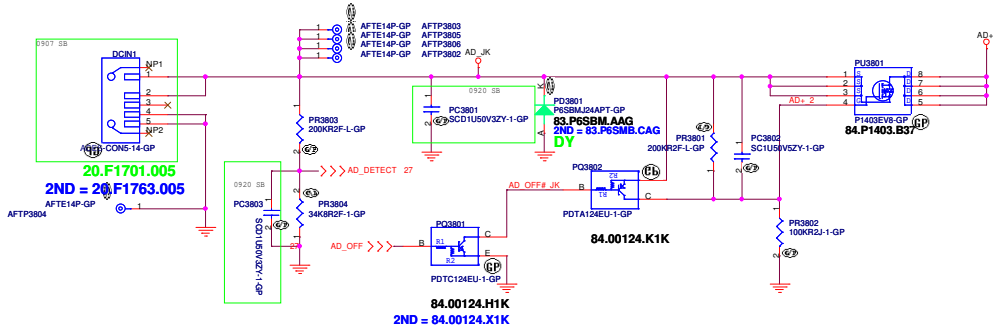
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***G-Sensor***

Size	Document Number	Rev
	B575	SA

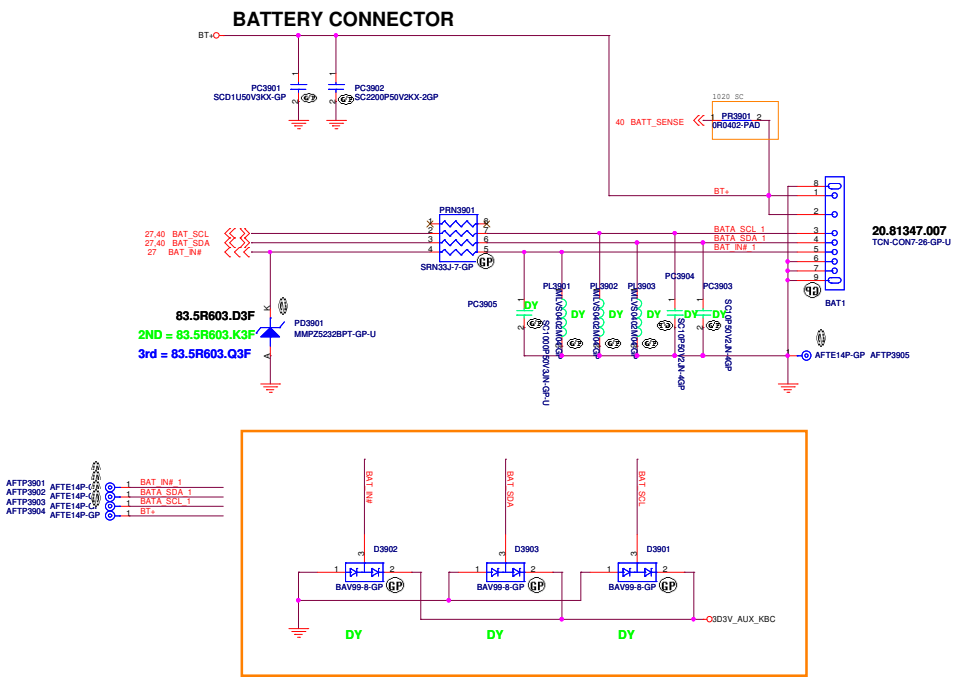
Date: Friday, March 25, 2011 Sheet 37 of 103

Adaptor in to generate DCBATOUT



JV10-CS

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***DCIN_JACK***	
Size	Document Number	Rev SA
Date: Monday, March 28, 2011	Sheet 38 of 103	



<Core Design>

緯創資通 **Wistron Corporation**

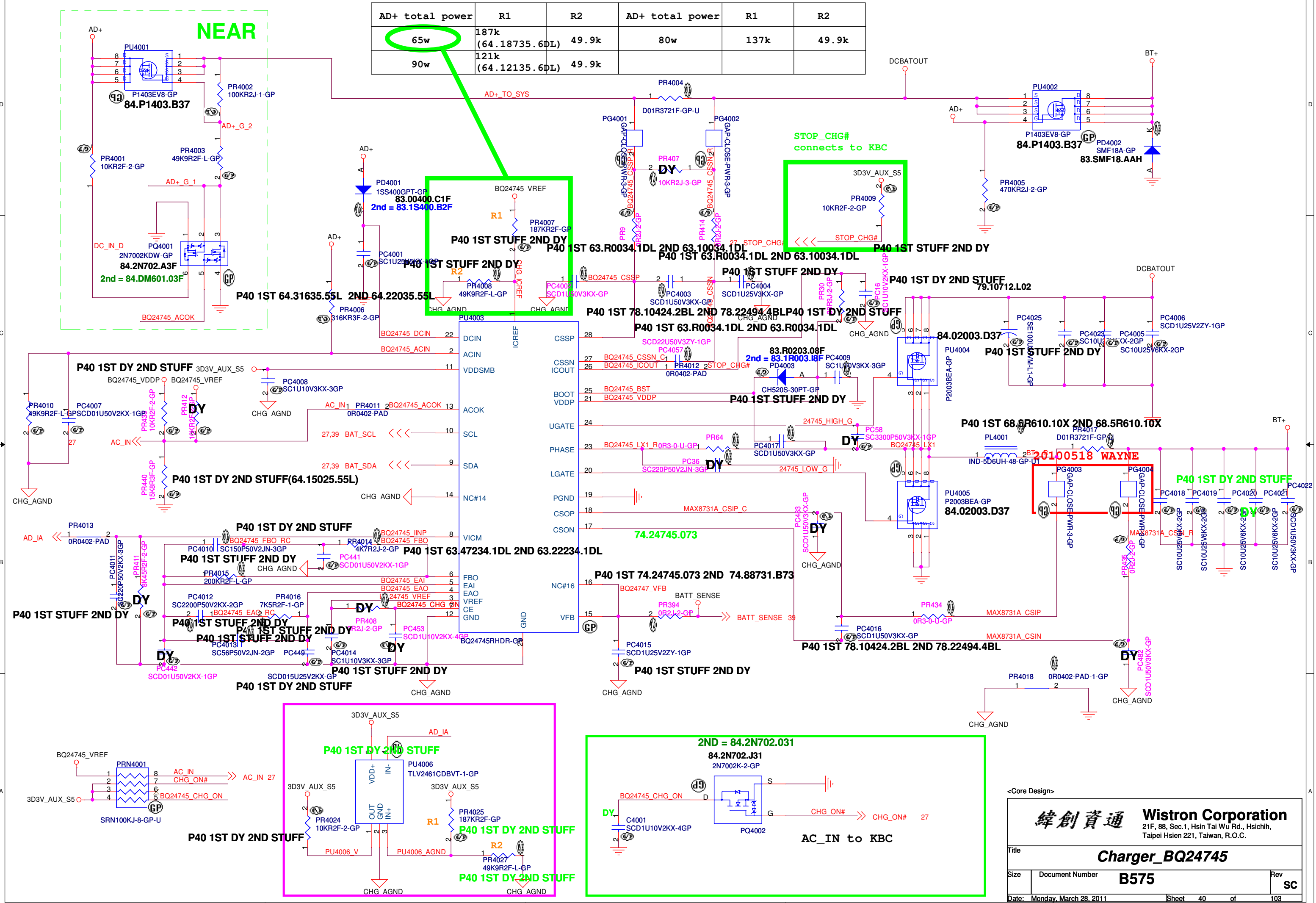
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AD / BATT CONN**

Size	Document Number	Rev
A3	B575	SA

Date: Monday, March 28, 2011 Sheet 39 of 103

AD+ total power	R1	R2	AD+ total power	R1	R2
65w	187k (64.18735.6DL)	49.9k	80w	137k	49.9k
90w	121k (64.12135.6DL)	49.9k			



<Core Design>

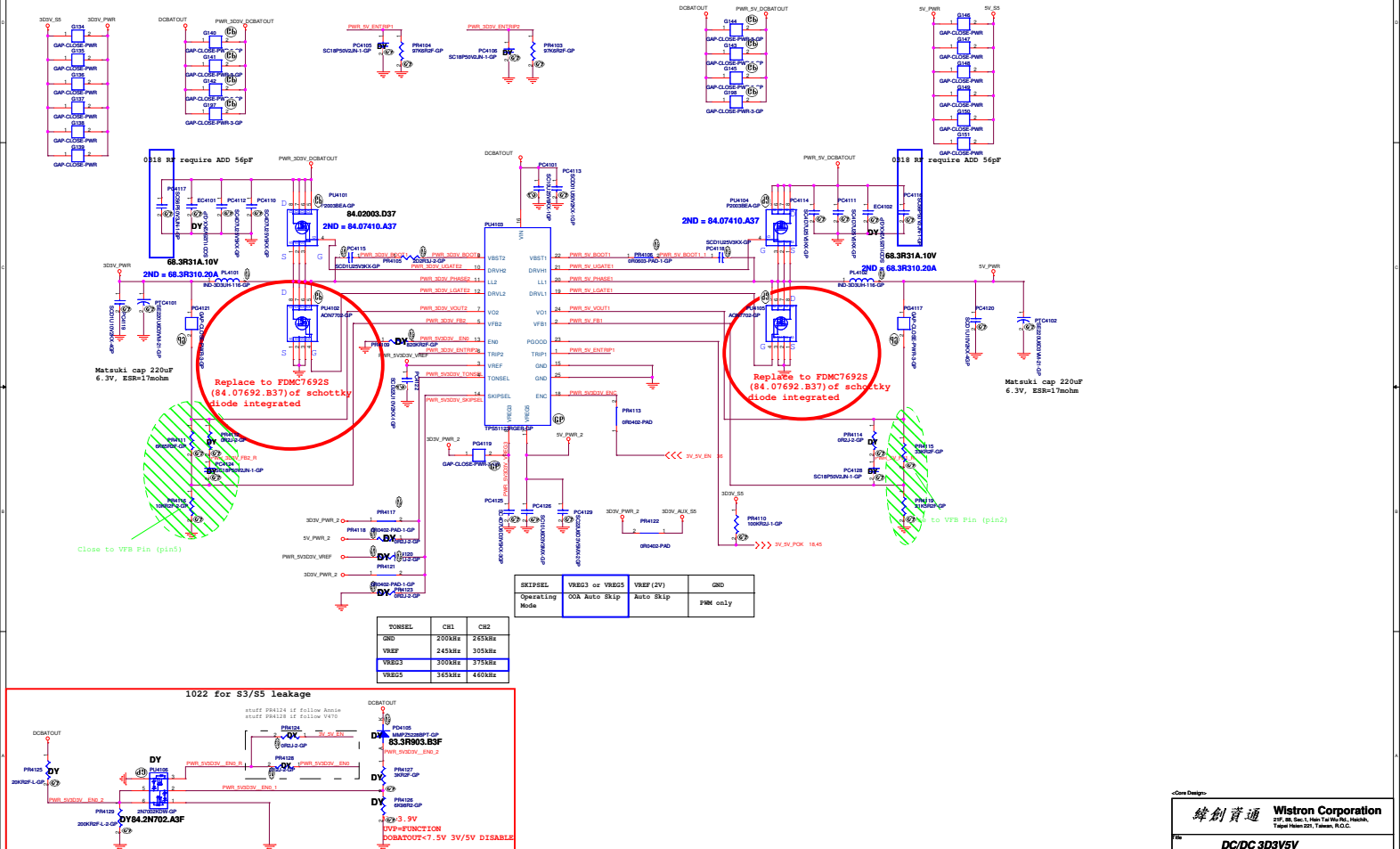
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Charger_BQ24745**

Size | Document Number: **B575** | Rev: SC

Date: Monday, March 28, 2011 | Sheet 40 of 103

SSID = PWR.Plane.Regulator_5v3p3v



SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

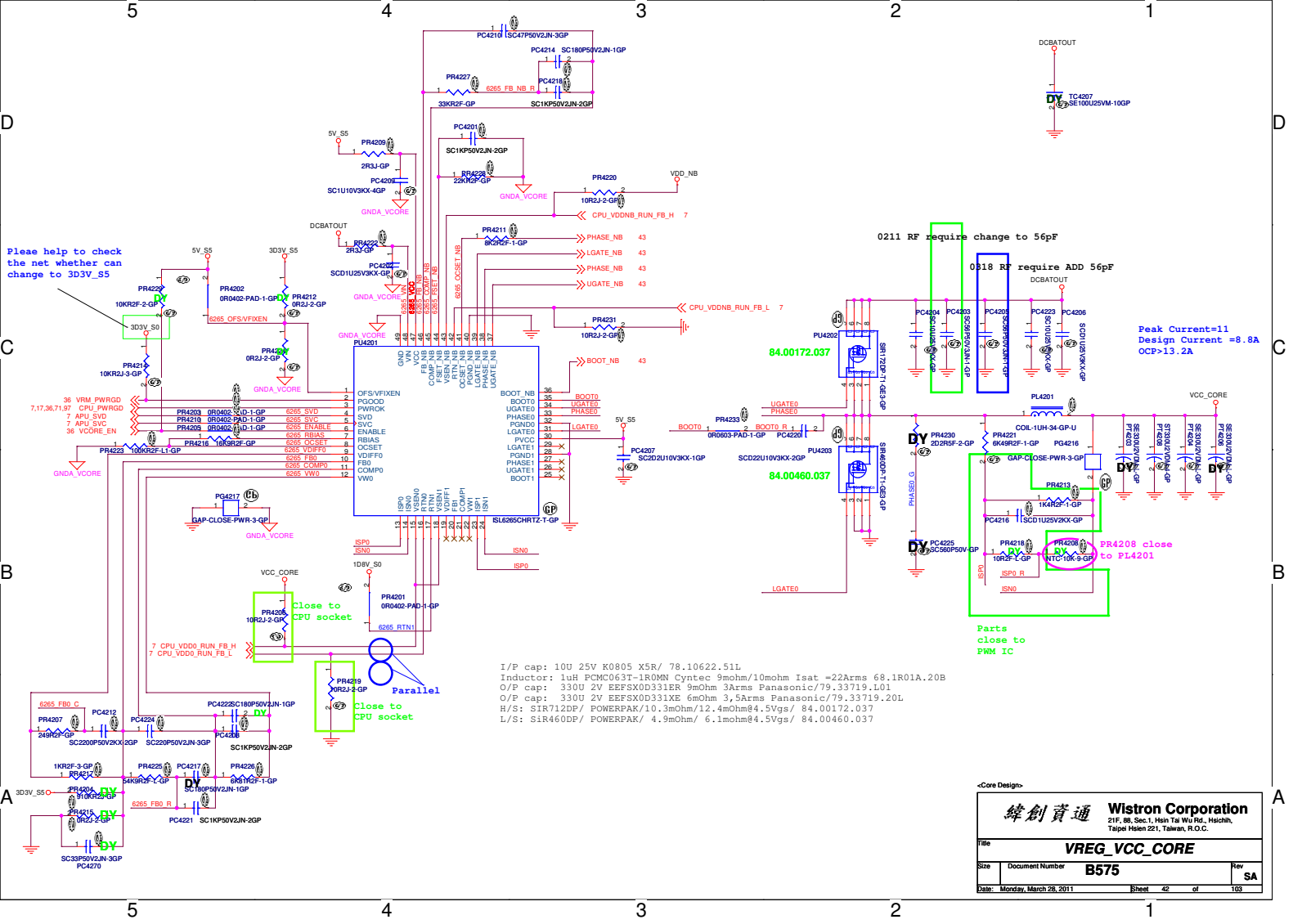
TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

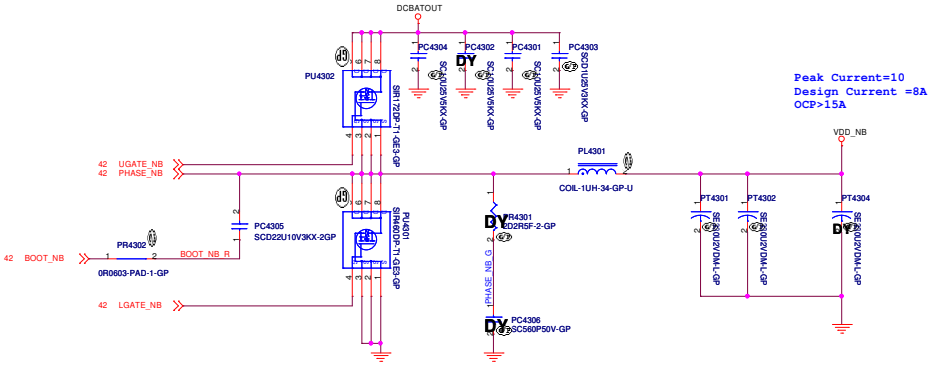
<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC/DC 3D3V5V

Size	Document Number	Rev
	B575	SA

Date: Monday, March 28, 2011 Sheet 41 of 103


Pleae help to check the net whether can change to 3D3V_S5
0211 RF require change to 56pF
0318 RF require ADD 56pF
Peak Current=11
Design Current =8.8A
OCP>13.2A
84.00172.037
84.00460.037
PR4208 close to PL4201
Parts close to PWM IC
Close to CPU socket
Close to CPU socket
Parallel
I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 1uH PCMC063T-1R0MN Cyntec 9mohm/10mohm Isat =22Arms 68.1R01A.20B
O/P cap: 330U 2V EEFSXOD331ER 9mOhm 3Arms Panasonic/79.33719.L01
O/P cap: 330U 2V EEFSXOD331XE 6mOhm 3,5Arms Panasonic/79.33719.20L
H/S: SIR712DP/ POWERPAK/10.3mOhm/12.4mOhm@4.5Vgs/ 84.00172.037
L/S: SiR460DP/ POWERPAK/ 4.9mOhm/ 6.1mohm@4.5Vgs/ 84.00460.037
ISL6265CHRTZ-T-GP
SIR712DP-T1-GE3-GP
SIR460DP-T1-GE3-GP
COIL-1UH-34-GP-U
GAP-CLOSE-PWR-3-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
VREG_VCC_CORE
B575
Monday, March 28, 2011
42
103



I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 1uH PCMC063T-1R0MN Cyntec 9mohm/10mohm Isat =22Arms 68.1R01A.20B
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3Arms Panasonic/79.33719.L01
H/S: SIR712DP/ POWERPAK/10.3mOhm/12.4mOhm@4.5Vgs/ 84.00172.037
L/S: SiR460DP/ POWERPAK/ 4.9mOhm/ 6.1mohm@4.5Vgs/ 84.00460.037

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

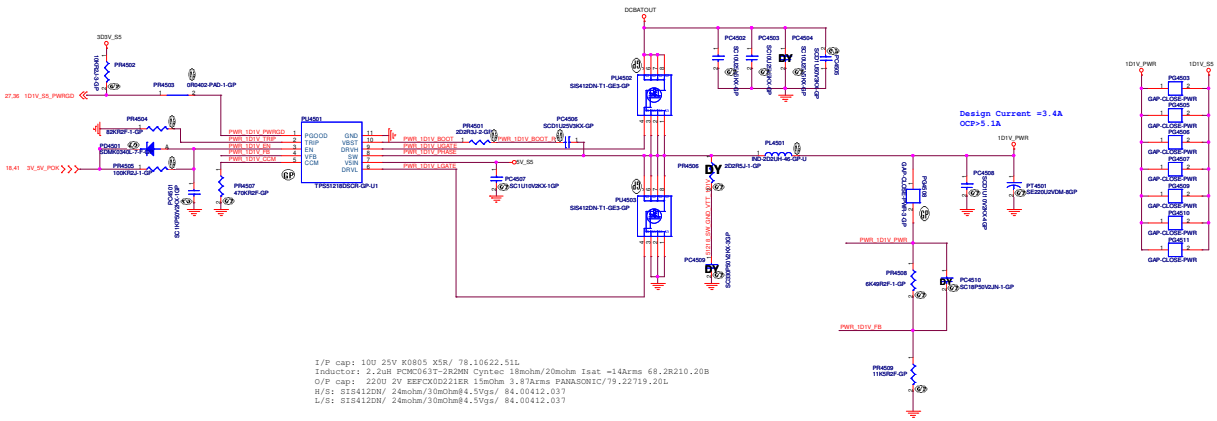
Title	VREG_VDDNB		
Size	Document Number B575		Rev SA
Date: Monday, March 28, 2011	Sheet 43 of 103		

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Size	Document Number	Rev
	B575	SA
Date: Friday, March 25, 2011	Sheet 44 of 103	

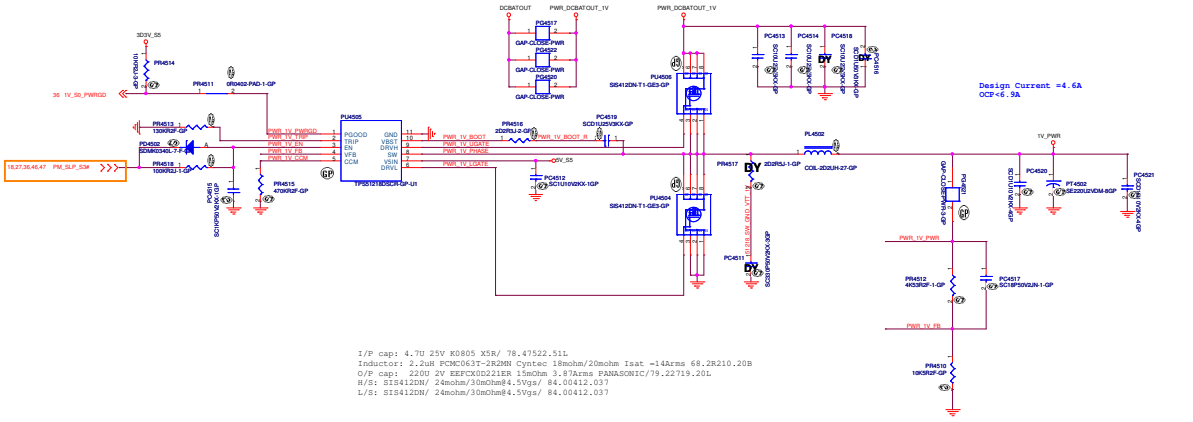
SSID = PWR.Plane.Regulator_1D1V_S5



Design Current =3.4A
OCP>5.1A

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 2.2uH PCMC063T-2R2MN Cyntec 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P cap: 220U 2V EEFCX0D221ER 15mOhm 3.87Arms PANASONIC/79.22719.20L
H/S: SIS412DN/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S: SIS412DN/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037

Vout=0.704V*(R1+R2)/R2



Design Current =4.6A
OCP<6.9A

I/P cap: 4.7U 25V K0805 X5R/ 78.47522.51L
Inductor: 2.2uH PCMC063T-2R2MN Cyntec 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P cap: 220U 2V EEFCX0D221ER 15mOhm 3.87Arms PANASONIC/79.22719.20L
H/S: SIS412DN/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S: SIS412DN/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037

Vout=0.704V*(R1+R2)/R2

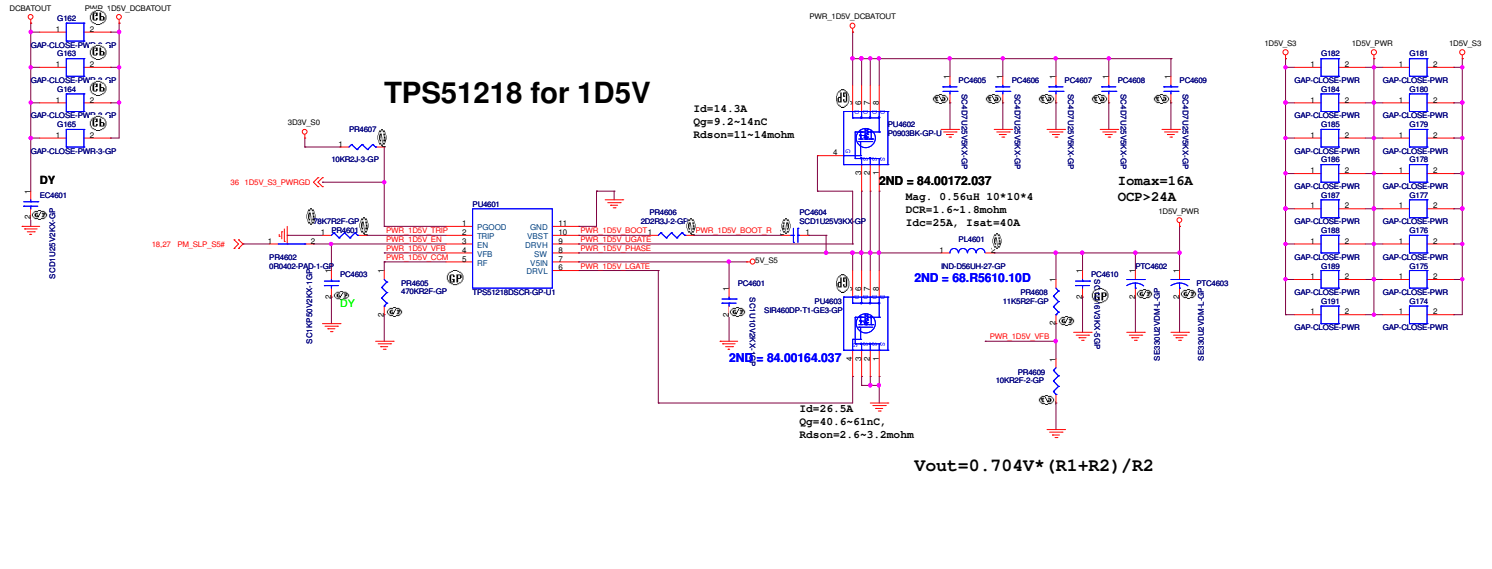
<Core Design>

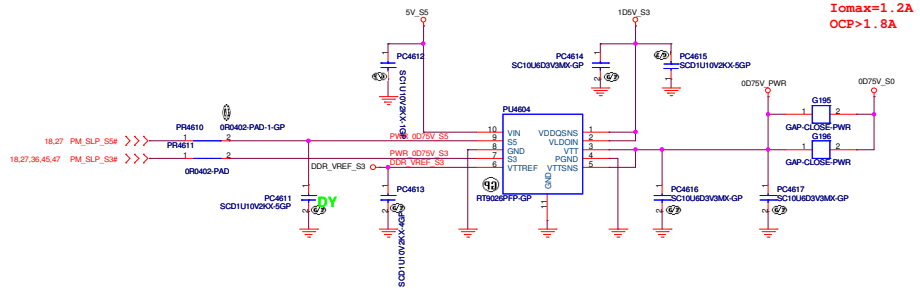
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: VREG_1D1V_S5 & 1V_S0

Size	Document Number	Rev
	B575	SA

Date: Monday, March 28, 2011 Sheet 45 of 103



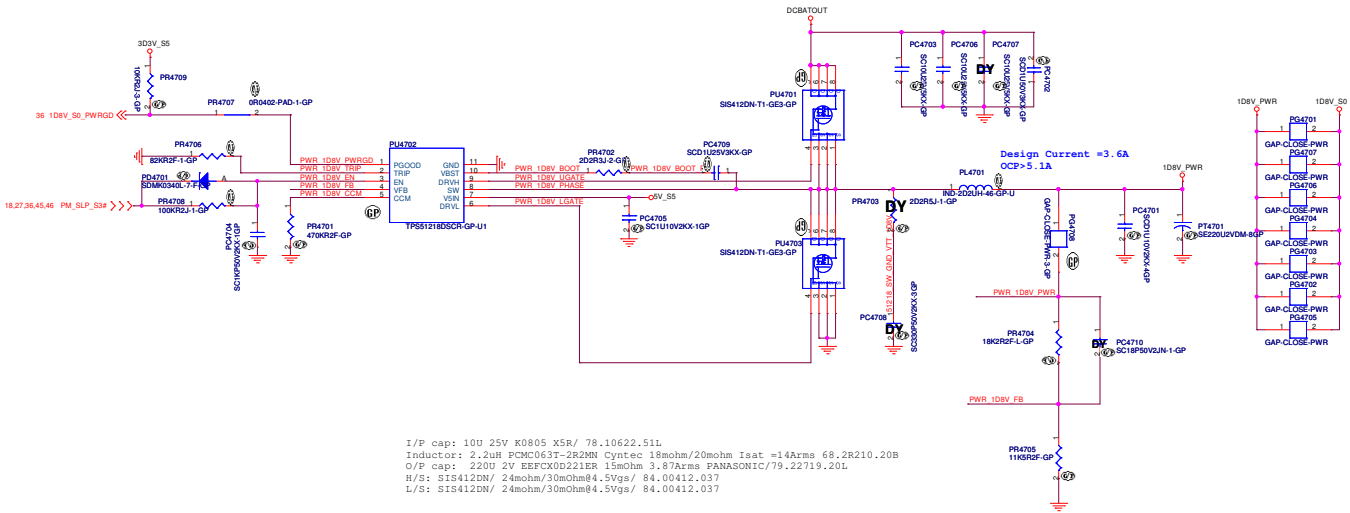


<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51128_1D5V & RT9026PFP-GP_0D75V

Size	Document Number	Rev
		SA

Date: Monday, March 28, 2011 Sheet 46 of 103



I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 2.2uH PCMC063T-2R2MN Cyntec 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P cap: 220U 2V EEFCX0D221ER 15mOhm 3.87Arms PANASONIC/79.22719.20L
H/S: SIS412DN/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S: SIS412DN/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037

Vout=0.704V*(R1+R2)/R2

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPS51218_1D8V_S0**

Size	Document Number	Rev
	B575	SA

Date: Monday, March 28, 2011 Sheet 47 of 103

<Core Design>

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

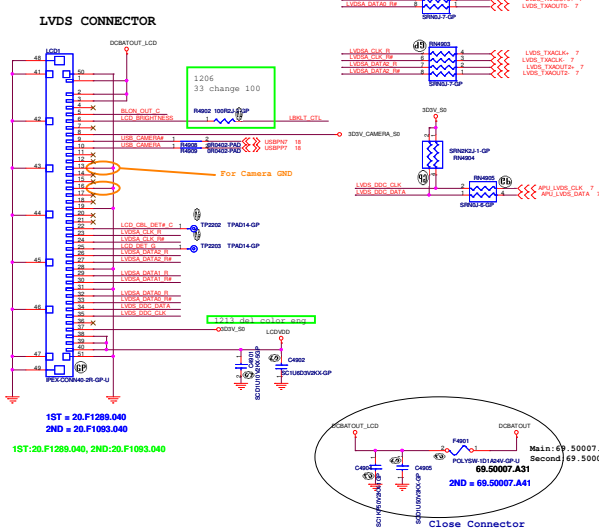
G-Sensor

Size	Document Number	Rev
	B575	SA

Date: Friday, March 25, 2011 Sheet 48 of 103

SSID = VIDEO

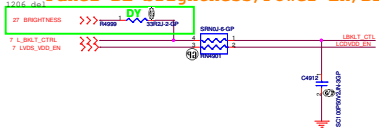
LVDS CONNECTOR



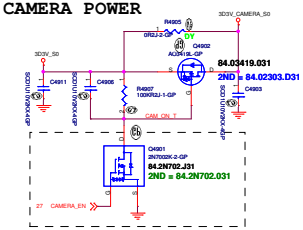
1ST = 20.F1289.040
2ND = 20.F1093.040

1ST:20.F1289.040, 2ND:20.F1093.040

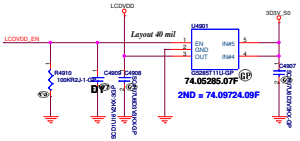
Panel BL brightness/Power En/BL En

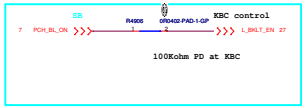


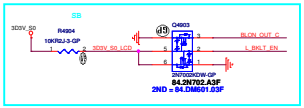
CAMERA POWER

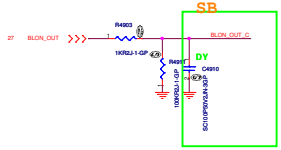


SSID = VIDEO



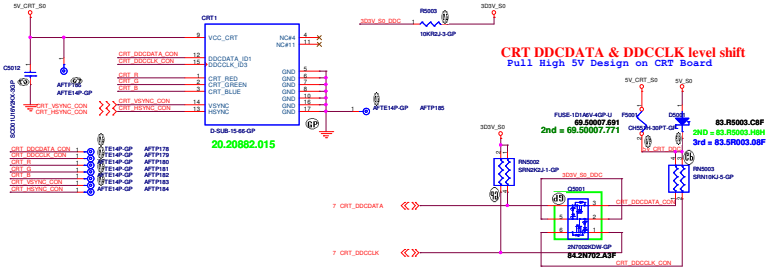


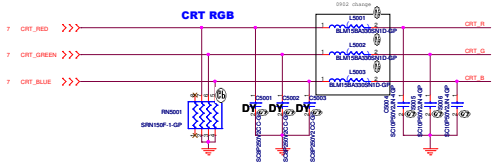




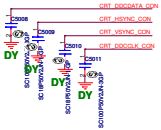
<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

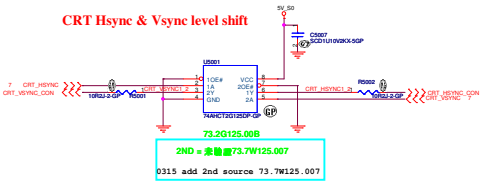
Title: LCD Connector
Size: A2 | Document Number: B575 | Rev: SA
Date: Monday, March 28, 2011 | Sheet 49 of 103





Pull high 在CRT





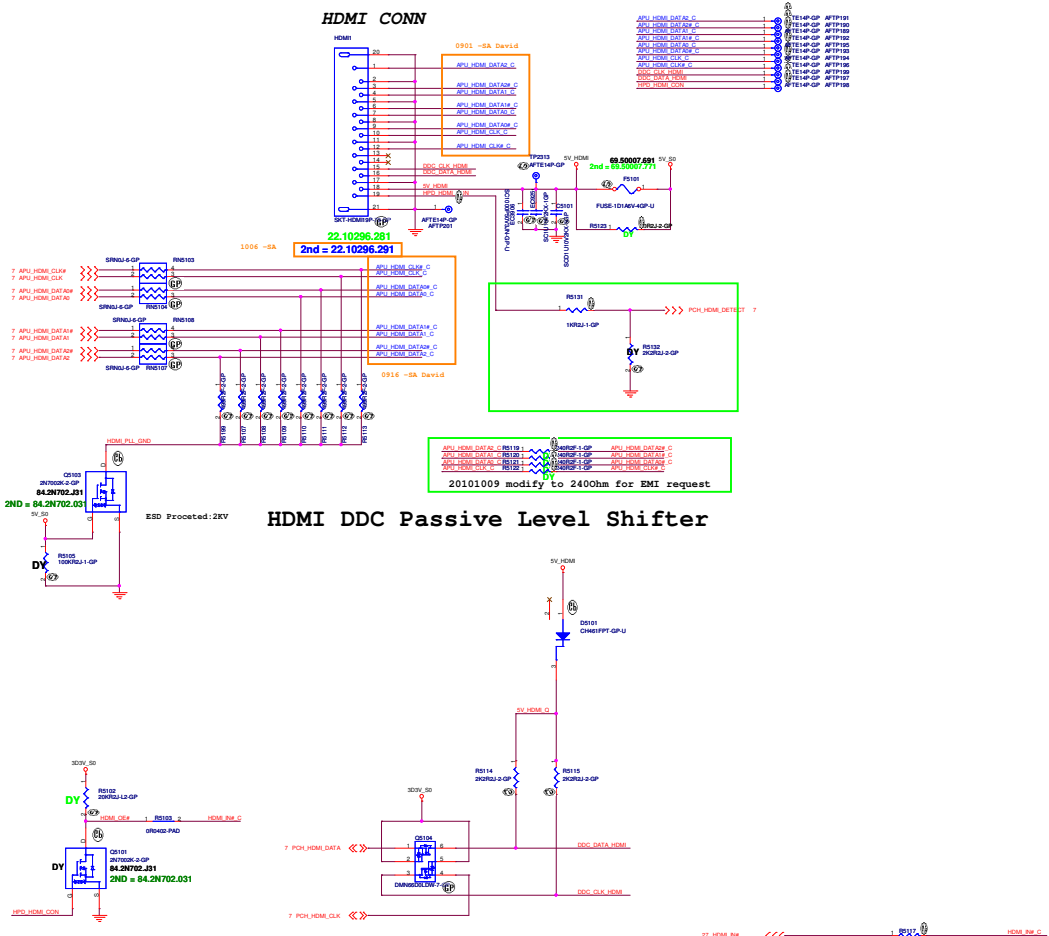
<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT CONN

Size	Document Number	Rev
	B575	SA

Date: Monday, March 28, 2011 Sheet 50 of 103

HDMI Level Shifter & CONNECTOR



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	HDMI Level Shifter / Conn	
Size: A2	Document Number: B575	Rev: SA
Date: Sunday, March 07, 2011	Sheet 51 of 103	

(Blanking)

(Blanking)

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***S-VIDEO***

Size	Document Number	Rev
A4	B575	SA

Date: Friday, March 25, 2011 Sheet 53 of 103

(Blanking)

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

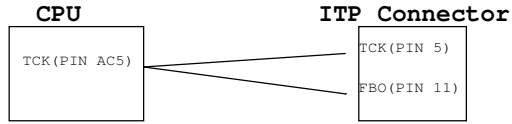
Size	Document Number	Rev
A4	B575	SA

Date: Friday, March 25, 2011 Sheet 54 of 103

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



<Core Design>

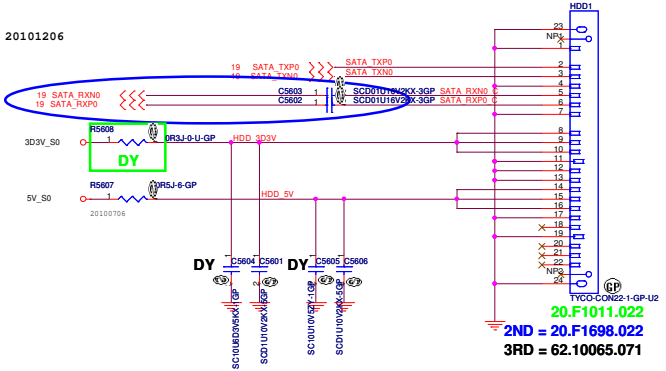
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

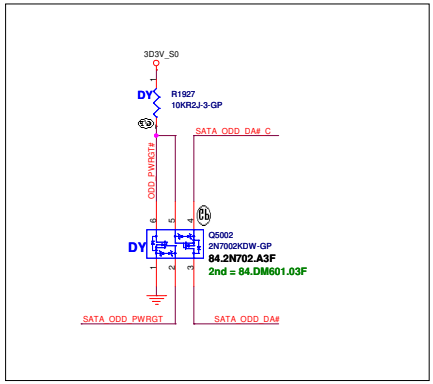
Title: ITP

Size: A4 | Document Number: B575 | Rev: SA

Date: Friday, March 25, 2011 | Sheet 55 of 103

SATA HDD Connector

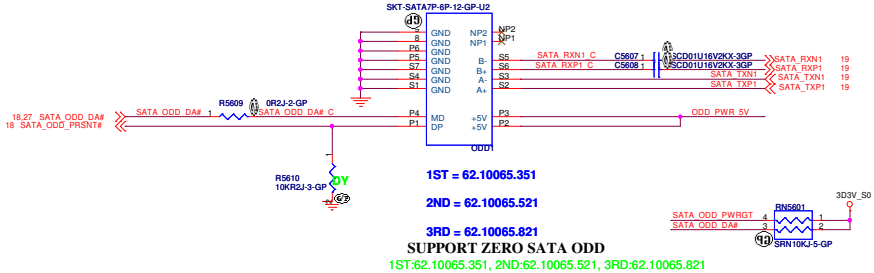




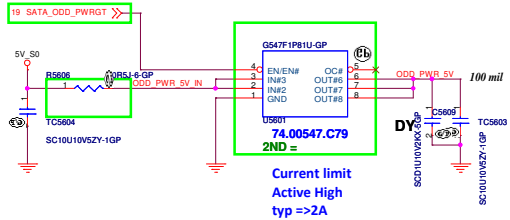
ODD Connector

SATA_RX- and SATA_RX+ Trace
Length match within 20 mil

Mars:
Exchange ODD and ESATA differential pair each other.

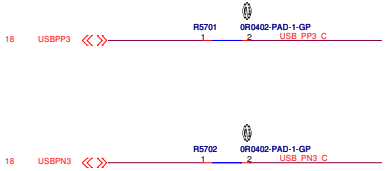


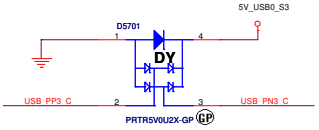
SATA Zero Power ODD

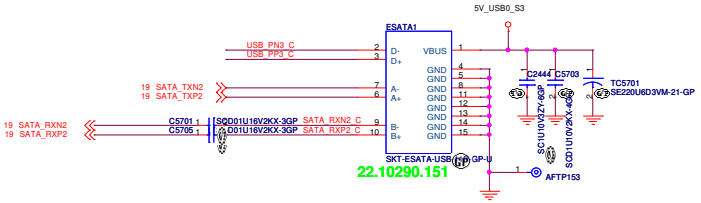


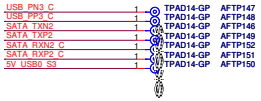
<Core Design>

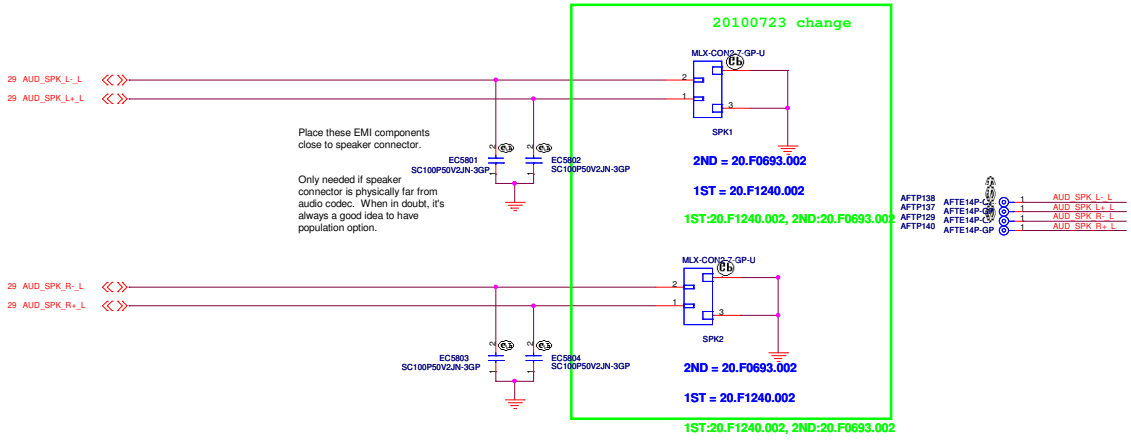
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	HDD / ODD CONN	
Size	Document Number: B575	Rev: SA
Date: Monday, March 28, 2011	Sheet 56 of 103	


18 USBPP3
R5701
0R0402-PAD-1-GP
USB_PP3_C
18 USBPN3
R5702
0R0402-PAD-1-GP
USB_PN3_C


5V_USB0_S3
D5701
DY
USB_PP3_C
USB_PN3_C
PRTR5V0U2X-GP


5V_USB0_S3
ESATA1
USB_PN3_C
USB_PP3_C
19 SATA_TXN2
19 SATA_TXP2
19 SATA_RXN2
19 SATA_RXP2
C5701
C5705
SCD01U16V2KX-3GP
SATA_RXN2_C
SATA_RXP2_C
D-
D+
A-
A+
B-
B+
VBUS
GND
C2444
C5703
TC5701
SE220U6D3VM-21-GP
SC1U10V2ZY-6GP
SCD1U10V2KX-4GP
SKT-ESATA-USB-GP-U
AFTP153
22.10290.151


USB_PN3_C
USB_PP3_C
SATA_TXN2
SATA_TXP2
SATA_RXN2_C
SATA_RXP2_C
5V_USB0_S3
TPAD14-GP
AFTP147
AFTP148
AFTP146
AFTP149
AFTP152
AFTP151
AFTP150



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: SPEAKER		
Size: A3	Document Number: B575	Rev: SA
Date: Monday, March 28, 2011	Sheet 58 of 103	

Reserved

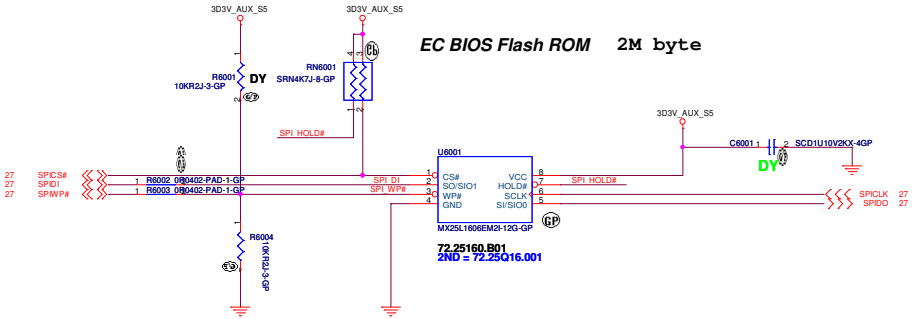
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

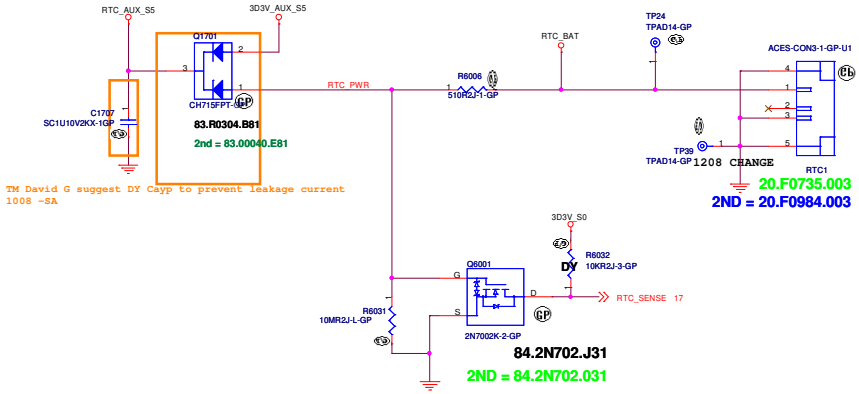
Title: Reserved

Size	Document Number	Rev
A3	B575	SA

Date: Friday, March 25, 2011 Sheet 59 of 103



DN have eccounter RTC battery no power from field side feedbackfor Larry suggestion,
add Diode when 3.3V_Aux_S5 provide power to FCH RTC



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

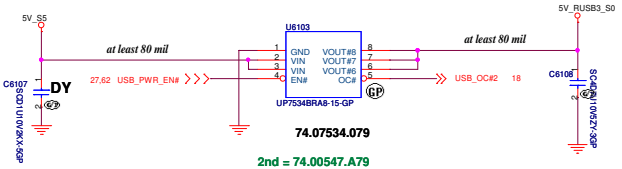
Title: BIOS / RTC

Size	Document Number	Rev
	B575	SA

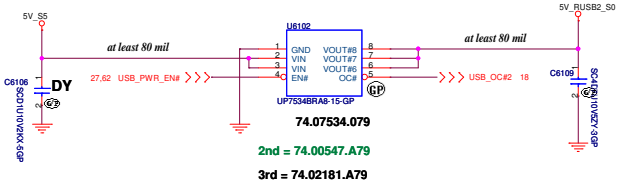
Date: Monday, March 28, 2011 Sheet 60 of 103

SSID = USB

RJ45_USB Board USB Power



I/O Board USB Power



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

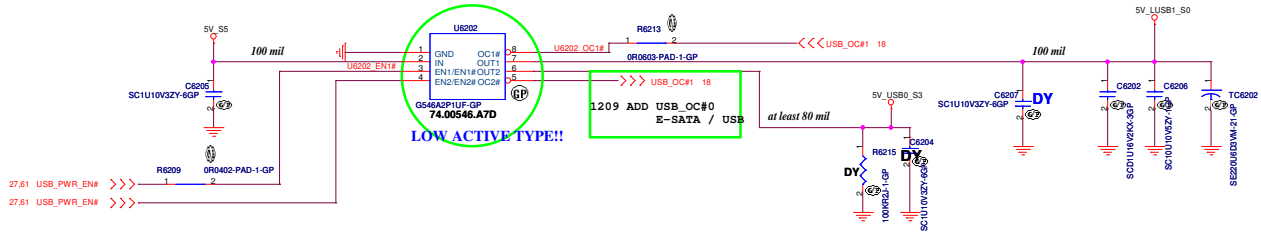
Title: USB Power SW

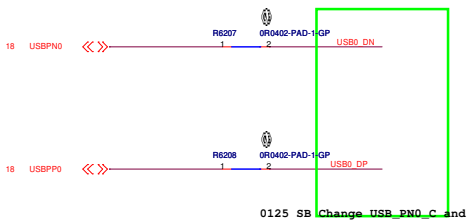
Size	Document Number	Rev
A3	B575	SA

Date: Monday, March 28, 2011 Sheet 61 of 103

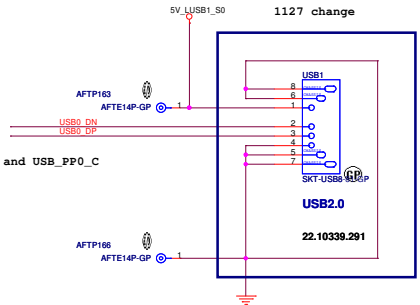
MB USB Port - #3

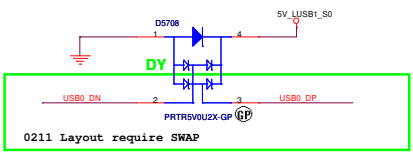
Left Side USB Power Switch

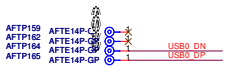




0323 DEL RN6201, net USB_PN0_C and USB_PP0_C



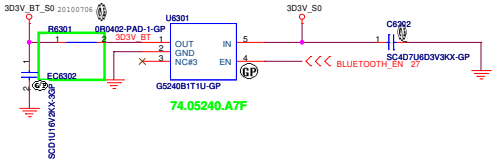




<Core Design>

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	USB CONN
Size	Document Number: B575 — Rev: SA
Date: Monday, March 28, 2011	Sheet 62 of 103

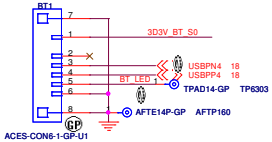
Bluetooth Power

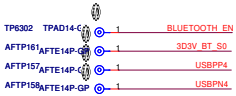


BT CONN.

EC6302 put near BLUE1 / all USB put one choke near connector by EMI request

200mA



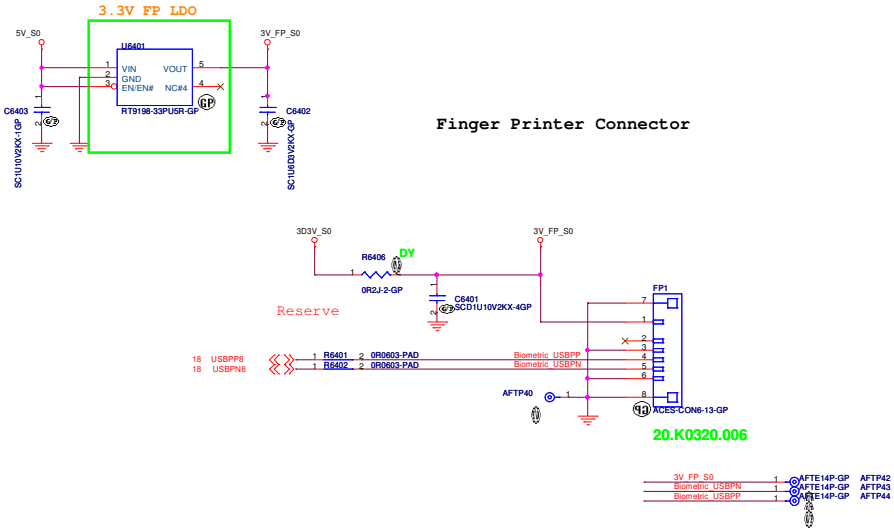


20.F0772.006

2ND = 20.F1804.006

<Core Design>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Bluetooth CONN	
Size	Document Number B575	Rev SA
Date: Monday, March 28, 2011	Sheet 63 of 103	



LA57 UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

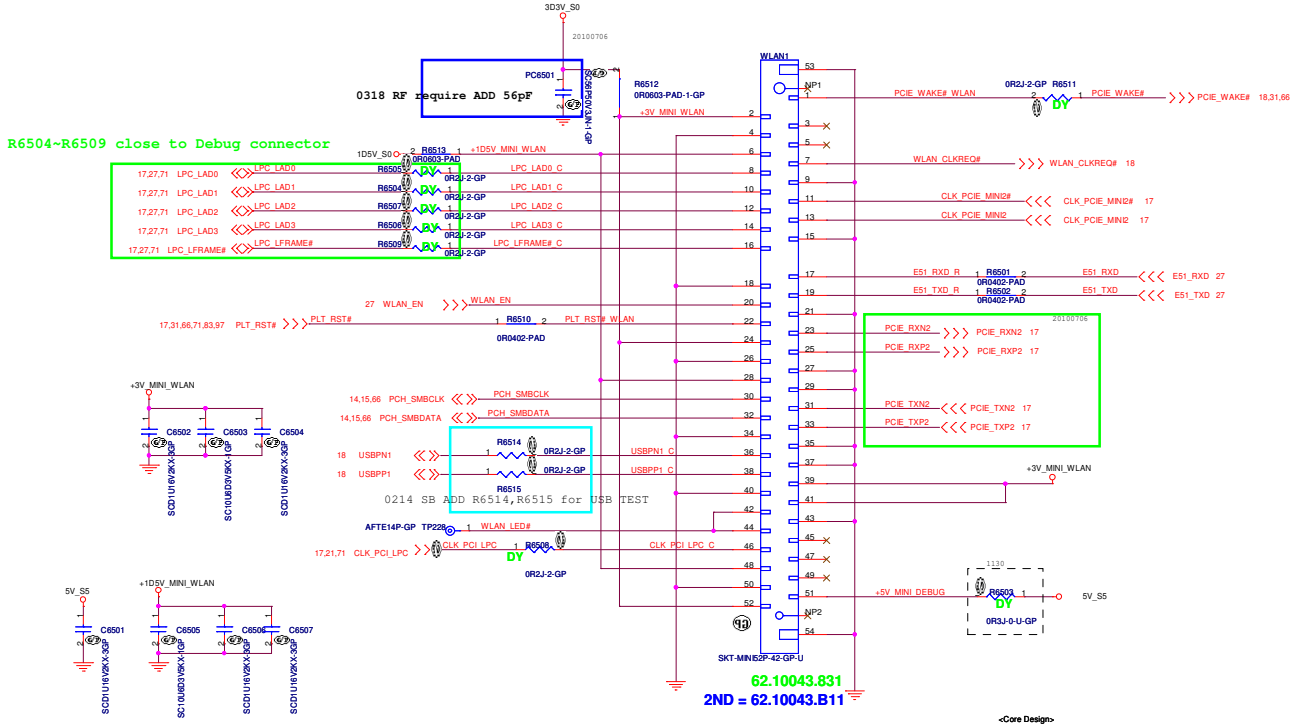
Title: ***RESERVED***

Size	Document Number	Rev
A3	B575	SA

Date: Monday, March 28, 2011 Sheet 64 of 103

SSID = Wireless

Mini Card Connector(802.11a/b/g/n)

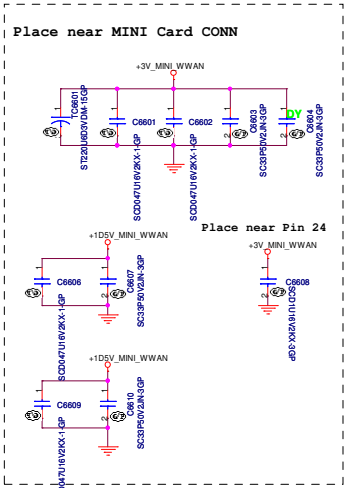


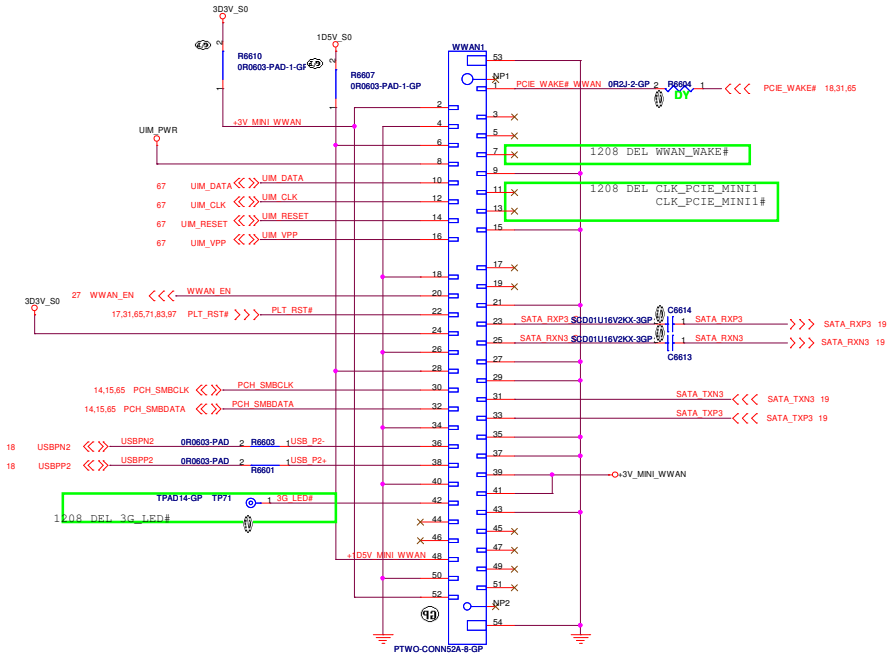
<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MINICARD WLAN		
Size	Document Number: B575	Rev: SA
Date: Monday, March 28, 2011	Sheet 65 of 103	

SSID = Wireless

Mini Card Connector(WWAN)





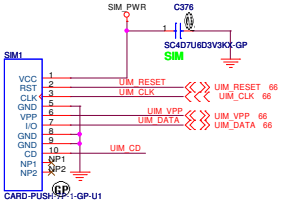
<Core Design>

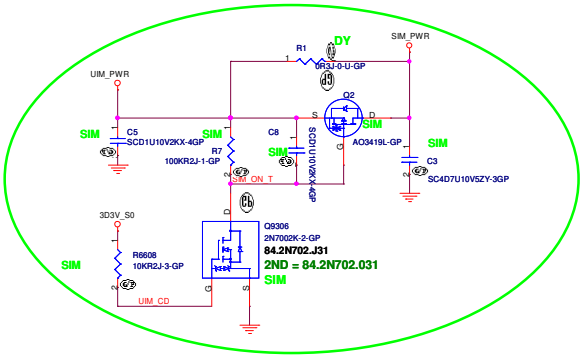
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINICARD WWAN

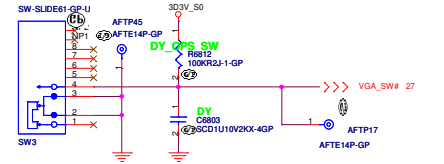
Size	Document Number	Rev
	B575	SA

Date: Monday, March 28, 2011 Sheet 66 of 103

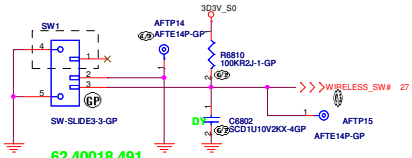

SIM_PWR
C376
SC4D7U6D3V3K2-GP
SIM
SIM1
VCC
RST
CLK
GND
VPP
I/O
GND
GND
CD
NP1
NP2
UIM_RESET
UIM_CLK
UIM_VPP
UIM_DATA
UIM_CD
UIM_RESET 66
UIM_CLK 66
UIM_VPP 66
UIM_DATA 66
CARD-PUSH-8P-1-GP-U1
20.I0073.001


DY
SIM_PWR
R1
0R3J-0-U-GP
UIM_PWR
Q2
AO3419L-GP
SIM
C5
SCD1U10V2KX-4GP
C8
SCD1U10V2KX-4GP
R7
100KR2J-1-GP
C3
SC4D7U10V5ZY-3GP
UIM_ON_T
3D3V_S0
R6608
10KR2J-3-GP
Q9306
2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031
UIM_CD

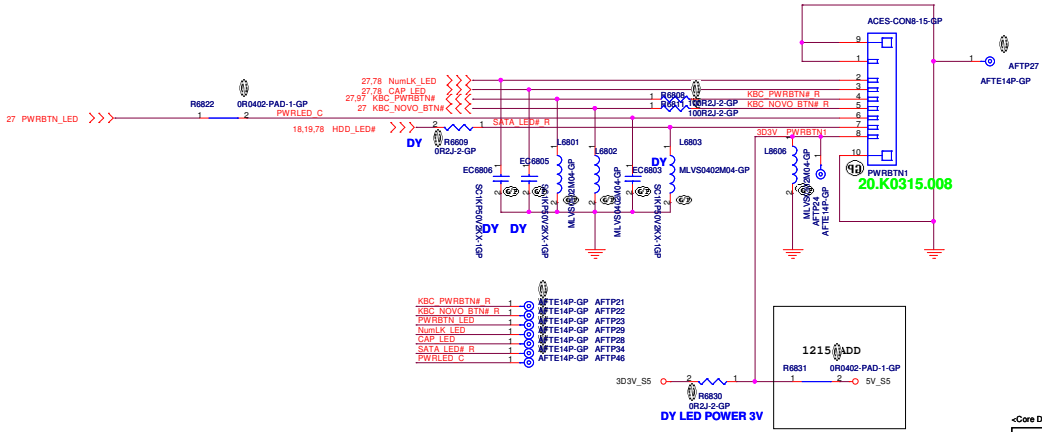
SSID = User.Interface



1208 ADD VGA SW



1208 ADD BT SW

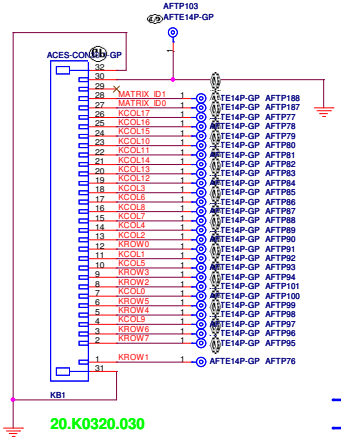


<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**POWER BUTTON**
Size: A3	Document Number: B575 — Rev: SA
Date: Monday, March 28, 2011	Sheet 68 of 103

SSID = KBC

Internal KeyBoard Connector



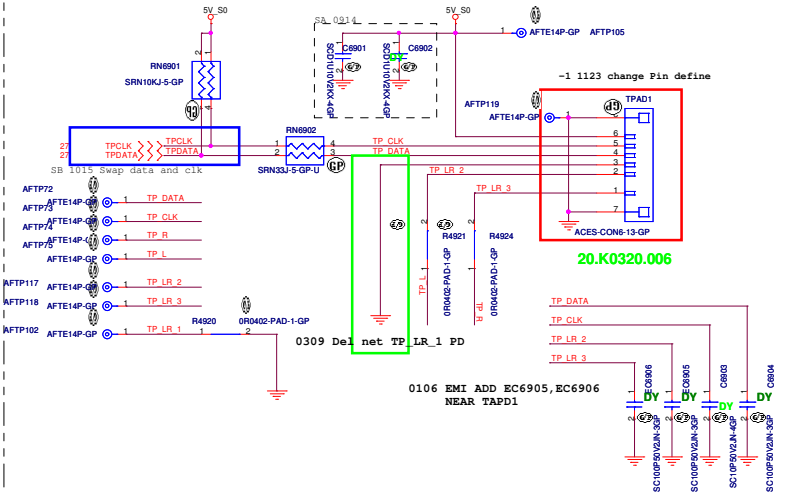
S205少兩PIN,
原廠測點已補上

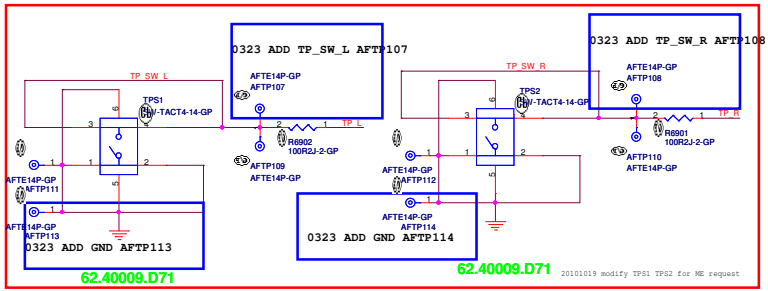
ID KEY MATRIX	SENSE			
	27	28	29	30
	ID0	ID1	ID2	GND
US	GND	GND	X	GND
GB	GND	X	X	GND
JP	X	GND	X	GND

KROW[7..0] 27

KCOL[17..0] 27

SSID = Touch.Pad





<Core Design>

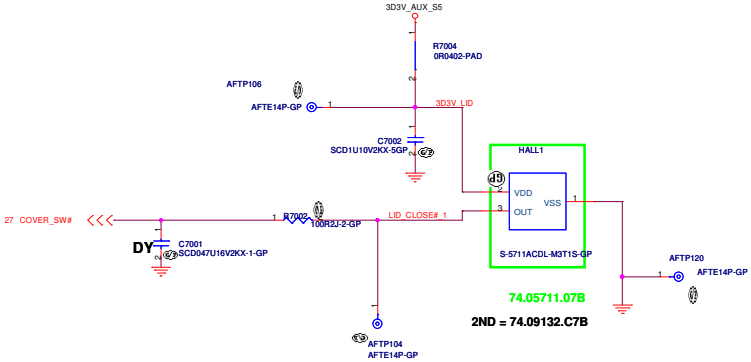
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KB/TP CONN

Size	Document Number	Rev
A3	B575	SA

Date: Monday, March 28, 2011 Sheet 69 of 103

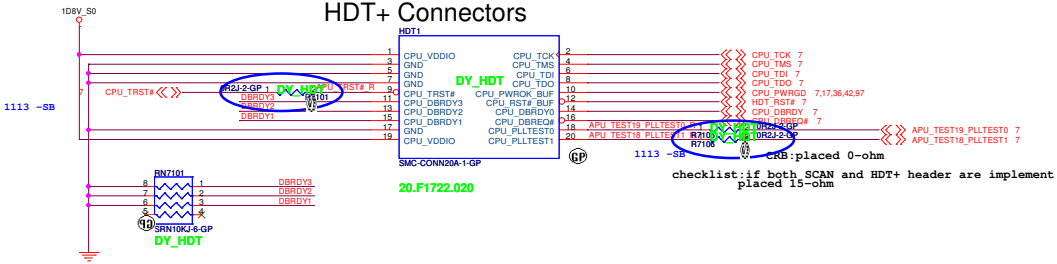
Hall Sensor



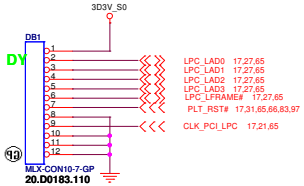
<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***HALL Sensor***	
Size	Document Number **B575**	Rev SA
Date: Monday, March 28, 2011	Sheet 70 of 103	

HDT+ Connectors



GOLDEN FINGER FOR DEBUG BOARD



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Debug Port***

Size	Document Number	Rev
	B575	SA

Date: Monday, March 28, 2011 Sheet 71 of 103

(Blanking)

LA57 UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	B575	SA

Date: Friday, March 25, 2011 Sheet 72 of 103

(Blanking)

LA57 UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A4	B575	SA

Date: Friday, March 25, 2011 Sheet 73 of 103

LA57 UMA

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CARD Reader CONN

Size	Document Number	Rev
A4	B575	SA

Date: Friday, March 25, 2011 Sheet 74 of 103

LA57 UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***New Card***

Size	Document Number	Rev
A4	B575	SA

Date: Friday, March 25, 2011 Sheet 75 of 103

(Blanking)

LA57 UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	B575	SA

Date: Friday, March 25, 2011 Sheet 76 of 103

(Blanking)

LA57 UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

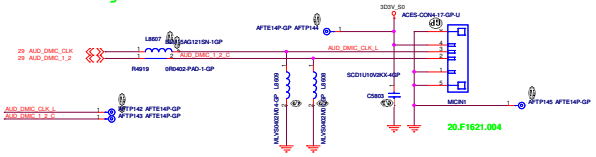
Title: ***Reserved***

Size	Document Number	Rev
A4	B575	SA

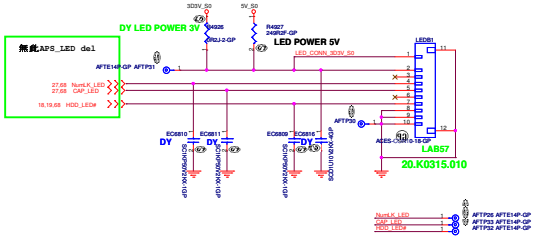
Date: Friday, March 25, 2011 Sheet 77 of 103

LB575 => Digital MIC

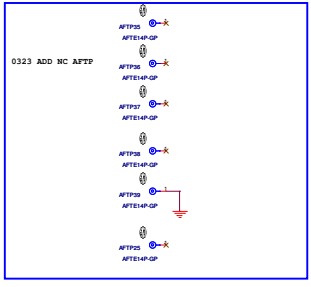
20101019 change L8607 L8608 L8609



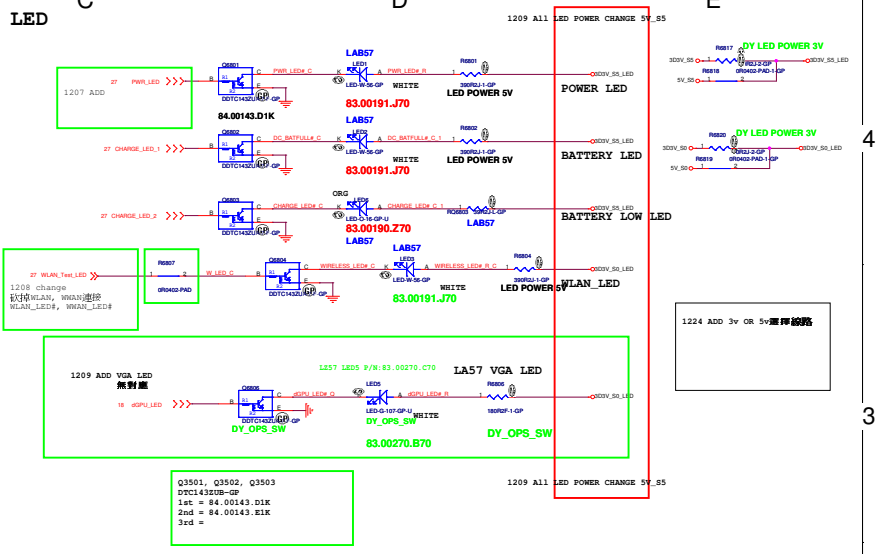
LED Bord CONN.



0323 ADD NC AFTP



LED



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

File: REFERENCE

Size: B | Document Number: B575 | Rev: SA

Date: Monday, March 28, 2011 | Sheet 78 of 105

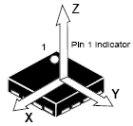
	ADXL322 LIS244AL LIS34AL	No Accel
R530	NO_ASM	ASM
R509	ASM	ASM
All other	ASM	NO_ASM

STMicro LIS34AL: 74.00034.0BZ
ADXL335 : 74.00335.0BZ

Layout Comment :

(1) Place C483, C484, Q46, R528, R530, C479, C476, R509, R508 close to U55.

(2) Avoid routing under DCDC switching area.



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***G-Sensor***

Size	Document Number	Rev
Custom	B575	SA

Date: Friday, March 25, 2011 Sheet 79 of 103

(Blanking)

LA57 UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A4	B575	SA

Date: Friday, March 25, 2011 Sheet 80 of 103

(Blanking)

LA57 UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

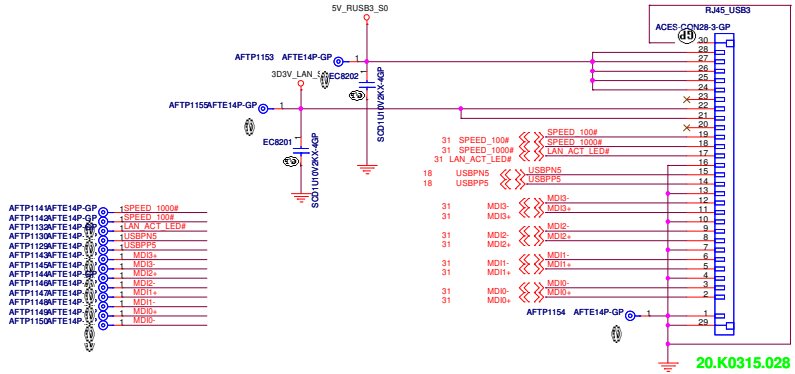
Title: ***Reserved***

Size	Document Number	Rev
A4	B575	SA

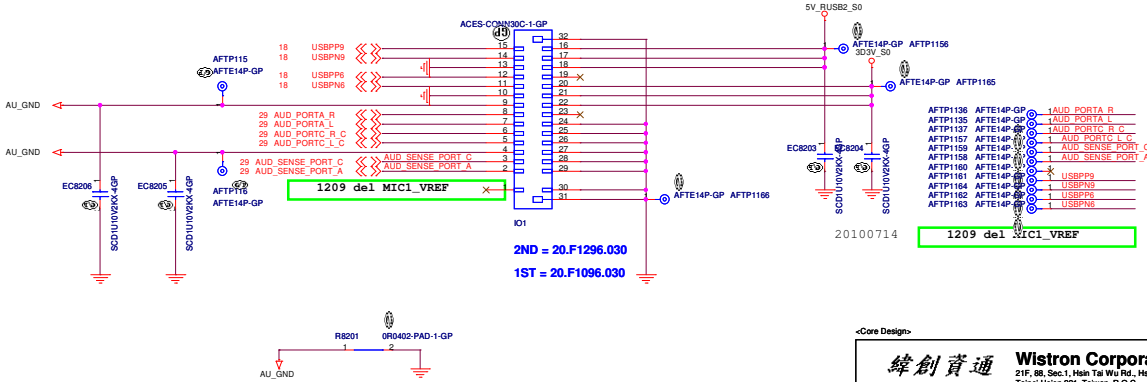
Date: Friday, March 25, 2011 Sheet 81 of 103

20100728 swap net

RJ45_USB CONN.

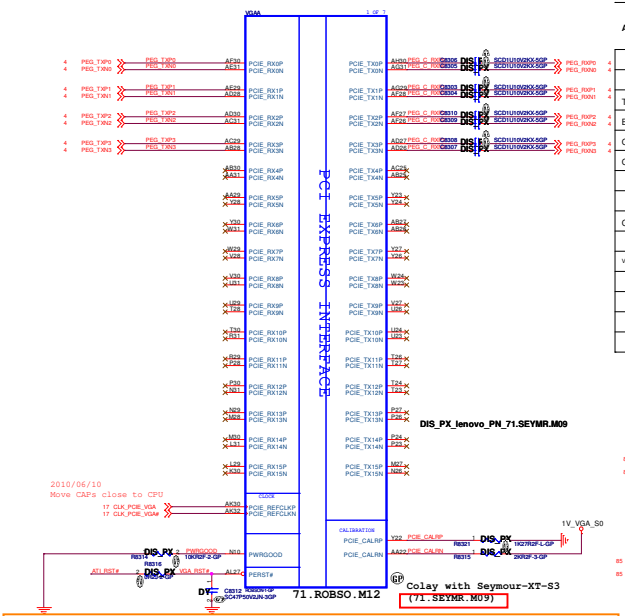


Card Reader Board CONN.



<Core Design>

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	IO BD CONN
Size	Document Number: B575 — Rev: SA
Date: Monday, March 28, 2011	Sheet 82 of 103

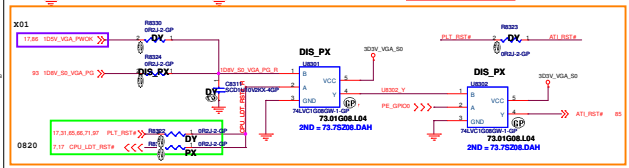


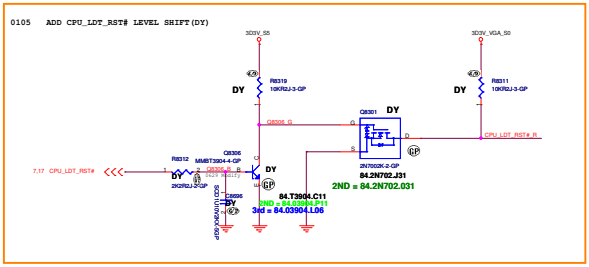
CONFIGURATION STRAPS

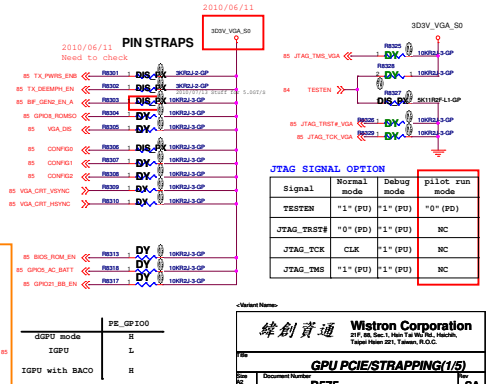
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMEND	PLATFORM SETTING
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	X	1
BIF_GEN2_EN_A	GPIO2	0:Advertises the PCIe device as 2.5GT/s capable at power on. 1:Advertises the PCIe device as 5.0GT/s capable at power on.	0	0
GPIO5_AC_BATT	GPIO5	optional input allow the system to request a fast power reduction by setting GPIO5 to low.	?	0
GPIO8_ROMSO	GPIO8	RESERVED	0	0
VGA_DIS	GPIO9	0:VGA Controller capacity enabled 1:The device won't be recognized as the system's VGA controller	0	0
ROMIDCFG[2:0]	GPIO[13:11]	BIOS_ROM_EN=1, Config[2:0] defines the ROM type BIOS_ROM_EN=0, Config[2:0] defines the primary memory aperture size	x x x	0 0 1 (256MB)
GPIO21_BB_EN	GPIO21	RESERVED	0	0
BIOS_ROM_EN	GPIO_22_ROMCSB	0:Disable external BIOS ROM device 1:Enable external BIOS ROM device	x	0
VIP_DEVICE_STRAP_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver that it sense whether or not a VIP device is connected on the VIP Host interface.	x	0
RSVD	H2SYNC	RESERVED	0	0
RSVD	GENERICC	RESERVED	0	0
AUD[1]	HSYNC	AUD[1:0]:11-Audio for both DisplayPort and HDMI	X	1
AUD[0]	VSYNC		X	1







Signal	Normal mode	Debug mode	pilot run mode
TESTEN	"1" (PU)	"1" (PU)	"0" (PD)
JTAG_TRST#	"0" (PD)	"1" (PU)	NC
JTAG_TCK	CLK	"1" (PU)	NC
JTAG_TMS	"1" (PU)	"1" (PU)	NC

	PE_GPIO0
dGPU mode	H
IGPU	L
IGPU with BACO	H

<Variant Name>

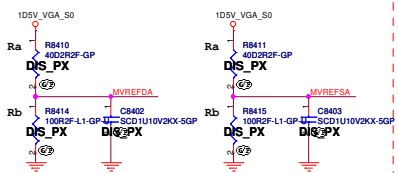
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU PCIE/STRAPPING(1/5)

Size	Document Number	Rev
A2	B575	SA

Date: Monday, March 28, 2011 Sheet 83 of 103

PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC



DDR3/GDDR3 Memory Stuff Option (ROBSON-S3/SEYMOUR-XT-S3)

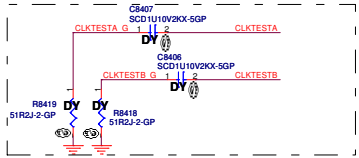
	DDR5	DDR3
MVDDQ	1.5V	1.5V/1.8V
Ra	40.2R	40.2R
Rb	100R	100R

DPC_CALR (Park/Robson-S3):
Analog calibration.
Connect DPxx_CALR to GND through a 150-Ω (1%) resistor.

**This basic topology should be used for DRAM_RST for DDR3/GDDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

Designator	For SEYMOUR	For Robson
R_MEM_1	10R	10R
R_MEM_2	50R	50R
R_MEM_3	5K	5K
C_MEM	120pF	120pF

Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except R_MEM_2



For normal GPU operation, these signals can be left floating (do not populate the capacitors and resistors).

2010/07/06
Schematics check list:
A pull-down resistor is required.

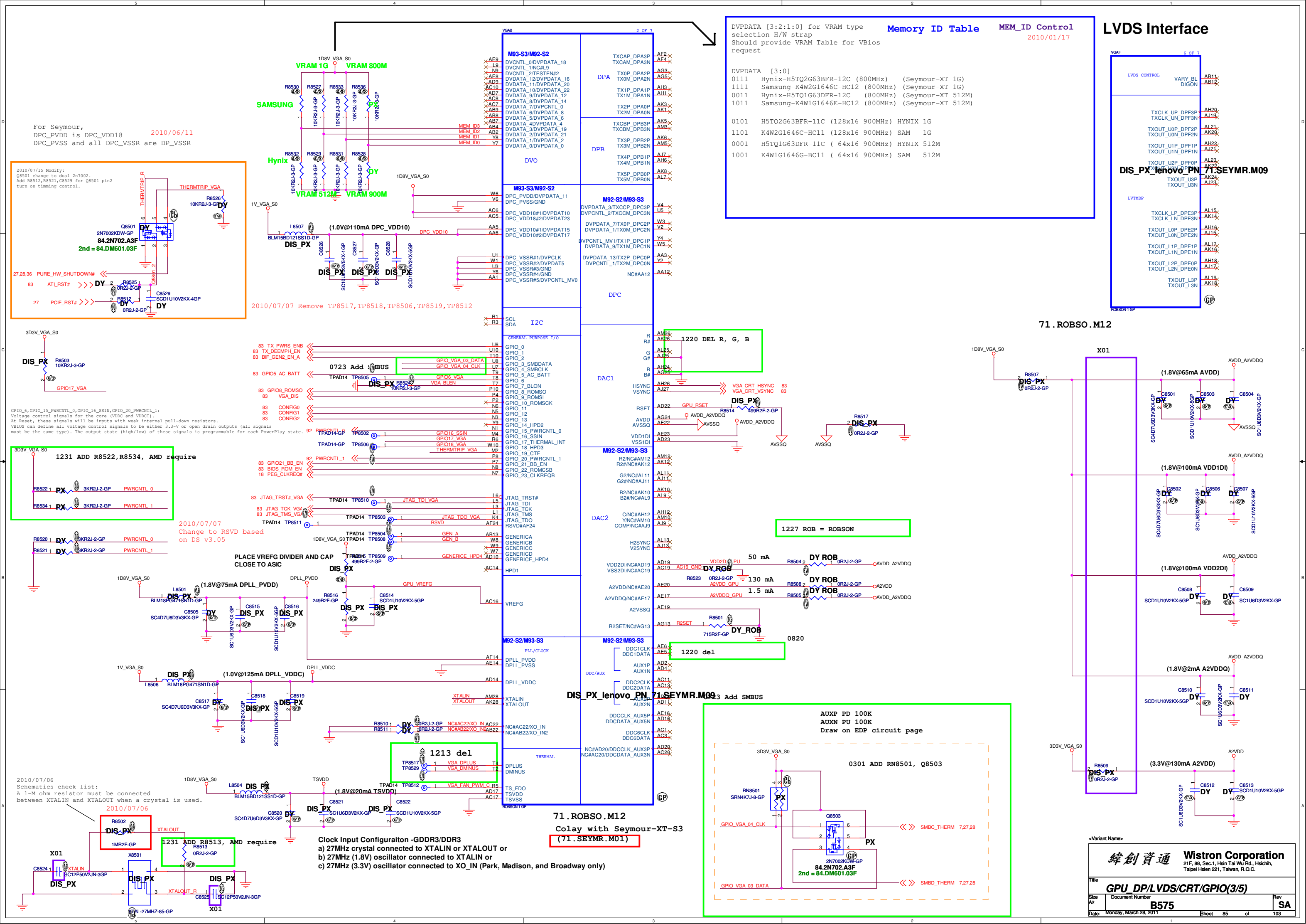
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

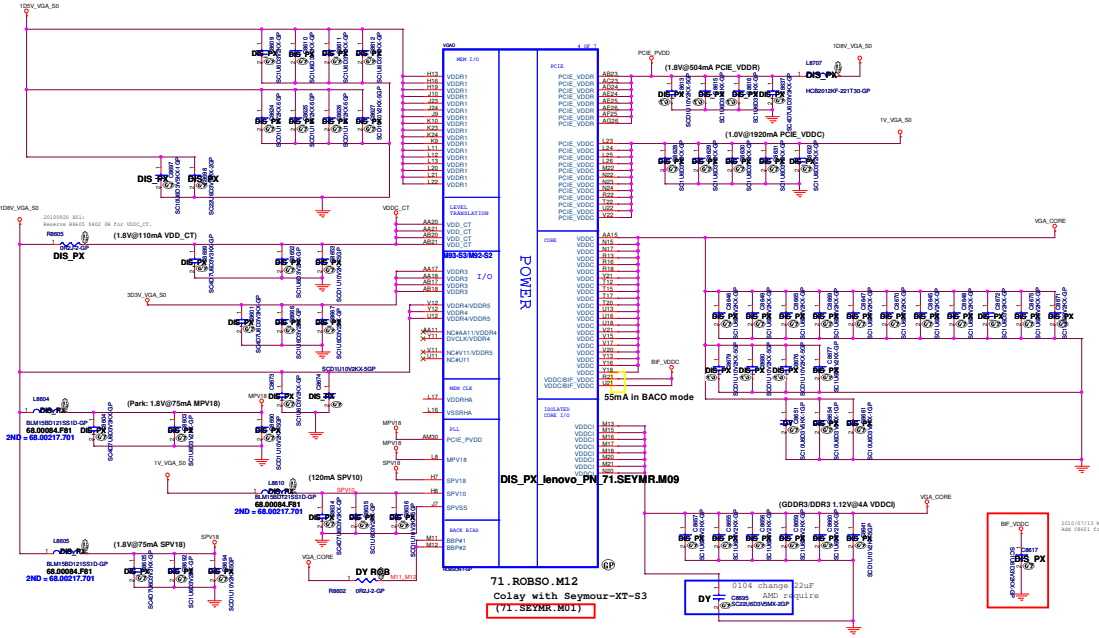
Title: GPU Memory(2/5)

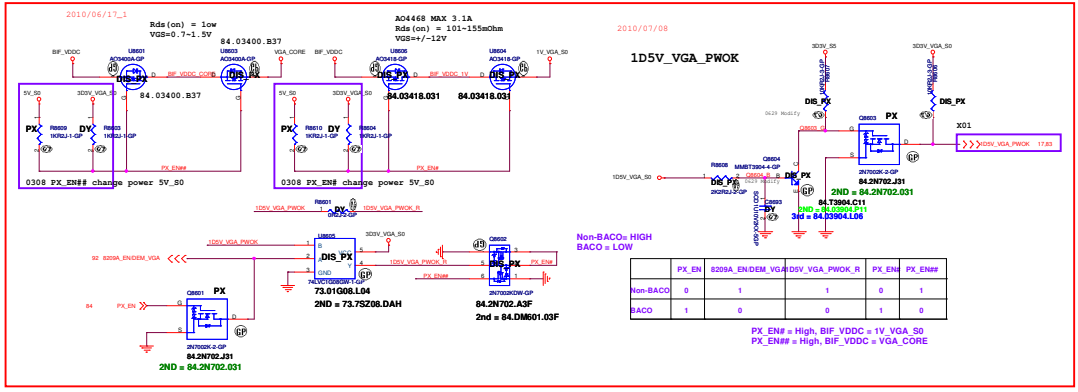
Size	Document Number	Rev
A3	B575	SA

Date: Monday, March 28, 2011 Sheet 84 of 103



LVDS Interface
Memory ID Table
MEM_ID Control
2010/01/17
DVPDATA [3:2:1:0] for VRAM type selection H/W strap
Should provide VRAM Table for VBios request
DVPDATA [3:0]
0111 Hynix-H5TQ2G63BFR-12C (800MHz) (Seymour-XT 1G)
1111 Samsung-K4W2G1646C-HC12 (800MHz) (Seymour-XT 1G)
0011 Hynix-H5TQ1G63DFR-12C (800MHz) (Seymour-XT 512M)
1011 Samsung-K4W1G1646E-HC12 (800MHz) (Seymour-XT 512M)
0101 H5TQ2G63BFR-11C (128x16 900MHz) HYNIX 1G
1101 K4W2G1646C-HC11 (128x16 900MHz) SAM 1G
0001 H5TQ1G63DFR-11C (64x16 900MHz) HYNIX 512M
1001 K4W1G1646G-BC11 (64x16 900MHz) SAM 512M
For Seymour,
DPC_PVDD is DPC_VDD18
DPC_PVSS and all DPC_VSSR are DP_VSSR
2010/06/11
2010/07/15 Modify:
Q8501 change to dual 2n7002.
Add R8512,R8521,C8529 for Q8501 pin2 turn on timing control.
2010/07/07 Remove TP8517,TP8518,TP8506,TP8519,TP8512
VRAM 1G
VRAM 800M
VRAM 512M
VRAM 900M
SAMSUNG
Hynix
1220 DEL R, G, B
0723 Add SMBUS
1231 ADD R8522,R8534, AMD require
2010/07/07
Change to RSVD based on DS v3.05
PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC
1227 ROB = ROBSON
71.ROBSO.M12
1220 del
0820
DIS_PX_lenovo_PN_71.SEYMR.M09
0323 Add SMBUS
AUXP PD 100K
AUXN PU 100K
Draw on EDP circuit page
0301 ADD RN8501, Q8503
1213 del
2010/07/06
Schematics check list:
A 1-M ohm resistor must be connected between XTALIN and XTALOUT when a crystal is used.
2010/07/06
1231 ADD R8513, AMD require
Clock Input Configuraiton -GDDR3/DDR3
a) 27MHz crystal connected to XTALIN or XTALOUT or
b) 27MHz (1.8V) oscillator connected to XTALIN or
c) 27MHz (3.3V) oscillator connected to XO_IN (Park, Madison, and Broadway only)
71.ROBSO.M12
Colay with Seymour-XT-S3
(71.SEYMR.M01)
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
GPU_DP/LVDS/CRT/GPIO(3/5)
Size A2
Document Number B575
Rev SA
Date: Monday, March 28, 2011
Sheet 85 of 103





	PX_EN	8209A_EN/DEM_VGA	1D5V_VGA_PWOK_R	PX_EN#	PX_EN##
Non-BACO	0	1	1	0	1
BACO	1	0	0	1	0

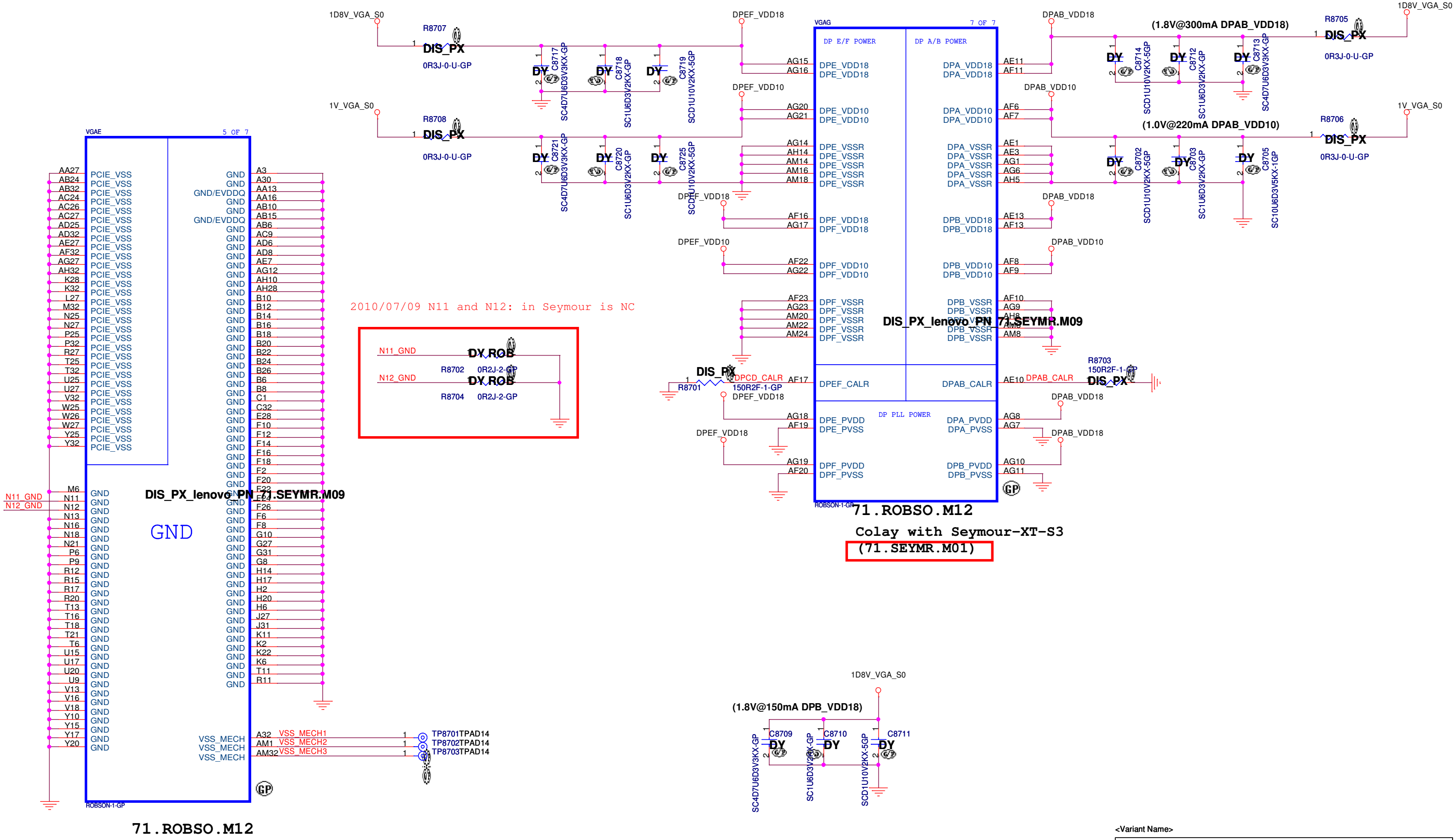
UMA 3G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_POWER(4/5)

Size	Document Number	Rev
A2	B575	SA

Date: Monday, March 08, 2010 Sheet 85 of 103



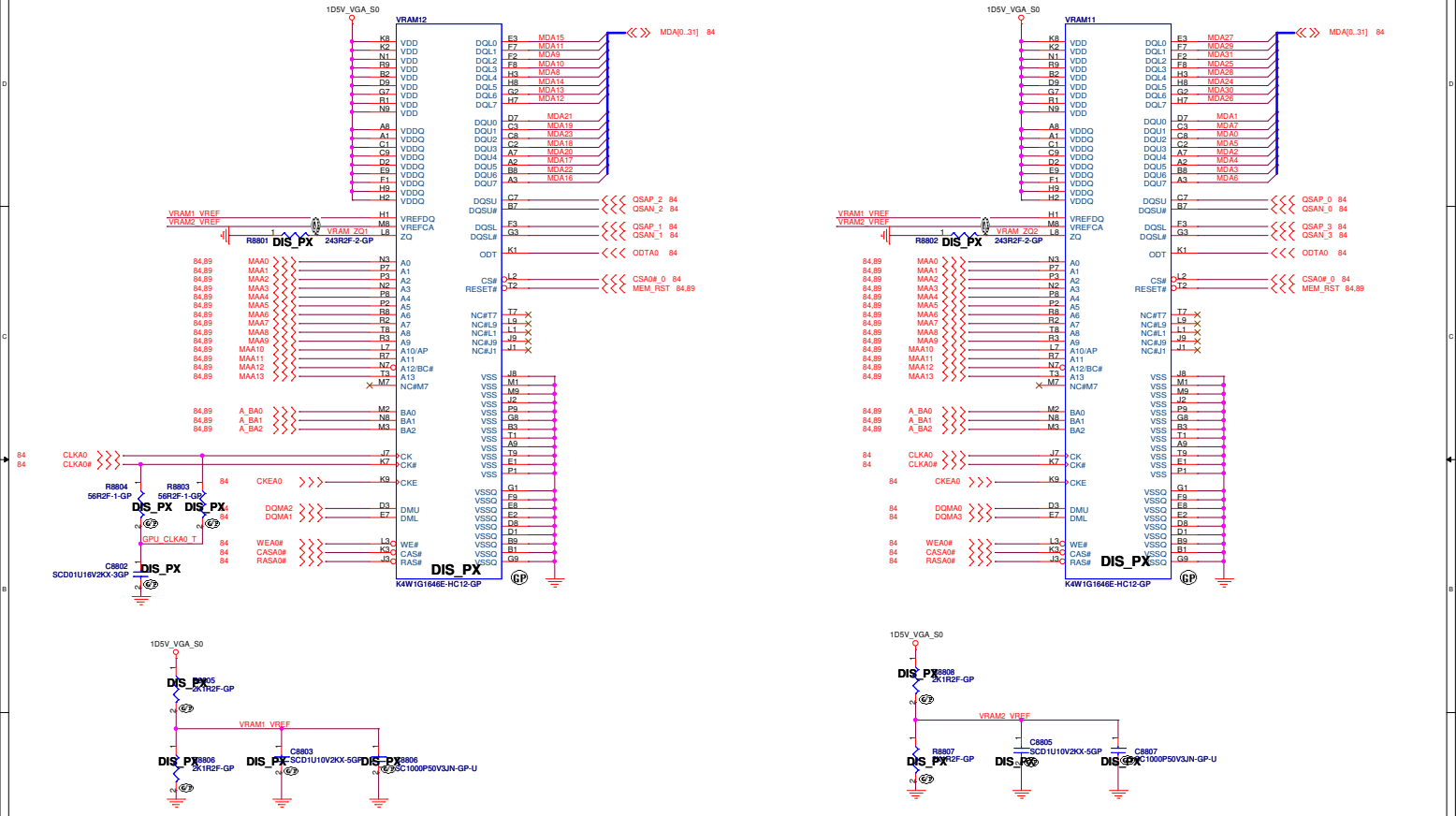
1D8V_VGA_S0
R8707
DIS_PX
0R3J-0-U-GP
C8717
SC4D7U6D3V3KX-GP
C8718
SC1U6D3V2KX-GP
C8719
SCD1U10V2KX-5GP
DPEF_VDD18
1V_VGA_S0
R8708
DPEF_VDD10
C8721
C8720
C8725
DY
VGAG
7 OF 7
DP E/F POWER
DP A/B POWER
DPE_VDD18
DPA_VDD18
DPE_VDD10
DPA_VDD10
DPE_VSSR
DPA_VSSR
DPF_VDD18
DPB_VDD18
DPF_VDD10
DPB_VDD10
DPF_VSSR
DPB_VSSR
DPEF_CALR
DPAB_CALR
DP PLL POWER
DPE_PVDD
DPE_PVSS
DPA_PVDD
DPA_PVSS
DPF_PVDD
DPF_PVSS
DPB_PVDD
DPB_PVSS
ROBSON-1-GP
71.ROBSO.M12
Colay with Seymour-XT-S3
(71.SEYMR.M01)
DIS_PX_lenovo_PN_71.SEYMR.M09
DPAB_VDD18
(1.8V@300mA DPAB_VDD18)
R8705
C8714
SCD1U10V2KX-5GP
C8712
SC1U6D3V2KX-GP
C8713
SC4D7U6D3V3KX-GP
DPAB_VDD10
(1.0V@220mA DPAB_VDD10)
R8706
C8702
C8703
C8705
SC10U6D3V5KX-1GP
R8701
150R2F-1-GP
DPCD_CALR
R8703
DPAB_CALR
2010/07/09 N11 and N12: in Seymour is NC
N11_GND
N12_GND
DY_ROB
R8702
R8704
0R2J-2-GP
VGAE
5 OF 7
PCIE_VSS
GND
GND/EVDDQ
VSS_MECH
VSS_MECH1
VSS_MECH2
VSS_MECH3
TP8701TPAD14
TP8702TPAD14
TP8703TPAD14
1D8V_VGA_S0
(1.8V@150mA DPB_VDD18)
C8709
C8710
C8711

<Variant Name>

緯創資通 **Wistron Corporation**

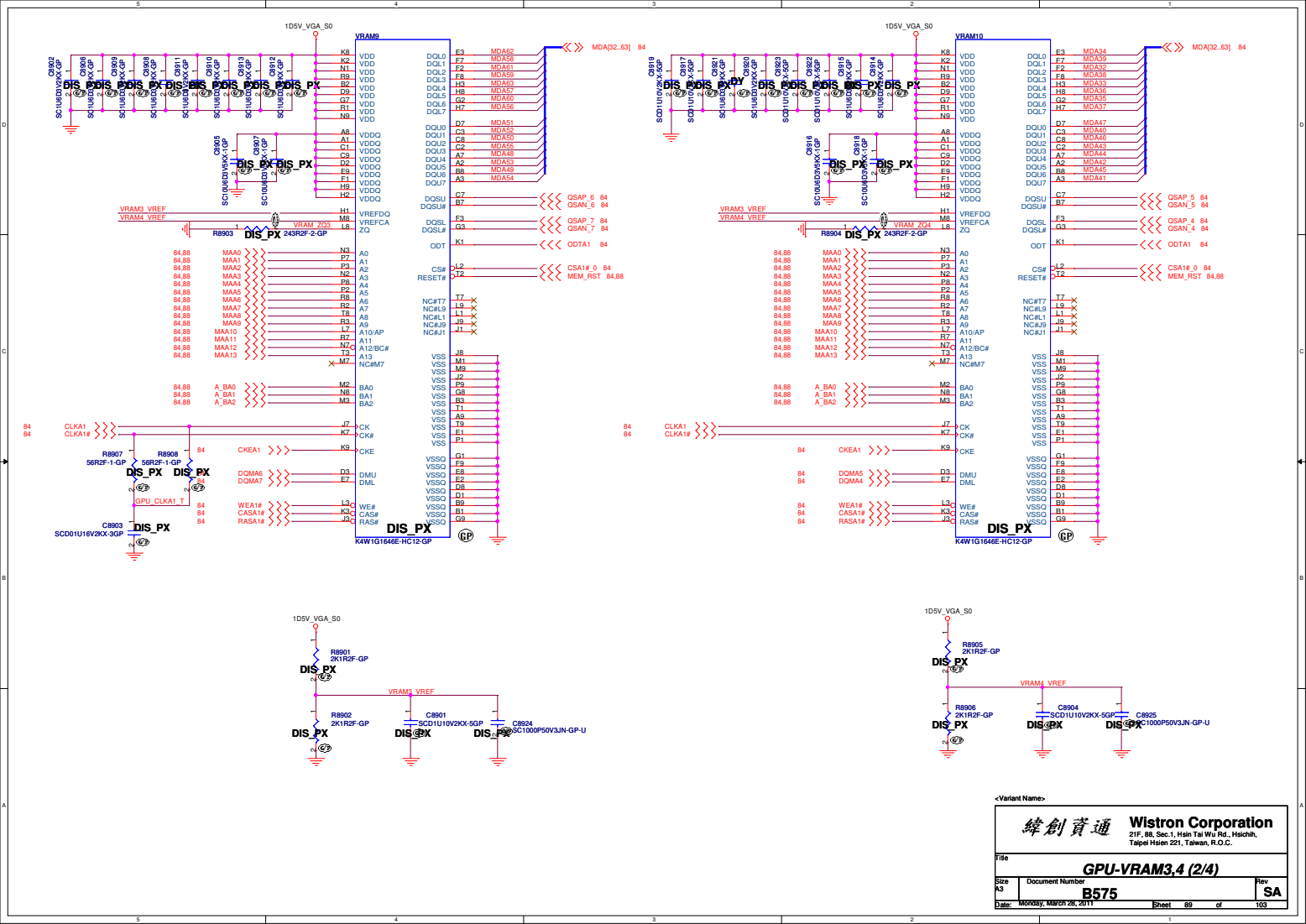
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	GPU_DPPWR/GND(5/5)		
Size A3	Document Number B575		Rev SA
Date: Friday, March 25, 2011		Sheet 87 of 103	



<variant_name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: GPU-VRAM1,2 (1/4)		
Size: A3	Document Number: B575	Rev: SA
Date: Monday, March 28, 2011	Sheet 88 of 103	



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

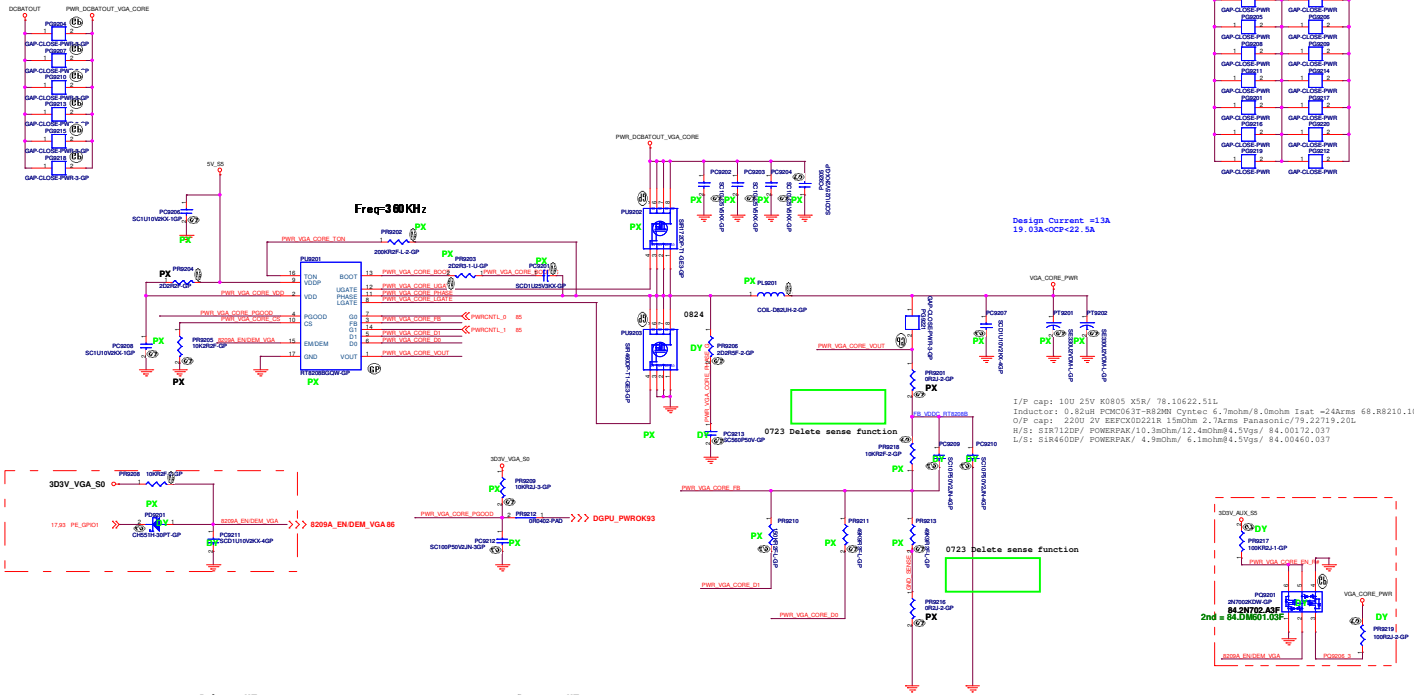
<Variant Name>

Title: GPU-VRAM3,4 (2/4)

Size	Document Number	Rev
A3	B575	SA

Date: Monday, March 28, 2011 Sheet 89 of 103

SSID = PWR.Plane.Regulator_VGACORE



Robson-XT

PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
L	L	1.10V
L	H	0.95V
H	L	1.05V
H	H	0.9V

Seymour-XT

PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
L	L	1.1V
L	H	0.95V
H	L	1.05V
H	H	0.9V

Vout=0.75V*(R1+R2)/R2

For ROBSON

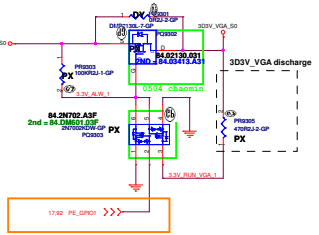
PR9210=44K.2K(64.44225.6DL)

PR9211=150K(64.15035.6DL)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

File:	RT8208B_+VCC_GFXCORE		
Size	Document Number	B575	Rev SA
Date: Monday, March 28, 2011		Sheet 59 of 103	

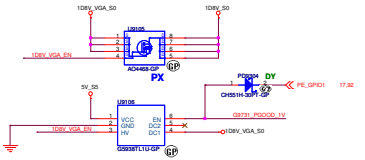
+3VS to 3.3V_DELAY Transfer

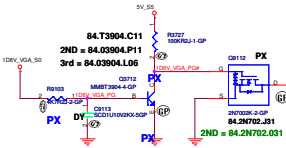


Different To Intel, AMD Is High Active

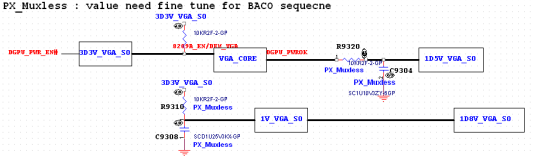
	PE_GPIO0	PE_GPIO1
dGPU mode	H	H
IGPU	L	L
IGPU with BACO	H	H

G9731 for 1D8V_VGA





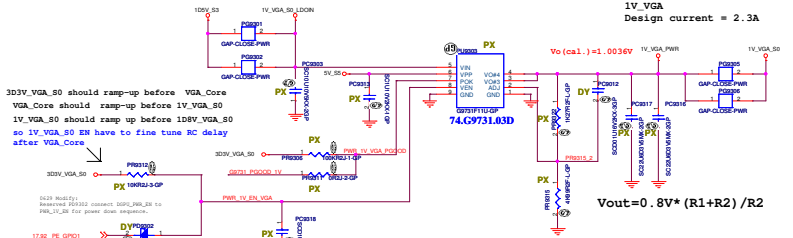
PX_Muxless : value need fine tune for BAC0 sequecne



G9731 for 1V_VGA_S0

Park_Madison Does Not Support BACO, So follow Old Sequence
Seymour_Whistler_Robson Support BACO, So Change Sequence

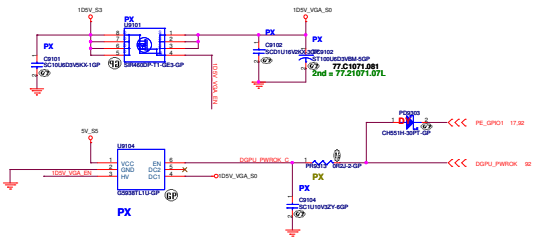
3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1V_VGA_S0
1V_VGA_S0 should ramp up before 1D8V_VGA_S0
so 1V_VGA_S0 EN have to fine tune RC delay after VGA_Core



1V_VGA
Design current = 2.3A

Vout=0.8V*(R1+R2)/R2

1D5V_VGA_S0



UMA 3G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: DISCRETE VGA POWER

Size	Document Number	Rev
D	B575	SA

Date: Monday, March 08, 2011 Sheet 23 of 103

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

HDD / ODD CONN

Size	Document Number	Rev
	B575	SA

Date: Friday, March 25, 2011 Sheet 94 of 103

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CRT Switch***

Size	Document Number	Rev
A3	B575	SA

Date: Friday, March 25, 2011 Sheet 95 of 103

LA57 UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

TOUCH PANEL

Size	Document Number	Rev
A4	B575	SA

Date: Friday, March 25, 2011 Sheet 96 of 103

CPU Plate

H13 HOLE276R178-GP — ZZ.00PAD.N11
H14 HOLE276R178-GP — ZZ.00PAD.N11
H15 HOLE276R178-GP — ZZ.00PAD.N11

VGA Std-Off

H10 STF237R128H42-GP — PX
H11 STF237R128H42-GP — PX

34.4GD01.101 34.4GD01.101

Structure boss

H1 HOLE355X355R111-S1-GP — ZZ.00PAD.571
H2 HOLE355X355R111-S1-GP — ZZ.00PAD.571
H3 HOLE355X355R111-S1-GP — ZZ.00PAD.571
H5 HOLE355X355R111-S1-GP — ZZ.00PAD.571
H6 HOLE355X355R111-S1-GP — ZZ.00PAD.571
H12 HOLE355X355R111-S1-GP — ZZ.00PAD.571
H7 HOLE335R115-GP — ZZ.00PAD.D01
H8 HOLE335R115-GP — ZZ.00PAD.D01

MiniPCI Std-Off

H4 STF237R113H115-GP — 34.4V802.101

Check test point

3D3V_S0	TPAD14-GP	TP96
3D3V_AUX_S5	TPAD14-GP	TP95
3D3V_S5	TPAD14-GP	TP83
5V_S5	TPAD14-GP	TP82
18,27 PM_PWRBTN#	TPAD14-GP	TP78
7,17,36,42,71 CPU_PWRGD	TPAD14-GP	TP79
27,36 S5_ENABLE	TPAD14-GP	TP80
17,31,65,66,71,83 PLT_RST#	TPAD14-GP	TP81

Test Point放在Dimm Door打開可量測處

H16 GNDPAD — ZZ.NDPAD.XXX
H17 GNDPAD — ZZ.NDPAD.XXX

1216 改過footprint

POWER TESTING POINT--TOP

27,68 KBC_PWRBTN# — TP9701 TPAD40-GP, TP9700 TPAD40-GP

0106 EMI ADD EC CAP

1D5V_S3

EC9706 EC9705 EC9704 EC9703 EC9702 EC9701 — DY — SCD1U25V2KX-GP

0211 SB

DCBATOUT

EC9716 EC9715 EC9714 EC9713 EC9710 EC9709 EC9708 EC9707 EC9712 EC9711 — DY — SCD1U25V2KX-GP

0211 SB EMI require

BT+

EC9716 EC9717 — SCD1U25V2KX-GP

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SPRING/HALL

Size: A3 | Document Number: B575 | Rev: SA

Date: Monday, March 28, 2011 | Sheet 97 of 103

待確認

(Blanking)

<Core Design>

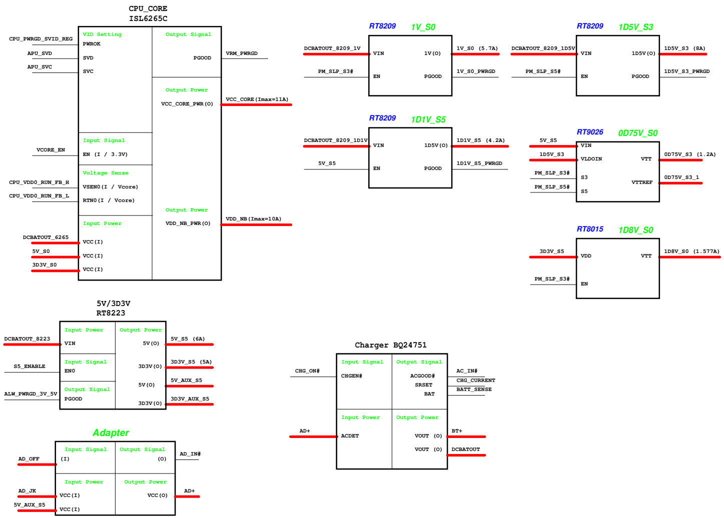
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Change History*

Size	Document Number	Rev
A4	B575	SA

Date: Friday, March 25, 2011 Sheet 98 of 103

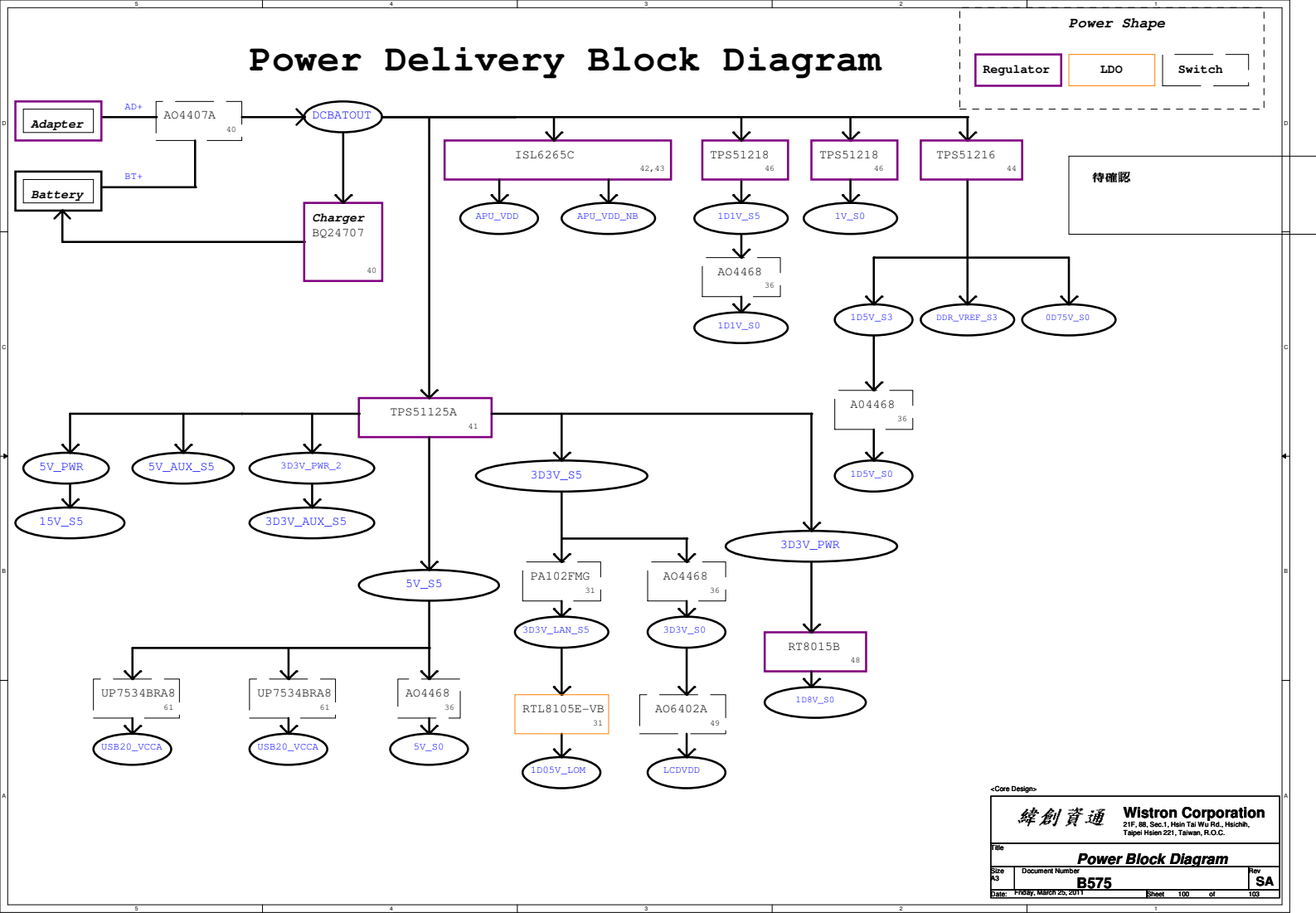
待確認


CPU_CORE
ISL6265C
VID Setting
PWROK
SVD
SVC
Output Signal
PGOOD
Output Power
VCC_CORE_PWR(O)
Input Signal
EN (I / 3.3V)
Voltage Sense
VSEN0(I / Vcore)
RTN0(I / Vcore)
Input Power
VCC(I)
VCC(I)
VCC(I)
Output Power
VDD_NB_PWR(O)
CPU_PWRGD_SVID_REG
APU_SVD
APU_SVC
VRM_PWRGD
VCC_CORE(Imax=11A)
VCORE_EN
CPU_VDD0_RUN_FB_H
CPU_VDD0_RUN_FB_L
VDD_NB(Imax=10A)
DCBATOUT_6265
5V_S0
3D3V_S0
RT8209
1V_S0
DCBATOUT_8209_1V
VIN
1V(O)
PM_SLP_S3#
EN
PGOOD
1V_S0 (5.7A)
1V_S0_PWRGD
RT8209
1D5V_S3
DCBATOUT_8209_1D5V
VIN
1D5V(O)
PM_SLP_S5#
EN
PGOOD
1D5V_S3 (8A)
1D5V_S3_PWRGD
RT8209
1D1V_S5
DCBATOUT_8209_1D1V
VIN
1D5V(O)
5V_S5
EN
PGOOD
1D1V_S5 (4.2A)
1D1V_S5_PWRGD
RT9026
0D75V_S0
5V_S5
1D5V_S3
PM_SLP_S3#
PM_SLP_S5#
VIN
VLDOIN
S3
S5
VTT
VTTREF
0D75V_S3 (1.2A)
0D75V_S3_1
RT8015
1D8V_S0
3D3V_S5
PM_SLP_S3#
VDD
EN
VTT
1D8V_S0 (1.577A)
5V/3D3V
RT8223
Input Power
VIN
Input Signal
EN0
Output Signal
PGOOD
Output Power
5V(O)
3D3V(O)
5V(O)
3D3V(O)
DCBATOUT_8223
S5_ENABLE
ALW_PWRGD_3V_5V
5V_S5 (6A)
3D3V_S5 (5A)
5V_AUX_S5
3D3V_AUX_S5
Charger BQ24751
Input Signal
CHGEN#
Output Signal
ACGOOD#
SRSET
BAT
Input Power
ACDET
Output Power
VOUT (O)
VOUT (O)
CHG_ON#
AC_IN#
CHG_CURRENT
BATT_SENSE
AD+
BT+
DCBATOUT
Adapter
Input Signal
(I)
Output Signal
(O)
Input Power
VCC(I)
VCC(I)
Output Power
VCC(O)
AD_OFF
AD_IN#
AD_JK
5V_AUX_S5
AD+

<Core Design>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	Power Sequence		
Size A1	Document Number B575		Rev SA
Date: Friday, March 25, 2011	Sheet 99	of	103

Power Delivery Block Diagram



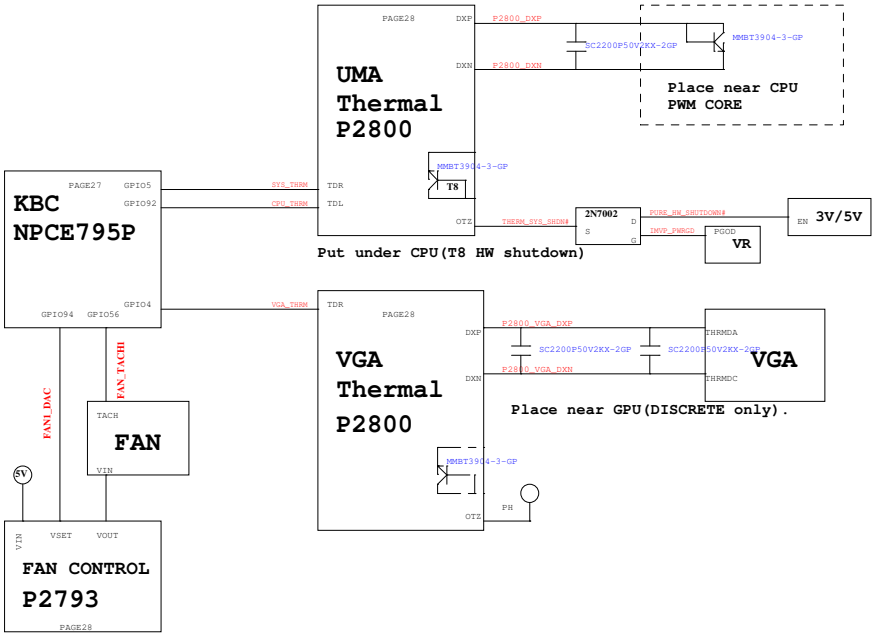
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

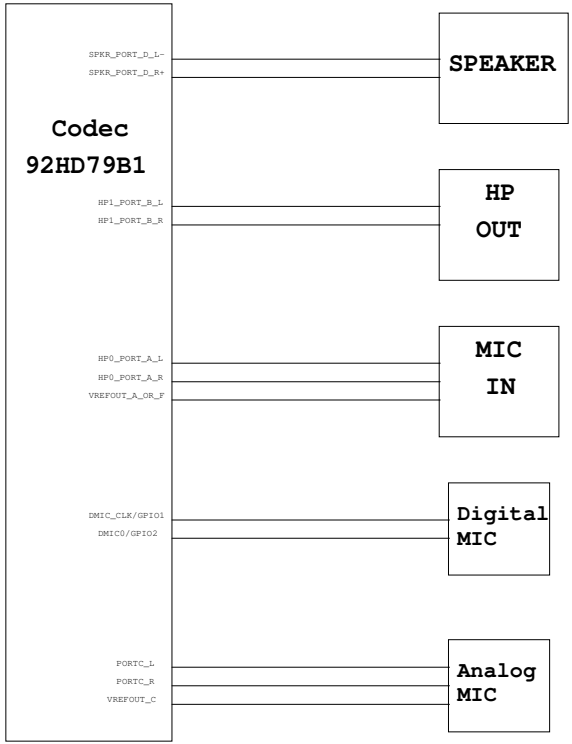
Title	Power Block Diagram	
Size: A3	Document Number: B575	Rev: SA
Date: Friday, March 25, 2011	Sheet 100 of 103	

Thermal Block Diagram

待確認



Audio Block Diagram



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Audio Block Diagram

Size	Document Number	Rev
Custom	B575	SA

Date: Friday, March 25, 2011 Sheet 102 of 103

+1D5V_MINI_WLAN +1D5V_MINI_WLAN 65
+1D5V_MINI_WWAN +1D5V_MINI_WWAN 66
+3V_MINI_WLAN +3V_MINI_WLAN 65
+3V_MINI_WWAN +3V_MINI_WWAN 66
0D75V_PWR 0D75V_PWR 46
0D75V_S0 0D75V_S0 14,15,36,46
1D05V_LAN_S5 1D05V_LAN_S5 31
1D05V_S0 1D05V_S0 4,6,45
1D1V_PWR 1D1V_PWR 45
1D1V_S0 1D1V_S0 20,36
1D1V_S5 1D1V_S5 20,36,45
1D5V_PWR 1D5V_PWR 46
1D5V_S0 1D5V_S0 29,36,65,66
1D5V_S3 1D5V_S3 5,6,14,15,36,46,93,97
1D5V_VGA_S0 1D5V_VGA_S0 84,86,88,89,93
1D8V_PWR 1D8V_PWR 47
1D8V_S0 1D8V_S0 6,7,17,20,42,47,71,93
1D8V_VGA_S0 1D8V_VGA_S0 85,86,87,93
1V_PWR 1V_PWR 45
1V_VGA_S0 1V_VGA_S0 83,85,86,87,93
1V_VGA_S0_LDOIN 1V_VGA_S0_LDOIN 93
3D3V_AUX_KBC 3D3V_AUX_KBC 27,39
3D3V_AUX_S5 3D3V_AUX_S5 18,27,28,40,41,60,70,92,97
3D3V_BT_S0 3D3V_BT_S0 63
3D3V_CAMERA_S0 3D3V_CAMERA_S0 49
3D3V_LAN_S5 3D3V_LAN_S5 31,82
3D3V_LAN_VDDSREG 3D3V_LAN_VDDSREG 31
3D3V_PWR 3D3V_PWR 41
3D3V_PWR_2 3D3V_PWR_2 41
3D3V_S0 3D3V_S0 6,7,14,15,17,18,19,20,21,27,28,29,31,36,42,46,49,50,51,56,60,63,64,65,66,67,68,71,78,82,93,97
3D3V_S0_LED 3D3V_S0_LED 78
3D3V_S5 3D3V_S5 7,18,20,21,27,31,36,41,42,45,47,68,78,83,86,97
3D3V_S5_LED 3D3V_S5_LED 78
3D3V_VGA_S0 3D3V_VGA_S0 83,85,86,92,93
3V_FP_S0 3V_FP_S0 64
5V_CRT_S0 5V_CRT_S0 50
5V_HDMI 5V_HDMI 51
5V_LUSB1_S0 5V_LUSB1_S0 62
5V_PWR 5V_PWR 41
5V_PWR_2 5V_PWR_2 41
5V_RUSB2_S0 5V_RUSB2_S0 61,82
5V_RUSB3_S0 5V_RUSB3_S0 61,82
5V_S0 5V_S0 7,28,29,36,50,51,56,64,69,78,86
5V_S5 5V_S5 36,41,42,45,46,47,61,62,65,68,78,92,93,97
5V_USB0_S3 5V_USB0_S3 57,62
A2VDD A2VDD 85
AD+ AD+ 38,40
AD_JK AD_JK 38
AUD_3D3V AUD_3D3V 29
AUD_3D3V_1D5V AUD_3D3V_1D5V 29
AUD_5V AUD_5V 29
AVDD_A2VDDQ AVDD_A2VDDQ 85
AVDD_SATA AVDD_SATA 19,20
AVDD_USB AVDD_USB 20
BIF_VDDC BIF_VDDC 86
BQ24745_VREF BQ24745_VREF 40
BT+ BT+ 39,40,97
DCBATOUT DCBATOUT 36,40,41,42,43,45,46,47,49,92,97
DCBATOUT_LCD DCBATOUT_LCD 49
DDR_VREF_S3 DDR_VREF_S3 5,14,15,46
DPAB_VDD10 DPAB_VDD10 87
DPAB_VDD18 DPAB_VDD18 87
DPEF_VDD10 DPEF_VDD10 87
DPEF_VDD18 DPEF_VDD18 87
DPLL_PVDD DPLL_PVDD 85
DPLL_VDDC DPLL_VDDC 85
LCDVDD LCDVDD 49
MPV18 MPV18 86
PCIE_VDDR PCIE_VDDR 17,20
PWR_1D5V_DCBATOUT PWR_1D5V_DCBATOUT 46
PWR_3D3V_DCBATOUT PWR_3D3V_DCBATOUT 41
PWR_5VD3V_VREF PWR_5VD3V_VREF 41
PWR_5V_DCBATOUT PWR_5V_DCBATOUT 41
PWR_DCBATOUT_1V PWR_DCBATOUT_1V 45
PWR_DCBATOUT_VGA_CORE PWR_DCBATOUT_VGA_CORE 92
RTC_AUX_S5 RTC_AUX_S5 17,27,60
RTC_BAT RTC_BAT 60
RUN_ENABLE RUN_ENABLE 36
RUN_ENABLE_S RUN_ENABLE_S 36
SIM_PWR SIM_PWR 67
SPV18 SPV18 86
TSVDD TSVDD 85
UIM_PWR UIM_PWR 66,67
VCC_CORE VCC_CORE 6,42
VDD_NB VDD_NB 6,42,43
VDDAN_3D3V_HWM VDDAN_3D3V_HWM 20
VDDC_CT VDDC_CT 86
VDDIO_AZ VDDIO_AZ 20
VDDPL_1D1V VDDPL_1D1V 20
VDDPL_3D3V VDDPL_3D3V 20
VGA_CORE VGA_CORE 86,92
VGA_CORE_PWR VGA_CORE_PWR 92
AU_GND AU_GND 29,82
CHG_AGND CHG_AGND 40
AVSSQ AVSSQ 85
GNDA_VCORE GNDA_VCORE 42

<Variant Name>

Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Change History

Size: A2 | Document Number: B575 | Rev: SA

Date: Monday, March 08, 2010 | Sheet 1 of 103