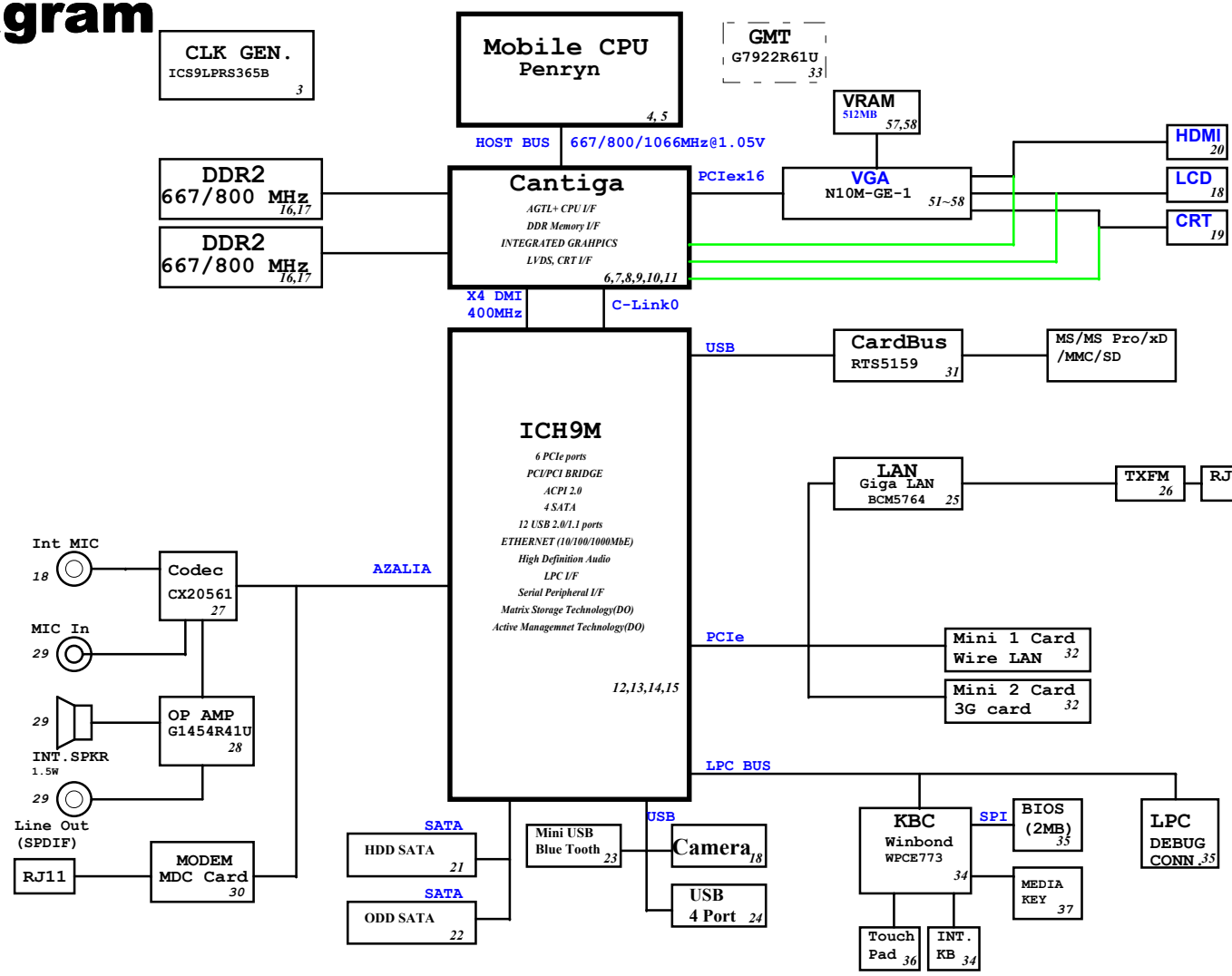
SJV50 Block Diagram

Project code: 91.4BU01.001
PCB P/N : 48.4BU01.0SB
REVISION : 08244-SB



PCB STACKUP

TOP		L1
GND		L2
S		L3
S		L4
GND		L5
BOTTOM		L6

SYSTEM DC/DC ISL62392 — 41

INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(7A) 5V_AUX_S5 3D3V_AUX_S5

SYSTEM DC/DC TPS51124 — 42

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(9A) 1D8V_S3(13A)

RT9026 — 43

1D8V_S3	DDR_VREF_S3 (1.2A)

RT9018 — 44

1D8V_S3	1D1V_S0(2A)

RT9018 — 44

1D8V_S3	1D5V_S0 (2.5A)

CHARGER ISL88731A — 46

INPUTS	OUTPUTS
DCBATOUT	BT+

CPU DC/DC ISL6266A — 40

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 38A

VGA_CORE RT8202 — 48

INPUTS	OUTPUTS
DCBATOUT	VGA_CORE 13A

GFXCORE ISL6263A — 45

INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE (11A)

SJV50

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Title: BLOCK DIAGRAM

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ICH9M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9M Integrated Pull-up and Pull-down Resistors

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) **1=The iTPM Host Interface is disalbed(default)**
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality (default)**
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1= Disabled (default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) **11 = Disabled (default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation(Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 =Digital display Port and PCIe are operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	**0 =No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG/12/CFG13 straps can be enabled at any time.

SJV50

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Title: **Reference**

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A3	SJV50	SA

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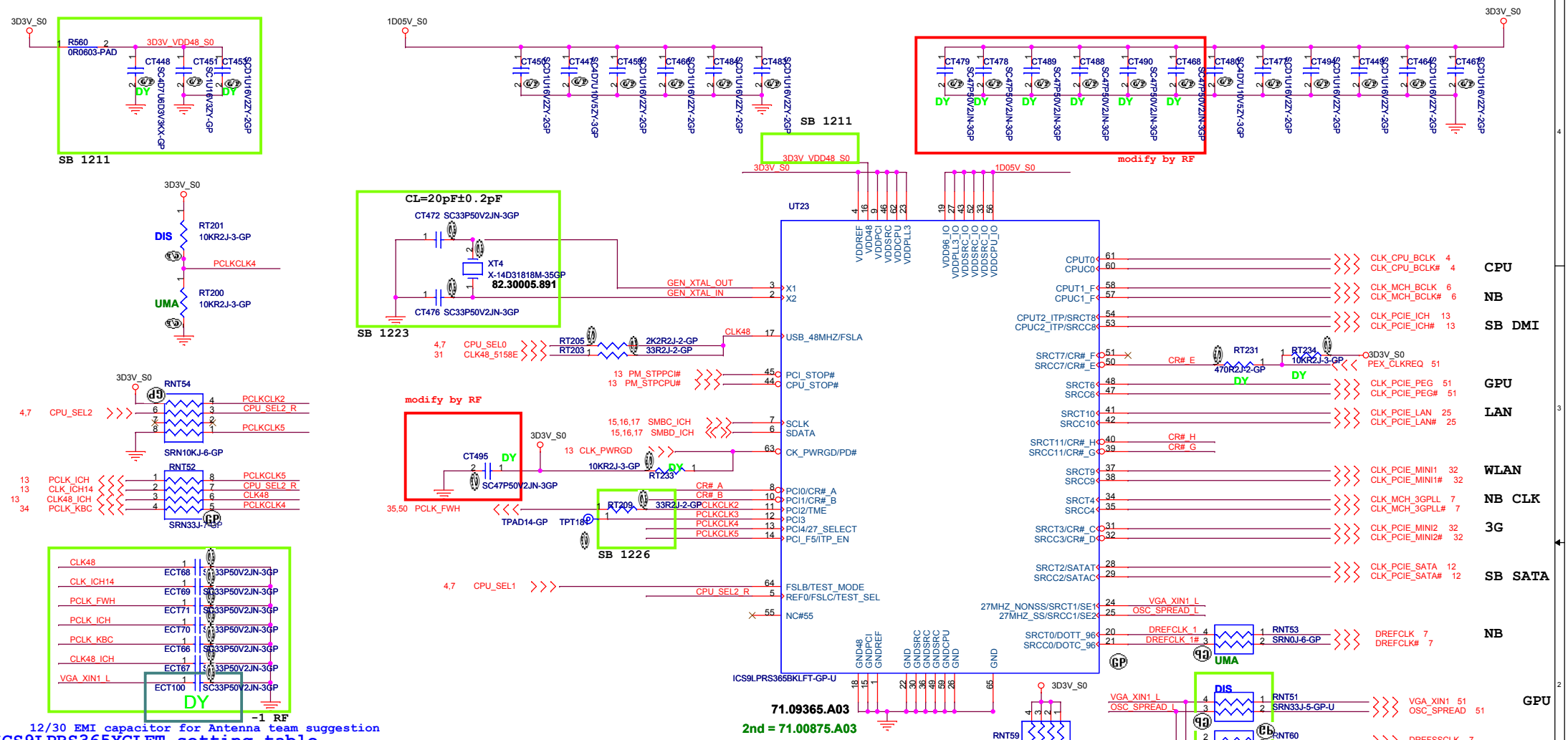

ICS9LPRS365YGLFT setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3	
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#
SRCT3/CR#_C	Byte 5, bit 3 0 = SRC3 enabled (default) 1= CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1= CR#_C controls SRC2 pair

PIN NAME	DESCRIPTION
SRCC3/CR#_D	Byte 5, bit 1 0 = SRC3 enabled (default) 1= CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1= CR#_D controls SRC4 pair
SRCC7/CR#_E	Byte 6, bit 7 0 = SRC7# enabled (default) 1= CR#_F controls SRC6
SRCT7/CR#_F	Byte 6, bit 6 0 = SRC7 enabled (default) 1= CR#_F controls SRC8
SRCC11/CR#_G	Byte 6, bit 5 0 = SRC11# enabled (default) 1= CR#_G controls SRC9
SRCT11/CR#_H	Byte 6, bit 4 0 = SRC11 enabled (default) 1= CR#_H controls SRC10

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M

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Title: *Clock Generator*

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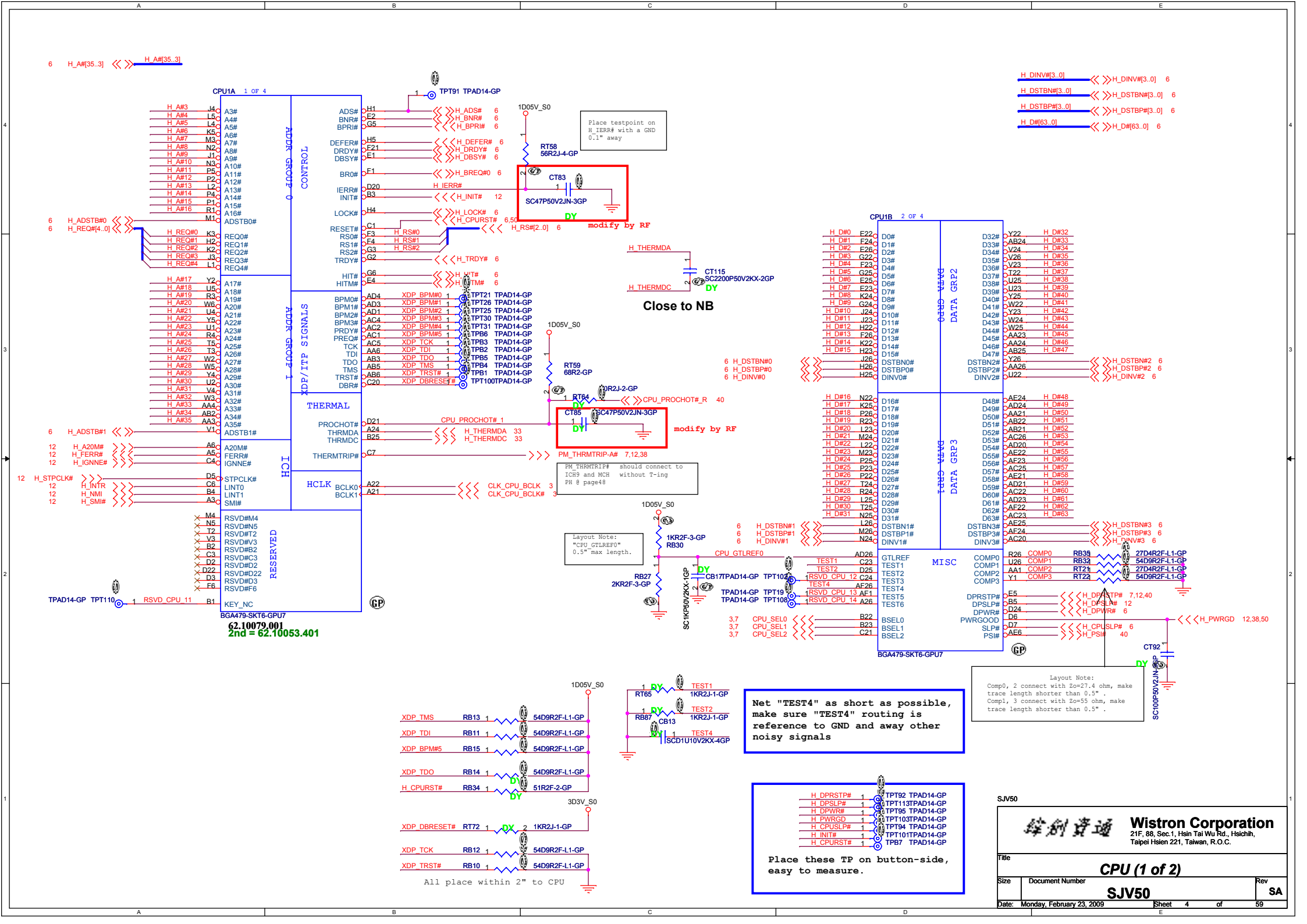
CPU1A 1 OF 4
ADDR GRP0
CONTROL
ADDR GRP1
XDP/ITP SIGNALS
THERMAL
ITCH
HCLK
RESERVED
BGA479-SKT6-GPU7
CPU1B 2 OF 4
DATA GRP2
DATA GRP1
DATA GRP3
DATA GRP0
MISC
BGA479-SKT6-GPU7
Close to NB
modify by RF
Place testpoint on H_IERR# with a GND 0.1" away
PM_THRMTRIP# should connect to ICH9 and MCH with T-ing PH @ page48
Layout Note: "CPU_GTLREF0" 0.5" max length.
Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" . Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .
Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals
Place these TP on button-side, easy to measure.
All place within 2" to CPU
62.10079.001
2nd = 62.10053.401
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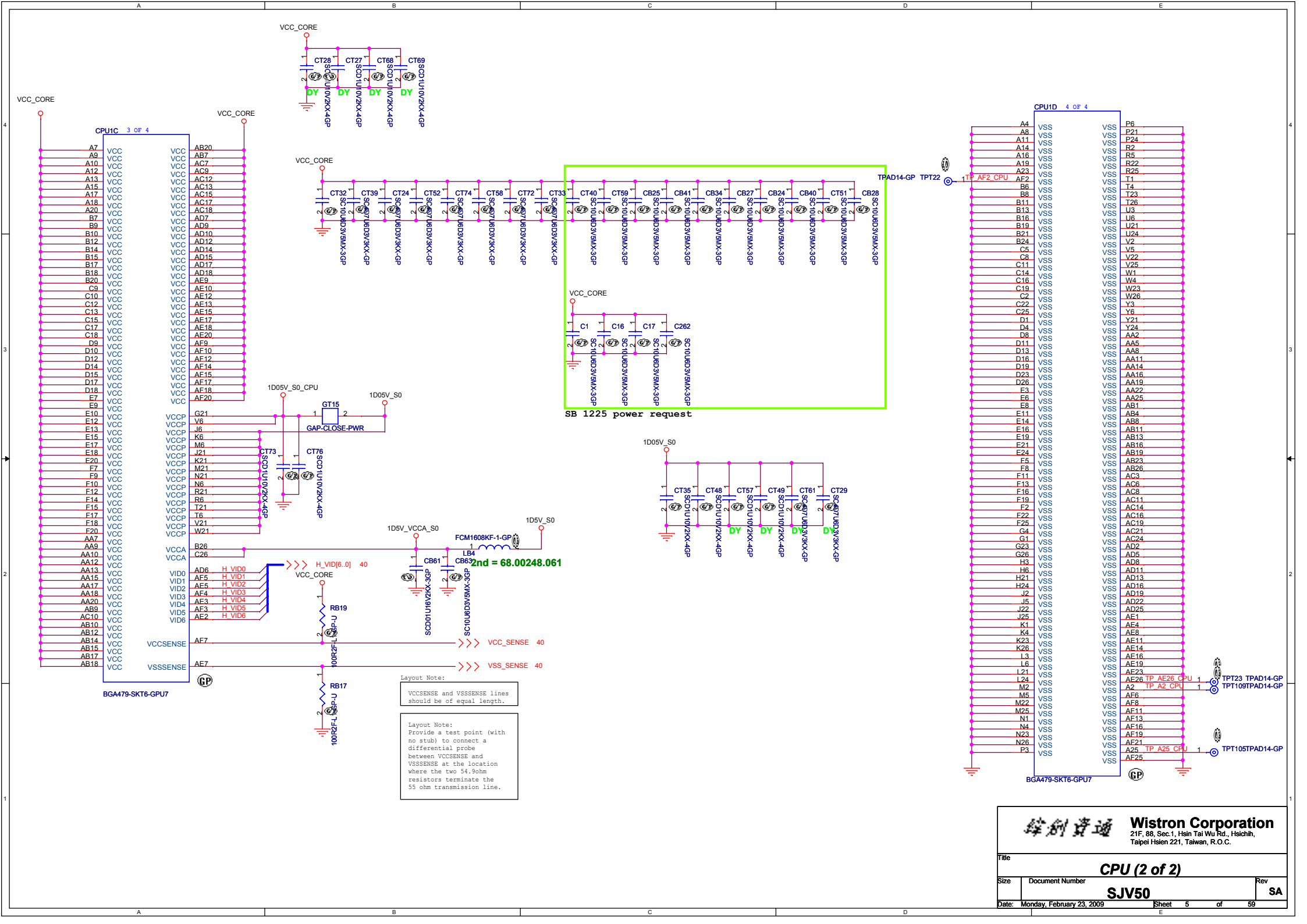
VCC_CORE
CPU1C 3 OF 4
BGA479-SKT6-GPU7
CT28 CT27 CT68 CT69
SCD1U10V2KX-4GP
DY
CT32 CT39 CT24 CT52 CT74 CT58 CT72 CT33 CT40 CT59 CB25 CB41 CB34 CB27 CB24 CB40 CT51 CB28
SC10U6D3V5MX-3GP
SC407U6D3V3KX-GP
SB 1225 power request
C1 C16 C17 C262
1D05V_S0_CPU
1D05V_S0
GT15
GAP-CLOSE-PWR
CT73 CT76
1D05V_VCCA_S0
FCM1608KF-1-GP
LB4
2nd = 68.00248.061
CB61 CB63
SCD01U16V2KX-GP
SC10U6D3V5MX-3GP
H_VID[6..0] 40
RB19 RB17
100R2F-L-GP-U
VCC_SENSE 40
VSS_SENSE 40
Layout Note:
VCCSENSE and VSSSENSE lines should be of equal length.
Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.
TPAD14-GP TPT22
TP_AF2_CPU
CPU1D 4 OF 4
TP_AE26_CPU TPT23 TPAD14-GP
TP_A2_CPU TPT109TPAD14-GP
TP_A25_CPU TPT105TPAD14-GP
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Title
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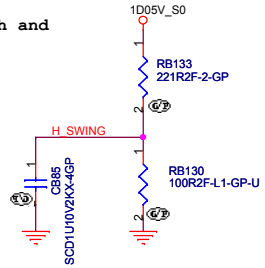
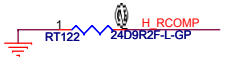
H_SWING routing Trace width and Spacing use 10 / 20 mil

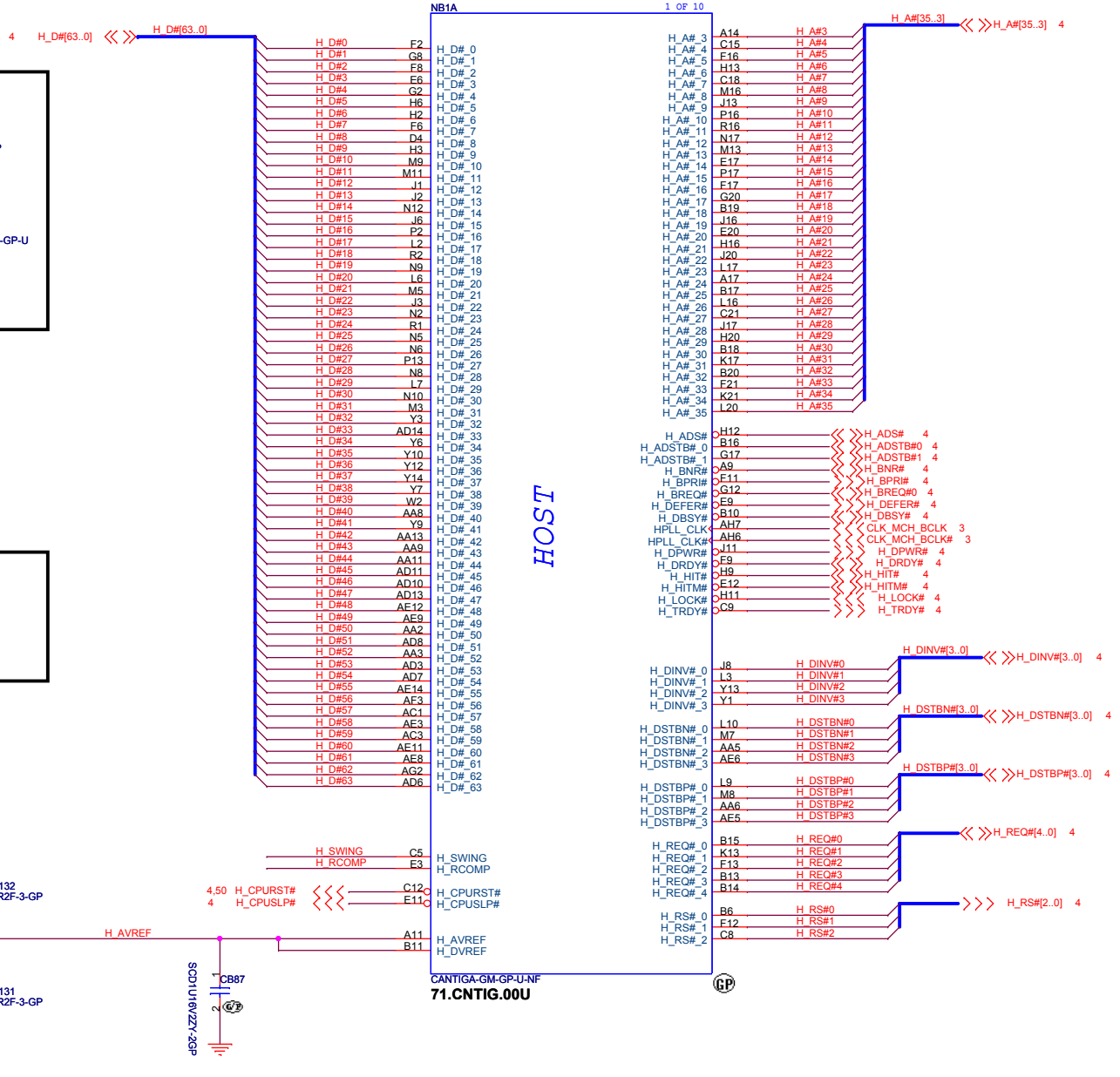
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")



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Title: Cantiga (1 of 6)

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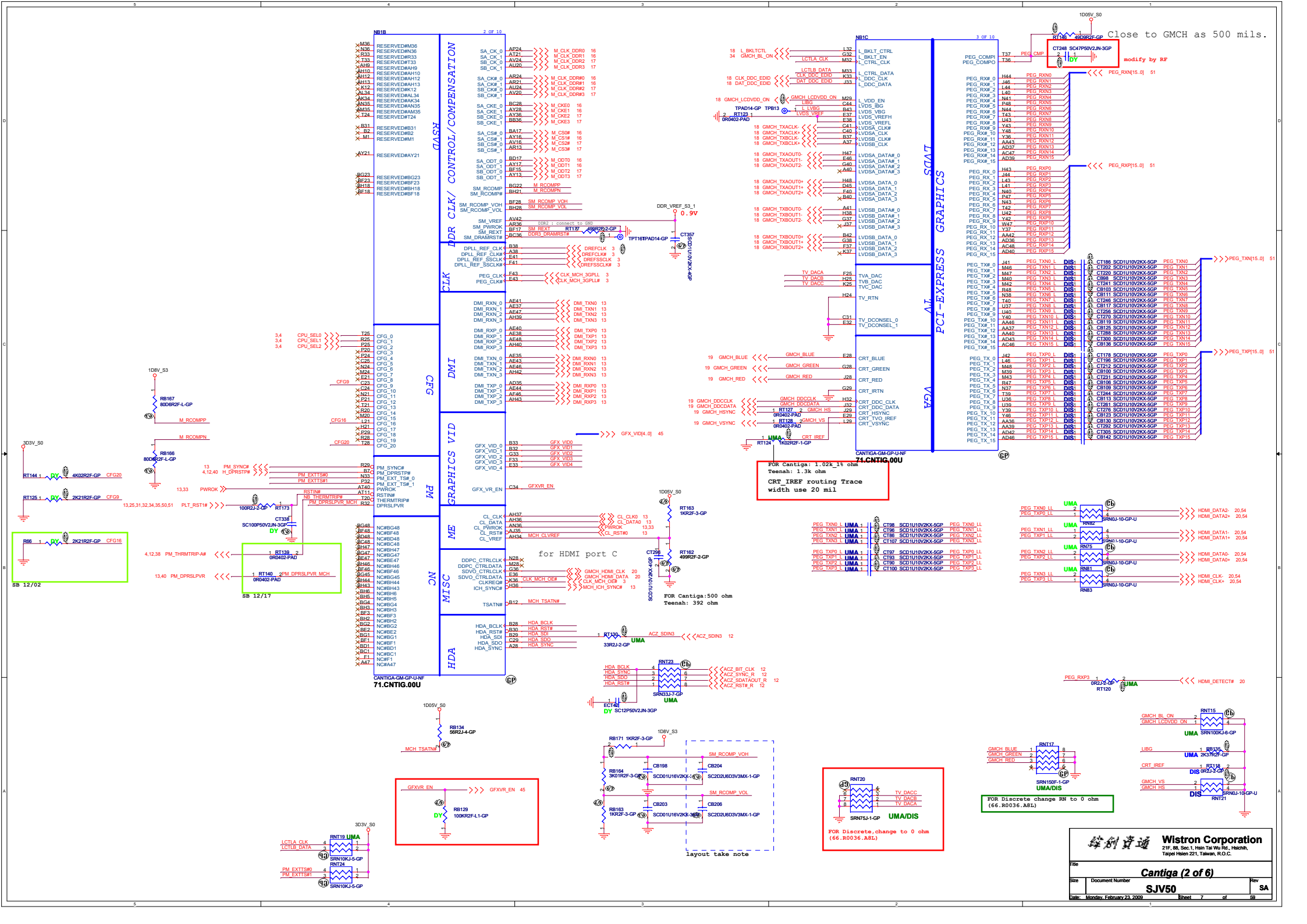
Close to GMCH as 500 mils.
modify by RF
NB1B
NB1C
RESERVED
CLK_MCH_3GPLL
CLK_MCH_3GPLL#
DDR_VREF_S3_1
0.9V
DDR2 : connect to GND
DDR3_DRAMRST#
SM_REXT
SM_RCOMP_VOH
SM_RCOMP_VOL
SM_PWROK
SM_RCOMP
SM_RCOMP#
M_CLK_DDR0
M_CLK_DDR1
M_CLK_DDR2
M_CLK_DDR3
M_CLK_DDR#0
M_CLK_DDR#1
M_CLK_DDR#2
M_CLK_DDR#3
M_CKE0
M_CKE1
M_CKE2
M_CKE3
M_CS0#
M_CS1#
M_CS2#
M_CS3#
M_ODT0
M_ODT1
M_ODT2
M_ODT3
M_RCOMPP
M_RCOMPN
DREFCLK#
DREFSSCLK
DREFSSCLK#
DMI_TXN0
DMI_TXN1
DMI_TXN2
DMI_TXN3
DMI_TXP0
DMI_TXP1
DMI_TXP2
DMI_TXP3
DMI_RXN0
DMI_RXN1
DMI_RXN2
DMI_RXN3
DMI_RXP0
DMI_RXP1
DMI_RXP2
DMI_RXP3
GFX_VID0
GFX_VID1
GFX_VID2
GFX_VID3
GFX_VID4
GFX_VID[4..0]
GFX_VR_EN
CL_CLK0
CL_DATA0
CL_PWROK
CL_RST#0
CL_VREF
CL_CLK
CL_DATA
CL_PWROK
CL_RST#
CL_VREF
MCH_CLVREF
CL_RST#
for HDMI port C
GMCH_HDMI_CLK
GMCH_HDMI_DATA
CLK_MCH_OE#
CLK_MCH_OE#
GMCH_MCH_SYNC#
MCH_ICH_SYNC#
TSATN#
HDA_BCLK
HDA_RST#
HDA_SDI
HDA_SDO
HDA_SYNC
ACZ_SDIN3
HDA_BIT_CLK
ACZ_SYNC_R
ACZ_SDATAOUT_R
ACZ_RST#_R
L_BKLTCTL
GMCH_BL_ON
LCTLA_CLK
LCTLB_DATA
CLK_DDC_EDID
DAT_DDC_EDID
GMCH_LCDVDD_ON
LIBG
LVDS_VBG
LVDS_VSEF
LVDS_VREFH
LVDS_VREFL
LVDSA_CLK#
LVDSA_CLK
LVDSB_CLK#
LVDSB_CLK
GMCH_TXACLK-
GMCH_TXACLK+
GMCH_TXBCLK+
GMCH_TXBCLK+
GMCH_TXAOUT0-
GMCH_TXAOUT1-
GMCH_TXAOUT2-
GMCH_TXAOUT0+
GMCH_TXAOUT1+
GMCH_TXAOUT2+
GMCH_TXBOUT0-
GMCH_TXBOUT1-
GMCH_TXBOUT2-
GMCH_TXBOUT0+
GMCH_TXBOUT1+
GMCH_TXBOUT2+
LVDSA_DATA#_0
LVDSA_DATA#_1
LVDSA_DATA#_2
LVDSA_DATA#_3
LVDSA_DATA_0
LVDSA_DATA_1
LVDSA_DATA_2
LVDSA_DATA_3
LVDSB_DATA#_0
LVDSB_DATA#_1
LVDSB_DATA#_2
LVDSB_DATA#_3
LVDSB_DATA_0
LVDSB_DATA_1
LVDSB_DATA_2
LVDSB_DATA_3
TV_DACA
TV_DACB
TV_DACC
TVA_DAC
TVB_DAC
TVC_DAC
TV_RTN
TV_DCONSEL_0
TV_DCONSEL_1
GMCH_BLUE
GMCH_GREEN
GMCH_RED
CRT_BLUE
CRT_GREEN
CRT_RED
CRT_IRTN
GMCH_DDCCLK
GMCH_DDCDATA
GMCH_HSYNC
GMCH_VSYNC
CRT_DDC_CLK
CRT_DDC_DATA
CRT_HSYNC
CRT_TVO_IREF
CRT_VSYNC
CRT_IREF
PEG_COMPI
PEG_COMPO
PEG_RXN[15..0]
PEG_RXP[15..0]
PEG_TXN[15..0]
PEG_TXP[15..0]
PEG_RX#_0
PEG_RX#_1
PEG_RX#_2
PEG_RX#_3
PEG_RX#_4
PEG_RX#_5
PEG_RX#_6
PEG_RX#_7
PEG_RX#_8
PEG_RX#_9
PEG_RX#_10
PEG_RX#_11
PEG_RX#_12
PEG_RX#_13
PEG_RX#_14
PEG_RX#_15
PEG_RX_0
PEG_RX_1
PEG_RX_2
PEG_RX_3
PEG_RX_4
PEG_RX_5
PEG_RX_6
PEG_RX_7
PEG_RX_8
PEG_RX_9
PEG_RX_10
PEG_RX_11
PEG_RX_12
PEG_RX_13
PEG_RX_14
PEG_RX_15
PEG_TX#_0
PEG_TX#_1
PEG_TX#_2
PEG_TX#_3
PEG_TX#_4
PEG_TX#_5
PEG_TX#_6
PEG_TX#_7
PEG_TX#_8
PEG_TX#_9
PEG_TX#_10
PEG_TX#_11
PEG_TX#_12
PEG_TX#_13
PEG_TX#_14
PEG_TX#_15
PEG_TX_0
PEG_TX_1
PEG_TX_2
PEG_TX_3
PEG_TX_4
PEG_TX_5
PEG_TX_6
PEG_TX_7
PEG_TX_8
PEG_TX_9
PEG_TX_10
PEG_TX_11
PEG_TX_12
PEG_TX_13
PEG_TX_14
PEG_TX_15
CANTIGA-GM-GP-U-NF
71.CNTIG.00U
FOR Cantiga: 1.02k_1% ohm
Teenah: 1.3k ohm
CRT_IREF routing Trace width use 20 mil
FOR Cantiga:500 ohm
Teenah: 392 ohm
SB 12/02
SB 12/17
layout take note
FOR Discrete change RN to 0 ohm (66.R0036.A8L)
FOR Discrete,change to 0 ohm (66.R0036.A8L)
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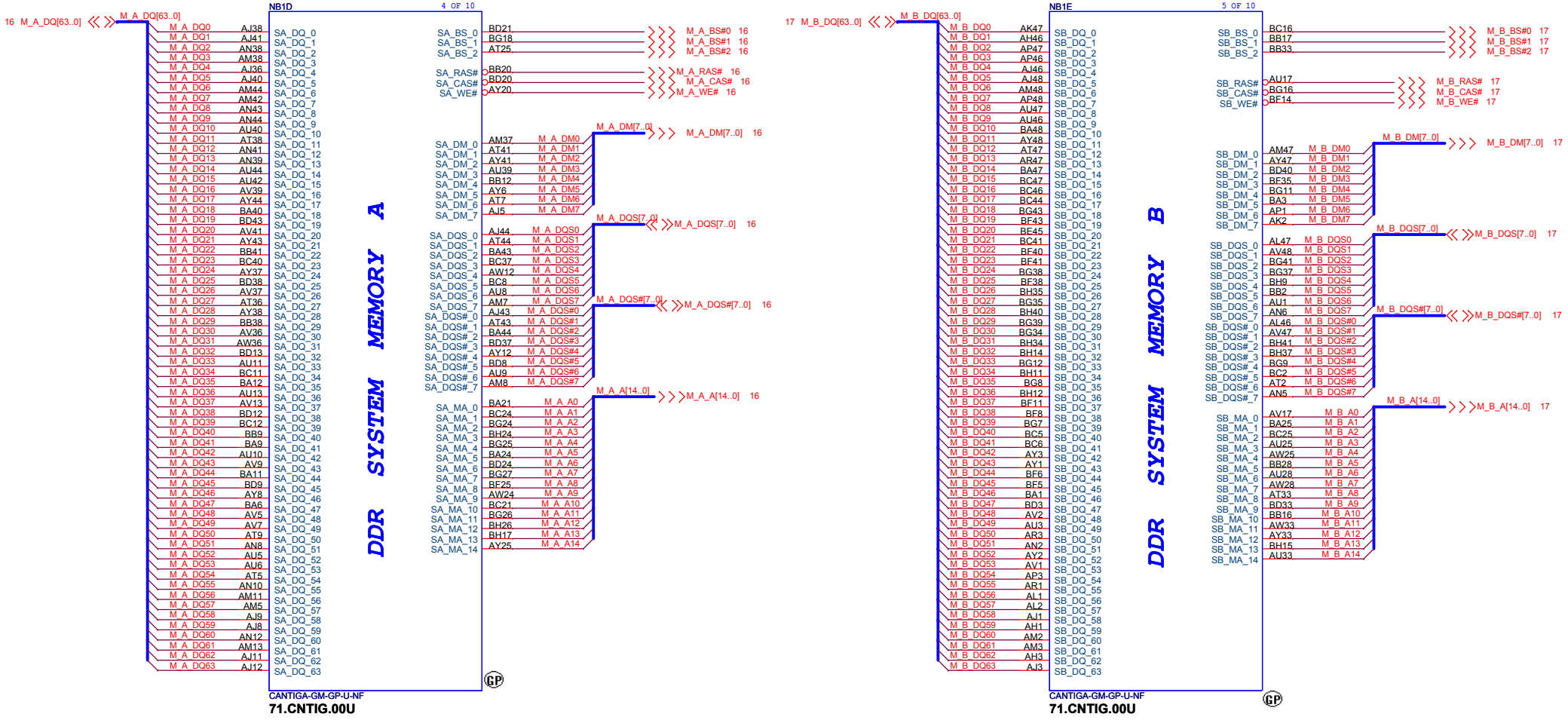

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Title: *Cantiga (3 of 6)*

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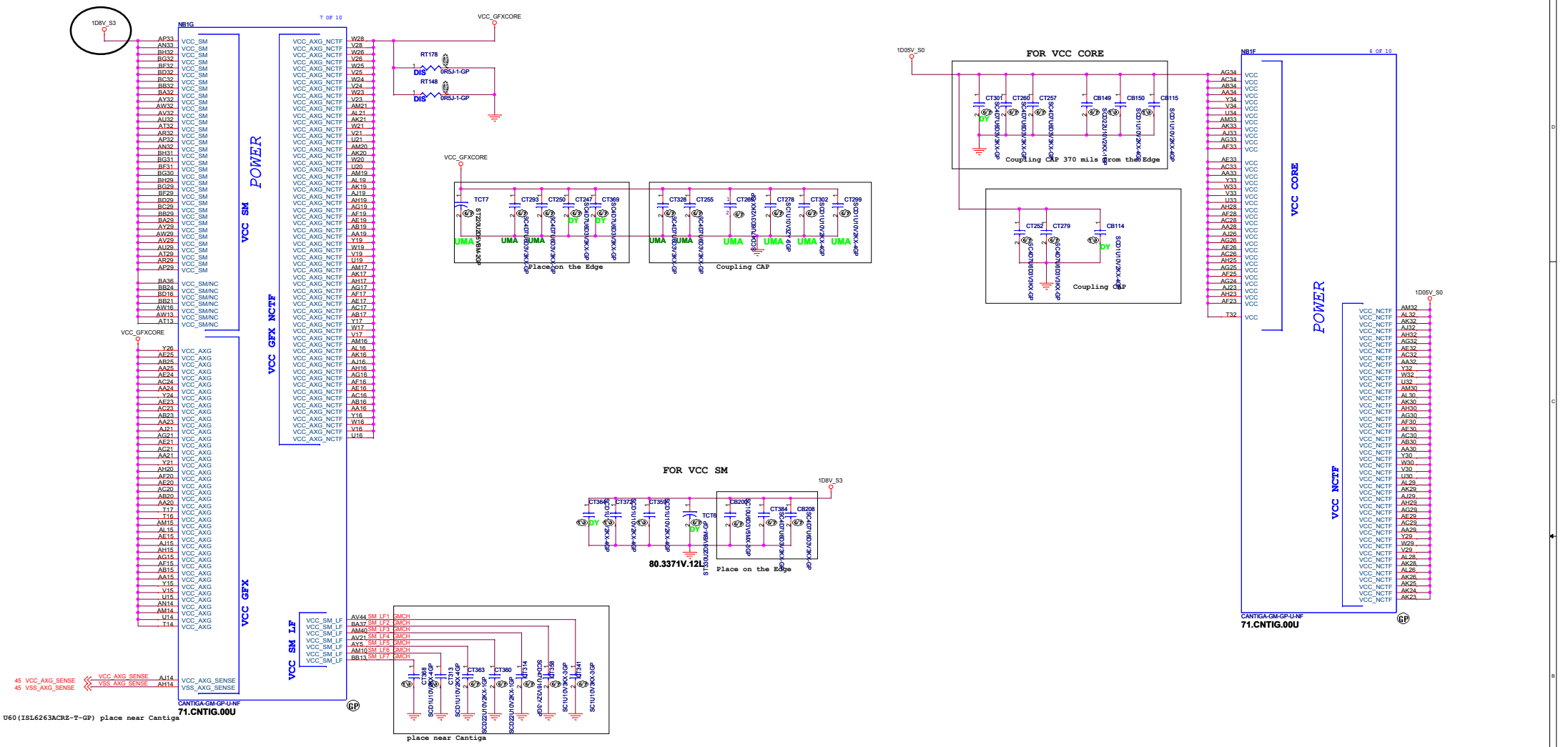

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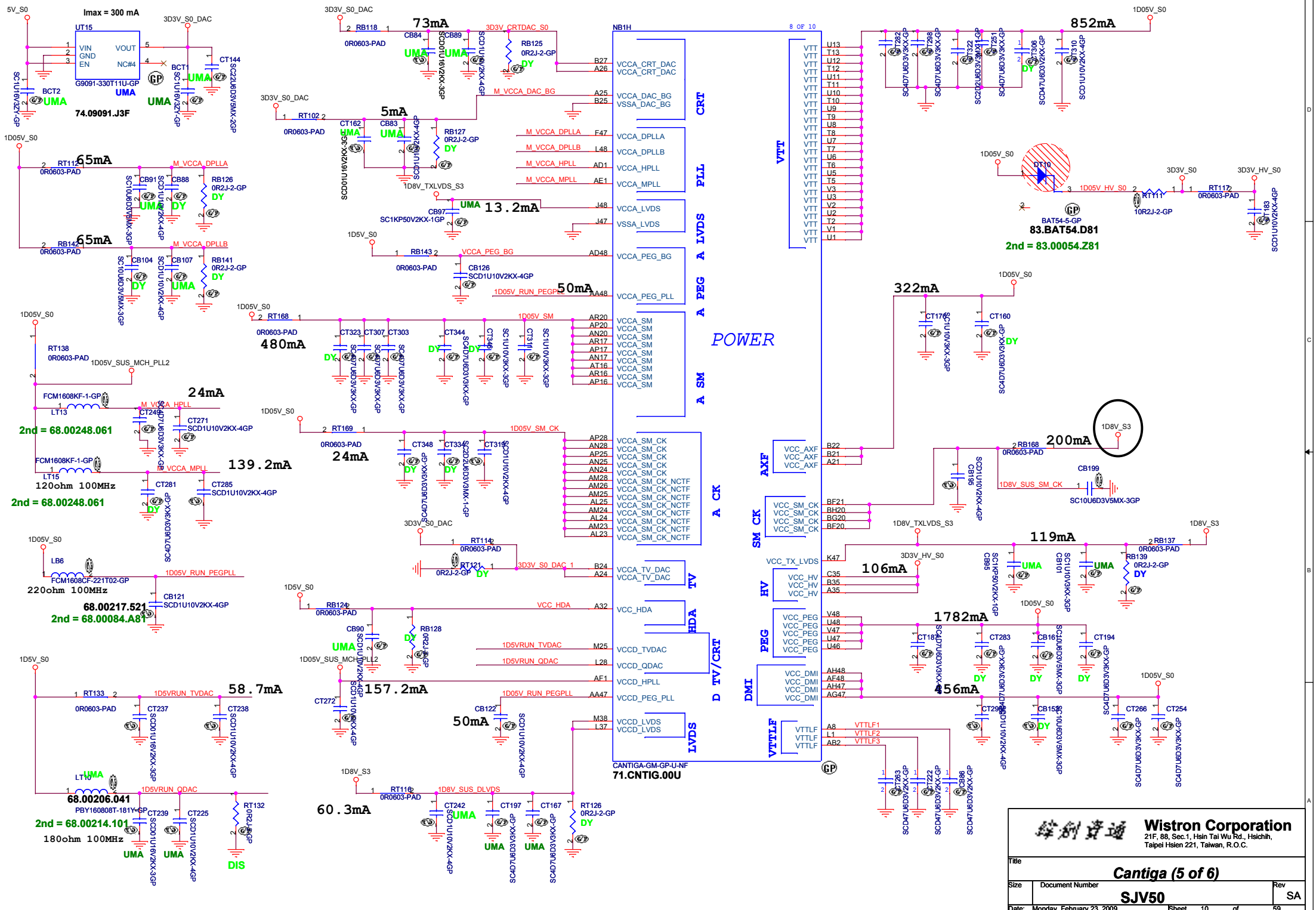
Imax = 300 mA
UT15
G9091-330T11U-GP
74.09091.J3F
73mA
5mA
65mA
65mA
13.2mA
50mA
480mA
24mA
139.2mA
68.00248.061
68.00248.061
68.00217.521
68.00084.A81
58.7mA
157.2mA
50mA
68.00206.041
68.00214.101
60.3mA
852mA
322mA
200mA
119mA
106mA
1782mA
456mA
83.BAT54.D81
83.00054.Z81
NB1H
8 OF 10
CRT
PLL
LVDS
A PEG
A SM
A CK
TV
HDA
D TV/CRT
LVDS
VTT
AXF
SM CK
HV
PEG
DMI
VTTLF
POWER
CANTIGA-GM-GP-U-NF
71.CNTIG.00U
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Cantiga (5 of 6)
Size
Document Number
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Rev
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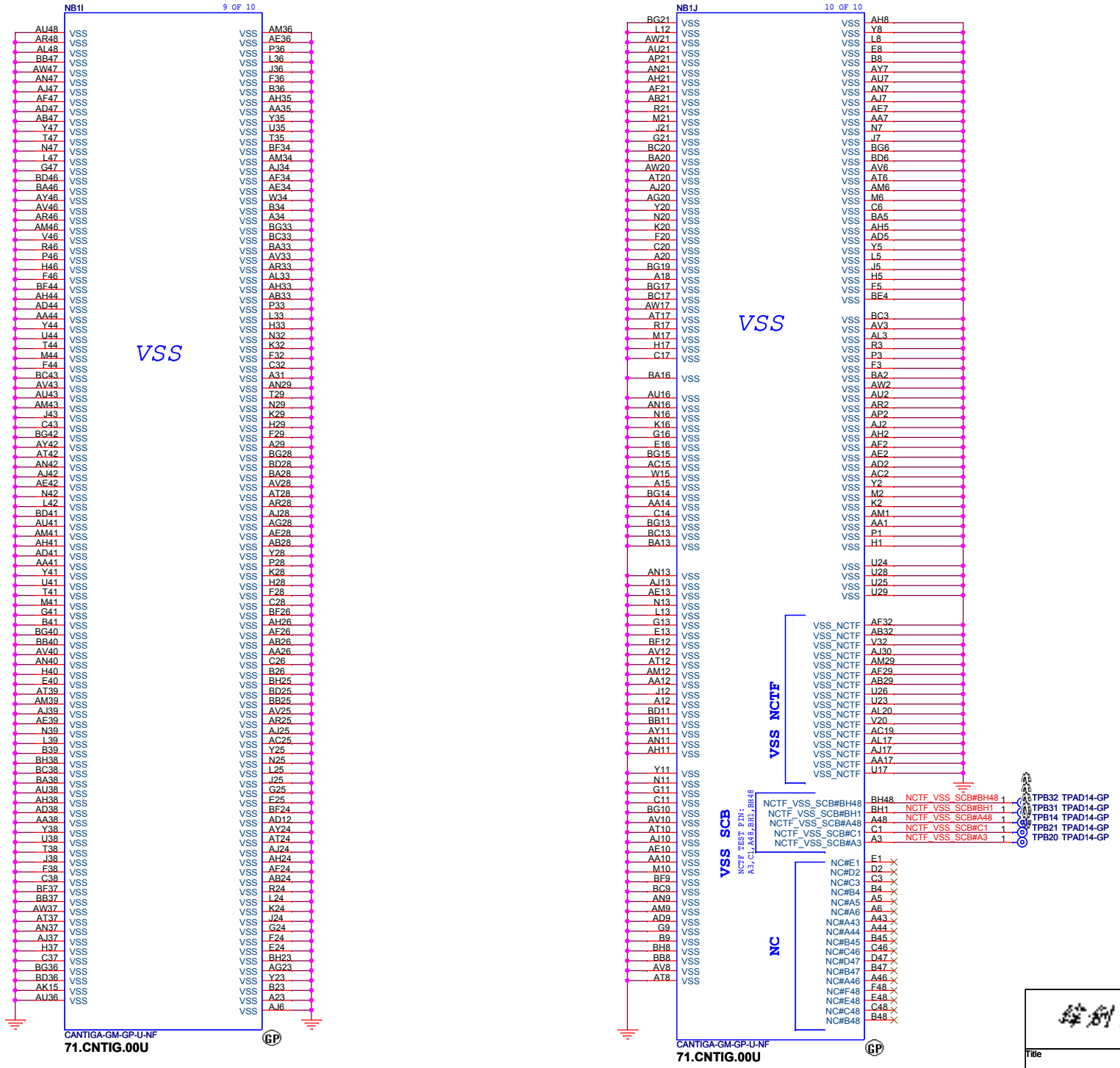
Sheet 10 of 59



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Title: *Cantiga (6 of 6)*

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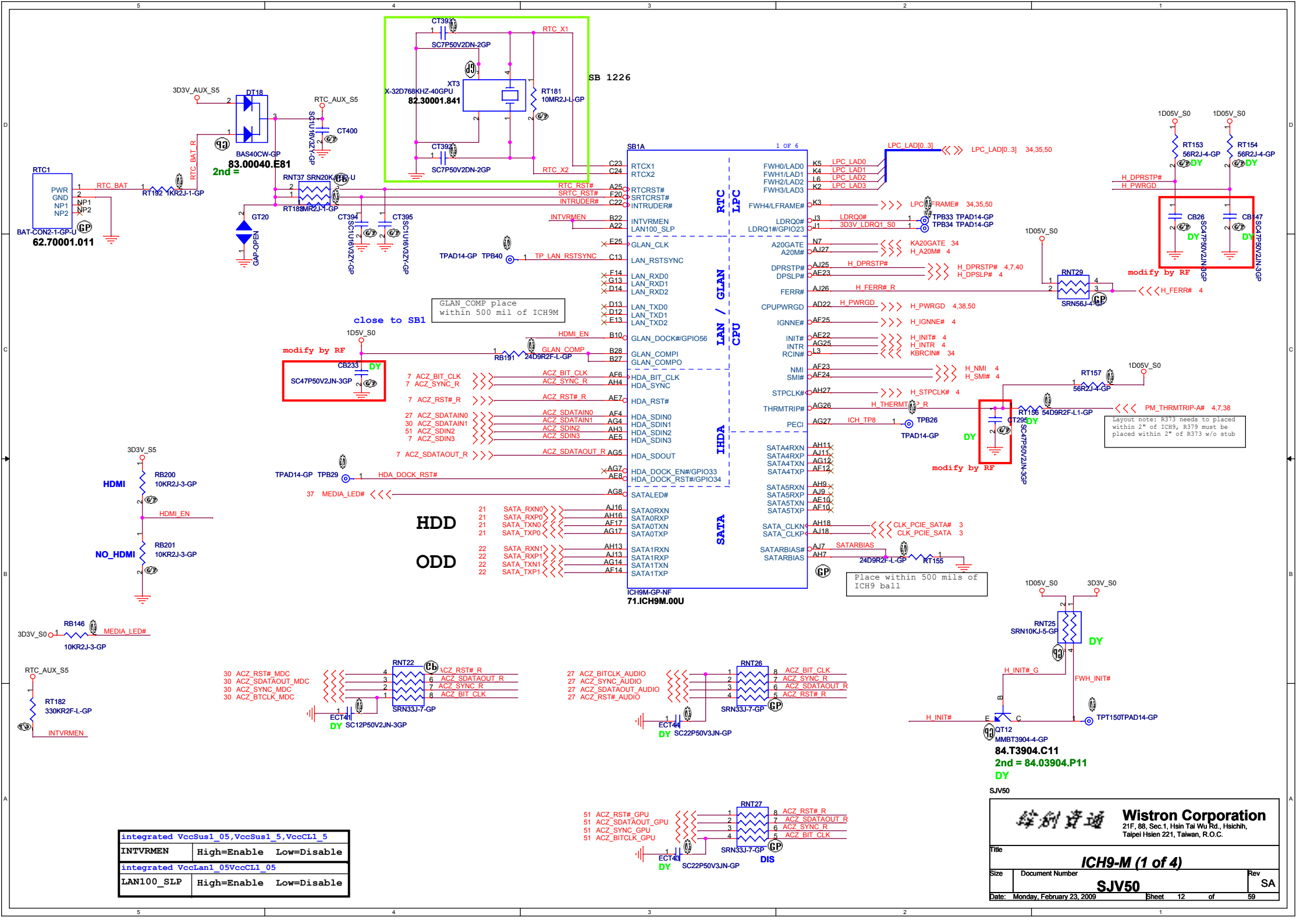
SB 1226
SB1A
ICH9M-GP-NF
71.ICH9M.00U
RTC
LPC
LAN / GLAN
CPU
HDA
SATA
HDD
ODD
close to SB1
GLAN_COMP place within 500 mil of ICH9M
modify by RF
Place within 500 mils of ICH9 ball
Layout note: R373 needs to placed within 2" of ICH9, R373 must be placed within 2" of R373 w/o stub
HDMI
NO_HDMI
83.00040.E81
2nd =
62.70001.011
84.T3904.C11
2nd = 84.03904.P11
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
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ICH9-M (1 of 4)
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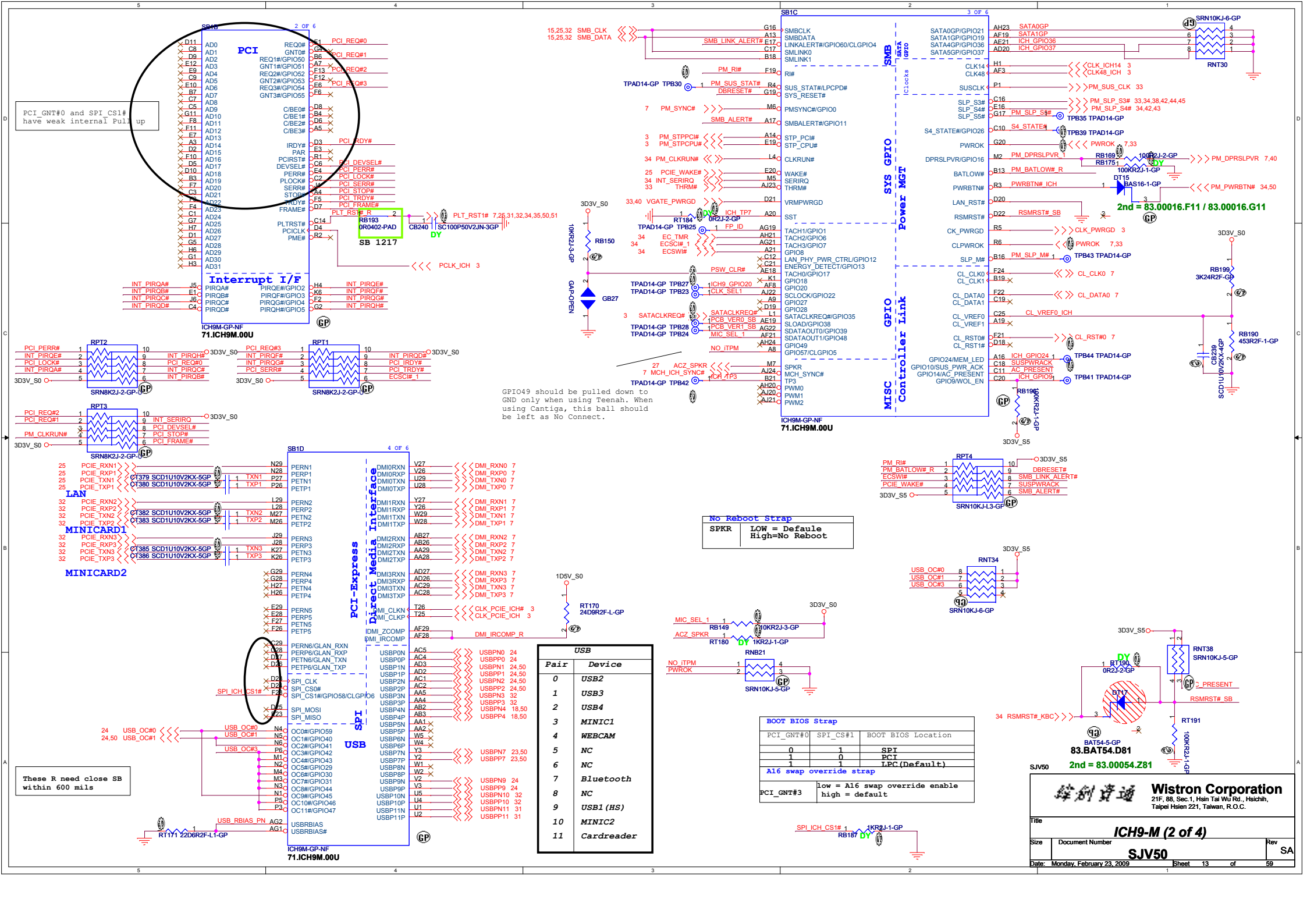
PCI_GNT#0 and SPI_CS1# have weak internal Pull up
PCI
Interrupt I/F
ICH9M-GP-NF
71.ICH9M.00U
SB 1217
SB1C
SMB
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
ICH9M-GP-NF
71.ICH9M.00U
GPIO49 should be pulled down to GND only when using Teenah. When using Cantiga, this ball should be left as No Connect.
SB1D
PCI-Express
Direct Media Interface
SPI
USB
ICH9M-GP-NF
71.ICH9M.00U
LAN
MINICARD1
MINICARD2
These R need close SB within 600 mils
No Reboot Strap
SPKR
LOW = Defaule
High=No Reboot
USB
Pair
Device
0
USB2
1
USB3
2
USB4
3
MINIC1
4
WEBCAM
5
NC
6
NC
7
Bluetooth
8
NC
9
USB1(HS)
10
MINIC2
11
Cardreader
BOOT BIOS Strap
PCI_GNT#0
SPI_CS#1
BOOT BIOS Location
0
1
SPI
1
0
PCI
1
1
LPC(Default)
A16 swap override strap
PCI_GNT#3
low = A16 swap override enable
high = default
2nd = 83.00016.F11 / 83.00016.G11
2nd = 83.00054.Z81
83.BAT54.D81
SJV50
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9-M (2 of 4)
Size
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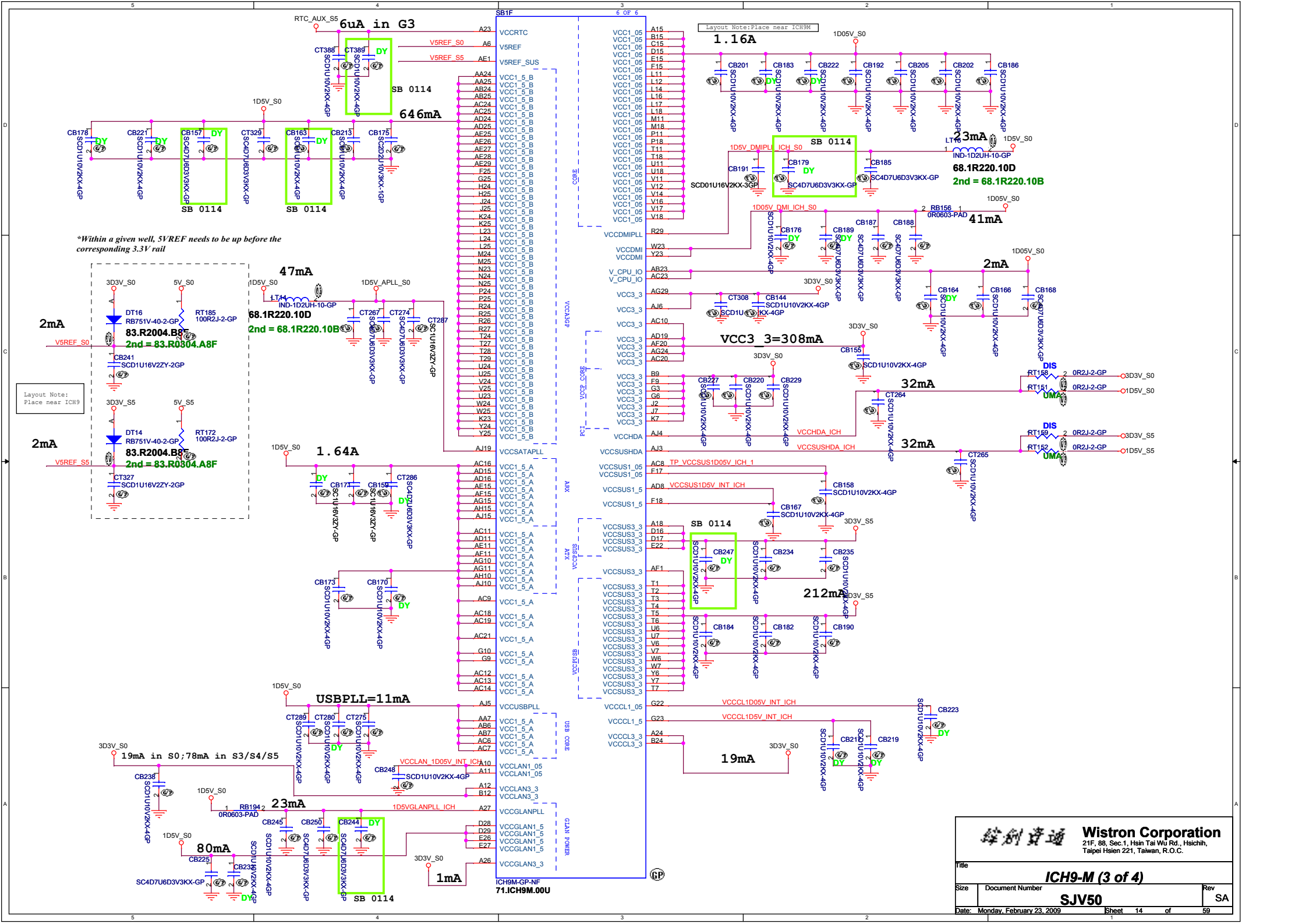
6uA in G3
SB 0114
646mA
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
47mA
68.1R220.10D
2nd = 68.1R220.10B
2mA
83.R2004.B8F
2nd = 83.R0304.A8F
Layout Note: Place near ICH9
1.64A
USBPLL=11mA
19mA in S0;78mA in S3/S4/S5
23mA
80mA
1mA
1.16A
41mA
VCC3_3=308mA
32mA
212mA
19mA
ICH9M-GP-NF
71.ICH9M.00U
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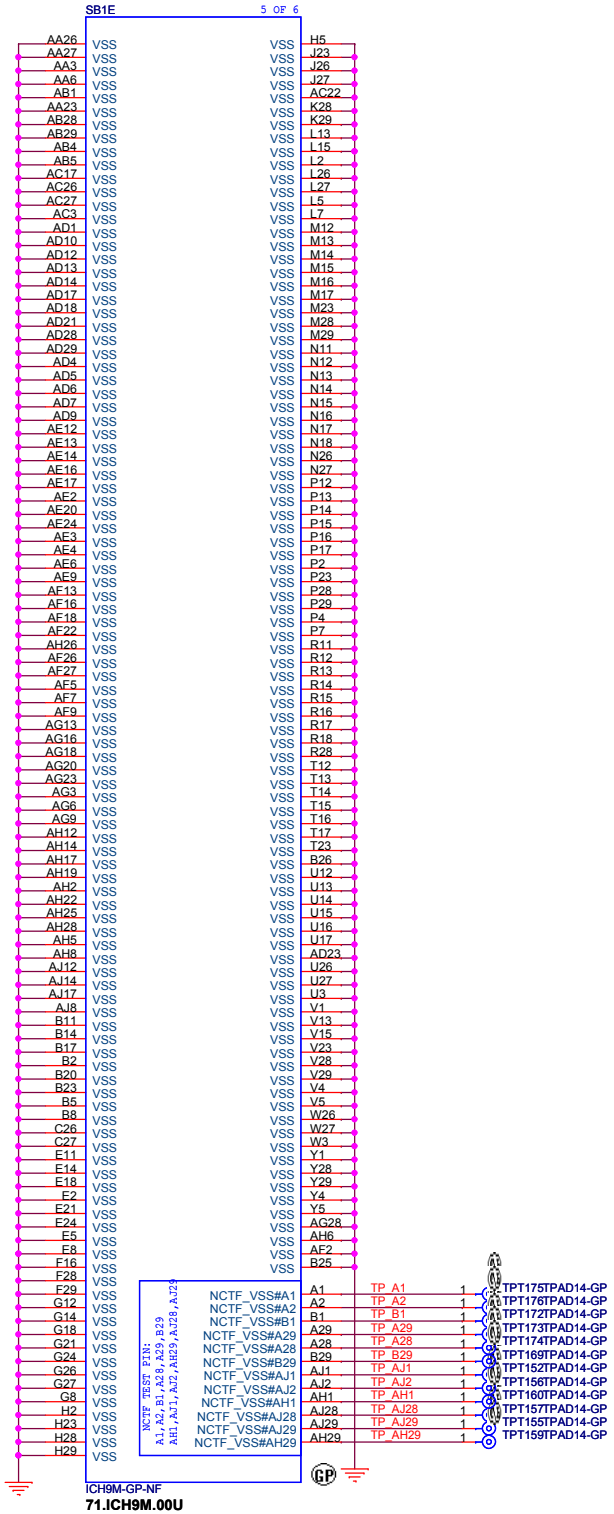

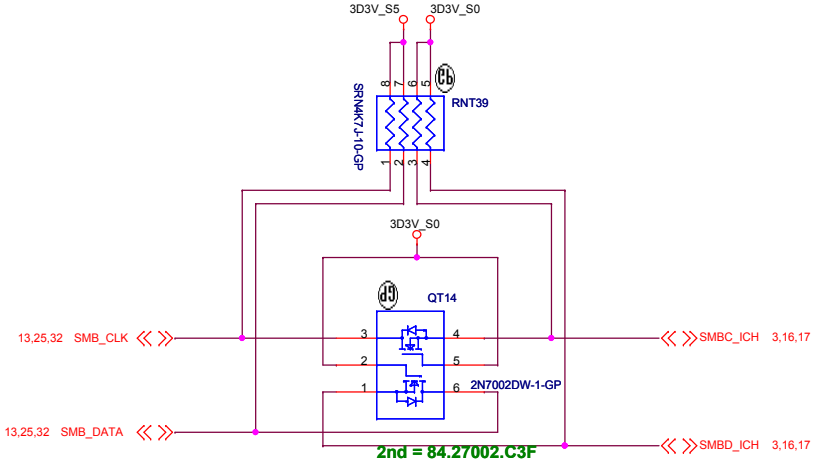

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Title: *ICH9-M (4 of 4)*

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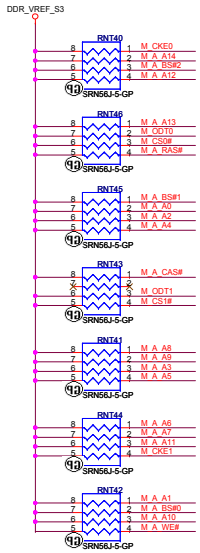
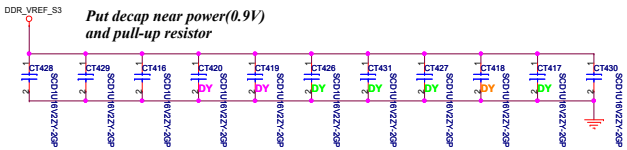
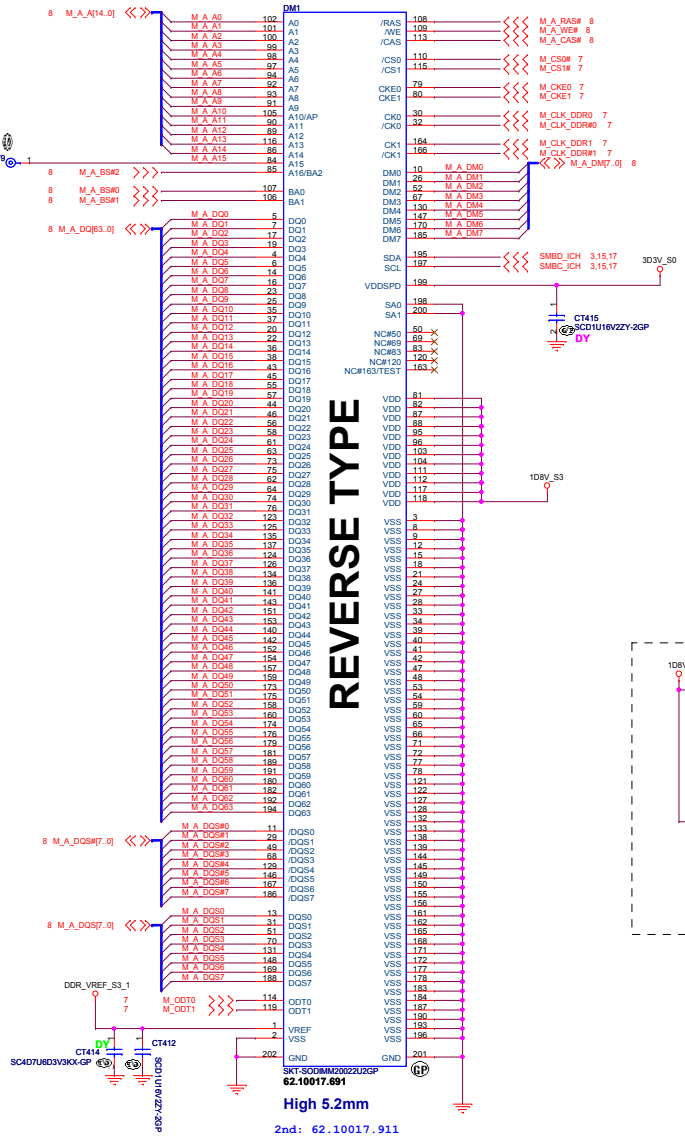
PARALLEL TERMINATION

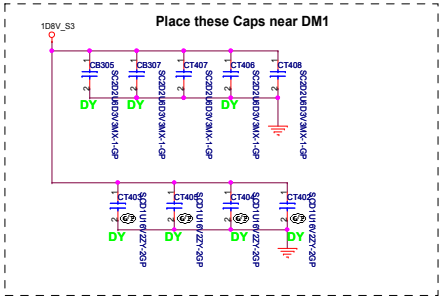
Put decap near power(0.9V) and pull-up resistor



Decoupling Capacitor







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Title: DDR2 Socket 0 (DM1)

Size: | Document Number: SJV50 | Rev: SA

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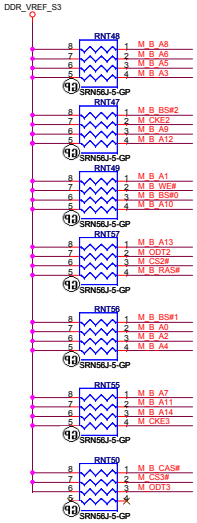
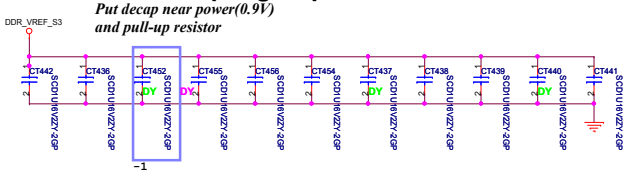
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

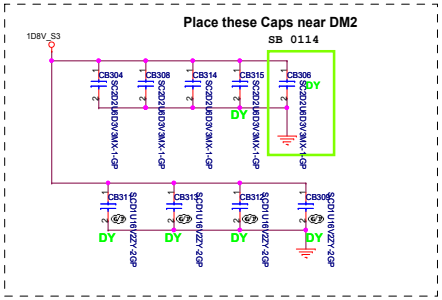


Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor



2nd: 62.10017.B51



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Title: DDR2 Socket 1 (DM2)

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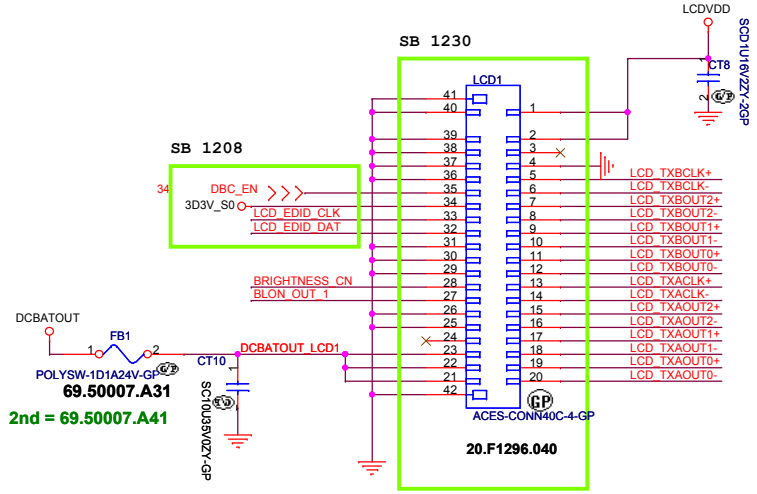
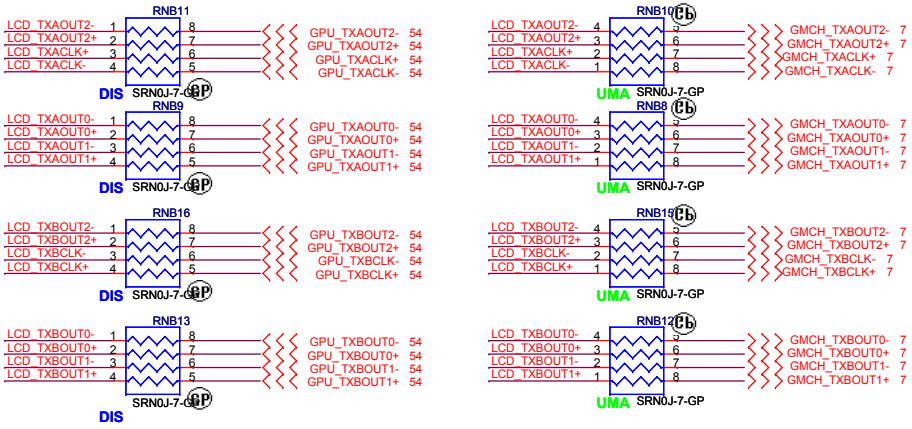
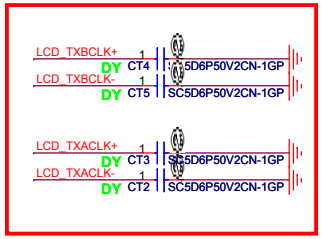
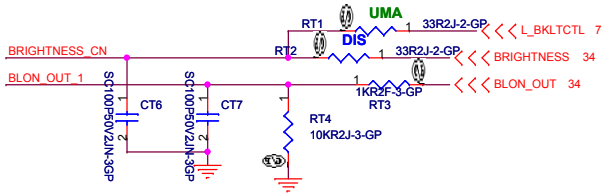
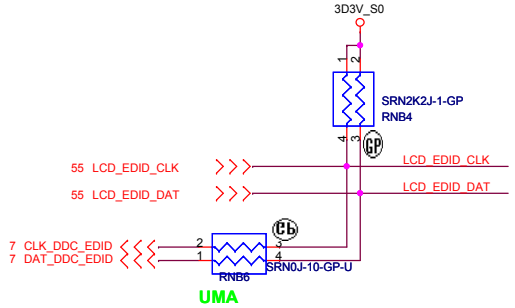
LCD/INVERTER/CCD CONN



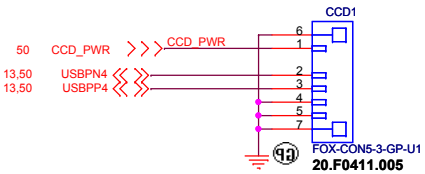


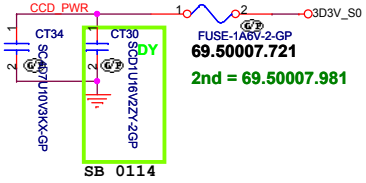


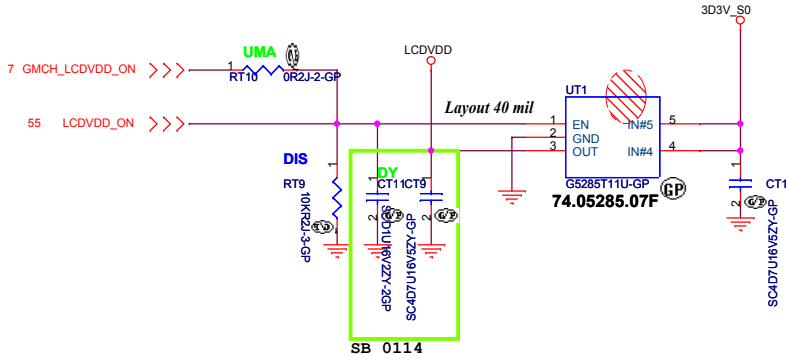




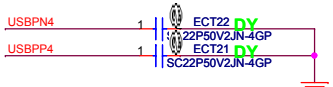
CCD

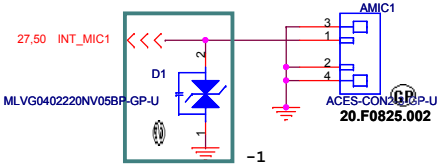






Internal Mic





SJV50

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Title: LCD CONN

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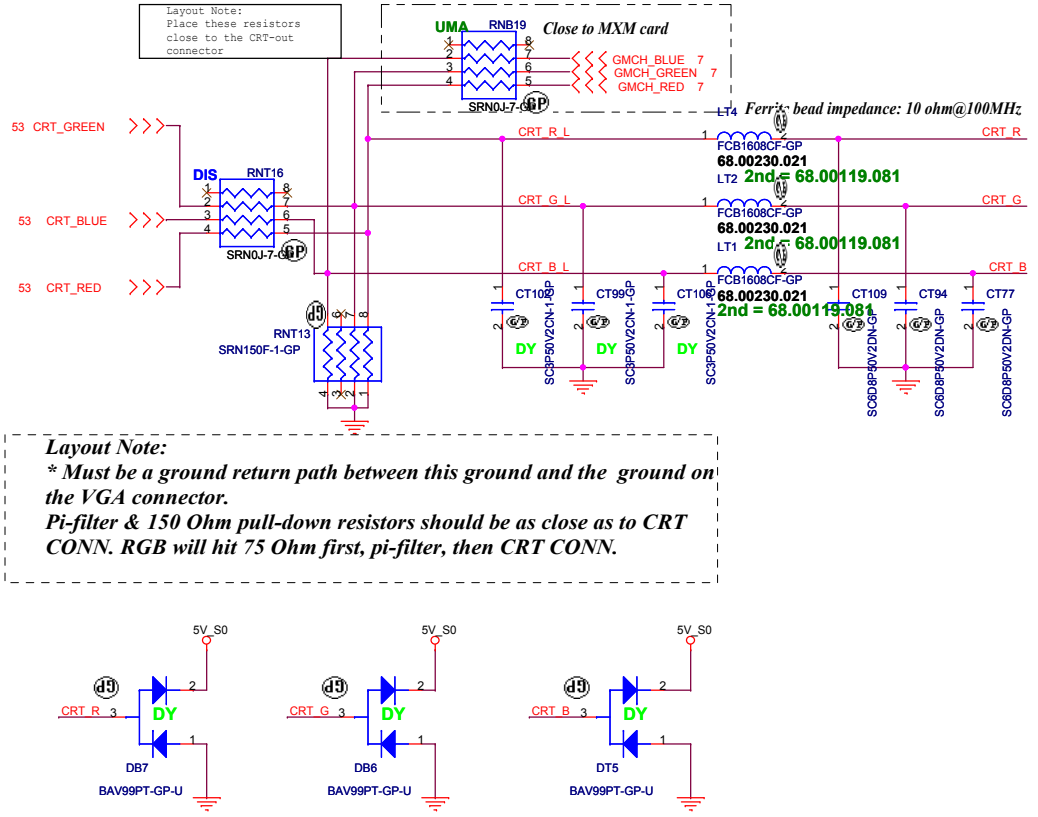
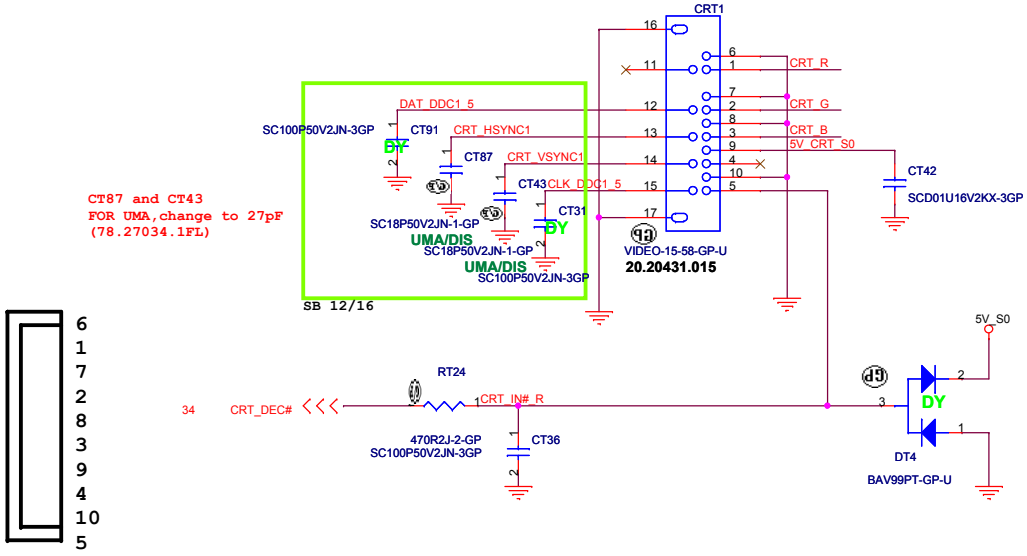
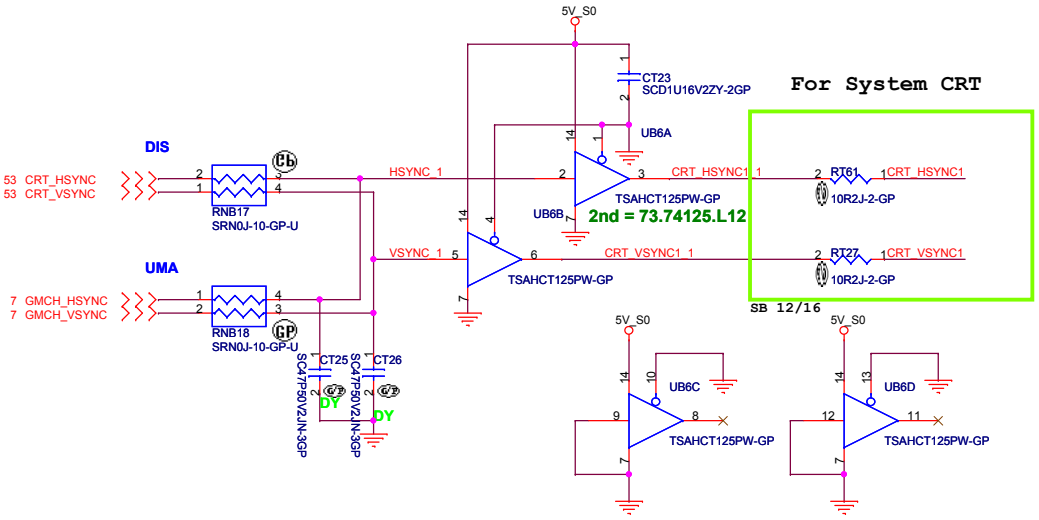


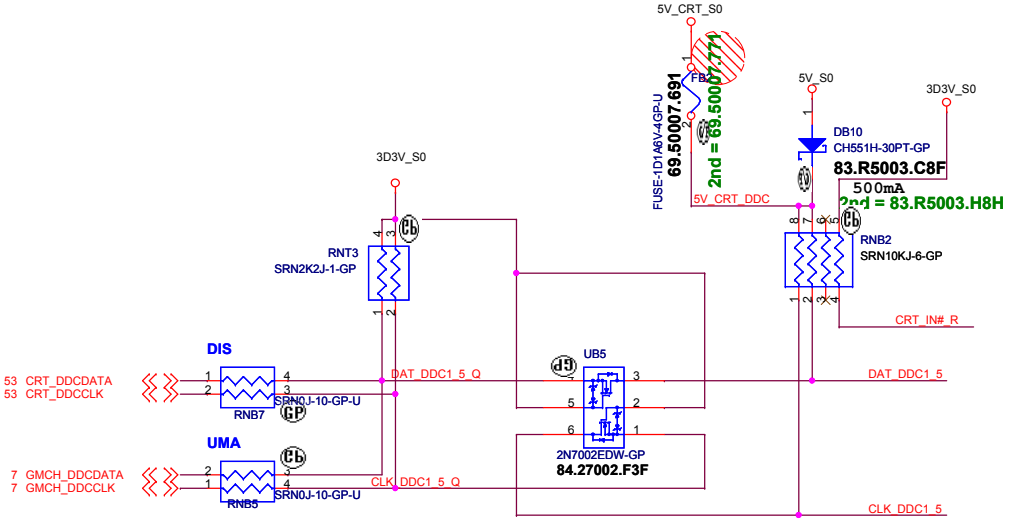
CRT I/F & CONNECTOR



Hsync & Vsync level shift



DDC_CLK & DATA level shift



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Taipei Hsien 221, Taiwan, R.O.C.

Title	CRT CONN	
Size	Document Number SJV50	Rev SA
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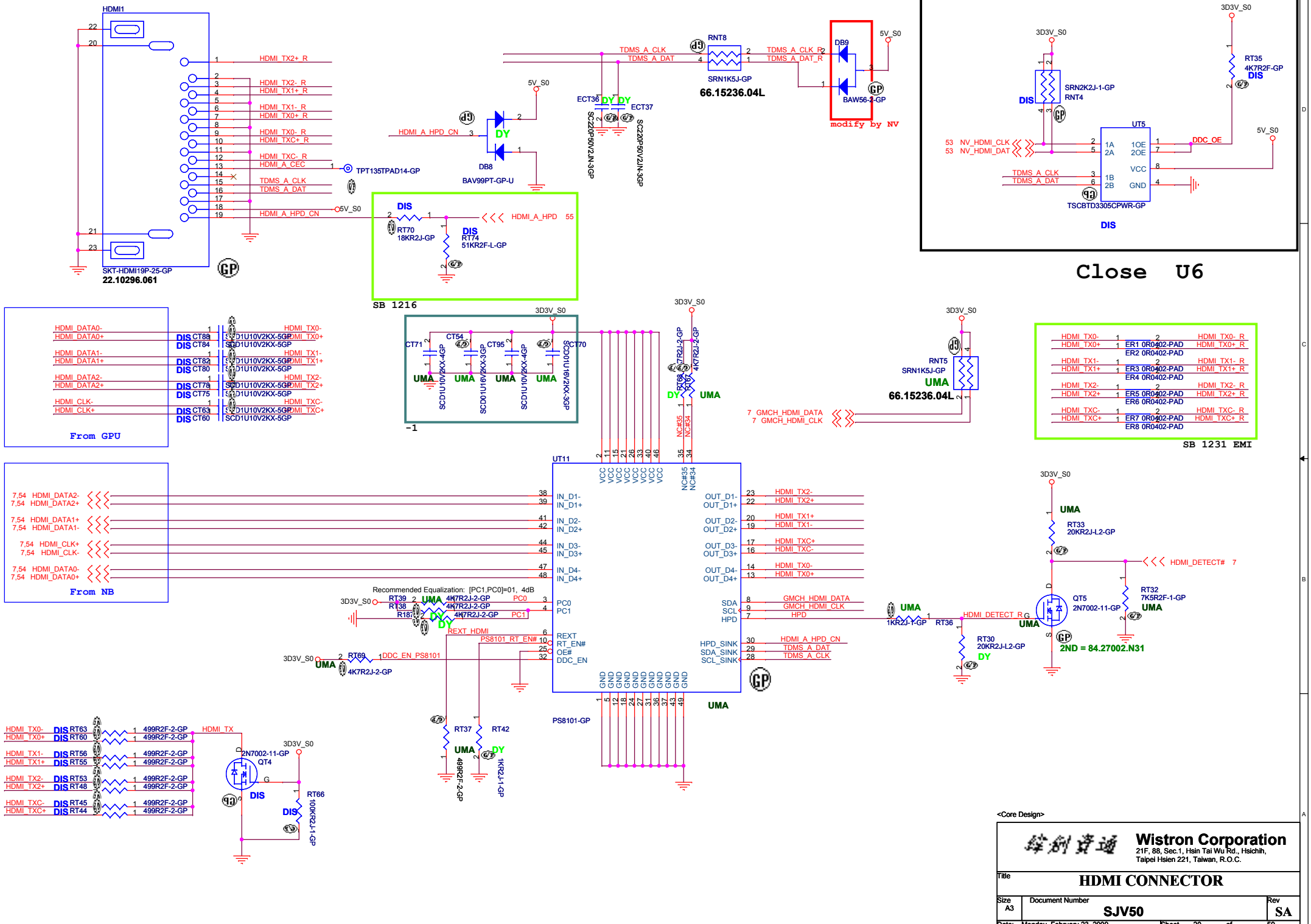

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

<Core Design>

Title: HDMI CONNECTOR

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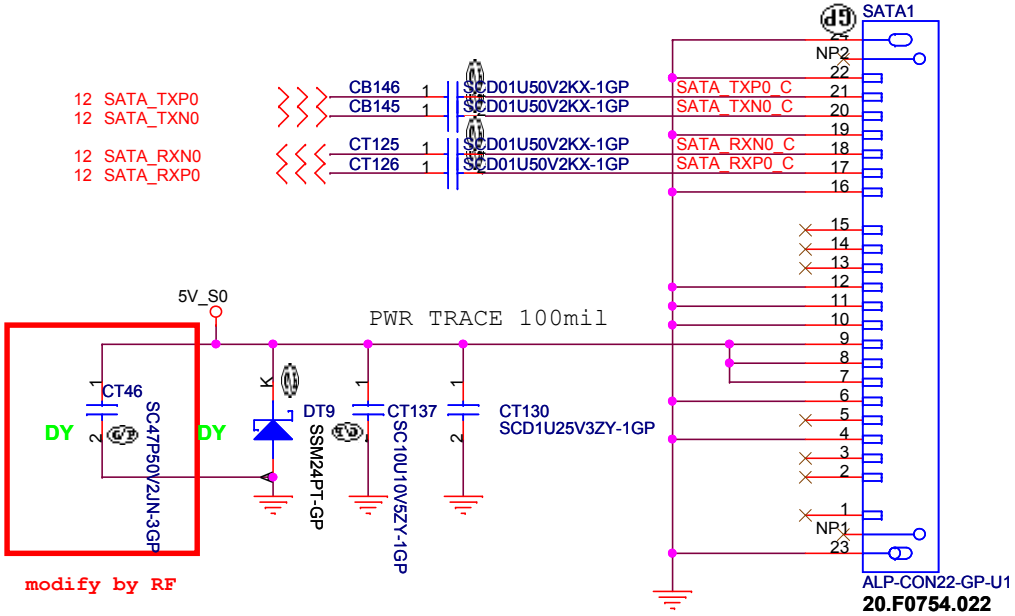
SATA Connector



SJV50

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***HDD CONN***	
Size	Document Number **SJV50**	Rev SA
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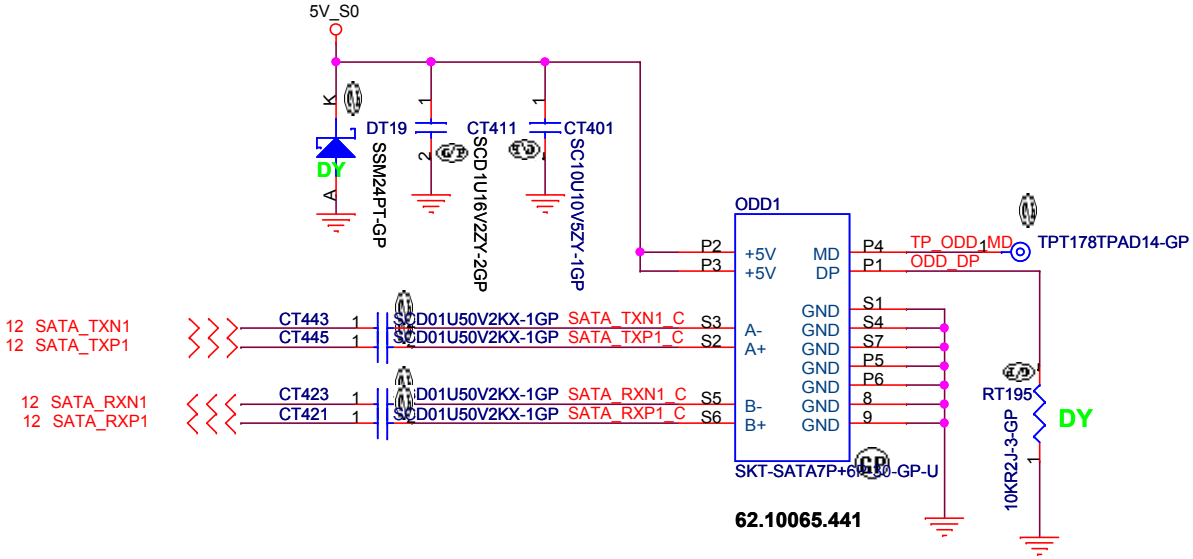
ODD Connector



SJV50

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**ODD**
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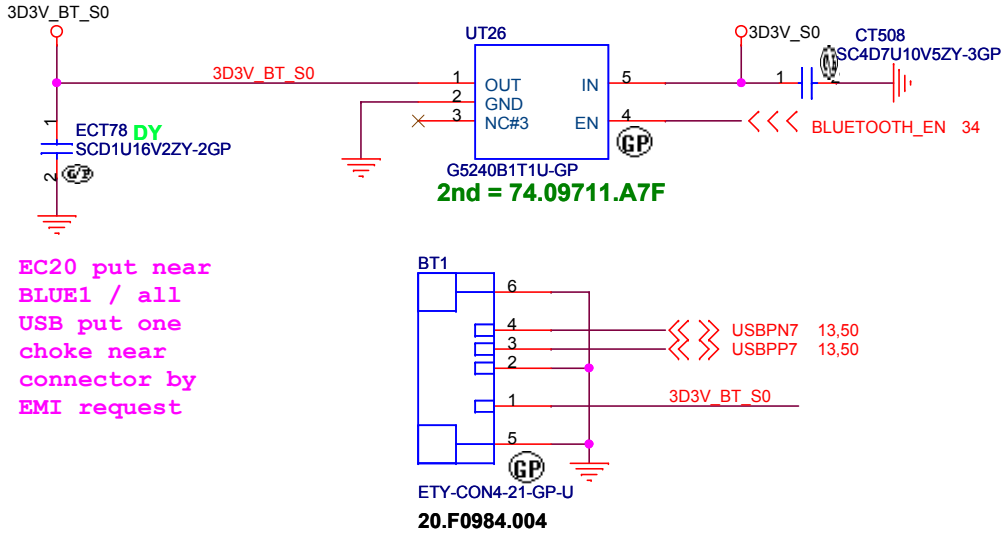
BLUETOOTH MODULE



SJV50

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***BLUETOOTH***
Size	Document Number: **SJV50** — Rev: SA
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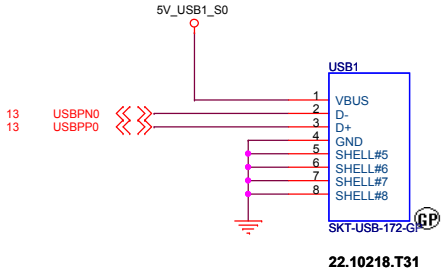

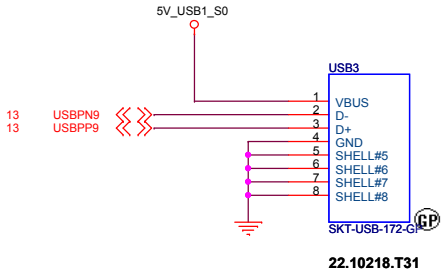

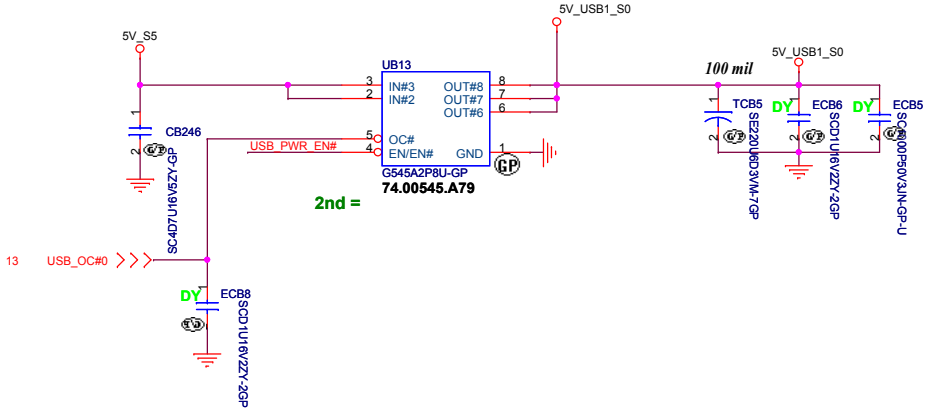

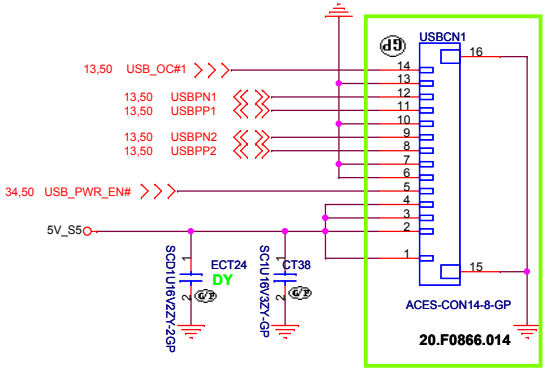

SB 1230

SJV50

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*USB CONN*	
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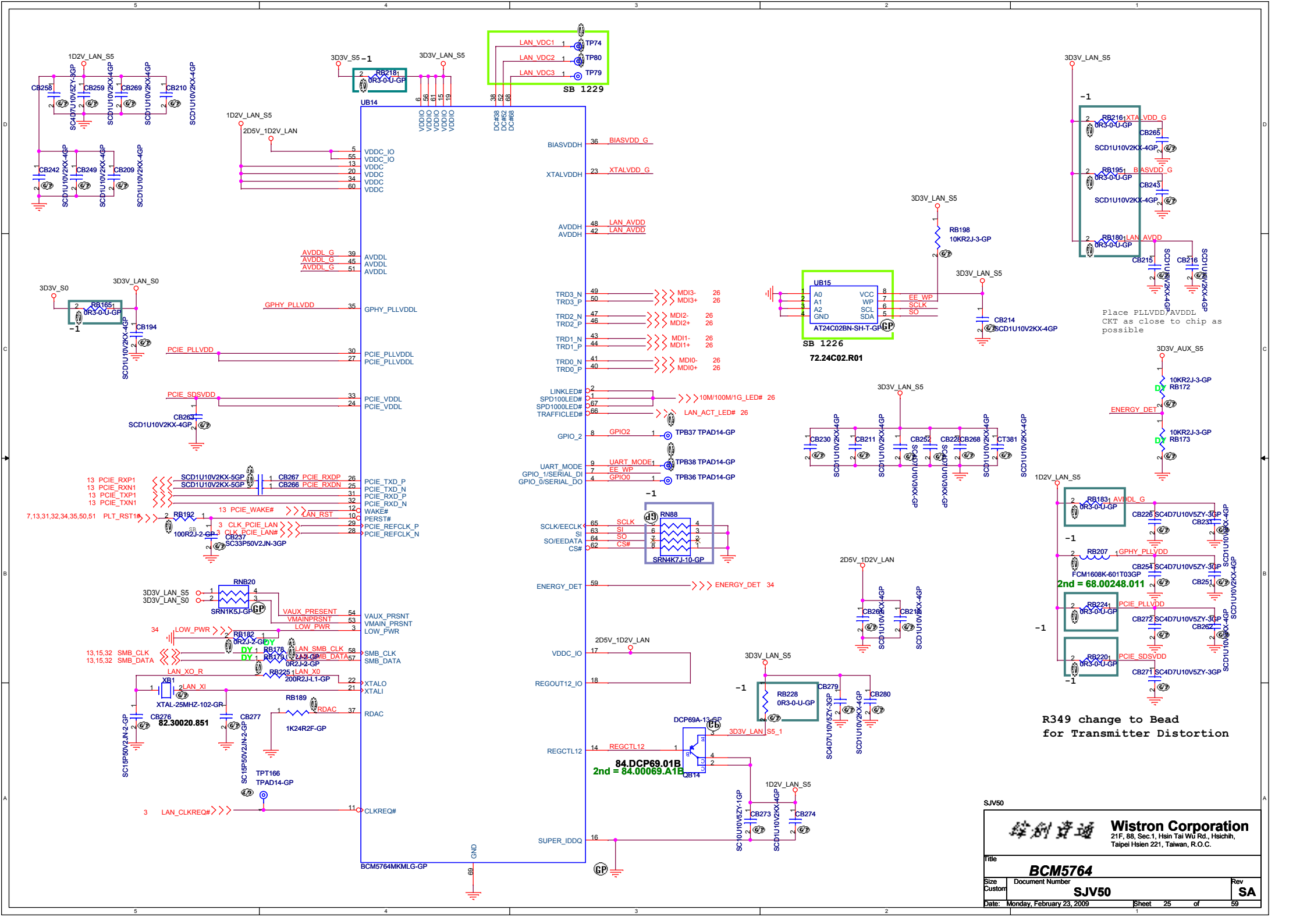
UB14
BCM5764MKMLG-GP
SB 1229
LAN_VDC1
LAN_VDC2
LAN_VDC3
TP74
TP80
TP79
UB15
AT24C02BN-SH-T-GP
SB 1226
72.24C02.R01
Place PLLVDD/AVDDL CKT as close to chip as possible
2nd = 68.00248.011
2nd = 84.00069.A1B
84.DCP69.01B
82.30020.851
R349 change to Bead for Transmitter Distortion
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
BCM5764
SJV50
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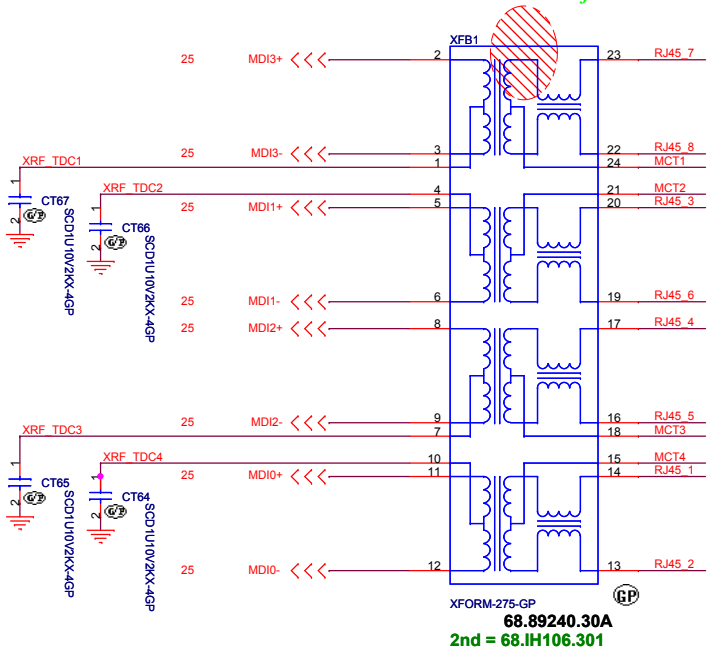
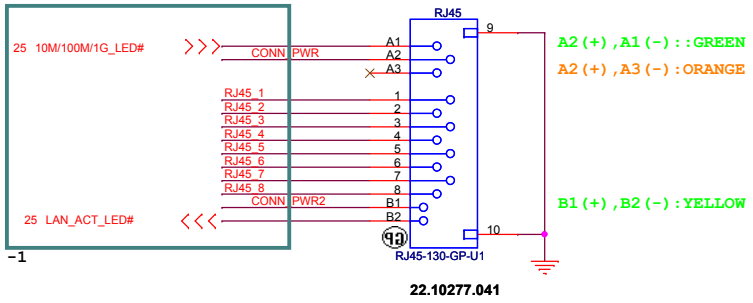
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

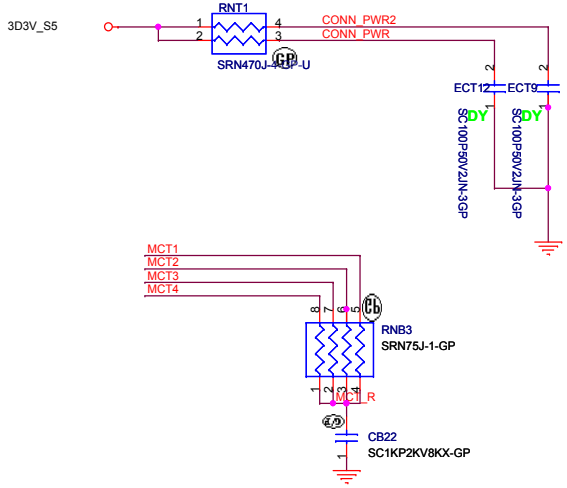
LAN Connector

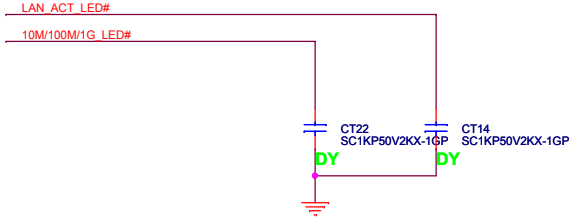
LAN Connector

GIGA Lan Transformer









SJV50

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN CONN

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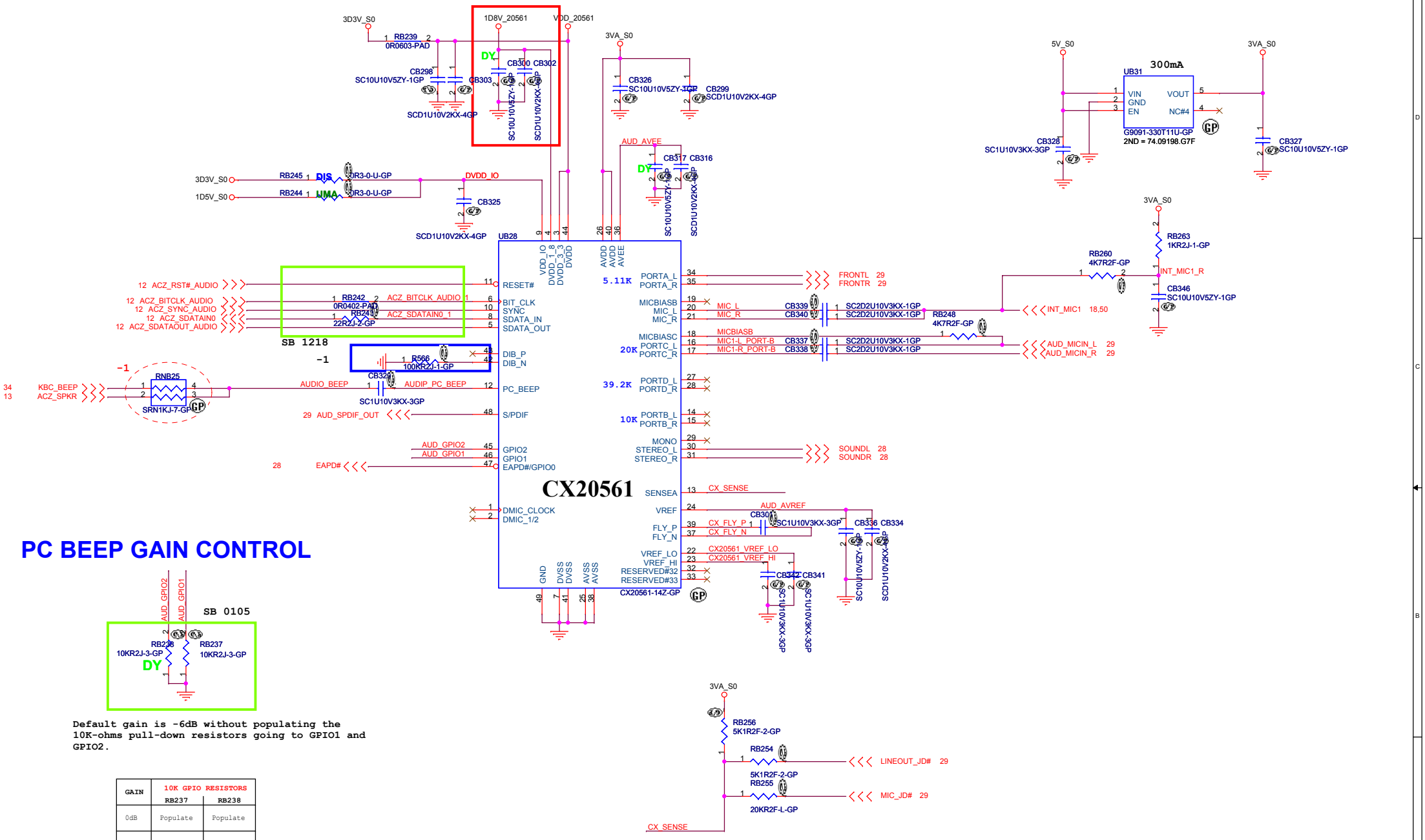

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Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Azalia codec CX20561

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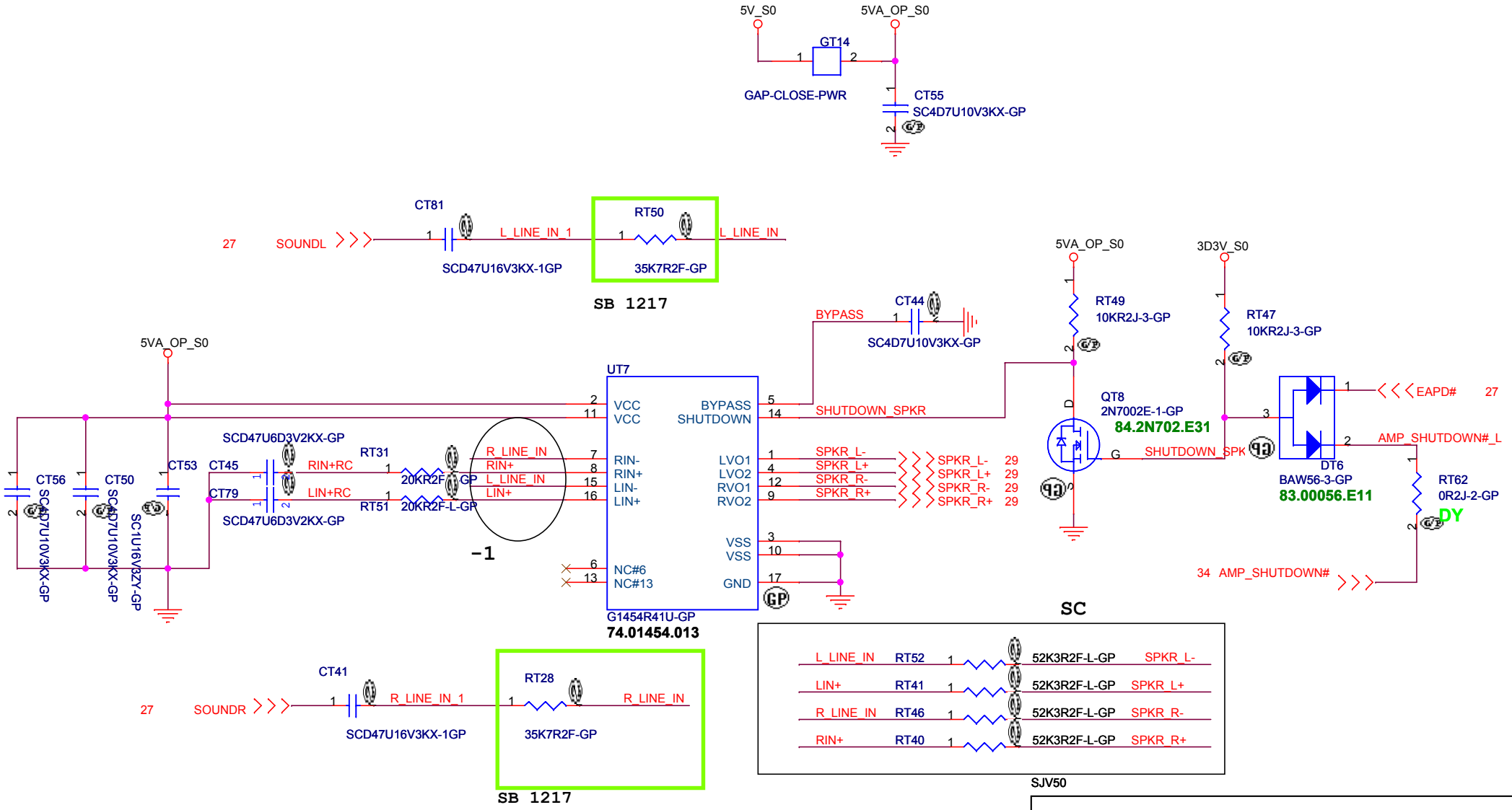
AUDIO OP AMPLIFIER



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	*AUDIO AMP AND JACK*		
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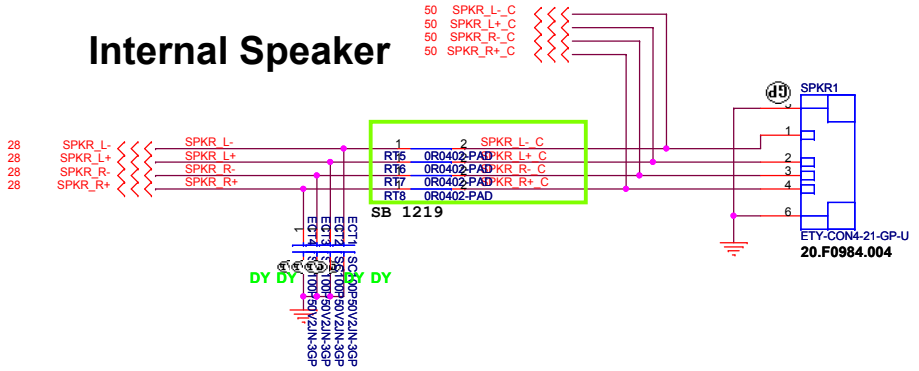
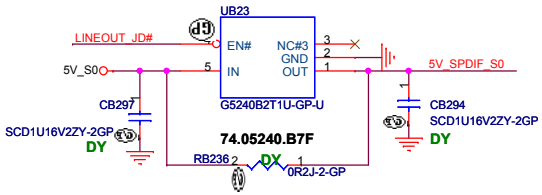
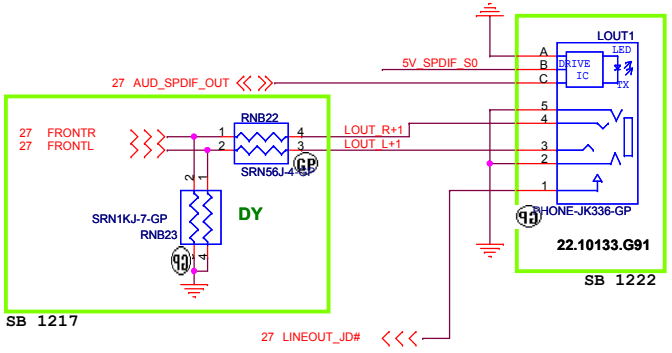
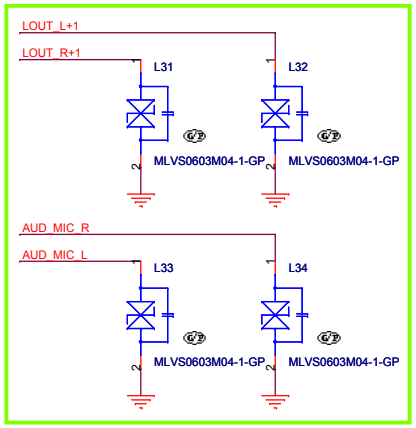
Internal Speaker



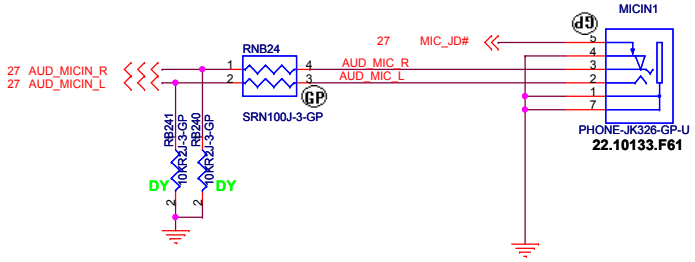
LINE OUT

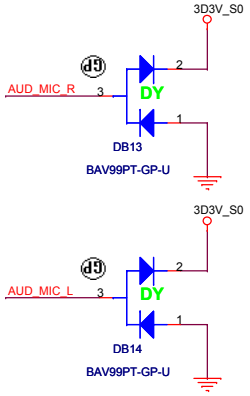






MIC IN





SJV50

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *AUDIO jack*		
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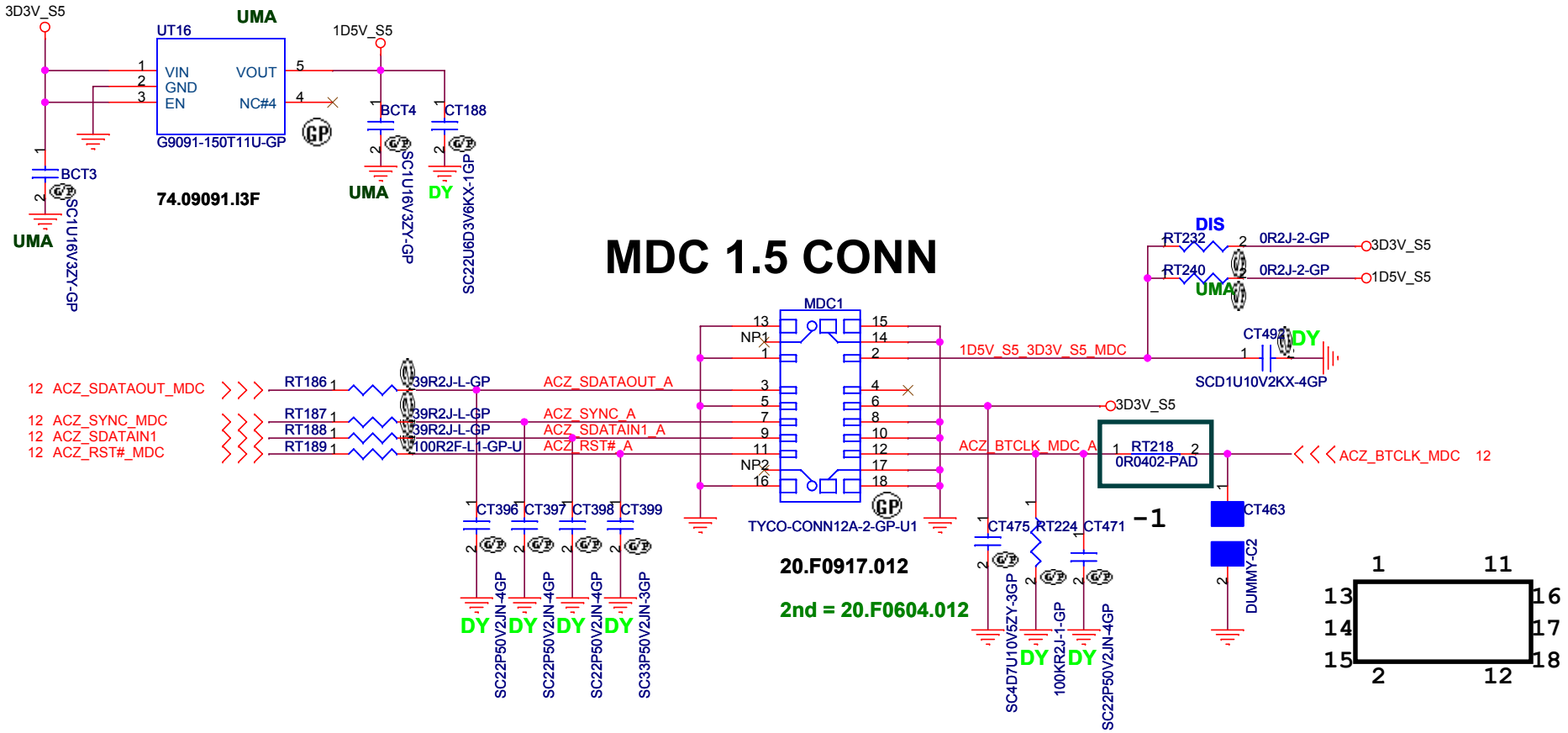

SJV50

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***MDC***	
Size	Document Number **SJV50**	Rev SA
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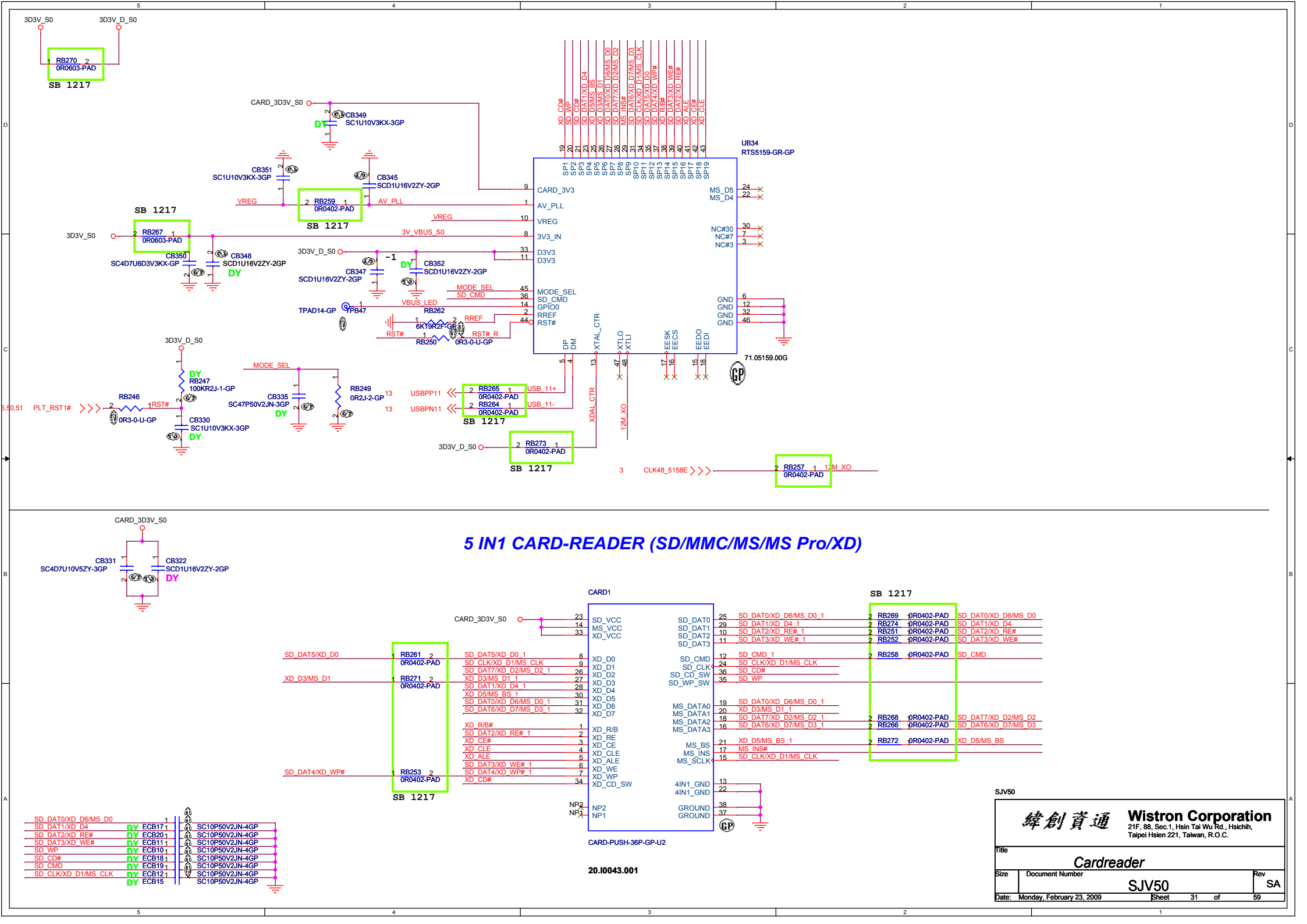
5 IN1 CARD-READER (SD/MMC/MS/MS Pro/XD)
UB34
RTS5159-GR-GP
CARD1
CARD-PUSH-36P-GP-U2
SB 1217
20.I0043.001
SJV50
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Cardreader
Size
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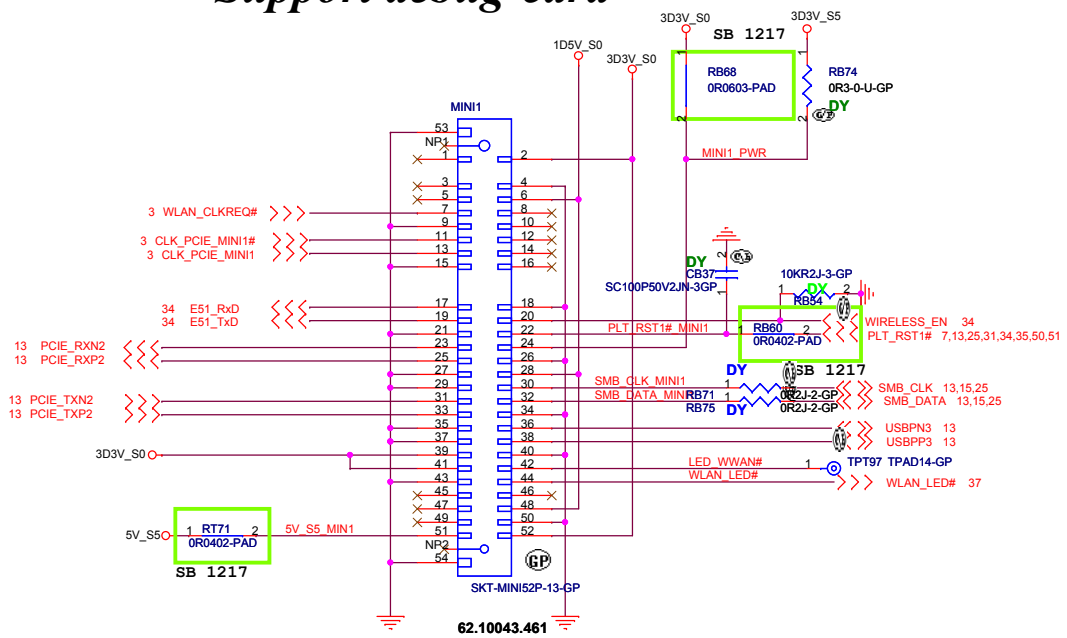
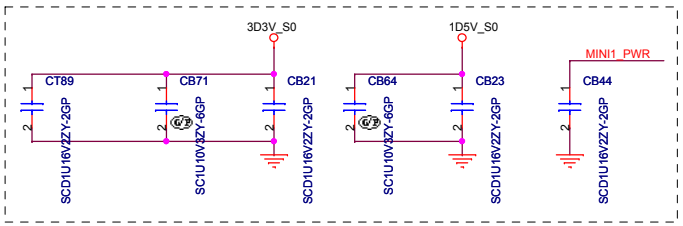
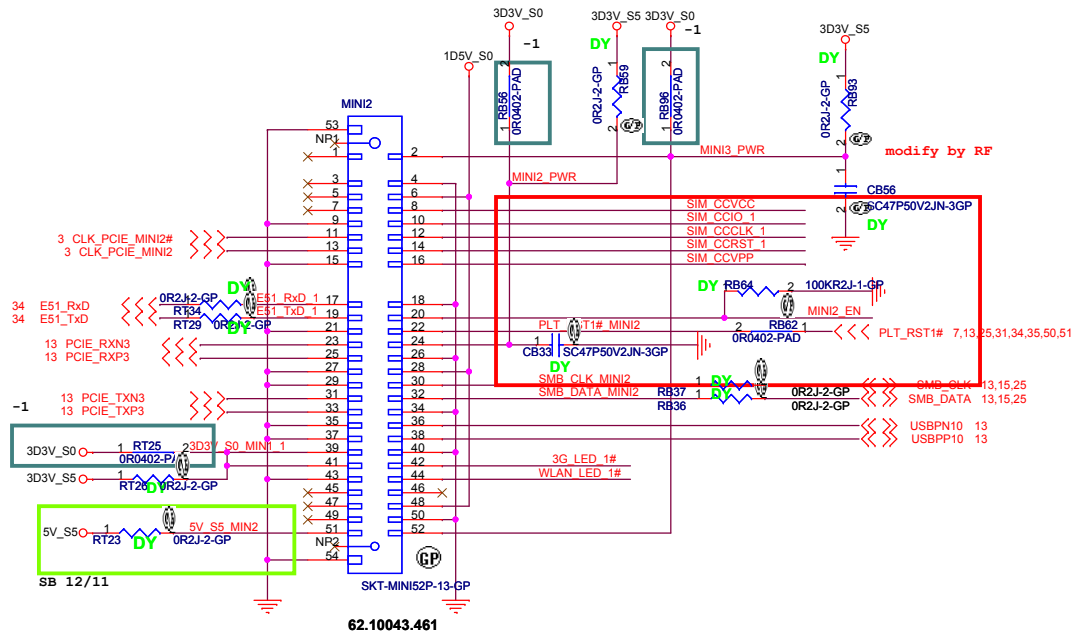
Mini Card Connector(WLAN) Half Card
Support debug-card

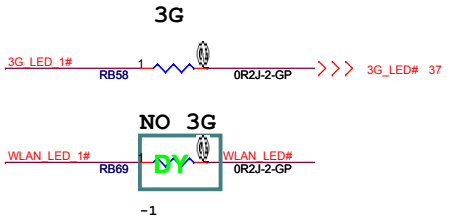


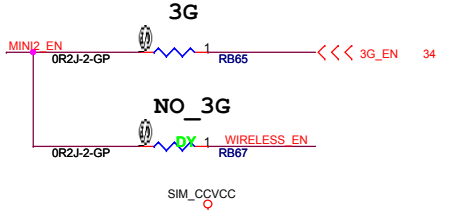
Place near MINI1



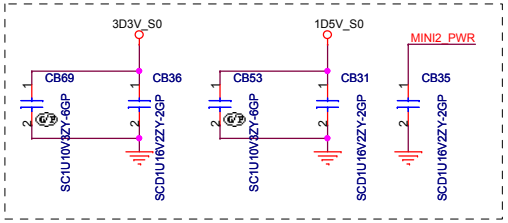
Mini Card Connector(Robson2 and 3G)

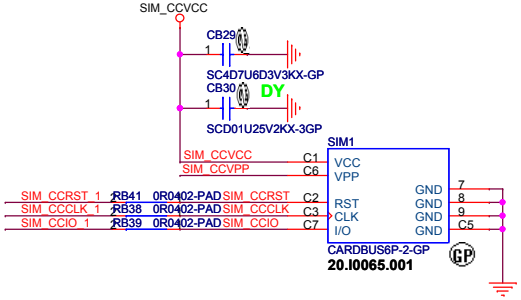






Place near MINIC2





SJV50

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title			
MINI CARD			
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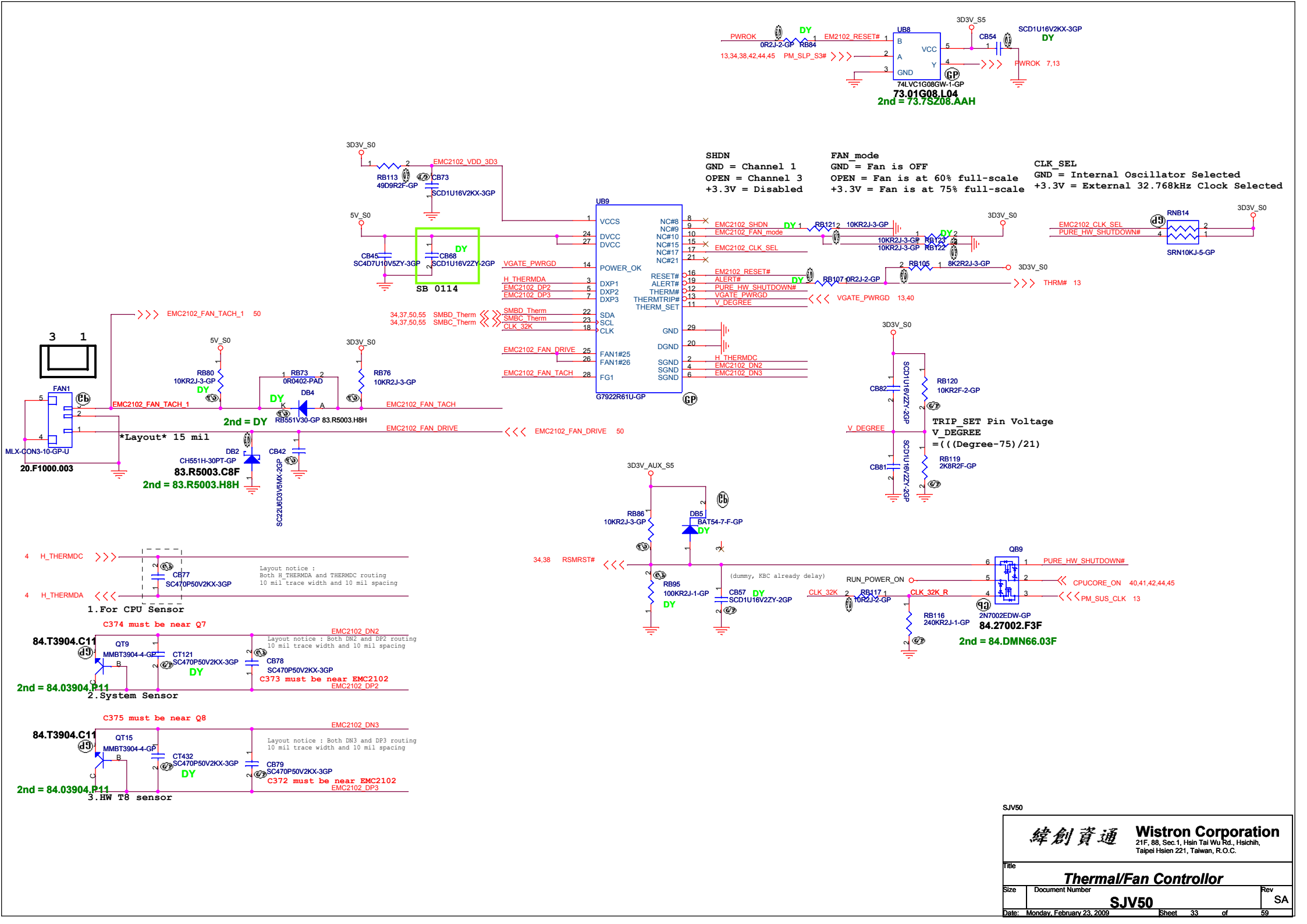
PWROK
0R2J-2-GP
RB84
DY
EM2102_RESET#
UB8
74LVC1G08GW-1-GP
73.01G08.L04
2nd = 73.7SZ08.AAH
3D3V_S5
CB54
SCD1U16V2KX-3GP
PWROK 7,13
13,34,38,42,44,45 PM_SLP_S3#
SHDN
GND = Channel 1
OPEN = Channel 3
+3.3V = Disabled
FAN_mode
GND = Fan is OFF
OPEN = Fan is at 60% full-scale
+3.3V = Fan is at 75% full-scale
CLK_SEL
GND = Internal Oscillator Selected
+3.3V = External 32.768kHz Clock Selected
3D3V_S0
EMC2102_VDD_3D3
RB113
49D9R2F-GP
CB73
SCD1U16V2KX-3GP
5V_S0
CB45
SC4D7U10V5ZY-3GP
CB68
SCD1U16V2ZY-2GP
SB 0114
UB9
G7922R61U-GP
VCCS
DVCC
DVCC
POWER_OK
DXP1
DXP2
DXP3
SDA
SCL
CLK
FAN1#25
FAN1#26
FG1
NC#8
NC#9
NC#10
NC#15
NC#17
NC#21
RESET#
ALERT#
THERM#
THERMTRIP#
THERM_SET
GND
DGND
SGND
SGND
SGND
EMC2102_SHDN
EMC2102_FAN_mode
EMC2102_CLK_SEL
EMC2102_RESET#
PURE_HW_SHUTDOWN#
VGATE_PWRGD
V_DEGREE
H_THERMDC
EMC2102_DN2
EMC2102_DN3
VGATE_PWRGD
H_THERMDA
EMC2102_DP2
EMC2102_DP3
SMBD_Therm
SMBC_Therm
CLK_32K
EMC2102_FAN_DRIVE
EMC2102_FAN_TACH
34,37,50,55 SMBD_Therm
34,37,50,55 SMBC_Therm
RB121
10KR2J-3-GP
RB123
RB122
RB107
0R2J-2-GP
RB105
8K2R2J-3-GP
THRM# 13
VGATE_PWRGD 13,40
RNB14
SRN10KJ-5-GP
EMC2102_CLK_SEL
PURE_HW_SHUTDOWN#
FAN1
MLX-CON3-10-GP-U
20.F1000.003
EMC2102_FAN_TACH_1 50
RB80
10KR2J-3-GP
RB73
0R0402-PAD
RB76
10KR2J-3-GP
DB4
RB551V30-GP 83.R5003.H8H
2nd = DY
Layout 15 mil
DB2
CH551H-30PT-GP
83.R5003.C8F
2nd = 83.R5003.H8H
CB42
SC22U6D3V5MX-2GP
EMC2102_FAN_DRIVE 50
TRIP_SET Pin Voltage
V_DEGREE
=(((Degree-75)/21)
CB82
SCD1U16V2ZY-2GP
RB120
10KR2F-2GP
CB81
SCD1U16V2ZY-2GP
RB119
2K8R2F-GP
3D3V_AUX_S5
RB86
10KR2J-3-GP
DB5
BAT54-7-F-GP
RB95
100KR2J-1-GP
CB57
SCD1U16V2ZY-2GP
(dummy, KBC already delay)
34,38 RSMRST#
RUN_POWER_ON
CLK_32K
CLK_32K_R
RB117
10KR2J-2-GP
RB116
240KR2J-1-GP
QB9
2N7002EDW-GP
84.27002.F3F
2nd = 84.DMN66.03F
PURE_HW_SHUTDOWN#
CPUCORE_ON 40,41,42,44,45
PM_SUS_CLK 13
4 H_THERMDC
4 H_THERMDA
CB77
SC470P50V2KX-3GP
Layout notice :
Both H_THERMDA and THERMDC routing
10 mil trace width and 10 mil spacing
1.For CPU Sensor
C374 must be near Q7
84.T3904.C11
QT9
MMBT3904-4-GP
CT121
SC470P50V2KX-3GP
CB78
SC470P50V2KX-3GP
C373 must be near EMC2102
EMC2102_DP2
EMC2102_DN2
Layout notice : Both DN2 and DP2 routing
10 mil trace width and 10 mil spacing
2nd = 84.03904.P11
2.System Sensor
C375 must be near Q8
84.T3904.C11
QT15
MMBT3904-4-GP
CT432
SC470P50V2KX-3GP
CB79
SC470P50V2KX-3GP
C372 must be near EMC2102
EMC2102_DP3
EMC2102_DN3
Layout notice : Both DN3 and DP3 routing
10 mil trace width and 10 mil spacing
2nd = 84.03904.P11
3.HW T8 sensor
SJV50
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Thermal/Fan Controllor
Size
Document Number
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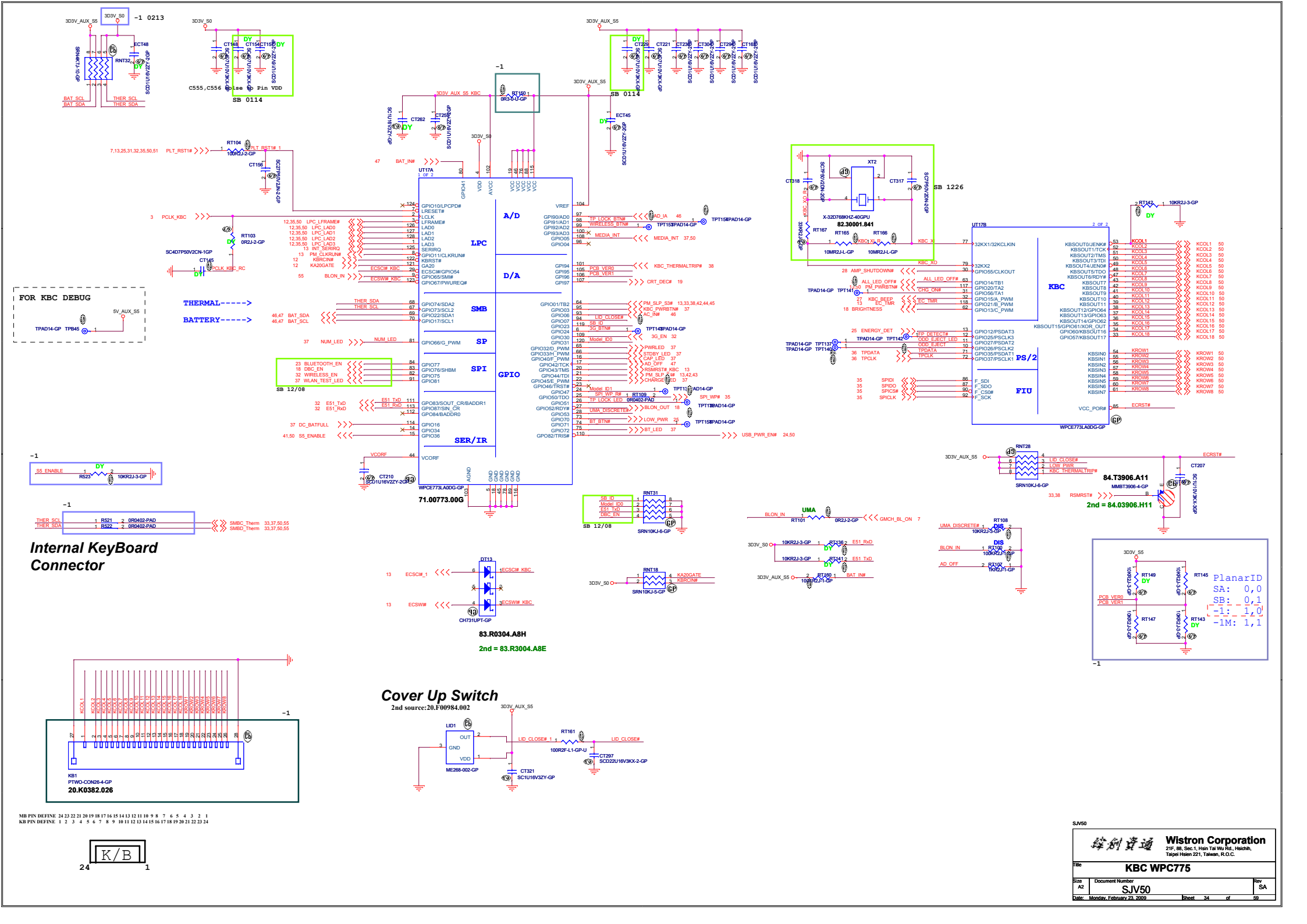

SJV50

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC WPC775

Size	Document Number	Rev
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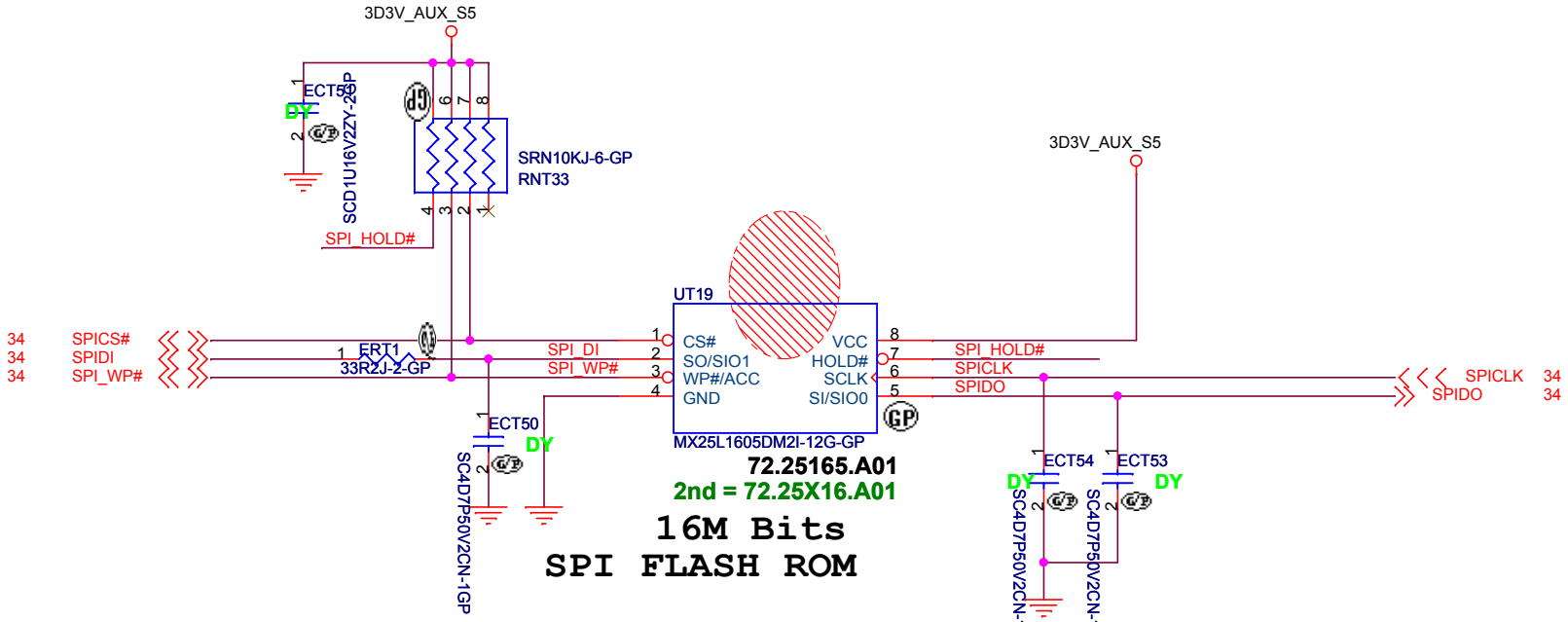
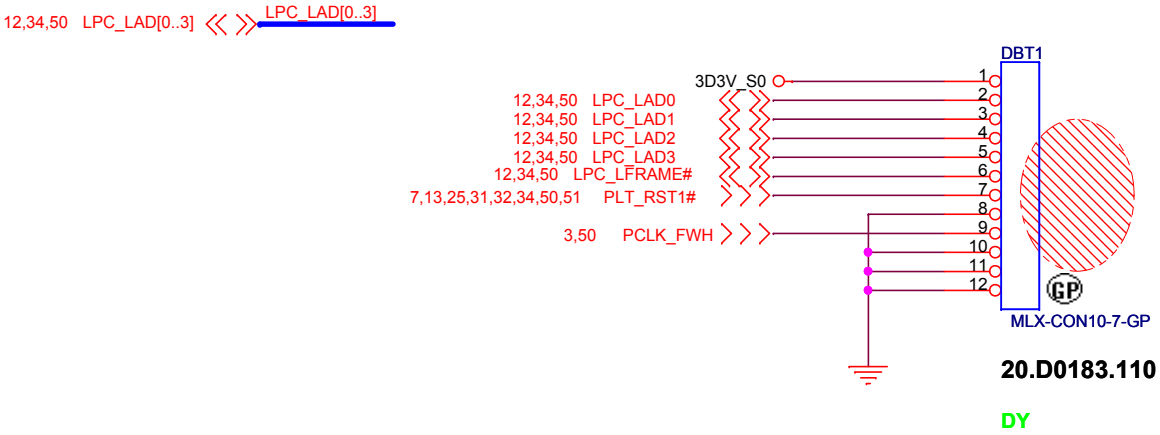


GOLDEN FINGER FOR DEBUG BOARD



SJV50

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***BIOS***	
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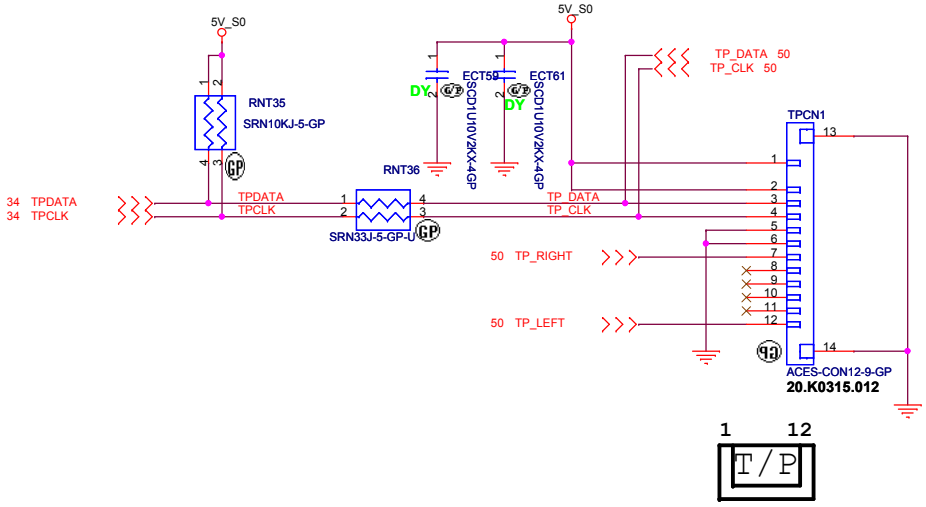
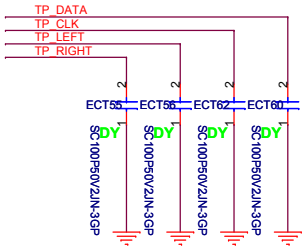
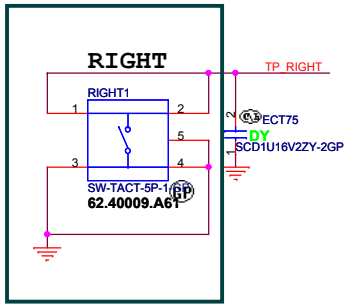
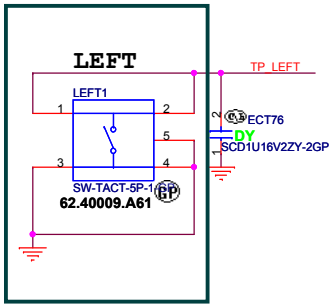
TOUCH PAD







-1 ME 0220



-1 ME 0220

SJV50

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Touch PAD and FP		
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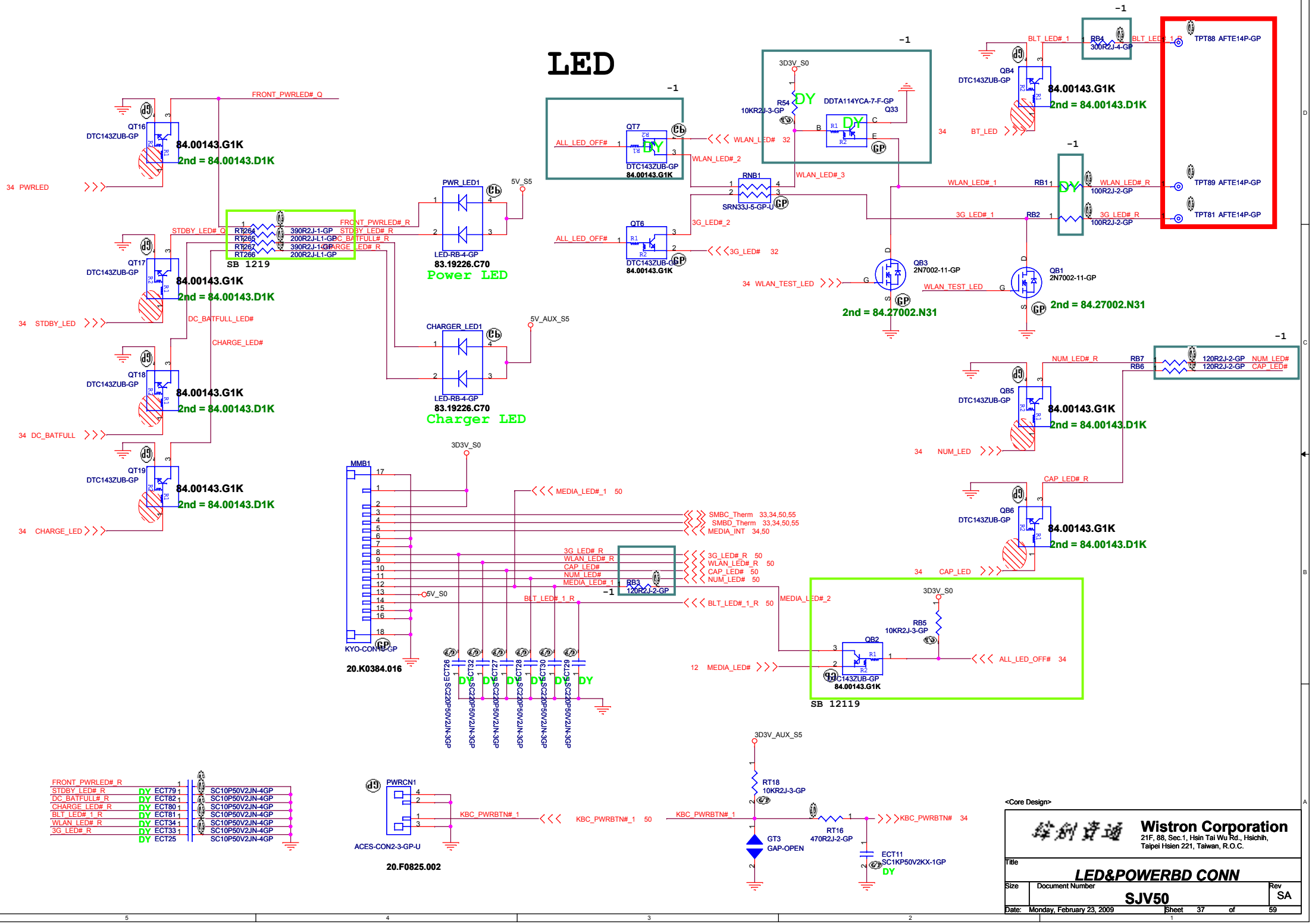
LED



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LED&POWERBD CONN**

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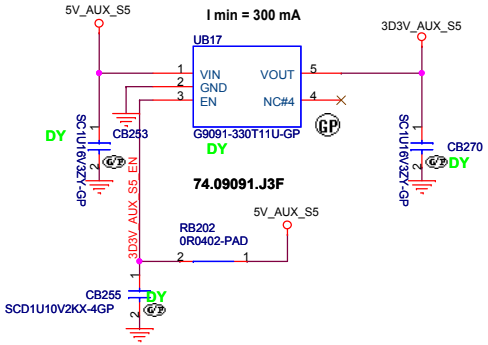
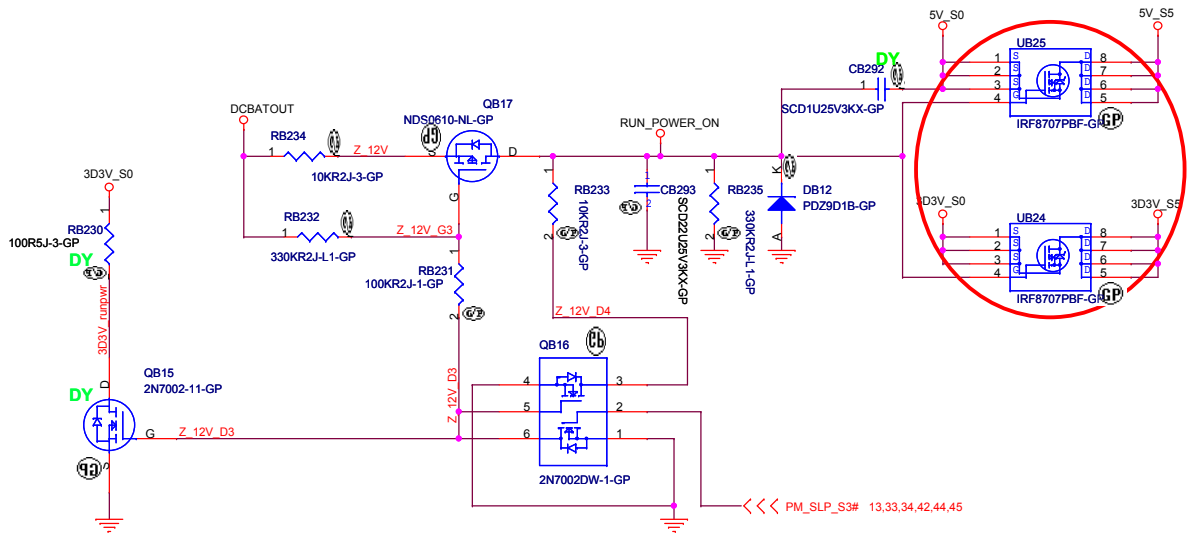
Aux Power 3D3V_AUX_S5



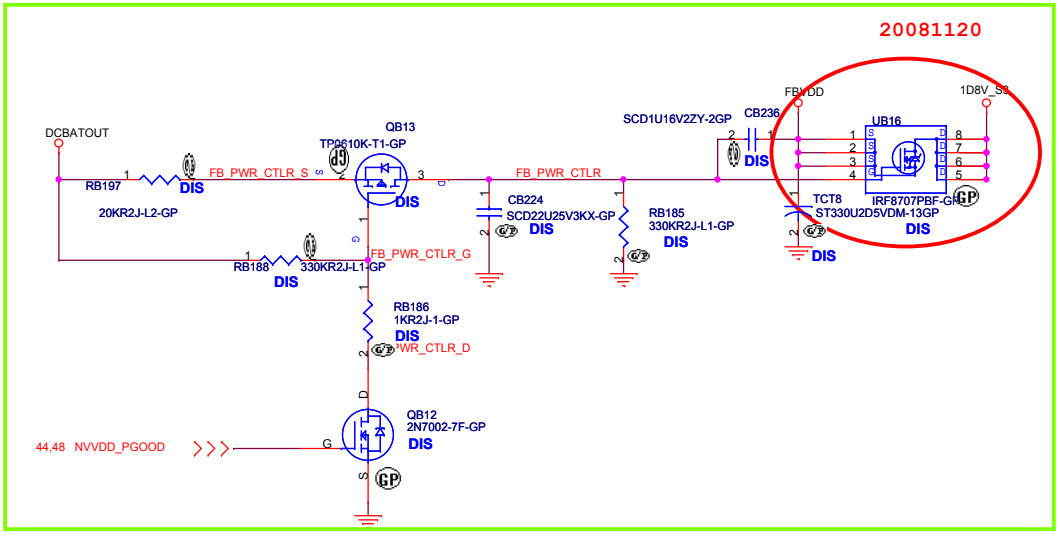
Run Power

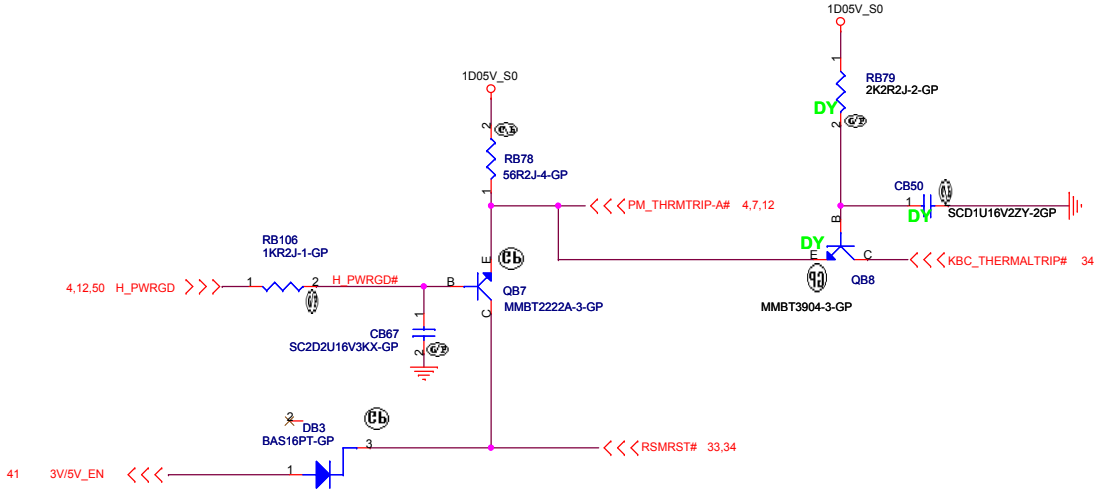
20081120



SB 12/11

20081120





Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RUN POWER and 3D3V_AUX_S5

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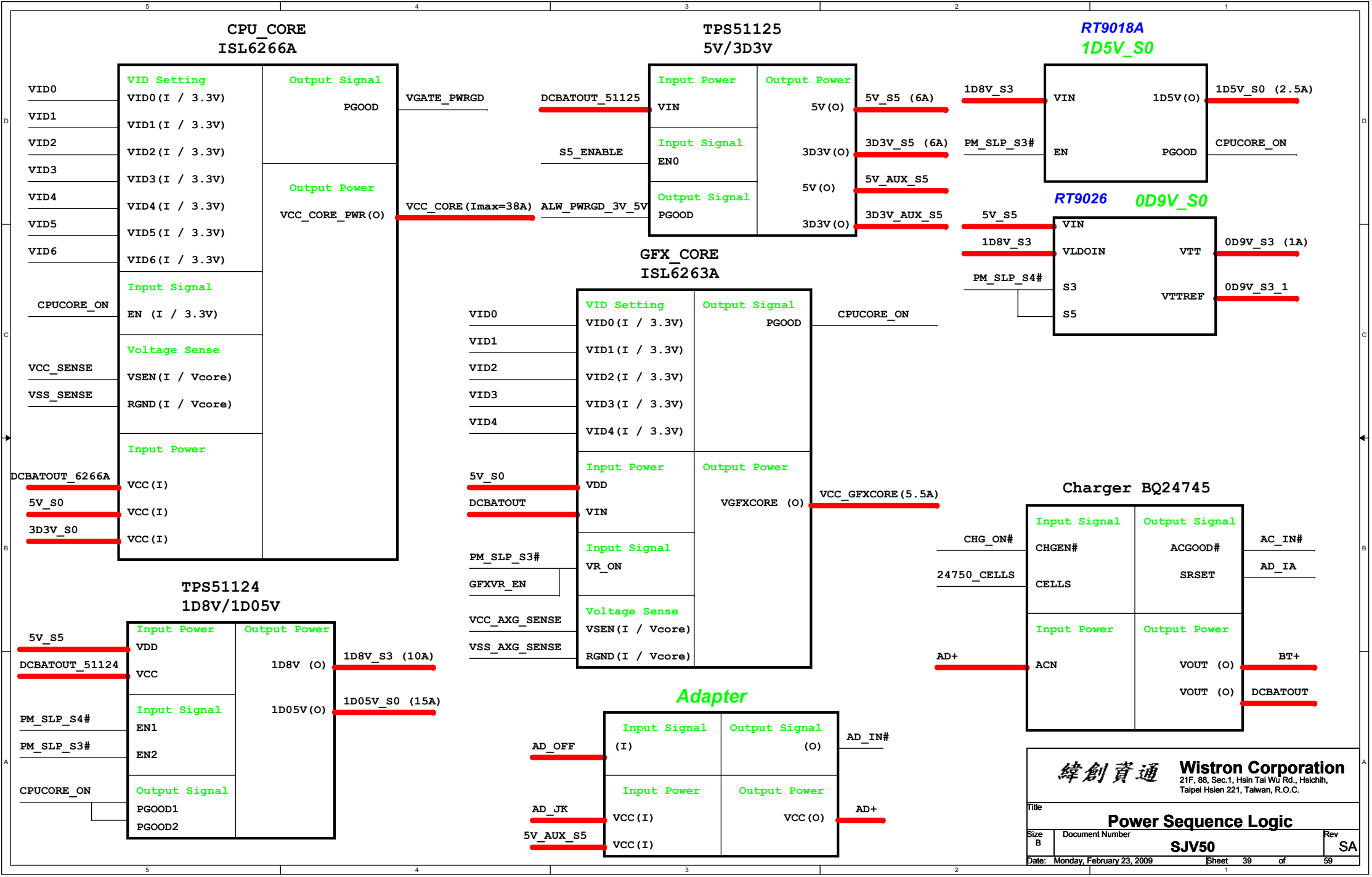
CPU_CORE
ISL6266A
VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
VID5(I / 3.3V)
VID6(I / 3.3V)
Input Signal
EN (I / 3.3V)
Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)
Input Power
VCC(I)
VCC(I)
VCC(I)
Output Signal
PGOOD
Output Power
VCC_CORE_PWR(O)
VID0
VID1
VID2
VID3
VID4
VID5
VID6
CPUCORE_ON
VCC_SENSE
VSS_SENSE
DCBATOUT_6266A
5V_S0
3D3V_S0
VGATE_PWRGD
VCC_CORE(Imax=38A)
TPS51125
5V/3D3V
Input Power
VIN
Input Signal
EN0
Output Signal
PGOOD
Output Power
5V(O)
3D3V(O)
5V(O)
3D3V(O)
DCBATOUT_51125
S5_ENABLE
ALW_PWRGD_3V_5V
5V_S5 (6A)
3D3V_S5 (6A)
5V_AUX_S5
3D3V_AUX_S5
RT9018A
1D5V_S0
VIN
EN
1D5V(O)
PGOOD
1D8V_S3
PM_SLP_S3#
1D5V_S0 (2.5A)
CPUCORE_ON
RT9026
0D9V_S0
VIN
VLDOIN
S3
S5
VTT
VTTREF
5V_S5
1D8V_S3
PM_SLP_S4#
0D9V_S3 (1A)
0D9V_S3_1
GFX_CORE
ISL6263A
VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
Input Power
VDD
VIN
Input Signal
VR_ON
Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)
Output Signal
PGOOD
Output Power
VGFXCORE (O)
VID0
VID1
VID2
VID3
VID4
5V_S0
DCBATOUT
PM_SLP_S3#
GFXVR_EN
VCC_AXG_SENSE
VSS_AXG_SENSE
CPUCORE_ON
VCC_GFXCORE(5.5A)
Charger BQ24745
Input Signal
CHGEN#
CELLS
Input Power
ACN
Output Signal
ACGOOD#
SRSET
Output Power
VOUT (O)
VOUT (O)
CHG_ON#
24750_CELLS
AD+
AC_IN#
AD_IA
BT+
DCBATOUT
TPS51124
1D8V/1D05V
Input Power
VDD
VCC
Input Signal
EN1
EN2
Output Signal
PGOOD1
PGOOD2
Output Power
1D8V (O)
1D05V(O)
5V_S5
DCBATOUT_51124
PM_SLP_S4#
PM_SLP_S3#
CPUCORE_ON
1D8V_S3 (10A)
1D05V_S0 (15A)
Adapter
Input Signal
(I)
Input Power
VCC(I)
VCC(I)
Output Signal
(O)
Output Power
VCC(O)
AD_OFF
AD_JK
5V_AUX_S5
AD_IN#
AD+
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Power Sequence Logic
Size
B
Document Number
SJV50
Rev
SA
Date: Monday, February 23, 2009
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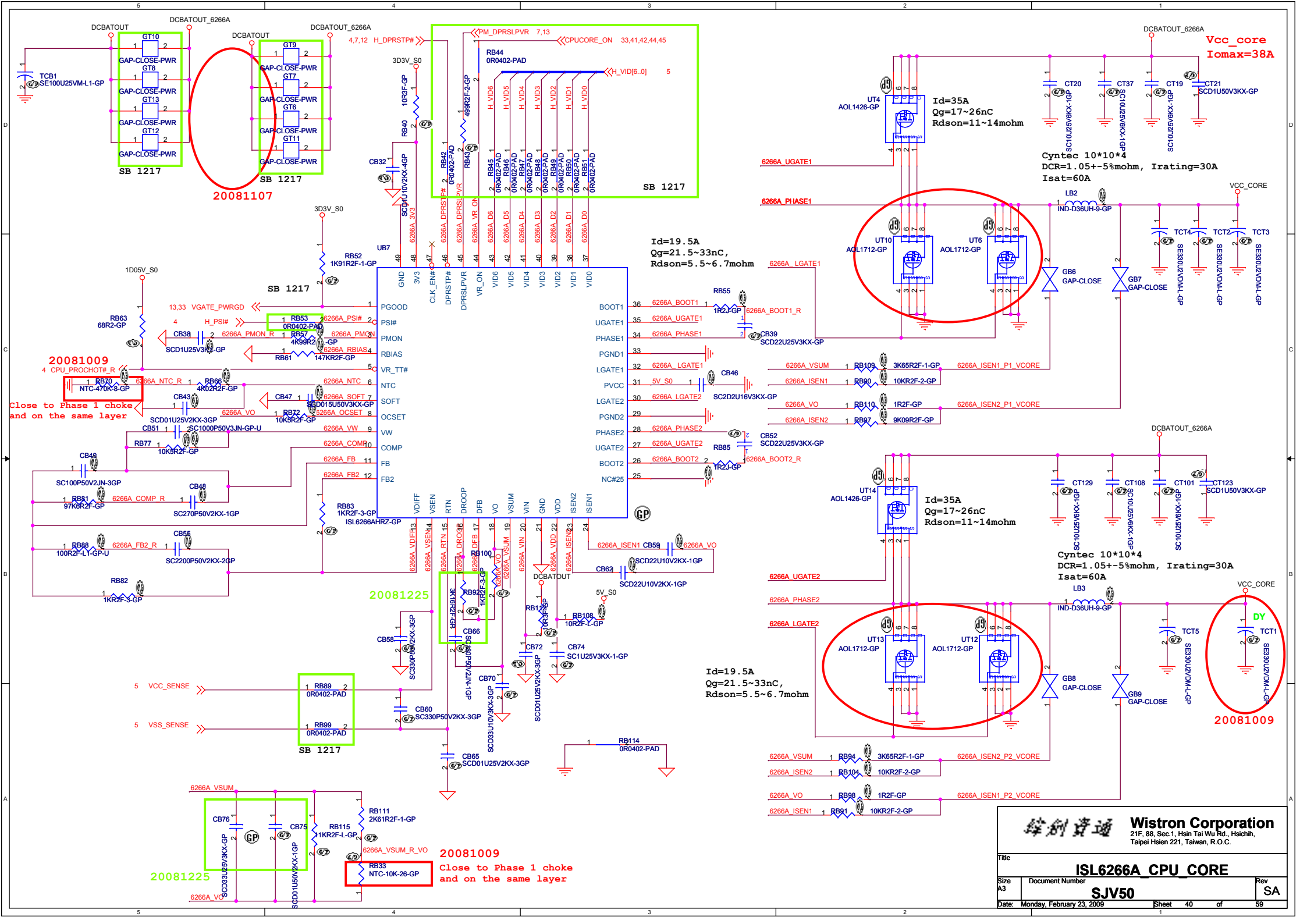
Vcc_core
Iomax=38A
Id=35A
Qg=17~26nC
Rdson=11~14mohm
Cyntec 10*10*4
DCR=1.05+-5%mohm, Irating=30A
Isat=60A
Id=19.5A
Qg=21.5~33nC,
Rdson=5.5~6.7mohm
Close to Phase 1 choke
and on the same layer
20081107
20081009
20081225
SB 1217
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL6266A_CPU_CORE
Size A3
Document Number
SJV50
Rev SA
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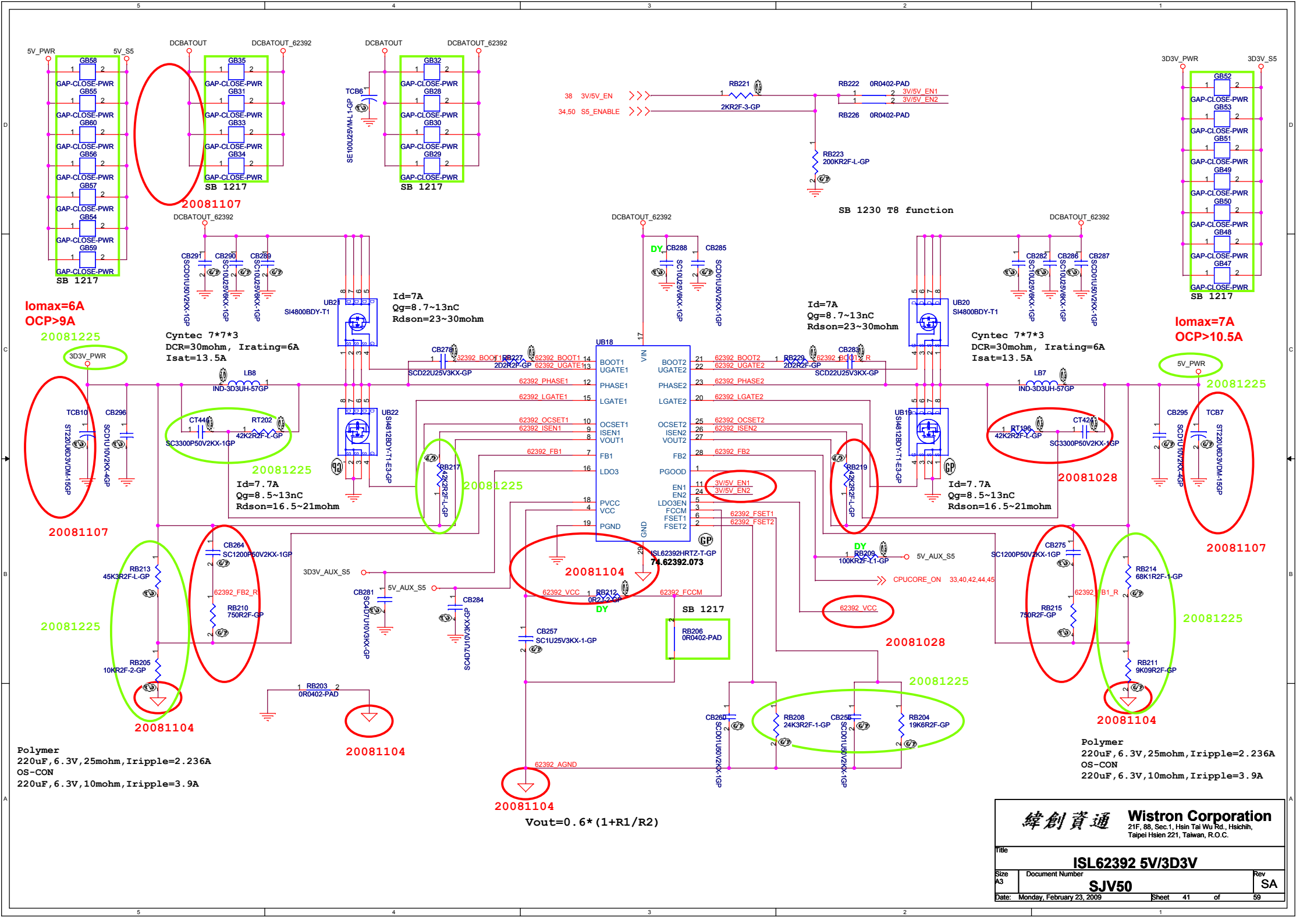
5V_PWR
5V_S5
DCBATOUT
DCBATOUT_62392
GAP-CLOSE-PWR
SB 1217
20081107
SE100U25VM-1-GP
3V/5V_EN
S5_ENABLE
RB221
2KR2F-3-GP
RB222 0R0402-PAD
RB226 0R0402-PAD
RB223 200KR2F-L-GP
SB 1230 T8 function
3D3V_PWR
3D3V_S5
lomax=6A
OCP>9A
20081225
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
SI4800BDY-T1
SCD22U25V3KXX-GP
IND-3D3UH-57GP
UB18
ISL62392HRTZ-T-GP
74.62392.073
BOOT1
UGATE1
PHASE1
LGATE1
OCSET1
ISEN1
VOUT1
FB1
LDO3
PVCC
VCC
PGND
BOOT2
UGATE2
PHASE2
LGATE2
OCSET2
ISEN2
VOUT2
FB2
PGOOD
EN1
EN2
LDO3EN
FCCM
FSET1
FSET2
VIN
GND
62392_BOOT1
62392_UGATE1
62392_PHASE1
62392_LGATE1
62392_OCSET1
62392_ISEN1
62392_FB1
62392_BOOT2
62392_UGATE2
62392_PHASE2
62392_LGATE2
62392_OCSET2
62392_ISEN2
62392_FB2
3V/5V_EN1
3V/5V_EN2
62392_FSET1
62392_FSET2
62392_VCC
62392_FCCM
62392_AGND
20081104
20081028
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
lomax=7A
OCP>10.5A
20081107
5V_AUX_S5
3D3V_AUX_S5
CPUCORE_ON 33,40,42,44,45
Polymer
220uF,6.3V,25mohm,Iripple=2.236A
OS-CON
220uF,6.3V,10mohm,Iripple=3.9A
Vout=0.6*(1+R1/R2)
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL62392 5V/3D3V
Size A3
Document Number
SJV50
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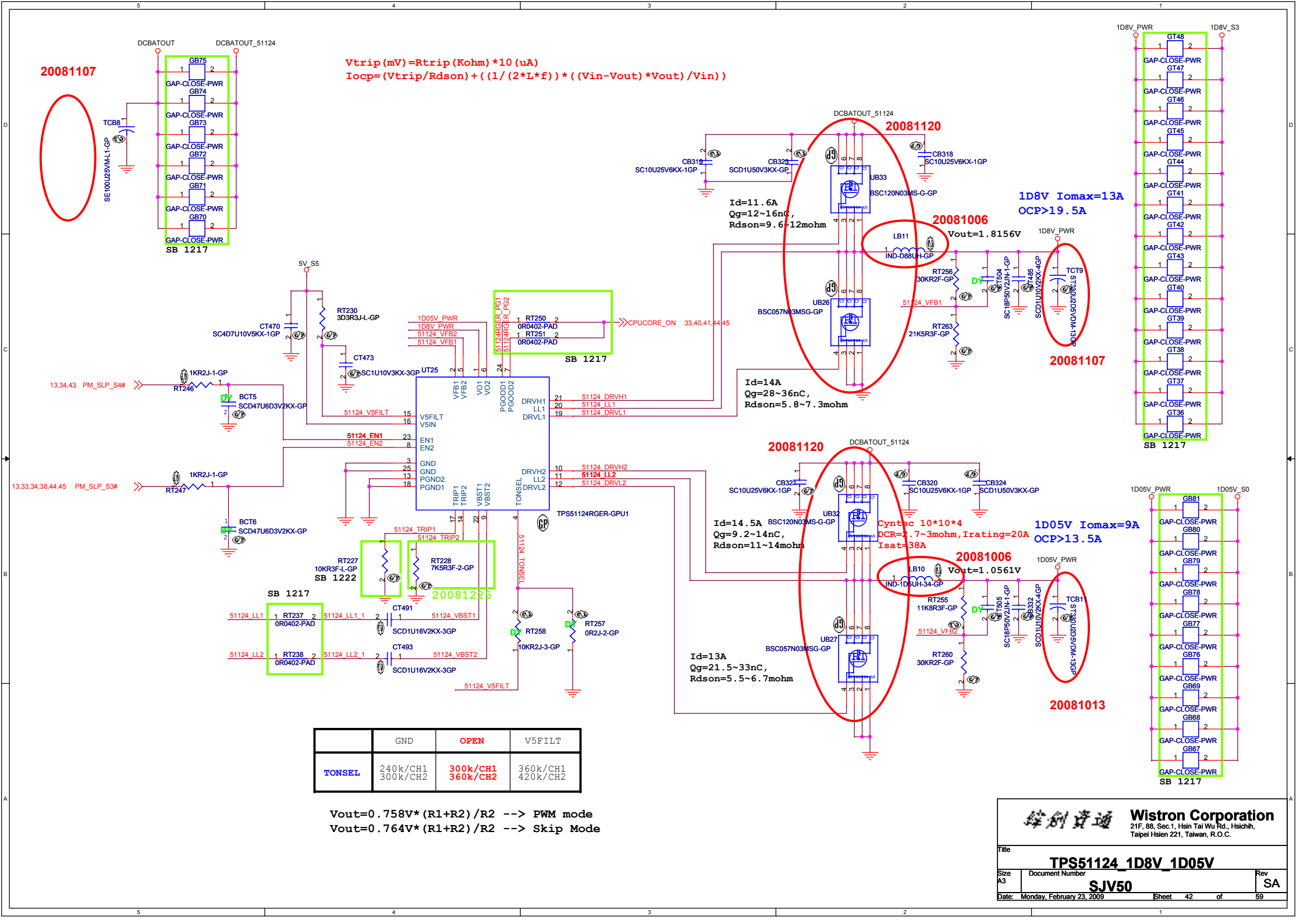

	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

Vout=0.758V*(R1+R2)/R2 --> PWM mode
Vout=0.764V*(R1+R2)/R2 --> Skip Mode

Wistron Corporation
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Title: TPS51124_1D8V_1D05V

Size: A3 | Document Number: SJV50 | Rev: SA

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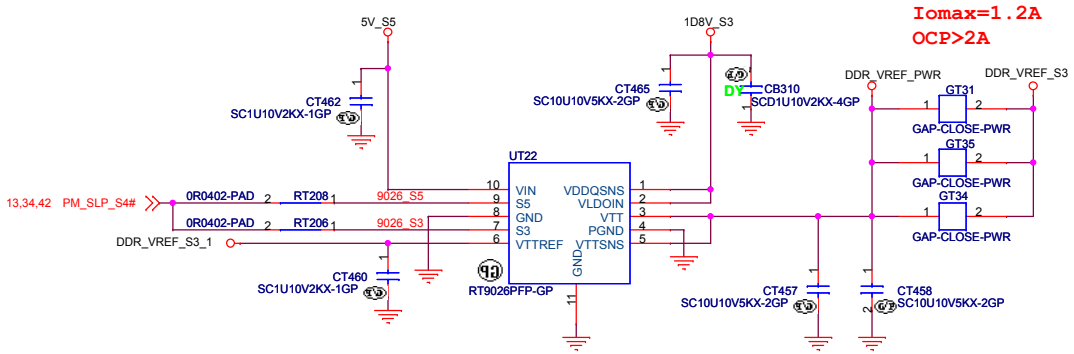

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *0D9V*

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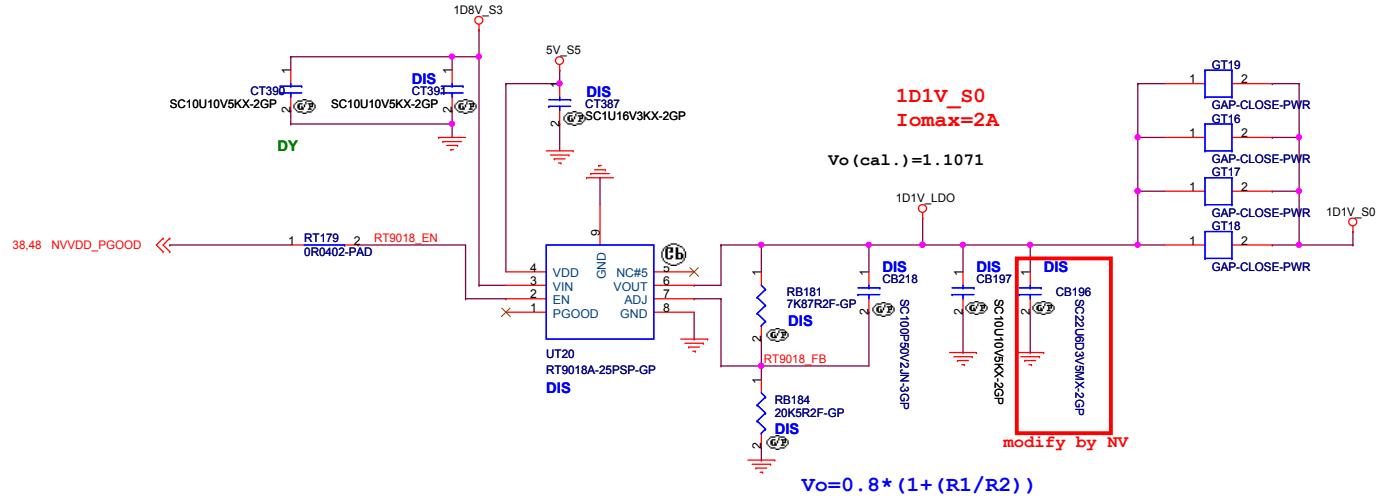

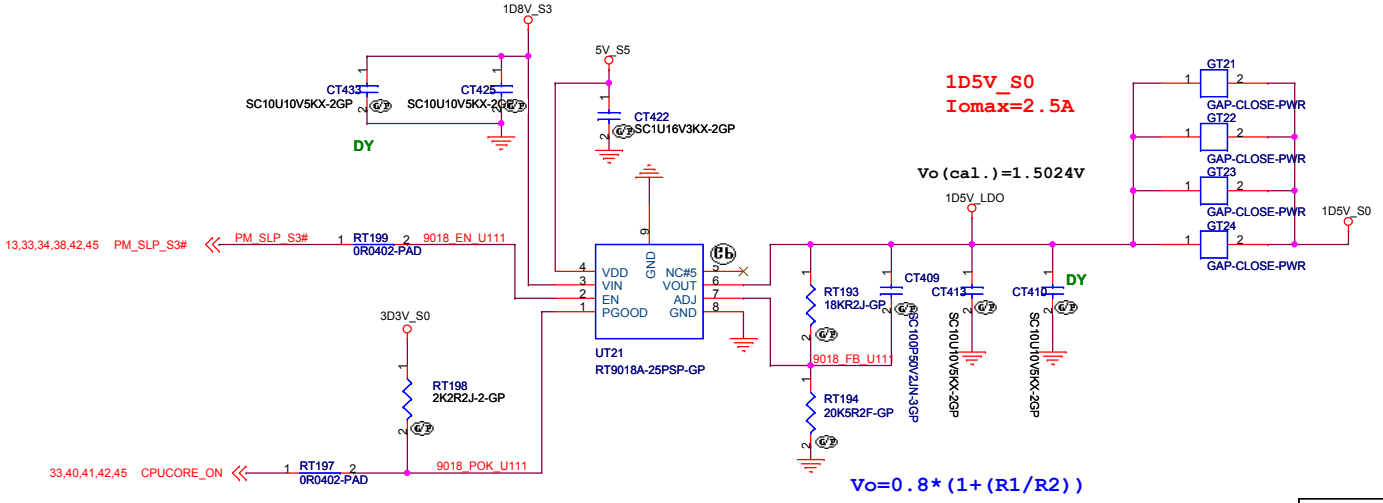

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 1D1V & 1D5V

Size	Document Number	Rev
A3	SJV50	SA

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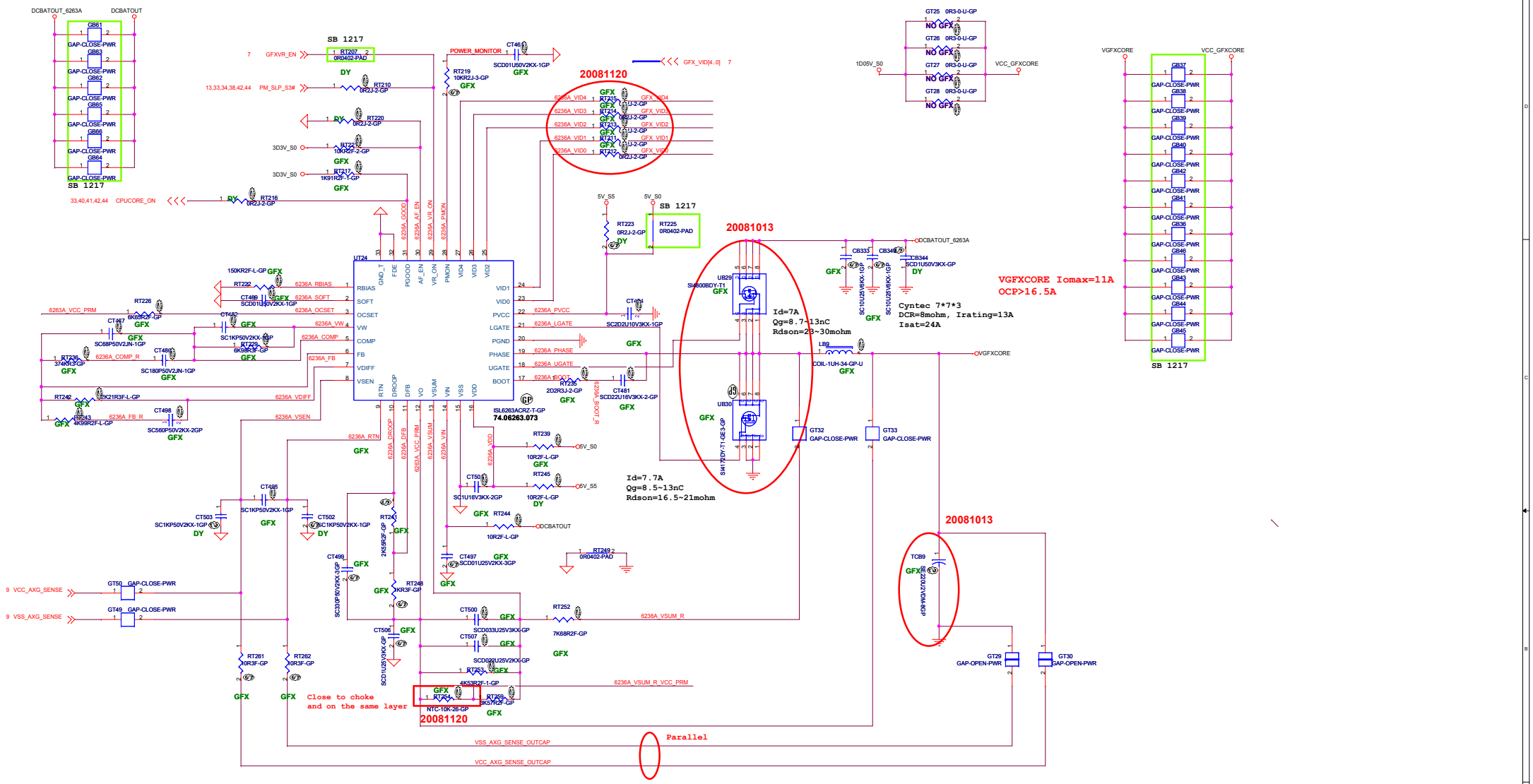

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	ISL6263A_NVDD
Size	A2
Document Number	SJV50
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Date:	Tuesday, February 24, 2009
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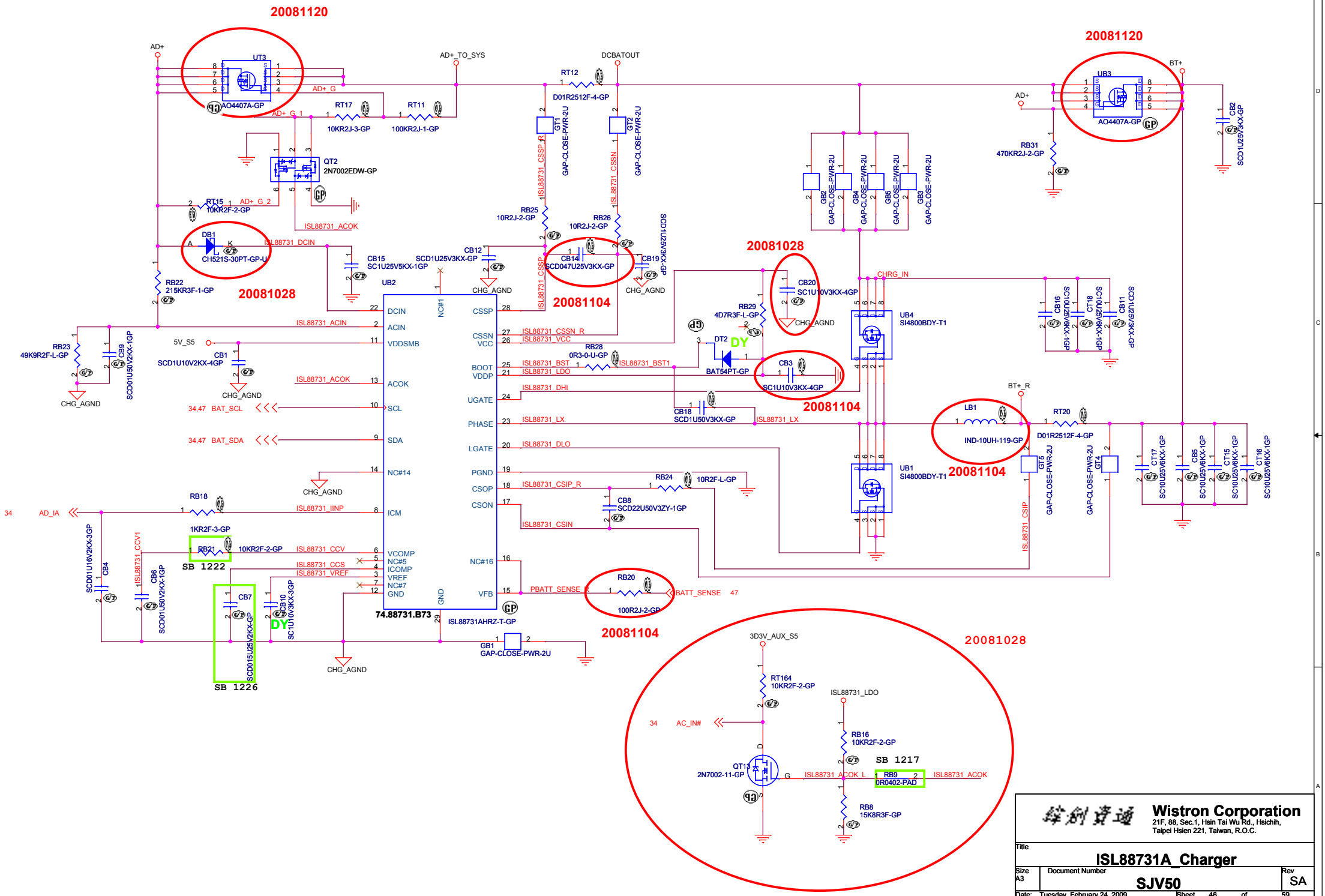
20081120
20081028
20081104
AD+
AD+_TO_SYS
DCBATOUT
BT+
UT3
AO4407A-GP
UB3
AO4407A-GP
AD+_G
AD+_G_1
AD+_G_2
RT17
10KR2J-3-GP
RT11
100KR2J-1-GP
RT12
D01R2512F-4-GP
QT2
2N7002EDW-GP
RT15
10KR2F-2-GP
RB31
470KR2J-2-GP
CB2
SCD1U25V3KX-GP
DB1
CH521S-30PT-GP-U
ISL88731_DCIN
ISL88731_ACOK
RB22
215KR3F-1-GP
CB15
SC1U25V5KX-1GP
CB12
SCD1U25V3KX-GP
RB25
10R2J-2-GP
RB26
10R2J-2-GP
CB14
SCD047U25V3KX-GP
CB19
SCD1U25V3KX-GP
ISL88731_CSSP
ISL88731_CSSN
GT1
GT2
GAP-CLOSE-PWR-2U
GB2
GB4
GB5
GB3
UB2
DCIN
ACIN
VDDSMB
ACOK
SCL
SDA
NC#14
ICM
VCOMP
NC#5
ICOMP
VREF
NC#7
GND
NC#1
CSSP
CSSN
VCC
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC#16
VFB
74.88731.B73
ISL88731AHRZ-T-GP
GB1
GAP-CLOSE-PWR-2U
CHG_AGND
5V_S5
ISL88731_ACIN
ISL88731_CSSN_R
ISL88731_VCC
ISL88731_BST
ISL88731_BST1
ISL88731_LDO
ISL88731_DHI
ISL88731_LX
ISL88731_DLO
ISL88731_CSIP_R
ISL88731_CSIN
ISL88731_IINP
ISL88731_CCV
ISL88731_CCS
ISL88731_VREF
PBATT_SENSE
BATT_SENSE
34,47 BAT_SCL
34,47 BAT_SDA
34 AD_IA
RB23
49K9R2F-L-GP
CB9
SCD01U50V2KX-1GP
CB1
SCD1U10V2KX-4GP
RB18
1KR2F-3-GP
RB21
10KR2F-2-GP
SB 1222
CB4
SCD01U16V2KX-3GP
CB6
SCD01U50V2KX-1GP
CB7
SCD015U25V2KX-GP
CB10
SC1U10V3KX-3GP
DY
RB28
0R3-0-U-GP
RB29
4D7R3F-L-GP
DT2
BAT54PT-GP
CB3
SC1U10V3KX-4GP
CB18
SCD1U50V3KX-GP
CB20
SC1U10V3KX-4GP
RB24
10R2F-L-GP
CB8
SCD22U50V3ZY-1GP
RB20
100R2J-2-GP
UB4
SI4800BDY-T1
UB1
SI4800BDY-T1
CHRG_IN
LB1
IND-10UH-119-GP
BT+_R
RT20
D01R2512F-4-GP
GT5
GT4
CB16
SC10U25V6KX-1GP
CT18
SC10U25V6KX-1GP
CB11
SCD1U25V3KX-GP
CT17
SC10U25V6KX-1GP
CB5
SC10U25V6KX-1GP
CT15
SC10U25V6KX-1GP
CT16
SC10U25V6KX-1GP
3D3V_AUX_S5
RT164
10KR2F-2-GP
34 AC_IN#
QT13
2N7002-11-GP
RB16
10KR2F-2-GP
SB 1217
RB9
0R0402-PAD
ISL88731_ACOK_L
RB8
15K8R3F-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL88731A_Charger
Size
A3
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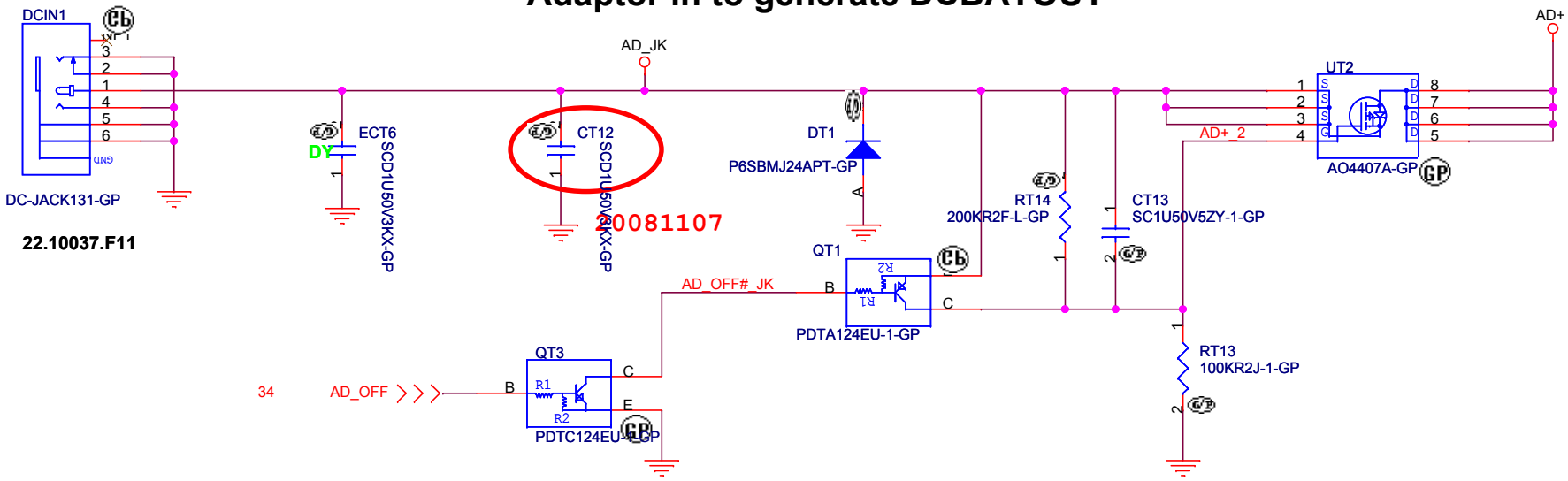
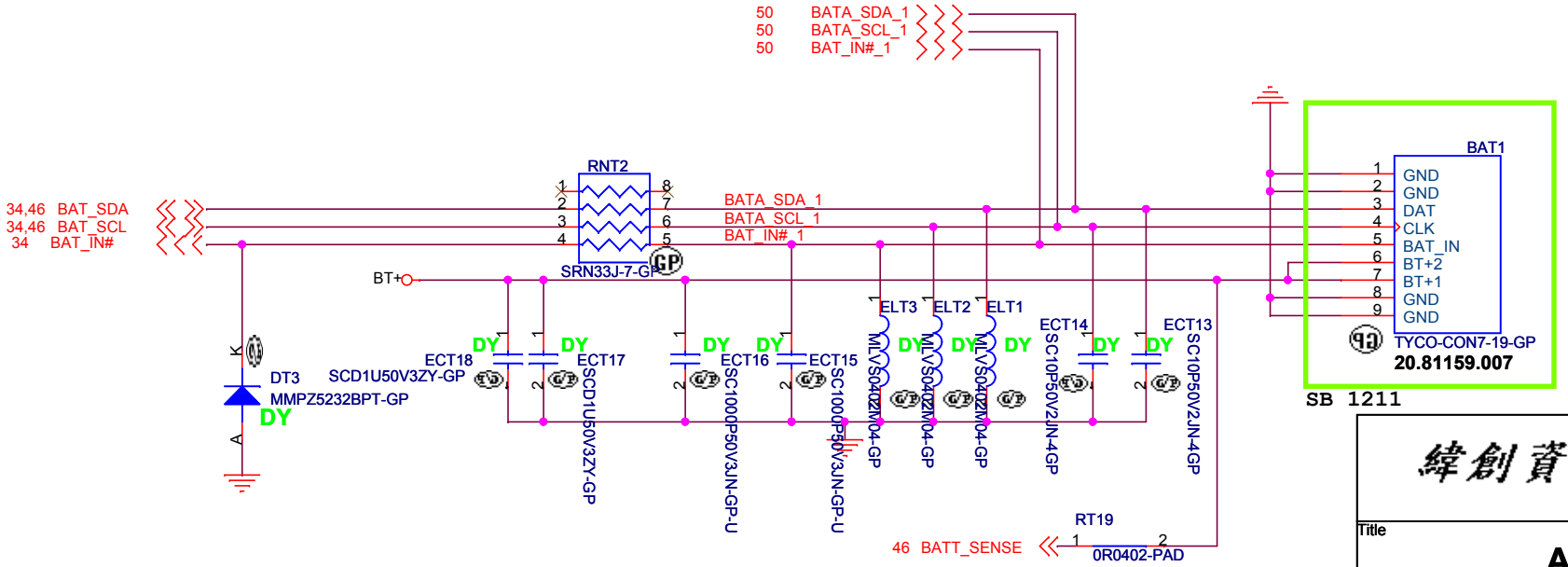
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	AD/BATT CONN	
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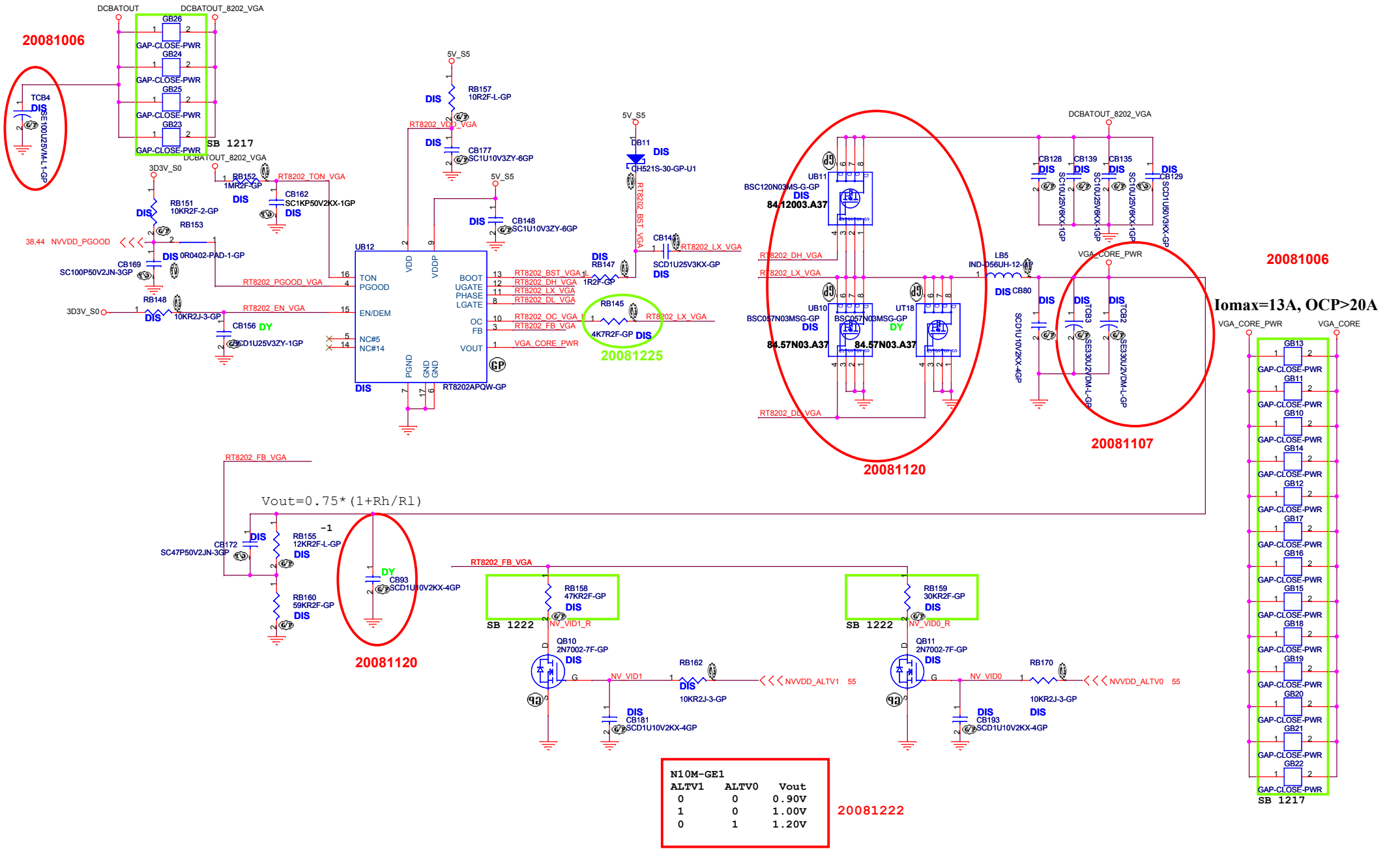

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA CORE

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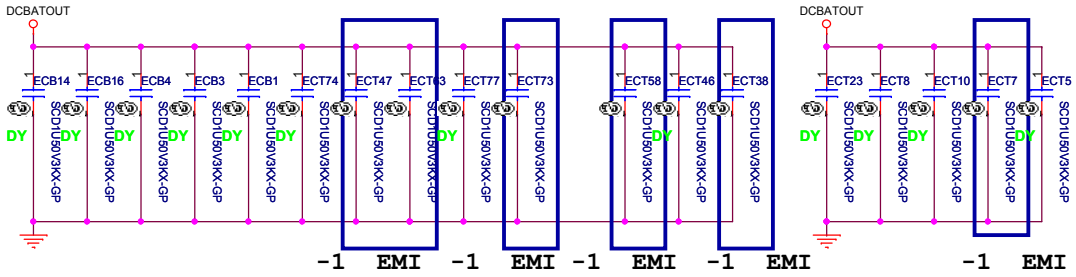

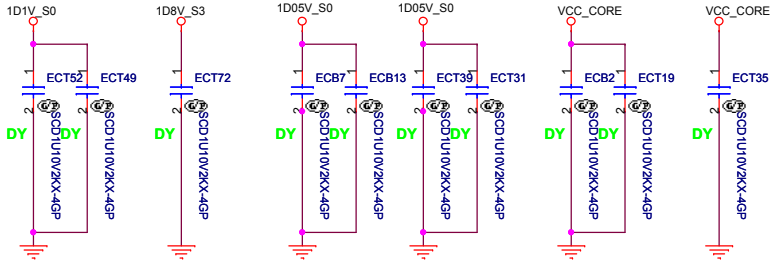

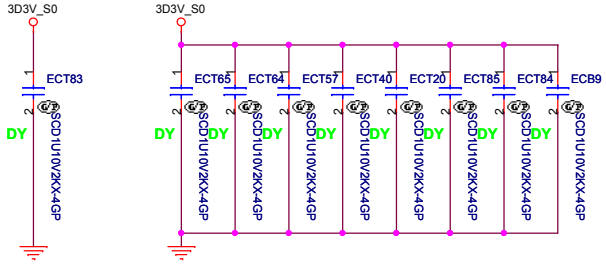

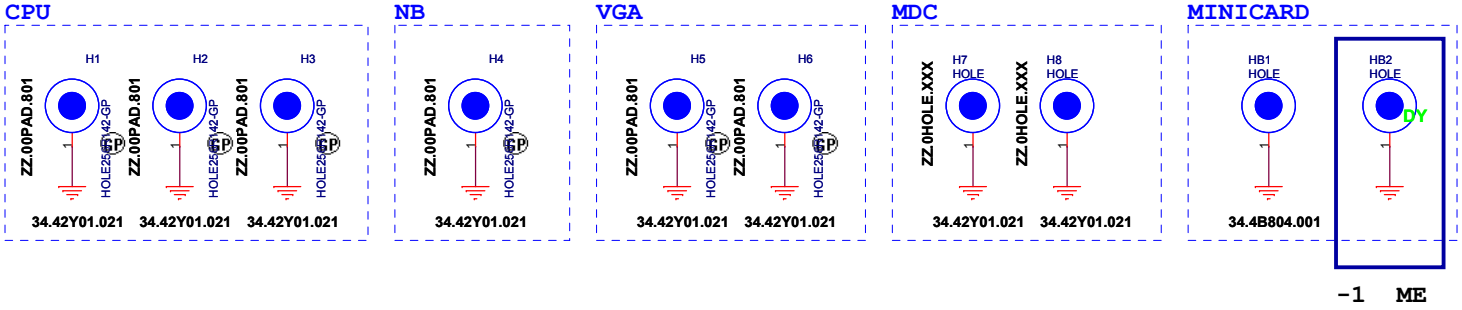

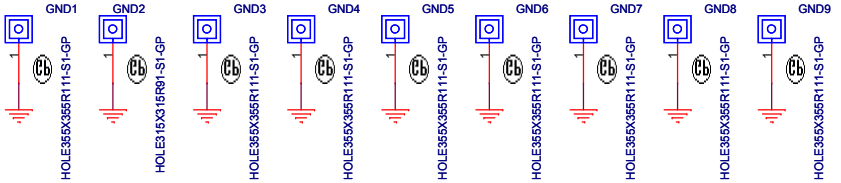

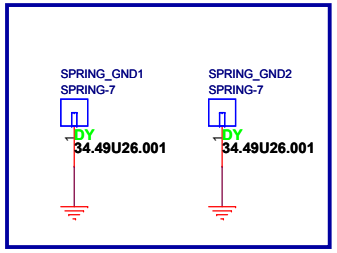

SJV50

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***EMI/Spring/Boss***

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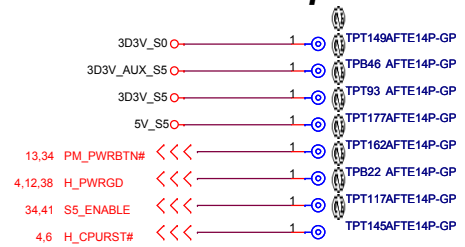
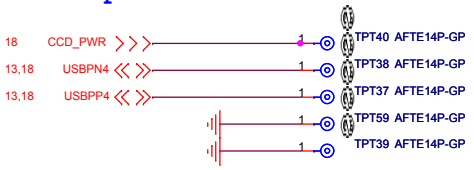
Check test point



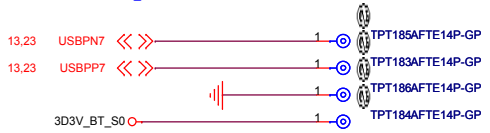
Test Point放在Dimm Door打開可量測處

CCD Conn. Test Point keep on connector side

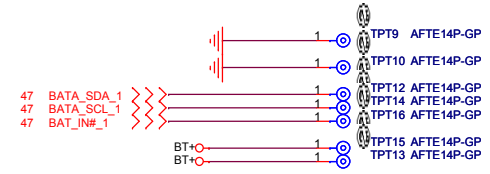


Internal MIC Conn. Test Point keep on connector side

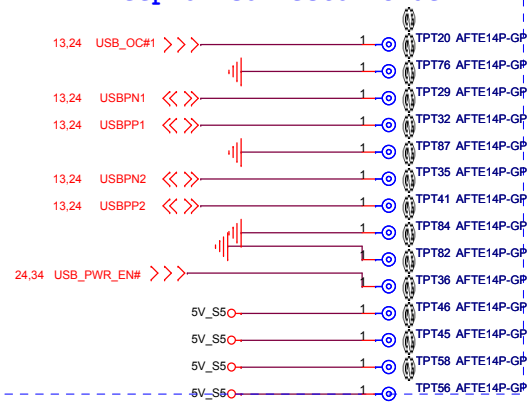
BT Conn. Test Point keep on connector side



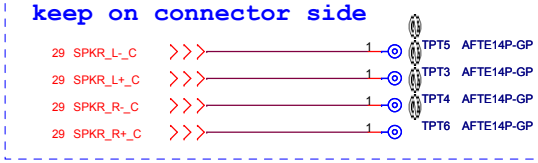
BAT Conn. Test Point keep on connector side



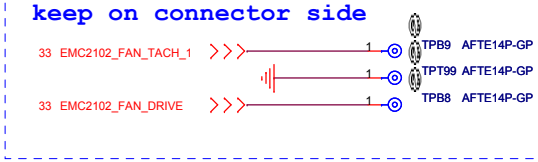
USB_CN1 Conn. Test Point keep on connector side



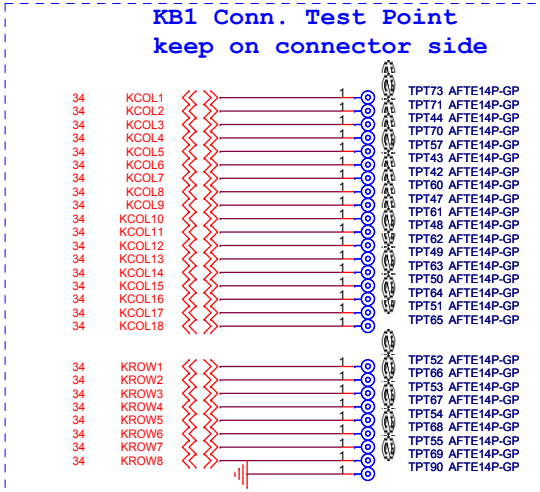
Speaker Conn. Test Point keep on connector side



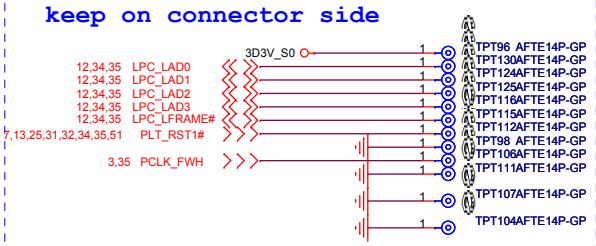
FAN1 Conn. Test Point keep on connector side



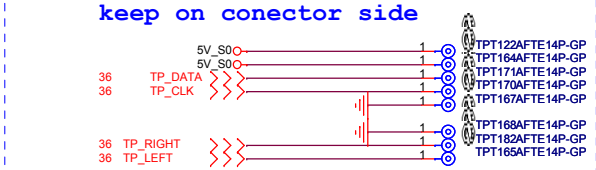
KB1 Conn. Test Point keep on connector side



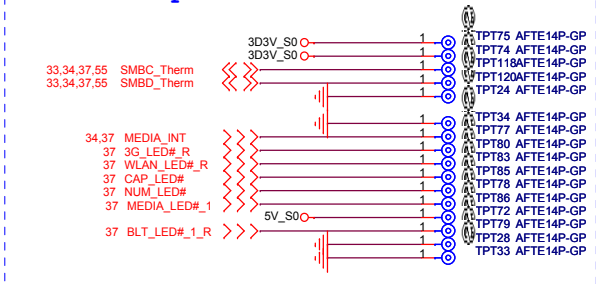
DEBUG BOARD Conn. Test Point keep on connector side



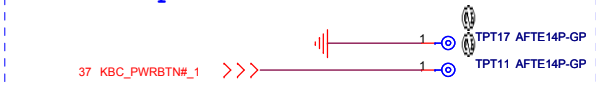
TOUCH PAD Conn. Test Point keep on conector side



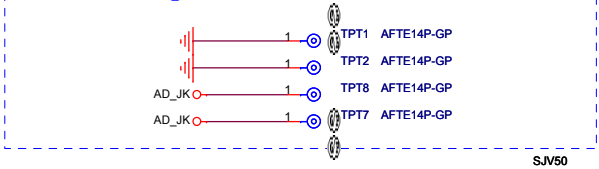
MMB1 Conn. Test Point keep on connector side



Powerbutton Conn. Test Point keep on connector side



DC-IN Conn. Test Point keep on connector side



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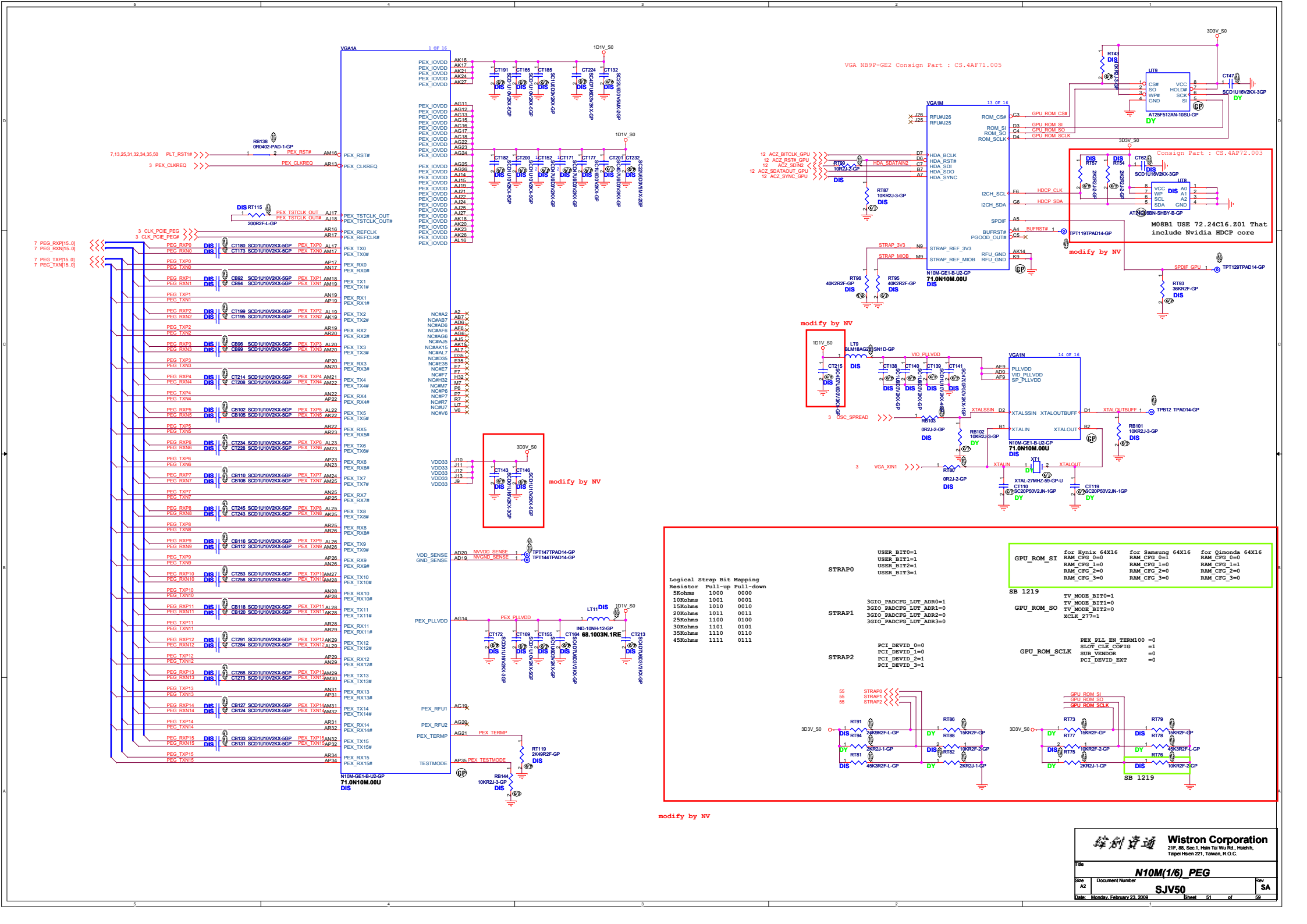
VGA1A
1 OF 16
N10M-GE1-B-U2-GP
71.0N10M.00U
DIS
modify by NV
Logical Strap Bit Mapping
Resistor Pull-up Pull-down
5Kohms 1000 0000
10Kohms 1001 0001
15Kohms 1010 0010
20Kohms 1011 0011
25Kohms 1100 0100
30Kohms 1101 0101
35Kohms 1110 0110
45Kohms 1111 0111
STRAP0
USER_BIT0=1
USER_BIT1=1
USER_BIT2=1
USER_BIT3=1
STRAP1
3GIO_PADCFG_LUT_ADR0=1
3GIO_PADCFG_LUT_ADR1=0
3GIO_PADCFG_LUT_ADR2=0
3GIO_PADCFG_LUT_ADR3=0
STRAP2
PCI_DEVID_0=0
PCI_DEVID_1=0
PCI_DEVID_2=1
PCI_DEVID_3=1
GPU_ROM_SI
for Hynix 64X16
RAM_CFG_0=0
RAM_CFG_1=0
RAM_CFG_2=0
RAM_CFG_3=0
for Samsung 64X16
RAM_CFG_0=1
RAM_CFG_1=0
RAM_CFG_2=0
RAM_CFG_3=0
for Qimonda 64X16
RAM_CFG_0=0
RAM_CFG_1=1
RAM_CFG_2=0
RAM_CFG_3=0
SB 1219
GPU_ROM_SO
TV_MODE_BIT0=0
TV_MODE_BIT1=0
TV_MODE_BIT2=0
XCLK_27?=1
GPU_ROM_SCLK
PEX_PLL_EN_TERM100 =0
SLOT_CLK_CONFIG =1
SUB_VENDOR =0
PCI_DEVID_EXT =0
VGA NB9P-GE2 Consign Part : CS.4AF71.005
Consign Part : CS.4AP72.003
M08B1 USE 72.24C16.Z01 That include Nvidia HDCP core
modify by NV
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Title
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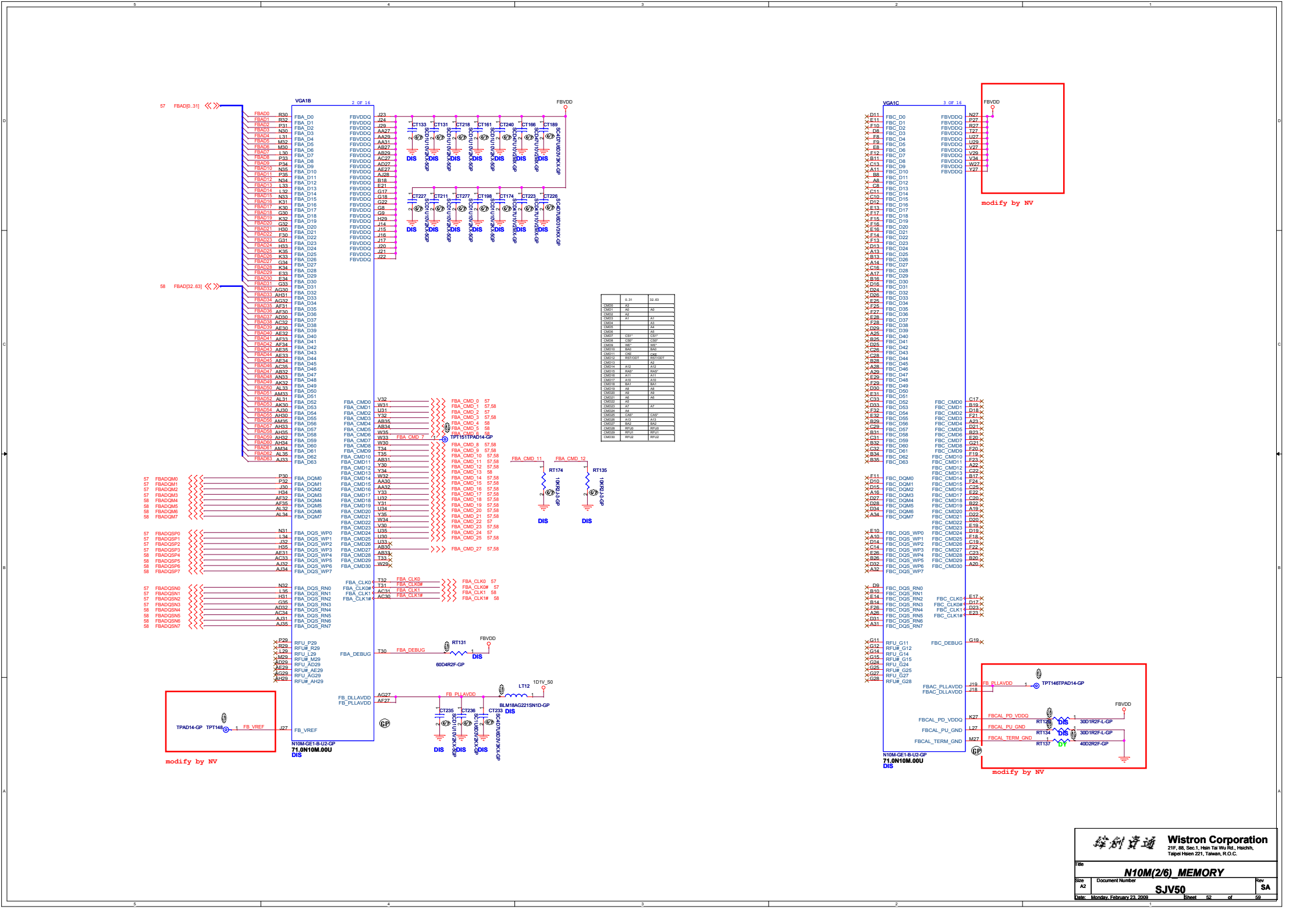

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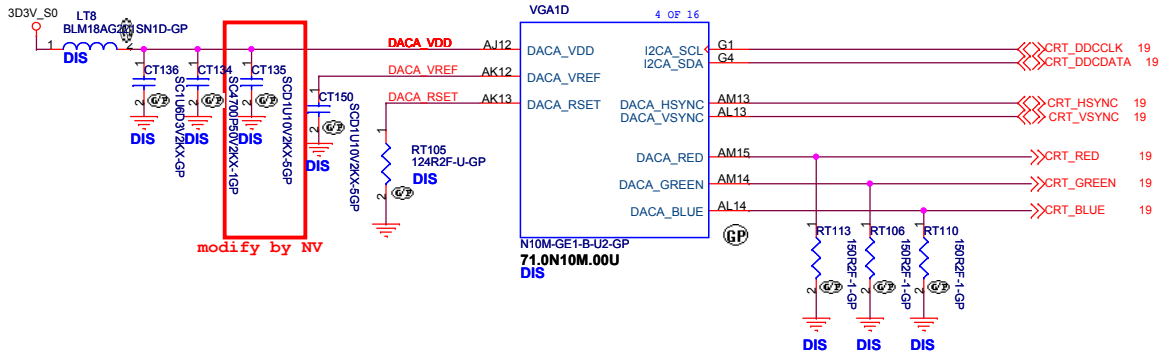

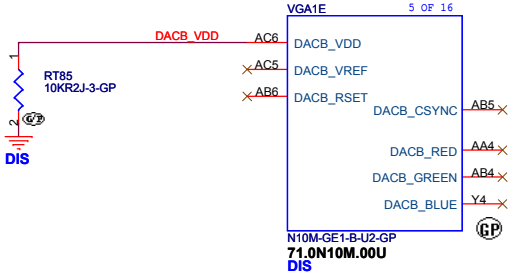

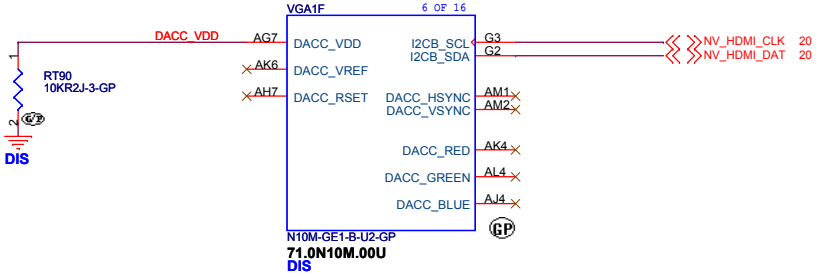

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Title: ***N10M(3/6)_DAC***

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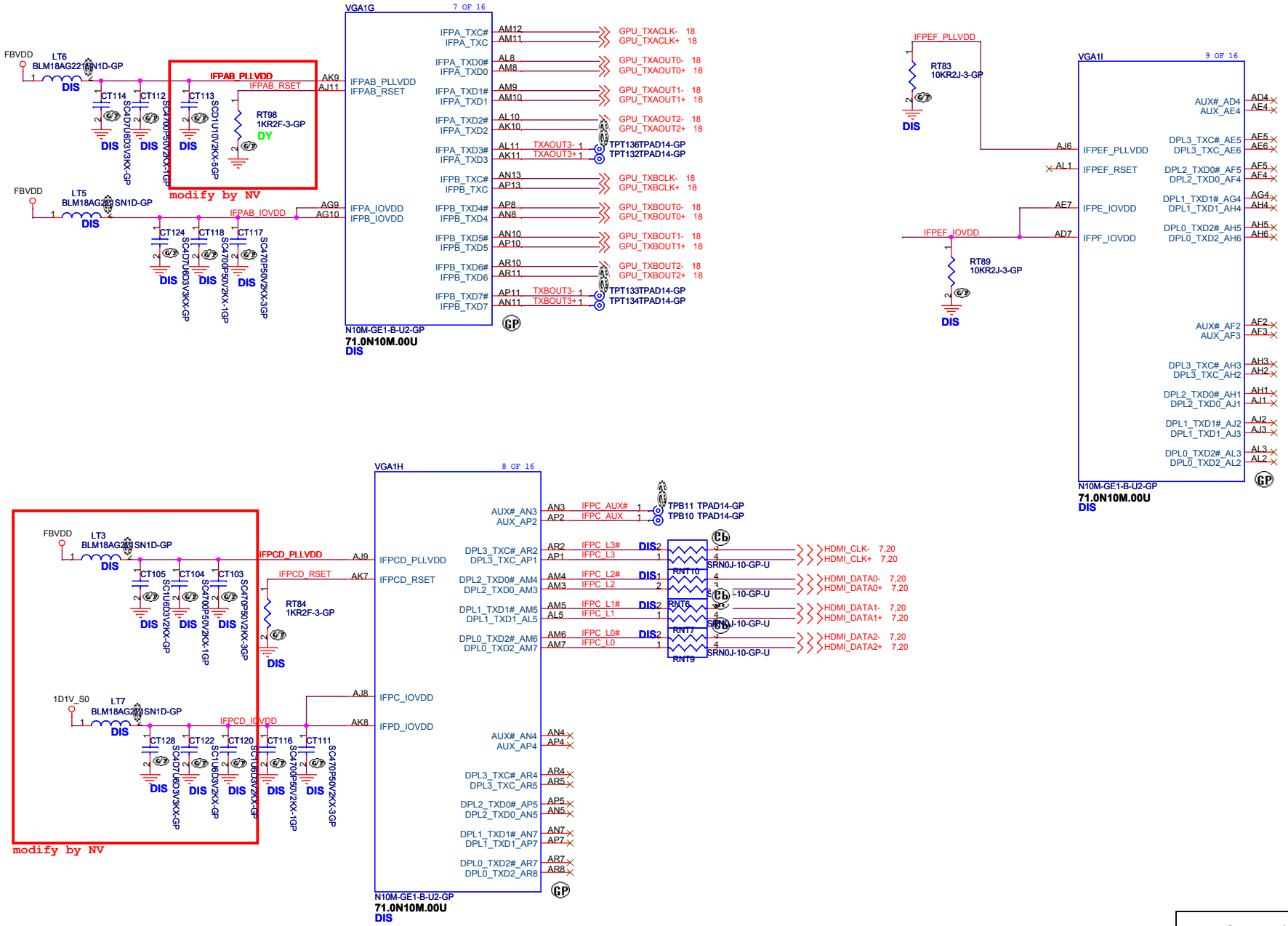

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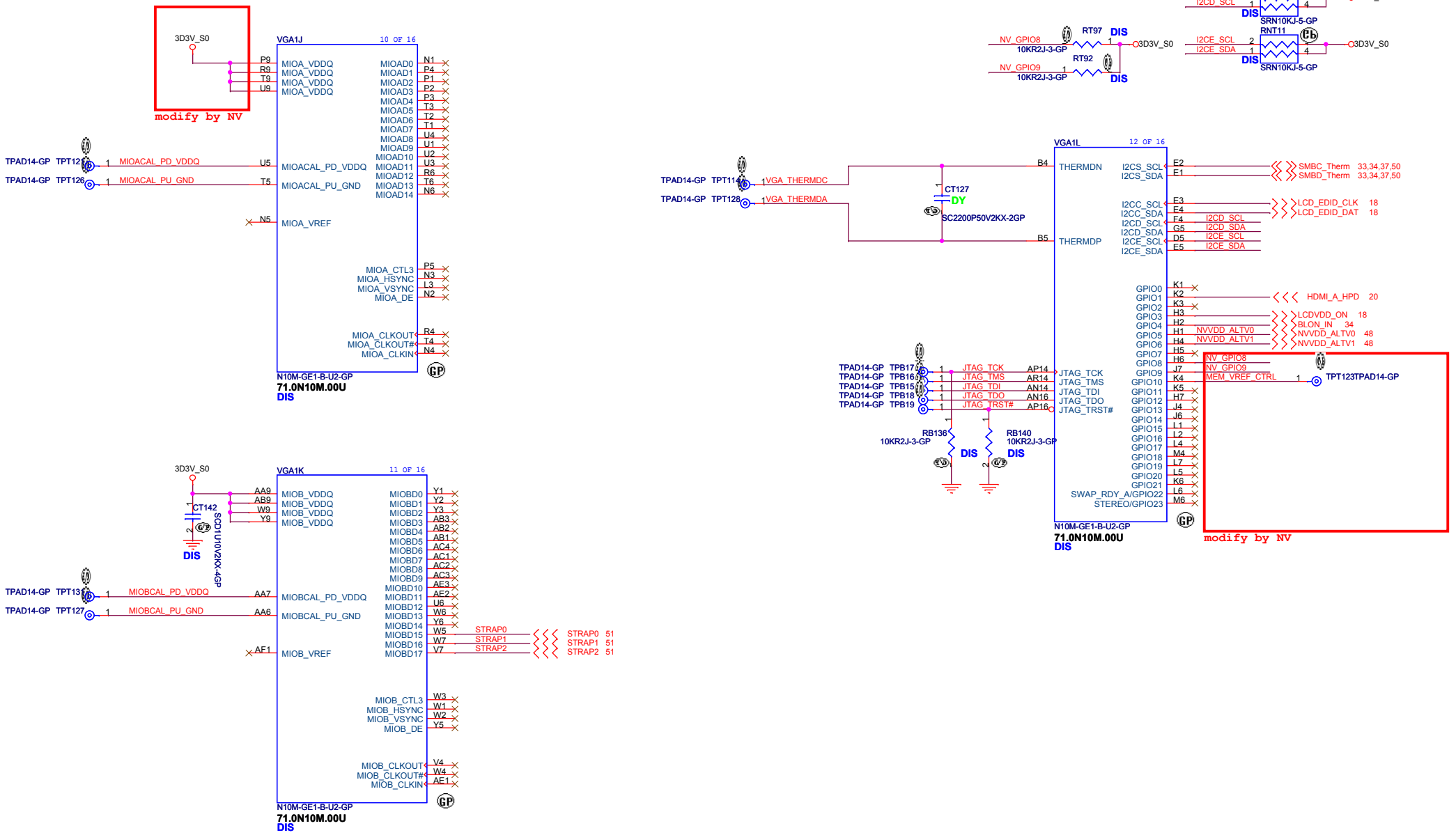

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Title: **N10M(5/6)_MIO/ GPIO**

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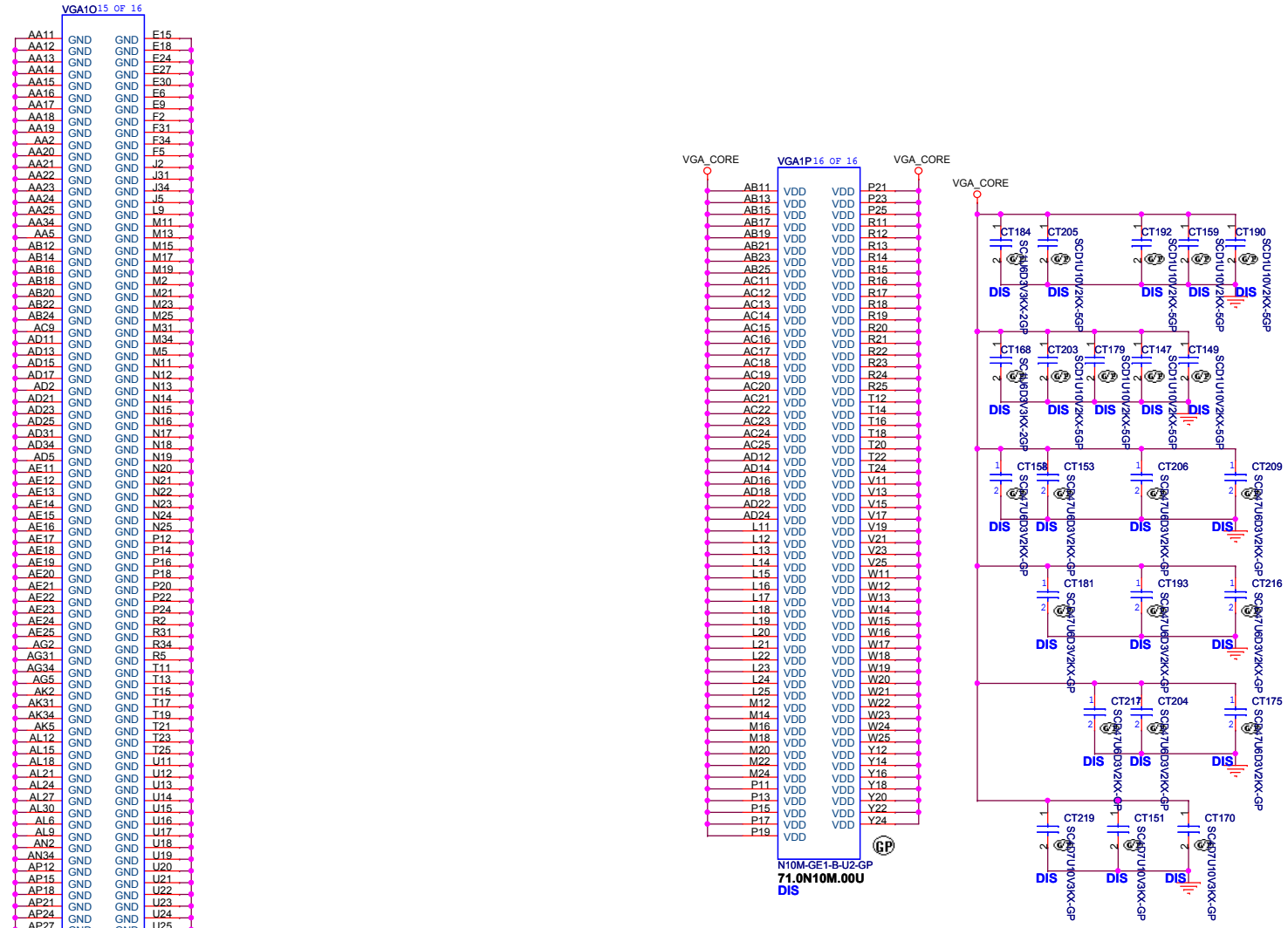

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Title: N10M(6/6)_POWER	
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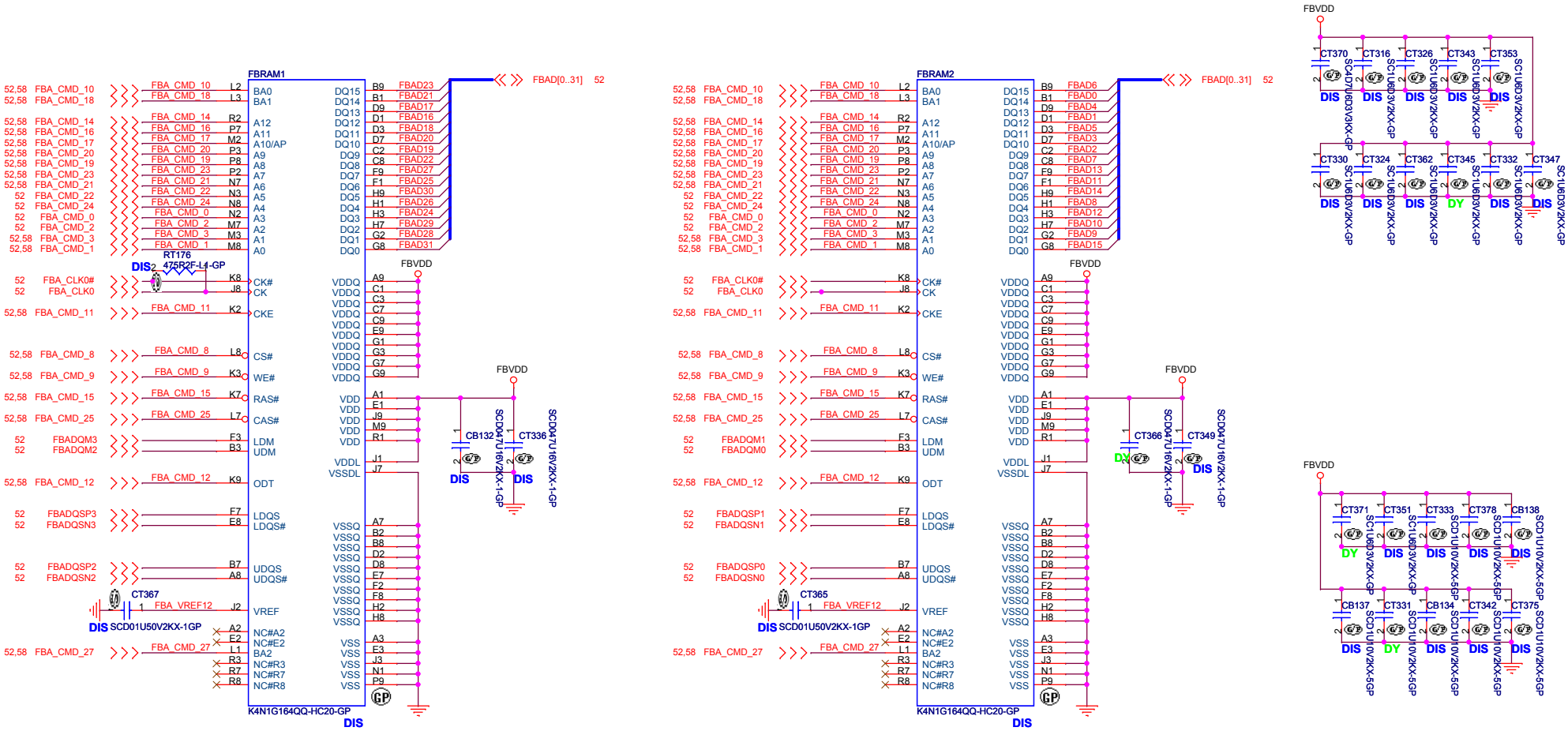

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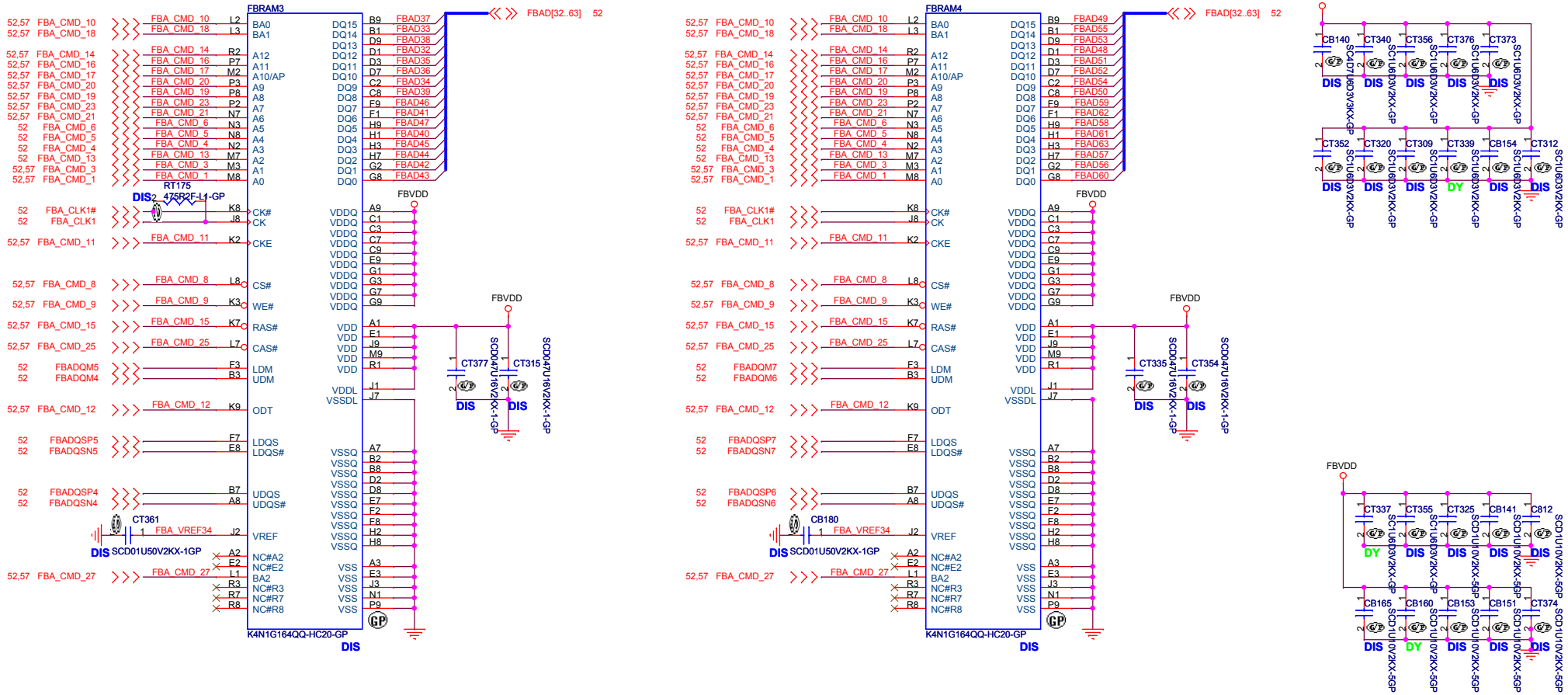

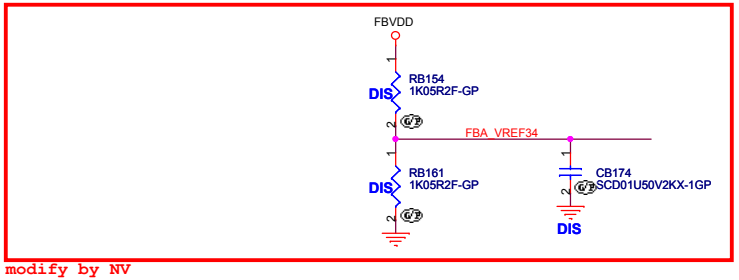

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